國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

射頻互補金氧半 E 類功率放大器設計

RF CMOS Class-E Power Amplifier Design

研 究 生：吳家岱　　Jia-Dai Wu

指導教授：溫瓌岸　博士　　Dr. Kuei-Ann Wen

共同指導：溫文燊　博士　　Dr. Wen-Shen Wuen

中 華 民 國 九 十 六 年 六 月

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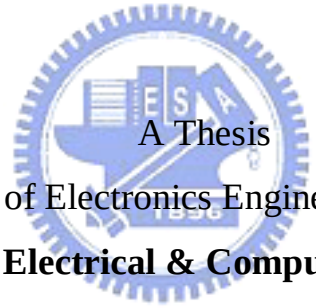

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical & Computer Engineering

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In

Electronic Engineering

中華民國九十六年六月

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摘　　要

本文提出一個完全整合在單一晶片上使用 0.13-μm CMOS 製程的 E 類功率放大器，此 E 類功率放大器結合了 F 類的前級放大器並採用有限的小面積電感來取代大面積的射頻阻隔器以易於整合在單一晶片上。此 E 類放大器在輸入功率為 -3dBm、操作頻率為 2.5GHz 之下，可達到 21dBm 的輸出功率和 48.4%的功率增加效率，在設計的頻帶內，2.3GHz~2.7GHz，功率增加效率仍然可以維持在 44%以上。且為了增加系統模擬的時間，本文提出此 E 類功率放大器的形為模型。藉由此形為模型，系統模擬的時間可以減少 93%左右。

RF CMOS Class-E Power Amplifier Design

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ABSTRACT

An on-chip CMOS Class-E Power Amplifier (PA) implemented in 0.13-μm CMOS technology is presented. The Class-E PA includes a Class-F driver and replaces a large RF choke with a small finite dc-feed inductor for on-chip integration. The proposed Class-E PA achieves power added efficiency (PAE) of 48.4 % while delivering 21 dBm output power with the input driving power of -3 dBm at 2.5 GHz. In the design band, 2.3 GHz ~ 2.7 GHz, PAE is still above 44%. In order to improve the simulation time of RF/Baseband co-simulation the behavior model of proposed PA is presented. The simulation time of RF/Baseband co-simulation can be reduced about 93% by the proposed behavior model.

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吳家岱

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Chapter 1

Introduction

Recently, the IEEE has come up with a new standard, 802.16e, is so-called WiMAX (World Interoperability for Microwave Access). WiMAX provides high data rates and long connection distances for residential and enterprise use. The modulation used to achieve high data rates is Orthogonal Frequency Division Multiplexing (OFDM). The modulated signals will display a high Peak-to-Average Power Ratio (PAPR) and a strict linearity requirement in transmitter. Beside, WiMAX also supports roaming which provides each user a connection with cell phone quality, therefore, a wide output power range is necessary. Figure 1.1 shows the WiMAX frequency band descriptions from 2 GHz to 6 GHz.

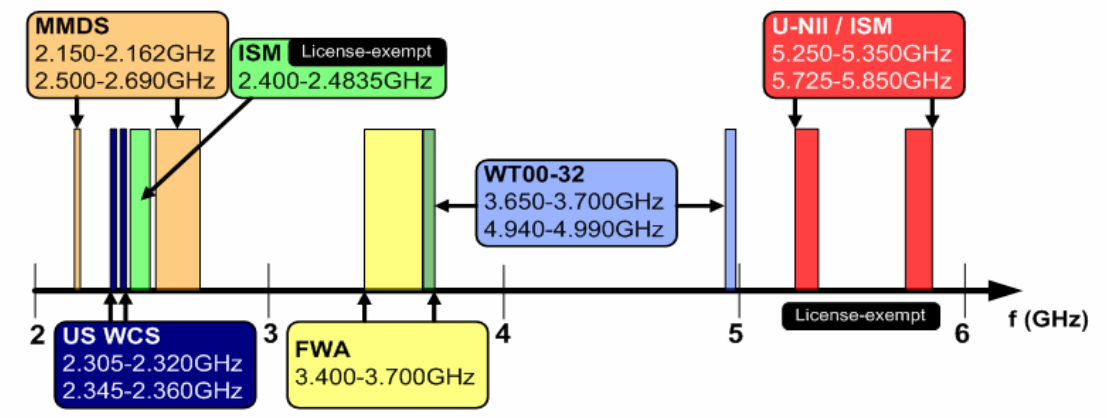


Figure 1.1 WiMAX frequency band descriptions from 2 GHz to 6 GHz.

1.1 Motivation

As the growth of wireless communication networks, there is constantly increasing demand for compact, low-cost and low-power portable devices. This motivates the investigation of single-chip transceivers realized in low-cost CMOS technology. A major difficulty to achieve the fully-integrated transceiver design is the complete integration of PA. The inability to provide on-chip solutions for RF PAs arises primarily from two factors: substrate loss of the on-chip passive components (mainly inductors) and the low breakdown voltage of the active devices. The power consumption of PA is the dominant part of total transmitter power consumption, making the PA efficiency crucial. The design of CMOS PA is still a challenging issue, such as high efficiency, high output power and fully-integrated PA in a single chip. However, the high efficiency linear PA is difficult to implement in a single chip. But the WiMAX linearity requirement is severely. Therefore, the on-chip Class-E PA with polar transmitter can achieve high efficiency and high linearity at the same time. In order to improve the RF/Baseband co-simulation speed the behavior model of the Class-E PA is necessary. Finally, on-chip PA design becomes more and more important with System-On-Chip (SoC) growing rapidly. Therefore, an investigation of on-chip PA is very interesting.

1.2 Basic Concepts of Class-E PA

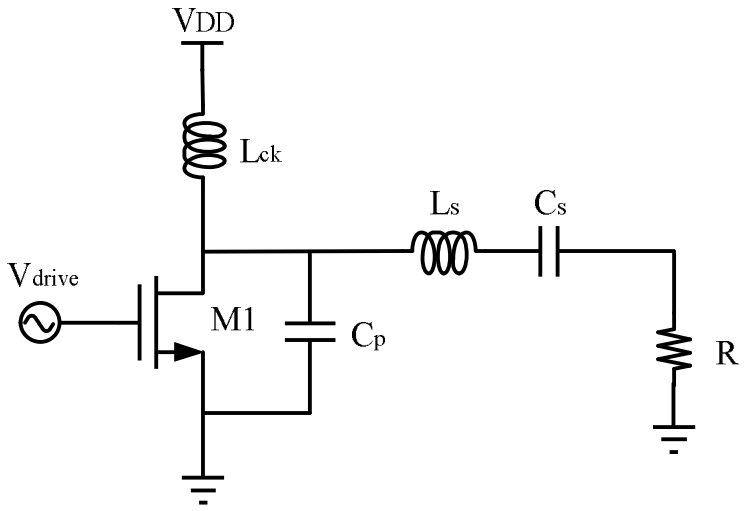


Figure 1.2 Class-E power amplifier.

Figure 1.2 shows the circuit schematic of the Class-E power amplifier [1] [2]. The dc current flowing through the RF choke (L_{ck}) is modulated by the power device (M_1), operating as a switch driven by the input signal at the operating frequency. The ideal Class-E PA has two conditions [3]. First, the drain voltage is zero at the switching instants. Second, the first derivative of the drain voltage is zero when the active device turns on. The first condition prevents dissipation of the energy stored by the shunt capacitor at turn on, while the second makes the circuit less sensitive to component, frequency and switching instants variations. The ideal efficiency is 100 percent. The RF choke provides a dc path to the supply and approximates an open circuit at RF. C_s and part of L_s form a series resonator tuned at fundamental frequency.

A fraction of L_s is needed together with the capacitor shunting the active device, C_p, to meet the Class-E PA conditions. Figure 1.3 shows V_D and I_D waveform of the Class-E PA. It shows that the peak drain voltage is approximately $3.6V_{DD}$, while the peak drain current is roughly $1.7V_{DD}/R_L$.

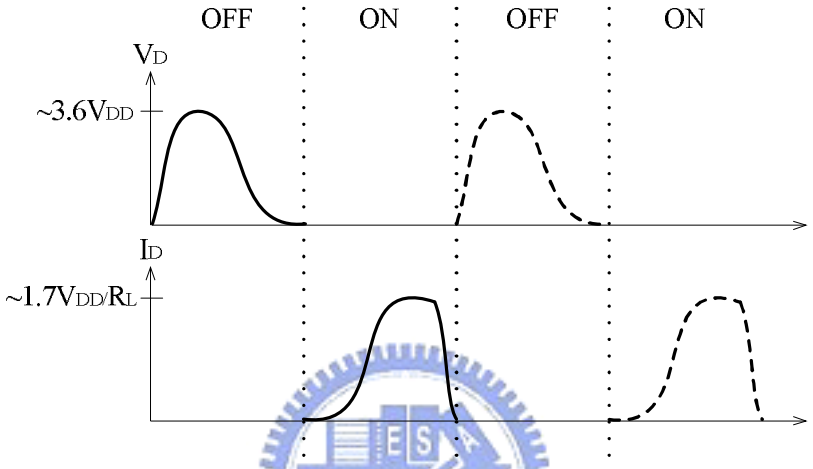
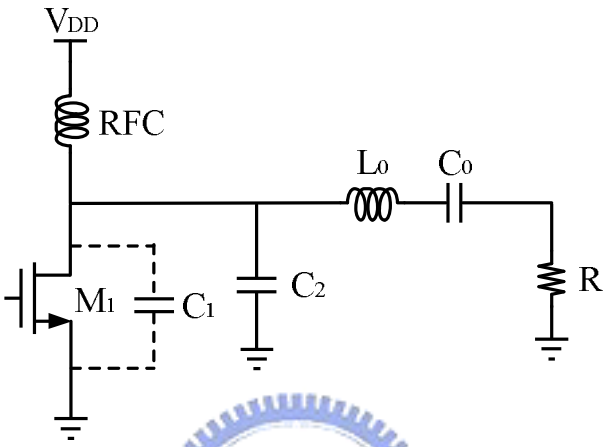


Figure 1.3 Drain voltage and current waveforms for Class-E power amplifier.

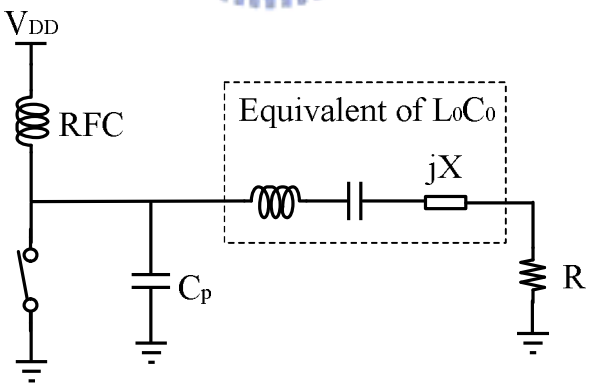
1.2.1 Ideal Class-E Power Amplifier

The brief concepts of the Class-E PA have discussed above. The more detail considerations of the Class-E PA will discuss in the subsequent sections. The Class-E PA had been first published in 1975s [4]. And the idealized operation of the Class-E tuned power amplifier was published in 1977s [5]. Figure 1.4 (a) and Figure 1.4 (b) shows the basic circuit and equivalent circuit of the Class-E power amplifier [5]. The Class-E PA includes a transistor operating as a switch, M_1, a shunt capacitor, C_2, an

RF choke, RFC, a series-tuned output circuit, L_0C_0, and the load resistor, R. C_1 is the parasitic capacitance in parallel at the switch including intrinsic transistor output capacitance and circuit stray capacitance.



1.4 (a)



1.4 (b)

Figure 1.4 (a) Basic circuit of the Class-E PA. (b) Equivalent circuit of the Class-E PA.

A simple equivalent circuit of the Class-E power amplifier is based on the following five assumptions [5].

- The RF choke only allows a dc current and has no series resistance.
- The quality factor of the series-tuned output circuit is high enough to make the output current is mainly a sinusoid at the operating frequency.
- The switching action of the active device is instantaneous and lossless. The transistor has zero saturation voltage, zero saturation resistance, and infinite off resistance.
- The total shunt capacitance is independent of the drain voltage.
- The transistor can pass negative current and withstand negative voltage. (This is inherent in MOS devices, but requires a combination of bipolar transistors and diodes.)

The series reactance jX is produced by the difference in the reactance of the inductor and capacitor of the series-tuned circuit. Note that the jX reactance applies only to the fundamental frequency, and it is assumed to be infinite at harmonic frequencies. The nominal component values for the idealized Class-E power amplifier are given by the following equations [5]:

$$R = 0.577 \frac{V_{dd}^2}{P_{out}} \tag{1.1}$$

$$B(= wC_P) = 0.183 \frac{1}{R} \tag{1.2}$$

$$X(= wL) = 1.152R \tag{1.3}$$

1.2.2 Practical Considerations

The analysis presented in section 1.2.1 is based on several simple assumptions which are not always acceptable for practical and on-chip design. For examples [6]:

- Non-ideal LC passive components

  The loss of the on-chip passive components (mainly inductors) in CMOS technology is larger than the off-chip passive components.

- Large RF choke

  It is hard to implement large RF choke in a single chip for on-chip design.

- Nonzero transition time

  Real transistors have nonzero transition times and, especially at high frequencies, it may cause a lot of loss.

- Effect of circuit variations

Variations in component values, operating frequency, and duty cycle can have an effect on the performance of the Class-E PA [7].

- Nonzero ON resistance or nonzero saturation voltage
- Finite loaded Q

The output current is not a pure sine wave, because the series-tuned output circuit has a finite loaded Q.

1.2.3 Finite DC-Feed Inductor

The Class-E PA has required a RF choke between the dc power supply and the active device in the previous description. But the RF choke itself is large in size, so it presents problems in terms of both large resistance loss and hard to implement in a single chip. Therefore, a smaller inductor is necessary for designing on-chip Class-E PA. However, using a finite dc-feed inductor instead of an RF choke in the Class-E PA has a number of benefits in the following [8].

- A small DC-feed inductor has lower loss due to a smaller series resistance.
- The cost and the chip size will decrease to make it implemented in a single chip easier.
- The load resistance will also increase, thus making the design of the matching network easier.

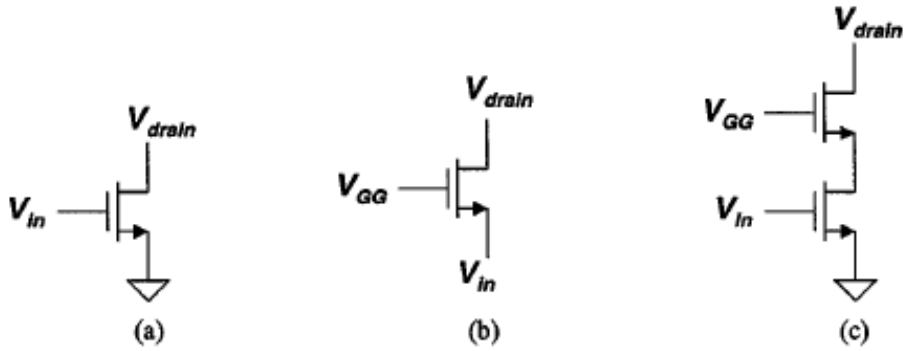
Therefore, there is a strong interest to pursue the design of the Class-E PA with finite dc-feed inductor.

1.2.4 Cascode Topology

In order to overcome the low breakdown voltage of the active devices the cascode topology can be used in designing an on-chip Class-E PA. With the finite DC-feed inductor, the load resistance can be increased for the same output power and supply voltage to achieve higher efficiency. From (1.1), for further increase of the load resistance (R), it is agreeable to allow higher supply voltage (V_{dd}) because the load resistance is proportional to the square of the supply voltage. As the technology scale down, however, the safe operating voltage will decrease and the supply voltage should be reduced in order not to stress the active devices. The voltage stress on the active device can be reduced by the cascode topology, so the load resistance could be increased by the supply voltage increasing [9].

Usually, the active device is switched from the gate as shown in Figure 1.5 (a), but the maximum voltage stress in the transistor is $V_{drain,max}$ which can be as high as 3.6 V_{dd} for an ideal Class-E PA, resulting in low supply voltage and small load resistance. On the contrary, if the active device is switched form the source instead of the gate as shown in Figure 1.5 (b), the maximum voltage stress is reduced to $V_{drain,max} - V_{GG}$

because the source of the switching transistor swings up with the input voltage. Therefore, the maximum allowable supply voltage is $V_{drain,max}$ /($V_{drain,max}$ –V_{GG}) times larger for common-gate switch than that for a simple common-source switch. In order to avoid presenting the input driving stage with a low impedance node, a common-source stage is combined with the common-gate switch into a cascode as shown in Figure 1.5 (c). This allows the supply voltage almost twice the value for a single common-source switch.



(a) (b) (c)

		(a)	(b)	(c)
ON	$V_{GS,max}$	V_{GG}	V_{GG}	V_{GG}
	$V_{DS,max}$	0	0	0
OFF	$V_{GS,max}$	0	0	$V_{GG} - V_T$
	$V_{DS,max}$	$V_{drain,max}$	$V_{drain,max} - V_{GG}$	$V_{drain,max} - V_{GG} + V_T$

(d)

Figure 1.5 (a) Common-source. (b) Common-gate switch. (c) Common-gate switch combined with common-source stage into a cascode in order not to provide low-impedance load to the driving. (d) Maximum voltage stress is shown for each case assuming the input signal Vin swings from 0 V to V_{GG} [9].

1.3 Class-F Power Amplifier

A suitable driver stage for lowering the input driver power in system level is very important. The Class-F PA is switched-mode PA with high efficiency, and it can shape the input waveform of the Class-E PA. Therefore, the Class-F PA is suitable for Class-E driver stage. The Class-F PA is shown in Figure 1.6 [6] [7]. The output tank is tuned to resonance at the operating frequency and is assumed to have a high enough Q to act as a short circuit at all frequencies outside of the desired bandwidth. The length of the transmission line is chosen to be precisely a quarter-wavelength at the operating frequency. At the operating frequency, the drain sees a pure resistance of $R_L=Z_o$, since the tank is an open circuit there, and the transmission line is therefore terminated in its characteristic impedance. At the second harmonic of the operating frequency, the drain sees a short, because the tank is a short at all frequencies away from the operating frequency(and its modulation sidebands), so the transmission line now appears as a half-wavelength piece of line. Clearly, the drain sees a short at all even harmonics of the operating frequency, because the tank still appears as a short circuit; the transmission line appears as an odd multiple of a quarter-wavelength and therefore provides a net reciprocation of the load impedance. Drain voltage and current of the ideal Class-F PA shows in Figure 1.7.

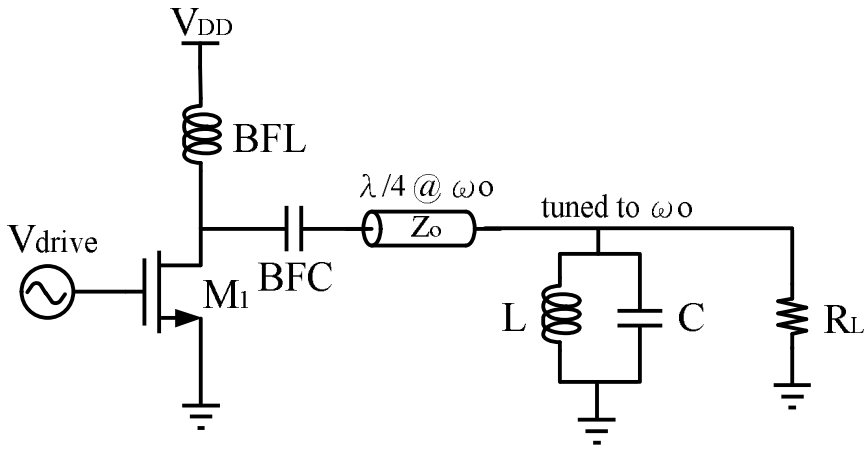


Figure 1.6 Class-F power amplifier.

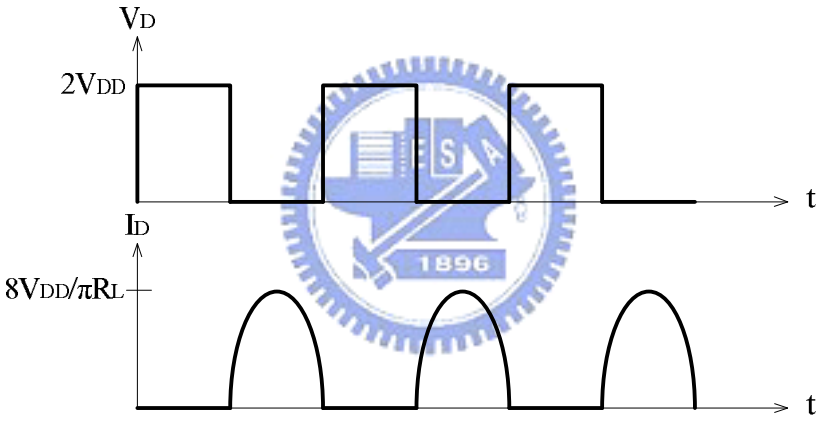


Figure 1.7 Drain voltage and current waveforms for Class-F power amplifier.

1.4 Polar Transmitter

The polar transmitter with Class-E PA can be used for WiMAX of severe linearity requirement. One of the first applications of polar technique is Envelope Elimination and Restoration (EER), as shown in Figure 1.8 [10] [11] [12] [13]. The EER means

that the envelope of the RF input is eliminated by a limiter to generate constant envelope phase signal, and the magnitude information is extracted by an envelope detector. The envelope and phase signal are amplified separately and

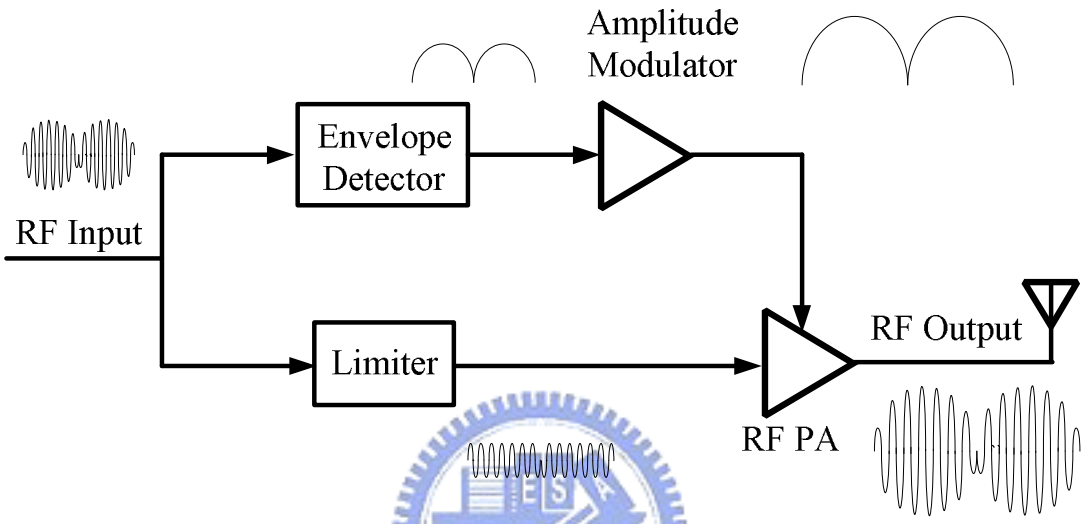


Figure 1.8 EER architecture.

then recombined to restore the magnitude and phase information using a switched mode RF PA. Therefore, the envelope and phase signal can be recombined if the envelope of the RF output of a switched-mode RF PA is proportional to its supply voltage. And using a switched-mode PA is more efficient than using a linear PA. That is, the EER architecture can linearize the switched-mode RF PA without compromising efficiency. But the EER system still has some disadvantages. First, it has delay mismatch between the envelope and phase paths because the two paths employ different type of circuits and operating at different frequencies. It must be

maintain below as an acceptable level. Second, limiters incorporating active stages such as differential pairs exhibit a substantial AM-to-PM conversion effect at high frequencies. Third, envelope detector also introduces AM-to-AM conversion effect. Using the polar transmitter could solve second and third disadvantages of EER system. But the first disadvantage of EER is also the challenge of polar transmitter.

The polar transmitter, as shown in Figure 1.9 [10] [14], includes baseband DSP, DAC, amplitude modulator, phase modulator and switched mode RF power amplifier. The amplitude modulator includes a Sigma-Delta Modulator (SDM) or a Pulse Width Modulator (PWM) and a Class-S Modulator. The phase modulator includes a synthesizer or a Voltage Control Oscillator (VCO). And the switched-mode RF PA is Class-E power amplifier. The I/Q signals are split into the envelope signal and constant envelope phase signal. The constant envelope phase signal (RF) is applied at the gate of the transistor of the Class-E PA, and the envelope signal (low-frequency) directly modulates the supply of the Class-E PA. A high efficiency linear RF PA can be achieved by combining two paths. Finally, we can use the polar transmitter with Class-E PA to achieve high linearity and high efficiency at the same time. The polar transmitter does not use the envelope detector and a limiter, so it could solve the second and third disadvantages of EER system. But the first disadvantage of EER, timing synchronous between the envelope path and phase path, is still the challenge of

polar transmitter. And the second challenge of the polar transmitter is the wider bandwidth of the envelope signal and phase signal. Because of the wider bandwidth of envelope and phase signal, it has to increase the bandwidth of the two paths to introduce noise largely. It has trade-off between the signal bandwidth and noise. And the synchronization between the envelope signal and the constant envelope phase signal is very difficult. On the contrary, the traditional transmitters use the in-phase and quadrature-phase components so the synchronization is easier. That is why the traditional transmitters used more frequently than the polar transmitter. Finally, the behavior model can be used for saving the RF/Baseband co-simulation time. This will discuss later.

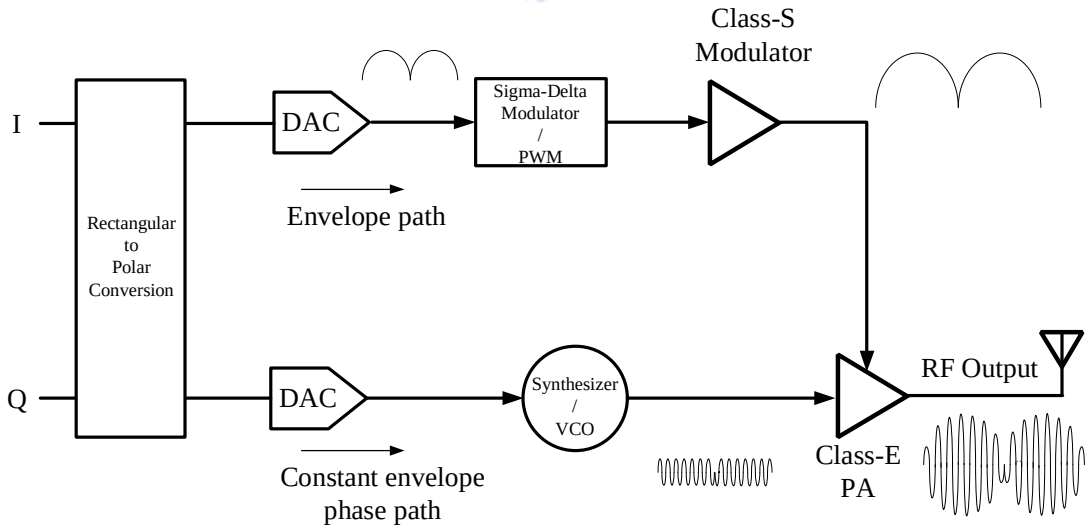


Figure 1.9 Polar transmitter architecture.

1.5 Organization

This thesis describes the design of on-chip RF CMOS Class-E PA.

Chapter 2 begins with the proposed Class-E PA consists of a cascode topology with finite dc-feed inductor and a Class-F driver to achieve an on-chip PA. Chapter 3 presents the implementation and experimental results including layout descriptions, measurement setup, and measurement results. Chapter 4 discusses the behavior modeling of the proposed Class-E PA for efficient RF/Baseband co-simulation. Chapter 5 makes conclusions and shows the future works.

Chapter 2

On-Chip RF CMOS Class-E Power Amplifier Design

2.1 The Proposed Class-E Power Amplifier

The frequency range of the Class-E PA is 2.3~2.7GHz. The output power should be larger than 20dBm to meet the transmitter of the WiMAX Class-2 specifications. Figure 2.1 shows the proposed Class-E PA. The proposed on-chip Class-E PA consists of a cascode topology with finite dc-feed inductor and a Class-F driver to obtain higher efficiency and output power. The detailed analysis of this work shall be discussed in the subsequent sections.

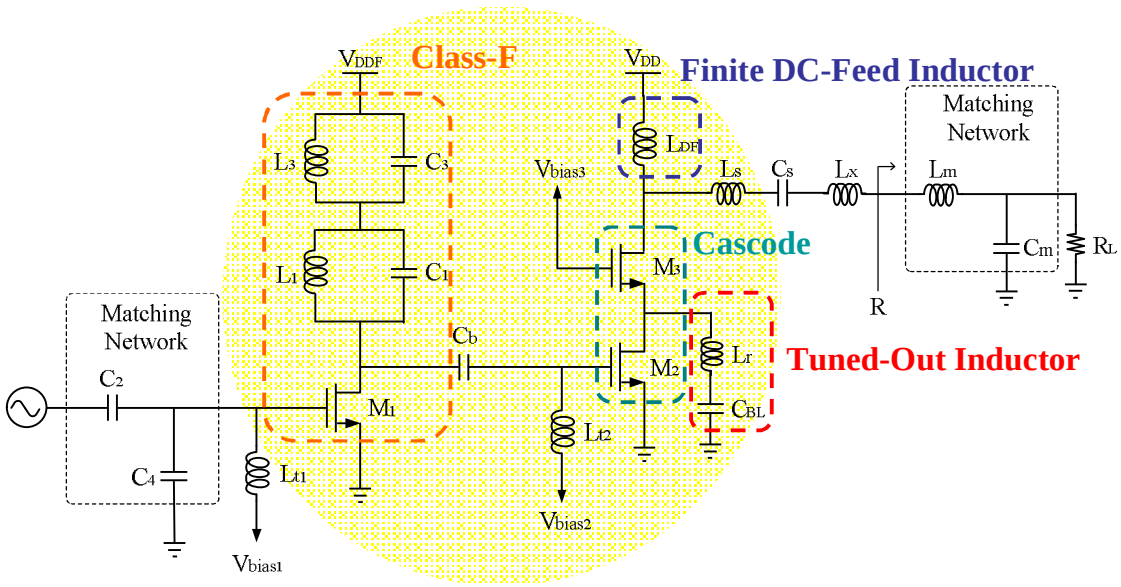


Figure 2.1 The proposed Class-E PA.

2.1.1 Cascode Topology

The design specifications include frequency range and output power. A supply voltage (V_{DD}) should be determined in the beginning. Table 2.1 shows the maximum V_{DG} when the switching device is on and off respectively. Assume the supply voltage of the Class-F driver equals to V_{DD}, and the voltage stress on the M_1 and M_2 are the same. We can obtain a maximum device stress of $V_{DG1}=V_{DG2}=2.3V_{DD}-V_{TH}$. Compared with the conventional common-course topology allows approximately the twice supply voltage. In other words, cascode topology solution ($V_{DG}=4.6V_{DD}-V_{TH}$), allows the use of a higher supply voltage for the same gate-oxide breakdown voltage. In the UMC CMOS 0.13-μm technology 3.3 V active devices, the minimum and typical gate-oxide breakdown voltages are 5 V and 8.1 V, respectively. According to

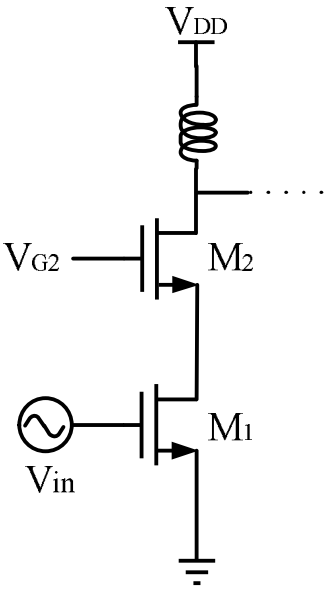


Figure 2.2 Cascode Topology.

	ON	OFF
M_2 (V_{DG2})	V_{G2}	$3.6V_{DD}-V_{G2}$
M_1 (V_{DG1})	$V_{DD}+V_{TH}$	$V_{G2}+V_{DD}-2V_{TH}$

$V_{DG1}=V_{DG2}=2.3V_{DD}-V_{TH}$

	$V_{Breakdown,min}$ (5 V)	$V_{Breakdown,typ}$ (8.1 V)
V_{DD}	~2.4 V	~3.7 V

Table 2.1 Analysis of supply voltage.

the equation in Table 2.1, we can obtain an initial design parameter, V_{DD}, of about 2.4 V. Now, we already have design parameters of operating frequency, supply voltage and output power. So we can start to obtain the other parameters of the Class-E PA.

2.1.2 Finite DC-Feed Inductor

Based on equations (A.1) ~ (A.8), we can obtain the other passive component parameters of the Class-E PA. Figure 2.3 shows the schematic of the Class-E PA with finite dc-feed inductor including the matching network.

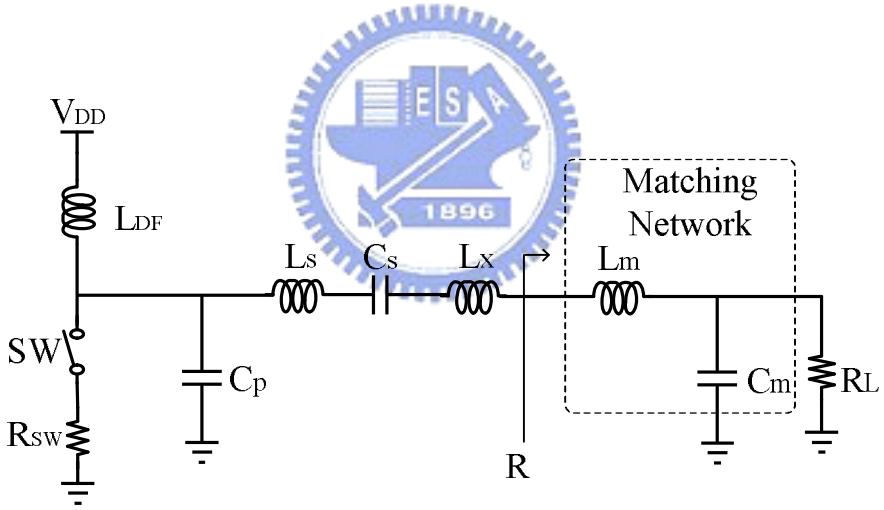


Figure 2.3 Schematic of Class-E PA with finite DC-feed inductor.

The Class-E PA specifications:

$V_{dc} = 2.4\ \ V,\ \ P_{out} = 24\ \ dBm \approx 251\ \ mW,\ \ f = 2.5\ \ GHz$

Assume a DC-feed inductance of L_{DF}=2 nH

Vdd(V)	2.4	
Pout(W)	0.251	
f(GHz)	2.5	
L_{DF}(nH)	2	
R_{dc}	22.94820717	
$X_{dc}(=\omega L_{DF})$	31.41592654	
$z(=X_{dc}/R_{dc})$	1.368992632	1<Xdc/Rdc<5
R	27.68459588	
$B(=\omega C_P)$	0.020116711	
$X(\omega L_X)$	7.586415102	
C_P	1.28067E-12	
L_X	4.82966E-10	

Table 2.2 Design parameters.

Resonator tank:

Select the quality factor of the loading network is about 3

$$L_s = \frac{R \cdot Q}{w} \tag{2.1}$$

$$C_s = \frac{1}{w^2 \cdot L_s} \tag{2.2}$$

Ls	3.95341E-09
Cs	1.02515E-12

Table 2.3 Design parameters.

Matching network [6]:

Because $R \approx 27.7 \ \Omega \ < R_L = 50 \ \Omega$

So

$$X_{L_m} = R\sqrt{\frac{R_L}{R} - 1} \tag{2.3}$$

$$X_{C_m} = \frac{R_L}{\sqrt{\frac{R_L}{R} - 1}} \tag{2.4}$$

X_{Cm}	55.69121853
X_{Lm}	24.85544095
Cm	1.14312E-12
Lm	1.58235E-09

Table 2.4 Design parameters.

2.1.3 Tuned-Out Indcutor

Base on cascode topology, efficiency could be improved by adding an inductor between M_1 and M_2 [3]. When M_1 is turned off, is associated to charging and discharging transients of the parasitic capacitor at node r, as shown in Figure 2.4, which is consist of M_1 drain-bulk and drain-source capacitances and M_2 source-bulk and gate-source capacitances. This power loss is not negligible at all and may degrade the advantages of an increased supply voltage. An effective way to minimize this power loss contribution is tuning out the capacitive parasitics by means of an inductor, resonating Cr at the desired operating frequency. A blocking capacitor C_{BL} is inserted between the inductor and ground. The inductor provides the current charging the parasitic capacitance, minimizing the current flow through the active devices, and their power dissipation [3]. The cascode Class-E PA with tuned out inductor shows in Figure 2.5.

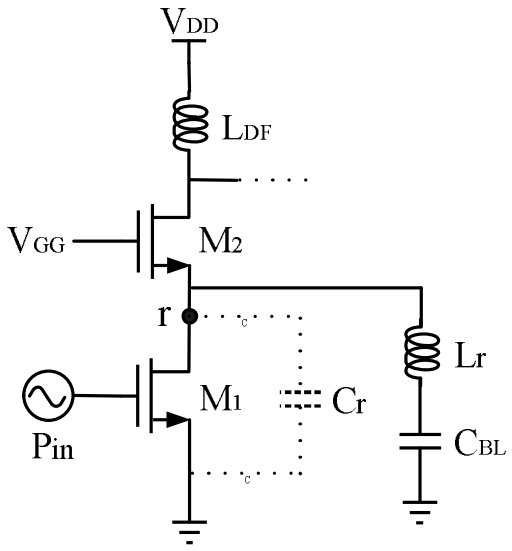


Figure 2.4 Cascode topology with tuned out inductor Lr.

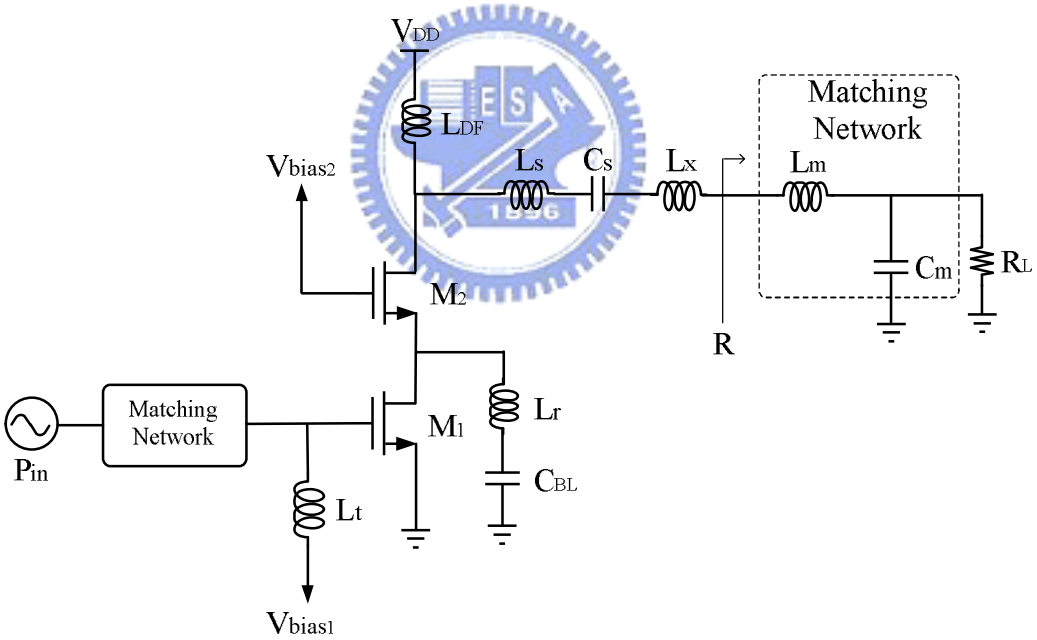


Figure 2.5 The cascode Class-E power amplifier with tuned out inductor.

2.1.3 Class-F Driver

Since the Class-E PA is performed in a switching mode operation, it is an important

issue to shape the input waveform for turning the transistor on and off. To obtain the shortest transition time from one switching state to the other, a square waveform should be applied into the Class-E PA. This function can be realized by using the Class-F PA as a driver stage, which can generate appropriate harmonics of the input signals and combining them into a square waveform [15] [16]. The Class-F driver stage, as shown in Figure 2.6, is used to produce square waveform signal to drive the Class-E power amplifier. The two parallel-tuned LC circuits operate at first and the third harmonics resonance of the input frequency where the inductance values can be computed by (2.5) and (2.6). The LC resonators are used to eliminate the even harmonics while the first and third harmonics are passed to next stage. And in order to loose the demand on high driving power in the Class-E power amplifier, using an inductor Lt to tune out the parasitic capacitor at M_1 gate [17].

$$1^{st} \quad harmonic: \quad L_1 = \frac{1}{w^2 C_1} \tag{2.5}$$

$$3^{nd} \quad harmonic: \quad L_3 = \frac{1}{9w^2 C_3} \tag{2.6}$$

where $w = 2pf$

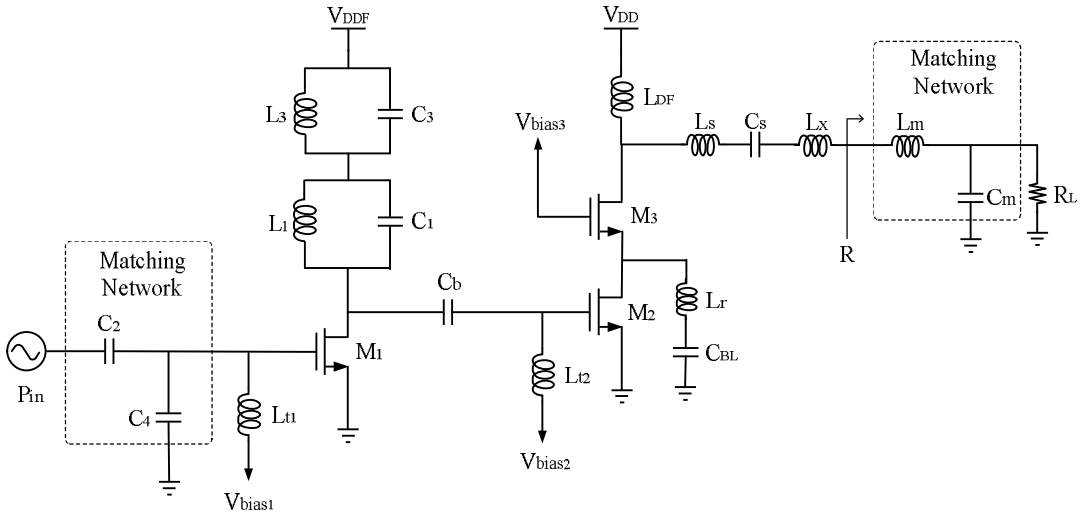


Figure 2.6 Cascode Class-E PA with Class-F driver.

2.1.4 Summary

In order to save the chip size we combine three inductors, Ls, Lx and Lm, into one, Lr, as show in Figure 2.7.

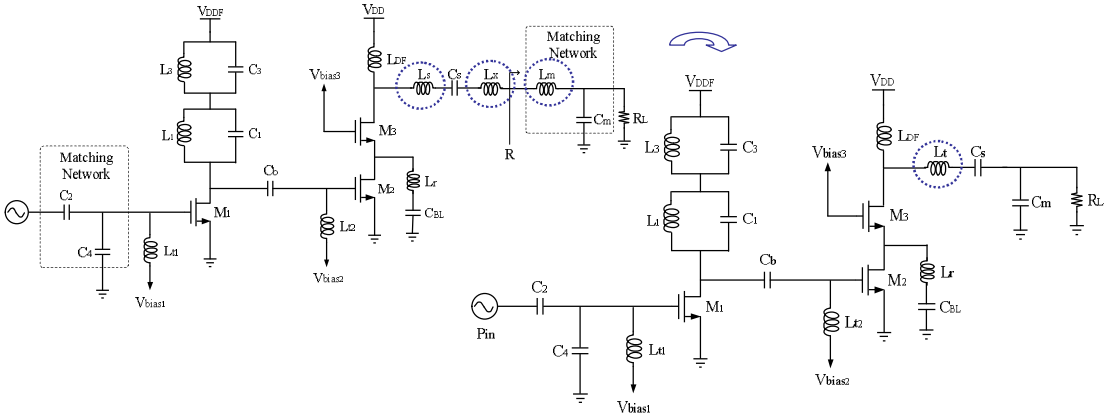


Figure 2.7 Combine three inductors into one for layout considerations.

2.2 Simulation Results

The simulation environment is on the cadence RFDE. And the simulation results are listed below:

- **Drain Voltage & Current of M_1 & M_2**

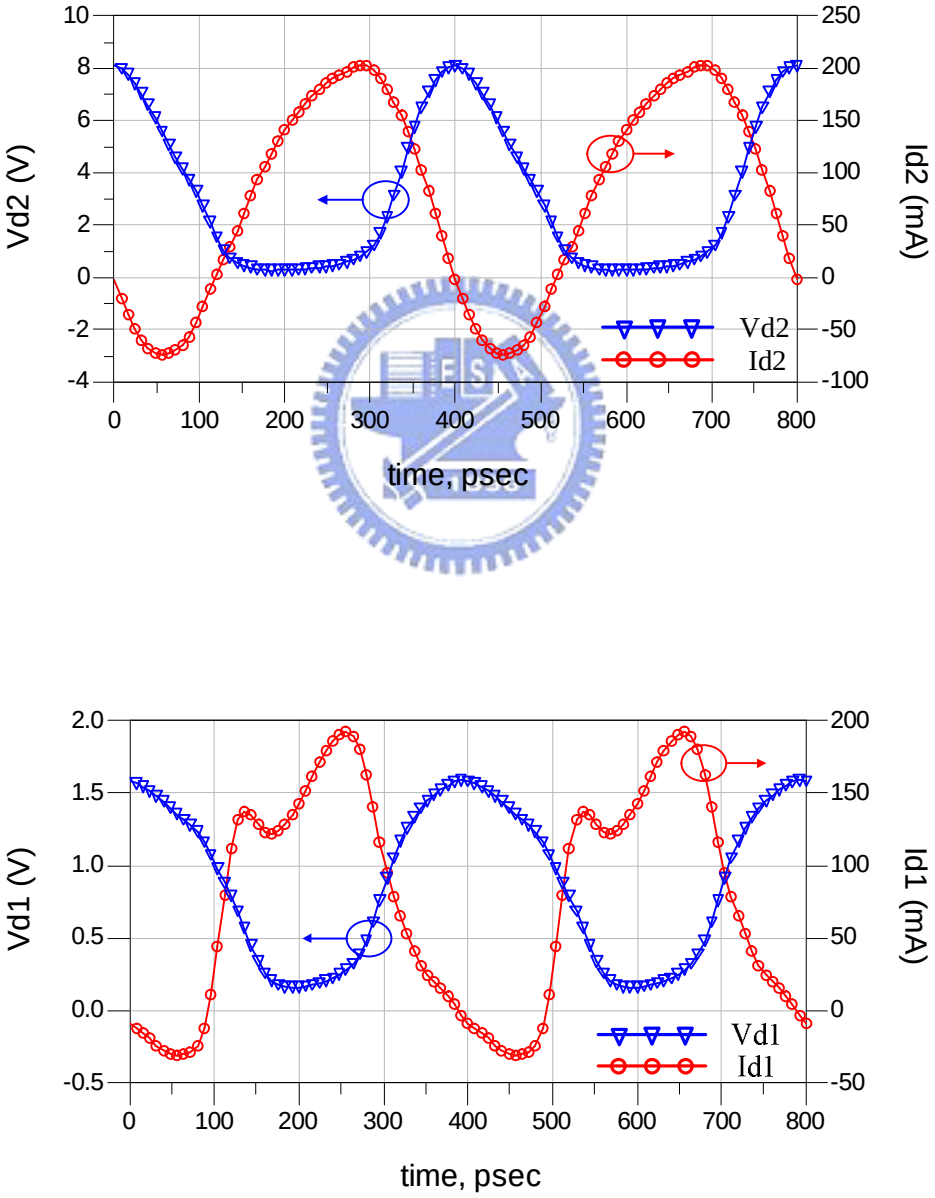


Figure 2.8 Drain voltage and current of M1 and M2.

• **Output Power & PAE v.s. Input Power**

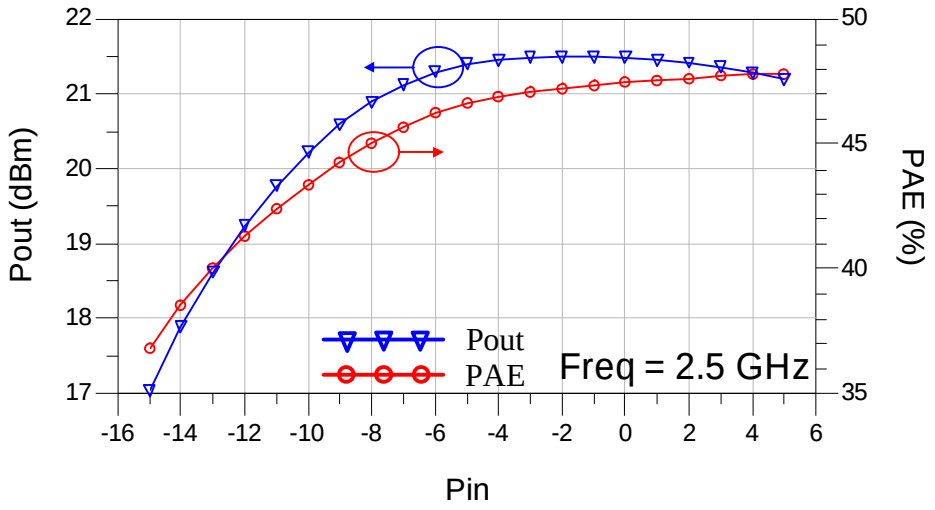


Figure 2.9 Simulation results of output power and PAE v.s. input power.

• **Output Power & PAE v.s. Operating Frequency**

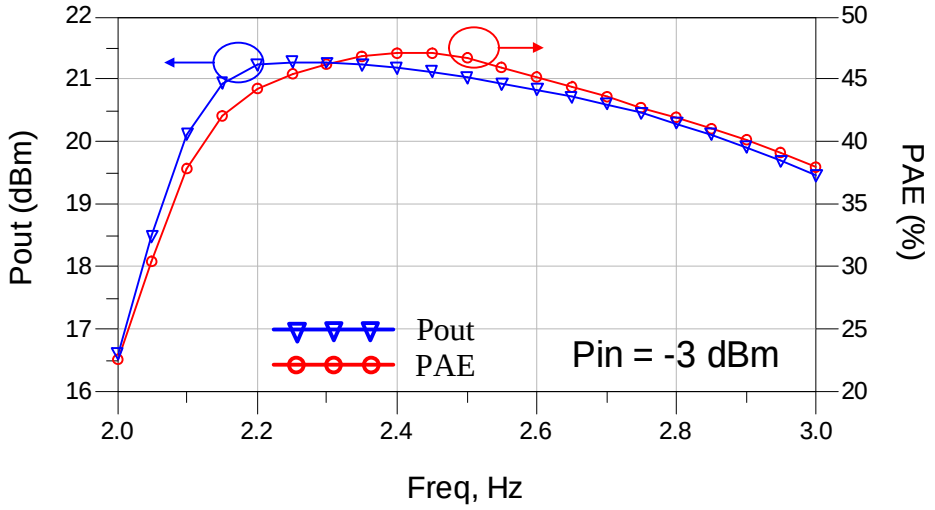


Figure 2.10 Simulation results of output power and PAE v.s. frequency.

• **Output Power & PAE v.s. Supply Voltage**

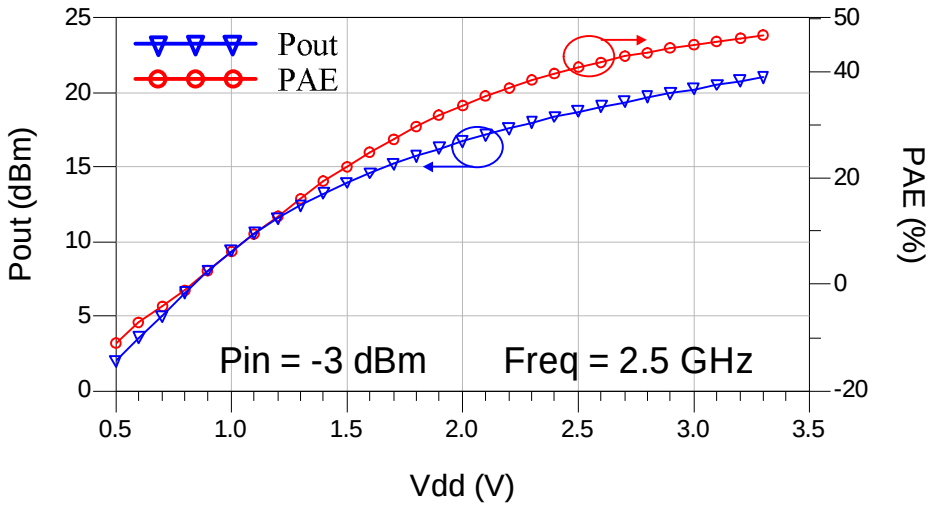


Figure 2.11 Simulation results of output power and PAE v.s. supply voltage.

• **LSSP (Large Signal S-Parameter)**

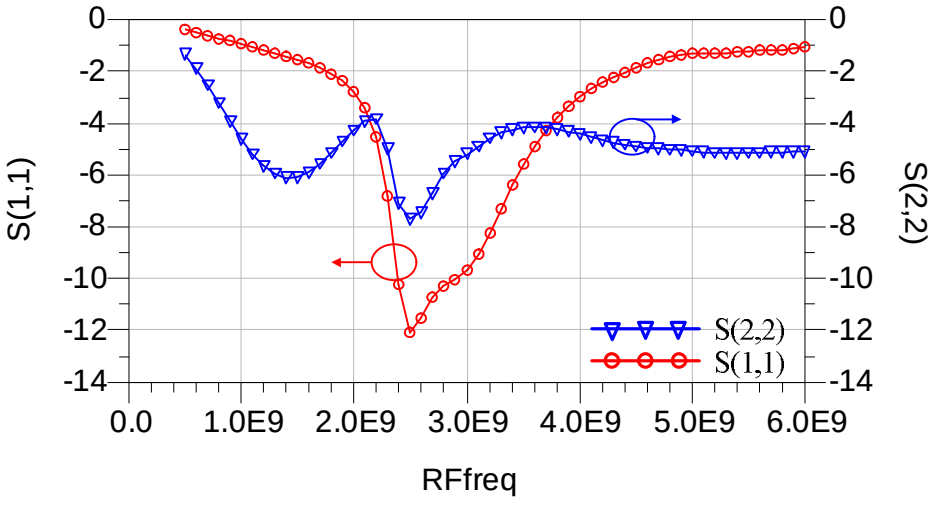


Figure 2.12 Simulation results of LSSP.

• **Comparisons**

Parameters	**Tech. (CMOS)**	**Operate Frequency (Hz)**	**Die Area (mm^2)**	**Supply Voltage (V)**	**Output Power (dBm)**	**PAE (%)**	**Gain (dB) *(Pin)***	**FOM**
[17] 2006 Radio & Wireless	0.18μm	2.35G	1.7	1.2	11	44.5	5 *(6)*	0.10
[18] 2005 Microwave Con.	0.18μm	2.4	1.1*1.1	1.2	9.5	33	11 *(-1.5)*	0.21
Proposed Work (Po-Sim)	0.13μm	2.5G	1*1.49	3.3	21	48.4	24 *(-3)*	95.66

• $FOM = P_{out} \times Gain \times PAE \times f^2 \quad (W \times GHz^2)$

Table 2.5 Comparisons with other published papers.

Chapter 3

Implementation and Measurement Results

3.1 Chip Layout Descriptions

The experimental chips, P1 and P2, are designed and fabricated by UMC 0.13-μm single-poly-eight-metal (1P8M) CMOS technology. P1 is Class-E PA without Class-F driver and P2 is Class-E PA with Class-F driver. The total chip area include pads, as shown in Figure 3.1 and 3.2, are 1mm×1mm and 1mm×1.49mm. The total width of M_1 and M_2 are 2112 μm. In order to decrease the device cell numbers for layout easier, we choose the maximum finger number and maximum width in one cell. Finally, M_1 and M_2 only need each 11 cells to achieve the total width of 2112 μm. The wider metal lines are used in power line because of the large current through it. The triangular metal lines are used to average the large current to each cells of the active device for preventing the device broken when large current through it. Using the MOS capacitors in order to meet the rules of DRC metal density, and these MOS capacitors also could be the bypass capacitors used in each dc bias at the same time. To decrease

the chip size, we combine three inductors, Ls, Lx and Lm, into one, Lt, as shown in Figure 3.1 and 3.2.

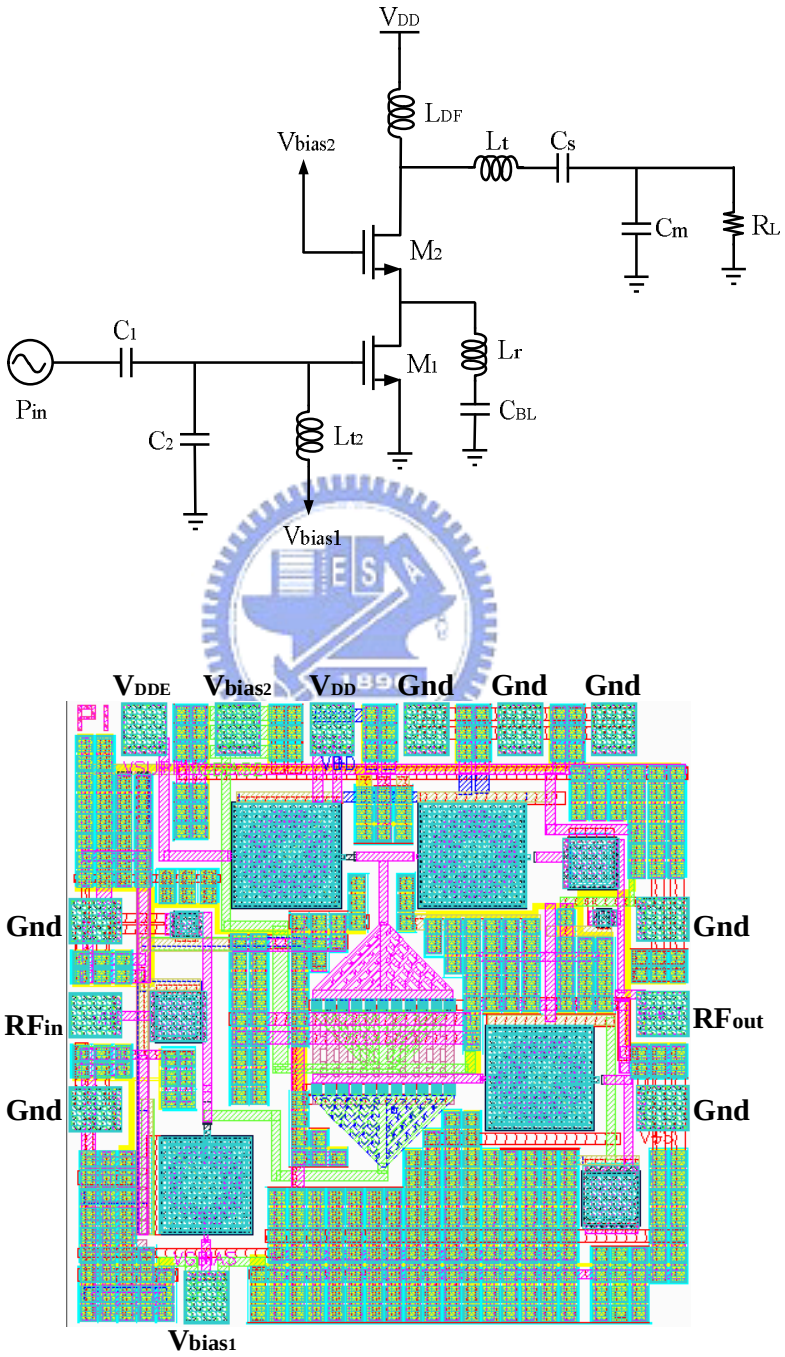


Figure 3.1 Schematic and layout views of Class-E PA without Class-F driver.

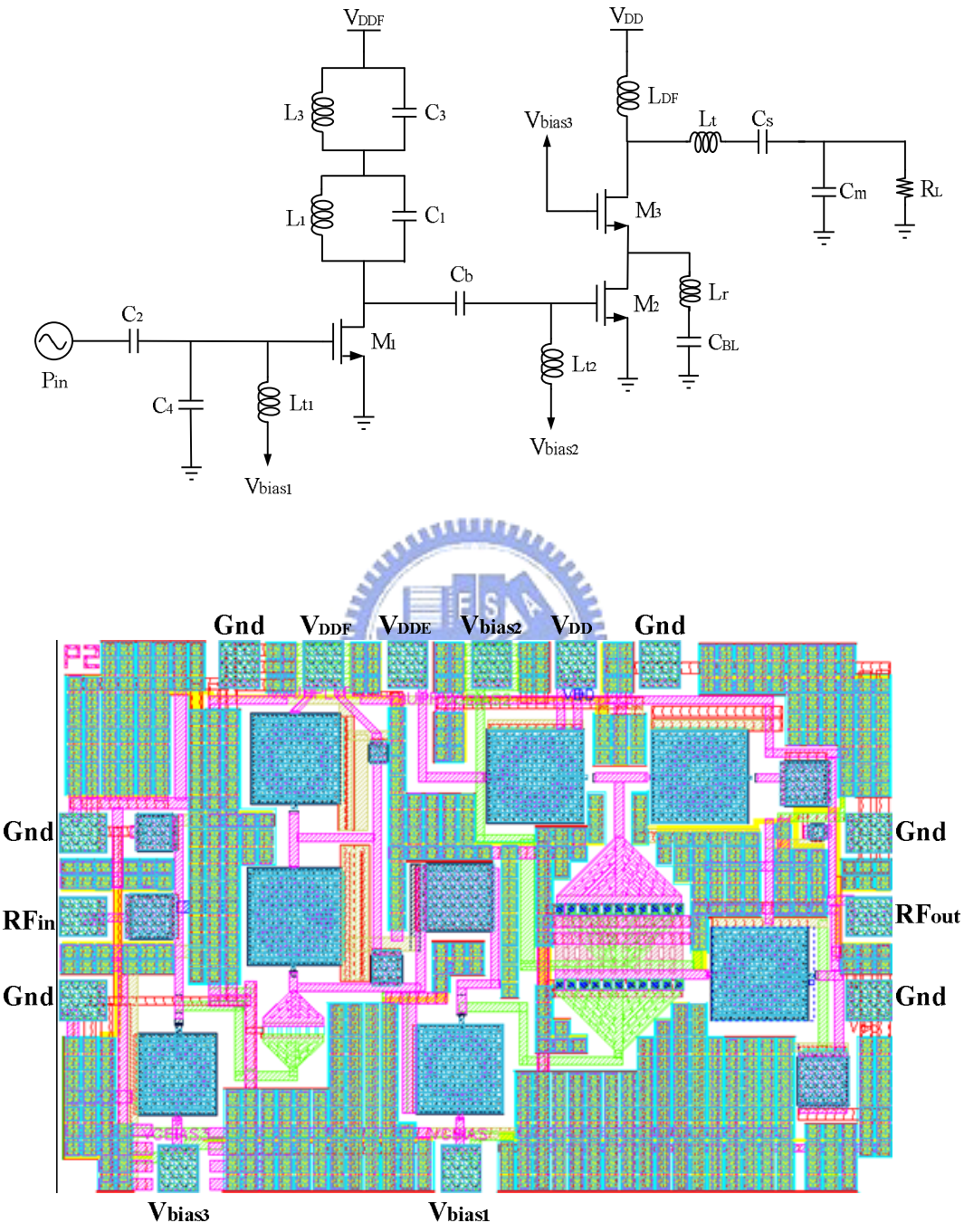


Figure 3.2 Schematic and layout views of Class-E PA with Class-F driver.

3.2 Measurement Results

3.2.1 Measurement Setup

The equipments used in this measurement are list below:

- Signal Generator (ESG) × 1
- Power Supply × 5
- Spectrum Analyzer × 1
- Oscilloscope × 1
- 150 μm GSG Probe × 2
- DC Probe (Single point) × 2
- DC Probe (6-pin, 150 μm) × 1

Designing the circuit must consider the impedance matching, and the ESG, Spectrum Analyzer and Oscilloscope are required to examine the matching condition. However, the impedance of these equipments are 50Ω. The measurement setup shows in Figure 3.3.

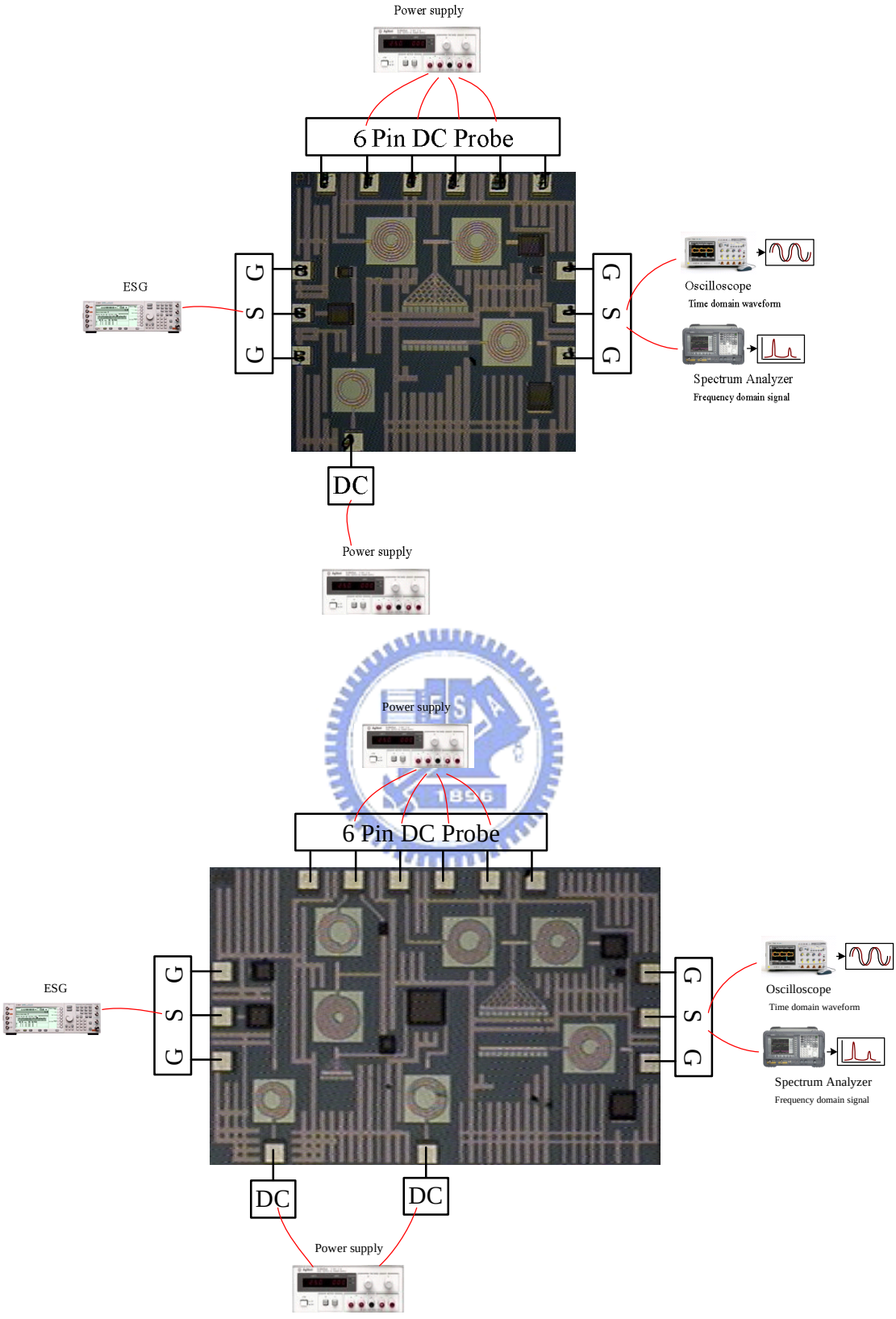
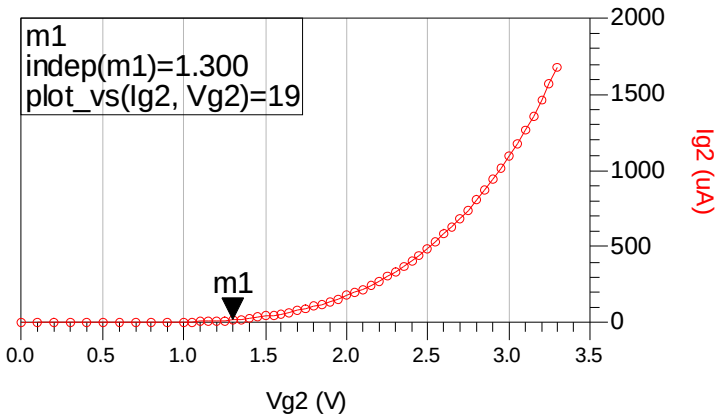


Figure 3.3 Measurement Setups of P1 and P2.

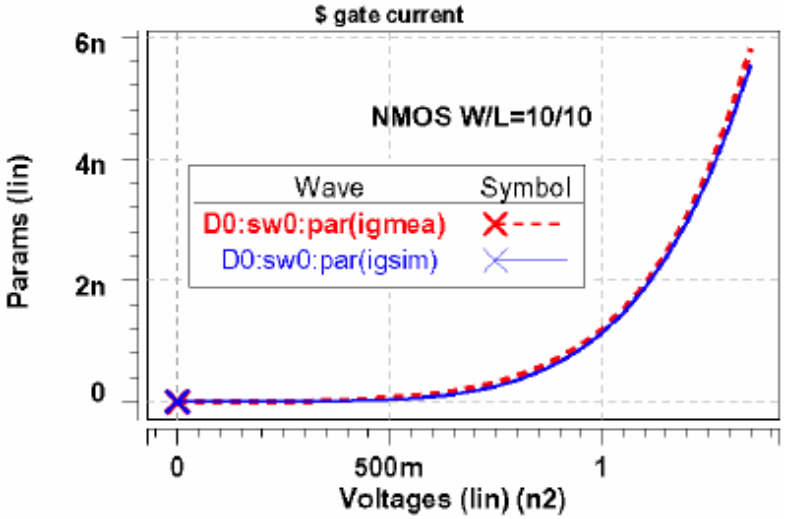
3.2.2 Simulation and Measurement Results

In the beginning, the DC measurement is performed. Unfortunately, a dc current is found at the gate of transistor M_2, as shown in Figure 3.4. But M_2 gate should not have dc current. So, some debug works is done after measurement. The reasonable answer could be due to the gate leakage current of MOS bypass capacitor. Since the 1.2V MOS bypass capacitors are used at each dc bias nodes. However, the bias voltage of M_2 gate is 2.1V that exceeding the 1.2 V, which may cause the gate-oxide of the MOS bypass capacitor breakdown and produce leakage current at M_2 gate. Therefore, the circuit performances have severely degradation due to incorrect bias. The measurement results of the P1 are list below.

- **M_2 Gate Current v.s. M_2 Gate Voltage**



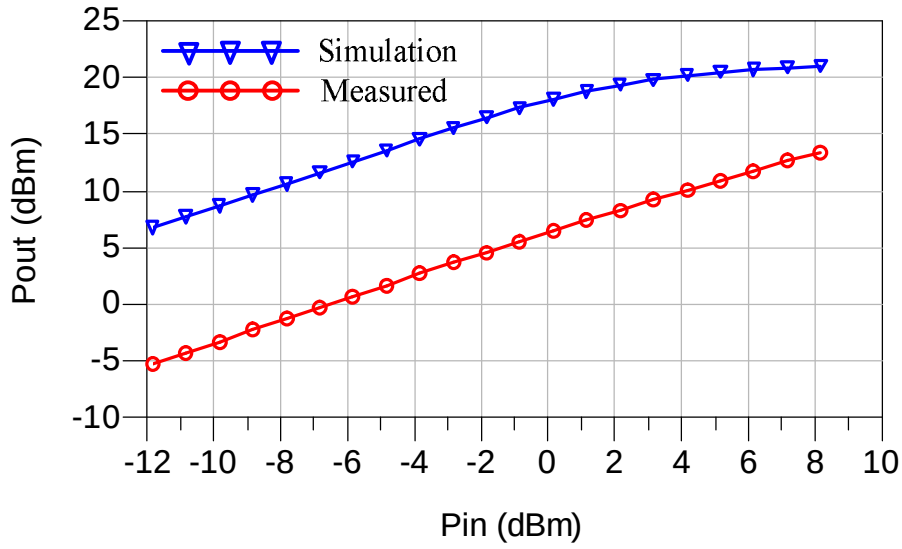
3.4 (a)



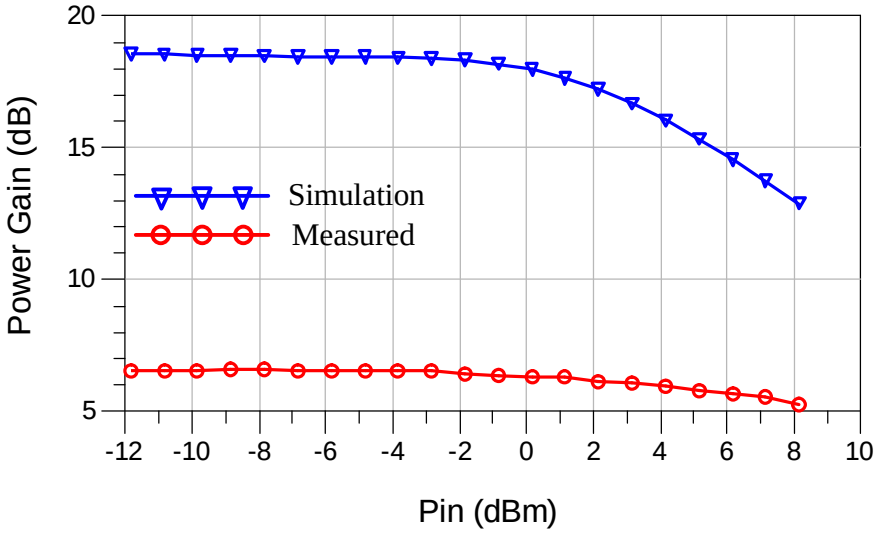
3.4 (b)

Figure 3.4 M2 gate leakage current of (a) simulation result (b) from UMC document [19].

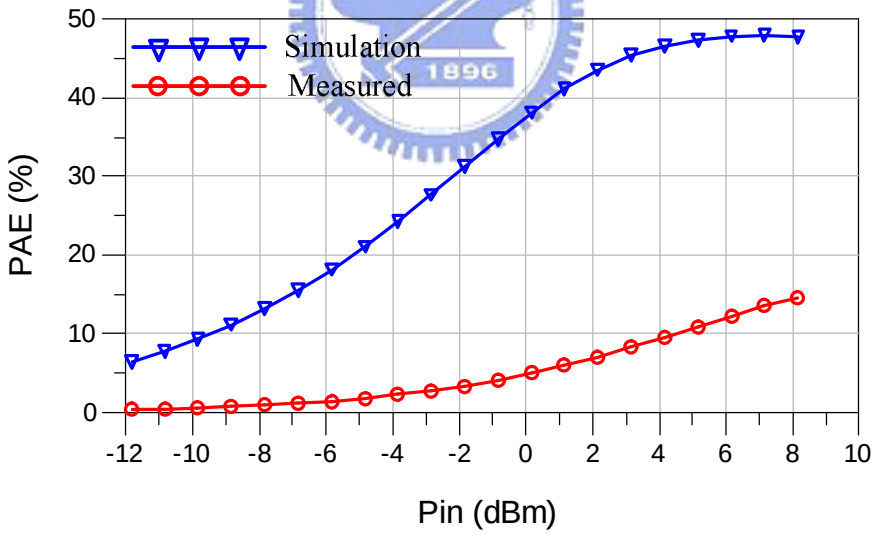
- **Output Power & Power Gain & PAE v.s. Input Power**



3.5 (a)



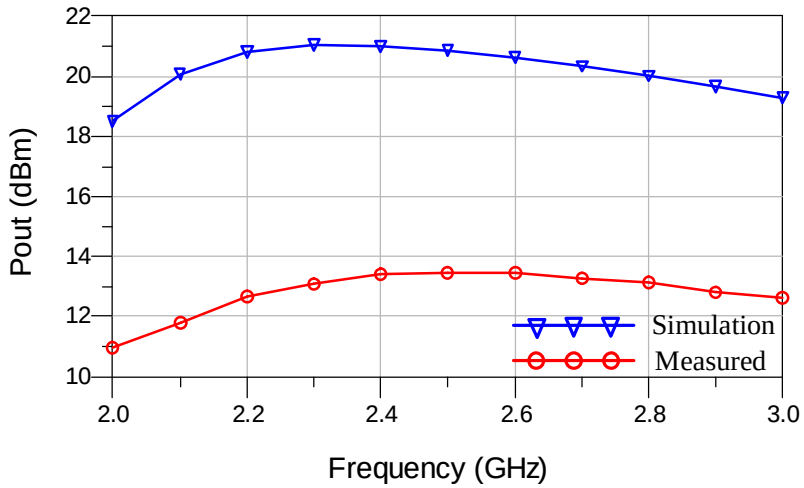
3.5 (b)



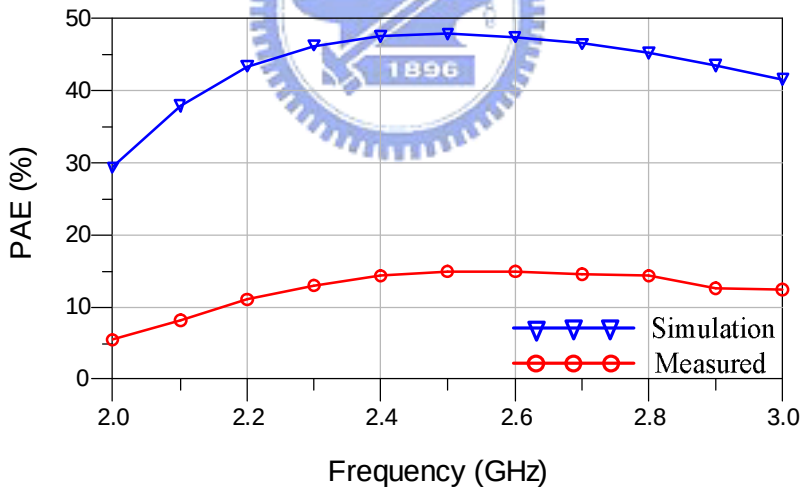
3.5 (c)

Figure 3.5 Simulation results of (a) output power v.s. input power (b) power gain v.s. input power (c) PAE v.s. input power.

• **Pout & PAE v.s. Freq.**



3.6 (a)

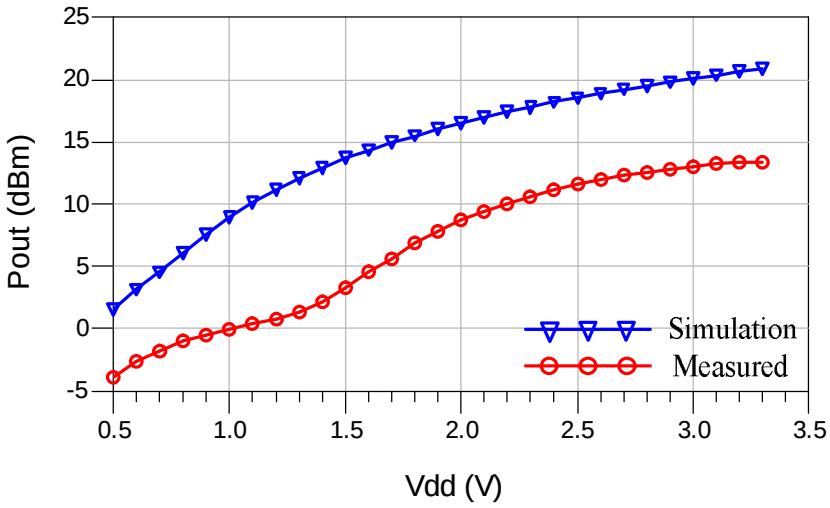


3.6 (b)

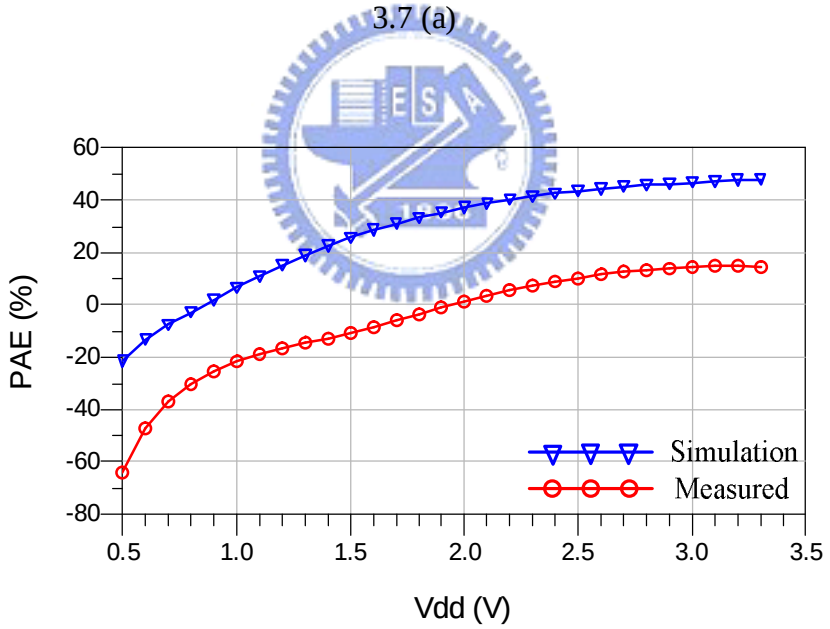
Figure 3.6 Simulation results of (a) output power v.s. operating frequency

(b) PAE v.s. operating frequency.

• **Output Power & PAE v.s. Vdd**



3.7 (a)



3.7 (b)

Figure 3.7 Simulation results of (a) output power v.s. supply voltage

(b) PAE v.s. supply voltage.

Chapter 4

Behavior Model

To do the RF/Baseband co-simulation of the proposed on-chip Class-E PA with polar transmitter the behavior model is needed. In order to reduce the time of circuit simulation and system verification, behavior models are used in circuit simulation and RF/Baseband co-simulation.

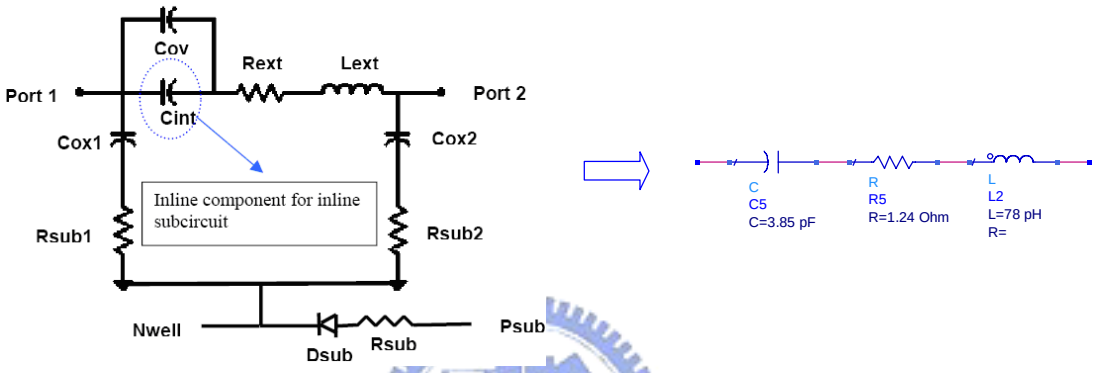
4.1 Behavior Model of Class-E PA

In the modeling flow from [20], the RF modules can be divided into three parts: input interface, output interface and G_m stage. We developed the behavior models of each part. Then circuit simulation and system simulation will be accomplished by these behavior models. In this chapter, the behavior model of Class-E PA without driver stage is for efficient and accurate RF/Baseband co-simulation. The modeling flow starts form the impedance networks and the switched-mode transistor.

4.1.1 Input and Output Matching

• **Capacitor**

Figure 4.1 (a) shows the capacitor model in UMC design kits documents and Figure 4.1 (b) is it equivalent circuit. The capacitor can be represented by series R, L and C. Figure 4.2 shows the s-parameter simulation results of the behavior model and transistor level.



4.1(a) [21] 4.1(b)

Figure 4.1 Capacitor of (a) UMC model (b) it equivalent circuit.

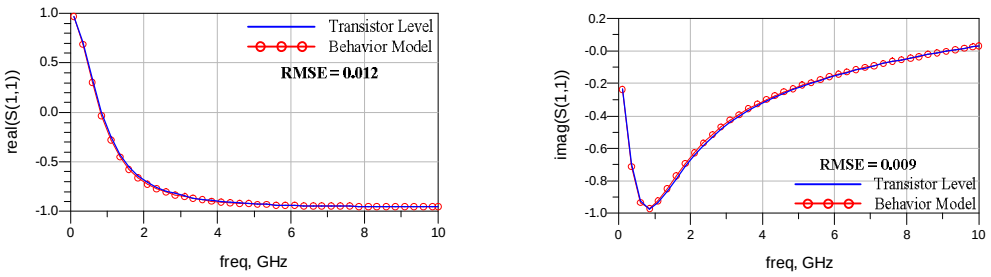
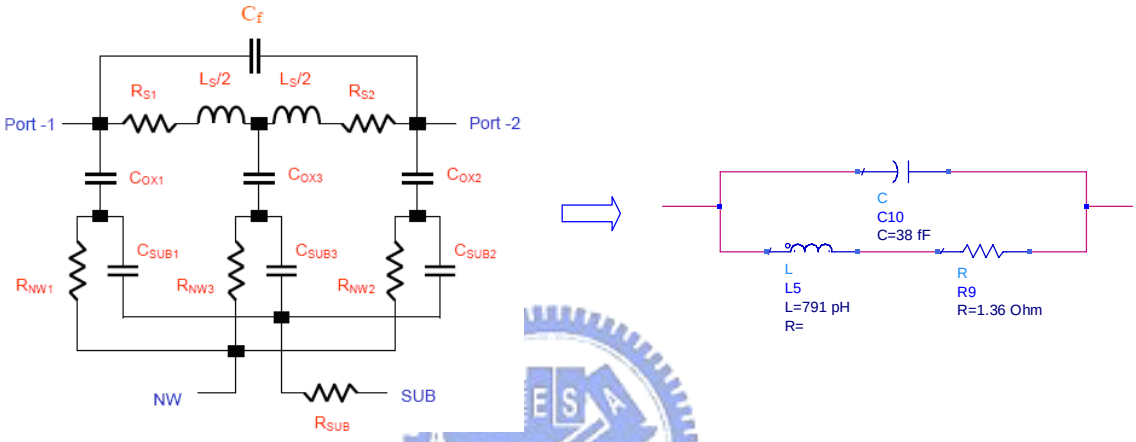


Figure 4.2 Capacitor's SP simulation results of behavior model and transistor level.

• **Inductor**

Figure 4.3 (a) shows the inductor model in UMC design kits documents and Figure 4.3 (b) is it equivalent circuit. The inductor can be represented by series R and L with parallel C. Figure 4.4 shows the s-parameter simulation results of the behavior model and transistor level.



4.3 (a) [21] 4.3(b)

Figure 4.3 Inductor of (a) UMC model (b) it equivalent circuit.

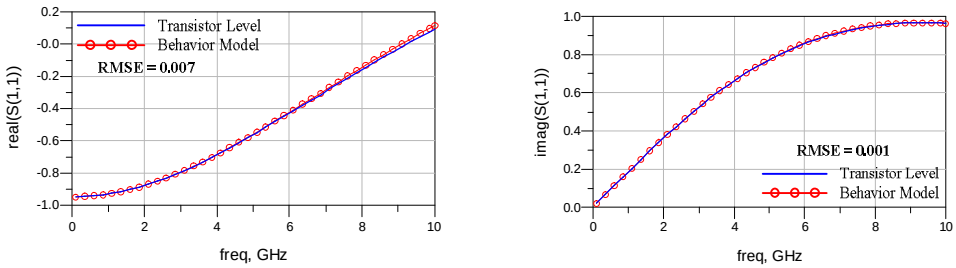
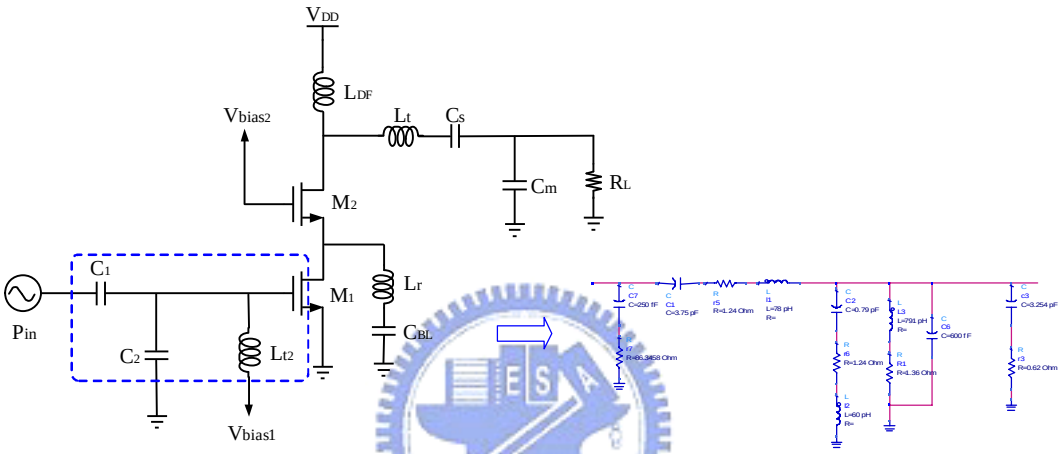


Figure 4.4 Inductor's SP simulation results of behavior model and transistor level.

• **Input Matching**

Figure 4.5 (a) and (b) shows the schematic and equivalent circuit of input matching. Similarly, use the method above the behavior model of input matching can be achieved by capacitors, inductors and resistances. Figure 4.6 shows the s-parameter simulation results of the behavior model and transistor level.



4.5 (a) 4.6 (b)

Figure 4.5 Input matching of (a) schematic (b) it equivalent circuit.

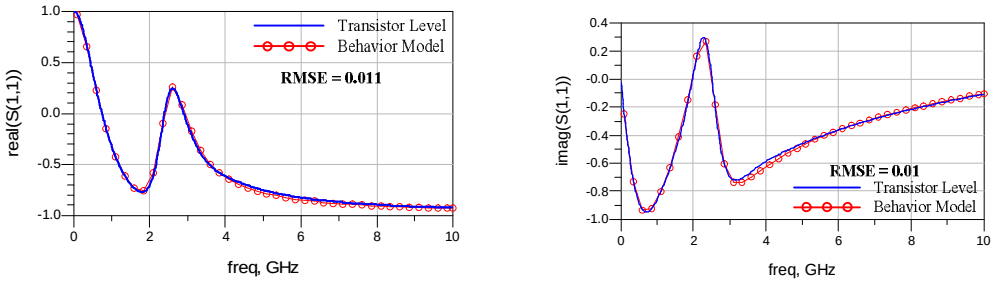
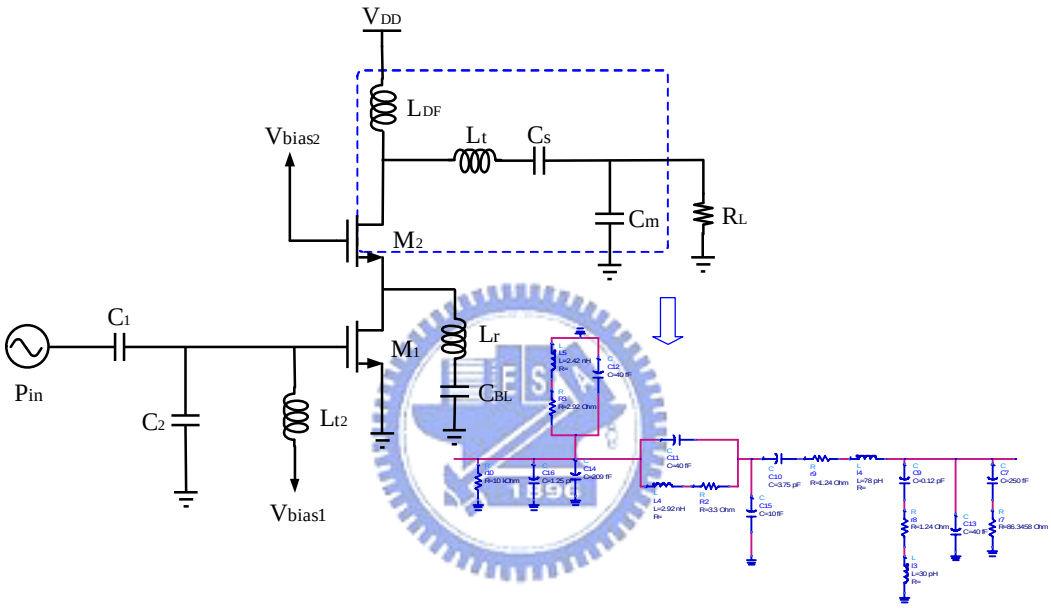


Figure 4.6 SP simulation results of the input matching of behavior model and transistor level.

• **Output Matching**

Figure 4.7 (a) and (b) shows the schematic and equivalent circuit of input matching. Similarly, use the method above the behavior model of output matching could be achieved by capacitors, inductors and resistances. Figure 4.8 shows the s-parameter simulation results of the behavior model and transistor level.



4.7 (a) 4.7(b)

Figure 4.7 Output matching of (a) schematic (b) it equivalent circuit.

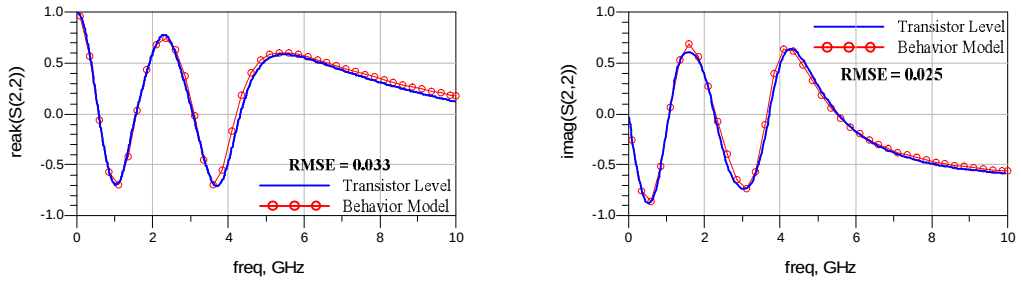


Figure 4.8 SP simulation results of the output matching of behavior model and transistor level.

4.1.2 Switched-Mode Transistor

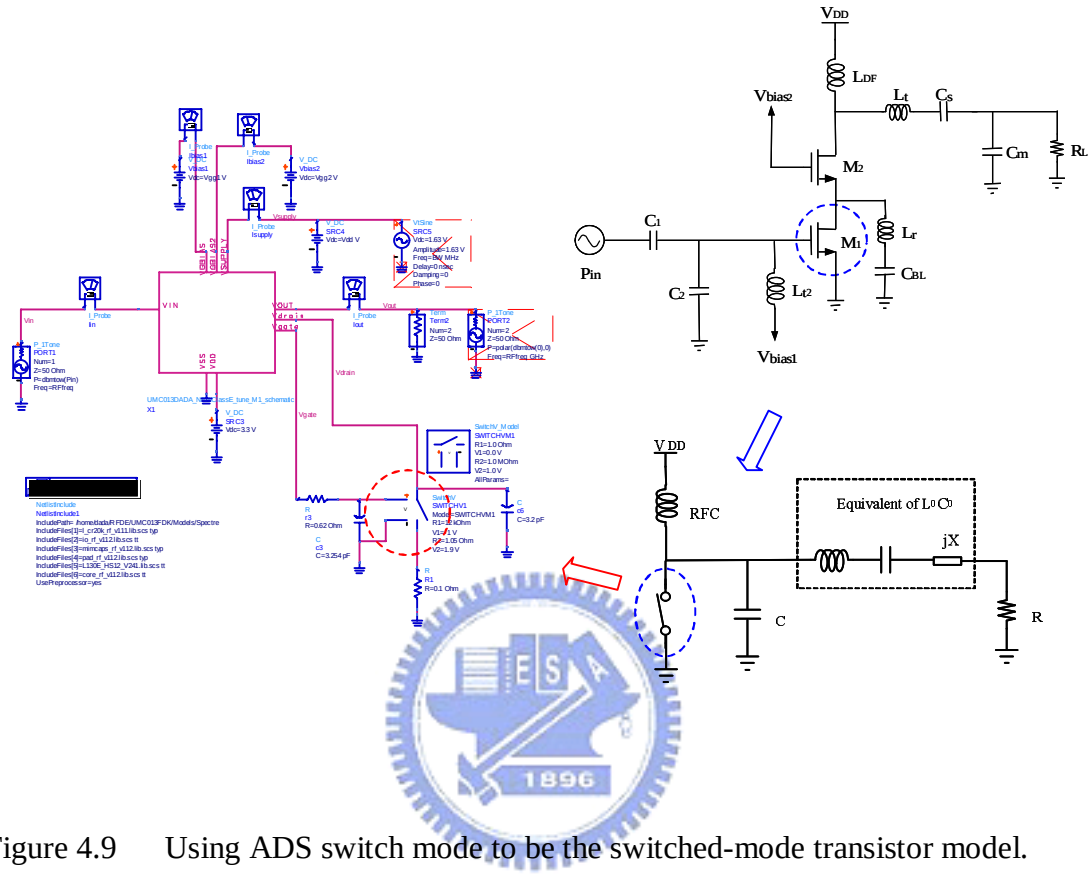


Figure 4.9 Using ADS switch mode to be the switched-mode transistor model.

Because the operation of the transistor M_1 is like a switch, it can not be modeled by a simple G_m stage. Hence, we use the switch model provide in ADS at first. Figure 4.10 shows the design procedure of the switched-mode transistor. Here, we have three thresholds, 0.3 V, 0.8 V and 1.8 V. When $V_{gg1} < 0.3$ V and $0.8V < V_{gg1} < 1.8$ V, the ADS switch can be used to model it, as shown in Step 1. When $V_{gg1} > 1.8$ V, the transistor's operation region might be in the triode-region. Therefore, the turn on

resistance equation in triode-region MOSFET can be used to model it, as shown in Step 2. When 0.3 V < V_{gg1} <0.8 V, we modify the parameter in step 1 to fit it, as shown in Step 3. Finally, we combine Step1 ~ Step 3, as shown in Step 4, to accomplish the behavior model of the switch-mode transistor. The comparisons of circuit simulation are shown in Figure 4.11.

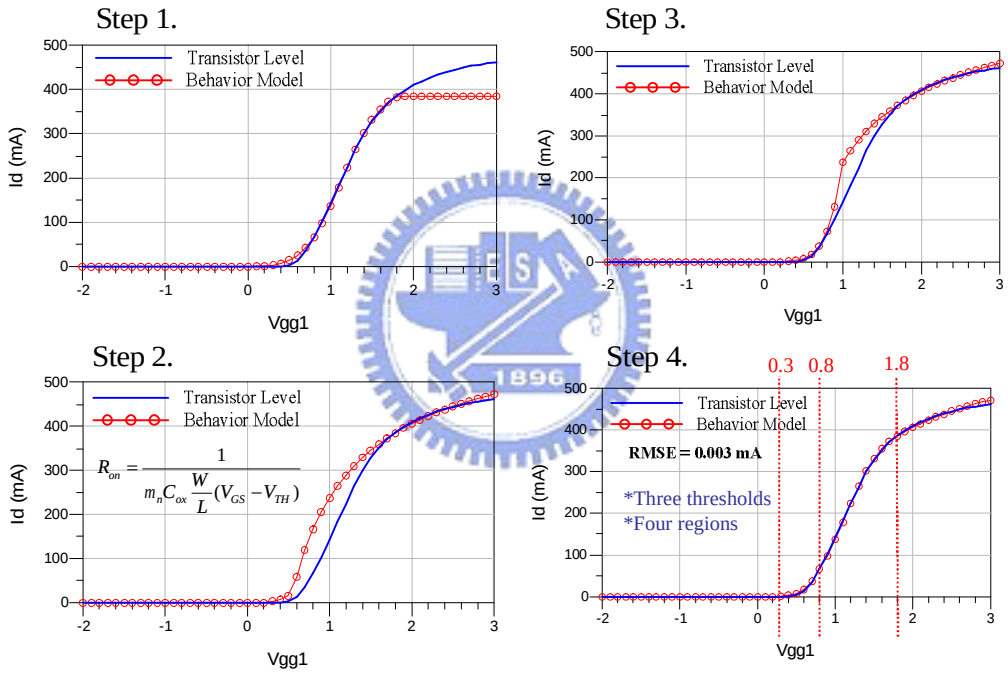


Figure 4.10 Summary of Step 1 ~ Step 4.

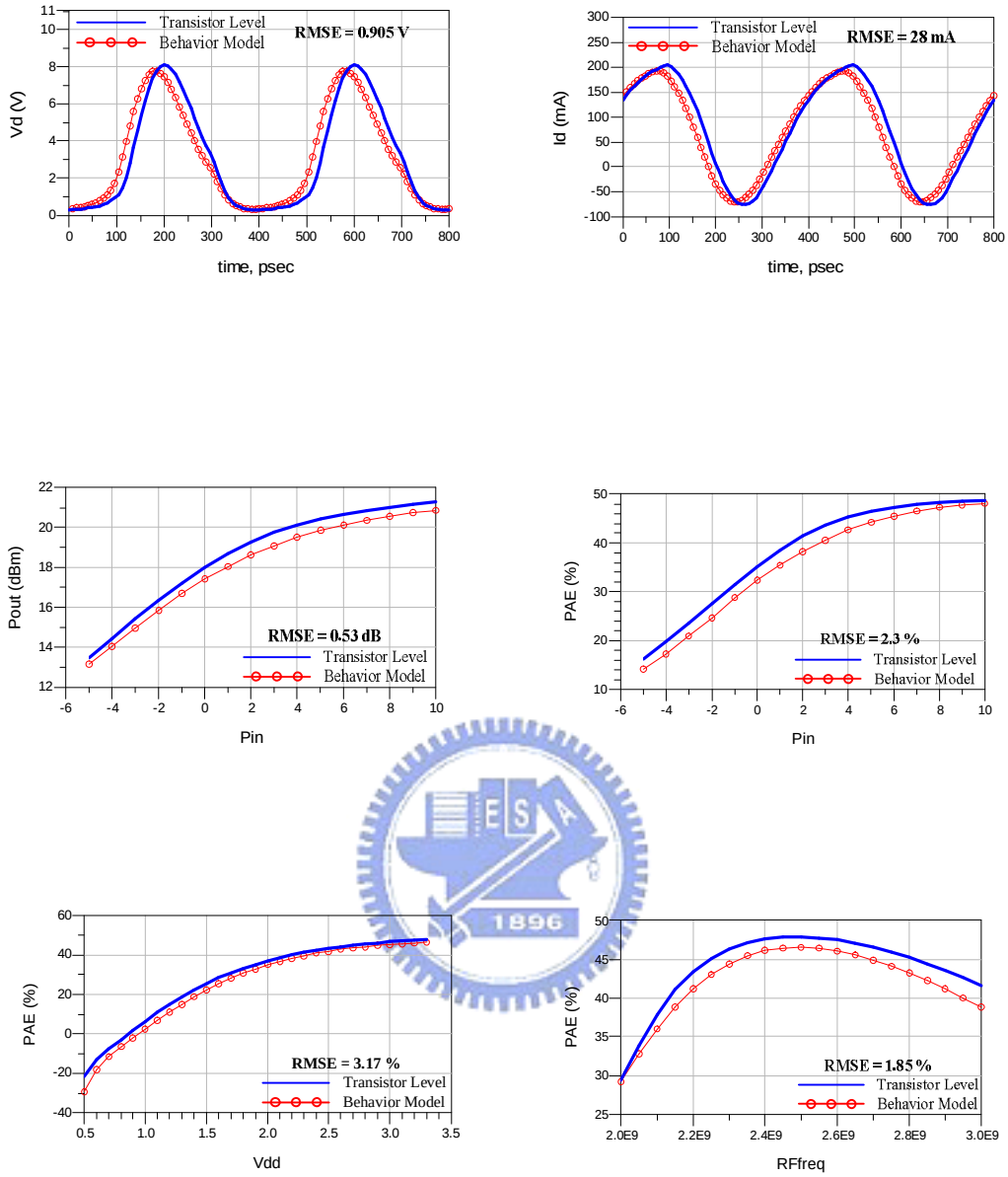


Figure 4.11 Comparisons of circuit simulation between transistor level and behavior model.

4.2 RF/Baseband Co-Simulation

For applying in a polar transmitter, the behavior model of the Class-E PA becomes

a three-port circuit, as shown in Figure 4.12. In order to do RF/Baseband co-simulation a simplified polar transmitter is presented, as shown in Figure 4.13. And the behavior model used in RF/Baseband co-simulation excludes the transistor M2. Figure 4.14 shows the schematic of behavior model without transistor M2. Because of RF/Baseband co-simulation in transistor level costs a lot of time, more the half month. Therefore, instead of using real passive components from UMC FDK model, inductors and capacitors, the ideal passive components in ADS to do RF/Baseband co-simulation. In other words, only the switched-mode transistor behavior model is used in RF/Baseband co-simulation.

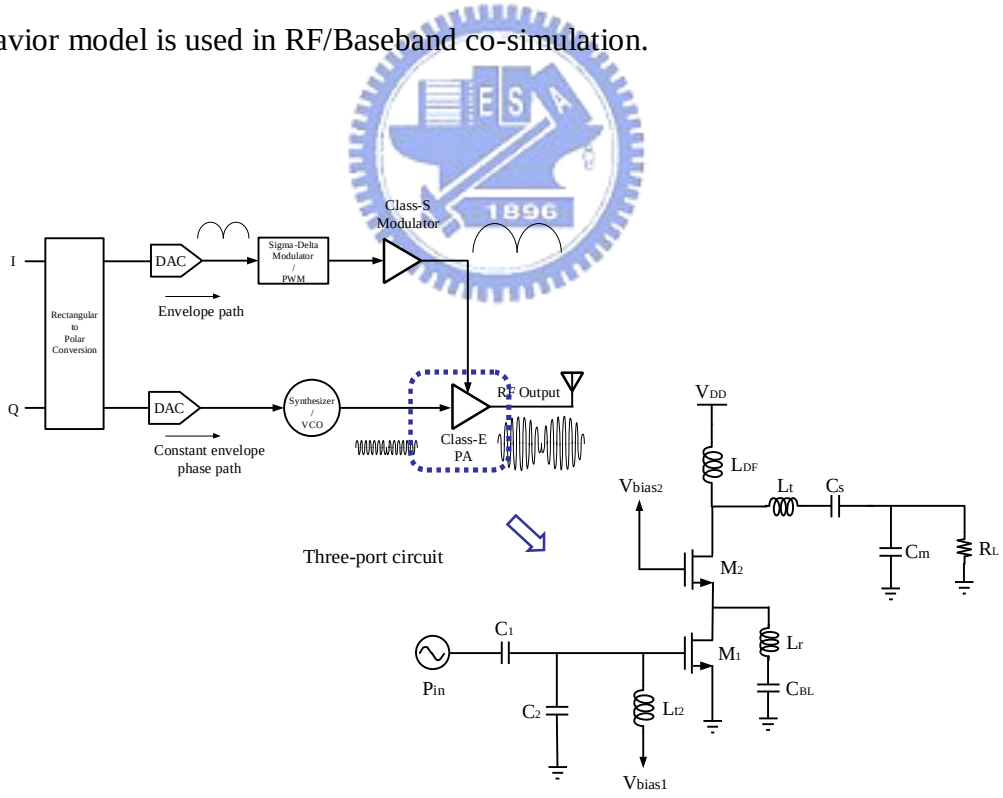


Figure 4.12 The three-port circuit.

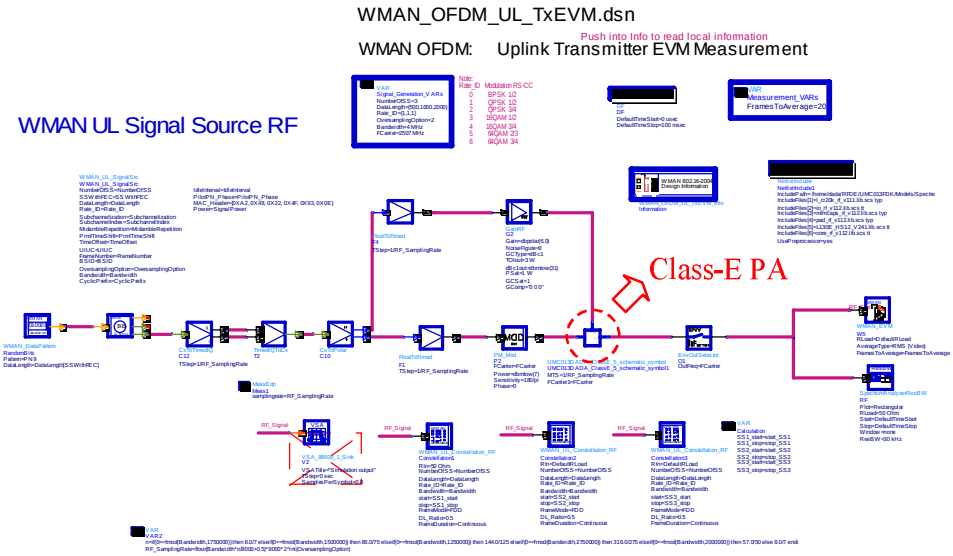


Figure 4.13 Schematic of simple polar transmitter in ADS.

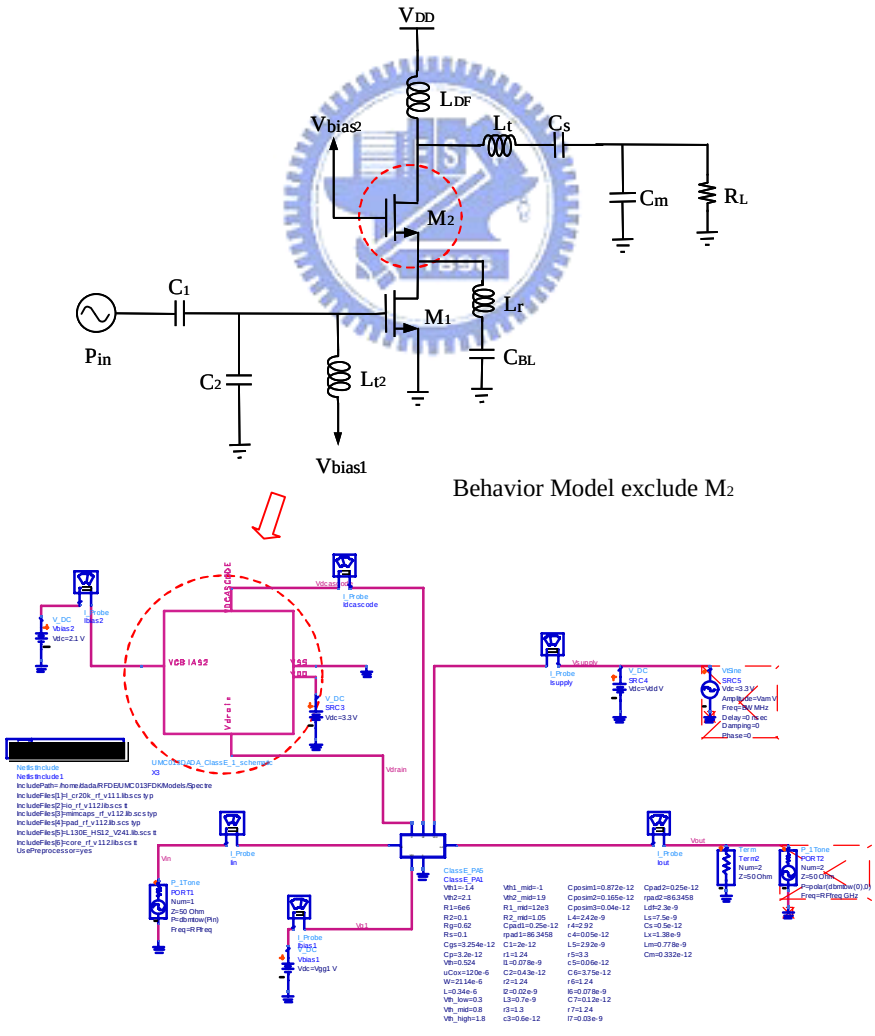


Figure 4.14 Schematic of behavior model without transistor M2.

The simulation results of RF/Baseband co-simulation are shown in Figure 4.15. The conditions are 14 MHz bandwidths and 2.5GHz carrier frequency. Three different modulation signals are considered in the RF/Baseband co-simulation. The results show the root-mean-squared error (RMSE) is about 0.125 dB.

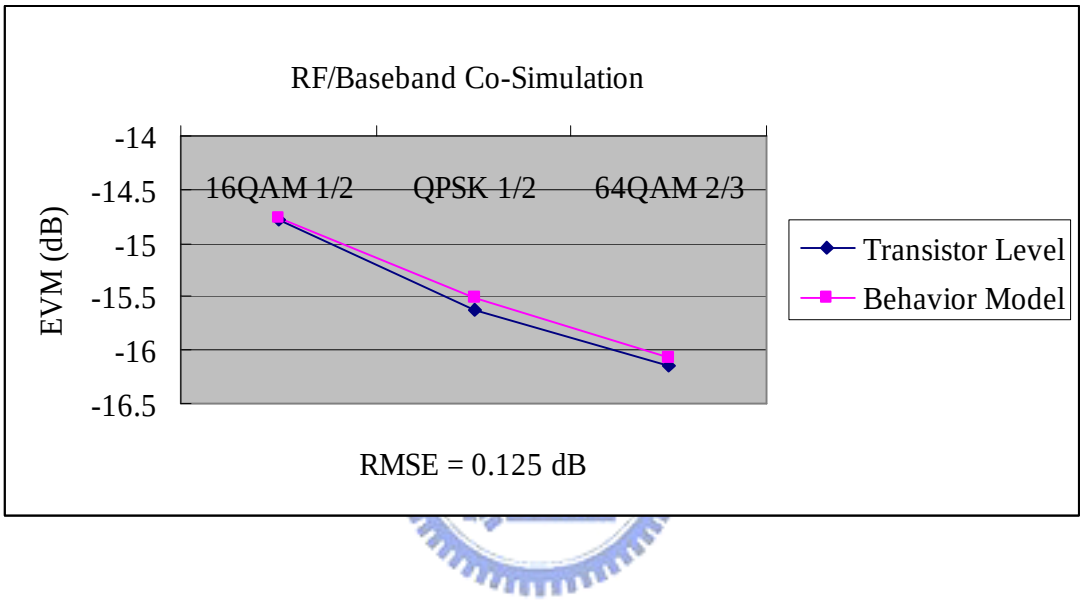


Figure 4.15 Comparisons of RF/Baseband co-simulation.

4.3 Comparisons of Simulation Time

After finishing the circuit simulation and RF/Baseband co-simulation, the simulation time comparisons are presented. Figure 4.16 shows the comparisons of the circuit simulation time, the simulation time of the proposed behavior model are less than transistor level. Figure 4.17 shows the comparisons of the simulation time of the RF/Baseband co-simulation, the behavior model could save about 93% simulation

time compared with the transistor level. Therefore, the proposed behavior model could save a lot of simulation time.

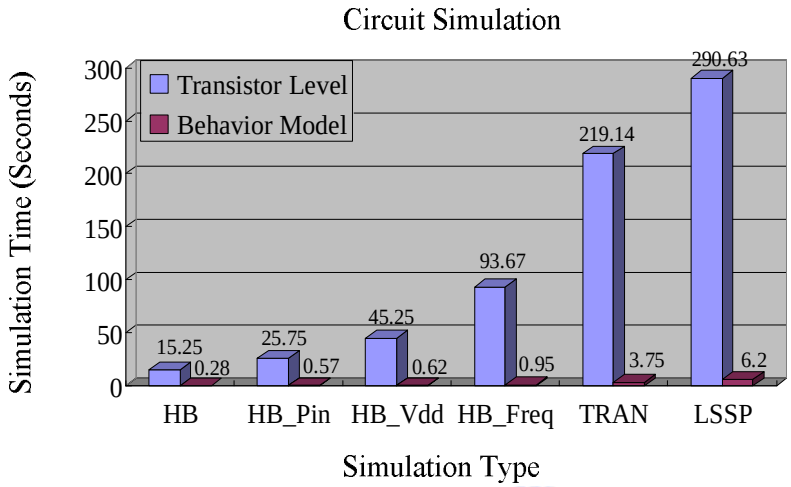


Figure 4.16 Comparisons of circuit simulation time.

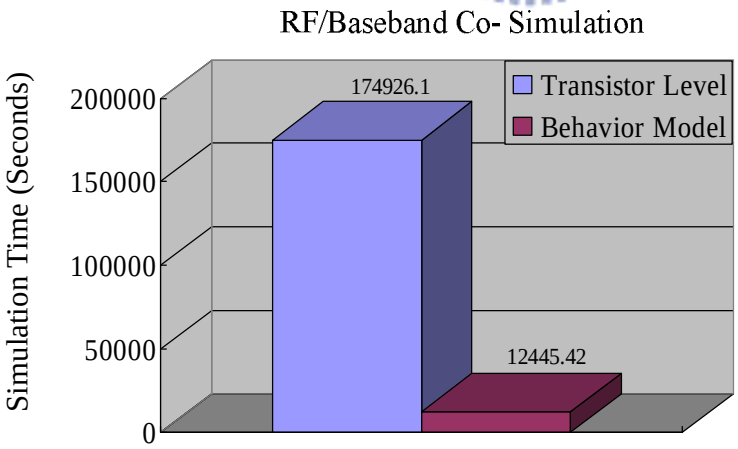


Figure 4.17 Comparisons of simulation time of RF/Baseband simulation.

Chapter 5

Conclusions and Future Works

5.1 Conclusions

This thesis presents an on-chip Class-E PA implemented in UMC 0.13-μm CMOS technology. Instead of the RF choke, the proposed design uses the finite dc-feed inductor technique for suitable implement in a single chip. In order to obtain higher output power, increasing the supply voltage (V_{DD}) by the cascode topology is successful. The efficiency could be improved by tuning out the parasitic capacitor between two transistors, M_1 and M_2. The proposed Class-E PA achieves power added efficiency (PAE) of 48.4 % while delivering 21 dBm output power with the input driving power of -3 dBm at 2.5 GHz. In the design band, 2.3 GHz ~ 2.7 GHz, PAE is still above 44 %. The simulation time of RF/Baseband co-simulation could be reduced about 93% by the proposed behavior model.

5.2 Future Works

For the future works, the behavior model of the Class-E PA can be further improved for the RF/Baseband co-simulation. And it also can be used in investigating

the effect of the loading network of the Class-E PA on polar transmitter to try to find out what kind of loading network of Class-E PA is suitable for polar transmitter.

Appendix 1

Analysis of Ideal Class-E PA with Finite DC-Feed Inductor

In [22], one of the first attempts was made to study finite dc-feed inductor. Some other relevant papers include [23] [24]. All these papers have something in common, the procedure of obtaining final circuit component values is either long, complex and iterative, and doesn't provide a direct insight into the circuit design, or is too simplistic and not exactly. Practically, the design of the Class-E PA with finite dc-feed inductor is a transcendent problem from the mathematical point of view. Therefore, the designer needs to iteratively figure out the system of equations for a certain set of input parameters to gain the final circuit component values. If any of the input parameters is changed, the calculation must be repeated from the beginning. Thus, it is a tedious and extremely impractical procedure. The [8] propose another approach to this problem. The system of transcendent equations is numerically solved for a certain number of discrete points of an input parameter, and the obtained results are interpolated by the Lagrange polynomial. The polynomial interpolation provides adequate accuracy and can be used for any value of the input parameter on that

segment, if it performs with enough density of points on the segment of interest. In other words, it obtains clear and directly usable design equations for the Class-E PA.

The design parameters of the Class-E PA have presented in equations (1.1), (1.2) and (1.3). These equations are base on the L_{ck} is RF choke. But in case of the Class-E PA with finite dc-feed inductor, these equations don't hold anymore [8]. At the beginning of the design procedure, the designer could choose a value of inductance that he would like to use for the finite dc-feed inductor. Therefore, the reactance of this inductor is known, and it is given by

$$X_{dc} = wL_{ck} \qquad \text{(A.1)}$$

On the other hand, an ideal Class-E PA provides a 100% DC-to-RF efficiency. Therefore, the DC resistance that the circuit presents to the supply source is also known from the PA specifications, and is simply given as

$$R_{dc} = \frac{V_{dd}^2}{P_{out}} \qquad \text{(A.2)}$$

Depending on the X_{dc}/R_{dc} ratio, the circuit parameters R, B and X will change their value from those given in equations (1.1), (1.2) and (1.3) for the RF choke based Class-E PA. These three parameters have calculated by numerically solving the transcendent circuit equations for a number of different values of X_{dc}/R_{dc} ratio. The results of these calculations are given in Table A.1 [8].

X_{dc}/R_{dc}	$P_{o\ t}R/V_{dc}^2$	BR	X/R
∞(RFC)	0.5768	0.1836	1.152
1000	0.5774	0.1839	1.151
500	0.5781	0.1843	1.150
200	0.5801	0.1852	1.147
100	0.5834	0.1867	1.141
50	0.5901	0.1899	1.130
20	0.6106	0.1999	1.096
15	0.6227	0.2056	1.077
10	0.647	0.2175	1.039
5	0.7263	0.2573	0.9251
3	0.8461	0.3201	0.7726
2	1.013	0.4142	0.5809
1	1.363	0.6839	0.0007

Table A.1 Class-E PA elements as function of the X_{dc}/R_{dc} ratio [8].

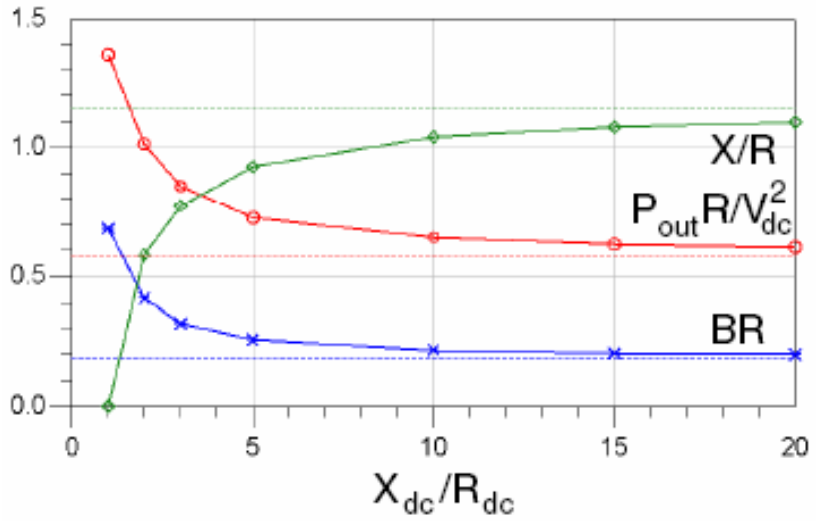


Figure A.1 Effect of the finite DC-feed inductor on the Class-E PA elements [8].

In order to obtain explicit design equations for the Class-E PA component values, [8] have used the Lagrange polynomial interpolation of the numerically obtained results. Finally, the new equations for Class-E power amplifier with finite dc-feed inductor are presented in the following equations.

If $1 < X_{dc}/R_{dc} \ (= z) < 5$,

$$R = \frac{V_{dc}^2}{P_{out}}(1.979 - 0.7783z + 0.1754z^2 - 0.01397z^3) \quad \text{(A.3)}$$

$$B = \frac{1}{R}(1.229 - 0.7171z + 0.1881z^2 - 0.01672z^3) \quad \text{(A.4)}$$

$$X = R(-1.202 + 1.591z - 0.4279z^2 + 0.03894z^3) \quad \text{(A.5)}$$

If $5 < X_{dc}/R_{dc} \ (= z) < 20$,

$$R = \frac{V_{dc}^2}{P_{out}}(0.9034 - 0.04805z + 0.002812z^2 - 5.707 \cdot 10^{-5} z^3) \quad \text{(A.6)}$$

$$B = \frac{1}{R}(0.3467 - 0.02429z + 0.001426z^2 - 2.893 \cdot 10^{-5} z^3) \quad \text{(A.7)}$$

$$X = R(0.6784 + 0.006641z - 0.003794z^2 + 7.587 \cdot 10^{-5} z^3) \quad \text{(A.8)}$$

Design equations (A.3)~(A.8) are explicit, relatively simple and can be used for any value of $z = X_{dc}/R_{dc}$ within the corresponding segment. But outside these segments, they are not valid.

The utilization of a finite dc-feed inductor has several major benefits. First, it results in a higher load resistance in comparison to the case of RF choke. This effect makes the design of low-loss matching networks easier, since the designer typically needs to transform a standard 50 Ohm termination to the load resistance of several

Ohms. Furthermore, the excessive inductance X is also lower, and the shunt susceptance B is increased. This increase of the shunt susceptance is particularly useful, as it extends the maximum frequency limitation of the device imposed by its output capacitance.

Appendix 2

Behavior Model of Switched-Mode Transistor

- Step 1 – Ideal switch in ADS

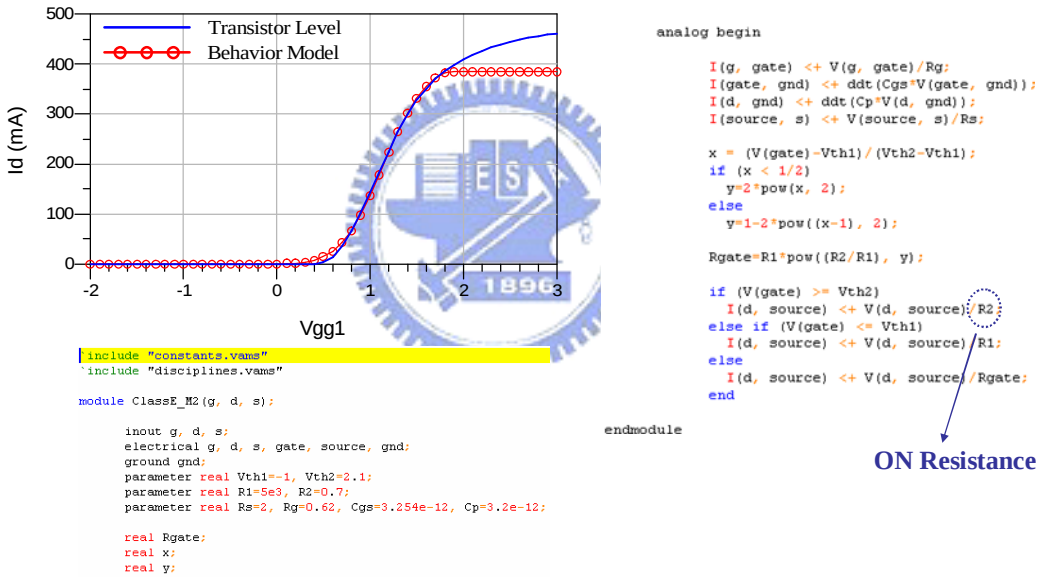
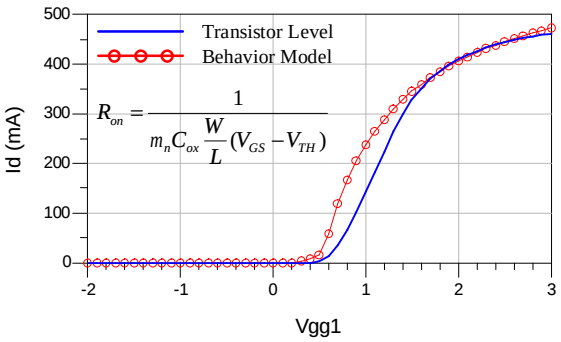


Figure A.2 Simulation results and Verilog-A code of step 1.

- Step 2 – Modify ON resistance at region of 0.3(V) < V_{gg1} < 0.8(V),

  where V_{gg1} is V_{bias1}

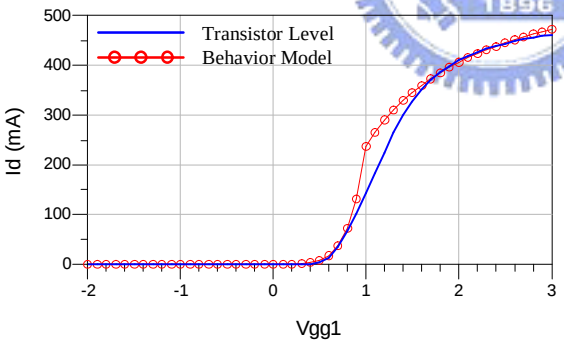



```
`include "constants.vams"
`include "disciplines.vams"

module ClassE_M5(g, d, s);

      inout g, d, s;
      electrical g, d, s, gate, source, gnd;
      ground gnd;
      parameter real Vth1=-1, Vth2=2.1;
      parameter real R1=5e3, R2=0.7;
      parameter real Rs=2, Rg=0.62, Cgs=3.254e-12, Cp=3.2e-12;
      parameter real uCox=200e-6, Vth=0.52, W=2014e-6, L=0.34e-6;
      parameter real Vth_low=0, Vth_high=1;

      real Rgate, Ron;
      real x;
      real y;

      analog begin
```

```
      I(g, gate) <+ V(g, gate)/Rg;
      I(gate, gnd) <+ ddt(Cgs*V(gate, gnd));
      I(d, gnd) <+ ddt(Cp*V(d, gnd));
      I(source, s) <+ V(source, s)/Rs;

      Ron=1/(uCox*(W/L)*(V(gate)-Vth));

      x = (V(gate)-Vth1)/(Vth2-Vth1);
      if (x < 1/2)
        y=2*pow(x, 2);
      else
        y=1-2*pow((x-1), 2);

      Rgate=R1*pow((R2/R1), y);

      if (V(gate) >= Vth_high)
        I(d, source) <+ V(d, source)/Ron;
      else if (V(gate) <= Vth_low)
        I(d, source) <+ V(d, source)/R1;
      else
        I(d, source) <+ V(d, source)/Rgate;
    end
endmodule
```

Figure A.3 Simulation results and Verilog-A code of step 2.

- Step 3 –Modify ON resistance at region of $V_{gg1} > 1.8$(V), where V_{gg1} is V_{bias1}

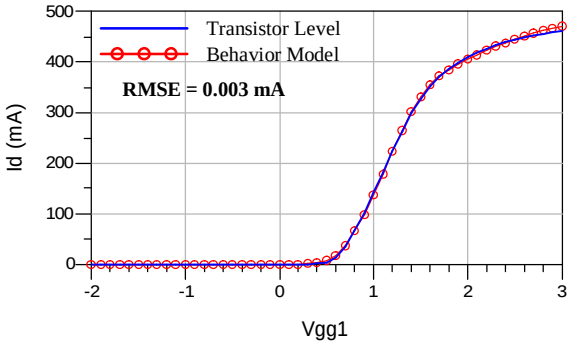



```
`include "constants.vams"
`include "disciplines.vams"

module ClassE_M5(g, d, s);

      inout g, d, s;
      electrical g, d, s, gate, source, gnd;
      ground gnd;
      parameter real Vth1=-1, Vth2=2.1;
      parameter real R1=5e3, R2=0.7;
      parameter real Rs=2, Rg=0.62, Cgs=3.254e-12, Cp=3.2e-12;
      parameter real uCox=200e-6, Vth=0.52, W=2014e-6, L=0.34e-6;
      parameter real Vth_low=0, Vth_high=1;

      real Rgate, Ron;
      real x;
      real y;

      analog begin
```

```
      I(g, gate) <+ V(g, gate)/Rg;
      I(gate, gnd) <+ ddt(Cgs*V(gate, gnd));
      I(d, gnd) <+ ddt(Cp*V(d, gnd));
      I(source, s) <+ V(source, s)/Rs;

      Ron=1/(uCox*(W/L)*(V(gate)-Vth));

      x = (V(gate)-Vth1)/(Vth2-Vth1);
      if (x < 1/2)
        y=2*pow(x, 2);
      else
        y=1-2*pow((x-1), 2);

      Rgate=R1*pow((R2/R1), y);

      if (V(gate) >= Vth_high)
        I(d, source) <+ V(d, source)/Ron;
      else if (V(gate) <= Vth_low)
        I(d, source) <+ V(d, source)/R1;
      else
        I(d, source) <+ V(d, source)/Rgate;
    end
endmodule
```

Figure A.4 Simulation results and Verilog-A code of step 3.

• Step 4 – Combine step 1, step 2 and step 3




```
`include "constants.vams"
`include "disciplines.vams"

module ClassE_M4(g, d, s);

      inout g, d, s;
      electrical g, d, s, gate, source, gnd;
      ground gnd;
      parameter real Vth1=-1.4, Vth2=2.1, Vth1_mid=-1, Vth2_mid=1.9;
      parameter real R1=6e6, R2=0.1, R1_mid=12e3, R2_mid=1.05;
      parameter real Rs=0.1, Rg=0.62, Cgs=3.254e-12, Cp=3.2e-12;
      parameter real uCox=130e-6, Vth=0.524, W=2014e-6, L=0.34e-6;
      parameter real Vth_low=0.3, Vth_mid=0.8, Vth_high=1.8;

      real Rgate, Rgate_mid, Ron;
      real x, x_mid;
      real y, y_mid;
```

```
analog begin

      I(g, gate) <+ V(g, gate)/Rg;
      I(gate, gnd) <+ ddt(Cgs*V(gate, gnd));
      I(d, gnd) <+ ddt(Cp*V(d, gnd));
      I(source, s) <+ V(source, s)/Rs;

      Ron=1/(uCox*(W/L)*(V(gate)-Vth));

      x = (V(gate)-Vth1)/(Vth2-Vth1);
      if (x < 1/2)
        y=2*pow(x, 2);
      else
        y=1-2*pow((x-1), 2);

      Rgate=R1*pow((R2/R1), y);

      x_mid = (V(gate)-Vth1_mid)/(Vth2_mid-Vth1_mid);
      if (x_mid < 1/2)
        y_mid=2*pow(x_mid, 2);
      else
        y_mid=1-2*pow((x_mid-1), 2);

      Rgate_mid=R1_mid*pow((R2_mid/R1_mid), y_mid);

      if (V(gate) <= Vth_low)
        I(d, source) <+ V(d, source)/R1;
      else if (V(gate) <= Vth_mid)
        I(d, source) <+ V(d, source)/Rgate;
      else if (V(gate) <= Vth_high)
        I(d, source) <+ V(d, source)/Rgate_mid;
      else
        I(d, source) <+ V(d, source)/Ron;
      end
endmodule
```

Figure A.5 Simulation results and Verilog-A code of step 4.

Bibliography

[1] Thomas H. LEE, “The Design of CMOS Radio-Frequency Integrated Circuits,” second edition, Cambridge University Press 1998.

[2] Frederick H. Rabb, Peter Asbeck, Steve Cripps, Peter B. Kenington, Zoya B. Popovich, Nick Pothecary, John F. Sevic and Nathan O. Sokal, “RF and Microwave Power Amplifier and Transmitter Technologies – Part 2,” High Frequency Electronics, May 2003.

[3] Mazzanti, A.; Larcher, L.; Brama, R.; Svelto, F., ”Analysis of Reliability and Power Efficiency in Cascode Class-E PAs,” Solid-State Circuits, IEEE Journal of Volume 41, Issue 5, May 2006 Page(s):1222 – 1229

[4] N.O Sokal and A.D. Sokal, “Class E-A new class of high-efficiency tuned single-ended switching power amplifiers,” IEEE, JSSC, vol. SC-10, pp. 168-176, June 1975.

[5] FREDERICK H. REBB, “Idealized Operation of the Class E Tuned Power Amplifier,” IEEE, Transactions on Circuits and Systems, Vol. 24, pp. 725-735, Dec. 1977.

[6] Mihai Albulet, “RF Power Amplifiers,” Noble Publishing Corporation, 2001.

[7] Raab, F. H. “Effects of Circuit Variations on the Class E Tuned Power Amplifier,” IEEE JSSC, vol. SC-13 (April 1978): 239-247.

[8] D. Milosevic, J. van der Tang and A. van Roermund, “Explicit Design Equations for Class-E Power Amplifiers with Small DC-feed Inductance,” Circuit Theory and Design, 2005. Proceedings of the 2005 European Conference on Volume 3, 28 Aug.-2 Sept. 2005 Page(s):III/101 - III/104 vol. 3

[9] C. Yoo and Q. Huang, “A Common-Gate Switched 0.9-W Class-E Power Amplifier with 41% PAE in 0.25- μ m CMOS,” JSSC, vol. 36, no. 5, May 2001.

[10] B. Razavi, “RF Microelectronic,” NJ, USA: Prentice-Hall PTR, 1998.

[11] L. R. Kahn, “Single-Sideband Transmission by Envelope Elimination and

Restoration," Proc. IRE, Vol.40, pp. 803-806, July 1952.

[12] D. Su and W. Sander, "An IC for Linearizing RF Power Amplifiers Using Envelope Elimination and Restoration," IEEE JSSC, Vol. 31, pp. 2252-2258, Dec. 1998.

[13] H. L. Kraus, C. W. Bostian, and F. H. Raab, "Solid State Radio Engineering," John Wiley & Sons, Inc., 1980.

[14] Nagle, P.; Burton, P.; Heaney, E.; McGrath, F.; "A Wide-Band Linear Amplitude Modulator for Polar Transmitter Based on the Conpect of Interleaving Delta Modulation," Solid-State Circuits, IEEE Journal of Vol. 37, Issue 12, Dec.2002 Page(s):1748-1756.

[15] C.C. Ho, C.W. Kuo, C.C. Hsiao, Y.J. Chan, "A Fully Integrated Class-E CMOS Amplifier with a Class-F Driver Stage," IEEE RFIC Symposium, June 2003.

[16] P. Luengvongsakorn, A. Thanachayanon, "A 0.1-W CMOS class-E power amplifier for Bluetooth applications," Digital Object Identifier, Page(s): 1348-1351 Vol.4, TENCON 2003.

[17] H.S. Oh, T. Song, E. Yoon, C.K. Kim, "A Power-Efficient Injection-Locked Class-E Power Amplifier for Wireless Sensor Network," IEEE Microwave and Wireless Components Letters, vol. 16, no. 4, April 2006.

[18] Munir M. El-Desouki, M. Jamal Deen and Yaser M. Haddara, "A Low-Power CMOS Class-E Power Amplifier for Biotelemetry Applications," Microwave Conference, 2005 Oct. European

[19] UMC Design Kits document, L130E_HS12_V241.pdf

[20] C. D. Hung, W. S. Wuen, Mei-Fen Chou, and Kuei-Ann Wen, "A Unified Behavior Model of Low Noise Amplifier for System-Level Simulation," accepted by European Conference on Wireless Technology (ECWT 2006), Manchester, UK, Sep. 2006.

[21] UMC Design Kits document, L130E RFCMOS model v1.3p1.pdf

[22] R.E. Zulinski and J.W. Steadman, “Class E Power Amplifiers and Frequency Multipliers with Finite DC-Feed Inductance,” IEEE Trans. Circuits and Systems, vol. CAS-34, no. 9, pp. 1074-1087, September 1987.

[23] D.K. Choi and S.I. Long, “Finite DC Feed Inductor in Class E Power Amplifiers-A Simplified Approach,” 2002 IEEE MTT-S Microwave Symposium Digest, vol. 3, pp. 1643-1646, June 2002.

[24] M. Iwadare and S. Mori, K. Ikeda, “Even Harmonic Resonant Class E Tuned Power Amplifier without RF choke,” Electronics and Communications in Japan, Part 1. vol.79, no. 1, 1996.

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論文題目 ： RF CMOS Class-E Power Amplifier Design

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