國　立　交　通　大　學

電子工程學系　　電子研究所碩士班

碩 士 論 文

一個九位元,每秒八十百萬次取樣
低功率管線式類比數位轉換器

A 9bit, 80MS/s Low Power
Pipelined Analog to Digital Converter

研 究 生：賴宗裕

指導教授：陳巍仁　教授

中 華 民 國 九十六 年 十二 月

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Submitted to Department of Computer and Information Science

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for the Degree of

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in

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摘　　要

管線式類比數位轉換器具有高速及中高解析度的特性,因此為可攜式電子產品中經常使用之架構。其可藉由低電壓及功率最佳化設計，降低電路整體功率消耗。然而，在低電壓的操作環境下, 由於信號的動態範圍減少, 電路的非理想效應會進一步劣化管線式類比數位轉換器的性能,包含飄移電壓、運算放大器的非線性增益及電容的不匹配等效應造成之增益誤差。至今，文獻上有許多校正電路技術發表, 其可藉由離線或背景補償等方式, 提升轉換器電路之性能。

本論文提出一個 1 伏特, 9 位元之管線式類比數位轉換器。 為改善低電壓操做運算放大器之增益與頻寬, 本論文提出轉導分離式運算放大器電路, 其在相同之功率消耗與單位增益頻寬之下, 可提升增益達 10 dB。此外, 為克服低電壓操做運算放大器之有限增益效應, 本架構內含運算放大器及倍乘數位類比轉換器(M-DAC) 之增益萃取電路, 本論文並提出偏移誤差補償方法, 以大達幅提高運算放大器增益萃取之準確性, 藉由離線補償可提升整體轉換器之有效位元數達 2 位元。

本實驗晶片以 0.18μm CMOS 製程實作完成, 晶片面積為 1.45×1.55 mm^2。本電路採用雙重取樣技術以提升運算放大器之使用效率, 同時倍增取樣率, 其轉換率可達每秒八十百萬次取樣。量測結果顯示其微分和積分非線性誤差(Differential and Integral Nonlinearity)分別為+1.1/-0.8LSB和+1.3/-1.3LSB。 本轉換器之核心電路皆操作在 1 伏特工作電壓, 整體功率消耗為 11.5mW， 其 FOM值達 0.88pJ/conversion。

A 9bit, 80MS/s Low Power Pipelined Analog to Digital Converter

student：Tsung-Yu Lai　　Advisors：Wei-Zen Chen

Department of Electronics Engineering National Chiao Tung University

ABSTRACT

Pipelined ADCs are widely applied in portable electronic devices thanks to its features of high speed operation and medium to high resolution in data conversion. Its power dissipation can be further reduced by applying low voltage and power scaling techniques. However, the dynamic range of the input signal is severely limited under a low supply voltage. The non-idealities of the data converter, such as offset voltage and gain error caused by OP gain nonlinearities and capacitor mismatches, will further degrade its overall performance. Nowadays, several calibration techniques have been proposed in the literature. The performance of the data converter can be enhanced by means of off-line or background calibrations.

This thesis proposes a 1 V, 9bits pipelined ADC. In order to improve the gain bandwidth performance of the operational amplifier under a low supply voltage, a novel OPAMP with split transconductance input stage is proposed. It can boost the conversion gain by 10dB under a given current consumption and without degrading its unity-gain bandwidth performance. Besides, in order to eliminate the OP finite gain effect under a 1 V supply, on-chip calibration circuits are incorporated to extract the conversion gain of the OP and MDAC. Furthermore, input offset cancellation techniques are proposed to improve the accuracy of the calibration circuits. The effective number of bits (ENOB) of the data converter can be improved by 2 bits by applying offline calibration.

The experimental prototype has been fabricated in a 0.18μm CMOS technology, the chip size is $1.55\times1.45mm^2$. Double-sampling technique is applied to improve the power efficiency of the

OPAMs as well as double the conversion rate. Experimental results reveal that the DNL and INL are +1.1/-0.8LSB and +1.3/-1.3LSB respectively at 80 MS/s. All the core circuits are operated under a 1 V supply, and the total power consumption is 11.5 mW. The corresponding FOM (Figure of Merit) is 0.88pJ/conversion.

誌　　謝

碩士班二年多來，我對於自己的成長感到滿意。很感謝陳巍仁老師的指導，也謝謝 307 及 319 實驗室所給予的資源，使我在學術上有十足的進步。當然，除了學術外，謝謝二位在當兵的室友，也很謝謝在交大所認識的朋友們，包括 307 曾經指導過我的學長、527 一起打拚的同學、520 一群歡笑的學弟們，很抱歉沒有細數你們的名字，但真的由衷感謝你們讓我有這麼快樂的回憶。松諭、巧伶及黃董，請你們繼續努力，相信你們以後一定成就非凡，祝福你們！

最後，謝謝女友、老爸、老媽，謝謝老天爺，我畢業了！

賴宗裕　2008,1,3

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INTRODUCTION

1.1 Motivation

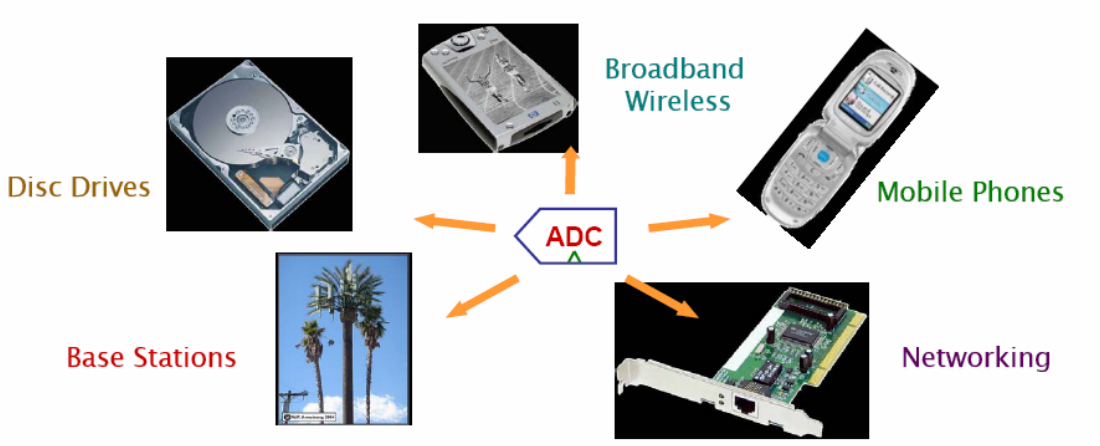


Figure 1.1 Applications of analog to digital converters

Many of the communication systems today utilize the digital signal processing to resolve the transmitted information. Therefore, between the received analog signal and the DSP system, an analog-to-digital interface is required. This interface achieves the digitization of the received waveform subject to a sampling rate requirement of the system. Being a part of communication system, the A/D interface also needs to adhere to the low power constraint. Figure 1.2[1] shows the surveys of ADC from 1999 to 2006. The figure-of-merit (FOM) is expressed as

$$FOM = \frac{Power}{2^{ENOB} \times Conversion\ rate} \tag{1.1}$$

where ENOB means effective number of bit. State-of-the-Art for ADC design is approximately 1-picoJoule per conversion step.

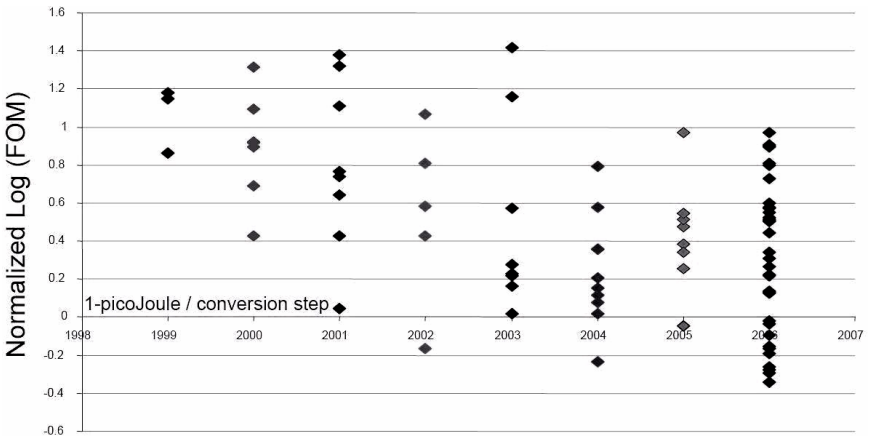


Figure 1.2 Survey of ADC Figure-of-Merit 1999-2006

Among many types of CMOS ADC architectures, a pipelined architecture can achieve good high input frequency dynamic performances and as a high throughput. Low-power small-area ADCs with 10bit resolution and several tens of MS/s sampling rate are considered to be one of the significant components in battery-operated commercial applications including data communication and image signal-processing systems.

In this research, it is expected to suppress the power consumption so as to use 1.0 V power supply in analog circuit. A 9-bit 80MS/s pipelined A/D converter with off-line calibration has been designed and implemented with standard TSMC 0.18μm CMOS 1P6M process.

1.2 Thesis Organization

This thesis is organized into six chapters. In Chapter 1, this thesis is briefly introduced. Chapter 2 begins with the concepts of analog-to-digital conversion and performance metrics used to characterize ADCs. Then, the architecture of pipelined ADC is reviewed. The pipelined architecture is described in detail from its basic operation to the actual implementation of each pipelined stage. The 1.5-bit architecture with accuracy and speed requirement are pointed out. The affection of gain error in low voltage ADC and calibration

technique are also discussed in detail. Finally, the behavioral level simulations of a pipelined ADC are built by MATLAB so as to obtain the specification of design.

Chapter 3 describes the design issues of each block. The key circuit blocks used in the low-voltage ADC is presented. Among them are the proposed operational amplifier, the dynamic common mode feedback, the comparator, the FADAC and the clock generator. Then, transistor level simulated results of each circuit are shown.

Chapter 4 describes the calibration circuit which is constructed by SAR (Successive Approximation) architecture. The goal is to calculate the gain error in pipelined ADC which is described in chapter 3. By the output digital code, off-line calibration can boost the efficiency of pipelined ADC.

Chapter 5 shows the experimental results, including the chip layout, system simulation result, and measurement consideration. Following the experimental test results for the low-voltage pipelined ADC described in Chapter 3 and Chapter 4 and fabricated in a standard TSMC 0.18μm CMOS technology are summarized.

The conclusions of this work are summarized in Chapter 6. Following additional areas of researches are suggested and recommendations for the future work.

CHAPTER 2

NYQUIST RATE DATA CONVERTER

2.1 Introduction

In this chapter, the first describes the concept of analog to digital conversions and discusses performance metrics to characterize ADCs. The second reviews some analog-to-digital converter (ADC) architectures, including flash ADC, cyclic ADC, and pipelined ADC. The fundamental issues in this design will be reviewed. Among them we focus on Nyquist rate pipelined ADC architecture. The third focuses on key building blocks in pipelined analog-to-digital converters. The specification of constraints and several techniques including of double sampling and power optimization are discussed. At the end of the chapter, the behavior model of pipelined analog-to-digital converter is built by MATLAB.

2.2 ADC Performance Metrics

The ADC converts the analog signal to digital domain. The ADC divides the continuous analog signal into several subranges. The size of each of the subranges is often referred to as the step size. These steps are usually uniform in size, but not always. During the conversion process, the ADC decides the input signal level in which subrange and sends the appropriate digital code to the output. Analog-to-digital converters are characterized in a number of different ways to indicate the performance efficiency, including resolution, SNR, SNDR, dynamic range, INL and DNL.

2.2.1 Resolution

Resolution describes the fineness of the quantization performed by the ADC. It is also named as effective number of bits (ENOB). A high resolution ADC means the input range can

be divided into a larger number of subranges than a low resolution ADC. In general cases, resolution is defined as the base 2 logarithm of subranges, and is usually affected by either noise or nonlinearity. Therefore, SNR, INL and DNL are applied to characterize the performance in noise and nonlinearity.

2.2.2 Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio of signal power to noise power in the output of the ADC. In Figure 2.1(a), the transfer characteristic curve is shown. The use of quantization introduces an error, quantization error, defined as the difference between the dash line and the output signal. Figure 2.1(b) shows the quantization error range is between $+\Delta$ and $-\Delta$.

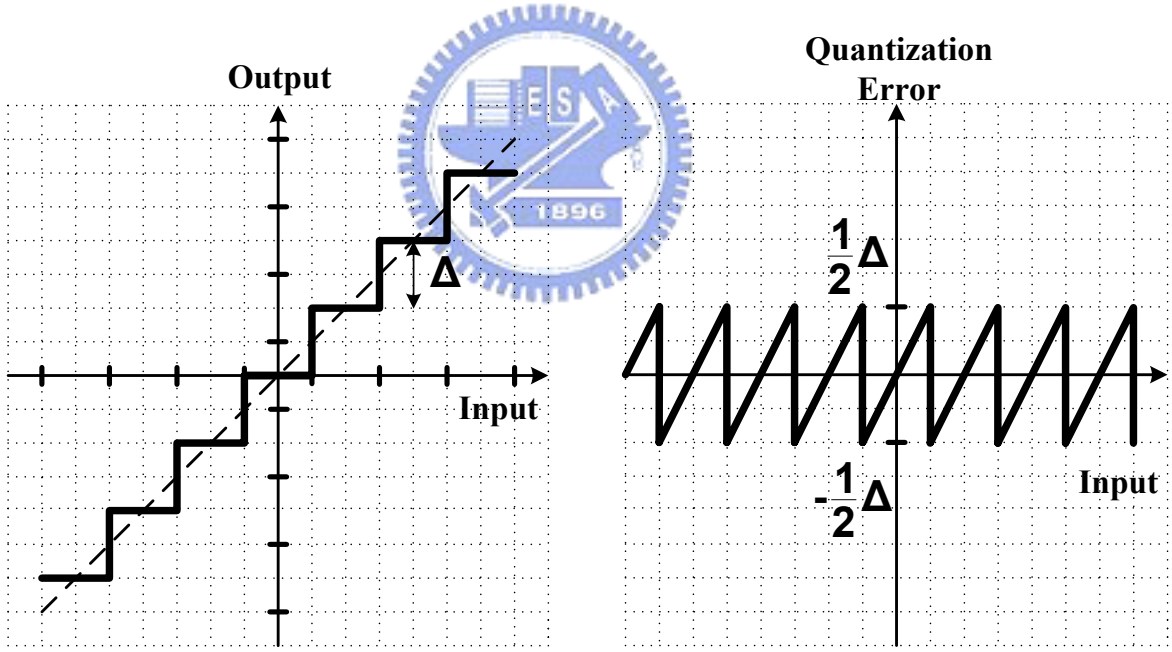


Figure 2.1 (a) Transfer characteristic curve (b) Quantization error

As figure 2.2(a) shows, the quantizer can be model as input signal added by quantization error. The symbol Δ presents the value of 1LSB. By assumption, the quantization

error is defined as a uniformly distributed random variable and the interfering effect on the quantizer input is similar to that of thermal noise. The probability density function for such an error signal will be a constant value and is independent of the sampling frequency, fs, and input signal, as the Figure 2.2(b) shows. The distribution of the quantization error is expressed as Equation (2.1).

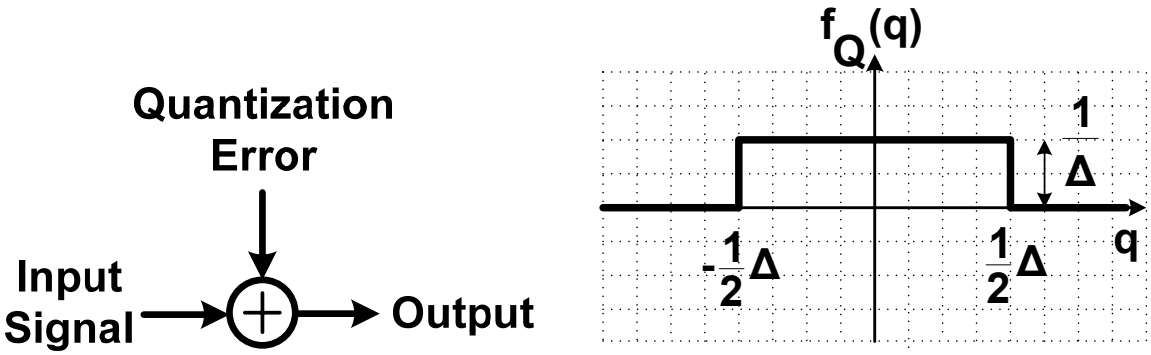


Figure 2.2 (a) Quantizer model

(b) The probability density function of the quantization error

$$f_Q(q) = \begin{cases} \frac{1}{\Delta}, & -\frac{\Delta}{2} < q < \frac{\Delta}{2} \\ 0, & otherwise \end{cases} \qquad (2.1)$$

Hence, the R.M.S. value of the quantization error is

$$V_{Q,rms}^2(q) = \frac{1}{\Delta}\int_{-\frac{1}{2}\Delta}^{\frac{1}{2}\Delta} q^2 dq = \frac{\Delta^2}{12} \qquad (2.2)$$

The SNR formula is to assume that V_{IN} is a sinusoidal waveform between $-V_{Swing}$ and V_{Swing}. Thus, the AC R.M.S. value of the sinusoidal wave is

$$V_{IN,rms} = \frac{V_{Swing}}{\sqrt{2}} \qquad (2.3)$$

Let N denote the number of bits used in the construction of the binary code. The Δ_{LSB} has a relationship with V_{ref}.

$$\Delta_{LSB} = \frac{2V_{Swing}}{2^N} \qquad (2.4)$$

Then, the SNR can be derived

$$SNR = 20\log_{10}\left(\frac{V_{IN,rms}}{V_{Q,rms}}\right) = 20\log_{10}\left(\frac{\frac{V_{Swing}}{\sqrt{2}}}{\frac{\Delta}{\sqrt{12}}}\right) = 20\log_{10}\left(\sqrt{\frac{3}{2}}2^{N}\right) \quad (2.5)$$

$$= 6.02N + 1.76\,(dB)$$

By equation (2.5), the simple equation shows the relation between SNR and ADC output bit number. As N increases by one, the SNR specification is added 6dB. For example, 8bit ADC requires at least 50dB. Besides, note that Equation (2.5) gives the best possible SNR for an N-bit ADC.

2.2.3 Spurious Free Dynamic Range (SFDR) and Signal to Noise Distortion Ratio (SNDR)

In ADC measurement, the input signal is usually a sinusoidal input. When a sinusoidal signal of a single frequency is applied to a system, the output of the system generally contains a signal component at the input frequency. Due to distortion, the output also contains signal components at harmonics of the input frequency. Otherwise, quantization error during conversion is also injected to output signal. As the figure 2.3 shows, the output signal consists of three components, input signal, distortion and noise level. The spurious free dynamic range (SFDR) is defined as the ratio of the largest spurious frequency and the fundamental frequency. The signal-to-noise-and-distortion ratio (SNDR) is the ratio of all error energy to signal energy. Quite often the term signal-to-noise ratio is used although SNDR is actually meant.

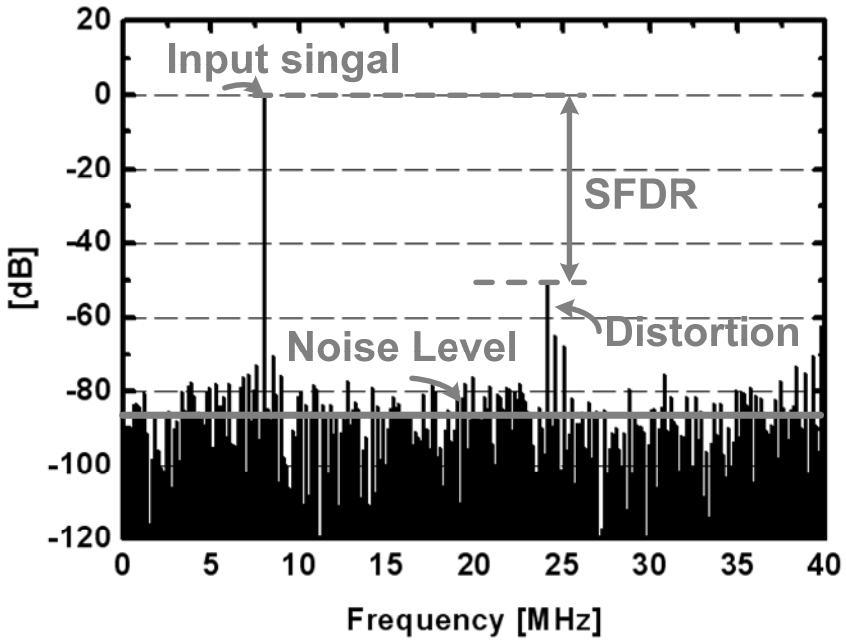


Figure 2.3 Example of frequency domain plot

2.2.4 Dynamic Range(DR)

Dynamic range is another useful performance benchmark. Dynamic range is a measure of the range of input signal amplitudes for which useful output can be obtained from a system. When the signal to noise ratio is 0dB, it means that it is the minimum detectable input signal power. Figure 2.4 illustrates a plot of SNR versus input level. The dynamic range is defined as the ratio of the input signal level for maximum SNR to the input signal level for 0dB SNR. If the noise power is independent of the level of the signal, the dynamic range is equal to the SNR at full scale. However, in some cases the noise power increases as the signal level increases. Therefore, the maximum SNR is less than the dynamic range normally.

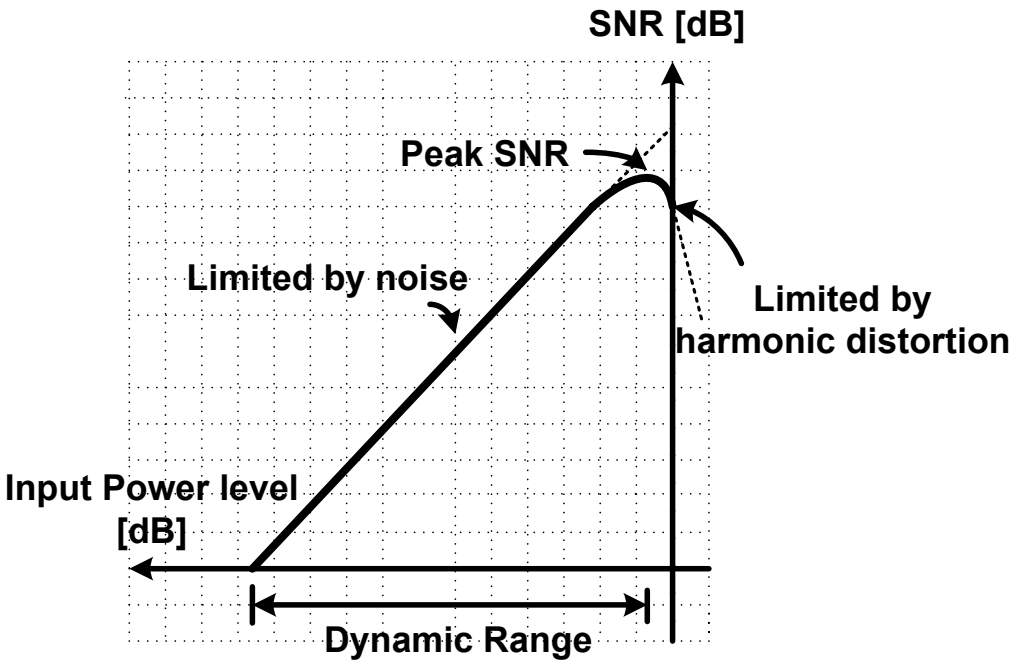


Figure 2.4 SNR versus input level

2.2.5 Imperfections

ADC has a transfer characteristic that approximates a straight line. The transfer characteristic for an ideal version of such an ADC input progresses from low to high in a series of uniform steps. However, the transfer characteristic of a practical ADC has several imperfections. Such non-idealities can be expressed in several ways as showing in Fig 2.5. In figure 2.5(a), the transfer curve all shift by a constant amount which is named offset. It may be caused by offset of operational amplifier but not affect the linearity of ADC. Figure 2.5(b) shows the practical ADC has gain error so the slope is not equal to ideal. The deviation between them comes from insufficient gain of operational amplifier and mismatch by manufacturing. In figure 2.5(c), steps are not perfectly uniform, and this deviation generally contributes to further non-idealities. Linearity error refers to the deviation of the actual threshold levels from their ideal values and is generated by distortion feature of transistor. The excessive linearity error results in missing code.

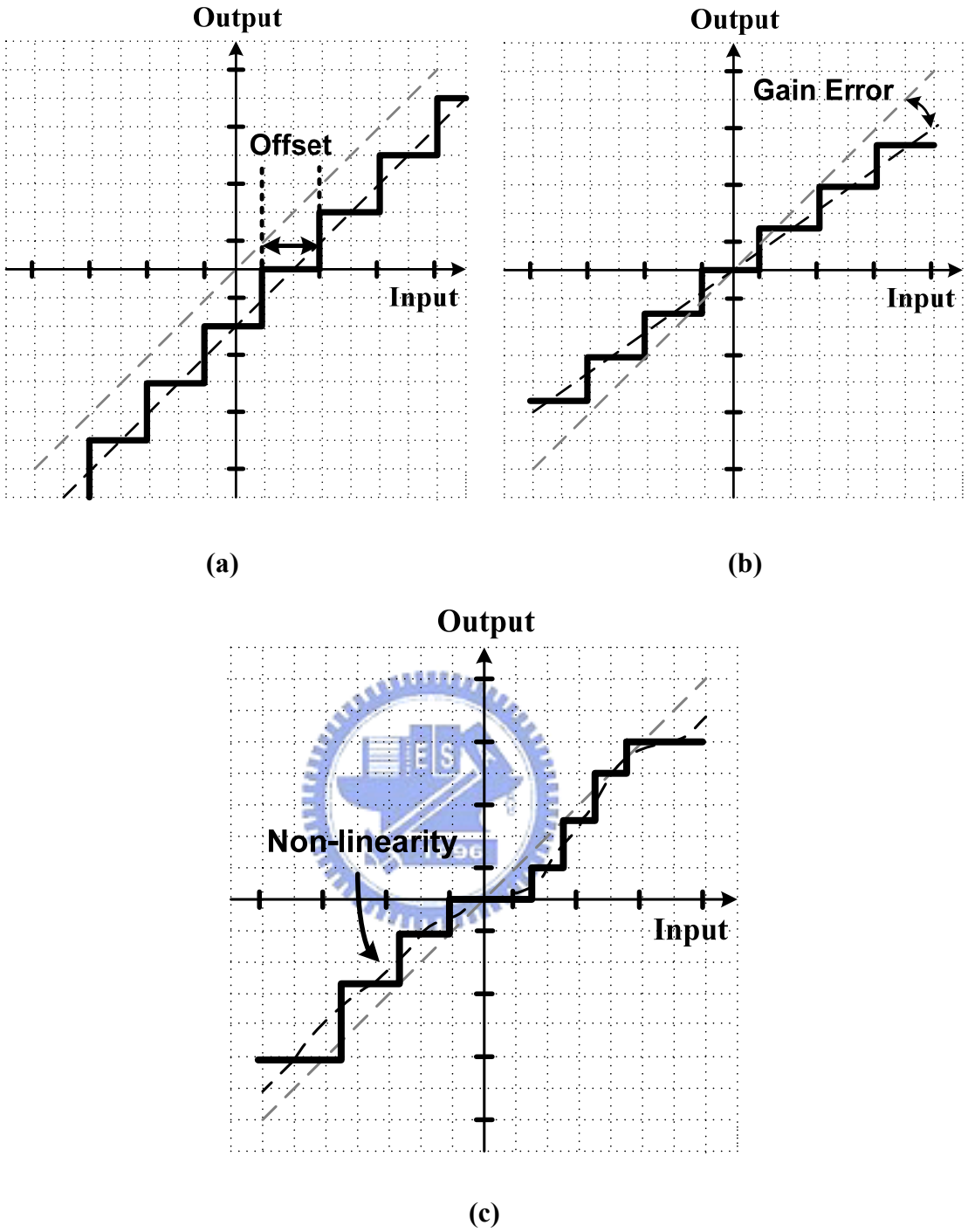


Figure 2.5 Imperfections in ADC (a) Offset (b) Gain error (c) Non-linearity

2.2.6 Differential Non-Linearity (DNL) and Integral Non-Linearity (INL)

Nonlinearity is characterized by INL and DNL admittedly. Differential nonlinearity (DNL) measures how far each of the step sizes deviates from the ideal value of the step size.

Integral nonlinearity (INL) is the difference between the actual transfer characteristic and the straight line characteristic which the ADC is intended to approximate. DNL and INL are both plotted as a function of code. DNL and INL are generally expressed in terms of least significant bit (LSB) of the input. The value of LSB has been shown by equation (2.4) previously. Figure 2.6 illustrates DNL and INL, which can be expressed as Equation (2.7) and Equation (2.8).

$$DNL(D_j) = \frac{S_j - \Delta_{LSB}}{\Delta_{LSB}} \tag{2.7}$$

$$INL(D_j) = \frac{T_j}{\Delta_{LSB}} \tag{2.8}$$

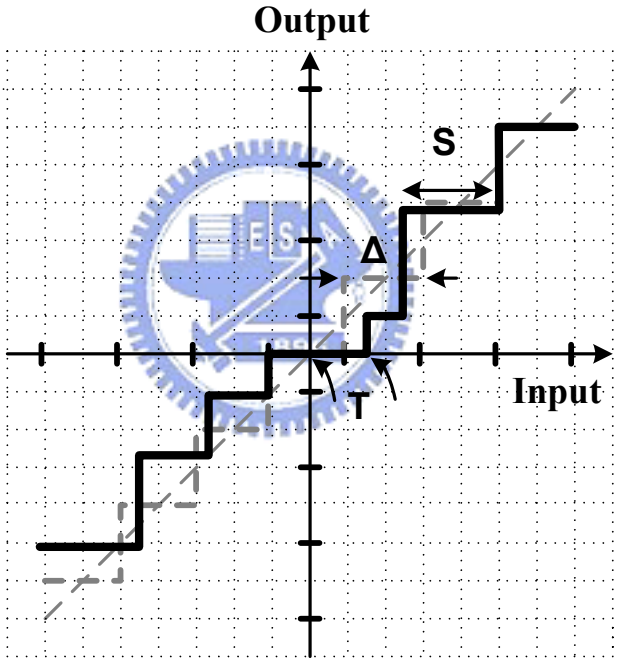


Figure 2.6 DNL and INL

2.3 Review of ADC Architecture

2.3.1 Flash ADC

Flash ADC, which is the fastest and one of the simplest ADC architectures, is shown in Figure 2.7. It performs 2^N-1 level quantization with an equal number of comparators. The

reference voltages for the comparators are generated using a resistor string, which is connected between the positive V_{REF} and the negative $-V_{REF}$ reference voltage determining the full scale signal range. Together the comparator outputs form a $2^N - 1$ bit code, where all the bits below the comparator whose reference is the first to exceed the signal value are ones, while the bits above are all zeros. This so-called thermometer code is converted to *N*-bit binary code with a logic circuit, which can also contain functions for removing bit errors (bubbles).

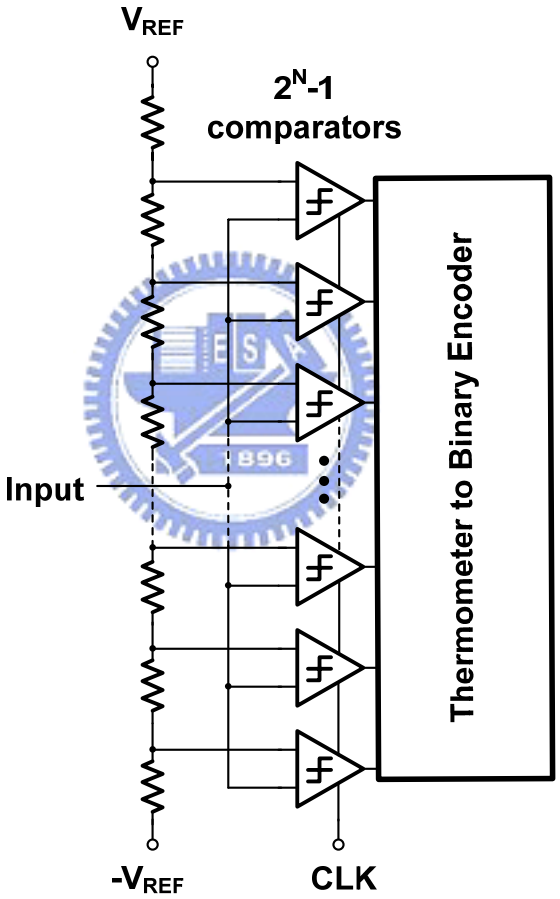


Figure 2.7 Flash ADC architecture

The most prominent drawback of flash ADC is the fact that the number of comparators grows exponentially with the number of bits. Increasing the quantity of the comparators also increases the area of the circuit, as well as the power consumption. And the other

disadvantage is comparator offset sensitivity. At high resolutions, this required comparator offset becomes very small and are difficult to design. Thus, very high resolution flash ADCs are not practical, typical resolutions are seven bits or below.

2.3.2 Cyclic ADC

A cyclic ADC operates the same as a single pipeline stage. With the output feedback to the input, the cyclic ADC converses the data during the next clock cycle. The block diagram is illustrated in Figure 2.8. The stage conversion time from the input sample to complete digital output is the same as for a pipelined ADC. However, the throughput rate is much less than for a pipelined ADC because the entire digital word must be generated after several clock cycles passed. However, a cyclic ADC is much superior in hardware and power because of just one stage is reused repeatedly.

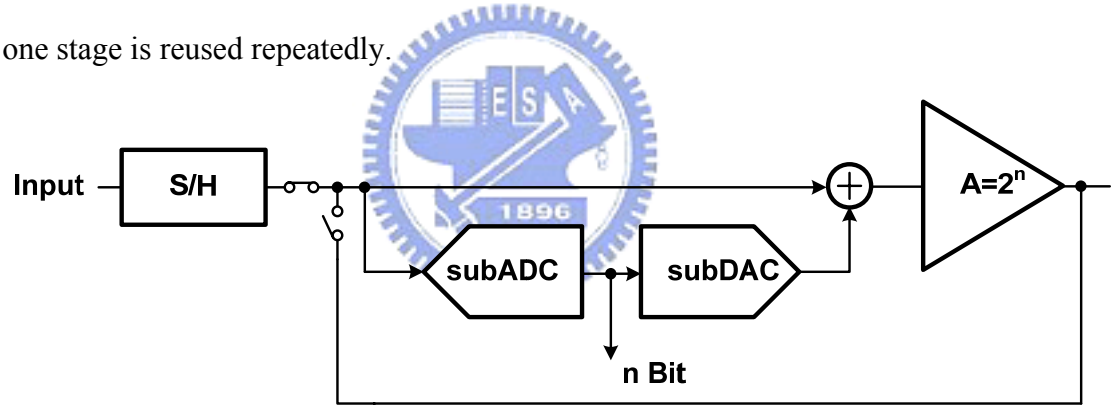


Figure 2.8 Cyclic ADC architecture

2.3.3 Pipelined ADC

The block diagram of a typical pipelined ADC is shown in Figure 2.9. Mostly, the beginning sample and hold relaxes the timing requirements of the first stage during its sampling phase by holding the instantaneous value of the analog input. Following the S/H, it consists of a coarse subADC, coarse subDAC result, subtraction, and amplification of the remainder.

Within each stage, the analog input signal from the last stage is first sampled and held.

The signal is coarsely quantized by a subADC to resolve n bits. Then using a subDAC, the quantized value is subtracted from original input signal to yield the output residue. For the output signal range is the same with the input signal range for each stage, this is made by the amplifier with gain of 2^n. The resulting residue signal is applied to the next stage for finer conversion on the next clock cycle. The function of the D/A, the subtraction, and the amplification of the remainder are combined into one single circuit called the multiplying DAC (MDAC).

Take 1.5bit conversion stage for example. Figure 2.11(a) shows the 1.5bit transfer curve which has three segments and is encoded as 00, 01, and 10. The input range is normally the same as output range. The conversion gain in each part is 2. The two side lines decided by subADC are $1/4V_{REF}$ and $-1/4V_{REF}$.

Now introduce some non-linearity affections, including of comparator offset, amplifier offset, and gain error. As illustrated in figure 2.11(b), comparator offset shifts the sight line by an offset value. Although the offset may lead output swing to over range, 1.5bit architecture has $1/4V_{REF}$ tolerance of comparator offset to overcome. Figure 2.11(c) shows the amplifier offset which moves the whole conversion curve by a value. But for linearity, amplifier offset is inessential. Figure 2.11(d), gain error in subDAC, will cause the slope of transfer curve less than 2 and the output digital code will be missing.

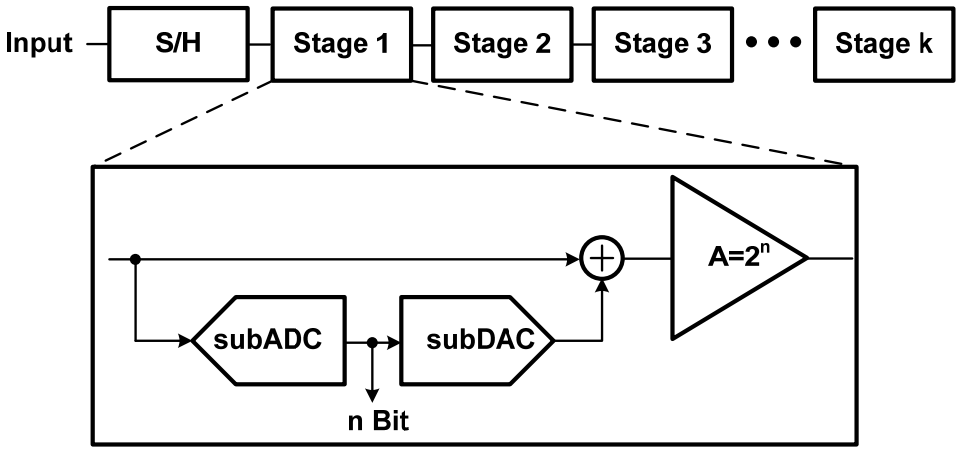


Figure 2.9 Pipelined ADC architecture

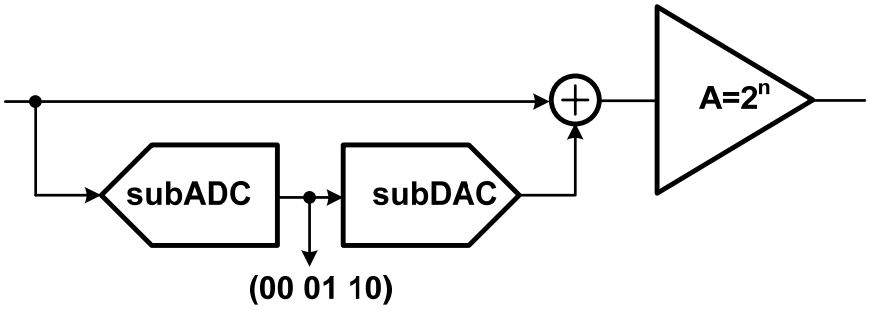


Figure 2.10 Block diagram of radix-2 1.5b pipeline stage

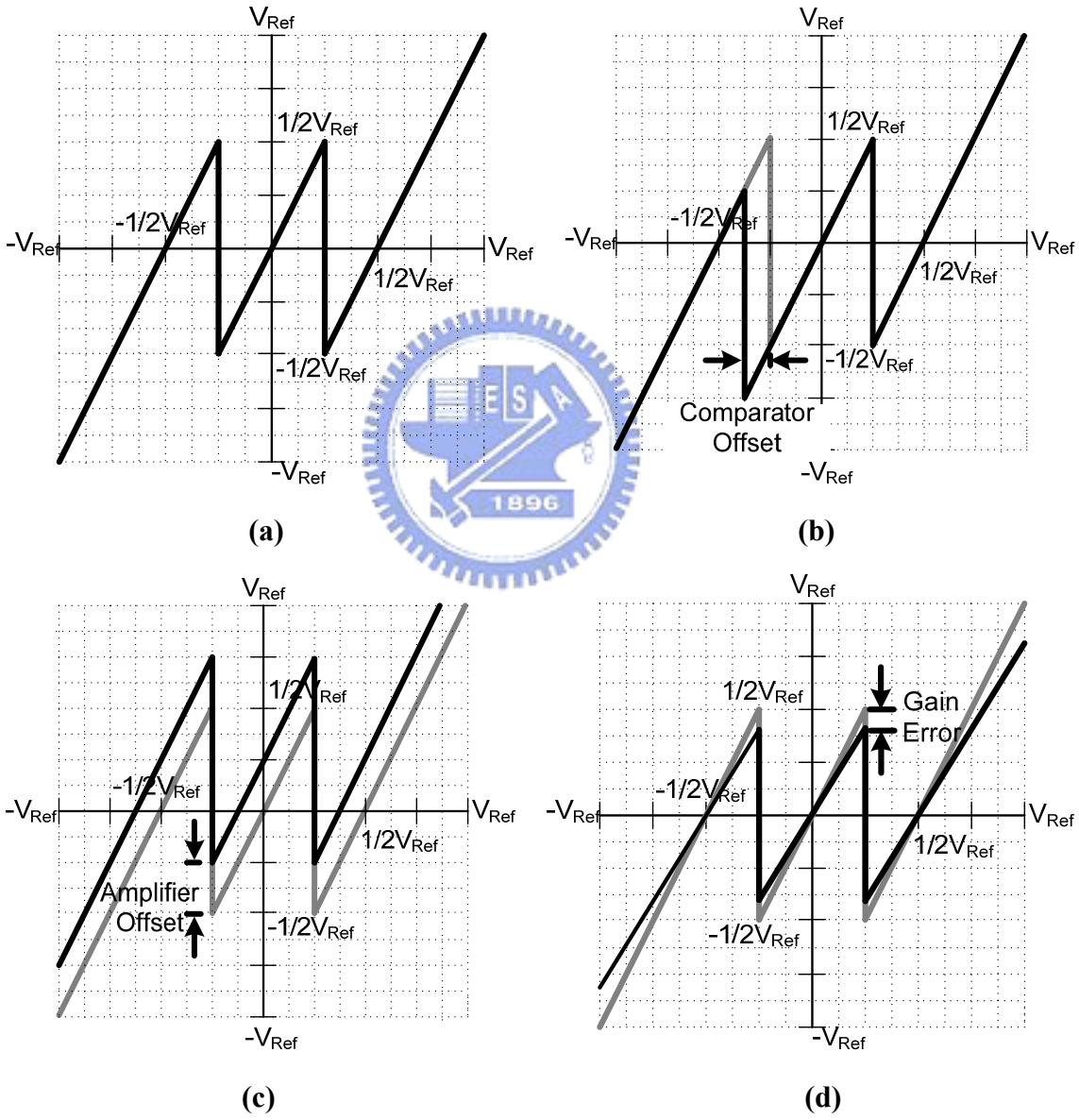


Figure 2.11 (a) Ideal transfer curve (b) With comparator offset

(c) With amplifier offset (d) With gain error

2.4 Design Issue of Pipelined ADC

2.4.1 Stage Accuracy and Speed Requirement

In the pipelined ADC, MDAC in each stage has two main specifications, speed and accuracy requirement. The speed requirement means the operation speed which is related to bandwidth of operational amplifier and feedback factor in MDAC architecture. The accuracy requirement is also affected by feedback factor but the main cause is the open-loop gain of operational amplifier. However, the constraint on each stage is different because the stage resolution decreases as the stage goes lower. Lower stage resolution means that design constraints are more relaxed. Considering the gain requirement becomes looser for later stages, several benefits are obtained if each stage is design specifically, for instance the power consumption and chip area.

General speaking, the way to implement the MDAC function is to use the switch capacitor technique. First of all, because the 1.5bit architecture is applied in this design, we just analyze this one that is shown as figure 2.12. By sampling the input signal on the capacitor and redistribution the signal charge on the capacitor, the output in hold mode is as (2.8). Note that equation ignores the time domain factor which will be discussed latter.

$$V_O = \frac{1 + C_S/C_f}{\left(1 + \frac{\left(C_f + C_S + C_P\right)/C_f}{A}\right)}\left(V_i - \frac{V_{REF}}{1 + C_f/C_S} D_j\right) \tag{2.8}$$

Where C_P is the input loading of opamp, V_{REF} comes from subDAC, and D_j is the output of subADC. Assume C_S and C_f are identical to C and the gain is larger than 1, equation (2.8) can be simplified and approximated as

$$V_O = \frac{2}{\left(1 + \frac{2 + C_P/C}{A}\right)}\left(V_i - \frac{V_{REF}}{2} D_j\right) = 2\left(V_i - \frac{V_{REF}}{2} D_j\right)\left(1 - \frac{2 + C_P/C}{A}\right) \tag{2.9}$$

Equation (2.9) shows that V_O has a gain error term due to A is finite. In order to achieve N-bit

performance, this gain error term should be less than 1LSB of the next stage resolution (z-bit) to prevent any information missing.

$$\frac{2+C_P/C}{A} < \frac{1}{2^Z} \tag{2.10}$$

Therefore, the specification of gain is given by

$$A > (2+C_P/C)2^Z \tag{2.11}$$

Subsequently, the equation of speed requirement for the MDAC's amplifier is derived. By assuming that the MDAC in hold mode is a single pole system and ignoring the slewing behavior, the MDAC settling time constant is

$$\tau = \frac{(2+C_P/C)}{\omega_u} \tag{2.12}$$

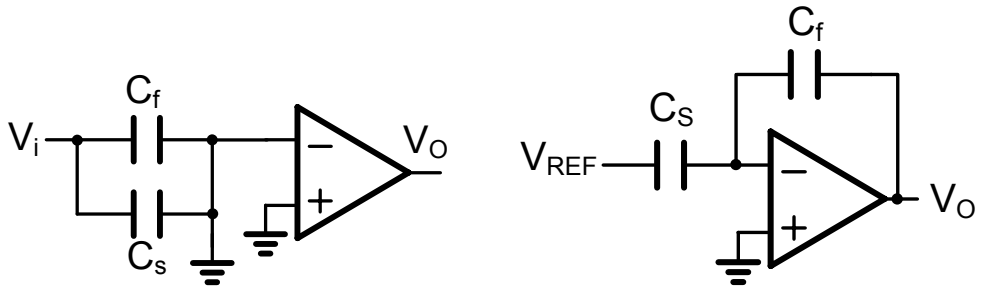
Where ω_u is unity-gain bandwidth of amplifier. Since the setting error of a single pole system is

$$e^{-T_{\phi_2}/\tau} < 2^{-Z} \quad , T_{\phi_2} = time\ interval\ in\ hold\ mode \tag{2.13}$$

The constraint of unity-gain bandwidth is expressed as

$$\omega_u > Z\left(2+\frac{C_P}{C}\right)\frac{\ln 2}{T_{\phi_2}} \tag{2.14}$$

According to equation (2.11) and (2.14), the gain and unity-gain bandwidth can be well designed to meet the constraints.



(a) **(b)**

Figure 2.12 (a) MDAC in sample mode (b) MDAC in hold mode

2.4.2 Double Sampling

Double sampling means another duplicated path is added to let the amplifier is always in hold conversion. Output data rate is equivalently doubled without any power added. Unfortunately, several nonlinearities are also induced to decrease the efficiency, including memory effect, timing skew, and gain mismatch.

Memory effect means a fraction of the previous sample remains stored in the parasitic capacitance in the input of the amplifier due to the finite gain of the amplifier. Timing skew is caused by the distance between two adjective sampled edges is not the same as clock period. It can be found in the frequency spectrum domain. If input frequency is *n* Hz and sampling rate is *m* Hz, the timing error will be produced in the position of *(m/2-n)* Hz. While there is a gain mismatch between the parallel circuits, the sampling sequences they produced have different amplitudes. In the frequency domain, additional component is at multiples of half sampling rate.

Memory effect and timing skew can be suppressed by proper circuit design, which will be introduced later. Gain mismatch is avoided by symmetry layout to get better device matching.

2.4.3 Power Optimization

Error source is the random component whose dominant source is thermal noise. They are contributed by transistors in amplifier and capacitors in each stage. Assuming that thermal noise is additive Gaussian, the noise at the amplifier output appears as being superimposed on the signal. The power of the thermal noise is then described by its variance, and the variance should be much less than one LSB in order to maintain sufficiently high SNR. So, for the pipeline stage with N-bit accuracy requirement, the total input referred noise should be much

less than one LSB at N-bit level.

$$\sigma_{total} < 1LSB \tag{2.20}$$

The total input referred noise can be found by summing all the noise components from subsequent stages and is given by

$$\sigma_{total}^2 = \sigma_1^2 + \left(\frac{1}{2^B}\right)^2 \sigma_2^2 + \left(\frac{1}{2^B}\right)^4 \sigma_3^2 + \left(\frac{1}{2^B}\right)^4 \sigma_4^2 + \cdots \quad \text{,where } \sigma_j \cong \frac{kT}{C_j} \tag{2.21}$$

Where B means inter stage gain which is 2 in 1.5bit architecture per stage and C_j means the thermal noise of capacitor in stage j. Notice that the dominant source of noise is from the first stage and the noise contribution from subsequent stages is reduced by the inter stage gain. Besides, equation (2.11) and (2.14) show the constraints will be relaxed down as the z parameter gets lower. Therefore, we can design stage by stage to optimize power consumption and the noise performance is still acceptable[15].

2.5 MATLAB Behavior Model

In this section, the behavioral model of a 10-bit pipelined ADC with the 1.5-bit per stage architecture is constructed by MLTLAB. The pipelined ADC consists with 9 stages is shown as figure 2.13. First stage is named FADAC[2], 2 to 8 stages use conventional MDAC and 2bit flash ADC is in final stage. Finally combine each 2bit output to produce 10bit digital code.

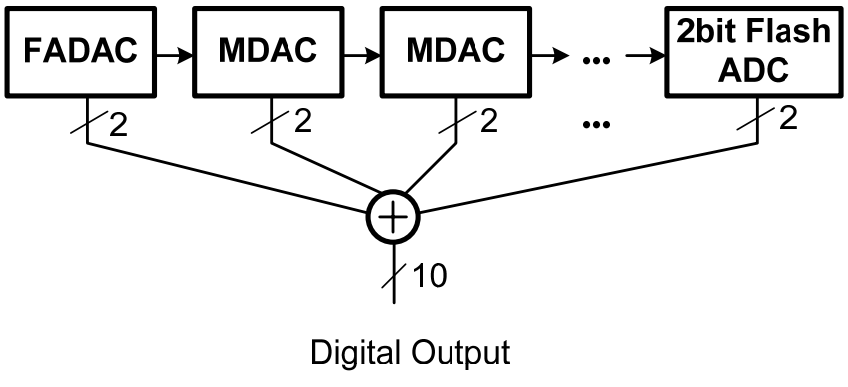
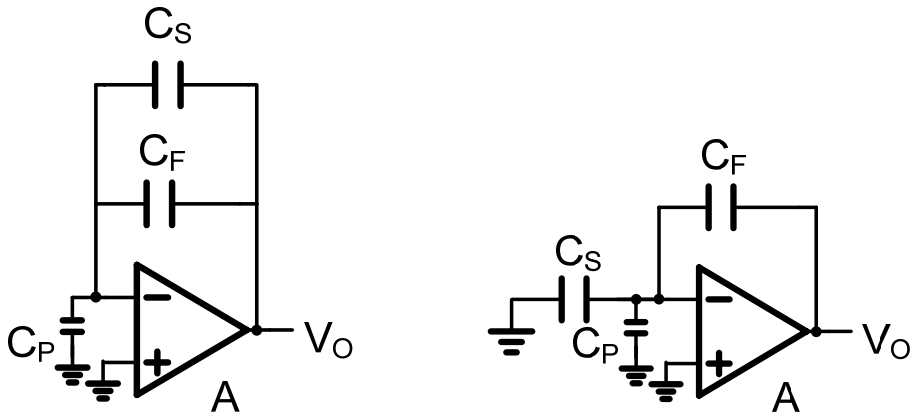


Figure 2.13 Block diagram of behavior model

First of all is finding out all of mathematical characteristics of each block including 1st stage FADAC, MDAC, and 2bit flash ADC. The FADAC and MDAC in hold time are shown in Figure 2.14. Besides, 2bit flash ADC can be described by if-then-else syntax in coding easily.



(a) **(b)**

Figure 2.14 (a) FADAC in hold mode (b) MDAC in hold mode

Discuss gain error effect in characteristic function of each stage. The transfer curve with finite gain error due to amplifier in FADAC and MDAC are shown in (2.22) and (2.23).

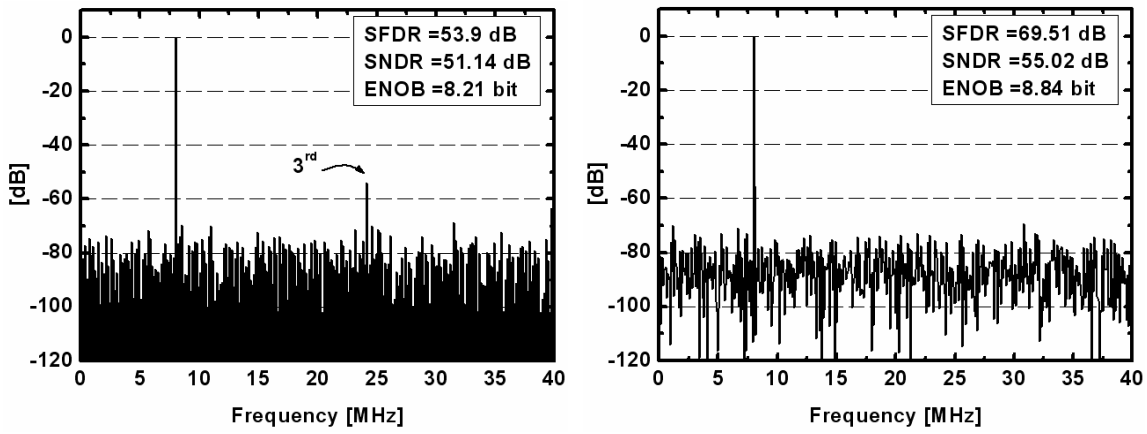
$$V_{O,FADAC} = V_{i,FADAC}\left(1 - \frac{1 + C_P/(C_S + C_f)}{A}\right) \tag{2.22}$$

$$V_{O,MDAC} = V_{i,MDAC}\left(1 - \frac{1 + (C_f + C_P)/C_S}{A}\right) \tag{2.23}$$

Where C_P is input capacitor of Amplifier, C_S and C_f are sample and hold capacitor, respectively. If the gain of amplifier is finite, V_O will have gain error.

The gain of amplifier is set 48dB which is the same as the circuit level simulation result. Figure 2.15 illustrates the spectrum domain of reconstructed digital output. While calibration off, the third harmonic tone is 54dB and ENOB is 8.21bit. After calibration, SFDR increases to 70dB and it means the non-linearity is suppressed well. As the figure 2.15 shows, the calibration can effectively reduce the harmonic tone to increase the performance but notice

that the noise flow is the same no matter the calibration is on or not.

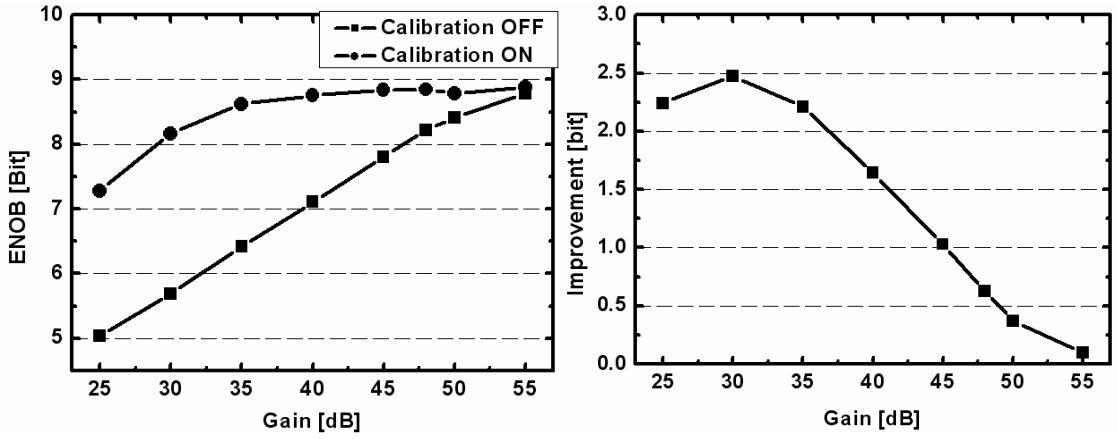


(a) (b)

Figure 2.15 Simulation result of Behavior model

(a)With calibration (b)Without calibration

Then plot the curve by changing the gain value from low to high as the figure 2.16(a). With gain increasing, the resolution also increases but settles to 8.88bit finally. The least gain to achieve above 8bit is about 30dB. Figure 2.16(b) is the difference between two curves in figure 2.16(a). The improvement is over 2bit with lower gain. With gain increasing to 55dB, the improvement is down to 0bit. The trade-off range of gain between the performance and improvement is from 30dB to 50dB. In the circuit level we design is about 48dB which meets the simulation result of behavior model.



(a) (b)

Figure 2.16 (a)Gain versus ENOB (b)Gain versus Improvement

CHAPTER 3
CIRCUIT SPECIFICATION AND SIMULAION

3.1 Time-interleaved Pipelined ADC Design

3.1.1 Design Issue

In this design, in order to propose low power consumption and high speed performance, several techniques are implemented.

In the first stage, we do not use sample-and-hold circuit. All analog circuits operator under 1V supply voltage will have low power efficiency. Time-interleaved technique doubles the output throughput and calibration circuit compensates error to improve the SFDR of ADC.

Without sample-and-hold in the first stage, aperture jitter will be induced[6]. It is because the signal between subDAC catches and comparator decides may be not the same. Therefore, the larger slope of the input signal will produce the larger error. Besides, in order to minimize the total power consumption, the power supply of operational amplifier in substage is applied to 1V. So there are some challenge to do low supply voltage design including of gain and bandwidth trade-off. The proposed operational amplifier is also declared.

Third, time-interleaved technique, also named double sampling, is implemented. Output throughput can be doubled without any power consumption addition, but the timing skew effect between two sampling paths must be emphasized. Clock generator should have property of timing skew insensitive. Nevertheless, the gain of operational amplifier is not enough as usual under low supply voltage. So calibration circuit is added to boost the performance of pipelined ADC. The calibration circuit measures the error due to gain error

and compensates deviation in the digital domain finally. Ideally, by calibration circuit, the total performance will be improved. In calibration circuit, we use the successive approximation architecture (SAR). The design key points are that accuracy must be higher than pipelined ADC and offset effect need to be cancelled.

3.1.2 Architecture

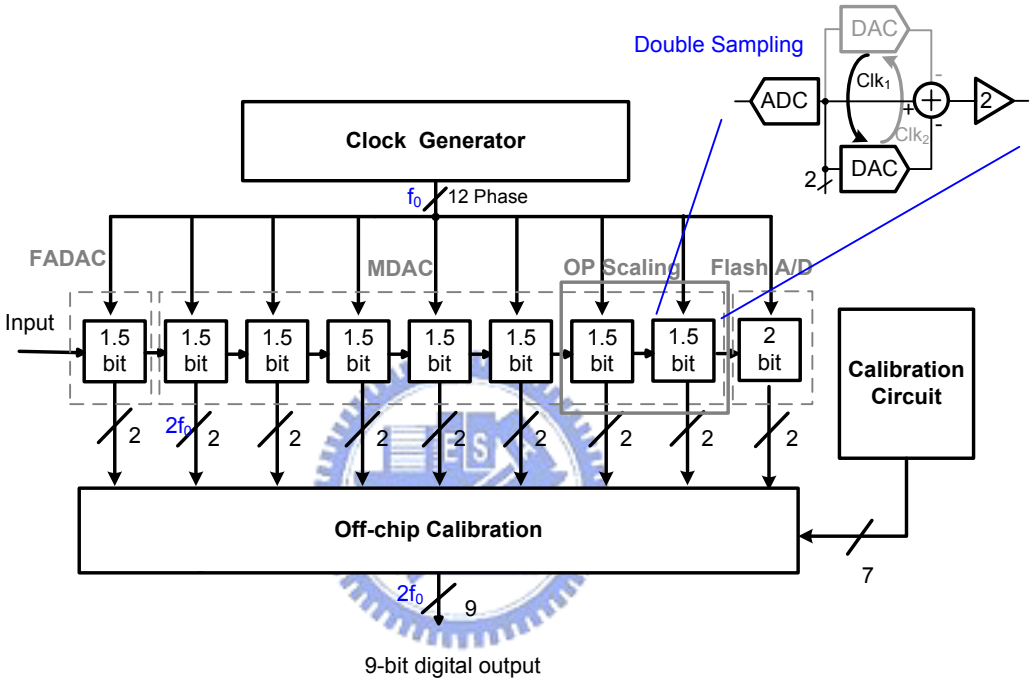


Figure 3.1 Pipelined ADC and calibration circuit architecture

Figure 3.1 shows the architecture which includes two blocks. One is pipelined ADC and another is calibration circuit. Consider the low power application and the power is almost dissipated by analog circuit, we wish to design opamp under 1V operation, but full swing of clock signal is remain 1.8V to relax the switch design complexity.

Under low voltage design, the performance of pipelined ADC will be decay due to gain is insufficient. So if we can measure the deviation due to gain error and compensate the value in the digital domain, the performance can be improved ideally. Therefore, calibration circuit

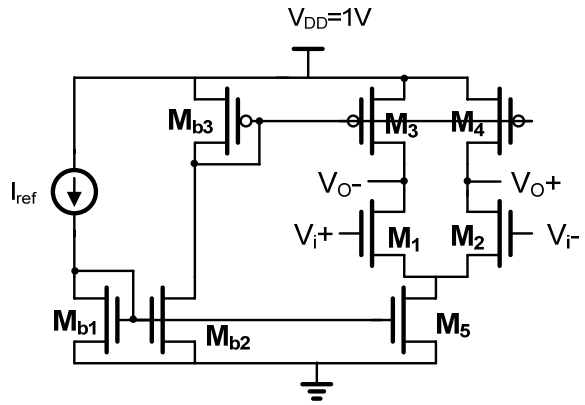
produces 7-bit digital codes which are relative to the value of opamp gain error. Then, combining the digital output codes from every stage in pipelined ADC and the 7 bit codes from calibration circuit, 9bit digital codes will be produced finally.

The each block in pipelined ADC will be described subsequently. At the beginning, 12 phase clocks from clock generator drive each 1.5 bit stage to work normally. By properly trading off between speed, accuracy, and circuit complexity, we decide using 1.5bit architecture per stage. Therefore, totally 9 stages are needed. In first stage, FADAC[2] architecture is applied. Traditional MDAC is used in 2 to 8 stage and 2bit flash ADC is in final. Because just calibrating the first 6 stages, the last two stages of MDAC can be allowed to have lower accuracy and reduce the power consumption of opamp. It is the meaning of op scaling technique.

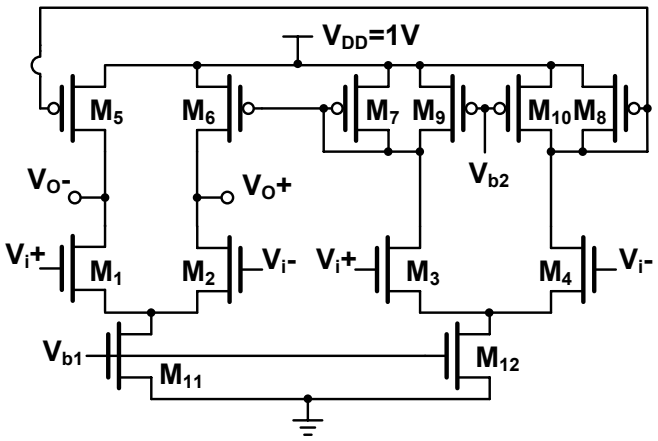
Besides, double sampling technique is applied. Adding a DAC additional path and operating the opamp not only in Clk_1 but also Clk_2 will equivalently double the throughput. It means that if clock speed from clock generator is f_0, digital output speed will be $2f_0$ while double sampling technique is applied.

3.2 Each Block of Pipelined ADC

3.2.1 Operational Amplifier



(a)



(b)

Figure 3.2 (a) One stage opamp schematic

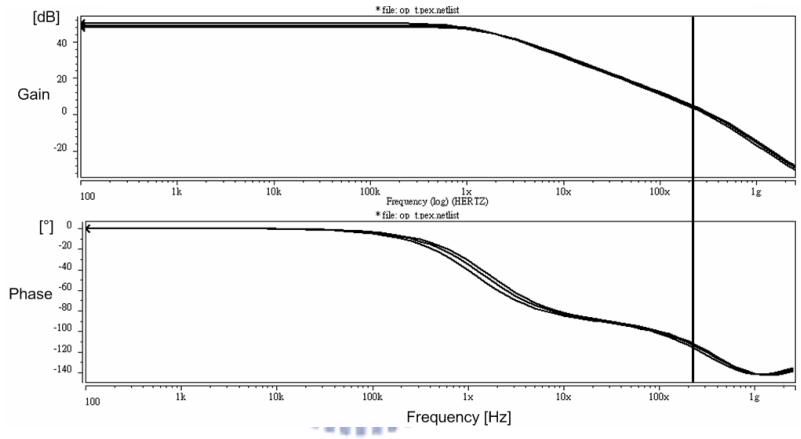
(b) Proposed opamp schematic

The operational amplifier used in every stage is the most critical element of the pipelined ADC. If we want to have higher throughput of pipelined ADC, the higher unity-gain bandwidth of operational amplifier is needed, but the power consumption is also increase. With current increase, gain of operational amplifier will be decay. In addition, if we wish to increase the resolution of pipelined ADC, the operational amplifier must have higher gain. In a word, unity-gain bandwidth and gain are trade-off.

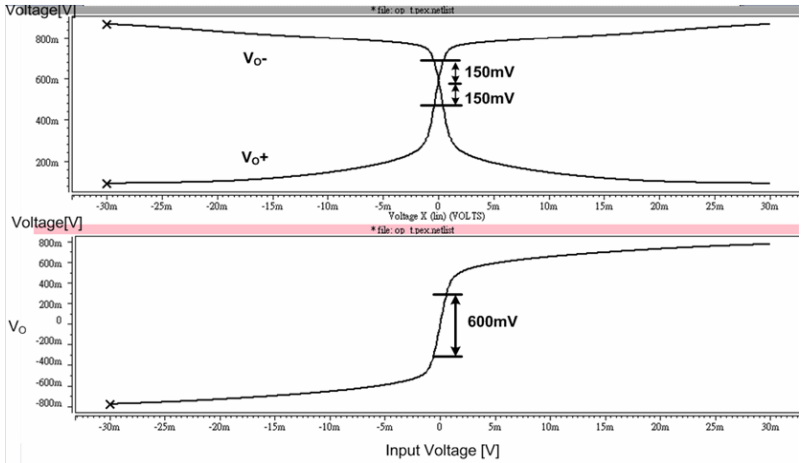
The schematic of operational amplifier used in FADAC and MDAC is shown in figure 3.2(b). Figure (a) is the simplest one stage opamp schematic. With the same current dissipation, one stage opamp will have best bandwidth performance but gain is the least. So the higher gain amplifier with split Gm stage is proposed and shown in figure (b). Comparing figure (a) and (b) under the same power consumption, architecture (b) has higher dc gain than (a) but the unity gain bandwidth are almost the same. In figure (b), additional M_3-M_4 pair steers the transconductance current which passes through current mirror M_6-M_7(M_5-M_{10}) into output node. Because of M_{11} current is half than M_5, the output impedance will be twice than figure (a). Besides, in order to break the relation between current source M_{11}(M_{12}) and current mirror M_6-M_7(M_5-M_{10}), current injection M_9-M_{10} is applied. In design, M_{11} current will be as

small as possible to get high gain and M_{12} current will be as large as possible to have high speed. The second pole which is at the $M_3(M_4)$ drain should be well design to meet the specification of speed.

Figure 3.3(a) shows gain and phase response of amplifier simulated result and figure (b) shows opamp output range is 600mV. In table 3.1, pre-simulation and post-simulation results are shown. Opamp gain is from 48dB to 50dB in different corner cases. Now choosing total 7 bit resolution to calculate the specification about speed and accuracy. The specification of opamp dc gain is above 43.6dB in both FADAC and MDAC and unity-gain frequency constraints are shown in table 3.2. Simulation results in table 2 all satisfy the specification.



(a)



(b)

Figure 3.3 Proposed operational amplifier simulation result

(a) Gain and phase response (b) Output linear range

Table 3.1 OP pre-simulation and post-simulation result

Temperature	50℃					
Supply Voltage	1V					
Input and output common mode voltage	0.75V , 0.6V					
Output Loading	1pF					
Differential Output Range	$600mV_{PP}$					
	Pre-simulation			*Post-simulation*		
Corner	TT	SS	FF	TT	SS	FF
DC Gain A_0 [dB]	49	50	48	49	50	48
Unity-Gain Frequency f_u [MHz]	332	304	351	329	301	347
Phase Margin [°]	59	58	60	59	58	60
Power Consuption [μW]	720	690	740	720	690	740

Table 3.2 OP specification in 1st FADAC and 2nd MDAC

	Unity-gain frequency	*DC gain*
1st FADAC	152MHz	43.6dB
2nd MDAC	262MHz	43.6dB

3.2.2 Common Mode Feedback Cicruit (CMFB)

Common mode feedback (CMFB) specifies the output common mode voltage of differential amplifier. As the figure 3.4(a) shows, the components of CMFB are several transistor switches and four capacitors. When Clk_2, the V_{cmo} and V_b charge to C2.V_{cmo} is output common mode voltage and V_b comes from bias circuit. When Clk_1 becomes high, C_2 connect to C_1. By charge sharing, the charge in C_2 will conduct to C_1. As several clock period pass, the two side of C_1 will be V_{cmo} and V_b, respectively. The V_{cmfb} controls the current

source of amplifier to do feedback function. Consequently, output common mode voltage is set to V_{cmo} as expectation. In design, to avoid output voltage violation, the size of C_1 is larger than C_2 four to ten times.

However, because double sampling is implemented in the ADC, output node capacitive loadings are different during Clk_1 and Clk_2. It will induce offset between the two paths. So the CMFB circuit is modified as figure 3.4(b). In a word, figure (b) is composed of two figure (a) circuits. In each clock phase, the capacitive effects are identical.

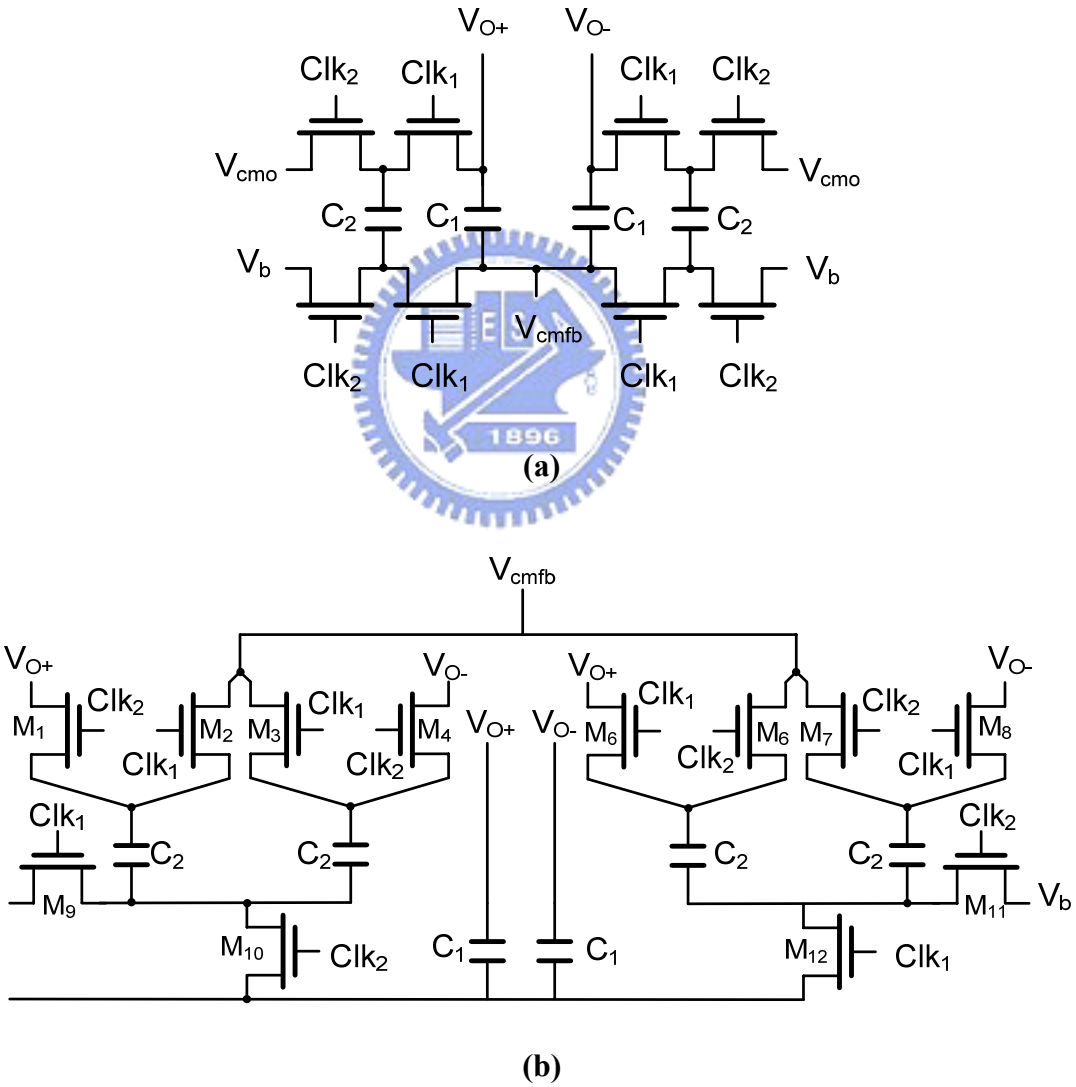


Figure 3.4 CMFB circuit (a) Conventional CMFB (b) Modify CMFB

3.2.3 Comparator

The schematic of the transconductance latched comparator[3] is shown in Figure 3.5(a). There are three advantages. One is that it can operate under low supply voltage. Second, it has no static power consumption, and third is that it is only one clock needed. When Clk is high, the two points a and b are low, and the output node, V_O^+ and V_O^-, are equally high. This is the state of reset. In this mode, M_9 and M_{10} are ON but M_{14} is OFF. Because of no path to conduct any current, there have no static power consumption. As the Clk signal becomes low, comparator operates in evaluate state. The two input pairs M_5-M_8 can be to consider as two resistances and the values are dependent on differential input and reference voltages. According to the resistances of two points a and b are low or high, it will introduce a small voltage difference between them. Then, M_3 or M_4 becomes ON, the set of cross couple pairs, M_1-M_4, will separate the difference to full scale. Finally, V_{O+} and V_{O-} are generated and the value is written as

$$V_O = \begin{cases} 1 & if \ V_i > V_{Ref} \\ 0 & if \ V_i < V_{Ref} \end{cases} \qquad (3.1)$$

In the evaluate state, when one of the two points, a and b, is higher than threshold voltage of inverter, M_9 or M_{10} will be turned off. It can be find no DC current path and no DC power consumption. Figure 3.5 shows the comparator simulated result. Assume V_{REF} is zero, the function between V_i and V_O is correct.

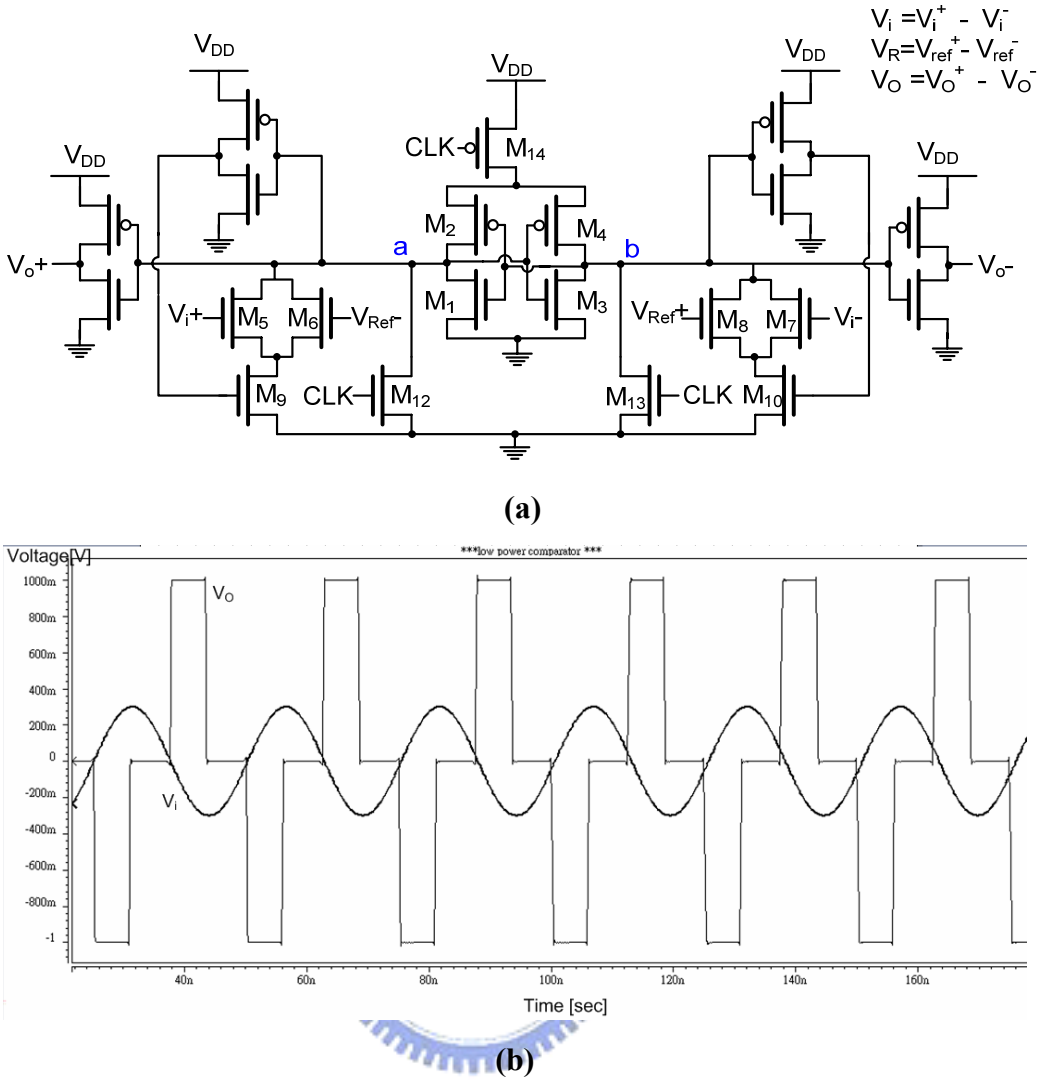


Figure 3.5 (a) Comparator schematic (b) Comparator simulated result

Due to mismatch and layout asymmetry, comparator will have offset voltage. However, comparator offset is allowed in 1.5bit per stage pipelined ADC. In this design, the tolerance is about 75mV. To emulate mismatches, randomly change the V_{t0}, channel width (W), and channel length (L) variations. Their standard deviations are

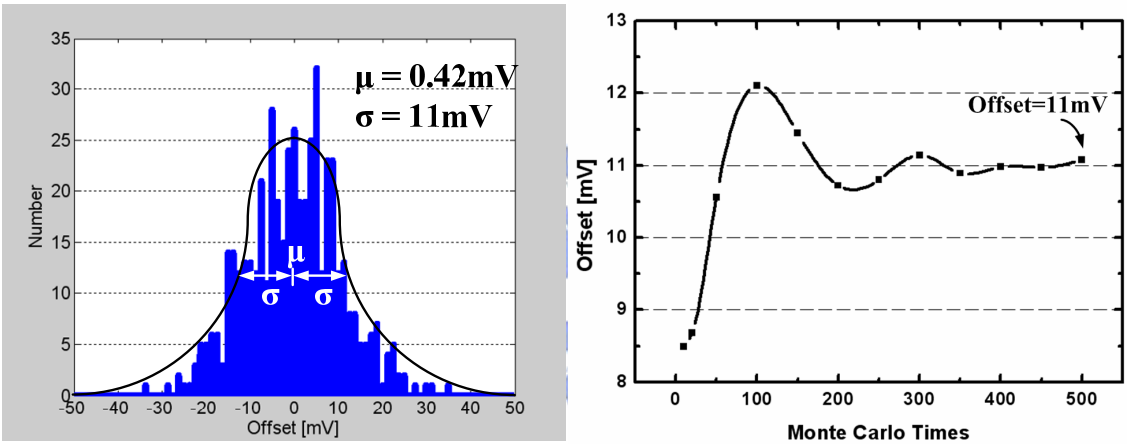
$$\sigma(\Delta V_t) = \frac{1}{2}\frac{A_{Vt}}{\sqrt{WL}} \qquad \frac{\sigma(W)}{W} = \frac{1}{2}\frac{A_\beta}{\sqrt{WL}}$$

For the 0.18μm CMOS technology, parameters are shown in table 3.3

Table 3.3 Mismatch parameter

A_{Vtn}	3.73mV×μm	$A_{\beta n}$	0.3635%×μm
A_{Vtp}	3.26mV×μm	$A_{\beta p}$	0.4432%×μm

From 500 time Monte Carlo simulations, the distribution of offset voltage is plotted in figure 3.6(a). By estimating as Gaussian distribution, the standard variation (σ) is 11mV. This value satisfies the constraint of comparator offset. Figure 3.6(b) shows the relation between the times of Monte Carlo simulation and offset value. As times number increase, the curve will settle to 11mV.



(a) **(b)**

Figure 3.6 (a) 500 times Monte Carlo simulation

(b) Times of Monte Carlo simulation and offset value relation

3.2.4 The 1.5 bit flash ADC

Figure 3.7 shows the 1.5bit flash ADC schematic. Signal V_i is the input and output is digital code "D_1D_2". They consist of two comparators, three level converters, and several logic gates. The last two elements are called encoder. The circuit is to convert input signal to digital level expression, as the table 3.4 shown.

Table 3.4 Input level expression

Condition	*D_1 D_2 D_3 (1V swing)*	*S_1 S_2 S_3 (1.8V swing)*
$V_i > (1/4)V_{Ref}$	1 0 0	1 0 0
$-(1/4)V_{Ref} < V_i < (1/4)V_{Ref}$	0 1 0	0 1 0
$V_i < -(1/4)V_{Ref}$	0 0 1	0 0 1

Instinctively, three NOR gates is applied to produce digital codes. Besides, it also has to switch the transistors in FADAC and MDAC circuit. Because the operation must be lager than phase of Clk_2 and supply voltage levels are different, three NAND gates and three level converters are needed.

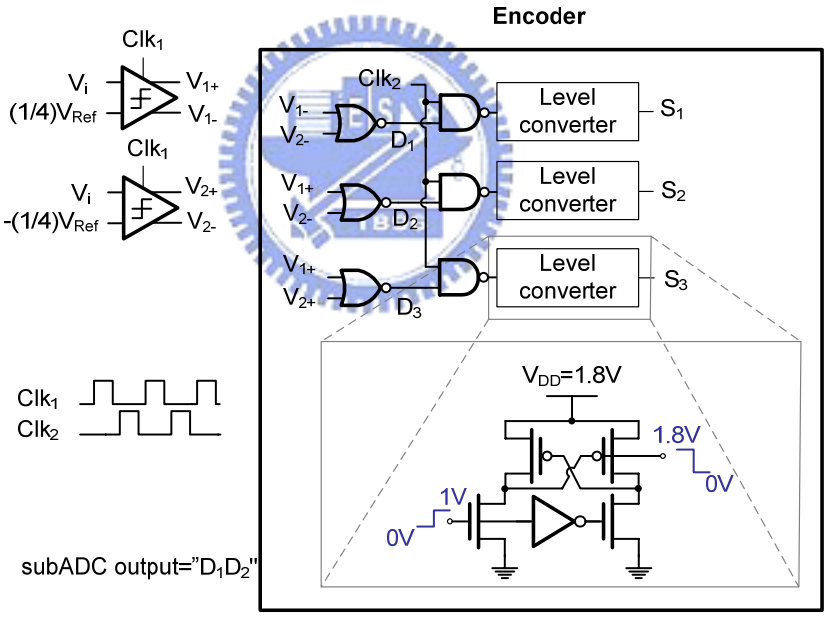


Figure 3.7 1.5bit flash ADC schematic

3.2.5 Flip-around DAC (FADAC)

Figure 3.8 is FADAC architecture which has been employed in an 125MHz 10bit pipeline ADC[2]. There are two features in this circuit. One is that feedback factor is almost equal to one in hold mode, so having good performance in speed and accuracy. Another is

because of gain is half one in hold mode, input range need to be amplified four times than output. Clock waveform is shown as figure (c). During Clk_1, figure (a), input is sampled in C_{S1} and another three references are sampled in C_{S1}, C_{S2}, and C_{S3}. The three references is $+2V_{REF}$, 0, and $-2V_{REF}$, respectively. Then, comparators estimate the input level when Clk_1 becomes high to low. When Clk_2 is high, capacitor is switched adequately by decoder and flipped-around with C_{S1} to the output node. By charge sharing and parallel connection, the input transfer function is represented as (4.2).Assume $C_{S1}=C_{S2}=C_{S3}=C_{S4}$,

$$V_i = \frac{1}{2}V_i + b_i V_{Ref} \tag{3.2}$$

Where b_i is +1 if digital code is “00”; b_i is 0 if digital code is “01”; b_i is -1 if digital code is “10”.

Figure (d) is the INL plot of FADAC. The transverse axle means input value which is from -1.2V to +1.2V. The INL, ideal output value minus real output then referred to input, is defined as (4.3),

$$INL = \frac{[(\frac{1}{2}V_i + b_i V_{Ref}) - V_O]}{2} \tag{3.3}$$

The simulated INL is about ±1.5 LSB. LSB is normalized to 9bit and $V_{p\text{-}p}$ is 600mV.

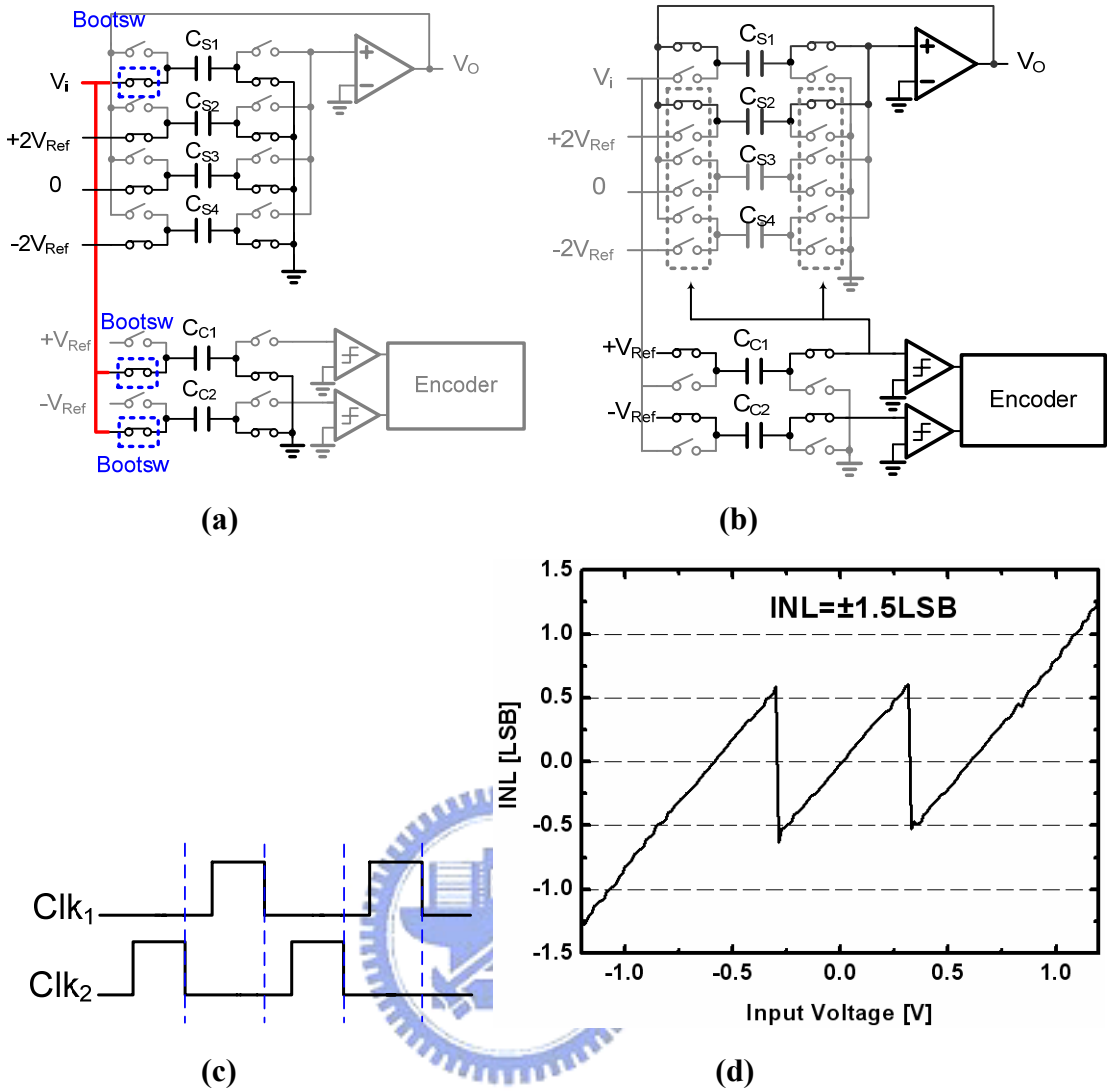


Figure 3.8 FADAC schematic

(a) During Clk_1 (b) During Clk_2 (c) Clock waveform (d)INL plot

Without sample-and-hold amplifier in the first stage, the aperture jitter will be induced[6]. In figure 3.9(a), while data sampled in C_{S1} differ from comparator estimate, it will cause error that can not be compensated. Therefore, the input stage in FADAC is shown in figure 3.8(a). Adding C_{C1} and C_{C2} sample paths to match C_{S1} path to make sure data in C_{S1}, C_{C2}, and C_{C1} are identical during Clk_1 phase. Figure (b) shows the clock waveform, clk_b and Clk_c are applied additionally.

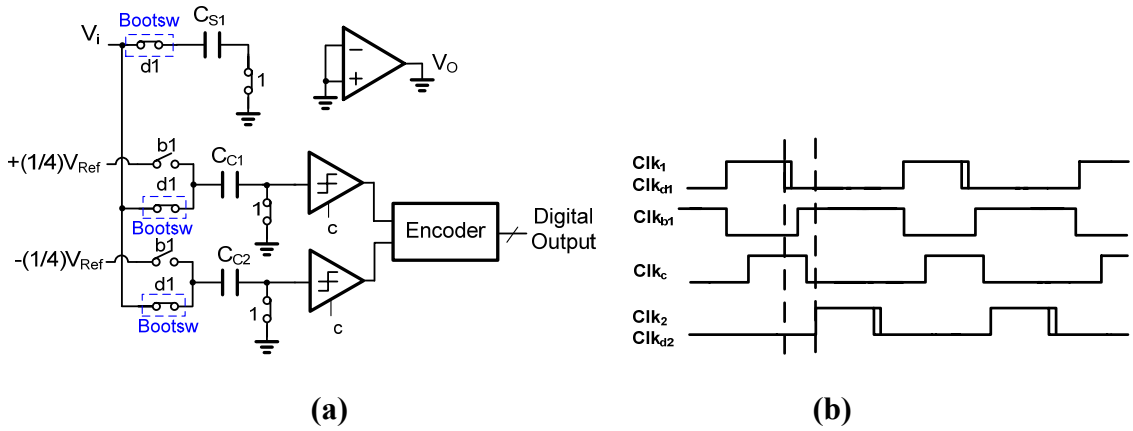


Figure 3.9 (a) FADAC input sampling circuit (b) Clock waveform

3.2.6 Bootstrapped Switch

Bootstrapped switch supports constant conductive impedance and is used to cancel the input dependent non-linearity. Figure 3.10 shows the schematic. Clk_b is complementary to Clk. when Clk is low, the voltage in right side of capacitor C_1 is V_{DD}, and left side is gnd, so C_1 is store the voltage drop of V_{DD}. When Clk becomes high, the right side of C_1 connects to M_9 gate and left side connects to V_i. It means the gate drive between M_9 gate and source will hold out V_{DD}. Therefore, M_9 has a good performance in linearity. The M_8 transistor is added to reduce the maximum V_{DS} of M_5.

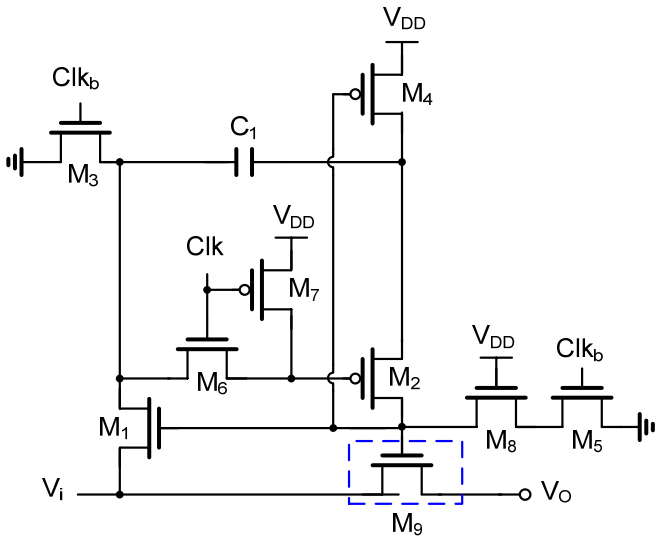


Figure 3.10 Bootstrapped switch schematic

Figure 3.11(a) is the circuit to simulate the linearity of bootstrapped switch. Figure 3.11(c) shows the SFDR of bootstrapped switch while input frequency is 40MHz and switch clock rate is 80MS/s. Then change input frequency to plot the SFDR curve of output FFT. The simulated result is shown in figure 3.11(b). From low input frequency to high, the SFDR are all above 78dB. Figure 3.11(d) is the time domain simulation result where the V_O and V_i have constant voltage gap 1.8V.

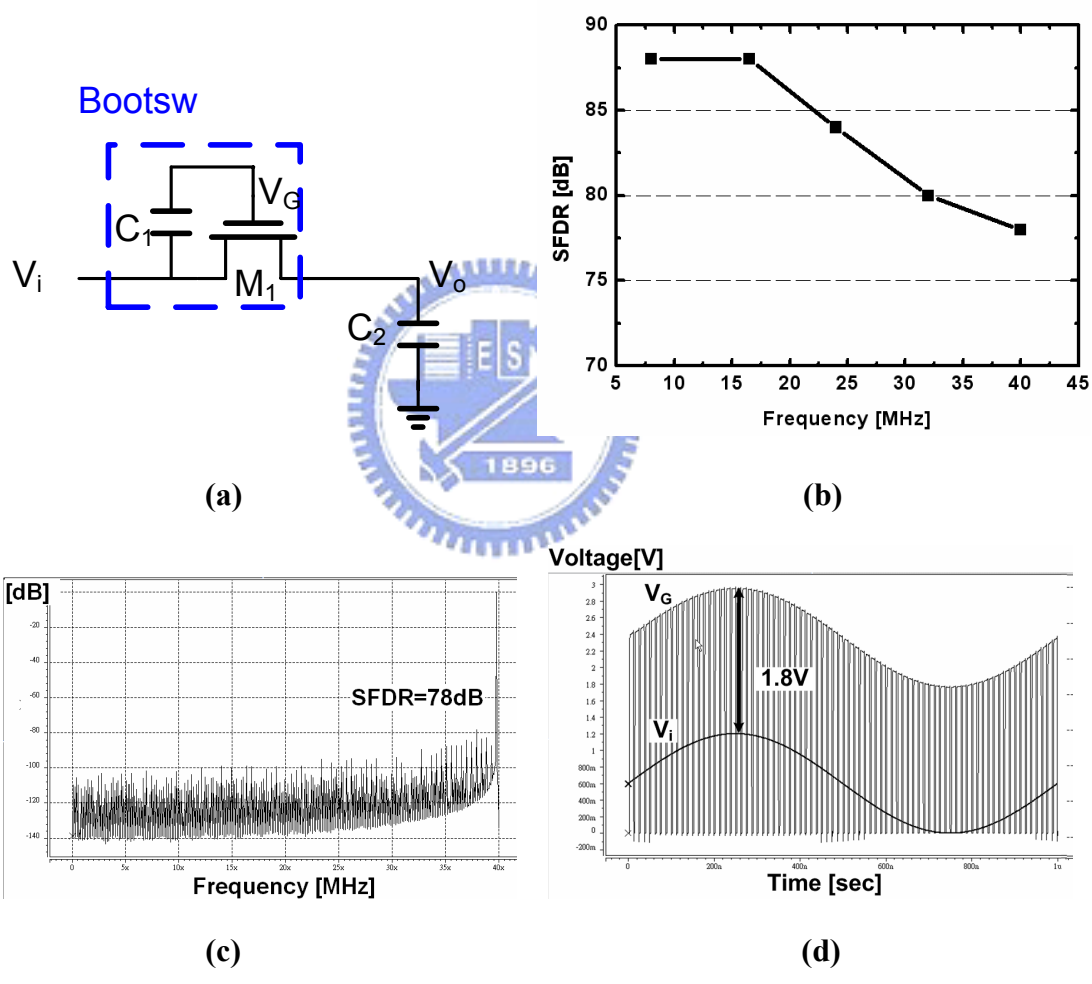


Figure 3.11 (a) Circuit to simulate SFDR of bootstrapped switch

(b) Dynamic simulation with different input frequency

(c) SFDR is 78dB when input frequency is 40MS/s and switch clock rate is 80MS/s

(d) Time domain simulation

3.2.7 Multiply DAC (MDAC)

Figure 3.12 is conventional MDAC architecture. Clock waveform is shown as figure (c). During Clk_1, figure (a), input is sampled in C_F and C_S. Then, comparators estimate the input level when Clk_1 becomes high to low. When Clk_2 is high, C_F flipped-around to output and encoder switches the adequate reference voltage to C_S to do the operation of subtraction and multiplication. The three references is $+V_{REF}$, 0, and $-V_{REF}$, respectively. By charge conservation rule, the input transfer function is represented as (3.4).Assume C_F=C_S,

$$V_i = 2V_i + b_i V_{Ref} \tag{3.4}$$

Where b_i is +1 if digital code is "00"; b_i is 0 if digital code is "01"; b_i is -1 if digital code is "10".

Figure (d) is the INL plot of MDAC. The transverse axle means input value which is from -0.3V to +0.3V. The INL, ideal output value minus real output then referred to input, is defined as (3.5),

$$INL = \frac{[(2V_i + b_i V_{Ref}) - V_O]}{2} \tag{3.5}$$

The simulated INL is about ±3LSB. 1 LSB is normalized to 9bit and $V_{p\text{-}p}$ is 600mV.

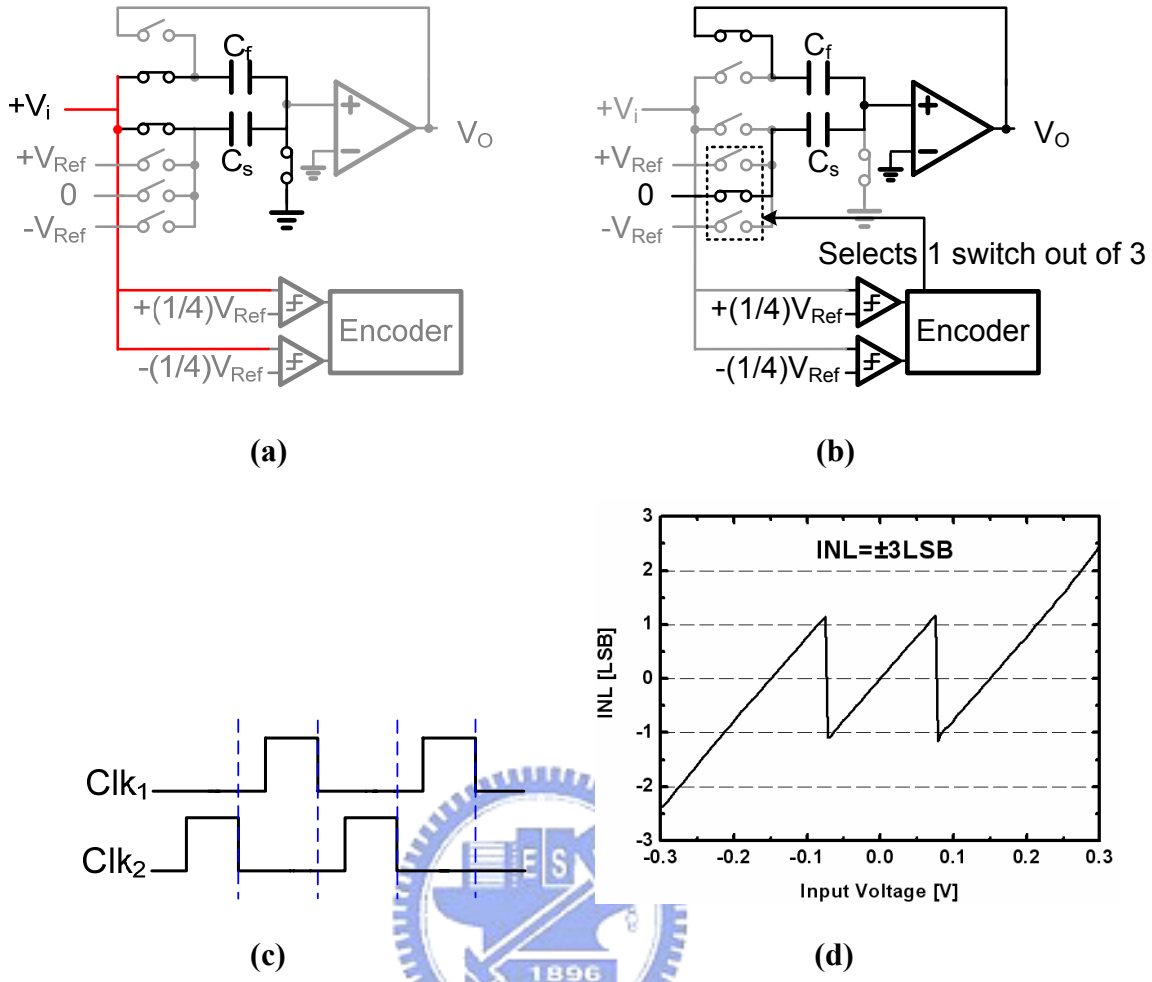


Figure 3.12 MDAC schematic

(a) During Clk_1 (b) During Clk_2 (c) Clock waveform (d) INL plot

3.2.8 Double Sampling

In order to double the output throughput, the technique of double sampling is realized. Easily, add another path to convert the input signal. Figure 3.12(a) and (b) mean the MDAC circuit during Clk_1 and Clk_2. When Clk_1 is high, C_{f1} and C_{S1} are applied to be sampled capacitors. Besides, C_{f2} and C_{s2} are flipped-around to be hold capacitors. During Clk_2, C_{f1} and C_{S1} are replaced to C_{f2} and C_{S2}. C_{f2} and C_{S2} become hold capacitors. By applying the technique, the opamp is always in used but has no power dissipated additionally. But, memory effect is induced as well. Due to the finite gain of the opamp a fraction of the previous sample

remains stored in the parasitic capacitance in the input of the opamp. Therefore, add clock Clk_{rst} between Clk_1 and Clk_2 to cancel the memory effect. As the figure 4.12(c) shows, the opamp resets its input and output to common mode voltage during Clk_{rst}. And figure (c) is the clock waveform.

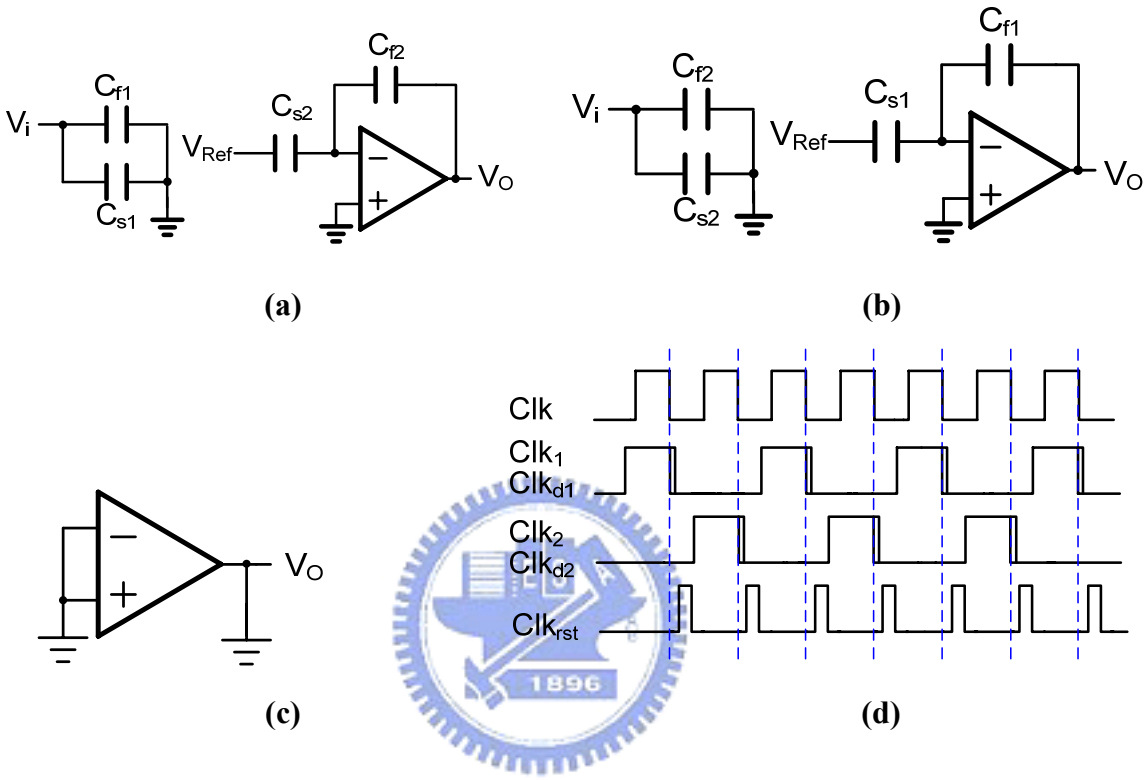


Figure 3.13 Double sampling

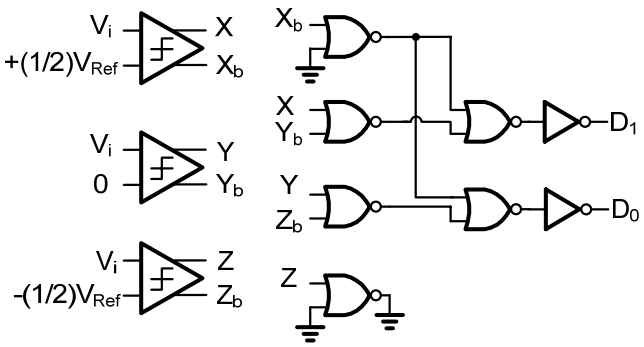
(a)During Clk_1 (b) During Clk_2 (c) During Clk_{rst} (d) Clock waveform

3.2.9 Final 2bit flash ADC

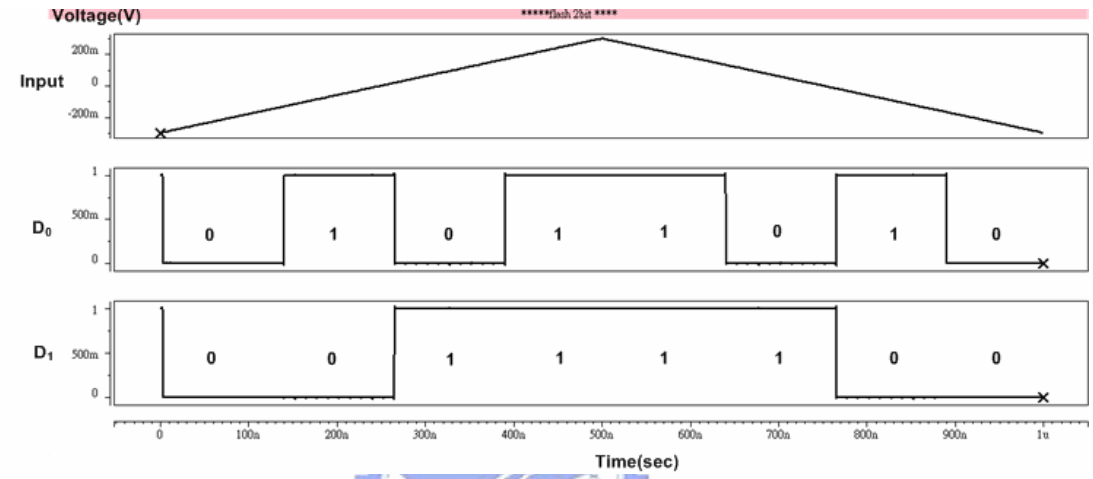
Figure 3.14(a), (b) shows the truth table and implemented schematic. Figure (c) is the simulation result. The two threshold voltages is $\pm(1/2)V_{REF}$ and 2bit digital output is "D_1D_0".

X	X_b	Y	Y_b	Z	Z_b	D_1	D_0
0	1	0	1	0	1	0	0
0	1	0	1	1	0	0	1
0	1	1	0	1	0	1	0
1	0	1	0	1	0	1	1

(a)



(b)



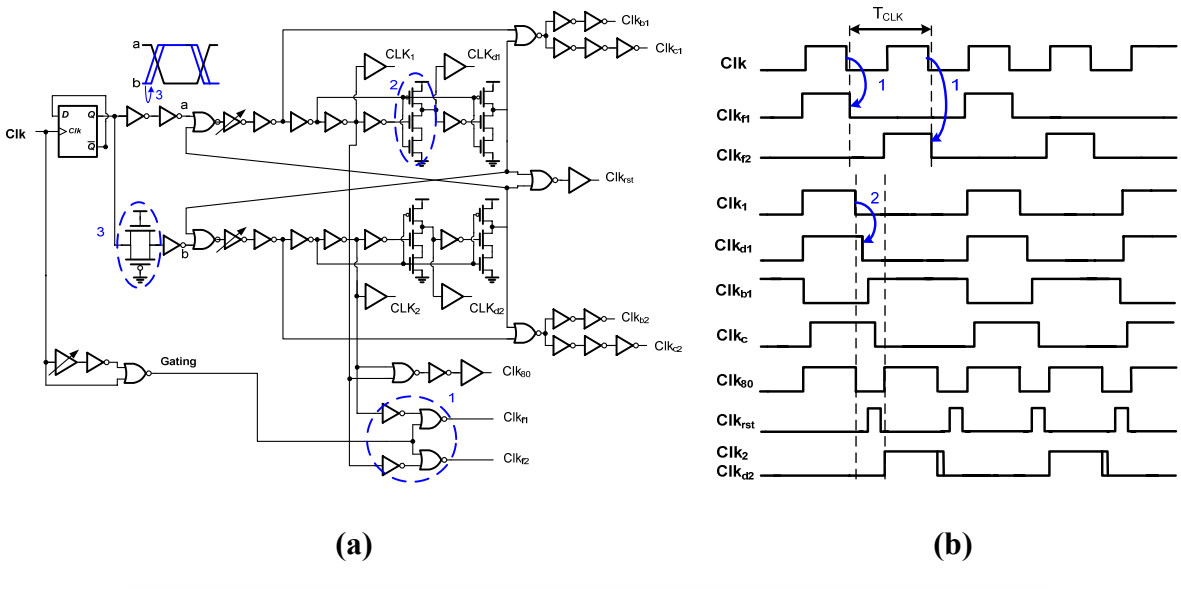
(c)

Figure 3.14 2bit flash ADC

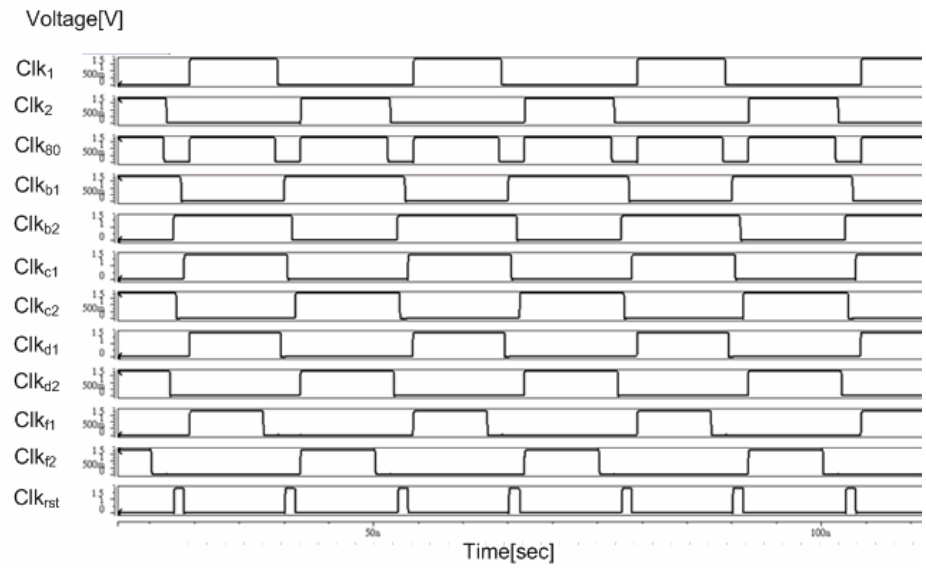
(a) True table (b) Gate level implement (c) Simulation waveform

3.2.10 Clock Generator

Figure 3.15 shows the clock generator schematic and waveform diagram. Because of the use of double sampling technique, we need to be aware of the clock skew effect. As the mark 1 show, creating a Gating signal to make sure the space between Clk_{f1} and Clk_{f2} falling edges can reduce clock skew. Mark 2 indicates Clk_{d1} falling production. Besides, we should let the point a and b have the same delay, so a transmission gate is added. It is shown as mark 3. By tuning the size of transmission gate, we can get the best situation which has least clock skew effect. Figure (c) shows the simulation result.



(a) (b)



(c)

Figure 3.15 (a) clock generatior schematic

(a) waveform diagram (c) simulation resolutoin

3.2.11 Timing Diagram

The important role in pipelined ADC is timing diagram. Figure 3.16 shows the timing diagram which ensures the ADC function correctly in timing sequence. Q1 and Q2 are alternate each other and represent the two channels under double sampling. Mark 1 shows FADAC samples data and comparator evaluates at this time. Mark 2 means encoder decides to do right subtraction and FADAC transit to hold mode. At the same time, MDAC in next stage

is in sample mode. Then, Mark 3 is the time at the end of MDAC hold state. Mark 4, the signal has already settled accurately and MDAC transit sample state to hold mode.

Besides, Clk_{rst} introduced in **3.2.8 Double Sampling** is between two adjacent states to cancel the memory effect.

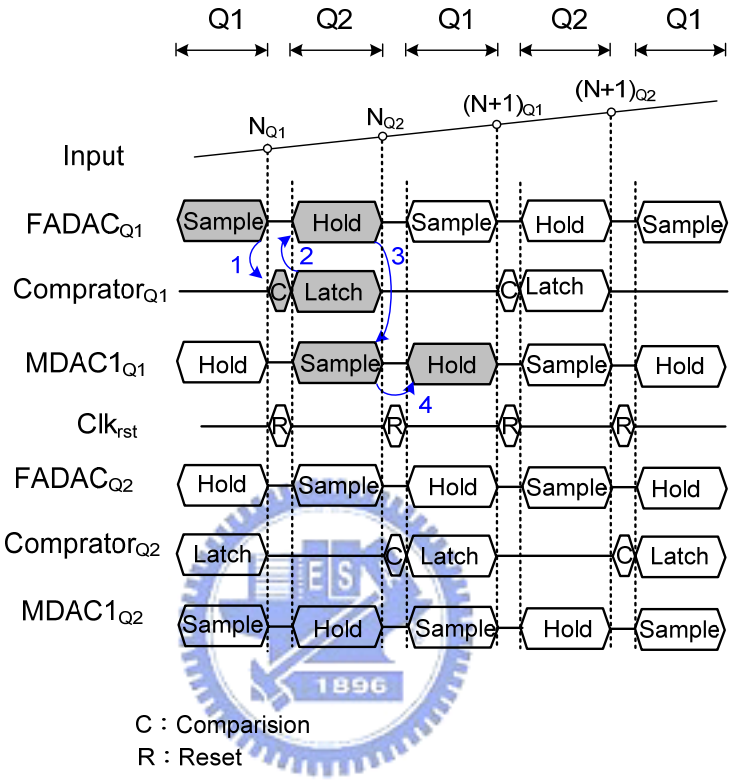


Figure 3.16 Timing diagram

CHAPTER 4

CALIBRATION CIRCUIT

4.1 Calibration Conception

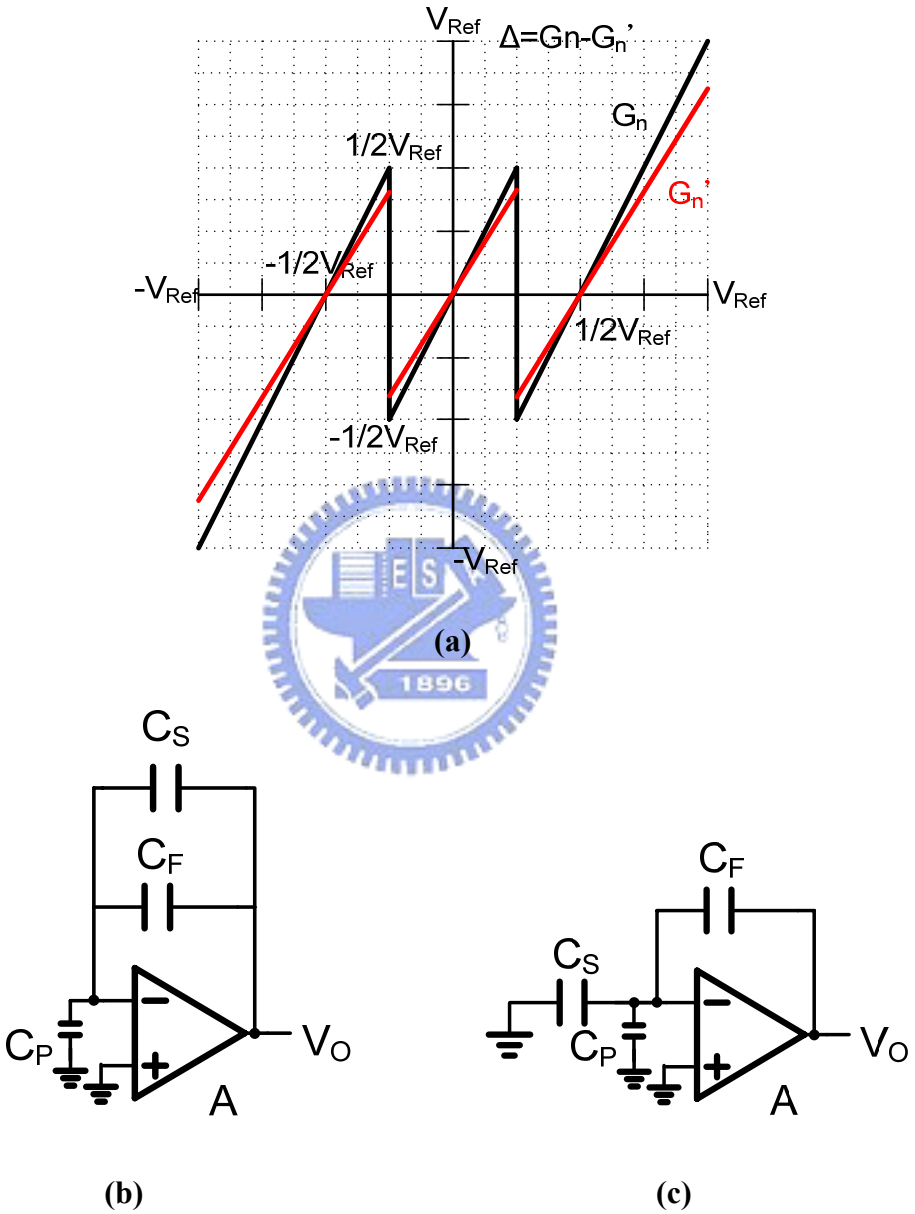


Figure 4.1 (a) Ideal and real transfer curves

(b) FADAC in hold mode (c) MDAC in hold mode

Figure 4.1 shows the radix-2 1.5bit transfer curve in MDAC circuit. The transverse axle means input value and longitudinal axle is output value. Black line is ideal curve and each

slope in the three segments is 2. Red line is less than 2 due to opamp gain error. Define slope in black line is G_n, slope in red line is G_n'. Figure 4.1(b) is FADAC circuit in hold mode and (c) is MDAC circuit in hold mode. By hand calculation, assume $C=C_S=C_F$, the slope can be written

$$G_n' \ in\ FADAC = \frac{G_n}{1+\left(1+\frac{C_P}{2C}\right)\Big/A} = G_n\left(1-\frac{1+\frac{C_P}{2C}}{A}\right) = G_n\left(1-\frac{\Delta_G}{2}\right)$$
$$G_n' \ in\ MDAC = \frac{G_n}{1+\left(2+\frac{C_P}{C}\right)\Big/A} = G_n\left(1-\frac{2+\frac{C_P}{C}}{A}\right) = G_n\left(1-\Delta_G\right) \quad (4.1)$$

Where $\Delta_G = \frac{2+\frac{C_P}{C}}{A}$ is gain error in MDAC. By (4.1), error in FADAC is half than which in MDAC due to the feedback factor in MDAC is almost twice than which in FADAC.

Then, define $G=G_1=G_2$, and assume the first stage is FADAC and others are MDACs, from 10bit analog to digital conversion equation

$$\begin{aligned} A &= A_1^{da} + \frac{A_2^{da}}{G_1'} + \frac{A_3^{da}}{G_1'G_2'} + \ldots + \frac{A_9^{da}}{G_1'G_2'\ldots G_8'} \\ &= A_1^{da} + \frac{A_2^{da}}{G}\left(1+\frac{\Delta_G}{2}\right) + \frac{A_3^{da}}{G^2}\left(1+\frac{\Delta_G}{2}\right)\left(1+\Delta_G\right) + \ldots + \frac{A_9^{da}}{G^8}\left(1+\frac{\Delta_G}{2}\right)\left(1+\Delta_G\right)^7 \end{aligned} \quad (4.2)$$

where A is the input signal, A_n^{da} is digital code from n-th subADC output, G is ideal conversion gain and G' is real conversion gain.

The value of Δ_A is what the calibration circuit need to measure. By (4.2) constructed, the gain error can be compensated ideally. So the performance of pipelined ADC should be improved.

4.1.1 Nonlinearity of gain

In the above discussion, the gain is assumed as a constant value. Accordingly, the transfer curve of each section is approximated to a straight line. In practical, the output impedance is dependant on the output value, so the gain value also varies with the output. As

the figure 4.2 shows, the slope of G' due to gain deviation is various with a small range. Define the gain deviation due to gain nonlinearity

$$\Delta_A = \frac{A_0 - A}{A_0} \tag{4.3}$$

Where A_0 is the gain without gain deviation and A is the gain with gain deviation. By the intuition, set parameter k is improvement of calibration circuit. We can get

$$\Delta_A < 2^k \tag{4.4}$$

On the other hand, the nonlinearity of gain is the dominant influence in the efficiency of calibration. Figure 4.3 shows the simulated nonlinearity of opamp which is the same as figure 3.2(b) shows. With the corner simulation, the gain deviation is about 25%. By the equation of (4.4), the improvement can be near 2 bit.

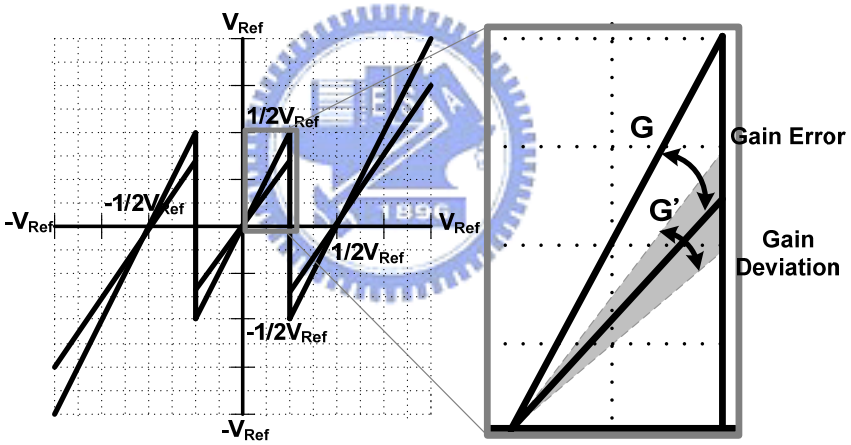


Figure 4.2 Slope deviation due to gain deviation

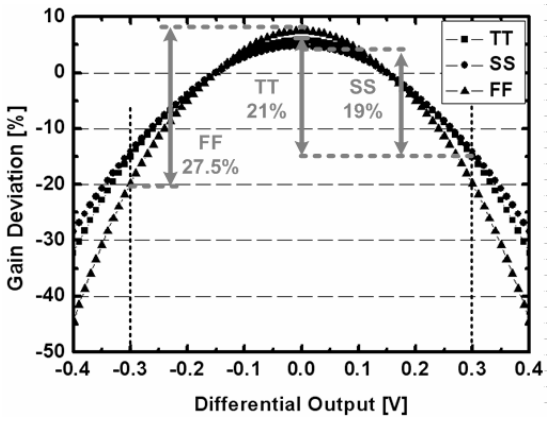
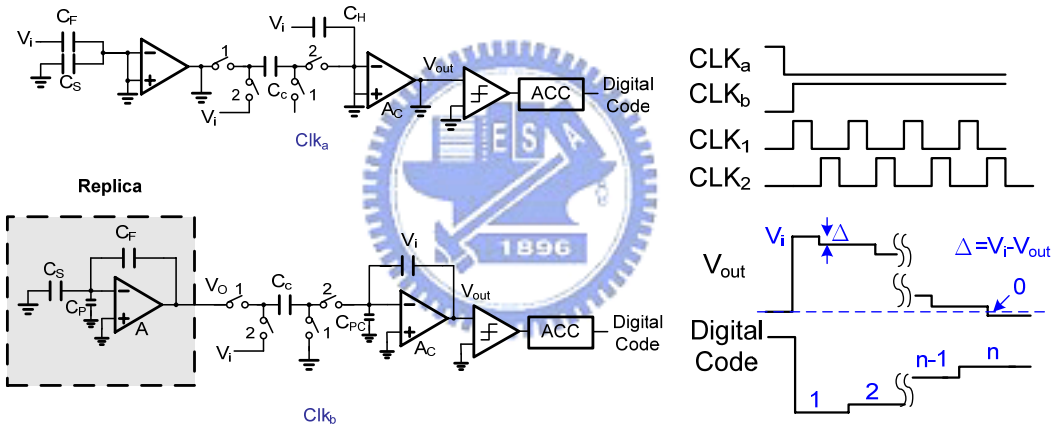


Figure 4.3 Nonlinearity of opamp versus differential output

4.2 Calibration Circuit

Figure 4.4 shows the calibration circuit which is applied to measure the gain error. The components are two opamps, one comparator, and an accumulator. One of the opamps is the same as which in first several stages and the other has higher gain to have higher resolution. In Clk_a, V_i samples to C_F and C_H. when Clk_b becomes high, due to the gain error V_O is a slightly smaller than V_i. Define the difference is symbol of Δ. Furthermore, V_{out} is much close to V_i because A_C gain is high. Then, Clk_1 and Clk_2 start to become high alternately. So V_{out} decreases one Δ as one clock period passes. As the figure (b) shows, while V_{out} becomes less than zero, comparator lets the accumulator stop counting. At this time, digital code output is produced and shown as (4.4).



(a) **(b)**

Figure 4.4 (a) Calibration circuit (b) Clock and output waveform

$$Digital\ Code = n = \left(\frac{A}{2+C_P/C}\right)\left(1-\frac{A}{A_C}+\frac{C_P-C_{PC}}{(2+C_P/C)C}\frac{A}{A_C}\right) \quad if\ A << A_C$$
$$\cong \left(\frac{A}{2+C_P/C}\right) = \frac{1}{\Delta_G} \tag{4.5}$$

From (4.5), there are a simple relation between *Digital Code* and gain error. Then combine (4.2) and (4.5)

$$A = A_1^{da} + \frac{A_2^{da}}{G_1^{'}} + \frac{A_3^{da}}{G_1^{'}G_2^{'}} + \ldots + \frac{A_9^{da}}{G_1^{'}G_2^{'}\ldots G_8^{'}}$$
$$= A_1^{da} + \frac{A_2^{da}}{G}\left(1+\frac{1}{2n}\right) + \frac{A_3^{da}}{G^2}\left(1+\frac{1}{2n}\right)\left(1+\frac{1}{n}\right) + \ldots + \frac{A_9^{da}}{G^8}\left(1+\frac{1}{2n}\right)\left(1+\frac{1}{n}\right)^7 \quad (4.6)$$

Where n is the calibration circuit output, G is ideal conversion gain, and A_n^{da} is digital code from n-th subADC output. Equation (4.6) means the compensated operation in off-line calibration and illustration is shown in figure 4.5. The division and add operations are needed.

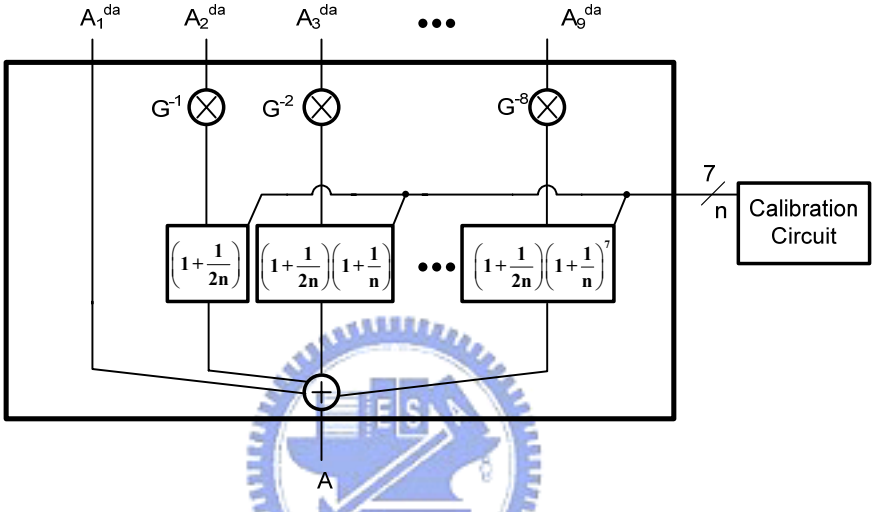
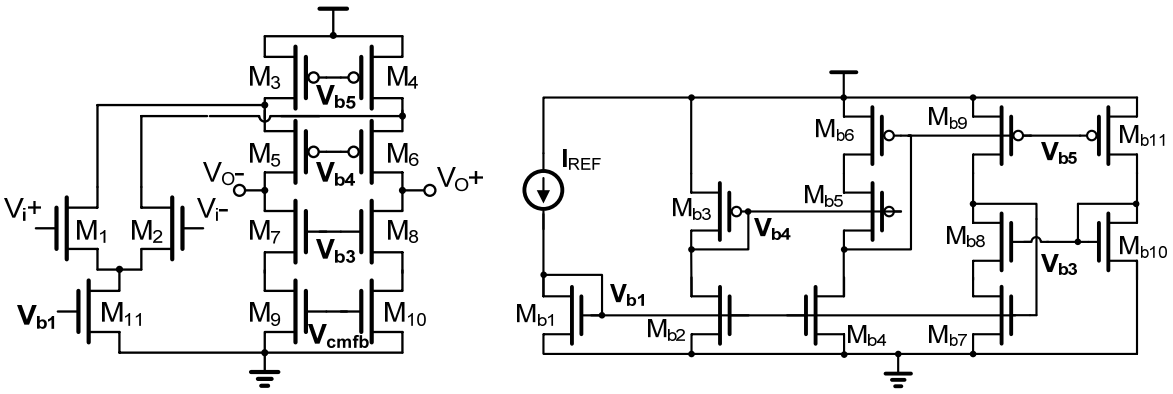


Figure 4.5 Illustration of off-line calibration operation

4.3 Operation Amplifier in Calibration Circuit

In calibration circuit, a high gain opamp is needed but the unity-gain frequency and output swing is not required strictly. As the figure 4.6(a) shows, folded-cascoded opamp is applied. The output swing just needs 150mV, so the V_{DD} is allowed to be 1V. The wide swing cascode bias circuit is shown in figure 4.6(b). The common mode feedback circuit (CMFB) is used as figure 3.4(a). The simulation result is shown in table 4.1. The dc gain is 64dB and power consumption is 220μW.



(a) **(b)**

Figure 4.6 (a) Amplifier in calibration circuit (b) Bias circuit

Table 4.1 Amplifier in calibration circuit simulated result

Temperature	50℃		
Supply Voltage	1V		
Input and output common mode voltage	0.75V , 0.5V		
Output Loading	0.2pF		
Differential Output Range	$300mV_{PP}$		
Corner	***TT***	***SS***	***FF***
DC Gain A_0 [dB]	64.4	63.3	64.3
Unity-Gain Frequency f_u [MHz]	100	94.5	103
Phase Margin [º]	58	59	57
Power Consuption [μW]	220	210	225

4.4 Calibration Circuit with Offset Cancellation

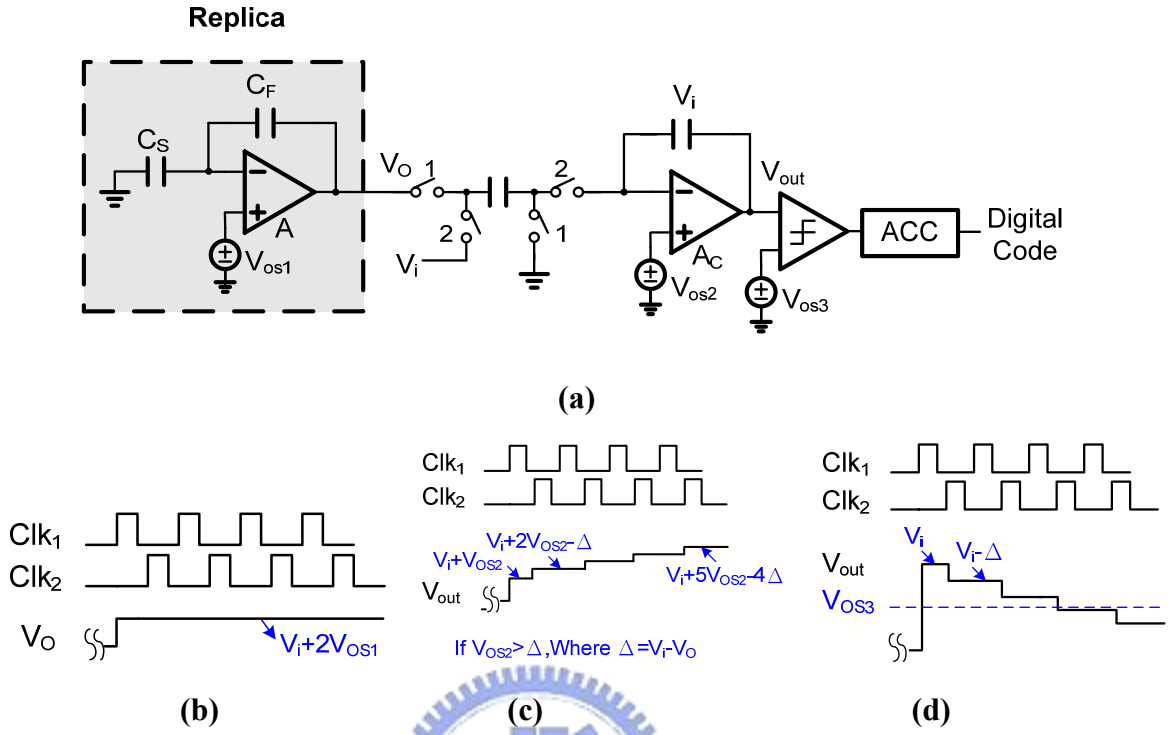


Figure 4.7 (a) Calibration circuit with offset.

(b) V_{OS1} affection (c) V_{OS2} affection (d) V_{OS3} affection

Now, consider the offset effect from each component in calibration circuit. There have three offsets contributed from replica opamp, calibration opamp, and comparator. As the figure 4.7 shows, discuss each offset effect due to V_{OS1}, V_{OS2}, and V_{OS3}, respectively. First, if V_{OS1} is not equal to zero, V_O will always have V_{OS1} term and finally let the subtraction operation have a false result. Second, assume V_{OS2} is larger than Δ, then V_{out} will increase step by step during clock period passing and finally be saturated. That is not desirable situation. Third, V_{OS3} cause the comparator decision level to shift by a value. Therefore, depend on V_{OS3} is negative or positive, digital output may be increase or decrease. Furthermore, in order to get accurate output data, offset cancellation is applied to eliminate the offset non-ideal effect.

The technique of input offset storage cancellation (IOS) is applied. The conception is to keep opamp differential inputs as voltage of V_{OS} during whether Clk_1 or clk_2. Because of opamp input and output common mode voltage are not the same, we use the capacitor to be feedback.

Figure 4.8 shows how to cancel V_{OS1} effect. In Clk_1, V_i samples to C_H, the feedback C_r is connect between opamp input and output node. The opamp input is virtual ground to be V_{OS1} under negative feedback loop. So the offset is retained in C_H. when next Clk comes, Clk_2, C_r is replaced by C_H. In this time, the voltage of opamp input is still the same as V_{OS1} and output have no offset effect. It means the offset is cancelled. As figure (b) shows, V_O is equal to V_i during Clk_2.

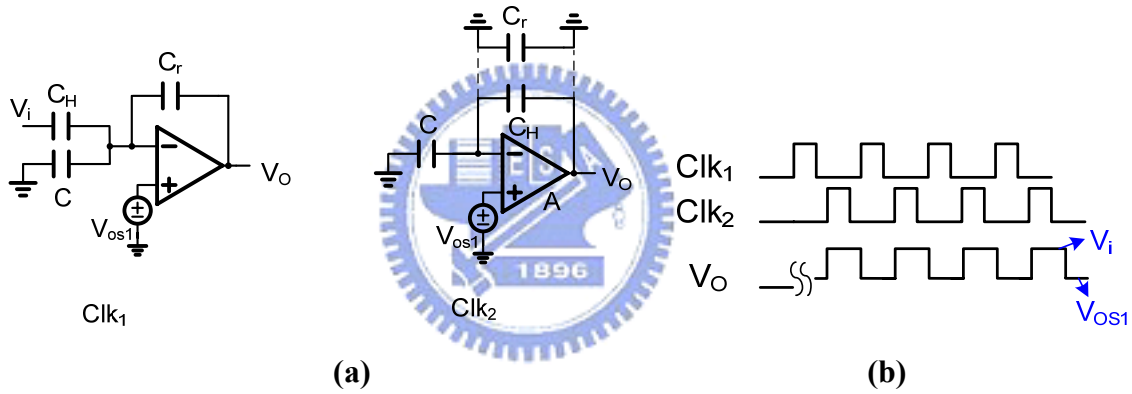


Figure 4.8 (a) V_{OS1} cancellation circuit (b) Waveform representation

Figure 4.9 shows cancellation circuit of V_{OS2}. The method is the same as above. C_r is the feedback capacitor and replaced by C in rotation. The output waveform is shown in figure. V_{out} decreases by Δ as one clock period passes. Although the gap of every step is correct but the initial value of V_{out} is still have V_{OS2} term. It will affect the output digital code of calibration circuit. Nevertheless, the problem will be solved in next paragraph.

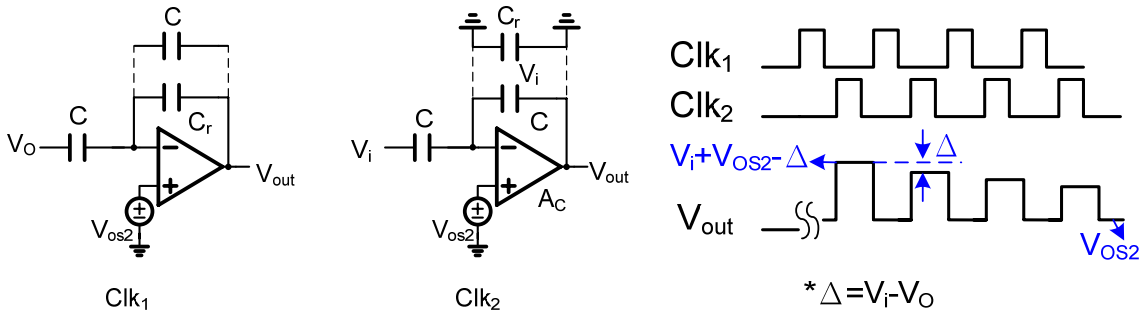
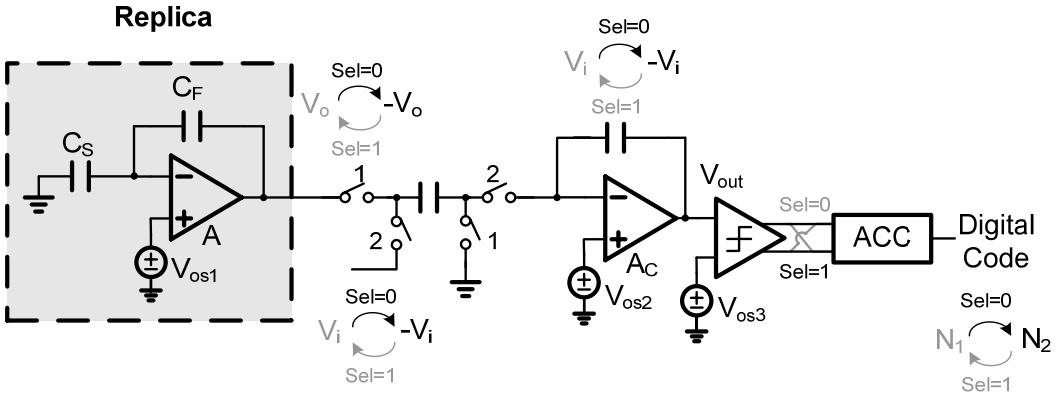


Figure 4.9 (a) V_{OS2} cancellation circuit (b) Waveform representation

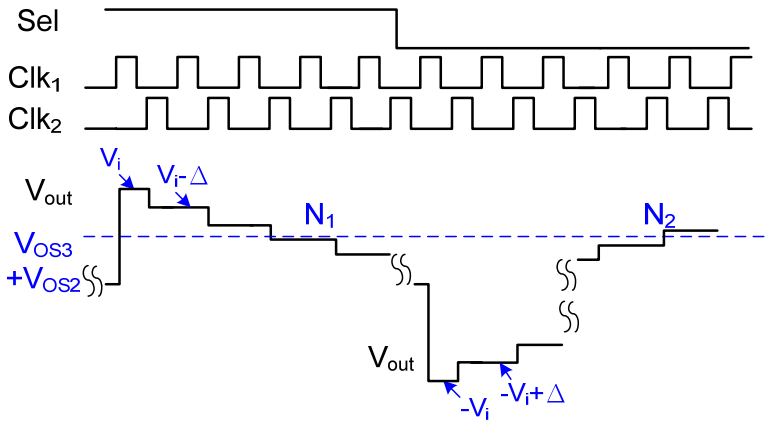
Finally, about V_{OS3} effect, we try to change polarity of input voltage in turns. Considering the V_{OS3} and residual V_{OS2} will be combined into a constant offset equivalently, offset affection can be cancelled by average operation. In positive polarity, Sel=1, V_i is positive input; On the other hand, Sel=0 means in minus polarity.

As figure 4.10 shows, during Sel=1 and Sel=0, digital output are N_1 and N_2, respectively. By average operation, calibration circuit output *n* is produced

$$n = \frac{N_1 + N_2}{2} \tag{4.7}$$



(a)

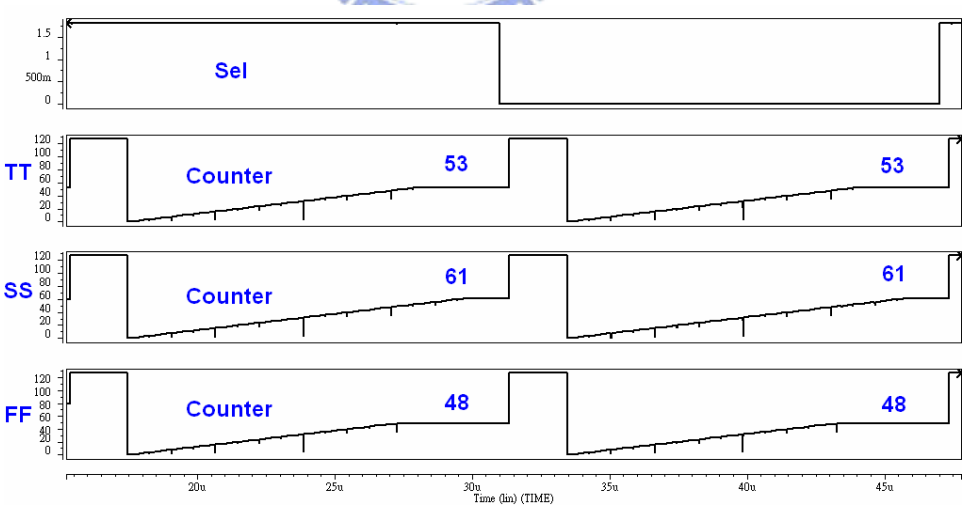


(b)

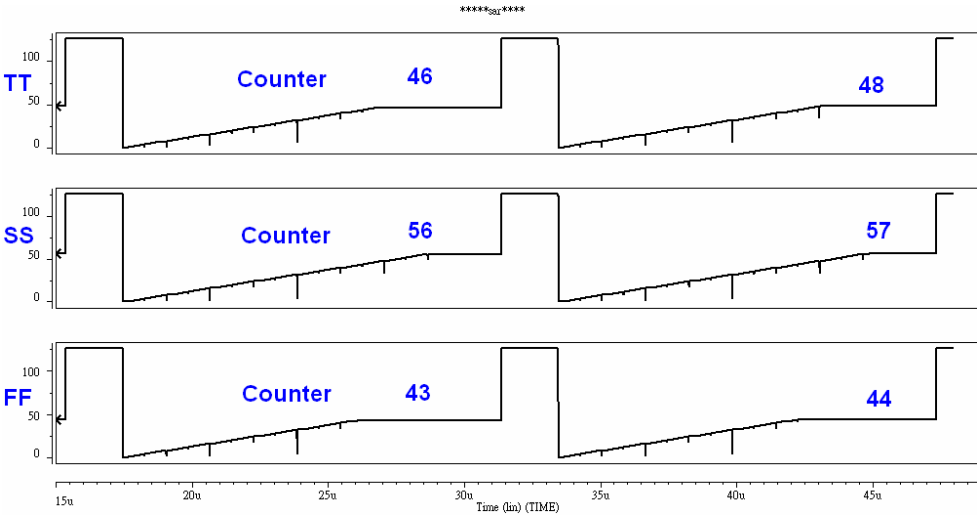
Figure 4.10 (a) V_{OS3} cancellation circuit (b) Waveform representation

4.5 Simulation Result

The simulation result of calibration circuit is shown in figure 4.11(a) and (b). Figure 4.11(a) is pre-simulation result, because of no offset effect, the digital output is equal no matter Sel is changed or not. In post-simulation result, by layout couple capacitor effect, the digital output are less than figure 4.11(a) and different in Sel=1 and Sel=0 cases. After layout, digital output is 47 in TT corner, 56.5 in SS corner, 43.5 in FF corner.



(a)



(b)

Figure 4.11 Calibration circuit simulation result

(a) Pre-simulation (b) Post-simulation

CHAPTER 5

EXPERIMENTAL RESULT

5.1 Floor-planning and Layout

The experimental implementation of time-interleaved pipelined ADC has been integrated in a 0.18μm CMOS process. The active area of ADC is 0.9×0.9mm^2 and the die area is 1.45×1.5mm^2. Figure 5.1 shows the floor-planning and layout of the chip. A differential analog signal is applied to the FADAC at the top left side. The stage 1 through 8 and ends up are shown in the figure. Calibration circuit is at the bottom left corner. Output buffer is at the middle and clock generation is space at the top left corner. Additionally, bypass capacitor is used to stable the reference voltages which connect to each stage. No matter the input or output pads, ESD pads are applied. And in order to isolate the couple noise, we separate pads into analog and digital parts.

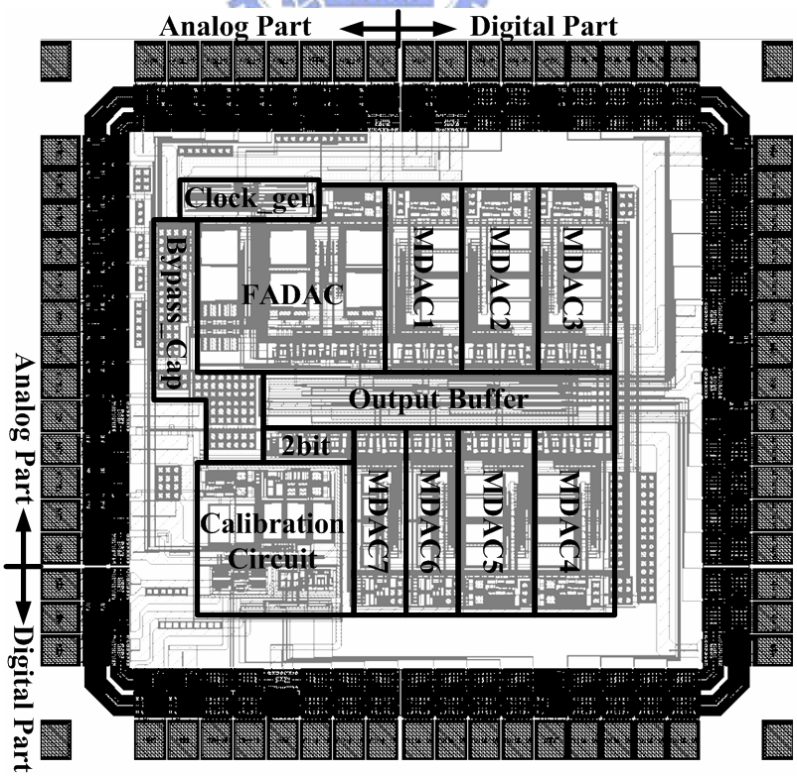
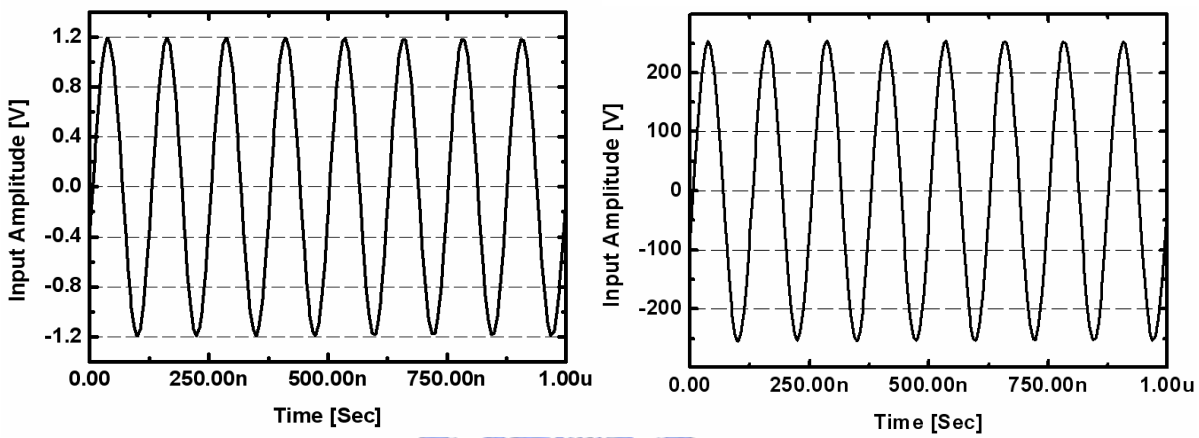


Figure 5.1 Floor-planning and layout

5.2 System Simulation Result

5.2.1 Time domain Simulation

Figure 5.2 shows the time domain simulation. Figure 5.2(a) is input waveform at amplitude is 1.2V and frequency is 8MHz. Figure 5.2 (b) is ADC digital output waveform. The output is reconstructed by ideal DAC and normalized from -128 to 128. The input and output waveform are almost the same and indicates the ADC function is correct.



(a) **(b)**

Figure 5.2 (a) Input waveform (b) Reconstructed output waveform

5.2.2 Dynamic Simulation

Figure 5.3 shows the pre-simulated and post-simulated FFT plot. The SNDR, SFDR, and ENOB at a 8MHz input and a 80MS/s sampling frequency are shown in each top right corner of figure. Before calibration, the ENOB of ADC is above 7bit both of pre-simulation and post-simulation. With calibration on, the performance of ADC is increased to 8.7bit at least. The 3rd harmonic tone is suppressed obviously and the improvement due to calibration circuit is about 1.5bit. In figure (d), at 32 MHz, timing error due to capacitor couple effect after layout is about 70dB. In the calibration operation, the accuracy of division operator is set to be 14bit, calibration circuit digital output are set 53 and 47 while pre-simulation and

post-simulation, respectively.

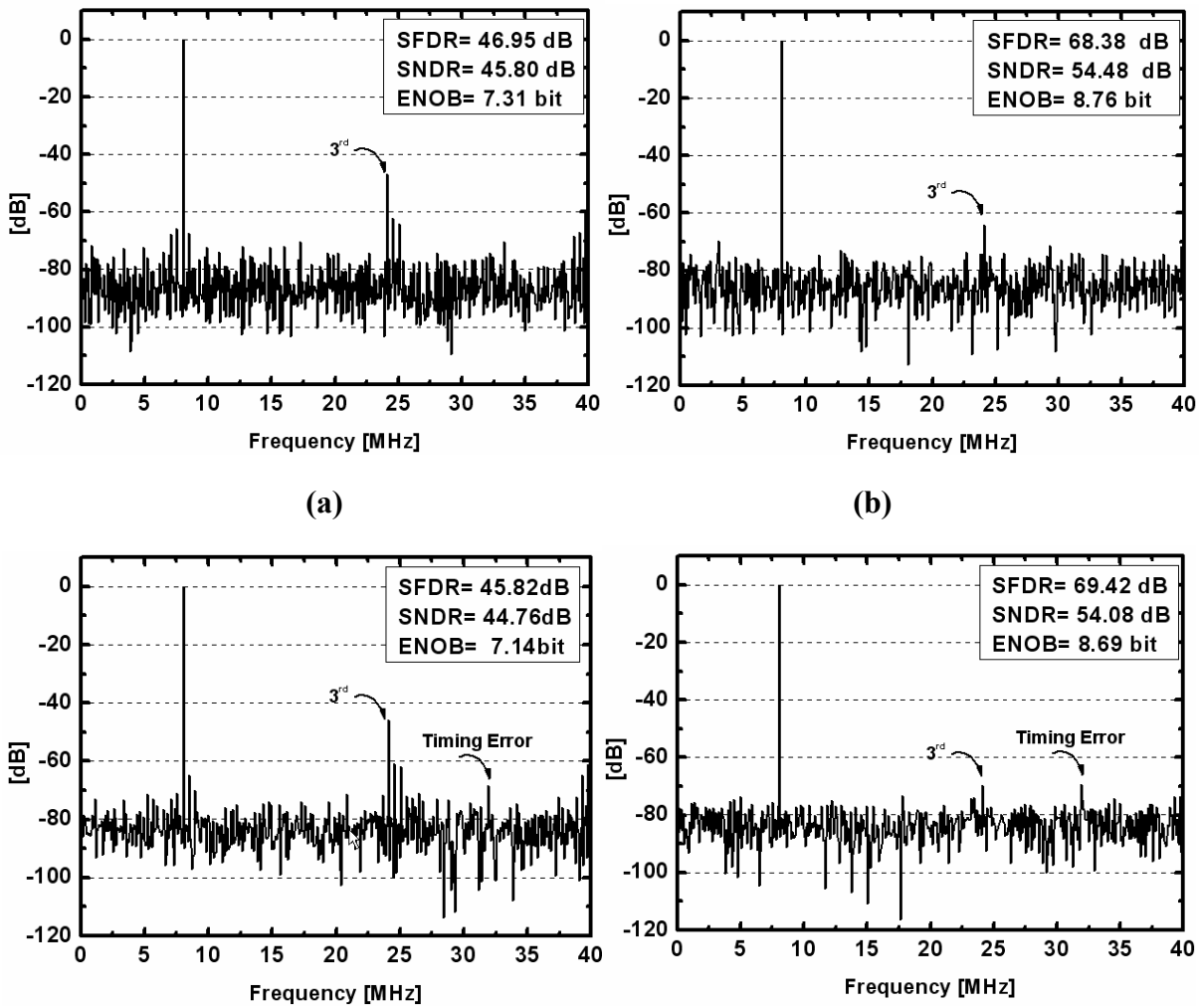


Figure 5.3 Simulated FFT in input frequency=8MHz,

Sampling rate=80MS/s

(a) Pre-simulation and calibration OFF (b) Pre-simulation and calibration ON

(c) Post-simulation and calibration OFF (d) Post-simulation and calibration ON

The relation between frequency of sampling clock and ADC performance is shown in figure 5.4. Lower line is without calibration curve and upper line is after calibration curve. It shows that the improvement due to calibration circuit can hold out 1.5bit when sampling frequency is lower than 80MS/s. When sampling frequency is above 80MS/s of, the efficiency

will degrade due to signal is not settled in each stage of ADC.

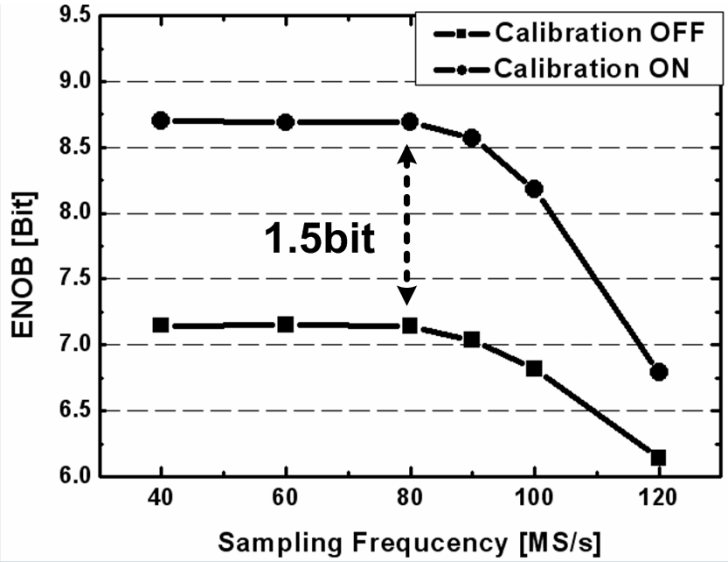


Figure 5.4 Post-simulated ENOB vs. sampling frequency

Then, discuss with affection of calibration output to ADC ENOB. From figure 4.8 of chapter 4, digital output of calibration circuit after layout is 47. By changing the digital output code from low to high, figure 5.5 shows the curve of improvement after calibration at input frequency is 8MHz and sampling frequency is 80MS/s. Without calibration, the ADC performance is 7bit. With the calibration on, the improvement is up to 1.5 bit at the calibration output is 47 and decreases with calibration output goes high or low.

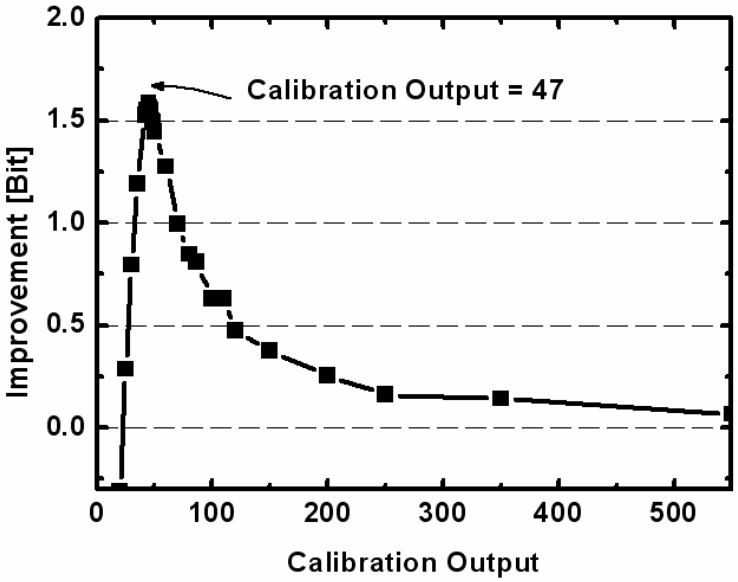
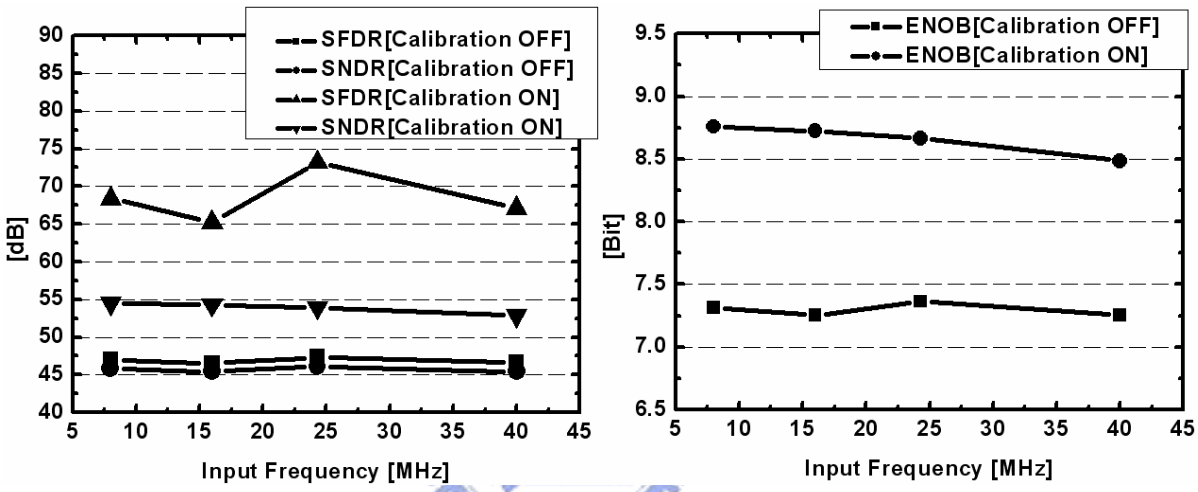
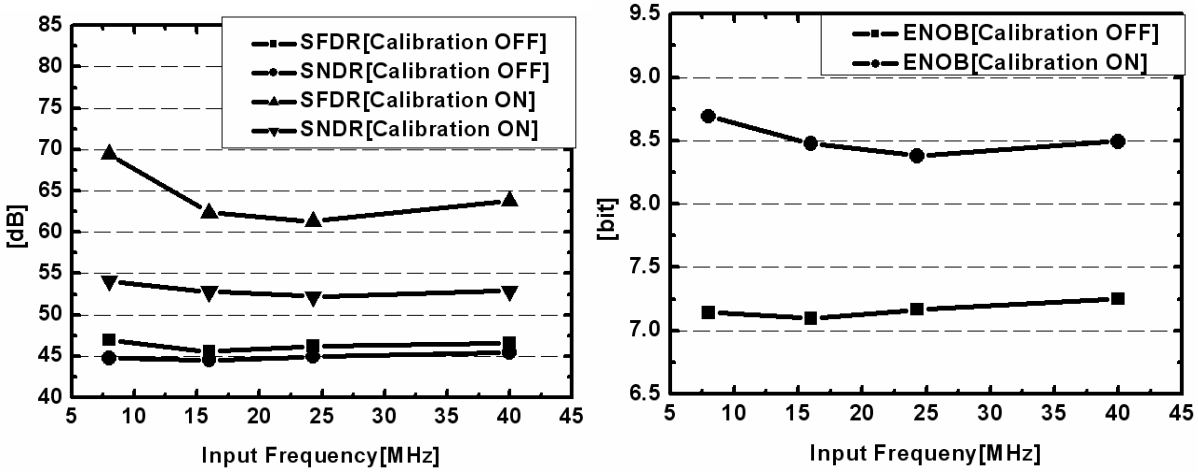


Figure 5.5 Improvement vs. calibration output digital code with calibration ON

Increase the input frequency up to half clock rate to plot the dynamic performance curve. Figure 5.6(a) is pre-simulation result, input frequency is from 8MHz to 40MHz, SFDR and SNDR is about 45dB and ENOB is about 7bit without calibration. When calibration on, SFDR and SNDR are obviously boosted to above 60dB and 52dB, respectively. And the ENOB is improved to 8.6 to 8.4bit with input frequency goes high. Figure 5.6(b) is post-simulation result, it also have the same tendency as curves in figure 5.6(a). The improved ENOB is from 0.5 to 0.8bit.



(a)

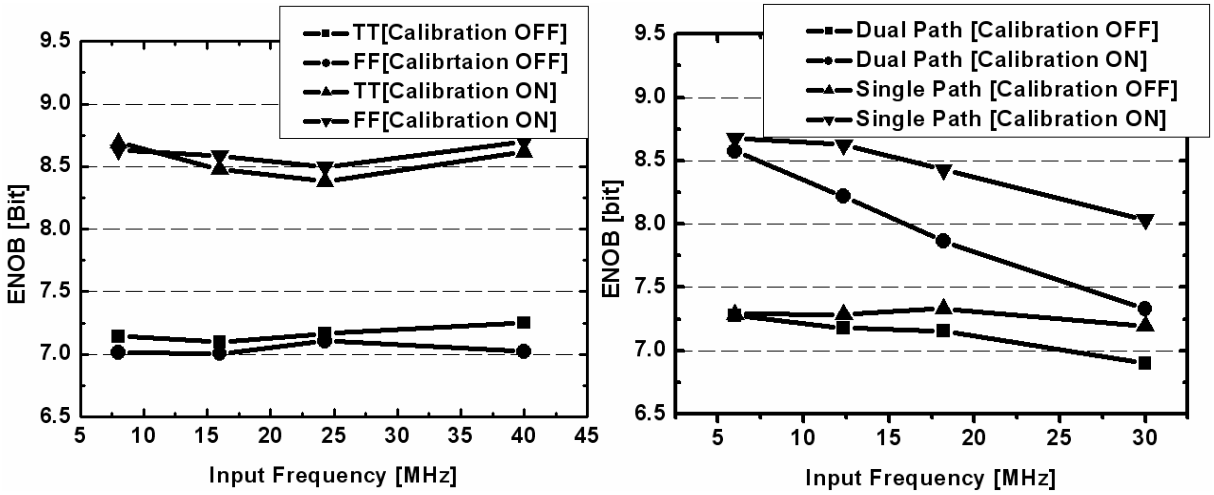


(b)

Figure 5.6 (a) Pre-simulation of SFDR, SNDR, and ENOB vs input frequency

(b) Post-simulation of SFDR, SNDR, and ENOB vs input frequency

Variation from foundry will affects characteristic of transistors, so corner simulation is also needed. Figure 5.7(a) shows the TT and FF simulation result. Basically, the two corner curves have the same tendency. Before calibration, ENOB is about 7 bit, and after calibration ENOB is about 8.4bit. The total calibration improvement is 1.4bit. Figure 5.7(b) is simulated in corner SS. Due to parasitic effect and timing error between two paths, sampling rate decreases to 60MS/s and one path is chosen to analyze in order to have the same performance as corner TT and FF. Equivalently, the ADC operates at sampling rate is 30MS/s. In the above-mentioned, the calibration digital output is applied with 47 in TT corner, 56.5 in SS corner, 43.5 in FF corner.



(a) **(b)**

Figure 5.7 Corner of post-layout simulation

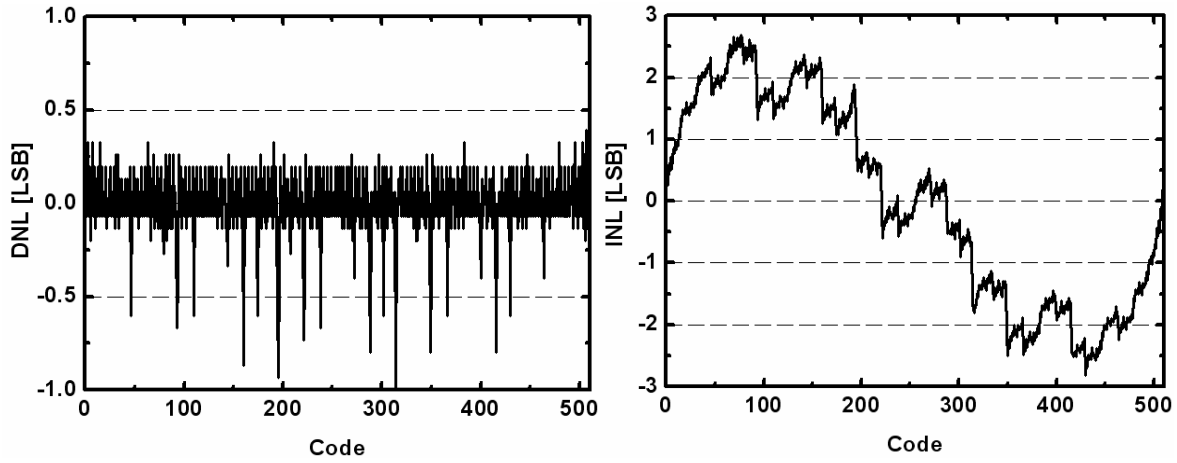
(a) Sampling frequency is 80MS/s in TT and FF corners

(b) Sampling frequency is 60MS/s in SS corner

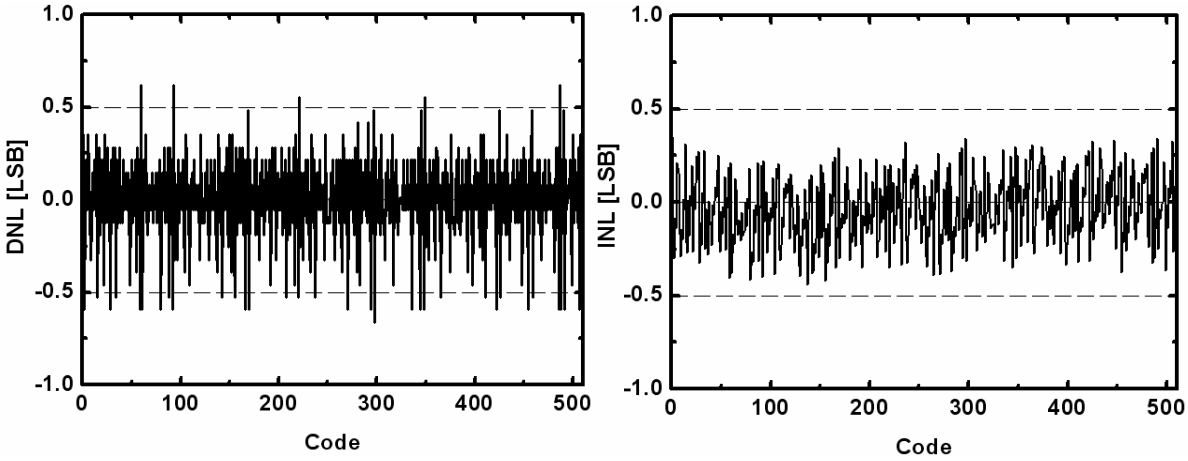
5.2.3 INL and DNL

INL and DNL show the non-linearity performance of pipelined ADC. Figure 5.8 (a) is before calibration, because gain error of opamp, DNL has missing code and INL is about ±3LSB. After calibration, Figure 5.8(b), the missing code in DNL is disappeared and INL is

improved to be less than ±0.5LSB, obviously. The LSB is 9bit resolution to full scale input.



(a)



(b)

Figure 5.8 INL and DNL

(a) Before calibration (b) After calibration

5.2.4 Dynamic Range

Figure 5.9 shows the dynamic range simulation result. Two curves with and without calibration are almost the same while input signal level is low. While input level becomes higher, the two lines will separate because gain error dominates in lower line. The dynamic range shown in figure is about 60dB.

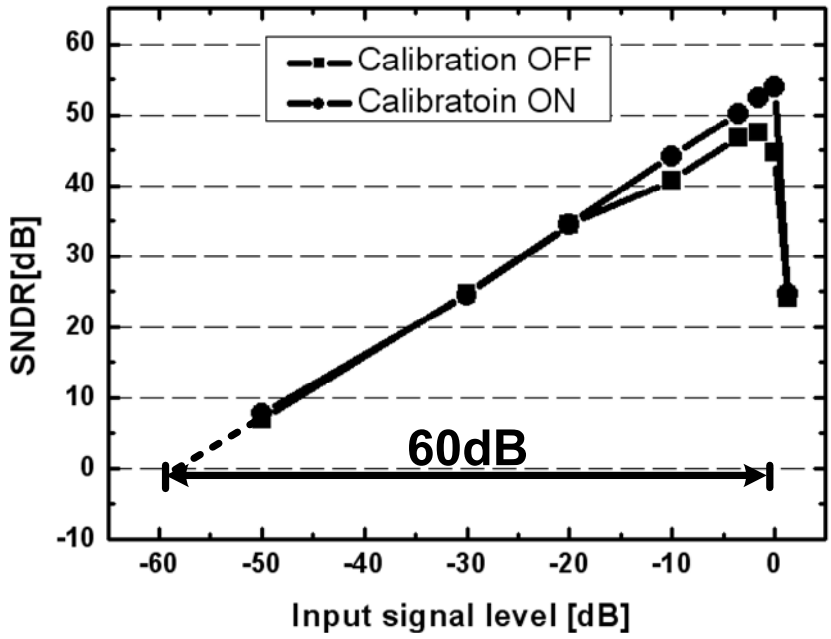


Figure 5.9 Dynamic range

5.2.5 Specification Table

Table 5.1 shows the performance summary simulated in 0.18μm CMOS process. The conversion rate is 80MS/s and resolution is 9bit. In post-simulation, the ENOB is 8.76bit and 8.69bit at input frequency is 8MHz and 40MHz, respectively. The total power added by ADC core, clock generator, and calibration circuit is 11.5mW. The FOM is defined as

$$FOM = \frac{Power}{2^{ENOB} \times Conversion\ rate} \tag{5.1}$$

In this design, the FOM is 0.40pJ/Setp at input frequency is 40MHz and 0.35pJ/Setp at input frequency is 8MHz at post-simulation.

Table 5.1 ADC specification of pre-simulation and post-simulation

	Pre-simulation	*Post-simulation*
Technology	0.18μm CMOS process	
Resolution	9bit	
Supply voltage	1.8V , 1V	
Signal swing	+/-300mV	
Conversion rate	80MS/s	
SNDR	54.49dB @ 8MHz input 52.84dB @ 40MHz input	54.1dB @ 8MHz input 52.89dB @ 40MHz input
ENOB	8.76bit @ 8MHz input 8.49bit @ 40MHz input	8.69bit @ 8MHz input 8.48bit @ 40MHz input
Power consumption	6.3mW [ADC core] 4.0mW [Clock generator] 1.2mW [Calibration Circuit]	
	11.5mW [Total]	
FOM⁎ (pJ/Step)	0.33 @ 8MHz input 0.40 @ 40MHz input	0.35 @ 8MHz input 0.40 @ 40MHz input

$$*FOM = \frac{Power}{2^{ENOB} \times Conversion\ rate}$$

5.3 Experimental Result

5.3.1 Measurement Consideration

Figure 5.10 depicts the measurement setup used to assess the performance of the experimental low voltage pipelined ADC described in this work. The supply voltages for both analog and digital parts to the board are generated by the power supply. In order to prevent the digital noise coupling to the analog circuits, analog and digital powers are isolated to each other in the PCB board. The input signal is provided by a high performance signal generator, Agilent E4438C and system clock is supplied by pulse generator, Agilent 8133A. Otherwise, the output bit streams are fed to the logic analyzer, Agilent 16700. The digital data stored in the logic analyzer is subsequently download to a personal computer and processed by

MATLAB, including of calibration and FFT analysis.

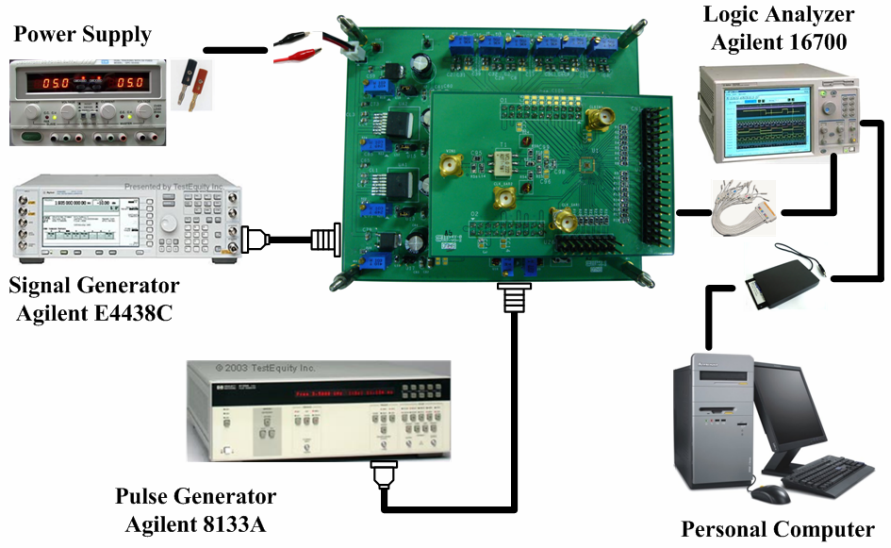


Figure 5.10 Measurement consideration

5.3.2 Experimental Result

Figure 5.11 shows the chip microphotograph of the fabricated ADC. The chip dimensions are 1.45×1.55 mm^2 and the active area is 0.85×0.9 mm^2. Operating at a 40MS/s sampling rate under 1.8 and 1V power supplies, the total analog circuit consumes a total of 7.3mW and digital circuit consumes 4.2mW.

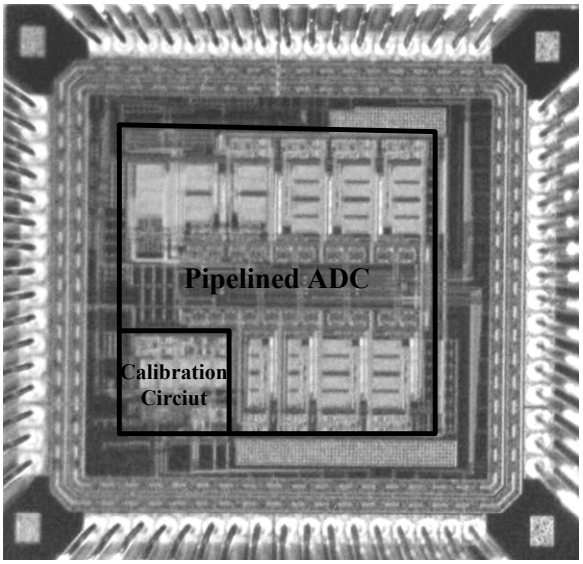
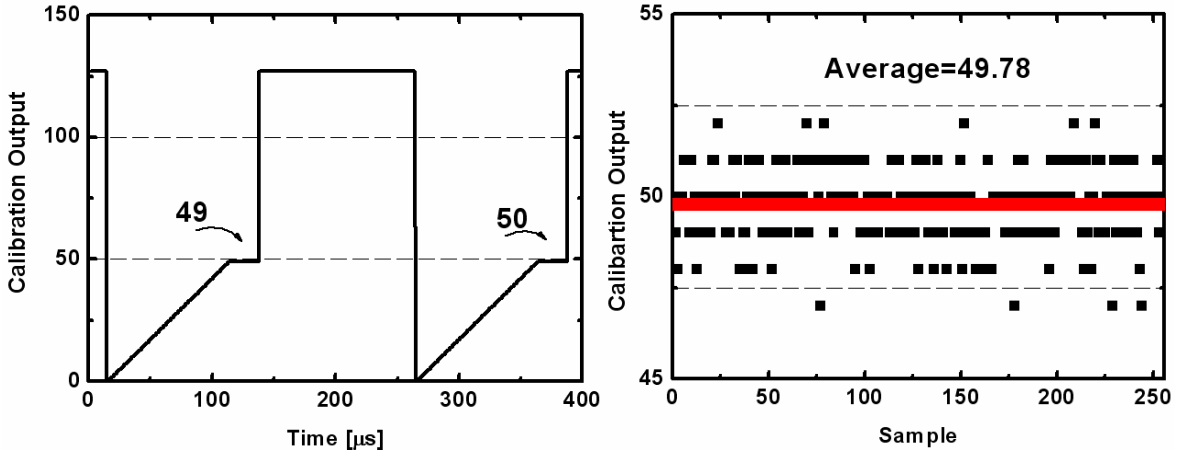


Figure 5.11 ADC chip microphotograph

Figure 5.12 shows the measured calibration circuit output. Figure 5.12(a) is at transient state and Figure 5.12(b) averages the outputs by 512 samples to suppress the noise. The value 49.78 is close to the post-simulation result.



(a) (b)

Figure 5.12 The measured calibration circuit output

Figure 5.13 shows the ADC's differential nonlinearity (DNL) and integral nonlinearity (INL) characteristics obtained from code-density measurements. The LSB is normalized to 9bit resolution in those figures. The number of registered output code is 16384. Figure 5.12 shows the ADC's native DNL and INL before activating the off-line calibration. The DNL is +1.2/-0.8 LSB and INL is +4/-4 LSB. Figure 5.14 shows the ADC's DNL and INL after calibration is activated. The DNL is +1.1/-0.8LSB, and the INL is reduced to +1.3/-1.3 LSB.

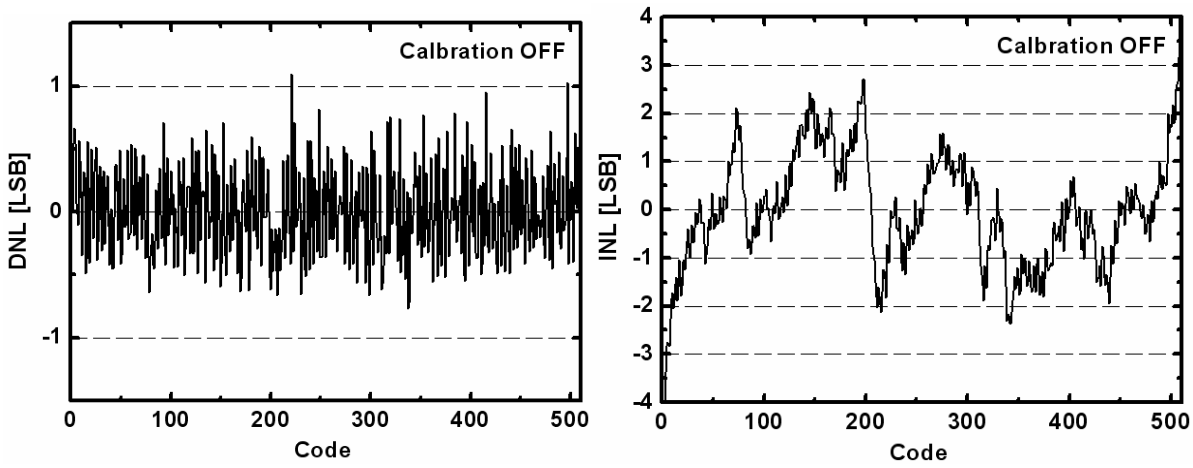


Figure 5.13 Measured DNL and INL at 80MS/s with calibration off.

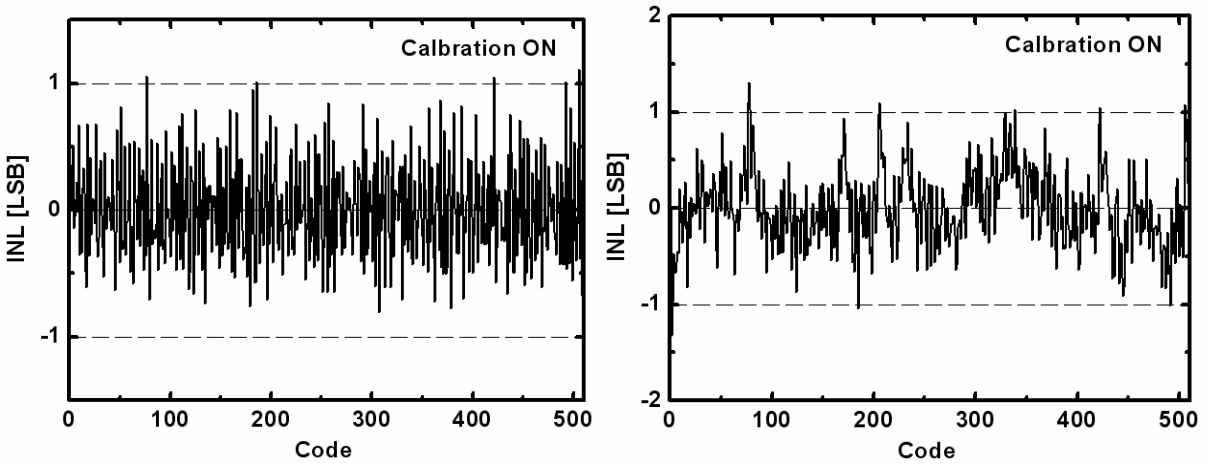


Figure 5.14 Measured DNL and INL at 80MS/s with calibration on.

Figure 5.15 shows the ADC's output fast Fourier transform (FFT) spectra at a 80MS/s sampling rate. The input is differential 600mV$_{PP}$ 1MHz sinusoidal signal. Without calibration, the third-order harmonic is the dominant distortion term, which is -46.4dB below the fundamental signal. The signal-to-distortion-plus-noise ratio (SNDR) is 42.3dB and the spurious-free dynamic range (SFDR) is 46.4dB. After calibration is activated, the SNDR is improved by 42.3dB to 46dB and the SFDR is improved by 46.4dB to 54.7dB. Notably, the ADC's noise level and timing error remain almost the same before and after calibration. The SNDR/SFDR improvement after calibration comes from the elimination of harmonic tones.

Figure 5.16 shows the ADC's measured SNDR and SFDR versus input frequencies at a 80HS/s sampling rate. The SNDR and SFDR decrease up to the Nyquist frequency because of aperture jitter dominating the performance. Generally, the calibration can improve the SNDR by 4dB and the SFDR by 10dB at low input frequency. Figure 5.17 shows the ADC's SNDR versus input signal level with calibration on and off respectively. The 1MHz input is sampled at 80MS/s. The figure 5.17 reveals that the measured dynamic range is 52dB. The figure 5.18 shows the measured ENOB versus sampling frequencies at a 1MHz sinusoidal signal. With increasing sampling rate above 80MS/s, the performance deceases below 7 bit after calibration is activated.

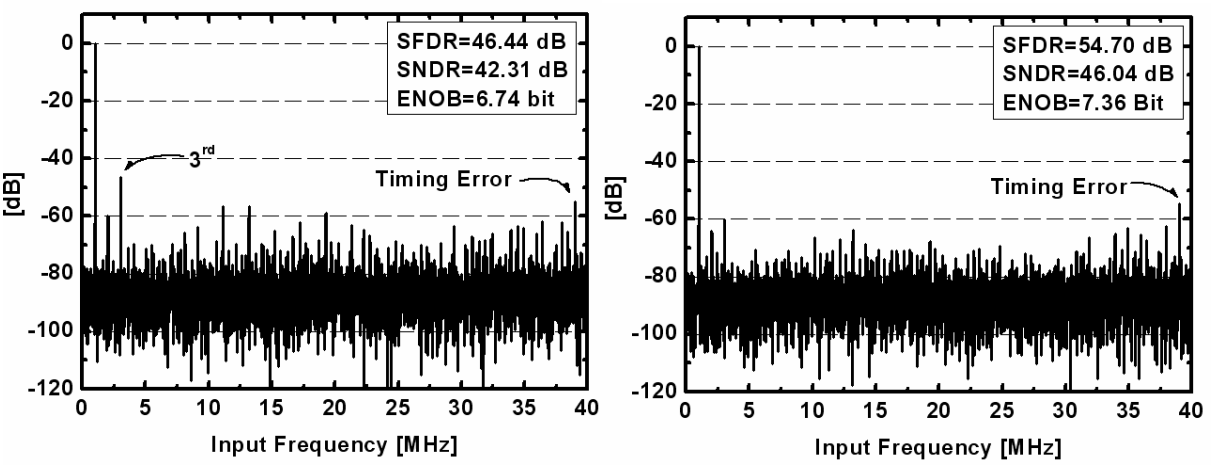


Figure 5.15 Measured output FFT spectra.

The 600mV$_{PP}$ 1MHz differential sinusoidal input is sampled at 80 MS/s.

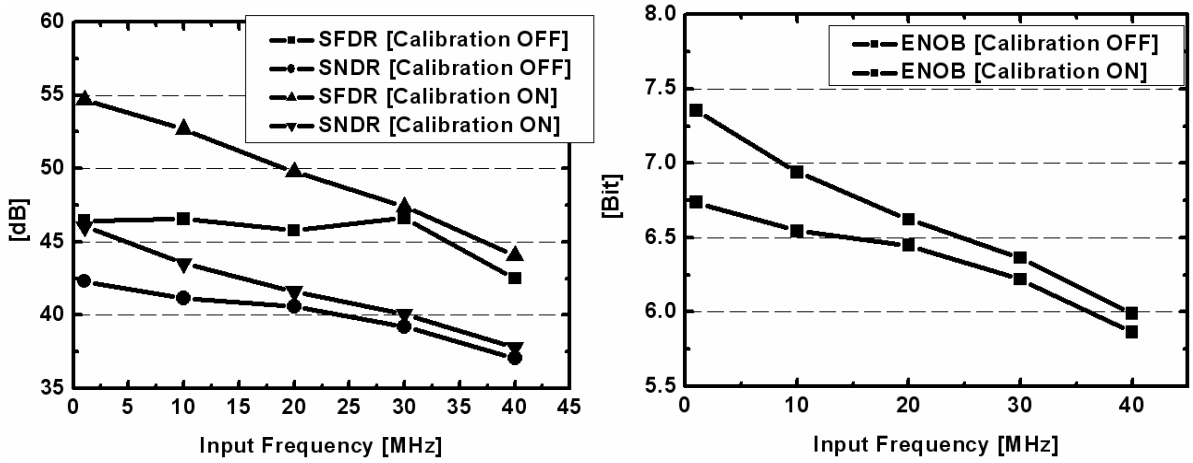


Figure 5.16 Measured SFDR,SNDR, and ENOB versus sinusoidal input is sampled at 80 MS/s.

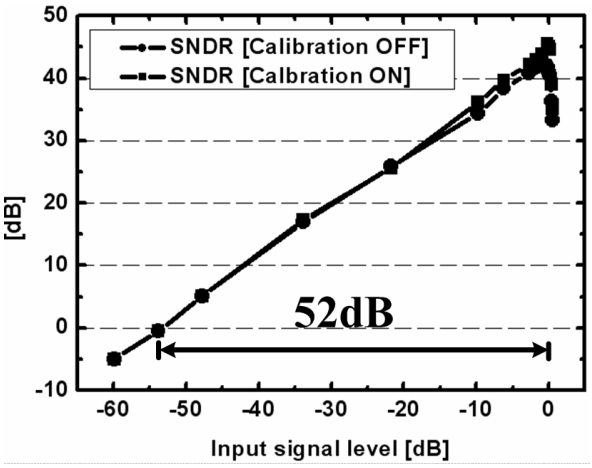


Figure 5.17 Measured SNDR and SNR versus input level. The 1MHz differential sinusoidal input is sampled at 80 MS/s

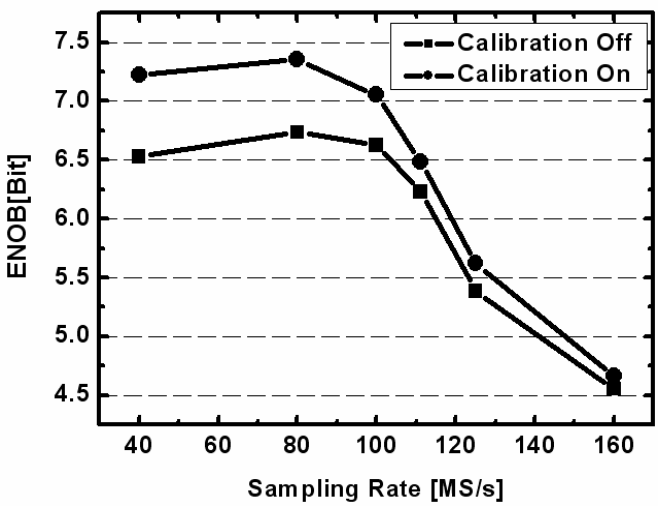


Figure 5.18 Measured SNDR and SNR versus input level. The 1MHz differential sinusoidal input is sampled at 80 MS/s

CHAPTER 6

CONCLUSION

Table 6.1 summarizes the measured performance of the ADC prototype at room temperature. The power supplies are 1.8V and 1V. With calibration on, the SNDR is 46.0dB and ENOB is 7.35bit at sampling rate is 80MS/s and input frequency is 1MHz. The FOM shows 0.88pJ/step. Compare to other references shown in table I, the performance is 4 times less than [4] and [7] but is similar to reference [1] under the same technology.

Table 6.1 Performance summary of ADC at room temperature

	2007 ISSCC[7]	2005 ISSCC[1]	2007 ISSCC[4]	This Work	
				Simulation	Measurement
Technology	90nm	0.18 μm	90nm	0.18 μm	0.18 μm
Supply Voltage	0.8V	1.8V	1V	1.8V,1V	1.8V,1V
Resolution	10bit	10bit	10bit	9bit	9bit
Conversion Rate	80MS/s	125MS/s	30MS/s	80MS/s	80MS/s
SNDR	55dB	53.7dB	58.4dB	54.1dB	46.0dB
ENOB	8.8bit	8.6bit	9.4bit	8.69bit	7.35bit
Signal Swing	+/-600mV	-	+/-500mV	+/-300mV	+/-300mV
Power Consumption	6.5mW	40mW	4.7mW	11.5mW	11.5mW
FOM(pJ/Step)	0.18	0.82	0.23	0.35	0.88

$$FOM = \frac{Power}{2^{ENOB} \times Conversion\ rate}$$

The low power 9bit, 80MS/s pipelined ADC was fabricated using a 0.18μm 1P6M CMOS technology, and occupied an area of 1.45×1.55mm^2. The techniques implemented in this design are summarized below:

(1) FADAC replaces the front-end sample and hold can save power and achieve higher accuracy of ADC by 1bit.

(2) Opamp scaling in last 2 stages is for power saving.

(3) A novel 1V OP with split G_m stage for gain enhancement by above 10dB.

(4) Double edge sampling operation doubles the conversion rate and makes efficient utilization of opamp.

(5) Improving accuracy of calibration circuit by chopper averaging and input offset cancellation.

(6) With calibration on, INL improved by 3X and ENOB improve by 0.6 bits (2 bits by simulation).

The total ADC consumes 11.5mW under 1.8V and 1V power supplies. It achieves an SFDR of 54dB and an SNDR of 46dB. The calibration circuit can improve SFDR by 10dB and SNDR by 4dB. The SNDR is limited by non-linearity opamp gain, timing error between two paths and coupling noises. The maximum sampling rate is limited by the speed of the opamps. The aperture jitter dominates the performance while the input frequency goes high.

The ADC achieved good FOM of 0.88pJ/conversion at 80MS/s sampling rate and 1MHz sinusoidal input with 1.8 and 1V power supplies. Typical differential nonlinearity (DNL) and integral nonlinearity (INL) are +1.1/-0.8LSB and +1.3/-1.3LSB, respectively.

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