國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

用於 WiMax 之互補金氧半類比基頻電路設計

A CMOS Analog Baseband Design for WiMax

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摘　　要

本論文針對 WiMax 無線網路應用提出低功率高動態範圍類比基頻電路之設計。為了達到多頻寬和高增益範圍，我們用了可單級提供 30dB 增益高範圍的假指數之可變增益放大器(VGA)和可以改變頻寬從 0.625 MHz 到 14 MHz 的多頻寬濾波器(LPF)，在這濾波器中是由兩個轉導電路組成的元件合成的。在高動態範圍的架構下，以較少可變增益放大器串接級來達成低功耗和用轉導電容的濾波器來減少所需面積。最後用這 VGA 和 LPF 電路設計整個類比基頻電路並分析雜訊、線性度和干擾。經由 0.13-μm CMOS 和 1.2 伏偏壓的製程進行電路實作，這電路可提供 86dB 的最大功率增益、16dB 的最低增益值，並在 400mVpp 輸出電壓時約可得 40dB 全諧波失真。

ABSTRACT

This thesis presents a low-power high dynamic range design of CMOS analog baseband circuitry for WiMax applications. To achieve multi-bandwidth and high gain range, the proposed variable gain amplifier employs a wide-range pseudo-exponential circuit topology providing about 30dB dynamic per-stage, and the proposed LPF(Low Pass Filter) incorporates two adjustable transconductor achieving various cut-off frequency from 0.625MHz to 14MHz. With the proposed topology, the number of amplifier stages can be reduced and the level of power consumption is tremendously lowered, and the gm-c based LPF stage help to reduce area. Base on the proposed VGA and LPF, the topology of analog baseband is analized to consider the trade-offs among noise, linearity and interference. The circuit is implemented in 0.13-μm CMOS process, and provides a maximum forward gain of 86 dB and a minimum forward gain of 16 dB from a 1.2-V supply. The harmonic distortion is 38.19dB under the output signal magnitude is 400m Vpp.

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A CMOS Analog Baseband Design for WiMax

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Chapter 1

Introduction

WiMAX (Worldwide interoperability for Microwave Access) is a standards-based technology defined in IEEE 802.16-2004 and IEEE 802.16e-2005. It offers the delivery of last mile wireless broadband access as an alternative to wired broadband like cable and DSL[1]. Large cover range, high transmission rate and wide variety of applications are the most obvious characteristics of this new technology, and these characteristics will cause a revolution in internet accessing of "moving" mobile device, "last mile" network constructing and even the communication network recovering after disaster. The convenience of WiMAX system not only pushes consumers to buy equipments which support the service, but saves huge money by not constructing and maintaining wires of last mile network. Therefore an enormous market can be expected, and it excites tremendous academic and industrial researches interest.

1.1 Motivation

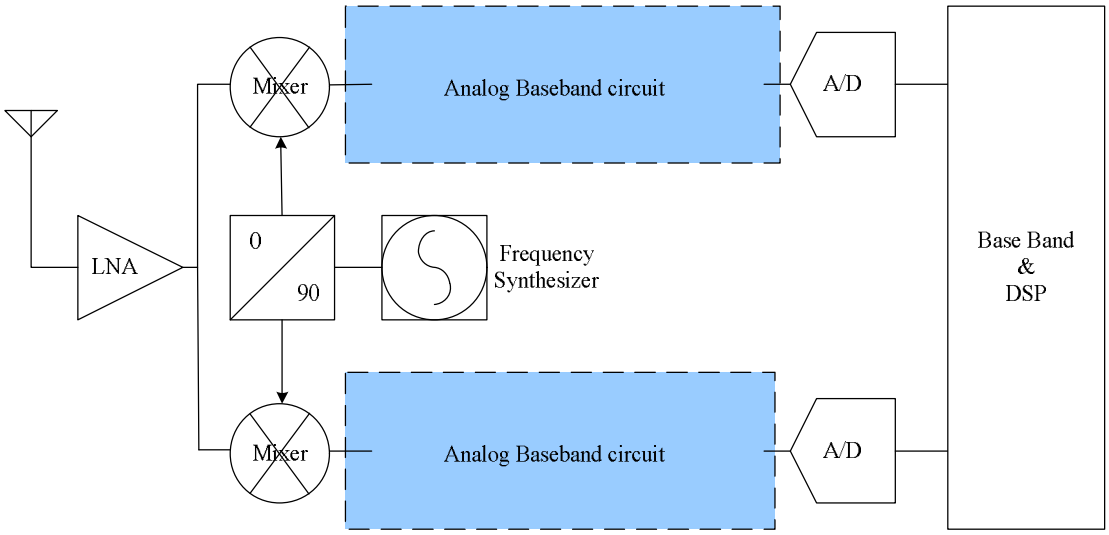


Figure 1 Proposed WiMax transceiver block diagram

For low power and low cost complementary metal-oxide semiconductor(CMOS) process can achieve this target. The analog baseband design is between mixer and ADC. It handles the signal that is downconverted from mixer, so the design needs low noise and analog baseband to have high dynamic range 50dB for 10 bit ADC. The WiMAX specification requires gain range 16~86dB and tunable cut-off frequency from 0.625M~14MHZ. For high gain range and controlling linearly on a decibel scale, the VGA employs pseudo-exponential circuit to generate exponential output current for linear control signal. Nevertheless, the intrinsic device transfer characteristic of a MOSFET is not logarithmic, and a pseudo-exponential approximation is required for CMOS VGAs. To tune the cut-off frequency of LPF, the LPF employs transconductor-C structure and the transconductors operate in triode region to linearty control the bandwidth.

1.2 WiMax System Requirements

Fig. 2 Shows the RF bands that can be used for WiMax. Figure shows licensed and unlicensed band, IEEE802.16e specifies only licensed bands for mobile application of WiMax. So the system that we design covers 2.3-2.7GHz. WiMax uses OFDM with modulations that can be adaptively changed among BPSK, QPSK, 16QAM, and 64QAM. The channel bandwidth is 0.625M, 0.875M, 1.5M, 1.75M, 2.75M, 3.5M, 4.375M, 5M, 7M, 8.75M, 10M, 12.5M, 14M with 13channels. Table 1 shows the channel bandwidth for different profiles. So the LPF in this system requires a tunable bandwidth technology to match the specification.

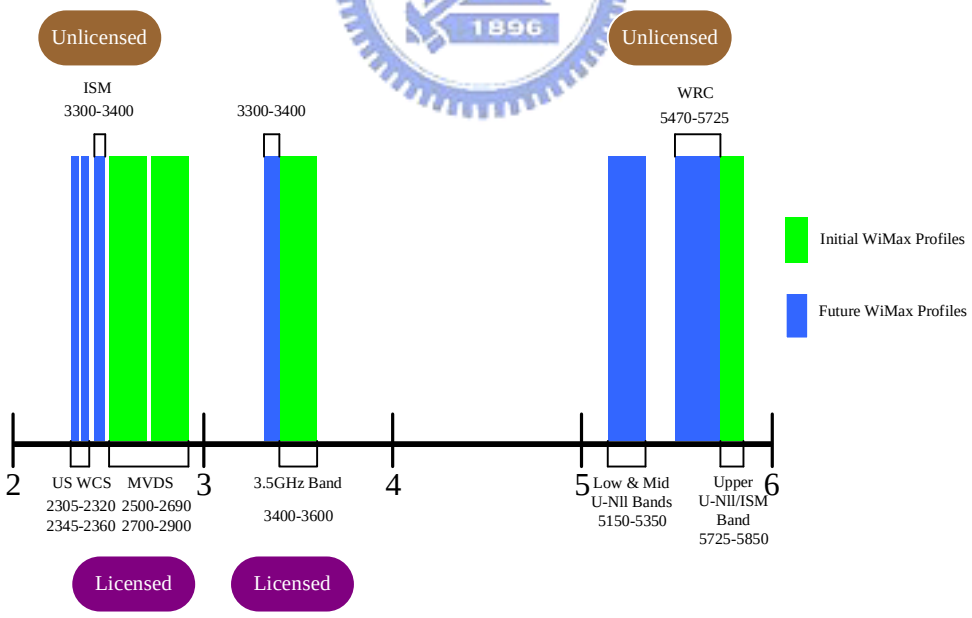


Figure 2 2GHz to 6GHz centimeter bands available for BWA [2]

A simple specification for a WiMax analog baseaband design is show at Table 1 Because the resolution of A/D converter is 10bit, hence the dynamic range (DR) is

required just more than 50dB.

	WirelessMAN-OFDM PHY	WirelessMAN-OFDMA
Channel bandwidth (MHz)	0.875, 1.5, 1.75, 2.75, 3.5, 5	0.625, 1.75, 3.5, 5, 4.375, 7, 8.75, 10, 14

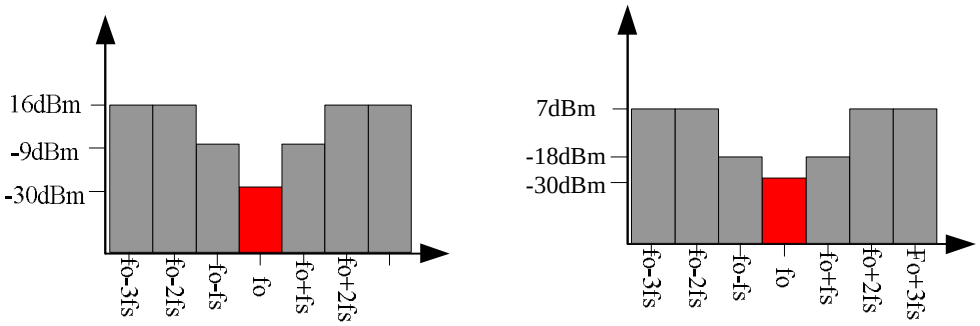
Table 1 Channel bandwidth for different profiles

Parameters	Spec.
Technology	CMOS 1.3um
Power supply	1.2V
3-dB bandwidth	0.625M~14MHz
Power consumption	As small as possible
Gain range	16dB-86dB
Out swing @ THD 50dB	400mVpp

Table 2 The specification for this analog baseband design

In addition, for the design considerations of adjacent and non-adjacent channel interference, the topology of analog baseband should be carefully arrange to meet both the linearity and noise Table 1.3 is minimum adjacent and alternate adjacent channel interference performance at BER 10^{-3} and 10^{-6}. From Table 3, Fig. 3(a) is the worst situation for BPSK blocker profile. From Table 4, Fig. 3(b) is the worst

situation for BPSK blocker profile. The maximum input signal power is defined as in 30dBm for WiMax specification.



(a) (b)

Figure 3 maximum adjacent channel interference C/I for BPSK blocker profile

	At BER 10^{-6} for 3dB degradation	At BER 10^{-6} for 1dB degradation
1^{st} adjacent channel interference C/I	BPSK:-21 QPSK:-18 16-QAM:-11 64-QAM:-4	BPSK:-17 QPSK:-14 16-QAM:-7 64-QAM:-0
2^{nd} adjacent channel interference C/I	BPSK:-46 QPSK:-43 16-QAM:-36 64-QAM:-29	BPSK:-42 QPSK:-39 16-QAM:-32 64-QAM:-25

Table 3 Minimum adjacent and alternate adjacent channel interference performance at BER 10^{-6}

	At BER 10^{-3} for 3dB degradation	At BER 10^{-3} for 1dB degradation
1^{st} adjacent channel interference C/I	BPSK:-21 QPSK:-18 16-QAM:-11 64-QAM:-4	BPSK:-17 QPSK:-14 16-QAM:-7 64-QAM:-0
2^{nd} adjacent channel interference C/I	BPSK:-46 QPSK:-43 16-QAM:-36 64-QAM:-29	BPSK:-42 QPSK:-39 16-QAM:-32 64-QAM:-25

Table 4 Minimum adjacent and alternate adjacent channel interference performance at BER 10^{-3}

1.3 Organization

The organization of this thesis is overviewed as follows. Chapter 2, firstly presents two topologies of analog baseband circuit with VGA and LPF. The design concepts of LPF with the proposed novel tunable frequency LPF technique are discussed. The VGA design with the novel high dynamic range VGA technique are also presented. Finally the optimum analog baseband architecture for interference and noise figure trade-off are analyzed. Chapter 3 describes simulation results of two topology and LPF measurement results. Chapter 4 concludes with a summary of contributions and suggestions for future work.

Chapter 2

Architecture of Analog Baseband

In order to meet the sensitivity of WiMax and the interference requirements, the dynamic range of adjacent channel, the analog baseband is severely affected by the arrangement of cascading of LPF and VGA. Some condition to design the analog baseband circuit like linearity, noise or interference. Section 2.1 discusses some arrangements of VGAs and LPF and compare the topology arrangements in terms of noise figure and interference. Section 2.2 discusses the design of tunable bandwidth LPF. Section 2.3 discusses the high dynamic range VGA. Section 2.4 discusses the optimum arrangement for interference and noise figure design trade-off.

2.1 Topology Analysis for Analog Baseband circuit

The design specification for total gain analog baseband is 16dB to 86dB. Generally a pseudo-exponential VGA stage can achieve 30dB gain range. So it requires three VGAs at least to meet the maximum gain specification. For low power

considerations, usage of a single LPF is preferred. The Architecture includes three VGAs and one LPF.

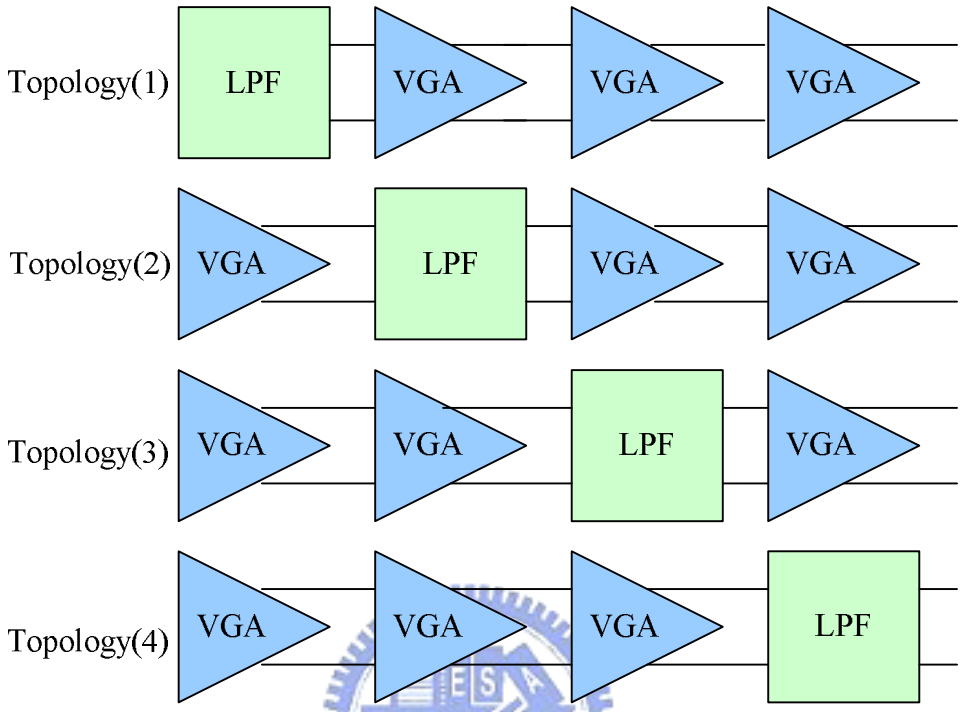


Figure 4 Four topologies for the analog baseband design

There are four ways to array the analog baseband as shown in Fig. 4. The design considerations are noise figure, linearity and in-band-distortion for determining the arrangement.

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \mathbf{K} + \frac{NF_m - 1}{A_{p1}\,\mathbf{L}\,A_{p(m-1)}} \qquad (2.1)$$

Equation (2.1) is Friis equation for cascaded stages. The gain of each VGAs is larger than 0dB but the gain of LPF is -3dB. So arranging LPF in the first stage, topology(1), will have the worst noise figure.

As for the linearity, each stage deals with signal with 40dB DR. The total circuit will produce a major tone and a second or third order harmonic tone that is less than

major tone about 40dB. If LPF has better linearity, saying DR is larger than 50dB, arranging LPF on the last stage will block the distortion produced by VGAs and the linearity of the total analog baseband circuit depend on the LPF.

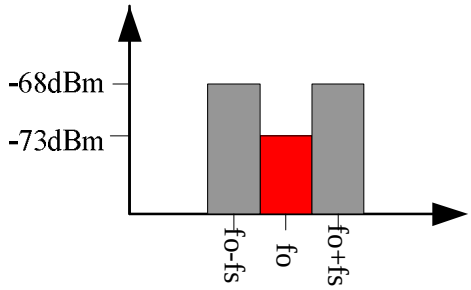


Figure 5 Example for QPSK blocker profile

Fig. 5 is one example of signal and interference situation for QPSK blocking profile in WiMax. When the signal comes from LNA and Mixer, adjacent channel interference may be larger than the desired signal. It means the interference may be so large as to make VGA into saturation without any rejection by LPF. Arranging LPF on the first stage, topology(1) will block adjacent channel interference in advance and avoids the VGAs getting into saturation.

From above-mentioned conditions, noise figure and interference are the trade-off. If LPF is in the first stage, noise figure is the worst. Whereas LPF is in the last stage, VGA may be driven into saturation. Table 5 shows the comparison of noise figure and adjacent channel interference. The optimum arrangement depends on the practical parameters LPF and VGA as well as the system requirements of noise and

interference. We'll discuss further for the optimum arrangement after the design of LPF and VGA.

	Topology(1)	***Topology(2)***	***Topology(3)***	***Topology(4)***
Noise Figure	***Bad***	***medium***	***Medium***	***good***
Distortion	***Good***	***medium***	***Medium***	***bad***

Table 5 Comparison with noise figure and in-band distortion

2.2 Tunable bandwidth LPF design for WiMAX

In this section, a tunable bandwidth LPF is presented. The LPF is an elliptic fifth-order transconductor-C filter. Using transconductor-C topology can adjust bandwidth easier without many switches and is able to reduce the capacitor. Section 2.2.1 presents the tunable bandwidth technique with transconductor-C cell. Section 2.2.2 presents the design of transconductor. Section2.2.3 presents the simulation result of the LPF.

2.2.1 Tunable bandwidth requirements for WiMAX

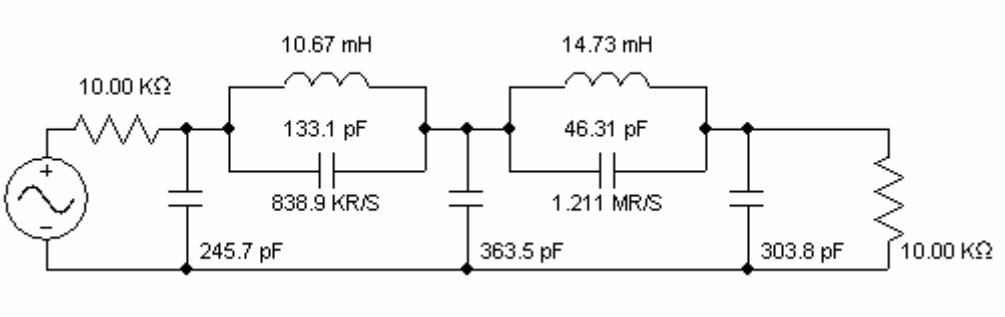


Figure 6　A 0.625 MHz passive LPF

Fig. 6 is a passive LPF and the cut-off frequency is 0.625M Hz. Passive LPF is a basic topology and has the best linearity, but it needs larger area for the inductors and capacitors. For changing the bandwidth of passive LPF, lots of devices such as resistor and inductor have to be tuned at the same time. So designing tunable bandwidth LPF requiresmore switches and larger chip area.

In this design we use transconductor-C topology to implement the LPF. Transconductor can replace the resistors and inductors, hence the LPF only contains gm blocks and capacitors. Fig. 7 and Fig. 8 show the common replacement of resistance and inductance by Gm blocks.

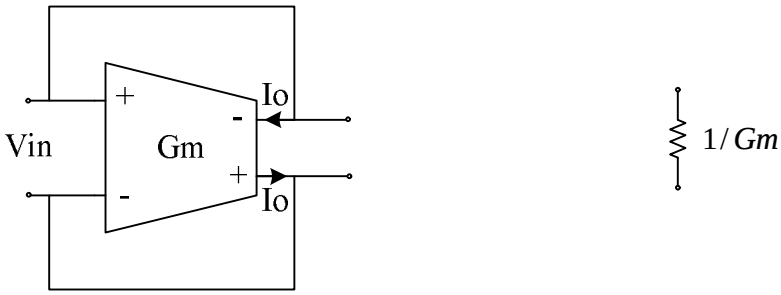


Figure 7　Differential Gm connected as resistance

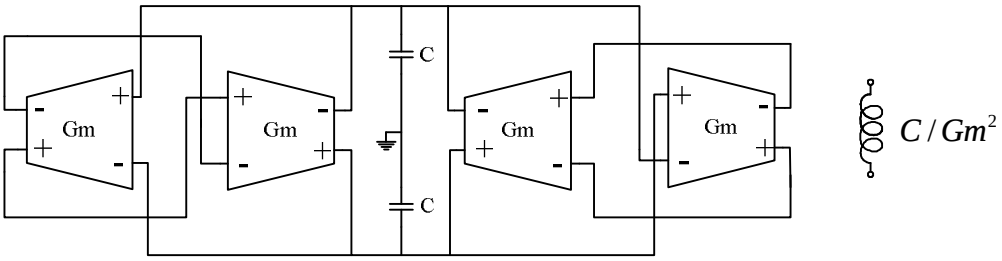


Figure 8 Differential Gm are connected as inductance by gyrator approach

Tuning the bandwidth of the LPF can be done by tuning the value of the gm, and then the bandwidth will be linear to gm. In the design, the bandwidth range of LPF is 0.625M ~ 14M Hz so the gm need to magnify 22.4 times. In order to decrease the difficulty of signal transconductor and increase the linear range of Gm cell,therefore, two transconductors are employed achieve the range of gm. Fig. 9 shows the transconductor-C LPF and each transconductor block contains both large and small transconductors. A small transconductor employ as a buffer after the LPF and increase a little gain.

For the same inductance value, the smaller transconductor enables less capacitance as well as small area, however, smaller transconductors are subject to noise and process variation. Therefore the gm range of small gm is edited to l0u ~50u (A/V) and for the large gm is 30u~224u (A/V).

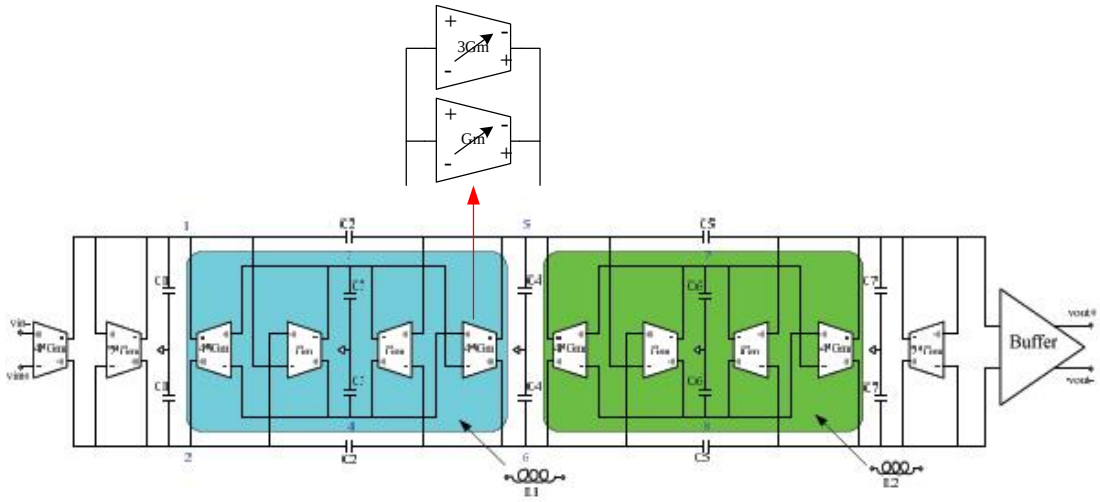


Figure 9 5^{th} order gm-c LPF

2.2.2 Tunable bandwidth transconductor design

For the tunablility of gm cell, a triode-biased MOS is adopted supply a linear gm [3].

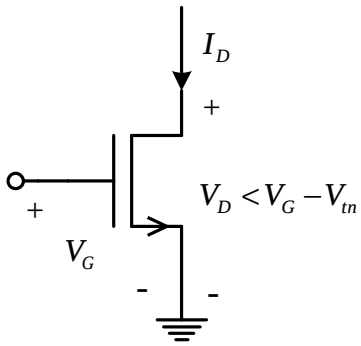


Figure 10 Single NMOS operating in triode region

Fig. 10 is a NMOS operating in triode region and has high linearity between the gate voltage and the drain current. The transconductance of the **transconductor** is the small- signal gate transcinductance, equation is as below:

$$Gm = gm @ \frac{dI_D}{dV_G} = bV_D$$

$$I_D = mC_{ox}W/L\left[(V_G - V_{tn})V_D - \frac{1}{2}V_D{}^2\right]$$

b is $mC_{ox}W/L$ for the NMOS. It can be observed the characteristic of linearity in voltage-to-current transfer characteristic is obtained and be controlled by drain voltage.

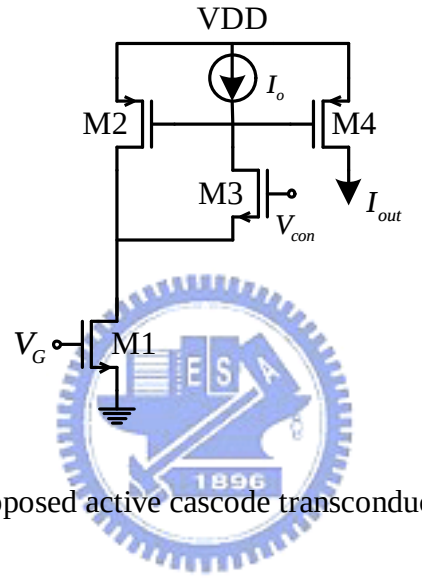


Figure 11 Proposed active cascode transconductor half circuit

Fig. 11 is a active-cascode transconductor core. M1 is a triode-biased transistor, its drain voltage is set by the control voltage V_{con}. M2 and M3 have feedback loop to stabilize the circuit. Current source I_o provides a little current which make M3 operate in weak inversion and M3 doesn't share the current of M1. The gm of M1 can be controlled and linear to the gate voltage of M3. M2 and M4 mirror the signal current to the output. M14 and M15 are the switches to switch the small and big transconductors. Input swing is limited by V_{con} and $V_{G_1} - V_{tn} > V_{D_1} = V_{con} - V_{tn}$ to avoid M1 into saturation region. The transconductance of the haft circuit is

$$Gm = gm_1 \times \frac{gm_4}{gm_2}$$

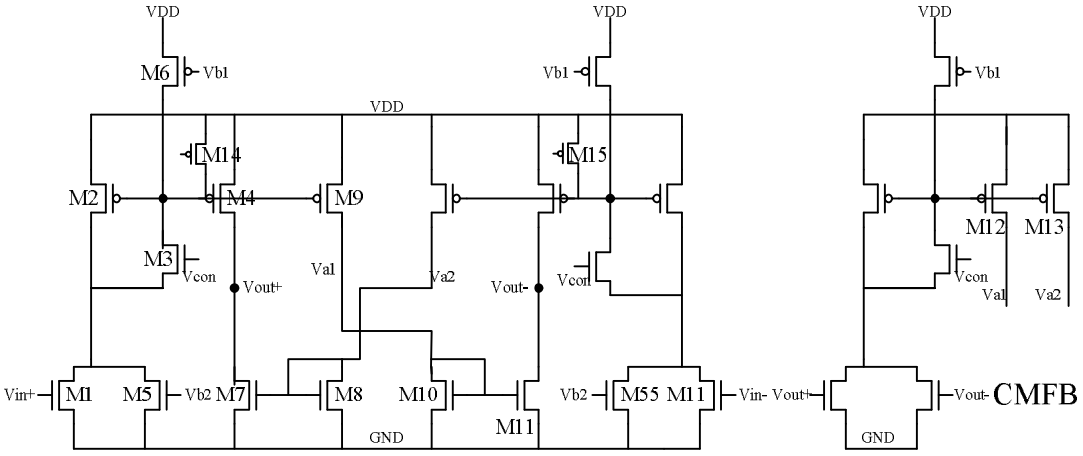


Figure 12 Fully differential active-cascode transconductor circuit and CMFB

The transconductor is showed in the Fig. 12. M1 is the input transistor. M5 is an active load to share the signal and increase the linear range. In the VGA design M1, M5, M11 and M55 are four input transistors for two differential small VGA circuit. M3 operate in weak inversion to control the drain voltage of M1 and M5. M6 is the current source. M2, M4 and M9 are the current mirror. M9, M10 and M11 provide negative current signals and connect to output. M12 and M13 is the current output of CMFB circuit and connect to the drain of M8 and M9 respectively. The same gm cell I is used a summer in the proposed of the VGA design.

2.2.3 LPF simulations result

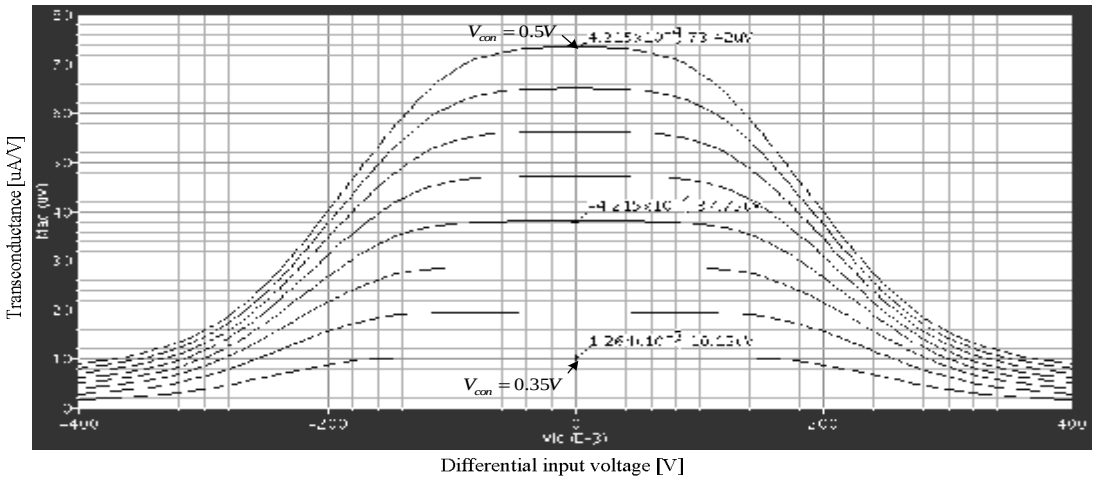


Figure 13 Simulation result of large-signal differential small transconductor

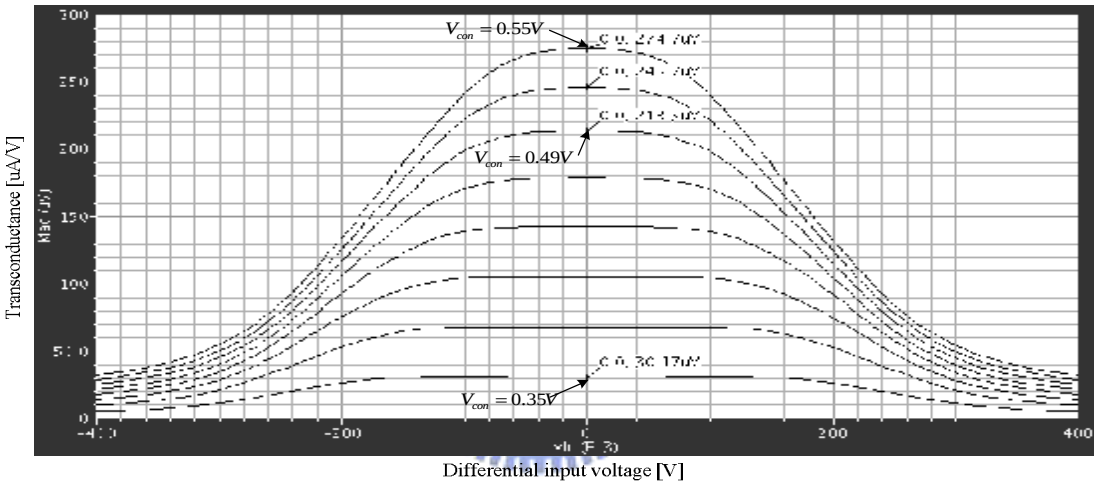


Figure 14 Simulation result of large-signal differential big transconductor

Fig. 13 and 14 show the simulation results of small and big gm for large-signal differential transconductor with 1.2V supply voltage. The range of transconductance covers l0u ~73u (A/V) and 30u~274u (A/V) respectively and match the specification

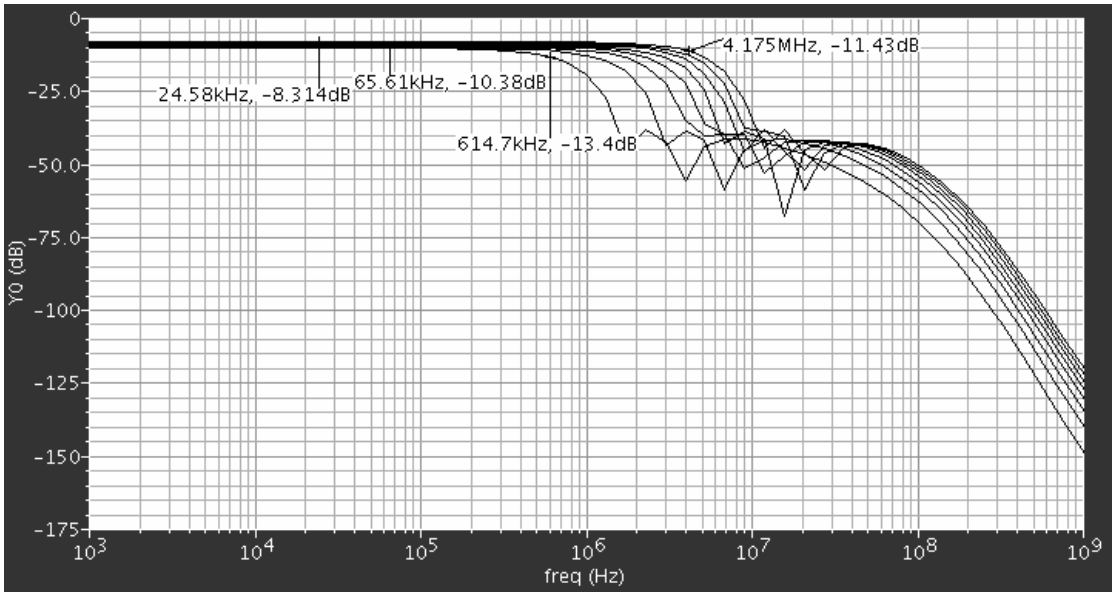


Figure 15 Frequency responses of LPF with small gm

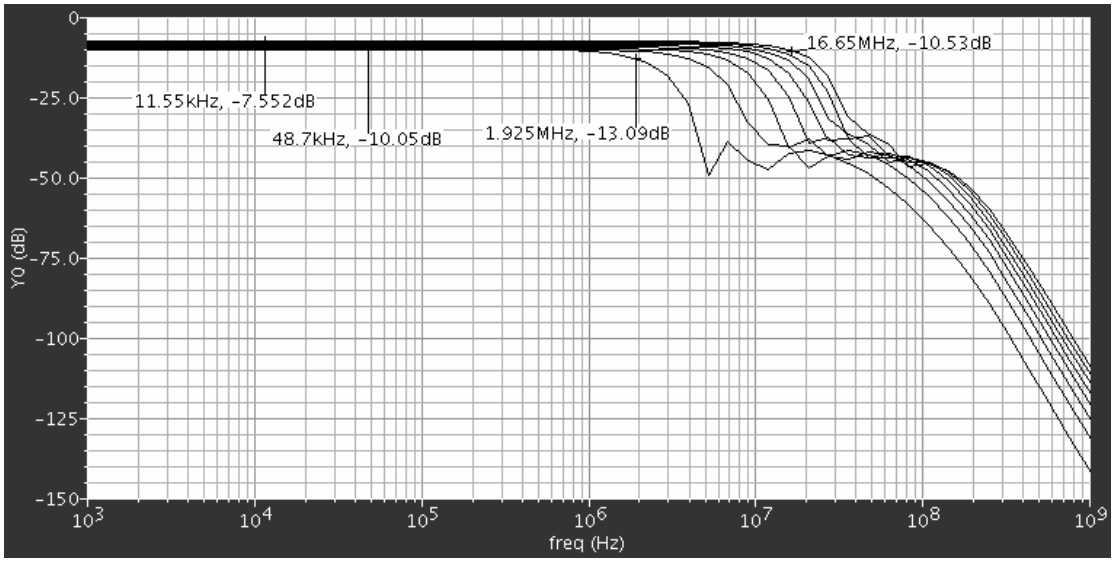


Figure 16 Frequency responses of LPF with big gm

Fig. 15 is the 5th-order LPF frequency response simulation result with small transconductor and the bandwidth is 0.6147~4.175 MHz. Fig. 16 is the 5th-order LPF frequency response simulation result with small transconductor and the bandwidth is 1.925~16.65 MHz. The tunable frequency range covers the specification. The DC gain is about -10dB.

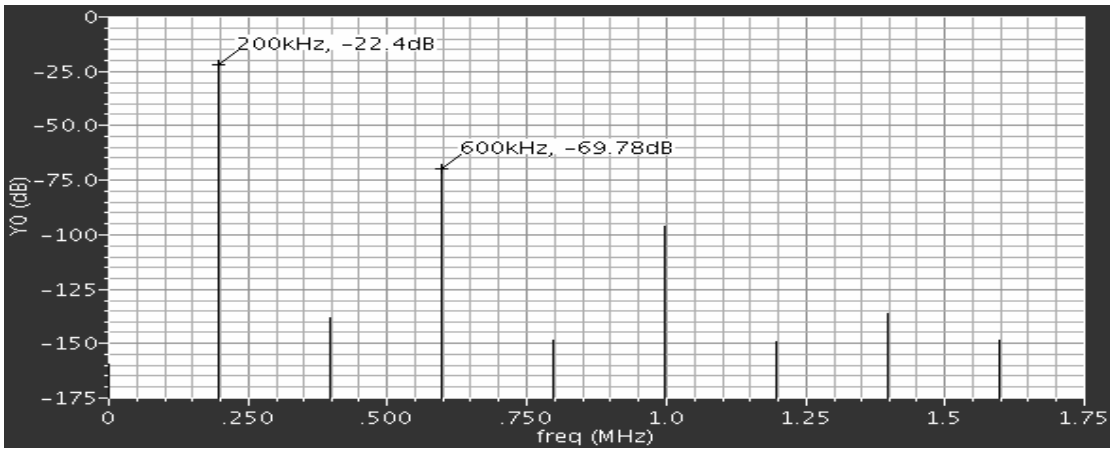


Figure 17 Harmonic simulation of LPF with small gm and 0.4Vpp 200 KHz input signal and Vcon=0.5V

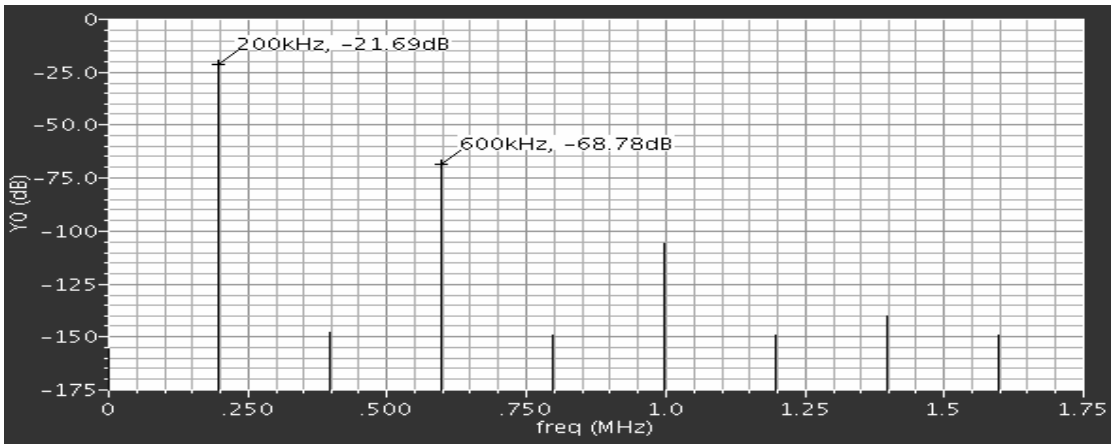


Figure 18 Harmonic simulation of LPF with big gm and 0.4Vpp 200 KHz input signal and Vcon=0.55V

A signal with 0.4Vpp 200 KHz is input to characterize the linearity. Fig. 17 is the LPF harmonic simulation result for V_{com}=0.5 with small transconductors and the dynamic range is 47.38 dB. Fig. 18 is the LPF harmonic simulation result for V_{com}=0.55 with big transconductors and the dynamic range is 47.09 dB. The total power is 1.072mW~14mW. The noise figure is 74.7 dB.

Parameters	Spec.	Simulation
Technology	CMOS 0.13um	CMOS 0.13um
Power supply	1.2V	1.2V
Power consumption	As small as possible	1.072mW~14mW
3-dB bandwidth	0.625M~14MHz	10.625M~14MHz
NF(dB)	As small as possible	74.4dB
Dynamic range(0.4Vpp)	50dB	>47.38dB

Table 6 The simulation results of WiMax LPF circuit

Table 6 shows the summary of the LPF simulation results.

2.3 High dynamic range VGA design

The section presents the proposed variable gain amplifier (VGA) circuit for high dynamic range applications. The gain range of VGA increases to 8.6~32dB to compensate the non-ideal -10dB DC gain of LPF. Section 2.3.1 discusses one example of pseudo-exponential topologies to approximate its gain polynomial to exponential and improve the gain range. In addition, rail to rail topology is used to increase the dynamic range. Section 2.3.2 discusses the variable gain amplifier architecture. Section 2.3.3 will discuss the simulation results.

2.3.1 High Dynamic Range Requirements for WiMAX

A pseudo-exponential gain control using MOS transistors had been developed as shown in Fig. 19 [4]. The amplifier make use of a source-couple pair with diode connected load. The output is the diode connected load (1/gm) since the gain will be equivalent to input and load transconductance ratio. The circuit consists of three part, gain cell (M1-M8), gain control (M11-M14), and common mode feedback. The gain cell possesses the pseudo exponential gain transfer curve with respect to the linear gain control signal that come from gain control circuit. Common feedback is used to stabilize the output common mode voltage.

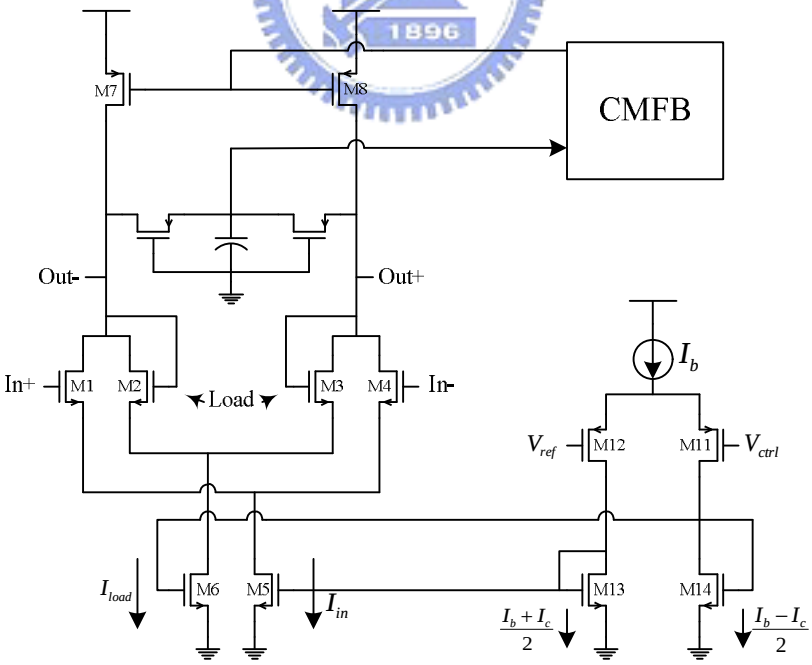
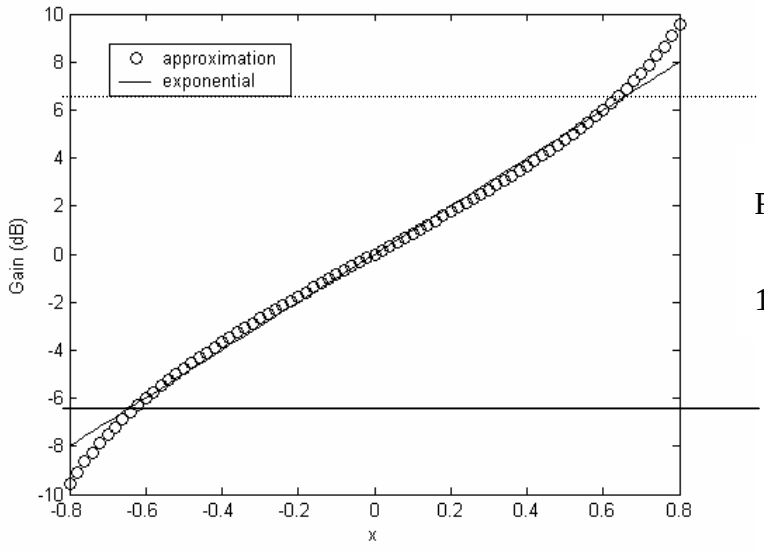


Figure 19 Schematic of the conventional variable gain amplifier [4]

In order to control amplifier gain, the transconductance of input and load

transistor varied with the change of control current. The current through input and load is constantly and equally to the current of PMOS (M7 and M8), so the output voltage will be constantly, too. The gain control block is another PMOS source couple pair (M11 and M12). The gain control current is a mirror to the tail current source (M5 and M6) of input source coupled pair and load respectively. The gain is proportional to the square root of the approximated polynomial as show in equation below (2-1).

$$
\begin{aligned}
gain &= \frac{gm_{in}}{gm_{load}} \\
&= \sqrt{\frac{mC_{ox}(W/L)_{in}gI_{in}}{mC_{ox}(W/L)_{load}gI_{load}}} \\
&= \sqrt{\frac{mC_{ox}(W/L)_{in}}{mC_{ox}(W/L)_{load}}}g\sqrt{\frac{I_b+I_c}{I_b-I_c}} \\
&= Kg\sqrt{\frac{1+x}{1-x}}
\end{aligned}
\qquad (2\text{-}1)
$$



Range:

15dB

Figure 20 Conventional circuit approximation

In equation (2-1), the transconductance of input and load transistor varies with the changes of current. The gain range is limited by the square-root nature of the device. The maximum gain range is showed in Fig. 20. In Fig. 20, the variable x is the ratio of the additional current I_c to DC bias current I_b when control signal is applied. Because the square the gain range is limited to about 15dB per stage.

The proposed approach[5] aims to improve the gain range by canceling the square-root of equation (2-1). The proposed method is change the control current with the varied voltage. The concept can be expressed as following:

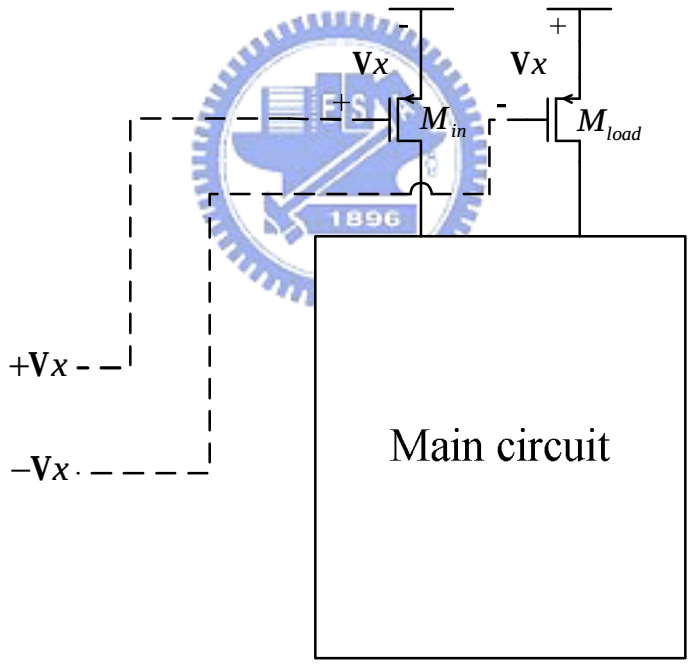


Figure 21 The concept of the proposed methodology

The pseudo exponential technique is based on equation (1+x) / (1-x). If we restrict the gate voltage of PMOS current source at the same time, we will increase (decrease) one PMOS over driver voltage and decrease (increase) other PMOS over driver

voltage simultaneously. From Fig. 21 supplying a $\mathbf{V}x$ and a opposite $\mathbf{V}x$ increases and decrease V_{in} and V_{load} respectively. The transconductance is proportioned to the over voltage of current source.

$$gain = \frac{gm_{in}}{gm_{load}} = \sqrt{\frac{(W/L)_{in}}{(W/L)_{load}}}\sqrt{\frac{I_i}{I_l}} \tag{2-2}$$

$$I_M = mC_{ox}\left(\frac{W}{L}\right)\left(V_{ctrl} - V_t\right)^2 \tag{2-3}$$

$$gain = k \times \left(\frac{1+x}{1-x}\right)$$

$$\text{gain range} = \left(\frac{1+x}{1-x}\right)^2 \tag{2-4}$$

If the over-drive voltage replaces the control variable X in (2-4) then the gain range will not be limited by square root.

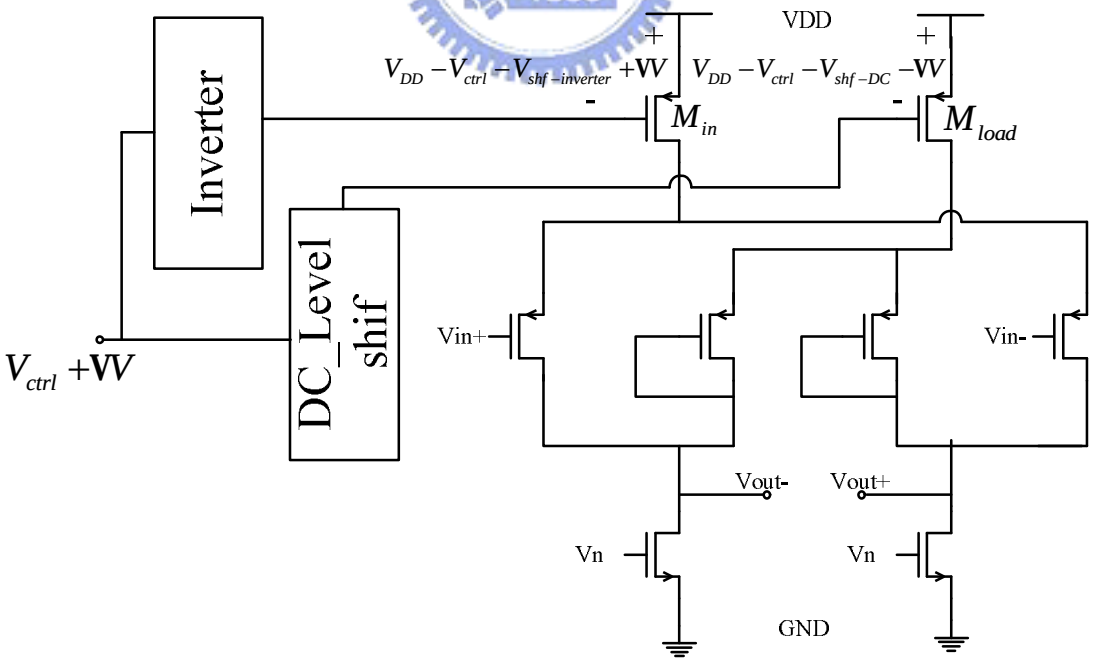


Figure 22 Propose technique

The amplifier for enhancing maximum gain range is shown in Fig. 22. The gain stage

is like reference circuit which has the same source couple gain cell but is different from control circuit instead. An inverter is used to reverse Δx. And a DC-level shift circuit is empilied to make it to shift the circuit DC level. The ratio of input to load transconductances is expressed as following:

$$gain = \frac{gm_{in}}{gm_{load}} = \sqrt{\frac{mC_{ox}(W/L)_{in}}{mC_{ox}(W/L)_{load}}}\sqrt{\frac{I_i}{I_l}}$$

$$= \sqrt{\frac{mC_{ox}(W/L)_{in}}{mC_{ox}(W/L)_{load}}}\sqrt{\frac{mC_{ox}(W/L)_{i}}{mC_{ox}(W/L)_{l}}} \times \left(\frac{V_{DD} - V_{shf-inverter} - |V_{tp}| + \Delta V}{V_{DD} - V_{shf-DC} - |V_{tp}| - \Delta V} \right) \quad (2\text{-}5)$$

With the condition,

$$V_{shf-inverter} = V_{shf-DC} \quad (2\text{-}6)$$

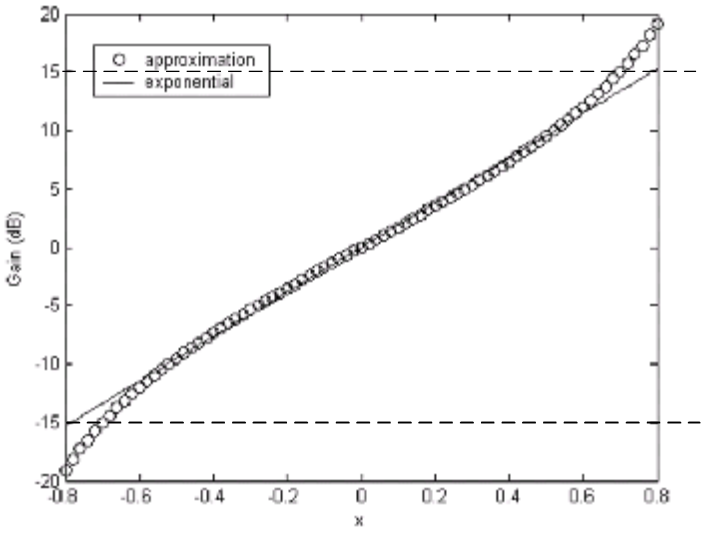
equation (2-5) is further simplified.

$$gain = K \times \left(\frac{1+x}{1-x} \right)$$

where $K = \sqrt{\frac{mC_{ox}(W/L)_{in}}{mC_{ox}(W/L)_{load}}}\sqrt{\frac{mC_{ox}(W/L)_{i}}{mC_{ox}(W/L)_{l}}}$

$$x = \frac{\Delta V}{V_{DD} - V_{shf-inverter} - |V_{tp}|} = \frac{\Delta V}{V_{DD} - V_{shf-DC} - |V_{tp}|} \quad (2\text{-}7)$$

From the above description, the pseudo exponential equation (1+x) / (1-x) is satisfied under the proposed method. The simulation result is shown in Fig. 23 and the gain range is about 30dB. Next we will use rail-to-rail topology to increase dynamic range.



Range:

30dB

Figure 23 proposed simulation

With 0.13 CMOS FDK, the output swing of the proposed circuit can be expressed as.

$$V_{swing} = V_{DD} - V_t - 3VV \tag{2-8}$$

Where V_t is the overdrive voltage for a MOS operated in saturation region. Assume $V_t \approx 0.35$, $VV \approx 0.2$ and VDD=1.2V, the V_{swing} is 0.25 Vpp. The output swing is too small to match the specification that has dynamic range 50dB for 0.4 Vpp. Rail-to-rail technique is applied to improve the output swing and the linear range. The proposed circuit design consists of a PMOS mode VGA, a NMOS mode VGA and a low gain OP to sum up the two path signal from rail to rail. From Fig. 24(a), when the signal voltage is approach to ground the P devices act, while the signal voltage is close to VDD the N devices act. The complete architecture is shown in Fig. 24(b). The low gain OP is the gm cell and described in the section 2.2.2, and the low gain amplifier

can increase the gain to meet specification. When the control voltage change, the DC operation point will change and the output swing voltage can't approach ideal rail-to-rail swing ($V_{VDD-gnd}$), the dynamic range is still improved at least 6dB.

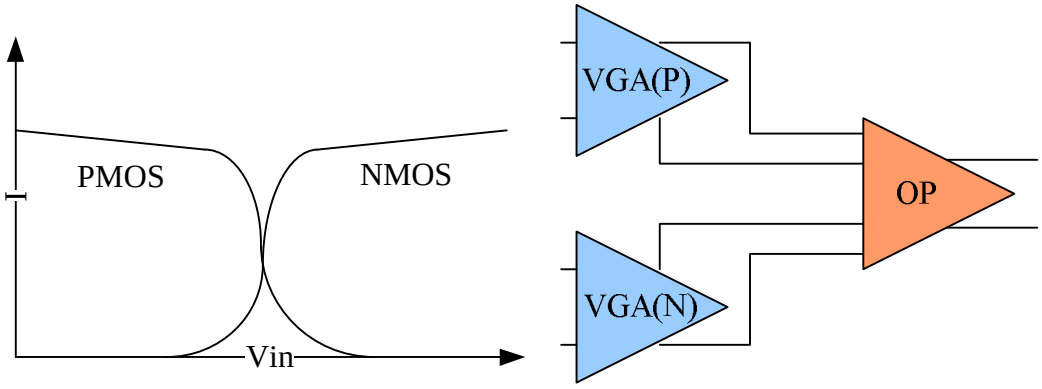


Figure 24 (a) Idea description of how to fit PMOS pair and NMOS pair into low voltage headroom (b) The total VGA circuit for rail-to-rail topology

2.3.2 High Dynamic Range VGA

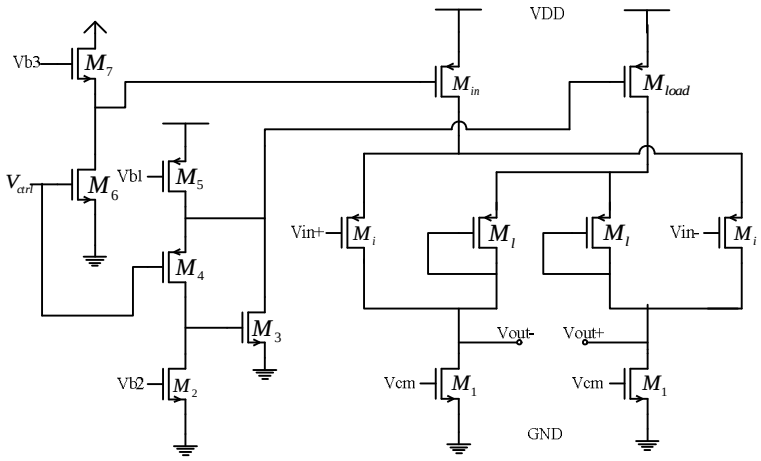


Figure 25 Schematic of the VGA

Fig. 25 shows the complete schematic of the P device VGA with an inverter and

a DC-level shift. Transistors M_i and M_l form the gain cell. Transistors M_{in} and M_{load} are used to control input and load transconductance together with the control voltage as mention earlier. Transistor M_1 is the current source and is adjusted by common-mode feedback (CMFB) to stabilize the output DC points. Transistors $M_2 \sim M_5$ are for the DC-level shift. Transistors M_6 and M_7 are the inverter to invert the control voltage.

There is an important parameter to be taken attention. In Equation (2-7), when the parameter K is 1, the ideal gain range is from -15dB to 15dB. Parameter K is the ratio of input transconductance to load transconductance. Because the gain range of specification is from 8.6dB to 32dB, the value of K can be adjust the shift gain range. In this design the value of K is 2 and the gain of the low gain OP is increased too. In order to reduce power consumption, transistors M_1, M_i and M_l is design to make the cut-off frequency of LPF to match the maximum cut-off frequency requirement.

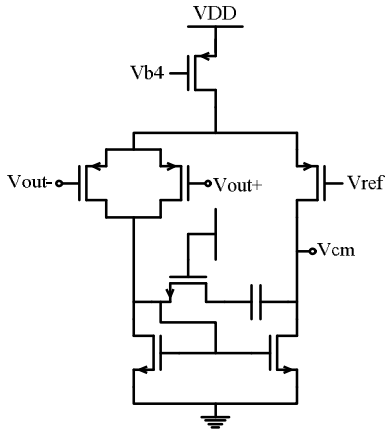


Figure 26 Common mode feedback circuit

Fig. 26 is the common mode feedback circuit to stabilize output. The common feedback output V_{cm} connects to M_1 gate to apply a DC negative feedback. The feedback loop will adjust the current source. The Output DC level is important in multi-stage design. If the output DC level of the first stage is not stable, the following stages will not operate at the best state and will decrease the total gain range.

2.3.3 VGA Simulations result

Fig. 27 shows the simulation result of the VGA gain range. Fig. 28 shows the dynamic range at each control voltage.

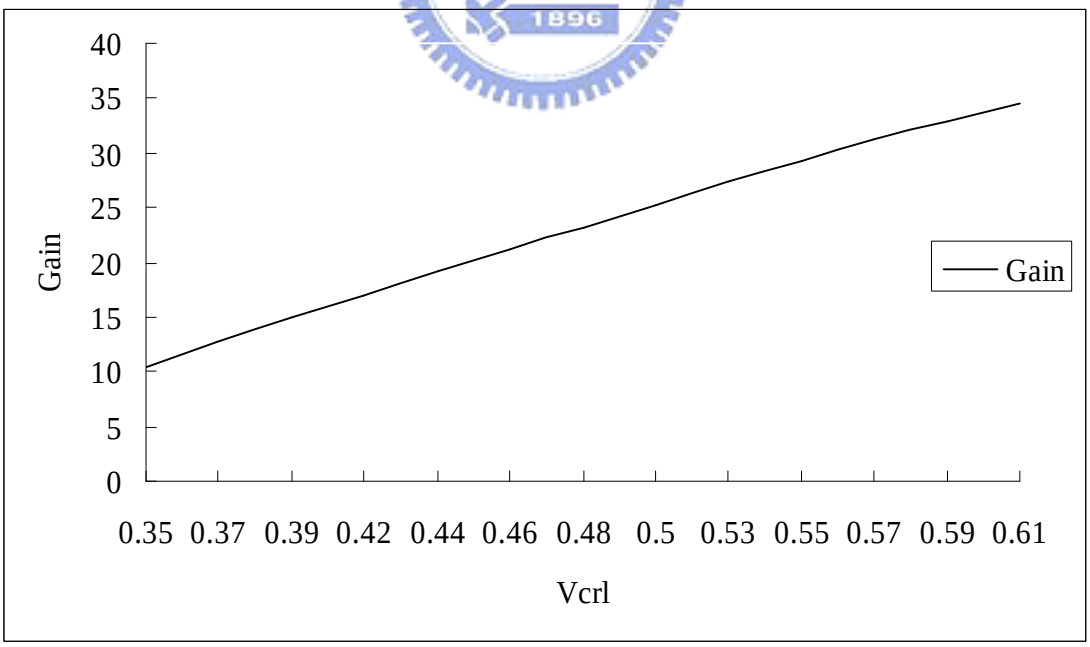


Figure 27 Dynamic gain range simulation result

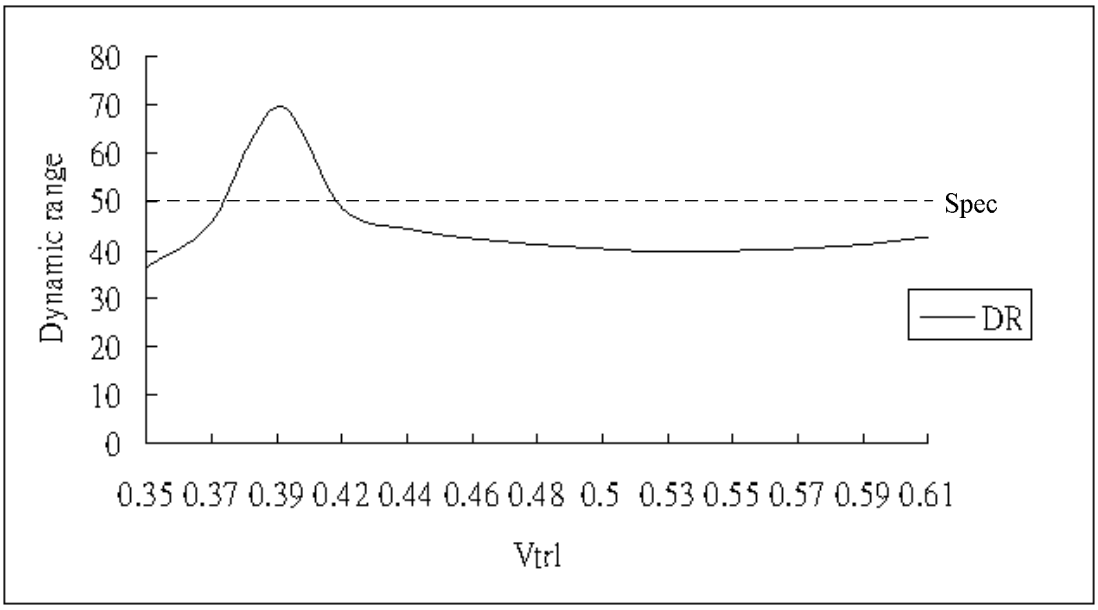


Figure 28 Dynamic range simulation result for different Vcrl

Vcr(V)	0.35	0.372	0.394	0.416	0.438	0.46	0.482	0.504	0.526	0.548	0.57	0.592	0.614
Gain(dB)	10.34	12.71	14.92	17.04	19.11	21.17	23.21	25.26	27.31	29.3	31.2	32.95	34.48
DR(dB)	36.44	45.39	69.75	48.41	44.37	42.36	41.09	40.29	39.86	39.81	40.24	41.17	42.56

Table 7 The gain and dynamic range simulation result in different control voltage for a VGA

The gain is not the same for each VGA requirement, it can be better linearity. The VGA gain range simulation result is about 10.3dB~34.4dB.

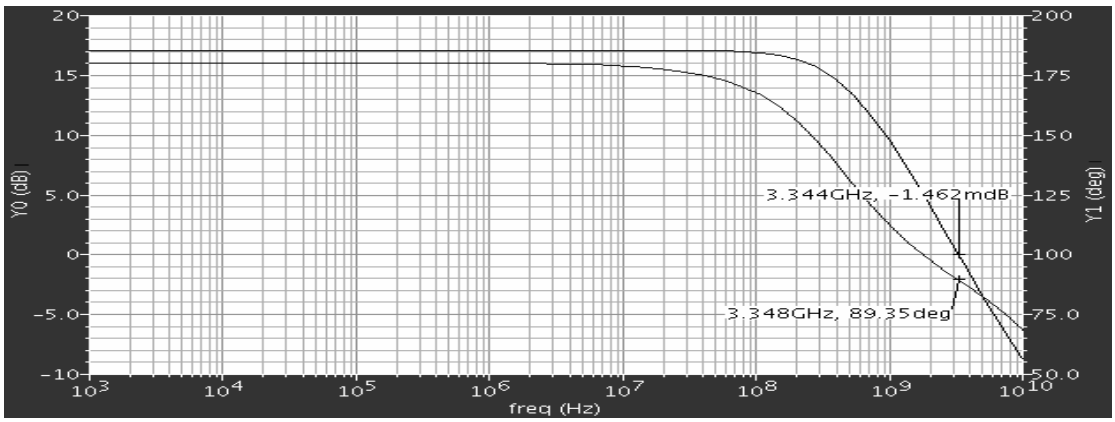


Figure 29 Phase margin simulation for PMOS VGA

Fig. 29 is PMOS VGA AC simulation result whose phase margin is 89.35deg and is worse than NMOS VGA. Fig. 30 is gm cell AC simulation result whose phase margin is 96.57 deg. The total VGA bandwidth is limited by low gain amplifier and the -3dB frequency is 14.79 MHz.

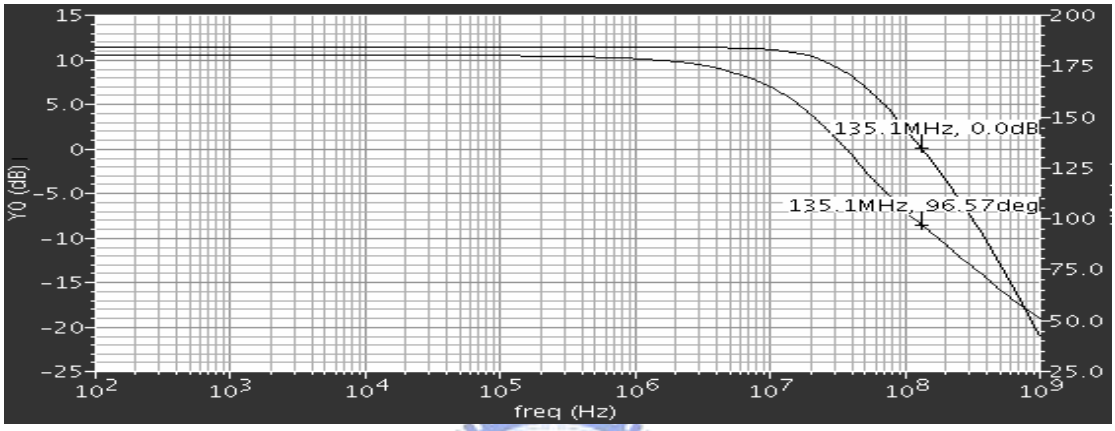


Figure 30 Phase margin simulation for gm cell.

Parameters	Spec.	Simulation
Technology	CMOS 0.13um	CMOS 0.13um
Power supply	1.2V	1.2V
Power consumption	As small as possible	2.184mW~4.287mW
Gain range	8.6 ~32dB	10.3dB~34.4dB
NF(dB)	As small as possible	28.8dB
Dynamic range(0.4Vpp)	50dB	>39.81dB

Table 8 The simulation results of WiMax VGA circuit

Table 8 shows the summary of the a VGA simulation results. The noise figure is 28.8dB.

2.4 Topology performance analysis

Now we can analysis the topologies by VGA and LPF from section 2.2, 2.3. Table 9 shows the two circuit simulation results.

Block	LPF	VGA
Bandwidth	0.615M~16.65MHz	14.79MHz
Gain range	-10dB	10.3dB~34.4dB
NF(dB)	74.4dB	28.8dB
Dynamic range(0.4Vpp)	>47.38dB	>39.81dB

Table 9the simulation result of LPF and VGA

We mainly analyze the noise figure and interference are analyzed to decide which topology can fit the WiMax specification and which have better performance. From topology(1), LPF arranges in the first stage and A 5-order elliptic LPF can reject 30dB gain at least. Since the maximum 1^{st} adjacent channel interference C/I is -21, so the LPF can reject the interference and no VGA stage will be saturated. But the noise figure will be the worst. After simulation the noise figure of topology(1) is 74.4dB.

From topology(2), the maximum 1^{st} adjacent channel interference is -1dBm and

the maximum swing is -4dBm. The interference will be amplified 10.3dB to 9.3dBm and it exceeds -4dBm (0.4Vpp) after a VGA, and the next stage, LPF, will be saturated. At BER 10^{-3} the maximum interference is -13dBm which considers -3dB attenuation in RF front end. The interference will be amplified 10dB to -3dBm. Topology(2) is constrained to be fit the interference specification at BER 10^{-3}. After simulation the noise figure of topology(2) is 51.87dB.

Only topology(1) can fit the interference requirement at BER 10^{-6} and Topology(2) is constrained to fit the interference specification at BER 10^{-3} needless to say topology(3) and topology(4).

2.5 Design Optimization for Noise Figure and Distortion Tradeoffs

Topology(1) can reject interference to avoid circuit into saturation but it has bad NF. Topology(2) has better NF but next stage, LPF, may be drove into saturation. The gain of the first stage influences the NF and interference.

Generally a specification will specify the maximum interference that the system can tolerate. When LPF rejectsthe interference that almost saturate LPF, the design is optimization, and can filter out the maximum interference and has best noise figure.

Figure 31 is an analog baseband circuit that has a tunable dB-linearity gain topology and LPF can insert in any location. The circuit can provide A~B dB gain. Each VGA and LPF has the same maximum input and output swing Vm (V_{p-p}) m dBv. The maximum input signal power is define Vp (p dBv)

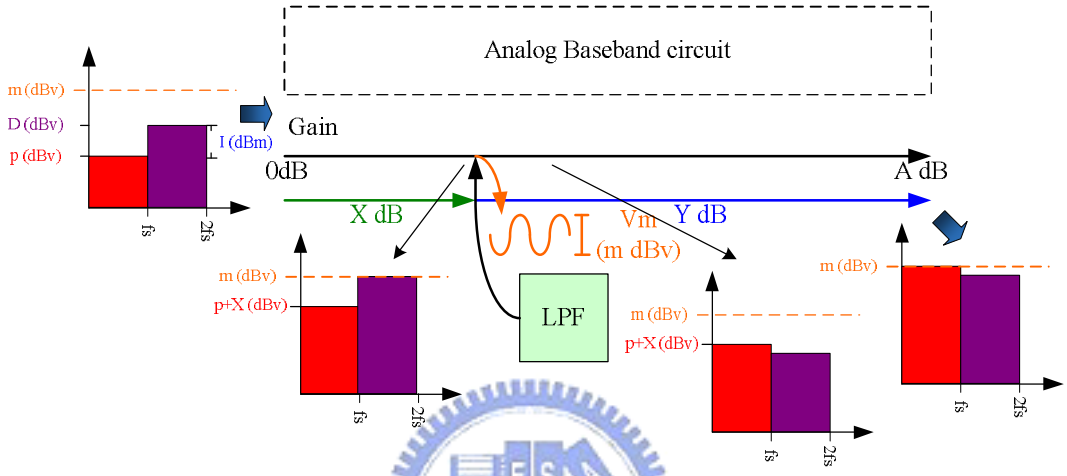


Figure 31 The optimization for noise figure and interference in one LPF and VGAs analog baseband design

Now consider the system receives maximum interference that the system can tolerate. In this time, the signal is maximum and interference is maximum in this worst case. So the gain of circuit will be set to minimal mode A dB. Suppose LPF inserting in location X can filter the interference and that is the optimization. The interference just makes the next VGA into saturation. In this situation, the interference is amplified X dB and has m dBv swing. The adjacent channel interference C/I that the design can tolerate is m – X - p (dBv). The noise figure is

$$NF_{tot-optimum} = 1 + (NF_{VGA_X} - 1) + \frac{NF_{LPF} - 1}{A_{VGA_X}} + \frac{NF_{VGA_Y} - 1}{A_{VGA_X} * A_{LPF}} \quad (2.9)$$

$$NF_{tot-worst} = 1 + (NF_{LPF} - 1) + \frac{NF_{VGA_X} - 1}{A_{LPF}} + \frac{NF_{VGA_Y} - 1}{A_{VGA_X} * A_{LPF}} \quad (2.10)$$

The noise figure we can improve is Equation (2.11) that Equation(2.10) subtracts Equation(2.9).

$$NF = (NF_{LPF} - NF_{VGA_X}) + \left(\frac{NF_{VGA_X} - 1}{A_{LPF}} - \frac{NF_{LPF} - 1}{A_{VGA_X}} \right) \quad (2.11)$$

So we can find the optimum location for LPF with Table 3. We definite the maximum deference of signal and interference is I. Consider the gain of LNA is 8dB and the attenuation in channel is 3dB.

$$I = m - X - p$$

$$X = m - p - I = -4 - (-25) - 21 = 0(dB)$$

If the lowest gain of first VGA is 0dB, the analog baseband circuit can avoid nest stage into saturated and have the best noise figure at BER 10^{-6} for WiMax specification.

Chapter 3

Simulations and Implementation of Analog baseband

In the chapter we show the simulation result of topology(1) and topology(2). In the latest tape-out the design uses topology(2) to arrange the VGAs and LPF even though Case(s) can't satisfy the worst interference specification but it almost can fit the specification at BER 10^{-3}. The difference between topology(1) and topology(2) is only the position of LPF, so the frequency response and harmonic simulation result will be almost the same. Section 3.1 presents the simulation result of our analog baseband circuit. Sec 3.2 presents the implementation and the measurement result of LPF.

3.1 Simulations for Analog baseband circuit

The last tape-out topology(2) is chosen, but we show the simulation result of two topologies. The VGAs and LPF design have been described in chapter 2.2 and chapter 2.3. The overall analog baseband design simulation will be shown in the

section.

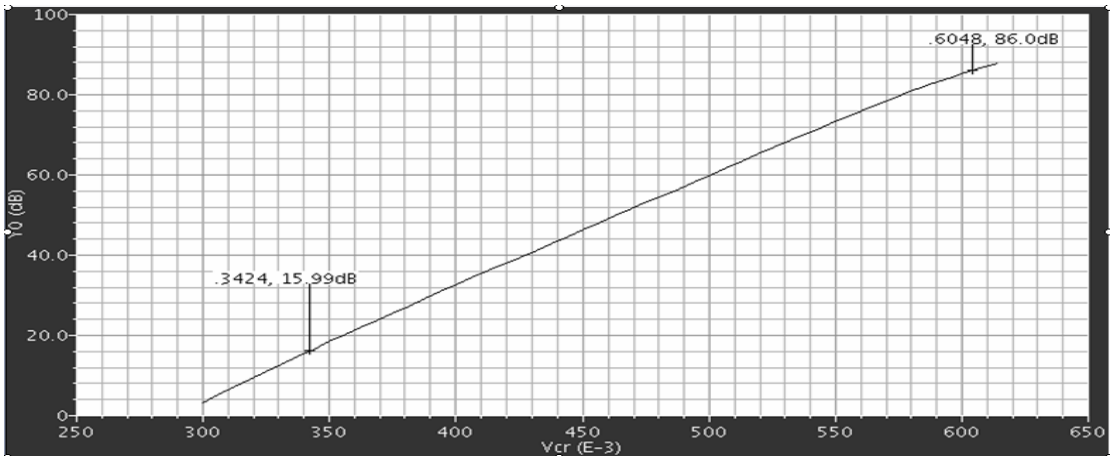


Figure 32 Dynamic gain range simulation result in topology(1)

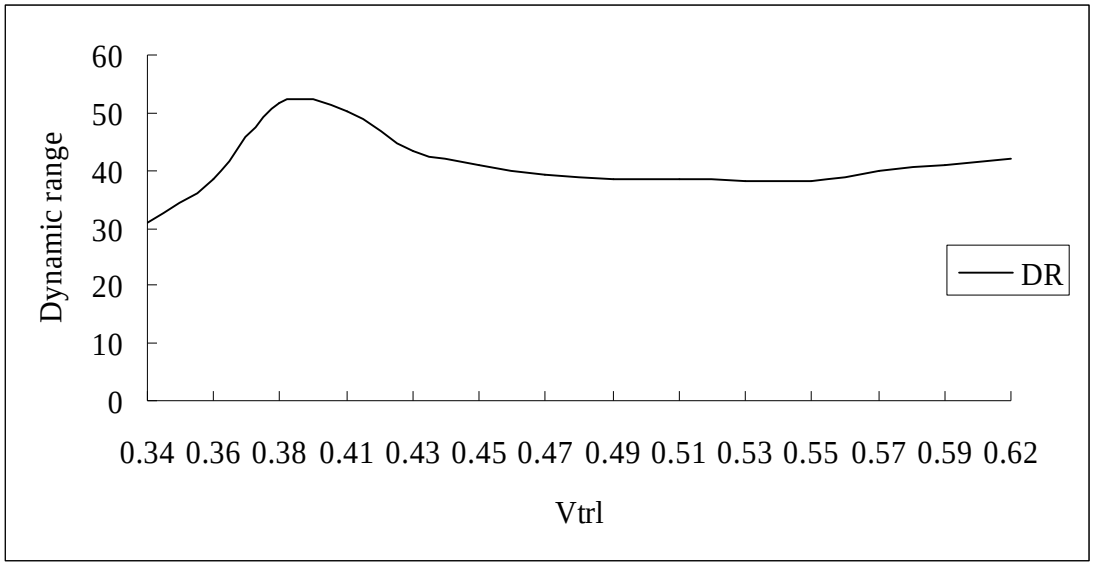


Figure 33 Dynamic gain range simulation result by harmonic simulation in topology(1)

Vcr(V)	0.34	0.36	0.38	0.41	0.42.5	0.45	0.47	0.49	0.51	0.53	0.55	0.57	0.59	0.62
Gain(dB)	15.24	21.88	27.3	33.8	39.66	45.45	51.21	56.97	62.73	68.43	74.19	79.25	84.01	88.35
DR(dB)	30.98	38.66	51.82	50.15	50.15	43.42	39.34	38.38	38.5	38.32	38.17	39.73	40.89	42.07

Table 10 The gain and dynamic range simulation result in different control

Fig. 32 shows the gain range after we run frequency response in topology(1). Fig.

33 shows the dynamic range simulation result in different control voltage and the output swing is 0.4Vpp. The dynamic range of analog baseband circuit is less than VGA about 2dB.

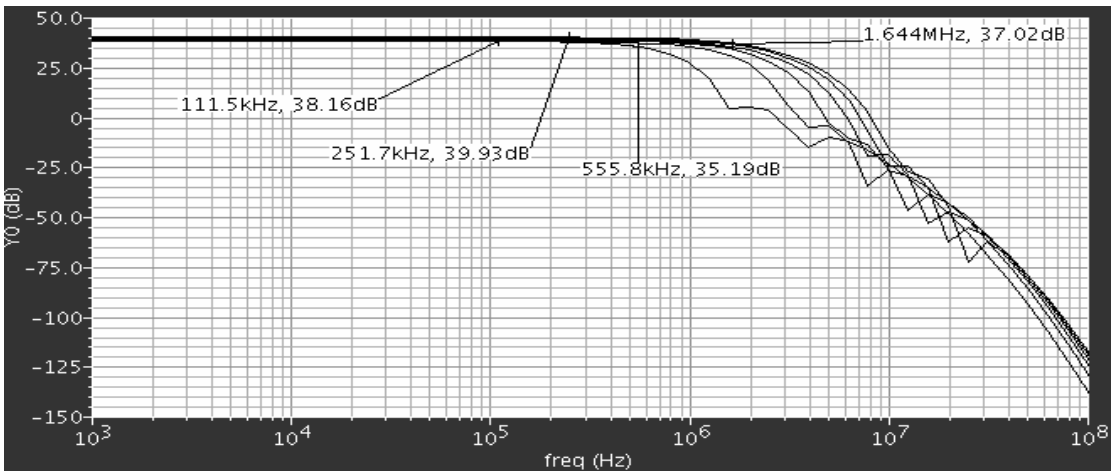


Figure 34 Frequency responses of analog baseband with small gm in topology(2)

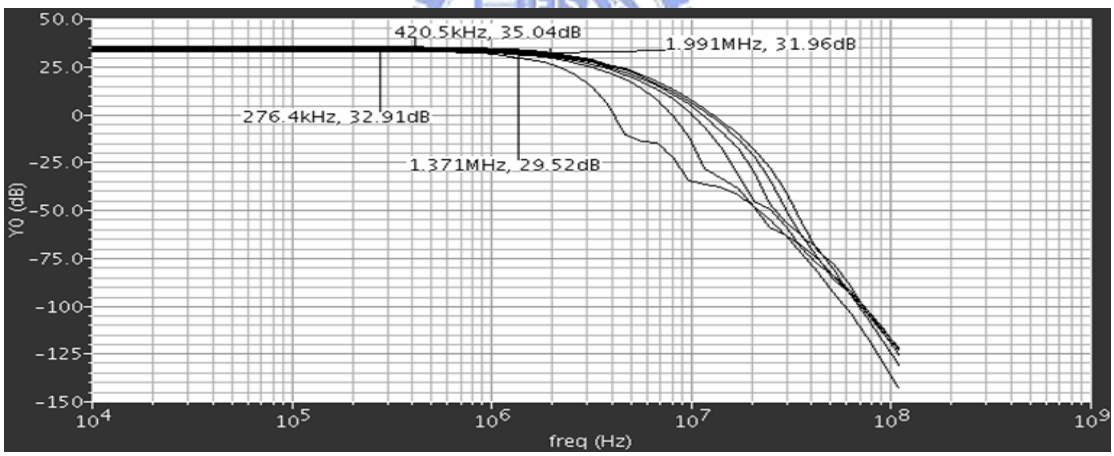


Figure 35 Frequency responses of analog baseband with large gm in topology(2)

Fig. 34 and 35 show the frequency response simulation result with small and big respectively. From Fig. 35 we can see the -3dB gain frequency have degraded to about 2MHz. This is because there is a parasitic pole between LPF and VGA. The pole equation is

$$Pole_{parasitic} = \frac{1}{R_{LPF} \cdot C_{LPF+VGA}}$$

R_{LPF} is the output resistor and $C_{LPF+VGA}$ is the sum of parasitic capacitor of LPF and VGA. So the gain degraded before frequency bandwidth expected.

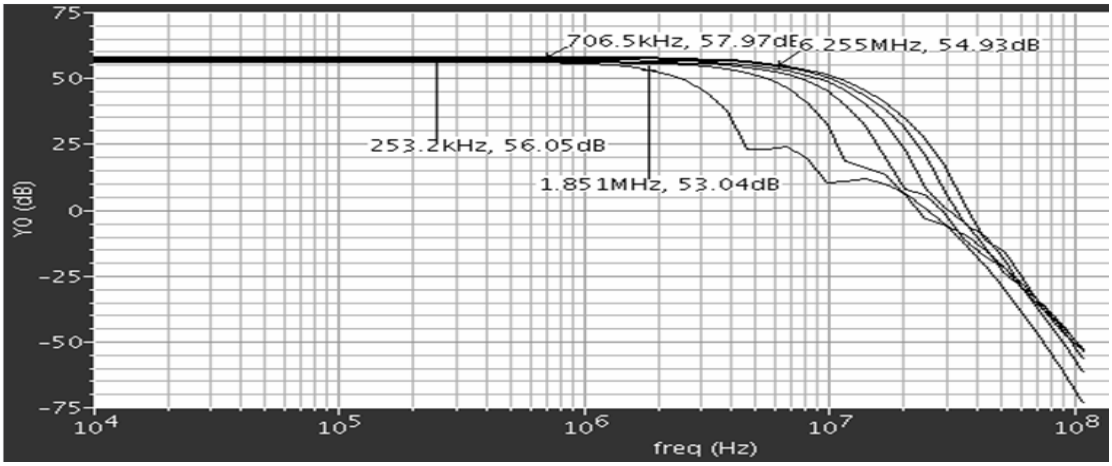


Figure 36 Frequency response simulation result after adding buffers in topology(1)

A buffers is added between LPF and VGA and simulation again. Fig. 36 shows the simulation result and the maximum -3dB frequency is 5.3MHz. The -3dB frequency can't increase to 14MHz is because the VGA -3dB frequency is 14.79MHz. The gain of VGA drops before 14MHz. After accumulating two VGA blocks the analog baseaband circuit -3dB frequency will decrease to 5.3MHz.

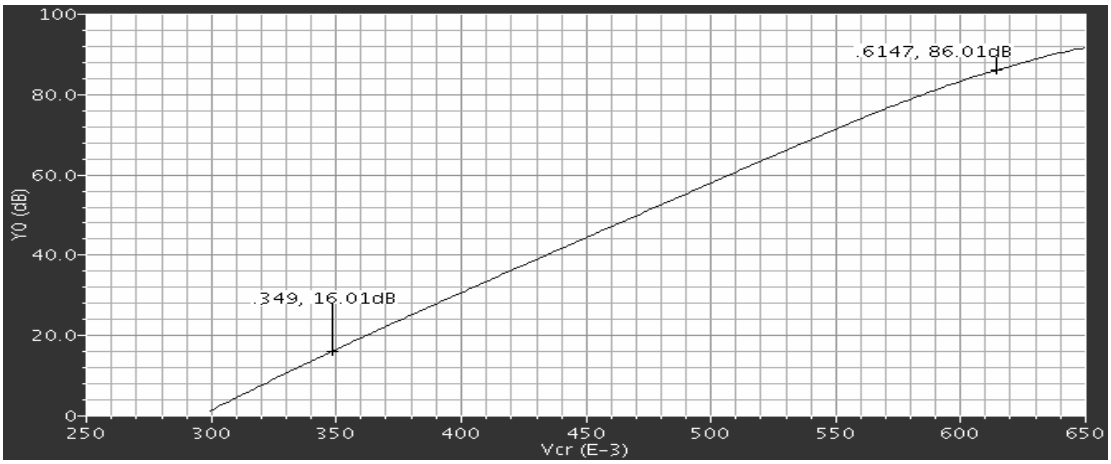


Figure 37 Dynamic gain range simulation result in topology(2)

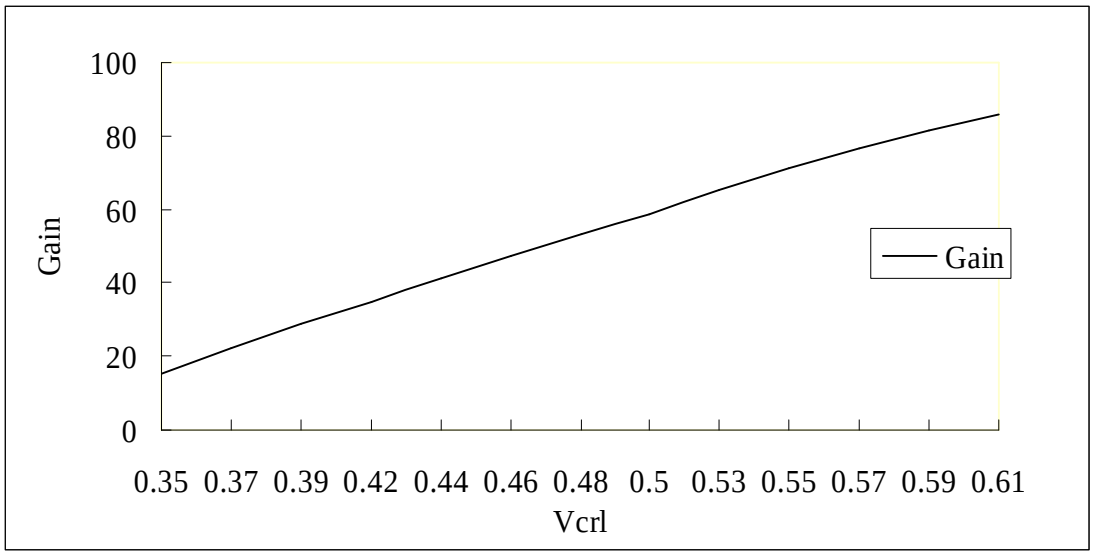


Figure 38 Dynamic gain range simulation result by harmonic simulation in topology(2)

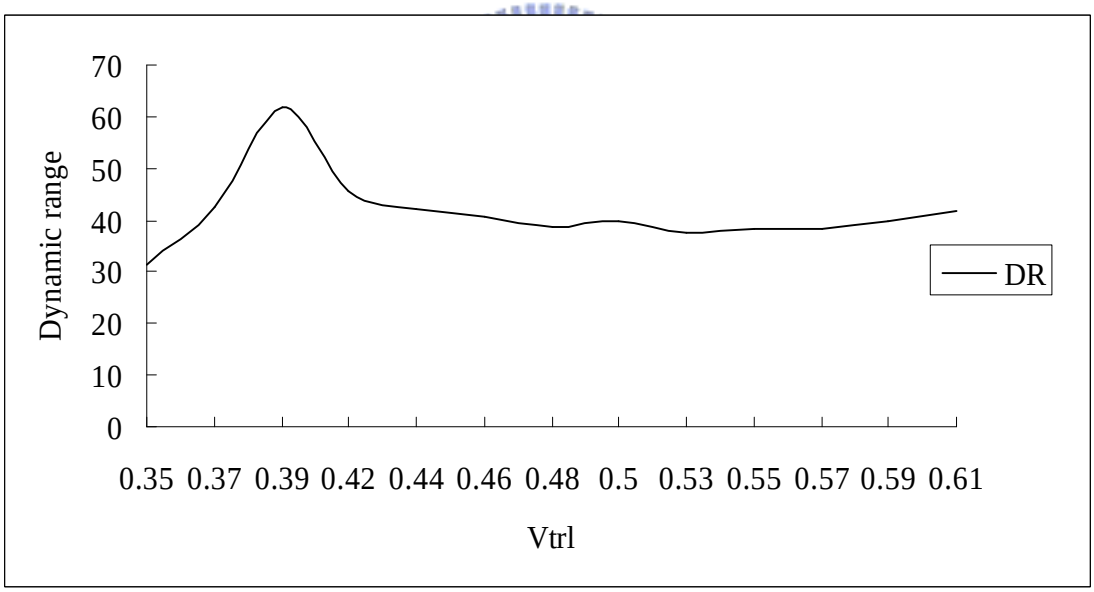


Figure 39 Dynamic range simulation result in different control voltage in topology(2)

Vcr(V)	0.35	0.372	0.394	0.416	0.438	0.46	0.482	0.504	0.526	0.548	0.57	0.592	0.614
Gain(dB)	15.44	22.4	28.78	34.9	41.06	47.09	53.14	58.58	65.18	71.03	76.62	81.69	86.69
DR(dB)	31.43	42.61	61.71	45.52	42.03	40.52	38.76	39.72	37.62	38.19	38.36	39.92	41.74

Table 11 The gain and dynamic range simulation result in different control voltage in topology(2)

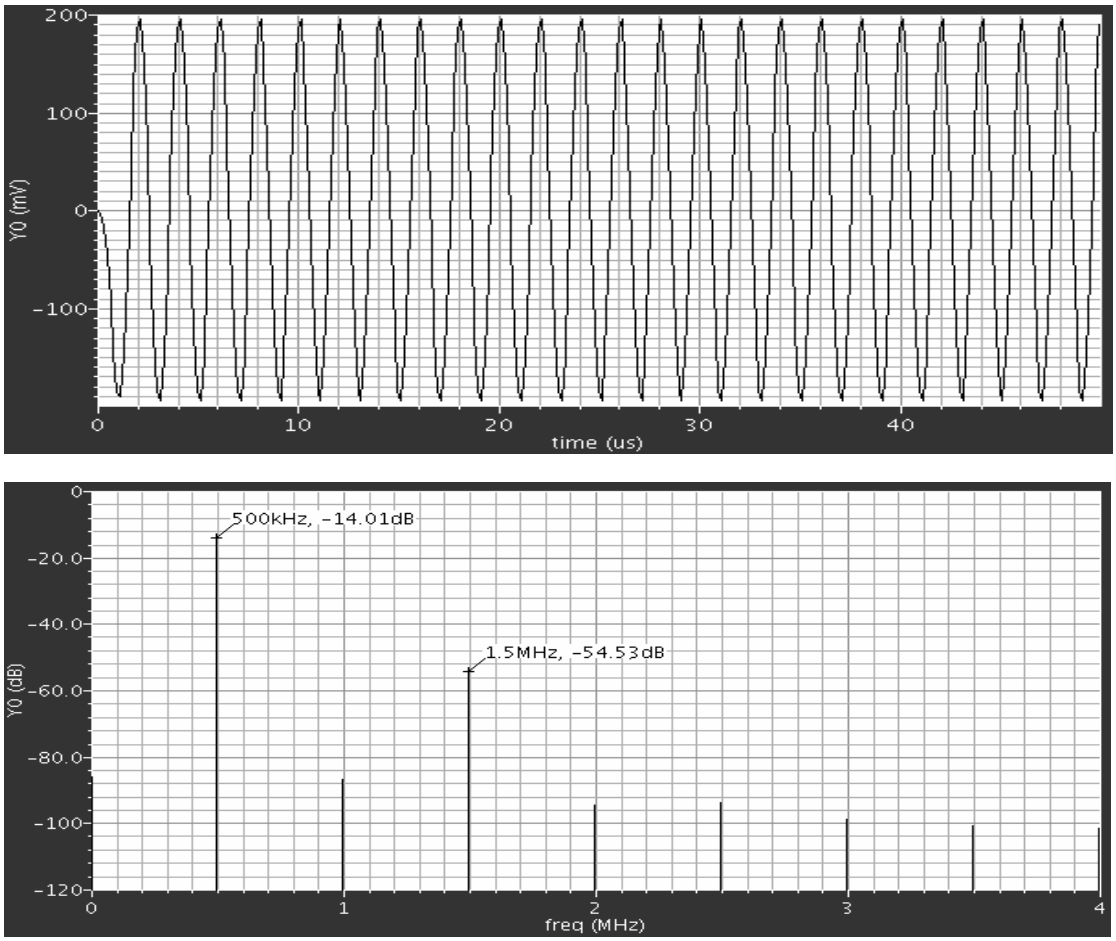


Figure 40 Output swing simulation with Vcr=460mV

Fig. 37 shows the gain range ac frequency response and Fig. 38 shows the gain range for harmonic simulation with output swing 0.4Vpp in topology(2). Fig. 39 shows the dynamic range simulation result in different control voltage and the output swing is 0.4Vpp too. The transient simulation is shown in Fig. 40. Under the V_{trl} =460mV the output swing is 0.4Vpp for differential output with 40dB dynamic range.

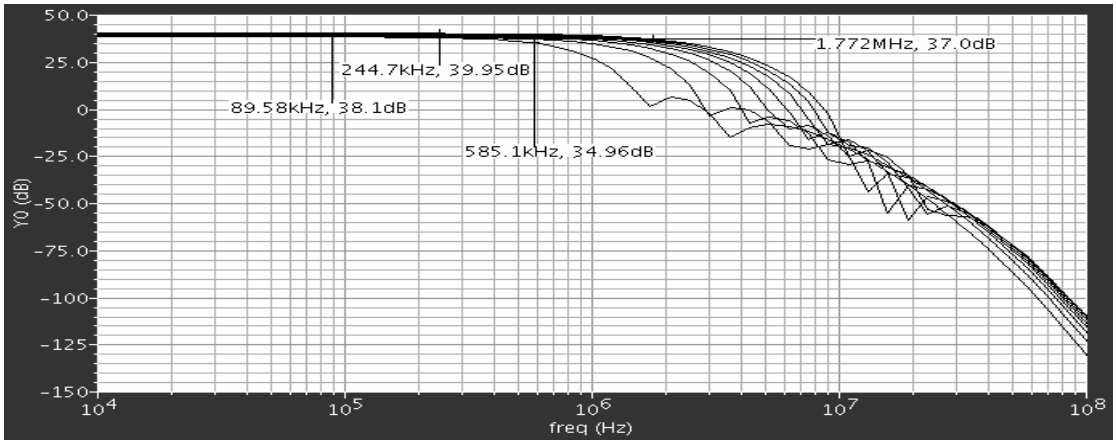


Figure 41 Frequency responses of analog baseband with small gm in topology(2)

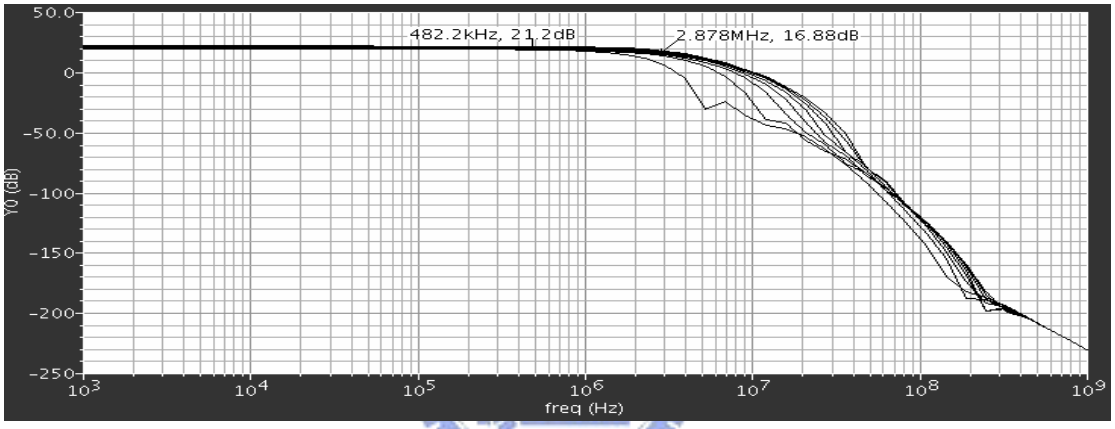


Figure 42 Frequency responses of analog baseband with large gm in topology(2)

Fig. 41 and 42 show the frequency response simulation result with small and large gm cell in LPF respectively. From Fig. 41 the -3dB gain frequency has degraded about 2.7MHz. Topology(2) has the same problem of topology(1). Fig. 43 shows the simulation result and the maximum -3dB frequency is 5.3MHz after adding buffers

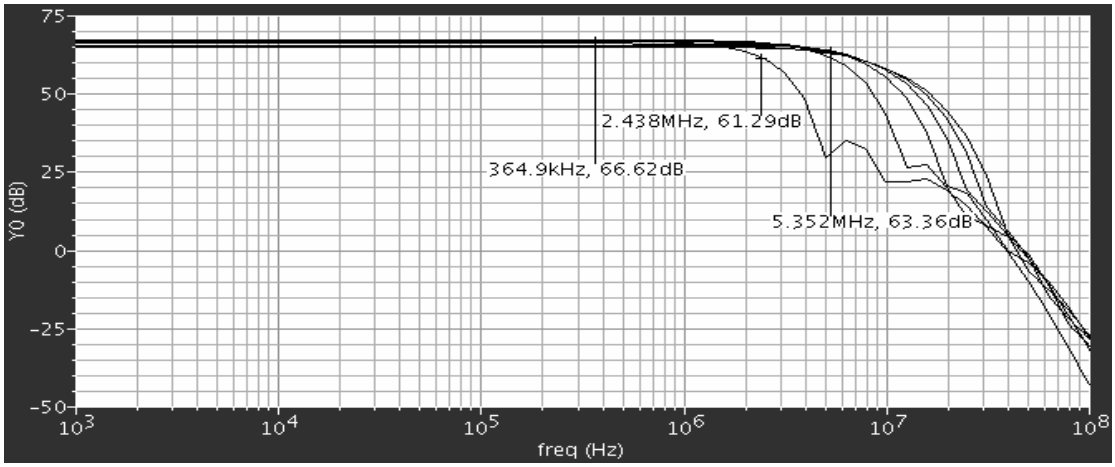


Figure 43 Frequency response simulation result after adding buffers in topology(2)

Parameters	Spec.	Topology(1)	Topology(2)
Technology	CMOS 0.13um	CMOS 0.13um	CMOS 0.13um
Power supply	1.2V	1.2V	1.2V
3-dB bandwidth	0.625M~14MHz	0.625B~5.3MHz	0.625B~5.3MHz
Power consumption	As small as possible	7.624mW~26.8mW	7.624mW~26.8mW
NF	As small as possible	84.9dB	51.87dB
Gain range	16dB-86dB	16~86dB	16~86dB
Dynamic range(0.4Vpp)	50dB	>38.17dB (0.4Vpp)	>38.19dB (0.4Vpp)

Table 12 The simulation results of WiMax analog baseband circuit

3.2 Implementation & Measurement

Fig. 44 shows the layout of VGA block and the size is 120um x 79um. There are a PMOS-type VGA, a NMOS-type VGA and a low gain amplifier.

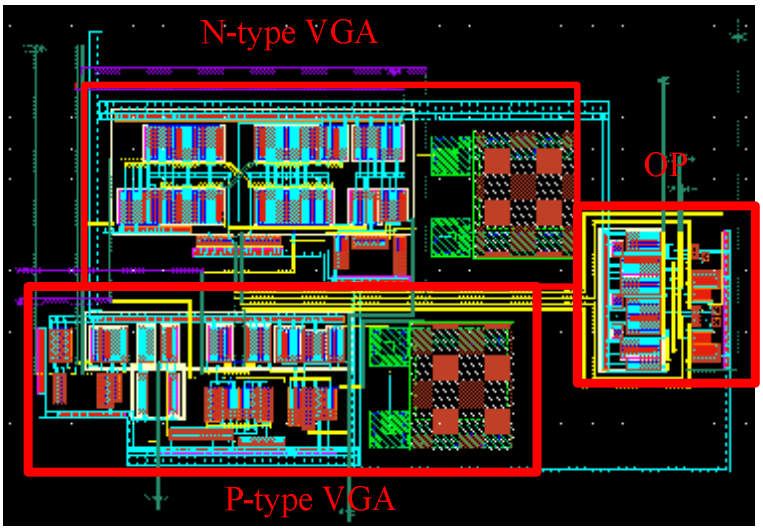
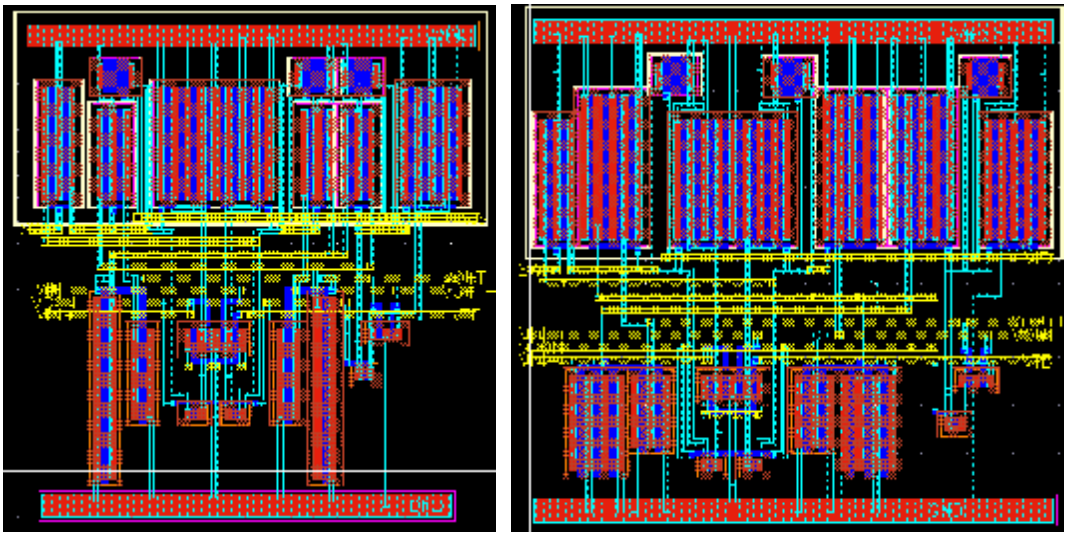


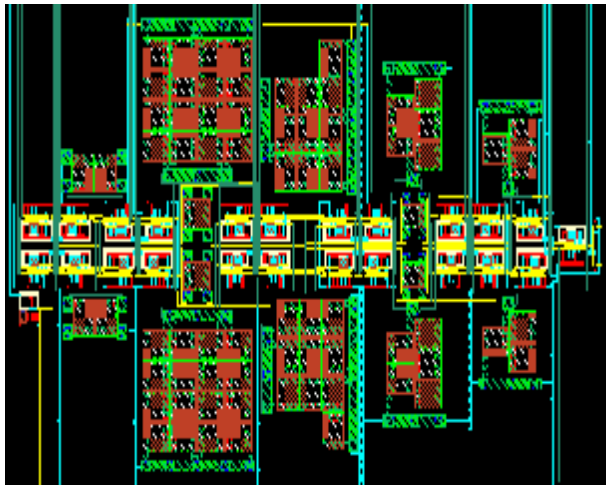
Figure 44　VGA block

The layouts of two Gm block is shown in Fig. 45(a) and Fig. 45(b). Small Gm and large Gm are only different from MOS size and the layout is close small to reduce parasitic capacitance. The size of small Gm is 21um x 22um. The size of large Gm is 24um x 22um.



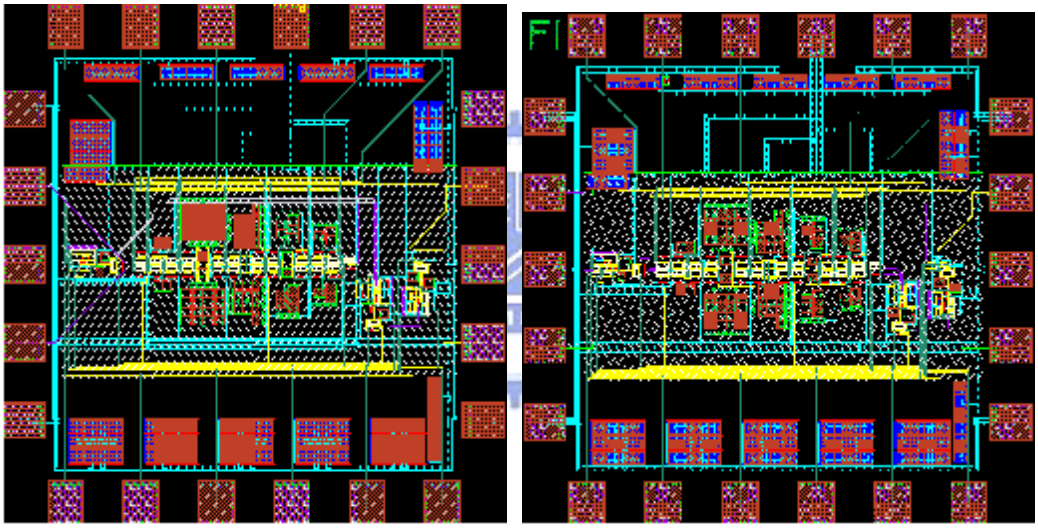
(a) Small Gm block　　(2) Big Gm block3

Figure 45　Two kind of Gm block



(a) LPF block

Figure 46 LPF circuit layout



(a) Layout of Topology(1) (a) Layout of Topology(2)

Figure 47 Analog baseband circuit layout

The layout of LPF block is shown in Fig. 46. The size of LPF is 463.1um x 273.6um. The layout of analog baseband circuit layout of topology(2) is shown in Fig. 47(b). In order to reduce area, a switch is added before buffer to switch the first VGA output or total circuit output to characterize the output signal of VGA. The layout of analog baseband circuit layout of topology(1) is showed in Fig. 47(a)

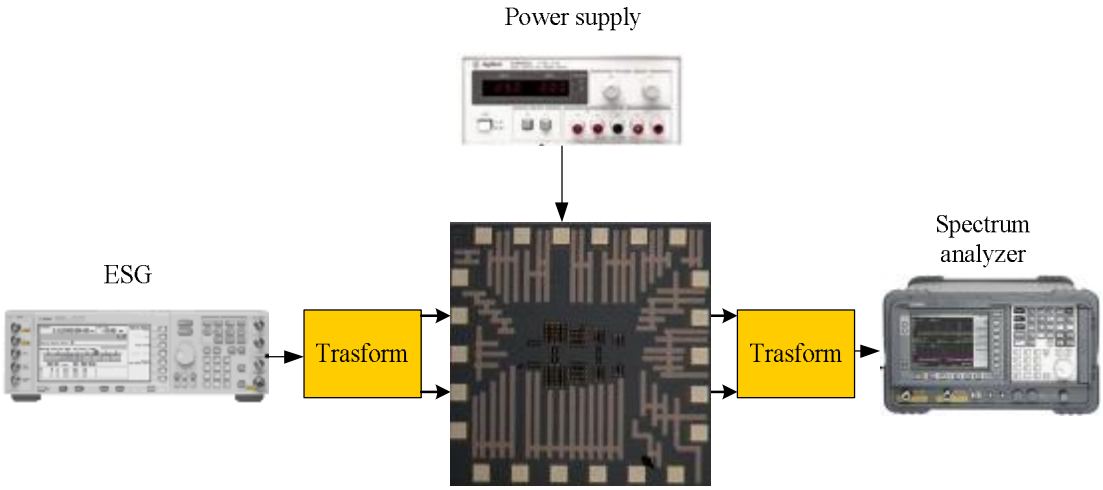


Figure 48 Test setup

Fig. 48 is the testing setup for measuring chip on wafer. In the circuit spectrum analyzer is used to measure frequency response and dynamic range. All of the design are fully-different. A transformer is applied to convert signal after ESG and before Spectrum analyzer.

Fig. 49 show a measurement result of harmonic distortion of the LPF when small Gm is opened and Vcrl=0.4. Because transformer has -8dB loss, 4dBm signal from ESG and LPF receives -4dBm signal for 0.4Vpp. From measurements the pole and zero is shifted the simulation but we can see the LPF still have two zeros. Fig. 50 shows the harmonic distortion measurement result when input signal is 4dBm at 1.73MHz. The dynamic range is limited by the high 2^{nd} tone and is 11dB.

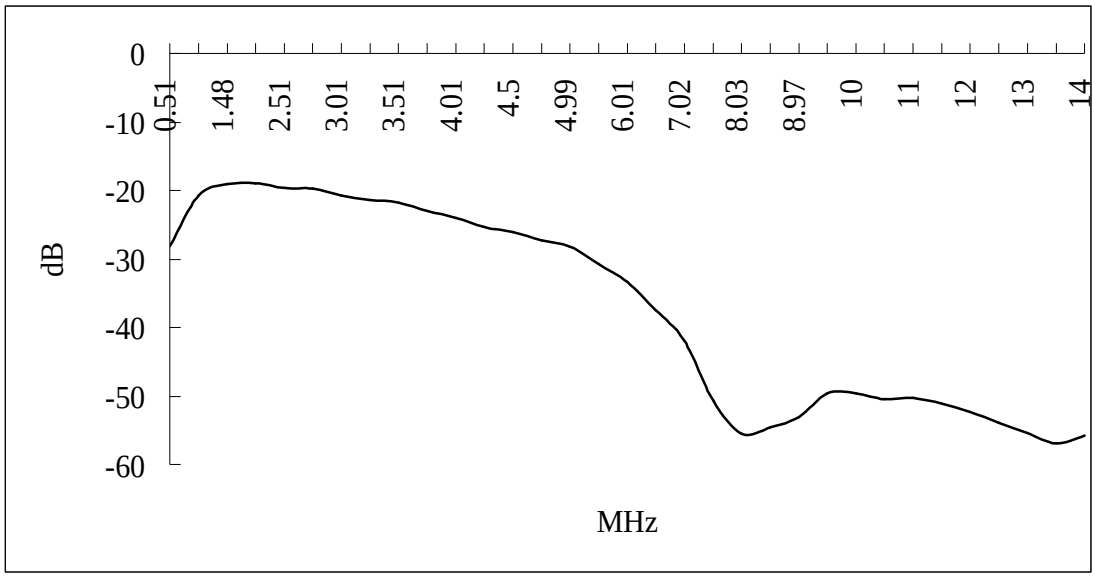


Figure 49 Measurement result of harmonic distortion

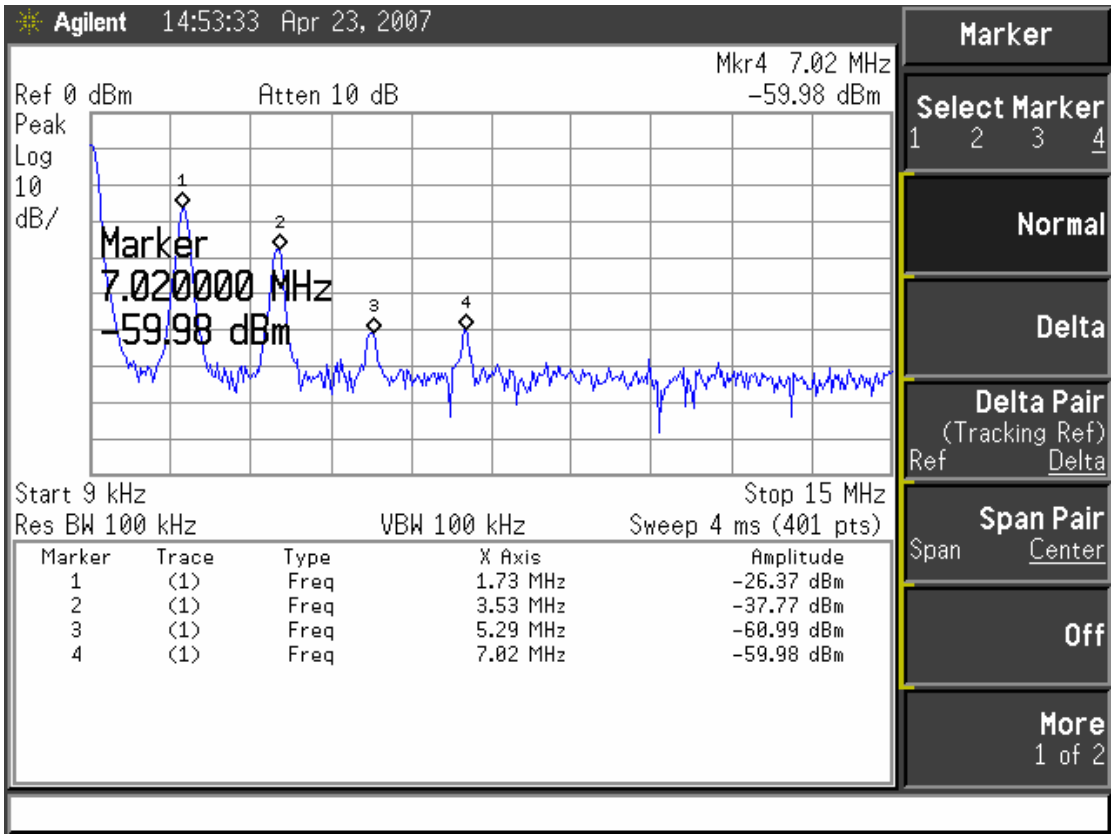


Figure 50 Measurement result of harmonic distortion

Several chip samples were measured and recode the -3dB from flat gain in different control voltage. Fig. 51 and Fig. 52 show the result of small and big Gm

respectively. The -3dB frequency is linearity to the control voltage. Because of the parasitic capacitor and the variation of gm cell, the -3dB bandwidth of different chips don't match the simulation results.

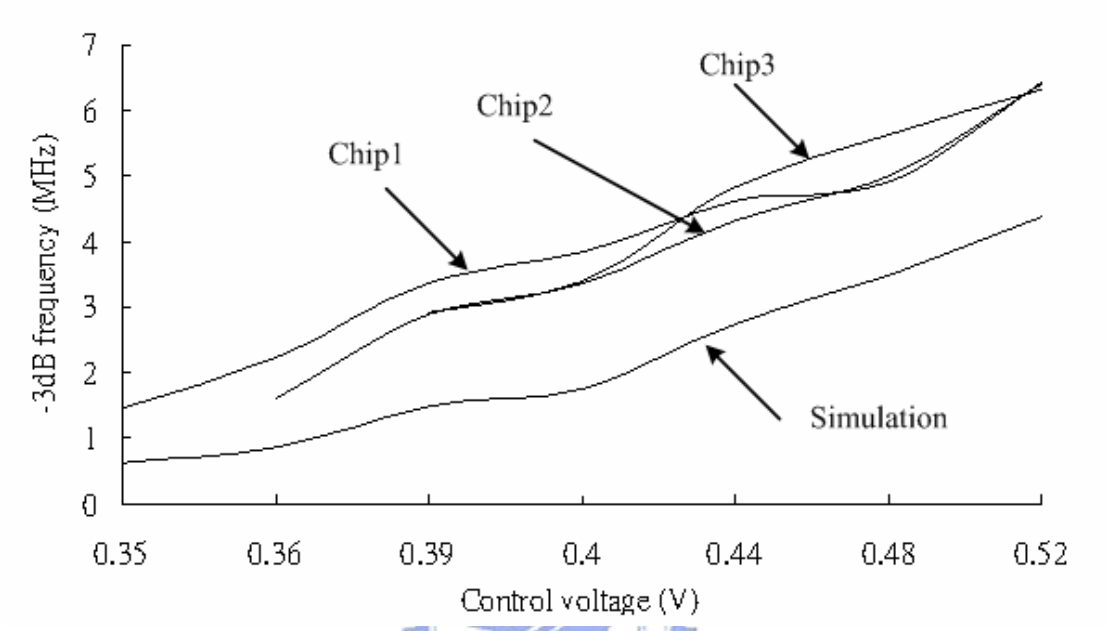


Figure 51 -3dB frequency in different control voltage for small Gm

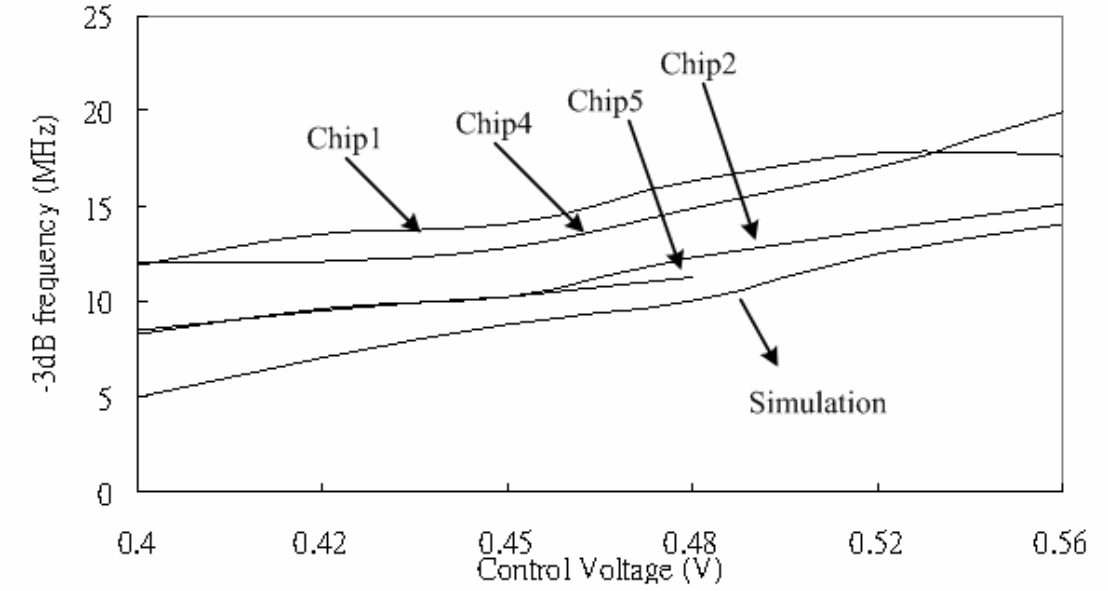


Figure 52 -3dB frequency in different control voltage for big Gm

The comparison between reference publications is shown in Table 13.

Parameters	Spec.	Topology(1)	Topology(2)	APMC.2005[6]
Technology	CMOS0 .13um	CMOS 0.13um	CMOS 0.13um	CMOS 0.16
Standard	WiMax	WiMax	WiMax	WLAN
Power supply	1.2V	1.2V	1.2V	1.8V
3-dB bandwidth	0.625M~14MHz	0.625B~6.2MHz	0.625B~5.3MHz	7.56 19.5 26.5MHz
Power consumption	As small as possible	7.624mW~26.8mW	7.624mW~26.8mW	22.248mW
NF	As small as possible	84.9dB (734.2uV/sqrt(Hz)@output noise)	51.87dB (42.19uV/sqrt(Hz)@output noise)	
Gain range	16dB-86dB	16~86dB	16~86dB	20~60dB
Dynamic range	50dB (0.4Vpp)	>38.17dB (0.4Vpp)	>38.19dB (0.4Vpp)	

Parameters	APMC.2005[7]	JSSC.2006[8]	TCSI.2006[9]
Technology	CMOS0.13um	CMOS0.18um	CMOS0.13
Standard	UMTS WLAN	WLAN	WLAN UMTS
Power supply	2.5V	1.6-2V	1.2
3-dB bandwidth		3.4~40MHz	2.1,11MHz
Power consumption	55mW	11.6mW	19.44mW
NF	51uVrms(IRN)	77.5nV/squrHz(Input noise)	1.12mVrms(output noise)
Gain range	-6~68dB	-8-32dB	8dB
Dynamic range		1.4%@ -8dB gain	52(1.4Vpp)

Table 13 Measurement comparison

Chapter 4

Conclusion

The thesis has presented an analog baseband circuit employing a linear-in dB VGA and a tunable LPF for WiMax. It includes of three 14MHz low power VGA and a tunable bandwidth low power LPF. The novel topology has been applied to the analog front-end for WiMax direct conversion receiver which perform low power, wide dynamic gain range and high data rate. In conclusion, the key contributions presented in previous chapters are summarized below.

4.1 Summary

An optimum arrangement of LPF and VGA for noise figure and interference trade-off is presented. Two transconductor operating in triode region for a tunable transconductor-C LPF is presented. A linear-in dB topology employing novel pseudo exponential technique for a low power VGA is presented. We use three VGA blocks and a LPF to constitute the analog baseband circuit. The analog baseband circuit

implemented in 0.13-mm CMOS process and arrange LPF in second location. The circuit provides a minimum gain of 16dB and maximum gain of 86dB while drawing 26.8wW from a 1.2-V supply. The dynamic range is 38.19dB for 0.4Vpp. The measurement result of LPF is presented

4.2 Future Work

In the thesis, there are some design considerations which we didn't attention. We give some recommendations and improvement in the section. First the analog baseband design is not optimum. The 2nd and 3rd VGA block gain range can be changed to have larger output swing for total design. The loading of each block didn't consider comprehensively so the bandwidth was limited. Second the non-ideal resistor of each transconductor is considered too much so the pole and zero will shift from the ideal value and the frequency response will decrease in advance. The layout didn't consider parasitic capacitors completely. Third the control circuit of the VGA block is only an inverter and DC shift circuit and the better choice is use OP to do control circuit. We didn't consider best choice is using OP for control circuit. We will make an improvement in the future work.

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