國 立 交 通 大 學

電子工程學系　　電子研究所

碩士論文

矽化鈷在含鍺介電質形成奈米點並構成非揮發性記憶體之研究

Study on $CoSi_2$ nanocrystals in Ge-doped dielectric layer for nonvolatile memory

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中華民國 九十七 年 五 月

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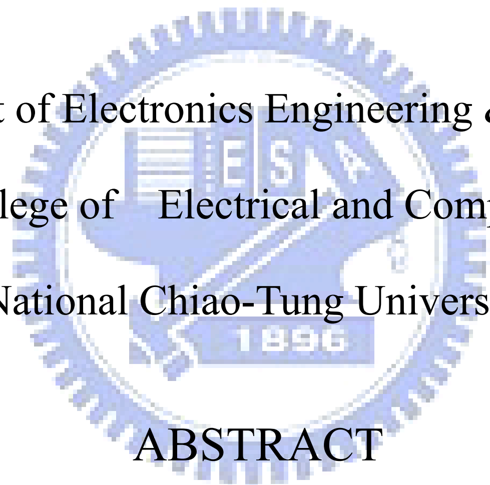

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ABSTRACT

In recent years, digital life has attracted great importance for Taiwan's electronics market. Then he portable electronic products have been applied widely, such as digital cameras, notebooks, hand-carry USB memories, a chip on credit card , PDA, GPS, memory card, MP3 audio players and so on. However, these portable electronic products are based on the nonvolatile memory (NVM) due to the need of low working power and portability. In a conventional nonvolatile memory (NVM), charge is stored in a ploy-silicon floating-gate (FG). However, it suffers some limitations for continual scaling down of the device structure. In FG memory, the electrons which injected from channel to the poly-silicon trapping layer influence the

shift of threshold voltage in the memory. Then it can be defined through the difference of threshold voltages as logic “0” & “1”. Nevertheless, the definition fails if the tunneling oxide provides a leakage path after repeatedly performing write/erase cycling. On other hand, the oxide will produce some defect after repeat impact during electrons the write/erase cycle because the whole structure of FG is semiconductor. All of the charge stored in FG will be trapped into trapping layer or be lost from trapping layer with leak path which was formed with defects. FG structure will have reliability problem when device scale down to nano-meter level.

Among the Metal Silicide, cobalt-silicide ($CoSi_2$) has been widely used as a contact source due to the lowest resistivity value (10-20 ~ $\mu\Omega$cm) and good thermal stability. In this thesis, $CoSi_2$ films were sputtered and we choose rapid thermal annealing (RTA) and sputter system in order to reduce process cost because of temperature controlling and reduce thermal budget because of diffusion reducing.

Co-sputtering approach was used to deposit the mixed cobalt, silicon and germanium film. After rapid temperature oxidation (RTO), Novel cobalt silicide nanocrystals embedded in the dielectrics which are doped with Ge have been formed. The charge storage effect of this novel trapping layer have also been investigated by capacitance-voltage (C-V), current density-voltage (J-V) measurement. Transmission Electron Microscopy (TEM), Secondary Ion Mass Spectrometer (SIMS) and X-ray photoelectron spectroscopy (XPS) have been used to analyze formation of the cobalt-silicide nanocrystals. In addition, the structure formed by co-sputtering the Co target with SiO_2, Si_3N_4 target and Al_2O_3 target have also been demonstrated in this work. The approach also shows good charge storage ability. The charge storage mechanism of various dielectrics has also been revealed by related material analysis.

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摘要

近年來，數位生活在台灣電子工業市場扮演了舉足輕重的角色，數位電子產品的應用已經受到廣大的青睞，像是數位相機、筆記型攜帶式、攜帶隨身聽 MP3 或 CD、信用卡晶片，攜帶型 USB 記憶體或記憶卡和日常生活會用到的 PDA、GPS 等等。這些個人式電子產品的發展則基於非揮發性記憶體元件的低功率消耗和可攜式。傳統的非揮發性記憶體是利用複晶矽浮停閘(floating gate)作為載子儲存的單元，而在元件尺寸持續微縮下，該結構將面臨一些瓶頸。當電子從通道注入

浮停閘儲存層，記憶體元件將會受到儲存載子影響它本身存在電場的影響，造成起始電壓的漂移。我們可將受浮停閘改變的起始電壓定義為1與0。然而，因為這種浮停閘結構為整層的半導體薄膜，在電子反覆的從穿遂氧化層進出這層浮停閘，會使得穿遂氧化層劣化以至於出現缺陷，當缺陷一旦產生之後，所有儲存的電子將會隨這層缺陷而產生局部漏電路徑，導致所寫入的儲存載子全部流失掉，無法達到原本應有之記憶的效果。

矽化鈷是一種金屬矽化合物現今已經因為它本身的低電阻(10-20 ~μΩcm)和熱穩定性而被廣大的應用在接觸面上。在本論文中我們使用共同濺鍍和快速退火系統分別進行薄膜沉積和進行退火。我們會使用快速退火系統是因為溫度控制的方便性和利用減少熱預算來降低擴散程度。

在本篇論文，我們透過濺鍍系統共打的方式沉積鈷、矽、鍺的混合性薄膜，再利用快速退火的方式製作一種新穎之矽化鈷物奈米點於含鍺介電層，並研究該結構金氧絕氧半(MOIOS)結構之儲存效益。除了此金氧半電容結構之C-V、J-V量測外，並透過一些材料分析如二次離子能譜(SIMS)、X光光電子能譜儀(XPS)釐清各元素扮演儲存機制之角色。此外，我們亦研究透過共同濺鍍金屬鈷和介電質材料如氧化矽，氮化矽及氧化鋁作為儲存層，透過電性量測，該結構亦展示不錯之載子儲存效果，除電性量測外亦透過相關之材料分析X光光電子能譜儀(XPS) 探討在不同介電質材料之間的形成機制。

致　　　　謝

這是一個過程，在撰寫本篇論文，在此論文即將完成的同時，研究所的生涯也即將告一段落。回想起這三年日子的每一天，聽著一些激勵歌曲，酸甜苦澀一點一滴不由自主的從心中竄起。在此過程，無論是碰到的人、經過的事，真的感觸良多。要感謝的人相當多，從醫界、學界、業界各式各樣的人都有，感激之情真的一言難示千意。

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新竹馬偕：郭岱宗　醫師

台北榮總：蔡昀岸、陳正豐、黃敏雄　醫師

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淑賢、雅芳、淑惠、淑偵、淑娟、淑雲、瑞文、慈蓮、欣怡　護

士、護理師

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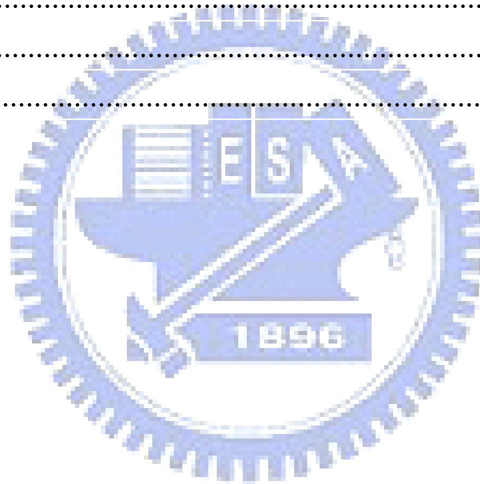

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Chapter 1
Introduction

To begin our study of memory, we need to address two central issues. First, what is memory? Second, what is the goal of research on memory?

1.1 General Background

1.1.1 The era of memory

In recent year, the portable electronic product have widely been applied due to the concept of low cost 、small volume and power-saving develop. Because of them, digital life has attracted great importance for electronics market in Taiwan. Then the portable electronic products have been applied widely, such as digital camera, notebook computer, MP3 walkman, hand-carry USB memory, a chip on credit card , PDA, GPS, memory card, MP3 audio players and so on. However, the electronic industry was subjected that electronic market was challenging it. The electronic industry urgently needs a new memory device to replace the magnetic-core memory because of its power consumption or other drawbacks then. Therefore, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory (or flash memory) at Bell Labs in 1967 [1.1] [1.2]. The stacked-gate FG device structure is shown in Fig. 1-1. Although a huge commercial success, conventional FG devices have their limitations. The trapped charges in the floating gate can be thermally stable without the disturbance by electric field and high temperature. However .it has a poly-silicon gate completely surrounded by dielectric.

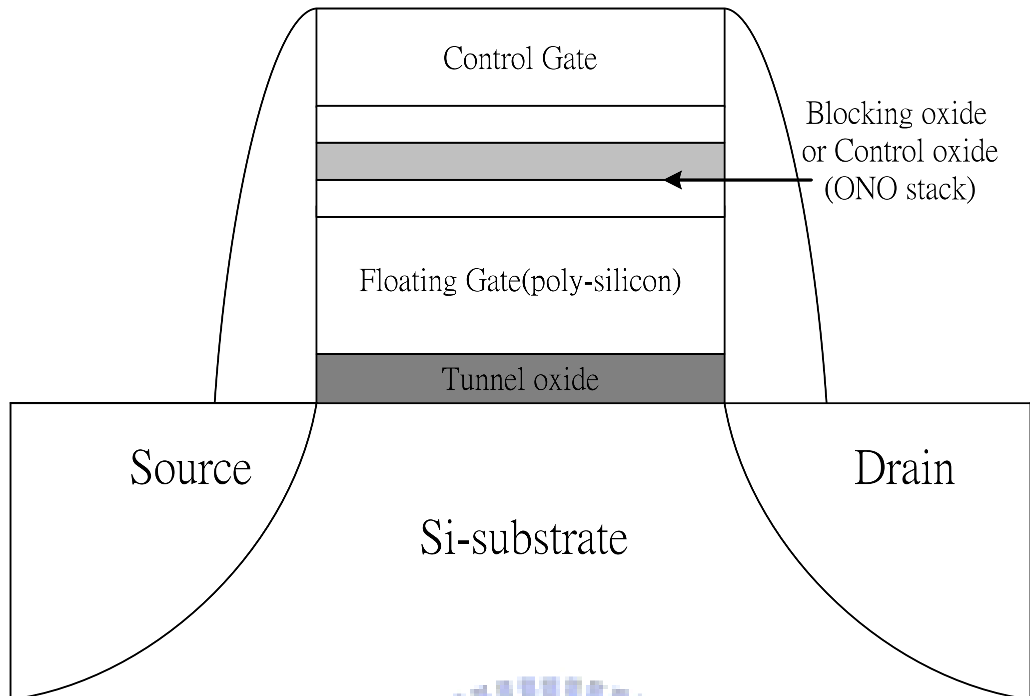


Figure 1-1 The structure of the conventional floating gate nonvolatile memory device. Continuous poly-Si floating gate is used as the charge storage element.
(Ref. Simon M. Sze, Kwok K. Ng, s "Physics of Semiconductor Device" Wiley, New York

Because of their research on memory and FG was invent, the electronics industry and market rapidly develop in Taiwan and world. We believe no one can diminish or deny the victory memory device has scored. The rapidly developed Endure rice science and technology allows us to explore more of it secret. The present storing device can be split into two main categories: One kind is volatile memory such as SRAM or DRAM and another is nonvolatile memory such as ROM、EPROM (Erasable Programmable Read Only Memory)、EEPROM (Erasable Programmable Read Only Memory). The volatile memory loses any data they store when the power is turned off; it requires constant power to remain viable. Most types of random

access memory (RAM) are very dense and have fast speed in writing and reading. RAM is massive applied in computer industry. The nonvolatile memories, we also could call NVM device, are a basic MOS transistor that has a source, a drain, an access, a control gate and a floating gate. It is structurally different from a standard MOSFET in its floating gate, which is electrically isolated, or "floating". The nonvolatile memories are subdivided into two main classes: floating gate and charge-trapping. The nonvolatile memory does not lose its data when the system or device is turned off (power off) named ROM, opposite one data will be lost or said volatile after power off named RAM. It was showed in Fig. 1-2. These two kinds of memories are most different in their data retention. In this research, research on nonvolatile memory is our priority. Although a huge commercial success, conventional FG devices still come to be in face of and challenge their limitations. The most prominent one is the limited potential for continued scaling down of vertical stack structure. This scaling limitation stems from the extreme requirements put on the tunnel oxide layer. Since the SiO_2 barrier between the floating gate and the MOSFET channel is thinner, its quality is critical to ensure good floating gate isolation. There were three major types of nonvolatile memory: (1) conventional FG memory (2) SONOS memory (3) nanocrystal memory. These memories have quick program/erase speed and low power losing.

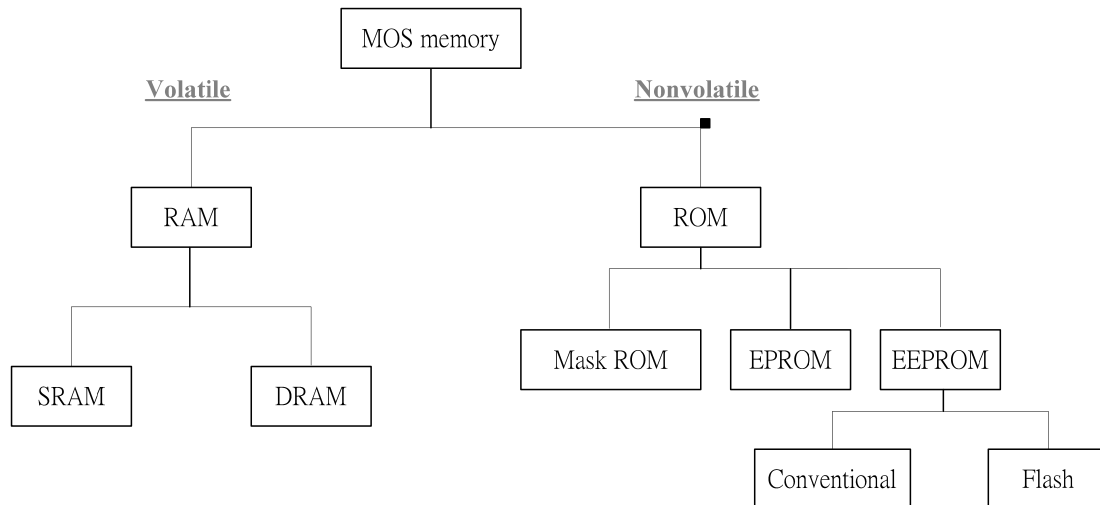


Figure 1-2 The history of memory tree

Moreover, in the coming years, portable systems will demand even more nonvolatile memories, either with high density and very high writing throughput for data storage application or with fast random access for code execution in place. Those digital products are based on the flash memory which is one kind of the nonvolatile memory that can be electrically erased and reprogrammed when power is off, so the flash memory device was more and more import in the world. The flash memory is the most important among the semiconductor industry. It can be classified into two major markets in Taiwan: code storage application and data storage application. In this chapter, we will introduce that some memory device how to develop in Taiwan and world, such as memory composed of metal nanocrystal2. In addition, the flash memory fabrication process is compatible with the current CMOS process and is a suitable solution for embedded memory applications. Therefore, flash memories are easily scalable replacements for EPROM (Erasable Programmable Read Only Memory) and EEPROM (Electrically Erasable Programmable Read Only Memory). EPROM can be electrically programmed, and need to be exposed to the ultra-violet

(UV) radiation for erasing the storage charge. However, EEPROM can be electrically erasable and programmable. Flash memories are new breeds of NVM in which not only every cell can be electrically programmed but also electrically erased at a large scale of cells at the same time. Since flash memory possesses these key advantages, it has become the mainstream nonvolatile memory device nowadays.

1.1.2 The basic structure of memory

In this kind of memory, electrons were transferred from the floating gate to the substrate by tunneling through about 3~5 nm thin silicon dioxide (SiO_2) layer or other high-k dielectric materials [1.3]. Tunneling is the process by which an NVM can be either erased or programmed and is usually dominant in thin oxides of thicknesses less than 12 nm. Storage of the charge on the floating gate allows the threshold voltage (V_T) to be electrically altered between a low and a high value to represent logic 0 and 1 respectively.

In floating gate memory devices, charge or data is stored in the floating gate and is retained when the power is removed. They consist of a stacked gate MOS transistor. Show like the above, there were three major types of nonvolatile memory: (1) conventional FG memory (2) SONOS memory (3) nanocrystal memory. For the conventional FG memory, Because of several defects such as interface defects in the tunnel oxide, they might induce a leakage path and all charge stored from the FG leaking back to the channel. That is why the conventional FG memory always needs thicker tunnel oxide to get better retention. There are many researches about leakage or high-K material in the world. From them, we can understand that its importance is not out of consideration about its operations. In order to overcome the scaling limitations of the conventional FG memory structure, SONOS memories [1-4 to 1-6] and nanocrystal memories [1-7 to 1-9] are two most mentioned candidates. We also

could clearly understand that the development history of NVM devices in Fig. 1-3 for SONOS memories structure in Intel corporate. One of them was FAMOS (Floating gate Avalanche injection MOS) device. It introduced by Frohman-Bentchkowsky [1-10]. High energetic electron created in the drain avalanche plasma writing the devices. Erasure is possible by UV or X-ray radiation. Fig. 1-4 was FAMOS. It was first operating floating gate device. And then, SAMOS (Stacked gate Avalanche injection MOS) is in Fig. 1-5(A) and was showed in [1-11]. This kind of device is written like FAMOS device. However, several difference in erasure mechanisms between FAMOS and SAMOS. Another, SIMOS cell was the n-channel version of the SAMOS devices Fig. 1-5(B). It was showed in [1-12]. Programming operation occurs because of Channel hot-electron (CHE) injection. This cell was used mainly for EPROM applications.

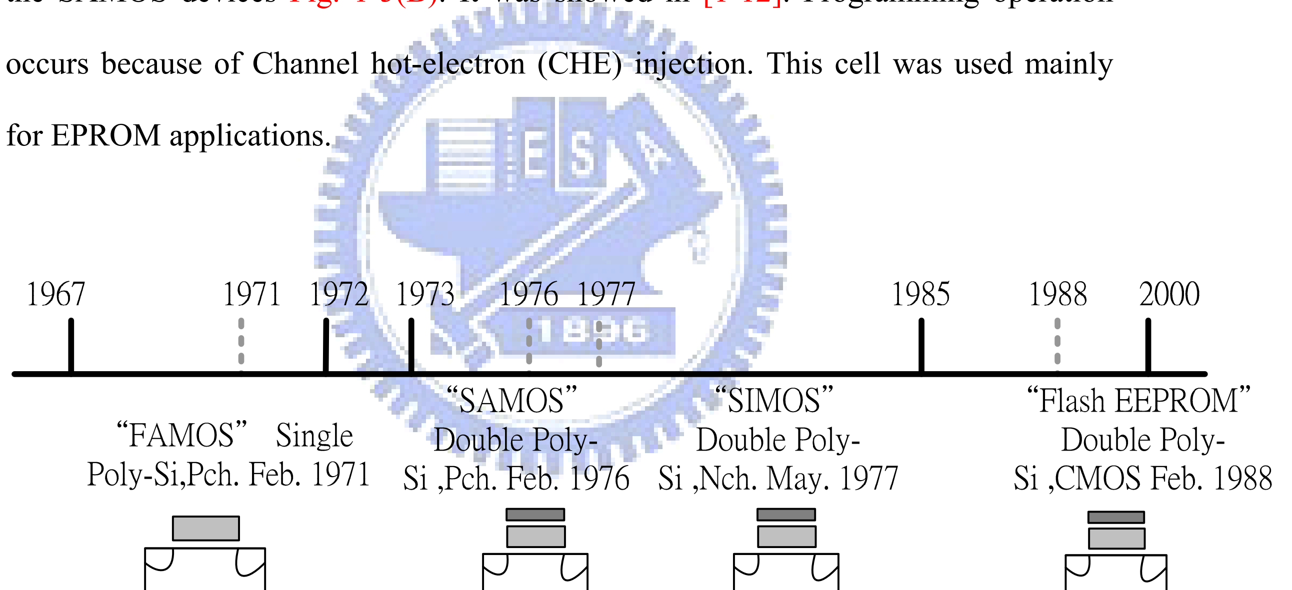


Figure 1-3 History of NVM (SONOS structure)

(Ref. Toshiba Corporation ULSI Research Center ***"Technology Trend of Flash-EEPROM — Can Flash-EEPROM overcome DRAM?"***, Symposium on VLSI Technology Digest of Technical Papers, 1992, pp.6~9.)

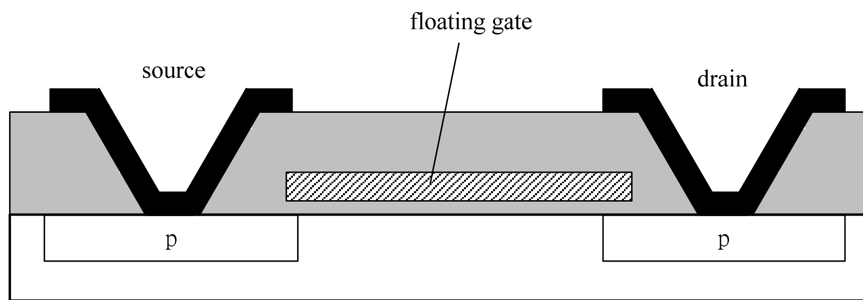


Figure 1-4 Basic structure of FAMOS

(Ref. Frohman-Bentchkowsky, D. "A fully decoded 2048-bit electrically programmable FAMOS read-only memory " Solid-State Circuits, IEEE Journal of, Volume: 6, Issue: 5 1971

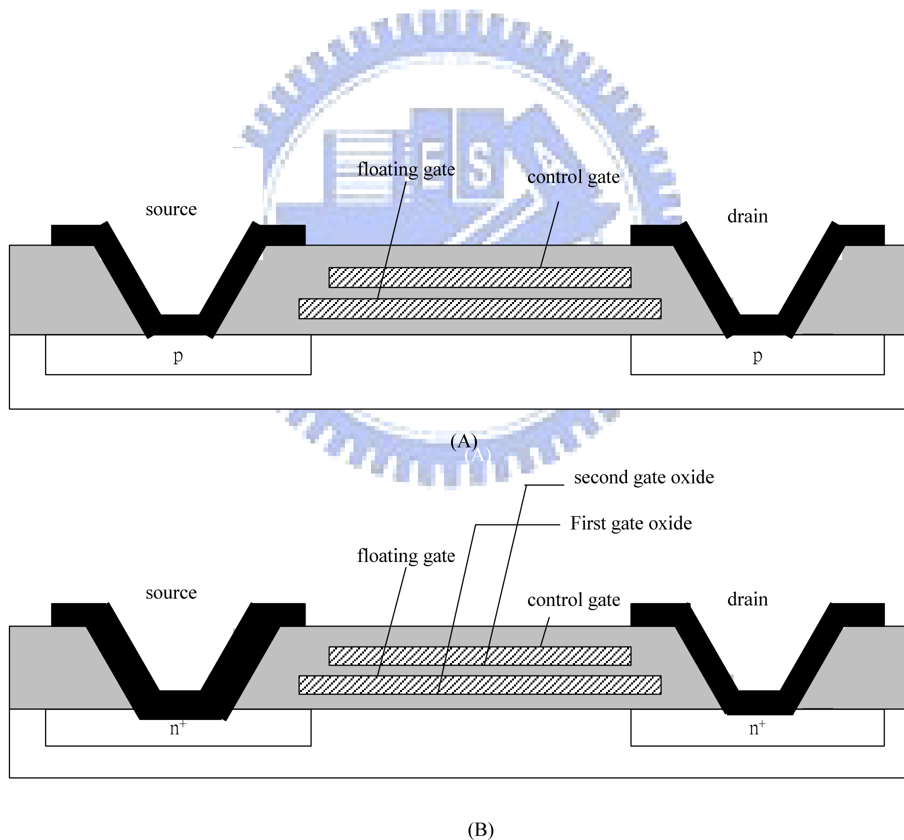


Figure 1-5 (A) basic structure of SAMOS (B) basic structure of SIMOS

(Ref. "Technology of a new n-channel one-transistor EAROM cell called SIMOS Electron Devices" IEEE Transactions on 1977)

1.2 SONOS Nonvolatile memory Devices

SONOS is the abbreviation of a basic memory. We could clearly understand that its basis structure is poly-Silicon/ (control or blocking) Oxide/Nitride/ (tunneling) Oxide/Silicon and show it in Fig. 1-6. The first nitride-base memory devices were extensively studied in the early 70s after the first metal-gate nitride device Metal/Nitride/Oxide/Silicon (MNOS) was reported in 1967 by Wegener et al [1-13]. It is showed in Fig. 1-7. However, MNOS were p-channel structures with aluminum gate electrodes and thick (45 nm) silicon nitride charge storage layers. Write/erase voltages were typically 25-30 V. In the late 1970s and early 1980s, scaling moved to n-channel silicon-nitride-oxide-silicon (SNOS) devices with write/erase voltages of 14-18 V. It is showed in. In the late 1980s and early 1990s n- and p-channel SONOS devices emerged with write/erase voltages of 5-12 V. SONOS based nonvolatile memory has emerged as the most mature nonvolatile semiconductor memory (NVSM or NVM) currently in use for a wide range of applications in our daily life and becomes the most popular charge trapping device because of its complete compatibility with existing advanced it CMOS technology. On the other hand, the SONOS memory device has received a lot f attention due to its advantages over the traditional floating-gate flash EEPROM device such as including reducing process complexity, lowering voltage operation, getting higher operation speed, improving cycling endurance and elimination of drain-induced turn-on [1-14]- [1-17]. The basis of this kind memory is trapping charge to change its threshold Voltage. Aside from them, they also can cost down because that it can achieve two-bit per cell. The charges of storage elements in SONOS memory are the charge traps distributed throughout the volume of silicon nitride layer. A typical trap has a density of order 10^{18}~ 10^{19}cm^{-3} according to Yang et al [1.18] and stores both electrons and holes

(positive charges) injected with F-N or direct tunneling from the channel. The intrinsic distributed storage is an advantage of the SONOS device over the FG device. It has improved endurance, since a single defect will not cause the discharge of the memory. In the meantime, SONOS memories hardly reach a data retention for 10 years. This is why the actual use of SONOS memories is limited to military applications needing high radiation hardness [1-19] and [1-20].

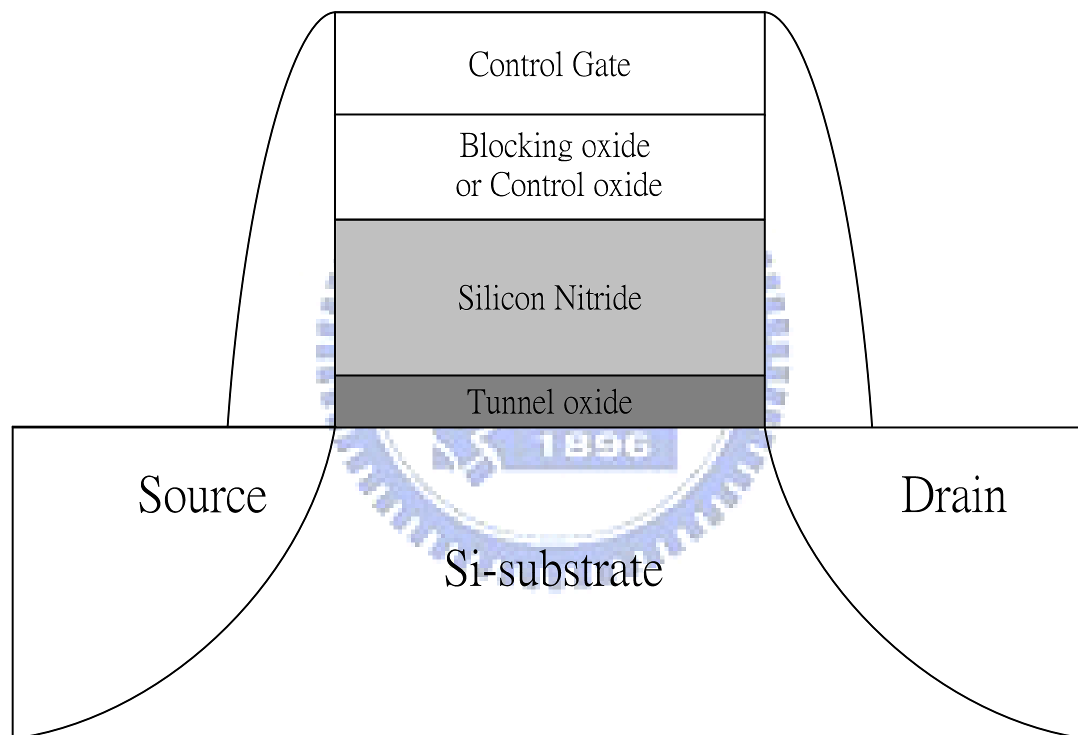
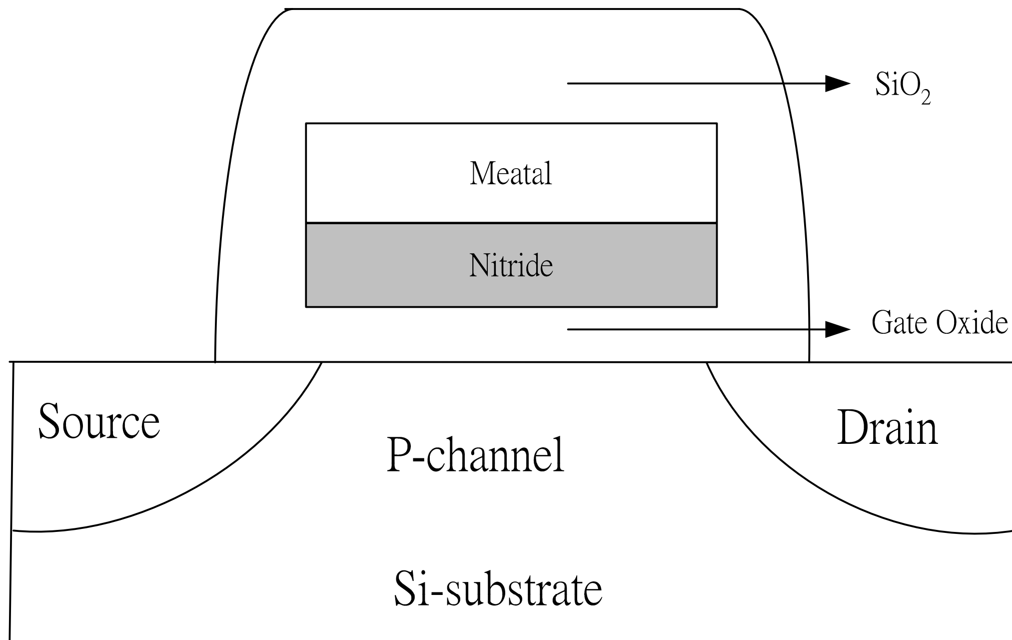


Figure 1-6　SONOS structure memory



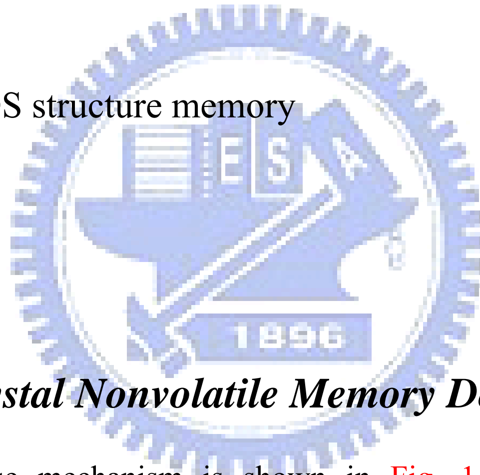


Figure 1-7 MNOS structure memory

1960s~1970s

1.3 Nanocrystal Nonvolatile Memory Devices

The program/erase mechanism is shown in Fig. 1-8. SONOS devices are programmed by channel hot electron (CHE) injection or Fowler-Nordheim (F-N) tunneling mechanism, mainly. In general, the program speed in CHE injection is 10^2~10^3 times faster than in F-N tunneling [1-21]. During programming, the control gate is biased positively so that electrons from the channel can tunnel across the SiO_2 into the nitride layer with F-N tunneling mechanism I_1 and some electrons will continue to move through the nitride layer then across the control oxide finally into the control gate I_2 with the same mechanism. Last, saturation of charging will be reached when I_1=I_2. The remaining trapped charges in the nitride layer provide the electrostatic screening of the channel from the control gate. Therefore, there is a

threshold voltage shift (ΔVT) resulting from trapped charges in nitride and because of that SONOS can be used as a memory device just like conventional floating gate devices.

Last, the SONOS memory device still has to face the challenge in the future for high density nonvolatile application, which require lower power (<5V), lower power consumption, faster operation speed, longer retention time and superior endurance characteristics.

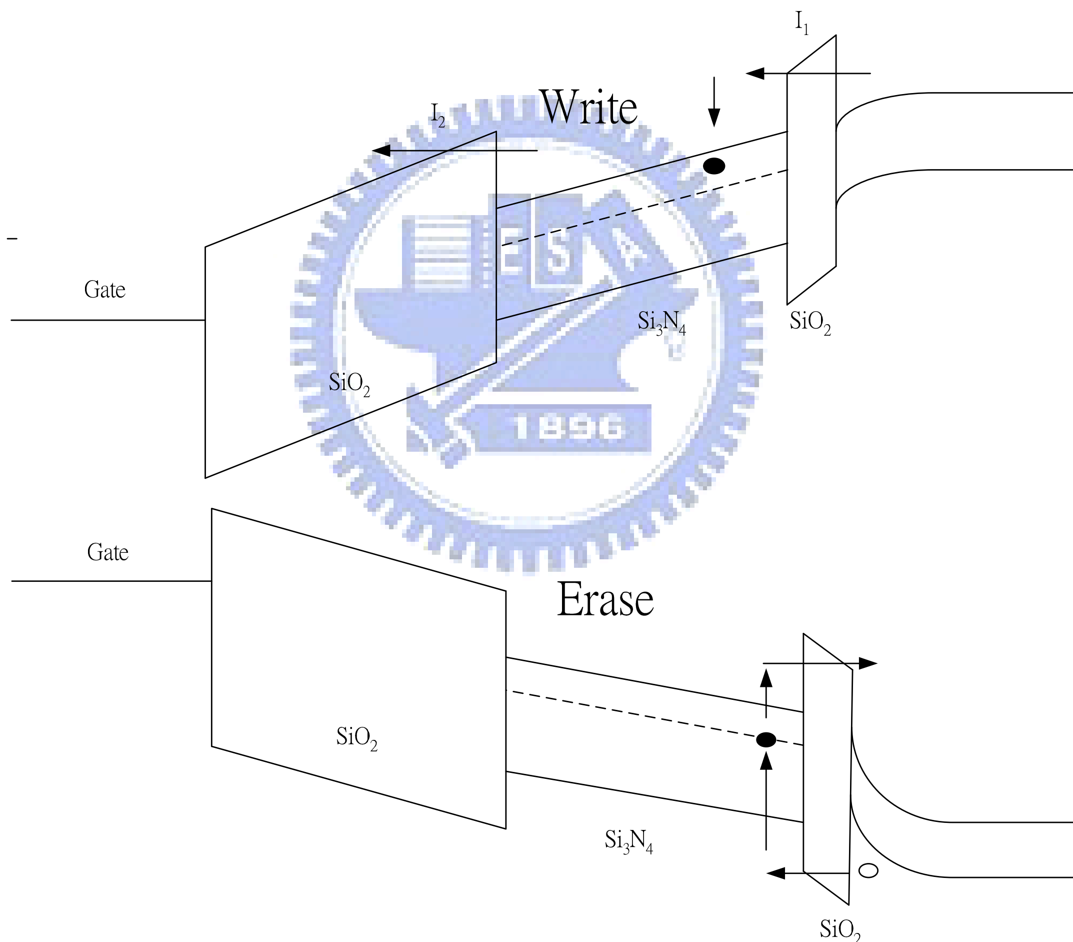


Figure 1-8 The energy band diagrams of the write/erase operation for a SONOS device.

In the early 1990s nanocrystal nonvolatile memories first was introduced by IBM researchers. Some of the most compelling studies have focused on the flash memory with a granular floating gate made out of silicon nanocrystals [1-22] [1-23]. Fig. 1-9 illustrates nanocrystal nonvolatile memory device structures. The employment of Si nanocrystals as discrete floating gates is a promising way to limit the lateral charge communication in an EEPROM, which in consequence provides a means for extending the scaling limit of flash memories. The tunneling oxide thickness of this memory device was 4.5 nm. Writing/Erasing time was smaller than 100 nanoseconds. Writing/Erasing number of times was greater than 10^9 times. Operating voltage was 2.5V and long retention time. Those proved that using discontinuing FG replacing continuing FG maybe nice method of improving floating gate memory. On the other hand, charge was not stored on a continuous FG poly-Si layer, but instead on a layer of discrete, mutually isolated, crystalline nanocrystals or dots typically made of semiconductor material. Each dot will typically store only a handful of electrons which tunneled from channel. Collectively the charges stored in these dots control the channel conductivity of the memory transistor. The charges loss often through lateral paths in nanocrystal-based memory devices can be suppressed by the oxide isolation or other insulator such as high-k material between nanocrystals, these devices exhibited superior charge storage characteristics compared with conventional floating-gate memory devices. All stored charges won't be lost through the few leaky paths since the charges are stored in distributed nanocrystals or called nanodots.

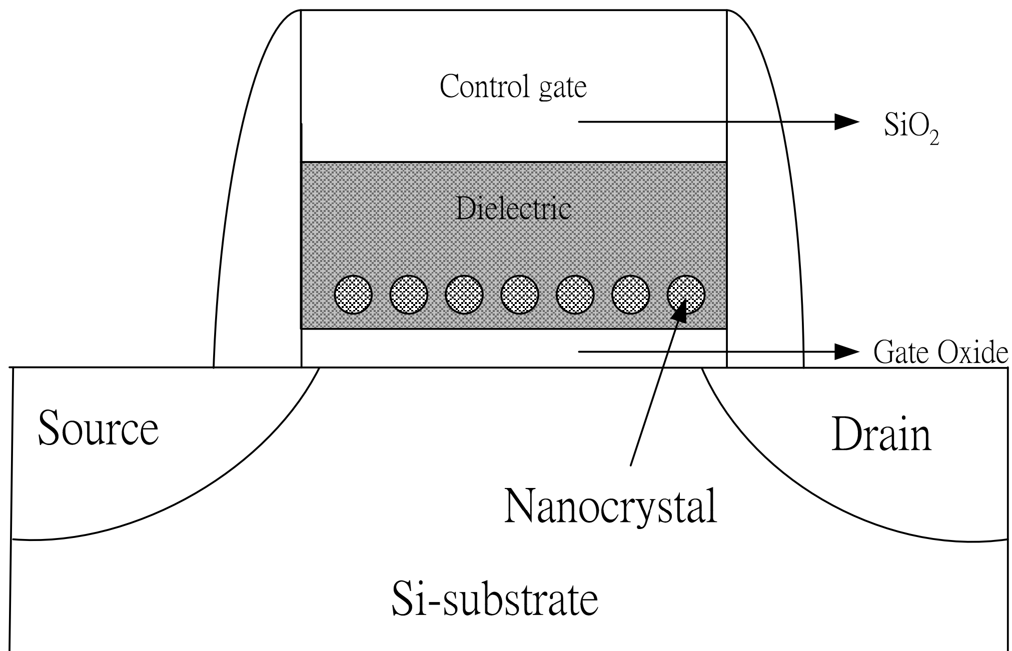


Figure 1-9 The structure of the nanocrystal nonvolatile memory device. The semiconductor nanocrystals or metal nanodots are used as the charge storage element instead of the continuous poly-Si floating gate

When comparing with conventional stacked gate NVSM devices the charge storage on nanocrystal offers several advantages. The first thing we notice is that its thinner tunnel oxide without sacrificing data volatility. Because of this, reducing the tunnel oxide thickness is not only a key to lowering operating voltages but also increasing operating speeds. This claim of improved scalability results not only from the distributed nature of the charge storage, which makes the storage more robust and fault-tolerant, but also from the beneficial effects of Coulomb blockade [1-24] and quantum confinement effects (band-gap widening; energy quantization). However, both them can be exploited in sufficiently small nanocrystal geometries (about sub-3 nm dot diameter) to further enhance the memory performance.

There are some other important advantages. First, nanocrystal memories use a more simplified fabrication process as compared to conventional stacked-gate FG

NVM by avoiding the fabrication complications and reducing costs of a dual-poly process. Further, due to decrease the effects of Drain -FG coupling, nanocrystal memories suffer less from drain-induced-barrier-lowering (DIBL).because of this, these devices have intrinsically better punch-through characteristics. One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time. Alternatively, it allows the use of shorter channel lengths and therefore smaller cell area (i.e., lowering cost). Finally, nanocrystal memories are characterized by excellent immunity to stress induced leakage current (SILC) and oxide defects due to the distributed nature of the charge storage in the nanocrystal layer.

Unlike volume distributed charge traps (ex: nitride in SONOS NVM or some high-k material [1-25]), nanocrystals be deposited in a two-dimensional layer at a fixed distance from the channel separated by a thin tunnel oxide. By limiting nanocrystals deposition to just one layer and adjusting the thickness of the top blocking dielectric, charge leakages to the control gate from the storage nodes can be effectively prevented.

However, there are some intrinsic weaknesses as well. Of particular importance is the low capacitive coupling between the external control gate and the nanocrystal charge storage layer. This does not only result in higher operating voltages, thus offsetting the benefits of the thinner tunnel oxide, but also removes an important design parameter (namely the coupling ratio) typically used to optimize the performance/reliability trade-off.

1.4 Motivation

Because the portable electronic products have been widely applied, we have

known that the memory plays an important role in the market on chapter 1-1 and I won't restate. In recent years, there are many researches on semiconductor or metal nanocrystals as memory and considerable attention has been focused on semiconductor or metal nanocrystals embedded in the silicon dioxide of a metal oxide semiconductor (MOS) device for future high speed and low power consuming memory device. The self-assembling of silicon or germanium nanocrystals embedded in SiO_2 layers has been widely studied, and strong memory effect in MOS devices were reported [1-26]. The major advantages of metal nanocrystals over semiconductor include (1) high density of states around the Fermi level, (2) strong coupling between the nanocrystal and the substrate [1-31] (3) a wide range of available work function, and (4) smaller energy perturbation due to carrier confinement. I had chosen a kind of metal as the storage material of memory device because of those advantages. The metal material I chosen was cobalt. On the other hand, our researches were chosen cobalt or cobalt Silicide as the main materials for some reasons.

Among several kinds of nanocrystals devices, the metal and metal-silicide NCs are considered to be beneficial in its variable work function, higher density of states around the Fermi level and so on. We could know that metal silicide has been receiving attention in VLSI devices for interconnects, gate and source/drain contacts. Among the Metal Silicide, cobalt-silicide ($CoSi_2$) has been widely used as a contact source due to the lower resistivity value (10-18μΩ/cm) and good thermal stability [1-32]. Over the past years, several studies have been made on the memory that was based on Co or $CoSi_2$ nanocrystals. $CoSi_2$ thin films are often employed in the semiconductor technology. They have been mentioned that there was a nice method used to form $CoSi_2$ nanocrystals embedded dielectric layer such as SiO_2. We observed that the $CoSi_2$ nanocrystals were nucleated in SiO_2 layer, leading to an obvious memory effect [1-33]. However, $CoSi_2$ nanocrystals embedded $Si_{0.5}Ge_{0.5}$ layer has

never been studied so far. There were a lot of experiments forming Ge nanocrystal by oxidizing the $Si_{0.5}Ge_{0.5}$ film. Germanium (Ge) element is also a semiconductor; SiGe Semiconductor plays a key role in enabling these technologies by providing high-performance, low-cost power amplifiers and chip-scale RF front-end modules that comply with the latest wireless standards and market requirements. The transistor uses a modified design and IBM's proven silicon germanium (SiGe) technology to reach speeds of 210 Gigahertz (GHz) while drawing just a milliamp of electrical current. This represents an 80 percent performance improvement and a 50 percent reduction in power consumption over current designs. Germanium element has higher dielectric constant (~16.0, i.e., stronger coupling with the conduction channel). Germanium element may improve data retention time due to its smaller energy band gap. Because of these, we think that germanium element maybe good memory device fabrication materials. Germanium element component was added into the Si and Co mixed layer. At the same, we tried to deposit $Si_{0.5}Ge_{0.5}$ thin film by co-sputter system and then anneal it by Rapid Thermal Annealing (RTA) system. We chose RTA to avoid Ge or Co over oxidizing. Several studies have been made on this memory which is based on the $Si_{0.5}Ge_{0.5}$ co-sputtered film. We also ascertain what role Ge and Co plays on the memory devices.

A three-phase study was designed to explore the formation of cobalt-silicide, the role of capped oxide before RTA and the procedure of oxidation mechanism. It this investigation about co-sputtered film we carried out three different experiment procedures and materials.

1.4.1 Study on formation of cobalt-silicide ($CoSi_2$) nanocrystals for the application on nonvolatile memory

Among several kinds of NCs devices, the metal and metal silicide NCs are

considered to be beneficial in its variable work function, higher density of states around the Fermi level. In addition, the dielectric layer that NCs embedded in also can contribute the charge storage sites by defects or traps created in the interfaces between different materials[10-11]. In this investigation, the formation of cobalt-silicide NCs was investigated by adding Ge elements into the cobalt-silicide film using co-sputtered Co and $Si_{0.5}Ge_{0.5}$ targets on tunnel oxide. After thermal oxidation process, the cobalt-silicide NCs are formed and the additional Ge elements are oxidized. Furthermore, the oxidized Ge elements contribute extra charge trap sites.

1.4.2 Post-oxidation annealing procedures of Co-Si-Ge thin film as trapping layers in oxygen ambient by annealing system

In previous section, we have studied on formation of cobalt-silicide ($CoSi_2$) nanocrystals and the role of capped oxide during the formation of cobalt-silicide ($CoSi_2$) nanocrystals in Ge-doped dielectric layer. We could understand that capped oxide plays a important role. In this section, let us now shift the emphasis away from the sample with cap to the sample without cap and let us examine the mechanism of oxidation in more detail. We chose pure Co and $Si_{0.5}Ge_0$ targets to form a Co_{rich}-Si-Ge thin film with sputter system because the SiO_2 and GeO_2 reaction is thermodynamically more preferable than CoO during annealing. Sufficient Co atoms could react with silicon to $CoSi_2$ nanocrystals according to previous section. It could realize the procedure of oxidation mechanism when the samples are annealed with varies material analysis.

1.4.3 The role of capped oxide during the formation of cobalt-silicide ($CoSi_2$) nanocrystals in Ge-doped dielectric layer

The floating-gate memory have faced a challenge to devices scaling down [1-34]-[1-35]. Among the reported literature, a structure with distributed nanocrystals as charge storage sites is considered a potential resolution to replace the conventional memory structure [1-36]-[1-37]. Many different researches of the nanocrystals such as the development of material, the improvement of performance and the electrical operation of nanocrystals devices have been reported in the recent year [1-38] to [1-43]. In the development of material, the structure combined with cobalt-silicide nanocrystals and oxidized germanium is presented as a trapping layer for the application of nonvolatile memory [1-44]. In order to form the cobalt-silicide nanocrystals and oxidized germanium, rapidly thermal oxidation (RTO) is necessary. However, the parameter of RTO process is difficult to control such as the flow rate of oxygen or the time of process affects the aggregation of nanocrystals seriously.

In this thesis, the aggregation behavior of cobalt-silicide nanocrystals during the RTO process has been studied. The results of Transmission electron microscopy (TEM) and Secondary Ion Mass Spectrometer (SIMS) indicate that the capped oxide enhances the aggregation of nanocrystals obviously. It also restrains the diffusion and oxidation behaviors of Co and Ge during thermal treatment. Therefore, a capped oxide before RTO process is essential for the aggregation of cobalt-silicide nanocrystals in Ge-doped dielectric layer by RTO process.

Chapter 2

Nonvolatile Memory basic concept, operation mechanism and material analysis

2.1 Reading operation

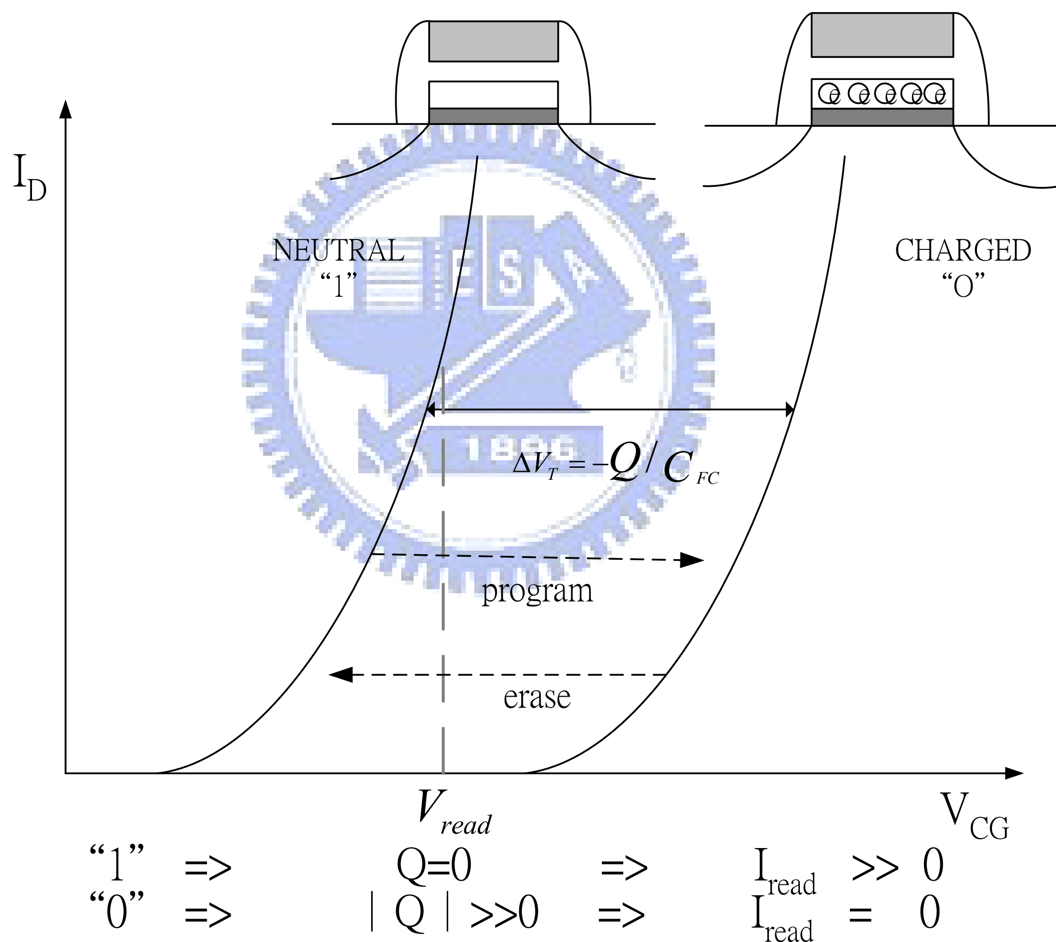
In this chapter, the program and erase mechanisms of nonvolatile memory device will be introduced. Most of operations on novel nonvolatile memories, such as nanocrystal and SONOS memories are base on the concept of Flash memory. The data stored in a Flash cell can be determined measuring the threshold voltage of the FG MOS transistor. The best and fastest way to do that is by reading the current driven by the cell at a fixed gate bias. If a dot or nanocrystal has to be stored in a bit of the memory, there will be different procedures. In the current–voltage plane two cells, respectively, logic "1" and "0" exhibit the same transconductance curve but are shifted by a quantity—the threshold voltage shift (ΔV_t). The threshold voltage shift of a flash transistor can be written as

$$\Delta V_T = -\frac{Q}{C_{FC}}$$

Where Q is the charge weighted with respect to its position in the gate oxide and C_{FC} is the capacitances between the floating gate and control gate. Hence, once a proper charge amount and a corresponding is defined, When writing operation is completed it is possible to fix a reading voltage in such a way that the current of the "1" cell is very high (in the range of tens of microamperes), while the current of the "0" cell is zero, in the microampere scale. It is showed in Fig. 2-1 clearly. In this way,

it is possible to define the logical state “1” from a microscopic point of view as no electron charge (or positive charge) stored in the FG and from a macroscopic point of view as large reading current. To a nonvolatile memory, it can be “written” into either state “1” or “0” by either “programming” or “erasing” methods, which are decided by the definition of memory cell itself. There are many solutions to achieve “programming” or “erasing”.

Besides, the importance of material analysis (such as XPS, SIMS and so on) was another point I focus on in this chapter. I will illustrate them in this chapter.



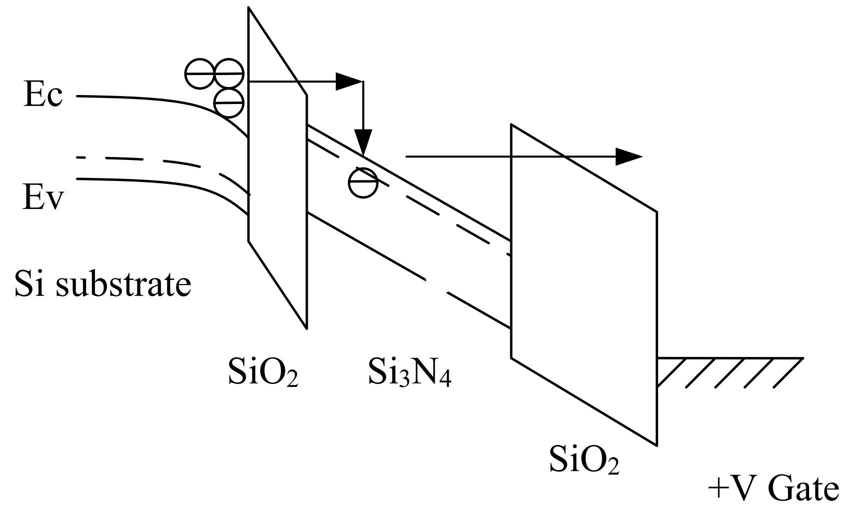
“1” => Q=0 => I_{read} >> 0
“0” => | Q | >>0 => I_{read} = 0

Figure 2-1 Floating-gate MOSFET reading operation
(Ref. ROBERTO BEZ, EMILIO CAMERLENGHI, ALBERTO MODELLI, AND ANGELO VISCONTI, **Introduction to Flash Memory,** PROCEEDINGS OF THE IEEE, VOL. 91, NO. 4, APRIL 2003)

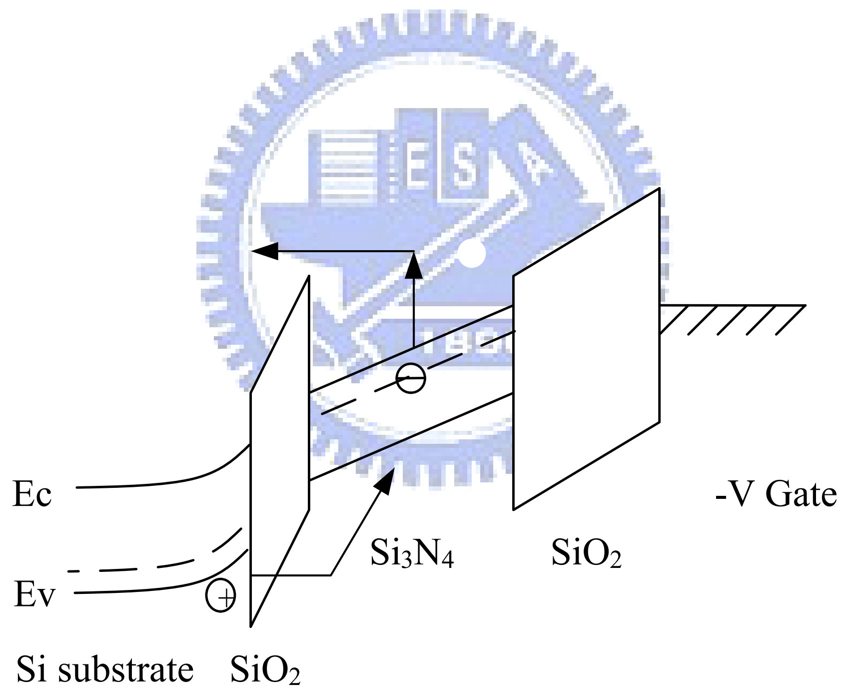
2.2 Basic Program/Erase Mechanisms

2.2.1 Carrier Injection Mechanisms

The problem of writing an FG cell corresponds to the physical problem of forcing an electron above or across an energy barrier. The problem can be solved exploiting different physical effects [2-1]. The three main physical mechanisms used to write an FG memory cell are sketched. Tunneling is a quantum mechanical process. For nonvolatile memory which has FG on the gate such as SONOS structure, the writing and erasing processes for an n-channel semiconductor memory device are illustrated schematically in Fig. 2-2. During the writing process, a positive gate voltage is applied to inject channel inversion-layer electrons into the nitride layer. I could talk by the same token. During the erasing process, a reverse gate bias is applied to cause the electrons to tunnel back into the channel and the accumulation layer holes to tunnel into the nitride from the channel. There are many ways to achieve “programming” or “erasing”. Tunneling through the oxide can be attributed to different carrier-injection mechanisms. Which process applies depends on the oxide thickness and the applied gate field or voltage. In general, hot carrier electron injection (CHE) and tunneling injection are two kinds of common operation mechanism employed in novel nonvolatile memories. Tunneling injection methods includes direct tunneling, Fowler–Nordheim (FN) tunneling, Modified Fowler–Nordheim tunneling (MFN) and trap assistant tunneling (TAT). These are the main programming mechanisms employed in memory [2-2] to [2-4]. They were showed in Fig. 2-3.



(a) write mode



(b) erase mode

Figure 2-2 Memory band diagram in (a)write mode (b)Erase mode

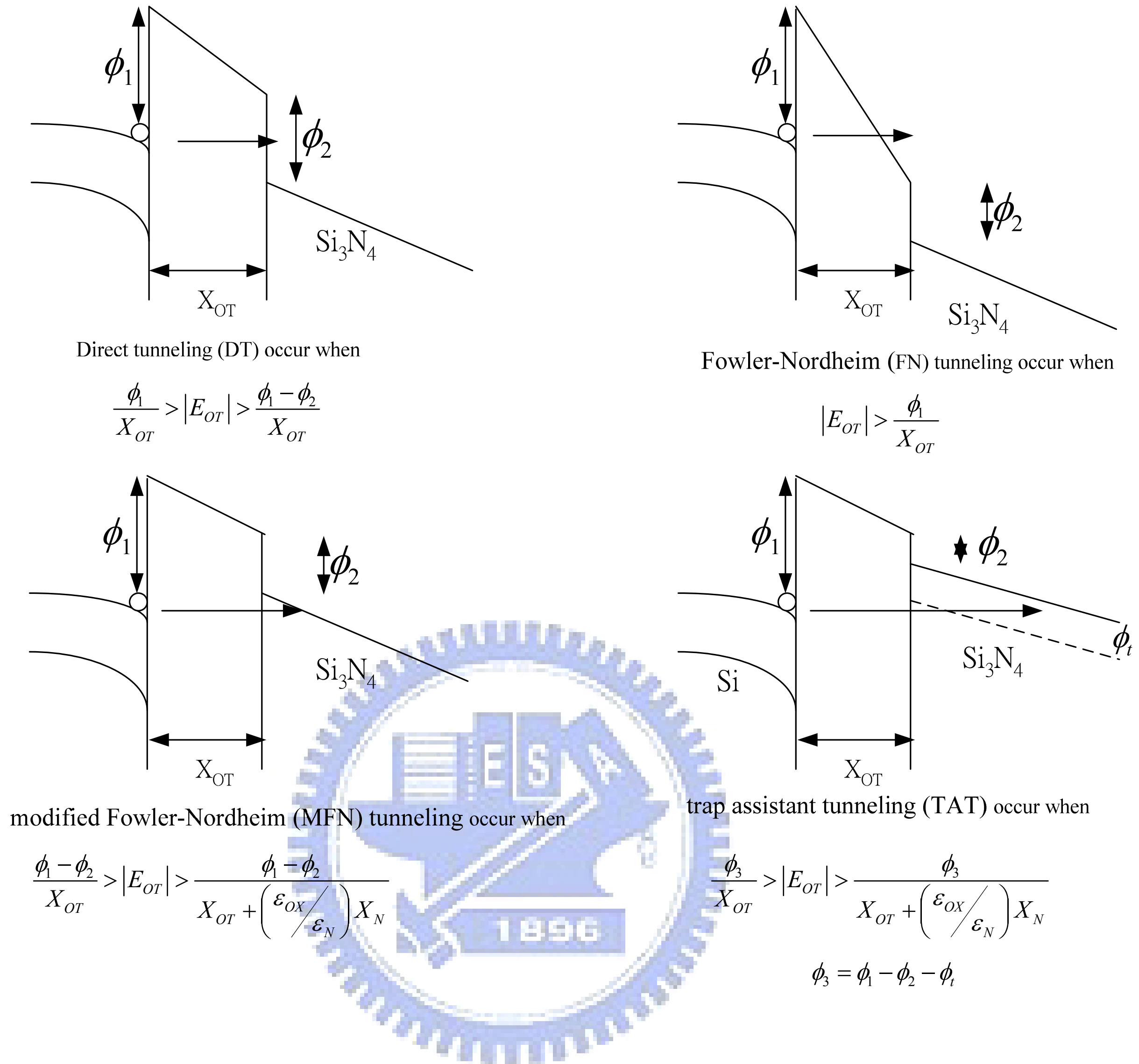


Figure 2-3 Fourth approaches to programming methods, described by Hu and White (Ref. Amit K. Banerjee, Yin Hu, Matthew G. Martin and Marvin H. White, An Automated SONOS NVSM Dynamic Characterization System, *0-7803-1290-N3* $3.00 01993 *IEEE)*

2.2.2 Channel Hot Electron (CHE) Injection

Channel hot electron (CHE) [2-5] injection is widely used as programming method in nonvolatile memories (NVM), especially in floating-gate [2-6] and

NROM^{TM} [2-7] [2-8] devices. The physical mechanism of CHE injection is relatively simple to understand qualitatively. An electron traveling from the source to the drain have gained very high kinetic energy after being accelerated by a strong electric field in areas of high field intensities within a semiconductor (especially MOS) device. At low fields, this is a dynamic equilibrium condition, which holds until the field strength reaches approximately 10^5V/cm [2-9]. For fields exceeding this value, electrons are no longer in equilibrium with the lattice, and their energy relative to the conduction band edge begins to increase. Because of their high kinetic energy, hot carriers can get injected and trapped in areas of the device where they shouldn't be, forming a space charge that causes the device to degrade or become unstable. Electrons are "heated" by the high lateral electric field, and a small fraction of them have enough energy to surmount the barrier between oxide and silicon conduction band edges (electrons need about 3.1eV). In the other hand, the effective mass of hole is heavier than one of electron. It is too hard to obtain enough energy to surmount oxide barrier. Therefore, hot-hole injection rarely is employed in nonvolatile memory operation.

2.2.3 Fowler–Nordheim (FN) Tunneling

Fowler-Nordheim (FN) tunneling mechanism is the process whereby electrons tunnel through a barrier in the presence of a high electric field and occurs when applying a strong electric field (in the range of 8-10 MV/cm) across a thin oxide. In these conditions, the energy band diagram of the oxide region is very steep. Fowler-Nordheim (FN) tunneling mechanism is based on the quantum mechanical process which is an important mechanism for thin barriers.

The tunnel probability that we derived from the time independent Schrödinger equation is

$$\Psi(L) = \Psi(0)\exp\left[-\int_0^L \frac{\sqrt{2m^*[V(x)-E]}}{\hbar}dx\right]$$

The minus sign is chosen since we assume the particle to move from left to right. For a slowly varying potential the amplitude of the wave function at $x = L$ can be related to the wave function at $x = 0$.

This equation is referred to as the WKB (Wentzel-Kramers-Brillouin) approximation [2-10]. Using a free-electron gas model for the metal and the WKB approximation for the tunneling probability, one obtains the following expression for current density [2-11]. The tunneling probability, Θ , can be written

$$\Theta = exp\left[-\frac{4}{3}\frac{\sqrt{2qm_{OX}^*}}{h}\frac{\phi_B^{3/2}}{E}\right]$$

the electric field equals E = ${}_{B}$/L

${}_{B}$ is the barrier height

m_{OX}^* is the effective mass of the electron in the forbidden gap of the dielectric

$\hbar$ is the Planck's constant,

q is the electronic charge,

E is the electric field through the oxide.

The carrier density equals the density of available electrons multiplied with the tunneling probability, yielding:

$$J = nqV_R\Theta \propto \phi_B^{3/2}$$

The tunneling current therefore depends exponentially on the barrier height to the 3/2 power. However, the exponential dependence of tunnel current on the oxide-electric field causes some critical problems of process control because, for example, a very small variation of oxide thickness among the cells in a memory array produces a great

difference in programming or erasing currents, thus spreading the threshold voltage distribution in both logical states.

2.2.4 Direct Tunneling (DT)

It occurs below ≈ 5nm and with such a thin insulator or other phenomena such as quantum effects cannot be ignored. For nanocrystal memories, the control-gate coupling ratio of nanocrystal memory devices is inherently small [2-12]. As a result, F-N tunneling cannot serve as an efficient write/erase mechanism when a relatively thick tunnel oxide is used, because the strong electric field cannot be confined in one oxide layer. The direct tunneling is employed in nanocrystal memories instead. In the direct-tunneling regime, a thin oxide with thickness less than 3~5 nm is used to separate the nanocrystals from the channel. During write/erase operations, electrons / holes can pass through the oxide by direct tunneling, which gives the advantages of fast write/erase and low operation voltage. In the other hand, the direct tunneling is more sensitive to the barrier width than barrier height, two to four orders of magnitude reduction in leakage current can still be achieved if large work function metals, such as Au or Pt.

2.3 Basic Physics Characteristics of Nanocrystal Memory

2.3.1 Quantum Confinement Effect

The study of nanometer-size effects in direct gap semiconductor crystallites is an active field. In this size range, three-dimensional quantum confinement completely changes the optical and electronic properties of these nanocrystals compared to those of the bulk. The band gap increases with decreasing diameter, and the excited

electronic states become discrete with high oscillator strength and therefore it dependence on nanocrystal size has been studied both experimentally and theoretically with the tight-binding model. However, there is little experimental understanding of the basic nature of confinement for indirect gap materials such as silicon [2-13], despite strong theoretical interest. Silicon confinement contains new physics as well as possible technological importance. Confinement could enhance band gap luminescence [2-14 to 2-16], which is forbidden in bulk material, possibly enough to enable laser or display applications. However, a quantitative characterization of this enhancement in real nanocrystals has not been explored. Compared with bulk Ge, a 3nm Ge nanocrystal can have a conduction band shift of 0.5eV, which is significant enough to affect the electrical performance of the nanocrystal memory cell.

2.3.2 Coulomb Blockade Effect

Coulomb blockade was first observed in tunnel junctions containing a small metallic particle [2-17].The stored electron charge will raise the nanocrystal potential energy and reduce the electric field across the tunnel oxide, resulting in reduction of the tunneling current density during the write process. It is showed in Fig. 2-4.The Coulomb blockade effect can effectively inhibit the electron tunneling at low gate voltage and improve the flash memory array immunity to disturbance. However, the Coulomb blockade effect should be reduced by employing large nanocrystals if large tunneling current and fast programming speed is desired. The Coulomb blockade effect has a detrimental effect on the retention time, since the electrons in the nanocrystal have large tendency to tunnel back into the channel if the nanocrystal potential energy is high in retention mode. Another, the quantum confinement energy shifts the nanocrystal conduction band edge upward so that the conduction band offset

between the nanocrystal and the surrounding oxide is reduced.

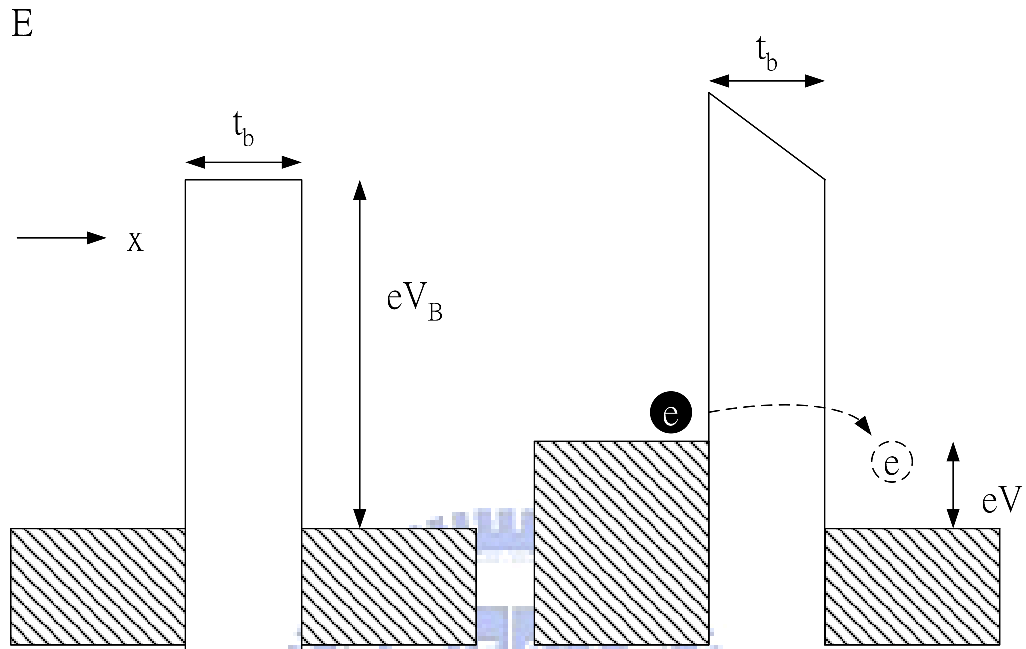


Figure 2-4 Coulomb blockade effect

Chapter 3
Experimental procedure

3.1 *Sample Preparation*

3.1.1 Method of Wafer pre-cleaning and fabricating tunnel oxide

P-type silicon wafers with <100> orientation were used for the fabrication of MIS capacitors. First, (100) oriented P-type 4 inch silicon wafers were chemically cleaned by standard Radio Corporation of America cleaning (RCA cleaning), followed by thermally growing of a about 5-nm-thick tunnel oxide at 1000°C by dry-oxidation horizontal furnace system(atmospheric pressure chemical vapor deposition, APCVD), and then the oxide measured by N&K 1200 was 41~55 Å.

3.1.2 Method and condition of fabricating Co-Si-Ge thin film

3.1.2.1 Sample study on formation of Cobalt-Silicide ($CoSi_2$) nanocrystals

a 10-nm-think Ge-doped Co-Si thin film was deposited by sputtering the Co and $Si_{0.5}Ge_{0.5}$ targets simultaneously. The pure Co target was sputtered by a DC power of 50W, the $Si_{0.5}Ge_{0.5}$ target sputtered by a DC power of 70W simultaneously. Then a 20-nm-thick SiO_2 film was deposited by plasma enhanced chemical vapor deposition (PECVD) system to form the capped oxide before rapid thermal oxidation (RTO) process. The above co-sputtered film deposited on the tunnel oxide at room temperature with 7.6mTorr pressure of the chamber. After RTO process at 650℃ for 30 sec in O_2 ambient, the cobalt-silicide NCs were nucleated in the dielectric layer and Si, Co and Ge on co-sputtered film were oxidized and formed one port of control oxide. Afterward annealing a 30nm SiO_2 film was deposited by plasma enhanced

chemical vapor deposition (PECVD) system to form the control oxide.

3.1.2.2 Sample study on Post-oxidation annealing procedures of Co-Si-Ge thin film

The following is a co-sputtered film of cobalt (Co) and silicon-germanium (SiGe) deposited onto the tunnel oxide by sputtering system. The pure Co target was sputtered by a DC power of 100W, the $Si_{0.5}Ge_{0.5}$ target sputtered by a RF power of 100W simultaneously during 30 seconds among the deposition. The above co-sputtered film deposited on the tunnel oxide at room temperature with 4.5mtorr pressure of the chamber. Some characters about cobalt list in Table 3-1.Next step, we annealed the sample with rapid thermal annealing (RTA) for 30s~90s in O_2 ambient that temperatures was about 550°C~750°C. During the annealing process Si、Co、Ge on co-sputtered film were oxidized and formed one port of control oxide. Also, cobalt elements had accumulated to form $CoSi_2$ nanocrystals which were embedded between silicon dioxide.

After annealing a 50nm SiO_2 film was deposited by plasma enhanced chemical vapor deposition (PECVD) system to form the control oxide.

Table 3-1 some character about metal cobalt

Cobalt general character	
Name, Symbol, Number	cobalt, Co, 27
Chemical series	transition metals
Group, Period, Block	9, 4, d
Density	8.90 g·cm^{-3}
Melting point	1768 K (1495 °C, 2723 °F)
Boiling point	3200 K (2927 °C, 5301 °F)
Heat of fusion	16.06 kJ·mol^{-1}
Heat of vaporization	377 kJ·mol^{-1}
Heat capacity	(25 °C) 24.81 J·mol^{-1}·K^{-1}
Work function	4.18eV

3.1.2.3 Sample study on the role of capped oxide

After growing of a about 5-nm-thick tunnel oxide we choose $CoSi_2$ as material to form the Co-Si-Ge thin film. See, for example, the flow path of growing tunnel oxide in preceding paragraph.

A about 10-nm-think Ge-doped Co-Si thin film was deposited by sputtering the $CoSi_2$ and $Si_{0.5}Ge_{0.5}$ targets simultaneously. The $CoSi_2$ target was sputtered by a DC power of 100W, the $Si_{0.5}Ge_{0.5}$ target sputtered by a RF power of 100W simultaneously during 30 seconds among the deposition. Then a 10-nm-thick SiO_2 film was deposited by plasma enhanced chemical vapor deposition (PECVD) system to form the capped oxide before rapid thermal oxidation (RTO) process. The above co-sputtered film deposited on the tunnel oxide at room temperature with 4.5mTorr pressure of the chamber. After RTO process at 750℃ for 30 sec~90 sec in O_2 ambient, the

cobalt-silicide NCs were nucleated in the dielectric layer and Si, Co and Ge on co-sputtered film were oxidized and formed one port of control oxide. Afterward annealing a 40nm SiO_2 film was deposited by plasma enhanced chemical vapor deposition (PECVD) system to form the control oxide.

3.1.3 Method and condition of fabricating Co-Si-Ge thin film

Finally the Al gate electrode on back and front side of the sample were finally deposited and patterned with thermal coater system to form a metal/oxide/silicon (MOS) structure with $CoSi_2$ nanocrystals. Fig. 3-1, Fig. 3-2, Fig. 3-3 was respectively showed the schematic diagrams of fabricating procedures for Co-Si-Ge thin film.

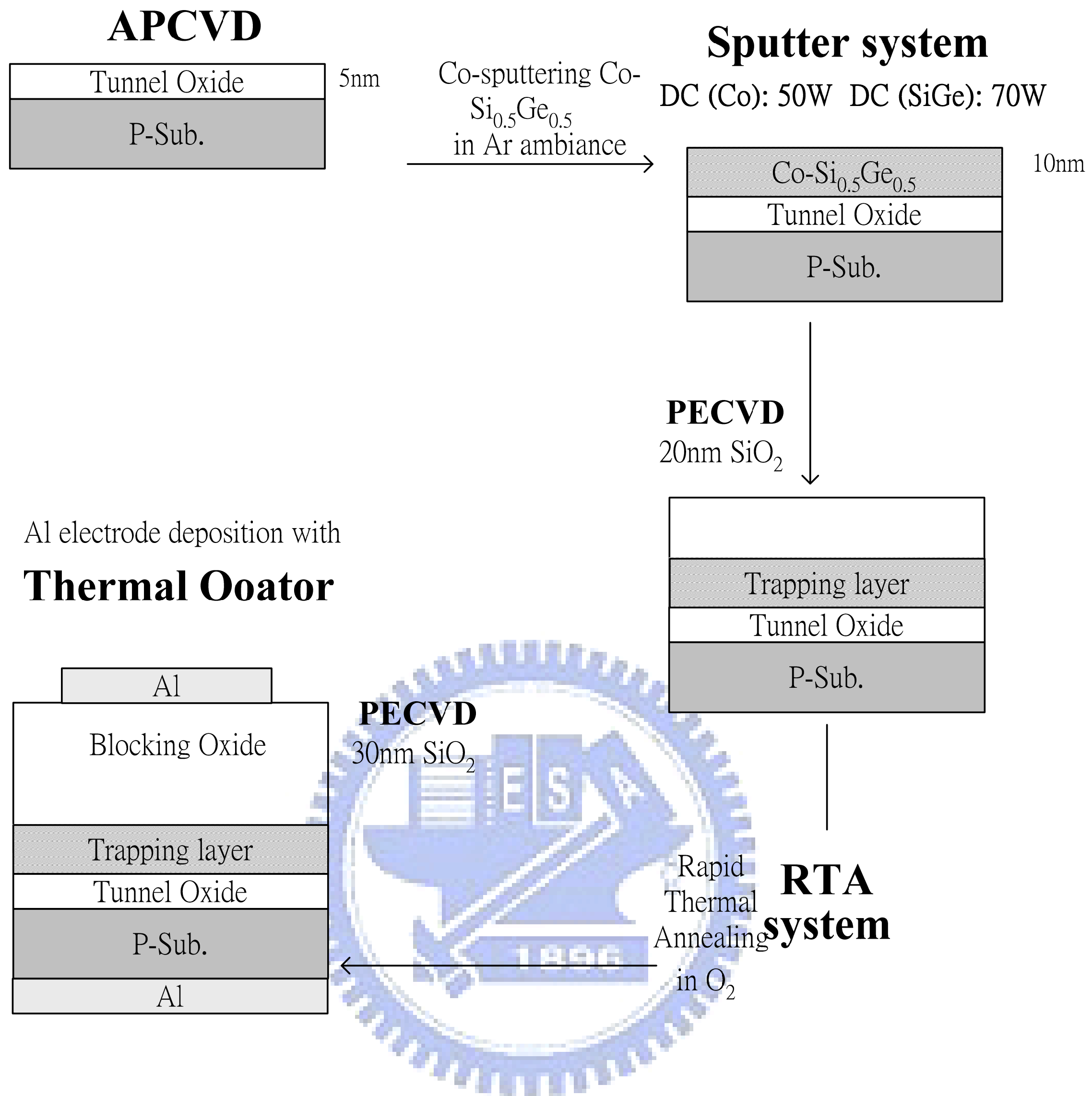


Figure 3-1 The schematic diagrams of fabricating procedures for the memory which is based on Co-incorporated $Si_{0.5}Ge_{0.5}$

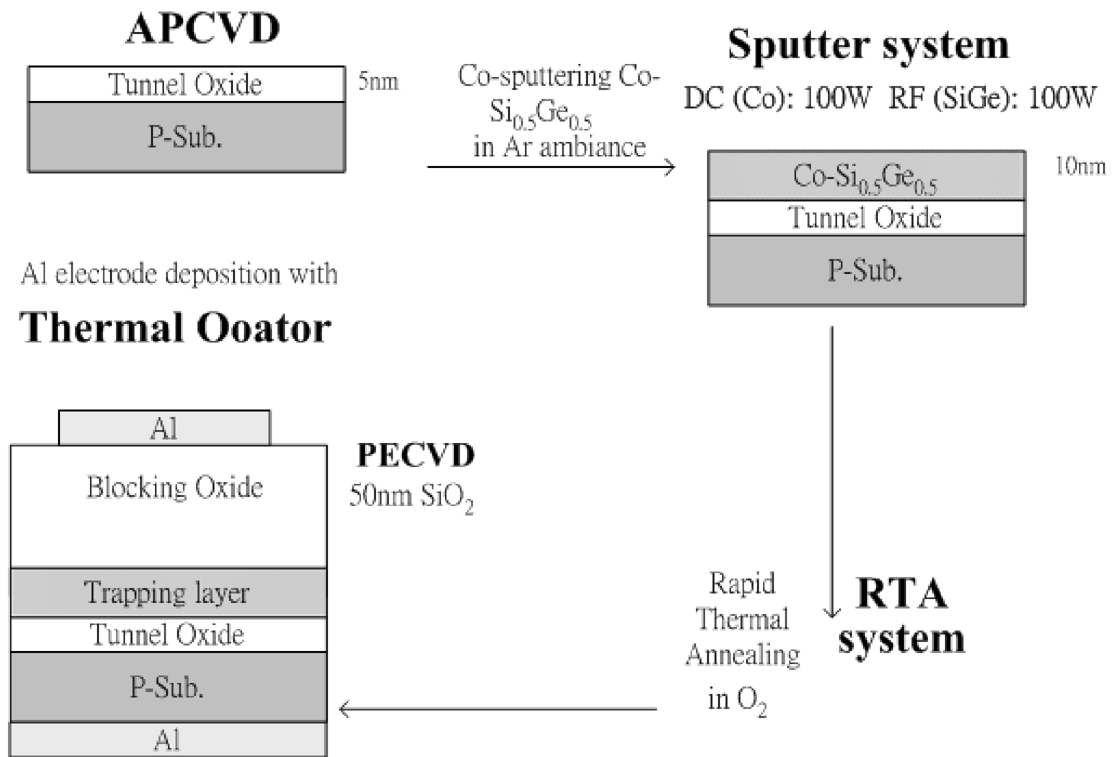
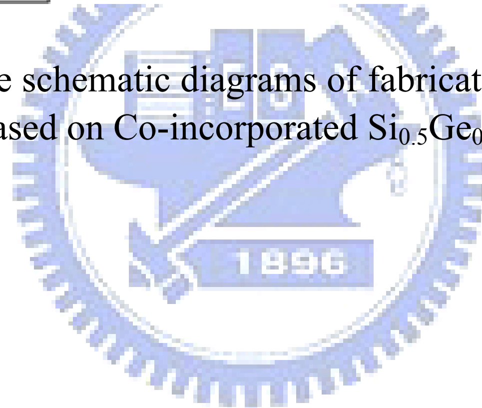
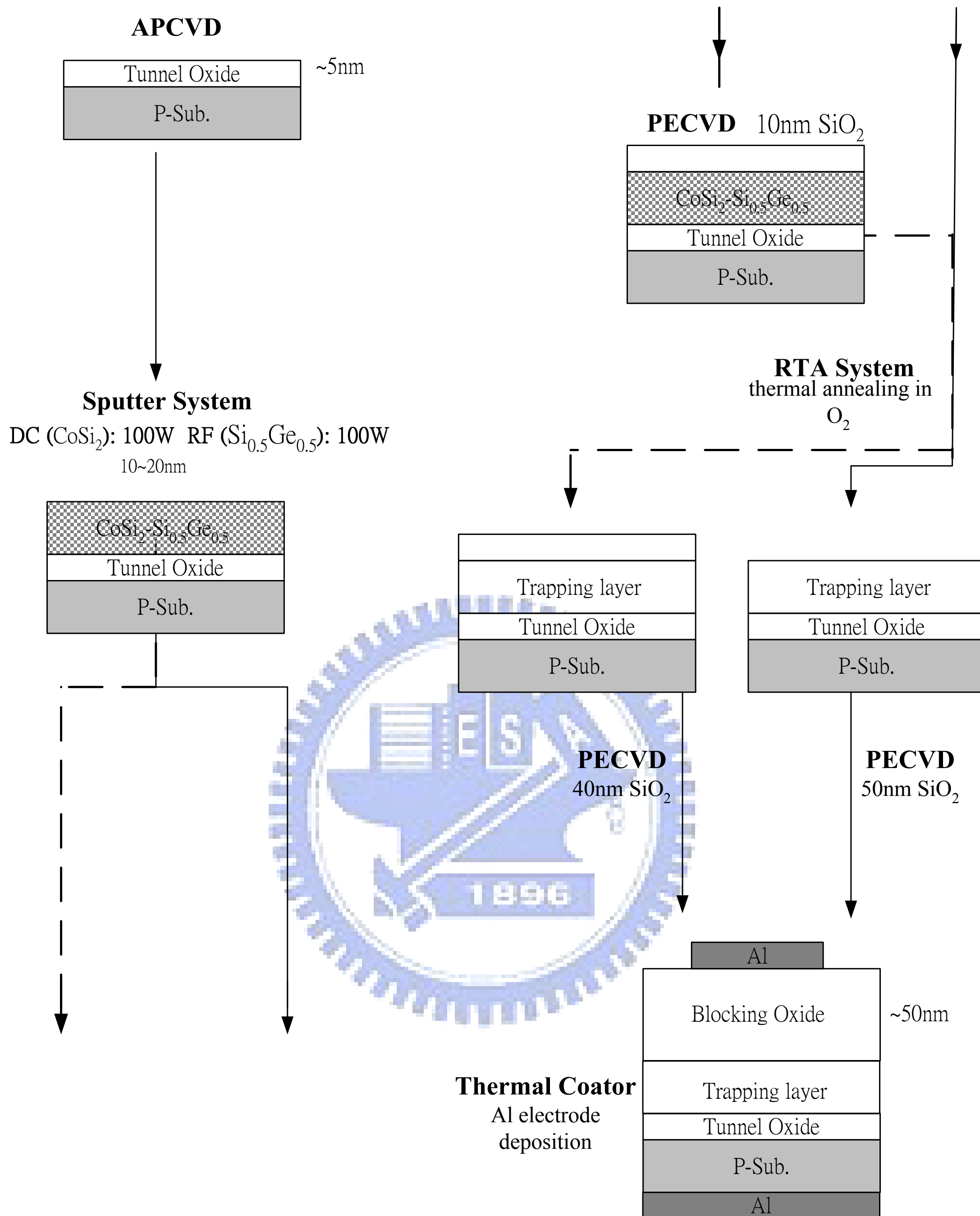


Figure 3-2 The schematic diagrams of fabricating procedures for the memory which is based on Co-incorporated $Si_{0.5}Ge_{0.5}$.





3-3 The schematic diagrams of fabricating procedures for the memory which is based on $CoSi_2$-incorporated $Si_{0.5}Ge_{0.5}$.

3.2 *Physical Characterization Techniques*

3.2.1 Focused Ion Beam (FIB)

FIB techniques are commonly used in high magnification microscopy. Many FIBs are largely used to prepare transmission electron microscope (TEM) cross-section sample lamellae because of inducing damage. (In NSYSU)

3.2.2 Transmission Electron Microscopy (TEM) and Energy dispersive X-ray spectroscopy (EDX)

The cross-sectional images were examined by TEM. We could clearly observe that nanocrystals or compounds exist in the trapping layer. We also understand what elements are in the trapping layer with EDX analysis. (In NTHU and NCU)

3.2.3 X-ray photoelectron spectroscopy (XPS)

X-ray photoemission spectroscopy (XPS) is a surface sensitive technique used to determine atomic compositions and learn information about the types of bonding that occurs within various compounds. We could get chemical information from XPS binding energy shifts. (In NCTU)

3.2.4 secondary ion mass spectrometry (SIMS)

Secondary Ion Mass Spectrometry (SIMS) is an analytical technique used to analyze the composition of solid surfaces and thin films by sputtering the surface of the specimen with a focused primary ion beam and collecting and analyzing ejected secondary ions. Secondary ions formed during the sputtering are extracted and analyzed using a mass spectrometer. It can provide elemental depth profiles over a depth range from a few angstroms to tens of microns.

3.3 Physical Characterization Techniques

Electrical characteristics, including the capacitance-voltage (C-V) hysteresis, current density-voltage (J-V), retention and endurance characteristic were also performed. We measured the electrical characteristics with Keithley 4200 and HP4284 Precision LCR Meter at 1 MHz.

Chapter 4
Results and Discussion

A three-phase study was designed to explore the formation of cobalt-silicide, the role of capped oxide before RTA and the procedure of oxidation mechanism. It this investigation about co-sputtered film we also carried out three different experiment discussion.

4.1 Study on formation of cobalt-silicide ($CoSi_2$) nanocrystals for the application on nonvolatile memory

Fig. 4-1 shows the forward and reverse capacitance-voltage (*C-V*) hysteresis for as-deposited samples obtained when the gate voltage was first swept from –10V to +10V (accumulation to inversion, forward sweep) and then from +10V to –10V (inversion to accumulation, reverse sweep) for the MIS structure which is based on co-sputtered Co- $Si_{0.5}Ge_{0.5}$ thin films. In Fig. 4-1, it is found that the memory window of about 5.64V is observed under ± 10 V gate voltage operation. We also measured 15V with the same process and could found that a more pronounced C-V shift is observed. The C-V hysteresis after bidirectional sweeps implies the electron charging and dish. As the swept voltage is increased to ± 15 V, a more pronounced C-V shift is observed. The charge storage ability of Ge-doped cobalt-silicon memory devices is attributed to the presence of cobalt-silicide NCs and the oxidized Ge elements, which provide extra charge trap sites.

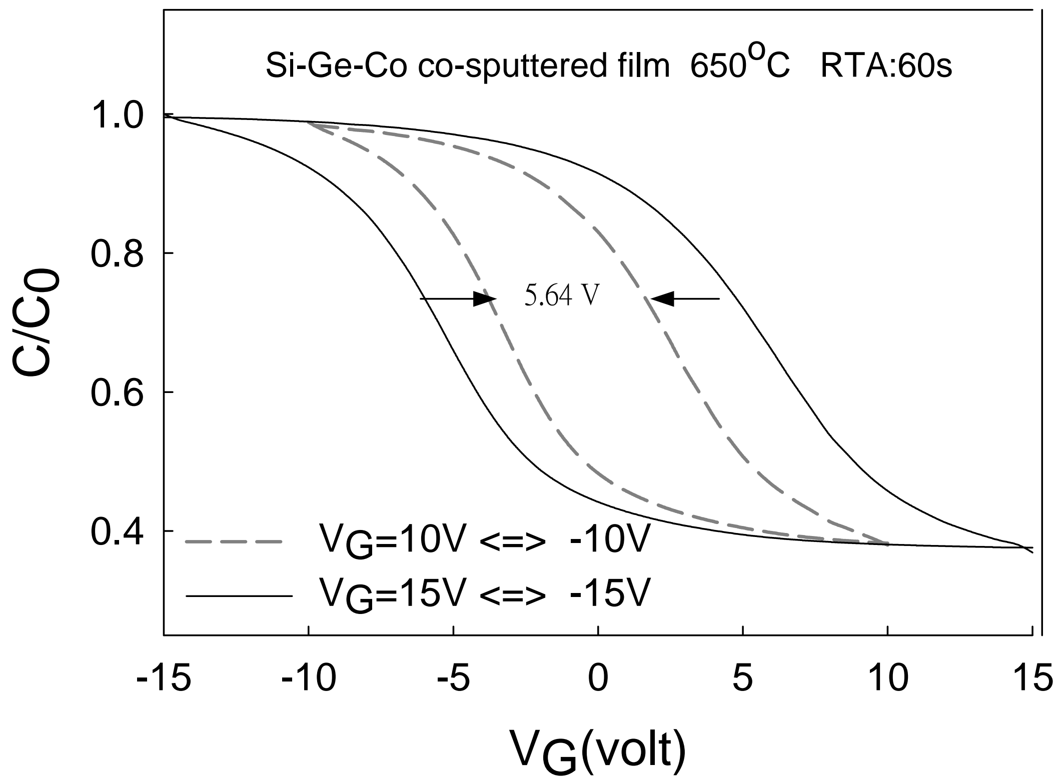


Figure 4-1 The *C-V* characteristics of the Co- Si-Ge co-sputtered film with capped oxide before annealing.

Moreover, the leakage current in the MOIOS structure is shown in Fig. 4-2. The lower leakage current could avoid the stored charge leaking into gate through the blocking oxide to get better retention time for the MOIOS structure. According to the reported paper, the asymmetry of J-V characteristics in the figure is because when the applied voltage is swept from 0 to +10V, some negative charges are trapped in the defects of the dielectric layer, leading to an increase of the injection barrier height and, therefore, to a decrease of the oxide conductivity. The leakage currents exhibit a nearly result about from 10^{-11} order to 10^{-12} order.

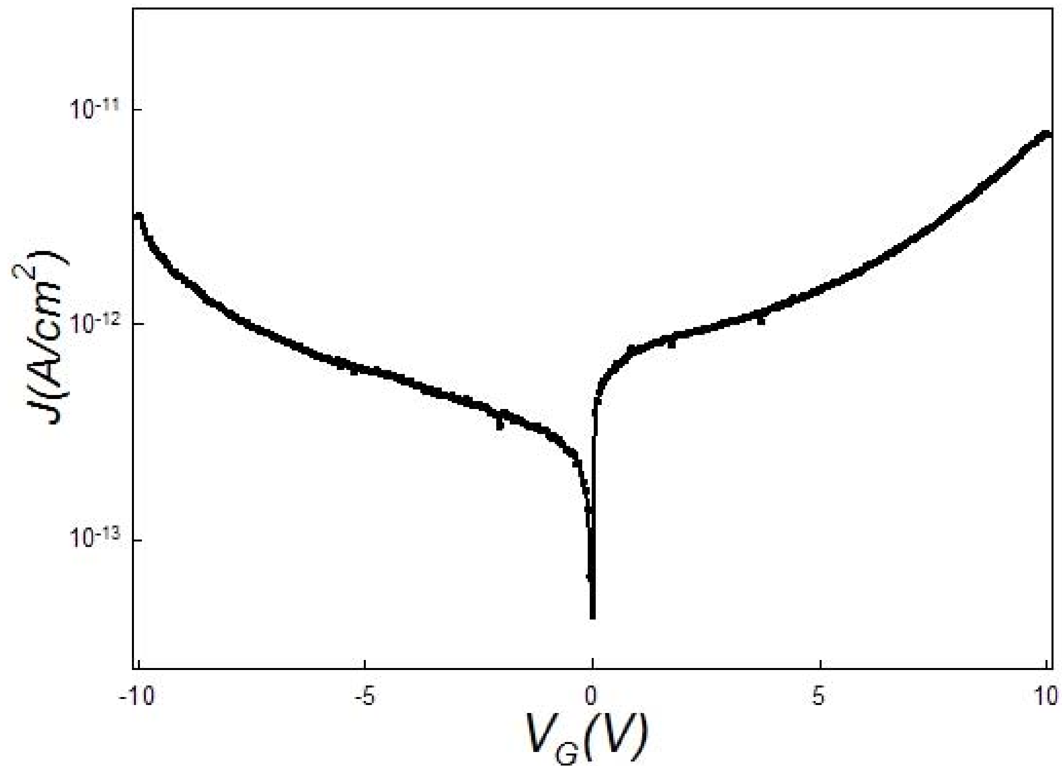


Figure 4-2 The *J-V* characteristics of the Co- Si-Ge co-sputtered film with capped oxide before annealing.

Fig. 4-3 shows (a) the cross-sectional and (b) the plane-view TEM image of the fabricated device sample. It can be found that the average diameter of cobalt-silicide NCs is around 8~10 nm from the cross-sectional TEM image and the area density of NCs is estimated to be about 1.03 $\times10^{11}$ cm^{-2} from the plane-view TEM image. According some papers, the Ge elements tend to segregate at interface during the formation of the NCs [4-1]. With the segregation of Ge elements, the component of NCs is nearly cobalt silicide. Moreover, according to the thermodynamic analysis, We have known that the Si and Ge elements are prior to be oxidized in the mixed film [4-2]. Therefore, the cobalt-silicide NCs nucleate in the thin dielectric film mixed with silicon oxide and oxidized Ge elements.

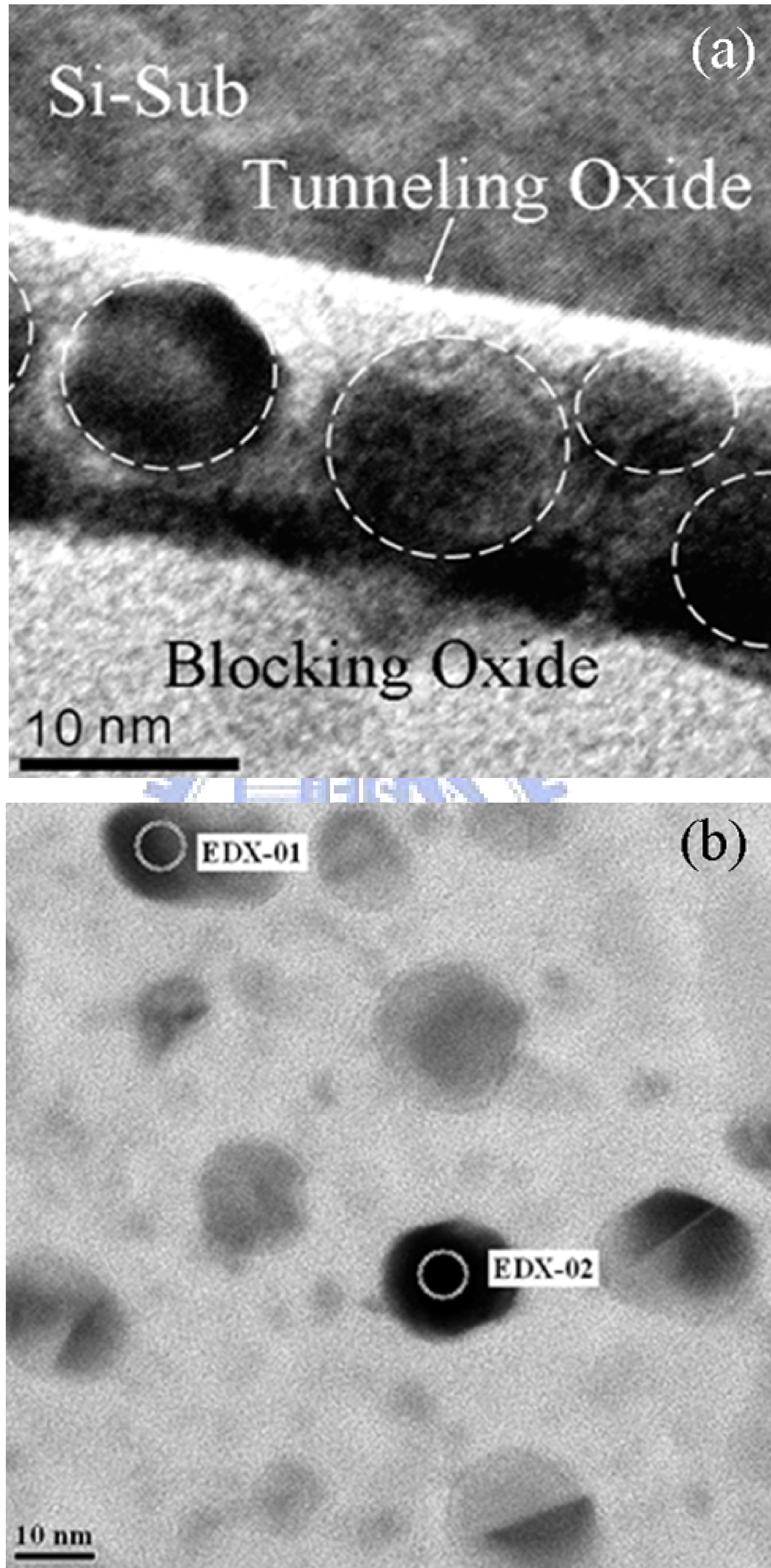


Figure 4-3 (a) the cross-sectional and (b) the plane-view TEM image of the fabricated device sample.

EDX Analysis stands for Energy Dispersive X-ray analysis Energy. Fig. 4-4 shows the EDX images of the fabricated device sample after RTO process. We could know that there are many kinds of element in the trapping layer such as cobalt, silicon, germanium and oxygen in the dot from Fig. 4-4 (a) and Fig. 4-4 (b). However, in Fig. 4-4 (c), we could know that a small amount of various elements was in the trapping layer wherever there are not dots in it.

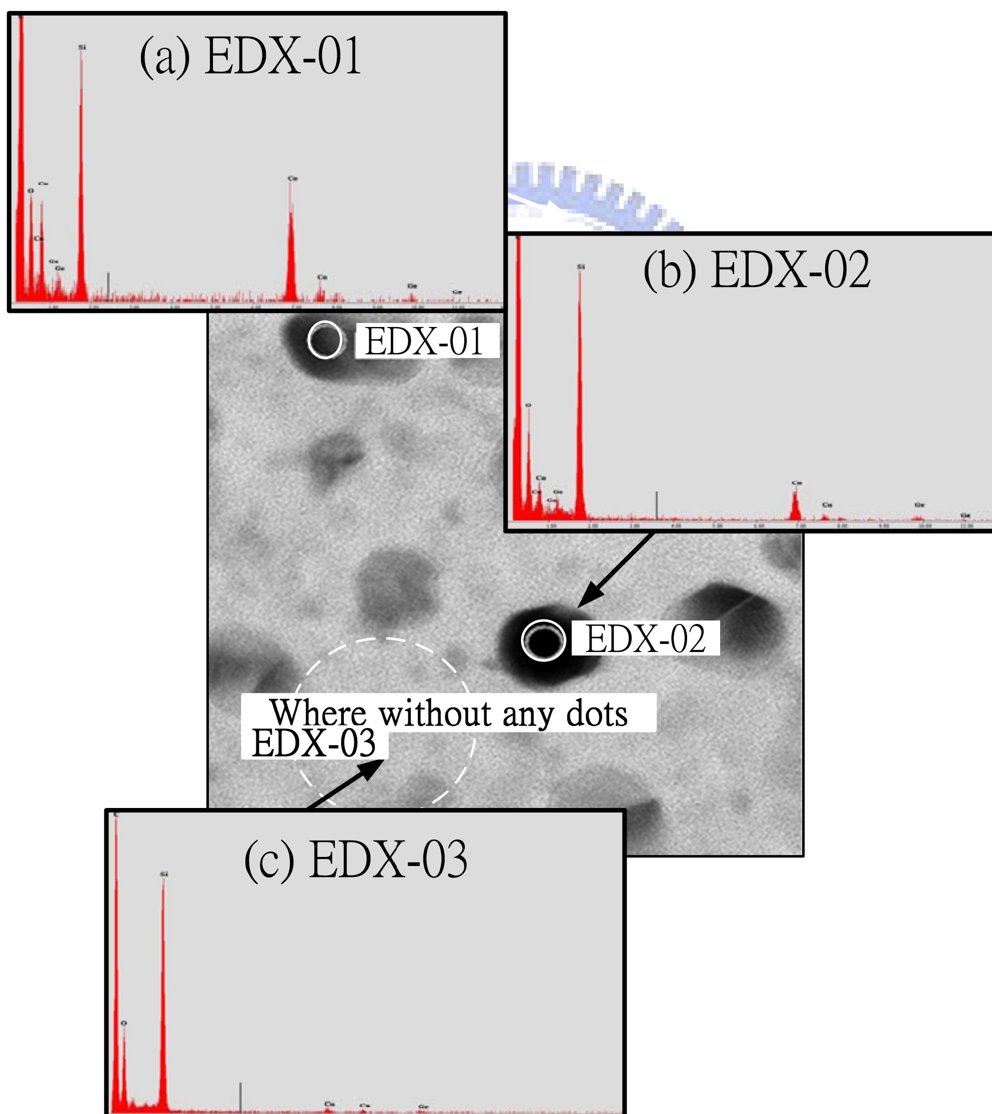
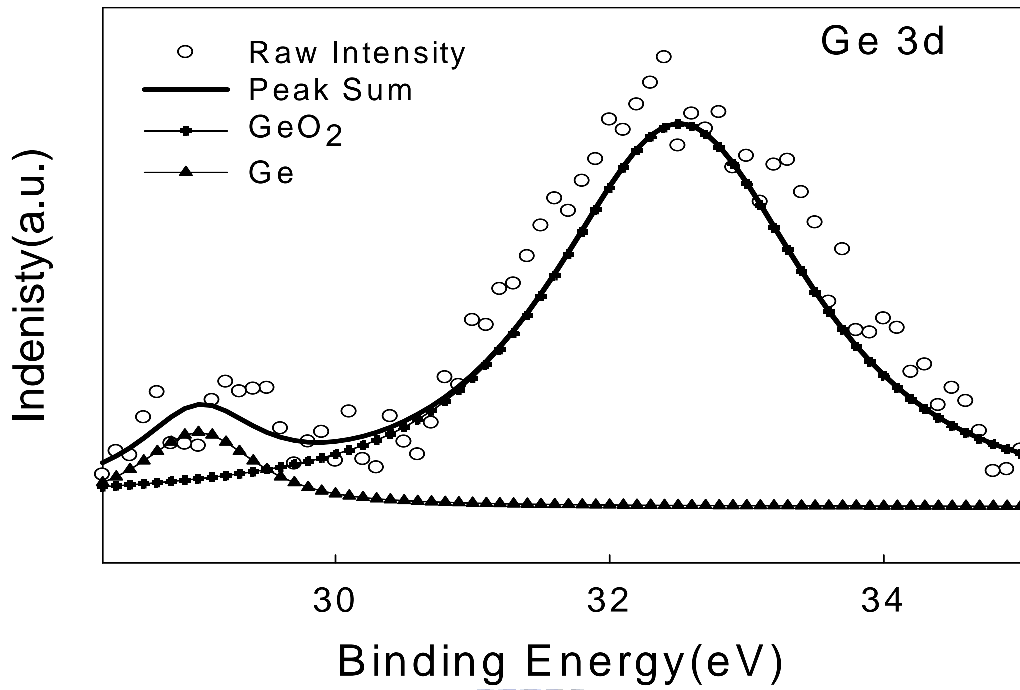
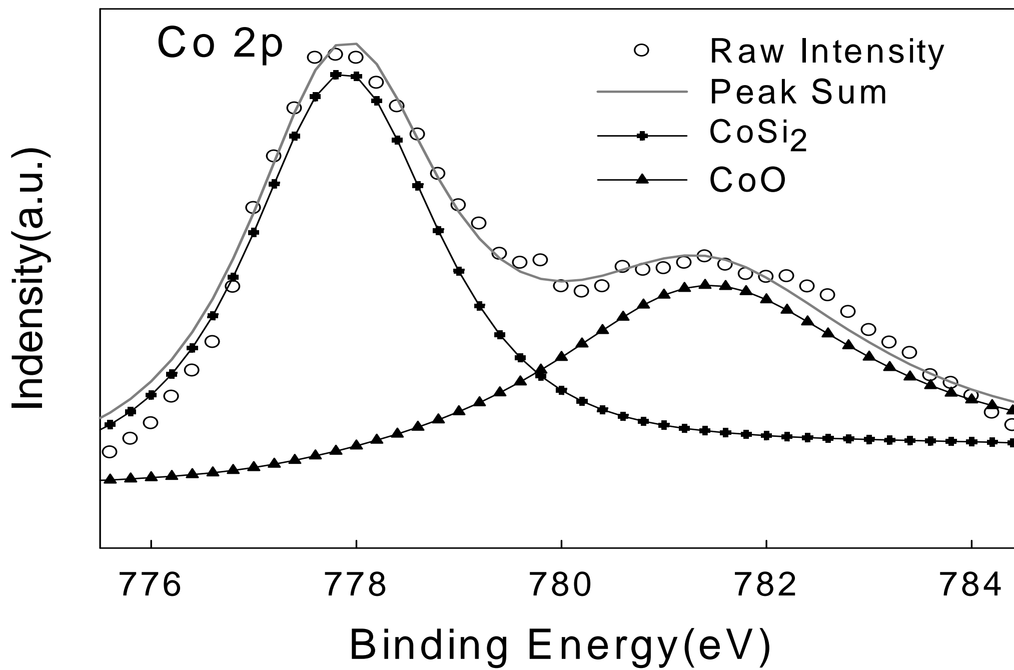


Figure 4-4 The EDX images of the fabricated device sample after RTO process.

Fig. 4-5 shows the XPS spectrum of Ge 3d and Co 2p3/2 in the Co-$Si_{0.5}Ge_{0.5}$ co-sputtered film after thermal oxidation process. The Ge 3d XPS spectrum is displayed in Fig. 4-5 (a). We found that the peak output occurs between 29 eV and 35 eV and there and this spectrum clearly indicates the peak at ~32.5 eV[16]. it can be found that the Co 2p XPS spectrum shows two peaks corresponding to cobalt silicide and cobalt oxide at ~778.5 eV and ~782 eV, respectively [4-3]. The result indicates that cobalt-silicide NCs are formed and partly cobalt elements are oxidized to cobalt oxide during thermal oxidation process. It is believed that the thermal oxidation process causes the formation of cobalt-silicide NCs and the oxidation of Ge elements.



(a)



(b)

Figure 4-5 The XPS spectrum of (a) Ge 3d and (b) Co 2p3/2 in the Co-$Si_{0.5}Ge_{0.5}$ co-sputtered film after thermal oxidation process.

4.2 Post-oxidation annealing procedures of Co-Si-Ge thin film as trapping layers in oxygen ambient by annealing system

4.2.1 Results

4.2.1.1 Electrical characteristics

Fig. 4-6 show the forward and reverse capacitance-voltage (*C-V*) hysteresis for as-deposited samples obtained when the gate voltage was first swept from –7V to +7V (accumulation to inversion, forward sweep) and then from +7V to –7V (inversion to accumulation, reverse sweep) for MIS structure which is based on co-sputtered Co- $Si_{0.5}Ge_{0.5}$ thin films. We also measured 9V with the same process and could found that a more pronounced C-V shift is observed. The C-V hysteresis after bidirectional sweeps implies the electron charging and dish.

We could observe that threshold-voltage shifts were reduced and memory window was also smaller as the memory was annealed during longer time or higher temperature in Fig. 4-6. For a fine example of this phenomenon, the threshold-voltage shifts of the memory which was annealed at 550°C were smaller when annealed time with Rapid Thermal Processing (RTP) system was longer. It is considered that there were less cobalt elements or $CoSi_2$ to form nanocrystals and partial cobalt elements form another chemical compound. The cobalt reacts with oxygen to make rust during annealing in O_2.ambiance. Here is an example of chemical reactions with the corresponding chemical equation. Cobalt oxide had large internal resistance [4-4] and therefore cobalt oxide had not been a good conductor. There is considerable validity in our ratiocination: some cobalt elements formed another chemical compound such as CoO during annealing in O_2 ambiance.

The C-V hysteresis of
Co-SiGe co-sputtered film 550°C RTA:60s
3.3 eV
C/C0
Vg(volt)

The C-V hysteresis of
Co-SiGe co-sputtered film 550°C RTA:90s
3.1 eV
C/C0
Vg(volt)

The C-V hysteresis of
Co-SiGe co-sputtered film 650°C RTA:60s
1.3 eV
C/C0
Vg(volt)

The C-V hysteresis of
Co-SiGe co-sputtered film 650°C RTA:90s
1.1 eV
C/C0
Vg(volt)

The C-V hysteresis of
Co-SiGe co-sputtered film 650°C RTA:30s
0.24 eV
C/C0
Vg(volt)

The C-V hysteresis of
Co-SiGe co-sputtered film 750°C RTA:60s
0.12 eV
C/C0
Vg(volt)

Thermal annealing with RTA during longer time

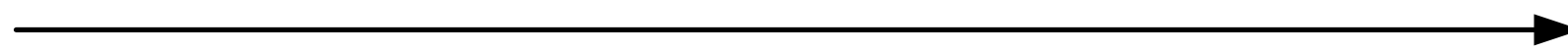


Figure 4-6 C-V hysteresis of the fabricated device sample after RTO process.

4.2.1.2 Material analysis

Fig. 4-7 shows the cross-sectional TEM and the C-V hysteresis of the fabricated device sample after RTO process. We can clearly find out the variation in chemical and physical composition of trapping layer. Co-sputtered film became two separate ports in trapping layer. One of them is a continuous film that is not formed with conductor and becomes one port of control oxide. Another one is clearly observed that many nanocrystals formed under continuous film and on tunnel oxide after thermal treatment.

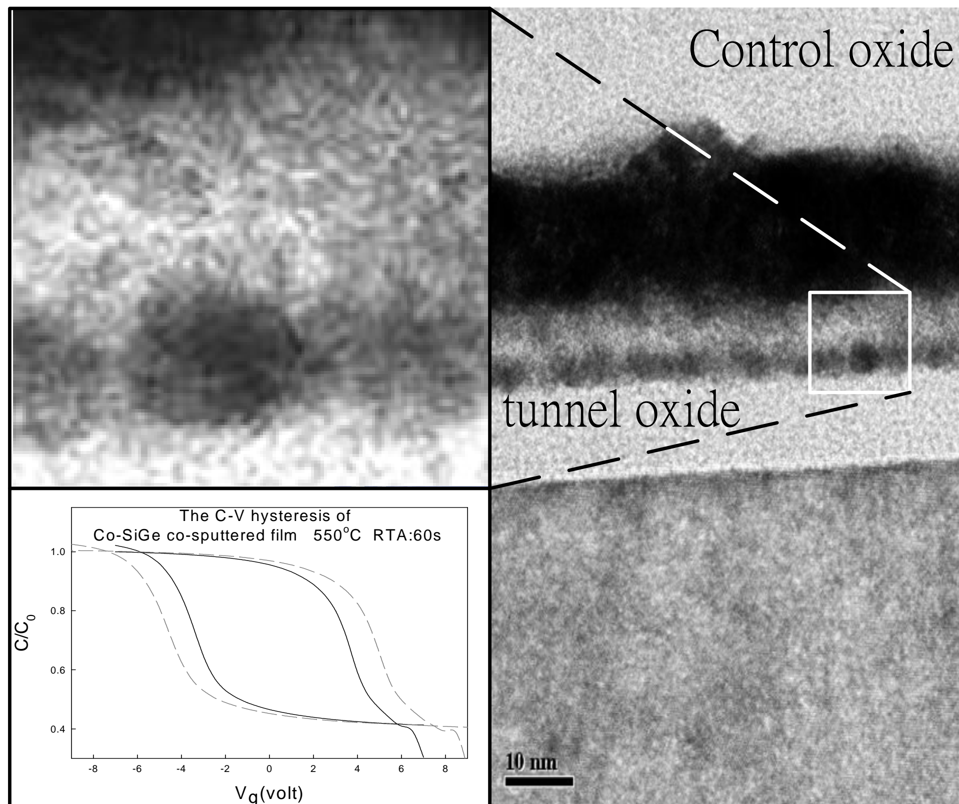
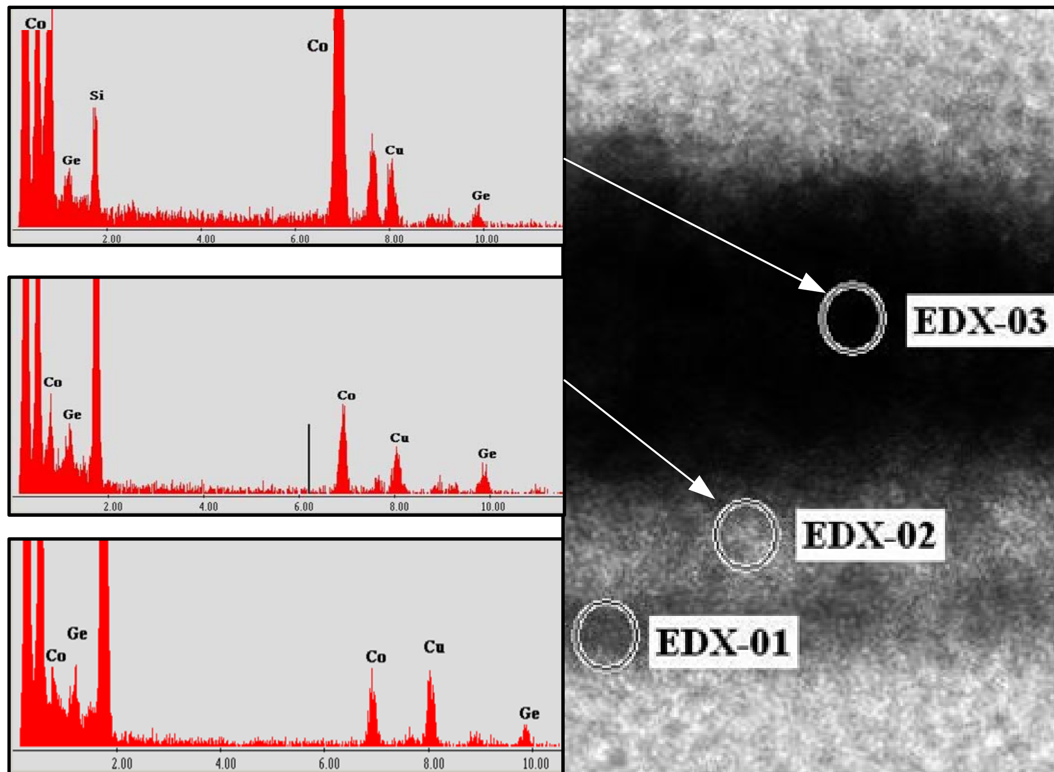


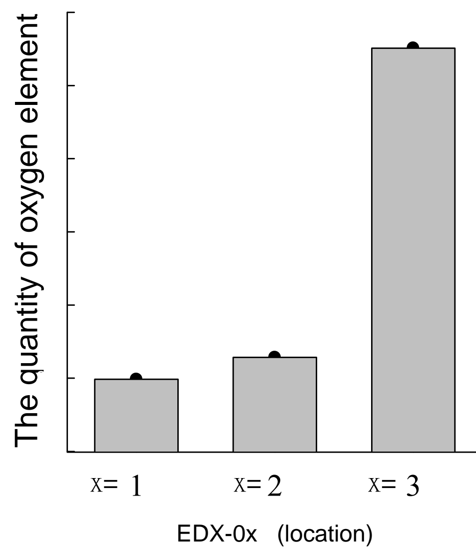
Figure 4-7 The cross-sectional TEM and the C-V hysteresis of the fabricated device sample after lower temperature RTO process.

EDX Analysis stands for Energy Dispersive X-ray analysis Energy. Fig. 4-8 (a)

shows the EDX images of the fabricated device sample after RTO process. It is sometimes referred to also as EDS or EDAX analysis. It is a technique used for identifying the elemental composition of the specimen. We could know that there are many kinds of element in the trapping layer such as cobalt, silicon, germanium and oxygen in the Fig. 4-8 (a). In the Fig. 4-8 (b), we made quantitative analysis and could understand that oxygen elements on the point, EDX-03, have plenty of oxygen elements on the point, EDX-01, and, EDX-02.



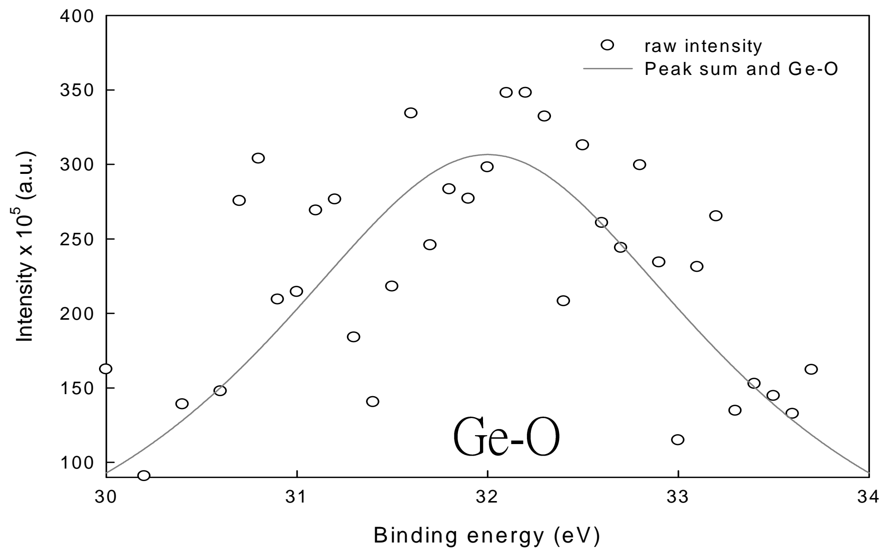
(a)



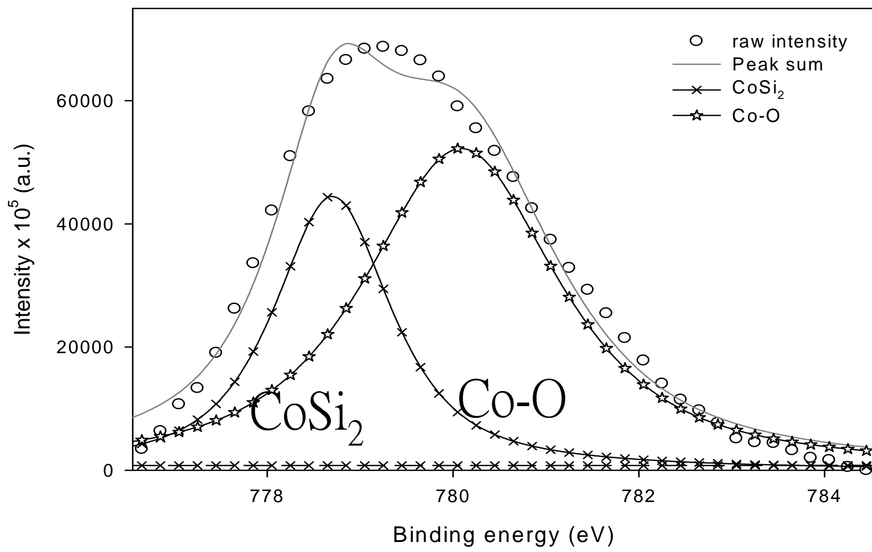
(b)

Figure 4-8 (a) Cross-sectional TEM and EDX (Energy Dispersive X-ray analysis) of the fabricated device sample after RTO process. (b) The quantitative analysis and could understand that oxygen elements on the point

Fig. 4-9 shows the XPS spectrum of Ge 3d and Co 2p3/2 in the co-sputtered Co-$Si_{0.5}Ge_{0.5}$ thin films after thermal oxidation process. The Ge 3d XPS spectrum is displayed in Fig. 4-9 (a). We found that the peak output occurs between 30 eV and 34 eV. It is believed that the executed oxidation process causes the oxidation of Ge element. In Fig. 4-9 (b), the Co 2p3/2 XPS spectrum shows two peaks corresponding to $CoSi_2$ and cobalt oxide at about ~778.6eV and ~780.5eV respectively. The result indicated that $CoSi_2$ NCs are formed and partly cobalt elements are oxidized to cobalt oxide during thermal oxidation process.



(a)



(b)

Figure 4-9 The XPS spectrum of (a) Ge 3d and (b) Co 2p3/2 in the Co-$Si_{0.5}Ge_{0.5}$ co-sputtered film after thermal oxidation process.

Fig. 4-10 shows the cross-sectional TEM and the C-V hysteresis of the fabricated device sample after RTO process. We can clearly find out the variation in chemical and physical composition of trapping layer. Co-sputtered film became two separate

ports in trapping layer. One of them is a continuous film which is not formed with conductor and another one of them is clearly observed that there no nanocrystals under continuous film by thermal treatment. In the Fig. 4-11, we also could know that there are many kinds of element in the trapping layer such as cobalt, silicon, germanium and oxygen with EDX analysis.

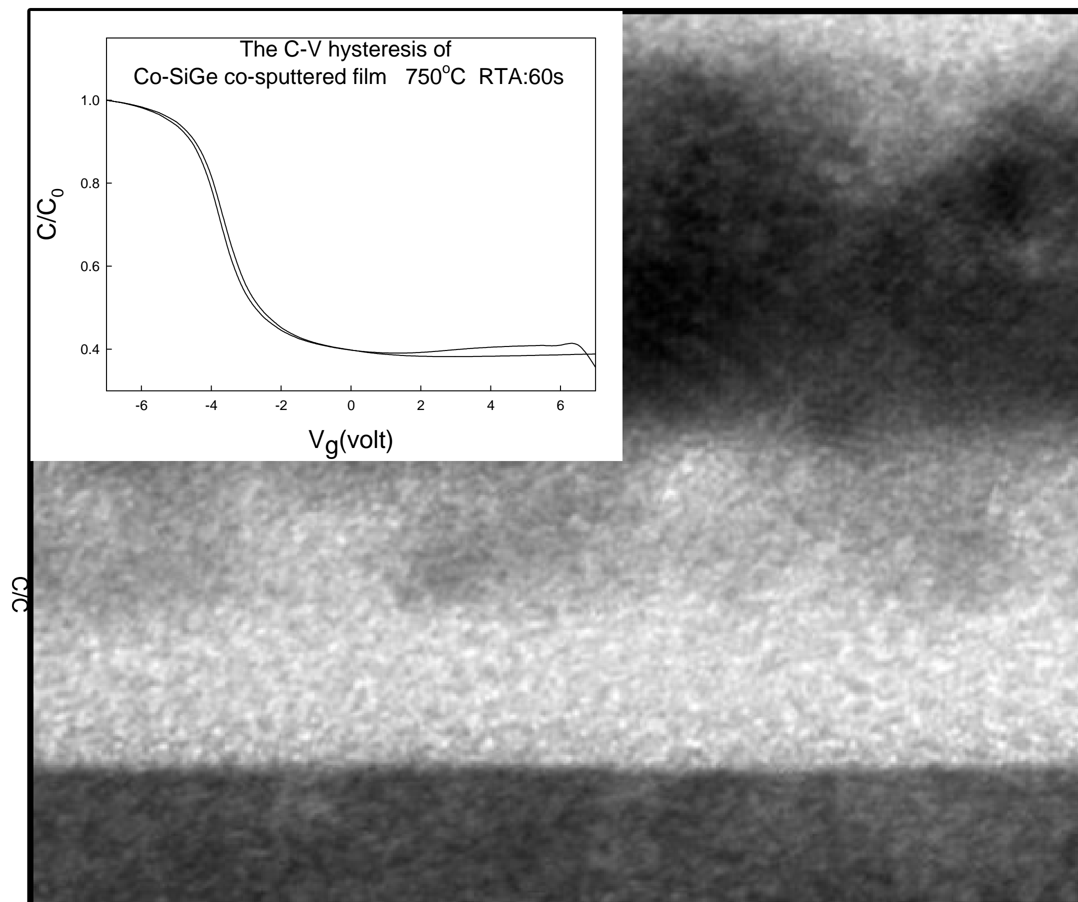


Figure 4-10 The cross-sectional TEM and the C-V hysteresis of the fabricated device sample after higher temperature RTO process.

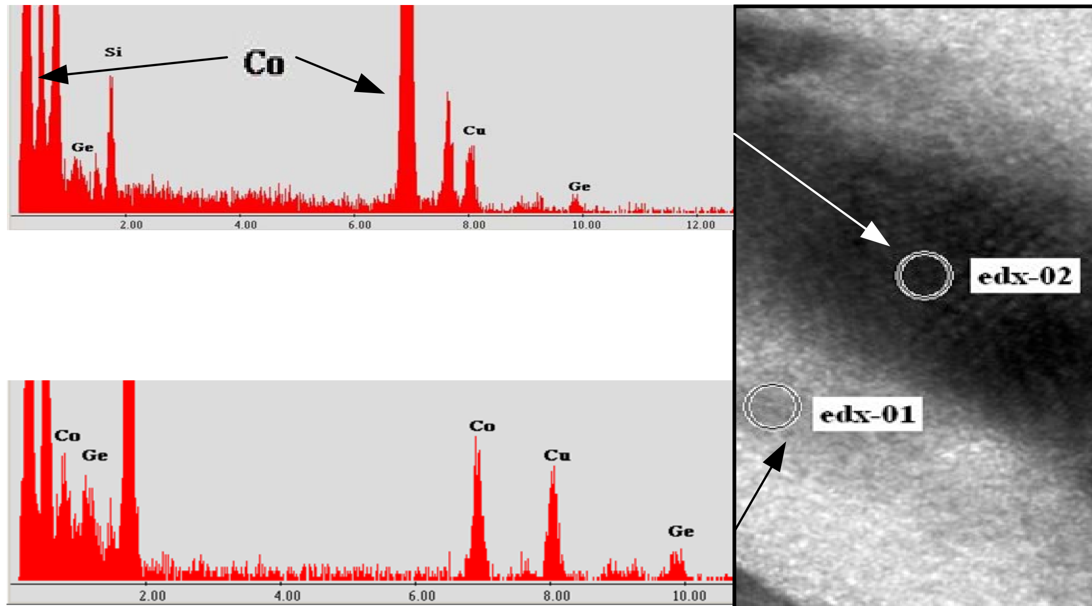
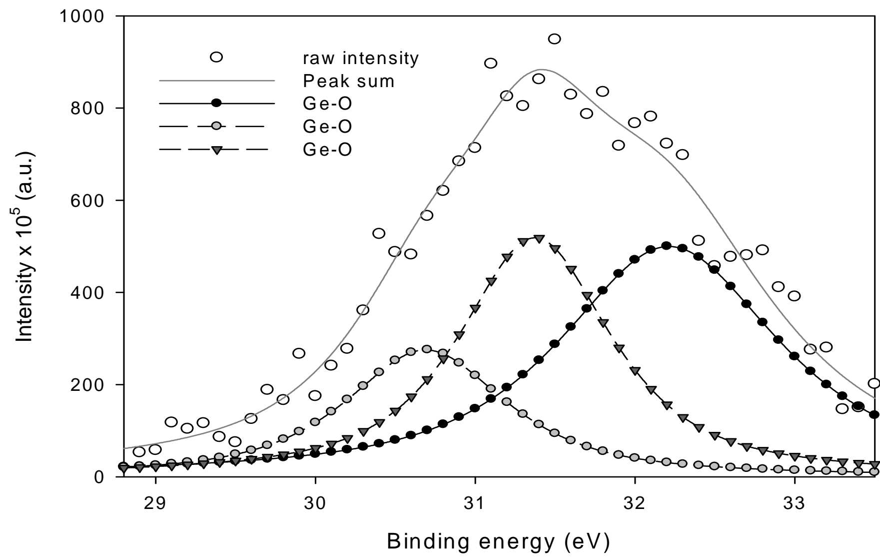
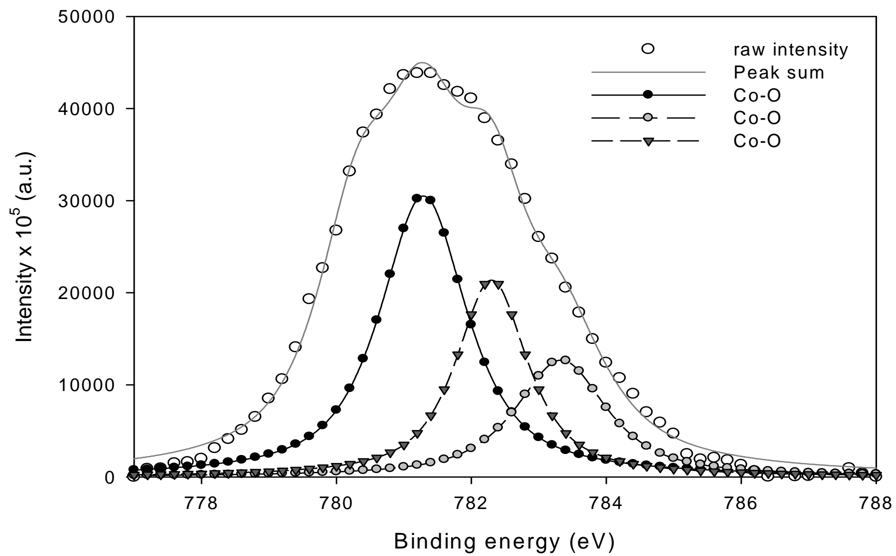


Figure 4-11 Cross-sectional TEM and EDX (Energy Dispersive X-ray analysis) of the fabricated device sample after RTO process.

Fig. 4-12 shows the XPS spectrum of Ge 3d and Co 2p3/2 in the Co- $Si_{0.5}Ge_{0.5}$ co-sputtered film after thermal oxidation process. The Ge 3d XPS spectrum is displayed in Fig. 4-12 (a). We found that this peak output occurs between 30 eV and 34 eV. It is believed that the executed oxidation process causes the oxidation of Ge element. In Fig. 4-12 (b), the Co 2p3/2 XPS spectrum shows three peaks corresponding to cobalt oxide at about 778eV and upward. This result indicated that the bulk of cobalt elements are oxidized to cobalt oxide during thermal oxidation process.



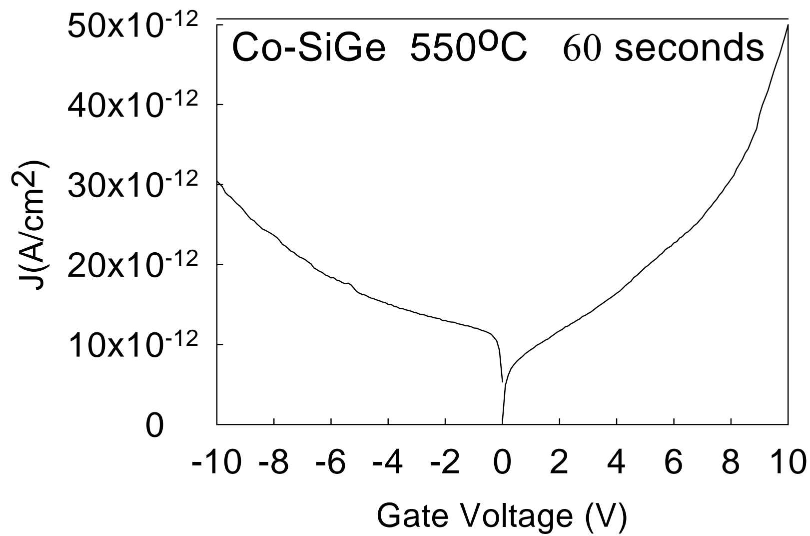
(a)



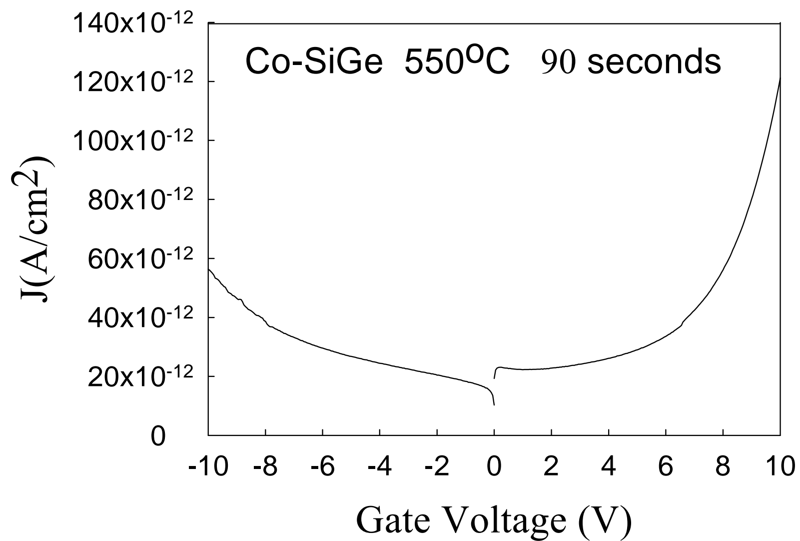
(b)

Figure 4-12 The XPS spectrum of (a) Ge 3d and (b) Co 2p3/2 in the Co-$Si_{0.5}Ge_{0.5}$ co-sputtered film after thermal oxidation process in higher temperature.

In addition, the electrical current density-voltage (*J*-*V*) hysteresis of three conditions in oxidation duration of the Co-$Si_{0.5}Ge_{0.5}$ is shown in Fig. 4-13. With the extension of oxidation duration at different temperature from 60 seconds to 90 seconds, the leakage current exhibited a nearly result about from 10^{-12} order to 10^{-10} order. It is torrent for carrier stored in charge trapping layer.



(a)



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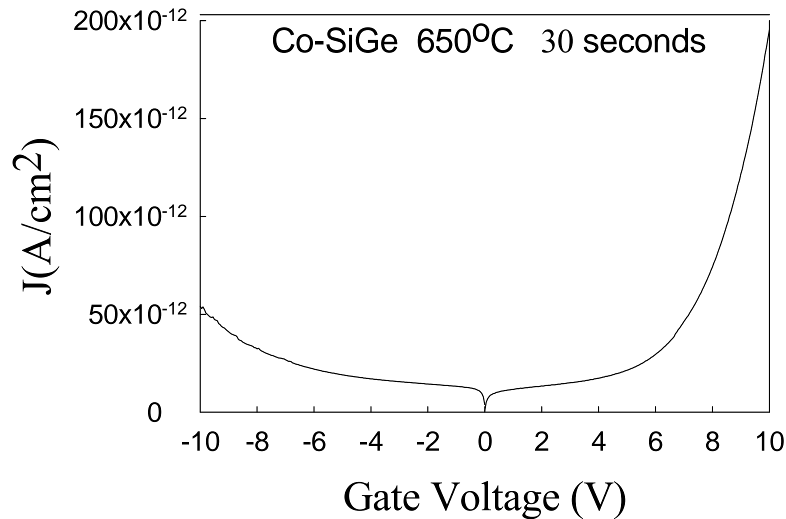


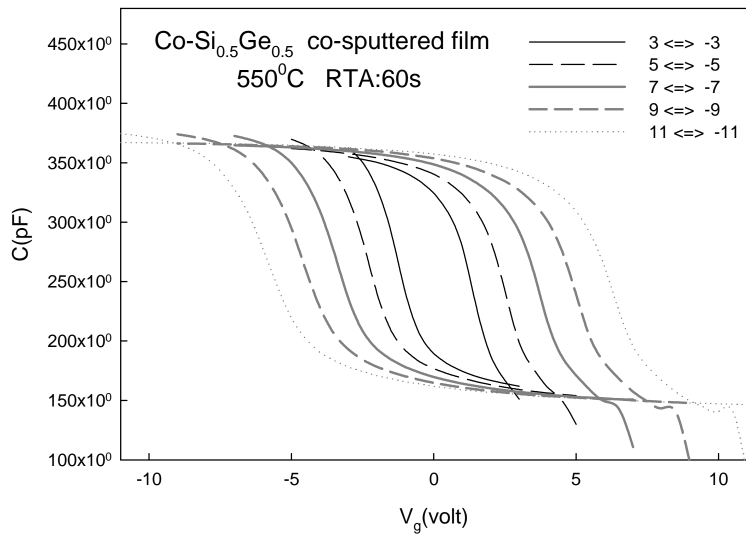
(c)

Figure 4-13 The *J-V* characteristics of the capacitor based on the Co- $Si_{0.5}Ge_{0.5}$ co-sputtered film with oxidation in different condition.

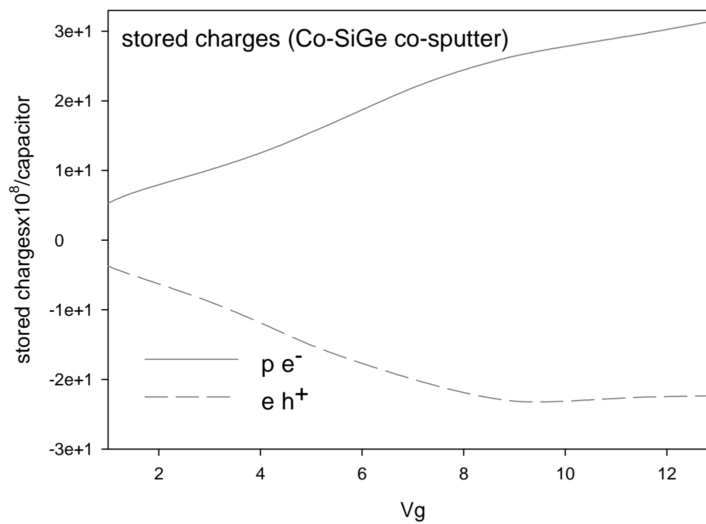
4.2.2 The discussion

4.2.2.1 Discussion on electrical characteristics

It is found that the memory window of 6.2V is observed under ±7 gate voltage operation and about 13.2V is observed under ±11 gate voltage operation in Fig. 4-14 (a). As the swept voltage is increased to ±7 and ±11, a more pronounced C-V shift is observed. The memory effect was observed from the hysteresis capacitance-voltage (*C-V*) characteristics of MIS capacitors embedded with the charge storage layer. According to the theoretical derivation [4-5], i.e. $Q= -V_{fb}C_{control}$, the total charges trapped in the capacitor can be approximately estimated and the model is schematized in Fig. 4-14 (b). We could know that the quantity of trapped charge is tied closely with gate voltage and it is pertinent to tunneling probability.



(a)

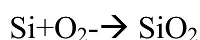


(b)

Figure 4-14 (a) he C-V hysteresis of the fabricated device sample and (b) the quantity of trapped charge after RTO process.

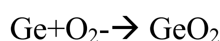
4.2.2.2 Reaction free energy

In pure O_2, oxidation of silicon, germanium and cobalt, forming SiO_2, GeO_2 and CoO occurs following the reaction [4-6]:



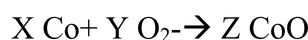
$$Si + O_2 \rightarrow SiO_2$$

With a free energy change of $\triangle G_1$=-732.94 kJ/mol



$$Ge + O_2 \rightarrow GeO_2$$

With a free energy change of $\triangle G_2$=--377.54 kJ/mol, whereas for

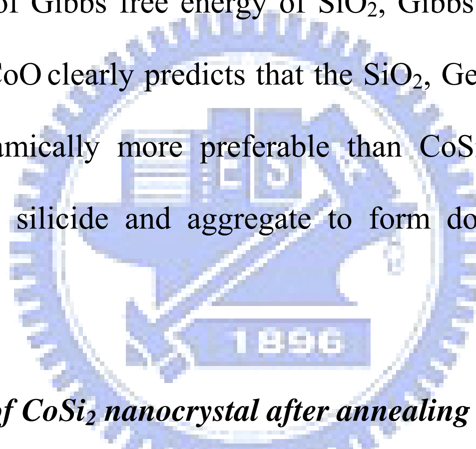


$$X\ Co + Y\ O_2 \rightarrow Z\ CoO$$

With a free energy change of $\triangle G_3$=--142.15 kJ/mol

The amount of Gibbs free energy reduction in forming the silicide phases from Co and Si elements are known at 727°C, but those are known: it is *-88.9* KJ/mole for CoSi and -95.1 KJ/mole for $CoSi_2$, with a difference of only -7%. [4-7]

The lower value of Gibbs free energy of SiO_2, Gibbs free energy of GeO_2 and Gibbs free energy of CoO clearly predicts that the SiO_2, GeO_2 and CoO reaction with oxygen is thermodynamically more preferable than $CoSi_2$.Cobalt will react with silicon to form cobalt silicide and aggregate to form dots in the region without unwanted oxygen.



4.2.2.3 Formation of $CoSi_2$ nanocrystal after annealing

From TEM image was showed in the Fig. 4-7 and that show the cross-sectional TEM and the C-V hysteresis of the fabricated device sample after RTO process. Co-sputtered film became two separate ports in trapping layer and the C-V hysteresis which there is large memory window indicates that trapping effect occurs. At high temperature condition and in the controlled-atmosphere chamber filled with oxygen at atmospheric pressure, silicon, germanium and cobalt will easily react with oxygen to form oxide. We also know that aggregation generally occurs at higher temperatures [4-8]. Fig. 4-10 also shows the cross-sectional TEM and the C-V hysteresis of the fabricated device sample after RTO process. The difference in temperature between Fig. 4-7 and Fig. 4-10 there is two hundred degrees. The TEM image in Fig. 4-7

shows the sample which was annealed in lower temperature. Besides, co-sputtered film became two separate ports in trapping layer. One of them is clearly observed that many NCs formed under continuous film and on tunnel oxide by thermal treatment. We could observe that the trapping effect occurred from its C-V hysteresis. Compare this with Fig. 4-10, we could find that there are no separate layers and NCs in this trapping layer after annealing in higher temperature. Besides, there was smaller but not zero memory window in its C-V hysteresis. Because of them, we could consider the main trapping effect occurs on the nanocrystal and the oxidized Ge elements contribute extra charge trap site.

We could know that cobalt oxide, germanium oxide and silicon oxide will be formed by chemical reactions in the Co- $Si_{0.5}Ge_{0.5}$ co-sputtered thin film and $CoSi_2$ will become agglomerate during the annealing process. The TEM image in Fig. 4-7 shows the sample which was annealed in lower temperature. We could observe that there are two layers in the Co- $Si_{0.5}Ge_{0.5}$co-sputtered thin film. The upper layer is a continuous film which is nonconductors and the lower layer is a discontinuous layer which is formed with many NCs and we can't observe it in Fig. 4-10 which was annealed after annealing in higher temperature.

We could understand the mechanism of $CoSi_2$ aggregation and oxidation. First, Co elements easily diffuse to silicon dioxide such as tunnel oxide or capped oxide. During the thermal process, the diffusion behavior of Ge and Co dominates the aggregation of nanocrystals. We know that that various elements will de agglomerate and oxidize simultaneously. In upper layer, Co, Si and Ge has been oxidized to form various oxide before agglomerating and form a capped oxide which is similar to silicon dioxide with various oxide such as CoO_x , SiO_y and GeO_z. It can be found that Ge and Co tend to diffuse out to the capped oxide obviously. The out-diffused Co and Ge react with external oxygen to form the cobalt oxide and germanium oxide during

the process of RTO rapidly. Because there is a capped oxide which is similar to silicon dioxide in the bottom layer, the driving force for the diffusion of oxygen interstitials into the Co-SiGe co-sputtered film would be the solubility limit of oxygen at the anneal temperature. On the other hand, the aggregative growth rate will be greater than oxidation rate in the bottom trapping layer. From the analysis of material in Fig. 4-9, we could understand that there are molecules with Ge-O, Co-O and Co-Si bonds in this trapping layer. The same thing may be said of Fig. 4-7. The XPS analysis in Fig. 4-9 is agreement with observation in Fig. 4-7.

From TEM image was showed in the Fig. 4-10 and that show the cross-sectional TEM and the C-V hysteresis of the fabricated device sample after RTO process. From Fig. 4-12 showed the XPS analysis of the trapping layer after annealing at higher temperature, we could know that there are molecules with Ge-O and Co-O but no Co-Si bonds in this trapping layer. The same thing may be said of this TEM image and the XPS analysis of this trapping layer. The oxidation rate will be greater than aggregative growth rate in the bottom trapping layer after annealing higher temperature.

Fig. 4-13 showed the electrical current density-voltage (*J-V*) hysteresis of three conditions differed from oxidation duration of the Co- $Si_{0.5}Ge_{0.5}$ co-sputtered thin film. In Fig. 4-13, we could observed that the leakage currents exhibit a nearly result about from 10^{-12} order to 10^{-13} order. As the sample was oxidized without capped oxide layer, shown in Fig. 4-15, the Ge elements without any block were out-diffused seriously. The cobalt elements react with Silicon to form $CoSi_2$ and with oxygen to form CoO. $CoSi_2$ will agglomerate when the aggregative growth rate was greater than oxidation rate in the bottom trapping layer.

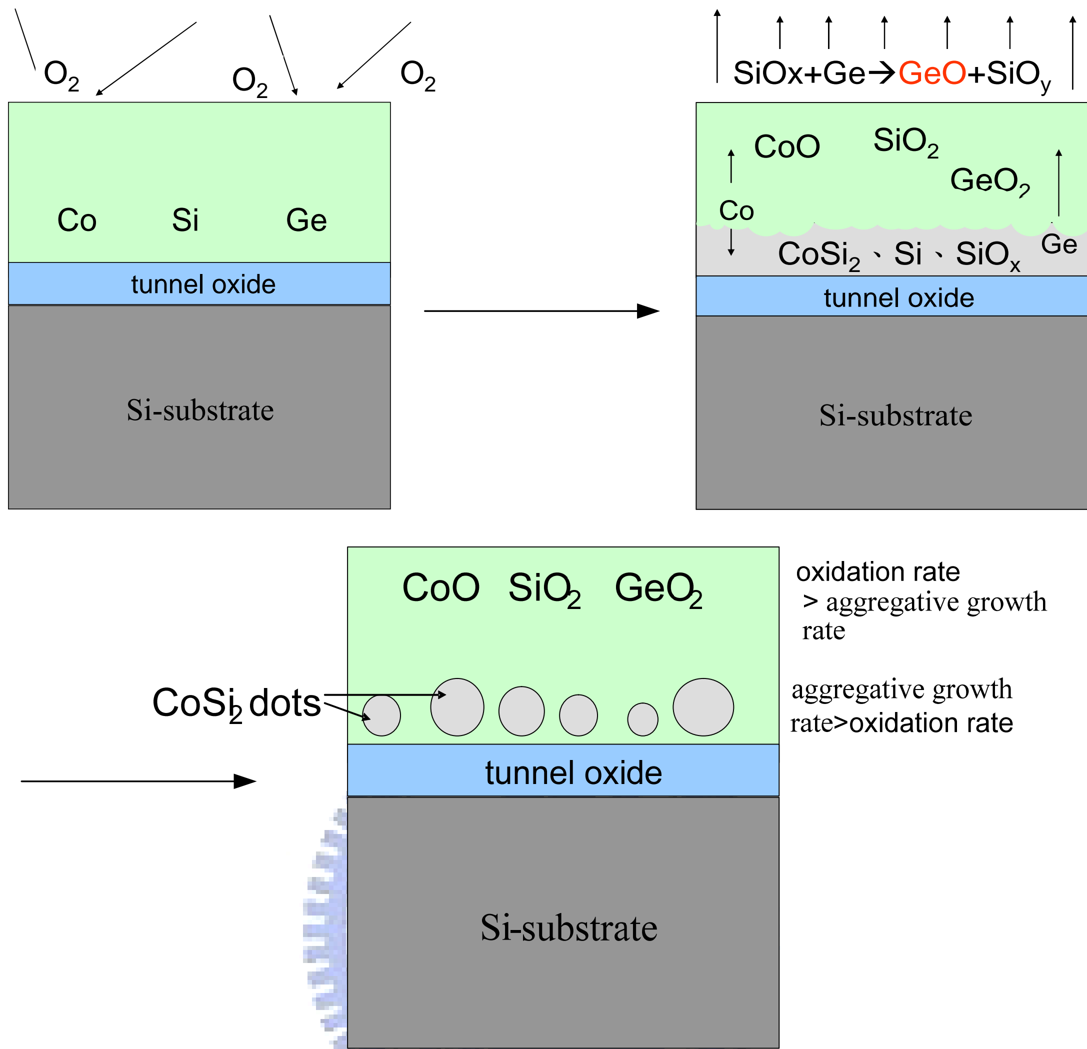


Figure 4-15 The oxidation and aggregative mechanism in the Co-$Si_{0.5}Ge_{0.5}$ co-sputtered thin film without capped oxide

4.3 The role of capped oxide during the formation of cobalt-silicide ($CoSi_2$) nanocrystals in Ge-doped dielectric layer

As for co-sputtered thin film which is formed with $CoSi_2$ and $Si_{0.5}Ge_{0.5}$. According to materials, it still was a Co-Si-Ge thin film but the proportion of materials is different.

Fig. 4-16 (a) (b) shows the C-V hysteresis after bidirectional sweeps, which implies the electron charging and discharging effects of the metal-oxide-insulator-oxide-silicon (MOIOS) structure. It can be found that the cobalt silicon germanium mixed film with capped oxide before RTO treatment shows 4.8V of flat-band voltage shift under ± 7V gate voltage operation. Also, a lager memory window can be obtained with a lager gate voltage operation. According the past literature, the memory window is attributed to the trapping center of cobalt-silicide nanocrystals and oxidized Ge elements because of the existence of GeO_x defective layer. However there is smaller memory window can be found in the structure without a capped oxide. Even the swept voltage is increased to ± 9 V; a lager flat-band voltage shift still can not be seen. It can be concluded that mechanism of charge storage between the structures is different.

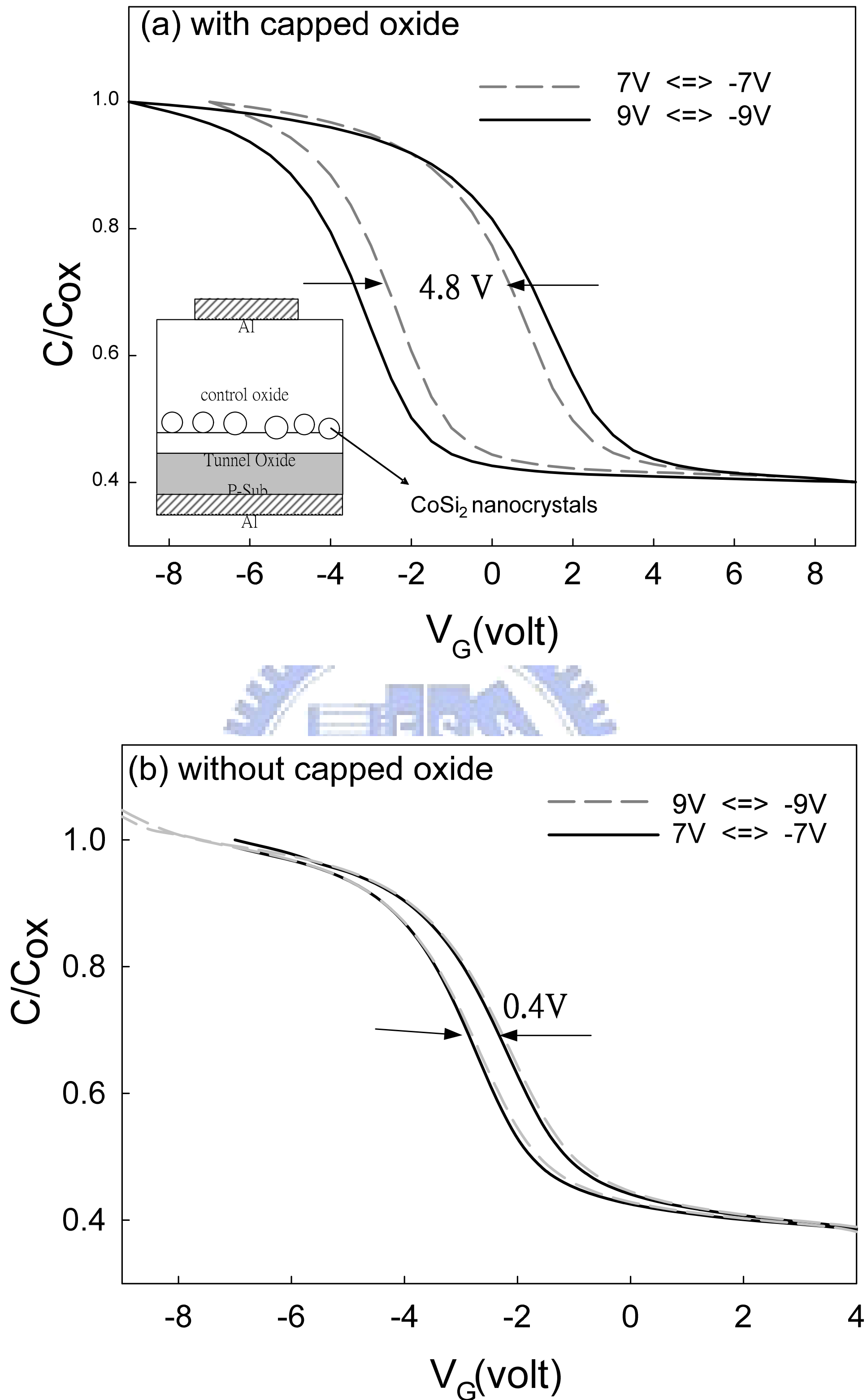
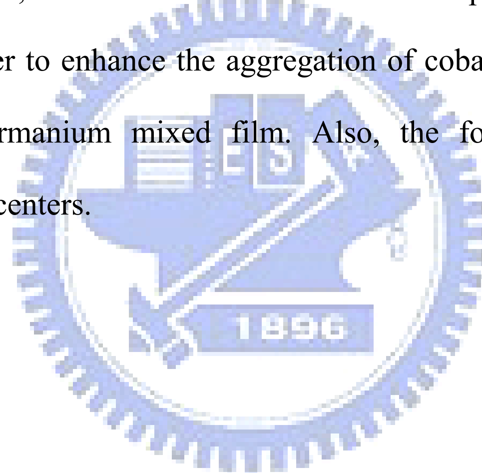
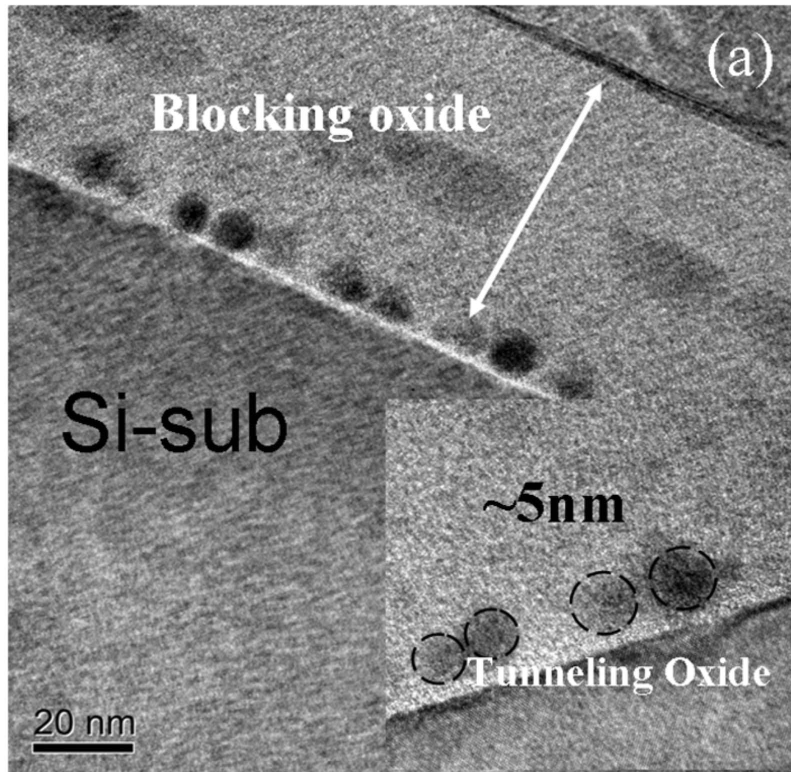


Figure 4-16 The *C-V* characteristics of the Co-Si-Ge co-sputtered film with $CoSi_2$ and SiGe targets (a) with and (b) without capped oxide before annealing.

A lager memory window was observed in the cobalt silicon germanium mixed film with capped oxide after RTO treatment. In order to realize the effect of the capped oxide during the RTO process, TEM analyzes had been used.

In Fig. 4-17, the structure (a) with and (b) without capped oxide can be appear on the Cross-sectional TEM. A clear image of nanocrystal can be seen in Fig. 4-17 (a). Nevertheless, the TEM image of the structure without capped oxide does not reveal obvious aggregation behavior. It can be found that the capped oxide can enhance the aggregation of nanocrystals. According the past paper, Gong-Ru Lin et al [4-9] indicates that the aggregation of nanocrystals can be accelerates through a buffer oxide[4-10]. Therefore, it can be conclude the capped oxide provides a heat-accumulation layer to enhance the aggregation of cobalt-silicide nanocrystals in the cobalt silicon germanium mixed film. Also, the formation of nanocrystals attributes the trapping centers.





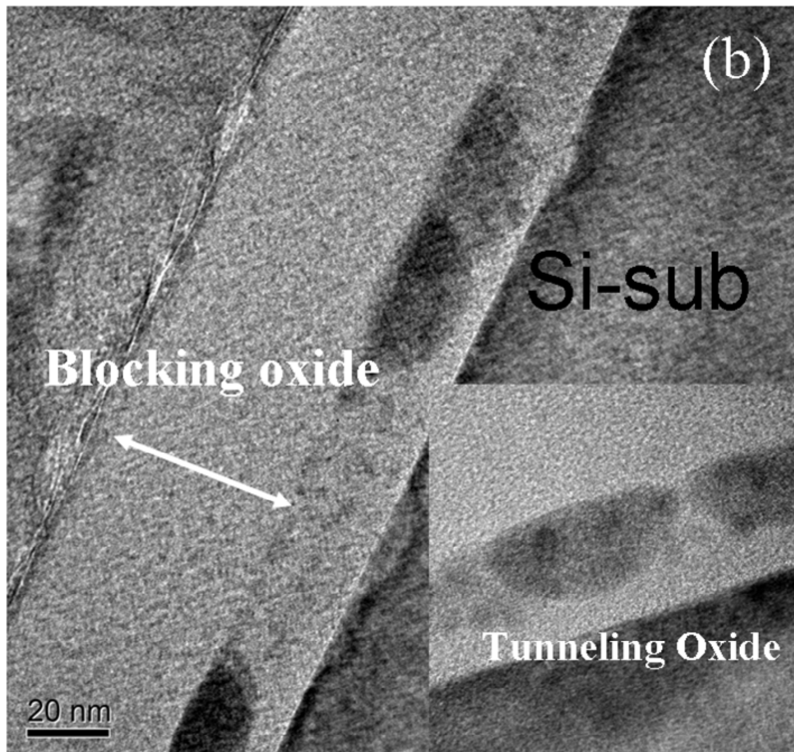
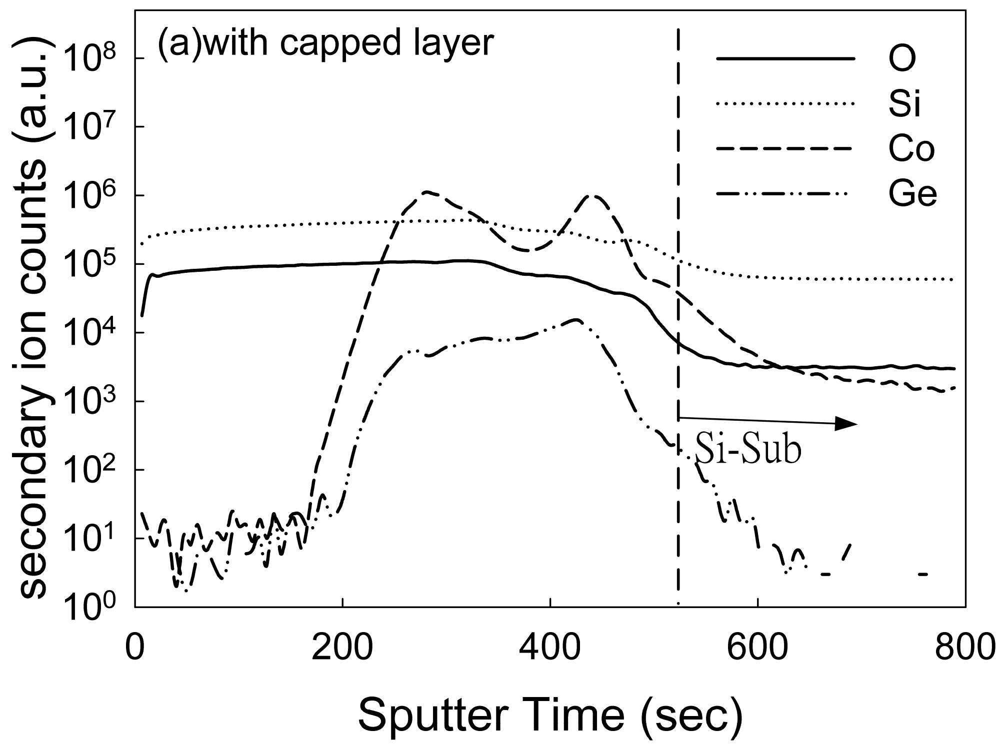


Figure 4-17 The structure (a) with and (b) without capped oxide can be appear on the Cross-sectional TEM.

Fig. 4-18 demonstrates the results of SIMS analysis for the cobalt silicon germanium mixed film with/without capped oxide. During the thermal process, the diffusion behavior of Ge and Co dominates the aggregation of nanocrystals [4-11]. It can be found that Ge and Co tend to diffuse out to the capped oxide obviously in Fig. 4-18 (a). The out-diffused Co and Ge react with external oxygen to form the cobalt oxide and germanium oxide during the process of RTO rapidly. Therefore, the fully oxidation of the cobalt silicon germanium mixed film occur with the excessive RTO treatment. It can be found the amount of Ge in Fig 4-18 (b) becomes less because the oxidized Ge is easy to volatile. In addition, that the oxidized Co and Ge elements are difficult to aggregate results in the cake in the front TEM image. Therefore, the oxidized Co and Ge only attribute an insignificant flat-band shift of Fig 4-16 (b). In addition, the diffusion behavior still occurred even if the capped oxide was used. Oxidation is inevitable during the aggregation of nanocrystals through RTO treatment. However, the capped oxide can restrain the immediate oxidation of the mixed film. With a slow oxidation, partial cobalt can react with silicon to form cobalt-silicide nanocrystals [4-12]. From the Fig 4-18(a), the cobalt forms two clumps which is due to the out-diffused cobalt and the aggregated cobalt-silicide. Then it can be assumed that the attribution of cobalt silicide nanocrystals, oxidized cobalt and oxidized cobalt bring about a larger flat-band shift than the structure without capped oxide.



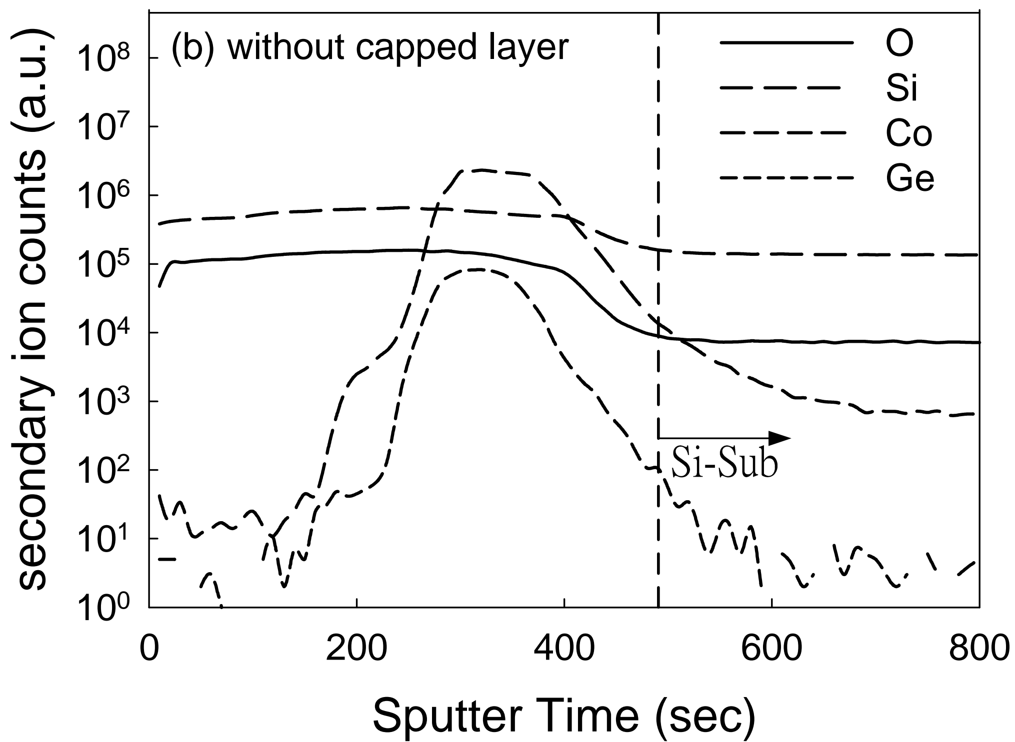


Figure 4-18 The results of SIMS analysis for the cobalt silicon germanium mixed film (a) with\ (b) without capped oxide.

Moreover, the leakage current in the MOIOS structure is shown in Fig. 4-19. The lower leakage current could avoid the stored charge leaking into gate through the blocking oxide to get better retention time for the MOIOS structure. According to the reported paper, the asymmetry of J-V characteristics in the figure is because when the applied voltage is swept from 0 to +10V, some negative charges are trapped in the defects of the dielectric layer, leading to an increase of the injection barrier height and, therefore, to a decrease of the oxide conductivity. The leakage currents exhibit a nearly result about from 10^{-11} order to 10^{-12} order.

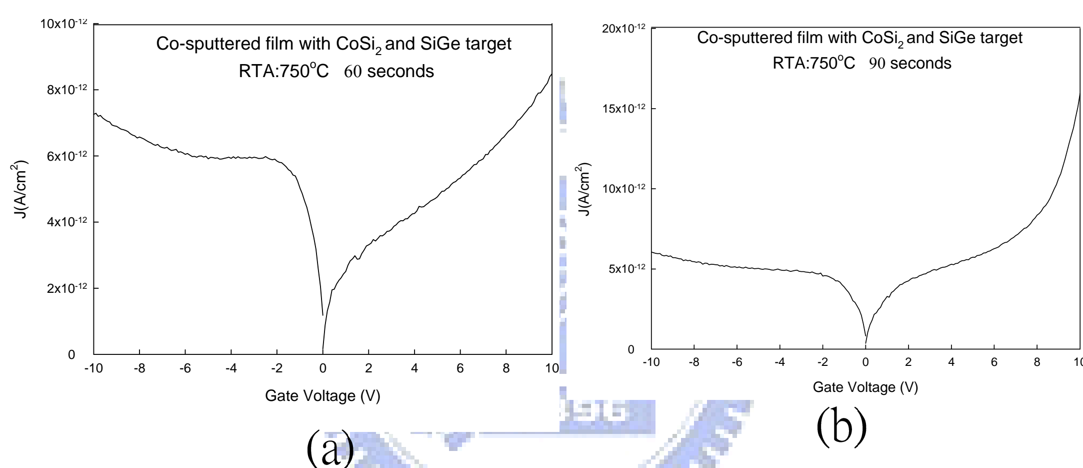
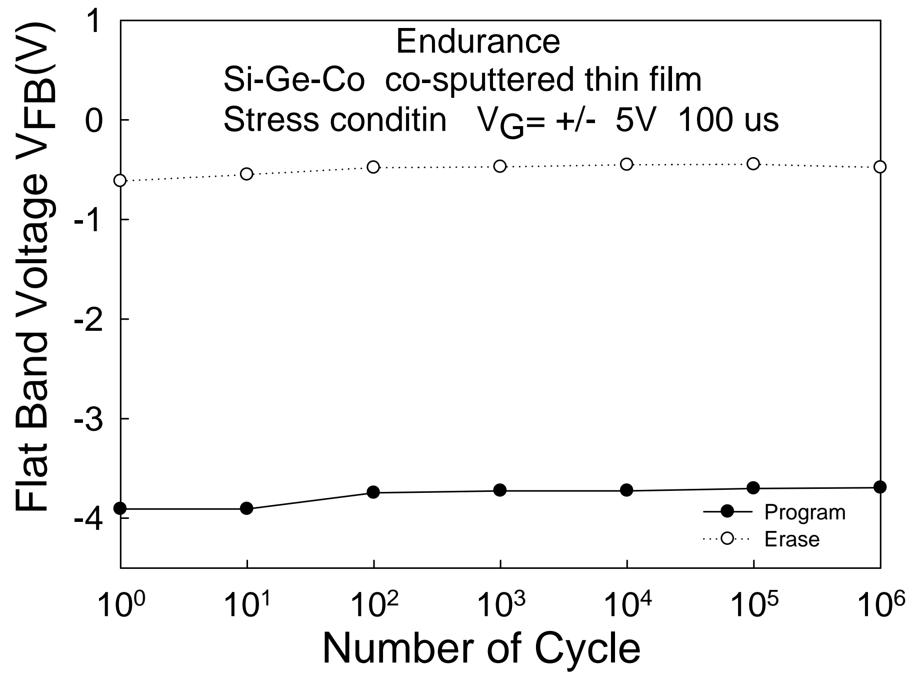


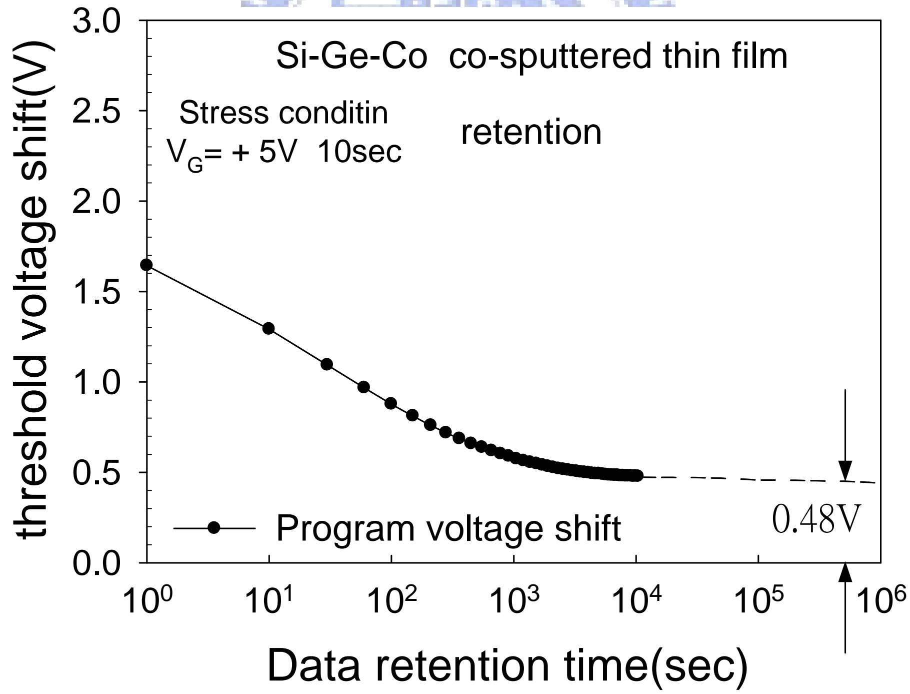
Figure 4-19 The *J-V* characteristics of the capacitor based on the Co- Si-Ge co-sputtered film with oxidation in different condition.

In Fig. 4-20 (a), the endurance characteristics of the memory which was base on the cobalt silicon germanium mixed film after RTO process. It indicates the memory window can be retained after 10^6 program/erase cycles at room temperature. In addition, In Fig. 4-20 (b) exhibits the charge retention characteristics of the memory which was base on the cobalt silicon germanium mixed film after RTO process at room temperature. It is found that the carrier charges can be kept after 10^4 seconds.

The good electrical reliability characteristics were also obtained in the proposed the memory which was base on the cobalt silicon germanium mixed film after RTO process.



(a)



(b)

Figure 4-20 Data (a) endurance and (b) retention characteristics of the memories which are based on cobalt-silicide nanocrystals

Chapter 5
Conclusion

5.1 Conclusion

In this study, a novel and simple fabrication of $CoSi_2$ nanocrystal was proposed and demonstrated for the application of nonvolatile semiconductor memory. The memory effect depends on the $CoSi_2$ NCs formation during thermal oxidation process. The superior memory windows and good electrical reliability characteristics can be all realized in the proposed structure in this work. The obvious memory window is attributed to both the cobalt-silicide NCs and the trap-rich oxidized Ge elements. We have realized the procedure of oxidation mechanism when the samples are annealed with varies material analysis in this study.

We could know that the oxygen diffusion from upper oxide plays an important role from TEM image, XPS, EDX and so on because oxygen may also be leached from the SiO_2, CoO and GeO_2. When the Co-Si-Ge co-sputtered film was annealed at lower temperature, the aggregative growth rate will be greater than oxidation rate in the bottom trapping layer. The nanocrystal will be formed in the bottom trapping layer by aggregative process and upper trapping layer will form continuous layer which is nonconductor. We could consider the main trapping effect occurs on the nanocrystal and the oxidized Ge elements contribute extra charge trap site.

We consider that the capped oxide before oxidizing plays an important role. In addition, this formation method of cobalt-silicide NCs with distributed storage elements is easy and compatible with the current manufacturing technology of semiconductor industry. We demonstrate the importance of the capped oxide during

the formation of the cobalt silicide nanocrystals in Ge-doped dielectric layer. The structure with a capped oxide reveals an obvious aggregation of cobalt-silicide nanocrystals. In order to form cobalt-silicide nanocrystals in brief RTO process, a capped oxide to be the heat-accumulated layer is necessary. In addition, the diffusion and oxidation behavior are inevitable during RTO process. The capped layer before RTO process treatment also can retard the diffusion of external oxygen. Therefore, it can be confirmed that the capped oxide is necessary for the control the aggregation of cobalt-silicide nanocrystals in Ge-doped dielectric layer.

Addendum A
Metal Co-SiO_2 and Co-Si_3N_4 co-sputtering as trapping film of Cobalt mixtures and future development

A.1 Motivation

Compared with the fabricated of cobalt nanocrystal memories surrounded in various dielectrics by cobalt target sputtered in former chapter and some papers [A-1],

In the past, they fabricated the charge storage layer with Co-Si co-sputtering system or dual e-guns system. The cobalt nanocrystals will embed in dielectrics layer to form memory devices. We know that memory with discrete charge elements allows more advanced scaling of tunneling oxide and exhibit superior characteristics compared to conventional FG structure memories in terms of operation voltage, write/erase speed, retention and endurance [A-2] to [A-4]. In this work, we describe a novel technique of fabricating cobalt nanocrystal quasinonvolatile memory capacitance. Co and Si-$CoSi_2$ targets were used to prepare the mixed film on tunnel oxide with DC guns co-sputtering. Metal cobalt has greater work function than silicon oxide. For example, Pt is 5,29eV, Pt is 4.84eV and Co is 4.18eV. Because of this, the electrons which trapped in such metal nanocrystals tunnel to the substrate or control gat will small amount due to the higher electron barrier height, resulting in the prolonged data retention time. A new method to manufacture cobalt nanocrystals was proposed in this chapter. The Co and SiO_2 targets were used to prepare the mixed film on tunnel oxide with sputter DC and RF guns. Using this method will also be the

same property. Because the time was not enough and there were no tools measuring thickness when co-sputtering on the machine. I will anneal with O_2 to reduce pure metal cobalt amount because of oxidation and confer on the influence of trapped effect on it and anneal with N_2. As the purpose of this thesis is concerned, it is not necessary to discuss fabrication of good memory but the memory windows in different conditions in detail.

A.2 Experimental procedure

P-type silicon wafers with <100> orientation were used for the fabrication of MIS capacitors. Fig. A-1 (a) and (b) was showed the schematic diagrams of fabricating procedures for Co-SiO_2 and Co-Si_3N_4. First, (100) oriented P-type 4 inch silicon wafers were chemically cleaned by standard Radio Corporation of America cleaning (RCA cleaning), followed by thermally growing of a about 5-nm-thick tunnel oxide at 1000°C by fry-oxidation horizontal furnace system(atmospheric pressure chemical vapor deposition, APCVD), and then the oxide measured by N&K 1200 was 45~51 Å. The pure Co target was sputtered by a DC power of 100W, the SiO_2 target sputtered by a RF power of 100W simultaneously during 2 minutes among the deposition. Similarly**,** a co-sputtered film of cobalt and silicon nitride was deposited on the tunnel oxide by sputtering system. The pure cobalt target was sputtered by a DC power of 100W and the Si_3N_4 target sputtered by a RF power of 120W during the same time. After that because the DC power is too large, we changed its power and depositing time to test. Both the above co-sputtered film deposited on the tunnel oxide at room temperature with 4.5mtorr pressure of the chamber. Some characters about cobalt list in table A-1.Next step ,we annealed the sample with rapid thermal annealing (RTA) for 30s~90s and Furnace for 5 minutes~20 minutes in N_2 and O_2 ambient that temperatures was about 550°C~750°C.

During the annealing process cobalt elements had accumulated to form cobalt nanocrystals which were embedded between silicon dioxide.

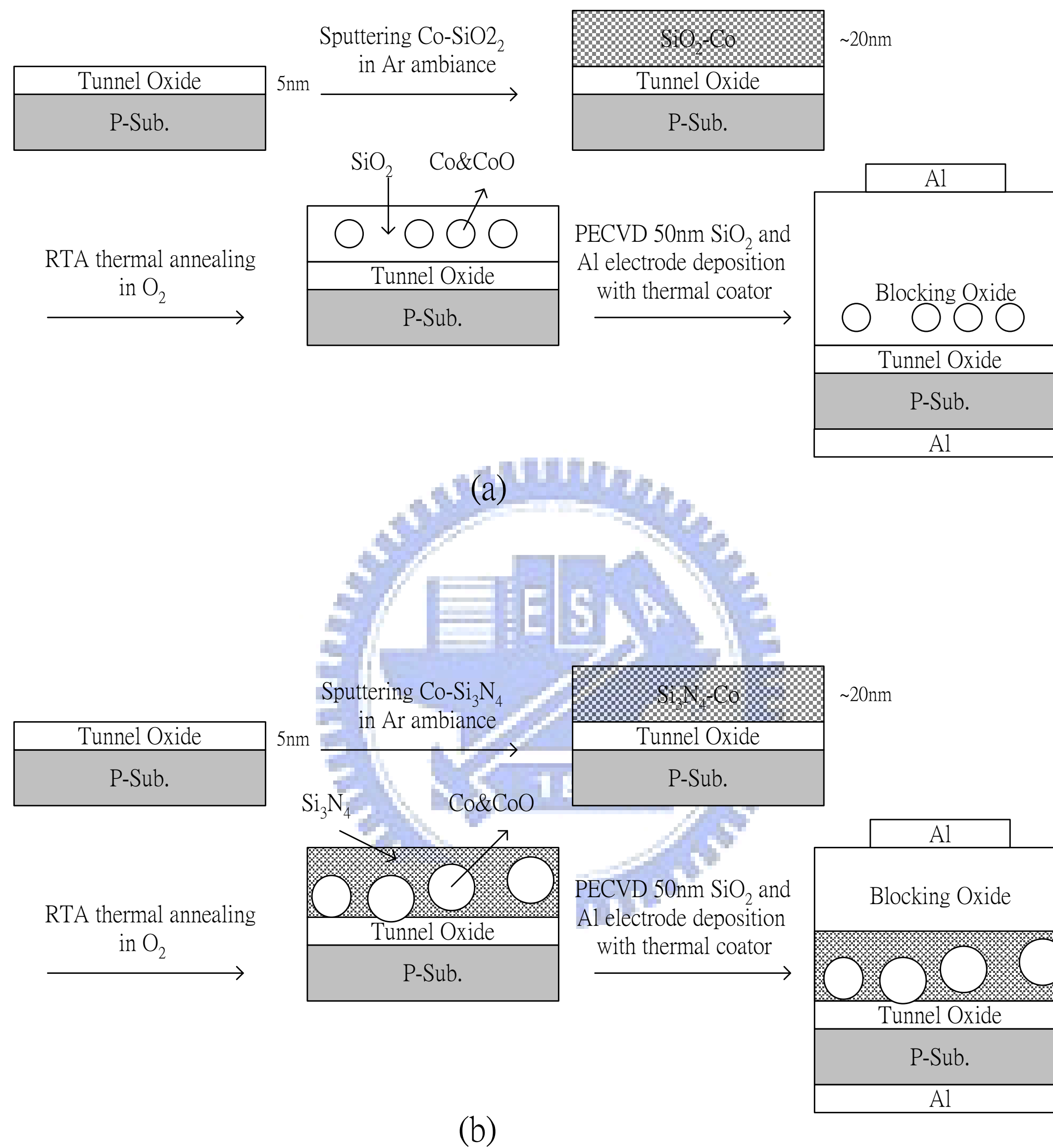


Figure A-1 The process flow of structure is (a) SiO_2/Co-SiO_2/ SiO_2/Si and (b) Si_3N_4/Co- Si_3N_4/ SiO_2/Si in this work.

Cobalt general character	
Name, Symbol, Number	cobalt, Co, 27
Chemical series	transition metals
Group, Period, Block	9, 4, d
Density	8.90 g·cm^{-3}
Melting point	1768 K (1495 °C, 2723 °F)
Boiling point	3200 K (2927 °C, 5301 °F)
Heat of fusion	16.06 kJ·mol^{-1}
Heat of vaporization	377 kJ·mol^{-1}
Heat capacity	(25 °C) 24.81 J·mol^{-1}·K^{-1}
Work function	4.18eV

Table A-1 Some character about metal cobalt

After annealing a 50nm SiO_2 layer was deposited by plasma enhanced chemical vapor deposition (PECVD) system to form the control oxide. Finally, the Al gate electrode was patterned and sintered to form metal/oxide/silicon (MOS) structure with Co nanocrystals. This MOS capacitance structure was prepared for material and electrical analyses.

A.3 Results and Discussion

Fig. A-2 presents typical bright-field, cross-section TEM images and its Energy dispersive X-ray spectroscopy (EDX) is an analytical technique used predominantly for the elemental analysis or chemical characterization of a specimen. EDX provides a powerful tool for identifying local composition within TEM images and is utilized extensively in applications ranging from failure analysis to elemental mapping. From

EDX spectroscopy, we know that what the local elemental composition is and there are cobalt and oxygen in the dot. It shows the structure of the film which is based on Co-SiO_2 co-sputtered film. As illustrated in Fig. A-2, the well-separated and spherical Co nanocrystals embedded between the control oxide layer and the tunnel oxide layer were observed clearly. The nanocrystals (the charge storage layer) embedded in dielectrics layer of metal-oxide–insulator- oxide silicon (MOIOS) memory device was utilized to capture the injected carriers from the channel, which caused a variation in the threshold. The insulator layer usually maybe Co-SiO_2 film or Co-Si_3N_4 film in this chapter.

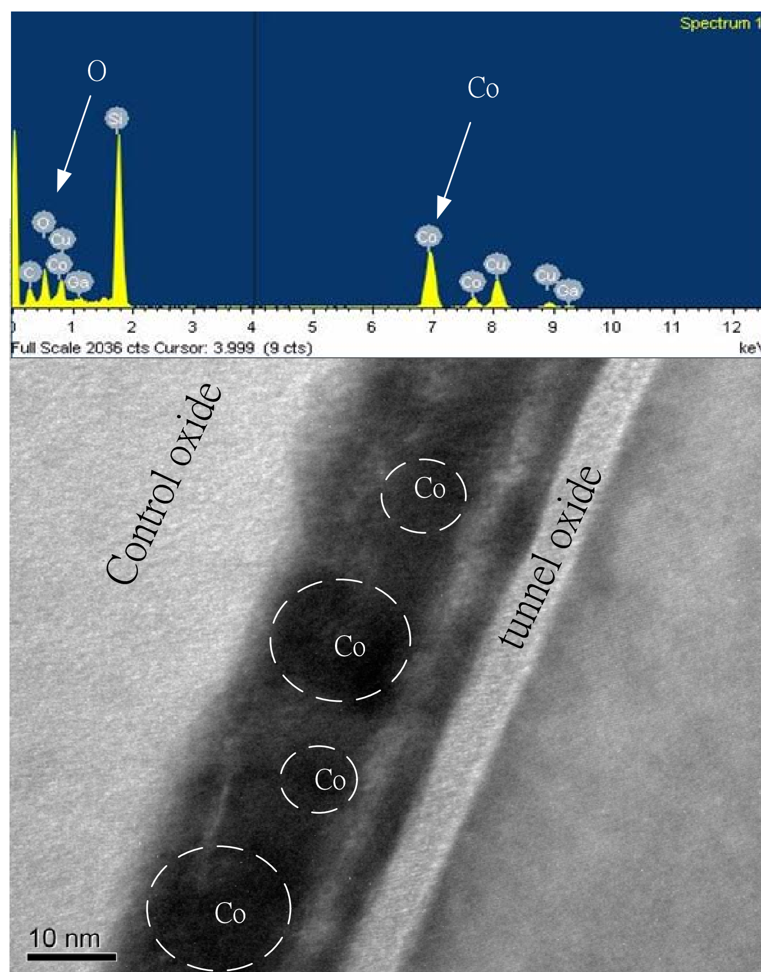


Figure A-2 Transmission electron microscopy (TEM) analyses and its EDX. After annealing cobalt elements had accumulated to form cobalt nanocrystals which were embedded between tunnel oxide and control oxide after anneal at 750℃ and during 30 seconds.

Fig. A-3 show the forward and reverse capacitance-voltage (*C*-*V*) curves for

as-deposited samples obtained when the gate voltage was first swept from –7V to +7V (accumulation to inversion, forward sweep) and then from +7V to –7V (inversion to accumulation, reverse sweep) for Co-SiO_2 co-sputtered based MIS structure. In the same way Fig. A-4 show the forward and reverse capacitance-voltage (*C-V*) curves for as-deposited samples obtained when the gate voltage was first swept from –7V to +7V (accumulation to inversion, forward sweep) and then from +7V to –7V (inversion to accumulation, reverse sweep) for Co-Si_3N_4 co-sputtered based MIS structure. One of them is different and the applied voltage also was ±9 volts over and above ±7. The bidirectional *C-V* sweeps were performed from deep inversion to deep accumulation and in reverse, which exhibited an electron charging effect.

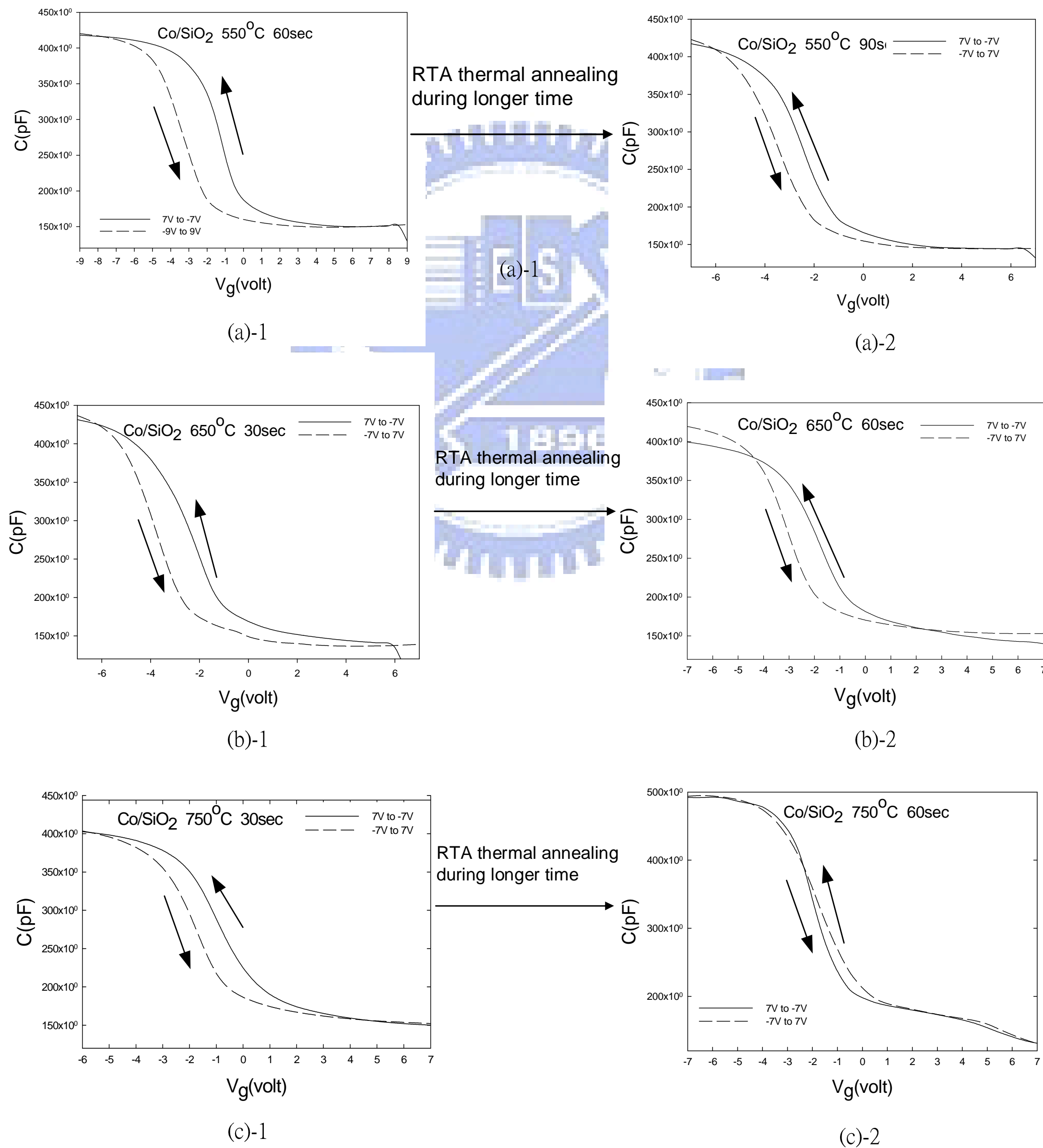


Figure A-3 The *C-V* hysteresis of the memory which is based on

Co-SiO_2 co-sputtered file.

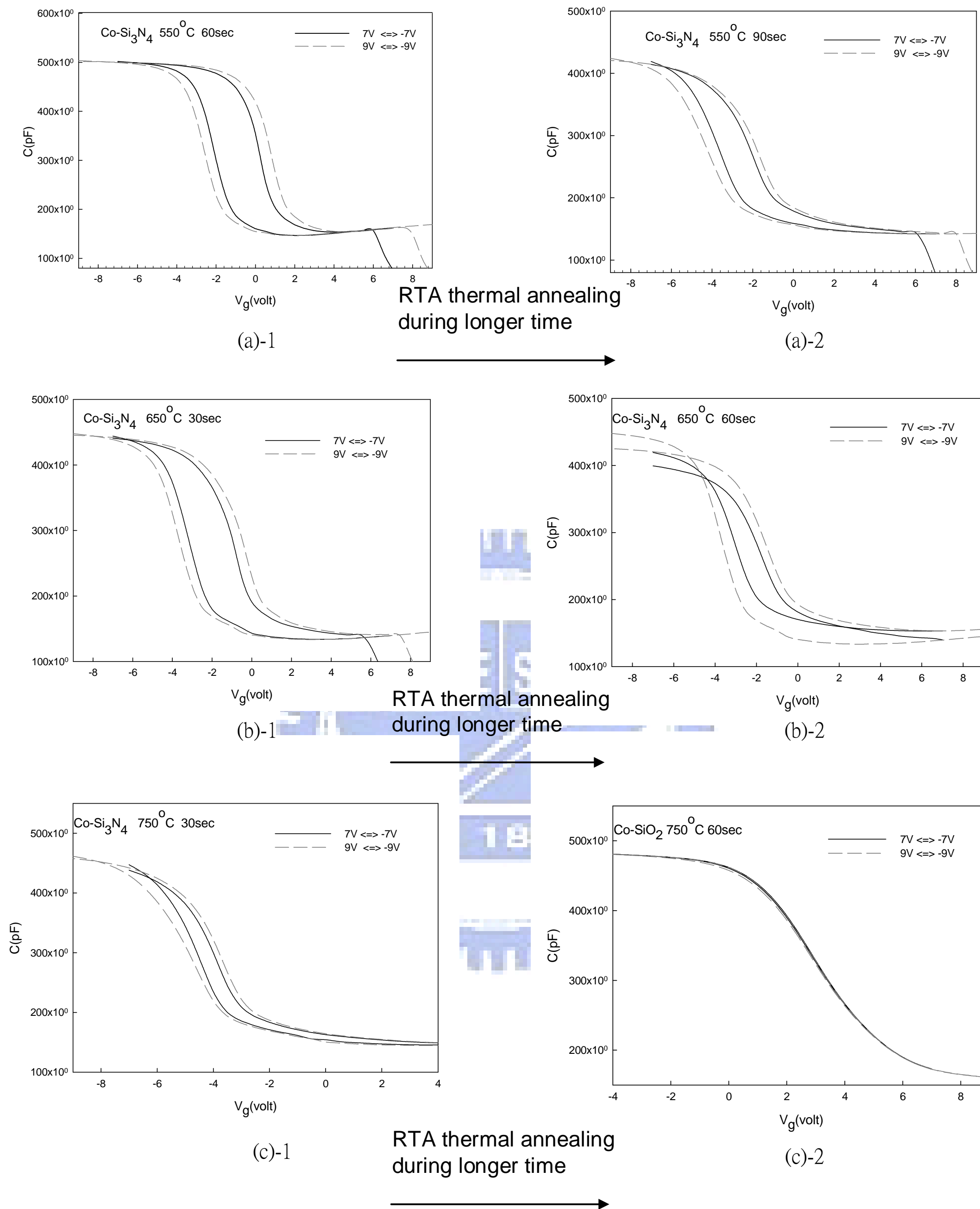


Figure A-4 The *C-V* hysteresis of the memory which is based on Co-Si_3N_4 co-sputtered file.

We could observe that threshold-voltage shifts were reduced and memory window also was smaller as the memory was annealed during longer time in Fig. A-3 and Fig. A-4. For a fine example of this phenomenon, the threshold-voltage shifts of

the memory which was annealed at 550°C during different time were smaller as annealed time with Rapid Thermal Processing (RTP) system was longer. There is the same phenomenon in the Co-SiO_2 co-sputtered film based or the Co-Si_3N_4 co-sputtered film based memory. It is considered that there were less cobalt elements to form nanocrystals and some cobalt elements to form another chemical compound. The cobalt reacts with oxygen to make rust during annealing in O_2.ambiance. Here is an example of chemical reactions with the corresponding chemical equation. Cobalt oxide had large internal resistance [A-5] and therefore cobalt oxide had not been a good conductor. There is considerable validity in our ratiocination: some cobalt elements formed another chemical compound during annealing in O_2 ambiance. It was shown in figure 3-3 (a)-1, (b)-1, (c)-1 the MOIOS structure have larger memory window than in figure 3-3 (a)-2, (b)-2, (c)-2 under ±7V *C-V* sweeping. As the oxidation time increasing, the threshold-voltage shifts became smaller reversely as former discussed. The memory effect was observed from the hysteresis capacitance-voltage (*C-V*) characteristics of MIS capacitors embedded with the charge storage layer. According to the theoretical derivation [A-6], i.e. $Q = -V_{fb}C_{control}$, the total charges trapped in the capacitor can be approximately estimated and the model is schematized in Fig. A-5. We could observe that the value of trapped electrons or holes in memory which was annealed during loner time is lower than the memory which was annealed during shorter time. The memory windows under ±7V operation for the two types of MOIOS structure were listed in Table A-2. We have discussed the electrical characteristics of cobalt nanocrystals embedded in silicon oxide or nitride film during different annealed time. We could know there are the points to be specially considered. The XPS, also called ESCA, analyses were carried out with previous ion bombardment cleaning of the sample surfaces. Since the diameter of X-ray beam is large so that the analyses of XPS were may contributed by

nanocrystal itself and dielectric layer, such as the embedded dielectric, tunnel oxide or capped oxide. However, the resolution can not clearly be indicated that the contribution of nanocrystals. As a consequence, all the XPS peaks show a fairly valuable contribution from the bonding between the element and oxygen. The XPS pecks were fitted with fitting program. The values of the binding energy corresponding to the main contributions for each XPS peaks were exhibited clearly [A-7]. Because of them, XPS is an effective and widely used surface analysis technique and therefore we analyzed the material in Co-SiO_2 and Co-Si_3N_4 co-sputtered film with XPS.

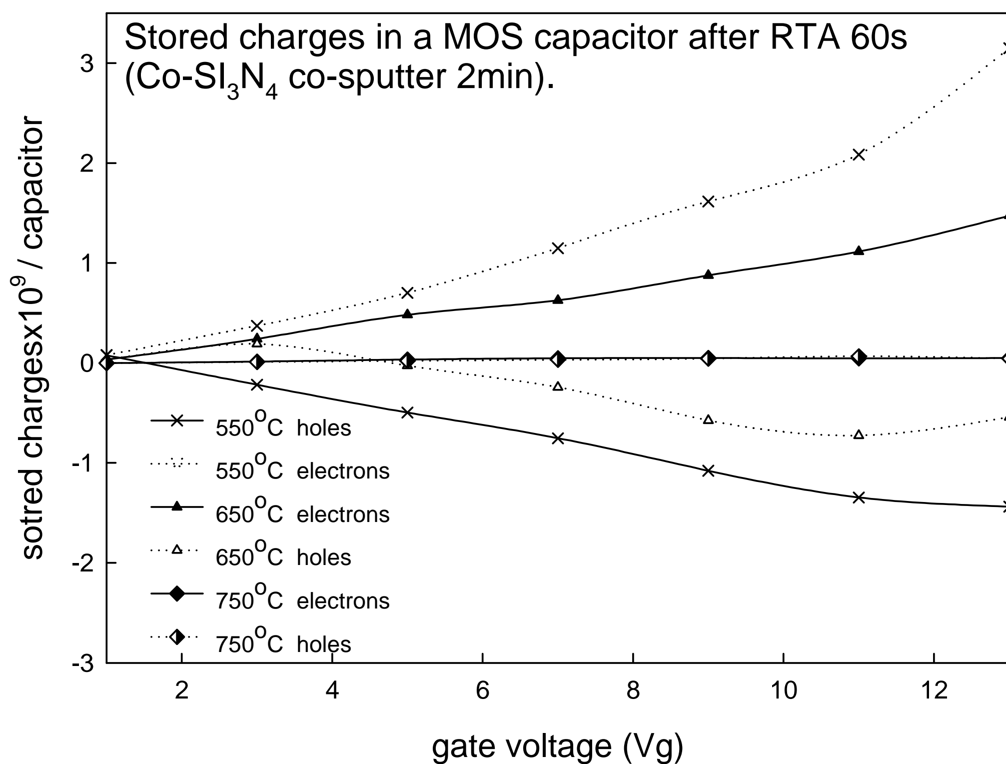


Figure A-5 The relations between gate voltage and flat-band voltage, stored charges in a MIS capacitor. The insets in this figure the high frequency *C*-*V* relations of MIS capacitors co-sputtered to form the charge storage film with metal Co embedded in the Si_3N_4 during different annealed time respectively.

Co-sputtered Co-SiO_2

Oxidation Time / temperature	Shorter tine	Longer tine
550 °C	2V	1V
650°C	1.5V	1V
650°C	1V	0V

Co-sputtered Co-Si_3N_4

Oxidation Time / temperature	Shorter tine	Longer tine
550°C	2.25V	1.8V
650°C	2.2V	1.2V
650°C	1.2V	0V

Table A-2 the comparison of memory windows in the memory which was based on the Co-SiO_2 co-sputtered film and the Co-Si_3N_4 co-sputtered film under ±7V operation with their corresponding oxidative conditions.

Fig. A-6 shows the XPS (ESCA) spectra of Co 2p3/2 peaks in the memory which is based on Co-SiO_2 co-sputtered film. It is found that the Co 2p3/2 peak is a superimposition of many peaks. We could observe that there are Co-O bonds and Co-Co bonds in this film after annealed process. By the same token, we also observed Co-Si_3N_4 co-sputtered film which was annealed. They were showed in Fig. A-7.

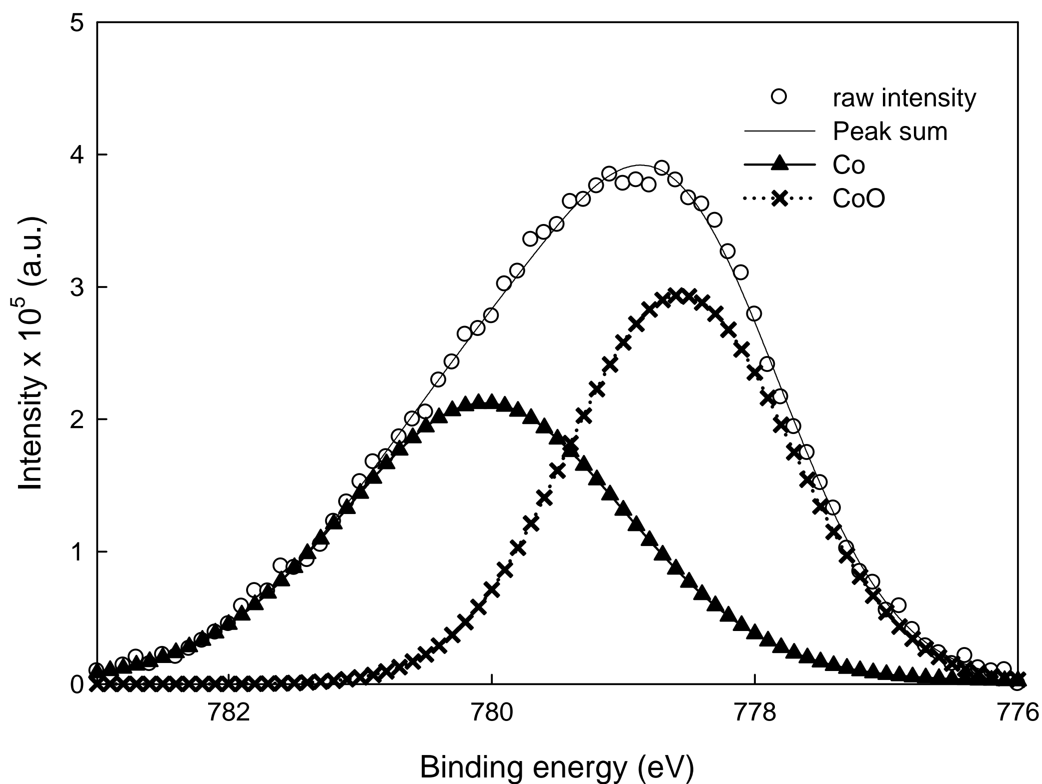
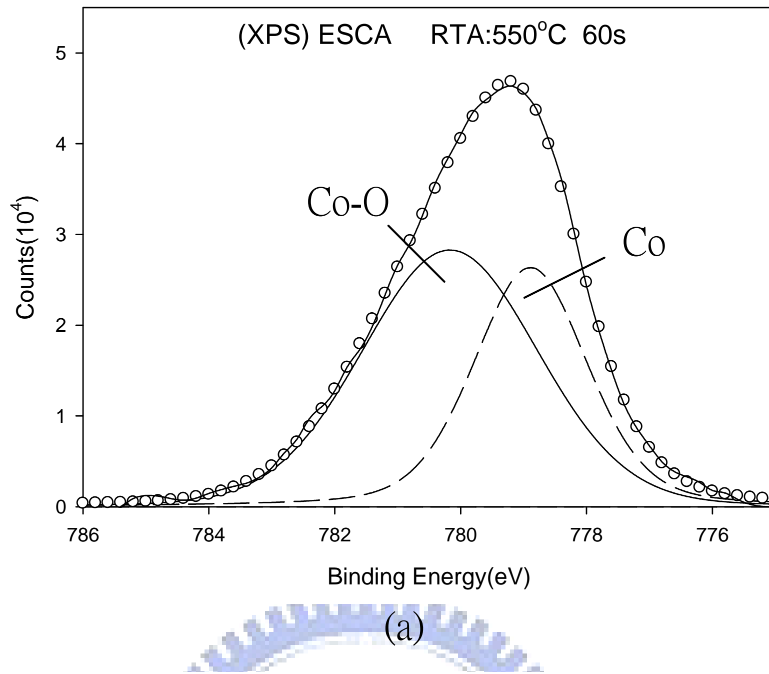
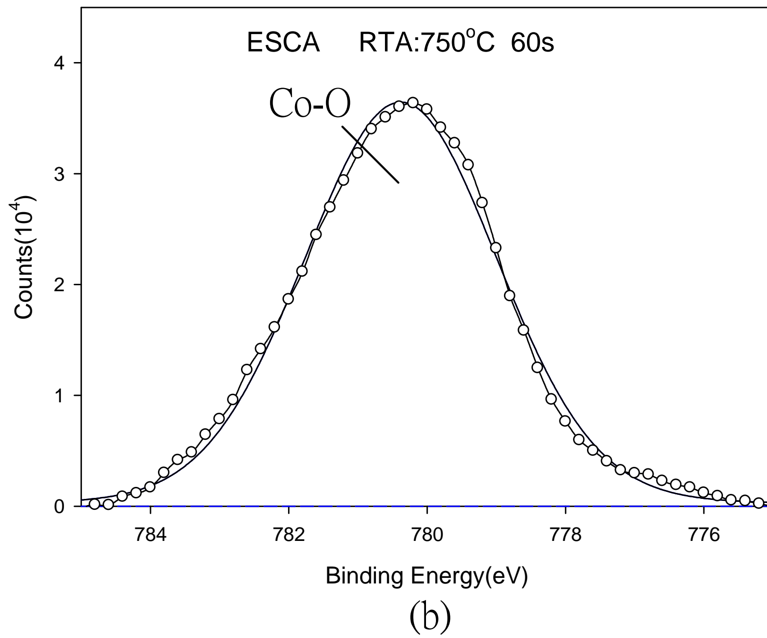


Figure A-6 The XPS spectra of Co 2p3/2 peaks in the memory which is based on Co-SiO_2 co-sputtered film.



(a)

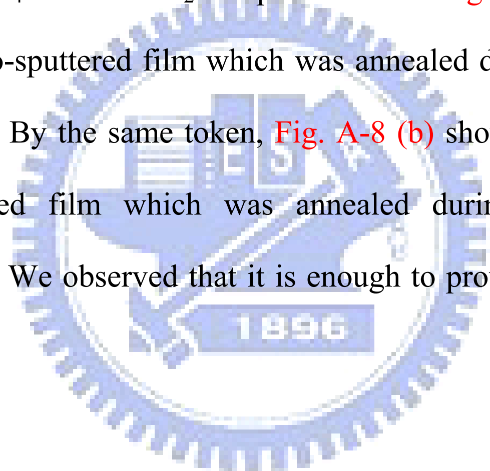


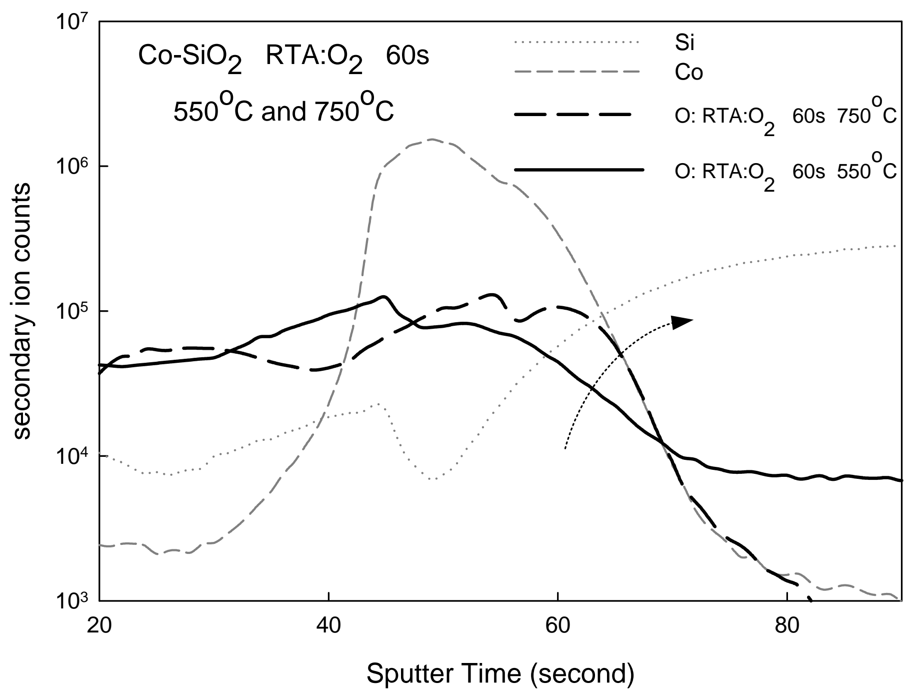
(b)

Figure A-7 The XPS spectra of Co 2p3/2 peaks in the memory which is based on Co-Si_3N_4 co-sputtered film.

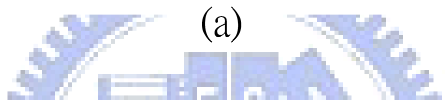
From Fig.A-6 and Fig. A-7, the point to observe is that cobalt elements will react with oxygen to make cobalt oxide during oxidation process. We could represent this assumption in XPS diagrams as follows. The lower pure Co elements in the oxidized film (replaced by Co-O) cause the lower memory effect. The partial contribution of Co nanocrystals transferred to the cobalt oxide dielectric after thermal oxidation.

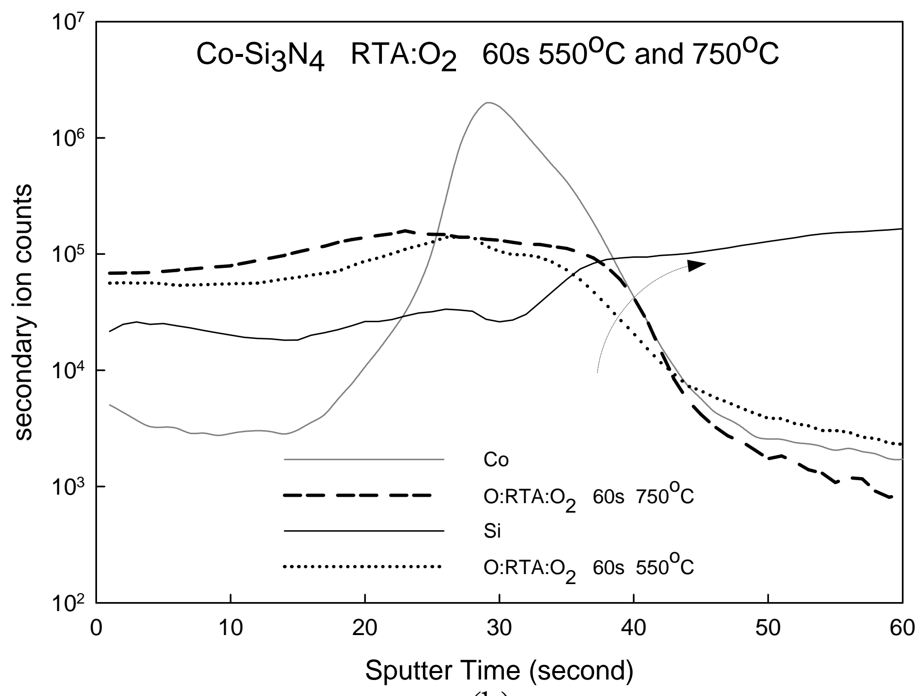
As the discussion said, there was no memory window in the samples which was annealed during longer time but obvious memory characteristics in that with during shorter time. To compare the two entirely different results, the series of SIMS analyses of the Co-Si_3N_4 and Co-SiO_2 co-sputtered film. Fig. A-8 (a) shows the SIMS analysis of Co-SiO_2 co-sputtered film which was annealed during 60 sec in different temperature ambiance. By the same token, Fig. A-8 (b) shows the SIMS analysis of Co- Si_3N_4 co-sputtered film which was annealed during 60 sec in different temperature ambiance. We observed that it is enough to prove that this hypothesis is true.





(a)





(b)

Figure A-8 (a) the SIMS analysis of Co-SiO_2 co-sputtered film which was annealed during 60 sec in different temperature ambiance (b) the SIMS analysis of Co-Si_3O_4 co-sputtered film which was annealed during 60 sec in different temperature ambiance.

The current density-voltage (J-V) characteristics of the memory which is based on the Co-SiO_2 and Co- Si_3N_4 co-sputtered film. It is shown in Fig. A-9. We could know that the leakage current exhibited a nearly result about from 10^{-9} order to 10^{-10} order after annealing during 30 sec. Other annealing time and temperature is quite similar to this.

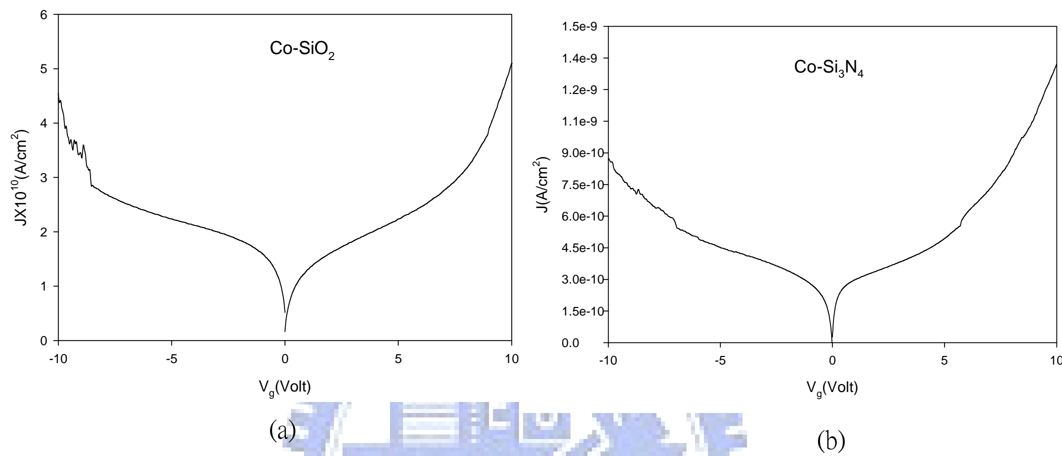


Figure A-9 The J-V characteristics of the memory which is based (a) on the Co-SiO_2 co-sputtered film (b) on the Co-Si_3N_4 co-sputtered film

The endurance characteristics of the MOIOS with Co nanocrystals embedded in the co-sputtered film are illustrated in Fig. A-10. One (Fig. A-10 (a)) of them is the memory that was based on Co-SiO_2 co-sputtered film and another (Fig. A-10 (b)) is the memory that was based on Co-Si_3N_4 co-sputtered film. Pulses (V_G=±5V) were applied to evaluate endurance characteristics for the Program/Erase operation. The schematic plots indicated the memory windows can be retain as their initial values after 10^6 program/erase cycles at room temperature. The same thing may be said of other conditions.

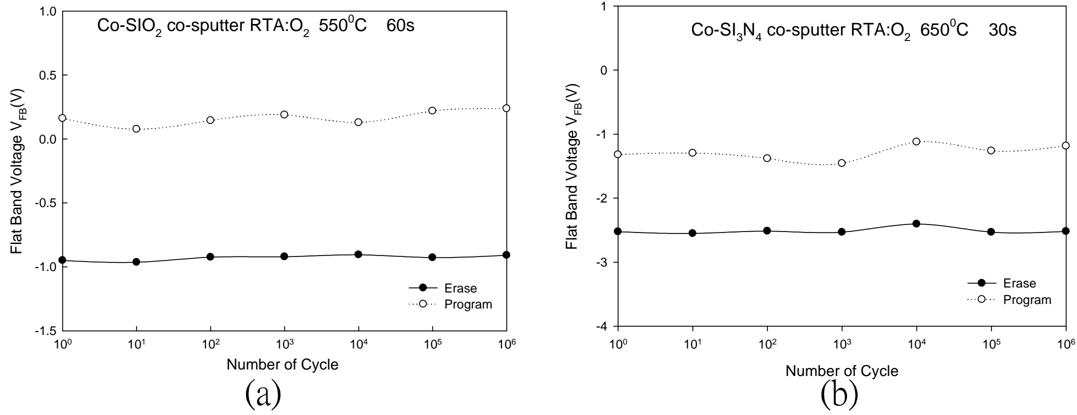


Figure A-10 The endurance characteristics of the MOIOS with Co nanocrystals embedded in the (a) Co-SiO_2 and (b) Co- Si_3N_4 co-sputtered film

The retention characteristics of the memory which is based on Co-SiO_2 co-sputtered film were measured at room temperature, as shown in the Fig. A-11. In Fig. A-11, the good retention characteristics and the memory effect without significant decreasing up to 10^4s can be founded.

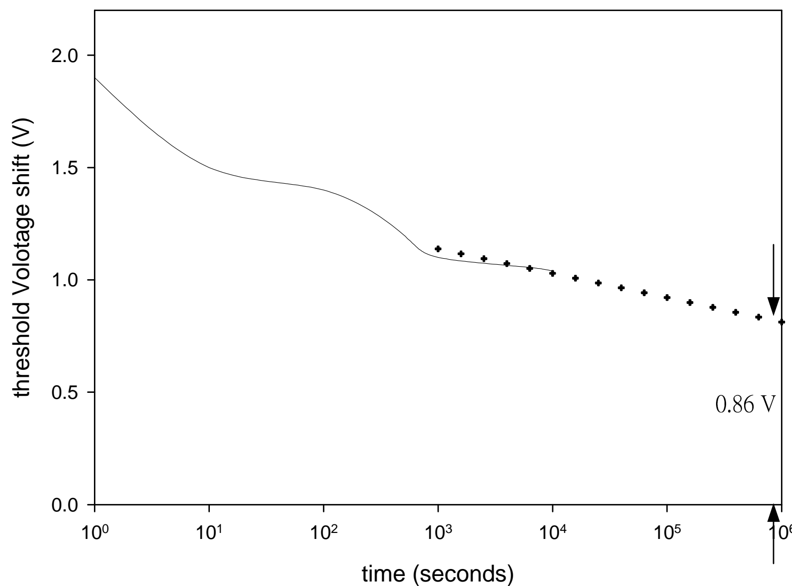


Figure A-11 The charge retention characteristic of memory which was based on Co-SiO_2 co-sputtered film.

A.4 Summary and future development

Cobalt nanocrystals embedded in SiO_2 or Si_3N_4 layer has been fabricated by using co-sputtered pure Co metal target and SiO_2 or Si_3N_4 physically target with appropriate control of the process temperature and oxidative time. We could observe that the cobalt reacts with oxygen easily make cobalt oxide during oxidation process. When quantities of metal element were too many to form nanocrystals, oxidation process will reduce amount of pure cobalt element. When the sample was reduced amount of pure cobalt element, the cobalt-cobalt oxide nanocrystals were well formed. The ease Co nanocrystals formation technology is also demonstrated by co-sputtering Co target and SiO_2/Si_3N_4 target after thermal oxidation. In this thesis, we annealed the sample in O_2 to reduce amount of pure cobalt element. Why didn't we directly reduce quantities of metal element during sputtering? We have no time and there are no measuring thick tools on the sputtering system. Taking into account the fact that the experiment was carried out under adverse condition, the results were reasonably reliable. Because of those, we encounter difficulties when we were sputtering. We were obliged to abandon the plan. There is still room for the study on the Co nanocrystals formation technology.

A.5 Future development

We know that there is still room for the study on the Co nanocrystals formation technology and the cobalt reacts with oxygen easily make cobalt oxide during oxidation process. We could take a similar view. Cobalt nanocrystals embedded in SiO_2 or Si_3N_4 layer can be fabricated by using co-sputtered pure Co metal target and SiO_2 or Si_3N_4 physically target with appropriate control of the process temperature. What difference does it make? Oxidation of the process is

canceled as it would reduce pure cobalt element.

Addendum B

Observations of metal Co-Al_2O_3 co-sputtering and future development

B.1 Motivation

In previous sections, we have discussed the electrical characteristics of cobalt nanocrystals embedded in silicon oxide or silicon nitride film and we look some papers about high-k material [B-1] [B-2]. We could know that Al_2O_3 is high-k material from reference [B-1]. Besides, we also know that barrier height between SiO_2 and Al_2O_3 is not high, about 0.7 eV, but the trap level is very deep form reference [B-3], therefore we chosen Al_2O_3 as high-k material we study and expected that the material show the lowest charge loss. We will focus on Co-Al_2O_3 co-sputtered film and discuss the future development about this material for memory devices. We will observe this material of the effect on trapping charge and we investigate the physics mechanism of these phenomena preliminarily.

B.2 Experiment Procedures

Fig. B-1 indicates a schematic of experimental procedures. This nonvolatile memory-cell structure in this letter was fabricated on a 4 inch p-type silicon (100) wafer. First, single-crystal 4 inch p-type silicon (100) wafers were chemically cleaned by standard RCA cleaning. The wafers were followed by a thermal oxidative process to form about 5-nm-thick dry SiO_2 layer as a tunnel oxide in an atmospheric pressure chemical vapor deposition (APCVD), we also call it Dry-Oxide-system furnace. After the growth of tunnel oxide we measure the thick with N-K 1200 and its thick was

about 4.5~5.6 nm. The co-sputtered film Co-Al_2O_3 was deposited onto the tunnel oxide sputtering system the following step. Among the deposition, the pure Co target sputtered by a DC gun of 100W power and the Al_2O_3 target by RF gun of 150W power simultaneously during 2 minutes. The co-sputtered film of cobalt and aluminum oxide was deposited onto the tunnel oxide by sputtering system. The co-sputtered film was deposited at room temperature with 4.5mtorr pressure of the chamber which was full argon. The basic principle of Al_2O_3 sputtering machine is sputter Al_2O_3 sample into particles by Ar particles.

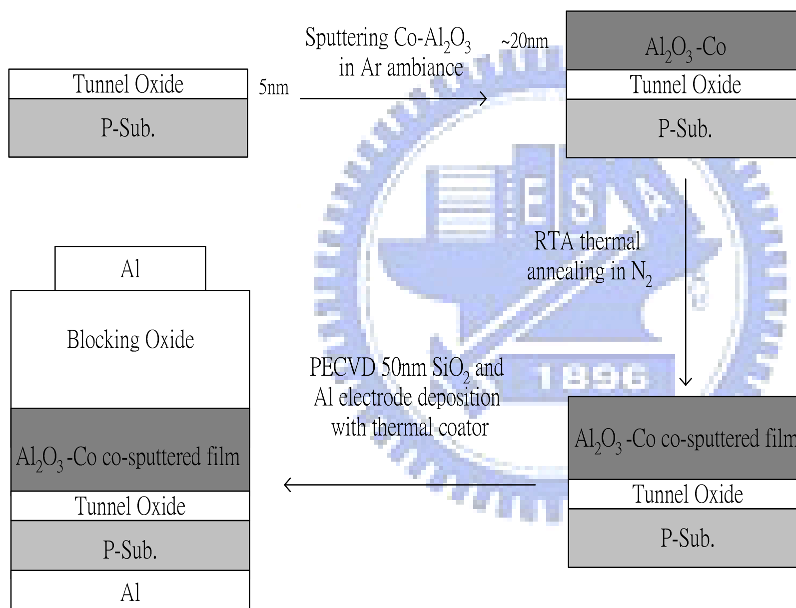


Figure B-1 The process flow of the structure with Al_2O_3-Co co-sputtered film.

Next step, we annealed the samples with rapid thermal annealing (RTA) system for 30s~90s in N_2 ambient that temperatures was about 550°C~750°C. During the annealing process cobalt elements had accumulated to form cobalt oxide or cobalt nanowires which were surrounded by cobalt oxide- aluminum oxide.

Subsequently, a50nm SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) system and was control oxide. Finally, the Al gate was

evaporated to form thin film as Al gate electrode with thermal evaporation coater and the samples will form metal/oxide/silicon (MOS) structure. This MOS capacitance structure was prepared for material and electrical analyses.

B.3 Results and Discussion

The charge storage layer embedded in dielectrics layer of metal-oxide–insulator -oxide silicon (MOIOS) memory device was utilized to capture the injected carriers from the channel, which caused a variation in the threshold voltage of the memory device. The charge storage effects in these memory structures were measured using capacitance-voltage techniques in these co-sputtered film structures. Fig. B-2 show the forward and reverse capacitance-voltage (*C-V*) curves for as-deposited samples obtained when the gate voltage was first swept from –7V to +7V (accumulation to inversion, forward sweep) and then from +7V to –7V (inversion to accumulation, reverse sweep) for Co-Al_2O_3 co-sputtered based MIS structure. The bidirectional *C-V* sweeps were performed from deep inversion to deep accumulation and in reverse, which exhibited an electron charging effect. We could observed that the memory window is about 3V (ΔV_{th}=3V) and 1.8V (ΔV_{th}=1.8V) after the sample was annealed at high temperature and the charge storage effects in these memory structures were a large number. Based on the illustrative band diagram shown in Fig. B-3, when the applied voltage is sufficiently high, Fowler-Nordheim (FN) tunneling of electrons from Si substrate to the charge storage layer I_1 and that from the charge storage layer to gate I_2 could occur simultaneously. Electrons were trapped in the charge storage layer with positive applied voltage at metal gate during programming. On the contrary, the holes might tunnel from the valence band of the Si substrate and recombined with the electrons trapped in the charge storage layer, or the electrons tunnel back to the Si

substrate from the charge storage layer during erasing operation.

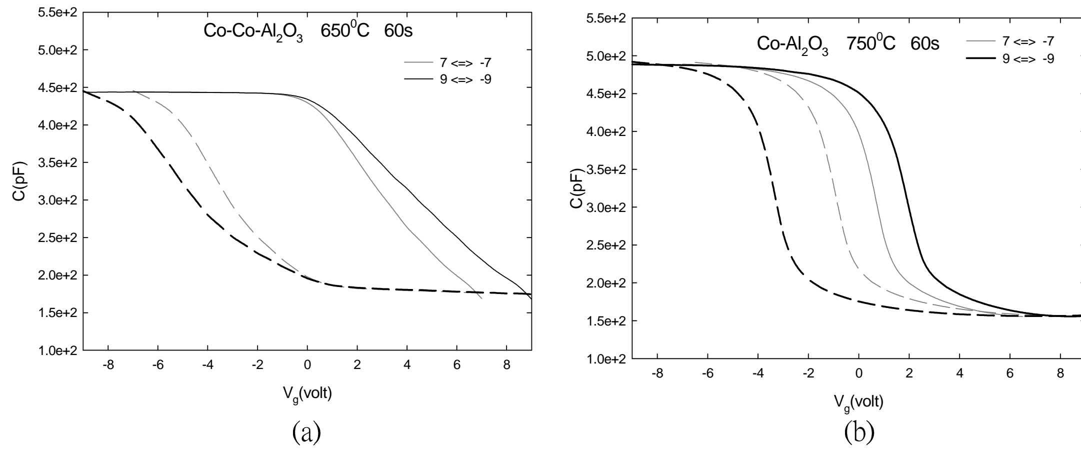


Figure B-2 The C-V characteristics of Al/SiO_2/ "The charge storage layer"/ SiO_2/Si-based as MIS structure, showing hysteresis of as-deposited and after PTA at 650 °C and 750 °C measured. The curves were obtained by gate voltage sweeping from forward to reverse and back.

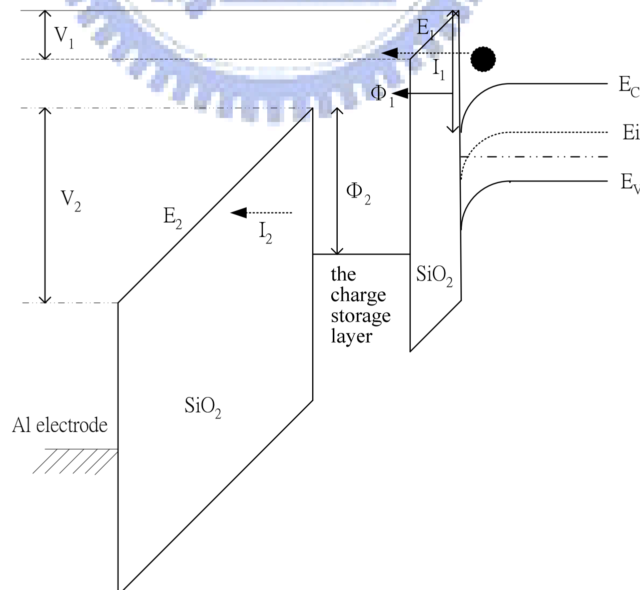
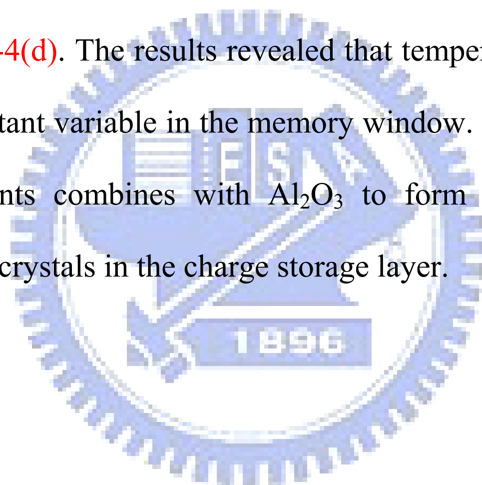


Figure B-3 The illustrative band diagram of a MIS structure (Al/SiO_2/ "The charge storage layer"/ SiO_2/Si) with positive applied

voltage at metal gate.

We could observe that different temperature and time conditions play important roles in generating the asymmetrical change in the memory window from Fig. B-4. It was showed the C-V hysteresis of this structure with two different conditions in temperature and two different time conditions in every temperature condition. We could observe that smaller memory window under ±7V *C-V* sweeping was obtained on Fig. B-4(a) and Fig. B-4(c). As RTP time was longer, the threshold-voltage shifts were increasing and memory window was 7V and 4V under ±7V, It was shown on the Fig. B-4(b) and Fig. B-4(d). The results revealed that temperature and annealing time appears to be an important variable in the memory window. It is considered that there were some Co elements combines with Al_2O_3 to form chemical compounds or agglomeration to form crystals in the charge storage layer.



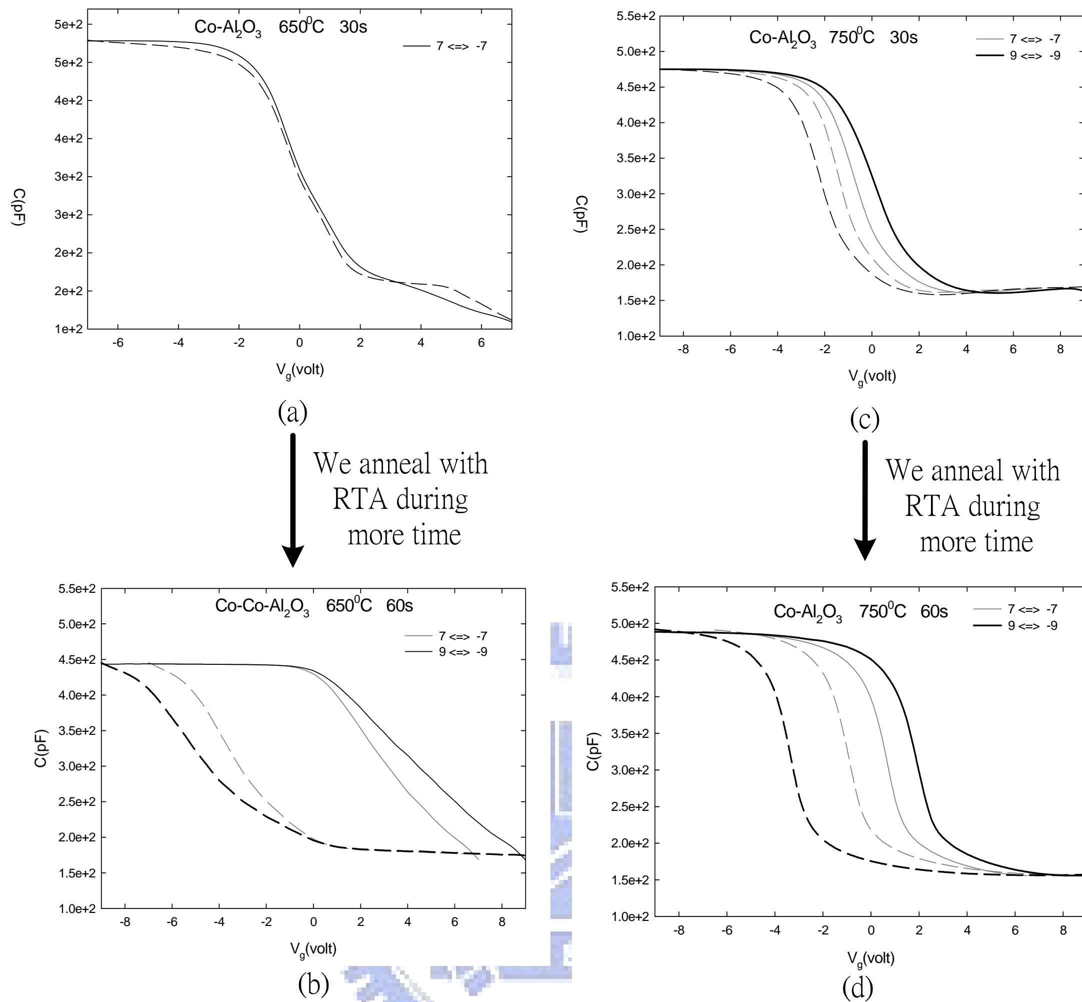


Figure B-4 The C-V characteristics of Al/SiO_2/ "The charge storage layer"/ SiO_2/Si-based as MIS structure, showing hysteresis of as-deposited and after PTA at 650 ˚C and 750 ˚C measured during different time. The curves were obtained by gate voltage sweeping from forward to reverse and back.

The memory effect was observed from the hysteresis capacitance-voltage (*C-V*) characteristics of MIS capacitors embedded with the charge storage layer. According to the theoretical derivation [B-4], i.e. $Q= -V_{fb}C_{control}$, the total charges trapped in the capacitor can be approximately estimated and the results are shown in Fig. B-5. We could observe that the value of trapped electrons or holes in Co-Si_3N_4 co-sputtered

film is lower than that in Co-Al_2O_3 co-sputtered film. This diagram tells us that the Co-Al_2O_3 co-sputtered film as the charge storage layer is a very good material for memory devices.

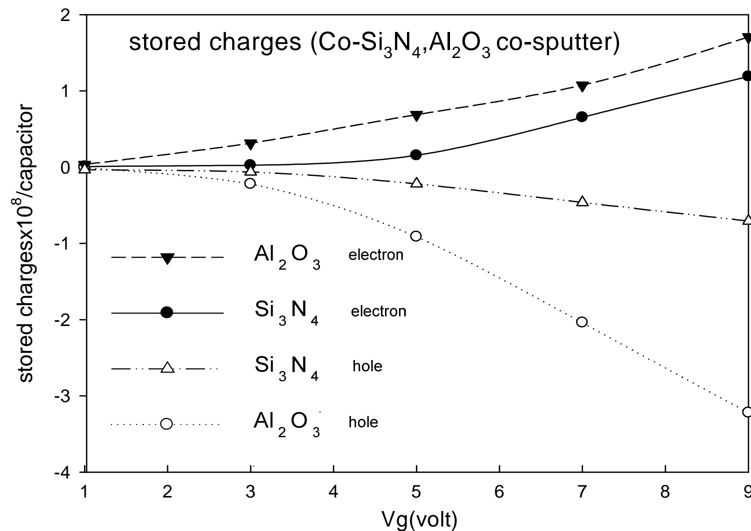
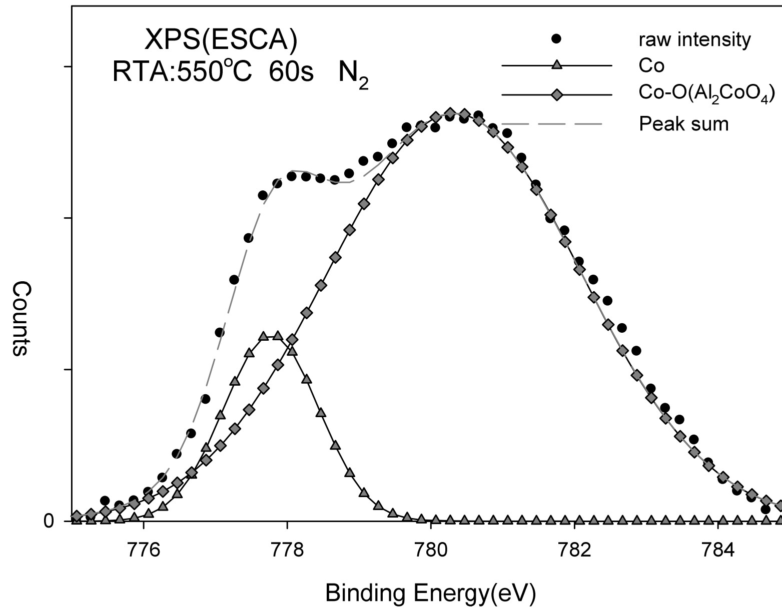


Figure B-5 The relations between gate voltage and flatband voltage, stored charges in a MIS capacitor. The insets in this figure the high frequency *C-V* relations of MIS capacitors co-sputtered to form the charge storage film with metal Co embedded in the Al_2O_3 and Si_3N_4 respectively.

What did the Co-Al_2O_3 co-sputtered film happened during the RTA process? We were so interested in that. XPS, also called ESCA, is an effective and widely used surface analysis technique and therefore we analyzed the material in Co-Al_2O_3 co-sputtered film with XPS. Fig. B-6 showed that there are chemical bonds of Co-Co, Co-O and Al-O in the Co-Al_2O_3 co-sputtered film after annealing in N_2 ambiance [B-5] [B-6]. Because of them, we considered that cobalt may react with aluminum oxide during annealing to make aluminate spinels. The $Co_xAl_yO_z$ is an aluminum transition metals oxide which falls into the category of aluminate spinels [B-7] [B-8]. Further research on XRD material analysis would clarity what binding energy exist in this material is.



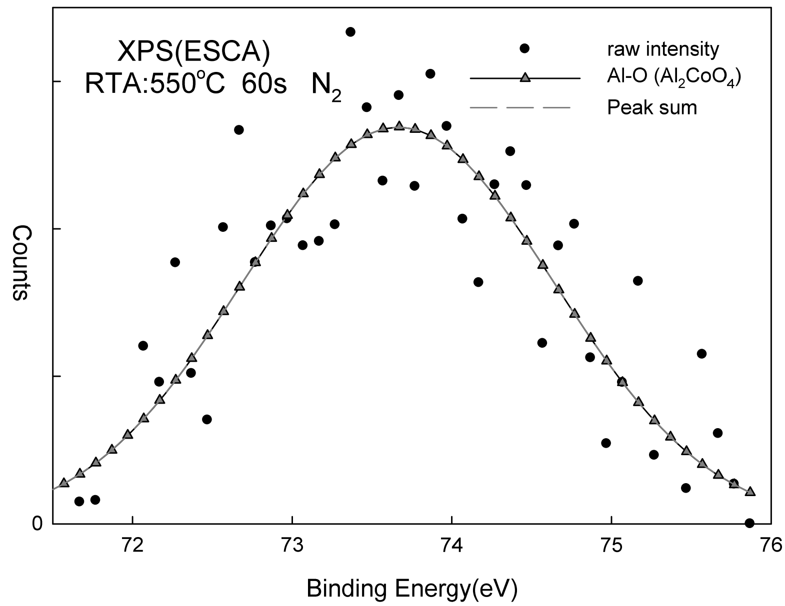


Figure B-6 The XPS (ESCA) spectra of Co-O and Al-O peaks in Co-Al_2O_3 co-sputtered film after RTA annealing in N_2 ambiance. We could know that is Co_xO_y-Al_zO_w mixture clearly.

Fig. B-7 showed the Transmission Electron Microscope (TEM) image of the $Co\text{-}Al_2O_3$ co-sputtered film. We could observe that cobalt come into being Discontinuous grains after annealing and the annealed film shows a strong contrast of Co grains and the remanent $(Co_xAl_{1-x})_zO_{3-v}$ matrix [B-9]. The average width of the Co grains is about 2–3 nm and the average length of the Co grains is about 10 nm to 20nm. It is quite likely that annealing temperature and time determine the chemical reaction in the $Co\text{-}Al_2O_3$ co-sputtered film and this chemical reaction made cobalt grains discontinuous. When we annealed during shorter time with RTA system, the memory window will be smaller. The memory effect was the sum of contributions from the charge trapping. When we annealed during shorter time, metal cobalt element had not been discontinuous grains and amount of cobalt element was too large to trap charges. We could observe this phenomenon from Fig. B-4 (a) and Fig. B-4 (c). When we annealed during longer time with RTA system, the memory window will be larger. The memory effect was the sum of contributions from the charge trapping. Therefore, it seems reasonable to conclude that metal cobalt element will be shown in discontinuous grains form and amount of pure metal cobalt element reduce after we annealed during longer time. The charges are stored in distributed grains and trapping centers of the $Co_{rich}\text{-}(Co_xAl_{1-x})_zO_{3-v}$ film. We could observe this phenomenon from Fig. B-4 (b) and Fig. B-4 (d).

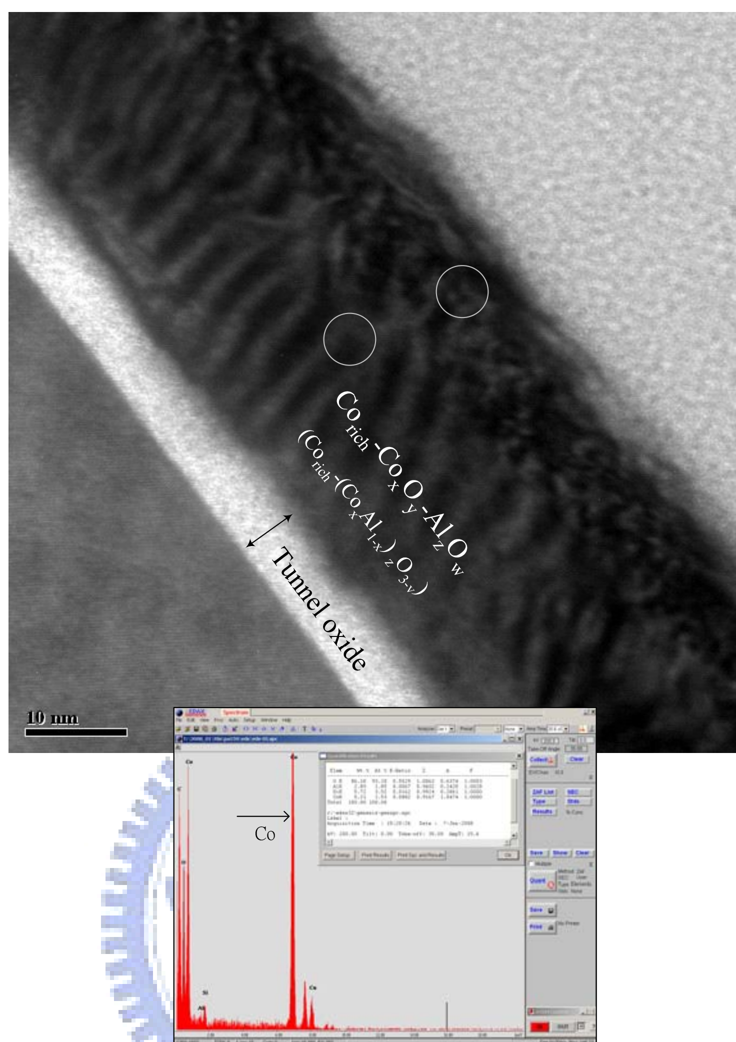


Figure B-7 The TEM image of Co-Al_2O_3 co-sputtered film and its EDX.

The current density-voltage (J-V) characteristics of the memory which is based on Co-Al_2O_3 co-sputtered film. It is shown in Fig. B-8. We could know that the leakage current exhibited a nearly result about from 10^{-8} order to 10^{-9} order after annealing during 60 seconds. The endurance characteristics of the MOIOS with Co discontinuous grains embedded in the $(Co_xAl_{1-x})_zO_{3-v}$ are illustrated in Fig. B-9. Pulses (V_G=±5V) were applied to evaluate endurance characteristics for the Program/Erase operation. The schematic plots indicated the memory windows can be

retain as their initial values after 10^6 program/erase cycles at room temperature.

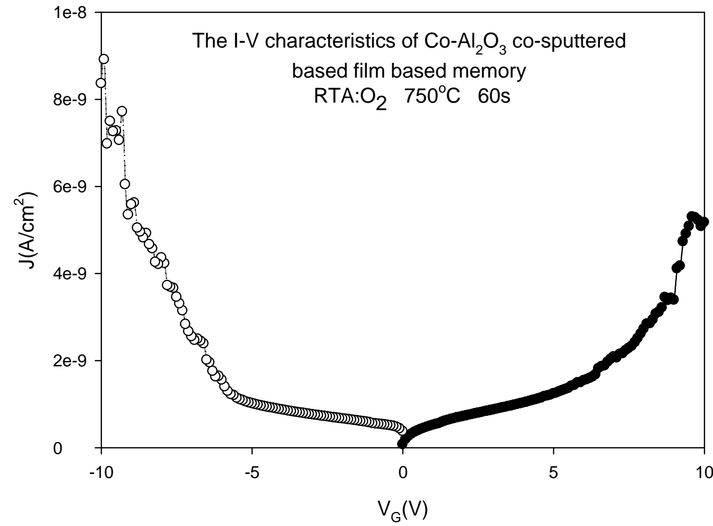


Figure B-8 The *I-V* characteristics of the memory which is based on Co-Al_2O_3 co-sputtered film with 750°C annealing process during 60 seconds.

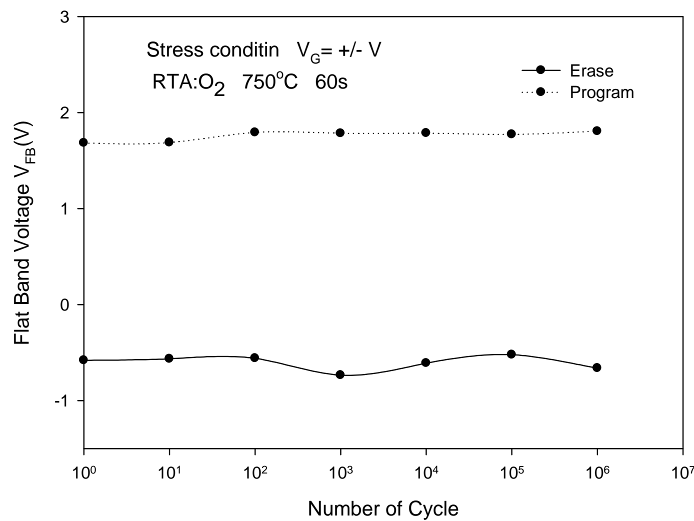


Figure B-9 The endurance of the memory which is based on Co-Al_2O_3 co-sputtered film.

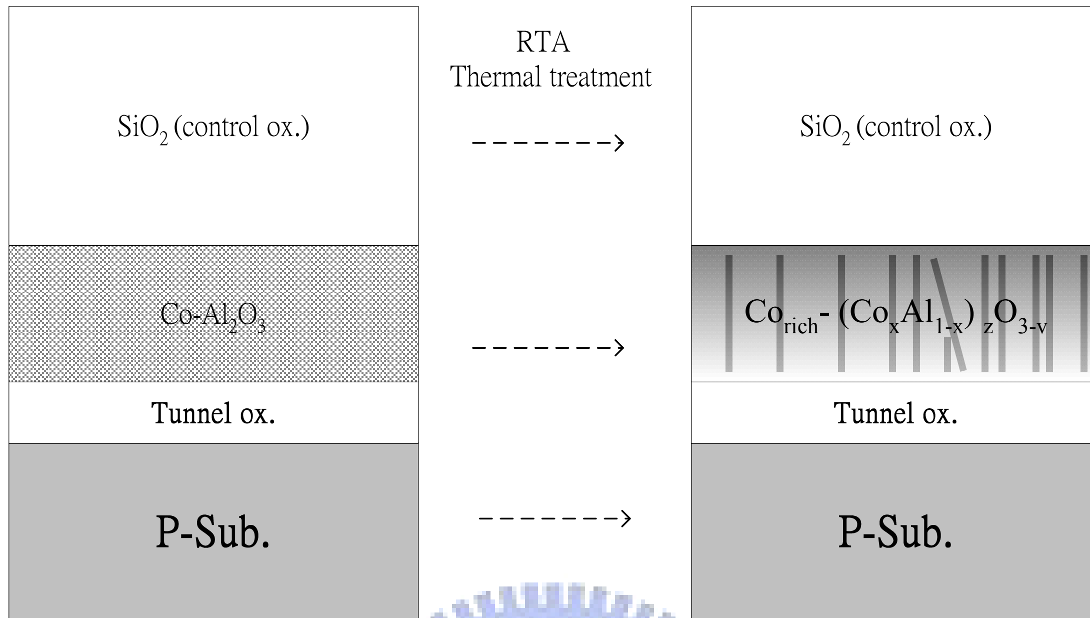
B.4 Summary

From the XPS (ESCA) schematic plots and TEM image, these results lead us to the conclusions that the containments of samples changed during annealing treatment.

The Co_{rich}-Co_xO_y-Al_zO_w (Co_{rich}- $(Co_xAl_{1-x})_zO_{3-v}$) film is very nice material to trap charges. There are numerous trapping center of the charge, one of them is discontinuous grain and one of them is the trap level of the $(Co_xAl_{1-x})_zO_{3-v}$ such as Al_2O_3 film. Those seem reasonable to conclude that metal cobalt element will be shown in discontinuous grain form and amount of pure metal cobalt element reduce after we annealed during longer time. The charges are stored in distributed discontinuous grain and trapping centers of the Co_{rich}-$(Co_xAl_{1-x})_zO_{3-v}$ film.

B.5 Future development

In the future, we could chose this material (Co_{rich}- $(Co_xAl_{1-x})_zO_{3-v}$) to fabricate the memory which is based on discontinuous grain and material $(Co_xAl_{1-x})_zO_{3-v}$ to fabricate SONOS structure memory with co-sputtering deposition film process such as reference [B-1]. Those are showed in Fig. B-10. Further research on X-ray diffraction analysis (XRD) material analysis or other would clarity what kind of this material is. There is still room for research in $(Co_xAl_{1-x})_zO_{3-v}$–based memory. Taking into account the face that the experiment was carried out under adverse conditions, the results were reasonably reliable.



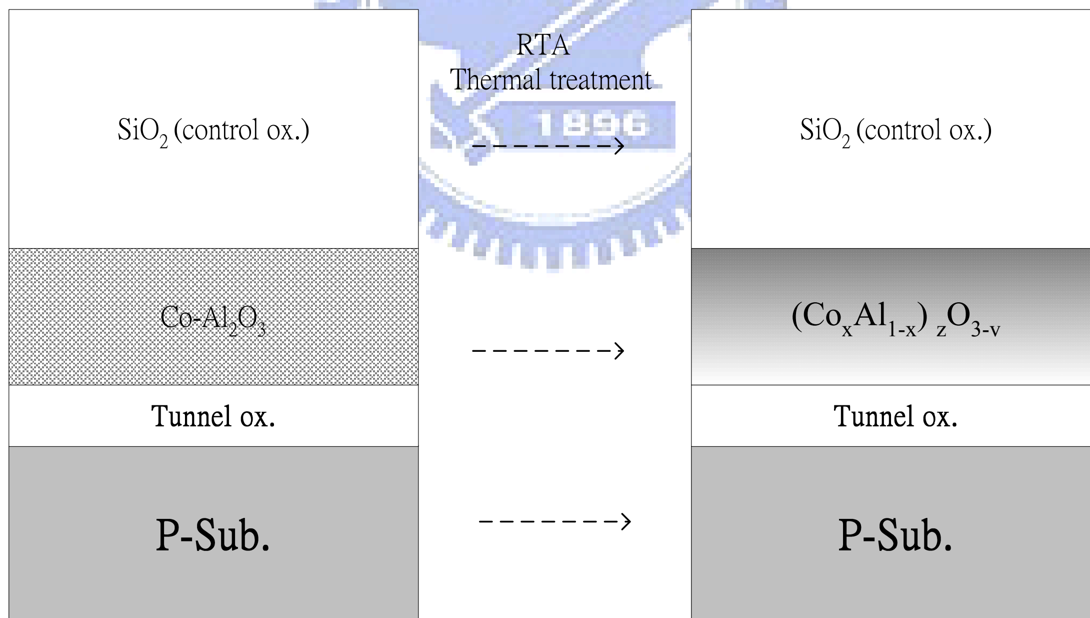


Figure B-10 (a) The discontinuous grain memory with material (Co_{rich}- $(Co_xAl_{1-x})_zO_{3-v}$) and (b) the SONOS structure memory with material $(Co_xAl_{1-x})_zO_{3-v}$

References

CHAPTER 1

[1-1] Simon M. Sze, Kwok K. Ng, s
"Physics of Semiconductor Device"
Wiley, New York

[1-2] Kahng, K. Sze, S.M.
"A floating gate and its application to memory devices "
1967

[1-3] Jong Jin Lee Xuguang Wang Weiping Bai Nan Lu Dim-Lee Kwong
"Theoretical and experimental investigation of Si nanocrystal memory device with HfO2 high-k tunneling dielectric" IEEE Trans. Electron Devices 50, 2067 2003

[1-4] M. H. White, Y. Yang, A. Purwar, and M. L. French
"A low voltage SONOS nonvolatile semiconductor memory technology"
IEEE Int'l Nonvolatile Memory Technology Conference, 52 1996

[1-5] M. H. White, D. A. Adams, and J. Bu
"On the go with SONOS"
IEEE circuits & devices, 16, 22 2000

[1-6] H. E. Maes, J. Witters, and G. Groeseneken
"17th European Solid State Devices Research Conference"
p. 157 1988

[1-7] S. Tiwari, F. Rana, K. Chan, H. Hanafi, C. Wei, and D. Buchanan
"Volatile and non-volatile memories in silicon with nano-crystal storage"
IEEE Int. Electron Devices Meeting Tech. Dig., 521 1995

[1-8] J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, and Y. Lee
"Room temperature operation of a quantum-dot flash memory"
IEEE Electron Device Lett., 18, 27 8 1997

[1-9] Y. C. King, T. J. King, and C. Hu
"MOS memory using germanium nanocrystals formed by thermal oxidation of Si1-xGex"
IEEE Int. Electron Devices Meeting Tech. Dig., 115 1998

[1-10] Frohman-Bentchkowsky, D.
"A fully decoded 2048-bit electrically programmable FAMOS read-only memory"
Solid-State Circuits, IEEE Journal of 1971

[1-11] Iizuka, H. Masuoka, F. Tai Sato Ishikawa, M.
"Electrically alterable avalanche-injection-type MOS READ-ONLY memory with stacked-gate structure"
Electron Devices, IEEE Transactions on 1976

[1-12] A. Scheibe , Heinz Schulte
"Technology of a new n-channel one-transistor EAROM cell called SIMOS"
Electron Devices, IEEE Transactions on 1977

[1-13] Wegener, H A R; Lincoln, A J; Pao, H C; O' Connell, M R; Oleksiak, R E; Lawrence, H
"The variable-threshold transistor, a new electrically-alterable, nondestructive READ-only storage device"
IEEE Transactions on Electron Devices. Vol. 15, no. 6, pp. 420-421 1968 presented at the Internaional Electron Devices Meeting 1967

[1-14] T. Y. Chan, K. K. Young, and C. Hu
"A true single-transistor oxide–nitride–oxide EEPROM device"
IEEE Electron Device Lett., vol EDL-8, pp. 93–95 Mar. 1987

[1-15] M. White, Y. Yang, P. Ansha, and M. L. French
"A low voltage SONOS nonvolatile semiconductor memory technology"
IEEE Trans. Compon,Packag., Manufactur. Technol., vol. 20, pp. 190–195 Jun. 1997

[1-16] M. K. Cho and D. M. Kim
"High performance SONOS memory cells free of drain turn-on and over-erase: Compatibility issue with current flash technology"

IEEE Electron Device Lett., vol. 21, pp. 399–401 Aug. 2000

[1-17] I. Fijiwara, H. Aozasa, K. Nomoto, S. Tanaka, and T. Kobayashi
"High speed program/erase sub 100 nm MONOS memory cell "
in Proc. 18th Non-Volatile Semiconductor Memory Workshop, pp. 75–75 2001

[1-18] Y Yang, A Purwar, MH White
"Reliability considerations in scaled SONOS nonvolatile memory devices"
Solid State Electronics 1999

[1-19] H. E. Maes, J. Witters, and G. Groeseneken
"in Proceedings of the 17th European Solid State Devices Reseach Conference"
Bologna, Italy, 1987, p. 157 1988

[1-20] S. Tiwari, F. Rana, K. Chan, H. Hanafi, C. Wei, and D. Buchanan
"Volatile and non-volatile memories in silicon with nanocrystal storage"
IEEE Int. Electron Devices Meeting Tech. Dig., 521 1995

[1-21] Suk-Kang Sung
"Program/Erase Characteristics of Nanoscale SONOS Memory and Feasibility of Multi-Level Operation in Multi-Layer SONOS"
SMDL Annual Report 2003

[1-22] F Rana, K Chan, H Hanafi, W Chan, D Buchanan
"Volatile and Non-Volatile Memories in Silicon with Nano-Crystal Storage"
IEDM Tech. Dig. p.521 1995

[1-23] Sandip Tiwari, Farhan Rana, Hussein Hanafi, Allan Hartstein, Emmanuel F. Crabbe,Kevin Chan
"A silicon nanocrystals based memory"
Appl. Phys. Lett. 68, pp1377 1996

[1-24] J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, and Y. Lee
"Room temperature operation of a quantum-dot flash memory"
IEEE Electron Device Letters., vol.18, pp. 278-280 1997

[1-25] Sugizaki, T. Kobayashi, M. Ishidao, M. Minakata, H. Yamaguchi, M. Tamura, Y. Sugiyama, Y. Nakanishi, T. Tanaka, H.

"Novel Multi-bit SONOS Type Flash Memory Using a High-k Charge Trapping Layer"
Symposium on VLSl Technology Digest of Technical Papers 2003

[1-26] T. C. Chang, S. T. Yan, P. T. Liu, C. H. Hsu, M. T. Tang , and S. M. Sze
"A novel distributed charge storage with GeO2 nano-dots"
Appl. Phys. Lett, 84(14), p.2581 2004

[1-27] Froment, B. Muller, M. Brut, H. Pantel, R. Carron, V. Achard, H. Halimaoui, A. Boeuf, F. and Wacquant, F
"Nickel vs. cobalt silicide integration for sub-50nm CMOS"
European Solid-State Device Research, p.215 2003

[1-28] Wang, L. Bridgman, B. Klein, G. Liying Wu, Darilek, J.
"Study of junction leakage caused by cobalt silicide defects"
SMTWP., pp. 201-203 2004

[1-29] Wein-Town Sun, Ming-Chi Liaw, and Hsu, C.C.-H.
"Suppression of cobalt silicide agglomeration using nitrogen (N2+) implantation"
Electron Device Letters, IEEE, vol. 19, NO. 5 1995

[1-30] Sarcona, G.T. Stewart, M. and Hatalis, M.K.
"Polysilicon thin-film transistors using self-aligned cobalt and nickel silicide source and drain contacts"
Electron Device Letters, IEEE, vol. 20, NO. 7 1999

[1-31] Zengtao Liu, Chungho Lee, Venkat Narayanan, Gen Pei, and Edwin Chihchuan Kan, Member, IEEE
" Metal Nanocrystal Memories—Part II: Electrical Characteristics"
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 49, NO. 9, SEPTEMBER 2002

[1-32] A. Alberti, F. La Via, M.G. Grimaldi, S. Ravesi.
"Cobalt silicide thermal stability: from blanket thin flm to submicrometer lines"
Solid-State Electronics 43 1039±1044, 1999

[1-33] F. M. Yang, T. C. Chang, P. T. Liu, P. H. Yeh_ and U. S. Chen, Y. C. Yu and J. Y. Lin, S. M. Sze and J. C. Lou
"Using double layer CoSi2 nanocrystals to improve the memory effects of nonvolatile memory devices"
Appl. Phys. Lett 90, 212108,2007

[1-34] Jae-Duk Lee; Sung-Hoi Hur; Jung-Dal Choi;
" Effects of floating-gate interference on NAND flash memory cell operation "
Electron Device Letters, IEEE Volume 23, Issue 5, May 2002 Page(s):264 - 266

[1-35] B. Govoreanu, D.P. Brunco and J. Van Houdt
" Scaling down the interpoly dielectric for next generation Flash memory: Challenges and opportunities "
Solid-State Electronics
Volume 49, Issue 11, November 2005, Pages 1841-1848

[1-36] F Rana, K Chan, H Hanafi, W Chan, D Buchanan.
" Volatile and Non-Volatile Memories in Silicon with Nano-Crystal Storage "
Int'l Electron Devices Meeting: Technical Digest, Washington …, 1995

[1-37] S Tiwari, F Rana, K Chan, L Shi, H Hanafi
" Single charge and confinement effects in nano-crystal memories "
Appl. Phys. Lett. 69, 1232 (1996); DOI:10.1063/1.117421

[1-38] J. H. Chen , Y. Q. Wang , W. J. Yoo , Y.-C. Yeo , G. Samudra , D. S. H. Chan , A. Y. Du and D.-L. Kwong
"Nonvolatile flash memory device using Ge nanocrystals embedded in HfAlO high-k "
Devices, vol. 51, pp. 1840, Nov. ,2004

[1-39] CH Tu, TC Chang, PT Liu, HC Liu, SM Sze, CY Chang
" Improved memory window for Ge nanocrystals embedded in SiON layer "
Appl. Phys. Lett. 89, 162105 ,2006; DOI:10.1063/1.2362972

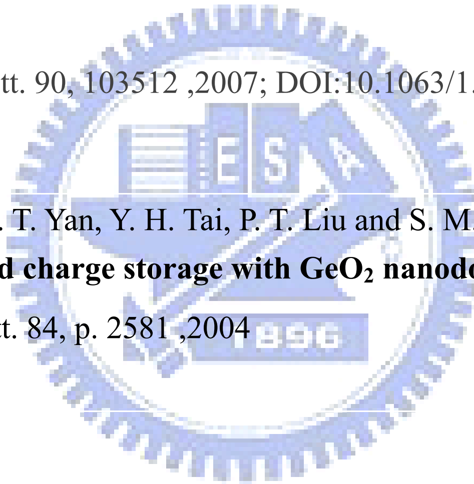
[1-40] M. Hocevar, P. Regreny, A. Descamps, D. Albertini, G. Saint-Girons, A. Souifi, M. Gendry, and G. Patriarche.
" InAs nanocrystals on SiO_2/Si by molecular beam epitaxy for memory applications "

Appl. Phys. Lett. 91, 133114 ,2007; DOI:10.1063/1.2793694

[1-41] YK Cha, S Park, Y Park, IK Yoo, D Cha, JH Shin, SH
" Effect of hydrogenation on the memory properties of Si nanocrystals obtained by inductively coupled plasma chemical vapor deposition "
Appl. Phys. Lett. 89, 202112 ,2006; DOI:10.1063/1.2388144

[1-42] Yu-Hsien Lin Chao-Hsin Chien Ching-Tzung Lin Ching-Wei Chen Chun-Yen Chang Tan-Fu Lei
" High performance multi-bit nonvolatile HfO/sub 2/ nanocrystal memory using spinodal phase separation of hafnium silicate "
IEEE Int. Electron Devices Meeting Tech. Dig., p. 1080 ,2004

[1-43] J. Sarkar, S. Tang, D. Shahrjerdi, and S. K. Banerjee
" Vertical flash memory with protein-mediated assembly of nanocrystal floating gate"
Appl. Phys. Lett. 90, 103512 ,2007; DOI:10.1063/1.2711528



[1-44] T. C. Chang, S. T. Yan, Y. H. Tai, P. T. Liu and S. M. Sze
" A distributed charge storage with GeO_2 nanodots "
Appl. Phys.Lett. 84, p. 2581 ,2004

CHAPTER 2

[2-1] L. Selmi and C. Fiegna
"Physical aspects of cell operation and reliability"
in Flash Memories, P. Cappelletti et al., Ed. Norwell, MA:Kluwer
1999

[2-2] J. Bu, M. H. White
"Design considerations in scaled. SONOS nonvolatile memory devices"
Solid-State Electronics., vol. 45, pp. 113-120,2004

[2-3] M. L. French, and M. H. White,
"Scaling of multidielectric nonvolatile SONOS memory structures"

Solid-State Electron., vol. 37, pp.1913-1923,1995

[2-4] M. L. French, C. Y. Chen, H. Sathianathan, and M. H. White
"Design and scaling of a SONOS multidielectric device for nonvolatile memory applications"
IEEE Trans. Comp. Pack and Manu Tech part A., vol. 17, pp. 390-397,1994

[2-5] B. Eitan and D. Frohman
"Hot-electron injection into the oxide in n-channel MOS devices"
IEEE Trans. Electron Devices, vol. ED–28 pp. 328–340, ,1981

[2-6] P. Pavan, R. Bez, P. Olivo, and E. Zanoni
"Flash memory cells—An overview"
Proc. IEEE, vol. 85, pp. 1248–1271,1997

[2-7] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi
"NROM: A novel localized trapping, 2bit nonvolatile memory cell"
IEEE Electron Device Lett., vol. 21, pp. 543–545,2000

[2-8] "Proc. SSDM 99, Tokyo, Japan, pp. 522–524.,1999

[2-9] P. E. Cottrell, R. R. Troutman, T. H. Ning
"Hot-electron emission in n-channel IGFET's"
IEEE Journal of Solid-State Circuits, vol. 14, pp. 442-455,1979

[2-10] A. Voros
"Wentzel-Kramers-Brillouin method in the Bargmann representation"
The American Physical Society,1989

[2-11] M. Lenzlinger and E.H. Snow
"Fowler-Nordheim Tunneling into Thermally Grown SiO2"
J. Appl. Phys., vol.40, p.278,1969

[2-12] Y. S. Hisamune, K. Kanamori, T. Kubota, Y. Suzuki, M. Tsukiji, E. Hasegawa,A. Ishitani, and T. Okazawa,
"A high capacitive-coupling ratio (HiCR) cell for3V-only 64Mb and future flash memories"
IEDM Tech. Dig., pp.19-22,1993

[2-13] K. P.Johansson, A. P. Marchetti, G. B. McLendon
"However, for studies of indirect AgBr"
J. Phys. Chem. 96, 2873,1992

[2-14] JP Proot, C Delerue, G Allan
"Electronic structure and optical properties of silicon crystallites: Application to porous silicon"
Appl. Phys. Lett. 61 1948,1992

[2-15] T Takagahara, K Takeda
"Theory of the quantum confinement effect on excitons in quantum dots of indirect-gap materials"
Physical Review B. 46. 15578 ,1992

[2-16] MS Hybertsen, Mater. Res. Soc. Proc. 256, 179 ,1992

[2-17] Gorter, C.J.
"A possible explanation of the increase of the electrical resistance of thin metal films at low temperatures and small field strengths"
17, 777 (1951) Aug 01

I. Giaever and H. R. Zeller
"Superconductivity of Small Tin Particles Measured by Tunneling"
Phys. Rev. Lett. 20, 1504 – 1507,1968

CHAPTER 4

[4-1] P. T. Goeller, B. I. Boyanov, D. E. Sayers and R. J. Nemanich
"Structure and stability of cobalt-silicon-germanium thin films"
Nuclear Instruments and Methods in Physics Research B. 133, p. 84-89 ,1997

[4-2] K. Prabhakaran, K. Sumitomo and T. Ogino
"Oxidation of cobalt pre-reacted SiGe epilayer grown on Si(100) "
Surface Science, Volume 429, Number 1, 15 June 1999 , pp. 274- 278(5)

[4-3] K. Prabhakaran and T. Ogino
"Oxidation behavior of cobalt silicide and cobalt germanide thin films "
Applied Surface Science Volumes 121-122, 2 November 1997, Pages 213-217
Iketani-6

[4-4] Han-Joo Kim, Soo-Gil Park
"Development of aqueous polymeric gel electrolyte for Pseudo capacitor "
San 48, Kaeshindong, Heungdukgu, Cheongju, Chungbuk 361-763, Korea

[4-5] Chen-Chan Wang, Jyun-Yi Wu, Yan-Kai Chiou, Che-Hao Chang, and Tai-Bor Wu
"Charge storage characteristics of Au nanocrystals embedded in high-k gate dielectrics on Si"
Appl. Phys. Lett S 91, 202110 2007

[4-6] M. K. Bera, S. Chakraborty, and R. Das,G. K. Dalapati and S. Chattopadhyay ,S. K. Samanta and W. J. Yoo,A. K. Chakraborty,Y. Butenko and L. Šiller,M. R. C. Hunt,S. Saha,C. K. Maiti
"Rapid thermal oxidation of Ge-rich $Si_{1-x}Ge_x$ heterolayers"
J.Vac. Sci. Technol. A,24(1),pp.1323-1329,2006

[4-7] Steve L. Hsial, Teh Y. Tanl., Patrick L. Smith, and Gary E. McGuire
"Assured Epitaxial CO& Phase Formation on (001) Si-On-Insulator Substrates Using CoSi/Ti Bimetallic Source Materials"
1994 Symposium on VLSl Technology Digest of Technical Papers
0-7803-19212-4/94/ 0 1994 IEEE

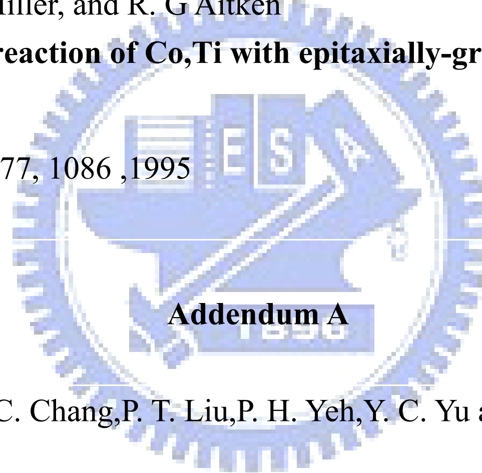
[4-8] Rudolf Zauner and Alan G. Jones
"Determination of nucleation, growth, agglomeration and disruption kinetics from experimental precipitation data: the calcium oxalate system"
Chemical Engineering Science
Volume 55, Issue 19, October 2000, Pages 4219-4232

[4-9] Gong-Ru Lin, Chun-Jung Lin
"Watt Enhanced Electroluminescent Power of Silicon Nanocrystal Light-Emitting Diodes Made on Nano-Scale Silicon-Tip-Array Substrate"
0989-A10-05 Materials Research Society (MRS)

[4-10] G.R. Lin, H.C. Kuo, H.S. Lin, and C.C. Kao
" Rapid self-assembly of Ni nanodots on Si substrate covered by a less-adhesive and heat-accumulated SiO_2 layers "
Appl. Phys. Lett. 89, 073108,2006

[4-11] O. Nur, M. Willander, L. Hultman, H. H. Radamson, G. V. Hansson, M. R. Sardela, Jr., and J. E. Greene
"$CoSi_2/Si_{1-x}Ge_x/Si(001)$ heterostructures formed through different reaction routes: Silicidation-induced strain relaxation, defect formation, and interlayer diffusion "
J. Appl. Phys. 78, 7063 ,1995

[4-12] W. J. Qi, B. Z. Li, W. N. Huang, Z. G. Gu, H. Q. Lu, X. J. Zhang, M. Zhang, G. S. Dong, D. C. Miller, and R. G Aitken
" Solid state reaction of Co,Ti with epitaxially-grown $Si_{1-x}Ge_x$ film on Si(100) substrate "
J. Appl. Phys. 77, 1086 ,1995



Addendum A

[A-1] F. M. Yang,T. C. Chang,P. T. Liu,P. H. Yeh,Y. C. Yu and J. Y. Lin,S. M. Sze and J. C. Lou
"Memory characteristics of Co nanocrystal memory device with HfO2 as blocking oxide"
Appl. Phys. Lett. 90, 132102,2007

[A-2] M. Takata, S. Kondoh, T. Sakaguchi, H. Choi, J. C. Shim, H. Kurino, and M.
"New nonvolatile memory with extremely high density metal nano-dots"
IEDM Tech. Dig., pp. 553–556,2003

[A-3] C. Lee, A. Gorur-Seetharam, and E. C. Kan
"Operational and reliability comparison of discrete-storage nonvolatile memories: Advantages of single- and double-layer metal NCs"
IEDM Tech. Dig., 2003, pp. 557–560,2003

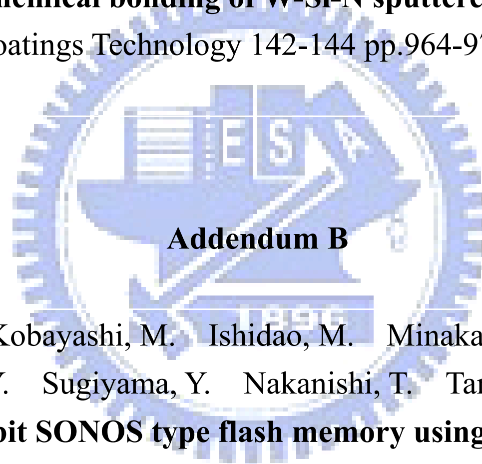
[A-4] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan

"Metal NC memories-Part 1: Device design and fabrication"
IEEE Trans. Electron Devices, vol. 49, pp. 1606–1613,2002

[A-5] Han-Joo Kim, Soo-Gil Park
" Development of aqueous polymeric gel electrolyte for pseudo capacitor"
San 48, Kaeshindong, Heungdukgu, Cheongju, Chungbuk 361-763, Korea

[A-6] Chungho Lee, Jami Meteer, Venkat Narayanan Edwin C. Kan **"Self-assembly of metal nanocrystals on ultrathin oxide for nonvolatile memory applications"**
Journal of Electronic Materials, volume 34. number 1,2005

[A-7] C. Louro, A. Cavaleiro, and F. Montemor,
"How is the chemical bonding of W-Si-N sputtered coatings? "
Surface and Coatings Technology 142-144 pp.964-970,2001



Addendum B

[B-1] Sugizaki, T. Kobayashi, M. Ishidao, M. Minakata, H. Yamaguchi, M. Tamura, Y. Sugiyama, Y. Nakanishi, T. Tanaka, H.
"Novel multi-bit SONOS type flash memory using a high-k charge trapping layer"
VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium on,2003

[B-2] V. A. Gritsenko,K. A. Nasyrov, Yu. N. Novikov, A. L. Aseev, S. Y. Yoon, Jo-Won Lee, E. -H. Lee and C. W. Kim
"A new low voltage fast SONOS memory with high-k dielectric"
Solid-State Electronics Volume 47, Issue 10, Pages 1651-1656 ,Oct. 2003

[B-3] T. Sugizaki, M. Kohayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka
"Novel Multi-bit SONOS Type Flash Memory Using a Highk Charge Trapping Layer"
Symposium on VLSl Technology Digest of Technical Papers,2003

[B-4] Chungho Lee, Jami Meteer, Venkat Narayanan Edwin C. Kan
"Self-assembly of metal nanocrystals on ultrathin oxide for nonvolatile memory applications"
Journal of Electronic Materials, volume 34. number 1,2005

[B-5] Patterson, T. A., Carver, J. C., Leyden Leyden, D. E., Hercules, D. M
"A Surface Study of Cobalt-Molybdena-Alumina Catalysts Using X-Ray Photoelectron Spectroscopy"
Department of Chemistry, University of Georgia, Athens, Georgia 30602 ,1976

[B-6] McIntyre N.S. Cook M.G
"X-Ray Photoelectron Studies on Some Oxides and Hydroxides of Cobalt, Nickel, and Copper"
Anal. Chem. 47, 2208 ,1975

[B-7] T.P. Yadav, N.K. Mukhopadhyay, R.S.Tiwari, O.N.Srivastava
"Synthesis of nanocrystalline (Co,Ni)Al2O4 spinel powder by mechanical milling of quasicrystalline material"
Materials Science. Accepted In JNN,2006

[B-8] Paolo Gazzana, Priaroggia, Piazza S,Ambrogio
"Use of barium copper oxide compounds as high critical temperature (Al2CoO4) "
Related U.S. applicationData,1993

[B-9] Y. F. Tian, Y. P. Zhang, Shi-shen Yan,G. L. Liu, Y. X. Chen, and L. M. Mei,G. Ji and Z. Zhang
"electrical transport properties of (CoXAl1-X)2O3-V oxide magnetic semiconductor and corresponding Co-Al2O3 granlar films"
Appl. Phys. Lett. 91, 013509,2007

Vita

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