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博 士 論 文

先進金氧半場效電晶體閘極工程對

改善元件特性及可靠度之研究

Gate Engineering of Advanced MOSFETs for

Device Performance and Reliability Improvement

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摘　　要

在本論文中，我們針對先進元件的閘極工程整合部分對特性及可靠度的改善進行研究，涵蓋的內容包括淺溝渠隔離(STI)所造成的區域性單向壓縮應力在<110>及<100>通道方向的比較；在(111)晶向基版上利用氮化矽覆蓋層來改善 N 型金氧半場效電晶體的特性；以電漿氮化氧化層或熱氮化氧化層使用在雙閘極氧化層厚度的 P 型金氧半場效電晶體上在負電壓溫度不穩定性及熱載子注入等可靠度之比較，以及元件使用以鉿為基本材料之高介電係數介電層在正電壓溫度不穩定性分析中捕捉/反捕捉電子的可靠度分析。

我們完整地研究了 65 奈米技術的 P 型金氧半場效電晶體在<110>及<100>通道方向上對主動區佈局的相依性以及淺溝渠隔離所造成的單向壓縮應力對其特性的影響。對 65 奈米的 P 型金氧半場效電晶體而言，當源/汲極長度從 0.21 微米增加到 10 微米，<100>通道方向在飽和汲極電流特性方面會比<110>通道的元件高出約從 8 % 提高到 15 ％。再者，我們也證明了對於不管在通道長度或寬度方向來說，<100>通道的元件對硼的擴散有較高的抑制能力以及對淺溝渠隔離所造成的應力也有較低的感受度。

我們亦利用高應力之氮化矽覆蓋層以及非晶矽與多晶矽堆疊之閘極結構等區域應變通道技術在(111)晶向矽基版上製作出 N 型金氧半場效電晶體。當氧化矽覆蓋層或非

晶矽層厚度增加時，元件的飽和電流及轉移電導也隨之上升。我們的實驗結果顯示相對於非晶矽厚度為 20 奈米的元件而言，非晶矽厚度為 70 奈米的元件在飽和電流方面有約 6.7 %的改善；在轉移電導方面則有約 10.2 %的增加。

此外，我們比較了使用電漿氮化氧化層及熱氮化氧化層兩種不同閘極介電層的核心與輸入/輸出之 P 型金氧半場效電晶體受到負電壓溫度不穩定性及熱載子注入等可靠度的影響。以電漿氮化氧化層作為閘極氧化層材料之 P 型金氧半場效電晶體在漂移率方面比熱氮化氧化層元件高了約 30 %，定電壓過驅動電流的值也比熱氮化氧化層高了約 23 %。相較於熱氮化氧化層，電漿氮化氧化層之核心 P 型金氧半場效電晶體因為在氧化層與矽基版界面有較低之氮的濃度，所以有較佳的負電壓溫度不穩定性及熱載子注入抵抗能力。然而，電漿氮化氧化層之輸入/輸出 P 型金氧半場效電晶體則表現出較高的熱載子注入造成的特性退化率因為其有較高的氧化層內的主體缺陷。不過對於操作在一般電壓之負電壓溫度不穩定性方面，仍是優於熱氮化氧化層歸因於較低的界面缺陷密度。

最後，我們論證了以二氧化鉿(HfO_2)及鉿之氮氧化矽(HfSiON)兩種材料作為閘極氧化層的N型金氧半場效電晶體在正電壓溫度不穩定性可靠度的特性退化。對以鉿為基本材料之高介電係數介電層而言，在正電壓溫度不穩定性可靠度測試期間所產生的氧化層主體缺陷會主導元件的正電壓溫度不穩定性之特性退化。在正電壓溫度不穩定性可靠度測試中，較低的臨界啟始電壓退化以及氧化層主體缺陷產生率，證明了鉿之氮氧化矽的薄膜品質優於二氧化鉿。此外，在正電壓溫度不穩定性可靠度測試期間，相對於二氧化鉿介電層而言，鉿之氮氧化矽則有較淺的電荷捕捉能階。

Gate Engineering of Advanced MOSFETs
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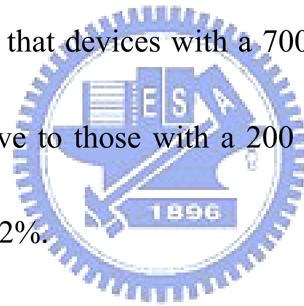
Abstract

In this dissertation, we investigated the gate engineering integration for advanced device performance and reliability improvement including the comparison of STI-induced local uniaxial compressive stress in <110>- and <100>-channel directions, the use of SiN capping layer on (111) orientation substrate to improve the NMOSFET performance, the reliability comparisons in negative-bias temperature instability (NBTI) and hot-carrier injection (HCI) between dual gate oxide PMOSFETs using plasma nitrided oxide (PNO) and thermally nitrided oxide (TNO) and the positive-bias temperature instability (PBTI) trapping/de-trapping reliability issues for devices using Hf-based high-k dielectrics.

Active-region layout dependence and STI-induced uniaxial compressive stress impact on the performance of 65 nm technology PMOSFETs with <110>- and <100>-channel directions were fully investigated. For 65 nm PMOSFET, <100>-channel show as higher as about 8 ~

15% in Id_sat than <110>-channel devices as S/D length increased from 0.21 m to 10 m. Furthermore, higher immunity to boron diffusion and less sensitivity on STI-induced strain in both of channel length and width directions for <100>-channel devices were also demonstrated.

We also investigated NMOSEFT fabricated with local strained channel techniques on a (111) Si substrate using a SiN capping layer with high mechanical stress and the stack gate of amorphous silicon (α-Si) and polycrystalline silicon (poly-Si). The on-current and transconductance (G_m) increased with increasing SiN capping layer or α-Si layer thickness. Our experimental results show that devices with a 700 Å α-Si layer show a 6.7% on-current improvement percentage relative to those with a 200 Å α-Si layer, and a corresponding G_m improvement percentage of 10.2%.



Besides, we compared the effects of NBTI and HCI on the core and input/output (I/O) PMOSFET fabricated using the different gate dielectrics of PNO and TNO. The mobility and constant overdrive current of the PMOSFETs fabricated using PNO as a gate oxide material are about 30% and 23% higher than those of the devices fabricated using TNO, respectively. The core PMOSFETs fabricated using PNO show a better NBTI and HCI immunity than those fabricated using TNO owing to the lower nitrogen concentration at the SiO_2/Si-substrate interface. However, the I/O PMOSFETs fabricated using PNO show a higher HCI-induced degradation rate because of a higher oxide bulk trap density but a better NBTI than the

devices fabricated using TNO at a normal stressed bias due to a low interface trap density.

In the final part, PBTI degradation for HfO_2 and HfSiON NMOSFETs with the metal gate electrode has been successfully demonstrated. The generated oxide trap during PBTI stress will dominate the PBTI characteristics for Hf-based gate dielectrics. The reduction of threshold voltage degradation and oxide trap generation under PBTI stress indicates that the HfSiON thin film quality is better than HfO_2. In addition, as compared to HfO_2 dielectrics, the HfSiON has shallower charge trapping level under PBTI stress.

致　謝

終於…畢業了！一本薄薄百來頁的博士論文，也許可以顯示出了這幾年的研究成果，但卻描述不出這些年遇到的挫折、低潮與掙扎。無論如何，總算是完成了我人生的一個重要目標。

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感謝在我博士求學生涯帶我、指導我的張勝傑學長與李耀仁學長。在學校求學以及在台積電工作的期間，因為有張勝傑學長對我的許多指導與幫助，讓我學到很多，也讓我人生規劃明確的多。李耀仁學長在學術實驗上嚴謹的態度是我最推崇的，在我畢業前這一年，也給予我很多課業上的討論與想法。在此也感謝在台積電工作期間一起工作的所有同事們，你們讓我的人生眼界寬廣不少。也感謝一起渡過漫長求學路的實驗室成員們，讓我在學校的生活更加多采多姿。相信不久之後在職場中，我們會再相遇的。

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最後，謹以這本博士論文，獻給我的爸媽，沒有你們無怨無悔的犧牲奉獻，不會有今日的我。還有我的老弟。我的成就，因為有你們，一切才具有了意義。你們永遠都是我最最最愛的家人！

2007 于 風城‧交大

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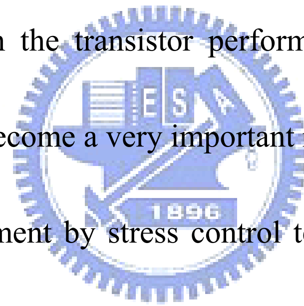
Chapter 1

Introduction

1-1 General Background

1-1-1 Mobility enhancement technology

As integrated circuit (IC) technology enters ultra-large-scale integration (ULSI) generation, geometric scaling of silicon complementary metal-oxide semiconductor (CMOS) transistors has enabled not only an exponential increase in circuit integration density, but also a corresponding enhancement in the transistor performance itself. For this reason, mobility enhancement technology has become a very important research in CMOS fabrication.



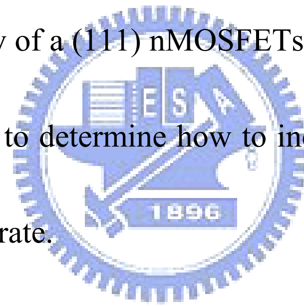
Recently, mobility enhancement by stress control technologies is emerging as one of the key elements in scaling of complementary metal-oxide-semiconductor (CMOS) transistors since it offers increased drive current without the penalty of additional capacitance and gate current leakage. There are two main approaches for implementing strain on metal-oxide-semiconductor field-effect-transistors (MOSFETs). One is the substrate biaxial stress where stress is introduced across the entire substrate [1-5]. When a thin film with a larger lattice constant (SiGe) is grown on a substrate with smaller lattice constant (Si), the film retains the in-plane lattice constant of the substrate and a biaxially compressive strain (or tensile strain under contrary condition) will be generated [6]. However, biaxial tensile stress

using strained Si on relaxed SiGe face a lot of challenges such as misfit and defects, Ge up-diffusion [7], high cost and modest hole mobility gain at high field because quantization effect [8-9]. In contrast, the second approach, process-induced uniaxial strain such as shallow-trench isolation (STI) [10], silicon nitride capping layer [11], silicidation process [12] and embedded SiGe source/drain (S/D) [13] can offer similar electron mobility enhancement compared with biaxial strain, while the hole mobility improvement is more significant at high field [7]. For this reason, although STI-induced strain in the channel region had generally considered a problem rather than an opportunity in the past, nowadays, STI-induced compressive stress in the channel has become a key point as device scaled down.

Another simple way to enhance mobility is using a wafer with a specific channel orientation which has smaller carrier effective mass. The <100>-channel device on (100), whose channel direction is rotated by 45 degree from the conventional <110>-channel device, had been reported that PMOS drive current could be improved, with NMOS performance maintained [14].

On the other hand, novel three-dimensional (3-D) device structures with a double or surrounded gate such as fin field-effect transistor (FinFET) [15-17] and vertical metal-oxide-semiconductor field-effect transistor (MOSFET) [18-20] are widely investigated. These specific structures enable the device channel to be fabricated on various surface crystal orientations. Since channel mobility is well known to be strongly dependent on crystal

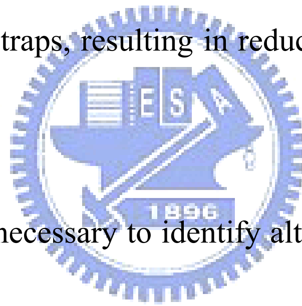
orientation [21-22], the characteristics of devices with various crystal orientations should be carefully studied to optimize the performance for ultra large-scale integration (ULSI) technology applications. It has recently been reported that oxide quality and reliability on a (111) substrate are slightly better than those on a conventional (100) substrate for ultrathin (< 2 nm) gate oxide [23]. It was also found that for a thin gate oxide of less than 2 nm, the oxidation rate of a (111) silicon substrate is lower than that of a (100) substrate such that the oxide uniformity of the (111) substrate is also improved [23-24]. The mobility of pMOSFETs on a (111) substrate can be improved owing to the low hole effective mass of the substrate; however, the low-field mobility of a (111) nMOSFETs is still less than that of (100) substrate. Therefore, it is very important to determine how to increase electron mobility in the channel region [25-27] on a (111) substrate.



1-1-2 Reliability issues

For advanced ultra-large-scale integration (ULSI) technology, nitrogen atoms are incorporated into silicon dioxide to block an undesirable boron penetration from a P^+ poly-gate electrode of a p-channel metal-oxide-semiconductor field-effect transistor (PMOSFET) [28-30]. Even for cutting-edge 65 nm complementary metal-oxide-semiconductor (CMOS) technology, nitrided oxide is still a key gate dielectric material for achieving a high device performance for both general and low-power applications

[31-33]. On the other hand, devices feature dual gate oxide (DGO) processes in which thin oxide is used for core and logic circuits and thick oxide is used for input/output (I/O) and analog circuits, owing to the decreasing size and increasing number of system-on-chip applications. Consequently, reliability issues, such as negative-bias temperature instability (NBTI) [34-35] and hot-carrier injection (HCI) [36-38], that could induce threshold voltage shift and performance degradation in DGO PMOSFETs become a serious concern for realizing highly reliable integrated CMOS devices. Therefore, both the concentration and distribution of nitrogen in the gate oxide should be optimized since excessive nitrogen at the interface may induce interface traps, resulting in reduced channel carrier mobility [39] and a degraded reliability [40].



Furthermore, it has become necessary to identify alternate high-k gate dielectrics that meet the stringent requirements for low leakage current and thin equivalent oxide thickness (EOT) [41-45]. High-k dielectrics are especially advantageous for low-power application and for thickness uniformity control owing to the thicker physical thickness. Among high-k gate dielectric materials, Hf-based gate dielectric including HfO_2 and Hf-silicate are the attractive materials because it has good device characteristics and is compatible with the conventional polysilicon gate process [46-49]. However, before Hf-based gate dielectrics being successfully integrated into future technologies, their reliability characteristics still need to be better identified. Bias temperature instability (BTI) has been recognized as one of the critical

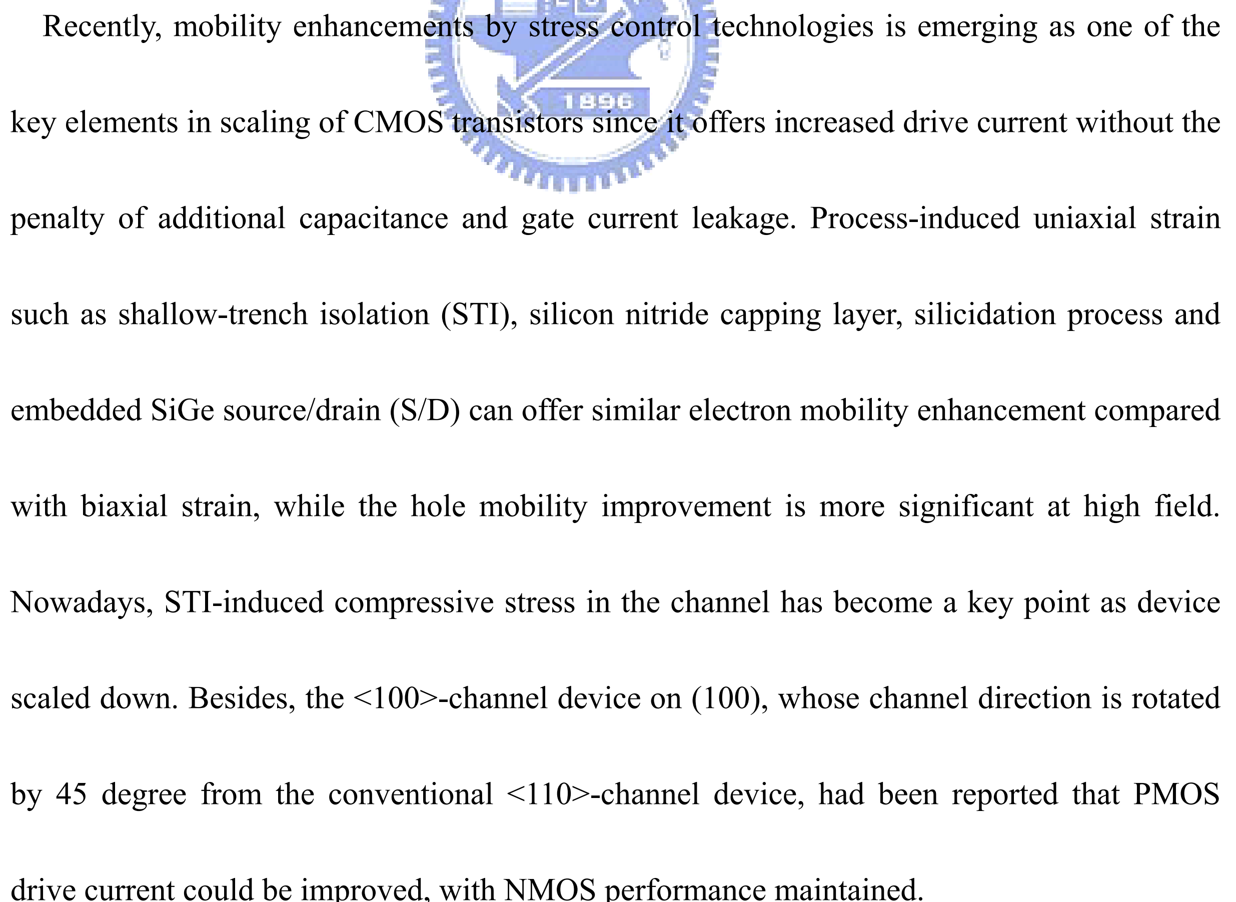
concern in the reliability of modern CMOS devices. Many of the past BTI researches on the SiO_2 dielectric have just focused on the negative BTI (NBTI) on PMOS devices [50-51], since it impacts more the devices reliability with respect to positive BTI (PBTI) on NMOS [52]. In conventional SiO_2 gate oxides, NMOS under PBTI stress shows little threshold voltage degradation and hence is not a reliability concern while PMOS under NBTI stress has a continued reliability issue as the gate oxide thickness is scaled thinner.

On the contrary, unlike conventional SiO_2 gate dielectrics, NMOS positive bias temperature instability (PBTI) could be a potential scaling limit of CMOS technology with Hf-based gate dielectrics [53]. Most of the previous studies showed a significant positive threshold voltage shift for the high-k gate stack under PBTI stressing, which was attributed to the preexisting traps in the high-k layer or the hole induced oxygen vacancy traps [54-58]. In addition, one of main issues for high-k gate dielectrics is the charge trapping/de-trapping characteristics during reliability test. Initial observation of instability was studied through capacitance–voltage (CV) characteristics in V_{fb} change and current–voltage (IV) in V_{th} change. Since electrons can be trapped and de-trapped in the high-k dielectrics with a minimal residual damage to its atomic structure, a V_{th} instability associated with electron trapping/detrapping in high-k layer can significantly affect the transistor performance [59]. Nevertheless, it also complicates the evaluation of the effects of stress-induced defect generation phenomenon on the high-k gate dielectrics, which typically is not an issue in the case of SiO_2 dielectrics [60]. In order to

investigate the additional electron trapping effects on top of defect generation, a de-trapping step has been proposed for studying generation of the electron trapping process and its impact on high-k device reliability [61]. Recently, the electron de-trapping behavior in the high-k films has used under specific gate bias conditions identifying charge trapping and relaxation mechanism [62]. However, the dependence of the dielectric electrical characteristics on the de-trapping conditions has not been investigated in detail.

1-2 Motivation

1-2-1 STI-induced compressive stress in <110> and <100>-channel direction



Recently, mobility enhancements by stress control technologies is emerging as one of the key elements in scaling of CMOS transistors since it offers increased drive current without the penalty of additional capacitance and gate current leakage. Process-induced uniaxial strain such as shallow-trench isolation (STI), silicon nitride capping layer, silicidation process and embedded SiGe source/drain (S/D) can offer similar electron mobility enhancement compared with biaxial strain, while the hole mobility improvement is more significant at high field. Nowadays, STI-induced compressive stress in the channel has become a key point as device scaled down. Besides, the <100>-channel device on (100), whose channel direction is rotated by 45 degree from the conventional <110>-channel device, had been reported that PMOS drive current could be improved, with NMOS performance maintained.

In this thesis, we have examined the fully study of STI-induced strain impacts on the performances of small devices with <110>- and <100>-channel orientations.

1-2-2 Tensile strain induced by SiN capping layer and stack of α-Si gate on (111) substrate

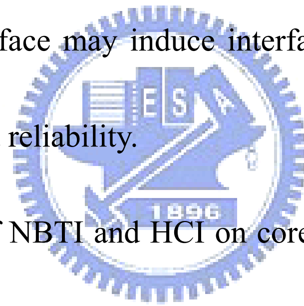
It has recently been reported that oxide quality and reliability on a (111) substrate are slightly better than those on a conventional (100) substrate for ultrathin (< 2 nm) gate oxide. It was also found that for a thin gate oxide of less than 2 nm, the oxidation rate of a (111) silicon substrate is lower than that of a (100) substrate such that the oxide uniformity of the (111) substrate is also improved. The mobility of pMOSFETs on a (111) substrate can be improved owing to the low hole effective mass of the substrate; however, the low-field mobility of a (111) nMOSFETs is still less than that of (100) substrate. Therefore, it is very important to determine how to increase electron mobility in the channel region on a (111) substrate.

In this thesis, we proposed the use of local strained channel techniques on a (111) Si substrate by depositing a SiN capping layer with high mechanical tensile stress and using the stack gate of amorphous silicon (α-Si) and polycrystalline silicon (poly-Si) to improve the performance of NMOSFETs with the <110> channel direction on a (111) substrate.

1-2-3 Reliability issues of dual-gate oxide PMOSFET with PNO and TNO

For ULSI generation, nitrogen atoms are incorporated into silicon dioxide to block an

undesirable boron penetration from a P^+ poly-gate electrode of a p-channel metal-oxide-semiconductor field-effect transistor (PMOSFET). Even for cutting-edge 65 nm CMOS technology, nitrided oxide is still a key gate dielectric material for achieving a high device performance for both general and low-power applications. Consequently, reliability issues, such as negative-bias temperature instability (NBTI) and hot-carrier injection (HCI), that could induce threshold voltage shift and performance degradation in DGO PMOSFETs become a serious concern for realizing highly reliable integrated CMOS devices. Therefore, both the concentration and distribution of nitrogen in the gate oxide should be optimized since excessive nitrogen at the interface may induce interface traps, resulting in reduced channel carrier mobility and a degraded reliability.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In this thesis, the impacts of NBTI and HCI on core and I/O PMOSFETs between devices with plasma nitrided oxide (PNO) and devices with thermally nitrided oxide (TNO) were compared systematically.

1-2-4 De-trapping effects in high-k dielectrics under PBTI stress

As CMOS devices are scaling down aggressively, it has become necessary to identify alternate high-k gate dielectrics that meet the stringent requirements for low leakage current and thin equivalent oxide thickness (EOT). However, before Hf-based gate dielectrics being successfully integrated into future technologies, their reliability characteristics still need to be

better identified. Unlike conventional SiO_2 gate dielectrics, NMOS positive bias temperature instability (PBTI) could be a potential scaling limit of CMOS technology with Hf-based gate dielectrics. In addition, one of main issues for high-k gate dielectrics is the charge trapping/de-trapping characteristics during reliability test. The electron de-trapping behavior in the high-k films has used under specific gate bias conditions identifying charge trapping and relaxation mechanism. However, the dependence of the dielectric electrical characteristics on the de-trapping conditions has not been investigated in detail.

In this thesis, the comparison of trapping/de-trapping effect of NMOSFET under PBTI stress test between NMOSFETs with HfO_2 and Hf-silicates (HfSiON) high-k dielectrics has been investigated.

1-3 Thesis outline

This dissertation is divided into six chapters as follows:

In chapter 1, a brief general background of gate engineering such as process-induced local strain, channel direction, substrate orientation and different gate dielectrics for performance and reliability improvement is introduced. Then we discuss some of the most important issues of CMOS technology and the motivation of our study. Then the outline throughout this dissertation is described here.

In chapter 2, the layout dimension dependence of relative performance for 65-nm

MOSFETs is systematically investigated. We have further examined the fully study of STI-induced strain impacts on the performances of small devices with <110>- and <100>-channel orientations. Furthermore, higher immunity to boron diffusion and less sensitivity on STI-induced strain in both of channel length and width directions for <100>-channel devices were also demonstrated.

In chapter 3, we proposed the use of local strained channel techniques on a (111) Si substrate by depositing a SiN capping layer with high mechanical tensile stress and using the stack gate of amorphous silicon (α-Si) and polycrystalline silicon (poly-Si) to improve the performance of NMOSFETs with the <110> channel direction on a (111) substrate. By using these techniques, the performance improvement of the NMOSFETs in the <110> channel direction on the (111) substrate was achieved.

In chapter 4, the impacts of NBTI and HCI on core and I/O PMOSFETs between devices with plasma nitrided oxide (PNO) and devices with thermally nitrided oxide (TNO) were compared systematically. The mobility of the PMOSFETs fabricated using PNO is higher than those of the devices fabricated using TNO. The core PMOSFETs with PNO show a better NBTI and HCI immunity than those fabricated using TNO. However, the I/O PMOSFETs fabricated using PNO show a higher HCI-induced degradation rate but a better NBTI than the devices fabricated using TNO.

In chapter 5, the comparison of trapping/de-trapping effect under PBTI stress test between

NMOSFETs with HfO_2 and Hf-silicates (HfSiON) high-k dielectrics has been investigated. We just primary focus on NMOS devices PBTI here since it is more significant than PMOS NBTI in the case of Hf-based dielectrics MOSFETs.

In chapter 6, we summary our experimental results and give a brief conclusion. Recommendations are also given for further study.

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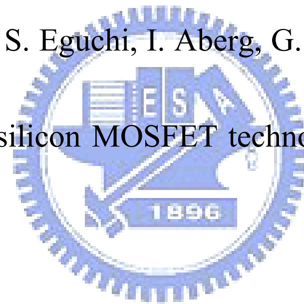

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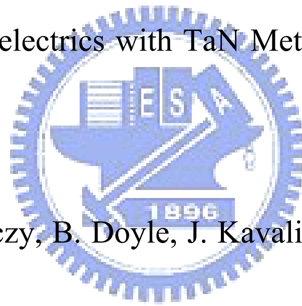

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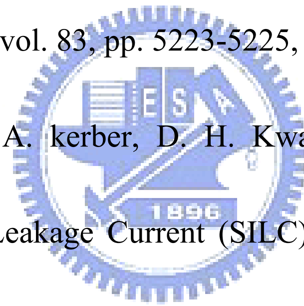

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Chapter 2

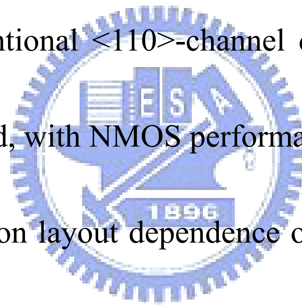
Systematical Comparisons on Performance Improvement by STI-Induced Strain between <110>- and <100>-Channel Directions Sub-65 nm PMOSFETs

2-1 Introduction

Recently, mobility enhancements by stress control technologies is emerging as one of the key elements in scaling of complementary metal-oxide-semiconductor (CMOS) transistors since it offers increased drive current without the penalty of additional capacitance and gate current leakage. There are two main approaches for implementing strain on metal-oxide-semiconductor field-effect-transistors (MOSFETs). One is the substrate biaxial stress where stress is introduced across the entire substrate [1-5]. When a thin film with a larger lattice constant (SiGe) is grown on a substrate with smaller lattice constant (Si), the film retains the in-plane lattice constant of the substrate and a biaxially compressive strain (or tensile strain under contrary condition) will be generated [6]. However, biaxial tensile stress using strained Si on relaxed SiGe face a lot of challenges such as misfit and defects, Ge up-diffusion [7], high cost and modest hole mobility gain at high field because quantization effect [8-9].

In contrast, the second approach, process-induced uniaxial strain such as shallow-trench

isolation (STI) [10], silicon nitride capping layer [11], silicidation process [12] and embedded SiGe source/drain (S/D) [13] can offer similar electron mobility enhancement compared with biaxial strain, while the hole mobility improvement is more significant at high field [7]. For this reason, although STI-induced strain in the channel region had generally considered a problem rather than an opportunity in the past, nowadays, STI-induced compressive stress in the channel has become a key point as device scaled down. Besides, another simple way to enhance mobility is using a wafer with a specific channel orientation which has smaller carrier effective mass. The <100>-channel device on (100), whose channel direction is rotated by 45 degree from the conventional <110>-channel device, had been reported that PMOS drive current could be improved, with NMOS performance maintained [14].

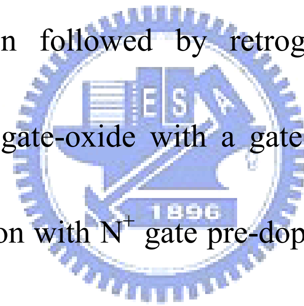


In this chapter, active-region layout dependence of 65 nm PMOSFET performance with <110>- and <100>- channel orientations were fully investigated. We have further examined the fully study of STI-induced strain impacts on the performances of small devices with <110>- and <100>-channel orientations. For 65 nm PMOSFET, <100>-channel show about 8-15% higher drain current than <110>-channel devices as S/D length increased from 0.21 m to 10 m. Furthermore, higher immunity to boron diffusion and less sensitivity on STI-induced strain in both of channel length and width directions for <100>-channel devices were also demonstrated.

2-2 Experiment

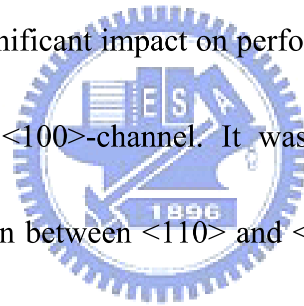
(100) orientation substrate with <110>- and <100>-notch wafers (Fig. 2-1(a), (b), respectively), where the wafer notched at different directions with 45 degree-off were used for experiment splits. CMOS devices were fabricated with state-of-the-art 300 mm wafer foundry technology [15] which includes super steep retrograde (SSR) indium and arsenic channels, aggressive poly Si gate control, multi-tilted pocket implants, shallow source/drain extensions, and deep source/drain with low junction leakage. Implants are followed by spike anneal process to minimize diffusion.

STI was used for isolation followed by retrograde well formation. After channel implantation, plasma nitrided gate-oxide with a gate oxide thickness (T_{ox}) of 1.4 nm and un-doped poly-silicon deposition with N^+ gate pre-doping and gate patterning were followed. After shallow source/drain extensions and pocket implantation, tetraethoxysilane (TEOS) liner and low-temperature silicon nitride were processed in sequence to form a sidewall spacer. Modified S/D implants were adopted to improve activation and junction capacitance while maintaining good SCE. The fabrication of a heavily doped source/drain junction by implantation was followed by rapid thermal annealing (RTA) and NiSi self-aligned silicidation. The symbols of layout parameters were also defined in Fig. 2-1(a).



2-3 Results and Discussions

The drive current (I_d at $V_g = V_d = -1.2$ V) improvement ratio of <100>-channel to conventional <110>-channel with varied channel length devices as a function of S/D length (La: length from gate edge to STI edge) are shown in Fig. 2-2 (a), (b) for NMOSFET and PMOSFET, respectively. It is found that NMOS characteristics won't be deteriorated by using <100>-channel. There is little difference of drain current between two kinds of NMOSFET with <110>- and <100>-channel. The drive current ratio of NMOS devices are all smaller than 4%, in spite of varied gate length and decreased La. This result indicates that STI-induced stress have no significant impact on performance of NMOSFET devices for both of conventional <110>- and <100>-channel. It was also reported that there is a slight difference of drift velocity even between <110> and <111> direction, but that the difference of saturated velocity becomes still minute with an increase in electric field [16]. In contrast, for long channel (L_g > 0.24 μm) PMOS devices with La = 10 μm where the STI-induced stress doesn't impact the channel region, the drain current ratio of <100>- to <110>-channel is as high as 24 %. The drive current improvement ratio decreases as channel length scales down to smaller than 0.24 μm due to velocity saturation. Furthermore, although the drive current ratio of PMOSFET decreases as La shrinks (higher STI-induces compressive stress), it still shows about 6 % ~ 10 % improvement for devices with shortest La (0.21 μm), as shown in Fig. 2-2 (b). Figure 2-3 shows comparisons the current ratio of <100>-channel to



<110>-channel between La = 10 μm and La = 0.21 μm for the devices with varied channel length for both of NMOSFET and PMOSFET. For NMOSFET devices, there is no significant difference in current ratio under STI-induced stress as devices length scales down. For PMOSFET with La = 10 μm, <100>-channel devices show a higher drive current than <110>-channel devices. Although the drive current improvement of <100>-channel to <110>-channel drops dramatically as channel length scales down, PMOSFET with <100>-channel still shows about 16% higher than <110>-channel. But if the channel region was influenced by STI-induced compressive stress, the current ratio of <100>-channel to <110>-channel will down to smaller than 10%. This result illustrates that the impact of STI-induced compressive stress on PMOSFET with <110>-channel was much higher than that of <100>-channel. Since there is no significant dependence of STI-induced compressive stress for NMOS devices with these two different channel directions, we'll focus on the device characteristics of PMOSFET hereafter.

Figures 2-4(a), (b) depict the characteristics of drain current I_d at V_d = -1.2 V and linear transconductance G_m at V_d = -0.05 V between <110>-channel and <100>-channel of 65 nm PMOSFET devices with a La =10 μm and 0.21 μm, accordingly. For the case of the La = 10 μm which no STI-induced strain in the channel region, <100>-channel shows a 37% higher than <110>-channel PMOSFET in G_m. As La shrunk from 10 μm to 0.21 μm, the G_m of <110>-channel device increases about 11% while <100>-channel devices show the

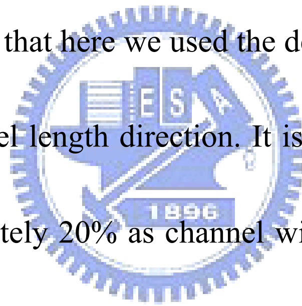
La-independent characteristics and this results in that the G_m difference between <110>- and <100>-channel PMOSFET is reduced to only 12%. This means that higher compressive stress in the channel region from STI edge can enhance hole mobility of <110>-channel PMOSFET devices. By contract, <100>-channel PMOS is almost free from to the change of STI-induced local compressive strain in the channel region. Figure 2-5 illustrates the hole band structure with two different channel directions to explain these different results between <110>- and <100>-channel PMOSFETs. Figure 2-5(a) depicts the band structure of hole with large La as no STI-induced strain. Unstrained Si has a lager effective mass of heavy hole in <110> than <100> direction so that <100>-channel PMOS device has higher hole mobility and so that higher G_m and drive current than <110>-channel devices. Figure 2-5(b) shows hole band structure under uniaxial STI-induced compressive strain. This strain not only lift the degeneracy in the valance band [17-18], but also to change the band shape of the heavy hole to the "light hole like" in <110> directionc so that this STI-induced uniaxial compressive stress can improve the performance of <110>-channel PMOSFET, while <100>-channel device is independent of this stress so that <100> direction keeps almost the same shape under the local strain.

Figure 2-6 (a) shows an I_{on} (I_d at $V_g = V_d = -1.2$ V) versus I_{off} (I_d at $V_g = 0$ V and $V_d = -1.2$ V) characteristics of 65 nm PMOSFET with La = 10 μm, it should be noted that I_{on} of <100>-channel PMOSFET is approximately 17% larger than that of <110> under the same I_{off}

conditions. As La shrunk to 0.21 μm, <100>-channel PMOSFET still shows better current drive than <110>-devices by 8%, although the drive current of <110>-channel devices are enhanced by STI-induced compressive stress, as shown in Fig. 2-6 (b). The dependence of I_{d_sat} on V_{th_sat} under STI-induced compressive stress for <110>- and <100>-channel devices are plotted in Fig. 2-7 (a) and Fig. 2-7 (b), respectively. For conventional <110>-channel PMOSFET, I_{d_sat} of the devices with La = 0.21 μm are higher than that of La = 10 μm ones by 7% at the same V_{th_sat} condition. In contrast, the Ids of <100>-channel devices are almost independent of layout dimensions and have higher I_{d_sat} as compared with <110>-channel. In order to eliminate the effect of Vth_sat variation on performance comparison in La dependence between <110>- and <100>-channel devices, the overdrive current (I_d at the bias of V_g -V_{th} = - 0.75 V) of 60 nm PMOSFETs with varied La are shown in Fig. 2-8. Although <110>-channel PMOSFETs gain an increase of 7% in overdrive current from La = 10 to 0.21 μm, <100>-channel devices still show 11% higher than <110>-channel devices. Furthermore, for fair comparison on short channel effect, Fig. 2-9 (a), (b) show the I_{d_sat} as a function of drain-induced-barrier-lowering (DIBL) for the devices with <110>- and <100>-channel, respectively. Compared with <110>-channel PMOSFET, <100>-channel device shows a less layout dependence of short channel effect owing to its non-sensitive to STI-induced local stain. In addition, under the same I_{d_sat} conditions, <100>-channel device also has smaller DIBL than <110>-channel PMOSFET, this indicates that <100>-channel has higher immunity

in short channel effect. To understand the reason of this result, Fig. 2-10 shows the comparison of drain (or source) to gate overlap capacitance (C_{gd}) for <110>- and <100>-channel devices. <100> direction shows a smaller and tighter distribution of C_{gd} than <110>. This is mainly due to the slower boron diffusivity in <100>-channel so that <100>-channel PMOSFET shows smaller DIBL and better short channel effect.

For comprehending the impact of STI-induced compressive stress from devices width direction on performance and narrow width effect, Fig. 2-11 (a), (b) show the I_{d_sat} versus V_{th_sat} for devices with varied channel width for <110>-channel and <100>-channel, respectively. It is worth to note that here we used the devices with La =10 μm to eliminate the effect of the stress from channel length direction. It is obviously that I_{d_sat} of <110>-channel devices are reduced approximately 20% as channel width scaled down while <100>-channel devices show no dependence on channel width direction contrarily. This result demonstrates that STI-induced uniaxial compressive stress from width direction is unfavorable for <110>-channel PMOSFET although this compressive stress from channel length direction can enhance the device performance. However, PMOSFET devices with <100>-channel is non-sensitive to STI-induced strain not only in channel length direction but also in width direction.



2-4 Summary

We have systematically study the STI-induced strain impacts on the performances of 65 nm technology PMOSFET with <110>- and <100>-channel directions, respectively. Table 2-1 summarizes the impact of STI-induces uniaxial compressive strain on PMOSFET performance for both of <110> and <100> channel directions. <100>-channel devices have smaller DIBL and less layout dependence due to lower boron diffusivity and its non-sensitive to STI-induced stress, accordingly. Furthermore, as Compared to <110>-channel, <100>-channel devices show not only higher hole mobility, but also keep the advantage of free from STI stress in both of channel length and width directions. This offers a very promising alternative CMOS technology and design window for high performance ULSI.

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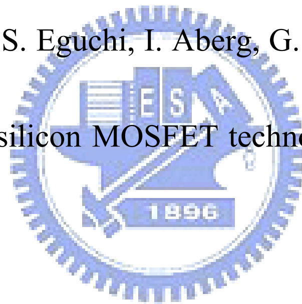

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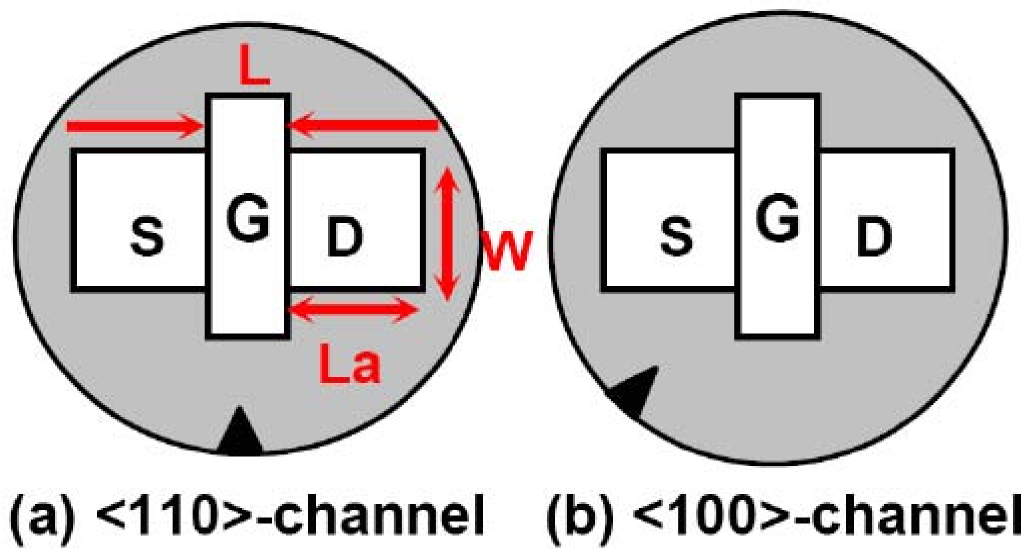
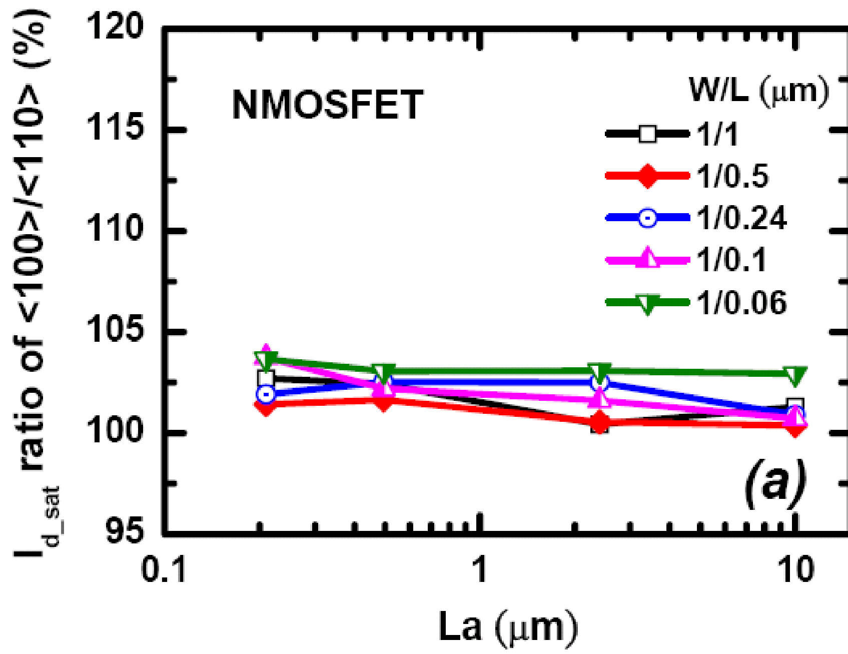


Fig. 2-1 (a) scheme of <110>-channel devices and layout parameter definition (b) scheme of <100>-channel devices. The definition of La is S/D length (the length from gate edge to STI edge).



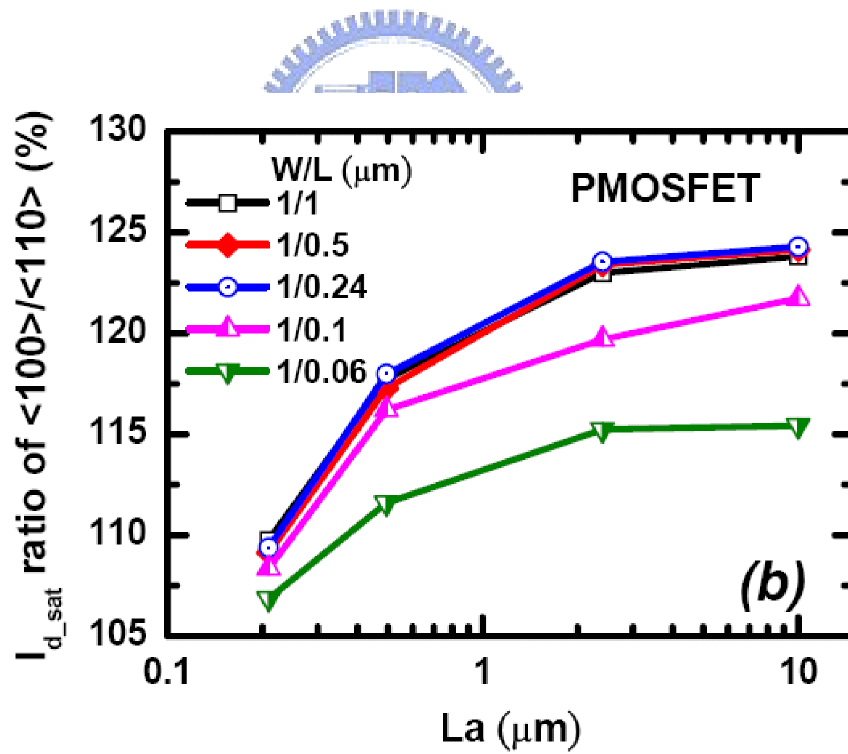


Fig. 2-2 I_{d_sat} (I_d at $V_g = V_d = -1.2V$) ratio of <100> to <110> with varied La and channel length for (a) NMOSFET (b) PMOSFET.

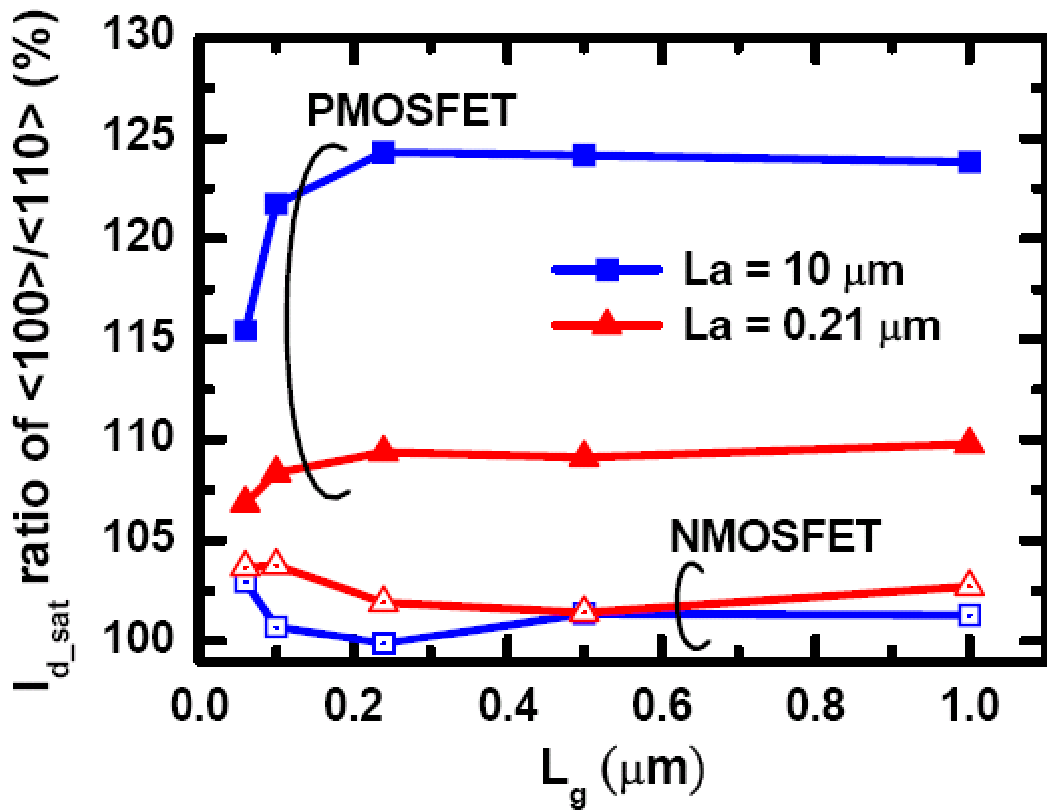


Fig. 2-3 I_{d_sat} (I_d at $V_g = V_d = -1.2V$) ratio of <100> to <110> with La = 10 μm and 0.21μm for NMOS and PMOS devices.

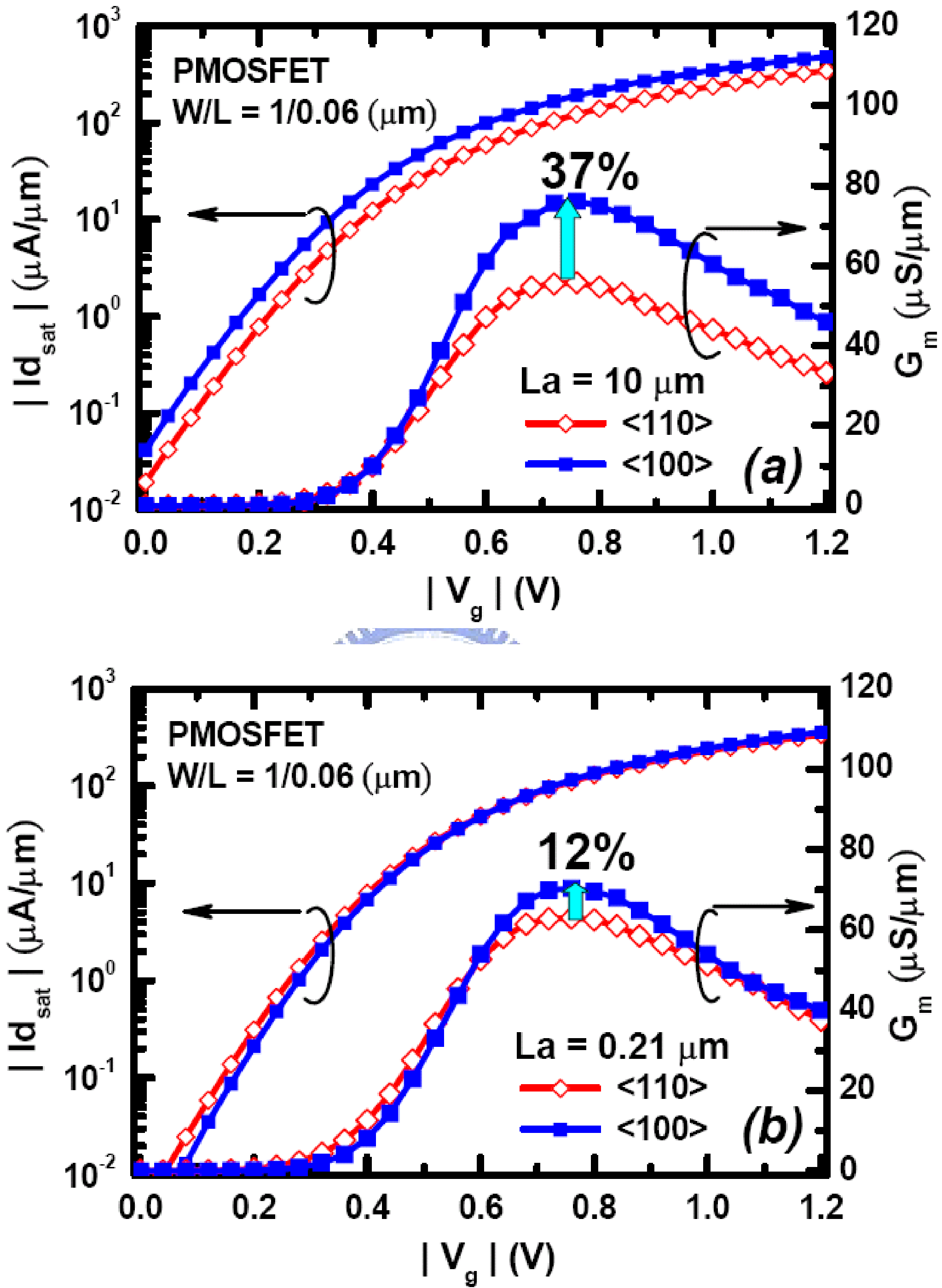


Fig. 2-4 I_d-V_g at V_d = -1.2V and G_m at V_d = -0.05V characteristics of 60 nm PMOS devices with <110>- and <100>-channel orientations for (a) La = 10 μm (b) La = 0.21 μm

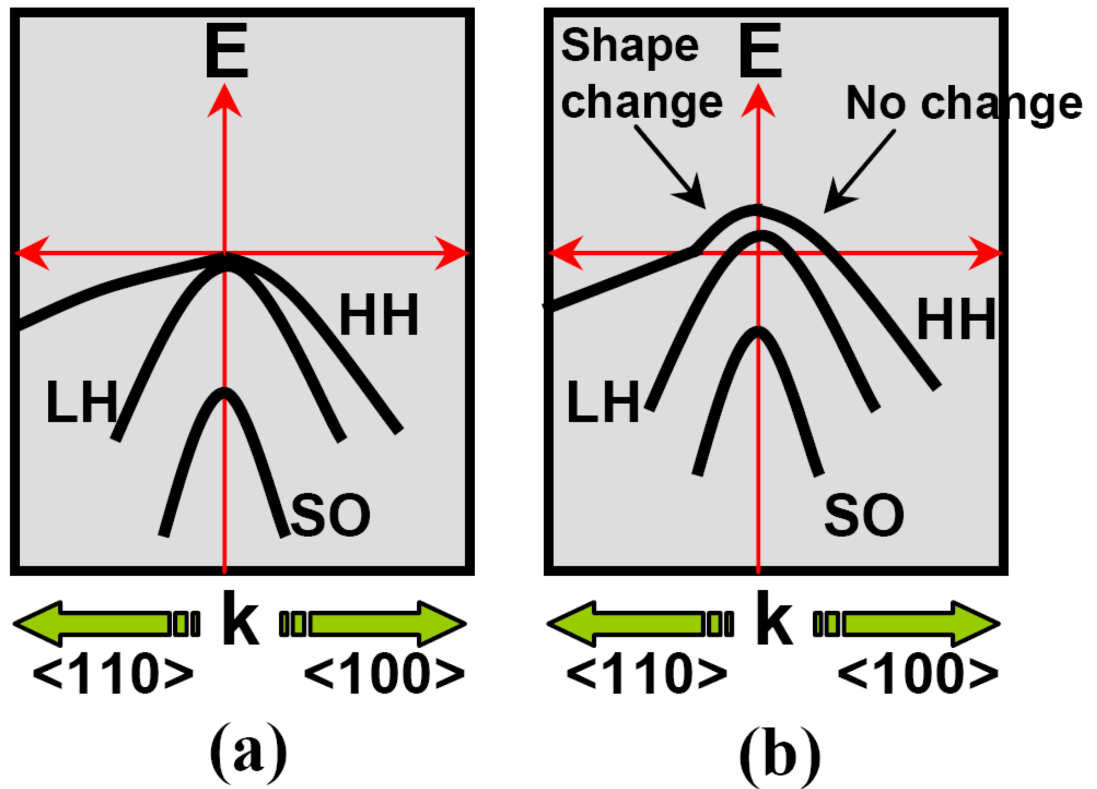


Fig. 2-5 Schemes of hole valence band structures for (a) unstrained Si and (b) Si under uniaxial compressive stress.

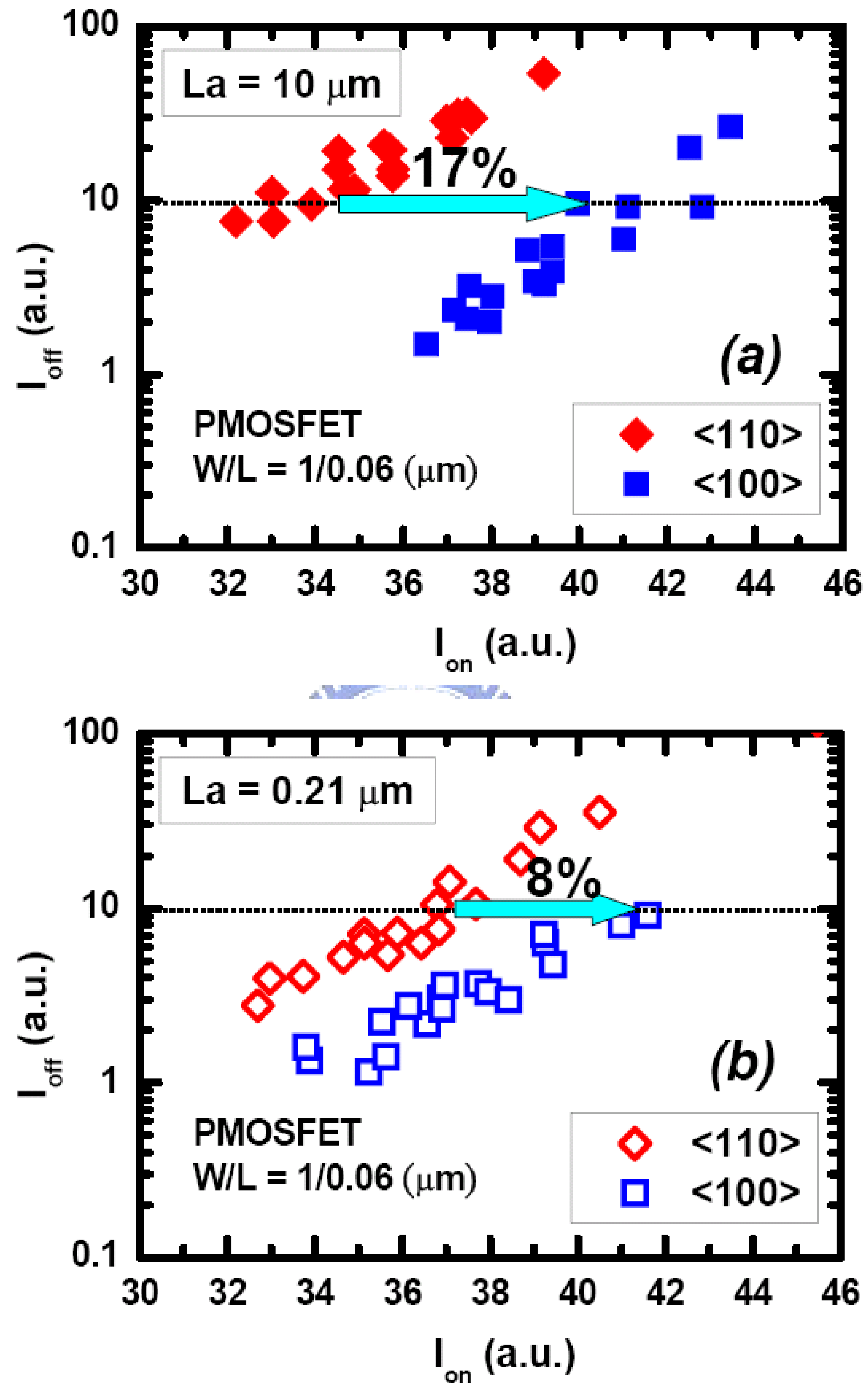


Fig. 2-6 I_{on}-I_{off} characteristics of 60 nm PMOSFETs between <110>- and <100>-channel orientations for (a) La = 10 μm and (b) La = 0.21 μm

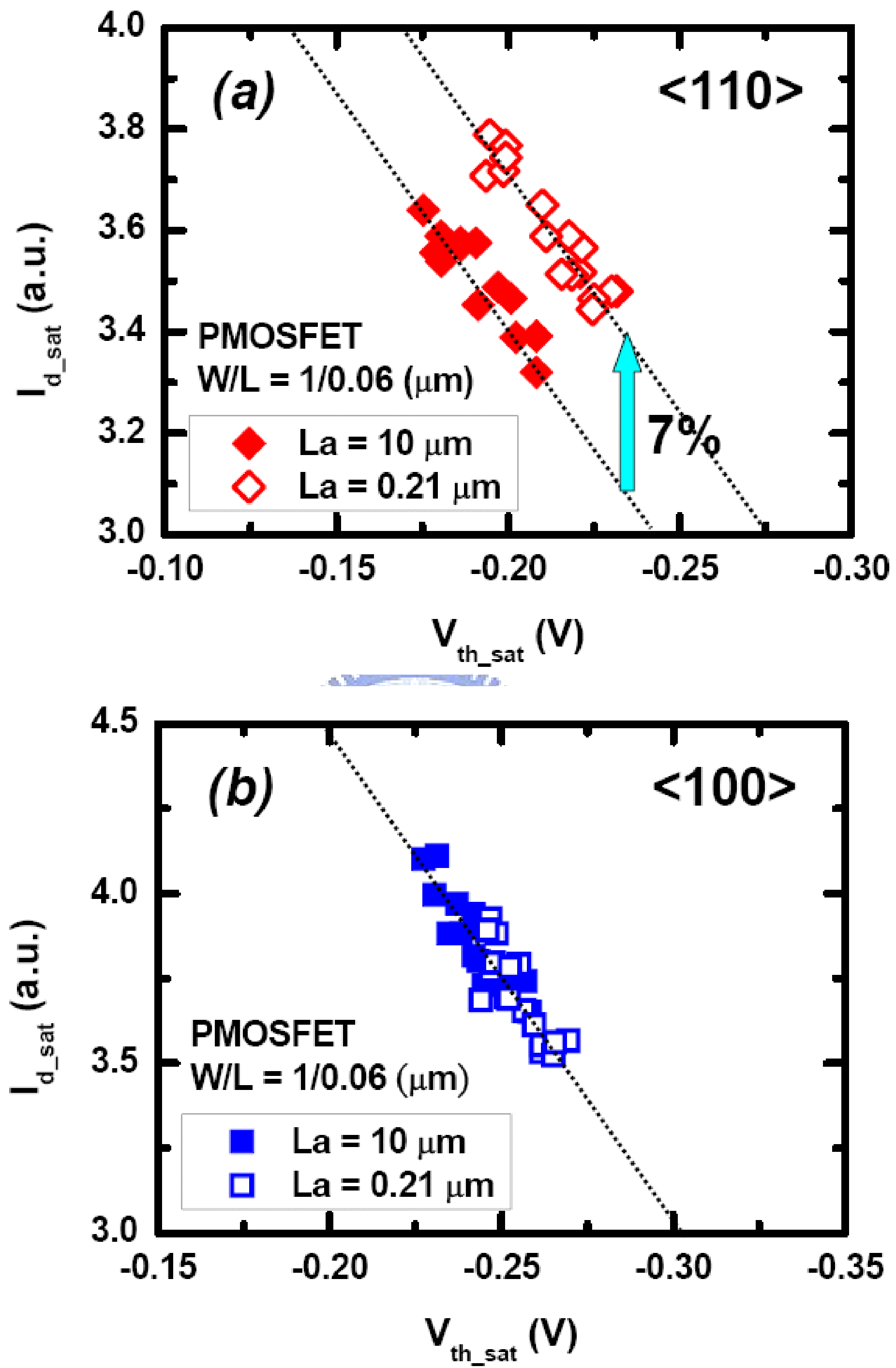


Fig. 2-7 I_{d_sat} dependence V_{th_sat} at V_d = -1.2V of 60 nm PMOS devices with La = 10 and 0.21 μm for (a) <110>-channel (b) <100>-channel directions.

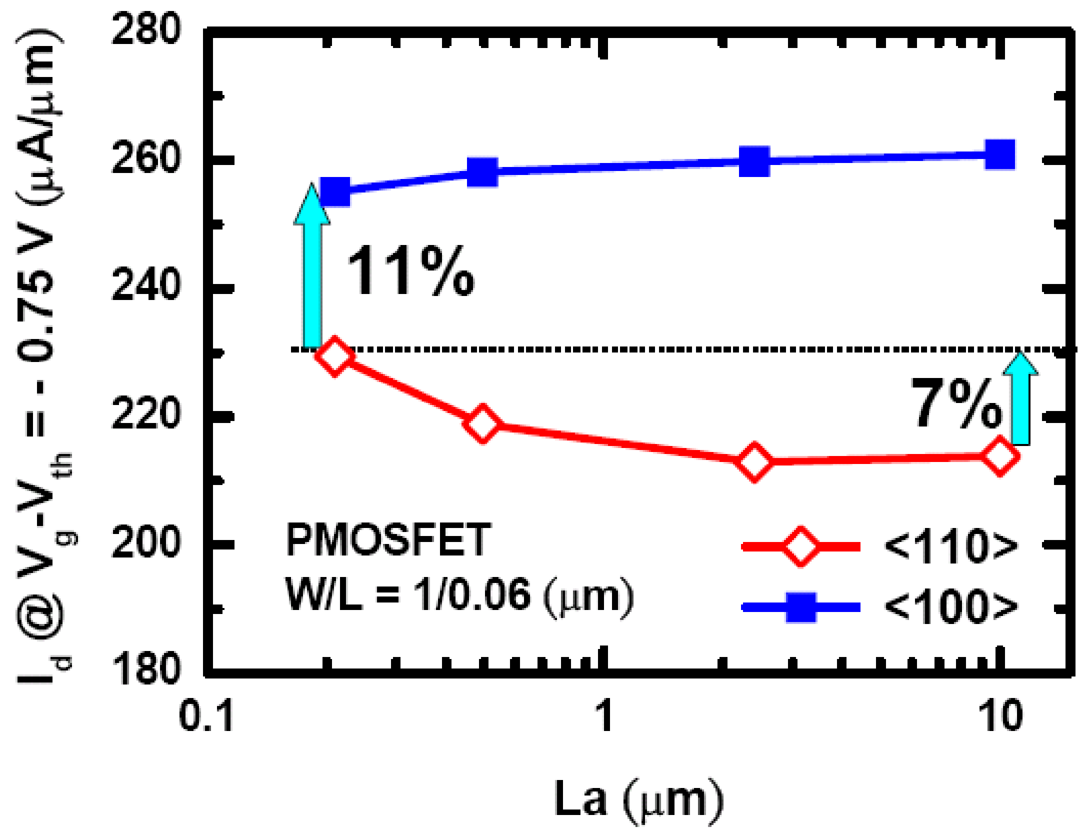


Fig. 2-8 Constant overdrive current at $V_g - V_{th}$ = -0.75V of 60 nm PMOSFETs with <110>- and <100>-channel.

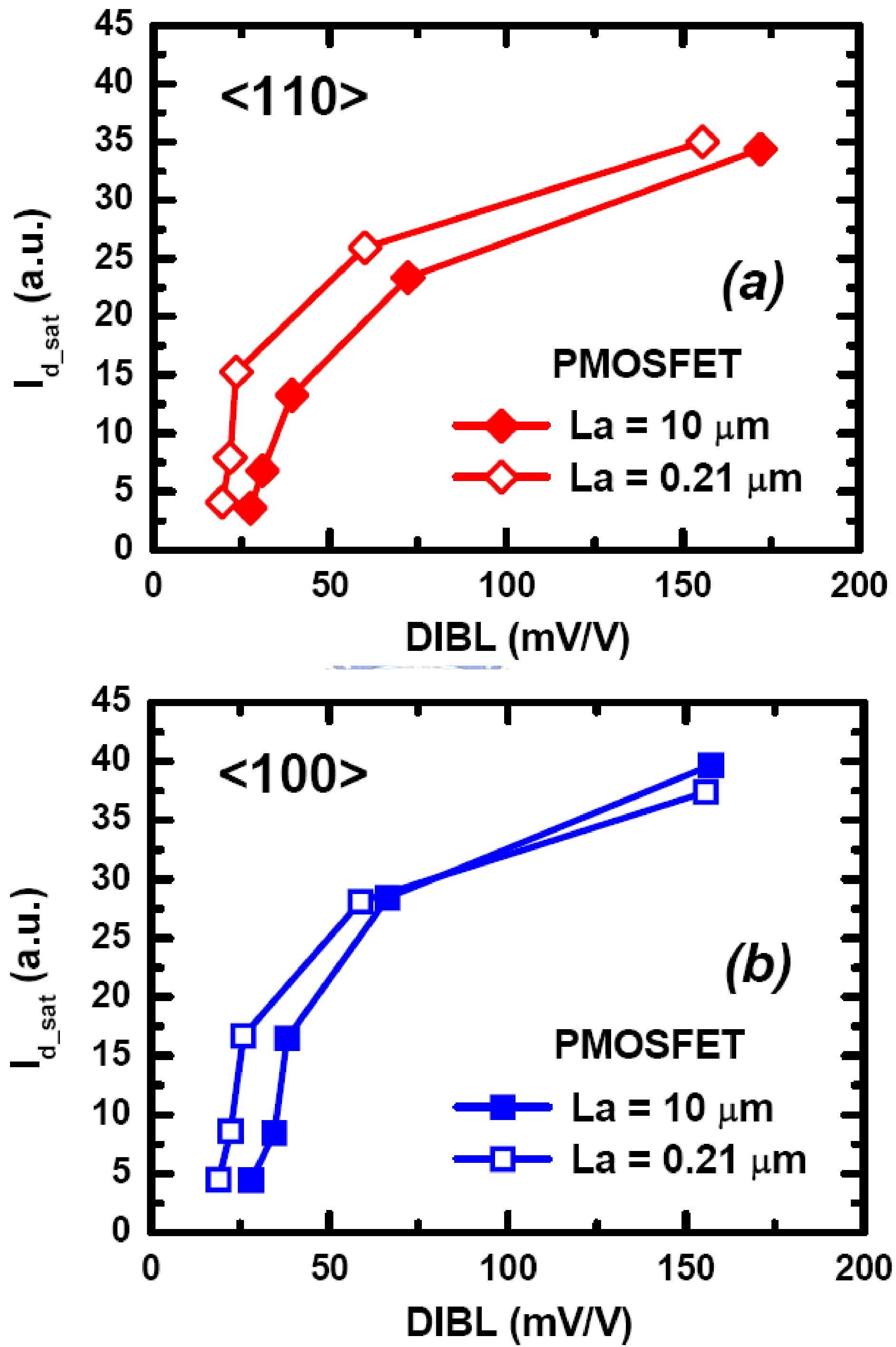


Fig. 2-9 I_{d_sat} versus DIBL of PMOSFET with La = 10 and 0.21 μm for (a) <110>-channel and (b) <100>-channel devices.

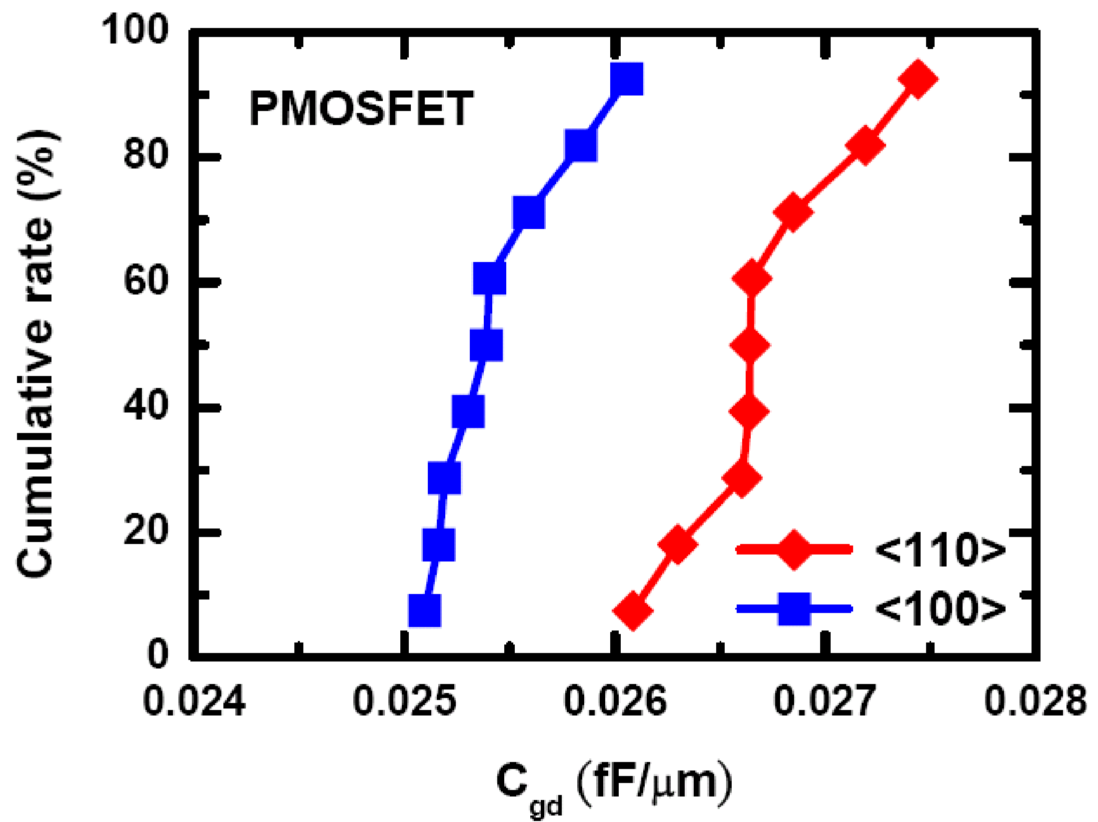


Fig. 2-10 PMOS overlap capacitance cumulative distributions of <110> and <100>- channel devices.

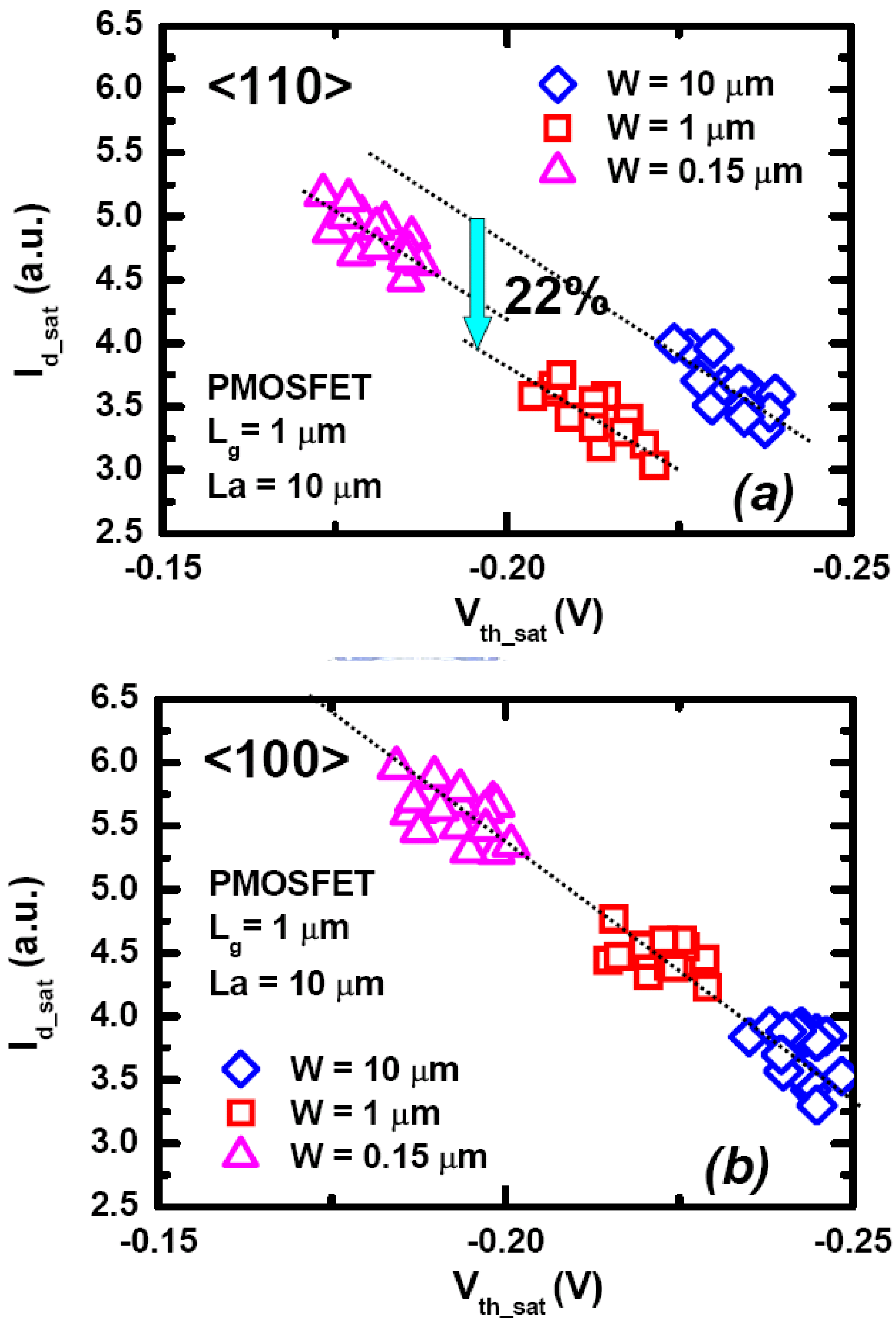
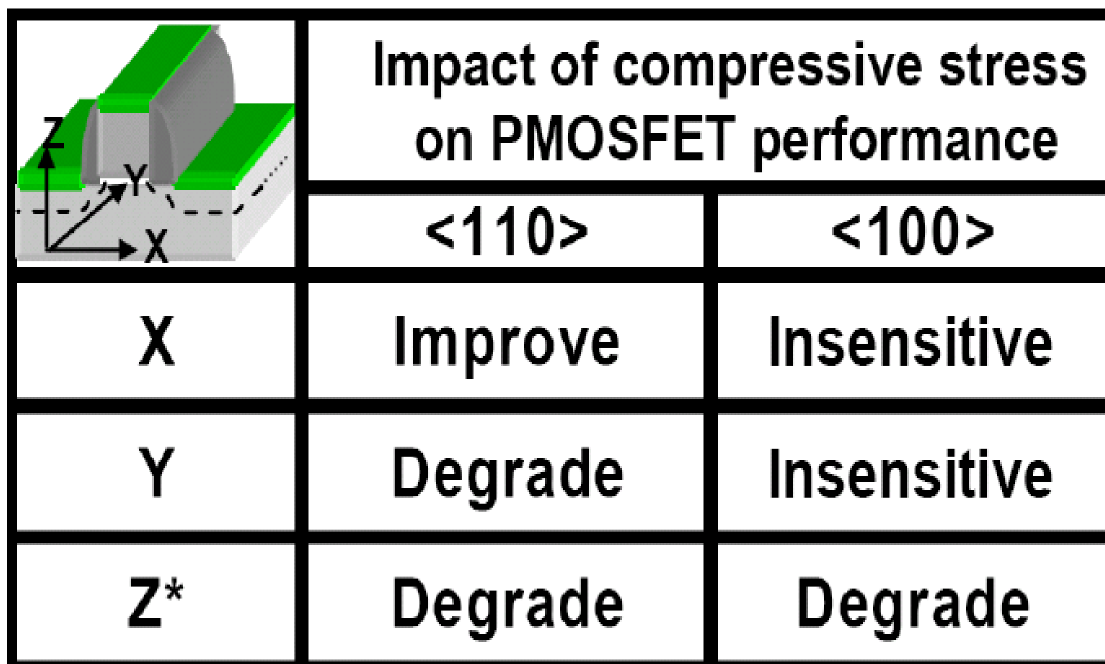


Fig. 2-11 I_{d_sat} dependence V_{th_sat} of L_g/La = 1 μm/10 μm PMOS devices with varied channel widths for (a) <110>-channel and (b) <100>-channel directions.



	Impact of compressive stress on PMOSFET performance	
	<110>	<100>
X	Improve	Insensitive
Y	Degrade	Insensitive
Z*	Degrade	Degrade

** Here we assume stress from Z direction is identical for <110> and <100> channel orientations, and use the result in ref. [1]*

Table 2-1 summarized table for compressive stress impacts on PMOSFET performance with <110> and <100> in 3D directions.

Chapter 3

Performance Enhancement by Local Strain in <110> Channel n-channel Metal-Oxide-Semiconductor Field-Effect Transistors on (111) Substrate

3-1 Introduction

In order to circumvent downsizing limitations and realize high-speed and high-performance scaled complementary metal-oxide-semiconductor (CMOS) devices, novel three-dimensional (3-D) device structures with a double or surrounded gate such as fin field-effect transistor (FinFET) [1-3] and vertical metal-oxide-semiconductor field-effect transistor (MOSFET) [4-6] are widely investigated. These specific structures enable the device channel to be fabricated on various surface crystal orientations. Since channel mobility is well known to be strongly dependent on crystal orientation [7-8], the characteristics of devices with various crystal orientations should be carefully studied to optimize the performance for ultra large-scale integration (ULSI) technology applications.

It has recently been reported that oxide quality and reliability on a (111) substrate are slightly better than those on a conventional (100) substrate for ultrathin (< 2 nm) gate oxide [9]. It was also found that for a thin gate oxide of less than 2 nm, the oxidation rate of a (111) silicon substrate is lower than that of a (100) substrate such that the oxide uniformity of the

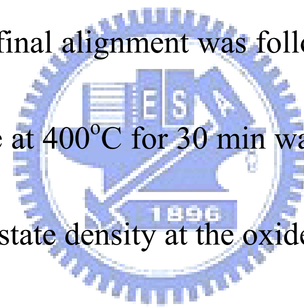
(111) substrate is also improved [9-10]. The mobility of PMOSFETs on a (111) substrate can be improved owing to the low hole effective mass of the substrate; however, the low-field mobility of a (111) NMOSFETs is still less than that of (100) substrate. Therefore, it is very important to determine how to increase electron mobility in the channel region [11-13] on a (111) substrate.

In this chapter, we proposed the use of local strained channel techniques on a (111) Si substrate by depositing a SiN capping layer with high mechanical tensile stress and using the stack gate of amorphous silicon (α-Si) and polycrystalline silicon (poly-Si) to improve the performance of n-channel metal-oxide-semiconductor field-effect transistors (NMOSFETs) with the <110> channel direction on a (111) substrate. By using these techniques, the performance improvement of the NMOSFETs in the <110> channel direction on the (111) substrate was achieved. The on-current and transconductance (G_m) increased with increasing SiN capping layer or α-Si layer thickness. Our experimental results show that devices with a 700 Å α-Si layer show a 6.7% on-current improvement percentage relative to those with a 200 Å α-Si layer, and a corresponding G_m improvement percentage of 10.2%. In addition, charge pumping current/interface state density decreased for the samples with a thicker SiN layer.

3-2 Experiment

A local strained structure with a stack of α-Si layer and a SiN capping layer was fabricated. The schematic cross section is shown in Fig. 3-1. After BF_2 implantation for the p-well region, the chemical vapor deposition (CVD) of SiO_2 for oxidation-enhanced diffusion (OED) in the well drive-in process was executed. Pad oxide and Si_3N_4 were deposited and active region alignment was followed. After Si_3N_4 etching, BF_2 was implanted for the sake of channel stop. Then, field oxidation was carried out in high-temperature ambience for local oxidation of silicon (LOCOS) isolation. Two runs of sacrificial oxide growth followed Si_3N_4 removal to eliminate the Kooi effect. To adjust the threshold voltage, BF_2 was implanted (50 keV, $5x10^{12}$). After RCA cleaning, a 2 nm gate oxide was grown in a vertical furnace (800^oC, O_2 ambience). The stacked gate, α-Si (550^oC, 20-70 nm) and in-situ-doped n^+ poly-Si (550^oC) were deposited in the same ambience. The total thickness of the poly gate for all the samples was 200nm. Poly-Si and α-Si were etched following gate alignment. To prevent leakage around the gate edge, poly-reoxidation was carried out here. After sidewall polymer removal, wafers underwent n+-source/drain implantation (As, 20 keV, $5x10^{15}$) followed by alignment. P^+-substrate alignment and implantation (BF_2, 50 keV, $2.5x10^{15}$) were executed and then rapid thermal annealing was carried out in nitrogen ambience at 1050^oC for 10 s. A thermal CVD SiN layer (at 780^oC) with different thicknesses, 100-300 nm, was directly deposited onto the transistor, followed by tetraethoxysilane (TEOS) deposition (700^oC, 350-450 nm). After contact alignment, contact etching was carried out by etching TEOS and SiN. At first, we

used dry etching to remove the upper TEOS and then wafer was dipped in a buffer oxide etchant (BOE) solution in order to confirm that the TEOS was completely removed. After removing the TEOS, we used another recipe to etch the lower SiN layer. In order to protect the Si surface from plasma etching damage, the SiN layer was etched using two steps. We calculated the SiN etching rate. We left a thin SiN layer of about 20 nm after the etching. Then, we used H_3PO_4 solution to etch the thin SiN layer. It is necessary to have an over-etching step in this wet etching process to ensure that the SiN layer is completely removed. (Ti/TiN/Al/TiN) four-level metallization was then carried out in a physical vapor deposition (PVD) system, and final alignment was followed. After carrying out metal etching, annealing in a H_2/ N_2 ambience at 400°C for 30 min was performed in order to mend dangling bonds and reduce the interface state density at the oxide/Si interface.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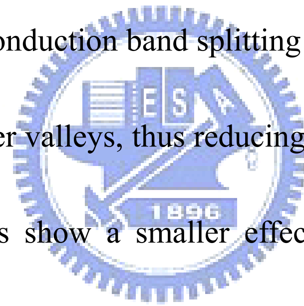
3-3 Results and Discussions

3-3-1 Single-poly-Si gate structure with SiN capping layer of different thicknesses

Figure 3-2 shows the electrical drain current and drain voltage (I_d-V_d) characteristics of the devices using a single-poly-Si gate with a fixed thickness (2000 Å) and various SiN capping layer thicknesses on a (111) orientation substrate. The improvement in drain current is proportional to the thickness of the SiN layers. Since the SiN capping layer can provide tensile strain in the channel region and thus increase the electron mobility of the devices

fabricated on a conventional (100) orientation substrate [13], this result implies that capping with SiN has also the same advantage of providing tensile strain in the channel region for NMOSFETs on the (111) substrate. For the devices on the (100) orientation substrate, this SiN-capping-layer-induced tensile strain can cause the sixfold degenerate valleys of the silicon conduction band to split into two degeneracy states: electrons with a longitudinal effective mass axis perpendicular to the interface in two lowered valleys, and those with a longitudinal mass axis parallel to the interface in four raised valleys [14-16]. For the NMOSFETs on the (111) substrate, which also shows sixfold-valley degeneracy [17], this tensile strain can also induce conduction band splitting and suppress the intervalley transitions of electrons from lower to upper valleys, thus reducing the intervalley scattering. Furthermore, in the lower valleys, electrons show a smaller effective mass in transport parallel to the interface. The combination of the reduced intervalley phonon scattering and the small effective mass increases electron mobility. The dependence of G_m on SiN capping layer thickness is shown in Fig. 3-3. G_m increased as SiN capping layer thickness increased. This result illustrates that capping with thicker SiN layers induced higher tensile strain, improving the mobility of electrons in NMOSFETs in the channel region on the (111) substrate, which is consistent with the trend of drain current shown in Fig. 3-1. However, at high vertical field (high Vg), G_m shows a little decreased as SiN thickness increases. This maybe due to hydrogen species from NH_3 gas exit at channel interface during SiN-capping layer deposited.



As vertical field increases, electrons are attracted more closed to oxide/channel interface, and the surplus hydrogen species at interface will impact the electrons drift from source to drain. The thicker SiN-capping layer, the more surplus hydrogen species at channel interface. In order to analyze our measured data more completely, Fig. 3-4 shows two-dimensional (2-D) simulation results of the SiN-capping-layer-induced stress along the channel length direction using the SILVACO simulation tool. The mechanical parameter, that is, the intrinsic stress of this simulation, is assumed to be $1.4x10^{10}$ dynes/cm^2 for a nitride film, as reported by Irene [18]. The device with the thickest SiN capping layer (3000 Å) used in this study showed the highest tensile stress (negative values for compressive stress and positive values for tensile stress) from the corner to the center region of the channel when compared with the samples with SiN layer thicknesses of 2200 and 1000 Å. The stress simulation results demonstrate that thicker SiN capping layers can induce higher tensile stresses in the channel region, and therefore improve the performance of the NMOSFETs fabricated on the (111) substrate.

Figure 3-5 shows the threshold voltages (V_{th}) of the devices with SiN capping layers of different thicknesses. For all the devices, except those without a SiN capping layer, the magnitude of the threshold voltage decreases with increasing thickness of the SiN layers. This is believed to be due to the effects of band gap narrowing resulting from local strain and the long processing time for the deposition of thicker SiN films [19]. The charge pumping currents of the devices with a 0.5 μm gate length and SiN layers of different thicknesses are

shown in Fig. 3-6. The charge pumping currents illustrate the quality of the SiO_2/Si interface after the strain was induced in the channel region. The devices without a SiN capping layer have the lowest charge pumping current, which indicates that they have the lowest number of interface traps of all the samples. The capping SiN layer may have also induced more interface traps at the oxide/Si interface. However, it is interesting that the charge pumping current decreases when the SiN layer thickness increases above 1000 Å. This implies that although the SiN capping layer may cause some damage and induces interface traps at the oxide/Si interface, SiN layer deposition may provide some hydrogen species from the NH_3 gas that passivate the interface states during the process. Thicker SiN layer capping required longer processing time; thus, more interface states were passivated.

3-3-2 Stack of -Si and Poly-Si gate with SiN capping layer of fixed thickness

The output characteristics of I_d-V_d and G_m for all the devices with a fixed SiN layer thickness (1500 Å) and various α-Si thicknesses in gate construction are shown in Figs. 3-7 and 3-8, individually. The drain current and transconductance increase as the thickness of the α-Si layer increases. The on-current improvement percentage of the devices with a 700 Å α-Si layer is 6.7 % relative to that of the devices with a 200 Å α-Si layer, and the corresponding G_m improvement percentage was 10.2 %. This result implies that there is a strain dependence of electron mobility enhanced by the stack of the α-Si gate structure. It is observed that the strain effect between the devices with 500 and 700 Å α-Si layers is not very

strong and this suggests that the strain effect saturates at an α-Si layer thickness of 500 Å. Figure 3-9 shows the simulated 2-D stress distribution contour of the NMOSFET with a 700 Å α-Si layer on the (111) orientation substrate. The simulation mechanical parameter of intrinsic stress is assumed to be $1.4x10^{10}$ dynes/cm^2 and $9x10^9$ dynes/cm^2 for the nitride and α-Si films, respectively. The simulation result shows that tensile strain is induced in the channel region owing to the stacking of α-Si for the gate structure. The mechanism of the stress elevation could be as follows: before the dopant activation, the n^+-poly gate is in the amorphous phase owing to the stacking of α-Si and the high-dose implantation of arsenic. The recrystallization of the amorphous region during rapid thermal annealing leads to n^+-poly gate expansion and residual compressive stress. Therefore, the compressive stress in the n^+-poly gate provides tensile strain to the channel region.

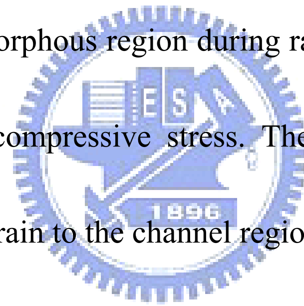
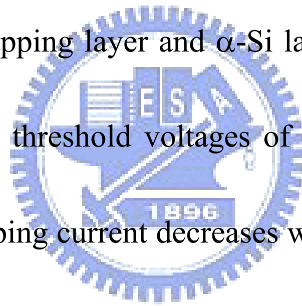


Figure 3-10 shows the threshold voltages of the devices with α-Si layers of different thicknesses. The threshold voltage of the device with a thick α-Si layer is apparently larger than that of the device with a thin α-Si layer owing to the wider poly depletion region in the stack gate structure with a thicker α-Si layer. Since the total thicknesses of all the stack gate structures are the same (2000 Å), the in-situ doping dose becomes lower when the in-situ-doped poly-Si layer becomes thinner. After the annealing, the doping concentration of the stack gate with a thinner poly-Si layer and a thicker α-Si layer is lower than that of the other stack gates. A lower doping concentration in the gate causes a wider poly depletion

region and a decrease in gate capacitance. As a result, the threshold voltage increases when the stack gate structure α-Si layer thickness increases.

3-4 Summary

Local strained channel techniques for depositing a SiN capping layer and a stack of α-Si and poly-Si gate structures on a (111) substrate were investigated in this study. We demonstrated that the use of the strain structures can improve the performance of NMOSFETs fabricated in the <110> channel direction on a (111) substrate. The device performance is further enhanced as the SiN capping layer and α-Si layer become thicker. The stack of α-Si gate structures also affects the threshold voltages of the gate because of its poly depletion width. In addition, charge pumping current decreases with increasing split SiN layer thickness. To optimize these strained conditions, advanced CMOS fabricated on a (111) substrate or novel 3-D device structures will achieve this advantage more completely and become more suitable for future ULSI applications.



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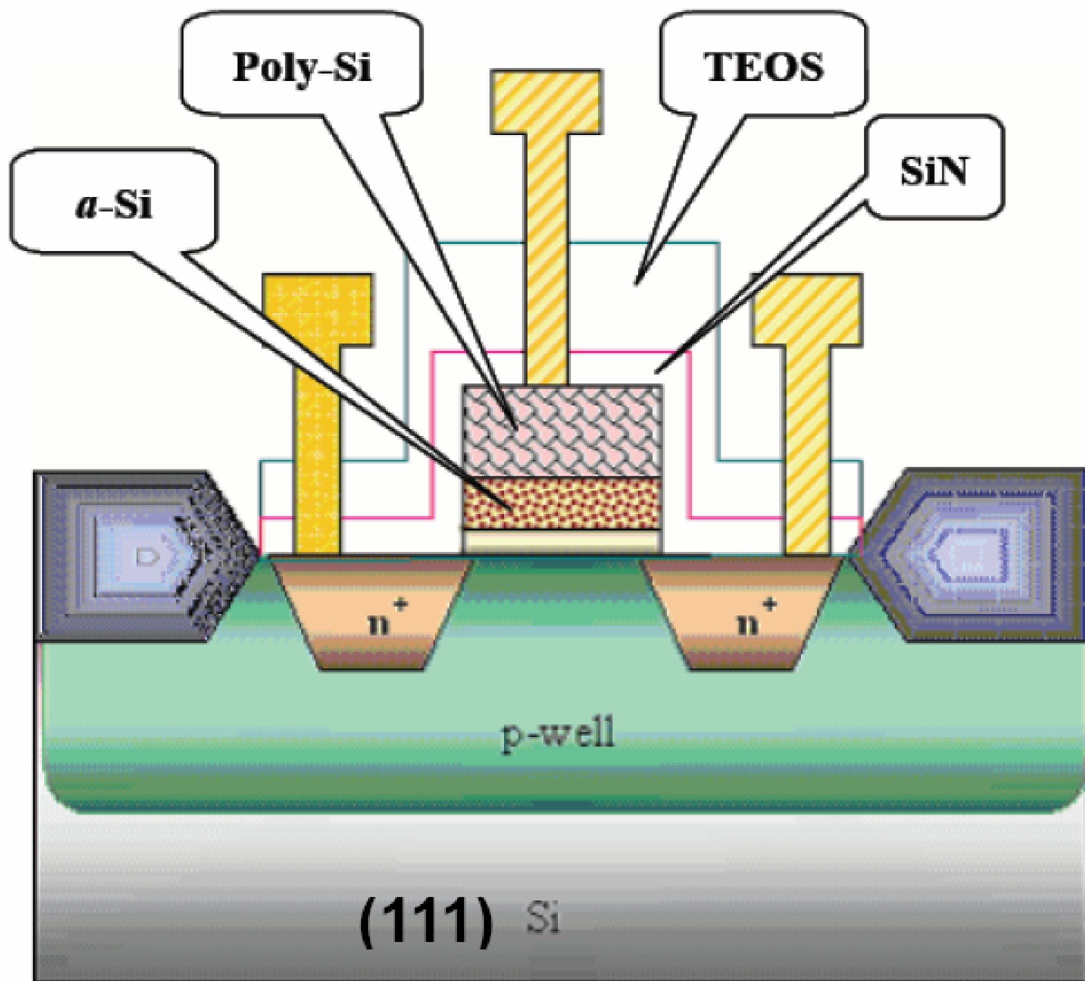


Fig. 3-1 Schematic cross section of local strained channel NMOSFET on (111) substrate.

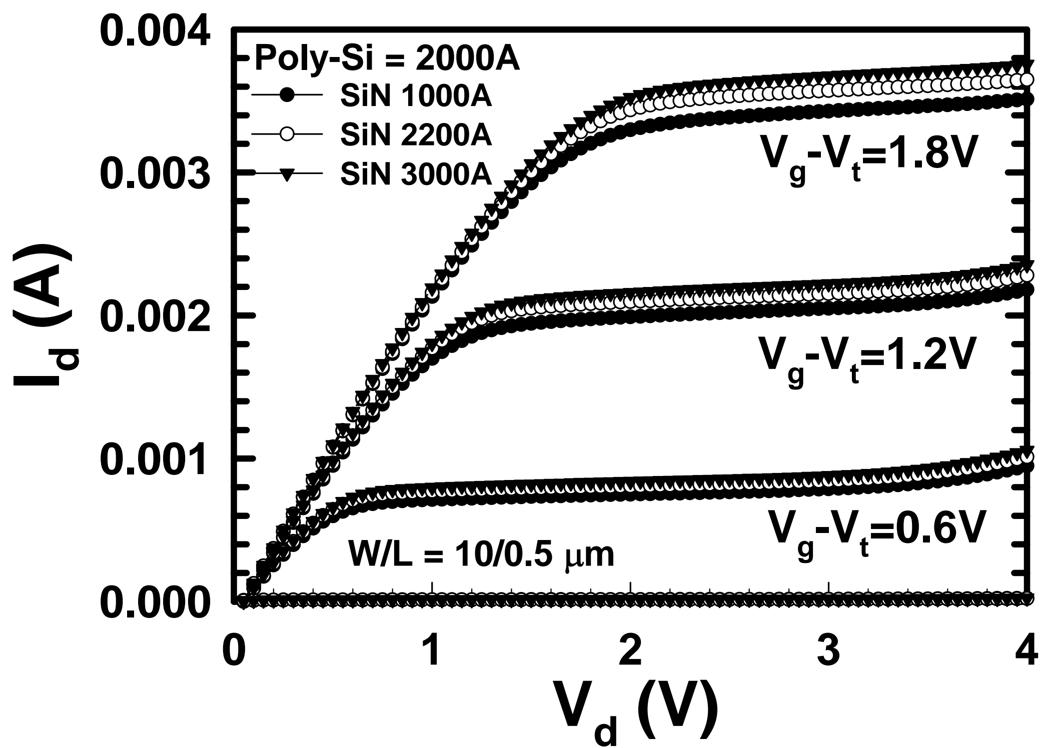


Fig. 3-2 Electrical I_d-V_d characteristics of devices using fixed single-poly-Si thickness (2000 Å) with various SiN capping layer thicknesses on (111) orientation substrate.

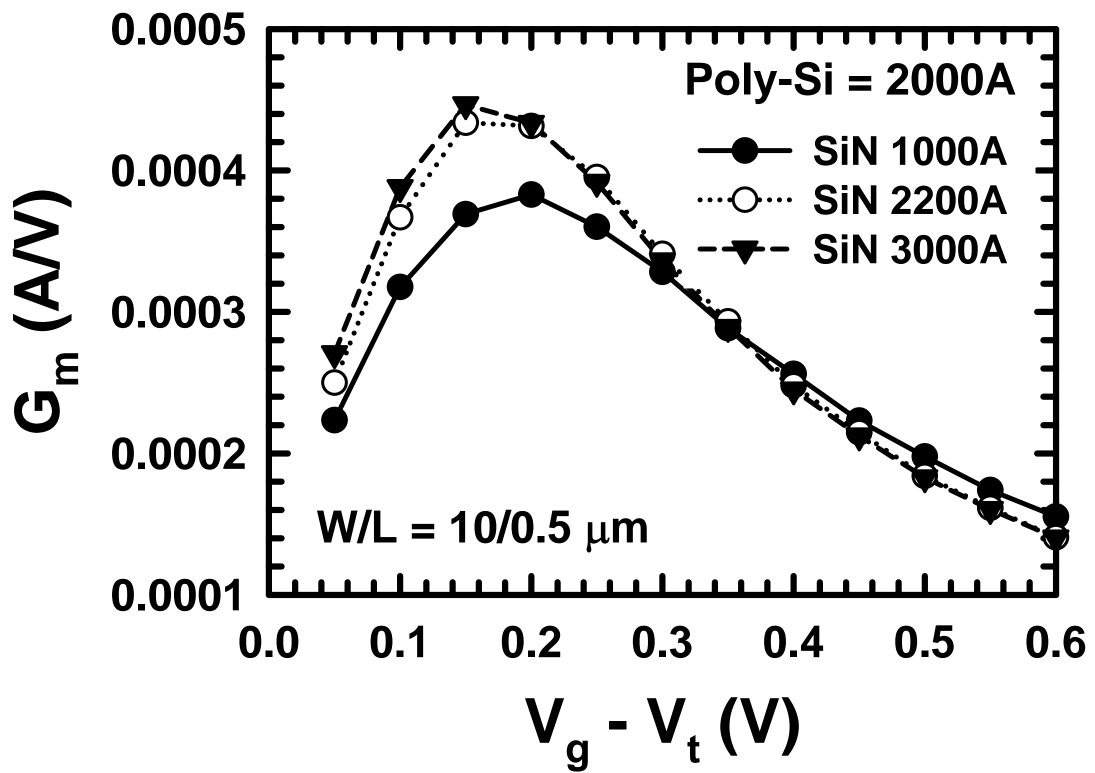


Fig. 3-3 G_m characteristics versus overdrive gate voltage for devices with various SiN capping layer thicknesses.

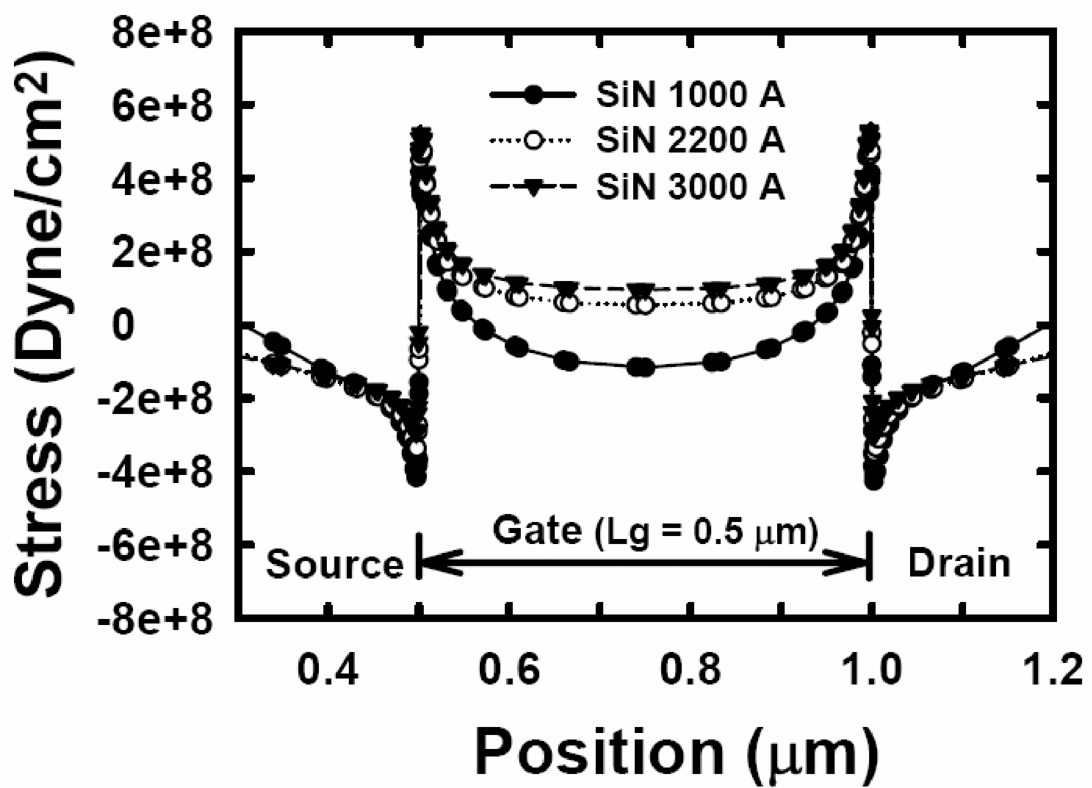


Fig. 3-4 2-D simulation results due to SiN-capping-layer-induced stress in channel region using SILVACO simulation tool. Negative values indicate compressive stress and positive values indicate tensile stress.

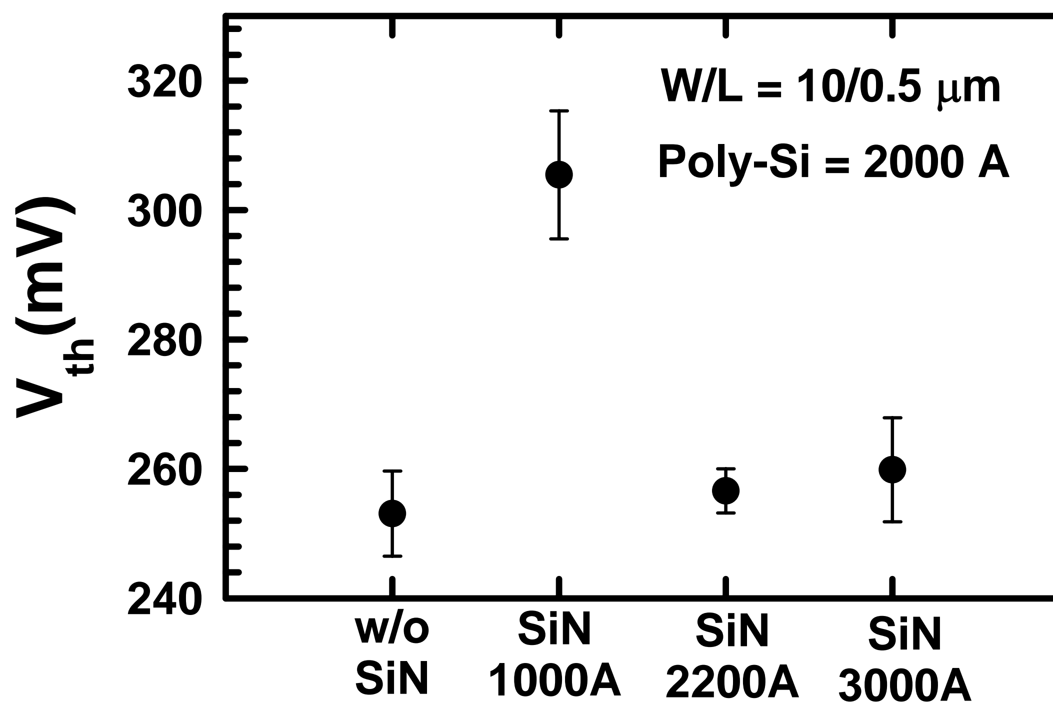


Fig. 3-5 Threshold voltages of devices with poly-Si = 2000 Å and different SiN thicknesses.

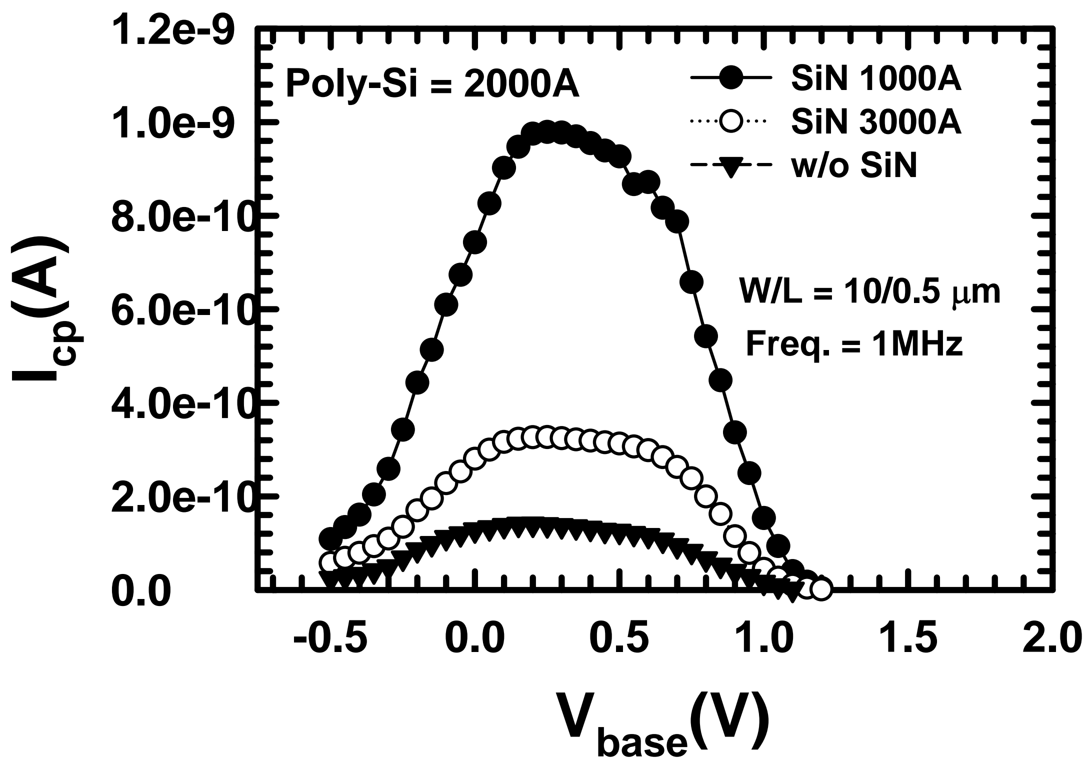


Fig. 3-6 Charging pumping current curves of devices with different SiN capping layer thicknesses.

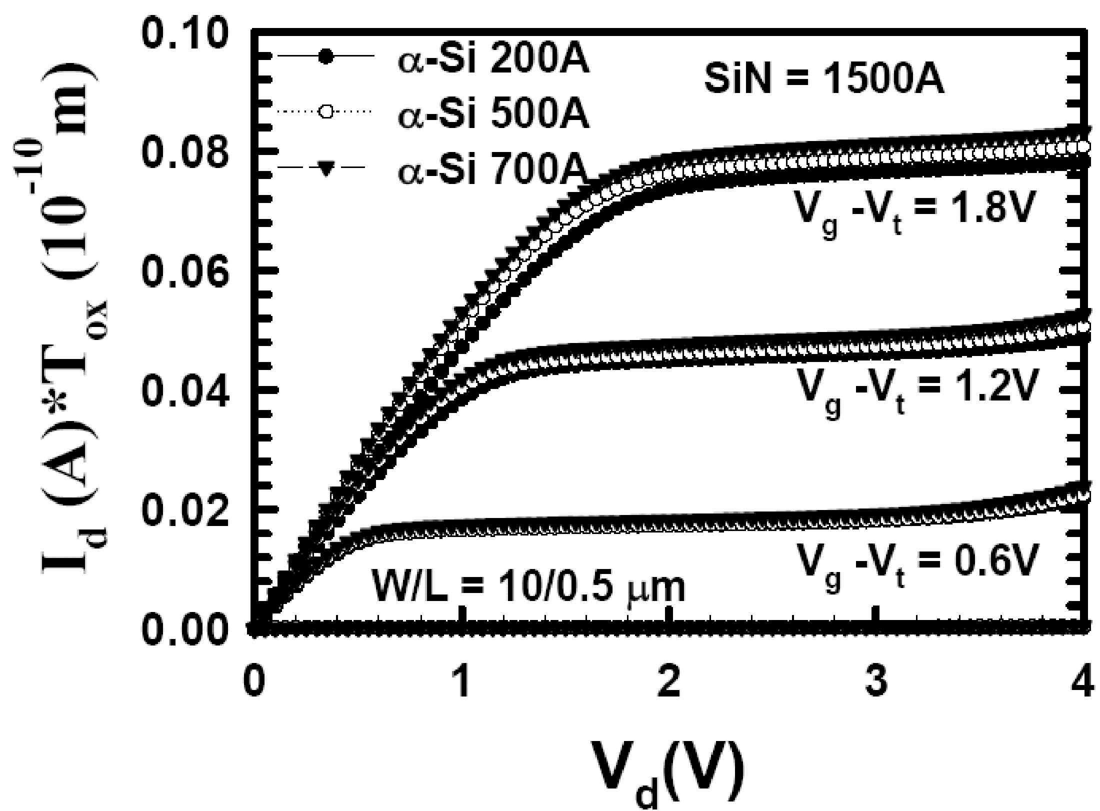


Fig. 3-7 I_d-V_d characteristics of devices with different α-Si thicknesses and fixed SiN capping layer thickness (1500 Å).

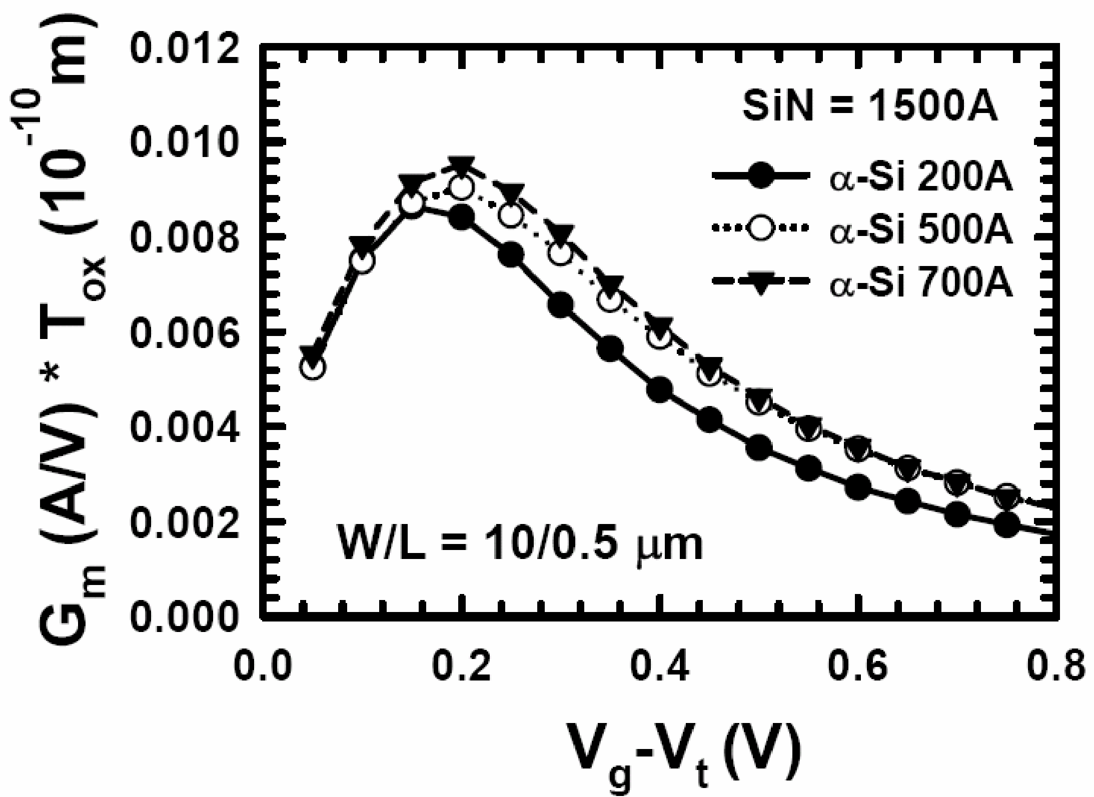


Fig. 3-8 Output characteristics of G_m for all devices with fixed SiN thickness (1500 Å) and various α-Si thicknesses in gate construction.

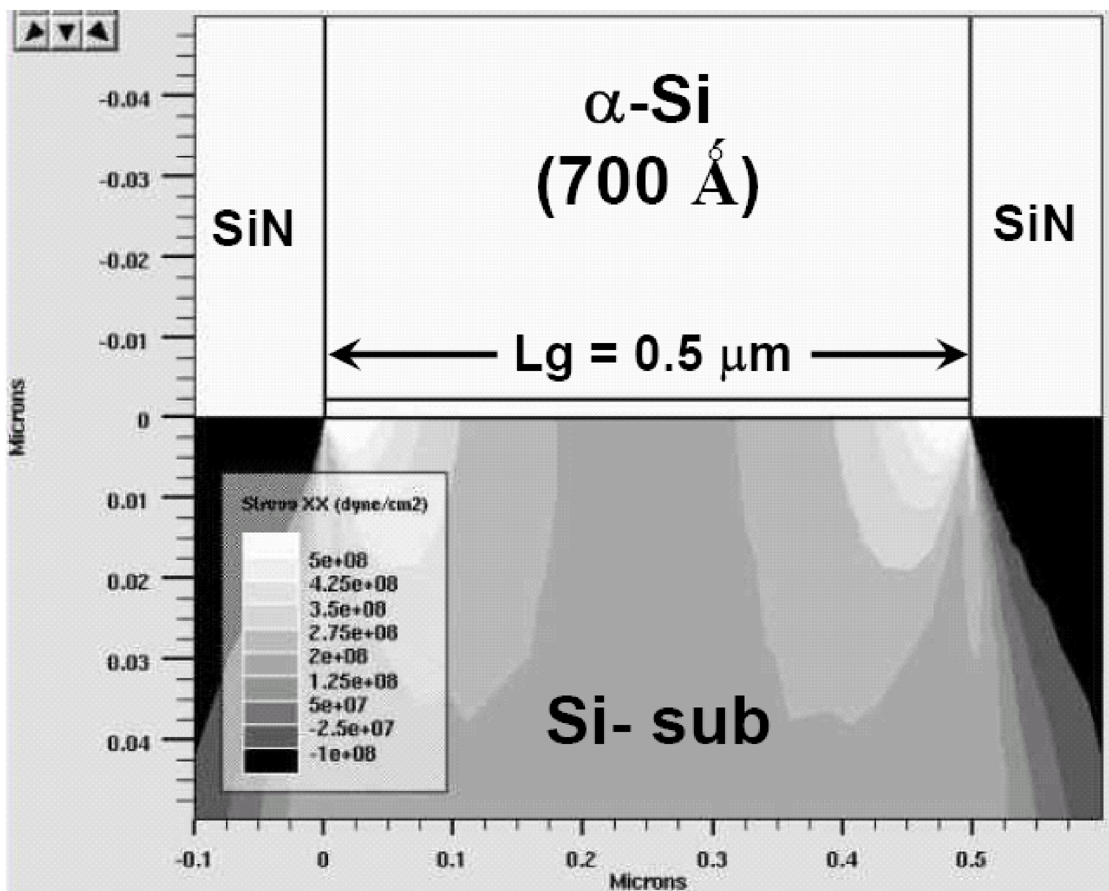


Fig. 3-9 Simulated 2-D stress distribution contour of NMOSFET with 700 Å α-Si on (111) orientation substrate.

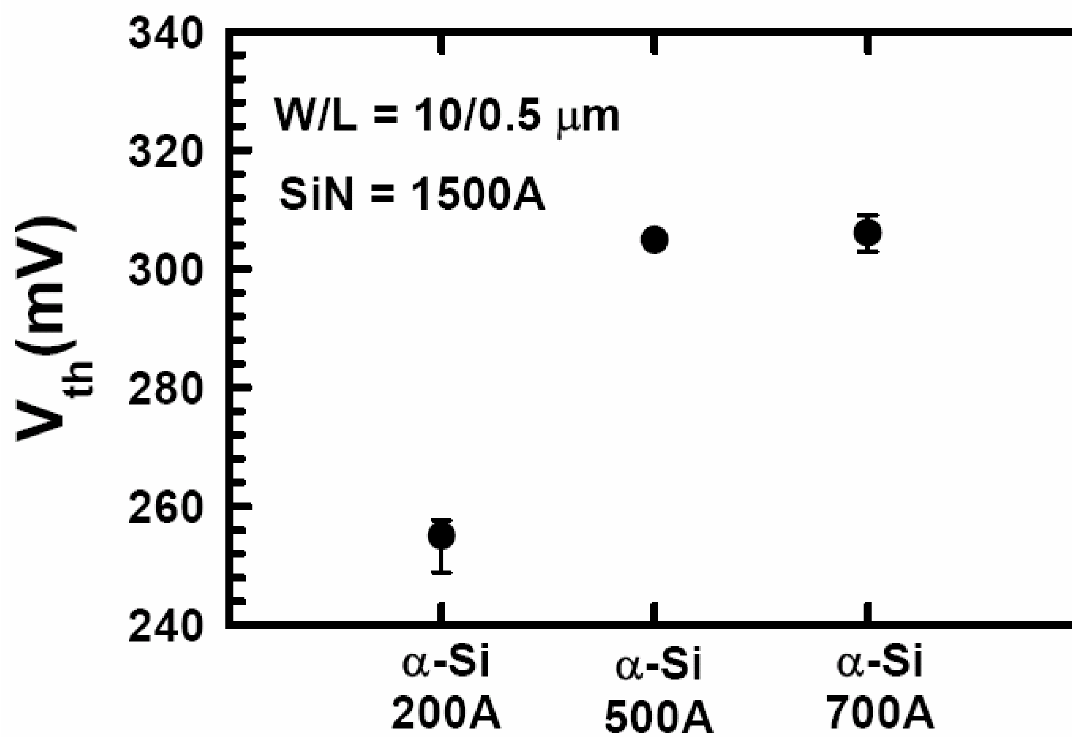


Fig. 3-10 Threshold voltages of devices with fixed SiN capping layer thickness (1500 Å) and various α-Si thicknesses.

Chapter 4

Systematical Study of Reliability Issues in Plasma-Nitrided and Thermally Nitrided Oxides for Advanced Dual-Gate Oxide PMOSFETs

4-1 Introduction

As IC technology enters sub- m dual-gate ultra-large-scale integration (ULSI) generation, nitrogen atoms are incorporated into silicon dioxide to block an undesirable boron penetration from a P^+ poly-gate electrode of a p-channel metal-oxide-semiconductor field-effect transistor (PMOSFET) [1-3]. Even for cutting-edge 65 nm complementary metal-oxide-semiconductor (CMOS) technology, nitrided oxide is still a key gate dielectric material for achieving a high device performance for both general and low-power applications [4-6]. On the other hand, devices feature dual gate oxide (DGO) processes in which thin oxide is used for core and logic circuits and thick oxide is used for input/output (I/O) and analog circuits, owing to the decreasing size and increasing number of system-on-chip applications. Consequently, reliability issues, such as negative-bias temperature instability (NBTI) [7-8, 20-21] and hot-carrier injection (HCI) [9-11], that could induce threshold voltage shift and performance degradation in DGO PMOSFETs become a serious concern for realizing highly reliable integrated CMOS devices. Therefore, both the concentration and distribution of nitrogen in

the gate oxide should be optimized since excessive nitrogen at the interface may induce interface traps, resulting in a reduced channel carrier mobility [12] and a degraded reliability [13].

In this study, the impacts of NBTI and HCI on core and I/O PMOSFETs between devices with plasma nitrided oxide (PNO) and devices with thermally nitrided oxide (TNO) were compared systematically. The mobility and constant overdrive current of the PMOSFETs fabricated using PNO as a gate oxide material are about 30% and 23% higher than those of the devices fabricated using TNO, respectively. The core PMOSFETs fabricated using PNO show a better NBTI and HCI immunity than those fabricated using TNO owing to the lower nitrogen concentration at the SiO_2/Si-substrate interface. However, the I/O PMOSFETs fabricated using PNO show a higher HCI-induced degradation rate because of a higher oxide bulk trap density but a better NBTI than the devices fabricated using TNO at a normal stressed bias due to a low interface trap density.

4-2 Experiment

PMOS devices were fabricated by state-of-the-art 300 mm wafer foundry technology. Shallow trench isolation (STI) was performed for devices isolation followed by super-steep retrograde well formation. After channel implantation, a DGO process was performed with different gate oxide thicknesses for low-power core and I/O devices. Following the thermal

base oxide growth, plasma nitridation post annealing and poly-silicon deposition steps were clustered together. The thermally nitrided oxide fabricated by exposing the oxide films to pure ammonia (NH_3) at an atmospheric pressure and high temperatures was used and compared with plasma nitrided oxide. After lightly-doped drain (LDD) and pocket implantation, tetraethoxysilane (TEOS) liner and low-temperature silicon nitride were processed in sequence to form a sidewall spacer. The fabrication of a heavily doped source/drain junction by BF_2 implantation was followed by rapid thermal annealing (RTA) and NiSi self-aligned silicidation.

Electrical characterizations, which included high-frequency capacitance-voltage (C-V) and current-voltage (I-V) curves and reliability tests, were performed using a Cascade probe station S-300, HP4156, and HP4284 system. Charge-pumping current measurements were also performed to extract the generation of interface states. NBTI stress tests were performed using a temperature-regulated hot chuck at 125°C, whereas HCI stress tests were performed under various with varied Vg = Vd stress bias conditions at room temperature.

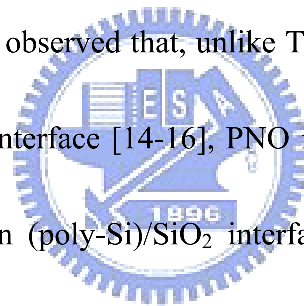
4-3 Result and Discussions

4-3-1 Material analysis and device performance of PNO and TNO PMOSFETs

Figure 4-1 shows a schematic illustration of nitrided oxide formation processes for both PNO and TNO. After base oxide growth, PNO and TNO were formed using nitrogen plasma

and NH_3 gas, respectively. The high-frequency C-V comparison between the TNO and PNO of core (1 MHz) and I/O (100 kHz) PMOS devices is shown in Fig. 4-2. The capacitance equivalent thicknesses measured in the inversion region of C-V (Tox_inv) are about 2.8 and 5.5 nm for low-power core and I/O PMOS devices respectively, for both PNO and TNO devices. The flat-band voltage difference between PNO and TNO I/O PMOSFETs is about 100mV.

Figure 4-3 shows the nitrogen concentration profiles of PNO and TNO for core devices analyzed by angle-resolved X-ray photoelectron spectroscopy (ARXPS). From the nitrogen concentration distribution, it is observed that, unlike TNO that incorporates a high amount of nitrogen into the SiO_2/sub-Si interface [14-16], PNO increases the concentration of nitrogen near the polycrystalline silicon (poly-Si)/SiO_2 interface. The normalized transconductance (Gm) of core PMOSFET devices as a function of gate overdrive voltage (V_g-V_{th}) is illustrated in the inset in Fig. 4-3. From the result, one observes that the hole mobility of PNO is always higher than that of TNO from a low field to a high field. The peak mobility is 31% higher for PNO devices. The degradation of the carrier mobility of TNO is attributed to the high interface trap density at the TNO SiO_2/sub-Si interface and/or the enhancement of coulomb scattering caused by a high nitrogen concentration [17-18]. Consequently, PMOSFET devices with PNO exhibit a higher driving current than those with TNO. The electrical I_d-V_d characteristics of the PNO and TNO core PMOSFETs are plotted in Fig. 4-4. As a result of the



low nitrogen incorporation into the oxide interface that induced a high mobility in the channel region, PNO devices exhibit a 23% higher drive current than TNO devices at V_g -V_t = -1.2 V.

4-3-2 NBTI and HCI comparison between PNO and TNO

To study the effects of interface trap density on the NBTI reliability of TNO and PNO PMOSFETs, a fixed base level charge pumping current measurement, in which a pulse with a high state voltage is fixed and a varying pulse low base level voltage is applied to the gate, was performed [19]. Figure 4-5 shows the charge pumping currents of PNO and TNO core PMOSFETs measured before and after a NBTI 4095 s stress at V_g = -2.5V at 125°C. Note that in order to remove the leakage current component during the charge pumping measurement, an incremental frequency charge pumping (IFCP) method [20], in which a correct charge pumping current is calculated by testing two charge pumping curves at different frequencies, was used. Both TNO and PNO devices show increasing charge-pumping currents after NBTI stressing, indicating an enhanced interface trap generation, particularly for TNO PMOSFETs. Compared with the fresh devices, the increases in charge pumping current after 4095 s NBTI stressing are 2.86 x 10^{-10} and 1.99 x 10^{-10} A for TNO and PNO, respectively. The calculated interface traps generation (ΔNit) and drain drive current degradation rate obtained by identical NBTI stress processed are plotted for both core TNO and PNO PMOSFETs, as depicted in Fig. 4-6. As observed from Fig. 4-6, not only the drain current degradation rate but

also the time dependence of interface trap generation follows a fractional power-law curve, which is in agreement with the previous literature [15]. Plasma nitridation suppresses the NBTI-induced drain current degradation. The amount of generated interface traps is lower for PNO than that of TNO, which is attributed to the low nitrogen concentration at the oxide interface. In addition, due to the superior capability of nitrogen plasma nitridation to pile up a high nitrogen concentration at the poly-Si/SiO_2 interface, which effectively blocks the penetration of boron to the SiO_2/sub-Si interface, TNO is also more vulnerable to boron-induced interface trap generation than PNO [21].

Figure 4-7(a) shows the time dependences of the threshold voltage degradation under various NBTI stress voltages for Core TNO and PNO devices. It is apparent that ΔV_{th} obeys a power-law dependence on stress time, as given by

$$\Delta V_{th} \propto t^{n}, \qquad \text{(eq. 4-1)}$$

where the exponent value n is found to be 0.25 for both TNO and PNO Core PMOSFETs. A similar exponent value has been recently reported, generally proving that this time dependence is due to the diffusion of hydrogen or hydrogen-related species in a diffusion-controlled electrochemical reaction model [22-23]. For PNO devices, the threshold voltage degradation by NBTI stress is lower than that for TNO devices under various stress voltages. To compare with core devices in Fig. 4-7(a), NBTI-induced threshold voltage degradation as a function of stress time for thick TNO and PNO I/O PMOSFETs are shown in

Fig. 4-7(b). The threshold voltage degradation for both TNO and PNO I/O devices are similar to that for thin nitrided oxide, indicating the power-law dependence and the PNO immunity to NBTI that is higher than the TNO immunity under various stress voltages in the range from -3.5 to -4.5 V.

Although the mean free path of holes in silicon is only about one-half of electrons, the hot-carrier-induced degradation of PMOSFETs has been critical as that of NMOSFETs. Figure 4-8(a) illustrates the time dependences of the threshold voltage degradation under various HCI stress voltages for Core TNO and PNO PMOSFETs at room temperature. Note that the HCI stress-bias conditions we used hereafter are all for $V_g = V_d$ since the positive oxide charge generation by hot holes injected into oxide is the most significant mechanism for deep-submicro-PMOSFETs with nitrided oxide [10]. The HCI-induced threshold voltage degradation of TNO and PNO Core PMOSFETs follows the power law dependence [eq. (4-1)], and in the bias range from -2.2 to -2.5 V, the threshold voltage degradation of PNO devices is always lower than that of TNO devices. The time dependences of the threshold voltage degradation under various HCI stress voltages from $V_g = V_d = -3.5$ to - 4.5 V for I/O devices are shown in Fig.4- 8(b). Although the initial threshold voltage shift of TNO PMOSFETs is higher than that of PNO PMOSFETs under the same bias conditions, the PNO PMOSFETs show a markedly higher degradation rate than the TNO PMOSFETs. At an electric oxide field higher than those mentioned above such as $V_g = V_d = -4.5$ V, the threshold voltage

degradation of the PNO devices is higher than that of the TNO devices. We will discuss this result more detail in next section.

4-3-3 Mechanism

Figure 4-9 shows the schematic illustration of the degradation mechanisms at NBTI and HCI stresses for core and I/O PMOSFETs with TNO and PNO, respectively. The exponent value in eq. (4-1) for the NBTI power law dependence is found to be 0.25 for both TNO and PNO core devices. This implies that the initial degraded value is strongly dependent on the number of interface traps for the NBTI of core thin nitrided oxide. On the other hand, for core PMOSFETs, TNO [Fig. 4-9(a)] shows a higher initial NBTI-induced degradation than PNO [Fig. 4-9(b)]. This can be attributed to the higher interface trap generation due to the higher nitrogen concentration at the SiO_2/sub-Si interface. In addition, for thick I/O oxide, the location where the interface traps and fixed positive oxide charges generated at NBTI "static" stress is relatively near the SiO_2/Sub-Si interface; therefore, for the NBTI reliability issue, the oxide interface quality is markedly more important for thick I/O oxide. This is the reason that the NBTI-induced degradation of I/O PNO devices [Fig. 4-9(d)] is always lower than that of I/O TNO devices [Fig. 4-9(c)] under the stress bias conditions in this study.

The degradation mechanism of HCI is different from NBTI. For HCI stress at $V_g = V_d$, holes exhibit a high energy owing to impact ionization and are injected into gate oxide

directly. In addition to the interface traps, the oxide bulk traps (N_{ot}) are also an important factor of HCI-induced degradation. However, for thin oxide whose thickness is smaller than 3 nm, the effect of the oxide bulk traps is insignificant and the interface traps are a predominant factor. For this reason, the core PMOSFETs with TNO show a higher initial degraded value than the core PMOSFETs with PNO owing to a higher nitrogen concentration at the oxide interface, but the exponent values for the degradation rate at HCI stress are similar for the TNO and PNO Core devices. In contrast, for I/O devices with Tox_inv of 5.5 nm, the plasma-induced oxide traps in the oxide bulk of PNO, when hot holes are injected into oxide, have a higher probability to be captured, forming charged oxide defects, than those in the oxide bulk of TNO. Although the initial degraded value of PNO at HCI stress is smaller than that of TNO owing to the lower number of interface traps, PNO I/O devices show a markedly higher degradation rate (higher exponent value of power law dependence) owing to a higher number of oxide traps, which are induced by plasma implantation.

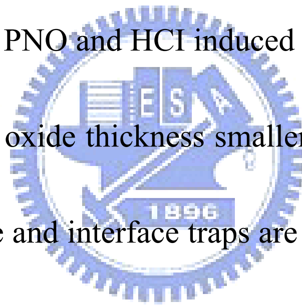
To prove this mechanism, the charge trapping characteristics were measured and are shown in Fig. 4-10. The normalized gate current density during Fowler-Nordheim (FN) stress at an electric field of about 10 MV/cm is plotted versus stress time for large-area PMOS capacitors with core and I/O TNO and PNO, respectively. The normalized gate current density is defined as $(J_g - J_{g0}) / J_{g0}$, where J_{g0} is the initial gate current density of the devices and J_g is the gate current density after FN stress. As observed, for 5.5-nm-thick I/O oxide, the normalized gate

leakage current density increases with stress time for both TNO and PNO PMOS devices, whereas PNO shows a higher rate of J_g increase than TNO. This result indicates that for thick I/O nitride oxide, there are more oxide defect traps in the oxide bulk of PNO, causing a higher number of holes trapped than in that of TNO. For the thin oxide of core devices, the J_g increases at constant voltage stress are lower than 1% and are negligible for both TNO and PNO capacitors. These should be due to the elimination of oxide traps and direct tunneling being the dominate mechanism for thin oxide. Furthermore, Figure 4-11 shows the electrical stress-induced leakage current (SILC) phenomena before and after a constant gate bias stress of 5.5V as functions of positive gate voltages of the TNO and PNO I/O capacitors. From the evolution of the J_g characteristics during stress, it is observed that PNO exhibits a larger SILC increase than TNO. Since the SILC has been explained to be due to a trap-assisted tunneling mechanism occurring in bulk oxide defects [24], the larger SILC of PNO indicates a higher oxide trap defect density, which is consistent to the proposed mechanism in Fig. 4-9.

The results of this work are summarized in Table 4-1. Owing to a lower interface trap density, PNO shows higher immunities to HCI and NBTI for core devices and a higher NBTI immunity for I/O devices when compared with TNO. However, due to the higher oxide trap density in thick I/O devices for PNO, PNO shows a higher HCI-induced degradation rate than TNO.

4-4 Summary

In this study, we have performed a systematical investigation of reliability issues, such as NBTI and HCI, for core and I/O PMOSFETs with TNO and PNO. As a result, the devices with TNO exhibit a lower NBTI immunity owing to the higher nitrogen concentration at the SiO_2/sub-Si interface than those with PNO, generating more interface traps during NBTI stress. In contrast, for HCI under the stress conditions of hot-hole injection, bulk oxide traps are an important factor for device degradation. For thick I/O devices, plasma induces more oxide traps in the bulk oxide of PNO and HCI induced a higher degradation rate than those for TNO devices. However, for an oxide thickness smaller than 3 nm in core devices, the effects of the oxide traps are negligible and interface traps are a predominant factor. This makes Core PMOSFETs with PNO have a higher immunity to HCI than those with TNO.



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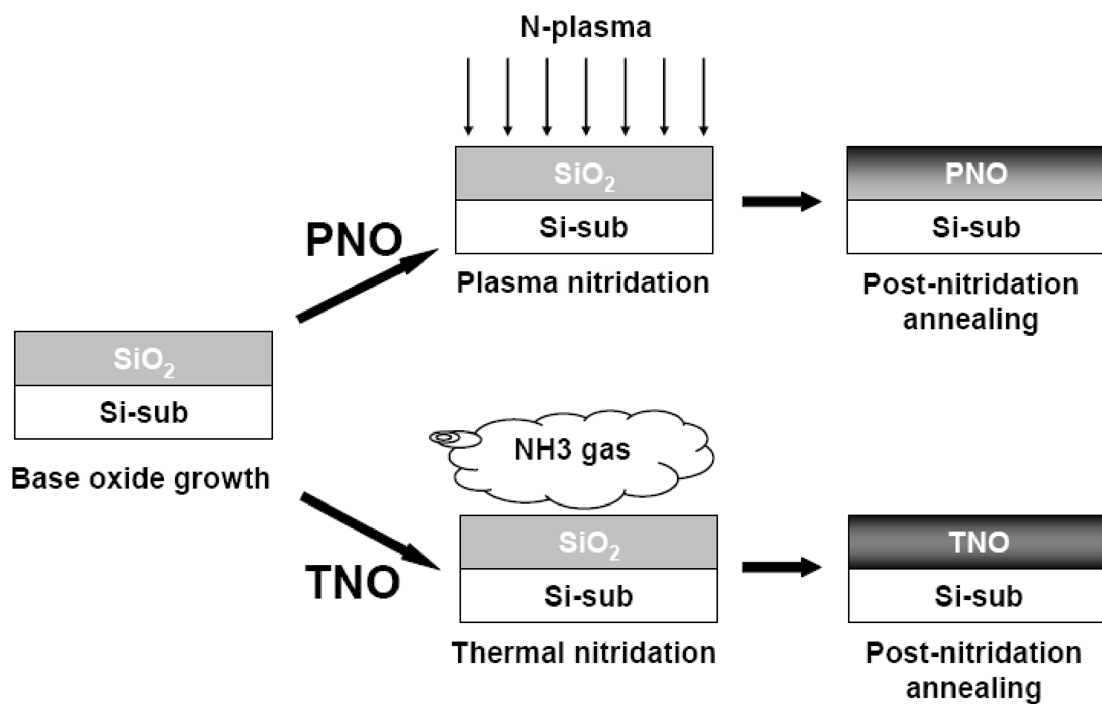


Fig. 4-1 Schematic illustration of nitrided oxide formation processes for PNO and TNO.

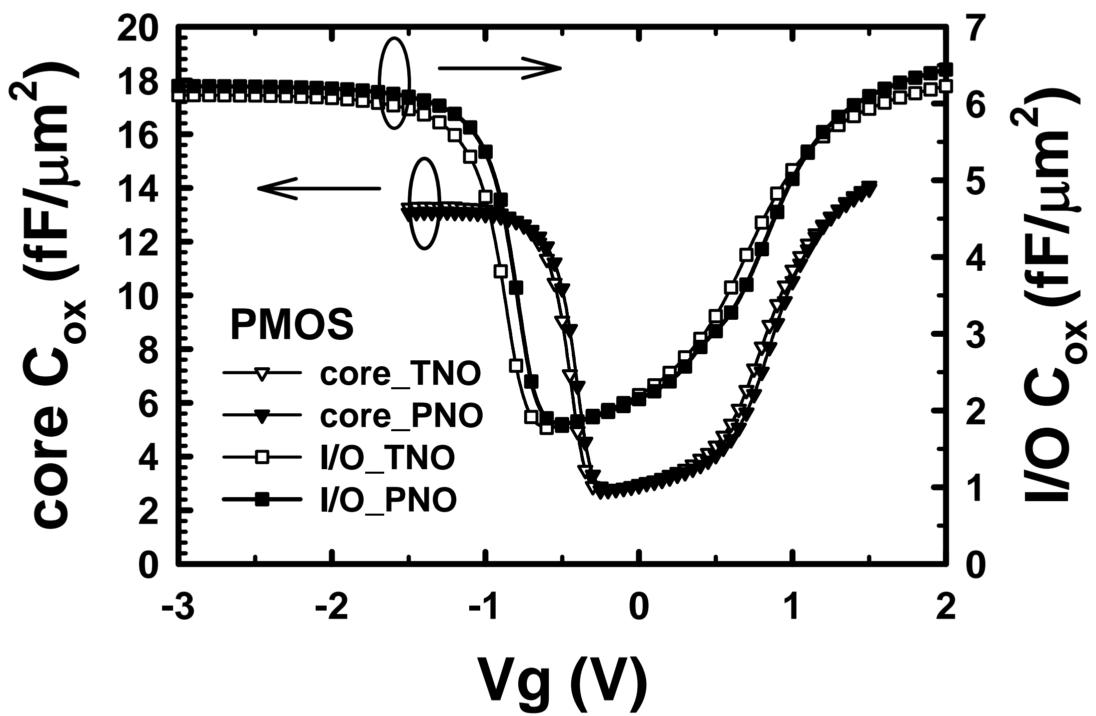


Fig. 4-2 High-frequency C-V characteristics of Core and I/O PMOS devices with gate dielectrics of PNO and TNO. The measurement frequency for core devices is 1 MHz and that for I/O devices is 100 kHz.

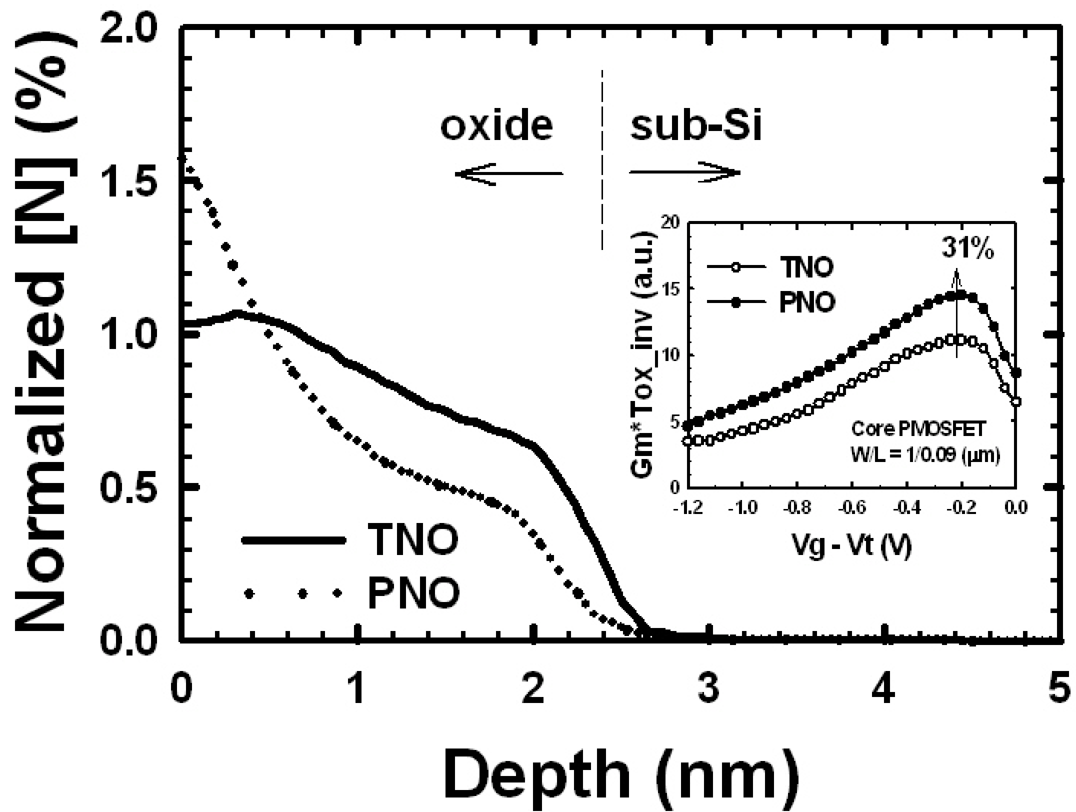


Fig. 4-3 Nitrogen concentration profiles of PNO and TNO in nitrided oxide analyzed by ARXPS. The insert shows the normalized Gm of core PMOSFETs as a function of V_g-V_{th} for both PNO and TNO.

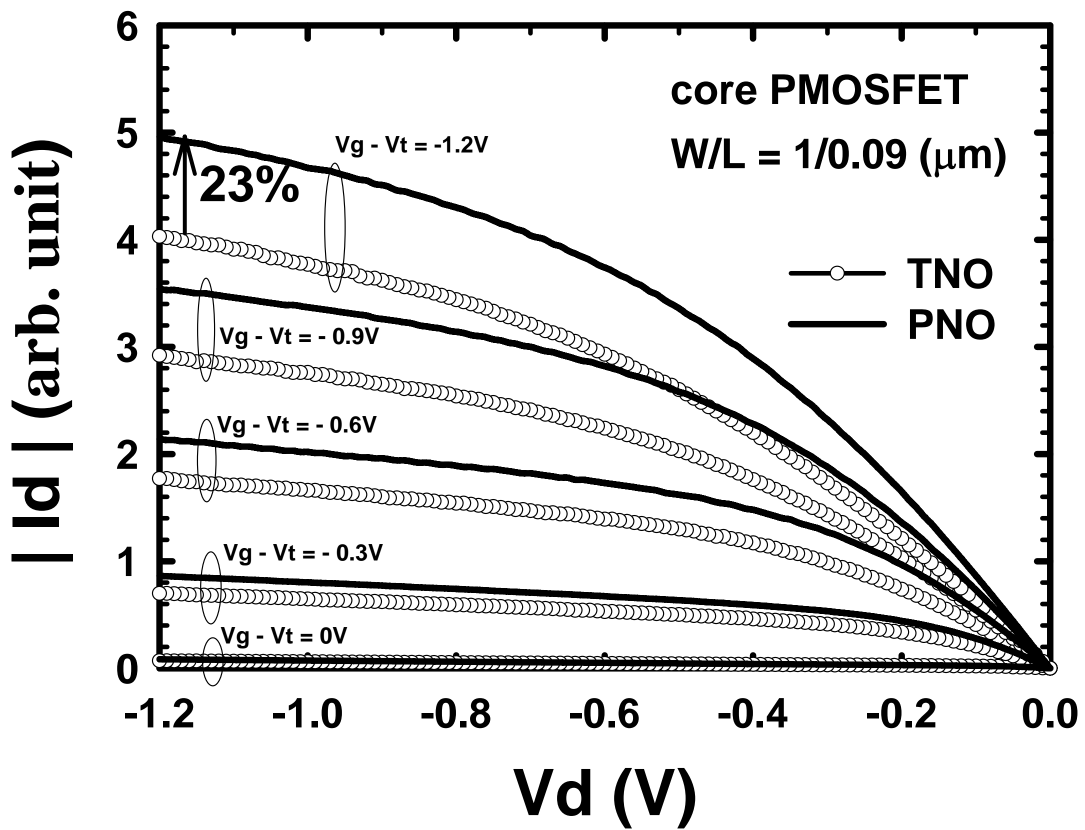


Fig. 4-4 Comparison of Id-Vd characteristics between PNO and TNO for Core PMOSFETs at Vg – Vt from 0 to -1.2 V with steps of -0.3 V.

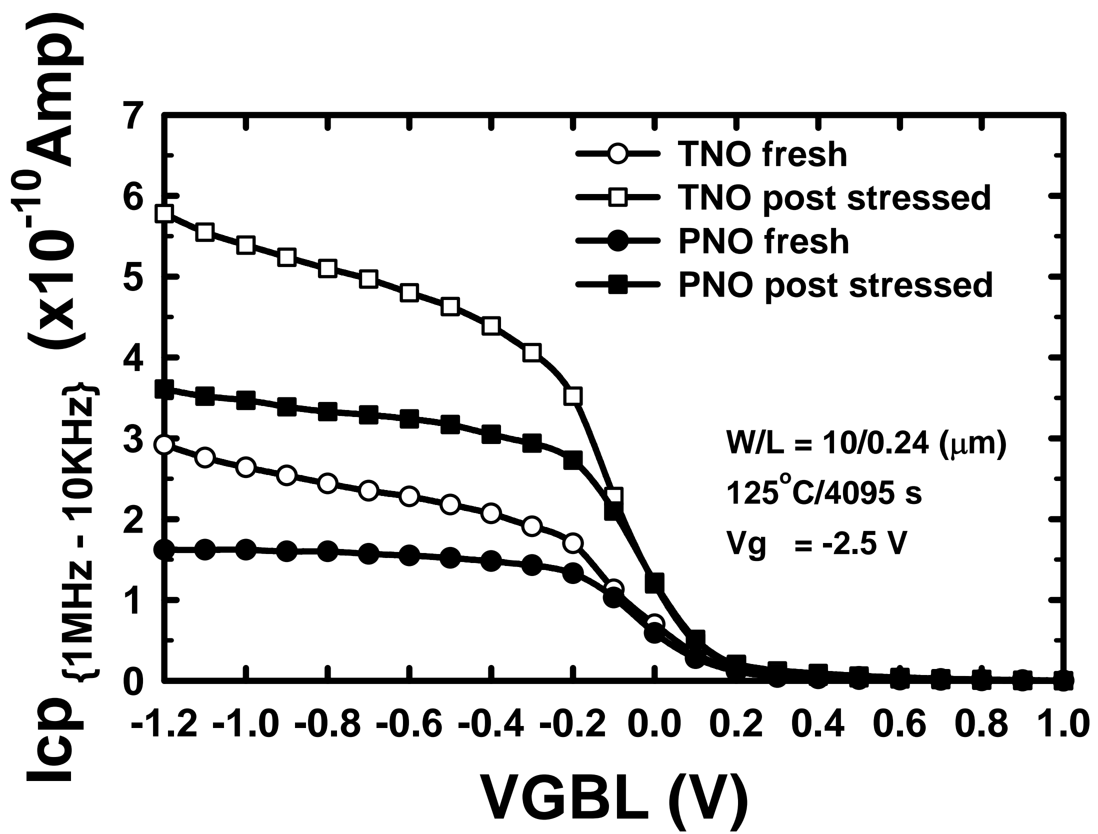


Fig. 4-5 Charge pumping currents of PNO and TNO Core PMOSFETs before and after 4095 s NBTI stress at Vg = -2.5 V at 125°C.

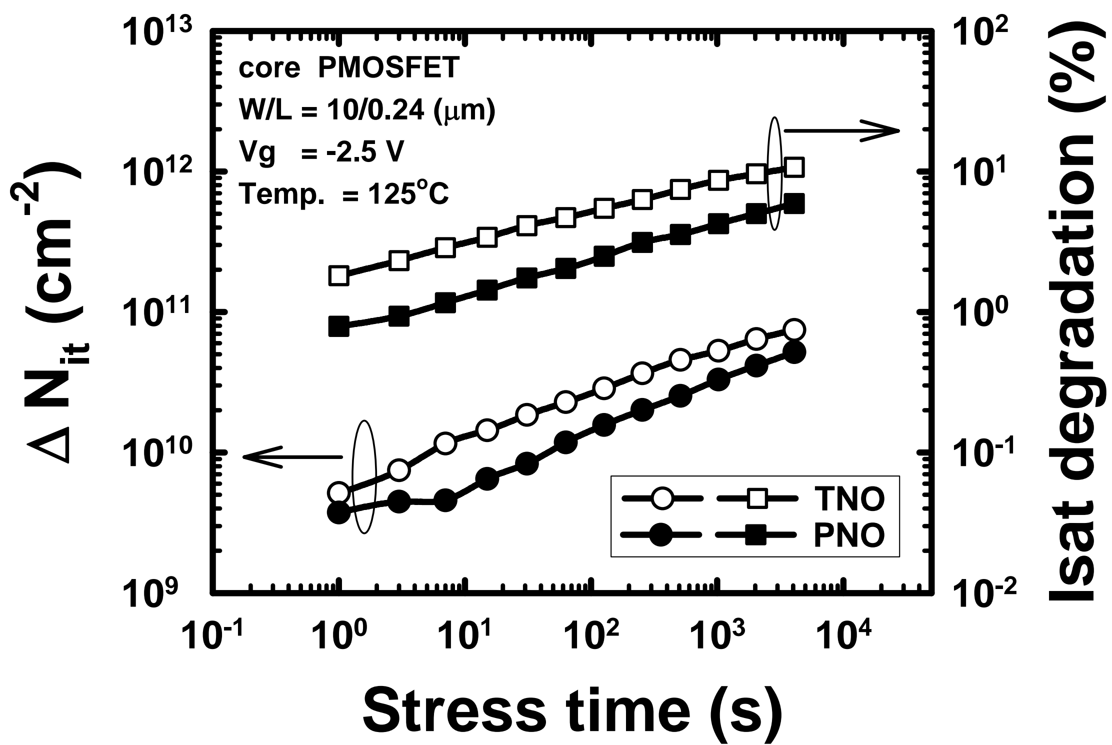


Fig. 4-6 NBTI-induced interface trap generation (Nit) and drive current degradation as functions of stress time for both PNO and TNO PMOSFETs. The stress bias Vg is -2.5 V and the temperature is 125°C.

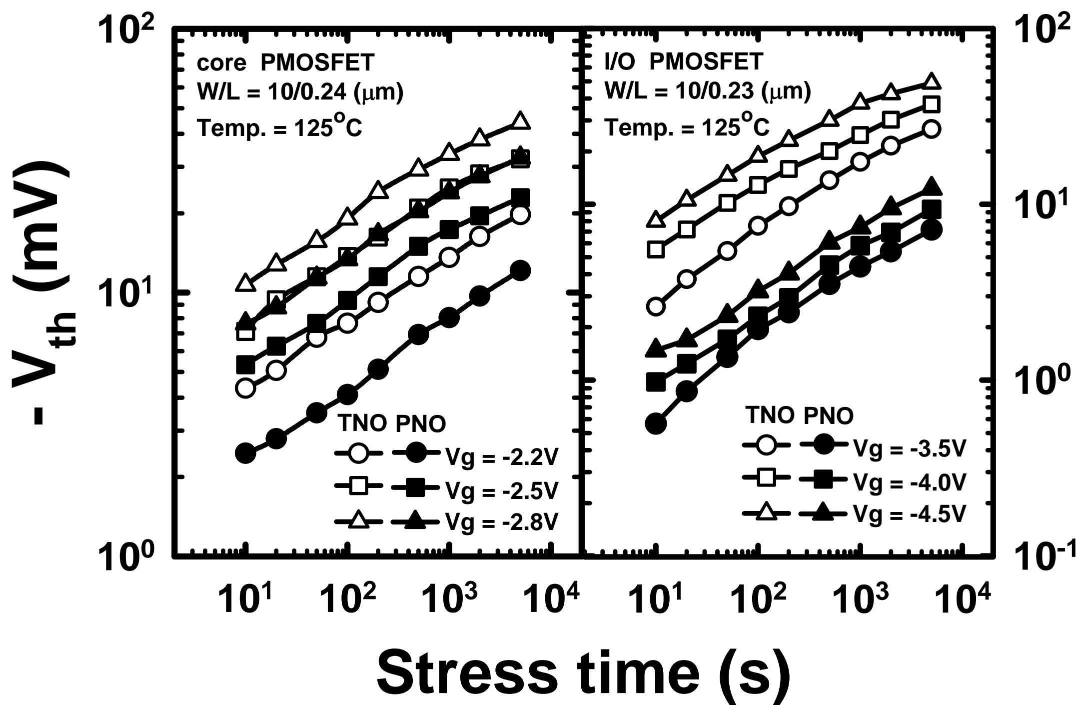


Fig. 4-7 Time dependences of NBTI-induced Vth degradation at various stress biases from -2.2 to -2.8 V per -0.3 V at 125°C for PNO and TNO for (a) core and (b) I/O PMOSFETs.

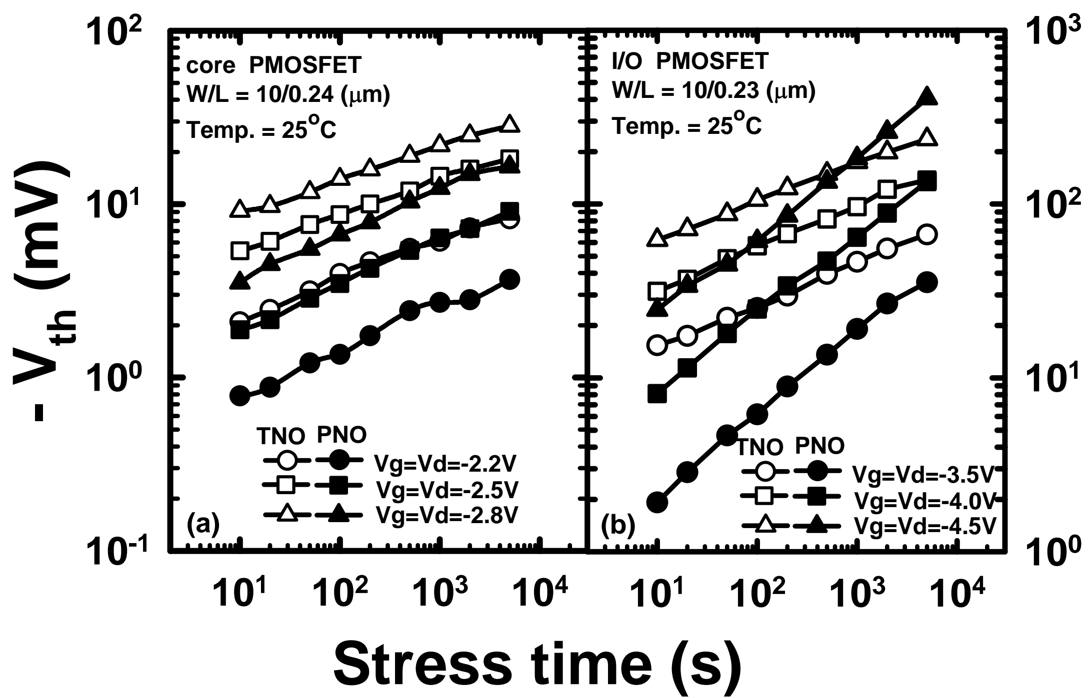


Fig. 4-8 HCI-induced Vth degradation, at various stress biases versus stress times of PNO and TNO for (a) Core and (b) I/O PMOSFETs. The stress bias conditions used are Vg = Vd from -2.2 to -2.8 V with steps of -0.3 V.

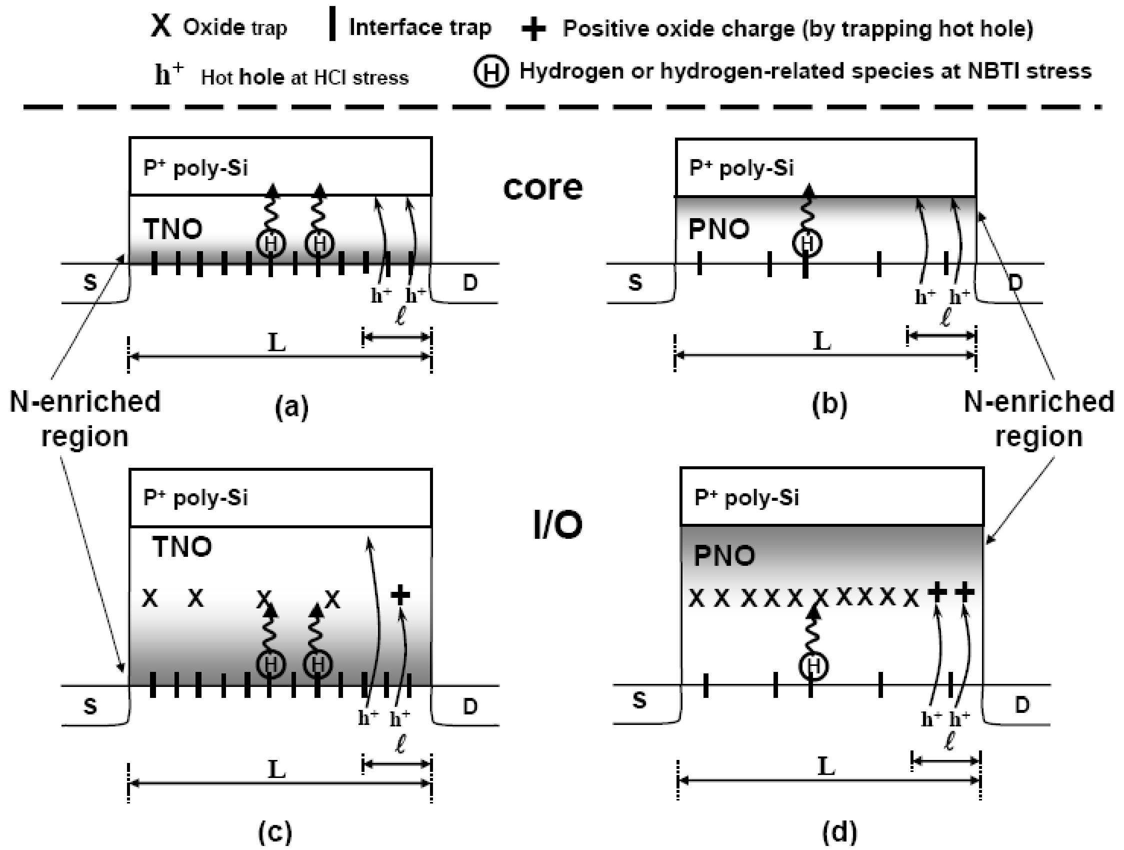


Fig. 4-9 Schematic illustration of degradation mechanism for (a) core TNO, (b) Core PNO, (c) I/O TNO, and (d) I/O PNO devices. "L" and "ℓ" indicate the channel regions where NBTI and HCI effects on devices are observed, respectively.

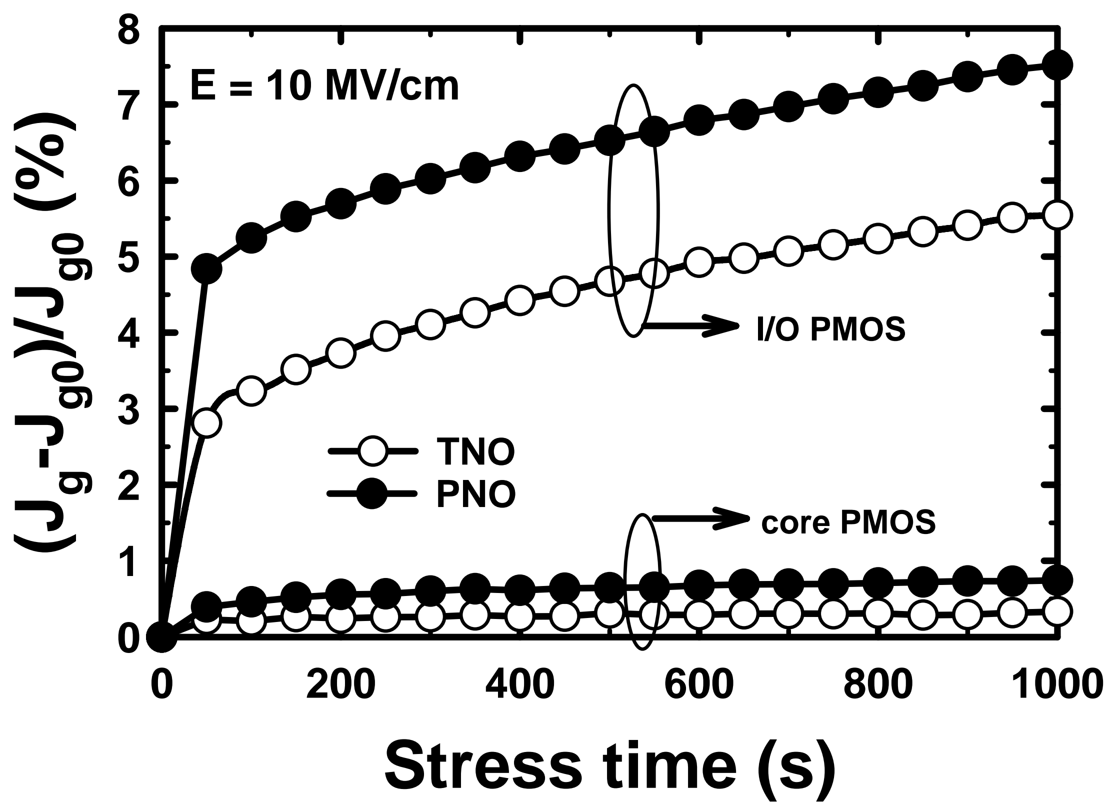


Fig. 4-10 The normalized gate current density ((Jg – Jg0)/Jg0) at a constant gate voltage of electric field is about 10 MV/cm versus the stress times of PNO and TNO core and I/O PMOS capacitors.

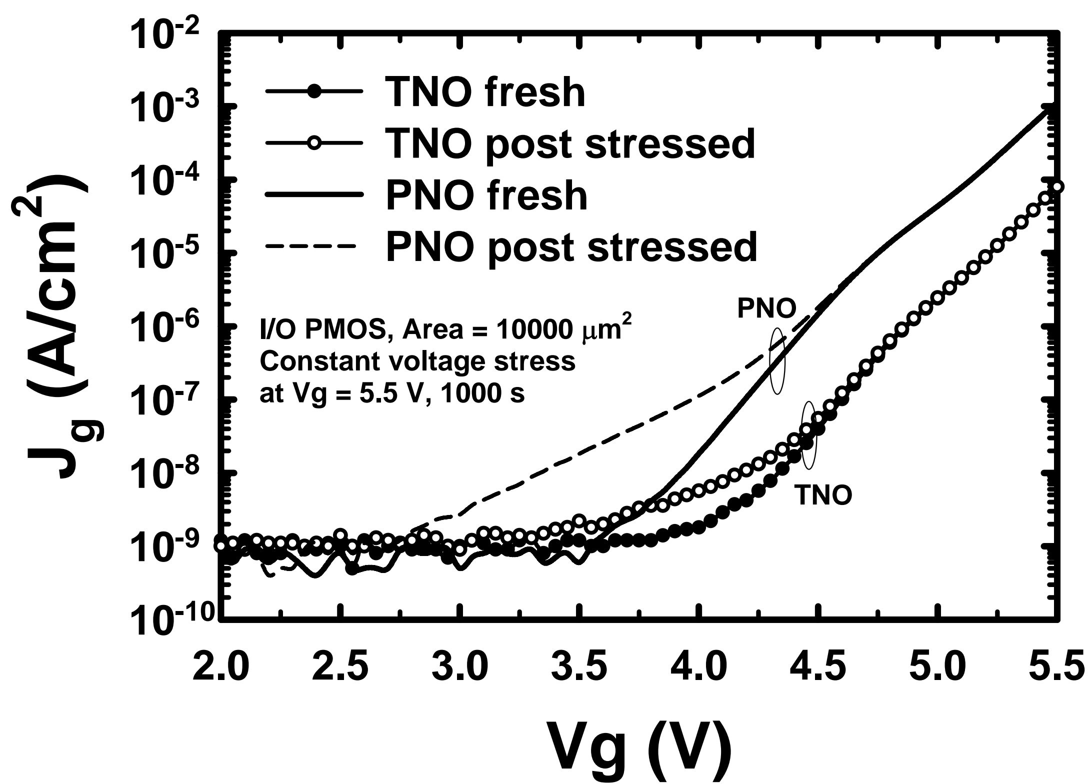


Fig. 4-11 SILC phenomena of Jg before and after constant 1000 s voltage stress of Vg = 5.5 V, as function of measured gate voltage of I/O PMOS capacitors with PNO and TNO oxides.

		core	I/O
NBTI Interface trap (N_{it}) and fixed oxide charge (N_f) generations	Result	PNO > TNO	PNO > TNO
	Due to	Less N_{it} for PNO	Less N_{it} for PNO
HCI at Vg=Vd High-energy hole injected from drain side into oxide --> localized N_{it} and N_{ot}	Result	PNO > TNO	TNO > PNO
	Due to	Less N_{it} for PNO	More N_{ot} for PNO
Comment		Impact of oxide trap (N_{ot}) was eliminated for Tox < 3 nm	Plasma induced more oxide traps (N_{ot}) in oxide bulk for PNO

Table 4-1 Summary of effect and mechanisms of NBTI and HCI on core and I/O PMOSFETs with PNO and TNO oxides.

Chapter 5

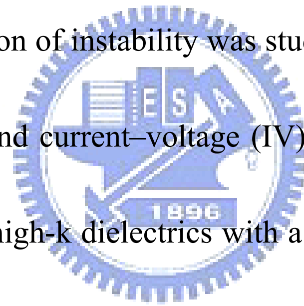
The Comparisons of Trapping and De-trapping effects in Positive Bias Temperature Instability Stress between HfO_2 and HfSiON Gate Dielectrics

5-1 Introduction

As CMOS devices are scaling down aggressively, it has become necessary to identify alternate high-k gate dielectrics that meet the stringent requirements for low leakage current and thin equivalent oxide thickness (EOT) [1-5]. High-k dielectrics are especially advantageous for low-power application and for thickness uniformity control owing to the thicker physical thickness. Among high-k gate dielectric materials, Hf-based gate dielectric including HfO_2 and Hf-silicate are the attractive materials because it has good device characteristics and is compatible with the conventional polysilicon gate process [6-9]. However, before Hf-based gate dielectrics being successfully integrated into future technologies, their reliability characteristics still need to be better identified. Bias temperature instability (BTI) has been recognized as one of the critical concern in the reliability of modern CMOS devices. Many of the past BTI researches on the SiO_2 dielectric have just focused on the negative BTI (NBTI) on PMOS devices [10-11], since it impacts more the devices reliability with respect to positive BTI (PBTI) on NMOS [12]. In conventional SiO_2 gate oxides, NMOS under PBTI stress shows little threshold voltage degradation and hence is not

a reliability concern while PMOS under NBTI stress has a continued reliability issue as the gate oxide thickness is scaled thinner.

On the contrary, unlike conventional SiO_2 gate dielectrics, NMOS positive bias temperature instability (PBTI) could be a potential scaling limit of CMOS technology with Hf-based gate dielectrics [13]. Most of the previous studies showed a significant positive threshold voltage shift for the high-k gate stack under PBTI stressing, which was attributed to the preexisting traps in the high-k layer or the hole induced oxygen vacancy traps [14-18]. In addition, one of main issues for high-k gate dielectrics is the charge trapping/de-trapping characteristics during reliability test. Initial observation of instability was studied through capacitance–voltage (CV) characteristics in V_{fb} change and current–voltage (IV) in V_{th} change. Since electrons can be trapped and de-trapped in the high-k dielectrics with a minimal residual damage to its atomic structure, a V_{th} instability associated with electron trapping/detrapping in high-k layer can significantly affect the transistor performance [19]. Nevertheless, it also complicates the evaluation of the effects of stress-induced defect generation phenomenon on the high-k gate dielectrics, which typically is not an issue in the case of SiO_2 dielectrics [20]. In order to investigate the additional electron trapping effects on top of defect generation, a de-trapping step has been proposed for studying generation of the electron trapping process and its impact on high-k device reliability [21]. Recently, the electron de-trapping behavior in the high-k films has used under specific gate bias conditions identifying charge trapping and relaxation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mechanism [22]. However, the dependence of the dielectric electrical characteristics on the de-trapping conditions has not been investigated in detail.

In this work, the comparison of trapping/de-trapping effect under PBTI stress test between NMOSFETs with HfO_2 and Hf-silicates (HfSiON) high-k dielectrics has been investigated. We just primary focus on NMOS devices PBTI here since it is more significant than PMOS NBTI in the case of Hf-based dielectrics MOSFETs.

5-2 Experiment

NMOS devices were fabricated by state-of-the-art 300 mm wafer foundry technology. Shallow trench isolation (STI) was performed for devices isolation followed by super-steep retrograde well formation. The high-K dielectric including HfO_2 and Hf-silicate were deposited by atomic-layer deposition (ALD). Chemical oxide was used as the interfacial layer unless it is specifically mentioned. The nitridation of HfSiO with Hf/(Hf+Si) ratio of 50% was carried by NH_3 annealing in the ambient. After shallow source/drain extensions and pocket implantation, tetraethoxysilane (TEOS) liner and low-temperature silicon nitride were processed in sequence to form a sidewall spacer. Modified S/D implants were adopted to improve activation and junction capacitance while maintaining good SCE. The fabrication of a heavily doped source/drain junction by implantation was followed by a rapid thermal annealing (RTA) of 1000 ^{o}C for 5s for S/D activation and thermal stability of HfSiON.

5-3 Results and Discussion

5-3-1 Device performance

Figure 5-1 shows the high-frequency C-V characteristics at 100 kHz for HfO_2 and HfSiON gate dielectrics, respectively. The well C-V characteristics under accumulation, depletion and inversion regions can be observed in this work for both HfO_2 and HfSiON gate dielectrics. The effective oxide thickness was also extracted from these C-V curves under accumulation without considering quantum effects. Since the EOT were almost the same (1.3 nm) for HfO_2 and HfSiON gate dielectrics as shown in Fig. 5-1, therefore, the reliability test can be analyzed by biasing the same gate voltage in this work. The effective electron mobility measured on HfO_2 and HfSiON gate dielectrics using split CV method is shown in Fig. 5-2. The effective mobility was almost the same for both HfO_2 and HfSiON gate dielectrics at low electric field as shown in this figure. However, at a higher field (>1 MV/cm), the mobility of HfSiON gate dielectrics was large than HfO_2 gate dielectrics, we speculate that the Si-O and Si-N bodings were formed for the HfSiON gate dielectrics resulting in annihilation of oxygen vacancies to offer mobility enhancement at high electric field. This result indicates that the HfSiON gate dielectrics can be suitable for high performance application. Besides, the effective mobility can meet the universal curve well at a higher field for both HfO_2 and HfSiON gate dielectrics as shown in inset of Fig. 5-2.

5-3-2 PBTI degradation for HfO_2 and HfSiON gate dielectrics

To understand the mechanism of PBTI in our high-k dielectrics, Fig. 5-3 shows the threshold voltage degradation (ΔV_{th}) of HfO_2 and HfSiON gate dielectrics under the same PBTI stress (Vg = +2.5 V) at room temperature. It is worth to note that the HfSiON dielectric leads to an obvious reduction in ΔV_{TH} under PBTI stress. Figure 5-4 shows the charge pumping current (I_{CP}) before and after PBTI stressing at +2.5V for HfO_2 and HfSiON. Contrast to ΔV_{th} , the HfO_2 gate dielectrics had better HfO_2/Si interface due to its less initial I_{CP}. However, although HfSiON dielectrics had larger initial I_{CP} than HfO_2, the increase in I_{CP} during PBTI stress was almost the same for HfO_2 and HfSiON gate dielectrics, as shown in Fig. 5-5. Furthermore, from the equation of charge pumping current as followed [23]:

$$I_{CP} = q \times N_{it} \times f \quad \text{(eq. 5-1)}$$

where q is electron charge, and f is measurement frequency. We can extract the number of interface trap generated during PBTI stress. Figure 5-6 shows the extracted result of Nit generation for both of HfO2 and HfSiON dielectrics, which is consist with Fig. 5-5. It should be noted that the N_{it} increase for both HfO_2 and HfSiON dielectrics is quite low ($< 2\times10^9$ cm^{-2}) in this work.

Furthermore, if we assume that the threshold voltage shift during PBTI stress is only contributed by generated interface trap ΔN_{it} and generated oxide bulk trap ΔN_{ot}, the equation can by expressed as followed [24]:

$$\Delta V_{th} = \frac{q}{C_i} \times (\Delta N_{it} + \Delta N_{ot}) \qquad \text{(eq. 5-2)}$$

where q is electron charge, and C_i is inversion capacitance. As eq. 5-2 and the results from Fig 5-3 to Fig. 5-6, the generated oxide trap (N_{ot}) during PBTI stress can be easily extracted in this work. Figure 5-7 shows the N_{ot} increase for both of HfO_2 and HfSiON dielectrics during PBTI stress, respectively. The HfSiON dielectric leads to an obvious reduction in ΔN_{ot} during PBTI stress as compared to HfO_2. The ΔN_{ot} is larger than 4×10^{12} cm^{-2} after 6000s PBTI stress for HfO_2 dielectrics while the ΔN_{ot} of HfSiON is smaller than 4×10^{12} cm^{-2}. This result demonstrates that the HfSiON thin film quality is better than HfO_2. As mentioned previous, the HfSiON gate dielectrics had the extra Si-O and Si-N bodings resulting in annihilation of oxygen vacancies, resulting in PBTI reduction for HfSiON dielectrics. On the other hand, it is worth to note that all these results show the ΔN_{ot} is about 2~3 orders larger than ΔN_{it}, indicating that the generated oxide trap will dominate the PBTI degradation characteristics for Hf-based gate dielectrics. Thus, the charge trapping model for Hf-based gate dielectrics under PBTI stress was illustrated in Fig. 5-8. At first, a little electron named as $I_{\text{Interface Trap}}$ will immediately trap in HfO_2/Si interface while the positive bias was applied in device. Then, the most of electrons $I_{\text{Bulk Trap}}$ will tunnel from Si substrate through the interfacial layer and are trapped at the bulk oxide, as shown in the schematic energy band diagram. However, there are still some electrons, which directly through the gate dielectrics named as I_{tunnel}.

5-3-3 Temperature-dependent de-trapping characteristics for HfO_2 and HfSiON gate dielectrics

In this section, the temperature-dependent trapping and de-trapping characteristics for both of HfO_2 and HfSiON were compared. After each biasing stress and sensing cycle, the stress bias was removed and held up for 0 and100 seconds respectively to examine the electron de-trapping characteristics.

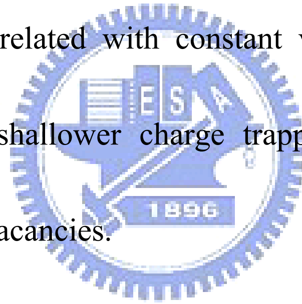
In Fig. 5-9, we compare the HfO_2 and HfSiON gate dielectrics under PBTI stress (Vg = +2.5 V) with no hold time at different temperatures, including 25, 75 and 100 ^{o}C. The ΔV_{TH} in PBTI stress increasing with increasing measuring temperature for both HfO_2 and HfSiON gate dielectrics. The difference of threshold voltage degradation under PBTI stress between HfO2 and HfSiON dielectrics is not quite apparent expect for 100 ^{o}C. On the other hand, the obvious improvement in PBTI characteristics was observed for HfSiON gate dielectrics while the hold time is 100 seconds as indicated in Fig. 5-10. The electron de-trap will result in ΔV_{TH} reduction in PBTI stress due to less electron being trapped in high-k thin films. This result indicates that the electron de-trapping will easily happen in HfSiON gate dielectrics. In generally, the electron will be trapped in gate dielectric of device while positive bias is applied, and de-trapped while remove the applied bias is removed. In addition, we assume that the charge de-trapping phenomenon results from some shallow trap in high-k gate dielectrics. It means that the extra Si-O and Si-N bodings effectively removed the dielectric vacancies to

have a lower trapping cross section and a lower concentration of generated traps, and reduce some trapping levels. This implies that some deep electron traps were effectively eliminated for HfSiON gate dielectrics, resulting in the characteristics as shown in Fig. 5-9 and 5-10.

The different hold time (0 & 100 s) under PBTI stress (Vg = +2.5 V) at different temperatures, including 25, 75 and 100 ^{o}C for HfO_2 gate dielectrics were shown in Fig. 5-11. There is almost no difference for ΔV_{TH} in PBTI stress at 25 and 75 ^{o}C between 0 and 100 s hold time as indicated in this figure. However, the ΔV_{TH} in PBTI stress is quite different at 100 ^{o}C for HfO_2 gate dielectric. The ΔV_{TH} with 0 s hold time is larger than ΔV_{TH} with 100 s hold time at the high temperature of 100 ^{o}C, indicating that the HfO_2 gate dielectric generated deeper charge trap during PBTI stress and trapped electrons need higher thermal energy to de-trap from HfO_2 film. On the other hand, the HfSiON gate dielectric shows the obvious dependence between ΔV_{TH} and measuring hold time as illustrated in Fig. 5-12. The ΔV_{TH} in PBTI stress with 0 s hold time is larger than ΔV_{TH} with 100 s hold time at different temperatures. As we mentioned above, some deep electron traps were effectively eliminated for HfSiON gate dielectrics, resulting in the characteristics in Fig. 5-12. Figure 5-13 (a), (b) illustrated the charge trapping/de-trapping models for HfO_2 and HfSiON gate dielectrics under PBTI stress respectively. As compared to HfO_2 dielectrics, the HfSiON has deep charge trapping level under PBTI stress as illustrated in Fig. 5-13(b).

5-4 Summary

In this chapter, the PBTI degradation for HfO_2 and HfSiON NMOSFETs with the metal gate electrode has been successfully demonstrated. The generated oxide trap during PBTI stress will dominate the PBTI characteristics for Hf-based gate dielectrics. In addition, the reduction of threshold voltage degradation and oxide trap generation under PBTI stress indicates that the HfSiON thin film quality is better than HfO_2 attributed to HfSiON gate dielectrics had the extra Si-O and Si-N bodings resulting in annihilation of oxygen vacancies. On the other hand, the electron trapping/de-trapping effect has been investigated in both HfO_2 and HfSiON NMOSFETs correlated with constant voltage stress. As compared to HfO_2 dielectrics, the HfSiON has shallower charge trapping level under PBTI stress due to elimination of deep dielectric vacancies.



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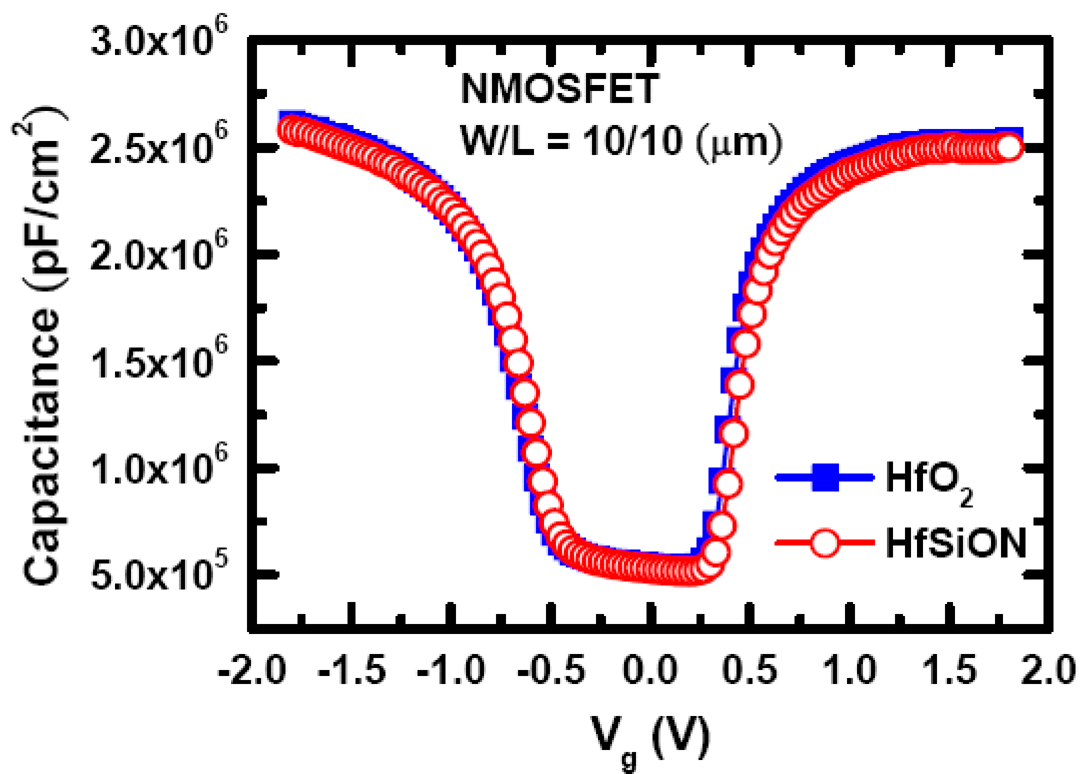


Fig. 5-1 High-frequency C-V characteristics at 100 kHz for NMOSFET with HfO_2 and HfSiON gate dielectrics, respectively.

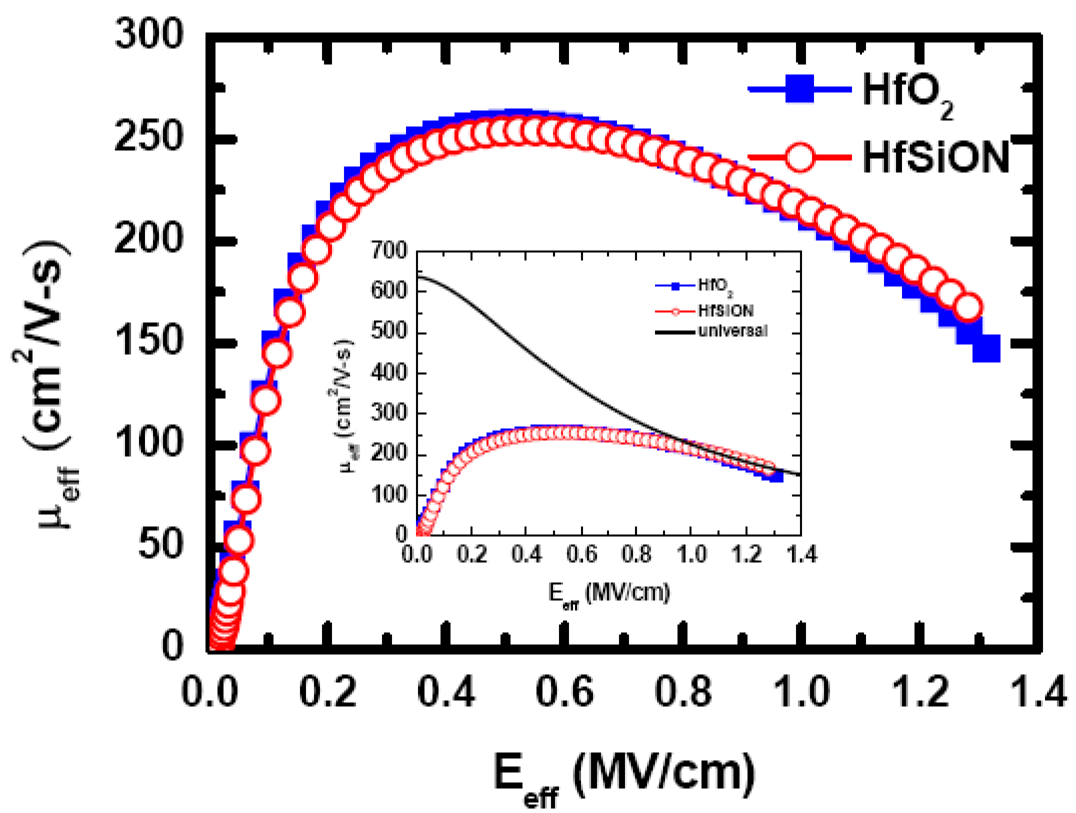


Fig. 5-2 The effective electron mobility measured on HfO_2 and HfSiON gate dielectrics using split CV method.

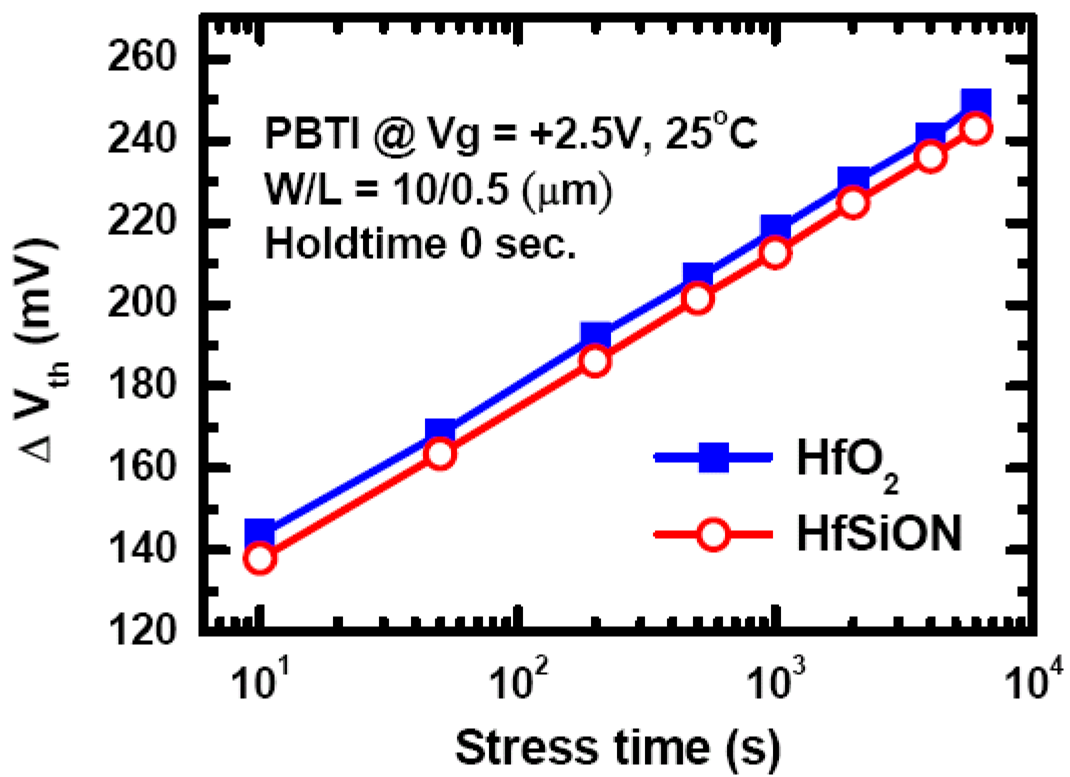


Fig. 5-3 Threshold voltage degradation (ΔV_{th}) of HfO_2 and HfSiON gate dielectrics under the same PBTI stress (Vg = +2.5 V) at room temperature.

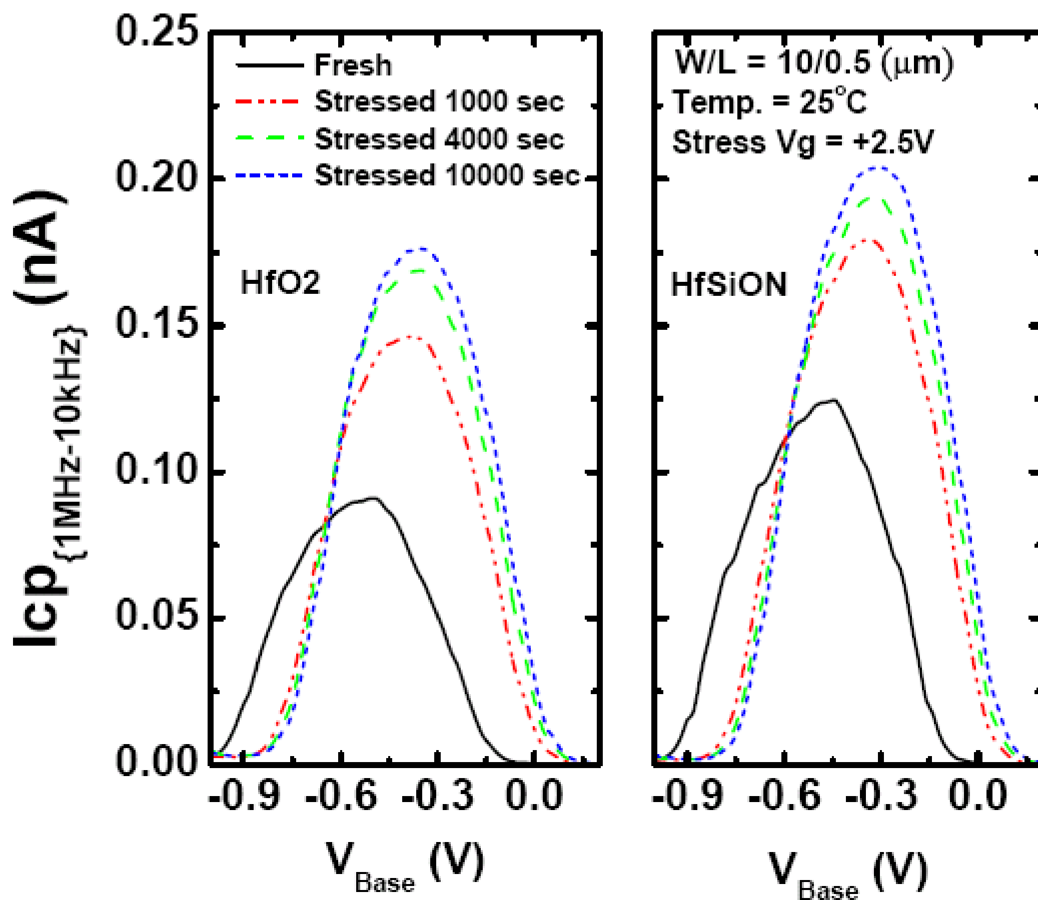


Fig. 5-4 Charge pumping current (I_{CP}) before and after PBTI stressing at +2.5V for HfO_2 and HfSiON dielectrics, respectively.

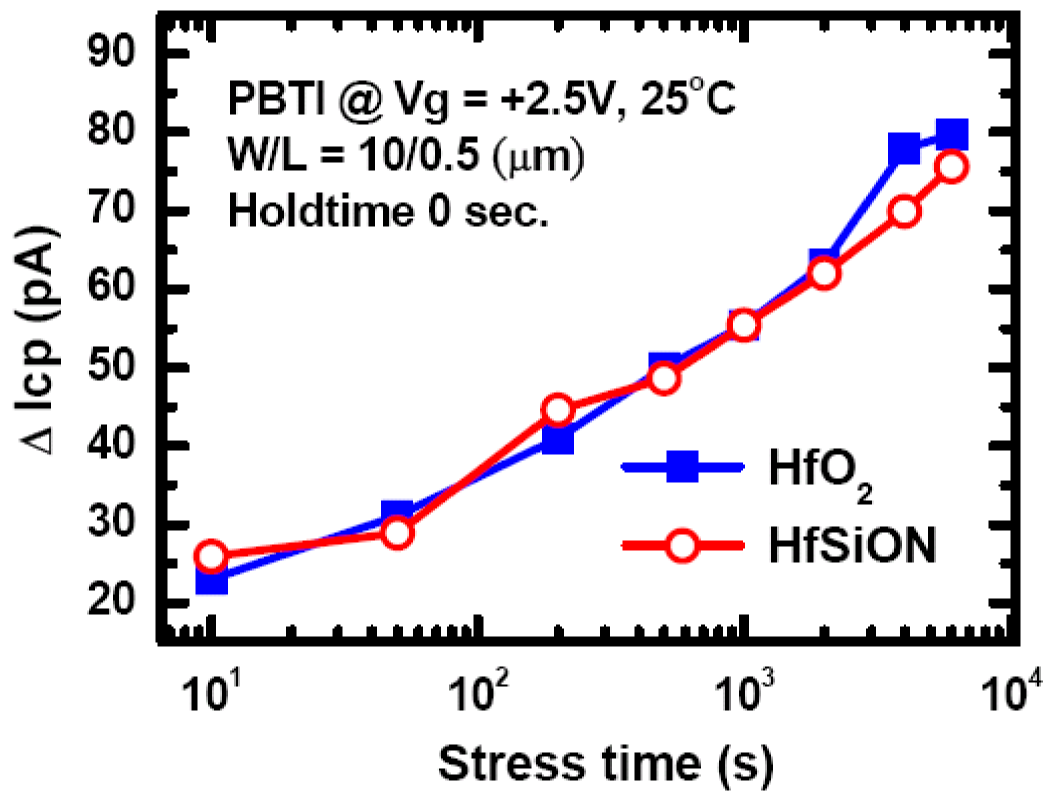


Fig. 5-5 Charging pumping increase (ΔI_{CP}) of HfO_2 and HfSiON gate dielectrics during the same PBTI stress bias (Vg = +2.5 V) at room temperature.

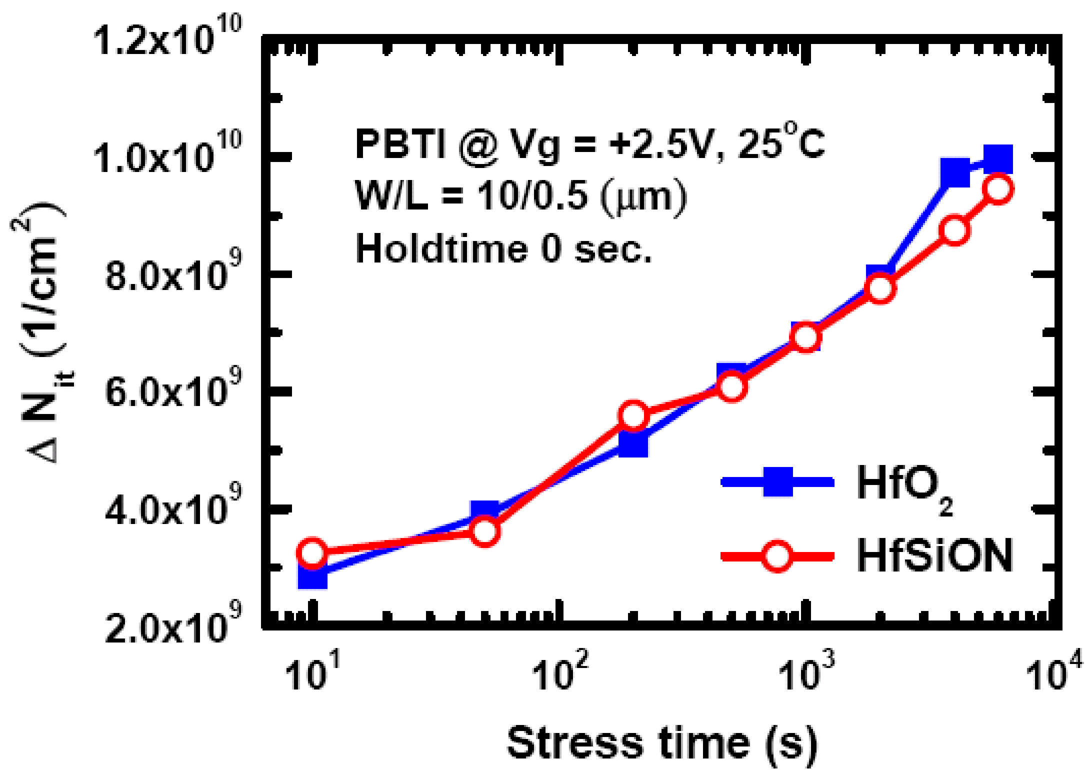


Fig. 5-6 Interface trap increase (ΔN_{it}) which extracted from ΔI_{CP} of HfO_2 and HfSiON gate dielectrics during the same PBTI stress bias (Vg = +2.5 V) at room temperature.

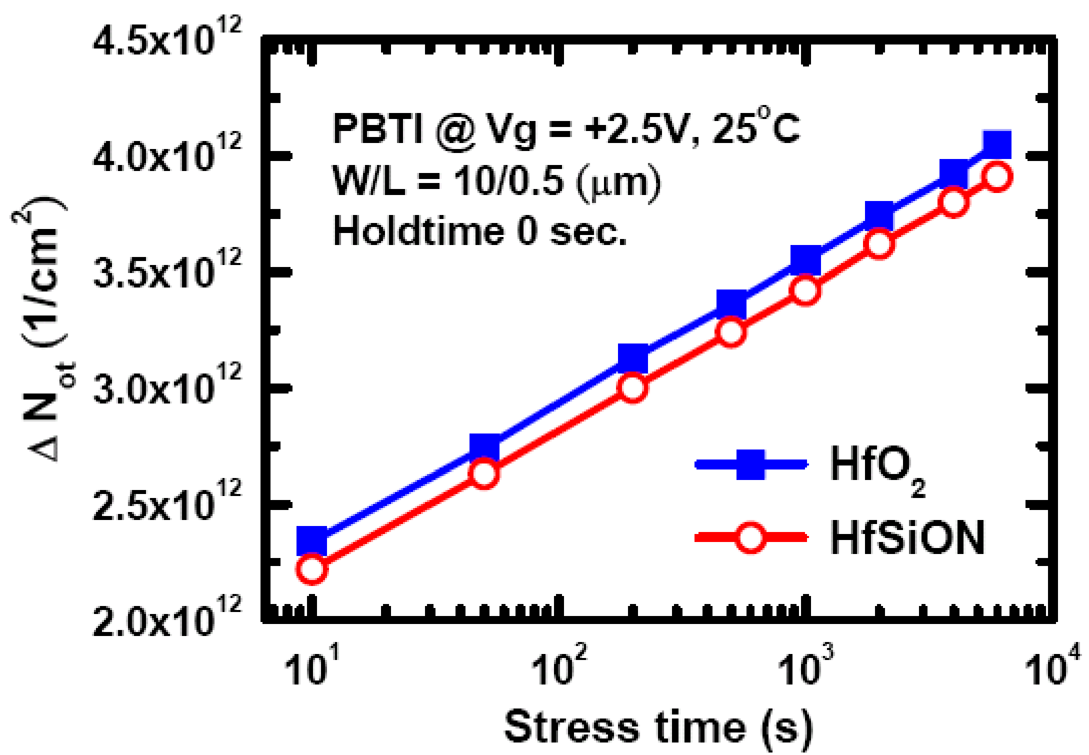


Fig. 5-7 Generated oxide trap (ΔN_{ot}) in the bulk of higk-k film during PBTI stress for both of HfO_2 and HfSiON dielectrics, respectively.

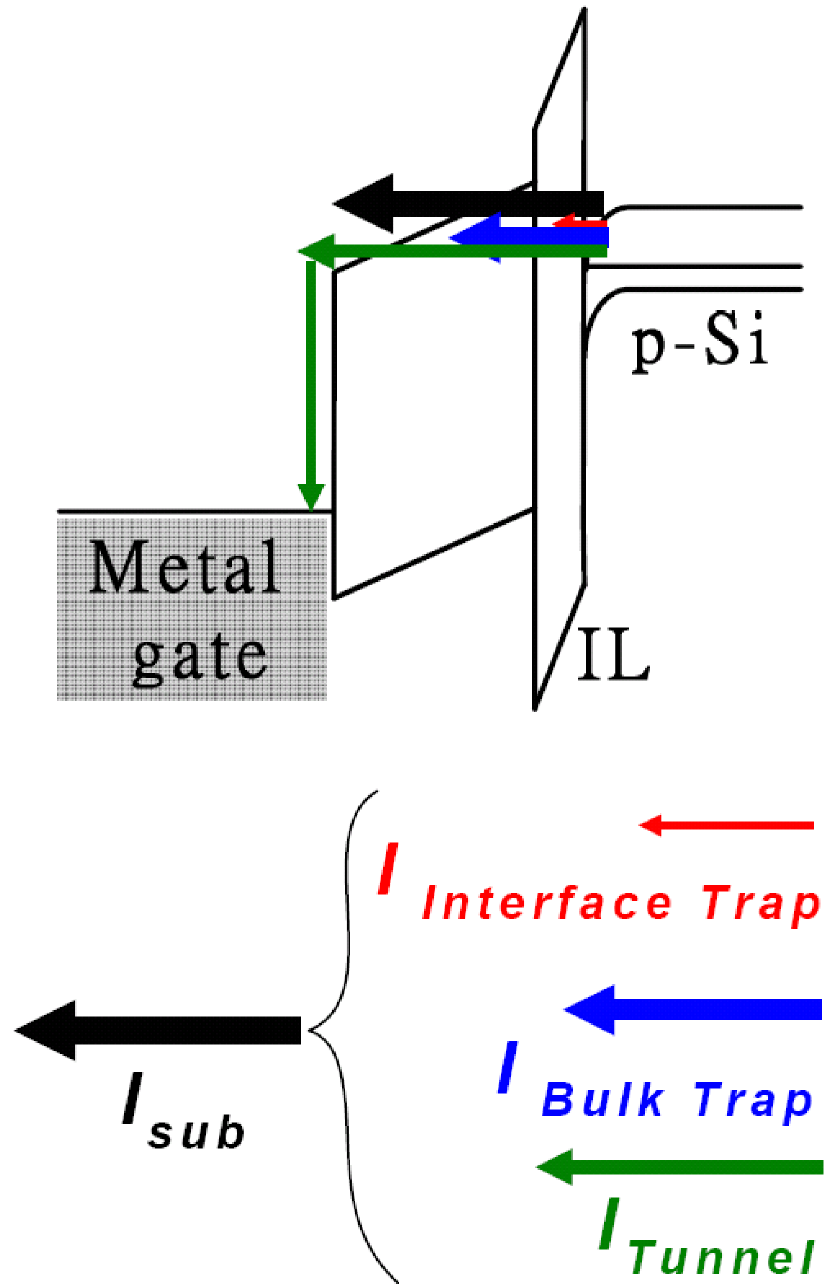


Fig. 5-8 Illustration of electron trapping model for Hf-based gate dielectrics under PBTI stress

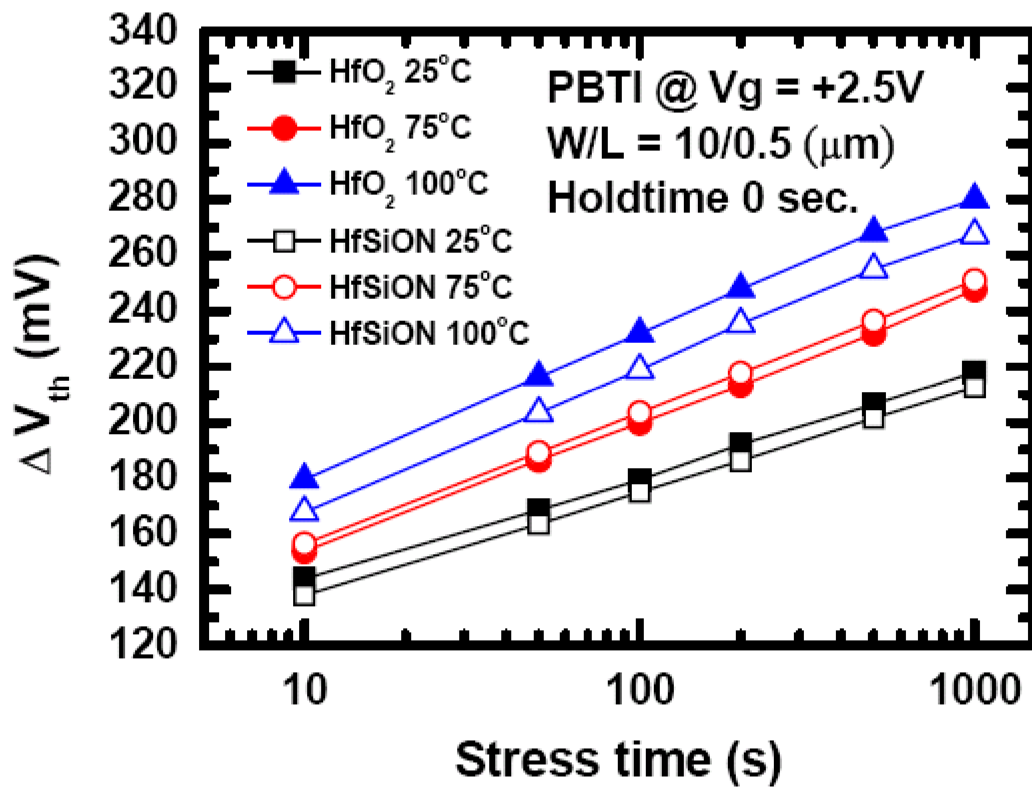


Fig. 5-9 Threshold voltage degradation of HfO_2 and HfSiON gate dielectrics during PBTI stress (Vg = +2.5 V) with no hold time at different temperatures, including 25, 75 and 100 ^{o}C.

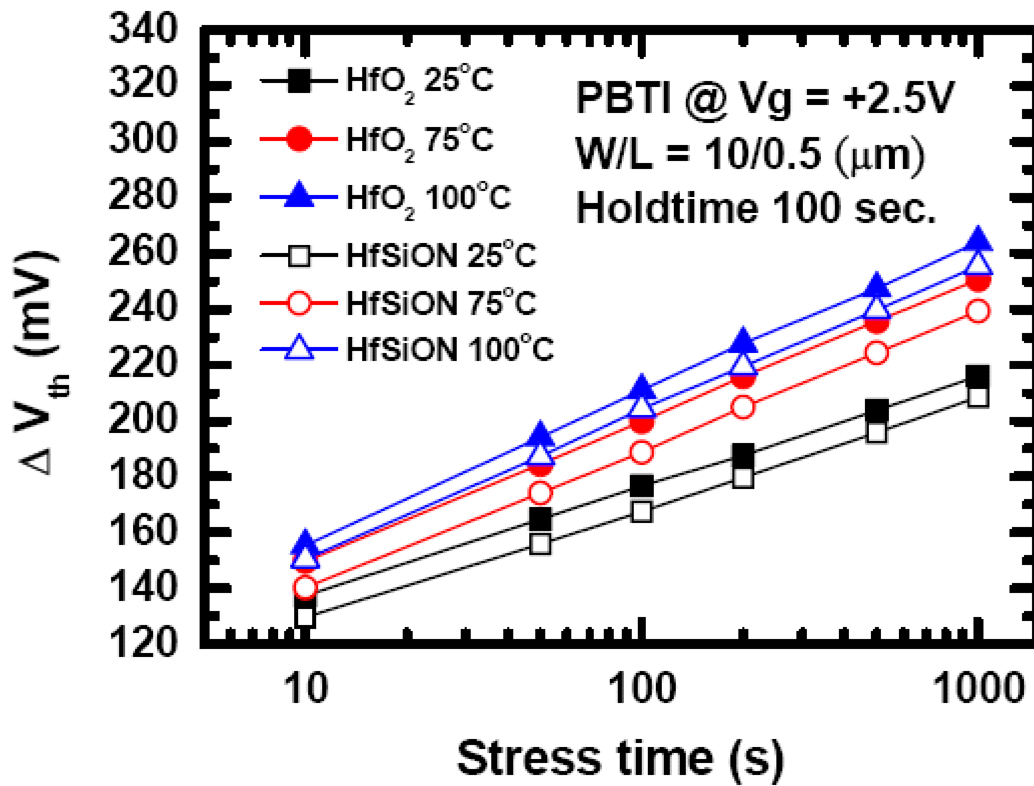


Fig. 5-10 Threshold voltage degradation of HfO_2 and HfSiON gate dielectrics during PBTI stress (Vg = +2.5 V) with hold time 100 s at different temperatures, including 25, 75 and 100 ^{o}C.

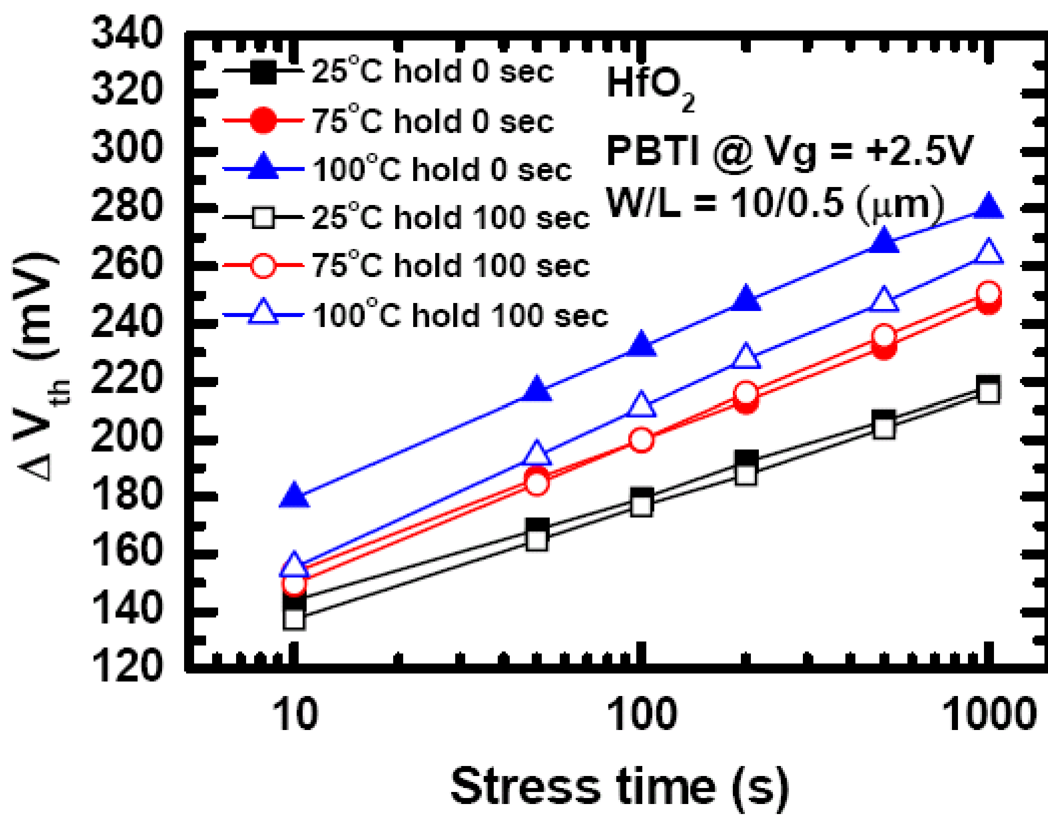


Fig. 5-11 Comparison of different hold time (0 & 100 s) under PBTI stress (Vg = +2.5 V) at different temperatures, including 25, 75 and 100 ^{o}C for HfO_2 gate dielectrics.

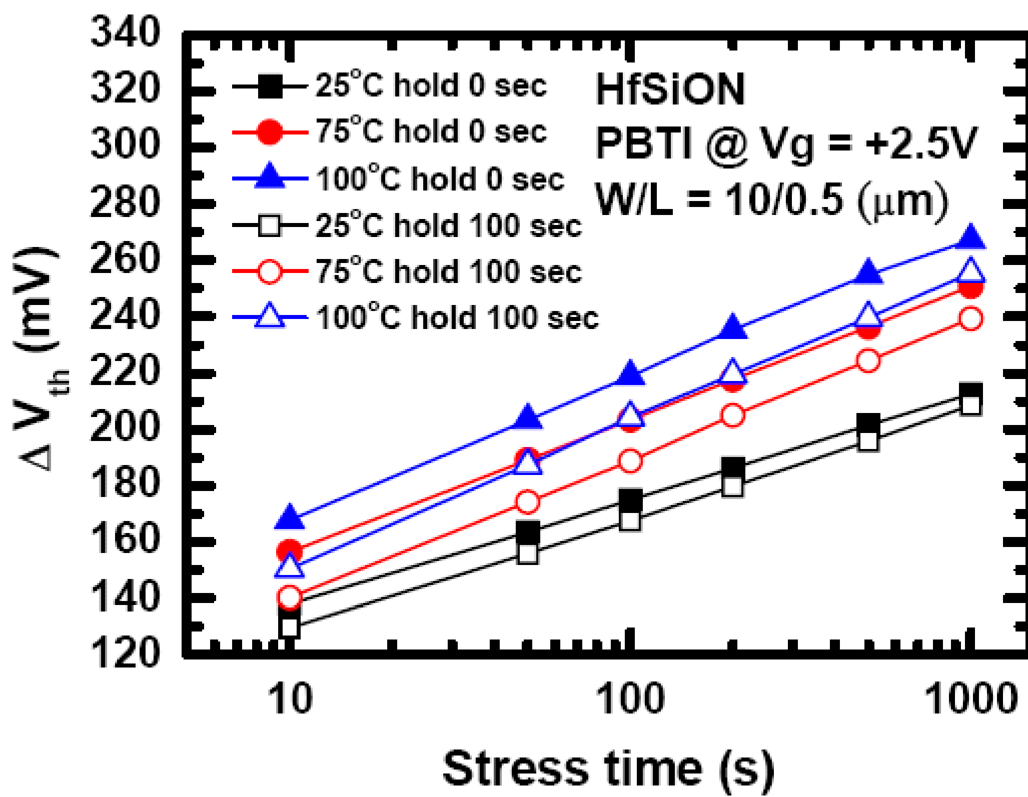


Fig. 5-12 Comparison of different hold time (0 & 100 s) under PBTI stress (Vg = +2.5 V) at different temperatures, including 25, 75 and 100 ^{o}C for HfSiON gate dielectrics.

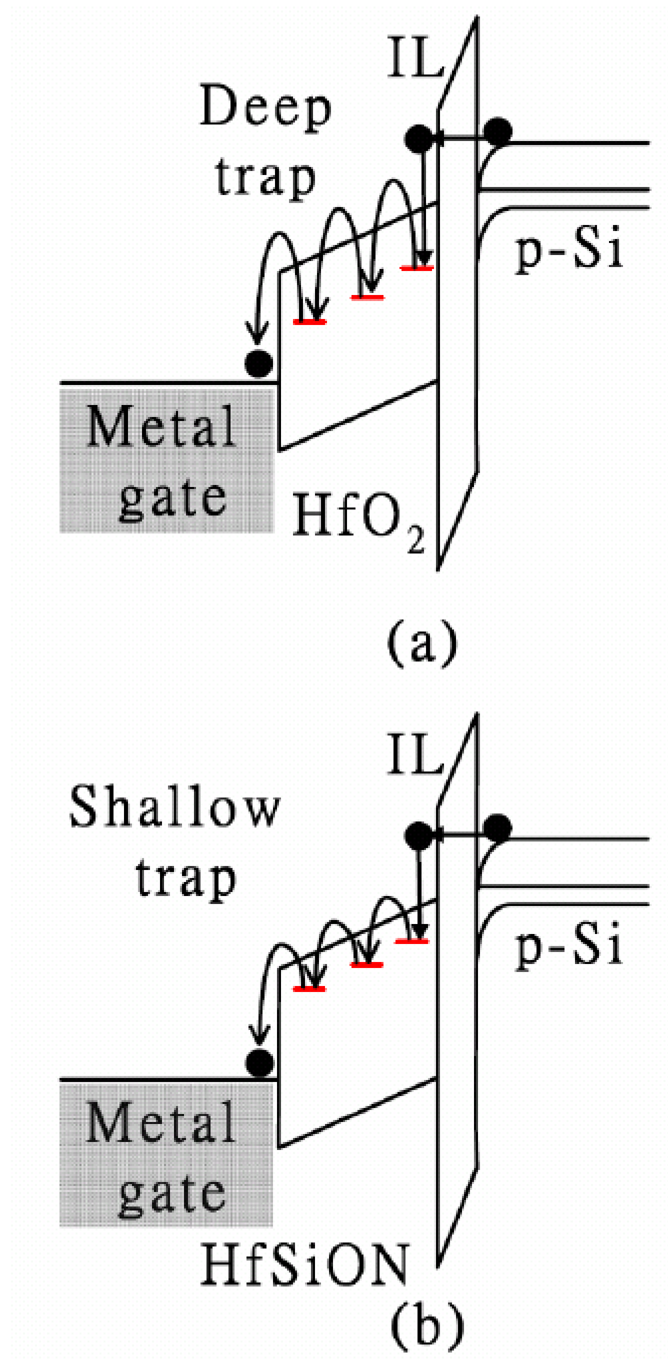


Fig. 5-13 Illustration of the charge trapping/de-trapping models for (a) HfO_2 and (b) HfSiON gate dielectrics under PBTI stress respectively.

Chapter 6

Conclusions and Recommendations for Future Study

6-1 Conclusions

In this dissertation, we investigated the gate engineering integration for advanced device performance and reliability improvement including the comparison of STI-induced local uniaxial compressive stress in <110>- and <100>-channel directions, the use of SiN capping layer on (111) orientation substrate to improve the NMOSFET performance, the reliability comparisons in NBTI and HCI between dual gate oxide PMOSFETs using PNO and TNO and the PBTI trapping/de-trapping reliability issues for devices using Hf-based high-k dielectrics. Several important results are obtained and summarized as follows:

1. We have systematically study the STI-induced strain impacts on the performances of 65 nm technology PMOSFET with <110>- and <100>-channel directions, respectively. <100>-channel devices have smaller DIBL and less layout dependence due to lower boron diffusivity and its non-sensitive to STI-induced stress, accordingly. Furthermore, as Compared to <110>-channel, <100>-channel devices show not only higher hole mobility, but also keep the advantage of free from STI stress in both of channel length and width directions.

2. Local strained channel techniques for depositing a SiN capping layer and a stack of α-Si and poly-Si gate structures on a (111) substrate were investigated in this study. We

demonstrated that the use of the strain structures can improve the performance of NMOSFETs fabricated in the <110> channel direction on a (111) substrate. The device performance is further enhanced as the SiN capping layer and α-Si layer become thicker. The stack of α-Si gate structures also affects the threshold voltages of the gate because of its poly depletion width. In addition, charge pumping current decreases with increasing split SiN layer thickness.

3. We have performed a systematical investigation of reliability issues, such as NBTI and HCI, for core and I/O PMOSFETs with TNO and PNO. As a result, the devices with TNO exhibit a lower NBTI immunity owing to the higher nitrogen concentration at the SiO_2/sub-Si interface than those with PNO, generating more interface traps during NBTI stress. In contrast, for HCI under the stress conditions of hot-hole injection, bulk oxide traps are an important factor for device degradation. For thick I/O devices, plasma induces more oxide traps in the bulk oxide of PNO and HCI induced a higher degradation rate than those for TNO devices. However, for an oxide thickness smaller than 3 nm in core devices, the effects of the oxide traps are negligible and interface traps are a predominant factor. This makes Core PMOSFETs with PNO have a higher immunity to HCI than those with TNO.

4. PBTI degradation for HfO_2 and HfSiON NMOSFETs with the metal gate electrode has been successfully demonstrated. The generated oxide trap during PBTI stress will dominate the PBTI characteristics for Hf-based gate dielectrics. In addition, the reduction of threshold

voltage degradation and oxide trap generation under PBTI stress indicates that the HfSiON thin film quality is better than HfO_2 attributed to HfSiON gate dielectrics had the extra Si-O and Si-N bodings resulting in annihilation of oxygen vacancies. On the other hand, the electron trapping/de-trapping effect has been investigated in both HfO_2 and HfSiON NMOSFETs correlated with constant voltage stress. As compared to HfO_2 dielectrics, the HfSiON has shallower charge trapping level under PBTI stress due to elimination of deep dielectric vacancies.

To optimize and integrate these gate engineering conditions, advanced research and develop for modern CMOS generation will achieve more complete and become more suitable for future ULSI applications.

6-2 Suggestions for future work

For the complete research on the topics of advanced CMOS devices gate engineering integration, some feasible study for our future work are proposed as follows:

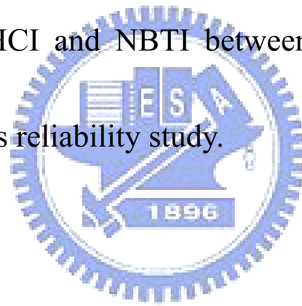
1. Investigating the impacts of the other strain including process-induced uniaxial strain and substrate engineering induced biaxial strain on different channel direction for both NMOS and PMOS devices.
2. Studying the quantum effects in small-dimension device to verify the real effects of strain on device performance and reliability.

3. Integrating the other kinds of strain for the NMOSFET fabricated on (111) substrate to achieve higher mobility improvement.

4. Developing an accurate formula to fit and verify the dependence of oxide thickness in NBTI and HCI for PNO and TNO.

5. Discussing the impacts of different Hf-silicate nitridation methods such as plasma nitridation or thermal nitridation on the HfSiON quality, device performance and reliability.

6. Investigating the trapping/de-trapping effects and temperature dependence under other reliability tests such as HCI and NBTI between HfO2 and HfSiON to complete the Hf-based high-k dielectrics reliability study.



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博士論文題目:

先進金氧半場效電晶體閘極工程對改善元件特性及可靠度之研究

Gate Engineering of Advanced MOSFETs for Device Performance and Reliability Improvement

發表或著作:(附於後頁)

Publication Lists

A. International Journal:

[1] **Wen-Cheng Lo**, Shien-Yang Wu, Sun-Jay Chang, Mu-Chi Chiang, Chih-Yung Lin, Tien-Sheng Chao, and Chun-Yen Chang, "**Systematical Study of Reliability Issues in Plasma-Nitrided and Thermally Nitrided Oxides for Advanced Dual-Gate Oxide p-Channel Metal-Oxide-Semiconductor Field-Effect Transistors**," *Jpn. J. Appl. Phys.*, vol. 46, no. 3A, pp.1124–1128, 2007.

[2] **Wen-Cheng Lo**, Ya-Hsin Kuo, Yao-Jen Lee, Tien-Sheng Chao, and Chun-Yen Chang, "**Performance Enhancement by Local Strain in <110> Channel n-channel Metal–Oxide–Semiconductor Field-Effect Transistors on (111) Substrate**," accepted for publication *Jpn. J. Appl. Phys.*, vol. 46, no. 9A, 2007.

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B. International Letter:

[1] **Wen-Cheng Lo**, Sun-Jay Chang, Chun-Yen Chang, and Tien-Sheng Chao, **"Impacts of Gate Structure on Dynamic Threshold SOI nMOSFETs,"** *IEEE Electron Device Lett.*, vol. 23, no. 8, pp.497–499, Augest 2002.

[2] **Wen-Cheng Lo**, Shien-Yang Wu, Sun-Jay Chang, Mu-Chi Chiang, Chih-Yung Lin, Tien-Sheng Chao, and Chun-Yen Chang, "**Comparisons of Plasma Induced Damage from BEOL Metallization Processes Between pMOSFETs with Thermal Nitrided Oxide and Plasma Nitrided Oxide**," submitted to *Jpn. J. Appl. Phys. Brief Communication.*

C. International Conference:

[1] **Wen-Cheng Lo**, Ya-Hsin Kuo, Yao-Jen Lee, Tien-Sheng Chao, and Chun-Yen Chang, "**Mobility Enhancement in Local Strained Channel nMOSFETs on (111) Substrate**," 2006 International Workshop on Dielectric Thin Films for Future ULSI Devices **(IWDTF2006)**, Kawasaki, 2006, pp. 35-36.