國 立 交 通 大 學

電子工程學系 電子研究所 碩士班

碩 士 論 文

射頻功率放大器之靜電放電防護設計

ESD PROTECTION DESIGN FOR RADIO-FREQUENCY POWER AMPLIFIER

研 究 生：蒙國軒

指導教授：柯明道 教授

中 華 民 國 九 十 六 年 九 月

射頻功率放大器之靜電放電防護設計

ESD PROTECTION DESIGN

FOR RADIO-FREQUENCY POWER AMPLIFIER

研 究 生：蒙國軒　　Student：Guo-Xuan Meng

指導教授：柯明道 教授　　Advisor：Ming-Dou Ker

國 立 交 通 大 學

電子工程學系　電子研究所 碩士班

碩 士 論 文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master

in

Electronics Engineering

September 2007

Hsinchu, Taiwan, Republic of China

中華民國九十六年九月

射頻功率放大器之靜電放電防護設計

學生: 蒙 國 軒　　指導教授: 柯 明 道 教授

國立交通大學

電子工程學系 電子研究所碩士班

摘要

本篇論文主旨在於設計適用於射頻功率放大器之靜電放電防護電路。其原理為利用元件或電路特性，使靜電放電防護電路對原電路的負面影響降到最低，且具有高水準之靜電放電防護能力。本論文提出兩個適用於射頻功率放大器的靜電放電防護策略，共下線了兩顆晶片以作驗證。所下線之兩顆晶片皆以標準零點一三微米互補式金氧半場效電晶體製程所製造。

第一種射頻功率放大器的靜電放電防護策略是利用電感性元件作為靜電放電箝制元件。因為靜電放電事件屬於較低頻行為，而射頻訊號佔據高頻頻譜，因此電感性元件可區分靜電放電事件和射頻訊號，作為一低阻抗之靜電放電路徑。此電感性箝制元件亦可作為輸出阻抗匹配網路之一部份，並與輸出阻抗匹配網路共同設計，因此電感性箝制元件可以對原射頻功率放大器完全無任何負面影響。同時，一個 MIM 電容可以與輸出訊號路徑串連，阻擋靜電放電電流直接貫穿而轟擊到內部主動核心元件，提高保護效果。實驗證明此靜電放電防護策略可有效提供防護等級超過八千伏特人體放電模式靜電放電轟擊測試，與四百伏特機器放電模式靜電放電轟擊測試。

第二種射頻功率放大器的靜電放電防護策略是利用低寄生電容之電容性靜電放電箝制元件。格狀陣列形式的矽控整流器和二極體可在相同晶片佈局面積下提供最大靜電放電路徑周長，因此可在貢獻最小寄生電容之前提下，提供最高靜電放電防護等級。實驗證明此靜電放電防護策略可有效提供防護等級超過八千伏特人體放電模式靜電放電轟擊測試，與八百伏特機器放電模式靜電放電轟擊測試。

實驗結果亦證明，靜電放電轟擊確實對射頻功率放大器的射頻操作效能有極大影響。射頻功率放大器極需靜電放電防護設計，否則無法於靜電放電轟擊存活。

ESD PROTECTION DESIGN FOR RADIO-FREQUENCY POWER AMPLIFIER

Student: Guo-Xuan Meng **Advisor: Prof. Ming-Dou Ker**

Department of Electronics Engineering & Institute of Electronics

National Chiao-Tung University

ABSTRACT

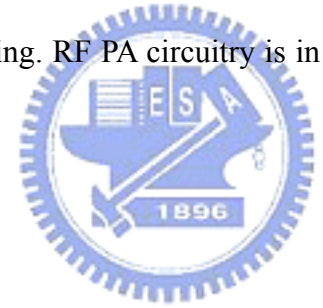
The aim of this thesis is to design the ESD protection circuits which are suitable in radio-frequency (RF) power amplifiers (PA). The ESD protection capability and the influence on the performance of the RF PA circuit after inserting the ESD protection circuit needs to be considered simultaneously. This thesis includes two RF PA ESD protection strategies which have been verified through two individual chips fabricated in standard 0.13-μm CMOS process.

The first RF PA ESD protection strategy is to use an inductive ESD clamp which can be co-designed with the RF PA output matching network. An inductive device can distinguish ESD event which occupies the lower frequency spectrum from the normal RF signals. It acts as the low impedance discharging path for ESD current and provides specific impedance for RF signal. A MIMCAP in series of the signal line can block out the ESD current from directly penetrating into the active devices in RF PA core. The measurement results have verified this ESD protection strategy and proved that the proposed ESD protection technique indeed provides excellent ESD robustness

of up to 8kV HBM ESD level and 400V MM ESD level.

The second RF PA ESD protection strategy is to use capacitive ESD devices with low parasitic capacitances. Waffle-structured SCR and diodes are utilized to provide maximum discharging peripheral within a given layout area for minimizing the parasitic capacitance. The waffle-structured SCR is designed with ESD detection and trigger circuit to provide the best ESD protection capability while contributing minimal parasitic capacitance to the RF PA. The measurement results have verified the effectiveness of the proposed ESD protection strategy and proved that this ESD protection technique indeed provides excellent ESD robustness of up to 8kV HBM ESD level and 800V MM ESD level.

Further, the measurement results also verify that an unprotected RF PA can not survive any single ESD zapping. RF PA circuitry is in urgent need of ESD protection with low parasitic effect.



誌謝

首先我要感謝我的指導教授柯明道博士，在這一年半來所給予我的指導與鼓勵。在研究上，教授指導我做研究的方向、方法、與態度：要求我追求研究的完整性與嚴謹性，讓我從一個一開始什麼都不懂的菜鳥，歷經多次的摸索與跌倒，開始對做研究有個比較清晰的概念。而在教授指導我的過程中，也間接地讓我瞭解到，研究跟人生其實有著相同的道理。現實生活中的研究，正如同現實生活中的人生，過程中往往會發生許多料想不到的意外，和很多很麻煩卻又不得不去做的 dirty work。繁雜瑣碎的意外鳥事，我們無法去避免；而我們唯一能做的，就是仔細地思考，用心地計畫未來必須做的工作，並且努力地去完成它。至於成功與否，就虛心接受，因為自己已經盡了最大的努力，而問心無愧。教授的苦口婆心，到最後才真正的有所體悟，並且為此由衷地感謝。

對於實驗室的學長們給予我的協助與指導，實在不勝感激。尤其是蕭淵文學長和黃俊學長，在 RF ESD 的電路設計與量測技巧上給予我許多實質的建議與帶領；王暢資學長所提供的下線機會讓我可以實際做出晶片並驗證。此外也感謝張瑋仁學長，顏承正學長，王資閔學長，陳世宏學長，和賴泰翔學長，不吝給予做研究的心態與經驗上的傳承。也感謝 307 實驗室的王文傑學長，給予專業的 RF 電路設計與量測技巧的建議與解答。

謝謝同年級的同儕們。感謝黃曄仁在工作繁忙之際仍協助我進行 wafer-level ESD 的測試，感謝林群祐在 waffle-structured SCR 元件實作上的協助，也感謝他在論文撰寫格式上的大力相助。另外也謝謝同一研究群的邱柏硯，莊介堯，和所有同在 527 研究室的同學和學長姐們，一起修課，做研究，偷閒時聊聊心中的快樂與酸苦，並且交流研究的經驗與技巧。這些讓單調苦悶的生活增添許多色彩與歡笑。

最後我要謝謝我的父母蒙志明先生和邱雪霞女士，和姊姊蒙秀婉小姐，給予我物質上的協助，使我無後顧之憂，並且在我失去信心時給我的支持與鼓勵，而從未對我失去過信心。這一直是我精神上最大的支柱。

還要感謝很多人，不可勝數，在此一併謝過，我不會讓你們失望的。

蒙國軒

九十六年九月

CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS

Chapter 1
Introduction

1.1 MOTIVATION

ESD robustness is one of the most serious reliability issues in CMOS IC manufacturing. With the continuously technology scale-down and rapidly increasing operation frequency in CMOS ICs, providing ESD protection circuits without influencing the normal core circuit function has become a great challenge.

To fulfill the requirement of ESD robustness for high-speed and RF circuits, a pair of diodes is inserted closed to the I/O pin along with a power-rail ESD protection circuit to provide whole-chip ESD protection ability without degrading the performance of the core circuit much [1], [2]. This pair of diodes is designed with certain sizes to provide an ESD protection level good enough for practical standards. Unfortunately, the parasitic capacitance of even such a small diode pair can still degrade the RF performance of the core circuit. Therefore, tradeoff emerges between the ESD robustness and the RF performance.

To minimize the negative impact of the ESD protection devices on the core circuit performance, the best solution is to co-design the core circuit with the ESD protection circuit. If it is possible to integrate partially, or even completely, the ESD clamp device into the core circuit normal function, the negative impact on performance may vanish.

ESD protection circuits are mainly applied to the I/O interface of the ICs to directly discharge the ESD current at the very first moment. For RF circuits, the input

interface first comes across a low-noise amplifier (LNA), while the output interface is typically a power amplifier (PA). Although the ESD protection design on LNA has been widely researched [3], [4], the ESD protection research on PA still remains little [5]. Therefore, this work focuses on the co-design of the RF PA and ESD protection strategies.

Two practical RF PA and ESD protection co-design schemes are proposed. One is to use inductor instead of the diode as the I/O ESD clamp device [4]. The other is to use silicon-controlled rectifier (SCR) [6].

Utilizing inductive devices for both RF matching and ESD discharge can provide excellent ESD robustness while preserving exact RF circuit performance without being degraded. The frequency-domain nature of an inductor can provide the ability to distinguish the ESD event from and the normal RF operation. Further more, this inductor can also serve in the RF matching network, providing normal RF circuit function. Therefore, in this way the ESD protection circuit is co-designed with the core circuit and has no negative impact on the normal RF circuit performance.

On the other hand, SCR devices can provide the best ESD level per unit chip area, that is, highest ESD robustness with minimum parasitic capacitance. In such sense, it can potentially provide excellent co-design capability. Therefore, careful co-design with proper triggering circuits is expected to exhibit good performance both on ESD robustness and RF circuit function.

Along with the co-design strategies, novel failure criteria specifically suitable for the RF circuits are presented. The RF circuitry is far different from the traditional digital circuitry [7-9], mainly because of the numerous passive devices in the input and output matching networks [10]. Not only the active devices but also these passive devices may be damaged by the ESD energy, and thus the overall RF operation behavior may be altered [11], [12]. The traditional leakage current test for digital

circuits is no longer suitable. Therefore, a complete functional test must be performed to examine the impact of the ESD event on the RF circuit performance, and new failure criteria must be set up specifically for high-speed/RF circuits.

The two co-design ideas were put into chip fabrication to verify their practicability. A narrowband class-AB PA is designed and utilizes an inductor as the output ESD clamp. An ultra-wideband class-AB distributed PA utilizing the SCR clamp device is designed, and the negative impact of the SCR devices on the RF bandwidth was investigated. Both PAs and corresponding ESD protection circuits were constructed in a standard 0.13-um CMOS process. The measurement results proved that both strategies indeed enhanced the ESD protection ability with tolerable degradation of the RF performance.

1.2 THESIS ORGANIZATION

The chapter 2 of this thesis investigates the basic principle and the consideration of two types of RF PAs. One of them is the narrowband class-AB PA and the other is the ultra-wideband class-AB distributed PA. A thorough discussion on the design equations and performance matrices are presented.

Chapter 3 investigates several ESD protection strategies. Two protection schemes for RF application are proposed. One of them is to use an inductive device as the ESD clamp, and the other is to use SCR devices as the ESD clamp. The co-design methodology and flow is proposed and investigated. Circuit topologies and corresponding design equations are presented in detailed. Also, basic ESD test set-up arrangement and the proposed novel RF circuit failure criteria are presented.

Chapter 4 summarizes the simulation and experimental results of both the

narrowband PA and the ultra-wideband distributed PA, along with the corresponding ESD protection schemes, both fabricated in a standard 0.13-um CMOS process. The measurement results are compared and analyzed. The result reveals that both of the proposed ESD protection schemes can indeed provide excellent ESD robustness.

Chapter 5 is the conclusions of this thesis and the future works on this topic.

Chapter 2

RF PA Basics

2.1 NARROWBAND CLASS-AB PA

2.1.1 Conventional Architecture

Fig. 2.1 is the conventional class-AB PA architecture. A class-AB PA is basically a transconductor (Gm-cell), providing a sufficient amount of the output current corresponding to the input driving power. Fig. 2.2 is a typical circuit implementation of this architecture. The cascode topology provides good voltage gain and good isolation; it also prevents drain overstress since the voltage swing may approach 2 times the VDD. The input and output matching networks provide suitable impedance matching for RF signal integrity, power transfer efficiency, and the narrowband selectivity [13].

2.1.2 Load-line Design

The loading impedance of the class-AB PA is designed for maximum output power capability, and therefore the load-line design aims to exploit the maximum usefulness of the circuit limit. To accomplish this goal, the load-line of the class-AB PA is designed as shown in Fig. 2.3. Fig. 2.3 is a typical I-V relationship of the conventional class-AB PA core output, along with the maximum output power efficiency load-line. From Fig. 2.3 the loading resistance, R_L, is defined in (2-1).

$$R_L = \frac{V_{MAX} - V_{knee}}{I_{MAX}} \tag{2-1}$$

R_L is the target impedance for the output matching network. V_{MAX} and V_{knee} are the maximum and minimum output voltage operation limit, respectively. I_{MAX} is the maximum output current capability of the device. All these parameters are set whenever the sizes and the bias of the active devices are set.

Once the class-AB PA is designed with a PA core loading of the optimal load-line impedance R_L, the PA can theoretically operate with maximum output power efficiency. Therefore, the output matching of a PA is also named as the load-line match.

2.1.3 Matching Network Design

Lossless devices (inductors and capacitors) are used in order not to dissipate any of the signal power. Their behaviors and the effects of impedance transform are shown in Fig. 2.4 on the ZY Smith chart. There are three commonly used matching network configurations to transform impedance to a desired position on the Smith chart. Namely, they are L-section (Fig. 2.5), T-section (Fig. 2.6), and π-section (Fig. 2.7). Form these figures and the attached design equations, proper input and output matching networks can be designed accordingly.

In the typical circuit implementation of this architecture in Fig. 2.2, the output matching network is in the π-section configuration, and the input matching network is as the L-section configuration.

2.1.4 The Design Principle of the Narrowband Class-AB PA

The output power is defined in (2-2).

$$P_{out} = \frac{1}{2} \cdot \frac{\left[\left(V_{MAX} - V_{knee} \right) / 2 \right]^2}{R_L} \qquad (2\text{-}2)$$

Once the output power specification is given, R_L is set by (2-2), according to the maximum output voltage swing available from the given circuit topology. The required maximum output current (I_{MAX}) is set by (2-1). Thus, the sizes and bias of the active devices are set.

Once the sizes and bias of the active devices are set, the input and output impedance of the active devices is defined. Then, the input and output matching networks can be designed to transform the input and output impedance of the active devices to a suitable impedance level accordingly. After the input and output matching networks are designed properly, the narrowband class-AB PA is ready to work.

2.2 UWB CLASS-AB DISTRIBUTED AMPLIFIER

2.2.1 Conventional Architecture

The distributed amplifier is an elegant way to overcome the limitation of maximum gain-bandwidth product [14]. This architecture achieves a gain-delay trade-off without the penalty on bandwidth. Theoretically, this architecture can provide possibly infinite bandwidth with arbitrary gain. Therefore, ultra-wideband amplification is accomplished.

Fig. 2.8 is the conventional distributed amplifier architecture. Each Gm-cell acts as a transconductor to provide a certain amount of output current corresponding to the input driving voltage signal. While the input driving voltage signal propagates down the input line, each Gm-cell is being excited in succession, producing the output current equal to the transconductance (Gm) of each Gm-cell multiplied by the input driving voltage signal. One half of the output current signals from each Gm-cell propagate backward to the output line termination resistor Rt and are absorbed. The

other half of the output current signals ultimately sum in time coherence if the delays of the input and output lines are matched. Therefore, the output current waves sum up coherently in constructive superposition manner.

2.2.2 Load-line Design of Each Gm-cell

Fig. 2.9 is a typical circuit implementation of this architecture. The cascode topology provides good voltage gain and good isolation. The input and output lines can be synthesized by lumped passive devices, exhibiting a transmission line characteristic impedance of Zo.

Fig. 2.10 shows the loading condition of each Gm-cell. The active device output is loaded with a characteristic impedance of Zo in both directions. Equivalently, each Gm-cell is loaded with Zo/2. Therefore, it is easy to show that the voltage gain, A_v, of the distributed amplifier is governed by equation (2-3).

$$A_v = \frac{1}{2} n \cdot Gm \cdot Zo \tag{2-3}$$

The n, the number of stages, in (2-3) is the number of Gm-cell in the distributed amplifier.

The distributed amplifier architecture provides the capability to achieve simultaneously 50-ohm conjugate match and load-line match. Since each direction seen by the active device output is designed to be 50-ohm for minimum signal reflection, the total loading seen by the active device output is 25-ohm as the 50-ohm output matching condition. If each Gm-cell is also designed to be with a 25-ohm optimal load-line R_L, as shown in Fig. 2.10, 50-ohm conjugate match and optimal load-line match is simultaneously achieved. Therefore, minimum output signal reflection and PA maximum output power efficiency can be accomplished at the same time. Note that this is impossible in the case of narrowband class-AB PA, which must

trade the output 50-ohm matching and the PA maximum output power efficiency, since the optimal load-line impedance is usually much smaller than 50-ohm.

Finally, the total output power can be derived and shown in (2-4).

$$Pout_{each} = \frac{1}{2} \cdot \frac{\left[\left(V_{MAX} - V_{knee} \right) / 2 \right]^2}{R_L}$$
$$Pout_{total} = \frac{1}{2} \cdot n \cdot Pout_{each} \tag{2-4}$$

$Pout_{each}$ is the output power of each Gm-cell; $Pout_{total}$ is the total output power appear at the output port.

2.2.3 Input and Output Line Design

Fig. 2.11 is the distributed amplifier architecture whose input and output lines are synthesized by lumped devices. In such manner, the input and output lines are named as the artificial lines.

From Fig. 2.11 the governing equation (2-5) of the characteristic impedance of Zo of the line is also straight forward [].

$$Zo = \frac{Z}{2}\left[1 \pm \sqrt{1 + \frac{4}{ZY}}\right] \approx \sqrt{\frac{Z}{Y}} \quad if\left(\frac{4}{ZY} >> 1\right) \tag{2-5}$$

To achieve 50-ohm matching, the characteristic impedance Zo of the line is designed to be 50-ohm. The terminal resistor Rt at the end of the line is also 50-ohm to ensure no signal reflection back to the input and output port.

There are three configurations for the artificial lines (Z and Y), namely low-pass line, high-pass line, and band-pass line, as shown in Fig. 2.12. From Fig. 2.11, it can be observed that the overcome of the bandwidth limitation of this architecture comes from the fact that the input and output parasitic capacitances of the Gm-cell are actually parts of the shunt Y devices. That is, the parasitic capacitances are absorbed

into the input and output line, causing entirely no degradation on the circuit operation speed. Therefore, until the cutoff frequency of the line itself is approached, the input and output impedance remains constant and equal to Zo, and the overall operation bandwidth is controlled solely by the input and output lines. It is obvious that the band-pass line structure is the most convenient way to control the overall band-pass type bandwidth.

2.2.4 Design Principle of the UWB Distributed Amplifier

First of all, the optimal load-line R_L condition of each Gm-cell is designed as the 25-ohm, as shown in Fig. 2.10. In this case, conjugate matching condition and maximum output power efficiency condition can be simultaneous achieved. Therefore, minimum signal reflection and excellent power efficiency can be guaranteed.

Once the optimal load-line R_L is set, the size and bias of the active devices is set. Also, the output power of each Gm-cell is defined, as shown in (2-4). Therefore, the input and output impedance of the active devices is defined. With the information of the input and output capacitances, along with the bandwidth specification, the input and output artificial line can be designed, according to Fig. 2.12.

Finally, from the output power specification, the number of stages can be defined, according to (2-4), and the ultra-wideband distributed amplifier is ready to work.

2.3 BASIC RF PA FIGURES OF MERITS

2.3.1 Scattering Parameters, S-parameters

To characterize the behavior of a RF two port network, scattering parameters (S-parameters) are used [14]. Fig. 2.13 is the demonstration of a two-port network

characterized by S-parameters.

S-parameters are defined by power waves. For RF systems, the signals are actually in the form of power waves, and thus S-parameters are suitable for characterizing these systems which operate at high frequency. On the other hand, the traditional Z-parameters and Y parameters are not capable of defining such systems. It is because the definitions of Z-parameters and Y parameters require perfectly open and short conditions, which are difficult to obtain at high frequency. Also, active devices, such as diodes, BJTs, and MOSFETs, cannot function stably under open and short terminal conditions. Therefore, S-parameters are the most common way to define a microwave/RF system.

S-parameters are defined in (2-6).

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \Rightarrow \begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 \\ b_2 = S_{21}a_1 + S_{22}a_2 \end{cases} \tag{2-6}$$

In (2-6), a_1 and a_2 represent the incident waves from the source and the load, respectively; b_1 and b_2 represent the reflected waves from Port 1 and Port 2 of the system to the source and the load, respectively. The physical meaning of the terms in the S-parameters matrix is in (2-7).

$$\begin{aligned} S_{11} &= \left.\frac{b_1}{a_1}\right|_{a_2=0} = \frac{reflected\_from\_Port\_1}{incident\_to\_Port\_1} = \Gamma_1 \\ S_{21} &= \left.\frac{b_2}{a_1}\right|_{a_2=0} = \frac{transmitted\_to\_Port\_2}{incident\_to\_Port\_1} = T_{21} \\ S_{12} &= \left.\frac{b_1}{a_2}\right|_{a_1=0} = \frac{transmitted\_to\_Port\_1}{incident\_to\_Port\_2} = T_{12} \\ S_{22} &= \left.\frac{b_2}{a_2}\right|_{a_1=0} = \frac{reflected\_from\_Port\_2}{incident\_to\_Port\_2} = \Gamma_2 \end{aligned} \tag{2-7}$$

S_{11} is the reflection coefficient seen at Port 1; S_{22} is the reflection coefficient seen at Port 2. S_{21} is the forward gain from Port 1 to Port 2; S_{12} is the reverse gain from

Port 2 to Port 1.

S-parameters of a PA are commonly used to demonstrate the small signal power handling capability of the PA over the frequency range of interest. S_{11} describes the input matching condition of the PA. S_{22} describes the output matching condition of the PA. S_{21} describe the small signal power gain of the PA. S_{12} describes the reverse isolation condition of the PA and stands for the unilateral property of the PA. Fig.2-14 shows a typical S-parameters behavior of a PA. Note that the S-parameters are indexed with frequency. Therefore, it can be somehow viewed as the frequency response of the PA small signal power handling capability.

From the S-parameters the stability of a RF amplifier can be extracted. The stability of a RF amplifier indicates the property that the RF amplifier can function properly without going into oscillation. This is crucial for RF amplifiers, especially for RF power amplifiers, since power amplifiers consume and output a large amount of power, which is prone to oscillation. Oscillation happens when the real part of the input or output impedances becomes negative. This condition results in the situation that input or output reflection coefficient, Γ_{in} or Γ_{out}, is greater than unity. Under this circumstance, the RF amplifier would no longer stably amplifying signals but behave as an oscillator.

The stability can be quantified by the S-parameters of the active devices, the matching conditions of the amplifier circuit, and the source and load impedances. There are two factors to describe this quantity of stability, k-factor and μ-factor. []

(1) k-factor:

Given a S-parameters of a two-port network between the input source and the output loading, the necessary and sufficient conditions for unconditional stability are that k is greater than unity and $|\Delta|$ is less than unity, as shown in (2-8).

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12} \cdot S_{21}|} \qquad k > 1$$
$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad \Rightarrow \quad |\Delta| < 1 \tag{2-8}$$

This expression can be further manipulated into another equivalent condition, as shown in (2-9).

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12} \cdot S_{21}|} > 1$$
$$b = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11}S_{22} - S_{12}S_{21}|^2 > 0 \tag{2-9}$$

The k factor is also named as stability factor and b factor is named as stability measure.

(2) μ-factor

The μ-factor gives the geometric distance from the center of the Smith chart to the nearest output (load) stability circle. This stability factor is given by (2-10).

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \cdot \Delta| + |S_{12}S_{21}|} \tag{2-10}$$

The single necessary and sufficient condition for unconditional stability of the 2-port network is that μ is greater than unity. This condition actually describes the fact that the output reflection coefficient, Γ_{out}, is less than unity, and thus the output impedance is not negative resistive. Positive real part of the output or input impedances guarantees unconditional stability.

Alternatively, the single necessary and sufficient condition for unconditional stability of the 2-port network is that μ′ is greater than unity, as shown in (2-11).

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^* \cdot \Delta| + |S_{12}S_{21}|} \tag{2-11}$$

This condition describes the geometric distance from the center of the Smith chart to the nearest input (source) stability circle. The μ′ actually describes the fact

that the input reflection coefficient, Γ_{in}, is less than unity, and thus the input impedance is not negative resistive, which also guarantees the unconditional stability.

2.3.2 Large Signal Transfer Characteristics

The plot of output power versus input power gives the power transfer characteristics (PTC) of a PA. PTC is commonly used to demonstrate the large signal power handling capability of a PA [13]. Fig.2-15 shows a typical PTC of a PA.

A commonly used unit for describing RF power is dBm, which is defined in (2-12).

$$dBm = 10 \cdot \log_{10}\left(\frac{Power\_in\_Watt}{1mW}\right) \tag{2-12}$$

From the PTC, two properties of the PA can be read. The first property is the saturation power, which is the maximum output power capability of the PA.

The second property is the large signal power gain, which is defined in (2-13).

$$Gain(dB) = 10 \cdot \log_{10}\left(\frac{P_{out}(W)}{P_{in}(W)}\right) = P_{out}(dBm) - P_{in}(dBm) \tag{2-13}$$

PTC can be further manipulated to extract the linearity property of the PA. One of the most important linearity indicators is the 1-dB compression point (P-1dB). From the PTC of a PA, it can be noticed that, for sufficient large input power, the output power would no longer be amplified by the same constant gain. The output power would eventually saturate, and there would be no further linear amplification relationship between the input and the output.

The reason for this phenomenon is that, for linear PAs, usually the active devices should remain in their active regions during the whole operation cycle. For MOSFETs the active region is its saturation region. For small output signal power this assumption stays true. However, when the output power increases, the signal swing at

the active device output node (for MOSFETs it means drain) would gradually increases, and eventually the devices would swing into the nonlinear region of the device I-V curve (for MOSFETs it means triode region). Thus, the output swing would be compressed, and so as the output power. No further output power can be delivered to the load since from now on the active devices have been driven to their maximal operation limit, as shown in Fig.2-16.

1-dB compression point, P1dB, quantifies this phenomenon. It is defined in (2-14).

$$OP1dB(\text{dBm}) - IP1dB(\text{dBm}) = \text{Gain}(\text{dB}) - 1 \quad (2\text{-}14)$$

OP1dB is the output power at P1dB, and IP1dB is the corresponding input power. The definition of P1dB is that at this power level the amplifier is unable to amplify the signal at the same constant rate as it can for much smaller signal level. At P1dB, the actual gain ($OP1dB_{(dBm)}$-$IP1dB_{(dBm)}$) is 1 dB smaller than the small signal linear gain. It is then defined that this point is the starting point at which the output power begins to be noticeably compressed. Therefore, OP1dB can be treated as the maximum linear output power capability of a PA.

Another performance metric for PA large signal operation is efficiency. Efficiency of a RF amplifier indicates the utilization of power participated in the process of transforming input power into output power. There is always inevitable loss in this transforming process; no one hundred percent perfect utilization of power. Thus the efficiency of this transforming process needs to be quantified to describe the PA performance of utilizing power to satisfy its output power requirements.

There are three factors to describe the quantity of efficiency: drain efficiency, power added efficiency, and total efficiency.

(1) Drain efficiency, η

$$\eta = \frac{P_{out}}{P_{VDD}}$$

Drain efficiency, η, describes the utilization of the DC supplying power (P_{VDD}) in the viewpoint that a PA's duty is to output power. Therefore, this metric describes how efficiently the supplying power is used to satisfy the output power requirement.

(2) Power added efficiency, PAE

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}$$

Power added efficiency, PAE, describes the utilization of the DC supplying power (P_{VDD}) in the viewpoint that a PA needs to output and amplifies power. In such manner, PAE describes how efficiently the supplying power is used in the PA to satisfy its output power capability and the power amplification capability, and thus is more suitable for a power amplifier metric of efficiency.

(3) Total efficiency, η_T

$$\eta_T = \frac{P_{out}}{P_{VDD} + P_{in}}$$

Total efficiency, η_T, describes the utilization of the DC supplying power (P_{VDD}) in the viewpoint that a PA output power by consuming supplying power and input power. In such manner, η_T describes how efficiently the supplying power and the input driving power are used in the PA to satisfy its output power capability, and thus is suitable for specifying overall system performance.

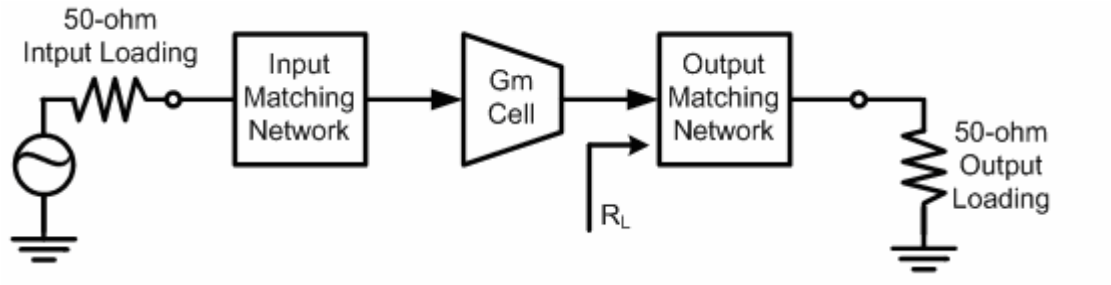


Fig. 2.1 Conventional class-AB PA architecture.

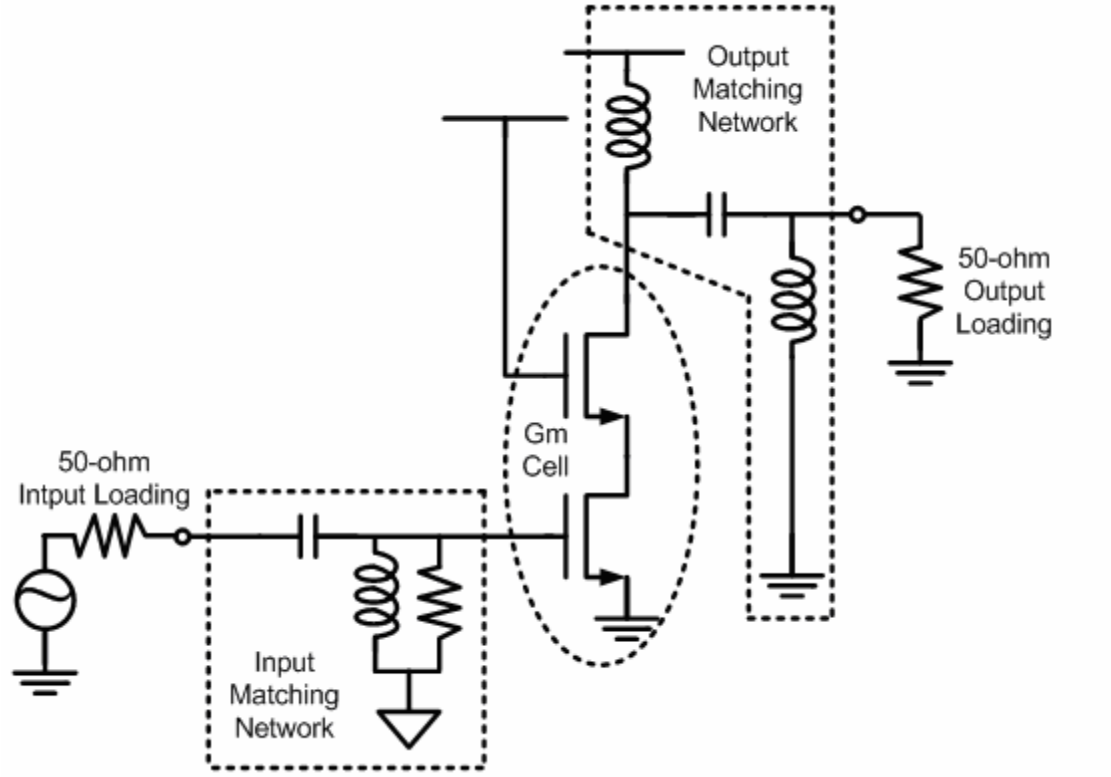


Fig. 2.2 Typical circuit implementation of the conventional class-AB PA architecture.

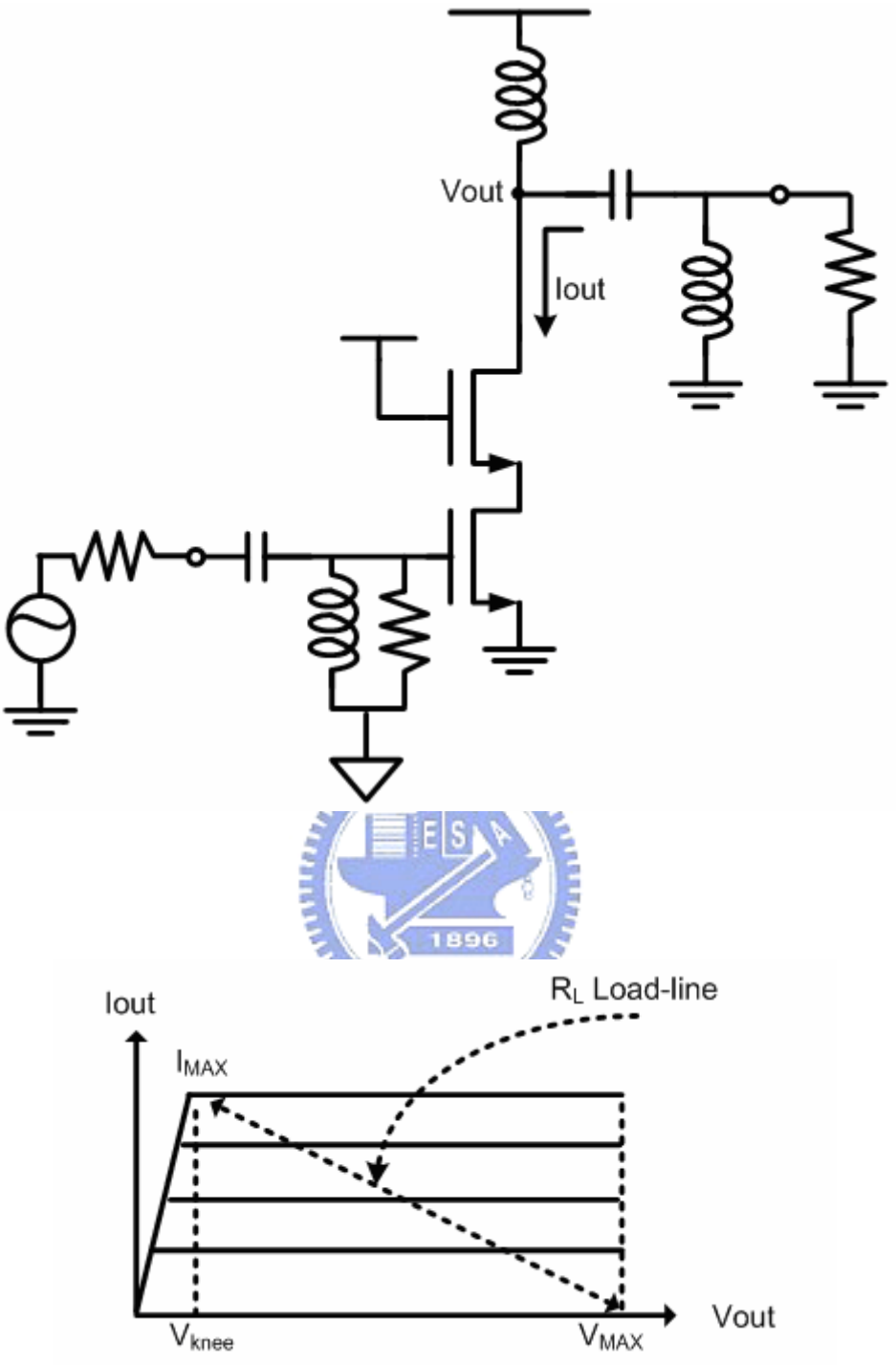


Fig. 2.3 Typical I-V relationship and the optimal load-line for maximum output power efficiency, of conventional class-AB PA core operation.

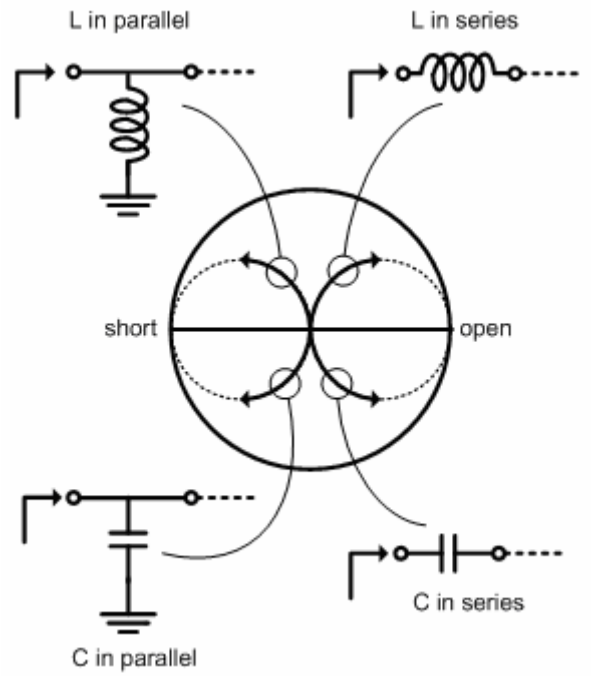


Fig. 2.4 Behaviors and effects of impedance transform on the ZY Smith chart.

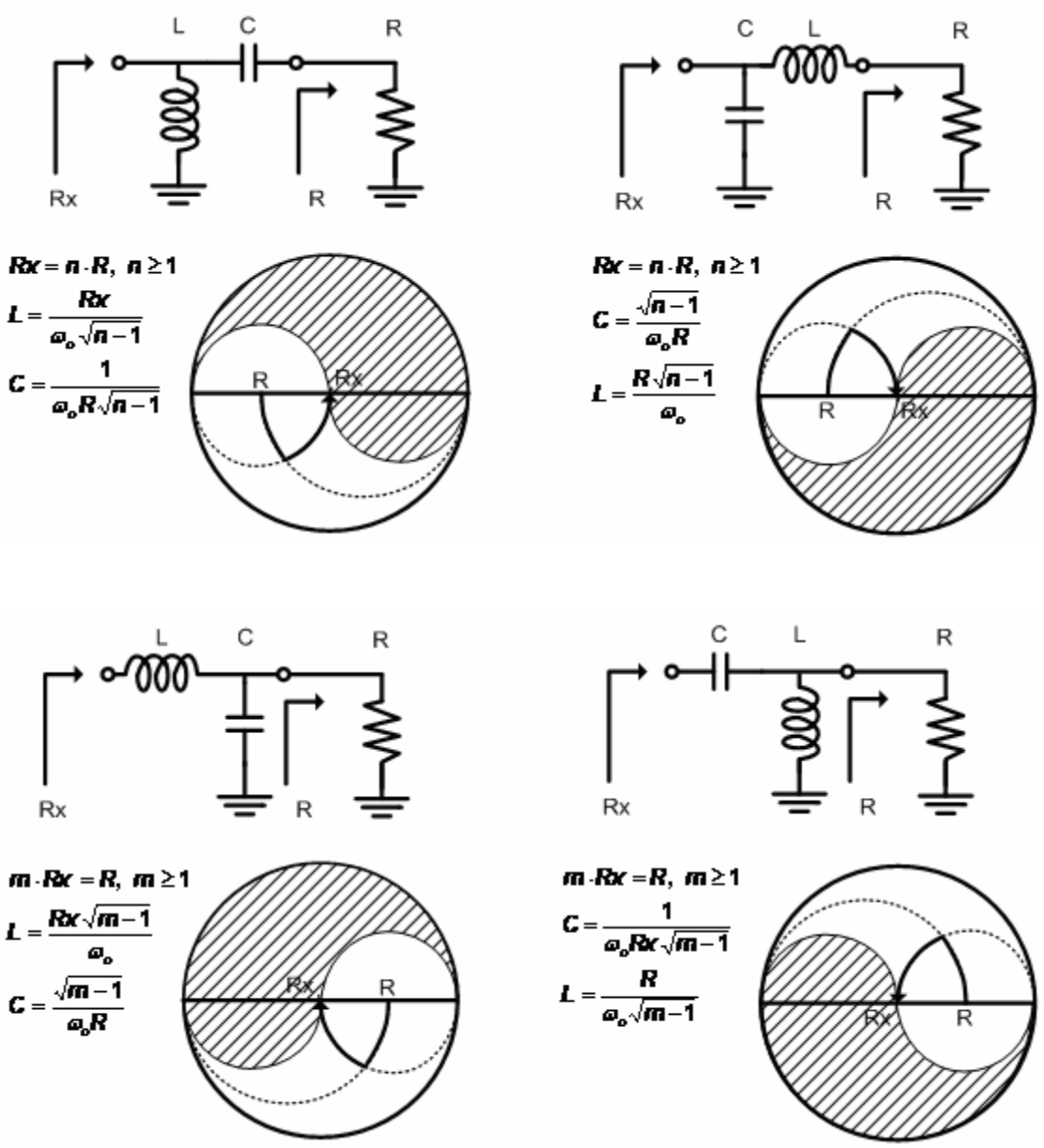
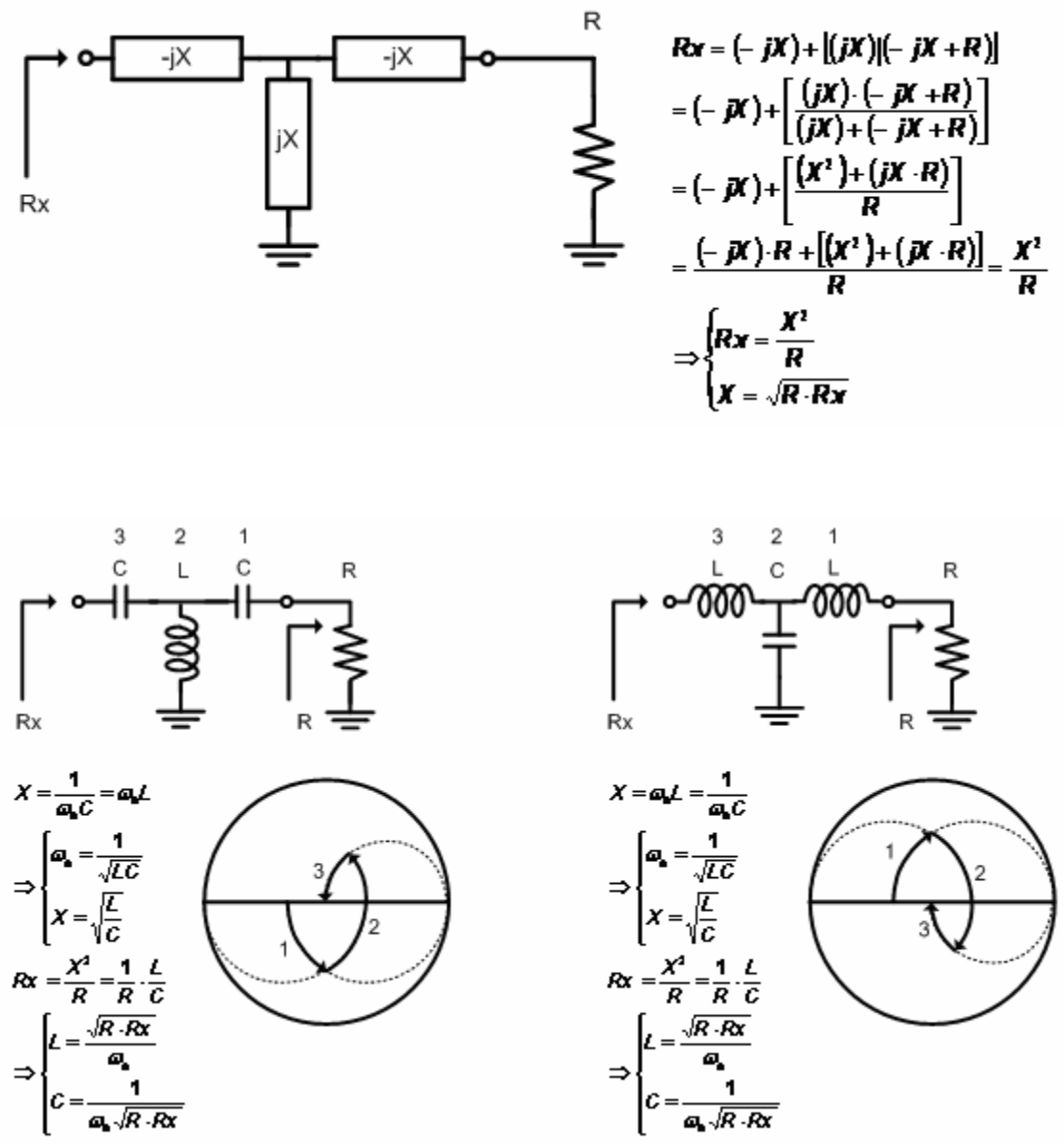


Fig. 2.5 Four types of the L-section with the corresponding design equations.

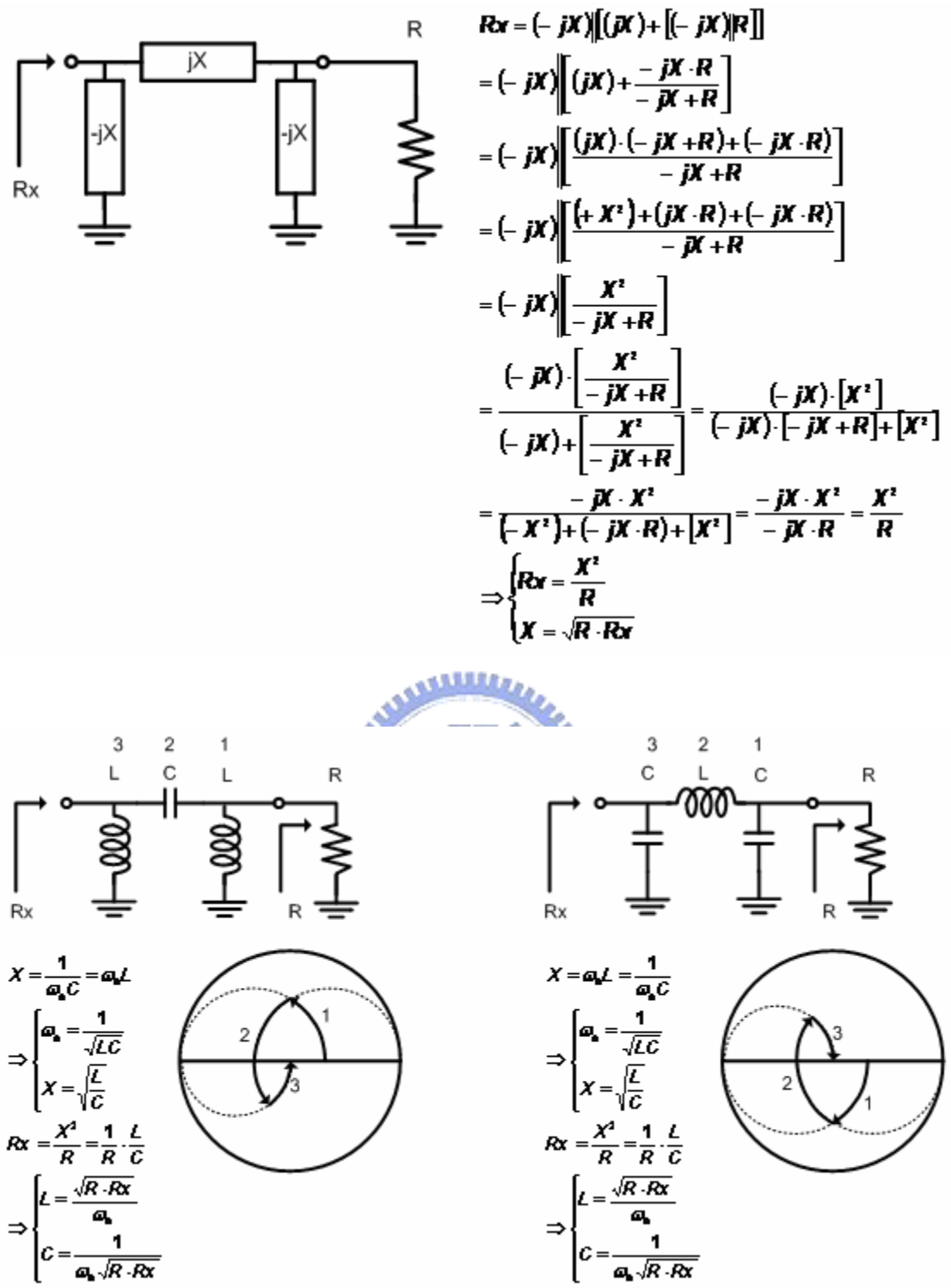


$$Rx = (-jX) + [(jX)\|(-jX+R)]$$
$$= (-jX) + \left[\frac{(jX)\cdot(-jX+R)}{(jX)+(-jX+R)}\right]$$
$$= (-jX) + \left[\frac{(X^2)+(jX\cdot R)}{R}\right]$$
$$= \frac{(-jX)\cdot R + [(X^2)+(jX\cdot R)]}{R} = \frac{X^2}{R}$$
$$\Rightarrow \begin{cases} Rx = \dfrac{X^2}{R} \\ X = \sqrt{R\cdot Rx} \end{cases}$$

$$X = \frac{1}{\omega_0 C} = \omega_0 L$$
$$\Rightarrow \begin{cases} \omega_0 = \dfrac{1}{\sqrt{LC}} \\ X = \sqrt{\dfrac{L}{C}} \end{cases}$$
$$Rx = \frac{X^2}{R} = \frac{1}{R}\cdot\frac{L}{C}$$
$$\Rightarrow \begin{cases} L = \dfrac{\sqrt{R\cdot Rx}}{\omega_0} \\ C = \dfrac{1}{\omega_0\sqrt{R\cdot Rx}} \end{cases}$$

$$X = \omega_0 L = \frac{1}{\omega_0 C}$$
$$\Rightarrow \begin{cases} \omega_0 = \dfrac{1}{\sqrt{LC}} \\ X = \sqrt{\dfrac{L}{C}} \end{cases}$$
$$Rx = \frac{X^2}{R} = \frac{1}{R}\cdot\frac{L}{C}$$
$$\Rightarrow \begin{cases} L = \dfrac{\sqrt{R\cdot Rx}}{\omega_0} \\ C = \dfrac{1}{\omega_0\sqrt{R\cdot Rx}} \end{cases}$$

Fig. 2.6 Four types of the T-section with the corresponding design equations.



$$Rx = (-jX) \| [(jX) + [(-jX) \| R]]$$

$$= (-jX) \left\| \left[(jX) + \frac{-jX \cdot R}{-jX + R} \right] \right.$$

$$= (-jX) \left\| \left[\frac{(jX) \cdot (-jX + R) + (-jX \cdot R)}{-jX + R} \right] \right.$$

$$= (-jX) \left\| \left[\frac{(+X^2) + (jX \cdot R) + (-jX \cdot R)}{-jX + R} \right] \right.$$

$$= (-jX) \left\| \left[\frac{X^2}{-jX + R} \right] \right.$$

$$= \frac{(-jX) \cdot \left[\frac{X^2}{-jX + R} \right]}{(-jX) + \left[\frac{X^2}{-jX + R} \right]} = \frac{(-jX) \cdot [X^2]}{(-jX) \cdot [-jX + R] + [X^2]}$$

$$= \frac{-jX \cdot X^2}{(-X^2) + (-jX \cdot R) + [X^2]} = \frac{-jX \cdot X^2}{-jX \cdot R} = \frac{X^2}{R}$$

$$\Rightarrow \begin{cases} Rx = \dfrac{X^2}{R} \\ X = \sqrt{R \cdot Rx} \end{cases}$$

$$X = \frac{1}{\omega_0 C} = \omega_0 L$$

$$\Rightarrow \begin{cases} \omega_0 = \dfrac{1}{\sqrt{LC}} \\ X = \sqrt{\dfrac{L}{C}} \end{cases}$$

$$Rx = \frac{X^2}{R} = \frac{1}{R} \cdot \frac{L}{C}$$

$$\Rightarrow \begin{cases} L = \dfrac{\sqrt{R \cdot Rx}}{\omega_0} \\ C = \dfrac{1}{\omega_0 \sqrt{R \cdot Rx}} \end{cases}$$

$$X = \omega_0 L = \frac{1}{\omega_0 C}$$

$$\Rightarrow \begin{cases} \omega_0 = \dfrac{1}{\sqrt{LC}} \\ X = \sqrt{\dfrac{L}{C}} \end{cases}$$

$$Rx = \frac{X^2}{R} = \frac{1}{R} \cdot \frac{L}{C}$$

$$\Rightarrow \begin{cases} L = \dfrac{\sqrt{R \cdot Rx}}{\omega_0} \\ C = \dfrac{1}{\omega_0 \sqrt{R \cdot Rx}} \end{cases}$$

Fig. 2.7 Four types of the π-section with the corresponding design equations.

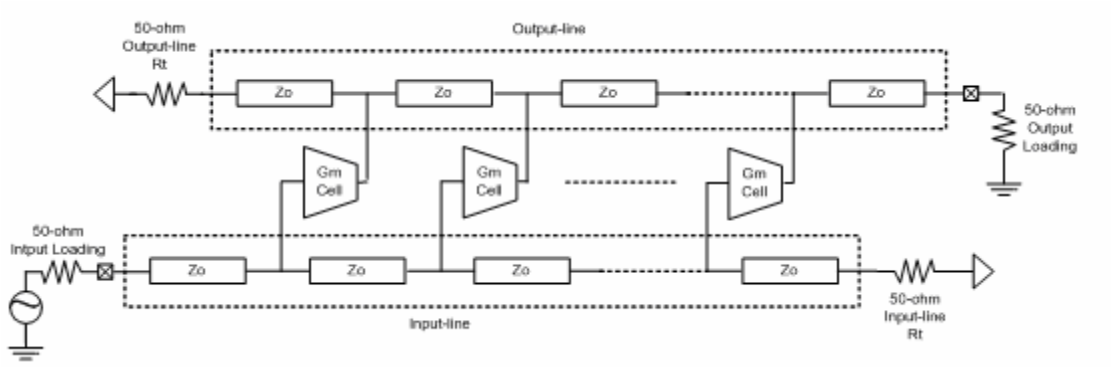


Fig. 2.8 Conventional distributed amplifier architecture.

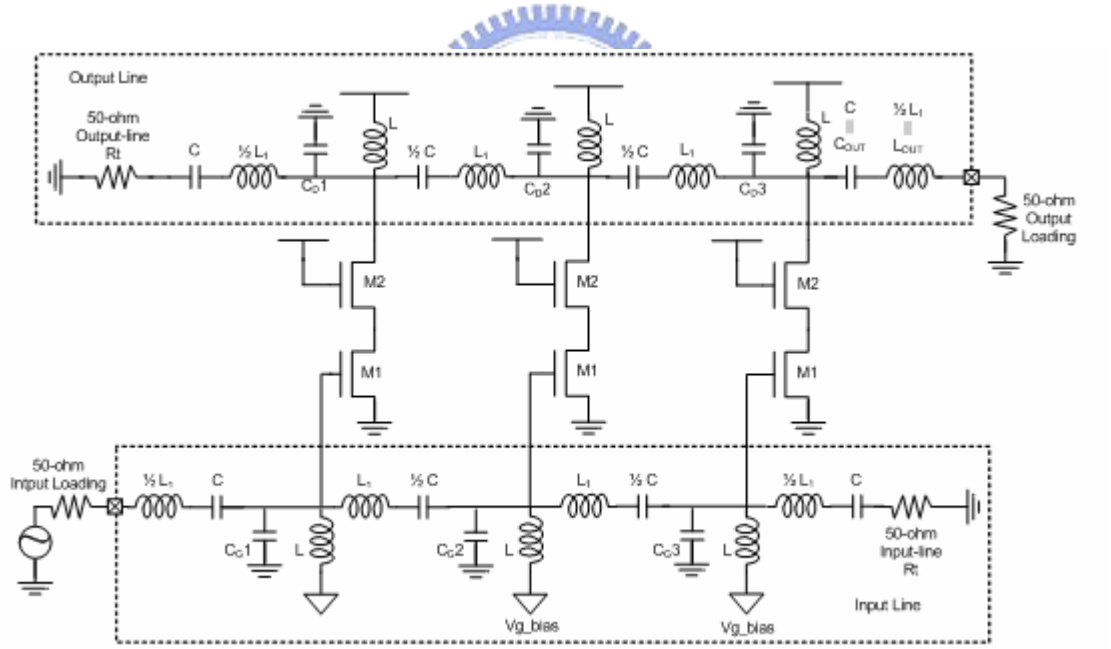


Fig. 2.9 Typical circuit implementation of the conventional distributed amplifier architecture.

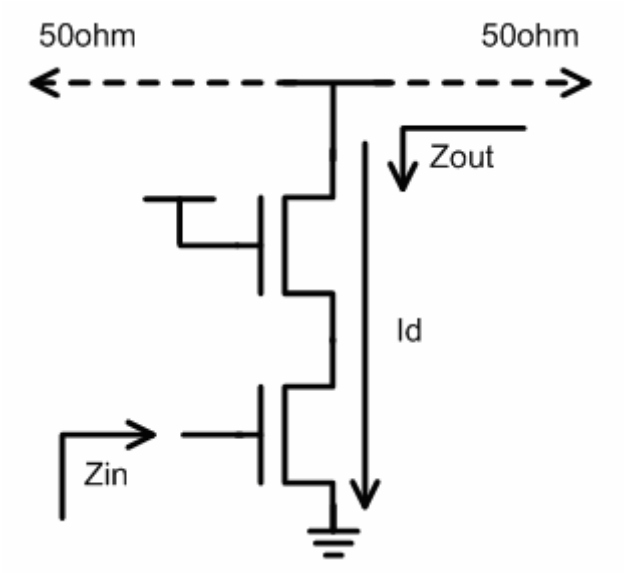


Fig. 2.10 Loading condition of each Gm-cell.

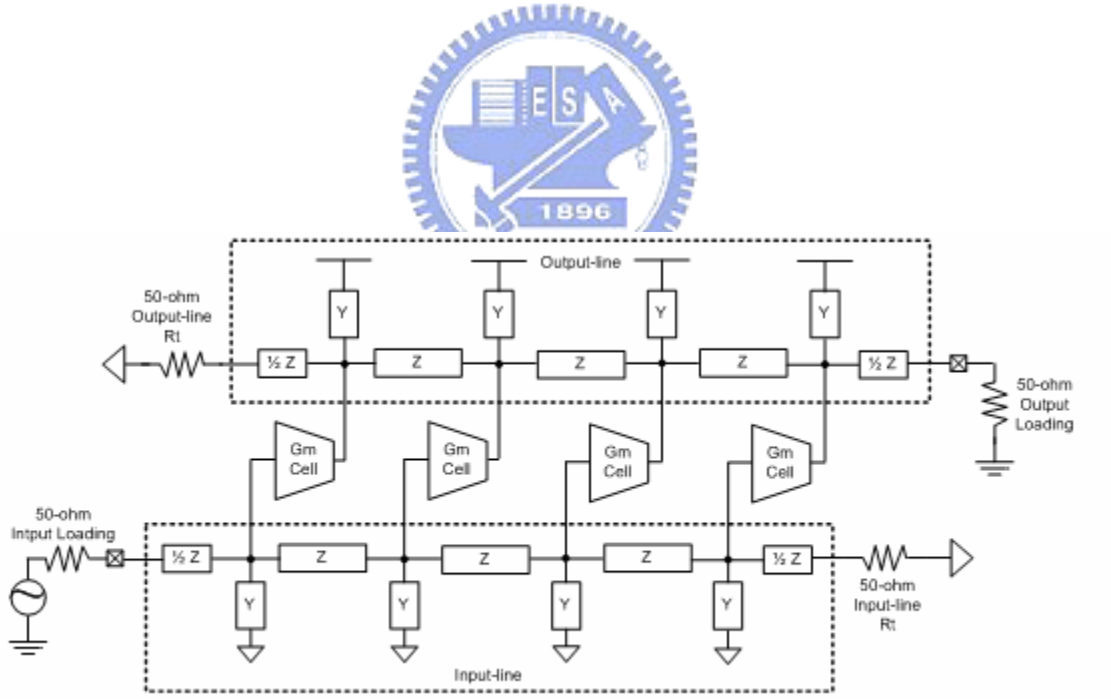
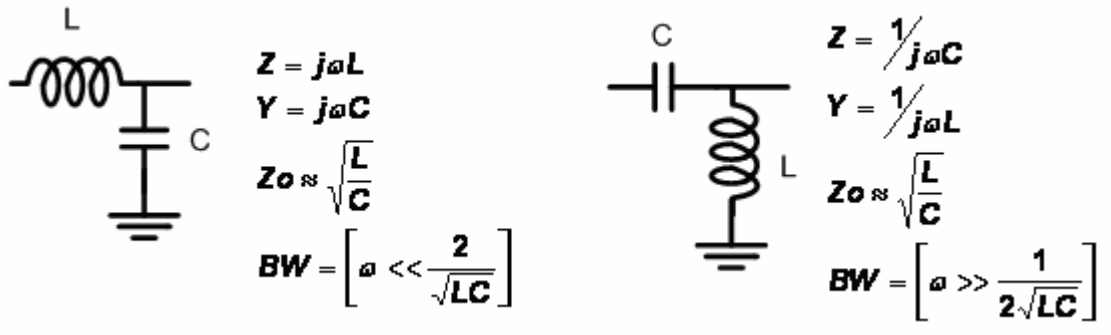
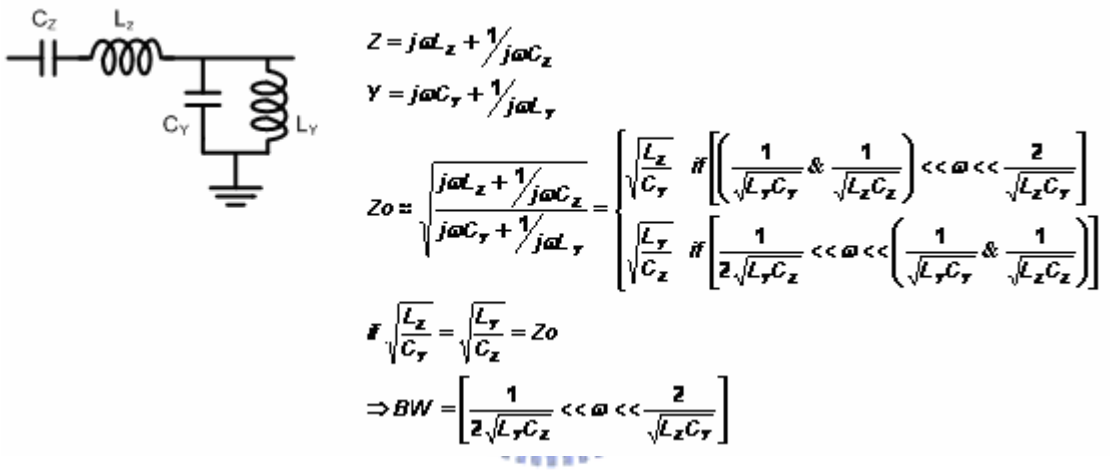


Fig. 2.11 Distributed amplifier with artificial line.



(a) (b)



(c)

Fig. 2.12 Detailed artificial line structure and corresponding design equations of (a) low-pass line, (b) high-pass line, and (c) band-pass line.

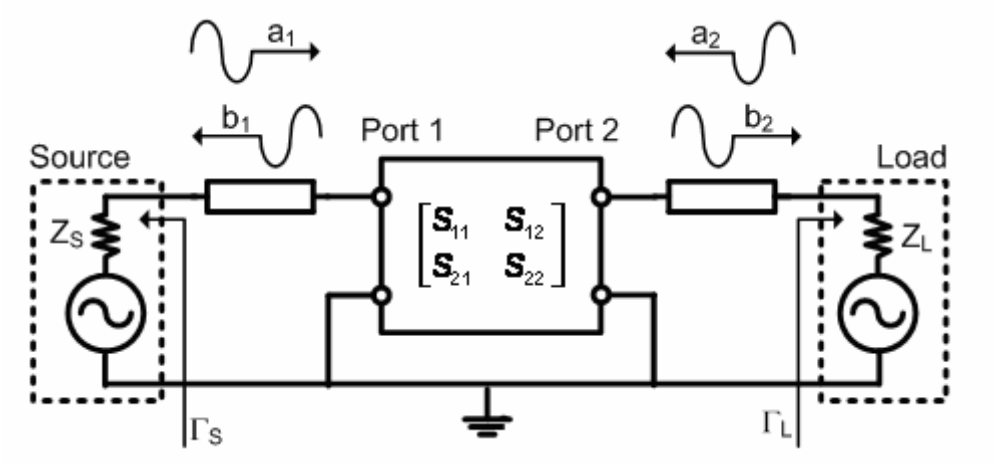


Fig. 2.13 Demonstration of the system characterized by the S-parameters.

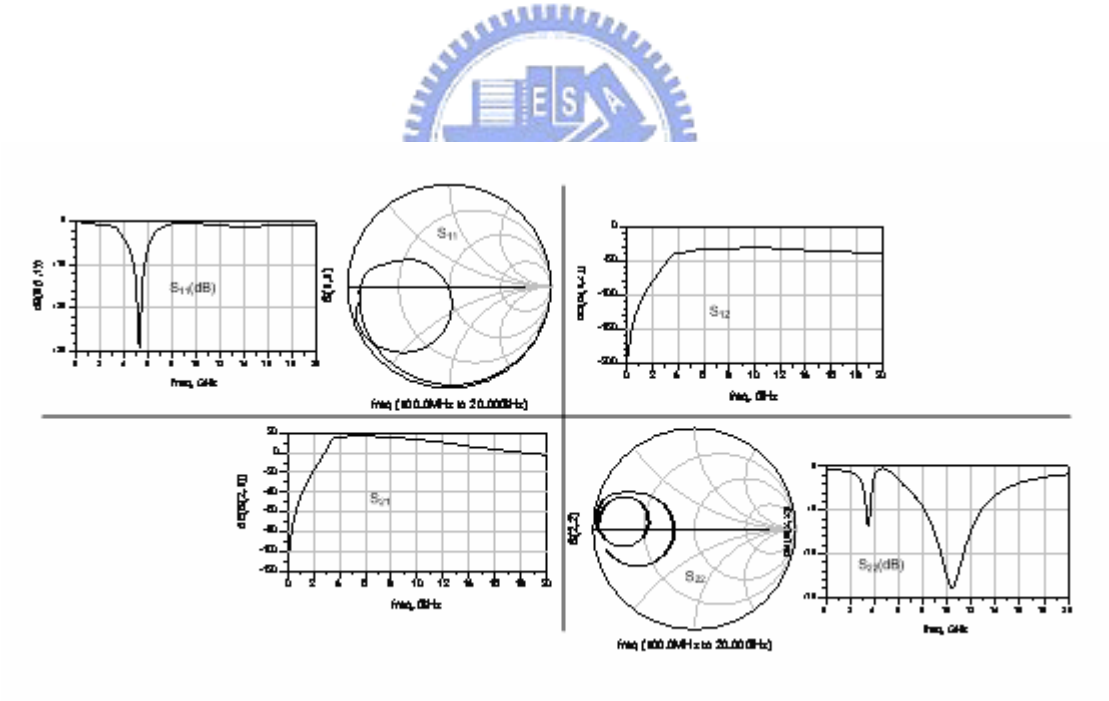


Fig. 2.14 Demonstration of the S-parameters of a typical PA.

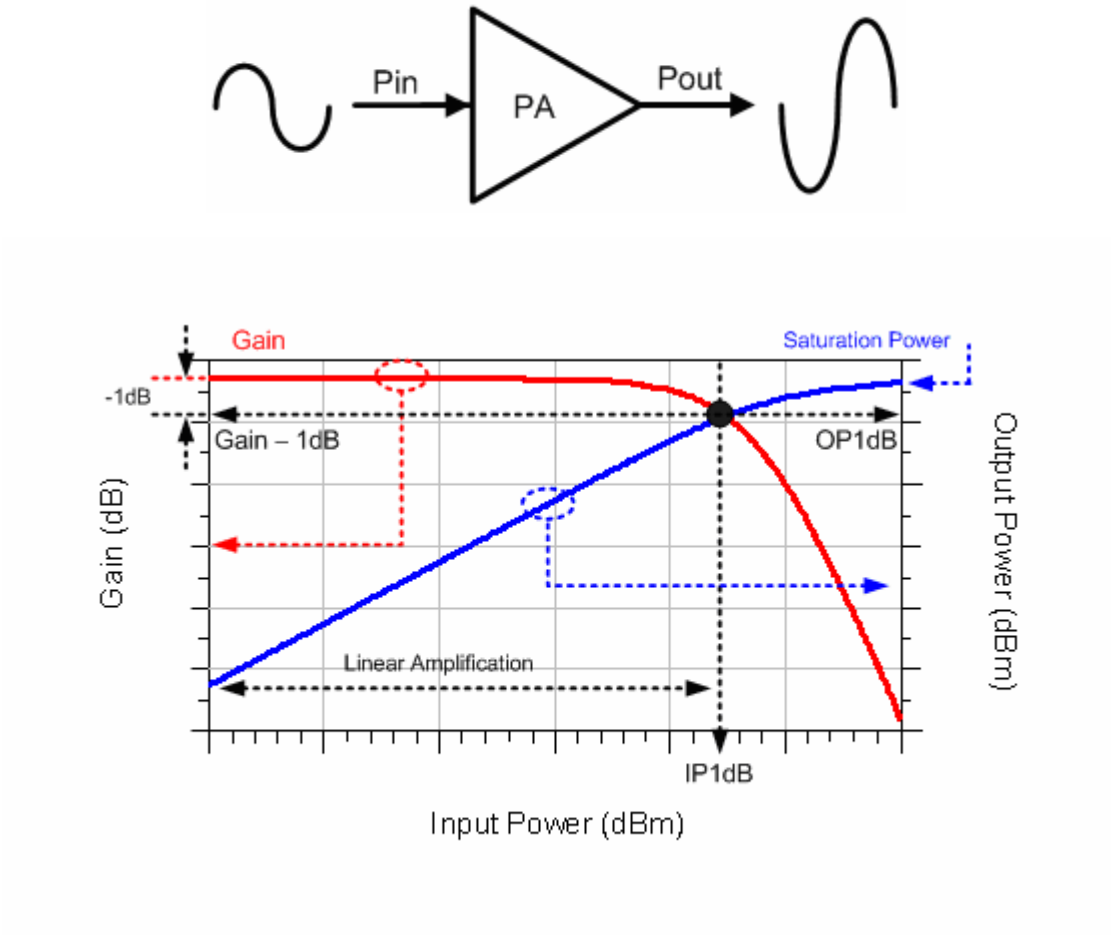


Fig. 2.15 Power transfer characteristic (PTC) of a PA.

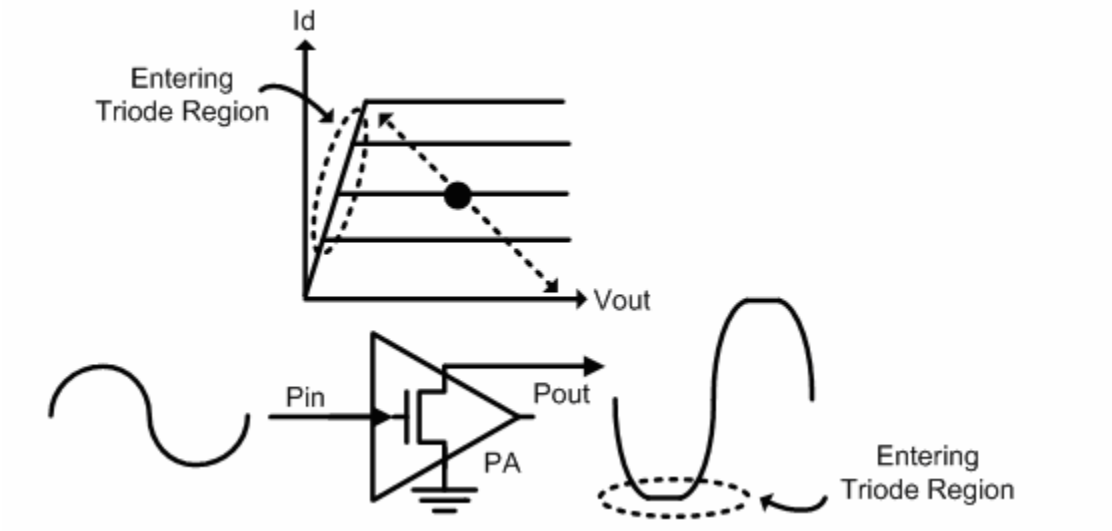


Fig. 2.16 Maximal linear operation limit of the PA active devices when 1-dB compression point is approached.

Chapter 3

RF ESD Protection Basics

3.1 ESD TESTING BASICS

3.1.1 ESD Testing Pin Assignments

Fig. 3.1 shows a typical pad layout allocation of a RF system IC. The input and output (I/O) pads of a RF system are in GSG style, providing good shielding and wave-guiding capability for signal power waves. The VDD pad provides the DC power supply for the system. All the GND pads should be carefully connected all together internally or externally to provide a stable voltage reference level for RF signals.

The ESD energy enters an IC device most likely through its I/O VDD, and GND pads, in the form of a discharging current or voltage overstress. All these pads serve as the communication interface between the IC internal circuits and the external environment. Through these pads, however, ESD current can also find its way and discharge into the IC, causing damage to the IC internal circuits. Therefore, the first priority of the ESD protection circuits is to shunt away the ESD current at the very first moment whenever the ESD current appears at the I/O, VDD, or GND pads.

There are four configurations of ESD testing pin assignments for I/O pads. Namely, they are PS-mode, NS-mode, PD-mode, and ND-mode, as shown in Fig. 3.2 (a) to (d). With these four configurations, the ESD robustness of an I/O pad can be thoroughly verified against all the ESD zap situations [15].

ESD testing pin assignments for VDD pads are shown in Fig. 3.3 (a) and (b).

Namely, they are positive VDD-to-VSS mode and negative VDD-to-VSS mode. With these two modes, the ESD robustness of a VDD pad can be thoroughly verified against all the ESD zap situations.

3.1.2 ESD Testing Models

There are three typical ESD testing models for industrial standards. Namely, they are Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM) [15]. These models define how semiconductor devices are being tested for ESD robustness under different situations of the build-up and discharge of electrostatic charges. Their equivalent testing circuit models and corresponding ESD energy characteristics are shown in Fig. 3.4, Fig. 3.5, and Fig. 3.6, respectively. The damage caused by ESD energy comes into two classes. One is the heat generated by the ESD current flowing through a resistive component. Power is generated in the form of heat, as shown in equation (3.1).

$$Power = I_{ESD}^2 \cdot R \tag{3.1}$$

This heat may damage the via and contacts of the interconnect or alter the doping profiles of well, diffusion, and substrate, changing the characteristics of active devices.

The other class of ESD damage is the overstress of ESD voltage potential. Strong electrical field accompanying the ESD overstress voltage may exceed the dielectric strength of the IC interior insulators and punch through the dielectric layers, such as the gate oxide layer of a MOSFET, causing device to fail.

The following sub-sections describe the 3 models in details.

(1) HBM

The Human Body Model (HBM) simulates the electrostatic discharge

phenomenon wherein a charged human body directly transfers all the accumulated electrostatic charges to an IC through its I/O interface or power supply pads. These electrostatic charges stored on a human body commonly occur when a person accumulates static charges by walking or any other mechanisms. Other non-human materials that accumulate and transfer charge in a similar manner are also covered by the HBM.

The HBM is the most commonly used model for testing the ESD robustness of an IC device. The general HBM ESD testing set-up for this model consists of a 100pF capacitor that can be charged to a certain voltage, and then discharged by a switching component into the device under test through a 1.5k-ohm resistor. Fig. 3.4 (a) shows the basic HBM test circuit.

Fig. 3.4 (b) illustrates a typical 2-kV HBM ESD current waveform. Fig. 3.4 (c) illustrates the corresponding power spectrum of the HBM ESD current. A typical 2-kV HBM ESD event may reach an instantaneous peak current of 1.33 amperes within 2~10ns, and an average current of several amperes within a HBM ESD duration of several hundreds ns.

(2) MM

The Machine Model (MM) simulates a more rapid and severe electrostatic discharge from a charged robotic arm, testing fixture, or tool of any kinds, as compared to the HBM. The general MM testing set-up consists of charging up a 200pF capacitor to a certain voltage and then discharging this capacitor directly into the device under test through a 500nH inductor with no series resistor. Figure 3.5 (a) shows the basic MM test circuit.

In the MM the stored electrostatic charges are much more than that in the HBM, since the storing capacitance is larger. Further more, the MM has no resistance (though, practically a few ohms) on the discharging path, and therefore the MM ESD

event is faster. Thus, the ESD current in the MM is much larger than that in the HBM.

Fig. 3.5 (b) illustrates a typical 400-V MM ESD current waveform. Fig. 3.5 (c) illustrates the corresponding power spectrum of the MM ESD current. A typical 400V MM ESD event may reach an instantaneous peak current of 6~8 amperes within 10~20 ns. Besides, there is a 500nH inductance on the discharging path. The effect of this inductor is that the MM ESD current appears as a positive-negative alternating style. This oscillatory MM ESD current causes even severer damage to IC devices.

(3) CDM

The Charged Device Model (CDM) simulates the electrostatic discharge from a charged IC device to another body (usually at the level of external ground). A device can accumulate electrostatic charges in a variety of ways, especially in situations where they undergo movement while in contact with another object, such as when sliding down a track or feeder. If they come into contact with another conductive body that is at a lower potential, it discharges into that body. This ESD current flows from the interior of the IC outward to the exterior and cause damage in the discharging process. Figure 3.6 (a) shows the basic CDM test circuit.

There is no equivalent circuit model for CDM, since the device under test possesses different equivalent circuit model according to different IC physical package, position, and even orientation. Therefore, it is difficult to simulate and predict the CDM ESD event. However, typically CDM can even be more destructive than HBM and MM ESD (despite its shorter pulse duration) because of its high current. From Fig. 3.6 (a) it can be seen that the discharging path has only 1 ohm resistance, and the CDM ESD event can be generally faster and severer than MM.

Fig. 3.6 (b) illustrates a typical 400-V CDM ESD current waveform. Fig. 3.6 (c) illustrates the corresponding power spectrum of the HBM ESD current. Typically a 400V CDM ESD current reaches its peak about tens of amperes within a few ns.

Therefore, it is expected that the CDM ESD is much more destructive than the MM and HBM ESD.

3.1.3 Failure Criteria of RF Circuits

Fig. 3.7 shows a traditional mixed-voltage I/O interface circuit of an IC [7-9]. Fig. 3.8 shows a general RF I/O interface circuit specifically designed for RF application [10]. Comparing these two figures, it can be noticed that the RF I/O interface circuit contains numerous passive device networks in between the active devices (LNA core, PA core, and the RF switch core) and the RF I/O pads. These passive device networks serve as filters and impedance transformers for RF signal processing. On the other hand, the traditional mixed-voltage I/O interface circuit has its active devices directly connected to the I/O pads. Further, they possess quite different circuit topologies in their nature. Consequently, two types of I/O interfaces exhibit different influences caused by ESD events.

In the traditional mixed-voltage I/O interface, the enormous and destructive ESD current directly damages the active device drain terminals. The consequence is an increase in the device dc leakage current and, even further, malfunctions of device operation in the form of drain-opening.

In the general RF I/O interface, the ESD current firstly encounters the passive device networks. Destructive current flows through these passive devices and causes shifting in the device characteristics, such as metal migration and a consequent increase in the series parasitic resistance. The active devices are damaged in succession. Depending on the circuit topology, the active devices may be directly zapped by the ESD current flowing through a connected metal traces, or non-directly zapped by the strong electrical field of the ESD overstress voltage potential coupled through a capacitor.

An increase in the dc leakage current of the device under test is the usual failure criterion for traditional mixed-voltage I/O interfaces. However, it is not clear that an increase in the dc leakage current can reliably predict performance degradation, or even failure, of a radio frequency (RF) circuit. The damage on any passive device networks may have an even more profound performance shift in RF operation since it alters the characteristics of a filter or matching network. It is showed in [11] that the performance of RF circuits and devices can degrade at ESD stress levels below the failure level established with a commercial HBM ESD tester. In [12], a combined TLP/RF ESD testing system for the detection of ESD failures in RF circuits is proposed and established to perform RF functionality tests, along with the conventional dc leakage current measurement, after each ESD testing zap to detect failure.

In short, it is evident that the ESD influence on RF system ICs needs to be qualified not just solely by a simple dc leakage current test but also by a complete RF functionality test. For complete RF PA ESD qualifications, the dc leakage current test incorporates the dc leakage current when the PA is off and the dc bias current when the PA is on. The RF functionality test incorporates the S-parameters measurement and the large signal RF operation.

3.2 Conventional Whole-chip ESD Protection Architecture

3.2.1 General Architecture

In order to provide an effective ESD protection for nano-scale RF CMOS ICs against unexpected ESD damages to the internal circuits, the on-chip ESD protection circuits have to be designed and placed around the input, output, and power pads. The

on-chip ESD protection circuits are to clamp the overstress voltage across the internal circuits and to discharging the ESD current of several amperes. The ESD protection circuits shunt away the destructive ESD current at the very first moment whenever the ESD current appears at the I/O, VDD, or GND pads. The locations of the ESD protection circuits to achieve whole-chip ESD protection for CMOS ICs are illustrated in Fig. 3.9 (a) [1].

The whole-chip ESD protection architecture consists of a pair of I/O ESD clamp and a power rail ESD clamp. When an ESD event happens, the I/O ESD clamp provides a low impendence path for ESD current and discharge the ESD current to the power rail (VDD and GND lines), preventing the ESD current to flow directly into the internal circuit and cause damage. The low impedance nature of the I/O ESD clamps is also capable of clamping the ESD overstress voltage which may damage the internal thin oxide layers by its strong electrical filed. The power rail ESD clamp serves a similar function to clamp the VDD-to-GND overstress and discharge the ESD current on the power rail. Since RF circuits incorporate numerous passive devices in between the I/O pads and the internal circuits, it is possible to design a signal line blocker. The signal line blocker can serve for RF normal operation purpose and also a passive network that appears open, such as a dc-coupling MIMCAP, for the ESD events in between the I/O pads and the internal circuits, as shown in Fig. 3.9 (b). In such manner, the I/O pads and internal circuit cores are isolated, resulting less possibility of direct damage by ESD current.

3.2.2 Power Rail ESD Clamp

Typical power rail ESD clamp architecture is illustrated in Fig. 3.10 (a) [16]. It consists of an ESD event detector, a clamp trigger circuit, and a main clamp device. The ESD event detector first detect if there is an ESD energy burst on the power rail.

The clamp trigger circuit is then activated and use a minor share of the ESD energy to send out a trigger signal. The main clamp device is then activated and forms a low impedance path to discharge the ESD energy on the power rail.

A conventional ESD event detector is a RC-detector. It makes use of a RC time constant to distinguish a normal power-on event and an ESD event. The speed of a normal power-on event is on the order of millisecond, and the speed of an ESD event is on the order of nanosecond. Therefore, if the RC time constant is designed to be on the order of microsecond, the ESD detector can easily distinguish the normal power-on event and the ESD event.

A conventional clamp trigger circuit is simply a CMOS inverter. For a normal power-on event, the ESD event detector output remains at high level; the resistor in the ESD event detector pulls the input of the clamp trigger circuit to the VDD level. Therefore, the N-MOS is turned on and the clamp trigger circuit output is held at GND level. When an ESD event happens, the whole circuit is floating, and a sudden burst of ESD voltage potential appears on the power rail. By proper design of the RC time constant in the ESD event detector, the capacitor in the ESD event detector holds the input of the clamp trigger circuit at GND level. Therefore, the P-MOS is turned on and the clamp trigger circuit conducts a partial share of the ESD current right in time. This current flows toward the main clamp device and forms the trigger current.

The main clamp device can be in various embodiments. A simple N-MOS of a large enough size (typically several hundreds of micrometers) can serve very well, as shown in Fig. 3.10 (b). A parasitic bipolar transistor inherent in the N-MOS structure can also function satisfactorily, as shown in Fig. 3.10 (c). A silicon-controlled rectifier (SCR) device is probably the most cost-effective solution for nano-scale CMOS ICs. The details of the SCR device will be addressed in the following section.

3.2.3 I/O ESD Clamp

Parasitic capacitance has a profound negative impact on the RF circuit performance. Since the operation frequency is high enough, even a tiny capacitance on the signal traces may result in relative low impedance and cause a great deal of RF signal loss.

The main parasitic capacitance contributed by the ESD protection circuit comes from the I/O ESD clamp. Therefore, it is unacceptable for the I/O ESD clamp to have a large capacitance value. A traditional I/O ESD clamp is a pair of a GGNMOS and a PGPMOS, as shown in Fig. 3.11 (a) [7, 9, 16, 17]. GGNMOS stands for grounded-gate N-MOS. PGPMOS is a P-MOS whose gate is connected to the VDD power line. The NS-mode and PD-mode ESD energy can be discharged through the parasitic diodes of the GGNMOS and the PGPMOS. The worst case of ESD event is the PS-mode and ND-mode. The ESD energy is discharged through drain breakdown of the GGNMOS and the PGPMOS. The drain breakdown is activated by a relative high switching voltage, as compared to a diode. Thus, it is triggered on much more slowly and clamps the I/O at a much higher voltage level (several volts). As a result, this type of I/O ESD clamp may not be suitable for nano-scale CMOS ICs. Further, this type of I/O ESD clamp contributed an unacceptable amount of parasitic capacitances, mainly comes from the gate oxide capacitance.

A practical solution is illustrated in Fig. 3.11 (b). The I/O ESD clamp is simply a pair of diodes. Since diodes can endure a large amount of current within a relative small die area. It can also clamp the I/O at an almost constant small voltage drop (about 0.7V) when forward biased. Thus, it is suitable to clamp the ESD overstress and discharge the ESD current. The discharged ESD energy through the I/O ESD clamp then reaches the power rail. The power rail ESD clamp can take care of remaining discharging of the ESD energy on the power rail. The corresponding ESD

zapping modes are illustrated in Fig. 3.12 and Fig. 3.13. Practically the diode only occupies a small amount of die area, and thus the parasitic capacitance of this I/O ESD clamp is quite small. The main parasitic capacitance of the on-chip diodes comes from the p-n junction. While normal operation the I/O ESD clamp diodes are reverse biased, and the junction parasitic capacitances are acceptably small. The power rail ESD clamp has theoretically no influence on the RF performance since it adds parasitic capacitance only on the power rail. The power rail ESD clamp can thus be designed with arbitrary ESD robustness without degrading the RF performance. Therefore, the key to high whole-chip ESD robustness without severely degrading the RF performance is to design the I/O ESD clamp with minimum parasitic capacitance but acceptable ESD capability.

The input port of a RF PA is usually integrated with internal circuits, such as up-converter or PA pre-driver. Therefore, the ESD protection design of a RF PA mainly focuses on the PA output port. For such a large signal operation of a PA, the I/O ESD clamp must be designed with additional caution to prevent unexpected activation of the I/O ESD clamp responding to the large signal swing at PA output port. In the whole-chip ESD protection architecture, this is accomplished by cascading a few up-ward diodes in between the output port and the VDD rail. The diode string remains off when normal operation, not cutting in for normal signal swing. However, more diodes mean higher impedance on the discharging path. Certainly it degrades the ESD protection capability, and trade-off comes in between safe operation and ESD robustness.

3.3 LOW-C ESD DEVICES

3.3.1 Silicon-controlled Rectifier Basics

For a specific ESD robustness, the I/O ESD clamp diode must occupy at least a certain amount of die area. It possesses a nonnegotiable amount of parasitic capacitance for a given ESD robustness. Therefore, the limit of RF performance is preset in advance once the ESD robustness specification is given.

To mitigate this problem, it is desired to use another device with similar ESD clamp capability but smaller die area. A SCR device can serve. The SCR device can sustain a much higher ESD level within a smaller layout area in CMOS ICs, so it has been used to protect the internal circuits against ESD damage for a long time. [6], [16].

A basic SCR structure cross-section view and the equivalent circuit schematic are shown in Fig. 3.14. A SCR structure is inherent in the CMOS processes. The SCR device is a 4-layer PNPN structure; it consists of P-plus (P+) diffusion, N-well (NW), P-well (PW), and N-plus (N+) diffusion. These layers (P+/NW/PW/N+) form a 2-terminal device composed of a lateral NPN and a vertical PNP bipolar transistor. A typical I-V characteristic of the SCR device operation is shown in Fig. 3.14 (d). The SCR operation principle is described as follow.

Let's assume that the cathode of the SCR is connected to the ground reference level. Before the positive voltage applied to the anode of the SCR exceeds the switching voltage (Vt1), the SCR acts as an open circuit, exhibiting purely capacitive. The switching voltage of the SCR device is dominated by the avalanche breakdown voltage of the N-well/P-well junction, which could be as much as 18V in a 130-nm CMOS process. When the positive voltage applied to the anode is greater than the NW-PW junction avalanche breakdown voltage, the hole and electron current will be

generated through the avalanche breakdown mechanism. The hole current will flow through the P-well to P+ diffusion connected to the cathode of SCR, whereas the electron current will flow through the N-well to N+ diffusion connected to the anode of SCR. Once the voltage drop across the P-well resistor (R_{PWELL}) (the N-well resistor (R_{NWELL})) is greater than 0.7V, the NPN (PNP) transistor will be turned on to inject the electrons (holes) to further bias the PNP (NPN) transistor. The consequence is the initiation of the SCR latching action which is intrinsically a positive-feedback regenerative mechanism. Once the positive-feedback regenerative mechanism is initiated, the SCR will be successfully triggered into its latching state through this positive-feedback regenerative mechanism.

Once the SCR is triggered on, the required holding current to keep both the NPN and PNP transistors on can be generated through the positive-feedback regenerative mechanism of latch-up without involving the avalanche breakdown mechanism again. Therefore, the SCR has a lower holding voltage (Vh) of typical 1.5 V in the bulk CMOS processes.

If the negative voltage is applied on the anode terminal of the SCR, the parasitic diode (N-well/P-well junction) inherent in SCR structure will be forward biased to clamp the negative voltage at a lower voltage level of 1 V (cut-in voltage of a diode).

In short, whatever the ESD energy is either positive or negative, the SCR device can clamp ESD overstresses to a lower voltage level. Therefore, the SCR device can sustain the highest ESD robustness within a smallest layout area in CMOS ICs.

3.3.2 Practical SCR structure

A slight modification on the SCR structure gives it faster turn-on efficiency and the ability to be triggered on by an external trigger circuit, as shown in Fig. 3.15 [6]. Once an additional p-plus diffusion layer is inserted right in between the p-well and

n-well layer, the SCR can have a much lower avalanche breakdown voltage since the p-plus diffusion doping concentration is higher than that in the p-well. Therefore, the switching voltage is reduced from the NW-PW junction avalanche breakdown voltage to the NW-P+ junction breakdown voltage. The SCR can then be turned on by a much lower positive anode voltage. Further, if a current is purposefully injected into this p-plus layer, this current serve as the base current of the lateral NPN transistor and thus the lateral NPN transistor can be triggered on. Consequently, the positive-feedback regenerative mechanism of latchup is initiated, and the SCR device will be soon turned on.

3.3.3 Whole-chip ESD Protection with SCR and Trigger Circuit

The detection and trigger circuit of the practical SCR can be exactly the same as the detection and trigger circuit incorporated in the power rail ESD clamp. The RC time constant distinguishes the ESD event from the normal power-on. The inverter-type trigger circuit makes use of a partial share of the ESD current and transfer this current to trigger on the SCR through its trigger terminal. It can be directly and safely applied to the power rail clamp circuit without further modification, as shown in Fig. 3.16. For nano-scale CMOS ICs, such as 130-nm, the VDD is about 1.2V which is lower than the holding voltage of the SCR. Thus no latch-up problem needs to be concerned. If applied to I/O ESD clamp, the detection and trigger circuits need a slight modification, as shown in Fig. 3.17. Fig. 3.18 (a) to (d) illustrate the 4 modes of I/O ESD testing events. The detection and trigger circuits are placed between the VDD and GND lines. From Fig. 3.18 (a) it can be observed that the worst case happens when PS-mode. The ESD energy is first altered to the power rail by the diode string. The detection and trigger circuits then detect and generate a trigger current. This trigger current is fed back to the SCR and triggers the SCR on. Careful

design of the detection and trigger circuit can guarantee the ESD protection circuits react to the ESD event right on time.

3.4 INDUCTIVE ESD DEVICES

3.4.1 ESD Power Spectrum

Typical ESD energy spectrums are illustrated in Fig. 3.3 (c), Fig. 3.4 (c), and Fig. 3.5 (c). It can be concluded that the ESD energy occupy the lower part (at most several hundreds of MHz) of the frequency spectrum as compared to the RF operation frequency (over GHz), as shown in Fig. 3.19 (a). Therefore, a straightforward inference is that it is possible to use a shunted passive device which exhibits low impedance at ESD low frequency but high impedance (or a particular value) at RF high frequency, as shown in Fig. 3.19 (b) [4]. It comes to an inductor. An inductor with inductance L at frequency f exhibits impedance (Z) characterized in equation (3.2)

$$Z = j \cdot 2\pi f \cdot L \tag{3.2}$$

Therefore, a shunted inductor provides an almost shorted path at low frequency but an almost open circuit condition (or a particular value) at high frequency. Further, in chapter 2 it is showed that in RF circuitry inductors are frequently used in the matching networks. Therefore, an inductor is in potential to be incorporated and co-designed for both RF functionality and ESD protection capability.

3.4.2 Inductor Co-design Methodology

[4] proposes a low-noise amplifier which incorporates a RF choke as ESD clamp. The RF choke is an inductor which exhibit nearly infinite impedance at RF frequency.

Therefore, it has no influence on RF circuit operation but has the capability to provide an almost shorted path to effectively discharge the ESD current. Similar ideas can be extended to the inductor co-design methodology. The ultimate goal is to use a single inductor which can serve both for RF functionality and ESD protection capability. Fig. 3.20 and Fig. 3.21 illustrate some potentially applicable RF circuits using this co-design methodology.

Fig. 3.20 (a) uses a RF choke, as in [4]. Further, this inductance can also be part of the matching network, as shown in Fig. 3.20 (b). For narrowband application, an inductor and a capacitor form a resonant tank, exhibiting an open condition at the resonance frequency. Further, the inductor can also serve as the ESD clamp, and the capacitor can be made by a diode or a SCR to serve an additional ESD clamp, as shown in Fig. 3.21 (a) and (b). In Fig. 3.21 (a) the shunted inductor serves as one part of the I/O ESD clamp and also resonates out all the parasitic capacitance at the I/O terminal. In Fig. 3.21 (b) the SCR is triggered on by the detection and trigger circuit activated by the ESD current flowing through the upward diode string to the power rail, as described in section 3.3.3. Proper design of this RC time constant and the trigger circuit may result in excellent capability to discharge the ESD current. The shunted inductor resonates out the SCR parasitic capacitance at the RF operation frequency, and the detection and trigger circuits are both on the power rail, contributing no parasitic capacitance to the I/O terminal. Therefore, impact on the normal RF performance can be minimized. For ultra-wideband application, the distributed ESD protection structure acts as an artificial transmission line and provide constant characteristic impedance over a considerable wide bandwidth, as shown in Fig. 3.21 (c) [18].

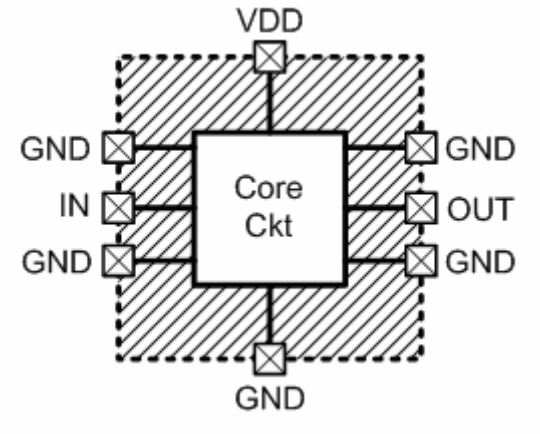


Fig. 3.1 Typical pad layout allocation of a RF system IC.

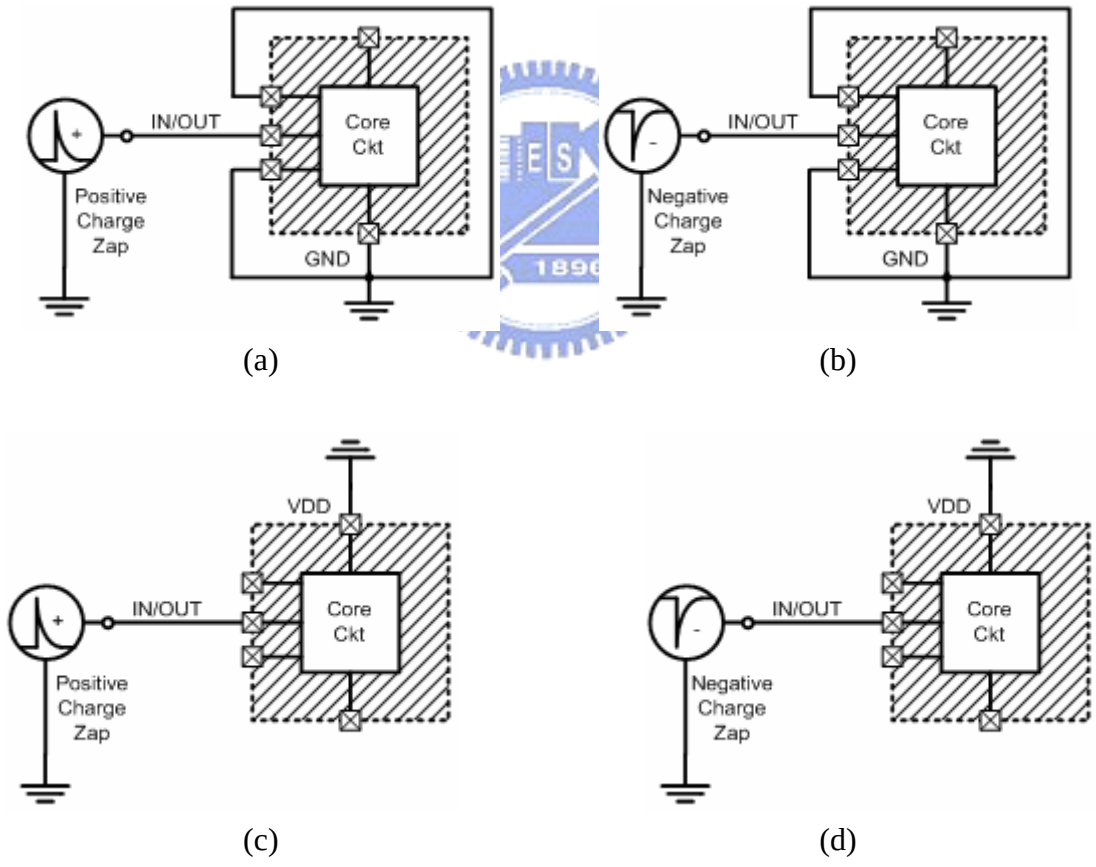
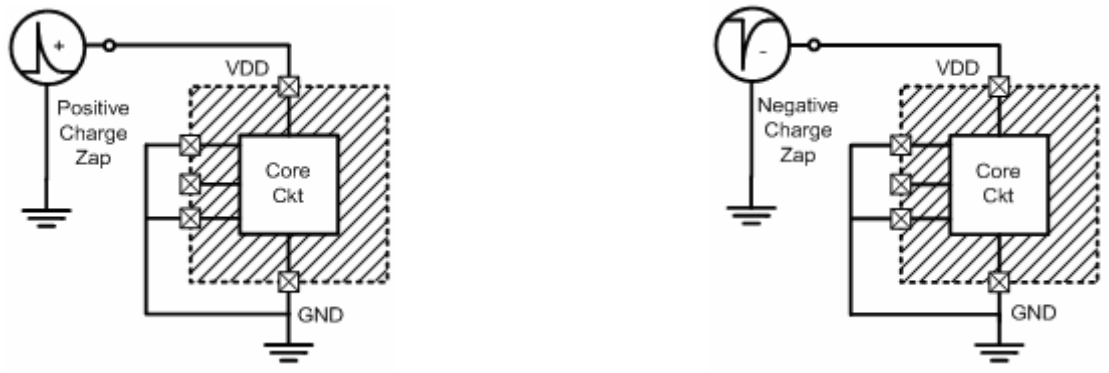
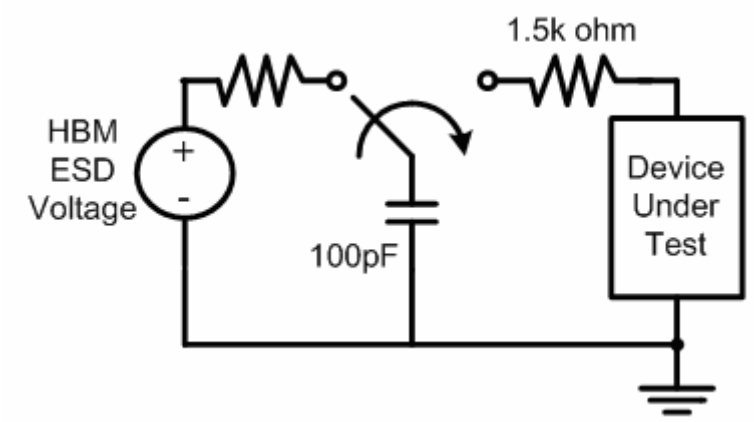


Fig. 3.2 Pin assignments of ESD test zapping for I/O pads of (a) PS-mode, (b) NS-mode, (c) PD-mode, and (d) ND-mode.

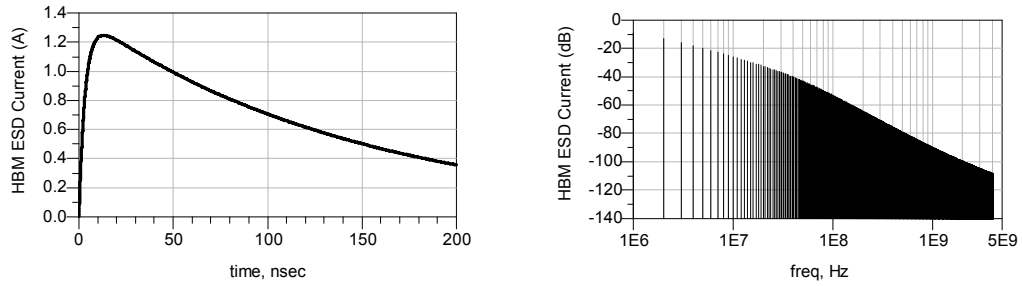


(a) (b)

Fig. 3.3 Pin assignments of ESD test zapping for VDD pads of (a) positive VDD-to-VSS mode and (b) negative VDD-to-VSS mode.

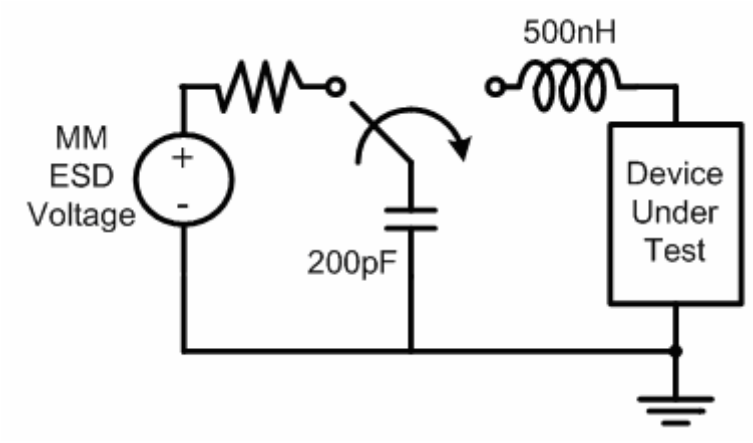


(a)

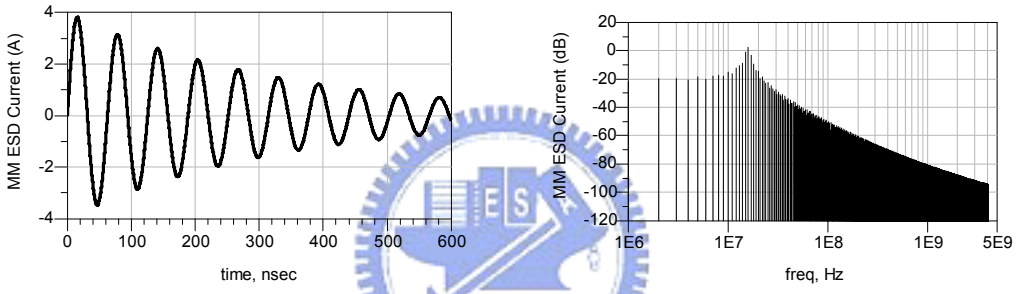


(b) (c)

Fig. 3.4 (a) Equivalent testing circuit models, (b) typical current waveform, and (c) corresponding power spectrum, of human-body-model (HBM) ESD testing.

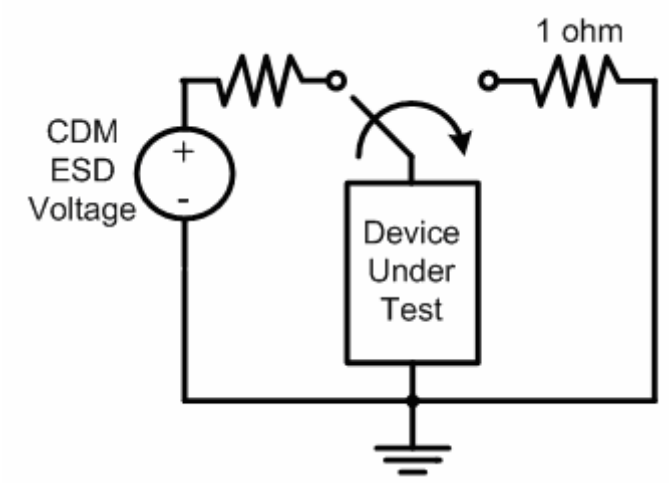


(a)

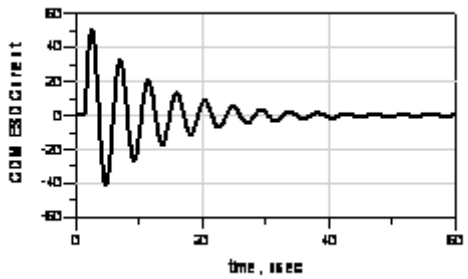


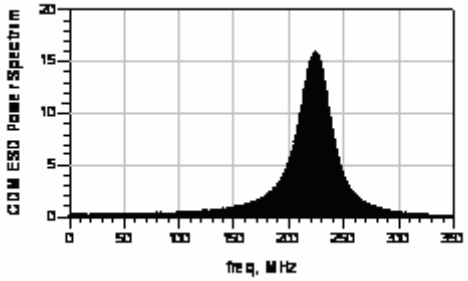
(b) (c)

Fig. 3.5 (a) Equivalent testing circuit models, (b) typical current waveform, and (c) corresponding power spectrum, of machine-model (MM) ESD testing.



(a)





(b) (c)

Fig. 3.6 (a) Equivalent testing circuit models, (b) typical current waveform, and (c) corresponding power spectrum, of charged-device-model (CDM) ESD testing.

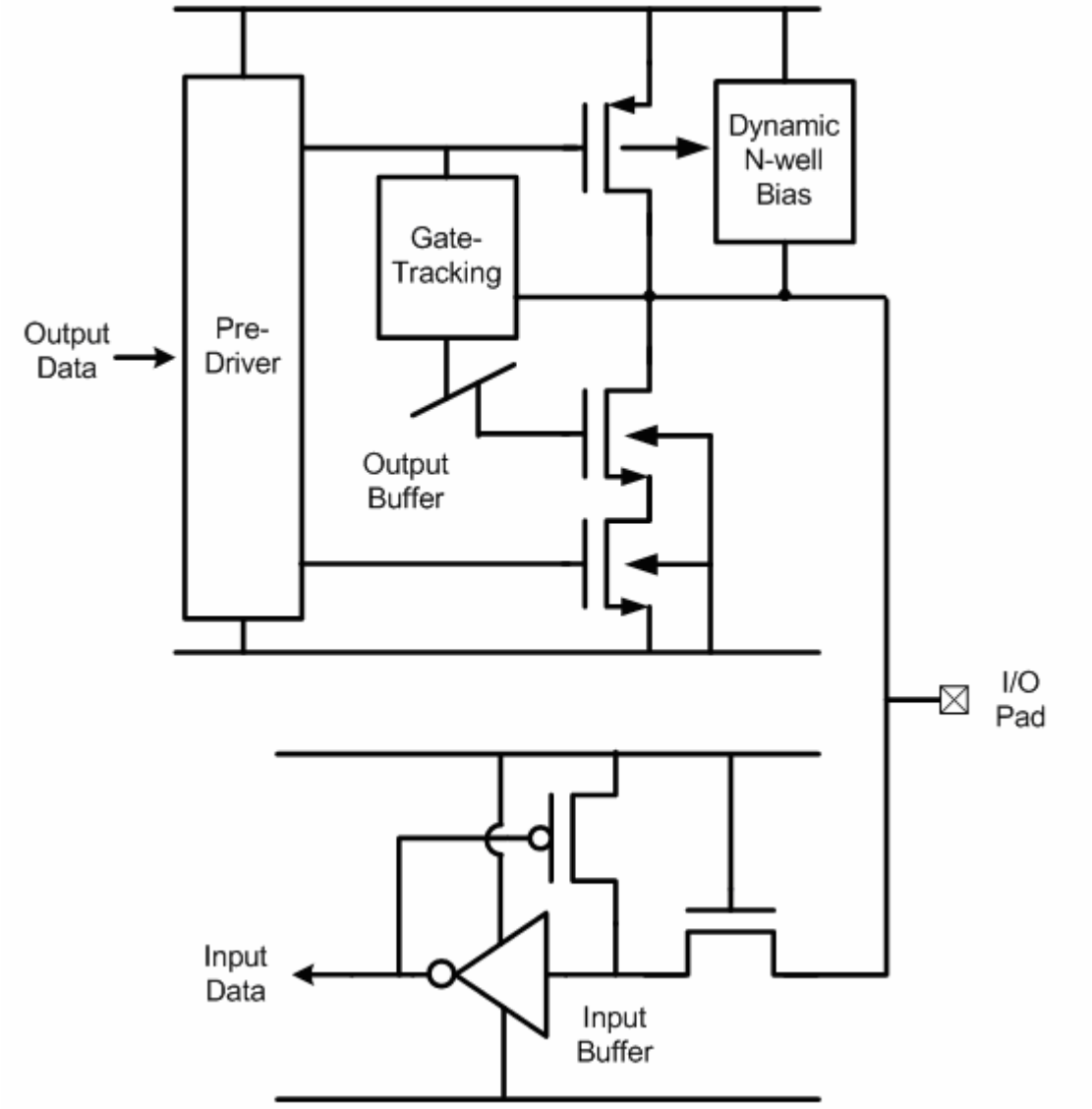
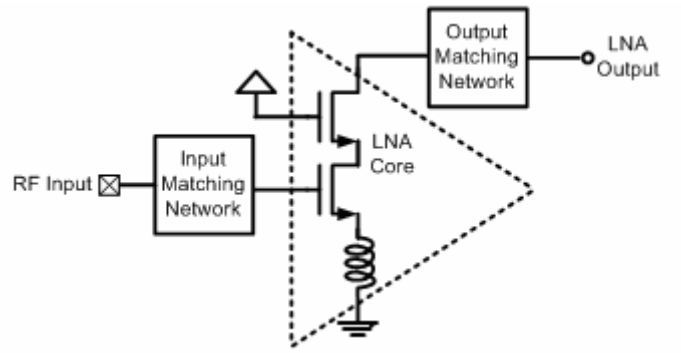
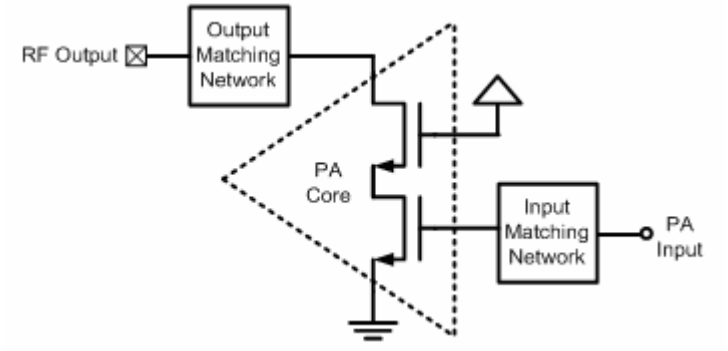


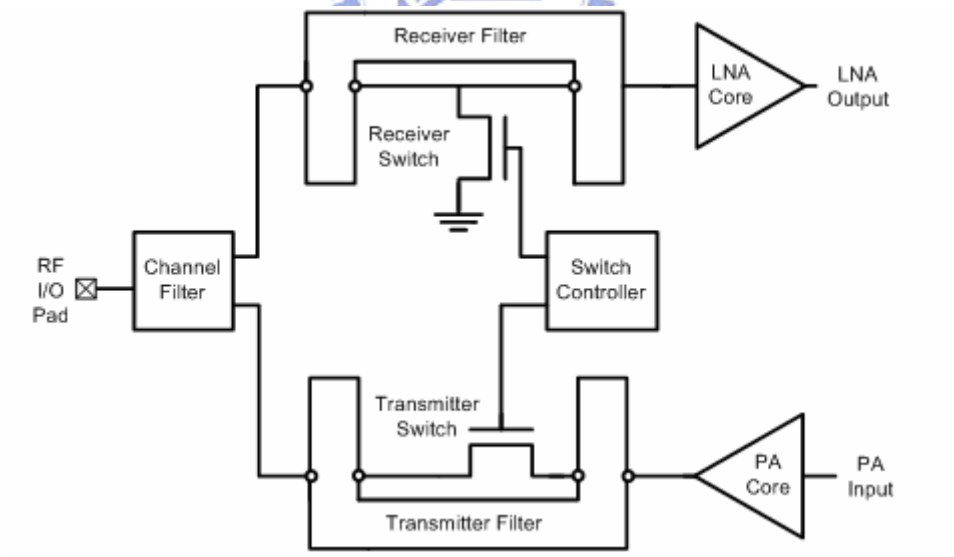
Fig. 3.7 Traditional mixed-voltage I/O interface circuit.



(a)

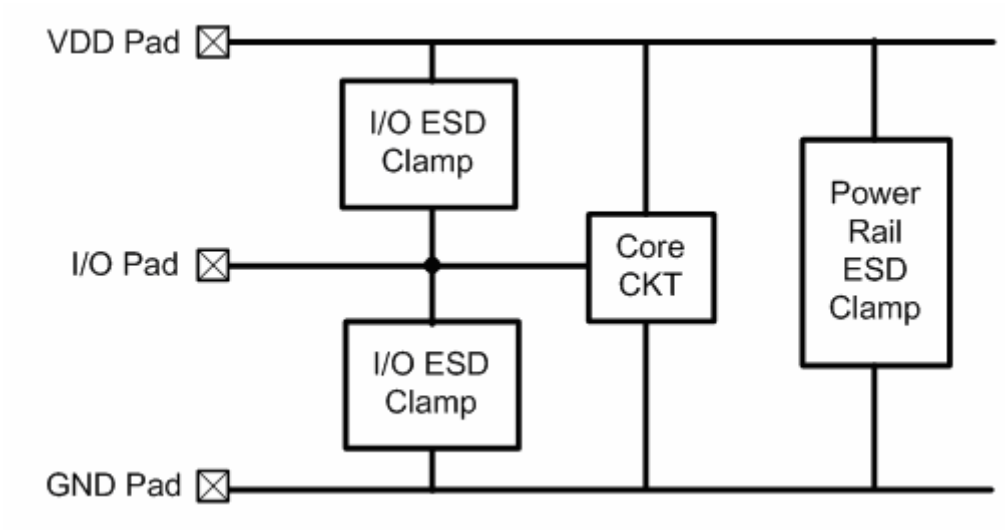


(b)

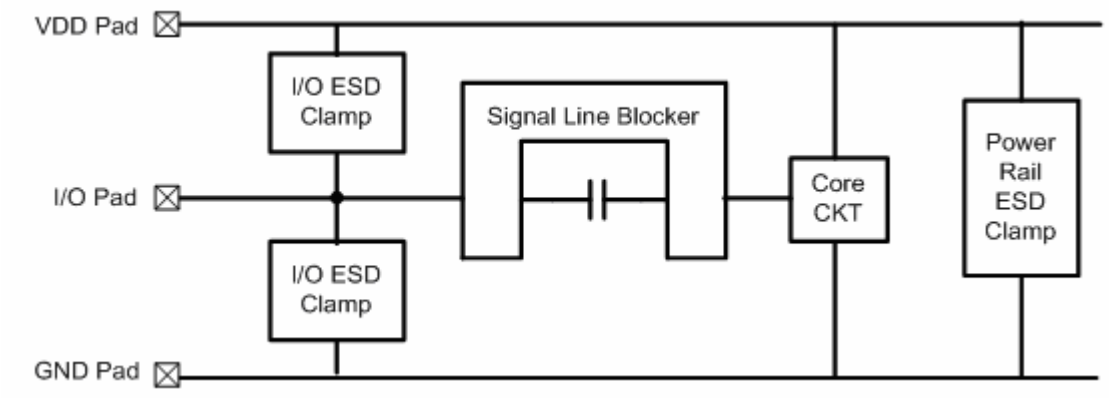


(c)

Fig. 3.8 General I/O interface circuit specifically designed for RF application: (a) low-noise amplifier (LNA) as the RF input interface, (b) power amplifier (PA) as the RF output interface, and (c) RF switch as an integrated RF I/O interface.

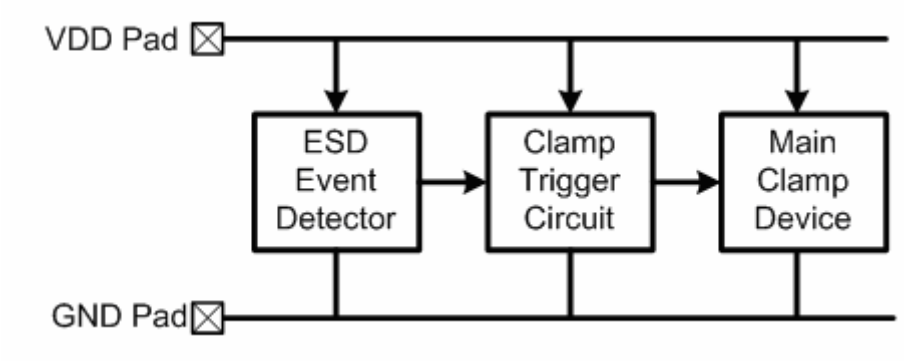


(a)

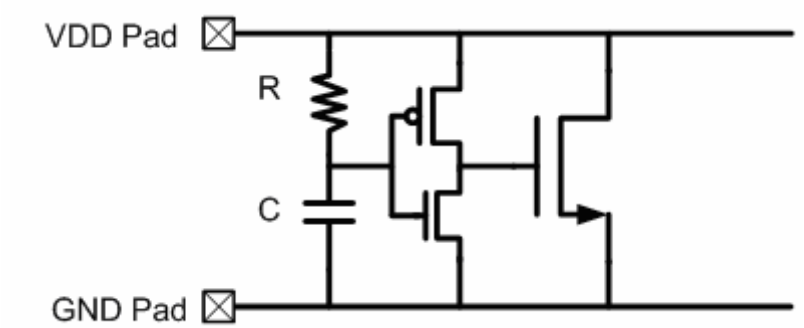


(b)

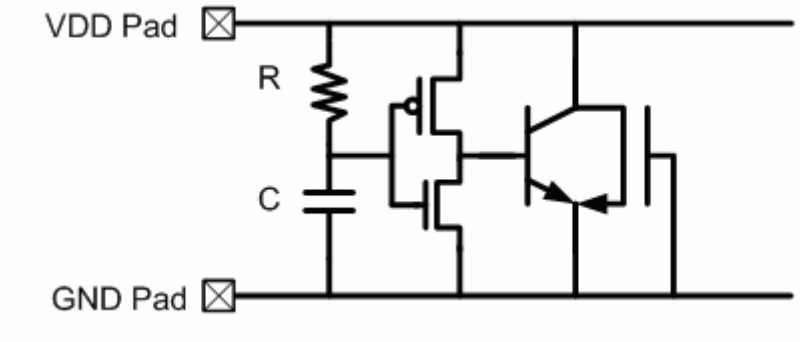
Fig. 3.9 Whole-chip ESD protection of (a) conventional architecture and (b) architecture with signal line blocker.



(a)

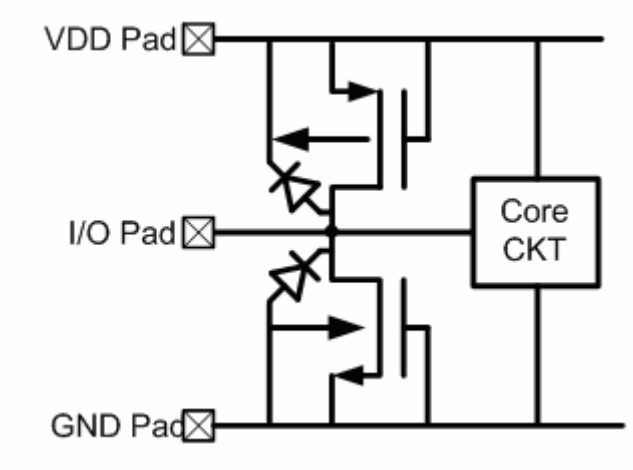


(b)

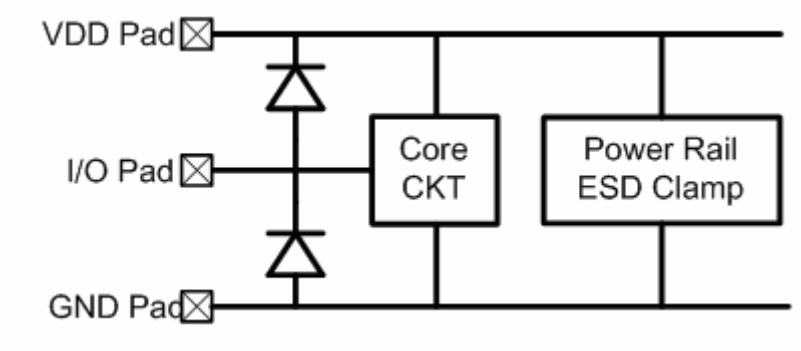


(c)

Fig. 3.10 Power rail ESD clamp with (a) typical architecture, (b) a big NMOS as the main clamp device, and (c) a parasitic bipolar transistor as the main clamp device.

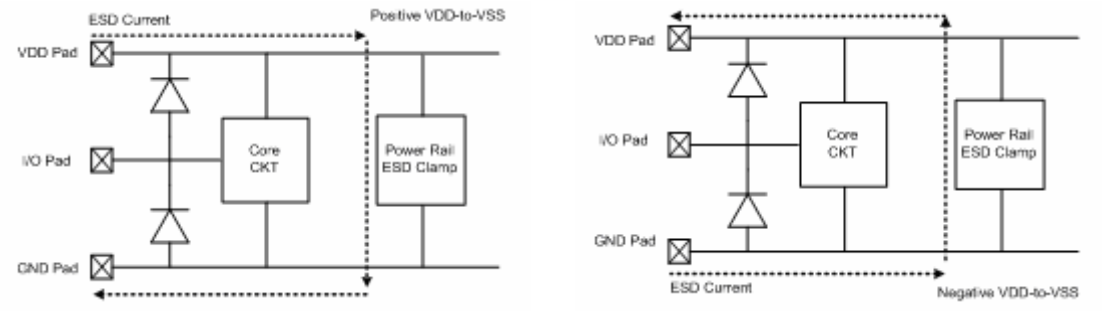


(a)



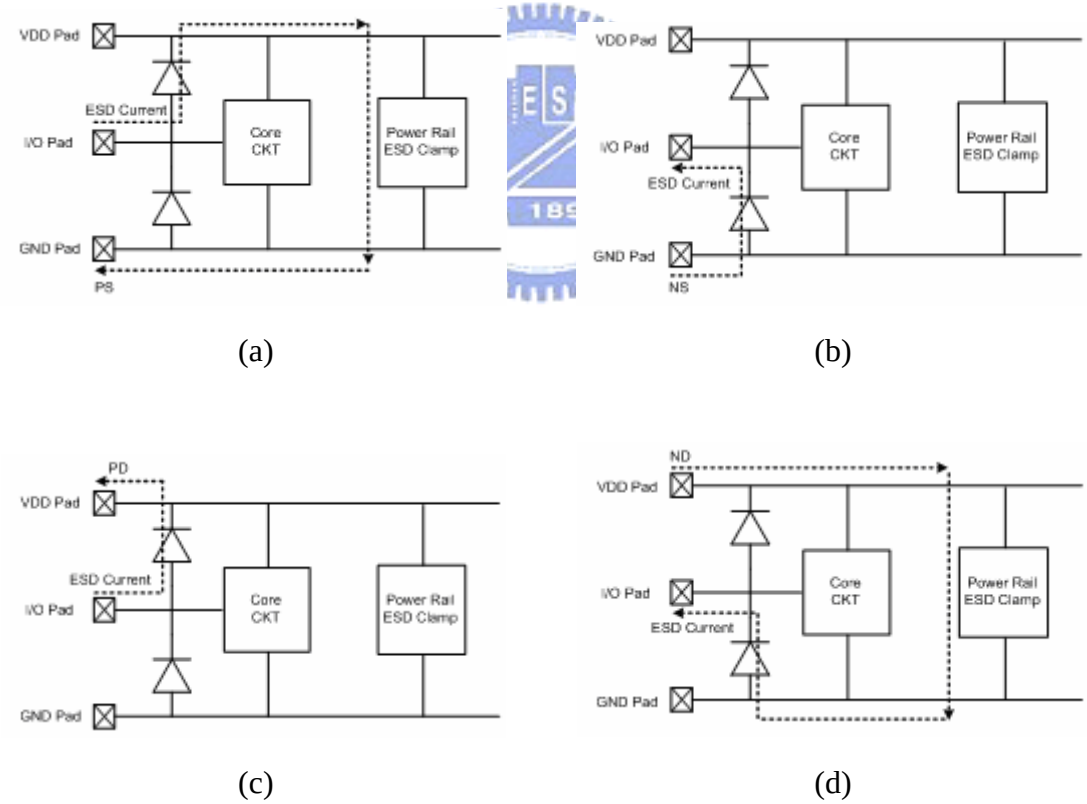
(b)

Fig. 3.11 I/O ESD clamp using (a) a pair of GGNMOS and PGPMOS, and (b) a pair of diodes within the whole-chip ESD protection architecture.



(a) (b)

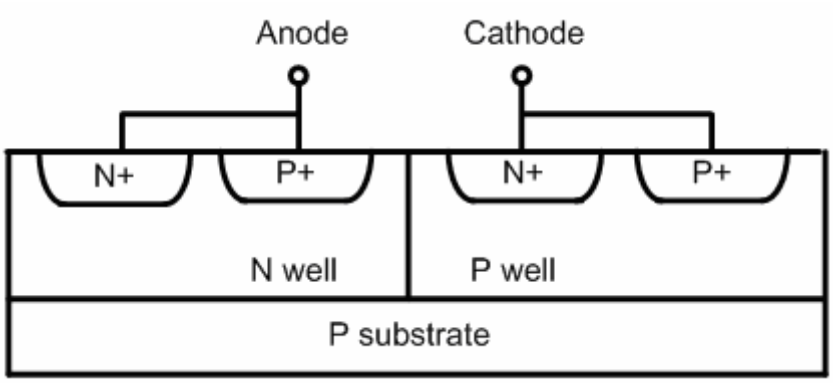
Fig. 3.12 ESD current under (a) positive, and (b) negative, VDD-to-VSS modes for the I/O ESD clamp using a pair of diodes within the whole-chip ESD protection architecture.



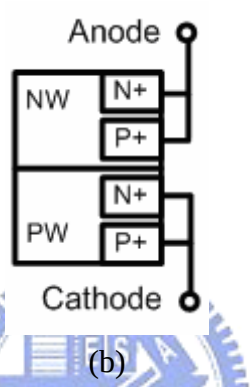
(a) (b)

(c) (d)

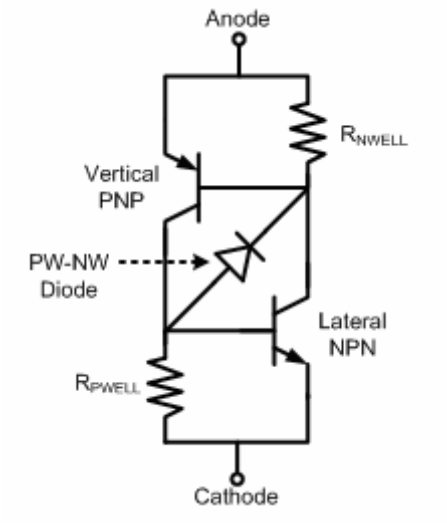
Fig. 3.13 ESD current under (a) PS-mode, (b) NS-mode, (c) PD-mode, and (d) ND-mode, for the I/O ESD clamp using a pair of diodes within the whole-chip ESD protection architecture.



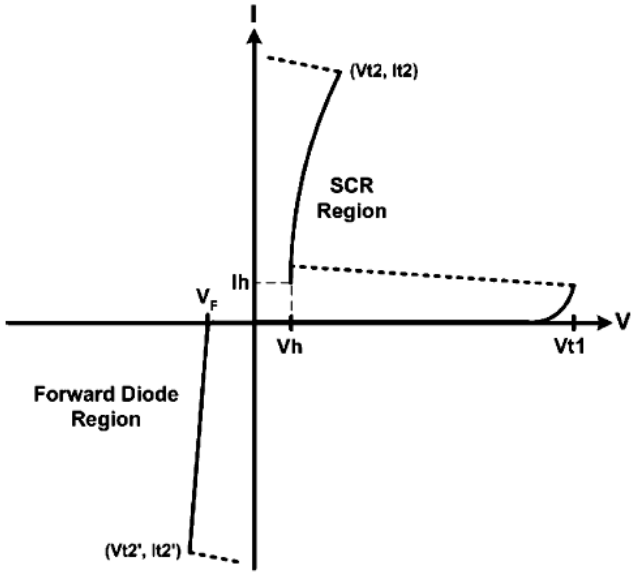
(a)



(b)

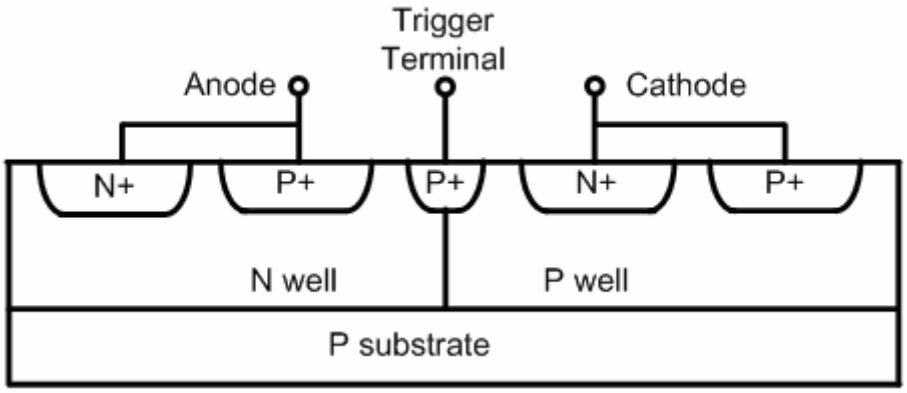


(c)

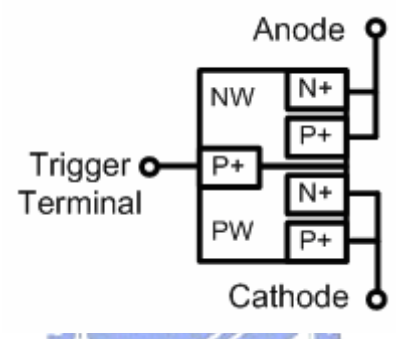


(d)

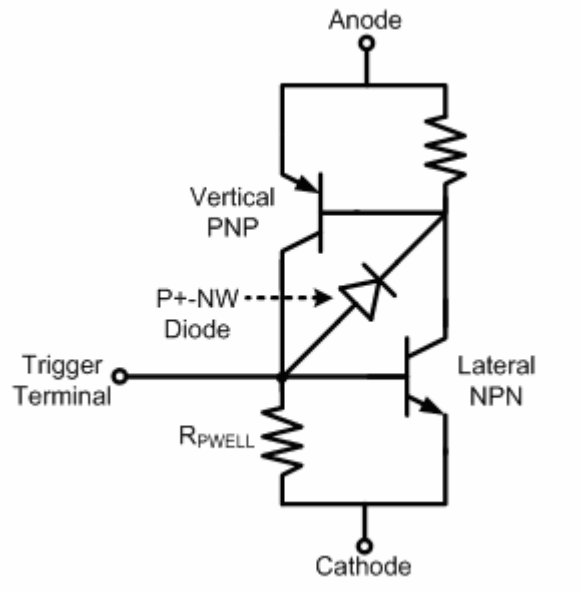
Fig. 3.14 (a) Device cross-sectional view, (b) simplified structural illustration, (c) equivalent circuit, and (d) typical I-V characteristic, of SCR device.



(a)



(b)



(c)

Fig. 3.15 (a) Device cross-sectional view, (b) simplified structural illustration, and (c) equivalent circuit, of another SCR device.

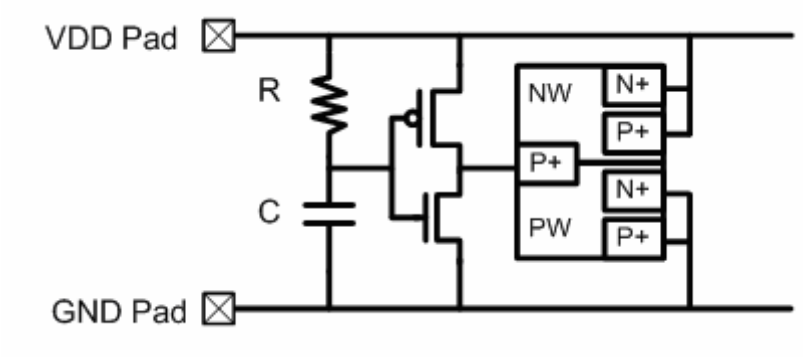


Fig. 3.16 Power rail ESD clamp using SCR device.

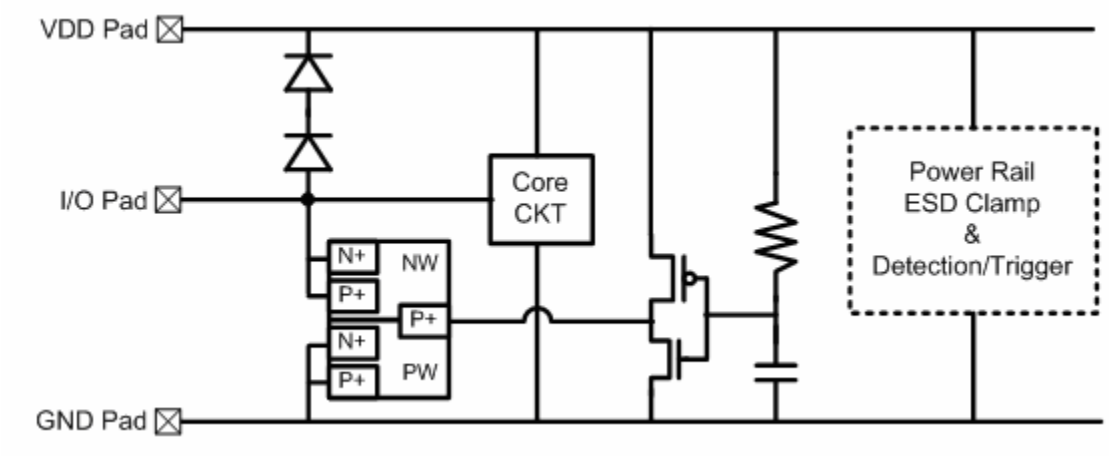
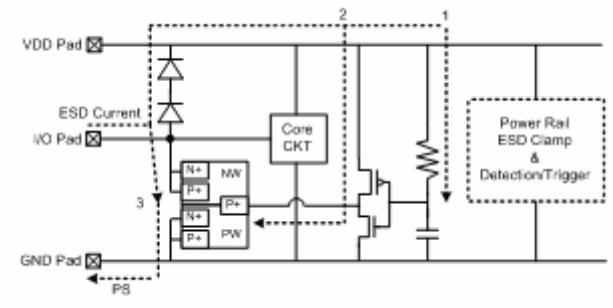
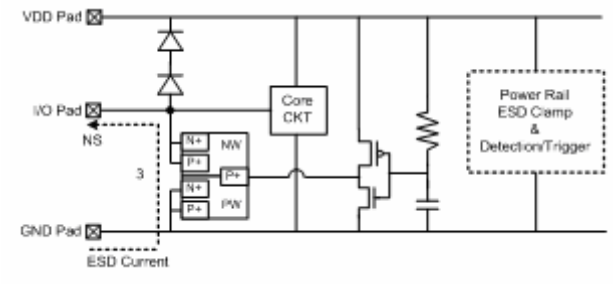


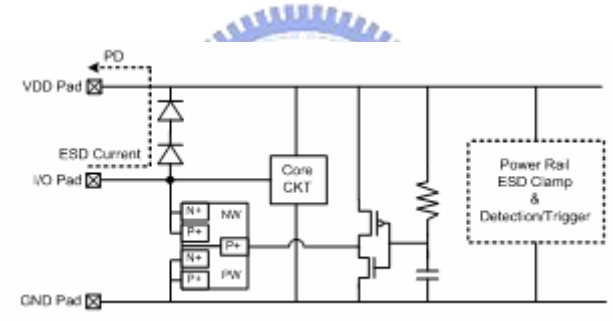
Fig. 3.17 Whole-chip ESD protection circuit with the I/O ESD clamp using SCR device.



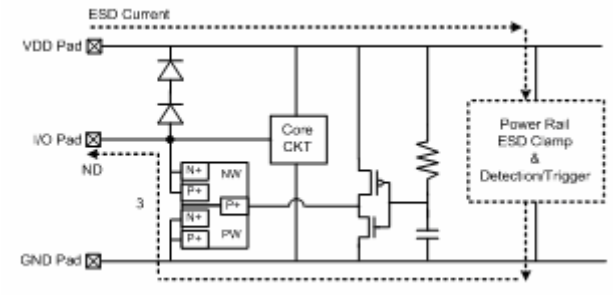
(a)



(b)

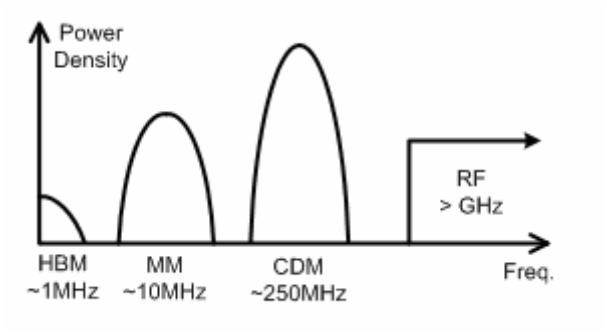


(c)

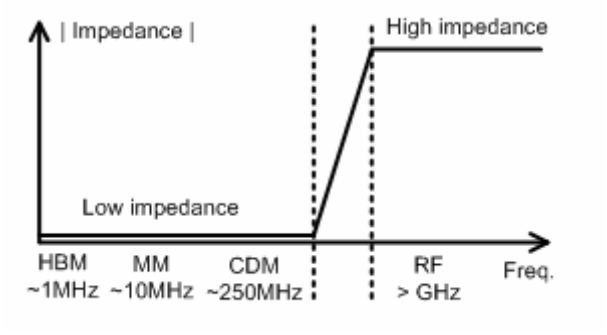


(d)

Fig. 3.18 ESD current under (a) PS-mode, (b) NS-mode, (c) PD-mode, and (d) ND-mode, for the whole-chip ESD protection circuit with the I/O ESD clamp using SCR device.

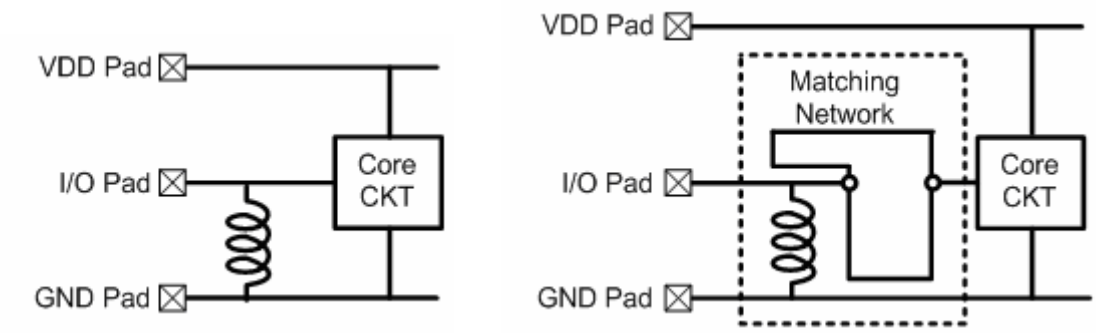


(a)



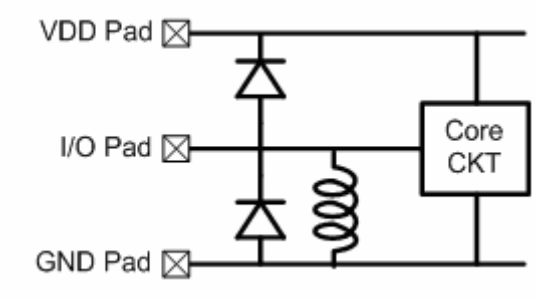
(b)

Fig. 3.19 (a) Spectral locations of ESD and RF power. (b) Clamp device characteristic in frequency viewpoint.

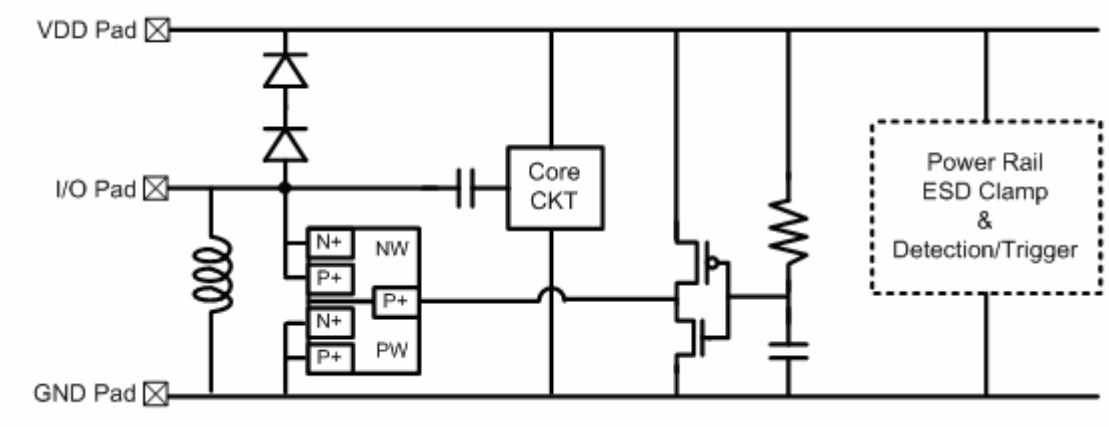


(a) (b)

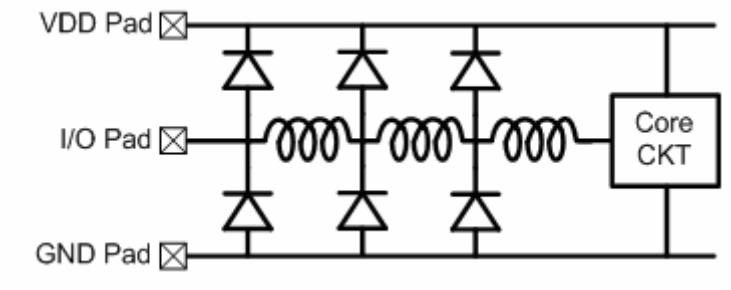
Fig. 3.20 Inductor as (a) a RF choke, and (b) part of the matching network, in potentially applicable RF circuits using inductor co-design methodology.



(a)



(b)



(c)

Fig. 3.21 (a) Parallel resonant tank composed of an inductor and a diodes, (b) parallel resonant tank composed of an inductor and a SCR, and (c) distributed ESD protection in potentially applicable RF circuits using inductor co-design methodology.

Chapter 4

Experimental Results

4.1 Narrowband Class-AB PA with an Inductive ESD Device

In this section the inductor co-design strategy and the signal line blocker concept are demonstrated. An on-chip planar inductor is designed to serve for both the PA output matching network and the output port ESD clamp. A metal-insulator-metal capacitor (MIMCAP) is designed to serve for both the PA output matching network and the signal line blocker. The protected PA is a narrowband class-AB PA designed to operate at 3-GHz and transmit a 0-dBm linear output power for demonstration. The measurement results reveal the truth that this inductor co-design strategy and the signal line blocker concept indeed provide excellent ESD robustness for the PA circuit and cause no degradation on the RF performance.

4.1.1 Design of the PA Circuit and the ESD Protection circuit

The PA circuit is illustrated in Fig. 4.1. The corresponding device parameters are organized in Table 4.1.

The active device core (M1 and M2) is in cascode topology. The cascode topology provides good voltage gain and good isolation. It also prevents drain overstressing since the voltage swing may approach 2 times the VDD. The size and bias of the coscode pair is designed to output a maximum current that satisfies the output power specification within its operational dynamic range. As a consequence, the optimal load-line resistance is decided, and the parasitic capacitances are set.

The input matching network is a simple L-section. The resistor (R_{IN}) provides the real part of the input impedance. The reactive components (C_{IN} and L_{IN}) provide suitable impedance transformation and match the PA input to 50-ohm.

The output matching network (L_D, C_{OUT}, and L_{OUT}) is a π-section. It transforms the 50-ohm external output loading to the optimal load-line resistance for the cascode pair output.

The inductor, L_{OUT}, in the output matching network also provides ESD protection capability. It serves as a low impedance discharging path for ESD power occupying the lower frequency spectrum. To achieve good ESD protection capability, the metal trace of L_{OUT} is purposefully designed to be as wide as possible. In such manner, the parasitic resistance is minimized and the discharging efficiency of this inductor can be maximized. With this series resistance concern, the inductor parameters are co-designed with the circuits to achieve its normal RF function, the output matching.

The capacitance, C_{OUT}, in the output matching network provides an additional ESD protection capability. It serves as a signal line blocker to block out the ESD current from directly penetrating into the active device core. It also acts as a capacitive voltage divider, with respect to the active device core. With C_{OUT} the active device core is not directly zapped by the ESD overstress; part of the overstress voltage potential is taken by C_{OUT}. Thus, M2 and M1 are protected. Certainly, C_{OUT} is also co-designed within the output matching network and serves for normal circuit operation.

The pre-layout simulation results are shown in Fig. 4.2, Fig, 4.3, and Fig. 4.4. Fig. 4.2 is the matching situations of the PA. Fig. 4.3 is the forward and reverse power transmission of the PA. Fig. 4.4 is the large signal PTC of the PA operating at its maximum output power frequency, 5.2-GHz. The results are organized in Table 4.2.

4.1.2 Chip Implementation

The layout of this narrowband Class-AB PA is shown in Fig. 4.5. The left-handed corner is the input GSG pads. The right-handed corner is the output GSG pads. The up-most pads are for DC bias (VG and VDD).

The post-layout simulation is illustrated in Fig. 4.6, Fig. 4.7, and Fig. 4.8. Fig. 4.6 is the matching situations of the PA. Fig. 4.7 is the forward and reverse power transmission of the PA. Fig. 4.8 is the large signal operation of the PA operating at its maximum output power frequency, 3.64-GHz. The results are organized in Table 4.2.

4.1.3 Measurement Results

The narrowband Class-AB PA is fabricated in a 130-nm mixed-signal/RF CMOS process. The fabricated chip photograph is shown in Fig. 4.9.

The setup for RF functionality measurement is as follow. An Agilent E8364B PNA is the instrument for S-parameters measurement. An Agilent E4448A spectrum analyzer and an Agilent E8257D signal generator are used to extract the power transfer characteristics of the PA. The measurement results of the PA are illustrated in Fig. 4.10, Fig. 4.11, and Fig. 4.12. Fig. 4.10 is the matching situations of the PA. Fig. 4.11 is the forward and reverse power transmission of the PA. Fig. 4.12 is the large signal PTC of the PA operating at its maximum output power frequency, 3.2-GHz. The results are organized in Table 4.2.

To compare the ESD protection capability, the PA was tested under HBM ESD zapping and MM ESD zapping. The ESD testing set-up is illustrated in Fig. 4.13. The ESD testing parameter arrangement is organized in Table 4.3. Each PA is zapped by a particular ESD testing pulse three times for complete testing; each PA is then measured to obtain its RF performance. The chip photograph of the PA which is observably damaged is illustrated in Fig. 4.14.

The S-parameters and the large signal operation data are extracted. The measurement results are organized in Fig. 4.15 to Fig.4.18.

Fig. 4.15 illustrates the S21 and S22 parameters of a set of tested PA zapped by a series of different HBM ESD level. Fig. 4.16 illustrated the large signal PTC of this set of PA (zapped by HBM ESD) operating at its maximum output power frequency, 3.2-GHz.

Fig. 4.17 illustrates the S21 and S22 parameters of a set of tested PA zapped by a series of different MM ESD level. Fig. 4.18 illustrated the large signal PTC of this set of PA (zapped by MM ESD) operating at its maximum output power frequency, 3.2-GHz.

After ESD zapping, it can be seen from the chip photographs that the chip is obviously damaged only after 800V MM test and 1kV MM test. L_{OUT} and C_{OUT} are clearly damaged. The RF functionality test also shows that the PA survives all the HBM ESD tests (up to 8kV HBM level). The PA survives up to 400V MM test, and its output terminal exhibits an open circuit after 800V MM test and 1kV MM test. In short, the output terminal which contains L_{OUT} and C_{OUT} is not severely damaged until 800V MM test. The inductor co-design strategy and the signal line blocker concept can effectively protect the PA core circuit.

L_{OUT} is damaged at the M8-M7-M6 via, as shown in Fig. 4.14. Via is one of the most fragile points in the metal interconnect. It has a relative small cross-section area and thus the resistance is large. Heat is generated when the ESD current flows through the tiny via cross-section, and finally the via is burned out and melt down. In short, the inductor is burned down and becomes an open circuit.

It is not clear, though, how the ESD current damage the MIMCAP. From the experimental data it can be seen that the output terminal appears as an open circuit after 400 MM test. The PA cannot survive an 800V MM test but does survive an 8kV

HBM test. Therefore, it is not likely that the ESD overstress exceeds the dielectric strength of the MIMCAP insulator and punch through this dielectric. A reasonable guess is that the destructive ESD current rushes toward the MIMCAP and peel off the metal layer of the MIMCAP. From Fig. 4.14 it can also be seen that the MIMCAP metal layer is indeed somehow peeled.

4.1.4 Conclusion

The experimental results of the 3-GHz 0-dBm Narrowband Class-AB PA are organized in Table 4.3 and Fig. 4.19. The ESD protection strategy using an output inductor and a MIMCAP co-designed with the output matching network provides excellent ESD protection capability but cause no degradation on the RF performance. Since the inductor and the capacitor are designed with RF performance concern from the very beginning of the circuit design, it has no negative impact on the RF circuit performance. The inductor can provide ESD robustness over 8-kV HBM ESD level and 400-V MM ESD level. Both levels far exceed the standard ESD robustness requirement.

4.2 UWB CLASS-AB DISTRIBUTED AMPLIFIER WITH LOW-C ESD DEVICES

This section demonstrates the truth that a RF PA is in urgent need of ESD protection. An ultra-wideband (UWB) class-AB distributed amplifier (DA) is designed to operate as a 3 to 10-GHz 0-dBm power amplifier and serve as the protected RF PA. The ESD protection strategy in this design utilizes the whole-chip ESD protection architecture. The power-rail ESD protection circuit is a SCR clamp as the main clamp device and a RC-inverter as the detection and trigger circuits. The I/O

ESD protection circuit utilizes an upward diode string and a SCR clamp with detection and trigger circuits. RF and ESD performance is compared between a pure PA without ESD protection circuit and a protected PA under a series of ESD testing to qualify the impact of ESD protection circuits on the RF PA performance. The RF performance of the unprotected distributed amplifier is measured to qualify the influence of ESD zapping on the circuit RF operation. The RF performance of the protected distributed amplifier is measured to qualify the ESD protection strategy in use. The layout of the SCR clamp and the upward diodes are in waffle-structured style which maximizes the peripheral within a given square area. Therefore the ESD capability is further increased; effective capacitance is reduced for a given ESD robustness. It is proved with experimental evidence that a RF PA is in urgent need of ESD protection. The ESD protection circuit certainly provides parasitic capacitance and degrades the RF PA performance; RF PA and ESD protection circuit co-design is of great importance to minimize this negative impact.

4.2.1 Design of the DA Circuit and the ESD Protection circuit

The PA circuit is illustrated in Fig. 4.20. The corresponding device parameters are organized in Table 4.4.

The active device core (M1 and M2) of each stage is in cascode topology. The cascode topology provides good voltage gain and good isolation. It also prevents drain overstressing since the voltage swing may approach 2 times the VDD. The size and bias of the coscode pair is designed to output a particular current that gives the active device core a 50-ohm for its optimal load-line resistance within its operational dynamic range. In such manner the distributed amplifier can simultaneously satisfies a 50-ohm conjugate match and optimal load-line match. The number of stages is decided according to the output power specification.

The input and output artificial line is in band-pass type. The design equation is illustrated in chapter 2. Characteristic impedance of both lines is designed to be 50-ohm. The upper and lower cut-off frequencies are set to be 10-GHz and 3-GHz, respectively.

The ESD protection circuit is shown in Fig. 4.21. The corresponding device parameters are organized in Table 4.5. It contains an upward diode string and a SCR. For PD-mode, the ESD current is discharge through the upward diode string. For the NS-mode, the ESD current is discharged through the SCR PW-NW diode. For ND-mode, the ESD current first shunted from VDD rail to GND rail through power-rail ESD clamp; then it goes through the SCR PW-NW diodes and discharged. For PS-mode, there exist two paths. One path is that partial ESD current first go through the upward diode string to the VDD rail and then activates the detection and trigger circuits. The detection and trigger circuits are then turn on the I/O SCR and discharge all the ESD current to GND. The other path is that the ESD current go through the upward diodes and then directly discharged to GND by the power-rail ESD clamp. Since the voltage swing at the PA output port can be as large as about 1 volt while outputting the required output power level, the upward diode string need two diodes for safe operation.

The diodes and SCR in the I/O ESD clamp are both in waffle-structured style. The layout sketches are illustrated in Fig. 4.22. It has been truth that the discharging capability of an ESD clamp is proportional to its peripheral (to be precise, its cross-sectional area), not to its area. Therefore, the waffle-structured layout can maximize the peripheral within a given square area. In such manner the discharging capability of a SCR within a specific layout area can be maximized. Thus, the parasitic capacitance contributed by the diodes and SCR clamp can be minimized under a given ESD robustness requirement.

Parasitic capacitance added to the output port of a RF amplifier by the ESD protection circuits certainly does degrade the circuit performance. The artificial line gives the circuit design an edge to minimize this effect. The parasitic capacitance at output port can be somehow absorbed into the artificial line and co-designed to minimize its impact on gain and bandwidth.

The pre-layout simulation results of an unprotected DA are shown in Fig. 4.23, Fig, 4.24, and Fig. 4.25. Fig. 4.23 is the matching situations of the unprotected DA. Fig. 4.24 is the forward and reverse power transmission of the unprotected DA. Fig. 4.25 is the gain and OP1dB versus frequency of the unprotected DA. The results are organized in Table 4.6.

4.2.2 Chip Implementation

The layout of this ultra-wideband Class-AB distributed amplifier is shown in Fig. 4.26. The left-handed corner is the input GSG pads. The right-handed corner is the output GSG pads. The up-most pads are for VDD bias. The up-most pads are for VDD bias. The bottom-most pads are for VG bias.

The parasitic capacitances (mainly by the SCR and diodes) contributed by the ESD protection circuit are extracted by a Layout Parasitic Extraction (LPE) CAD tool. Then the extracted capacitances can be incorporated to do the post-layout simulation, and the effect of the ESD protection circuit on the DA can be obtained.

The post-layout simulation of the unprotected DA is illustrated in Fig. 4.27, Fig. 4.28, and Fig. 4.29. Fig. 4.27 is the matching situations of the DA. Fig. 4.28 is the forward and reverse power transmission of the DA. Fig. 4.29 is the gain and OP1dB versus frequency of the DA. The post-layout simulation of the protected DA is illustrated in Fig. 4.30, Fig. 4.31, and Fig. 4.32. Fig. 4.31 is the matching situations of the DA. Fig. 4.32 is the forward and reverse power transmission of the DA. Fig. 4.33

is the gain and OP1dB versus frequency of the DA. The results are organized in Table 4.6.

4.2.3 Measurement Results

The ultra-wideband Class-AB distributed amplifier is fabricated in a 130-nm mixed-signal/RF CMOS process. The fabricated chip photograph is shown in Fig. 4.33. The DA at the left hand side is the protected DA; the DA at the right hand side is the unprotected DA.

The setup for RF functionality measurement is as follow. An Agilent E8364B PNA is the instrument for S-parameters measurement. An Agilent E4448A spectrum analyzer and an Agilent E8257D signal generator are used to extract the power transfer characteristics of the PA. The measurement results of the unprotected DA are illustrated in Fig. 4.34, Fig. 4.35, and Fig. 4.36. Fig. 4.34 is the matching situations of the DA. Fig. 4.35 is the forward and reverse power transmission of the DA. Fig. 4.36 is the gain and OP1dB versus frequency of the DA. The measurement results of the protected DA are illustrated in Fig. 4.37, Fig. 4.38, and Fig. 4.39. Fig. 4.37 is the matching situations of the DA. Fig. 4.38 is the forward and reverse power transmission of the DA. Fig. 4.39 is the gain and OP1dB versus frequency of the DA. The results are organized in Table 4.6.

To compare the ESD protection capability, the PA was tested under HBM ESD zapping and MM ESD zapping. The ESD testing set-up is illustrated in Fig. 4.40. The ESD testing parameter arrangement is organized in Table 4.7. Each PA is zapped by a particular ESD testing pulse three times for complete testing; each PA is then measured to obtain its RF performance. The chip photograph of the PA which is observably damaged is illustrated in Fig. 4.41.

The S-parameters and the large signal operation data are extracted. The

measurement results are organized in Fig. 4.42 to Fig.4.49.

Fig. 4.42 illustrates the S21 and S22 parameters of a set of unprotected DA zapped by a series of different HBM ESD levels. Fig. 4.43 illustrated the gain and OP1dB versus frequency of the unprotected PA (zapped by HBM ESD).

Fig. 4.44 illustrates the S21 and S22 parameters of a set of protected DA zapped by a series of different HBM ESD levels. Fig. 4.45 illustrated the gain and OP1dB versus frequency of the protected PA (zapped by HBM ESD).

Fig. 4.46 illustrates the S21 and S22 parameters of a set of unprotected DA zapped by a series of different MM ESD levels. Fig. 4.47 illustrated the OP1dB and gain versus frequency of the unprotected DA (zapped by MM ESD).

Fig. 4.48 illustrates the S21 and S22 parameters of a set of protected DA zapped by a series of different MM ESD levels. Fig. 4.49 illustrated t the OP1dB and gain versus frequency of the protected DA (zapped by MM ESD).

For the DAs without ESD protection circuit, after HBM ESD zapping, it can be seen from the chip photographs that the chip is obviously damaged after 4kV HBM test and 8kV HBM test. After MM ESD zapping, it can be seen from the chip photographs that the chip is obviously damaged after 400V MM test and 800V MM test. On the other hand, the protected DA exhibits no observable damage after up to 8kV HBM ESD test and 800V ESD test.

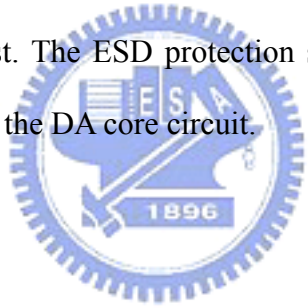
For the unprotected DA, L_{OUT} is clearly damaged, and the output terminal of the DA exhibits an open circuit. Further, the RF functionality test also shows that the unprotected PA begins to be degraded ever since it is zapped by ESD. The ESD damaging mechanism can be understood as follow. The ESD current flushes into the output terminal and rushes toward L_{OUT}. It passes through L_{OUT} and bumps into C_{OUT}. C_{OUT} is a robust MIMCAP; ESD current turns back as though it bumps into a great thick wall. The ESD current then is reflected and passes backward through L_{OUT} again,

vanishing in the external world. Therefore, L_{OUT} is stricken twice per ESD zapping and its metal trace and M8-M7-M6 via are damaged consequently severer. The ESD current burns this via twice per zapping and finally melt out L_{OUT}.

In short, the unprotected output terminal cannot survive any single the ESD tests. An RF PA is in urgent need of ESD protection.

For the DAs with ESD protection circuit, after HBM and MM ESD zapping, it can be seen from the chip photographs that the chip is not obviously damaged after any ESD test. Further, the RF functionality test shows that the protected DA performance is not influenced by any ESD zapping. It can survive any ESD tests (up to 8kV HBM and 800V MM) without degradation.

In short, the protected output terminal protected is not severely damaged up to 8kB HBM and 800V MM test. The ESD protection strategy using SCR and trigger circuits can effectively protect the DA core circuit.



4.2.4 Conclusion

The experimental results of the 3-to-10-GHz 0-dBm ultra-wideband Class-AB distributed amplifier are organized in Table 4.7, Fig. 4.50, and Fig. 4.51. It is proved with experimental evidence that a RF PA is in urgent need of ESD protection. The performance of a RF PA is severely degraded ever since the PA is zapped by an ESD current. The ESD protection strategy using an upward diode string and a SCR clamp within the whole-chip ESD protection architecture provides excellent ESD protection capability. Any parasitic capacitance contributed by the capacitive ESD protection circuits certainly does degrade the protected RF PA; waffle-structured SCR and diodes are utilized to provide the best ESD protection capability within minimum layout area to reduce the negative impact. The protection strategy can provide ESD robustness over 8-kV HBM ESD level and 800-V MM ESD level. Both levels far

exceed the standard ESD robustness requirement.

Table 4.1 Device parameters of the 3-GHz 0-dBm narrowband class-AB PA.

1.2V triple-well RF NMOS						
	Channel length	Finger width	Number of fingers	Multiplier		
M1	120nm	7.2μm	16	13		
M2	120nm	7.2μm	16	13		
Circular planar RF inductor						
	Outer diameter	Trace width	Trace spacing	Number of turns	Multiplier	Nominal value
L_D	145μm	10μm	2.52μm	2.5	3	0.297 nH
L_{OUT}	125μm	10μm	2.52μm	2.5	2	0.332 nH
L_{IN}	100μm	4.7μm	2.52μm	2.5	2	0.373 nH
Planar RF MIM capacitor						
	Width	Length	Multiplier	Nominal value		
C_{OUT}	36μm	36μm	2	2.624 pF		
C_{IN}	46μm	46μm	2	4.274 pF		
High-resistance poly resistor						
	Width	Length	Multiplier	Nominal value		
R_{IN}	2μm	5.08μm	20	118.2 ohm		
Pad						
Pad	Width	Length	Index	Parasitic capacitance		
RF Input/output	74.2μm	80.8μm	4	89.206fF		

Table 4.2 Summary of the RF performance of the 3-GHz 0-dBm narrowband class-AB PA.

	Specification	Pre-Layout Simulation	Post-layout Simulation	Measurement Results
Operation Frequency	3 GHz	5.2 GHz	3.8GHz	3.2GHz
S21	-	17.6 dB	13.8 dB	20.387 dB
S22	-	-0.59 dB	-4.73 dB	-24.047 dB
Linear Gain	-	17.4 dB	11.32 dB	16.53 dB
OP1dB	0 dBm	10.3 dBm	7 dBm	-0.5 dBm

Table 4.3 Summary of the RF performance of the 3-GHz 0-dBm narrowband class-AB PA after ESD testing zapping.

Testing conditions	S21 (dB)	S22 (dB)	Gain (dB)	OP1dB (dBm)
Fresh	20.387	-24.047	16.53	-0.5
HBM 1kV x3	20.401	-22.253	18.14	-2.1
HBM 4kV x3	20.357	-13.721	16.87	-1.5
HBM 8kV x3	19.935	-19.037	18.65	-2.1
MM 100V x3	20.102	-16.174	17.09	-1.9
MM 200V x3	19.898	-18.349	19.05	-2.8
MM 400V x3	19.526	-28.566	17.53	-1
MM 800V x3	< -28	Open	< -28.05	< -35.87
MM 1kV x3	< -12	Open	< -41.65	< -16.91

Table 4.4 Device parameters of the 3 to 10-GHz 0-dBm UWB class-AB distributed amplifier.

1.2V triple-well RF NMOS				
	Channel length	Finger width	Number of fingers	Multiplier
M1	120nm	2μm	16	6
M2	120nm	2μm	16	6

Circular planar RF inductor					
	Outer diameter	Trace width	Trace spacing	Number of turns	Nominal value
L_1	150μm	4.9μm	1.65μm	2.5	1.5015nH
1/2 L_1	95μm	4.6μm	1.51μm	2.5	0.75075nH
L	150μm	4.3μm	1.58μm	3.5	2.567nH

Planar RF MIM capacitor				
	Width	Length	Multiplier	Nominal value
C	14.15μm	14.15μm	9	2.054pF
1/2 C	13.35μm	13.35μm	5	1.027pF
CpG1	11μm	10.4μm	1	136.5 fF
CpG2	14.1μm	13.5μm	1	327.2 fF
CpG3	13.5μm	13.45μm	1	208.7 fF
CpD1	15.3μm	13μm	1	225.9 fF
CpD2	16.6μm	16.49μm	1	306.6 fF
CpD3	16.3μm	16.3μm	1	298.1 fF

High-resistance poly resistor				
	Width	Length	Multiplier	Nominal value
Rt	1.9μm	5μm	49	50ohm

Pad				
	Width	Length	Index	Parasitic capacitance
RF Input/output	74.2μm	80.8μm	4	89.206fF

Table4.5 Device parameters of the ESD protection circuit of the 3-to-10GHz 0-dBm ultra-wideband class-AB distributed amplifier.

Waffle-structured SCR (NW-PW size)			
	Unit cell width	Unit cell length	Array size
Output clamp	8.3μm	8.3μm	3 x 3
Power-rail clamp	8.3μm	8.3μm	4 x 4
Waffle-structured diodes (P+-NW size)			
	Unit cell width	Unit cell length	Array size
Output diodes	3.3μm	3.3μm	2 x 2
Detection and trigger circuit: RC-inv			
R		Nominal value	
N-well resistor		108.029k ohm	
C	Channel length	Total width	
3.3V thick oxide NMOS	3μm	480μm	
PMOS	Channel length	Total width	
1.2V PMOS	0.18μm	150μm	
NMOS	Channel length	Total width	
1.2V NMOS	0.18μm	20μm	

Table 4.6 Summary of the RF performance of the 3-GHz 0-dBm Narrowband class-AB PA before ESD testing.

		Bandwidth	S21	S22	Gain	OP1dB
Specification		3 to 10-GHz	-	-	-	0-dBm
Pre-Layout Simulation	W/O ESD	1.9 to 10.9-GHz	13.1~15.5 dB	<-15.2 dB	13.9 dB	6.3 dBm
Post-Layout Simulation	WO ESD	1.9 to 10.4-GHz	11.8~14.4 dB	<-17.1 dB	13.2 dB	5.6 dBm
	With ESD	1.94 to 10-GHz	11.9~13.7 dB	<-6.4 dB	12.4 dB	5.8 dBm
Measurement Results	W/O ESD	1.85 to 9.7-GHz	6.4~16 dB	< -2.2	12.4 dB	4.9 dBm
	With ESD	1.7 to 8.9-GHz	8.2~15.2 dB	<-3.2 dB	10.7 dB	3.3 dBm

Table 4.7 Summary of the RF performance of the 3-to-10GHz 0-dBm ultra-wideband class-AB distributed amplifier after ESD zapping.

		Bandwidth	S21	Gain	OP1dB
Fresh	W/O ESD	7.8 GHz	13.0 dB	12.4 dB	3.4 dBm
	With ESD	7.3 GHz	9.5 dB	9.8 dB	0.7 dBm
HBM 1kV x3	W/O ESD	7.7 GHz	9.9 dB	8.9 dB	1.2 dBm
	With ESD	7.4 GHz	9.3 dB	9.3 dB	1.1 dBm
HBM 2kV x3	W/O ESD	8.2 GHz	1.3 dB	-0.4 dB	-7.5 dBm
	With ESD	7.3 GHz	9.3 dB	9.2 dB	0.9 dBm
HBM 4kV x3	W/O ESD	0	-55.3 dB	-51.8 dB	-55.8 dBm
	With ESD	7.4 GHz	8.7 dB	8.5 dB	0.8 dBm
HBM 8kV x3	W/O ESD	0	-50.4 dB	-55.3 dB	-59.1 dBm
	With ESD	7.3 GHz	9.5 dB	9.5 dB	1.0 dBm
MM 100V x3	W/O ESD	7.6 GHz	7.5 dB	6.4 dB	-1.6 dBm
	With ESD	7.6 GHz	9.4 dB	9.5 dB	1.0 dBm
MM 200V x4	W/O ESD	7.4 GHz	2.2 dB	1.2 dB	-7.1 dBm
	With ESD	7.3 GHz	9.6 dB	9.6 dB	1.1 dBm
MM 400V x3	W/O ESD	0	-56.9 dB	-52.2 dB	-56.3 dBm
	With ESD	7.4 GHz	9.6 dB	9.0 dB	-0.7 dBm
MM 800V x4	W/O ESD	0	-59.0 dB	-55.6 dB	-60.0 dBm
	With ESD	7.4 GHz	7.6 dB	8.2 dB	-0.4 dBm

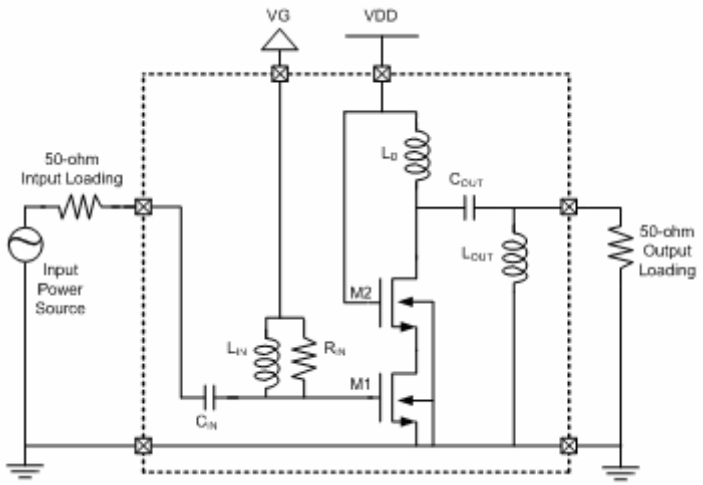
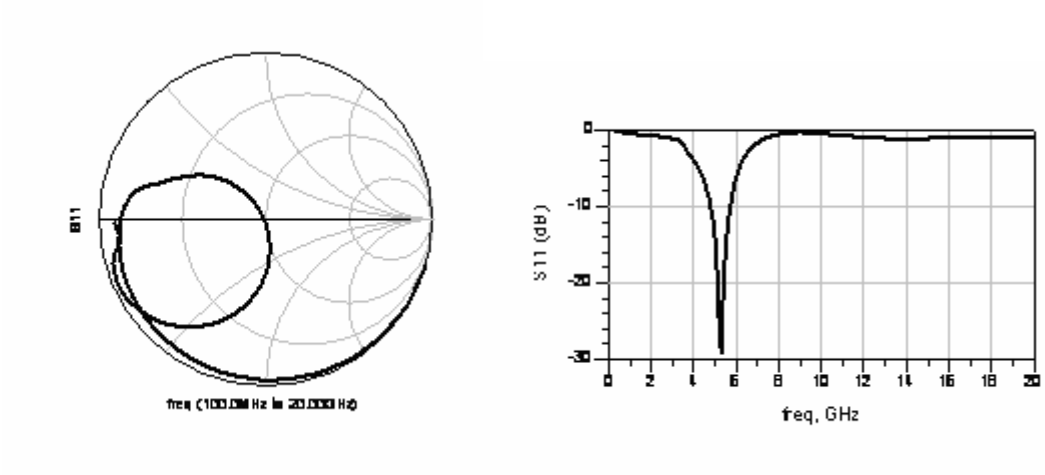
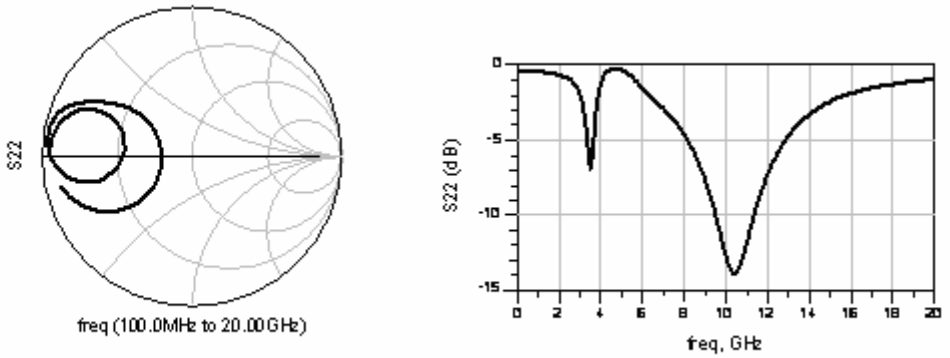


Fig. 4.1 Circuit schematic of the 3-GHz 0-dBm narrowband class-AB PA.

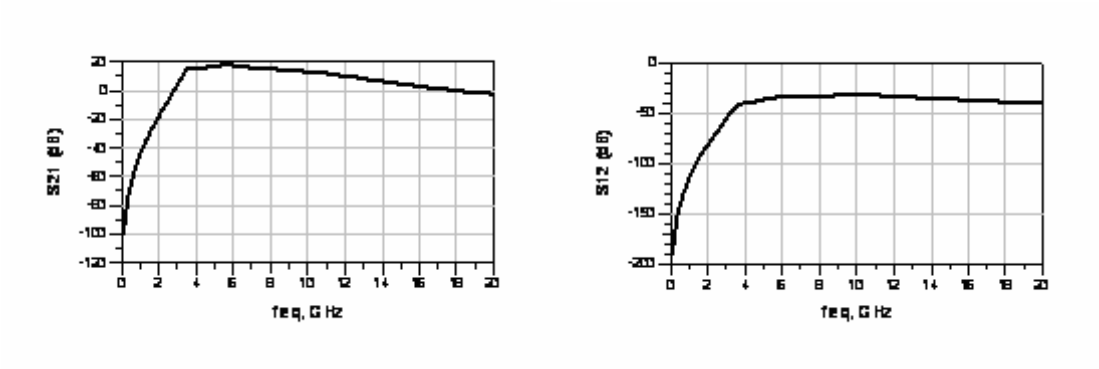


(a)



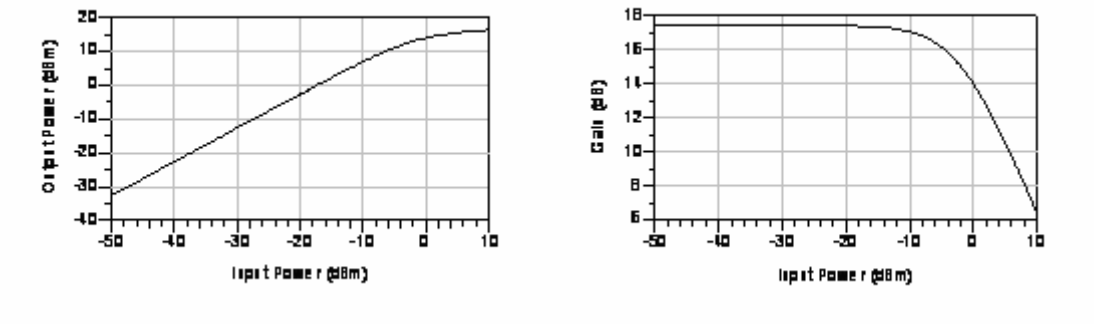
(b)

Fig. 4.2 Pre-layout simulation results: matching situations of (a) S11, and (b) S22, of the PA.



(a) (b)

Fig. 4.3 Pre-layout simulation results: power transmission of (a) S21, and (b) S12, of the PA.



(a) (b)

Fig. 4.4 Pre-layout simulation results: large signal PTC at 5.2-GHz of (a) output power versus input power, and (b) gain versus input power, of the PA.

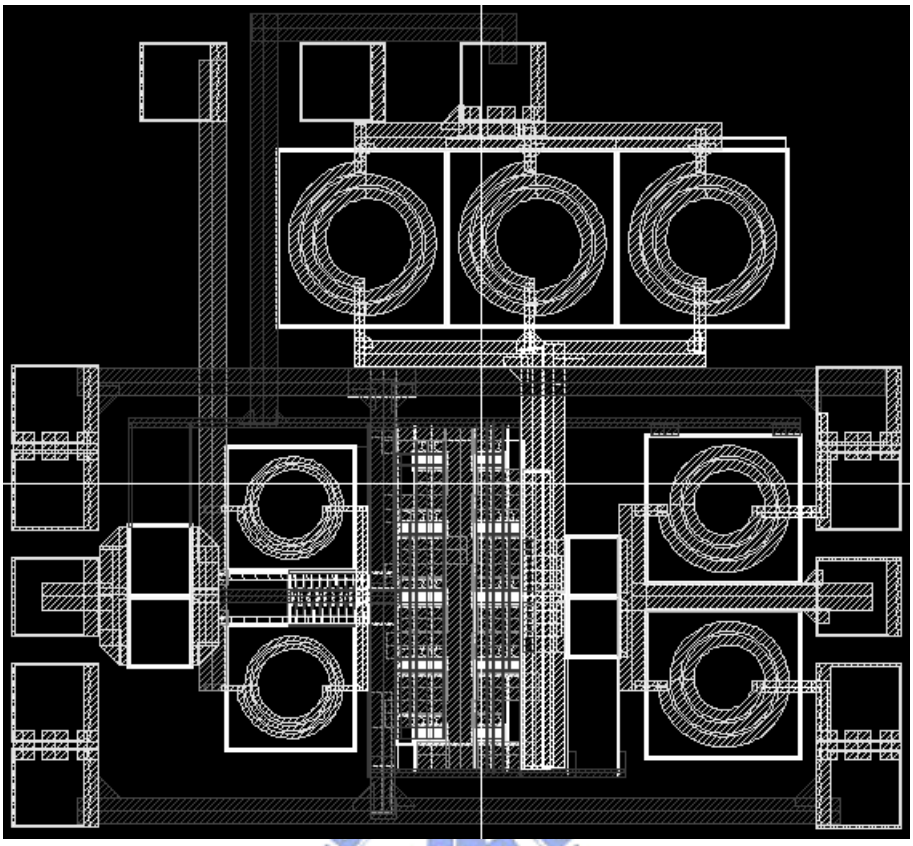
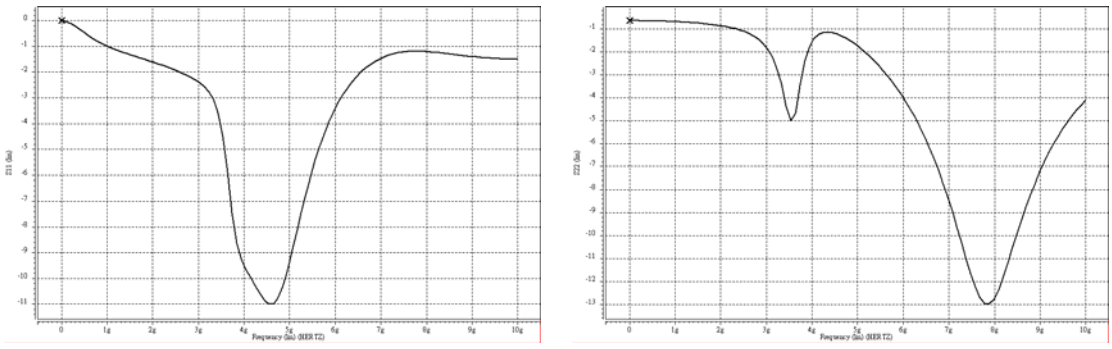
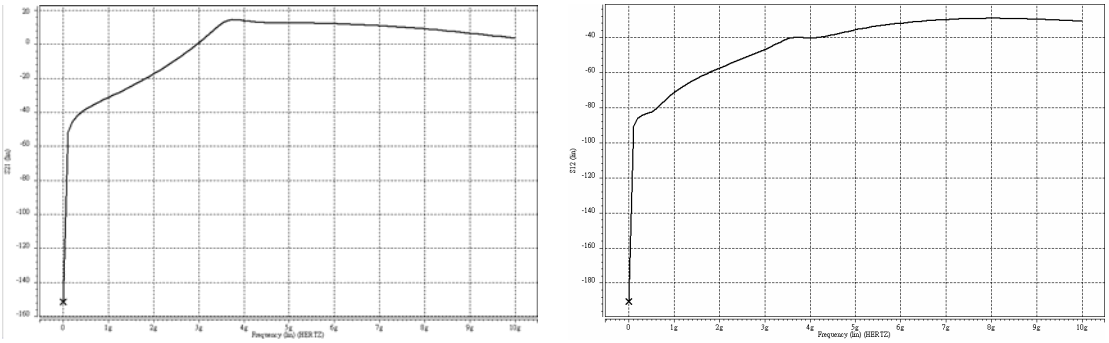


Fig. 4.5 Layout top view of the 3-GHz 0-dBm narrowband class-AB PA.



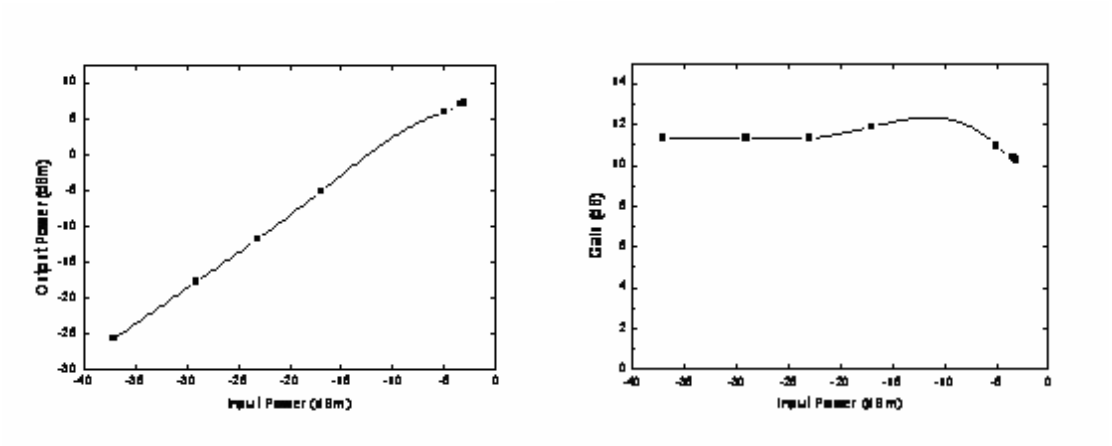
(a) (b)

Fig. 4.6 Post-layout simulation results: matching situations of (a) S11, and (b) S22, of the PA.



(a) (b)

Fig. 4.7 Post-layout simulation results: power transmission of (a) S21, and (b) S12, of the PA.



(a) (b)

Fig. 4.8 Post-layout simulation results: large signal PTC at 3.64-GHz of (a) output power versus input power, and (b) gain versus input power, of the PA.

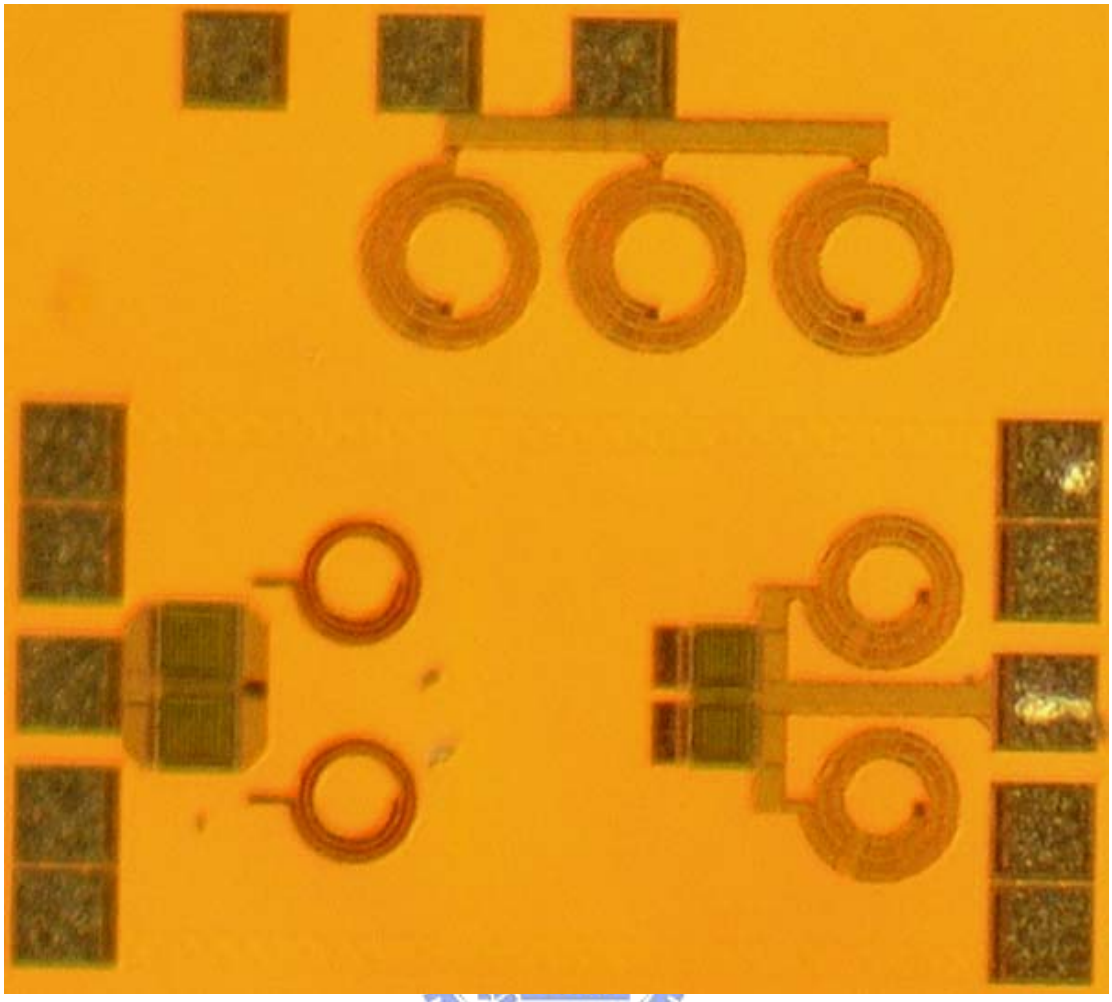
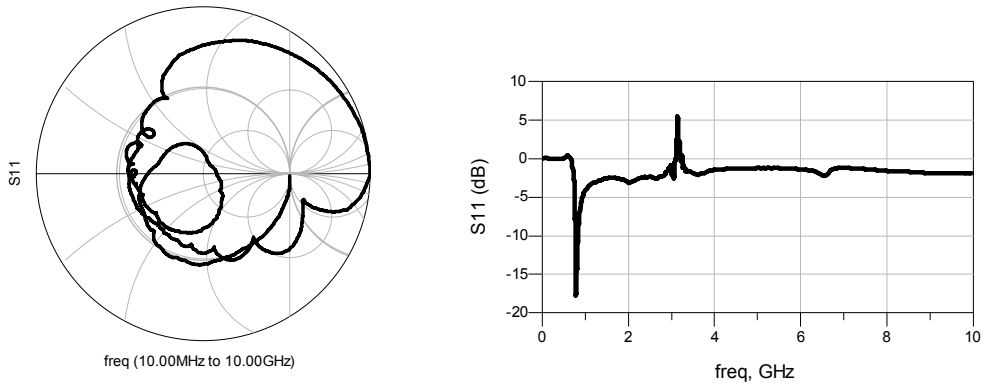
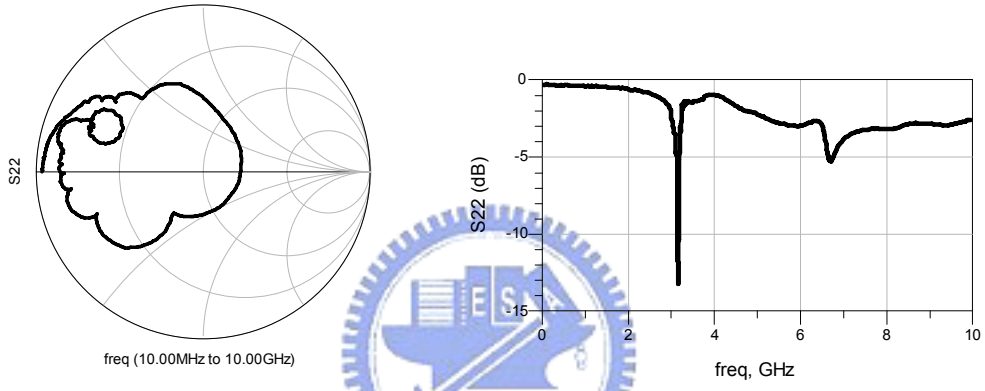


Fig. 4.9　Die photo of the 3-GHz 0-dBm narrowband class-AB PA.

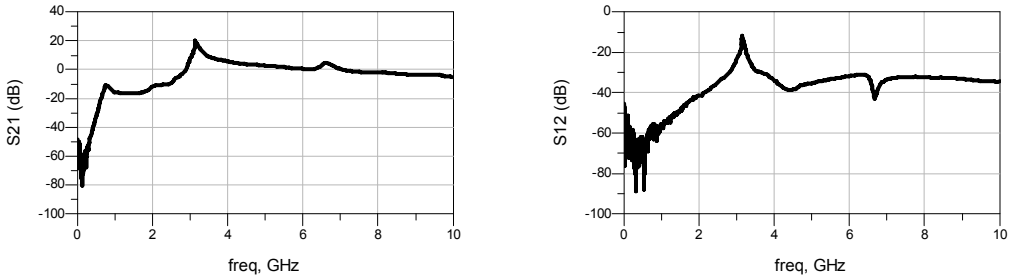


(a)



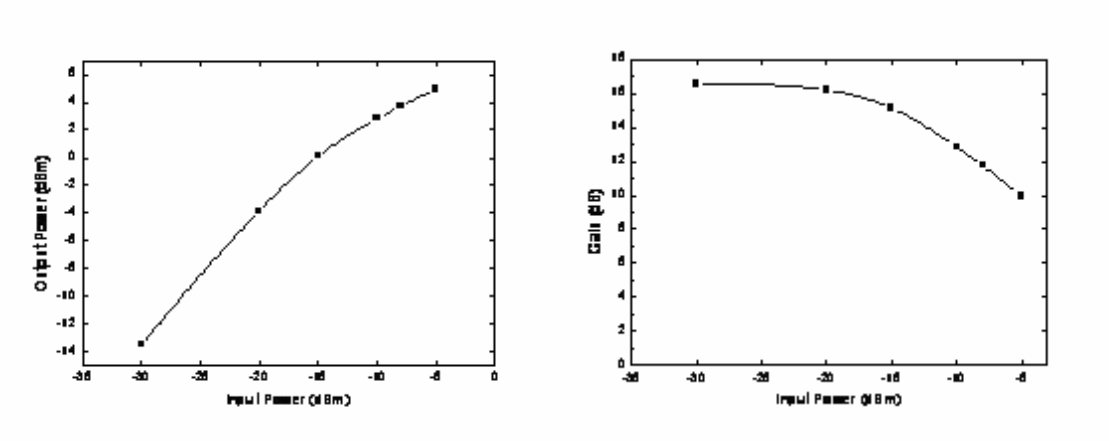
(b)

Fig. 4.10 Measurement results: matching situations of (a) S11, and (b) S22, of the PA.



(a) (b)

Fig. 4.11 Measurement results: power transmission of (a) S21, and (b) S12, of the PA.



(a) (b)

Fig. 4.12 Measurement results: large signal PTC at 3.2-GHz of (a) output power versus input power, and (b) gain versus input power, of the PA.

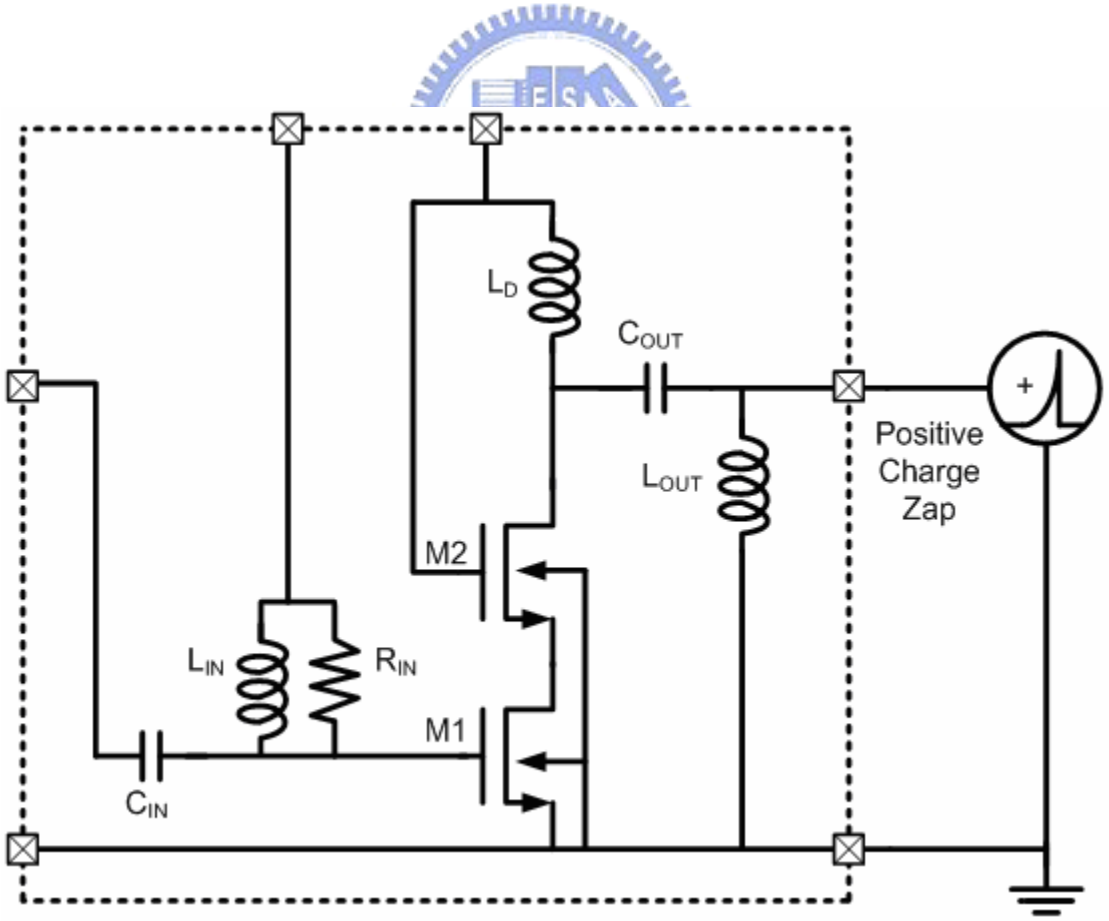
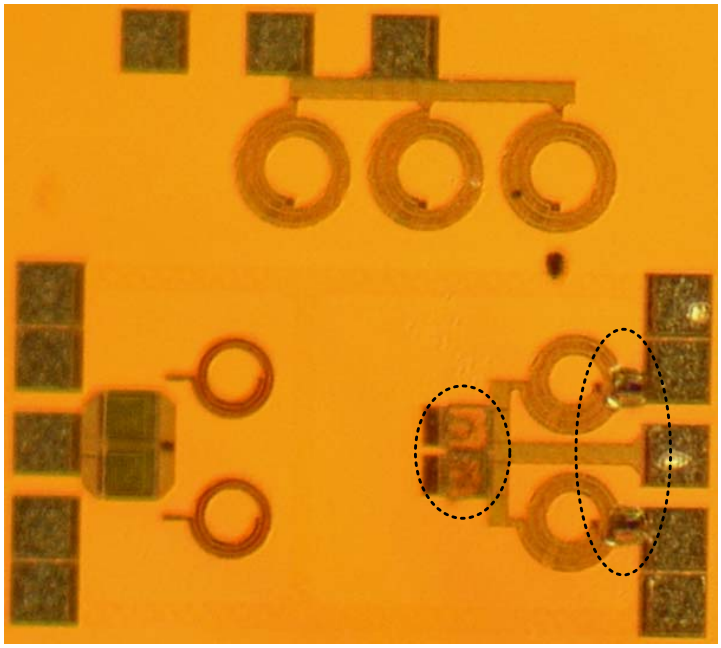
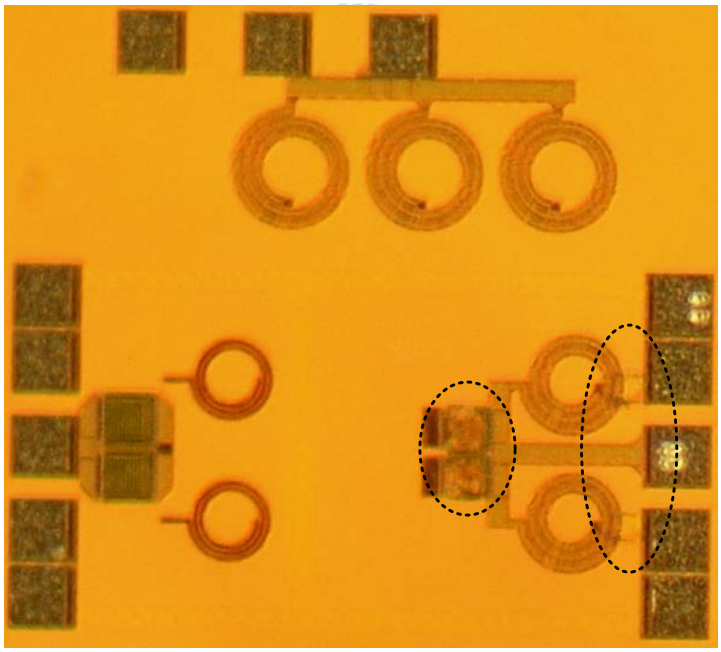


Fig. 4.13 ESD testing set-up for the 3-GHz 0-dBm narrowband class-AB PA.

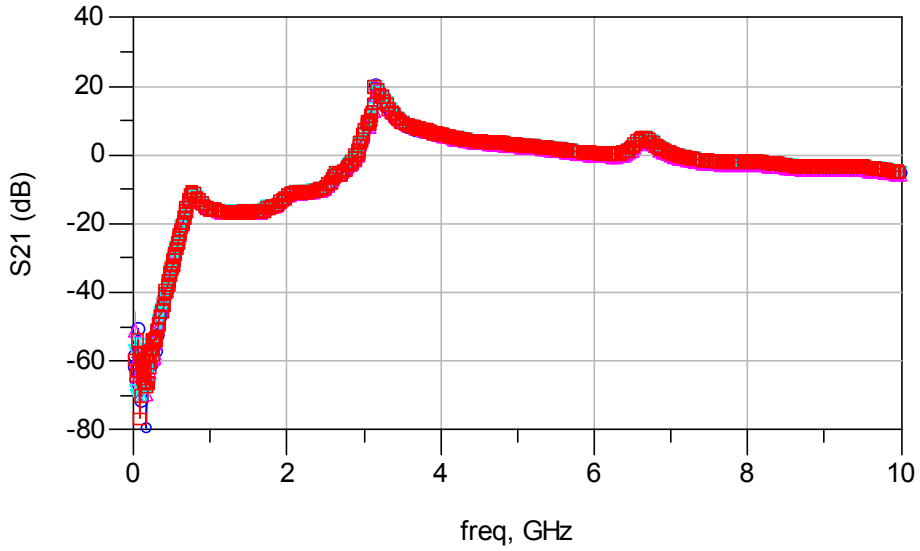


(a)

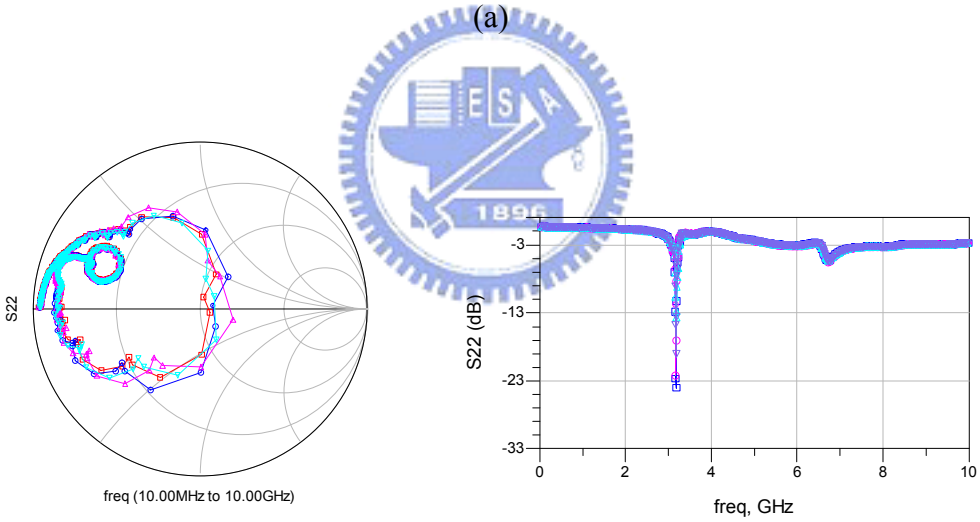


(b)

Fig. 4.14 Die photo of the 3-GHz 0-dBm narrowband class-AB PA after three times MM ESD zapping of (a) 800V and (b) 1kV.



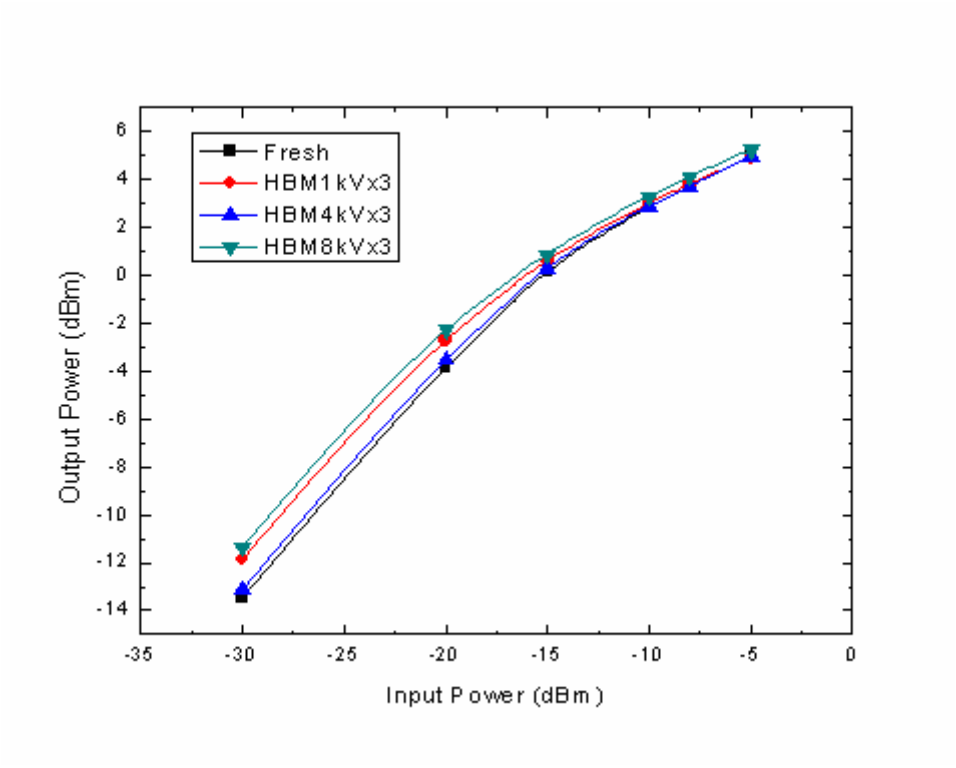
(a)



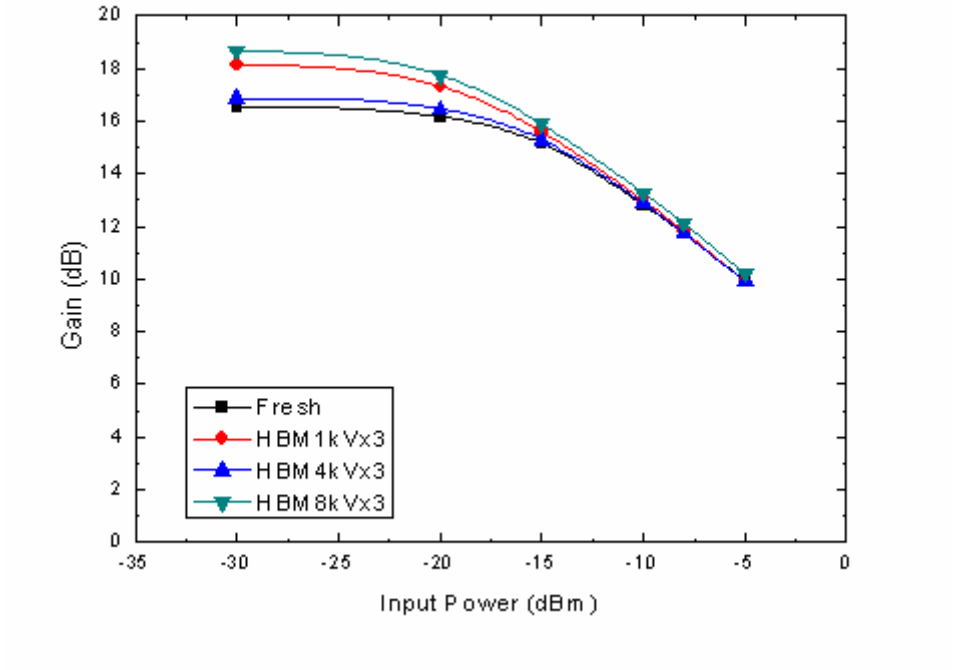
(b)

Fig. 4.15 Measurement results of (a) S21, and (b) S12, of the PA after three times HBM ESD zapping.

Fresh	■
HBM 1kV x3	●
HBM 4kV x3	▲
HBM 8kV x3	▼

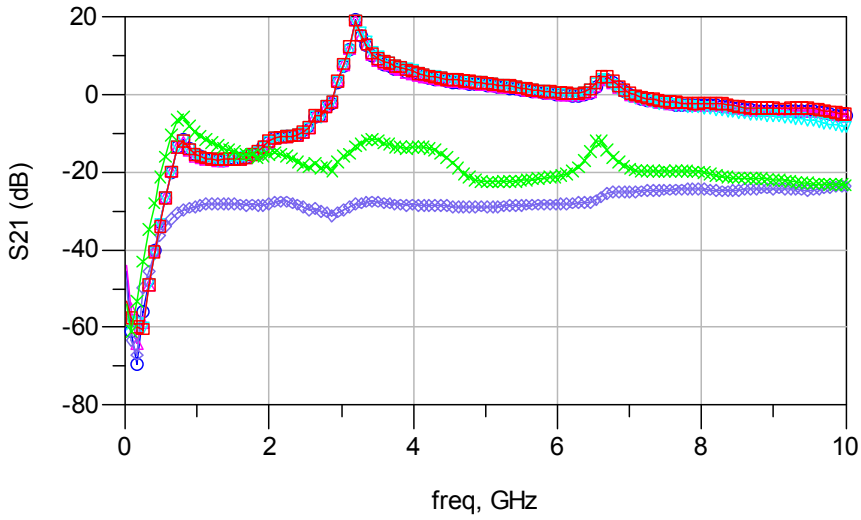


(a)

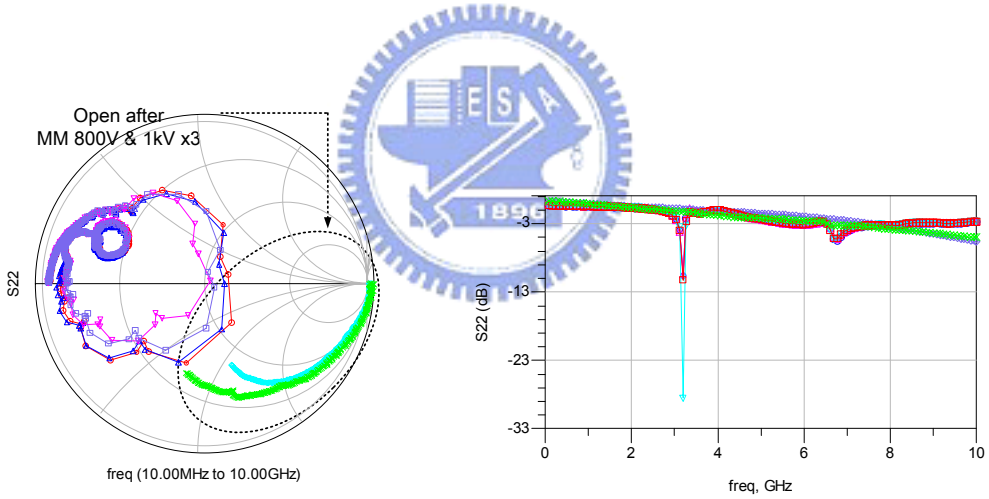


(b)

Fig. 4.16 Measurement results of (a) output power versus input power, and (b) gain versus input power, of the PA after three times HBM ESD zapping.



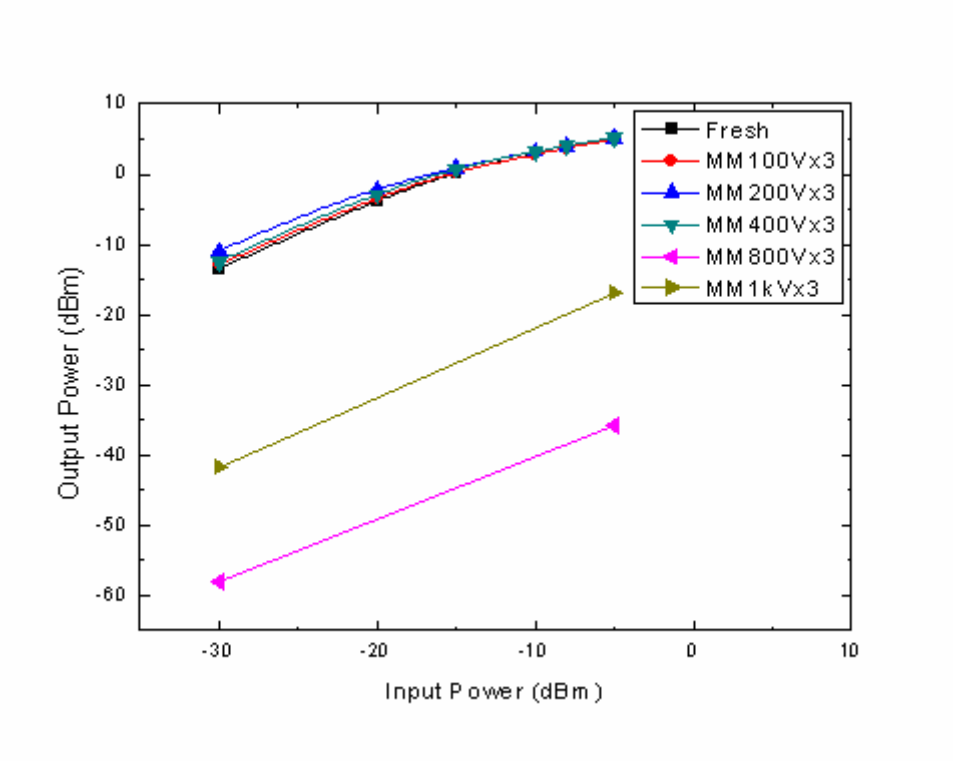
(a)



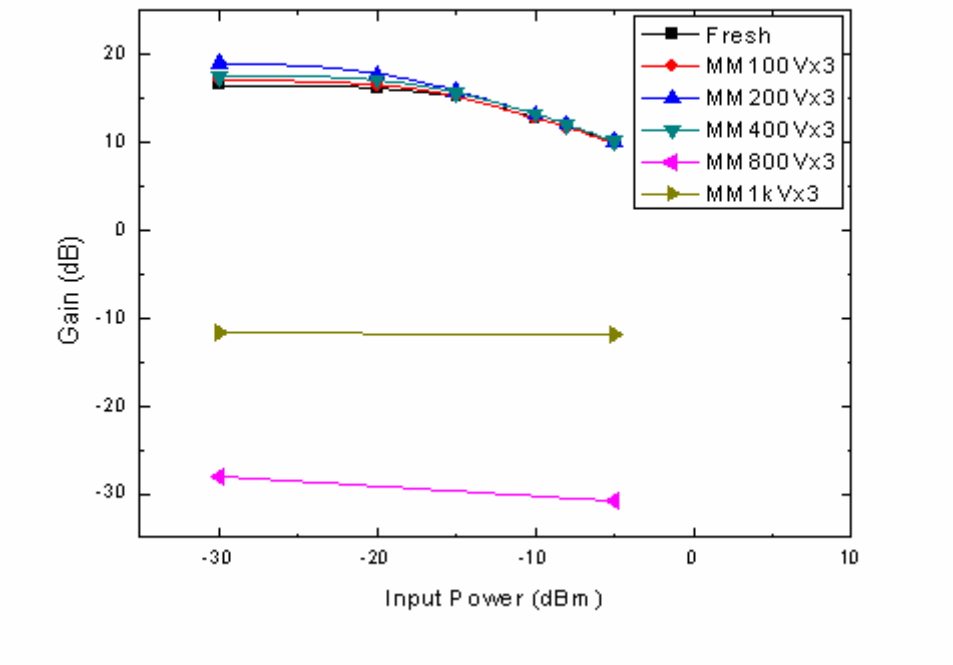
(b)

Fig. 4.17 Measurement results of (a) S21, and (b) S12, of the PA after three times MM ESD zapping.

Fresh	■
MM 100V x3	●
MM 200V x3	▲
MM 400V x3	▼
MM 800V x3	◆
MM 1kV x3	×



(a)



(b)

Fig. 4.18 Measurement results of (a) output power versus input power, and (b) gain versus input power, of the PA after three times MM ESD zapping.

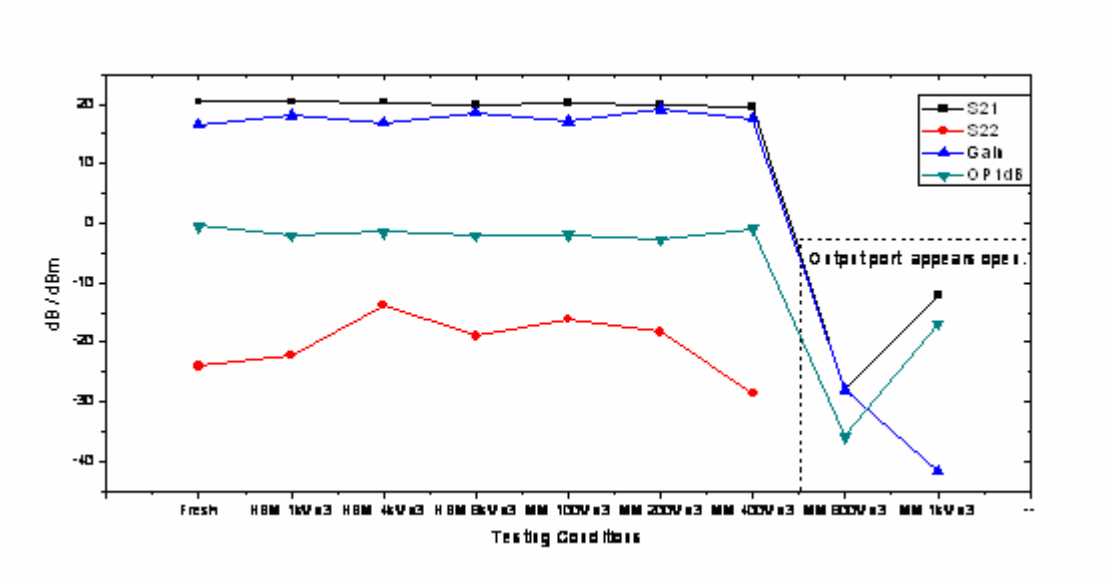


Fig. 4.19 Summary of the RF performance of the 3-GHz 0-dBm narrowband class-AB PA after ESD zapping.

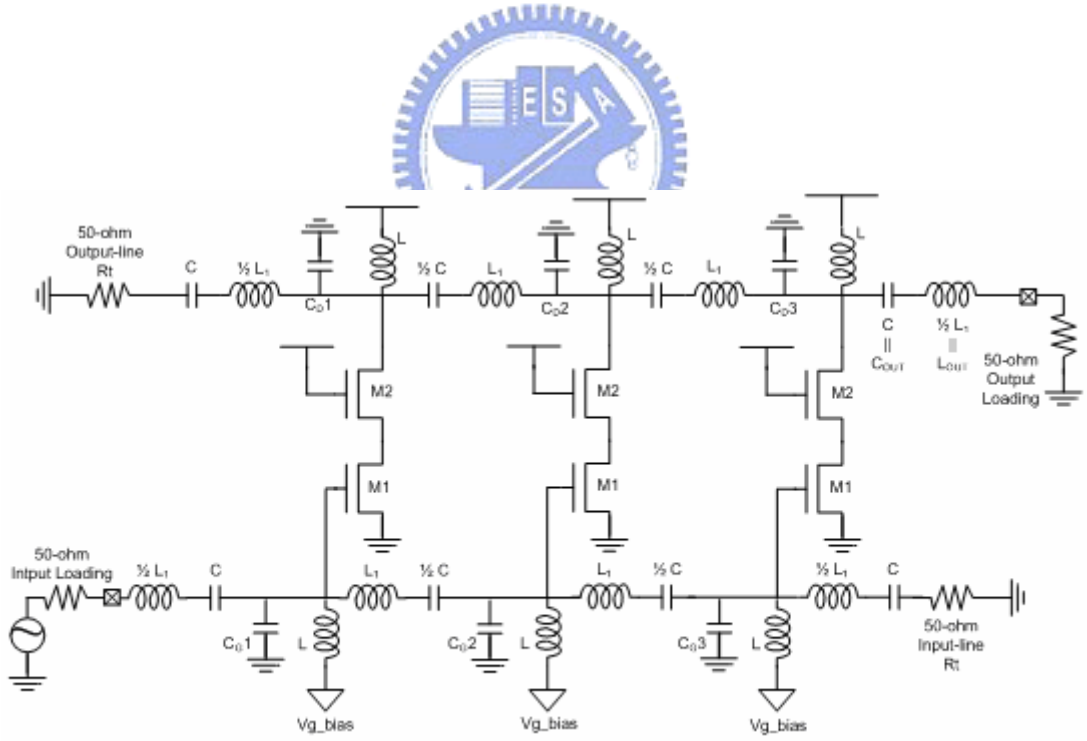


Fig. 4.20 Circuit schematic of the 3-to-10-GHz 0-dBm ultra-wideband class-AB distributed amplifier (DA).

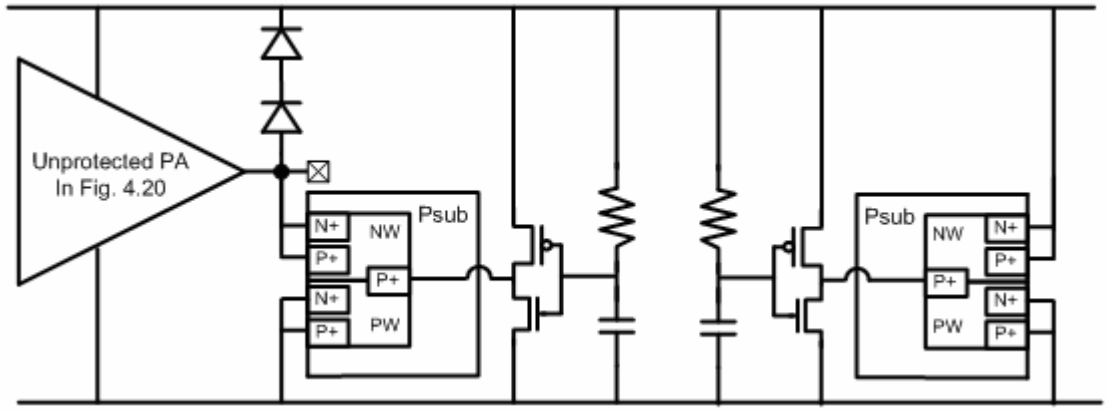
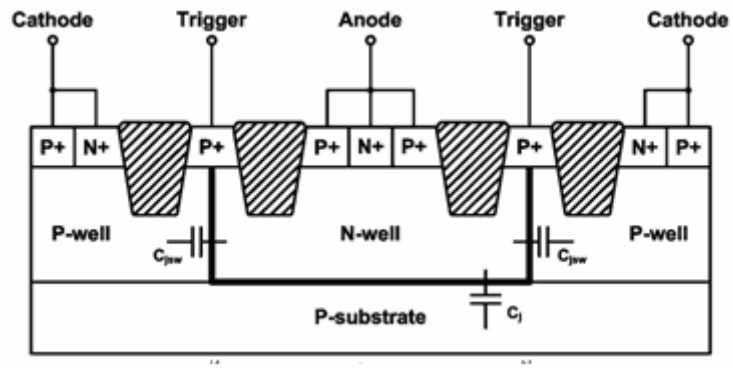
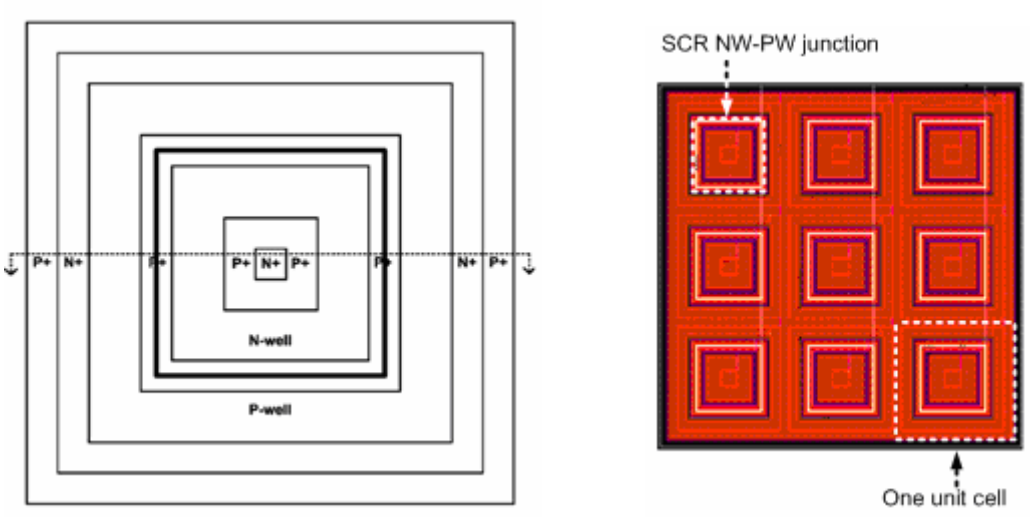


Fig. 4.21 The ESD protection circuit of the 3-to-10-GHz 0-dBm ultra-wideband class-AB distributed amplifier.

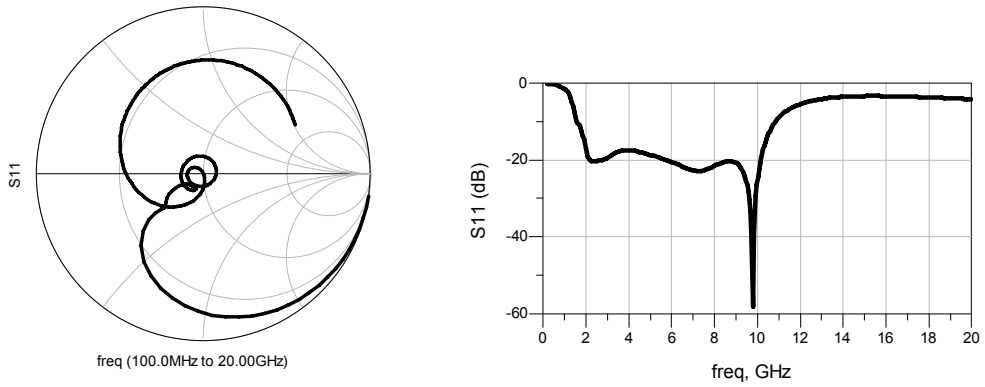


(a)

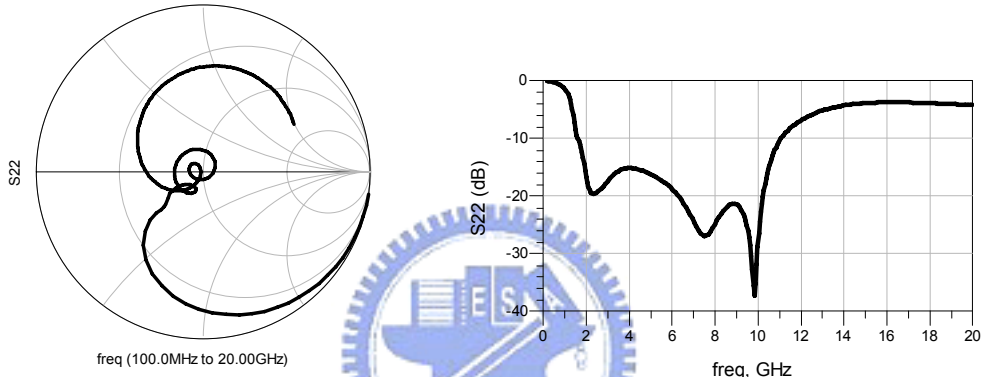


(b)

Fig. 4.22 (a) The device cross-sectional view, and (b) the layout top view, of the waffle-structured SCR.

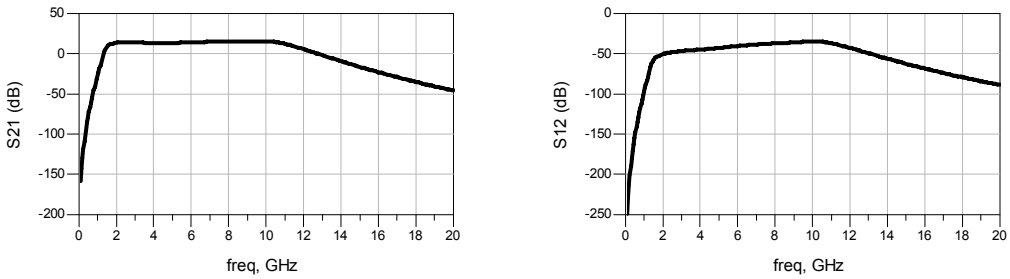


(a)



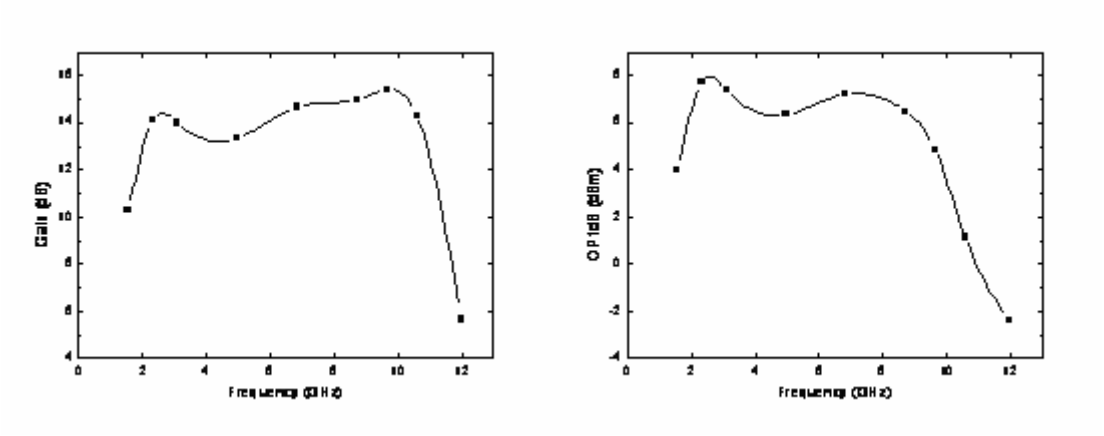
(b)

Fig. 4.23 Pre-layout simulation results: matching situations of (a) S11, and (b) S22, of the unprotected DA.



(a) (b)

Fig. 4.24 Pre-layout simulation results: power transmission of (a) S21, and (b) S12, of the unprotected DA.



(a) (b)

Fig. 4.25 Pre-layout simulation results: (a) gain, and (b) OP1dB, versus frequency of the unprotected DA.

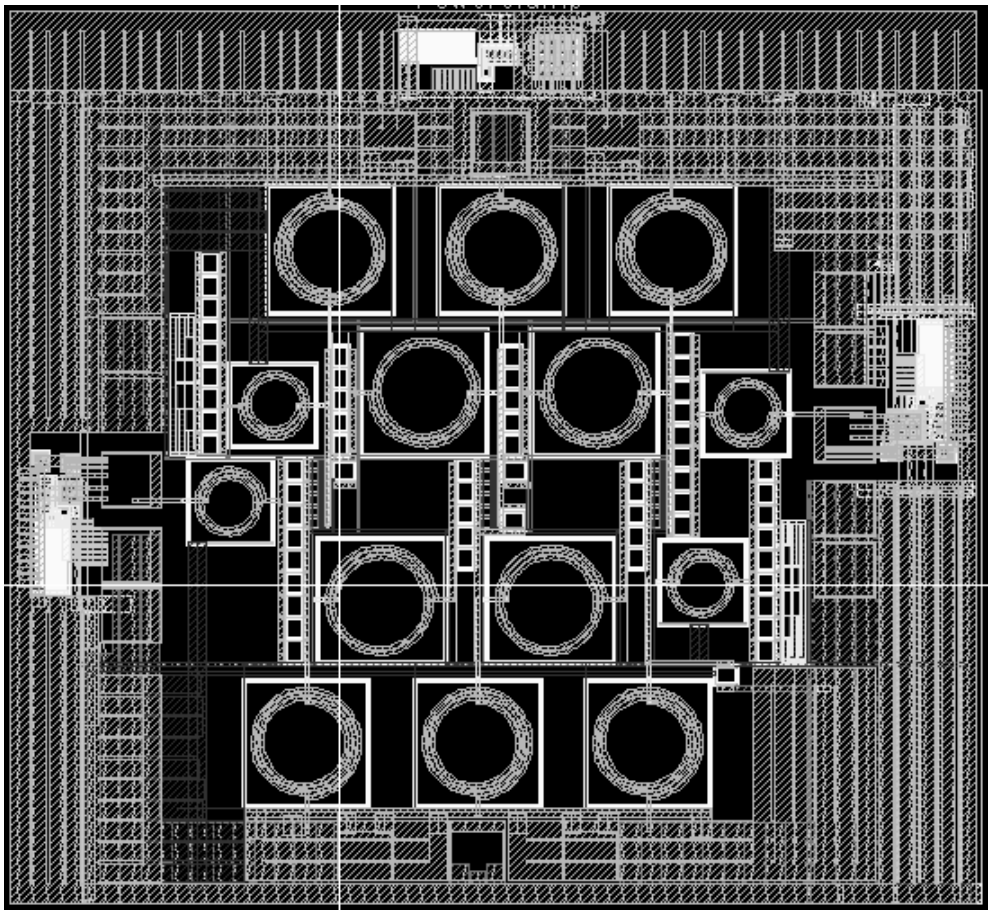
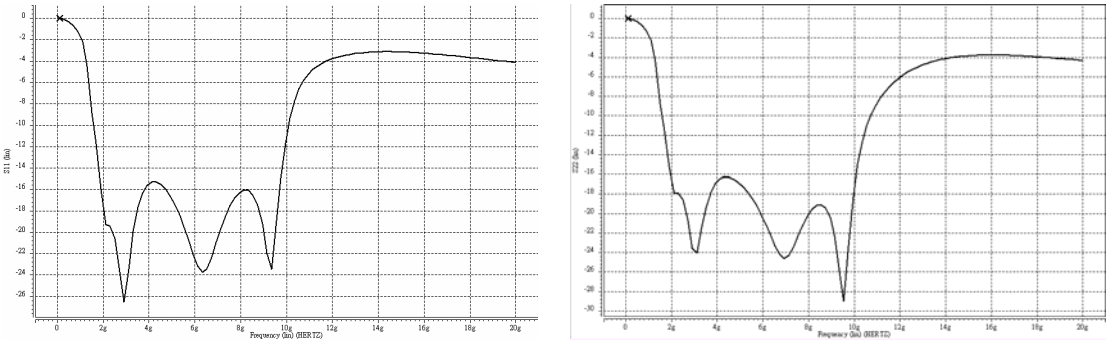
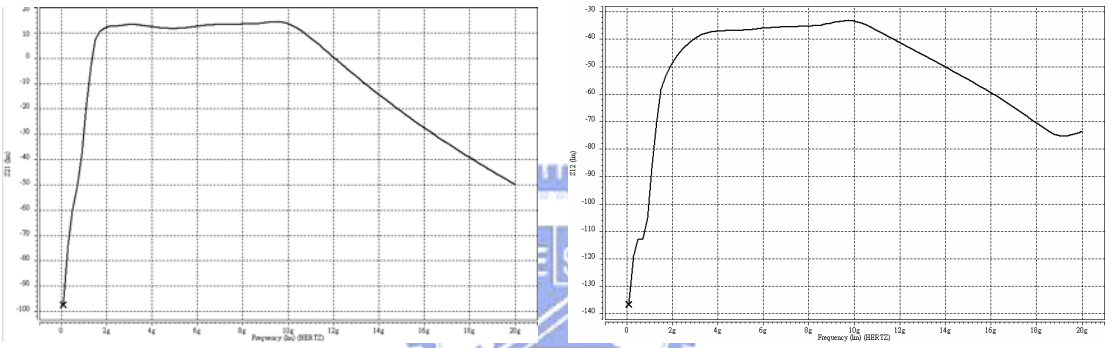


Fig. 4.26 Layout top view of the 3-to-10-GHz 0-dBm ultra-wideband class-AB distributed amplifier (DA).



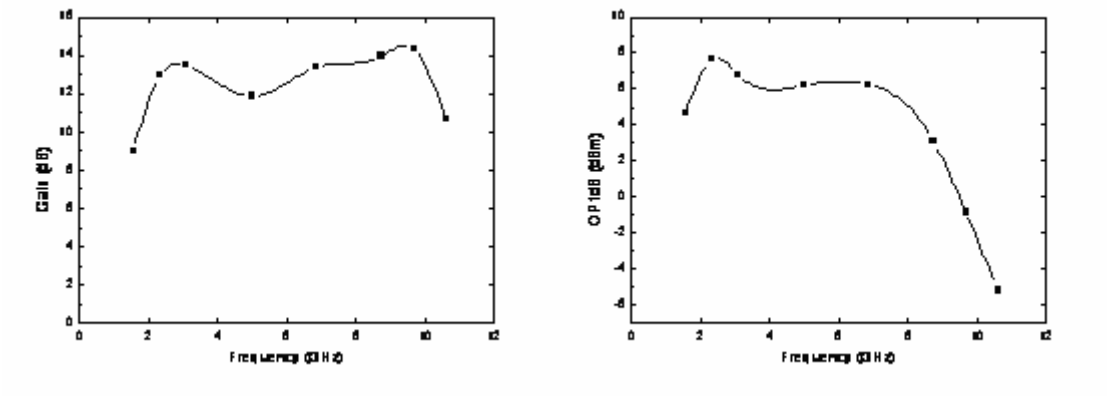
(a) (b)

Fig. 4.27 Post-layout simulation results: matching situations of (a) S11, and (b) S22, of the unprotected.



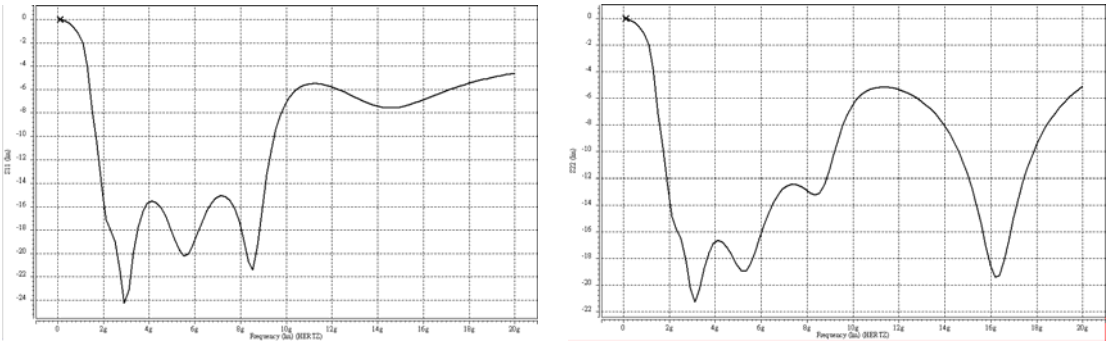
(a) (b)

Fig. 4.28 Post-layout simulation results: power transmission of (a) S21, and (b) S12, of the unprotected.



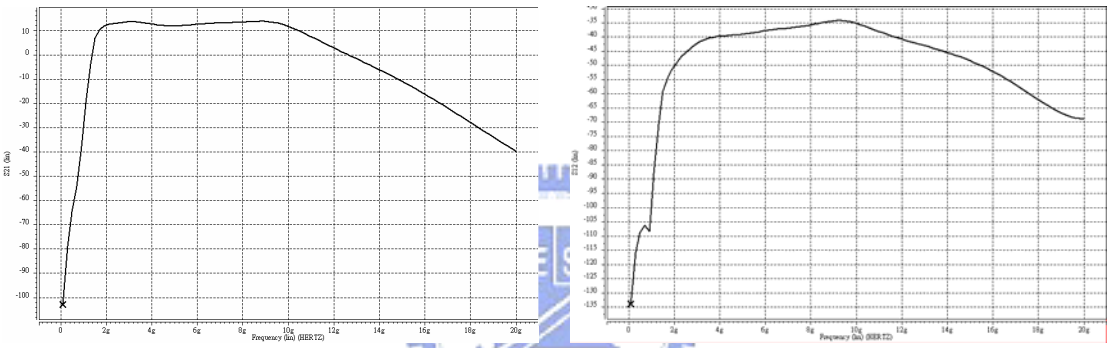
(a) (b)

Fig. 4.29 Post-layout simulation results: (a) gain, and (b) OP1dB, versus frequency of the unprotected DA.



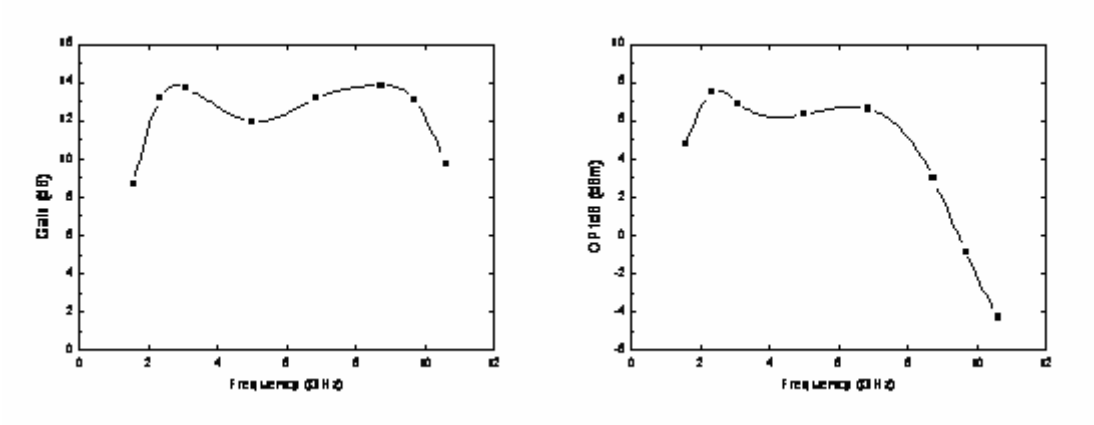
(a) (b)

Fig. 4.30 Post-layout simulation results: matching situations of (a) S11, and (b) S22, of the protected DA.



(a) (b)

Fig. 4.31 Post-layout simulation results: power transmission of (a) S21, and (b) S12, of the protected DA.



(a) (b)

Fig. 4.32 Post-layout simulation results: (a) gain, and (b) OP1dB, versus frequency of the protected DA.

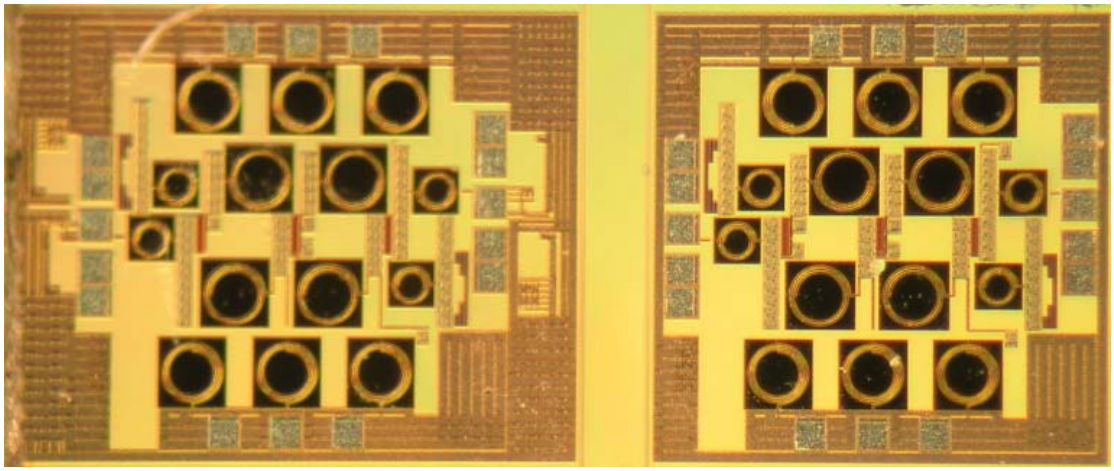
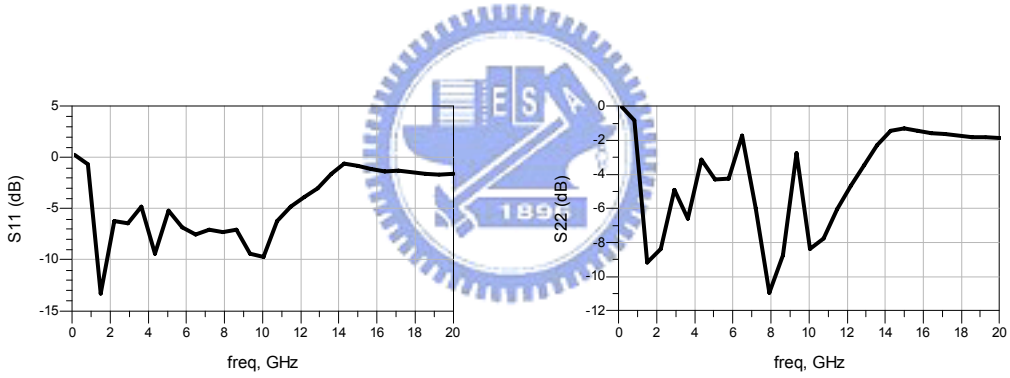
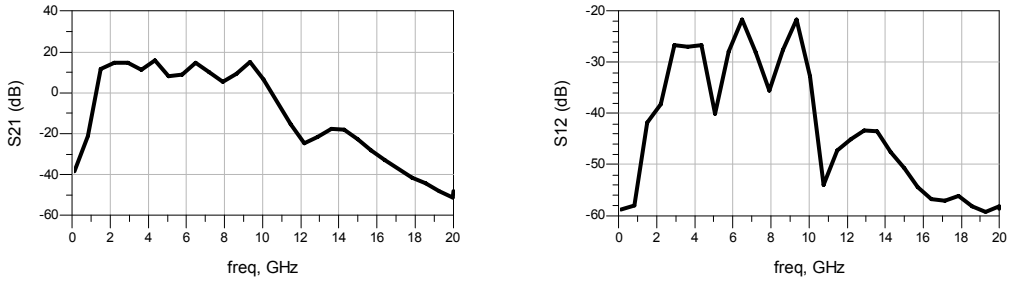


Fig. 4.33 Die photo of the 3-to-10-GHz 0-dBm ultra-wideband class-AB distributed amplifier (DA).



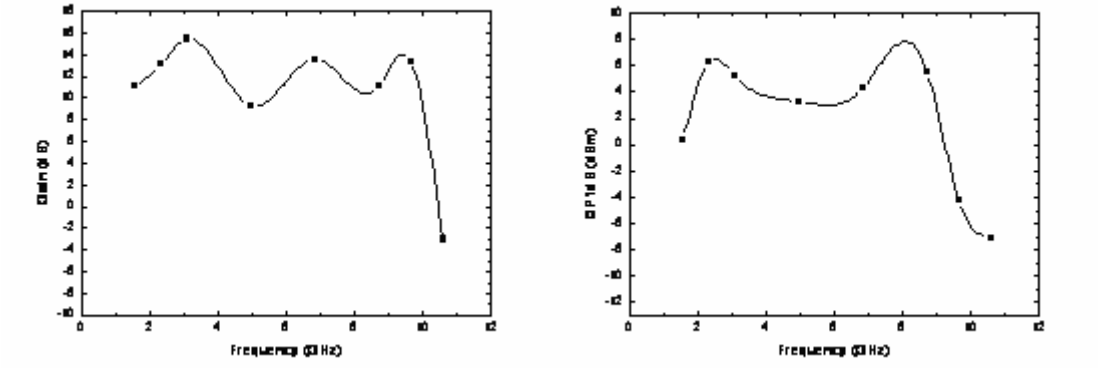
(a) (b)

Fig. 4.34 Measurement results: matching situations of (a) S11, and (b) S22, of the unprotected DA.



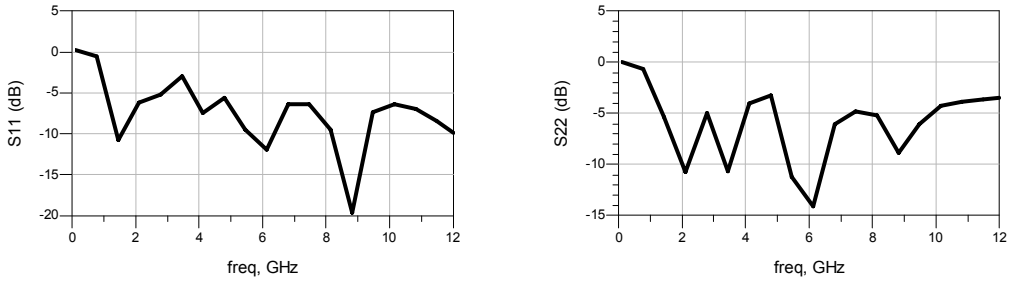
(a) (b)

Fig. 4.35 Measurement results: power transmission of (a) S21, and (b) S12, of the unprotected DA.



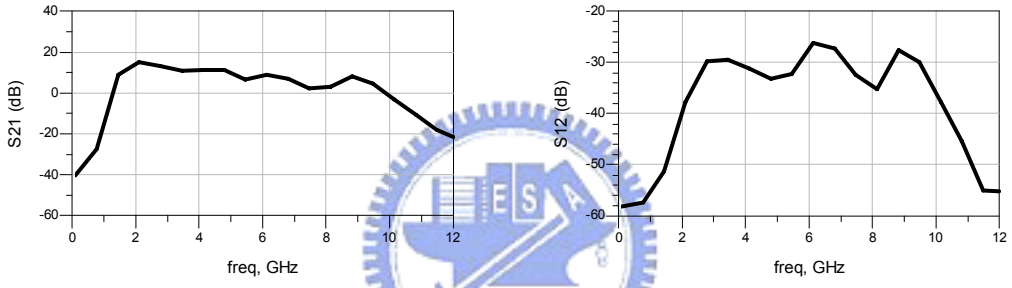
(a) (b)

Fig. 4.36 Measurement results: (a) gain, and (b) OP1dB, versus frequency of the unprotected DA.



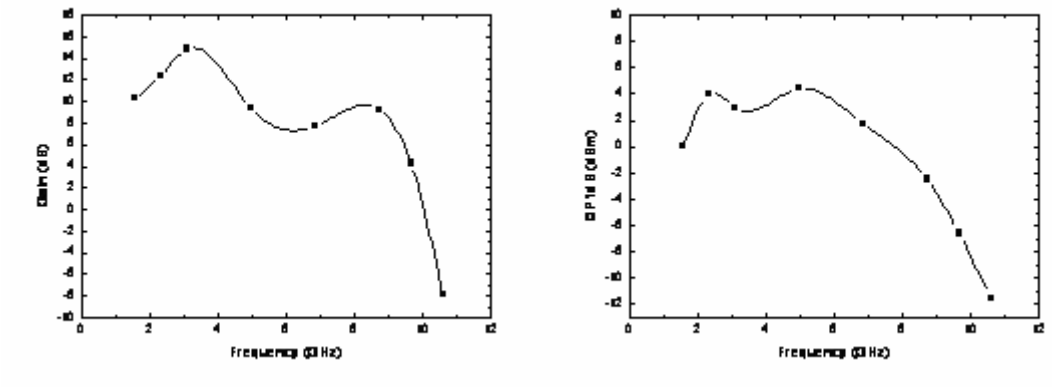
(a) (b)

Fig. 4.37 Measurement results: matching situations of (a) S11, and (b) S22, of the unprotected DA.



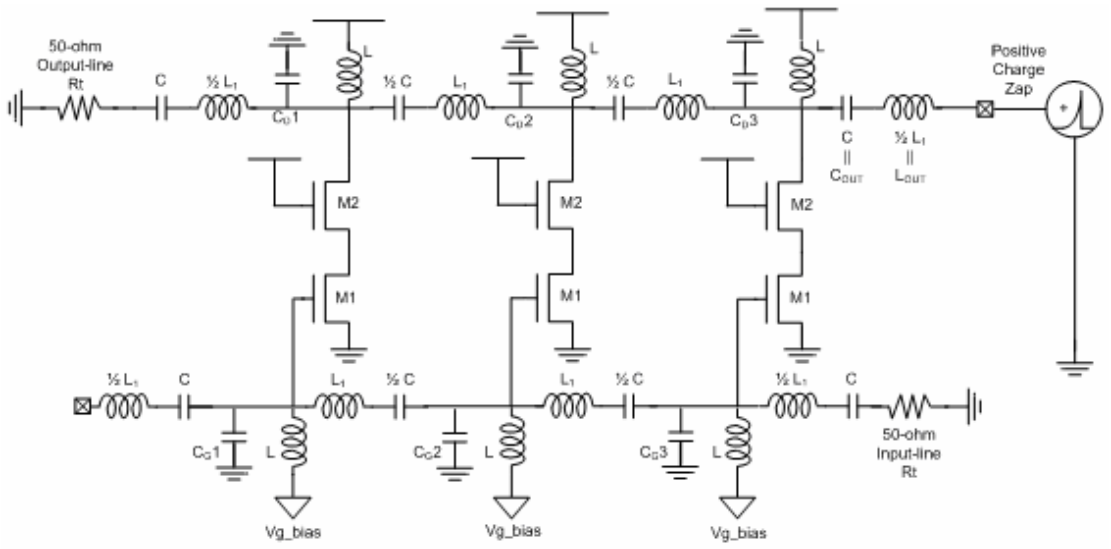
(a) (b)

Fig. 4.38 Measurement results: power transmission of (a) S21, and (b) S12, of the protected DA.

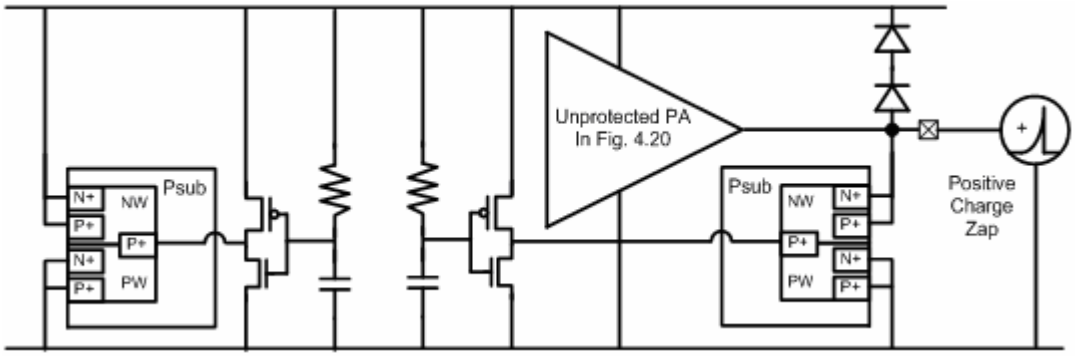


(a) (b)

Fig. 4.39 Measurement results: (a) gain, and (b) OP1dB, versus frequency of the protected DA.

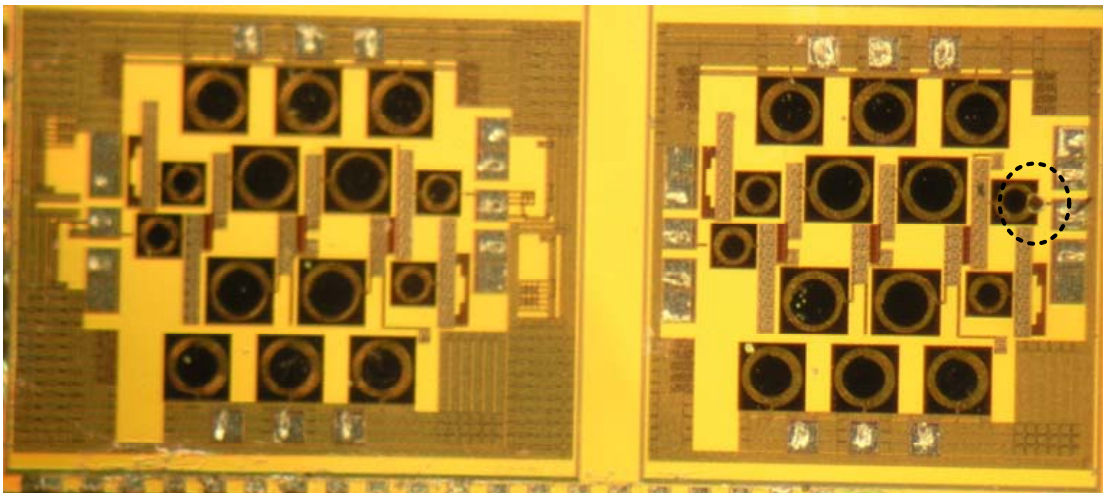


(a)

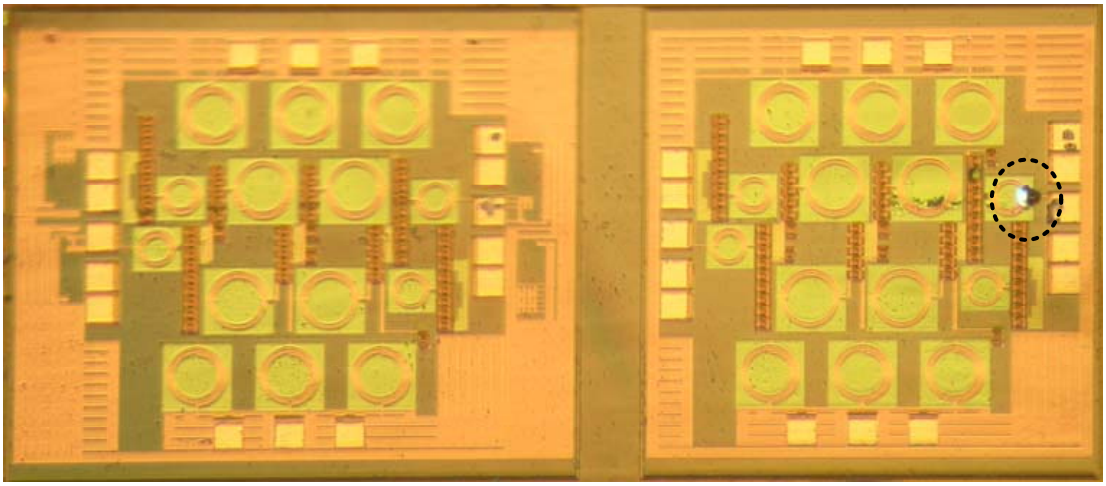


(b)

Fig. 4.40 ESD testing set-up for (a) the unprotected DA and (b) the protected DA.

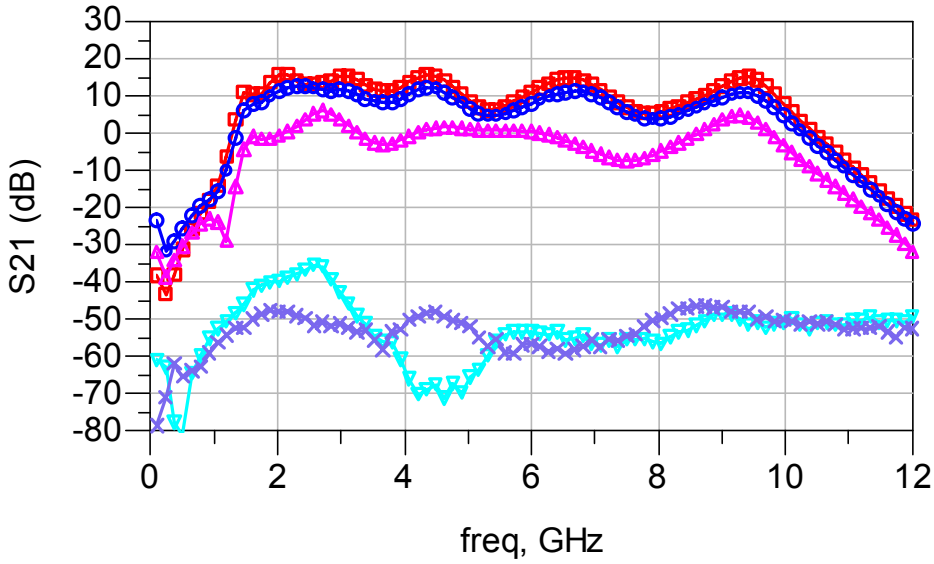


(a)

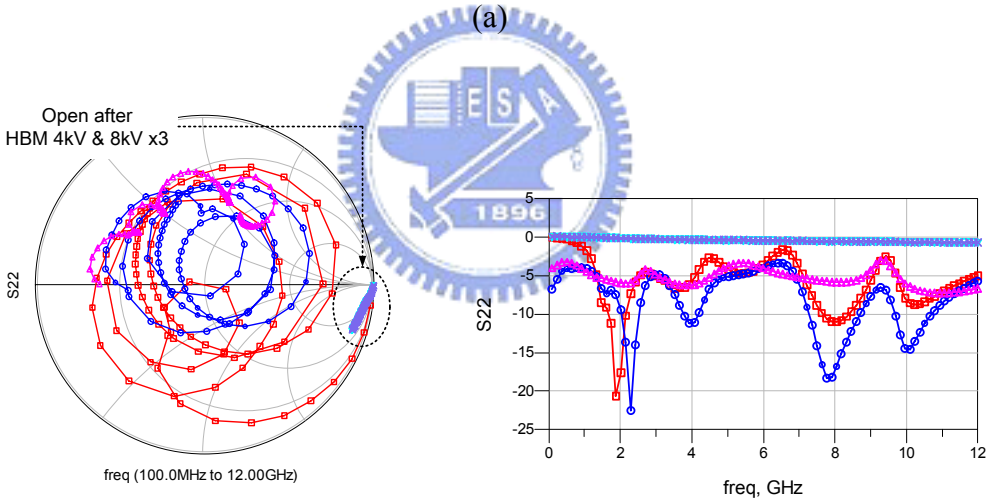


(b)

Fig. 4.41 Die photo of the unprotected DA after three times ESD zapping of (a) 4kV HBM and (b) 400V MM.



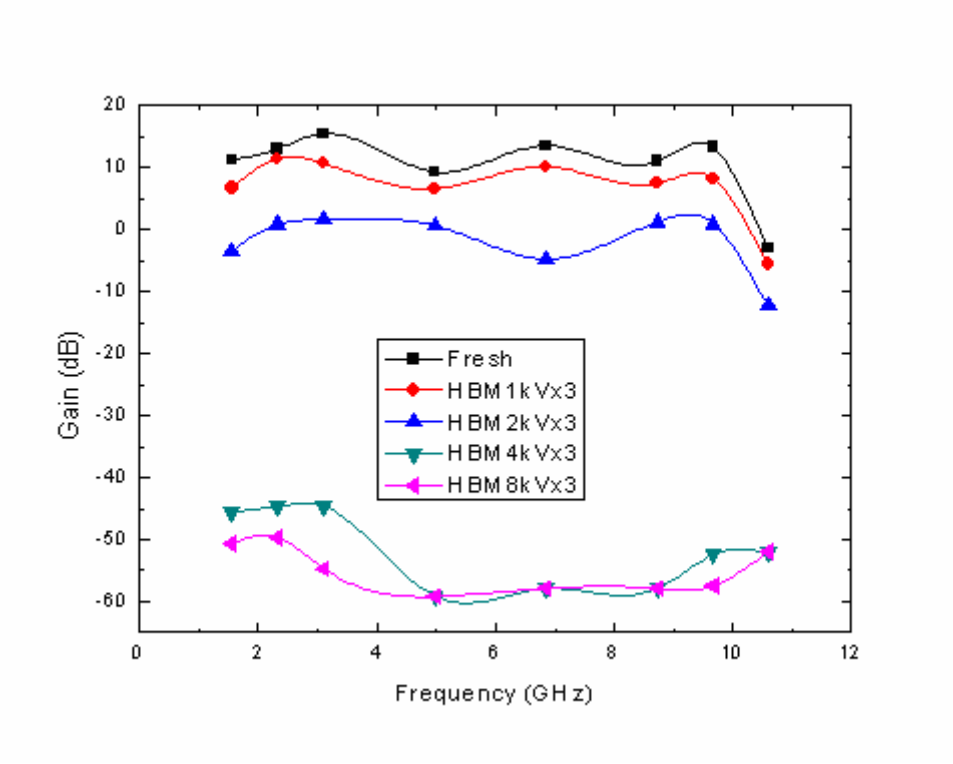
(a)



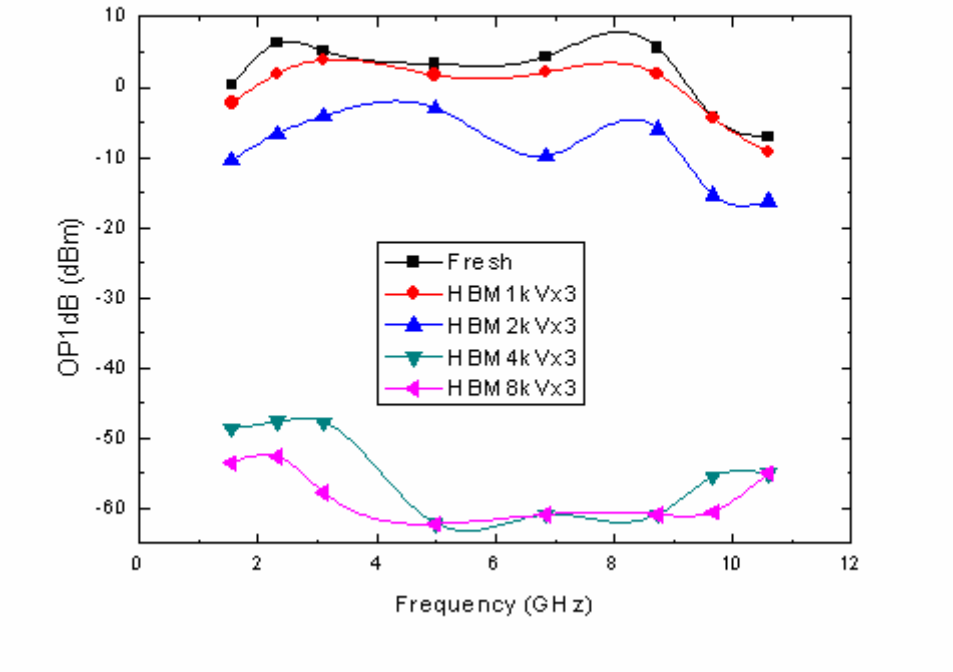
(b)

Fig. 4.42 Measurement results of (a) S21, and (b) S22, of the unprotected DA after three times HBM ESD zapping.

Fresh	■
HBM 1kV x3	●
HBM 2kV x3	▲
HBM 4kV x3	▼
HBM 8kV x3	×

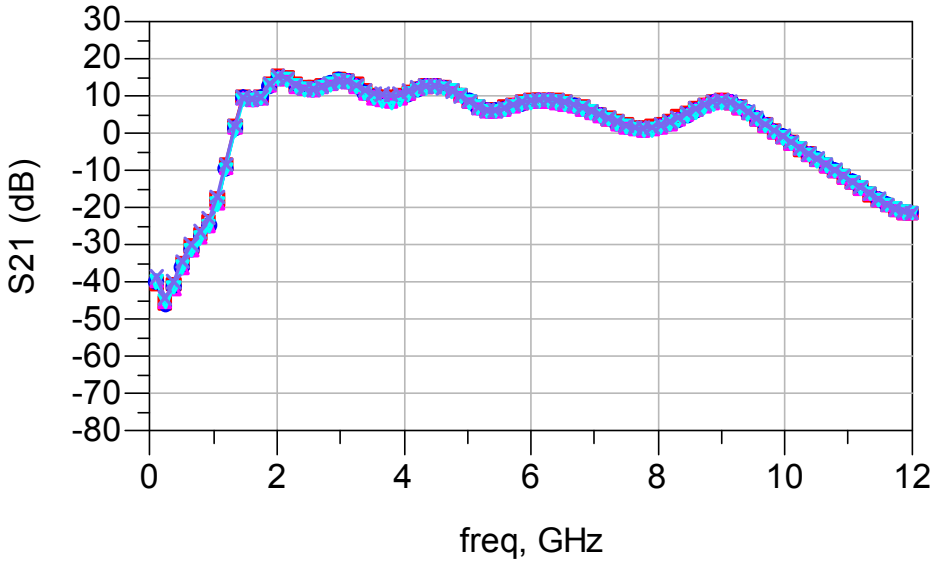


(a)

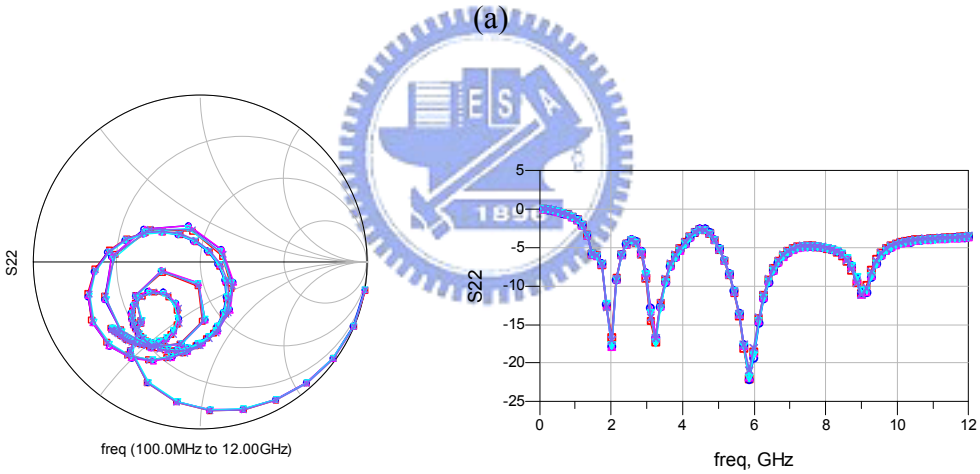


(b)

Fig. 4.43 Measurement results of (a) gain, and (b) OP1dB, versus frequency of the unprotected DA after three times HBM ESD zapping.



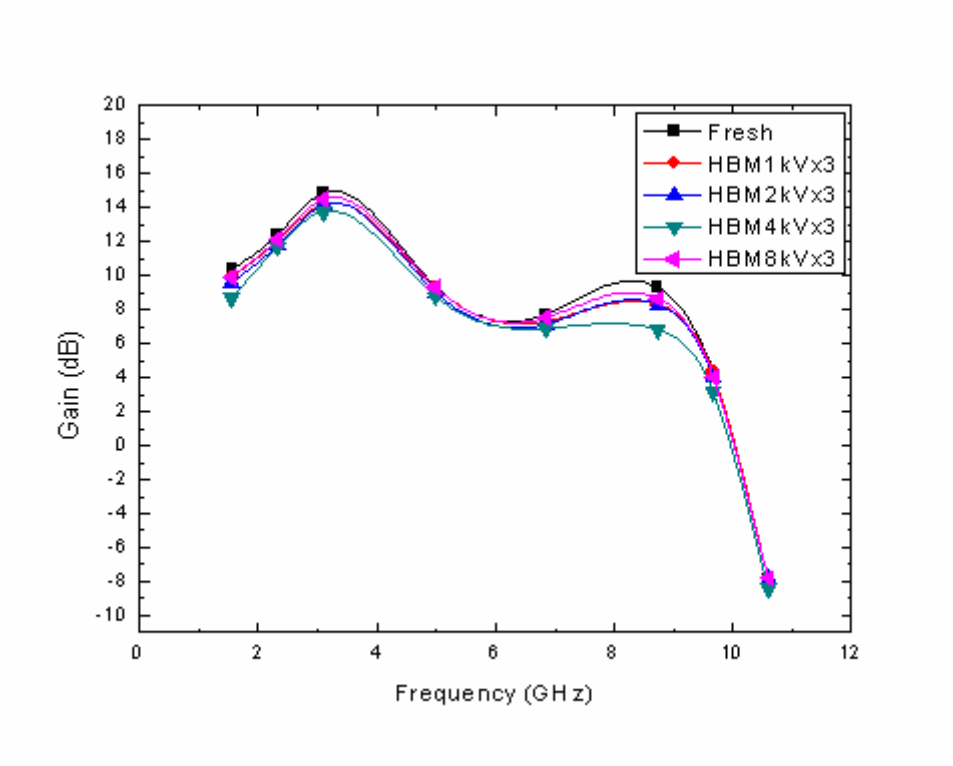
(a)



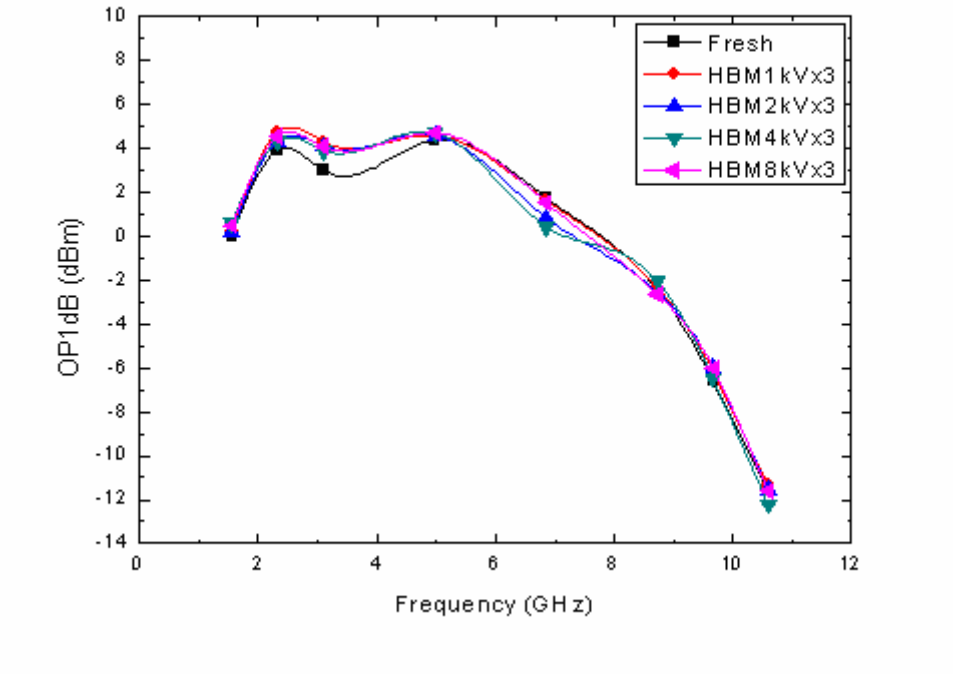
(b)

Fig. 4.44 Measurement results of (a) S21, and (b) S22, of the protected DA after three times HBM ESD zapping.

Fresh	■
HBM 1kV x3	●
HBM 2kV x3	▲
HBM 4kV x3	▼
HBM 8kV x3	×

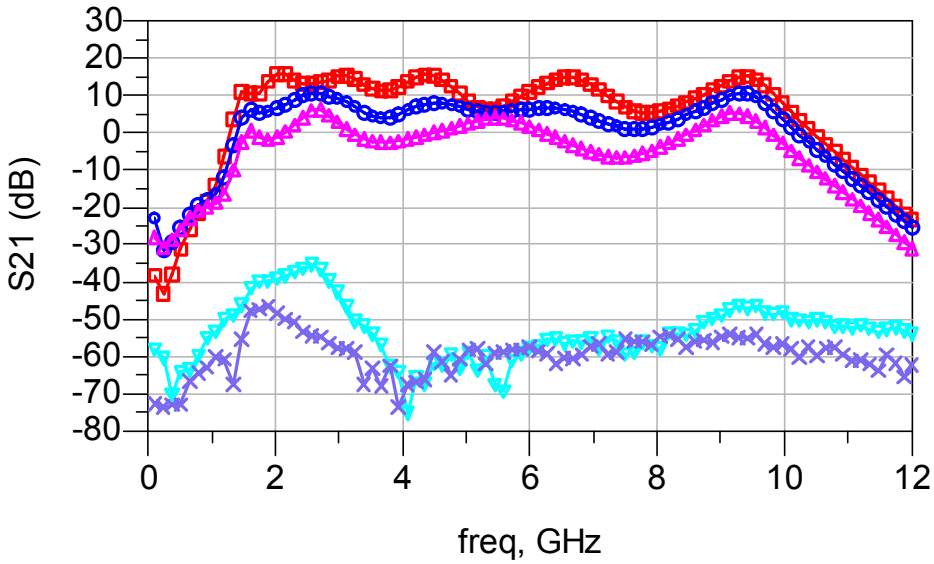


(a)

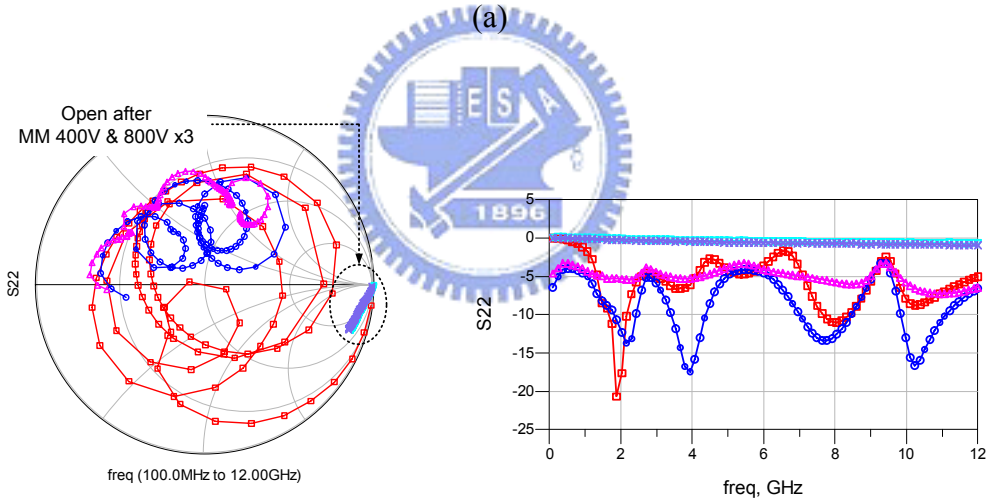


(b)

Fig. 4.45 Measurement results of (a) gain, and (b) OP1dB, versus frequency of the protected DA after three times HBM ESD zapping.



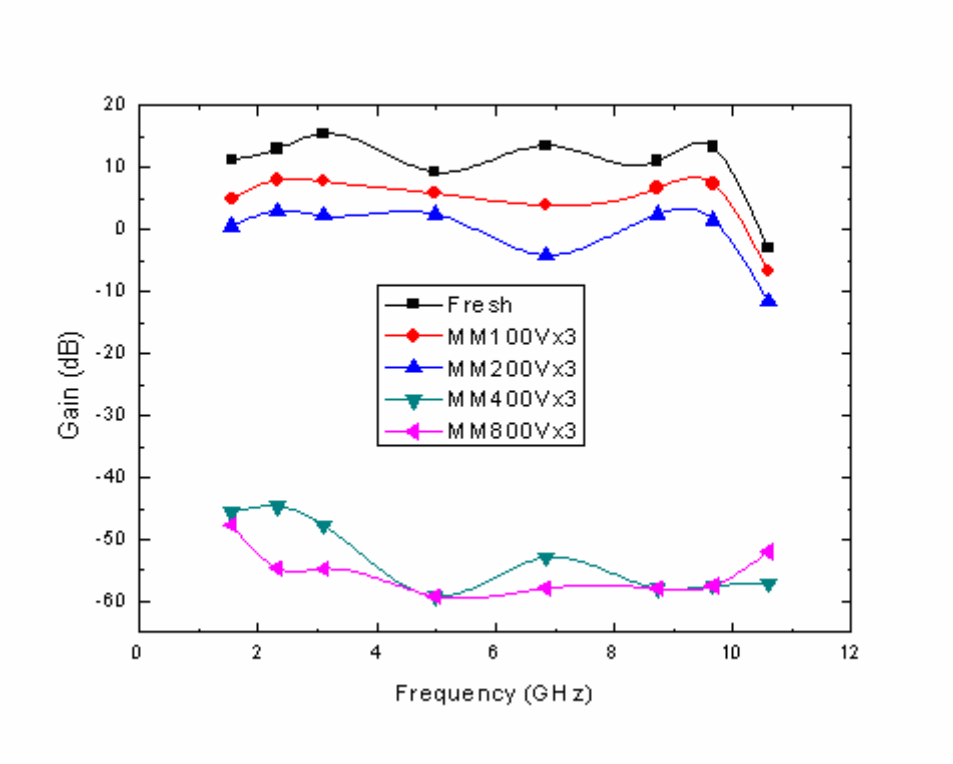
(a)



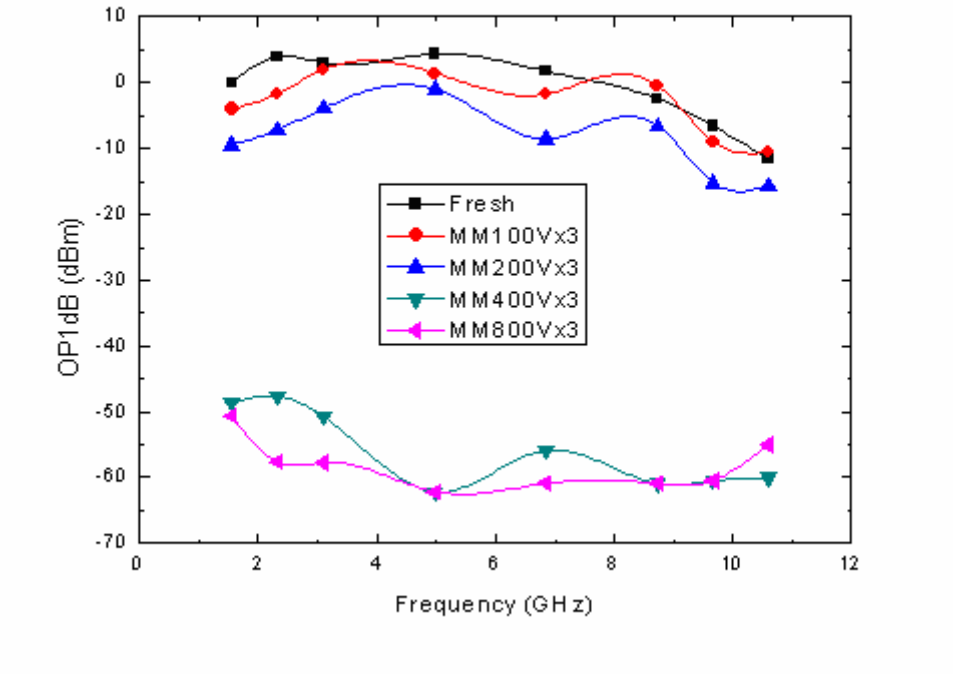
(b)

Fig. 4.46 Measurement results of (a) S21, and (b) S22, of the unprotected DA after three times MM ESD zapping.

Fresh	■
MM 100V x3	●
MM 200V x3	▲
MM 400V x3	▼
MM 800V x3	×

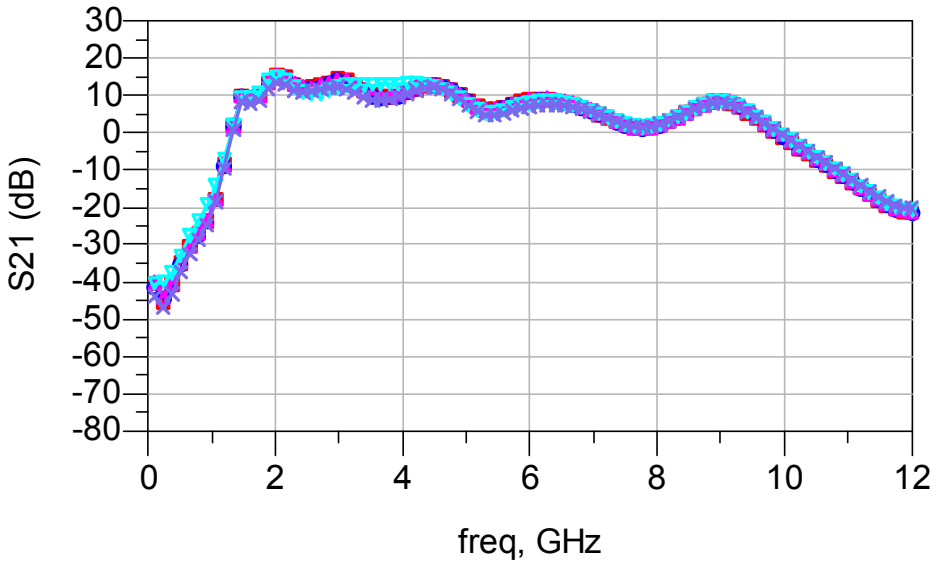


(a)

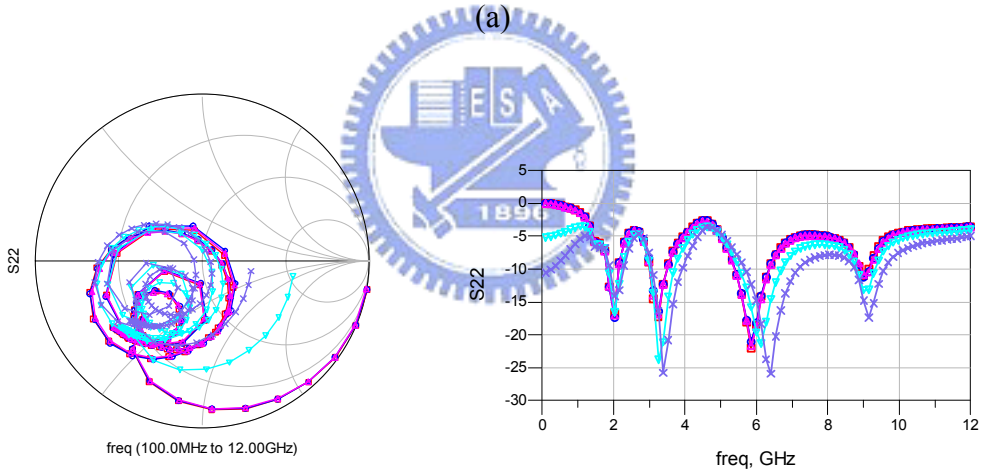


(b)

Fig. 4.47 Measurement results of (a) gain, and (b) OP1dB, versus frequency of the unprotected DA after three times MM ESD zapping.



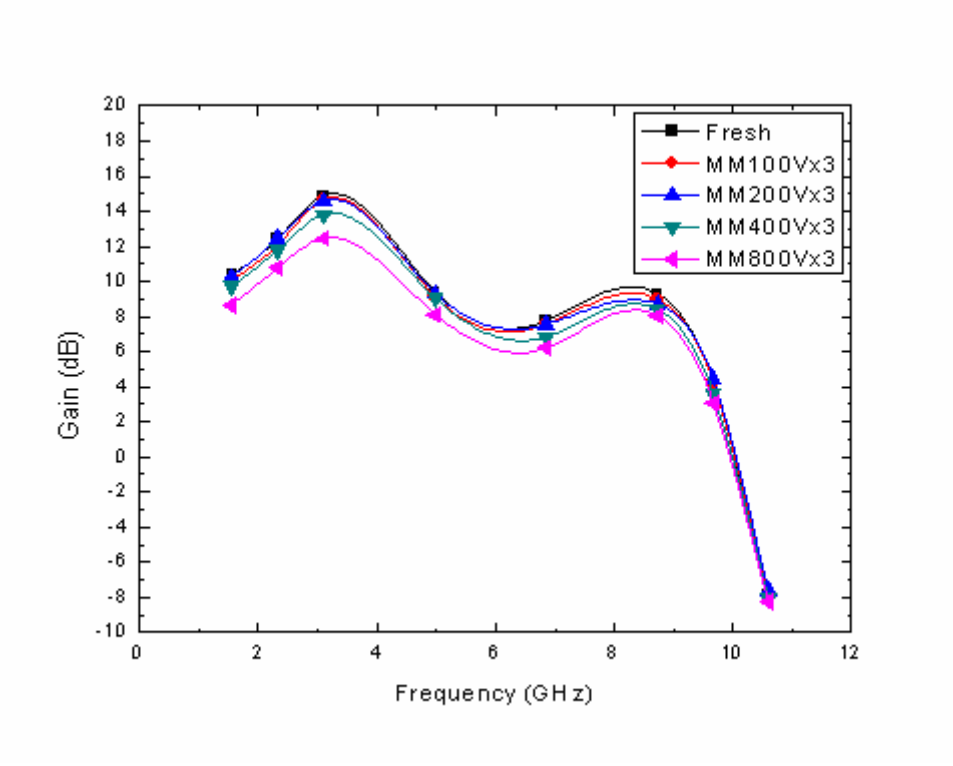
(a)



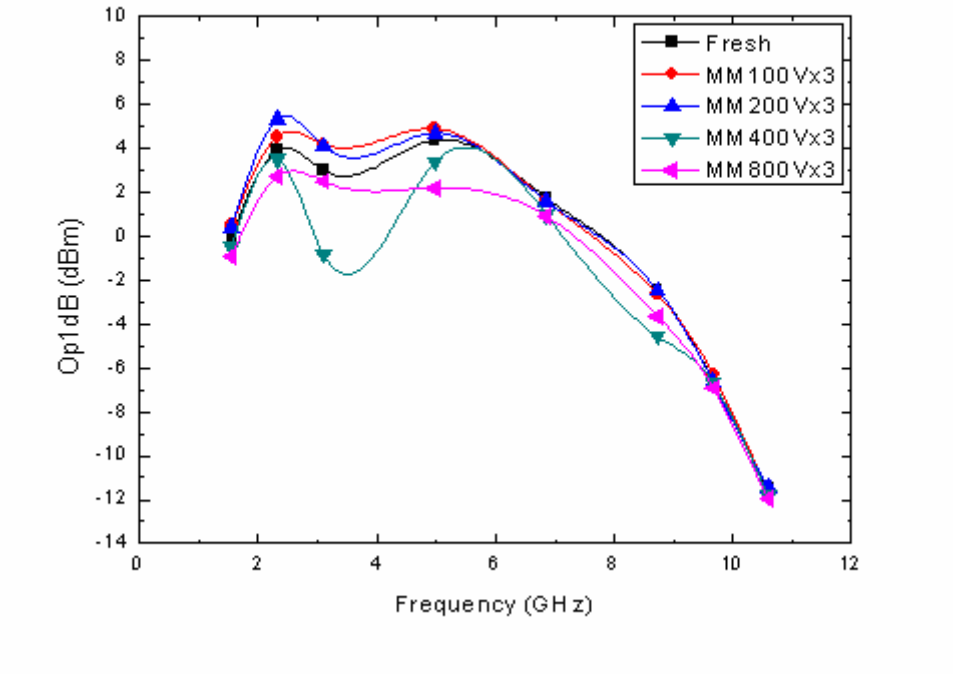
(b)

Fig. 4.48 Measurement results of (a) S21, and (b) S22, of the protected DA after three times MM ESD zapping.

Fresh	■
MM 100V x3	●
MM 200V x3	▲
MM 400V x3	▼
MM 800V x3	×

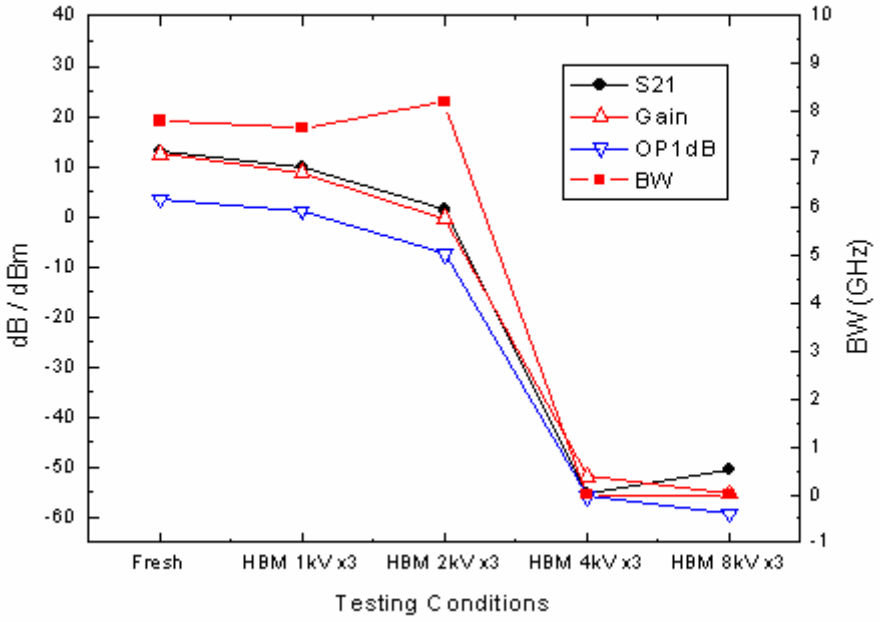


(a)

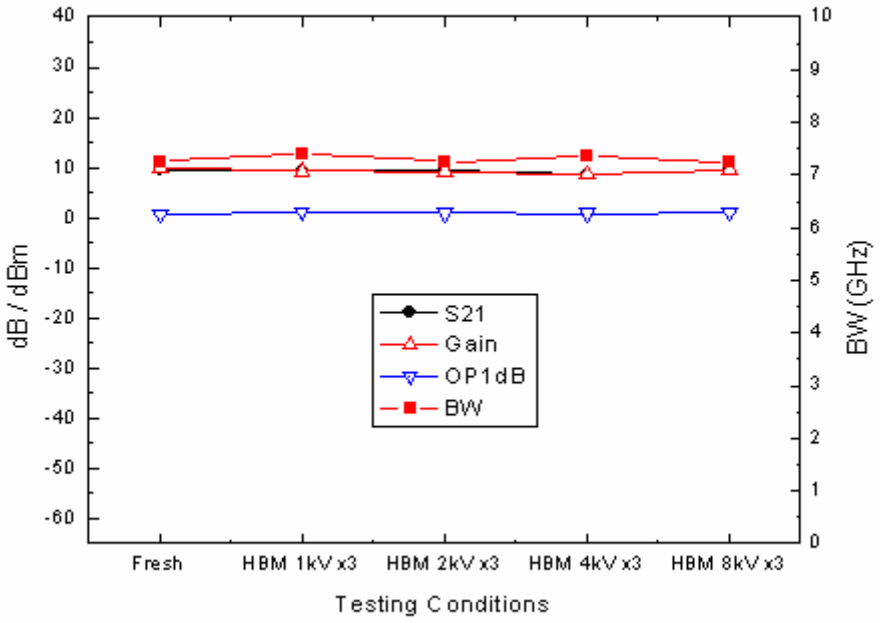


(b)

Fig. 4.49 Measurement results of (a) gain, and (b) OP1dB, versus frequency of the protected DA after three times MM ESD zapping.

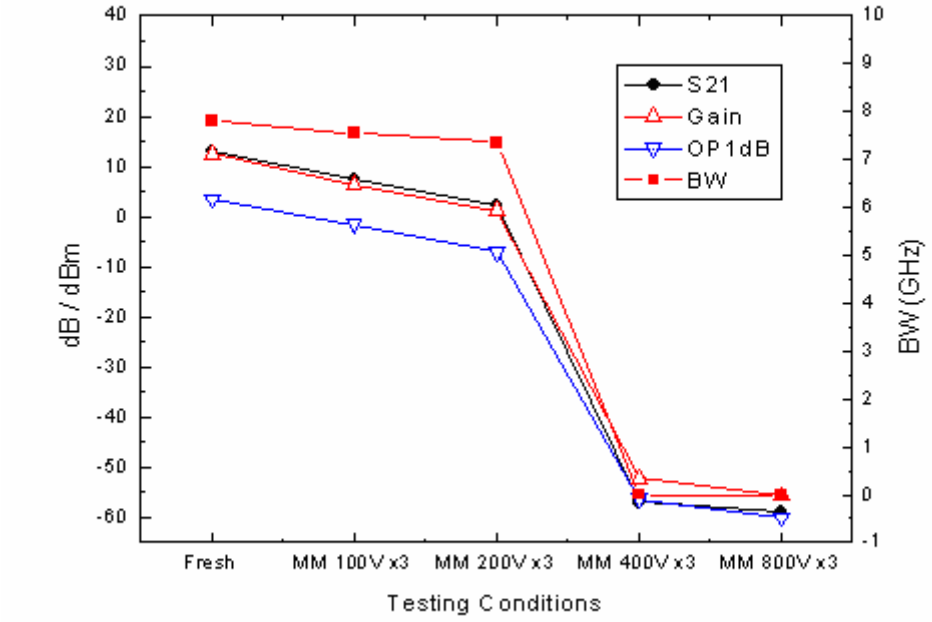


(a)

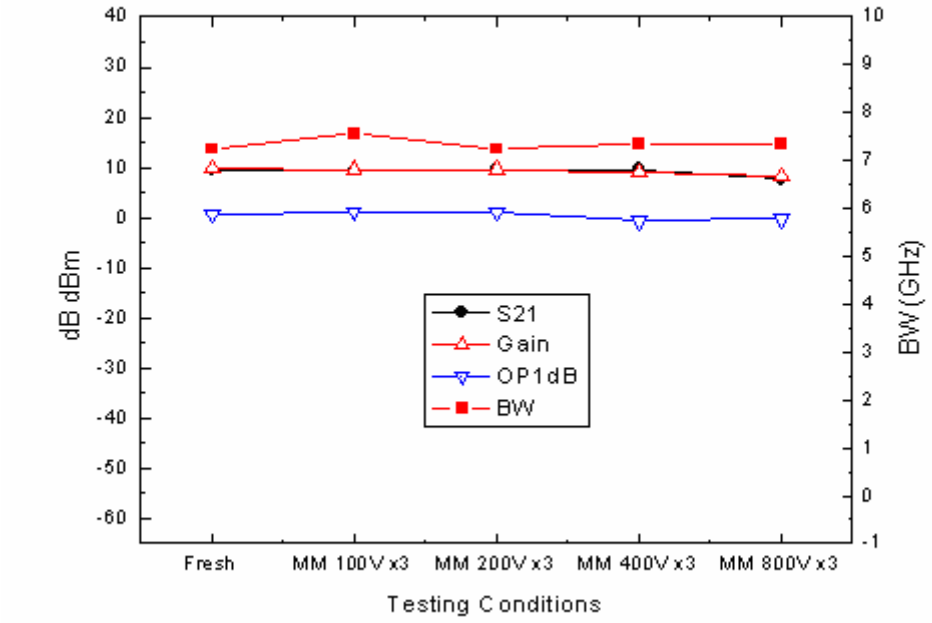


(b)

Fig. 4.50 Summary of the RF performance of the 3-to-10-GHz 0-dBm ultra-wideband class-AB distributed amplifier after HBM ESD zapping: (a) the unprotected DA and (b) the protected DA.



(a)



(b)

Fig. 4.51 Summary of the RF performance of the 3-to-10-GHz 0-dBm ultra-wideband Class-AB distributed amplifier after MM ESD zapping: (a) the unprotected DA and (b) the protected DA.

Chapter 5
Failure Analysis

5.1 ESD Damage Mechanism for Passive Devices

In this section the ESD damage mechanism for passive devices is further analyzed to obtain design insights for ESD protection circuit. On-chip inductor and metal-insulator-metal capacitor (MIMCAP) are both in common use in RF circuits and are proved to be in urgent need of ESD protection. Experimental results reveal the truth that once stressed by ESD zapping the passive devices may be immediately damaged, and the overall RF functionality pf the circuit may be degraded accordingly. Therefore, the best solution for increasing the overall RF circuit ESD robustness is to provide ESD protection for the entire circuit and to design the devices in use with intrinsically high ESD robustness. The following sections analyze the damaged passive devices mentioned in chapter 4 and provide the device design insight in details. L_{OUT} stands for the on-chip inductor closest to the output pad; C_{OUT} stands for the MIMCAP closest tot the output pad.

5.1.1 L_{OUT}

From the die photos it can be seen that an obviously damaged on-chip inductor is failed at the metal interconnect via. The resistance of a via is usually higher than the resistance of a metal trace. It is because the material used to form a via has intrinsically higher resistance, as compared to the material used to form a metal trace layer. Further, metal trace can have wide trace width, but the number of via contact is

limited by the small overlapping area of two metal trace layers, as in the case of an on-chip inductor. Therefore a lot more heat is generated by the ESD current flowing through via with the higher resistance and melts this via farm first, as compared to the metal traces. In short, the maximum allowable current density of the via for safe operation is much smaller than that of the metal trace. Therefore, the bottleneck of the ESD robustness of an on-chip inductor is the number of via contact, and increasing the via contact number can effectively improve the ESD robustness of the on-chip inductor and thus the entire circuit output circuit.

For RF application the inductance is in the range of several hundreds of pico-henry. For HBM and MM ESD events, the ESD current typically locates in the range of several tens of MHz; the RF signal locates in the range of several GHz. The difference is about one order (10 times). The effective discharging path impedance is about 0.05 to 0.1 ohm. Therefore, on-chip inductor forms an effective low impedance path for ESD current. Also, since MM ESD event is faster than HBM ESD event, MM ESD current consequently causes more damage on the inductor. The higher spectral location of the MM ESD event makes the inductor act less likely as a low impedance discharging path, as compared to the HBM ESD event located at the lower spectrum. Therefore, the MM ESD level of the inductor is lower than the HBM level. In such sense, the inductance of the inductor serving for the ESD protection device is best to be as small as possible. This is good to high speed RF circuit because the higher operation frequency leads to the smaller inductance needed, resulting in intrinsically better ESD robustness.

5.1.2 C_{OUT}

From the die photo it can be seen that the obviously damaged MIMCAP is failed at the top metal layer connected to the output pad. The damaging mechanism is quite

nontrivial to imagine; the concept of power wave transmission and reflection needs to be incorporated since ESD current is almost closed to an RF/Microwave signal (rise-time about 10ns or shorter). If electrical current can be viewed as a water current, the ESD current can be viewed as a tsunami, and the metal trace acts like a transmission line. This destructive tidal wave travels on the metal trace. It comes in through the output pad and rushes inward to the inner circuit (Fig. 5.1 (a)). Before it runs into any thing, it peels off the topmost layer of the metal trace material along with its journey by the high current density and fast transient rise-time as its destructive wave-front. It ends up with the MIMCAP which appears to be a dead end to the ESD current. The ESD current then bounces back and flushes backward to the output pad (Fig. 5.1 (b)). The MIMCAP needs not be punched through, since the input ESD current is almost all reflected back. However, ESD current indeed flows across the top metal layer of the MIMCAP, and such a high and fast transient current density indeed scrapes the metal trace, similar to the mechanism of metal-migration. Therefore, to effectively protect a MIMCAP from ESD zapping is to shunt away the ESD current and prevents the destructive ESD tsunami even reaching the device.

5.1.3 Effects of the Damage of the Passive Devices

Once zapped by ESD current, the physical structure of a passive device is certainly different from what it used to be. That is, the exhibiting electrical property is altered by ESD zapping. For an on-chip inductor, the parasitic series resistance is increased and the inductance may also be increased. This is the consequence of the metal-migration-like damage on the metal trace and via farm of an on-chip inductor. These damages ultimately prevent current to flow through an on-chip inductor, and the electrical effect is an increase in resistance and inductance. For a MIMCAP, peeling off the top metal layer is equivalent to increase the parasitic resistance in

series with the MIMCAP and lower the Q-factor of the device.

Slight variation of the passive device parameters results in a great deal of degradation on the overall circuit operation. Even a small difference of inductance or capacitance is multiplied by frequency of several GHz, and the result is a huge amount of RF functionality shift. For an output matching network, the matching property is altered, and the RF output power wave cannot be transmitted properly. For a distributed amplifier, the delay taps of the input and output artificial lines are not matched equally with each other and the RF power waves is not constructively superimposed properly. Further, the increase of parasitic series resistance and the lowering of the Q-factor results in losses of the RF signal power. All this alternations lead to a decrease in gain and output power. This is how the ESD zapping damages the passive devices and results in the degradation of the overall circuit RF functionality.

5.2 DAMAGE MECHANISM OF ESD ON THE LOW-C ESD CLAMP

In this section the ESD damage mechanism for the low-C ESD clamp is further analyzed to obtain design insight for ESD protection circuit. Unlike passive devices which is linear and time-invariant, ESD clamping devices usually exhibits nonlinear behavior. Their transfer I-V characteristics require a series of measurements to obtain their behavior models and design guide lines. Failure analysis is done with the help of SEM (Scanning Electron Microscope) to locate the hot spot firstly damaged by ESD current. The following subsections analyze the transfer I-V characteristics and the SEM photos of the low-C ESD clamps.

5.2.1 Transfer I-V Characteristics of the Low-C ESD Clamps

Fig. 5.2 (a) and (b) is the DC I-V characteristics curves of the I/O and power-rail Low-C ESD clamps, respectively. These two curves are obtained by measuring the I-V relationship of the output pad and VDD pad to GND pad of the protected DA using a HP 4156B parameter analyzer.

Fig. 5.3 (a) and (b) is the pulse I-V characteristics curves of the I/O and power-rail Low-C ESD clamps, respectively. These two curves are obtained by measuring the I-V relationship of the output pad and VDD pad to GND pad of the protected DA using a Tektronix 370B curve tracer.

The DC I-V characteristics curve and the pulse I-V characteristics curves can be used to obtain the operational behavior of the sole low-C ESD clamps.

Fig. 5.4 (a) and (b) is the TLP (transmission-line pulse) I-V characteristics curves of the I/O and power-rail Low-C ESD clamps, respectively. These two curves are obtained by measuring the I-V relationship of the output pad and VDD pad to GND pad of the protected DA using a TLP tester. The TLP tester setup schematic is illustrated in Fig. 5.4 (c). Its operation principle is as follow. Firstly the transmission line (TL) is charged by a high voltage source and then it generates a 100-ns current pulse into the device under test (DUT). This 100-ns current pulse simulates the HBM ESD current waveform. By increasing the TLP current step-by-step, high-current characteristics and failure points of the DUT can be quantitatively obtained. The TLP I-V relationship can be monitored from the oscilloscope. The TLP I-V characteristics curves can be used to obtain the operational behavior of the low-C ESD clamp along with the ESD detection and trigger circuits.

5.2.2 SEM Photos of the Low-C ESD Clamps

Fig. 5.5 shows the SEM photos of the observable damages of the DA with ESD

protection circuit.

It cab be seen that the PMOS of the RC-inverter, the ESD detection and trigger circuits, is failed at the drain to source region. The SCR device is in fact intact.

5.23 Operation of the Low-C ESD Clamps during ESD

From the I-V curves, it can be concluded that the SCR devices exhibit no obvious snapback in both the I/O ESD clamp and the power-rail ESD clamp. The SCR devices were turned on. Therefore, when PS-mode ESD zapping, ESD current cannot be discharged by the I/O SCR but by the upward diodes to the VDD rail. Certainly the power-rail SCR cannot discharge the ESD current since both the I/O SCR and the power-rail SCR are in the same structure. The only reasonable guess is that the ESD charges on the VDD rail can be discharged by the RC-inverter, which acts as the ESD detection and trigger circuit. This hypothesis is illustrated in Fig. 5.6 and the details are addressed as follow.

When VDD-to-VSS-mode ESD zapping, since the SCR is inactive, the ESD current is detected by the RC time constant and discharged directly by the activated PMOS of the inverter. The ESD current flows from the source to the drain of the PMOS. Finally it is discharged to the GND through the P-well resistor in the SCR structure.

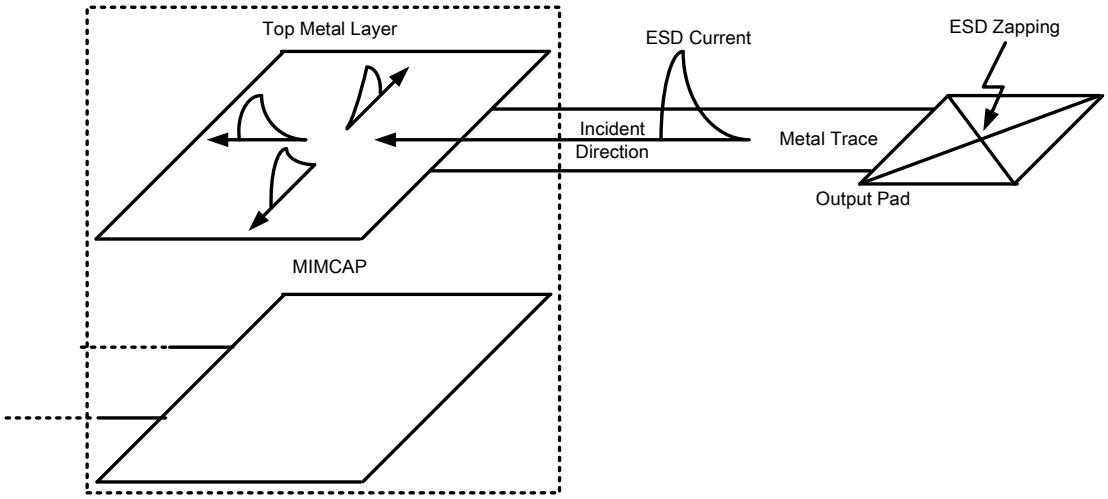
When PS-mode ESD zapping, the ESD current first goes to the VDD rail through the up-ward diodes. Then the ESD charges on the VDD rail is discharged by the same mechanism as described in the case of VDD-to-VSS-mode ESD zapping. The upward diodes consist of two diodes, and thus they contribute an additional voltage drop of about 1.6-volt (0.8-volt diode turn-on voltage drop for a single diode) for the PS-mode ESD zapping I-V curve, as compared to the VDD-to-VSS-mode ESD zapping I-V curve. The measured I-V curves confirm this hypothesis.

Two of the most fragile locations of this RC-PMOS discharging path are expected to be the gate oxide of the PMOS and NMOS of the inverter and drain-to-source discharging path of the PMOS. The gate oxide dielectric can be punched through by the strong electrical filed caused by the high voltage potential of the accumulated ESD charges. This overstressing voltage potential is about 5-V for devices of a 130-nm CMOS process. On the other hand, the ESD current flows through the PMOS channel which is basically a resistive current path. Heat is generated and finally burns through the PMOS drain-to-source channel. On both cases, the leakage current shall rise. The measured I-V curves and the SEM photos also confirm this hypothesis.

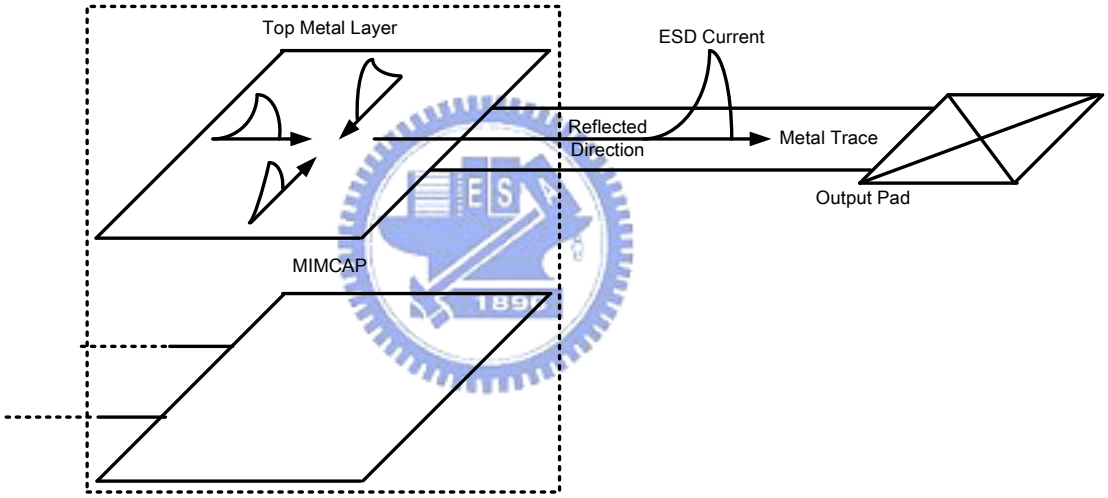
One last question remains. Why is the SCR not activated? Although there is indeed current flowing through the P-well resistor, the R_{PWELL} in Fig. 5.6 (b), the P-well resistor is too small to generate the cut-in voltage enough to activate the lateral NPN bipolar transistor. It is because the p-plus trigger nodes inserted between the P-well and N-well are so numerous that they act as numerous resistors in parallel. The effective resistance is the resistance of the P-well resistance with a single p-plus trigger nodes divided by the number of the trigger nodes. In such sense, the effective R_{PWELL} resistance is quite small. The base terminal of the lateral NPN bipolar transistor is effectively shorted to the emitter terminal, and the NPN bipolar transistor is difficult to be activated.

Therefore, it can be conclude that the trigger nodes of a SCR device cannot be placed much. Otherwise the SCR cannot be triggered on easily for that the R_{PWELL} resistance is too small to generate the required cut-in voltage to activate the NPN bipolar transistor. Once the SCR cannot activate, the PS-mode ESD current can only be discharged by the up-ward diodes and the RC-inverter (precisely speaking, the RC-PMOS- R_{PWELL}). There exists an optimal number of trigger nodes for a SCR

devices to guarantee fast and effective turning, and the whole-chip ESD protection architecture with the proposed waffle-structured SCR can bring the protected circuit maximal ESD robustness.

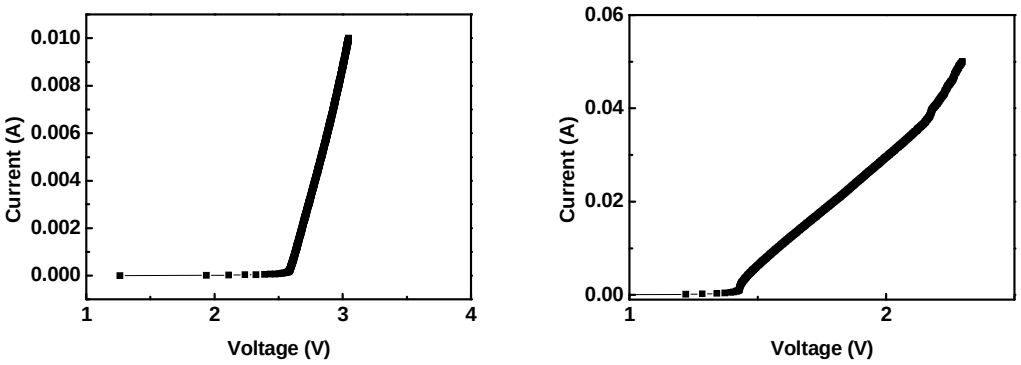


(a)



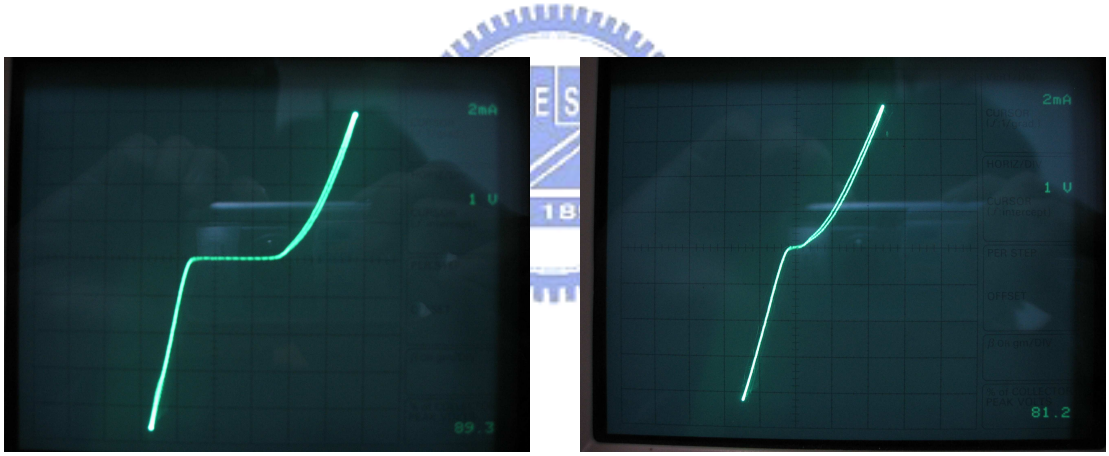
(b)

Fig. 5.1 Illustrations of the current wave propagations of (a) the incident ESD current and (b) the reflected current.



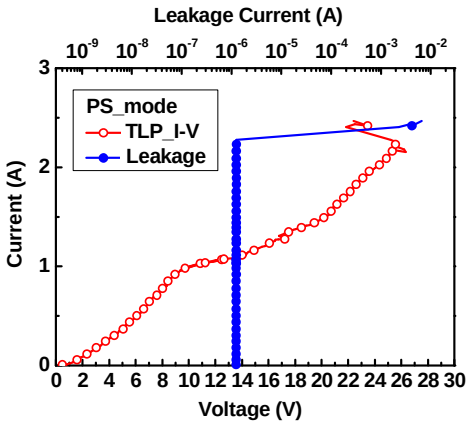
(a) (b)

Fig. 5.2 The DC I-V curves of (a) output pad to GND pad after PS-mode zapping and (b) VDD pad to GND pad after VDD-to-VSS-mode zapping.

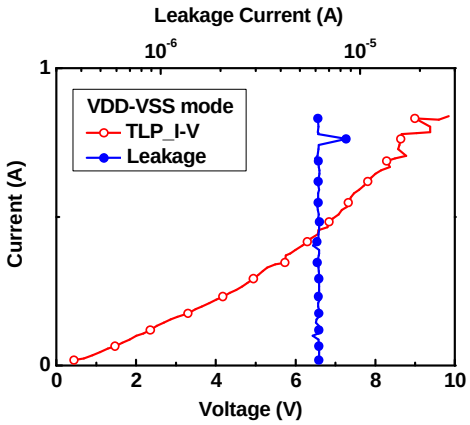


(a) (b)

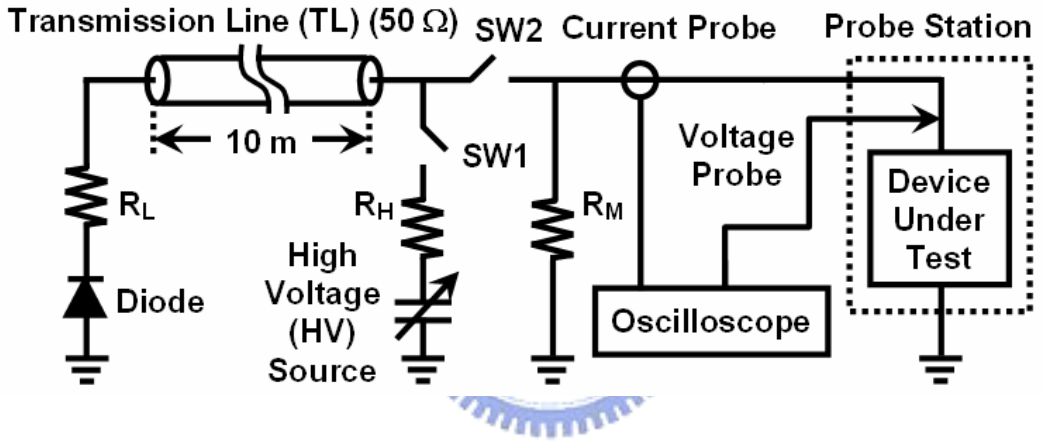
Fig. 5.3 The pulse I-V curves of (a) output pad to GND pad after PS-mode zapping and (b) VDD pad to GND pad after VDD-to-VSS-mode zapping.



(a)

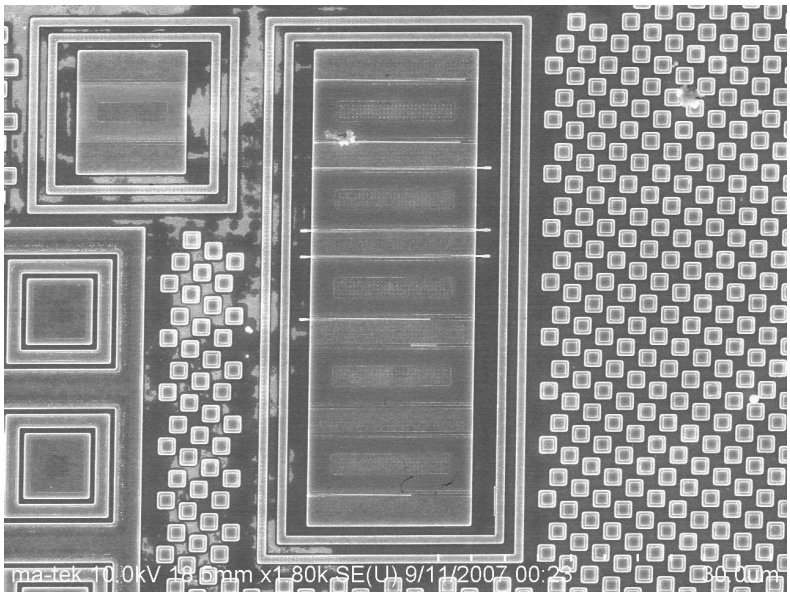


(b)

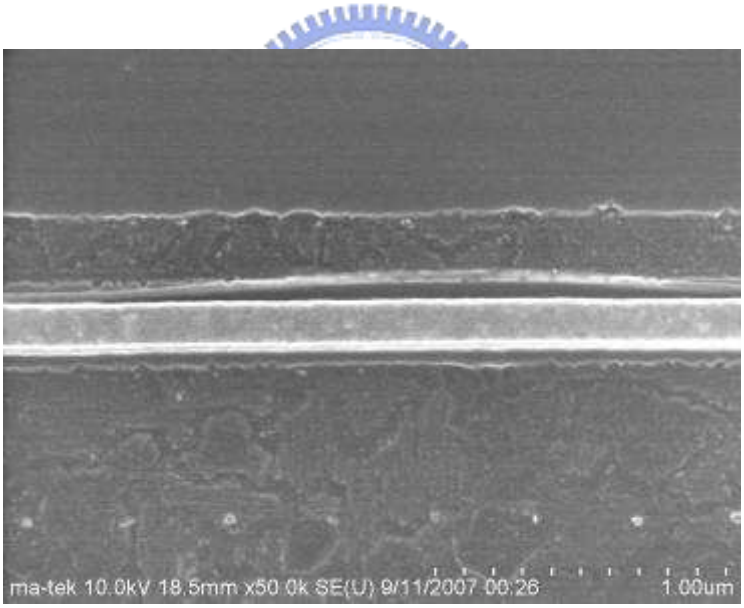


(c)

Fig. 5.4 The TLP I-V curves of (a) output pad to GND pad after PS-mode zapping, (b) VDD pad to GND pad after VDD-to-VSS-mode zapping, and (c) the TLP testing instrument set-up schematic.

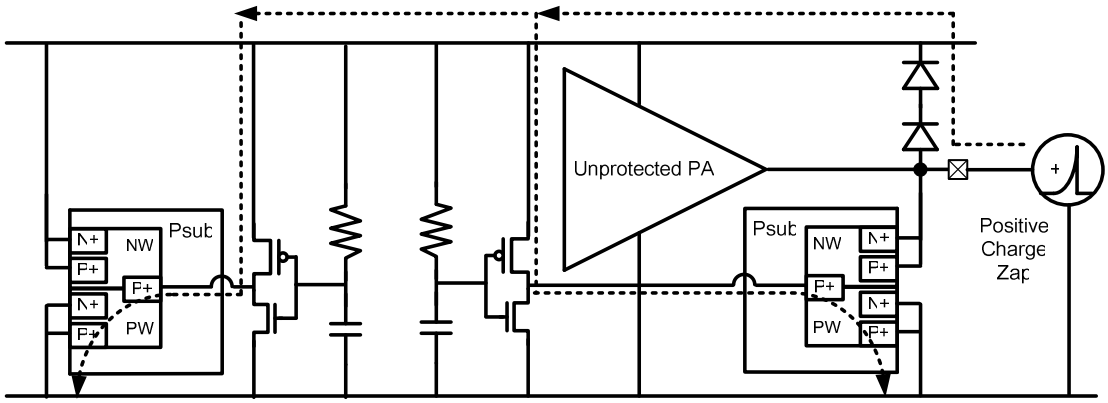


(a)

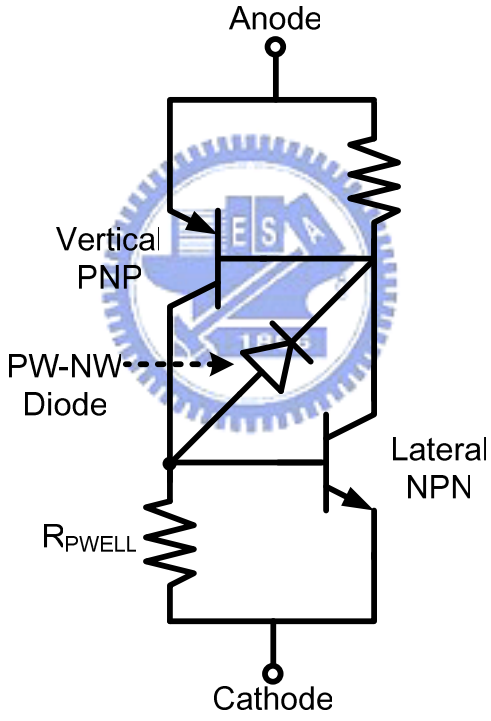


(b)

Fig. 5.5 The SEM photos of (a) the PMOS of the RC-inverter and (b) the observably damaged location of the PMOS.



(a)



(b)

Fig. 5.6 Circuit schematics of (a) the whole-chip ESD protection circuit with low-C SCR clamp for the DA and (b) the SCR device.

Chapter 6
Conclusions and Future Works

6.1 CONCLUSIONS

This thesis presents the experimental evidence that proves the urgent need of ESD protection for a RF PA. Further, for such a circuit whose performance is extremely sensitive to parasitic effects, the RF PA circuit must be co-designed with the ESD protection circuit, and novel ESD protection strategy specifically designed for a RF PA must be incorporated.

RF PA circuitry has a distinctive structure that is far different from the traditional mixed-signal I/O circuitry. The RF PA circuitry incorporates numerous passive devices in between the active device core and the output terminal pad. Therefore, traditional dc leakage current test is not enough for ESD testing failure criterion; complete RF functionality test must be utilized for the ESD testing failure criterion of a RF PA. It is proved with experimental evidence that an ESD event can damage the passive device network of the RF PA output terminal and causes degradation on the RF PA performance. In such cases only RF functionality test can reveal this kind of negative effect.

Two ESD protection strategies are proposed to provide the urgent need of ESD protection for RF PA circuitry. One is to use an inductive ESD device to distinguish an ESD event from normal RF signals. The other is to use capacitive ESD clamps but with low parasitic capacitance.

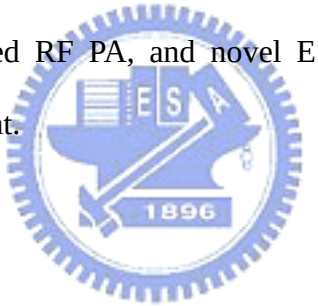
The inductive ESD device can be co-designed with the RF PA output matching

network. It can be simply an inductor shunted to ground at the RF PA output terminal. This inductor can be the low impedance discharging path for an ESD event whose power spectrum occupies the lower frequency range. It can also be co-designed to become a part of the output matching network and thus causes no negative impact on the RF PA performance. Further, a MIMCAP in series can act as a signal line blocker which blocks out the ESD current from directly penetrating into the RF PA core. Certainly this MIMCAP can also be co-designed in the output matching network, causing no degradation on the RF PA performance. This ESD protection strategy is designed and fabricated in a standard 0.13-μm CMOS process. A 3-GHz 0-dBm narrowband class-AB PA is designed and acts as the protected RF PA. The output matching network of the PA is co-designed with an inductor which acts as the inductive ESD device and a MIMCAP which acts as the signal line blocker. The measurement results verify this ESD protection strategy and reveal the truth that ESD protection technique in use indeed provide excellent ESD robustness up to 8kV HBM ESD level and 400V MM ESD level.

The low-C ESD device is a SCR with detection and trigger circuit incorporated in the whole-chip ESD protection architecture which utilizes an upward diode string to divert part of the ESD current to the power-rail and activate the detection circuit, trigger circuit, and the power-rail ESD clamp. The SCR and the diodes are in waffle-structured layout style which can maximize the discharging peripheral within a given layout area. Therefore, the waffle-structured layout style can provide maximum ESD protection capability but contributing minimum parasitic capacitance. This ESD protection strategy is designed and fabricated in a standard 0.13-μm CMOS process. A 3-to-10-GHz 0-dBm ultra-wideband class-AB distributed amplifier (DA) is designed and acts as the protected RF PA. The waffle-structured SCR and diodes are plugged to RF PA to provide ESD protection. Unprotected DAs and protected DAs are tested,

measured, and compared to understand the influence of ESD zapping. The measurement results prove that an unprotected DA cannot survive any ESD zapping. The gain and output power capability of an unprotected DA are largely degraded ever since a 1kV HBM test and a 100V MM test. It can be concluded that an unprotected RF PA may not survive any single ESD zapping; RF PA circuitry is in urgent need of ESD protection.

On the other hand, the measurement results verify the low-C ESD protection strategy and reveal the truth that this ESD protection technique in use indeed provide excellent ESD robustness up to 8kV HBM ESD level and 800V MM ESD level. The RF PA performance will certainly be degraded by the parasitic capacitance contributed by the ESD protection circuit. The ESD protection circuit needs to be co-designed with the protected RF PA, and novel ESD device with low parasitic capacitance is still being sought.



6.2 FUTURE WORKS

To further understand the effect of ESD zapping on the fabricated RF PAs and the proposed ESD protection strategies, more ESD testing needs to be carried out for further analysis.

The fabricated chips needs to be further verified under the four modes of ESD testing, namely, the PS, NS, PD, and ND modes for completion. Further, TLP testing needs to be carried out to understand the exact ESD behaviors of the ESD clamp devices. After all the ESD testing is completed, failure analysis is to be done for those chips whose RF functionality is damaged by ESD zapping; fully understanding of the ESD protection strategies can be obtained.

REFERENCE

[1] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.

[2] M.-D. Ker, W.-Y. Lo, C.-M. Lee, C.-P. Chen, and H.-S. Kao, "ESD protection design for 900-MHz RF receiver with 8-kV HBM ESD robustness," in *RFIC Symp. Dig.*, Jun. 2002, pp. 427–430.

[3] C.-P. Chang, J.-A. Hou, J. Su, C.-W. Chen, T.-S. Liou, S.-C. Wong, and Y.-H. Wang, "A high gain and low supply voltage LNA for the direct conversion application with 4-KV HBM ESD protection in 90-nm RF CMOS," *IEEE Microwave and Wireless Components Lett.*, vol. 16, no. 11, pp. 612–614, Nov. 2006.

[4] D. Linten, S. Thijs, M. Natarajan, P. Wambacq, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Donnay, and S. Decoutere, "A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1434–1442, Jul. 2005.

[5] Y. Ma and G.-P. Li, "ESD protection design considerations for InGaP/GaAs HBT RF power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 1, pp. 221–228, Jan. 2005.

[6] M.-D. Ker and K.-C. Hsu, "Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits," *IEEE Trans. Device Mater. Reliab.*, vol. 5, no. 2, pp. 235–249, Jun. 2005.

[7] M.-D. Ker and W.-J. Chang, "Overview on ESD protection design for mixed-voltage I/O interfaces with high-voltage-tolerant power-rail ESD clamp circuits in low-voltage thin-oxide CMOS technology," *Microelectronics Reliability*, vol. 47, no. 1, pp. 27–35, Jan. 2007.

[8] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Overview and design of mixed-voltage I/O buffers with low-voltage thin-oxide CMOS transistors," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 9, pp. 1934–1945, Sep. 2006.

[9] M.-D. Ker and K.-H. Lin, "Overview on electrostatic discharge protection designs for mixed-voltage I/O interfaces: design concept and circuit implementations," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 2, pp. 235–246, Feb. 2006.

[10] B. Razavi, "Challenges in portable RF transceiver design," *IEEE Circuits Devices Mag.*, vol. 12, no. 5, pp. 12–25, Sep. 1996.

[11] S. Voldman *et al.*, "Test methods, test techniques and failure criteria for

evaluation of ESD degradation of analog and radio frequency (RF) technology," in *Proc. EOS/ESD Symp.*, 2002, pp. 92–100.

[12] S. Hyvonen, S. Joshi, and E. Rosenbaum, "Combined TLP/RF testing system for detection of ESD failures in RF circuits," *IEEE Trans. Electron. Packag. Manufact.*, vol. 28, no. 3, pp. 224–230, Jul. 2005.

[13] B. Razavi, *RF Microelectronics*, NJ: Prentice-Hall, 1998.

[14] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004.

[15] M.-D. Ker, J.-J. Peng, and H.-C. Jiang, "ESD test methods on integrated circuits: an overview," *IEEE International Conference on Electronics, Circuits and Systems*, pp. 1011–1014, Sep. 2001.

[16] M.-D. Ker and K.-H. Lin, "ESD protection design for I/O cells with embedded SCR structure as power-rail ESD clamp device in nanoscale CMOS technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2329–2338, Nov. 2005.

[17] M.-D. Ker and Y.-W. Hsiao, "ESD protection design with low-capacitance consideration for high-speed/high-frequency I/O interfaces in integrated circuits," *Recent Patents on Engineering*, vol. 1, no. 2, pp. 131–145, Jun. 2007.

[18] M.-D. Ker and B.-J. Kuo, "Decreasing-size distributed ESD protection scheme for broad-band RF circuits," *IEEE Trans. Microwave Theory and Techniques*, vol. 53, no. 2, pp. 582–589, Feb. 2005.

簡歷

姓名：蒙國軒

學歷：

台北市立建國高級中學	(89 年 9 月 ~91 年 6 月)
國立交通大學電子工程學系	(91 年 9 月 ~95 年 1 月)
國立交通大學電子研究所碩士班	(95 年 2 月 ~96 年 10 月)