國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

全金屬矽化物互補式金氧半製程之矽控整流器及其在射頻電路之靜電放電防護設計與應用

SCR-BASED ESD PROTECTION DESIGNS FOR RADIO-FREQUENCY INTEGRATED CIRCUITS IN FULLY SILICIDED CMOS PROCESS

研 究 生：林 群 祐 (Chun-Yu Lin)

指導教授：柯 明 道 (Ming-Dou Ker)

中華民國九十八年七月

全金屬矽化物互補式金氧半製程之矽控整流器及其在射頻電路之靜電放電防護設計與應用

SCR-BASED ESD PROTECTION DESIGNS FOR RADIO-FREQUENCY INTEGRATED CIRCUITS IN FULLY SILICIDED CMOS PROCESS

研 究 生：林群祐　　**Student: Chun-Yu Lin**

指導教授：柯明道　　**Advisor: Ming-Dou Ker**

國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

A Dissertation
Submitted to Department of Electronics Engineering
and Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy
in
Electronic Engineering

July 2009
Hsinchu, Taiwan, Republic of China

中華民國九十八年七月

全金屬矽化物互補式金氧半製程之矽控整流器及其在射頻電路之靜電放電防護設計與應用

研究生：林群祐　　指導教授：柯明道 博士

國立交通大學電子工程學系電子研究所

摘要

在所有積體電路產品中，皆必須於量產時符合可靠度 (Reliability) 的規範，以提供該積體電路產品足夠的耐用年限。而隨著奈米級互補式金氧半製程的持續發展，靜電放電 (Electrostatic Discharge, ESD) 防護已成為積體電路產品可靠度中相當艱鉅的挑戰，大多數電子產品的故障與損壞均與遭受靜電放電轟擊有關。為避免積體電路遭受靜電放電的威脅與破壞，所有積體電路與外界接觸的銲墊 (Pad) 皆須搭配靜電放電防護設計。

無線通訊裝置中的射頻 (Radio Frequency, RF) 電路，因其連接射頻收發機與外接之濾波器或天線，因此亦需搭配靜電放電防護設計。由於射頻電路操作在數十億赫茲 (Gigahertz, GHz) 以上的工作頻率，如此高頻的工作頻率對於訊號路徑上的寄生效應有極為極嚴格的限制，靜電放電防護電路的寄生效應必須達到最小化的設計，以避免射頻電路性能的嚴重衰減。在寄生效應嚴格限制的情況下，矽控整流器 (Silicon-Controlled Rectifier, SCR) 是極為有用的靜電放電防護元件。由於在二極體 (Diode)、矽控整流器、雙載子電晶體 (BJT)、金氧半場效電晶體 (MOSFET)、或者是場氧化層電晶體 (Field Oxide Device, FOD) 等眾多的靜電放電防護元件中，矽控整流器具有面積最小、寄生效應最小、靜電放電耐受度最好的優點，並且完全相容於一般互補式金氧半製程的步驟，不需額外的光罩去遮蔽金屬矽化物 (Silicide Blocking)，尤其將它應用在先進製程中不會有閂鎖效應 (Latchup) 的問題，因此可以廣泛應用在積體電路中當作靜電放電防護元件。然而過高的觸發電壓與較慢的導通速度，使得矽控整流器在實際應用上必須搭配有

效地低電壓觸發與高效率導通之設計。矽控整流器基本特性是由電流觸發而導通的元件，所以當有一觸發電流施加於矽控整流器的基體時，矽控整流器便可很快地經由正回授再生機制 (Positive-Feedback Regeneration Mechanism) 觸發進入導通狀態。

搭配矽控整流器的射頻電路之靜電放電防護設計是本論文的研究主題，本論文的章節包括：(1) 使用交叉耦合 (Cross Couple) 的矽控整流器之差動式低雜訊放大器 (Low-Noise Amplifier, LNA) 設計、(2) 超低寄生電容的矽控整流器設計、(3) 搭配超低寄生電容的矽控整流器之超寬頻功率放大器 (Power Amplifier, PA)、(4) 應用在射頻電路與靜電放電防護電路共同設計之寄生電容模型、(5) 利用矽控整流器設計之可耐高工作電壓以及低漏電之靜電放電箝制電路。

本論文第二章針對一種射頻窄頻前端電路與靜電放電防護電路共同設計。本章使用 130 奈米互補式金氧半製程設計一個工作於 5 GHz 的差動式低雜訊放大器，並探討差動式低雜訊放大器接點對接點 (Pin to Pin) 之靜電放電耐受度。新提出的靜電放電防護設計於兩個差動輸入銲墊間使用交叉耦合的矽控整流器，除了可提供單一輸入銲墊至電源線與接地線的靜電放電防護外，更可提供兩個差動輸入銲墊間的接點對接點模式靜電放電防護功能。此設計的人體放電模式 (Human Body Model, HBM) 與機械放電模式 (Machine-Model, MM) 靜電放電耐受度分別為 3.5 kV 與 300 V。相關的射頻性能以及靜電放電耐受度皆於第二章內比較與討論。

第三章藉由改變矽控整流器的元件佈局方式以降低寄生效應。在矽控整流器中使用方塊狀 (Waffle) 之新型佈局結構，可在相同晶片佈局面積下提供最大靜電放電路徑周長，因此可在最小寄生電容的前提下，提供最高的靜電放電防護能力。換句話說，方塊狀之矽控整流器可降低元件本身的寄生電容值。本研究於 0.18 微米互補式金氧半製程中實現此新型設計，並且不需增加元件和其他成本，故十分適合應用於射頻電路之靜電放電防護設計。

利用新提出之方塊狀矽控整流器，第四章將其應用於射頻功率放大器之靜電放電防護電路。本章使用 130 奈米互補式金氧半製程實現此射頻電路，實驗證明此靜電放電防護策略可有效地提供防護等級超過 8-kV 人體放電模式之靜電放電轟擊測試、與 800-V 機械放電模式之靜電放電轟擊測試。實驗結果亦證明，靜電放電轟擊確實對射頻功率放大器的射頻操作效能有極大的影響，射頻功率放大器極需靜電放電防護設計，否則無法於靜電放電轟擊下存活。

隨著射頻電路工作頻率持續升高，靜電放電防護電路的寄生效應也愈來愈難以掌

握，因此，需要將電路中所使用的元件模型建立起來，才能更有效地控制靜電放電防護電路的寄生特性。本論文第五章建立起矽控整流器在高頻操作時的元件模型，以便利用射頻電路與靜電放電防護電路共同設計的方式，設計出具有良好射頻效能以及優異靜電放電防護能力的射頻積體電路。除了靜電放電防護元件以外，銲墊也會在訊號路徑上對射頻訊號造成負面影響。本章針對一種具有低電容值的銲墊進行研究，利用其等效電路模型進一步提出低損耗 (Loss) 設計，並於 65 奈米互補式金氧半製程中實現此設計。實驗結果顯示，銲墊的等效電容可於特定頻段內大幅降低，同時訊號損耗也可降低，因此可避免影響射頻電路之性能。

電源箝制靜電放電防護電路 (Power-Rail ESD Clamp Circuit) 是達成積體電路產品全晶片靜電放電防護極為重要的設計，本論文第六章提出了新型的可耐高工作電壓以及低漏電之靜電放電箝制電路。本章使用 65 奈米互補式金氧半製程實作，在此可耐高工作電壓之靜電放電箝制電路中，所有電晶體都是利用低壓元件來實現，可以安全地偏壓在兩倍工作電壓下而不會有閘極氧化層的可靠度問題，並且不需使用低漏電製程即可達成降低漏電的目標。由實驗結果可知，此電路擁有極高的靜電放電能力，而且在正常操作的情況下只有 100-nA 等級的漏電流，因此，本靜電放電箝制電路十分適合應用在系統單晶片 (System-on-a-Chip, SoC) 之混合電壓輸入輸出界面 (Mixed-Voltage I/O Interfaces)。

第七章總結本論文的研究成果，並提出數個接續本論文研究方向的研究題目。本論文所提出的各項新型設計，皆已搭配實驗晶片加以驗證。此外，本研究有數篇國際期刊與國際研討會論文發表，並有數項創新設計已提出中華民國及美國專利申請。

SCR-BASED ESD PROTECTION DESIGNS FOR RADIO-FREQUENCY INTEGRATED CIRCUITS IN FULLY SILICIDED CMOS PROCESS

Student: Chun-Yu Lin **Advisor: Dr. Ming-Dou Ker**

Department of Electronics Engineering and Institute of Electronics

National Chiao-Tung University

Abstract

In order to be safely used and provide moderate life time, all microelectronic products must meet the reliability specifications during mass production. Electrostatic discharge (ESD), which was one of the most important reliability issues in the integrated circuit (IC), must be taken into consideration during the design phase of all IC products. All pads which connect the IC and the external world, including the input/output (I/O) pads, VDD pads, and VSS pads, need to be equipped with ESD protection circuits to provide effective ESD protection for the IC. Since the radio-frequency (RF) front-end circuits in wireless communication devices connect the RF transceiver to the external antenna or band-select filter, they must need ESD protections. However, the ESD protection devices at the I/O pads inevitably cause parasitic effects on the signal path. For the RF front-end circuits operating in the frequency band from several gigahertzes to tens of gigahertz, they have the strict limitations of the parasitic effects on the signal path in such high operating frequency. This situation leads to the challenge in ESD protection design for RF circuits, which is to achieve the highest ESD robustness with the smallest performance degradation. In other words, the parasitic effects of the ESD protection devices need to be minimized. Moreover, the evolution of CMOS process increases the difficulty of ESD protection design. As CMOS process is continuously scaled down, the power-supply voltage is decreased and the gate oxide becomes thinner, which leads

to the reduced gate-oxide breakdown voltage of MOS transistor. However, ESD was not scaled down with the CMOS technology, so the MOS transistors with thinner gate oxide are more vulnerable to ESD. The aforementioned design challenges form the motivation of this dissertation. The research topics of this dissertation including: (1) ESD protection design on a 5-GHz differential low-noise amplifier with cross-coupled SCR, (2) optimization on SCR device with low capacitance for RF ESD protections, (3) ESD protection design on an ultra-wideband power amplifier with waffle-structured SCR, (4) modeling parasitic capacitance for matching network co-designed in RF ICs, and (5) high-voltage-tolerant ESD clamp circuit by using only low-voltage devices with low standby leakage in nanoscale CMOS process.

In chapter 2, the pin-to-pin ESD protection design on a 5-GHz differential LNA is proposed. The 5-GHz differential LNA is implemented in a 130-nm CMOS process. The new ESD protection scheme for differential input pads is realized with the cross-coupled SCR. This ESD protection scheme achieves 3.5-kV HBM and 300-V MM ESD levels, respectively.

SCR realized in waffle layout structure is proposed to improve ESD current distribution efficiency for ESD protection and to reduce the parasitic capacitance in chapter 3. The proposed waffle-structured SCR has been verified in a 0.18-μm CMOS process. The waffle layout structure of SCR can achieve smaller parasitic capacitance under the same ESD robustness. With smaller parasitic capacitance, the degradation on RF circuit performance due to ESD protection devices can be reduced. The proposed waffle SCR with low parasitic capacitance is suitable for on-chip ESD protection in RF ICs. Besides, the desired current to trigger on the SCR device with waffle layout structure and its turn-on time has also been investigated in silicon chip.

In chapter 4, the waffle-structured SCR is applied to an ultra-wideband (UWB) RF power amplifier (PA). The waffle-structured SCR is designed with ESD detection and trigger circuit to provide the best ESD protection capability while contributing minimum parasitic capacitance to the RF PA in a 130-nm CMOS process. The measurement results have verified the effectiveness of the proposed ESD protection strategy and proved that this ESD protection technique indeed provides excellent ESD robustness of up to 8kV HBM ESD level and 800V MM ESD level.

As the operating frequencies of RF front-end circuits are increased, on-chip ESD protection designs for RF applications are more challenging, and they should be designed more carefully. In chapter 5, the small-signal circuit model of waffle-structured SCR has been presented and proved in silicon. The measured parasitic capacitances well agree with the

simulated capacitances. The RF circuits can be well co-designed with the presented small-signal model to eliminate the negative impacts from ESD protection SCR on RF performances. Besides, the optimized design of the bond pad for RF applications was also investigated. The experimental results in a 65-nm CMOS process have proven that the bond pad capacitance and insertion loss can be successfully reduced by the optimized bond pad structure. The small-signal circuit model of the optimized bond pad has also been presented for RF circuit designs.

The efficient power-rail ESD clamp circuit must be included into the RF ICs to reduce the dimensions of ESD devices connected to the I/O pad. In chapter 6, the new 2×VDD-tolerant ESD clamp circuit by using only low-voltage devices with low standby leakage current and high ESD robustness for system-on-a-chip (SoC) applications with mixed-voltage I/O interfaces has been successfully designed and verified in a 65-nm CMOS process. The 2×VDD-tolerant ESD clamp circuit can operate without gate-oxide reliability issue, and the leakage current is only in the order of 100 nA under normal circuit operating condition. Besides, there is no latchup concern in this design. The new ESD clamp circuit by using only low-voltage devices with very low standby leakage current and high ESD robustness is the useful circuit solution for on-chip ESD protection design with mixed-voltage I/O interfaces in SoC applications.

In this dissertation, several novel designs have been proposed in the aforementioned research topics. Measured results of the fabricated test chips have demonstrated the performance improvement. The achievements of this dissertation have been published or submitted to several international journal and conference papers. Several innovative designs have been applied for patents.

Acknowledgment

在交通大學電子研究所的碩博士班生涯中，首先要感謝我的指導教授柯明道教授三年多來的耐心指導與鼓勵，讓我能順利完成博士學業。除了專業領域上的訓練，柯教授認真且積極的研究態度與明快且嚴謹的處事原則，讓我學得如何快速解決問題、有效率地處理各項事務、並交出高水準成果的正確態度與方式。作研究的過程雖然備感艱辛，但培養的能力將造就無可取代的價值。柯教授為研究群同學爭取的許多福利，更讓人感念在心。此外，還要感謝實驗室中另外三位教授：吳重雨校長、吳介琮教授、陳巍仁教授給我的指導與建議。

感謝交通大學吳重雨校長、晶焱科技姜信欽博士、奇景光電陳東暘博士、工業技術研究院吳文慶博士、中央大學邱煥凱教授、交通大學蘇朝琴教授在百忙之中抽空擔任我的口試委員，並給予珍貴的指導與建議，讓此博士論文更加完整。

感謝任職於聯華電子的唐天浩先生、黃新言先生、王暢資先生，與任職於智原科技的蔡富義先生、彭彥華先生，鼎力協助實驗晶片下線與研究工作進行，使本論文的研究成果得以成功驗證，並順利發表於國際期刊與國際研討會。

感謝實驗室的前輩林昆賢博士、陳世倫博士、許勝福博士、張瑋仁博士、陳榮昇博士、蕭淵文博士、陳世宏博士、顏承正博士、李健銘學長、郭秉捷學長、王資閔學長、陳穩義學長、陳志豪學長、賴泰翔學長、黃俊學長、王文傑博士、黃祖德學長、盧台祐學長、黃鈞正學長，以及蒙國軒、邱柏硯、陸亭州、竹立煒、蔡惠雯、莊介堯、黃曄仁、林彥良、許哲綸、溫詠儒、張堂龍等同學與學弟妹們在研究與生活上的協助與扶持。此外，感謝實驗室助理卓慧貞小姐在行政事務上的許多協助。

最後，由衷感謝親愛的父親林宏聲先生、母親鄭瓊如女士、哥哥林群傑先生，以及女友一路走來無悔的相伴。由於親人的鼓勵、支持、陪伴與照顧，讓我能順利完成學業。感謝所有幫助我、陪伴我一同成長的師長、朋友、學長姊、同學、學弟妹們，願大家平安喜樂。

林 群 祐
誌於竹塹交大
九十八年 夏

Contents

Table Captions

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

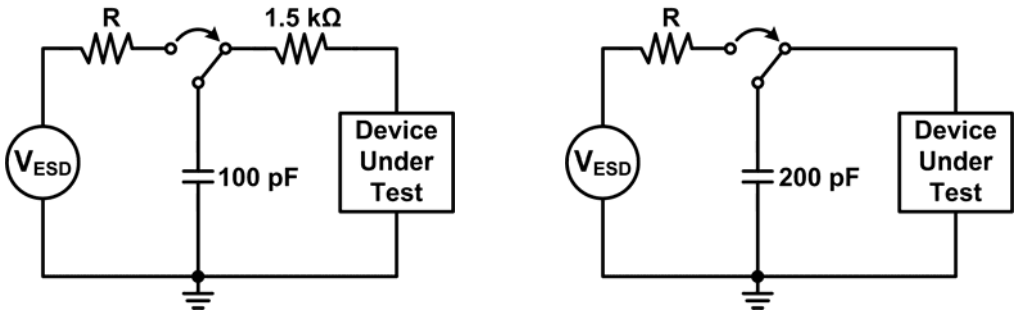
Chapter 1

Introduction

In this chapter, the background and the organization of this dissertation are discussed. First, the electrostatic discharge (ESD) protection designs on radio-frequency (RF) circuits in fully silicided complementary metal-oxide-semiconductor (CMOS) processes are introduced. Then, the organization of this dissertation is described.

1.1. Background of ESD Protection Design for Radio-Frequency Circuits

RF circuits have been widely designed and fabricated in CMOS processes due to the advantages of high integration and low cost for mass production. ESD, which has become one of the most important reliability issues in IC products, must be taken into consideration during the design phase of all ICs [1]-[4], including the RF front-end circuits. Without ESD protection circuits at all I/O pads, the RF performance of a wireless transceiver can be easily damaged by ESD stresses, because RF front-end circuits are always fabricated in advanced CMOS processes. Usually the I/O pads are connected to the gate terminal of MOS transistor or silicided drain/source terminal, which leads to a very low ESD robustness if no ESD protection design is applied to the I/O pad. Once the RF front-end circuit is damaged by ESD, it can not be recovered and the RF functionality is lost. Therefore, on-chip ESD protection circuits must be provided for all I/O pads in ICs. Two common chip-level ESD test standards are human-body-model (HBM) and machine-model (MM) ESD test standards [5], [6]. HBM and MM ESD tests are used to evaluate the ESD robustness of the IC when it is touched by the charged human body or charged machine. The equivalent circuits of HBM and MM ESD tests are shown in Figs. 1.1(a) and 1.1(b), respectively. In order to protect the internal circuits against ESD stresses, ESD protection circuits must be provided at all I/O pads. Fig. 1.2 shows the concept of whole-chip ESD protection design.



(a) (b)

Fig. 1.1. Equivalent circuits of (a) HBM, and (b) MM, ESD tests.

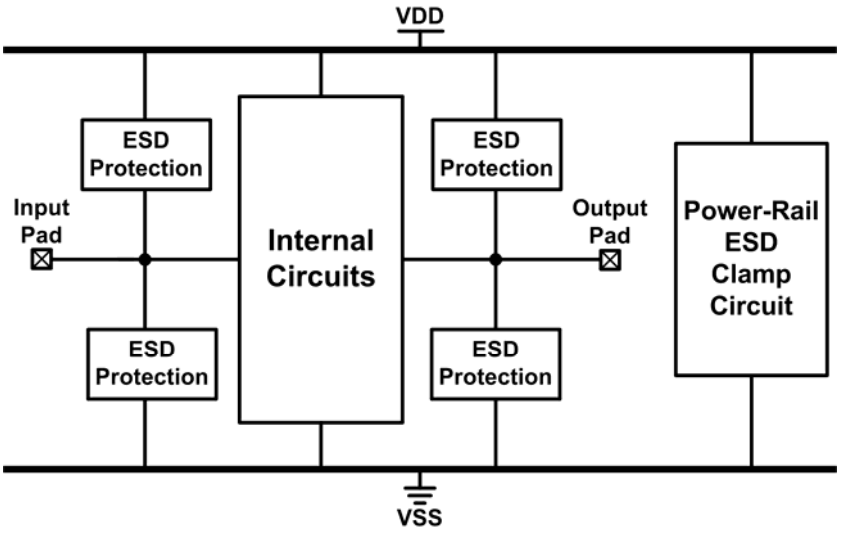


Fig. 1.2. Typical design of on-chip ESD protection circuits in CMOS ICs.

Fig. 1.3 shows the ESD-test pin combinations. ESD stresses may have positive or negative voltages on an I/O pin with respect to the grounded VDD or VSS pin. The typical ESD specifications for commercial IC products in HBM and MM are 2 kV and 200 V, respectively. For comprehensive ESD verification, the pin-to-pin ESD stresses and VDD-to-VSS ESD stresses had also been specified to verify the whole-chip ESD robustness, which are shown in Figs. 1.4 and 1.5, respectively.

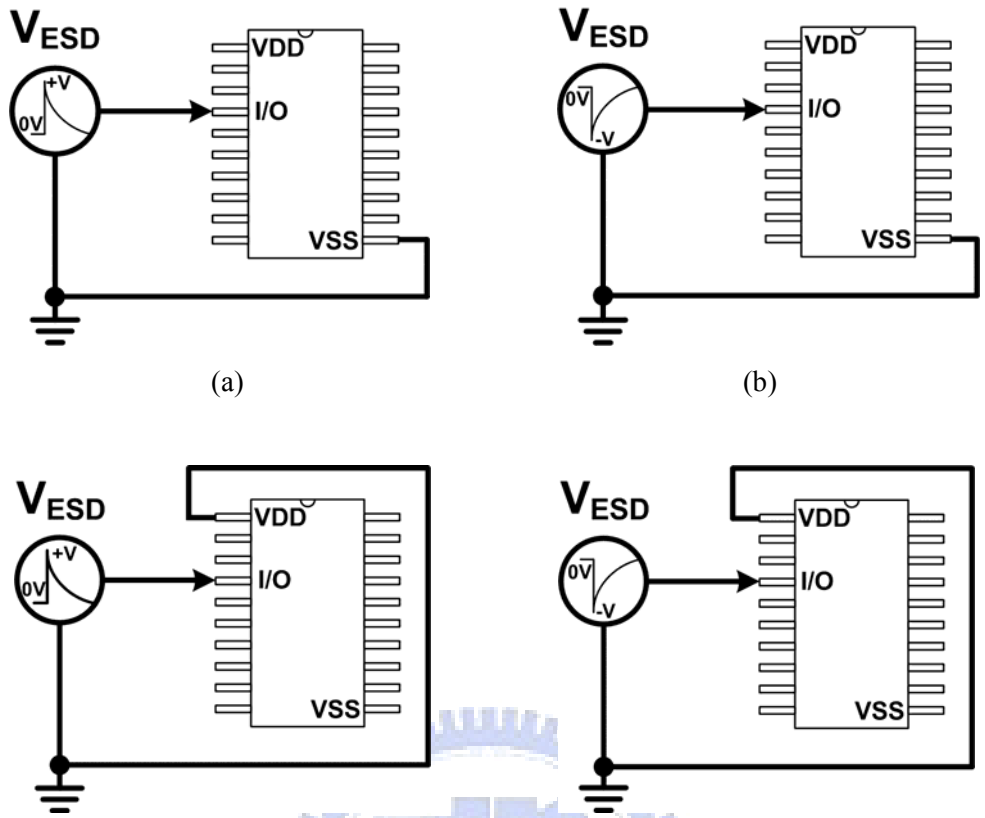


Fig. 1.3. ESD-test pin combinations: (a) positive-to-VSS mode (PS-mode), (b) negative-to-VSS mode (NS-mode), (c) positive-to-VDD (PD-mode), and (d) negative-to-VDD (ND-mode).

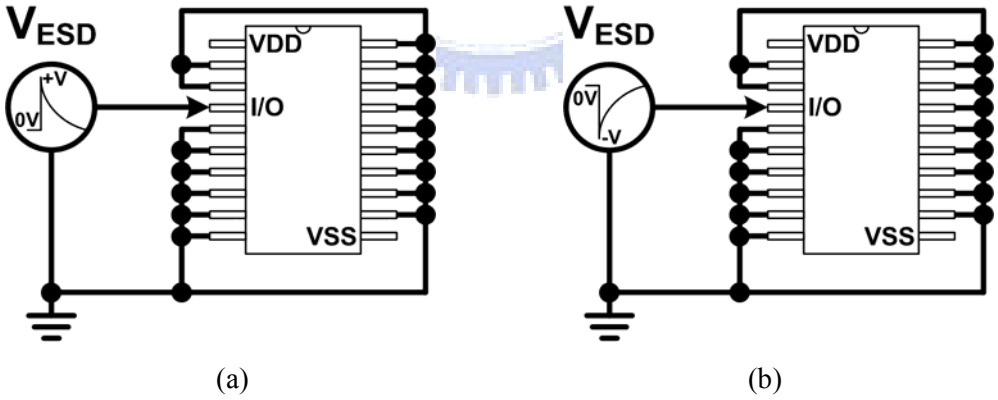
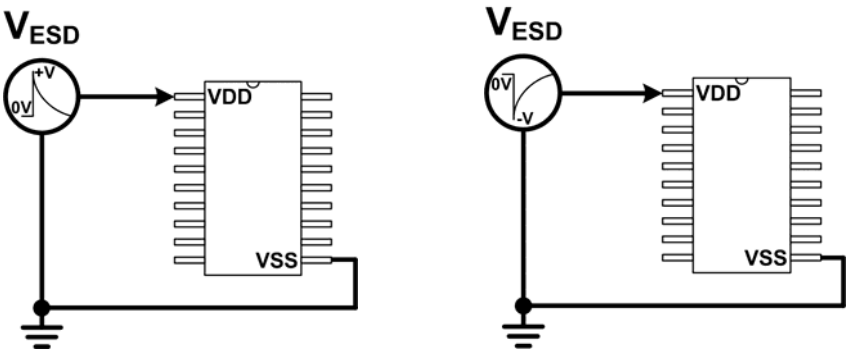


Fig. 1.4. Pin-to-pin ESD tests: (a) positive mode, and (b) negative mode.



(a) (b)

Fig. 1.5. VDD-to-VSS ESD tests: (a) positive mode, and (b) negative mode.

The typical on-chip double-diode ESD protection scheme is shown in Fig. 1.6, which two ESD diodes at I/O pad are co-designed with the power-rail ESD clamp circuit to prevent internal circuits from ESD damage [7]. In Fig. 1.6, a P+/N-well diode (D_P) and an N+/P-well diode or an N-well/P-substrate diode (D_N) are placed at input pad or output pad. When the D_P and D_N are under forward-biased condition, they can provide discharge paths from I/O pad to VDD and from VSS to I/O pad, respectively.

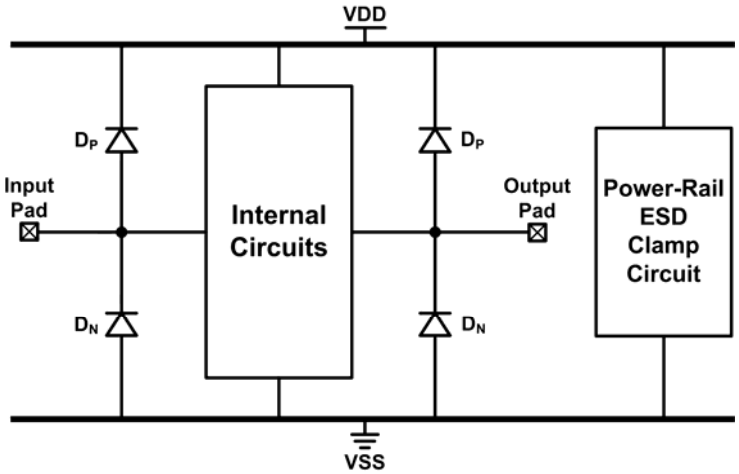
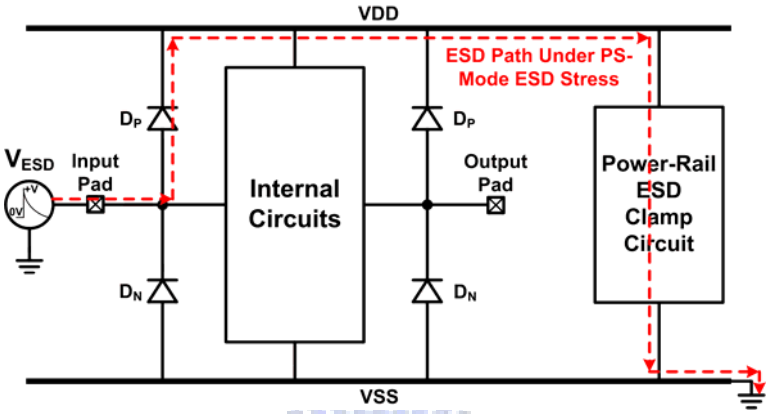


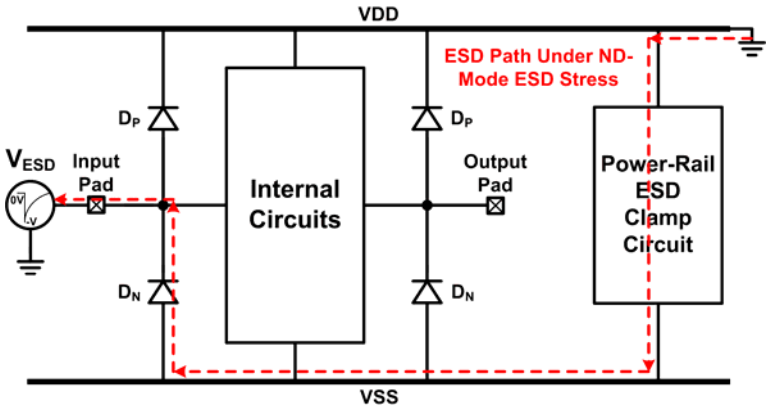
Fig. 1.6. Typical double-diode ESD protection scheme.

Under positive-to-VDD mode (PD-mode) and negative-to-VSS mode (NS-mode) ESD stresses, ESD current is discharged through the forward-biased D_P and D_N, respectively. To avoid the ESD diodes from being operated under breakdown condition during positive-to-VSS mode (PS-mode) and negative-to-VDD mode (ND-mode) ESD stresses, which results in a substantially lower ESD robustness, the power-rail ESD clamp circuit is used between VDD and VSS to provide ESD current paths between the power rails [8]. Thus,

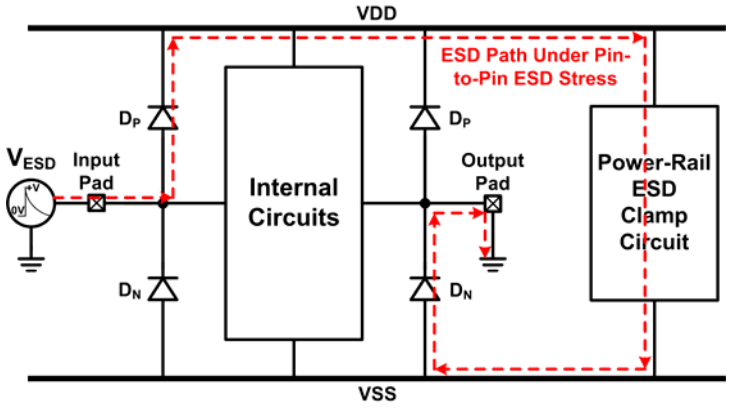
ESD current is discharged from the I/O pad through the forward-biased D_P to VDD, and discharged to the grounded VSS pin through the turn-on efficient power-rail ESD clamp circuit during PS-mode ESD stresses, as shown in Fig. 1.7(a). Similarly, ESD current is discharged from the VDD pin through the turn-on efficient power-rail ESD clamp circuit and the forward-biased D_N to the I/O pad during ND-mode ESD stresses, as shown in Fig. 1.7(b).



(a)



(b)



(c)

Fig. 1.7. ESD current paths in the typical double-diode ESD protection scheme under (a) PS-mode, (b) ND-mode, and (c) pin-to-pin, ESD stresses.

During pin-to-pin ESD stresses, ESD current flows from the zapped I/O pad through the forward-biased D_P, the power-rail ESD clamp circuit, and the forward-biased D_N to the grounded I/O pad, as shown in Fig. 1.7(c). Under VDD-to-VSS ESD tests, ESD current flows through the power-rail ESD clamp circuit between VDD and VSS. Since the power-rail ESD clamp circuit works independently between VDD and VSS, its parasitic effects do not have any impact on the internal circuits. With the turn-on efficient power-rail ESD clamp circuit, the ESD diodes can be assured to be operated in the forward-biased condition under all ESD test modes, which leads to higher ESD robustness.

Although using power-rail ESD clamp circuit between VDD and VSS does not cause any effect on the internal circuits, applying ESD protection devices at the I/O pads inevitably introduce some negative impacts to circuit performance due to their parasitic effects. The main parasitic effect caused by ESD protection devices which deteriorates the high-frequency performance is the parasitic capacitance. Since the input signal swing is small at the RF input pad, it is sensitive to the shunt parasitic capacitance of ESD protection devices. Therefore, the parasitic capacitance of the ESD protection device at the RF input pad is strictly limited. For the RF transmitter, the devices in the output stage are implemented with large dimensions to transmit the output signals with large enough signal power. With proper design, the devices in the RF output stage can be used to protect the RF output pad against ESD stresses. Thus, ESD protection design for the input pad of the RF receiver is more challenging than that for the output pad of the RF transmitter.

A typical request on the maximum loading capacitance of ESD protection device for a 2-GHz RF input pin was specified as only ~200 fF, which includes the parasitic capacitances of bond pad and ESD protection device [9]. Recently, the negative impacts of ESD protection devices to RF circuit performance had been investigated [10], [11], which had demonstrated that the RF performance such as power gain and noise figure are significantly degraded by the parasitic capacitance of ESD protection devices. The impacts become more serious as the operating frequency of RF front-end circuits increases. Thus, the parasitic capacitance of ESD protection device must be minimized in ESD protection design for high-frequency applications. Generally, ESD protection circuits cause RF performance degradation with several undesired effects, which are will be discussed in the following.

Parasitic capacitance is one of the most important design considerations for RF ICs. Conventional ESD protection devices with large dimensions have the parasitic capacitance which is too large to be tolerated for RF front-end circuits. As shown in Fig. 1.8, the parasitic

capacitance of ESD protection devices causes signal loss from the pad to ground. Moreover, the parasitic capacitance also changes the input matching condition. Consequently, the noise figure is deteriorated and the power gain is decreased.

Noise factor is one of the most important merits for RF receivers. Since the RF receiver is a cascade of several stages, the overall noise factor of the RF receiver can be obtained in terms of the noise factor and power gain of each stage in the receiver. For example, if there are m stages cascaded in the RF receiver, the total noise factor of the RF receiver can be expressed as [12]

$$F_{total} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_{p1}} + \cdots + \frac{F_m - 1}{G_{p1} \cdots G_{p(m-1)}} \tag{1.1}$$

where F_i and G_{pi} are the noise factor and the power gain of the i-th stage, respectively. According to (1.1), the noise factor contributed by the first stage is the dominant factor to the total noise factor of the RF receiver (F_{total}). With the ESD protection circuit added at the input pad to protect the RF receiver IC against ESD damages, the ESD protection circuit becomes the first stage in the RF receiver IC, which is shown in Fig. 1.9. For simplicity, only the first two stages, which are the ESD protection circuit and the low-noise amplifier (LNA), are taken into consideration, as shown in Fig. 1.10. The overall noise factor (F_{LNA_ESD}) of the LNA with ESD protection circuit is

$$F_{LNA\_ESD} = F_{ESD} + \frac{F_{LNA} - 1}{G} \tag{1.2}$$

where G is the power gain of the LNA, and F_{ESD} and F_{LNA} denote the noise factors of the ESD protection and LNA circuits, respectively. Thus, the noise factor of the ESD protection circuit must be minimized, because it directly increases the total noise factor of the RF receiver and the increased noise factor can not be suppressed by the power gains of succeeding stages. Moreover, the signal loss due to the ESD protection circuit would also cause power gain degradation in RF circuits.

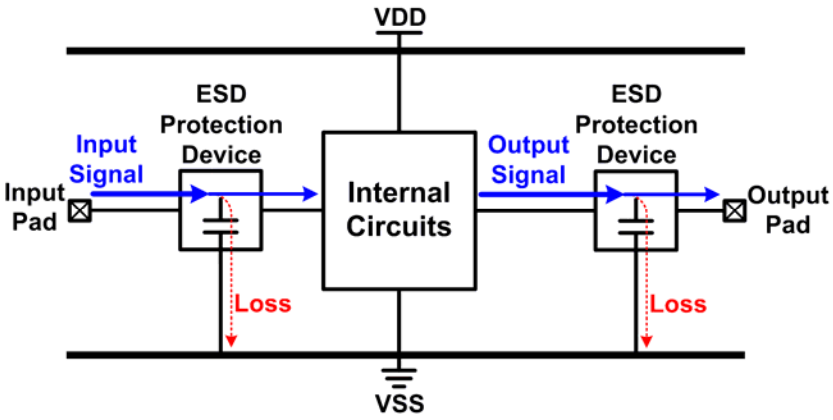


Fig. 1.8. Signal loss at input and output pads of IC with ESD protection devices.

Another negative impact caused by the ESD protection circuit is the input impedance mismatching, which is particularly critical for narrow band RF circuits. With the ESD protection circuit added at the input node, the original input matching condition is changed by the parasitic capacitance from the ESD protection circuit. As a result, the center frequency of the narrow band RF circuit is shifted and the power gain is decreased due to impedance mismatching. The impedance mismatching due to ESD protection devices can be mitigated by co-designing the ESD protection circuit and the input matching network. With the co-design of ESD protection scheme and input matching network, the operating frequency can be tuned to the desired frequency. However, the noise figure is definitely increased after ESD protection circuit is added because more devices indicate more noise sources.

Besides the impacts caused by ESD protection device on RF front-end circuits, the parasitic capacitance of the ESD protection device causes signal loss from the pad to ground, which decreases the signal swings. Moreover, RC delay is another impact caused by the ESD protection circuit. With the ESD protection circuit added to the input and output pads, the parasitic capacitance and parasitic resistance from the ESD protection device and the interconnection introduce RC delay to the input and output signals. Thus, the rising and falling time of the signals at the I/O pads with ESD protection become longer.

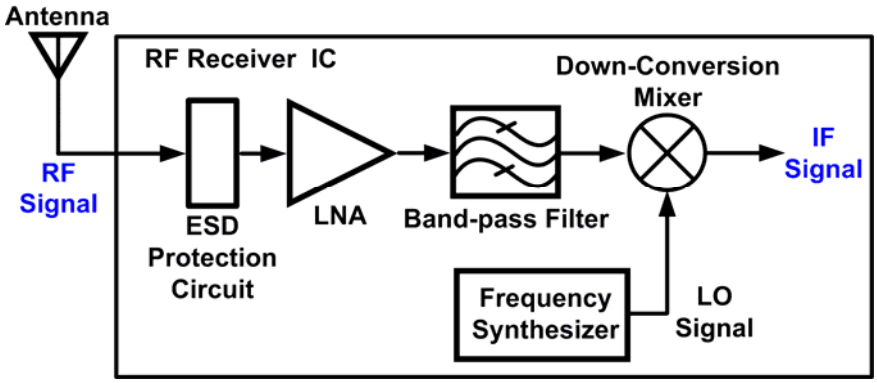


Fig. 1.9. Block diagram of an ESD-protected RF receiver.

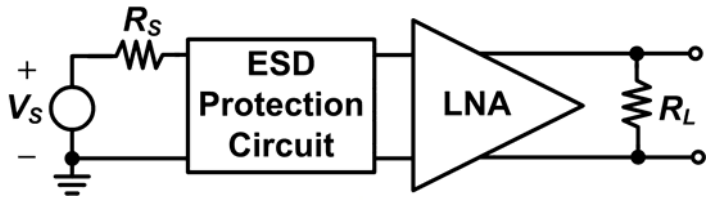


Fig. 1.10. Block diagram of an LNA with ESD protection circuit. V_S, R_S, and R_L denote the source voltage, source resistance, and load resistance, respectively.

In addition to parasitic capacitance, the requirements of ESD protection device characteristics under ESD stresses introduce some design considerations. To provide effective ESD protection, the voltage across the ESD protection device during ESD stresses should be carefully designed. First, the trigger voltage and holding voltage of ESD protection device must be designed lower than the gate-oxide breakdown voltage of MOS transistors to prevent the internal circuits from damage before the ESD protection device is turned on during ESD stresses. Second, the trigger voltage and holding voltage of the ESD protection device must be higher than the power-supply voltage of the IC to prevent the ESD protection devices from being mis-triggered under normal circuit operating conditions. Moreover, the turn-on resistance of ESD protection device should be minimized in order to reduce the joule heat generated in the ESD protection device and the voltage across the ESD protection device during ESD stresses. As CMOS process is continuously scaled down, the power-supply voltage is decreased and the gate oxide becomes thinner, which leads to reduced gate-oxide breakdown voltage of MOS transistor. Typically, the gate-oxide breakdown voltage is decreased to only ~5 V in a 65-nm CMOS process with gate-oxide thickness of ~15 Å. As a result, the ESD design window, defined as the difference between the gate-oxide breakdown voltage of the MOSFET and the power-supply voltage of the IC, becomes narrower in nanoscale CMOS technologies [13]. Furthermore, ESD protection circuits need to be quickly

turned on during ESD stresses in order to provide efficient discharge paths in time. In summary, ESD protection design becomes more challenging in nanoscale CMOS technologies.

1.2. Review of RF ESD Protection Design Techniques

To mitigate the performance degradation due to ESD protection devices, circuit design techniques had been used to reduce the parasitic capacitance from the ESD protection device. In this section, the ESD protection designs in standard CMOS processes are reviewed.

1.2.1. Stacked ESD Protection Devices

Fig. 1.6 has show the conventional double-diode ESD protection design for RF frond-end circuits; however, it is only suitable for small ESD protection devices [14]. The device dimensions of ESD diodes should be decreased to reduce the parasitic capacitance at I/O pad, and then the performance degradation caused by the parasitic capacitances from the ESD diodes could be reduced. However, ESD robustness needs to be maintained, so the minimum device dimensions of ESD diodes can not be shrunk unlimitedly. In order to further reduce the parasitic capacitance from ESD diodes without sacrificing ESD robustness, the ESD diodes in stacked configuration had been proposed, as shown in Fig. 1.11 [15], [16]. The overall equivalent parasitic capacitance will theoretically becomes C_{ESD}/n, where C_{ESD} is the parasitic capacitance of each ESD protection device and n ESD protection devices are stacked. Thus, more stacked ESD devices lead to the more significant parasitic capacitance reduction. Besides reducing parasitic capacitance, using the stacked configuration can also reduce the leakage current of ESD diodes under normal circuit operating conditions. Although stacked ESD protection devices can reduce the parasitic capacitance and leakage current, this technique is adverse to ESD protection because the overall turn-on resistance and the voltage across the stacked ESD protection devices during ESD stresses were increased as well.

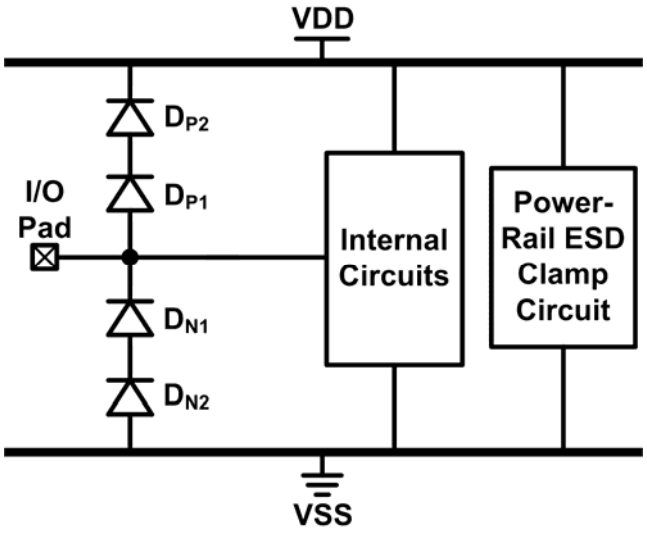


Fig. 1.11. Stacked ESD protection devices to reduce the parasitic capacitance.

1.2.2. Parallel LC Resonator

This technique was also called the impedance cancellation, which was composed of a resonant with the parallel inductor and capacitor. In such a resonator, the resonant frequency (ω_o) is

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{1.3}$$

where L and C denote inductance and capacitance, respectively. An ideal parallel LC resonator and the simulated S_{21}-parameters under different frequencies are shown in Fig. 1.12. The signal loss at the resonant frequency is ideally zero, which means that the equivalent capacitance at the resonant frequency is zero. Based on this concept, the ESD protection circuit with a parallel inductor had been proposed, as shown in Fig. 1.13 [17]-[21]. Using the inductance of L_1, it was designed to resonate with the parasitic capacitance of the ESD protection device at the operating frequency of the RF front-end circuit. With the parallel LC network resonating at the operating frequency, the shunt impedance of the resonator becomes very large, which can effectively suppress signal loss. Therefore, the ESD protection design using parallel LC resonator can mitigate the impacts on RF performances for circuits operating in a narrow frequency band.

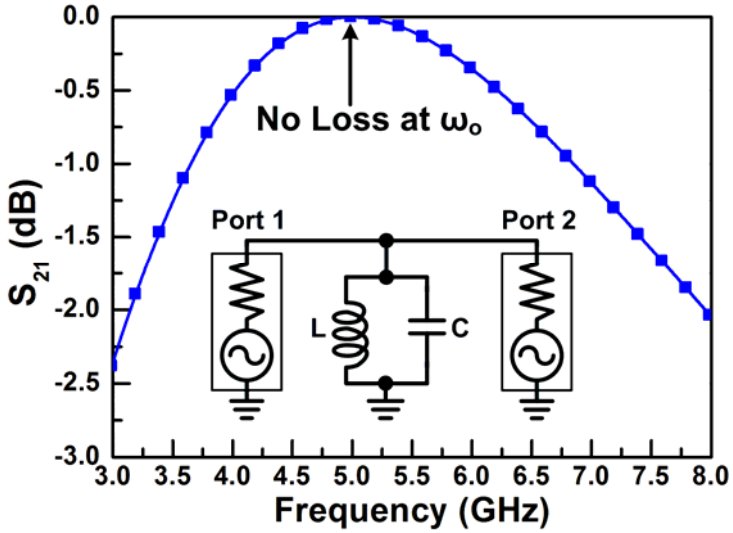


Fig. 1.12. An ideal parallel LC resonator and its simulated S_{21}-parameters under different frequencies.

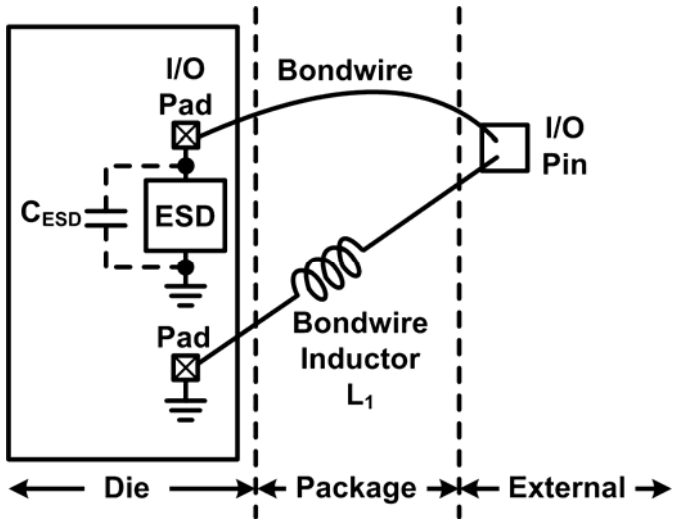


Fig. 1.13. An example of ESD protection design with the parallel LC resonator.

Besides the bondwire inductor L_1, the inductor can also be realized by the on-chip inductor [17]-[20]. Furthermore, the inductor can not only resonates with the parasitic capacitance of the ESD protection device but also serves as an ESD protection device by itself. In this configuration, the parallel LC resonator can be realized as shown in Fig. 1.14 [22]. Since VDD is an ac ground node, the inductor L_P is connected between the I/O pad and VDD with the ESD protection device between the I/O pad and VSS to form a parallel LC resonator. The inductor L_P also serves as an ESD protection device between I/O pad and VDD. The inductor and the parasitic capacitance of the ESD protection device are designed to resonate at the operating frequency of the RF front-end circuit to minimize performance

degradation caused by the ESD protection device. With an inductor directly connected between the I/O pad and VDD, the ESD protection device is reverse biased with the largest possible dc voltage under normal circuit operating conditions, which leads to the minimum the parasitic PN-junction capacitance in the ESD protection device. The placement of the inductor and the ESD protection device can be interchanged to provide the same function. It should be noted that the dc biases in this configuration must be equal on both sides of the inductor. A dc blocking capacitor C_{block} is required to provide a separated dc bias for the internal circuits.

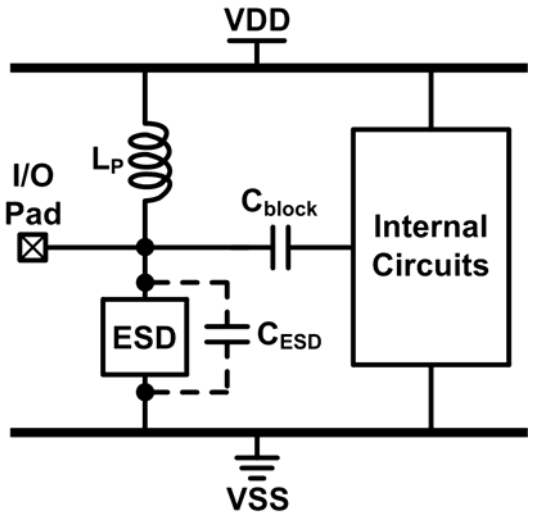


Fig. 1.14. Another example of ESD protection design with the parallel LC resonator, where the inductor L_P provides ESD current path between VDD and the I/O pad.

1.2.3. LC-Tank

LC-tank has been reported for the low-capacitance ESD protection design, which consists of an inductor, a capacitor, and an ESD diode [23]-[28]. As shown in Fig. 1.15, a pair of the LC-tanks was placed at the I/O pad. One LC-tank consists of the inductor L_P and the capacitor C_1, which is placed between the I/O pad and ESD diodes D_P. Another LC-tank consists of the inductor L_N and the capacitor C_2, which is placed between the I/O pad and ESD diodes D_N. These ESD diodes D_P and D_N are used to block the steady leakage current path from VDD to VSS under normal circuit operating conditions. Furthermore, the capacitors C_1 and C_2 can also be realized with the ESD protection devices. At the resonant frequency of the LC-tank, there is ideally infinite impedance from the signal path to the ESD diode. Consequently, the parasitic capacitances of the ESD protection devices are isolated, which can mitigate the parasitic effects from the ESD protection devices.

To further reduce the parasitic capacitance from the ESD protection devices, the modified design with stacked LC-tanks had also been proposed, as shown in Fig. 1.16 [24]-[27]. Two or more LC-tanks are stacked to provide better impedance isolation at resonant frequency, and the impacts of the ESD protection devices can be significantly reduced.

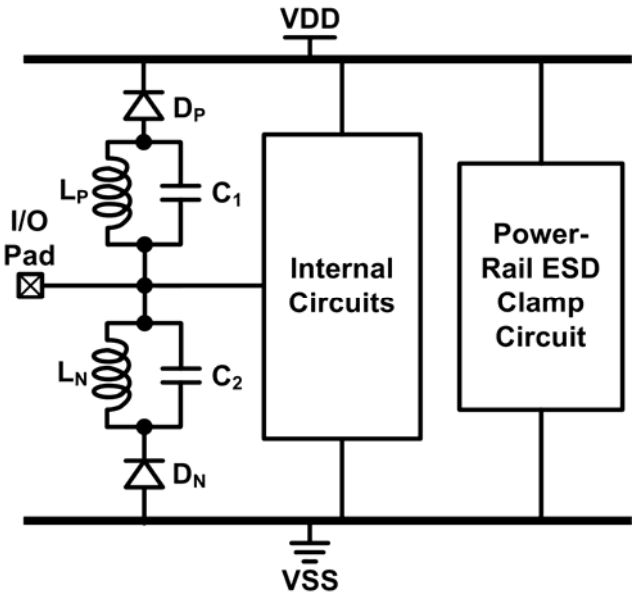


Fig. 1.15. ESD protection design with a pair of LC-tanks.

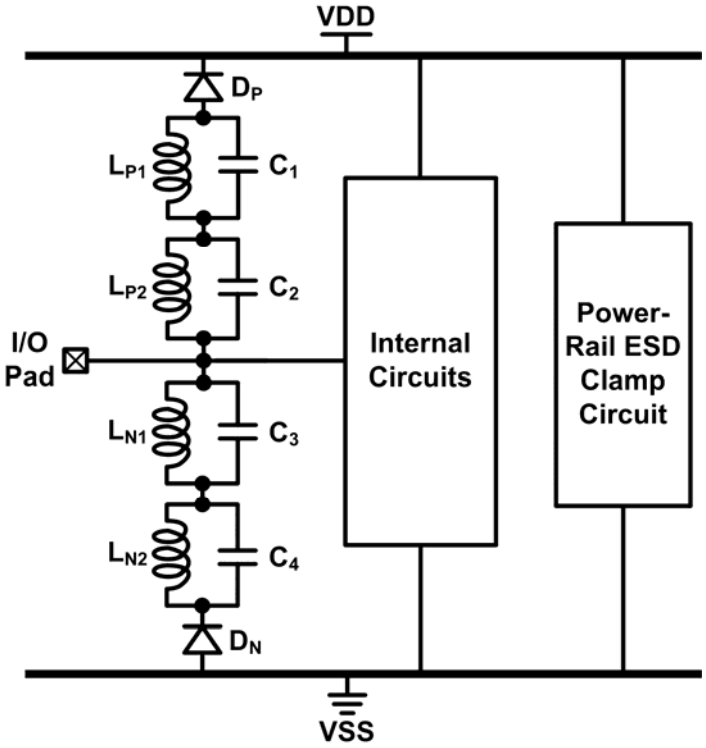


Fig. 1.16. ESD protection design with stacked LC-tanks.

1.2.4. Series LC Resonator

The narrow band ESD protection design can be achieved by using the parallel LC resonator. For the wideband RF front-end circuits, the series LC resonator can be used for ESD protection. The simulated S_{21}-parameter of an ideal series LC resonator under different frequencies is shown in Fig. 1.17. With inductance L and capacitance C in the series LC resonator, the resonant frequency (ω_o) is identical to that shown in (1.3). There is a notch at the resonant frequency, where the signal loss is very large, and the signal will be totally lost. However, at frequencies above the resonant frequency, the magnitude of impedance increases, which means the signal loss becomes much smaller. Thus, wideband ESD protection can be achieved by designing the application band of the series LC resonator to cover the frequency band of the RF signal. Fig. 1.18 shows the ESD protection design utilizes the series LC resonator [17]-[20]. The inductance of L_1 and the parasitic capacitance of the ESD protection device (C_{ESD}) are designed to resonate. During ESD stresses, the ESD current can be discharged through the inductor L_1 and the ESD protection device.

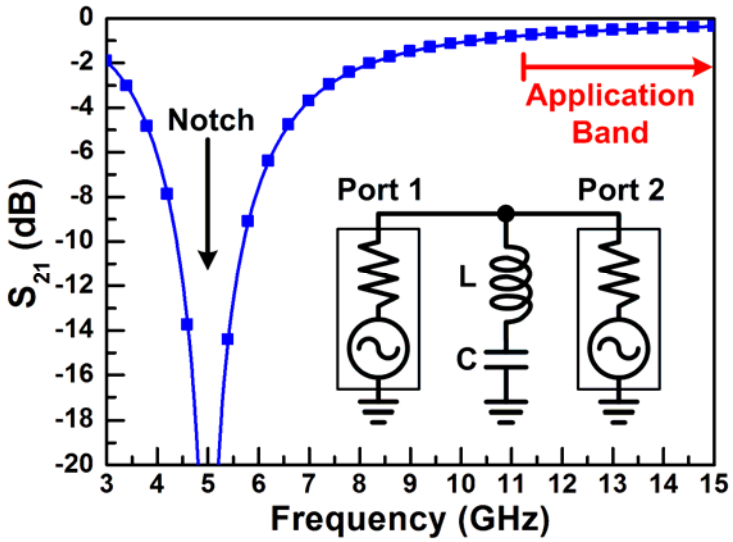


Fig. 1.17. An ideal series LC resonator and its simulated S_{21}-parameters under different frequencies.

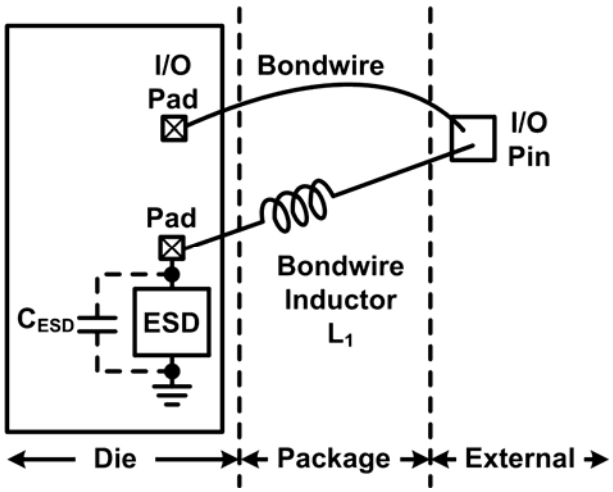


Fig. 1.18. An example of ESD protection design with the series LC resonator.

Another example of ESD protection design utilizing the series LC resonator is shown in Fig. 1.19 [29]-[31], where a pair of the series LC resonators was placed at the I/O pad. ESD current paths from the I/O pad to both VDD and VSS are provided by the inductors and the ESD protection devices.

To reduce the inductors used in the series LC resonators, a modified design used only one inductor is shown in Fig. 1.20 [29]-[31]. One inductor is connected in series with two ESD protection devices connected to VDD and VSS. Because the capacitance in the series LC resonator is the sum of the parasitic capacitances of two ESD protection devices, the inductance used in Fig. 1.20 is smaller than that used in Fig. 1.19 under the same resonant frequency. Consequently, total cost can be reduced in this modified design.

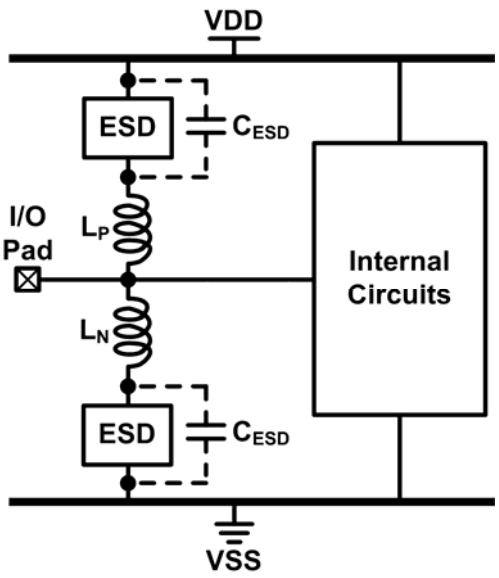


Fig. 1.19. Another example of ESD protection design with the series LC resonator.

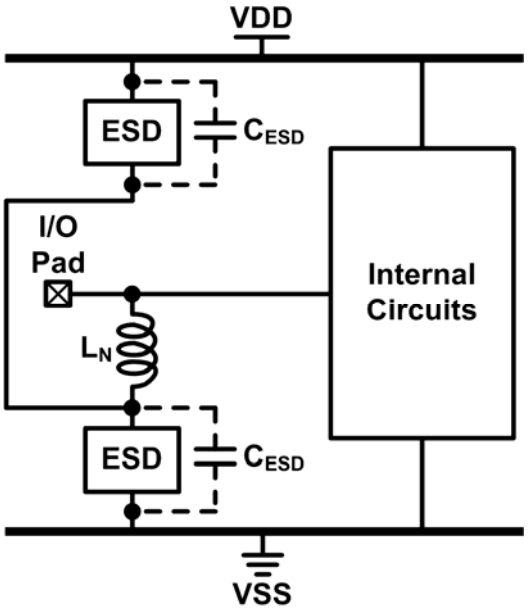


Fig. 1.20. ESD protection design with modified series LC resonator, where only one inductor is connected in series with two ESD protection devices.

1.2.5. Impedance Matching

The size of ESD protection devices must be large enough to perform good ESD robustness. However, parasitic effects will increase with the large ESD protection devices. To solve this dilemma, ESD protection devices can be treated as a part of the impedance matching network. By co-designing the ESD protection circuit and the impedance matching network, large ESD protection devices can be used to achieve high ESD robustness with their parasitic capacitance matched. The impedance matching technique of ESD protection device had been proposed in [32]-[35]. Fig. 1.21 shows the ESD protection circuit with the impedance matching design. In this design, ESD current can be discharged from the I/O pad through the ESD protection devices to VDD and VSS. The combined impedance of the shunt and series impedance is designed to provide impedance matching at the I/O pad with ESD protection [32], [33]. The shunt and series impedance can be realized by various circuit components.

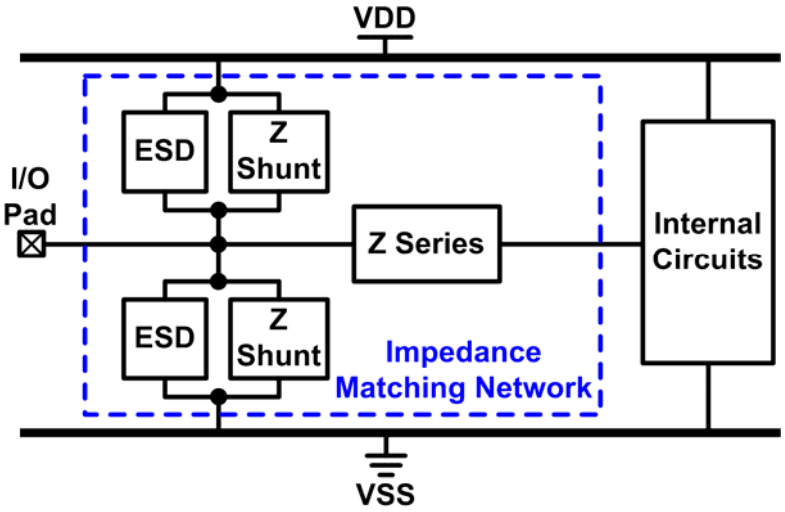


Fig. 1.21. ESD protection design with impedance matching by using shunt and series components.

One example of ESD protection design with impedance matching technique is shown in Fig. 1.22, where uses inductance to match the parasitic capacitances of ESD protection devices [34]. The ESD protection devices are placed next to the I/O pad, and provide ESD protection for the internal circuits. The transmission line (T-Line) connects to the external components. The inductive component L, which can be an inductor or a transmission line, is connected in series with the signal line, and matches the parasitic capacitances of the ESD protection devices, internal circuits, bond pad, and termination element (R_T). The small-signal equivalent circuit model of this matching network is shown in Fig. 1.23, where the inductive component L separates two parasitic capacitances C_1 and C_2. These C_1 and C_2 are

$$C_1 = C_{\text{int}} + C_{RT} \tag{1.4}$$

and

$$C_2 = C_{Pad} + C_{ESD} \tag{1.5}$$

where C_{int}, C_{RT}, C_{Pad}, and C_{ESD} denote the parasitic capacitance at the input node of the internal circuit, the parasitic capacitances of the termination element, bond pad, and ESD protection devices, respectively. The design goal is to neutralize the capacitance of C_1 and C_2 at the operating frequency by using the inductance of L. Therefore, the design target is

$$X_{C1} + X_{C2} + X_L = 0 \tag{1.6}$$

where X_{C1}, X_{C2}, and X_L are the reactance of C_1, C_2, and L, respectively. The overall impedance matching can be achieved as (1.6) holds.

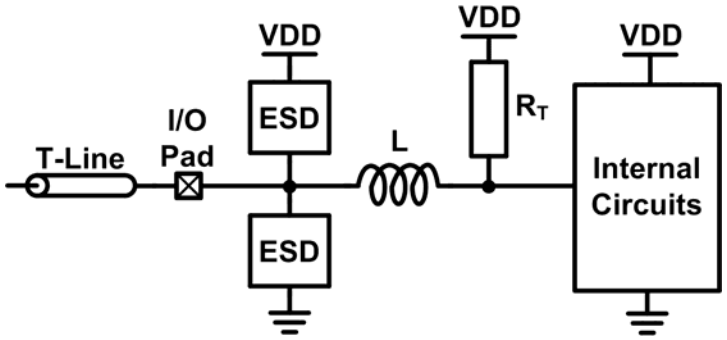


Fig. 1.22. An example of ESD protection design with impedance matching.

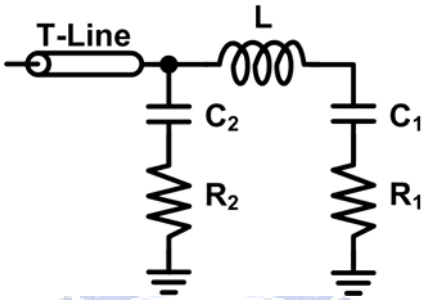


Fig. 1.23. Equivalent small-signal model of the schematic shown in Fig. 1.22.

1.2.6. Inductive ESD Protection

ESD protection design for RF circuits by using inductor as the ESD protection device has been reported [36], [37]. In Fig. 1.24, the ESD protection inductor (L_{ESD}) is placed between the input pad and VSS. Inductors exhibits higher impedance at higher frequencies. Since the frequency component of ESD is much lower than that of the RF signal, the inductor can pass the ESD currents while block the RF signal. In the inductor-based ESD protection design, L_{ESD} was selected to resonate with the parasitic capacitances at the RF operating frequency. Therefore, the parasitic effects of the ESD protection inductor are compensated. To efficiently sink the ESD current, the metal width of the ESD protection inductor should be wide enough to enhance the current handling capability and the parasitic series resistance. However, inductors realized very wide metal traces occupy large chip area. This is the main design concern in the inductor-based ESD protection. Besides, an ac coupling capacitor C_c is needed in this design to avoid the steady leakage current through the ESD protection inductor.

Another inductor-based ESD protection design is shown in Fig. 1.25. The ESD protection inductor can be merged with the gate inductor to save the chip area, since most of the LNAs need a gate inductor connected between the input pad and the gate terminal of the

input MOS transistor [38]. The ESD protection inductor is placed under the gate inductor to form a transformer. Consequently, the transformer-based ESD protection design provides not only the gate inductor in the impedance matching network, but also the ESD protection for the input pad.

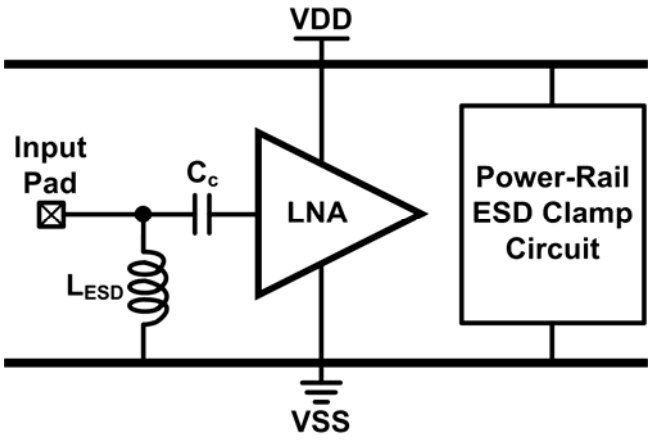


Fig. 1.24. Inductive ESD protection design for an LNA.

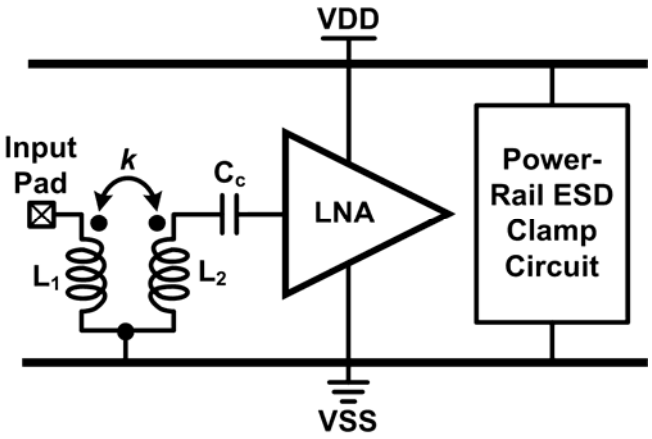


Fig. 1.25. Inductive ESD protection design with transformer.

1.2.7. T-Coil

The ESD protection design with T-coil for wideband applications had been reported [39]. As shown in Fig. 1.26, this circuit can provide a purely resistive input impedance of R_T, under the proper impedance matching design. Once the following conditions hold, the input impedance Z_{in} remains resistive at all frequencies:

$$L_1 = L_2 = \frac{C_L R_T^{\,2}}{4}\left(1+\frac{1}{4\zeta^2}\right) \tag{1.7}$$

$$C_B = \frac{C_L}{16\zeta^2} \tag{1.8}$$

and

$$k = \frac{4\zeta^2 - 1}{4\zeta^2 + 1} \tag{1.9}$$

where ζ is the damping factor of the network transfer function V_X/I_{in}. In the T-coil-based ESD protection design, C_L can be realized by the parasitic capacitance of ESD protection device. Therefore, large ESD protection device can be used without degrading the RF performances. The NMOS and PMOS transistors with gate-coupled technique is used in the first ESD protection design with T-coil. Recently, the silicon-controlled rectifier (SCR) has been used as the ESD protection device in the T-coil-based ESD protection design for a high-speed transmitter [40]. The return loss of the transmitter was improved with the T-coil to compensate the parasitic effects of the SCR.

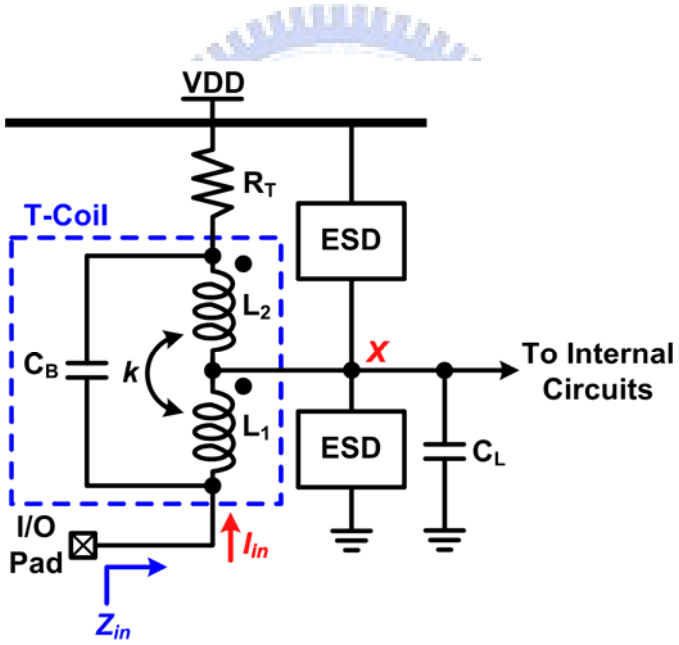


Fig. 1.26. ESD protection design with T-coil.

It has been reported that the transformer plus diode (T-diode) is used to protect the wideband LNA [41], as shown in Fig. 1.27. This is another T-coil-based ESD protection design. In this design, the capacitor C_B in the T-diode was realized with the parasitic capacitance between the inductors L_1 and L_2.

Since the T-coil and the T-diode can overcome the band-limiting problems in the narrow band ESD protection circuits, they are suitable for wideband RF front-end circuits. However, the design concern for the T-coil-based ESD protection was the inductor L_1, which must be

realized by wide metal trace and occupied large chip area.

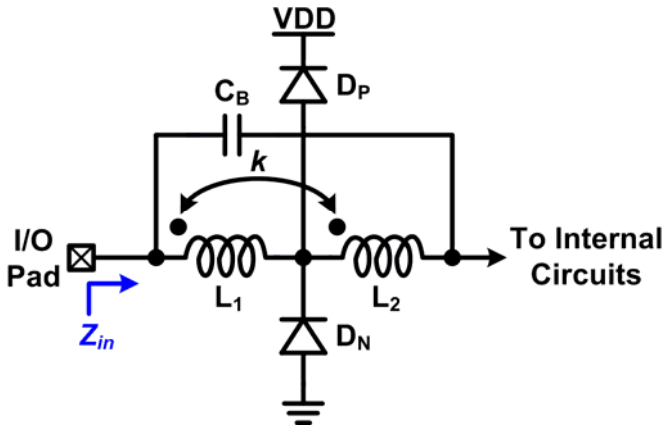


Fig. 1.27. ESD protection with T-diode.

1.2.8. Distributed ESD Protection

The distributed ESD protection scheme had been proposed to achieve wideband impedance matching with ESD protection devices [42]-[44]. The ESD protection devices are divided into several sections and are impedance matched by the transmission lines (T-lines) or inductors, as shown in Fig. 1.28. With the ESD protection devices divided into small sections and matched by the transmission lines, such a distributed ESD protection scheme can achieve wideband impedance matching. The number of ESD protection devices can be varied to optimize the performance. The first reported distributed ESD protection scheme is the equal-size distributed ESD (ES-DESD) protection scheme with ESD diodes, as shown in Fig. 1.29. In the ES-DESD protection scheme, the ESD protection diodes are equally divided into four sections. However, most of ESD current is expected to flow through the section which is closest to the I/O pad. To improve ESD robustness of distributed ESD protection scheme, the modified design of the decreasing-size distributed ESD (DS-DESD) protection scheme had been reported [45].

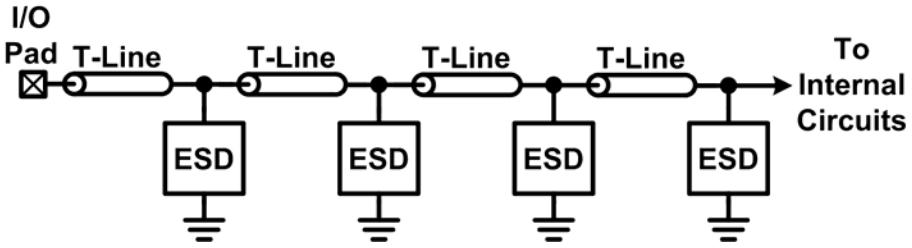


Fig. 1.28. Distribute ESD protection scheme.

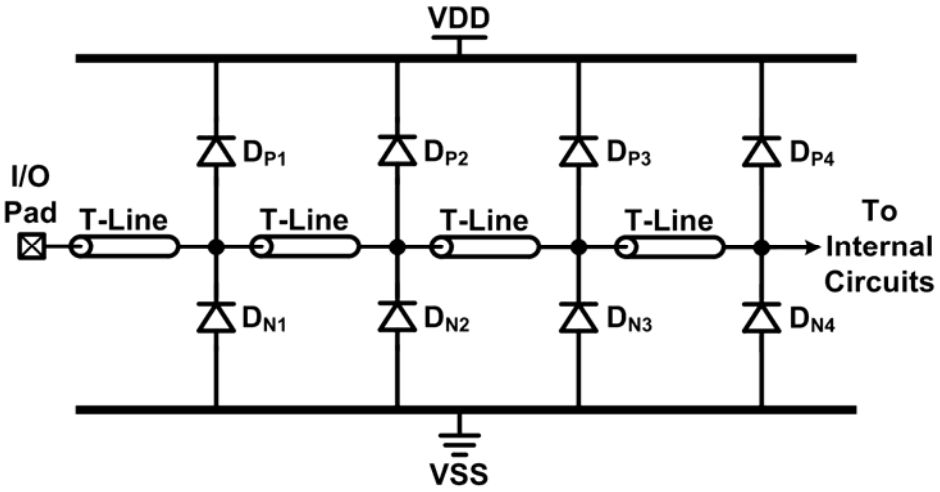


Fig. 1.29. Distribute ESD protection scheme with equal-size ESD diodes.

The DS-DESD protection scheme is shown in Fig. 1.30, which allocates the ESD protection devices with decreasing sizes from the I/O pad to the internal circuit. With larger ESD protection devices close to the I/O pad, ESD robustness is improved. Because the first section of the ESD protection devices in the DS-DESD protection scheme is larger than that in the ES-DESD protection scheme, the DS-DESD protection scheme had been proven to have higher ESD robustness than that of the ES-DESD protection scheme under the same total parasitic capacitance of the ESD protection devices. Moreover, it had also been verified that good wideband impedance matching is still maintained in the DS-DESD protection scheme. However, in these ES-DESD and DS-DESD protection circuits, the de-embedding calculation must be executed to remove the parasitic effects of the I/O pads, and extract the intrinsic characteristics.

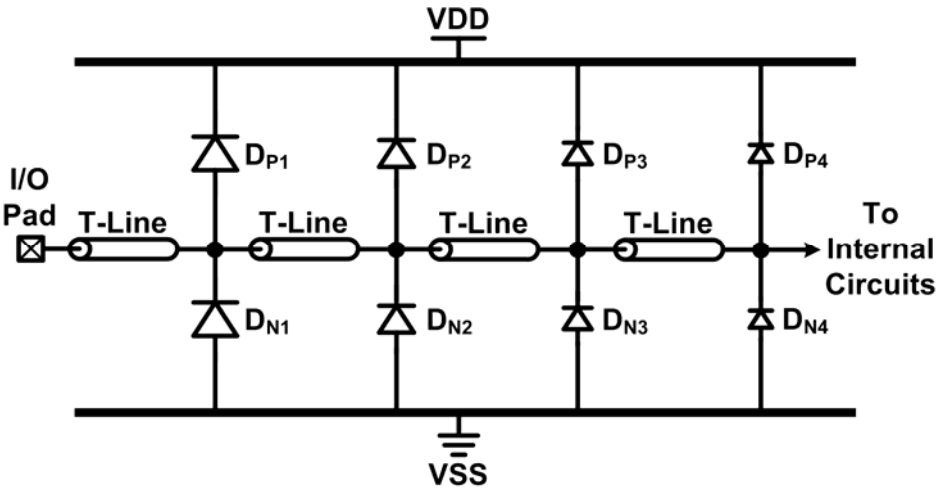


Fig. 1.30. Distribute ESD protection scheme with decreasing-size ESD diodes.

Considering the parasitic capacitance of I/O pad (C_{Pad}), the π-model ESD protection scheme was shown in Fig. 1.31 [46]. The π-model ESD protection scheme consists of one set of ESD protection devices close to the I/O pad, the other set close to the internal circuits, and a transmission line matching these parasitic capacitances. The π-model ESD protection scheme can also be designed to achieve good wideband impedance matching with ESD protection devices.

Another distributed ESD protection scheme with the consideration of the capacitive I/O pad is shown in Fig. 1.32 [47]. The wideband impedance matching can be obtained by scaling these ESD protection devices and the transmission lines. Besides, this scheme can be suitable for wideband RF ESD protection with the large tolerance for the parasitic capacitance of I/O pad.

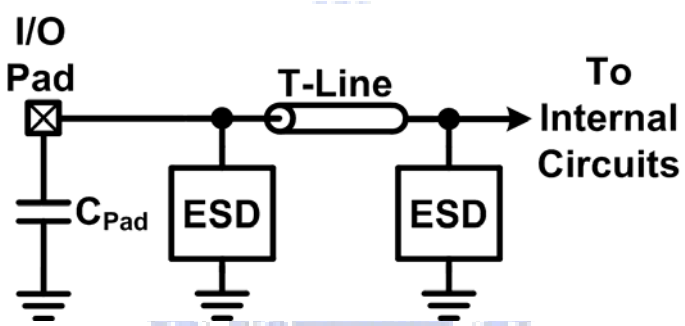


Fig. 1.31. π-model ESD protection scheme.

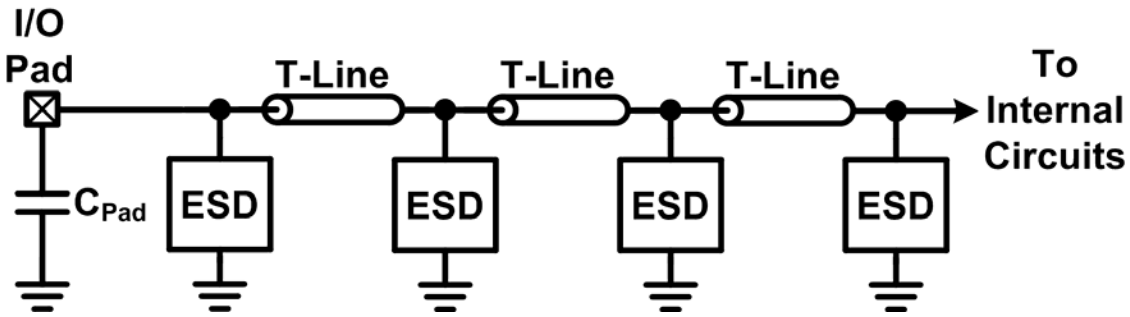


Fig. 1.32. Distributed ESD protection scheme with the consideration for parasitic capacitance of I/O pad.

1.2.9. Discussion and Comparison

The comparison among various ESD protection designs for RF circuits is summarized in Table 1.1. The evaluated parameters are explained as following.

- Design Complexity:
  - "Low": The stand-alone ESD protection device is the ESD protection circuit without extra auxiliary component.
  - "Moderate": The stand-alone ESD protection device is the ESD protection circuit without extra auxiliary component, but the layout of the ESD protection device needs careful consideration.
  - "High": Besides the ESD protection device, extra auxiliary components are needed, and the auxiliary components should be carefully designed.
- Parasitic Capacitance:
  - "Small": The parasitic capacitance of the ESD protection circuit at the I/O pad can be very small with proper design.
  - "Moderate": The parasitic capacitance of the ESD protection circuit at the I/O pad is moderate for RF applications.
  - "Large": The parasitic capacitance of the ESD protection circuit at the I/O pad is large for RF applications.
- ESD Robustness:
  - "Poor": ESD robustness of the ESD protection design is poor.
  - "Moderate": ESD robustness of the ESD protection design is moderate.
  - "Good": ESD robustness of the ESD protection design is good.
  - "Adjustable": For some ESD protection designs by circuit solutions, ESD robustness can be adjusted by using different ESD protection devices and dimensions.
- Area Efficiency:
  - "Poor": The area efficiency of the ESD protection design is poor.
  - "Moderate": The area efficiency of the ESD protection design is moderate.
  - "Good": The area efficiency of the ESD protection design is good.

According to Table 1.1, most of the reported ESD protection designs need additional components to lower the parasitic capacitance. As a result, the chip area is substantially increased, which in turn increases the fabrication cost. Moreover, characteristics of the ESD protection device and the additional components need to be carefully investigated to minimize the undesired effects.

Among the ESD protection devices, silicon-controlled rectifier (SCR) is a promising device because it has both good ESD robustness and low parasitic capacitance under a small

layout area. Besides, the holding voltage and turn-on resistance of SCR are quite low. As the power-supply voltage of ICs decreases to be less than SCR's holding voltage, the latchup issue is avoided. These factors reveal the advantages of SCR devices. With suitable trigger circuit to enhance the turn-on speed and to reduce the trigger voltage, SCR could be the most promising component in the ESD protection design for RF applications.

Table 1.1

Comparison Among the ESD Protection Designs for RF Circuits

ESD Protection Design	Design Complexity	Parasitic Capacitance	ESD Robustness	Area Efficiency
Stacked ESD Protection Devices	Low	Moderate	Moderate	Good
Parallel LC Resonator	High	Small	Adjustable	Poor
LC-Tank	High	Small	Adjustable	Poor
Series LC Resonator	High	Small	Adjustable	Poor
Impedance Matching	High	Small	Adjustable	Poor
Inductive ESD Protection	High	Small	Adjustable	Poor
T-Coil	High	Small	Adjustable	Poor
Distributed ESD Protection	High	Small	Adjustable	Poor

1.3. Organization of This Dissertation

In order to solve the challenges of ESD protection design for RF circuits, several new SCR-based ESD protection designs are proposed and verified in this dissertation. This dissertation consists of seven chapters. In chapter 2, the pin-to-pin ESD protection design on a 5-GHz differential LNA is investigated. In chapter 3, SCR realized in waffle layout structure is proposed to improve ESD current distribution efficiency for ESD protection and to reduce the parasitic capacitance. With the reduced parasitic capacitance, the waffle-structured SCR co-designed with RF power amplifier (PA) was investigated in chapter 4. In chapter 5, the small-signal model of SCR in RF frequency band is presented firstly. With the matching network co-design between SCR device and RF circuits, the parasitics of the SCR device can be cancelled. Besides, with the consideration of low standby leakage in nanoscale CMOS processes, a new 2×VDD-tolerant ESD clamp circuit by using only 1×VDD devices was presented in chapter 6. The outlines of each chapter are summarized below.

In chapter 2, the pin-to-pin ESD protection design on a 5-GHz differential LNA is

proposed. The new ESD protection scheme for differential input pads is realized with the cross-coupled SCR. Verified in a 130-nm CMOS process, this ESD protection scheme achieves 3.5-kV HBM and 300-V MM ESD levels, respectively.

In chapter 3, SCR realized in waffle layout structure is proposed to improve ESD current distribution efficiency for ESD protection and to reduce the parasitic capacitance. The proposed waffle-structured SCR has been verified in a 0.18-μm CMOS process. The waffle layout structure of SCR can achieve smaller parasitic capacitance under the same ESD robustness. With smaller parasitic capacitance, the degradation on RF circuit performance due to ESD protection devices can be reduced. The proposed waffle SCR with low parasitic capacitance is suitable for on-chip ESD protection in RF ICs. Besides, the desired current to trigger on the SCR device with waffle layout structure and its turn-on time has also been investigated in silicon chip.

With the reduced parasitic capacitance, the waffle-structured SCR is applied to an ultra-wideband (UWB) RF power amplifier (PA) in chapter 4. The waffle-structured SCR is designed with ESD detection and trigger circuit to provide the best ESD protection capability while contributing minimum parasitic capacitance to the RF PA in a 130-nm CMOS process. The measurement results have verified the effectiveness of the proposed ESD protection strategy and proved that this ESD protection technique indeed provides excellent ESD robustness of up to 8kV HBM ESD level and 800V MM ESD level.

As the operating frequencies of RF front-end circuits are increased, on-chip ESD protection designs for RF applications are more challenging, and they should be designed more carefully. In chapter 5, the small-signal circuit model of waffle-structured SCR has been presented and proved in silicon. The measured parasitic capacitances well agree with the simulated capacitances. The RF circuits can be well co-designed with the presented small-signal model to eliminate the negative impacts from ESD protection SCR on RF performances. Besides, the optimized design of the bond pad for RF applications was also investigated. The experimental results in a 65-nm CMOS process have proven that the bond pad capacitance and insertion loss can be successfully reduced by the optimized bond pad structure. The small-signal circuit model of the optimized bond pad has also been presented for RF circuit designs.

In order to reduce the parasitic effects of ESD devices connected to the I/O pad, the efficient power-rail ESD clamp circuit must be included into the RF ICs. In chapter 6, the new 2×VDD-tolerant ESD clamp circuit by using only low-voltage devices with low standby leakage current and high ESD robustness for SoC applications with mixed-voltage I/O

interfaces has been successfully designed and verified in a 65-nm CMOS process. The 2×VDD-tolerant ESD clamp circuit can operate without gate-oxide reliability issue, and the leakage current is only in the order of 100 nA under normal circuit operating condition. Besides, there is no latchup concern in this design. The new ESD clamp circuit by using only low-voltage devices with very low standby leakage current and high ESD robustness is the useful circuit solution for on-chip ESD protection design with mixed-voltage I/O interfaces in SoC applications.

Chapter 7 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in this chapter.

Chapter 2

ESD Protection Design on A 5-GHz Differential Low-Noise Amplifier With Cross-Coupled SCR

In the typical ESD protection design, the ESD test results have shown that the pin-to-pin ESD stress is the most critical ESD-test pin combination for the differential input pads with the conventional double-diode ESD protection scheme. In this chapter, a new ESD protection scheme for differential input pads, which is realized with cross-coupled SCR, is proposed to protect the differential low-noise amplifier (LNA). In Section 2.2, the reference differential LNA was implemented without ESD protection for comparison. In Section 2.3, the conventional double-diode ESD protection scheme is applied to protect the differential LNA. ESD test results have shown that the pin-to-pin ESD test is the most critical ESD-test pin combination for the LNA with double-diode ESD protection scheme. To improve overall ESD robustness of the ESD-protected differential LNA, a new ESD protection scheme with the cross-coupled SCR is proposed in Section 2.4. As compared with the conventional double-diode ESD protection scheme, the pin-to-pin ESD robustness is substantially improved by the new proposed ESD protection scheme in this work. Experimental results have shown that the new proposed on-chip ESD protection circuit co-designed with the input matching network of the LNA can achieve excellent ESD robustness and good RF performance.

2.1. Background

As the feature size of MOS transistor in CMOS technology is continuously scaled down to improve the high-frequency characteristics, the advanced nanoscale CMOS technology is more attractive to implement radio-frequency integrated circuits (RF ICs). In an RF front-end, the low-noise amplifier (LNA) plays a very important role because it is the first stage in the RF receiver. In LNA design, differential configuration is popular because the differential LNA has the advantages of better common-mode noise rejection, as well as less sensitivity to substrate noise, supply noise, and bond-wire inductance variation [48]-[54]. In addition, the

differential output signals of the differential LNA can be directly connected to the differential inputs of the double balanced mixer.

Electrostatic discharge (ESD) is getting more attention in nanoscale CMOS technology, because it has become one of the most important reliability issues in IC chips [1], [3], [4], [55]. With the evolution of CMOS technology, ESD protection design in nanoscale CMOS processes becomes more challenging, because the upper bound of the ESD protection design window for an input pad, which is set by the gate-oxide breakdown voltage, is lowered. To achieve satisfactory ESD robustness without seriously degrading circuit performance, ESD protection design should be taken into consideration during the design phase of all ICs, especially RF ICs [2]. Since the LNA is usually connected to the external of the RF receiver chip such as the off-chip antenna, on-chip ESD protection circuits are needed for all input pads of the LNA.

In the ESD-test standards, there are several ESD-test pin combinations. Besides the positive-to-VDD (PD-mode), positive-to-VSS (PS-mode), negative-to-VDD (ND-mode), and negative-to-VSS (NS-mode) ESD tests, the pin-to-pin ESD test is also specified to evaluate ESD robustness of the differential input pads. Under the pin-to-pin ESD test, one input pad is stressed with the other input pad relatively grounded, while all the other pads including all VDD and VSS pads are floating [56]. To provide efficient pin-to-pin ESD protection, the ESD protection device should be turned on quickly with low enough clamping voltage and low enough turn-on resistance under ESD stresses to effectively protect the thin gate oxides of MOS transistors in the differential input stage. As the gate-oxide thickness becomes much thinner in nanoscale CMOS processes, robust ESD protection design against all ESD-test pin combinations, especially including pin-to-pin ESD tests, becomes more challenging. Recently, an ESD protection scheme with a local ESD clamp device between the differential input pads had been proposed to improve ESD robustness of LNA under pin-to-pin ESD stresses [57].

2.2. Low-Noise Amplifier Without ESD Protection

2.2.1. Differential LNA Design

Differential configuration is popular for LNA design because differential LNA has the advantages of common-mode noise rejection, less sensitivity to substrate noise, supply noise, and bond-wire inductance variation. In addition, the differential output signals of the differential LNA can be directly connected to the differential inputs of the double balanced mixer.

There are several requirements on the performance of LNA. First, the noise figure of LNA should be minimized because it dominates overall noise figure of the whole RF receiver. Besides, the power gain of LNA should be high enough to suppress the impacts caused by the noise figures in the succeeding stages in RF receiver. Moreover, the power consumption needs to be low enough to facilitate portable applications.

The circuit schematic of the LNA without ESD protection for comparison reference is shown in Fig. 2.1. The architecture of common-source with inductive degeneration is applied to match the input impedance of LNA to the source impedance (50 Ω) at the operating frequency of 5 GHz. Good isolation between the input and output can be enhanced by using the cascode configuration. Moreover, the cascode configuration reduces Miller effect and provides good stability [58]. The dimensions of the input NMOS transistors M_1 and M_3 were designed according to the compromise between noise figure and power consumption. Since the small-signal operation of the differential LNA is symmetrical, the half circuit can be referred to analyze the LNA. The input impedance (Z_{in}) of the RF IN_1 pad can be calculated as

$$Z_{in} = \frac{1}{j\omega(C_{gs1} + C_{G1})} + j\omega(L_{G1} + L_{S1}) + \omega_T L_{S1} \tag{2.1}$$

where C_{gs1} is the gate-source capacitance of M_1, C_{G1} is the added capacitance between the gate and source terminals of M_1, L_{G1} is the gate inductance, and L_{S1} is the source inductance. The ω_T is the unity-gain angular frequency of M_1, which can be expressed as

$$\omega_T = \frac{g_{m1}}{C_{gs1}} \tag{2.2}$$

where g_{m1} is the transconductance of M_1. With the input matching network resonating at the operating frequency, the input impedance ($Z_{in\_Resonance}$) is purely real and can be given by

$$Z_{in\_Resonance} = \omega_T L_{S1} = \frac{g_{m1}}{C_{gs1}} L_{S1}. \tag{2.3}$$

To match the input impedance at resonance to the source impedance, L_{S1} is determined once the size of M_1 has been chosen. The resonance angular frequency (ω_0), which is designed to be the operating frequency, can be obtained by

$$\frac{1}{\omega_0(C_{gs1} + C_{G1})} = \omega_0(L_{G1} + L_{S1}). \tag{2.4}$$

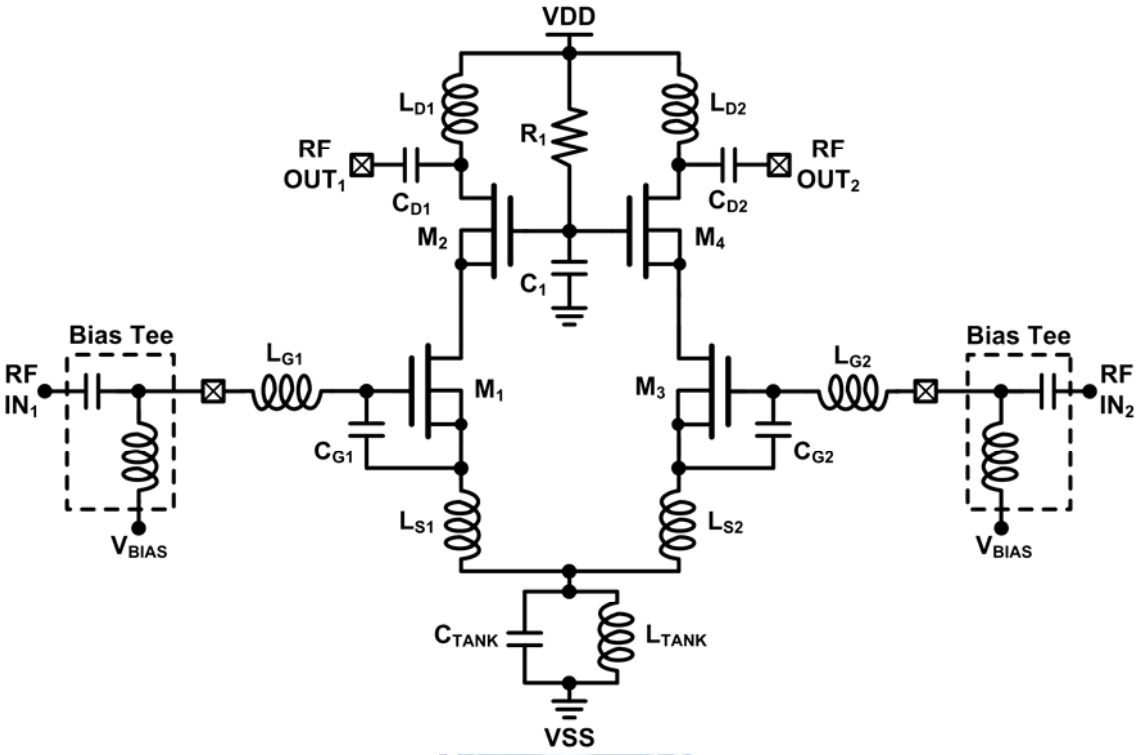


Fig. 2.1. Differential LNA without ESD protection for comparison reference.

At resonance, the source inductor L_{S1} and gate inductor L_{G1} compensate the capacitance at the gate terminal of M_1. After L_{S1} is determined to match the source impedance, the remaining capacitive impedance needs to be cancelled by L_{G1}. However, the small C_{gs1} leads to intolerable large L_{G1}. Therefore, an extra capacitor C_{G1} is added in parallel with C_{gs1} to reduce the required inductance of L_{G1}. The drain inductor L_{D1} and drain capacitor C_{D1} form the output matching network to match the output impedance of LNA to 50 Ω.

The gate voltages of M_2 and M_4 are biased to VDD through the resistor R_1. The capacitor C_1 acts as a decoupling capacitor. L_{TANK} and C_{TANK} form a LC-tank to enhance the common-mode rejection. With the deep N-well structure, the P-well (bulk) region of each NMOS transistor can be fully isolated from the common P-substrate, so the source and bulk terminals are connected together to eliminate the body effect. All of the inductors are the on-chip spiral inductors implemented by the top metal layer, and all of the capacitors in the differential LNA are realized by the metal-insulator-metal (MIM) capacitors. The aforementioned active and passive devices are fully integrated in the experimental test chip in a 130-nm CMOS process. In order to verify the effectiveness of the on-chip ESD protection circuits at the input pads, the ac coupling capacitor between the input pad and L_{G1} (L_{G2}) is not realized in the test chip, because the ac coupling capacitor connected to the input pad can block some ESD energy when the input pad is stressed by ESD. Thus, the off-chip bias tee is

needed to combine the RF input signal and the dc bias at the input node during RF measurement.

2.2.2. Experimental Results

On-wafer measurements were performed to characterize the RF performance and ESD robustness. The differential LNA without ESD protection consumes 10.3 mW under 1.2-V power supply. To measure the S-parameters of the differential LNA, four-port S-parameter measurement with Agilent E8361A network analyzer was performed. The measurement system converted the measured four-port S-parameters to the differential two-port S-parameters. Fig. 2.2 shows the measured S-parameters of the differential LNA without ESD protection. At 5 GHz, the S_{11}-, S_{21}-, and S_{22}-parameters are -27.2 dB, 16.2 dB, and -9.3 dB, respectively. The measured output matching condition (S_{22}-parameter) is not as good as expectation due to the drain capacitances (C_{D1} and C_{D2}), which are sensitive to the parasitic effects at the output node. The S_{12}-parameter is better than -29 dB because good reverse isolation is one of the advantages of the cascode configuration. The noise figure was measured by using Agilent N8975A noise figure analyzer and Agilent 346C noise source. The reference differential LNA has the noise figure of 2.16 dB at 5 GHz.

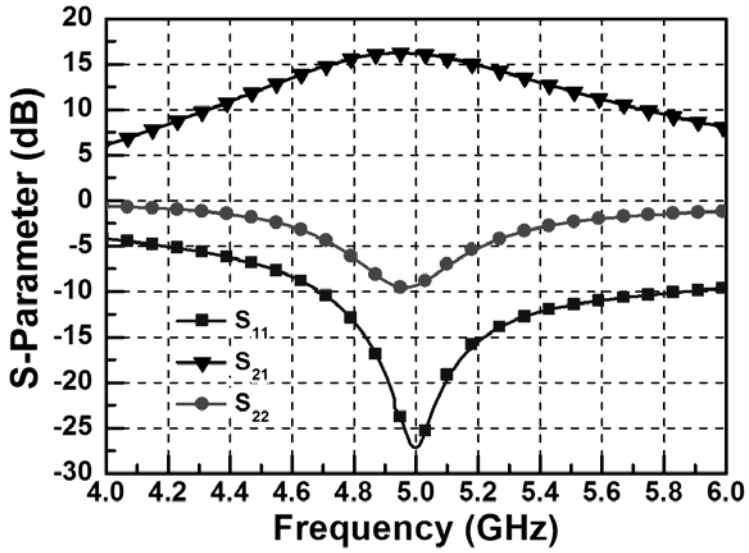


Fig. 2.2. Measured S-parameters of the differential LNA without ESD protection.

The human-body-model (HBM) and machine-model (MM) ESD levels were also measured from the differential LNAs. The failure criterion is 30% voltage shift under 1-μA current bias. During ESD tests, the off-chip bias tee was not included. The measured HBM

and MM ESD levels of the LNAs are listed in Table 2.1. The LNA without ESD protection is very vulnerable to ESD, because it fails at 50-V HBM and 10-V MM ESD tests.

Table 2.1

HBM and MM ESD Robustness Under Different Test Pin Combinations

ESD Robustness	LNA Without ESD Protection		ESD-Protected LNA (Double-Diode)		ESD-Protected LNA (Cross-Coupled SCR)	
	HBM	MM	HBM	MM	HBM	MM
Positive to VSS	< 50 V	< 10 V	3 kV	250 V	3.5 kV	300 V
Negative to VDD	< 50 V	< 10 V	7 kV	400 V	3.5 kV	350 V
Pin to Pin	< 50 V	< 10 V	2.5 kV	200 V	> 8 kV	800 V
VDD to Vss	0.5 kV	< 10 V	> 8 kV	> 1000 V	> 8 kV	>1000 V

2.3. Differential LNA With Conventional Double-Diode ESD Protection Scheme

2.3.1. Double-Diode ESD Protection Scheme

The conventional double-diode ESD protection scheme is applied to protect the differential LNA in Fig. 2.3. As shown in Fig. 2.3, a P+/N-well diode (D_P) is connected between each input pad and VDD, while an N+/P-well diode (D_N) is connected between each input pad and VSS. The total parasitic capacitance from the ESD protection diodes at each input pad is specified as 300 fF. To achieve the total parasitic capacitance of 300 fF, the P+/N-well diode and N+/P-well diode are realized with parasitic capacitance of only 150 fF, respectively. The P+/N-well diode (D_P) is implemented with two parallel fingers, and each finger was drawn with the dimension of 16 μm × 5 μm in layout. Similarly, the N+/P-well diode (D_N) is implemented with two parallel fingers, and each finger has the dimension of 19.2 μm × 5 μm.

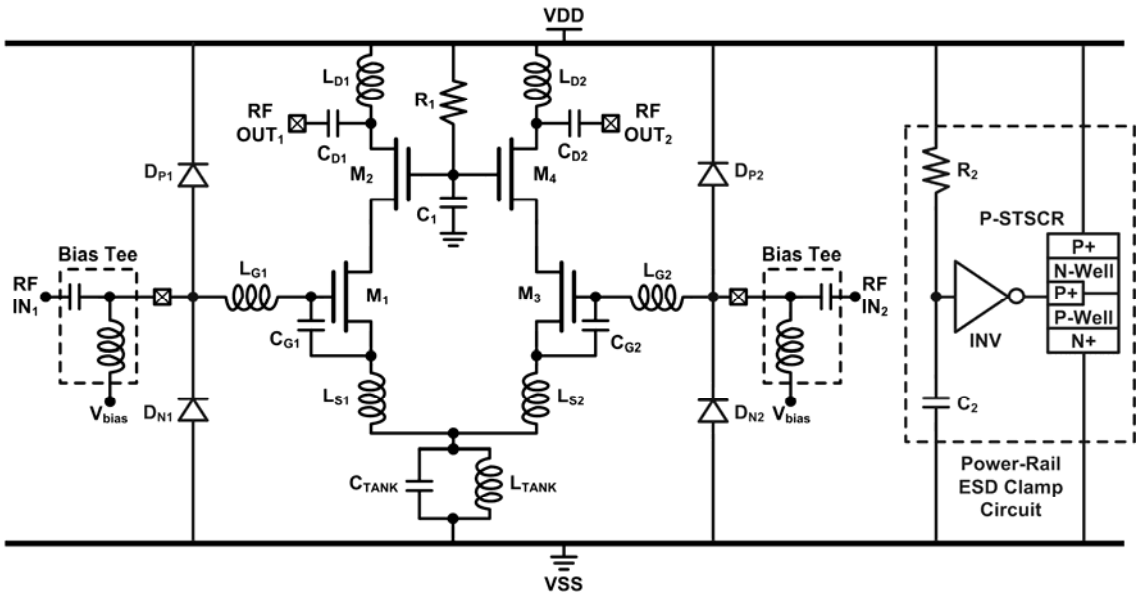


Fig. 2.3. Differential LNA with conventional double-diode ESD protection scheme.

To co-design the input matching network of LNA with ESD protection devices, the source inductors (L_{S1} and L_{S2}) and gate inductors (L_{G1} and L_{G2}) are adjusted to achieve impedance match at 5 GHz.

2.3.2. Power-Rail ESD Clamp Circuit

The power-rail ESD clamp circuit is used to provide ESD current paths between VDD and VSS under ESD stresses. Fig. 2.4 shows the power-rail ESD clamp circuit used in this work, where the P-type substrate-triggered silicon-controlled rectifier (P-STSCR) is used as the ESD clamp device. SCR had been demonstrated to be suitable for ESD protection design for RF ICs, because it has the advantages of high ESD robustness and low parasitic capacitance under a small layout area [57], [59]-[61]. The cross-sectional view and equivalent circuit of the P-STSCR is shown in Fig. 2.5. The SCR path exists among the P+ diffusion (anode), N-well, P-well, and N+ diffusion (cathode). The equivalent circuit of the P-STSCR consists of a parasitic vertical PNP BJT Q_{PNP} and a parasitic lateral NPN BJT Q_{NPN}. Q_{PNP} is formed by the P+ diffusion (anode), N-well, and P-well. Q_{NPN} is formed by the N-well, P-well, and N+ diffusion (cathode). In this power-rail ESD clamp circuit, the anode and N-well terminals of P-STSCR are connected to VDD, and the cathode and P-well terminals are connected to VSS. Under ESD stresses, the positive-feedback regenerative mechanism [62] of Q_{NPN} and Q_{NPN} results in the great current handing capability of SCR, and makes SCR very robust against ESD stresses. To reduce the trigger voltage and increase the turn-on speed

of the P-STSCR under ESD stresses, the P+ trigger diffusion (in the P-well region) is added between the anode and cathode. Besides, an extra ESD detection circuit is designed to inject the trigger current into the P-trigger node under ESD stresses, as shown in Fig. 2.4. The ESD detection circuit consists of an RC timer and an inverter. The resistor R_2 and capacitor C_2 form the RC timer with the time constant of 0.3 μs, which can distinguish the ESD transients from the normal circuit operating conditions [8].

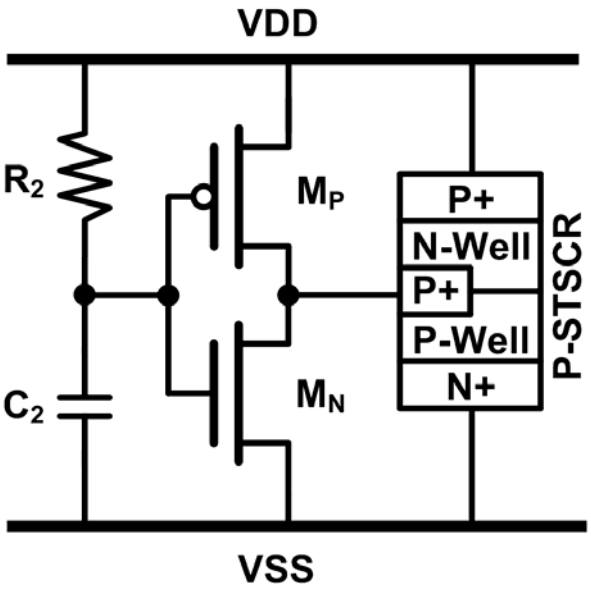


Fig. 2.4. Power-rail ESD clamp circuit realized with P-STSCR.

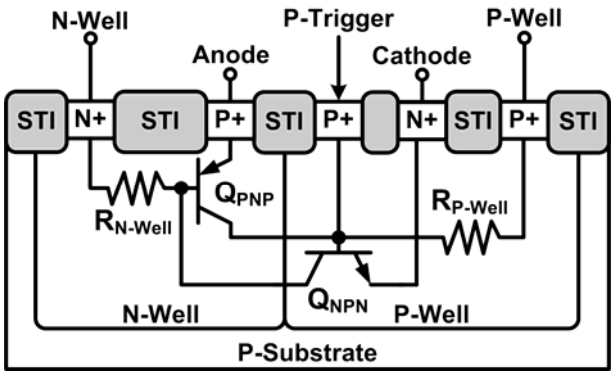


Fig. 2.5. Cross-sectional view and equivalent circuit of P-STSCR.

Under normal circuit operating conditions, the node between R_2 and C_2 is charged to high potential (VDD). Since NMOS M_N is turned on and PMOS M_P is turned off, the P-trigger node of the P-STSCR is tied to VSS and no trigger current is injected to the P+ trigger node of P-STSCR. Thus, the P-STSCR is kept off under normal circuit operating conditions. Under ESD stresses, the ESD voltage at VDD has the rise time in the order of ns.

With the RC delay provided by R_2 and C_2, the gate voltages of M_P and M_N are initially kept at low potential (~0 V). Therefore, M_P is turned on to inject trigger current into the P-trigger node. As a result, the P-STSCR is turned on to provide ESD current path from VDD to VSS. Since the power-rail ESD clamp circuit is placed between VDD and VSS, it does not contribute any parasitic capacitance to neither input nor output pads. Hence, the size of the P-STSCR in the power-rail ESD clamp circuit is not limited by the specification of parasitic capacitance at the RF pad.

2.3.3. Experimental Results

The differential LNA with double-diode ESD protection scheme has been fabricated in the same 130-nm CMOS process. The chip micrograph of the differential LNA with double-diode ESD protection scheme is shown in Fig. 2.6. This ESD-protected differential LNA occupies the chip area of 1090 μm × 750 μm, which has the same power consumption as that of differential LNA without ESD protection.

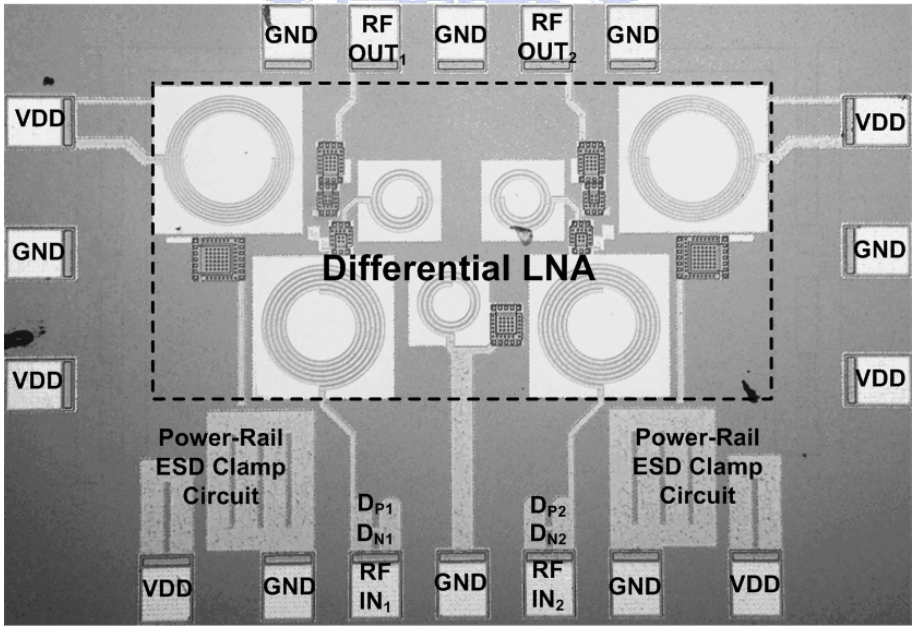


Fig. 2.6. Chip micrograph of differential LNA with conventional double-diode ESD protection scheme.

The measured HBM and MM ESD levels are listed in Table 2.1. The LNA with double-diode ESD protection scheme has 2.5-kV HBM and 200-V MM ESD levels. Besides, the power-rail ESD clamp circuit can sustain over 8-kV HBM and over 1000-V MM VDD-to-VSS ESD stresses.

Using SCR as the ESD protection device could introduce latchup concern. To avoid latchup issue, the holding voltage of SCR must be higher than the power-supply voltage, which is 1.2 V in this work. The dc I-V characteristics of the stand-alone SCR were measured by Tektronics 370B curve tracer. As shown in Fig. 2.7, the holding voltages of the stand-alone SCR under 25 °C, 85 °C, and 125 °C are 2.84 V, 2.58 V, and 2.38 V, respectively. With the holding voltage higher than the power-supply voltage (1.2 V), the SCR can be safely used in this RF chip without latchup issue.

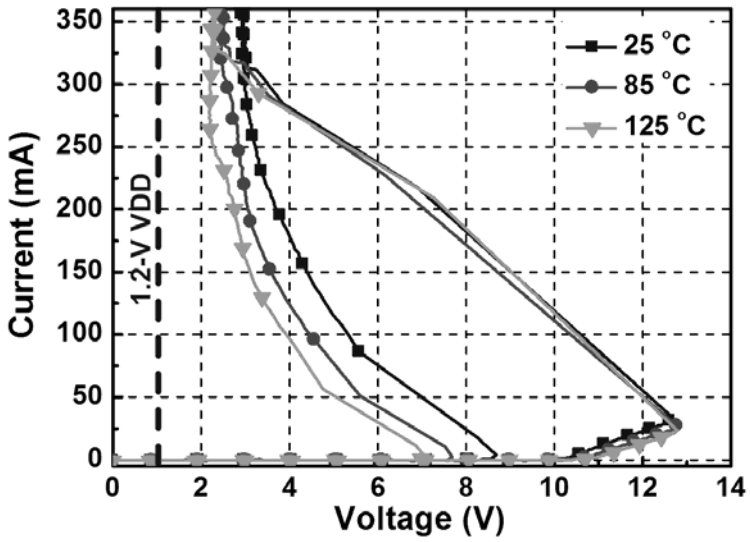


Fig. 2.7. Measured dc I–V curves of stand-alone SCR under different temperatures.

2.3.4. Discussion on ESD Robustness

In the conventional double-diode ESD protection scheme, the PS-mode ESD current path consists of D_{P1}, VDD bus, and P-STSCR, as shown in Fig. 2.8(a). Thus, the voltage drop ($V_{PS\text{-}Mode}$) along the PS-mode ESD current path is

$$V_{PS-Mode} = V_{DP1} + V_{VDD\_Bus} + V_{P-STSCR} \tag{2.5}$$

where V_{DP1}, V_{VDD_Bus}, and VP-STSCR are the voltage drops across D_{P1}, VDD bus, and P-STSCR, respectively. Since D_{P1} is placed very close to the RF IN_1 pad, the voltage across the metal connected between D_{P1} and the RF IN_1 pad is neglectable. Since the source and bulk terminals of M_1 are connected to VSS through L_{S1} and L_{TANK}, $V_{PS\text{-}Mode}$ is all across the gate and source terminals of M_1.

Under ND-mode ESD stresses, the ESD current path consists of P-STSCR, VSS bus, and D_{N1}, as shown in Fig. 2.8(b). The voltage drop ($V_{ND\text{-}Mode}$) along the ND-mode ESD current path is

$$V_{ND-Mode} = V_{P-STSCR} + V_{VSS\_Bus} + V_{D_{N1}} \tag{2.6}$$

where V_{VSS_Bus} and V_{DN1} are the voltage drops across VSS bus and D_{N1}, respectively. Since D_{N1} is placed very close to the RF IN_1 pad, the voltage across the metal connected between D_{N1} and the RF IN_1 pad is neglectable. However, $V_{ND\text{-}Mode}$ is not all across the gate and drain terminals of M_1, because some voltage drop is across M_2. Besides, the size of D_N is 20% larger than that of D_P, which makes the turn-on resistance of D_N smaller than that of D_P. With smaller resistance along the ESD current path, the overshooting/undershooting ESD voltage is lower under the same ESD current. Thus, the ND-mode ESD level is higher than the PS-mode ESD level in the differential LNA with double-diode ESD protection scheme.

Under pin-to-pin ESD stresses, one differential input pad is stressed by ESD pulse with the other differential input pad grounded, and both VDD and VSS are floating. The ESD current path in the LNA with double-diode ESD protection scheme is shown in Fig. 2.9. The voltage drop ($V_{Pin\text{-}to\text{-}Pin}$) along the pin-to-pin ESD current path is

$$V_{Pin-to-Pin} = V_{D_{P1}} + V_{VDD\_Bus} + V_{P-STSCR} + V_{VSS\_Bus} + V_{D_{N2}} \tag{2.7}$$

where V_{DN2} is the voltage drop across D_{N2}. With the source and bulk terminals connected to VSS, the voltage drop ($V_{Pin\text{-}to\text{-}Pin\_GS}$) across the gate and source terminals of M_1 is

$$V_{Pin-to-Pin\_GS} = V_{D_{P1}} + V_{VDD\_Bus} + V_{P-STSCR} + V_{VSS\_Bus} \tag{2.8}$$

Compared with (2.5), the voltage drop across the gate and source terminals of M_1 under the pin-to-pin ESD stress is higher than that under the PS-mode ESD stress with the additional term of V_{VSS_Bus}. Therefore, the pin-to-pin ESD stress is the most critical ESD-test pin combination for the differential LNA with double-diode ESD protection scheme. Table 2.1 shows that the lowest ESD robustness in the differential LNA with the conventional double-diode ESD protection scheme indeed exists in the pin-to-pin ESD test. The difference between the PS-mode and pin-to-pin ESD robustness is not obvious in this work, because the power-rail ESD clamp circuit is placed close to the differential input pads. However, the power-rail ESD clamp circuit may not be able to be placed close to the differential input pads in all practical chip implementations, which could lead to higher V_{VSS_BUS}. Hence, the pin-to-pin ESD robustness is expected to be lower than the PS-mode ESD robustness in the differential input stage with the conventional double-diode ESD protection scheme.

To investigate the failure mechanism of the ESD-protected LNA, failure analysis was performed. The scanning electron microscope (SEM) picture in Fig. 2.10 shows the failure locations of the differential LNA with double-diode ESD protection scheme after 3-kV HBM pin-to-pin ESD test. The ESD damages are all located on the gate oxide of the input NMOS

M_1, whose gate is connected to the zapped pad. This failure mechanism indicates that even if the ESD protection device did not fail, the overshooting ESD voltage across the gate oxide is so high to damage the thin gate oxide of the input transistor in the LNA.

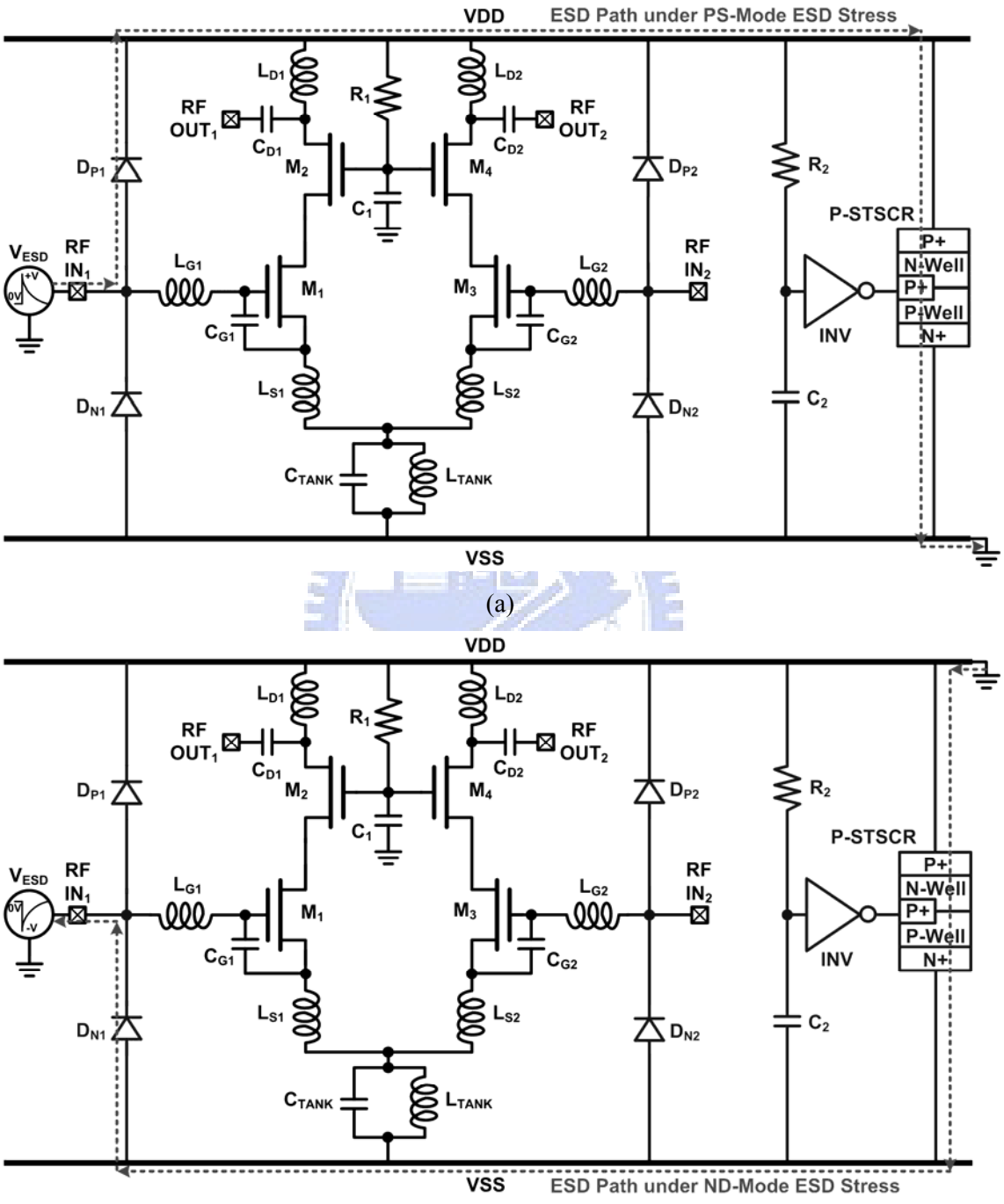


Fig. 2.8. ESD current paths in differential LNA with conventional double-diode ESD protection scheme under (a) PS-mode, and (b) ND-mode ESD stresses.

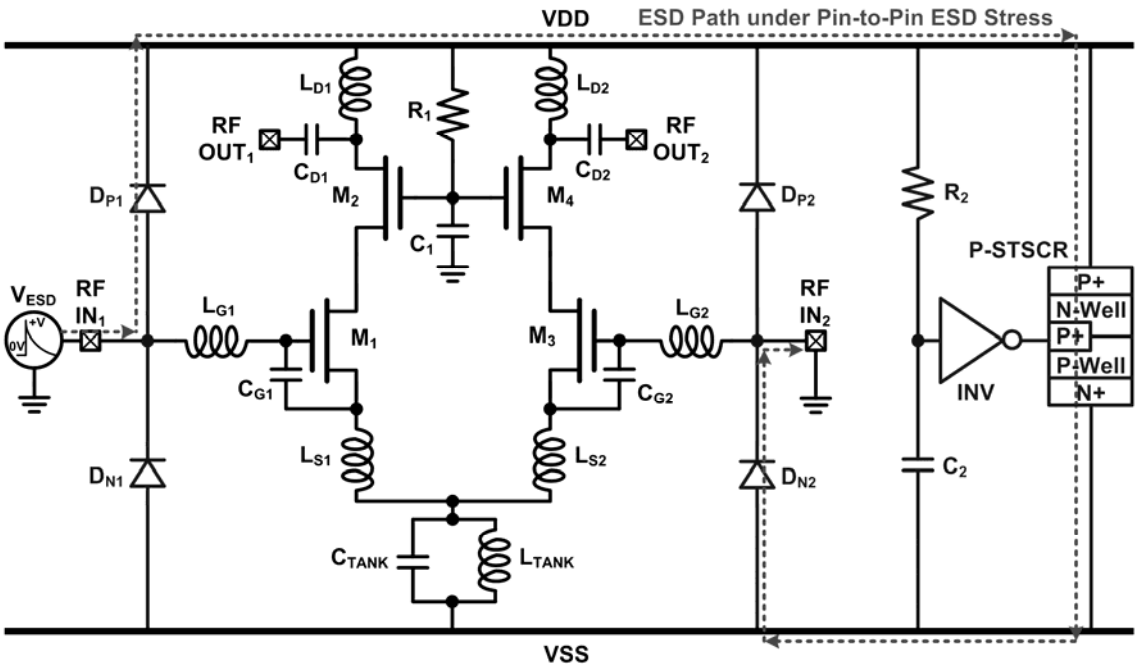


Fig. 2.9. ESD current path in differential LNA with conventional double-diode ESD protection scheme under pin-to-pin ESD stresses.

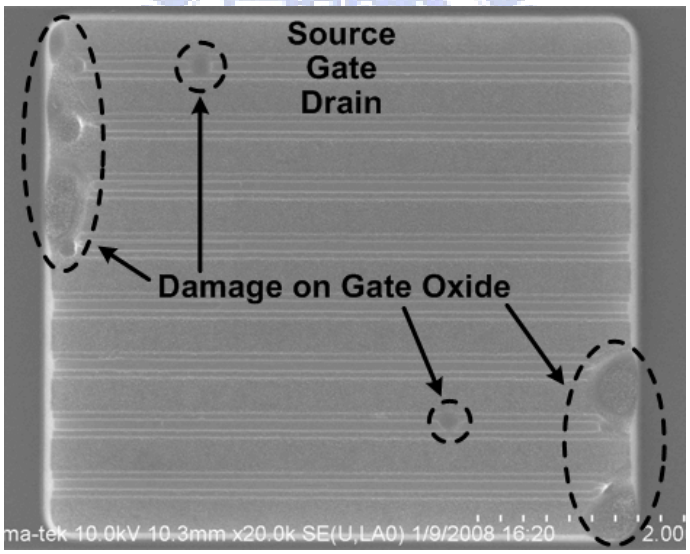


Fig. 2.10. SEM picture at the failure points of differential LNA with conventional double-diode ESD protection scheme after 3-kV HBM pin-to-pin ESD test. The failure locations are all at the gate oxide of the input NMOS M_1.

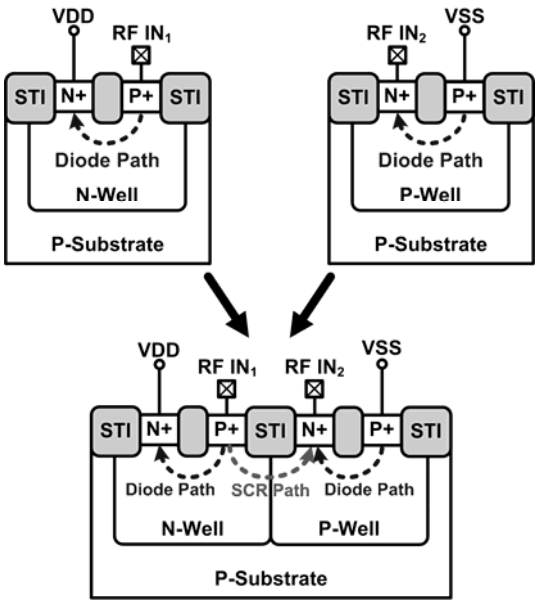
2.4. Differential LNA With New Proposed ESD Protection Scheme of Cross-Coupled SCR

2.4.1. New Proposed Cross-Coupled-SCR ESD Protection Scheme

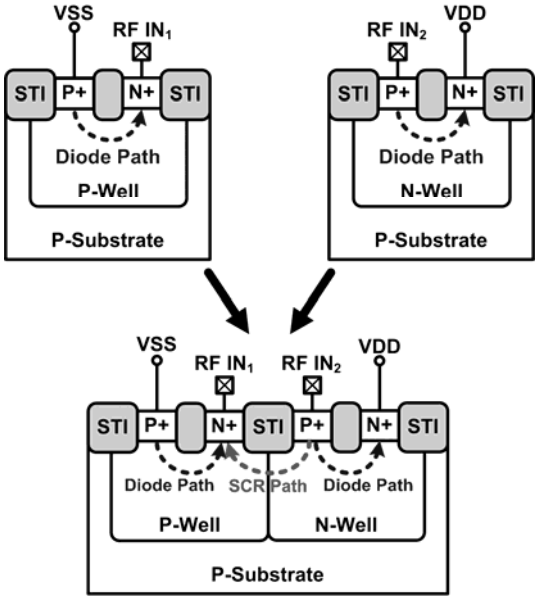
To improve pin-to-pin ESD robustness, the voltage drop along the pin-to-pin ESD

current path needs to be reduced. In this new proposed ESD protection design, the SCR path is established directly from one differential input pad to the other differential input pad without adding any extra device. The four ESD protection diodes at the differential input pads in the conventional double-diode ESD protection scheme, which include two P+/N-well diodes (D_P) and two N+/P-well diodes (D_N), are reserved in the new proposed design, but the placement is changed. Fig. 2.11 illustrates the concept of the proposed ESD protection scheme. As illustrated in Fig. 2.11(a), by merging D_{P1} (P+/N-well diode for RF IN_1 pad) and D_{N2} (N+/P-well diode for RF IN_2 pad) together, an SCR path from RF IN_1 pad to RF IN_2 pad can be established for pin-to-pin ESD protection without adding any extra device. Similarly, D_{P2} (P+/N-well diode for RF IN_2 pad) and D_{N1} (N+/P-well diode for RF IN_1 pad) can be merged together to form an SCR path from RF IN_2 pad to RF IN_1 pad, as illustrated in Fig. 2.11(b). Since D_{P1}, D_{N1}, D_{P2}, and D_{N2} still exist, the pad-to-VDD and pad-to-VSS ESD current paths are not altered.

Fig. 2.12 shows the circuit schematic of the differential LNA with the new proposed ESD protection scheme of cross-coupled SCR. P-$STSCR_1$ is placed close to the RF IN_1 pad to provide efficient pin-to-pin ESD current path from the RF IN_1 pad to the RF IN_2 pad. Similarly, P-$STSCR_2$ is placed close to the RF IN_2 pad to provide efficient ESD current path from the RF IN_2 pad to the RF IN_1 pad under pin-to-pin ESD stresses. To achieve the total parasitic capacitance of 300 fF at each differential input pad, the anode and cathode diffusion regions of P-$STSCR_1$ and P-$STSCR_2$ are all drawn as 60 μm × 2.4 μm. In the proposed ESD protection scheme, the PS-mode ESD current path for the RF IN_1 (RF IN_2) pad is provided by DP_1 (DP_2) embedded in P-$STSCR_1$ (P-$STSCR_2$) and the power-rail ESD clamp circuit. The ND-mode ESD current path for the RF IN_1 (RF IN_2) pad is provided by the power-rail ESD clamp circuit and D_{N1} (D_{N2}) embedded in P-$STSCR_2$ (P-$STSCR_1$). Under pin-to-pin ESD stresses, the ESD current paths between the differential input pads are provided by the cross-coupled SCR with P-$STSCR_1$ and P-$STSCR_2$. To enhance the turn-on speed, the P+ trigger diffusions are also inserted into P-$STSCR_1$ and P-$STSCR_2$. Since P-$STSCR_1$ and P-$STSCR_2$ are the same devices as that used in the power-rail ESD clamp circuit, the ESD detection circuit in the power-rail ESD clamp circuit can also serve as the ESD detection circuit for the cross-coupled SCR. By connecting the P+ trigger diffusions to the output of the ESD detection circuit in the power-rail ESD clamp circuit, P-$STSCR_1$ and P-$STSCR_2$ can be quickly turned on to provide efficient pin-to-pin ESD protection.



(a)



(b)

Fig. 2.11. Establishing the SCR paths between the differential input pads by combining (a) D_{P1} (P+/N-well diode for RF IN_1 pad) with D_{N2} (N+/P-well diode for RF IN_2 pad), and (b) D_{P2} (P+/N-well diode for RF IN_2 pad) with D_{N1} (N+/P-well diode for RF IN_1 pad).

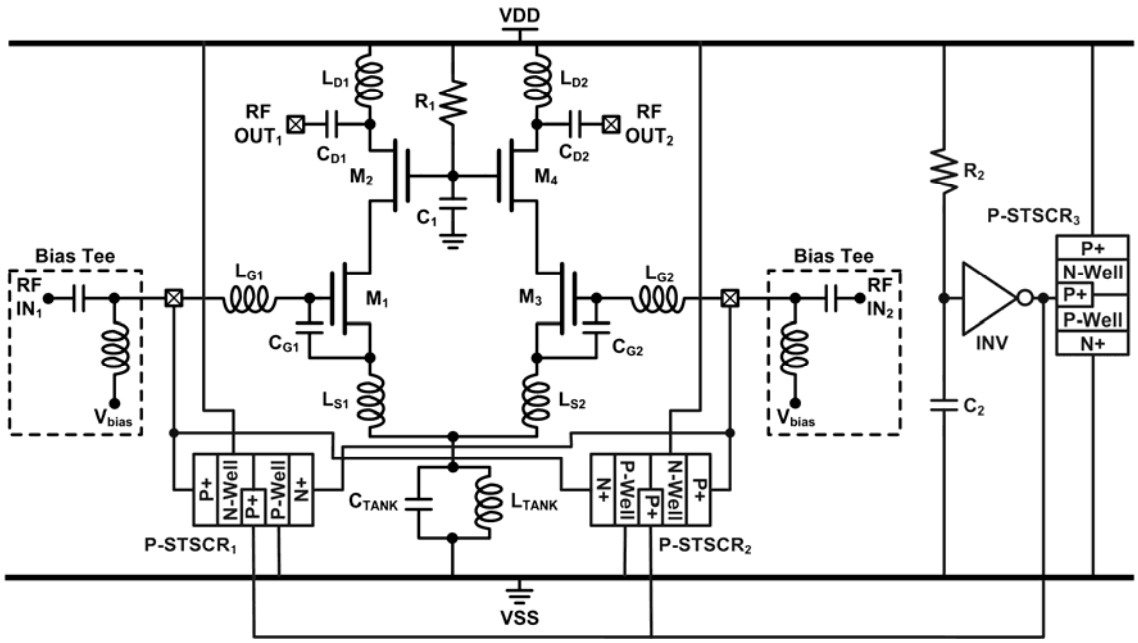


Fig. 2.12. Differential LNA with proposed ESD protection scheme of cross-coupled SCR.

2.4.2. Experimental Results

The differential LNA with the new proposed cross-coupled-SCR ESD protection scheme has been fabricated in a 130-nm CMOS process. The chip micrograph of the differential LNA with cross-coupled-SCR ESD protection scheme is shown in Fig. 2.13. It has the same chip area and power consumption as the differential LNA with double-diode ESD protection scheme.

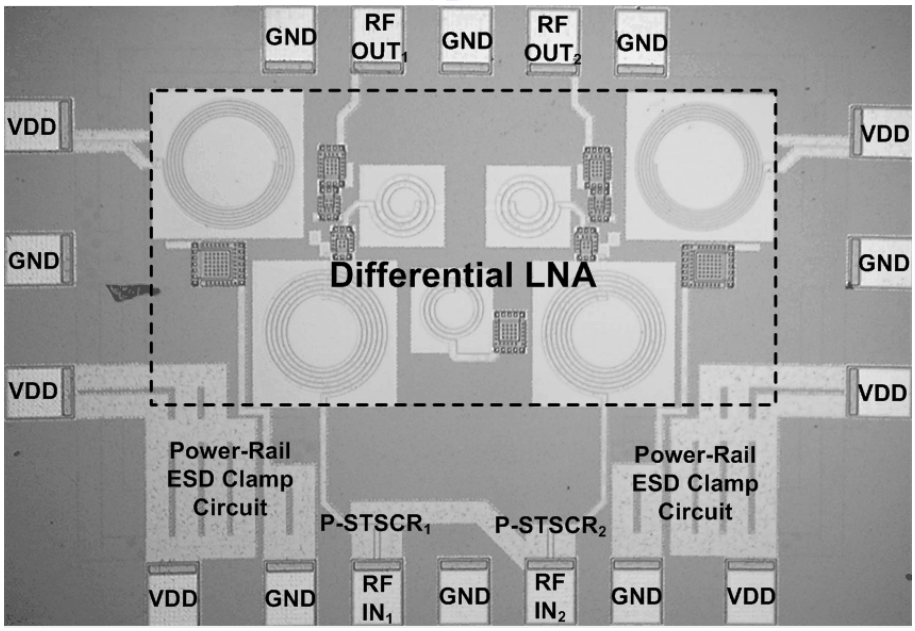


Fig. 2.13. Chip micrograph of differential LNA with proposed cross-coupled-SCR ESD protection.

The measured RF performance of the differential LNA with cross-coupled-SCR ESD protection scheme is compared with those of the original differential LNA without ESD protection in Figs. 2.14 - 2.17. To compare the input matching conditions, the measured S_{11}-parameters of these two differential LNAs are shown in Fig. 2.14. It is observed that the operating frequency of the differential LNA with cross-coupled-SCR ESD protection scheme is shifted from 5 GHz to 4.8 GHz. At 4.8-GHz, the measured S_{11}-parameter is -26.3 dB. The shift in the operating frequency is due to the lack of RF model for SCR device in the given CMOS process. The macro model of SCR was ever reported to simulate its turn-on mechanism during ESD stress [63], [64]; however, the small-signal model of SCR in RF circuit operation condition is still scarce. If the precise RF model of SCR device in the desired RF frequency band can be obtained, the input matching network for LNA can be well co-designed with the SCR device.

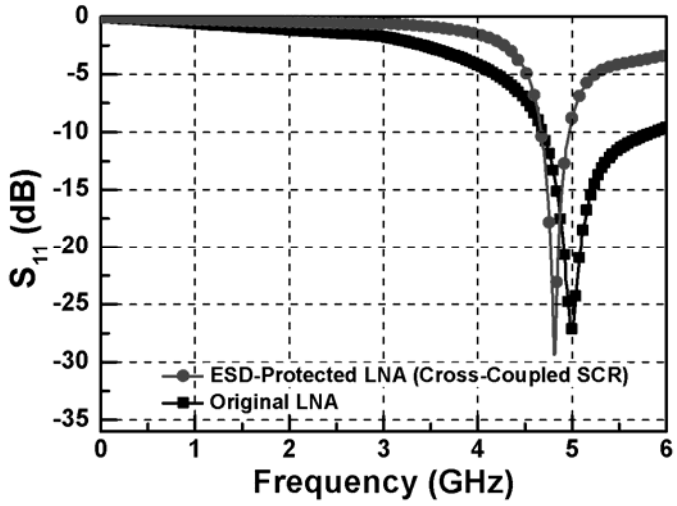


Fig. 2.14. Measured S_{11}-parameters of differential LNA with the proposed cross-coupled-SCR ESD protection scheme, and the original differential LNA without ESD protection.

Fig. 2.15 compares the measured power gains (S_{21}-parameters) of these two differential LNAs. At 4.8 GHz, the S_{21}-parameter of differential LNA with cross-coupled-SCR ESD protection scheme is 17.2 dB. The measured S_{22}-parameters of these two differential LNAs are compared in Fig. 2.16. The S_{22}-parameter of differential LNA with cross-coupled-SCR ESD protection scheme is -8 dB at 4.8 GHz. Satisfactory reverse isolation is also achieved in differential LNA with cross-coupled-SCR ESD protection scheme, where the S_{12}-parameter is lower than -26 dB at 4.8 GHz. Fig. 2.17 shows the measured noise figures of these

differential LNAs. At 4.8 GHz, the noise figure of differential LNA with cross-coupled-SCR ESD protection scheme is 3.58 dB. As compared with the original differential LNA without ESD protection, the minimum noise figure of differential LNA with cross-coupled-SCR ESD protection scheme is somewhat increased. The increase in the noise figure is attributed to the parasitic effects of ESD protection devices with the overlapped wide metal lines in layout, which are connected between the differential input pads and the cross-coupled SCR devices.

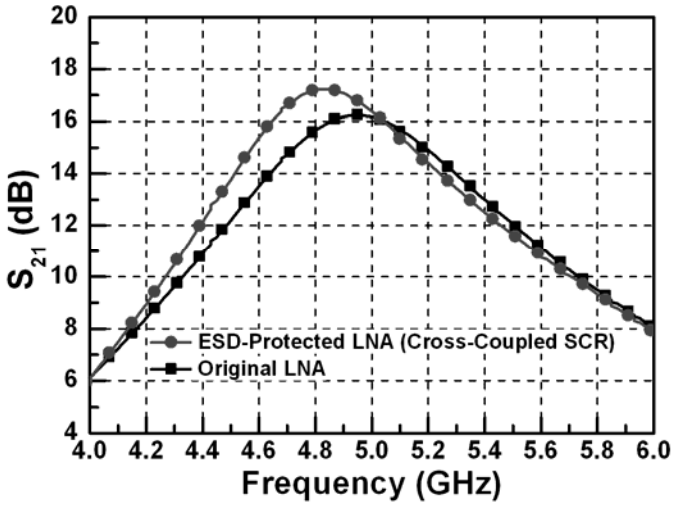


Fig. 2.15. Measured S_{21}-parameters of differential LNA with the proposed cross-coupled-SCR ESD protection scheme, and the original differential LNA without ESD protection.

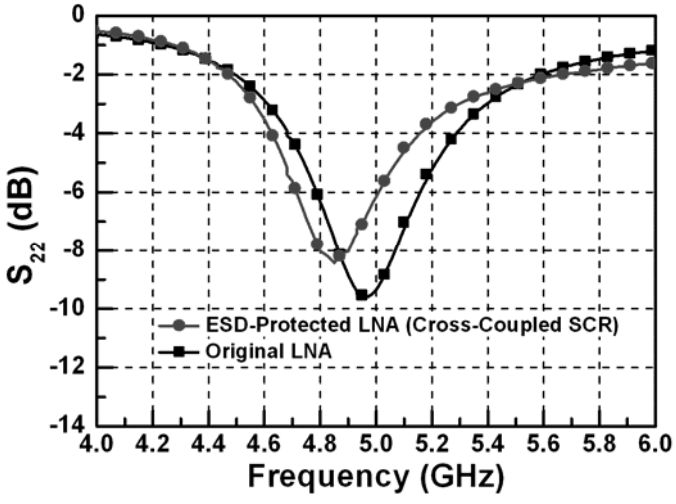


Fig. 2.16. Measured S_{22}-parameters of differential LNA with the proposed cross-coupled-SCR ESD protection scheme, and the original differential LNA without ESD protection.

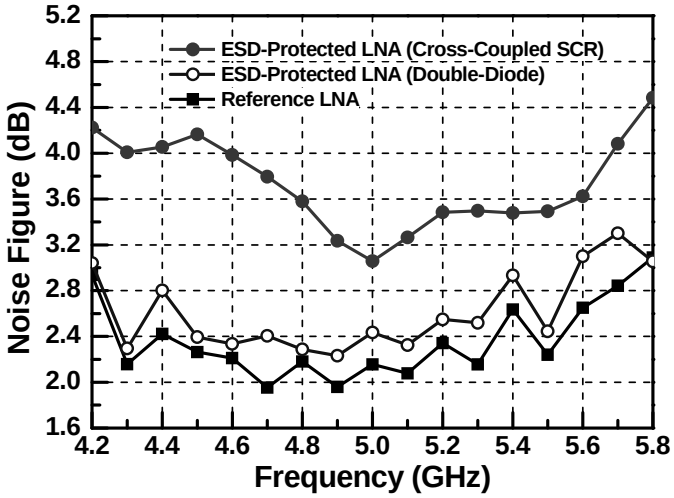


Fig. 2.17. Measured noise figures of differential LNA.

The HBM and MM ESD levels of differential LNA with the proposed cross-coupled-SCR ESD protection scheme under different test pin combinations are also listed in Table 2.1. Since the PS-mode ESD current paths are the same for the two ESD-protected LNAs, their PS-mode ESD levels do not have significant difference. However, the ND-mode ESD robustness of differential LNA with cross-coupled-SCR ESD protection scheme is lower than that of differential LNA with double-diode ESD protection scheme, because D_{N1} embedded in P-STSCR$_2$ is placed close to the RF IN$_2$ pad instead of the RF IN$_1$ pad. Thus, V_{VSS_Bus} in (2.6) and the routing resistance between D_{N1} and the RF IN$_1$ pad are increased in the differential LNA with cross-coupled-SCR ESD protection scheme. Consequently, the ND-mode ESD robustness is degraded in this LNA with cross-coupled-SCR ESD protection scheme.

The pin-to-pin ESD current path in the differential LNA with cross-coupled-SCR ESD protection scheme is illustrated in Fig. 2.18. The voltage drop along the pin-to-pin ESD current path is

$$V_{Pin-to-Pin} = V_{P-STSCR_1} + V_{P-STSCR_1-to-RFIN_2} \tag{2.9}$$

where $V_{P\text{-}STSCR1}$ and $V_{P\text{-}STSCR1\text{-}IN2}$ are the voltage drops across P-STSCR$_1$ and the metal line between P-STSCR$_1$ and the RF IN$_2$ pad, respectively. As compared with (2.7), the voltage drop along the pin-to-pin ESD current path is substantially reduced. Thus, the pin-to-pin ESD robustness is significantly improved in differential LNA with the new proposed cross-coupled-SCR ESD protection scheme. The ESD test result shows that the differential LNA with cross-coupled-SCR ESD protection scheme can sustain pin-to-pin ESD stresses of

over 8-kV HBM and 800-V MM.

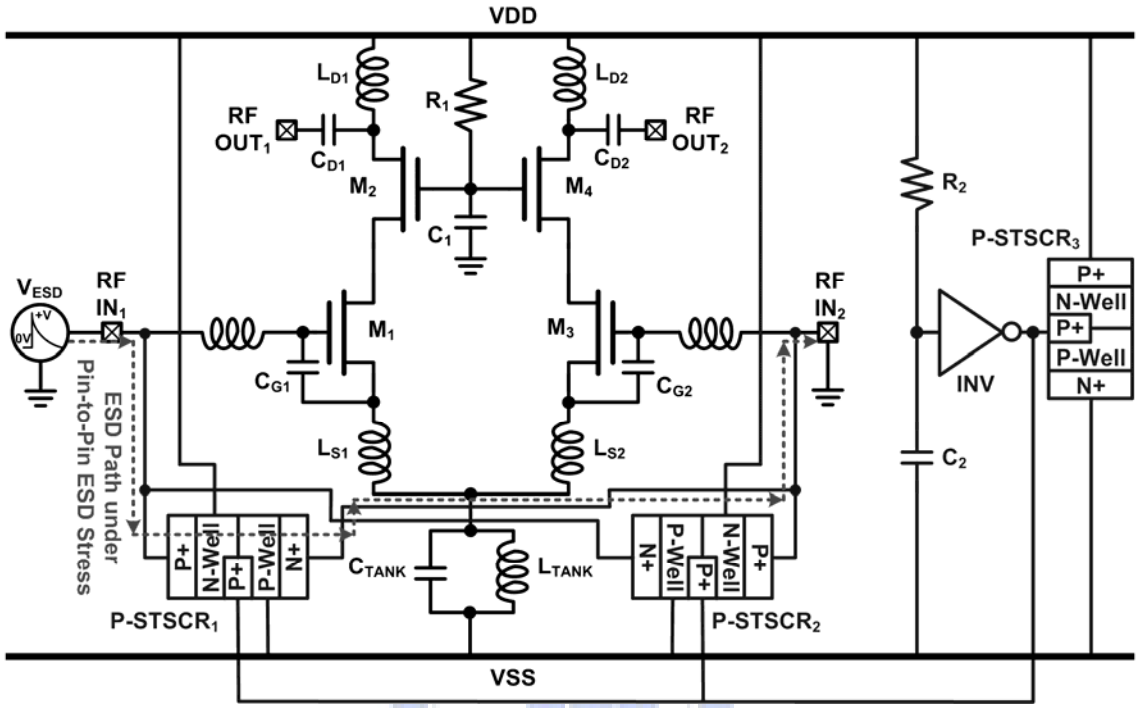


Fig. 2.18. ESD current path in differential LNA with the proposed cross-coupled-SCR ESD protection scheme under pin-to-pin ESD stresses.

Table 2.2 summarizes the measured performances of the original differential LNA without ESD protection and the differential LNA with the new proposed cross-coupled-SCR ESD protection scheme, and compares their performances to those of the prior CMOS differential LNAs. The proposed ESD-protected differential LNA in this work exhibits excellent ESD robustness as compared with the other differential LNAs, especially in the pin-to-pin ESD stress.

2.5. Summary

A new ESD protection scheme for differential input pads has been proposed and successfully verified to protect the differential LNA. Realized with the cross-coupled SCR, the proposed ESD protection scheme can significantly reduce the voltage drop along the ESD current path under the pin-to-pin ESD test, which is the most critical ESD-test pin combination for the differential input stage with the conventional double-diode ESD protection scheme. With lower voltage drop along the ESD current path, the internal circuits can be efficiently protected against ESD damages. Verified in a 130-nm CMOS process,

pin-to-pin ESD robustness of differential LNA with the proposed cross-coupled-SCR ESD protection scheme has been substantially improved, as compared to that of differential LNA with the conventional double-diode ESD protection scheme. With the evolution of CMOS technology, the gate-oxide breakdown voltage becomes lower, which indicates that reducing the voltage drop along the ESD current path becomes more important for ESD protection design in advanced nanoscale CMOS processes. To achieve good RF performance and high ESD robustness simultaneously, the proposed ESD protection scheme in this work can be well co-designed with the differential LNA.

Table 2.2

Comparison on ESD Robustness Among CMOS Differential LNAs

	Technology	f_0 (GHz)	VDD (V)	P_{dc} (mW)	NF (dB)	S_{21} (dB)	S_{11} (dB)	HBM ESD Level (kV)	MM ESD Level (V)
LNA Without ESD Protection	**0.13-μm CMOS**	**5**	**1.2**	**10.3**	**2.16**	**16.2**	**-27.2**	**< 0.05**	**< 10**
ESD-Protected LNA (Cross-Coupled SCR)	**0.13-μm CMOS**	**4.8**	**1.2**	**10.3**	**3.58**	**17.2**	**-26.3**	**3.5**	**300**
Ref. [48]	**0.18-μm CMOS**	**5.75**	**1**	**16**	**0.9**	**14.2**	**N/A**	**N/A**	**N/A**
Ref. [49]	**0.18-μm CMOS**	**5.8**	**1.8**	**14.4**	**3.7**	**12.5**	**-15**	**N/A**	**N/A**
Ref. [50]	**0.18-μm CMOS**	**6**	**1.8**	**6.48**	**3**	**7.1**	**-10**	**N/A**	**N/A**
Ref. [51]	**0.13-μm CMOS**	**3 - 5**	**1.5**	**45**	**4**	**25.8**	**-11**	**1.5**	**N/A**
Ref. [52]	**0.13-μm CMOS**	**2 - 4.6**	**1.5**	**16.5**	**3.5**	**9.5**	**-10**	**N/A**	**N/A**
Ref. [53]	**90-nm CMOS**	**0.2 - 3.2**	**1.2**	**25**	**1.76**	**15.5**	**-10**	**2.4**	**N/A**
Ref. [54]	**0.13-μm CMOS**	**18**	**1.5**	**36**	**4.1**	**22.4**	**-7**	**2**	**N/A**

Chapter 3

Optimization on SCR Device With Low Capacitance for RF ESD Protections

Silicon-controlled rectifier (SCR) has been used as an effective on-chip electrostatic discharge (ESD) protection device in CMOS technology due to the highest ESD robustness in nanoscale ICs. In this chapter, SCR realized in waffle layout structure is proposed to improve ESD current distribution efficiency for ESD protection and to reduce the parasitic capacitance. The waffle layout structure of SCR can achieve smaller parasitic capacitance under the same ESD robustness. With smaller parasitic capacitance, the degradation on RF circuit performance due to ESD protection devices can be reduced. The proposed waffle SCR with low parasitic capacitance is suitable for on-chip ESD protection in RF ICs. Besides, the desired current to trigger on the SCR device with waffle layout structure and its turn-on time has also been investigated in silicon chip.

3.1. Background

Electrostatic discharge (ESD), which is the major reliability issue for integrated circuits (ICs), must be taken into consideration during the design phase of all ICs. In the nanoscale CMOS technologies, the thinner gate oxide in the advanced processes greatly degrades the ESD robustness of IC products. Against ESD damages, ESD protection devices must be included in ICs [1]-[4]. A general concept of on-chip ESD protection for RF ICs is illustrated in Fig. 3.1 [15], [65]. The ESD protection devices must be provided for all I/O pads in RF ICs. The parasitic capacitance (C_{ESD}) of ESD protection device is one of the most important design considerations for RF ICs [2], [7], [9], [66]. The parasitic capacitance of ESD protection devices will degrade the high frequency performance of RF ICs. The ESD protection device realized in the conventional stripe layout structure often has a large parasitic capacitance which may not be tolerated in RF ICs. The parasitic capacitance induces RC delay on the signal path and lowers the operating frequency of RF ICs. Moreover, the parasitic capacitance of ESD protection device loses RF signals from the pad to ground. For

RF receivers, noise figure (NF) is an important merit. Adding ESD protection devices to the RF receiver had been proven to degrade the noise figure [36]. For example, the overall noise figure of the low-noise amplifier (LNA) with ESD protection device in Fig. 3.2 is

$$NF_{total} = NF_{ESD} + \frac{NF_{LNA} - 1}{L^{-1}} = L \cdot NF_{LNA} \tag{3.1}$$

where L is the power loss of ESD protection device, and NF_{LNA} and NF_{ESD} denote the noise figures of the low-noise amplifier and ESD protection device, respectively. The noise figure of the ESD protection device is equal to its power loss because ESD protection device is a passive reciprocal network [12]. To mitigate the RF performance degradation caused by ESD protection device, its parasitic capacitance must be minimized. Therefore, devices with large ratio of ESD robustness to parasitic capacitance are desired. The figure of merit (FOM) used in this chapter is V_{MM}/C_{ESD}, where V_{MM} is the machine-model (MM) ESD level and C_{ESD} is the parasitic capacitance of ESD protection device.

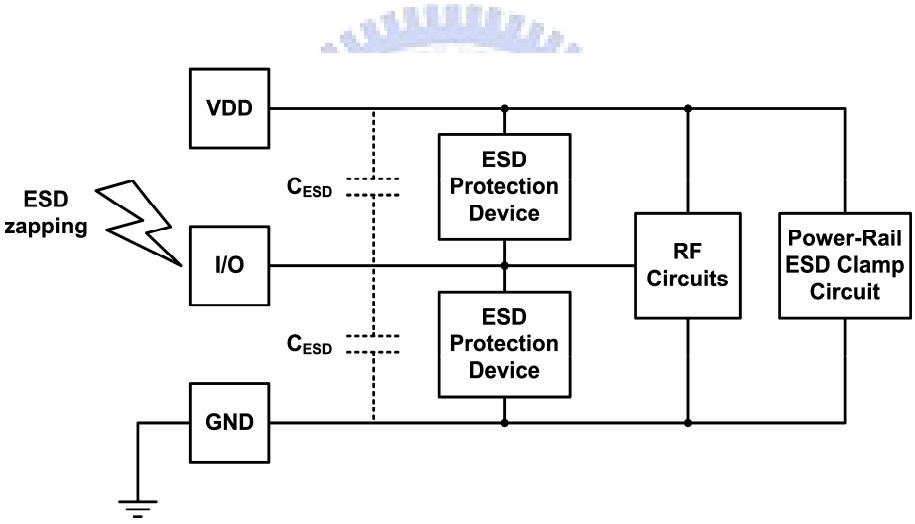


Fig. 3.1. A general concept of on-chip ESD protection in RF ICs.

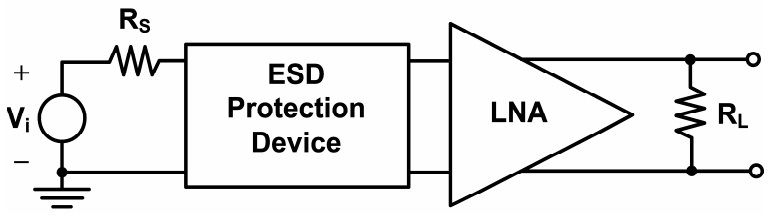


Fig. 3.2. Diagram of the low-noise amplifier (LNA) with ESD protection device.

With the highest ESD robustness within a smaller layout area and lower parasitic capacitance, the silicon-controlled rectifier (SCR) device was reported to be useful for RF ESD protection design [67], [68]. The SCR device has very low holding voltage (V_{hold}, about

~1.5 V in general bulk CMOS processes), so the power dissipation (~ I_{ESD} x V_{hold}) and the joule heating at the SCR device during ESD stresses are significantly less than that at other ESD protection devices, such as the diode, MOS, BJT, or field-oxide device. Therefore, the SCR device can sustain a much higher ESD level within a smaller layout area in CMOS ICs [59], [69]. A smaller layout area introduces less parasitic capacitance. Thus, using SCR device for RF ESD protection can achieve better FOM of V_{MM}/C_{ESD}. Besides, the SCR with holding voltage of about ~1.5 V can be designed safely without latchup danger in advanced CMOS ICs with a low supply voltage.

3.2. SCR Structures

The SCR device was traditionally implemented in the stripe and double-sided layout. Under ESD stresses, ESD current primarily flows through the two edges of SCR, while other two edges do not discharge ESD current, but still contribute to parasitic capacitance. The proposed SCR device with waffle layout structure can discharge ESD current through four edges. Therefore, the FOM of V_{MM}/C_{ESD} can be maximized by using the waffle layout structure to implement SCR.

The MOS transistors in waffle layout structures had been studied [70]. The waffle layout structures for diodes had also been proposed to reduce its parasitic capacitance for ESD protection in high-speed I/O applications [71]. In this section, SCR realized in the waffle structure is investigated in a 0.18-μm CMOS process.

3.2.1. SCR With Stripe Layout

The conventional stripe SCR (SSCR) is shown in Fig. 3.3(a), which is implemented in the stripe and double-sided layout. The anode of SSCR is electrically connected to P+ diffusion and N+ diffusion, which are formed in the N-well. The cathode is electrically connected to N+ diffusion and P+ diffusion, which are formed in the nearby P-well. The shaded regions in the cross-sectional view in Fig. 3.3(a) are the regions of shallow trench isolation in CMOS process. The equivalent circuit of the SCR device, which consists of a PNP and a NPN bipolar transistors, is shown in Fig. 3.4. Because of the reverse-biased junction between the N-well and P-well regions, the SCR device is turned off under normal circuit operating conditions. When a positive ESD stress is zapped from the anode with cathode grounded, the high voltage drop between the anode and cathode causes breakdown on the base-collector junction of BJT. In the meantime, PNP and NPN transistors will be

turned on by the breakdown current. With the positive-feedback mechanism [62] of the cross-coupled bipolar transistors, the SCR device becomes highly conductive. Therefore, the ESD current can be quickly discharged by the SCR device.

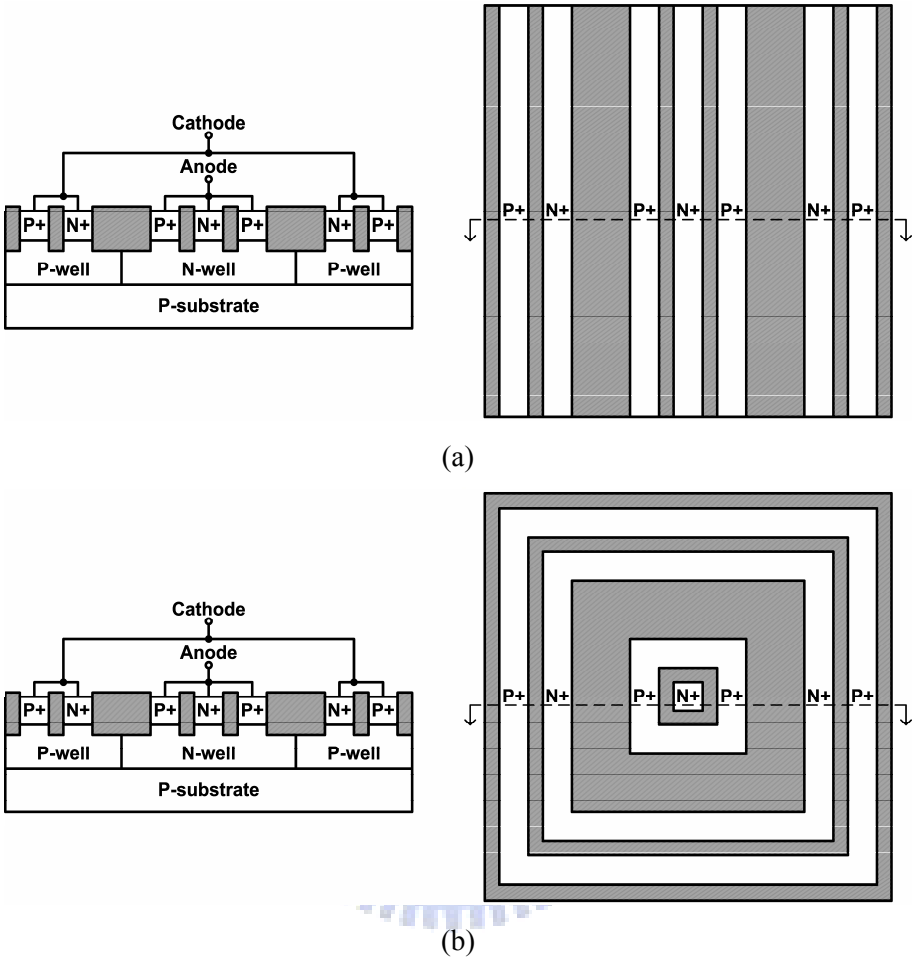


Fig. 3.3. Device cross-sectional view and layout top view of (a) stripe SCR (SSCR), and (b) waffle SCR (WSCR).

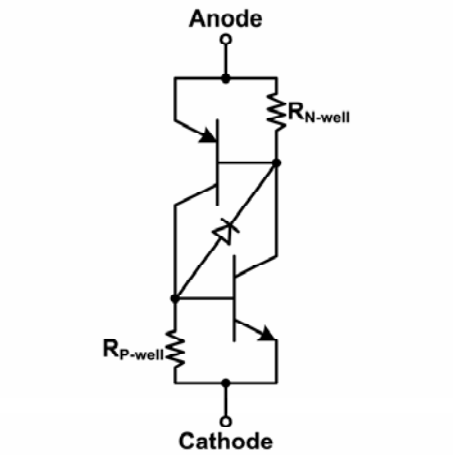


Fig. 3.4. Equivalent circuit of the SCR device.

While a positive ESD stress is zapped from the anode with cathode grounded, the discharge path of the SCR device is P+/N-well/P-well/N+. The ESD currents primarily flow through only two edges of the N-well in SSCR. The other two edges of the N-well in SSCR are unused. While a negative ESD stress is zapped from the anode with cathode grounded, the discharge path in the SCR device is the parasitic N-well/P-well diode. The ESD currents still flow through only two edges of the N-well in SSCR. The other two edges of the N-well in SSCR are not used to bypass ESD current.

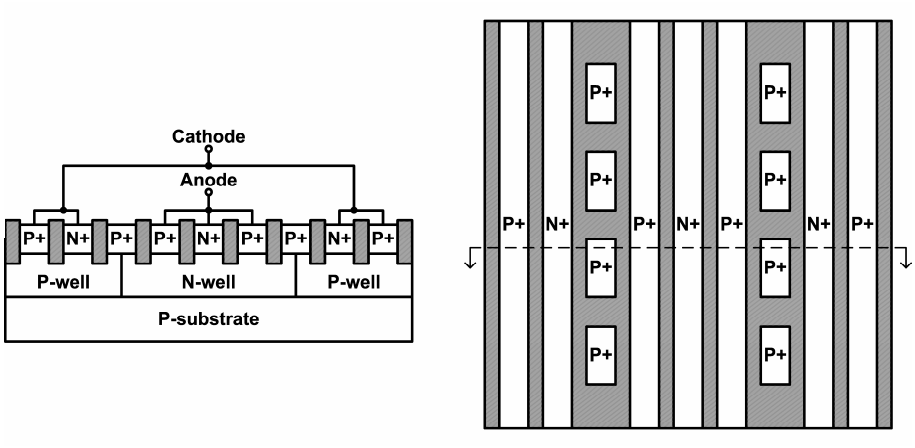
3.2.2. SCR With Waffle Layout

Fig. 3.3(b) shows the proposed waffle SCR (WSCR). The anode of WSCR is electrically connected to P+ diffusion and N+ diffusion, which are formed in the N-well. The cathode surrounds the anode, and is electrically connected to N+ diffusion and P+ diffusion, which are formed in the nearby P-well. WSCR can discharge both positive and negative ESD current in four edges of the device.

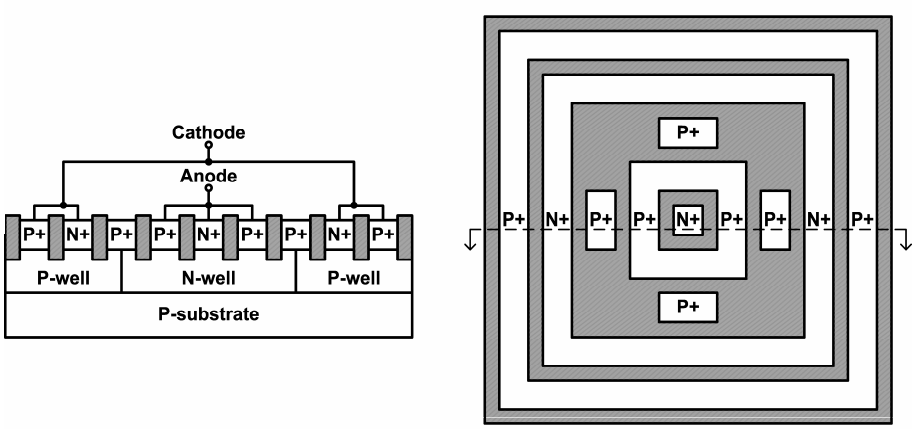
3.2.3. Modified SCR With Stripe Layout

In Figs. 3.3(a) and 3.3(b), the trigger voltage ($V_{trigger}$) of the SSCR or WSCR under positive stress is the breakdown voltage of the N-well/P-well junction. The modified SCR can improve the turn-on efficiency and reduce the trigger voltage. As shown in Fig. 3.5(a), the trigger P+ diffusion is added across the N-well/P-well junction in the stripe p-modified SCR (SPMSCR) to reduce the junction breakdown voltage. When a positive or negative ESD stress is zapped from anode to cathode, the ESD currents primarily flow through two edges of the device.

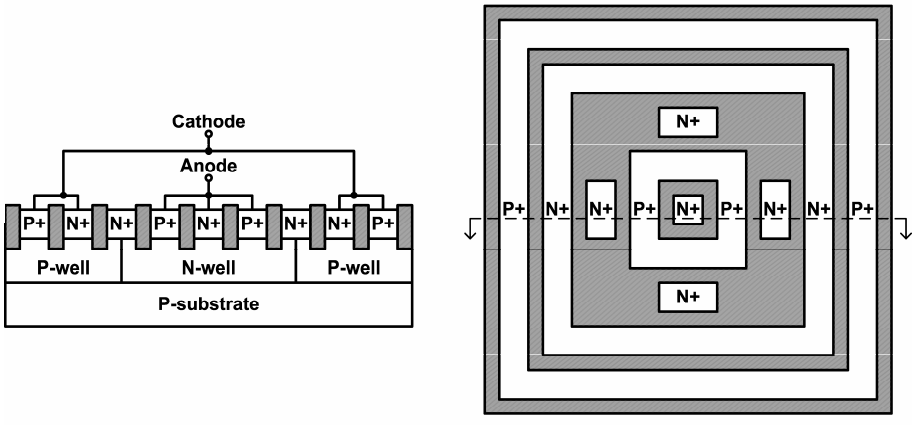
Since the large trigger diffusion often increases the parasitic capacitance, the SPMSCR was implemented with separated trigger diffusion areas to evaluate the device characteristics and ESD robustness. The trigger diffusion areas of $SPMSCR_1$ and $SPMSCR_2$ are 123.2 μm^2 and 242.48 μm^2, respectively, as listed in Table 3.1.



(a)



(b)



(c)

Fig. 3.5. Device cross-sectional view and layout top view of (a) stripe p-modified SCR (SPMSCR), (b) waffle p-modified SCR (WPMSCR), and (c) waffle n-modified SCR (WNMSCR).

Table 3.1

Comparisons on Measured Device Characteristics of SCR Under Different Test Structures

Structure	Name	Device Size (μm^2)	Trigger Diffusion		$V_{trigger}$ (V)	R_{on} (Ω)	+/- It_2 (A)	+/- V_{HBM} (kV)	+/- V_{MM} (kV)	C_{ESD}@ 2.4GHz (fF)	+/- FOM @ 2.4GHz (V/fF)
			Type	Area (μm^2)							
Stripe	SSCR	60.62×60.62		0	16.92	0.95	>6 / <-6	>8 / <-8	1.80 / -0.90	118.51	15.2 / -7.6
Stripe	$SPMSCR_1$	60.62×60.62	P+	123.2	12.52	1.09	>6 / <-6	>8 / <-8	1.63 / -0.75	178.47	9.1 / -4.2
Stripe	$SPMSCR_2$	60.62×60.62	P+	242.48	12.54	1.02	>6 / <-6	>8 / <-8	1.68 / -0.95	212.81	7.9 / -4.5
Waffle	WSCR	60.62×60.62		0	16.17	0.96	>6 / -5.2	>8 / <-8	1.53 / -0.65	77.17	19.8 / -8.4
Waffle	$WPMSCR_1$	60.62×60.62	P+	70.24	11.91	1.08	>6 / -5.0	>8 / <-8	1.52 / -0.55	115.39	13.2 / -4.8
Waffle	$WPMSCR_2$	60.62×60.62	P+	140.48	11.81	1.10	>6 / -4.7	>8 / <-8	1.59 / -0.55	139.63	11.4 / -3.9
Waffle	$WPMSCR_3$	60.62×60.62	P+	264.96	12.55	1.22	>6 / -4.8	>8 / <-8	1.56 / -0.65	165.25	9.4 / -3.9
Waffle	$WNMSCR_1$	60.62×60.62	N+	70.24	10.08	0.99	>6 / -4.3	>8 / -7.0	1.53 / -0.65	178.67	8.6 / -3.6
Waffle	$WNMSCR_2$	60.62×60.62	N+	140.48	10.08	1.08	>6 / -4.1	>8 / -7.5	1.48 / -0.60	205.68	7.2 / -2.9
Waffle	$WNMSCR_3$	60.62×60.62	N+	264.96	11.00	1.03	>6 / -4.1	>8 / <-8	1.50 / -0.53	204.78	7.3 / -2.6

3.2.4. Modified SCR With Waffle Layout

With the trigger P+ diffusion across the N-well/P-well junction, the proposed waffle p-modified SCR (WPMSCR) is shown in Fig. 3.5(b). The WPMSCR can discharge both positive and negative ESD current through the four edges of the device, so the FOM of V_{MM}/C_{ESD} can be increased. The WPMSCR was also implemented with separated trigger diffusion areas to evaluate the device characteristics and ESD robustness. The trigger diffusion areas of $WPMSCR_1$, $WPMSCR_2$, and $WPMSCR_3$ are 70.24 μm^2, 140.48 μm^2, and 264.96 μm^2, respectively, as listed in Table 3.1.

The trigger P+ diffusion can be replaced by the trigger N+ diffusion. As shown in Fig. 3.5(c), the trigger N+ diffusion is added across the N-well/P-well junction of the waffle n-modified SCR (WNMSCR) to characterize the ESD robustness and high frequency performances.

3.2.5. Metal Routing Strategy

The top metal (metal 6) in a 0.18-μm CMOS process, which is far from the grounded P-substrate, is used for routing on the anode of each SCR device. This is critical to reduce the parasitic capacitance at the I/O pad in RF circuits. The bottom metal (metal 1) is used for routing on the cathode of each SCR device. With such a metal routing strategy, the parasitic capacitance between the anode and cathode of SCR device can be further reduced [22].

All the aforementioned devices have been fabricated in a 0.18-μm CMOS process. The size of each SCR device in layout is kept at 60.62 x 60.62 μm^2. The FOM of V_{MM}/C_{ESD} of SCR devices in different layout styles have been measured to investigate their effectiveness.

3.3. Experimental Results and Discussion

3.3.1. Transmission Line Pulsing (TLP) Measurement

The trigger voltage ($V_{trigger}$), the secondary breakdown current (I_{t2}), and the turn-on resistance (R_{on}) in the holding region of the fabricated SCR devices under positive stresses were characterized by the TLP system. The I_{t2} of the devices under negative stresses were also evaluated by the TLP system. The TLP-measured I-V curves for SSCR and WSCR are shown in Figs. 3.6(a) and 3.6(b), respectively. Excluding the difference in trigger voltages, the similar I-V curves were obtained in the other SCR devices. The trigger voltages among the SCR devices under different trigger diffusion areas are compared in Fig. 3.7. Both SSCR and WSCR under positive stresses are triggered at about 16-17 V. With the P+ or N+ trigger diffusion added into the modified SCR, the trigger voltages can be significantly reduced. The TLP-measured holding voltage under positive stresses of the stripe and the waffle SCRs are ~1.5 V, which is lower than 1.8-V VDD. To increase the holding voltage, one solution is to decrease the $R_{P\text{-well}}$ in SCR device (Fig. 3.4). In other words, the holding voltage can be increased by lower the voltage drop across the base and emitter terminals of the NPN transistor in SCR device. The other solution is to realize the SCR device with a diode in series. The TLP-measured turn-on R_{on} under positive stresses of the stripe and the waffle SCRs in high-current holding region are as low as ~1 Ω. The I_{t2} of all SCR devices under positive stresses exceed 6 A, which is the measurement limitation of a given TLP system. The secondary breakdown currents of all SCR devices under negative stresses are 4.1 A at least. Because of the reduction of N+ diffusion area in N-well in the proposed waffle layout structure, the secondary breakdown currents of devices in waffle layout were lower than those with the conventional stripe layout. The measured results on the characteristics of the fabricated SCR devices are listed in Table 3.1.

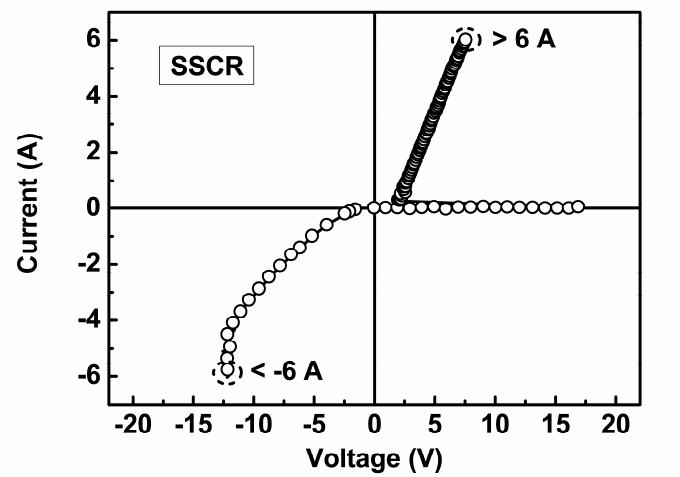
3.3.2. ESD Robustness

The human-body-model (HBM) and machine-model (MM) ESD robustness of the fabricated SCR devices were evaluated by the ESD simulator. The I_{t2} is approximately linear to the HBM ESD level of the device under test (DUT). The relationship between the HBM ESD level (V_{HBM}) and the I_{t2} is

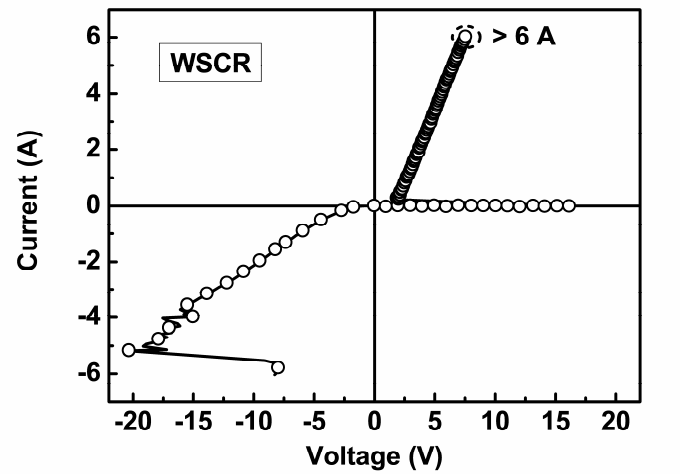
$$V_{HBM} \approx (1500 + R_{on}) \times It_2 \tag{3.2}$$

where R_{on} is the turn-on resistance of DUT. Since the I_{t2} of each SCR device is larger than 6

A, the HBM ESD robustness of each SCR device is quite high. After measurement, the positive HBM ESD levels of all SCR devices were found to exceed 8 kV, which verifies the relationship between V_{HBM} and I_{t2}. The positive MM ESD levels are within the range of 1.4-1.8 kV. The negative HBM ESD levels of all SCR devices are 7 kV at least, and negative MM ESD levels are within the range of 0.5-1.0 kV, as listed in Table 3.1.



(a)



(b)

Fig. 3.6. The TLP-measured current-voltage (I-V) characteristics of (a) SSCR and (b) WSCR.

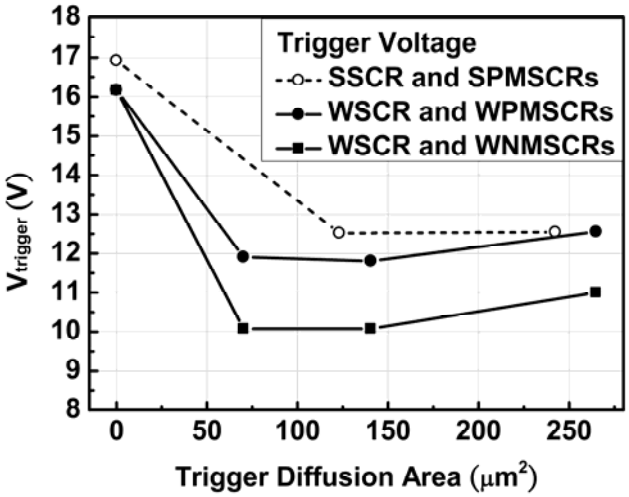


Fig. 3.7. The dependence of TLP-measured $V_{trigger}$ on the trigger diffusion area of SCR devices with different layout structures.

3.3.3. Parasitic Capacitance

The SCR devices were implemented with ground-signal-ground (G-S-G) pads to facilitate on-wafer two-port S-parameter measurement. The two-port S-parameters were measured by using the vector network analyzer HP 8510C. During the S-parameter measurement, the anode of the SCR device was connected to port 1 and biased at 0.9 V, which is VDD/2 in the given 0.18-μm CMOS process, and the cathode was connected to port 2 and biased at 0 V.

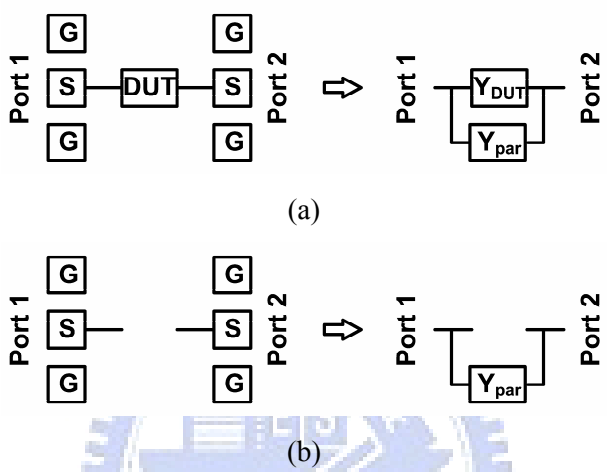
In order to extract the characteristics of the intrinsic device in high frequency, the parasitic effects of the bond pad must be removed. The test patterns, one including the DUT and the other excluding the DUT, as shown in Figs. 3.8(a) and 3.8(b), were fabricated in the same experimental test chip. The Y_{11}-parameter can be obtained from the measured two-port S-parameters by using

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{Z_0\left((1 + S_{11})(1 + S_{22}) - S_{12}S_{21}\right)} \tag{3.3}$$

where Z_0 is the termination resistance and equals to 50 Ω [72]. The measured Y-parameter of the including-DUT pattern is labeled as Y_{11_meas}, and the measured Y-parameter of the excluding-DUT pattern is labeled as Y_{11_par}. The intrinsic device characteristics (Y_{11_DUT}) can be obtained by subtracting Y_{11_par} from Y_{11_meas}. The parasitic capacitance (C_{ESD}) of each SCR was extracted from the Y-parameter of the intrinsic device by using

$$C_{ESD} = \frac{\mathrm{Im}(Y_{11\_DUT})}{2\pi f} \tag{3.4}$$

where f is the operating frequency. Fig. 3.9 shows the extracted capacitances from 2.4 GHz to 5 GHz of the SCR devices. For each SCR device, the parasitic capacitance is decreasing as the frequency increasing. Because the parasitic capacitance was in series with a resistor, which is caused by the parasitic N-well resistance and P-well resistance in each SCR device, the parasitic capacitance in high frequency is decreasing with the increasing frequency. The parasitic capacitances of the fabricated SCRs at 2.4 GHz (for wireless LAN applications) were listed in Table 3.1.



(a)

(b)

Fig. 3.8. The layout top view with ground-signal-ground (G-S-G) pads and the equivalent model of (a) including-DUT pattern and (b) excluding-DUT pattern.

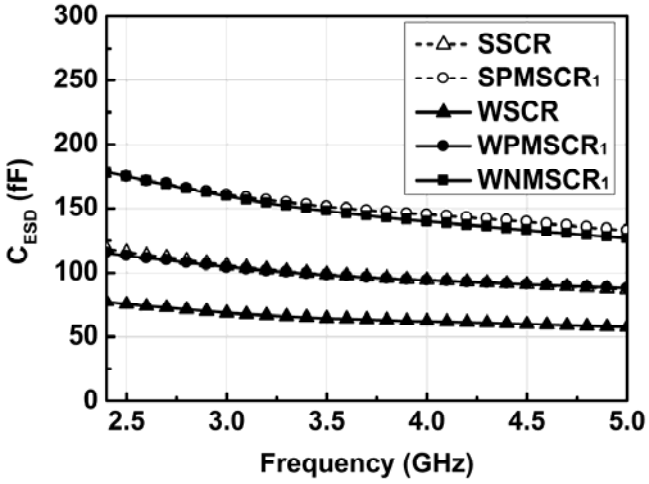


Fig. 3.9. The extracted capacitances of the SCR devices from 2.4 GHz to 5 GHz.

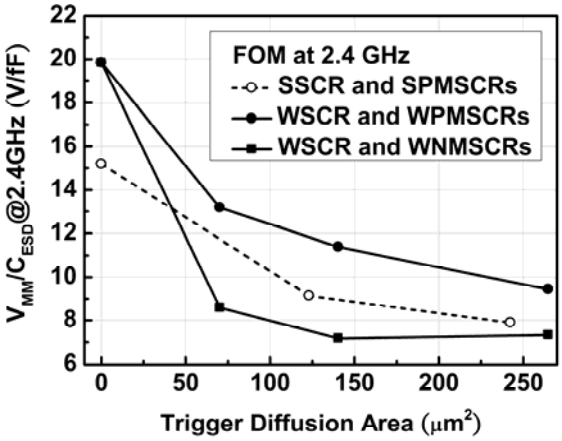
3.3.4. Comparison on FOM

The FOM (V_{MM}/C_{ESD}) of SSCR, WSCR , SPMSCR, WPMSCR, and WNMSCR under positive and negative ESD stresses are compared in Figs. 3.10(a) and 3.10(b), respectively.

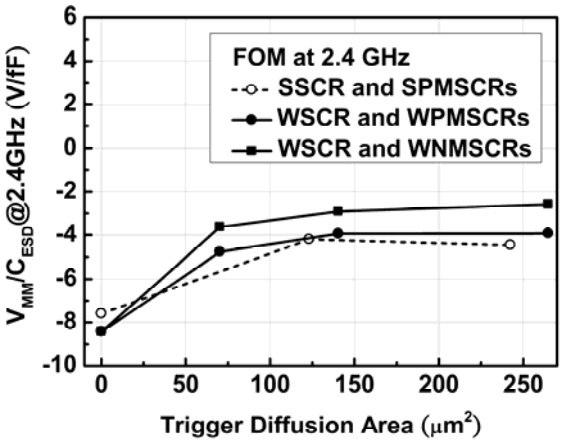
Even though the positive V_{MM} of WSCR is worse than the SSCR due to the reduction of the N-well area in the proposed waffle layout structure, the parasitic capacitance can be greatly reduced. Without the trigger diffusion, the FOM of the proposed WSCR under positive stress has an increase of about 30%, as compared with the conventional SSCR. With the trigger diffusion, the FOM of the proposed WPMSCR under positive stress has an increase of about 25%, as compared with the conventional SPMSCR. Although the FOM is decreased with the increase of trigger diffusion area, the trigger voltage can be significantly reduced to effectively protect the RF circuits. The decreased FOM of SCR with trigger diffusion was due to the increased junction capacitance of the trigger diffusion. Comparison on the FOM among the SCR devices, the best FOM under positive stress was found in WPMSCR. The negative MM ESD levels of the SCR devices with waffle layout structures were lower than the SCR devices with stripe layout structures due to the reduction of N+ diffusion area in N-well in the proposed waffle layout structure. The FOM of stripe and waffle structure devices under negative stresses are almost the same. However, the FOM of waffle SCR under positive stress can be increased, which can increase the PS-mode ESD robustness (the critical ESD-test-combination for RF circuits).

3.3.5. Trigger Mechanism

Among the SCR devices, WPMSCR was demonstrated to have the improved FOM and the best RF performance. To further reduce the trigger voltage of WPMSCR, the trigger current ($I_{trigger}$) can be injected into the P+ trigger diffusion to enhance the turn-on efficiency. To investigate the suitable trigger current for a WPMSCR, the curve tracer (Tektronix 370B) was used to measure the dc current-voltage (I-V) curves of the WPMSCR, as shown in Fig. 3.11. The dc I-V curves of each WPMSCR under different trigger currents are shown in Figs. 3.12(a) - 3.12(c). The static trigger voltages of WPMSCR devices without trigger currents are larger than the dynamic (TLP) trigger voltages listed in Table 3.1, which were measured by TLP and involved in the dV/dt transient current of the ESD-like pulse. The dependences of the static trigger voltage of WPMSCR devices on the trigger current are compared in Fig. 3.13.



(a)



(b)

Fig. 3.10. The dependence of FOM (V_{MM}/C_{ESD}) at 2.4 GHz under (a) positive and (b) negative ESD stresses on the trigger diffusion area of SCR devices under different layout structures.

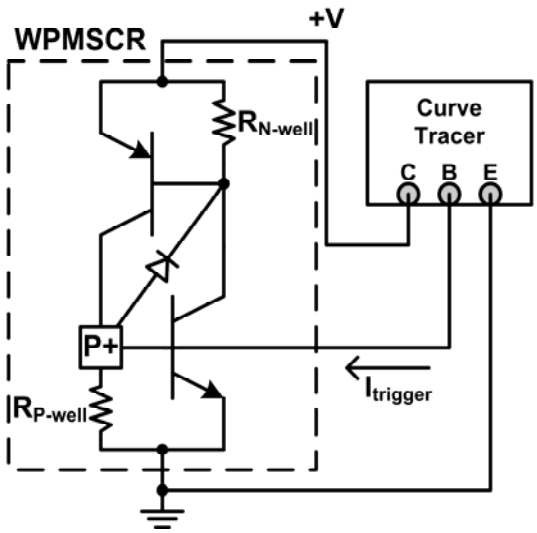
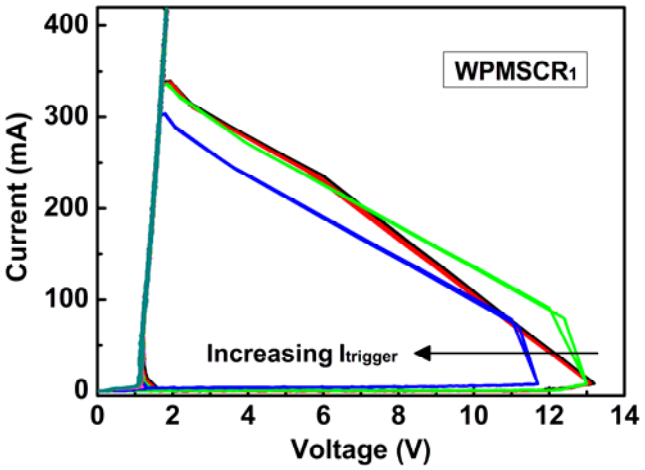
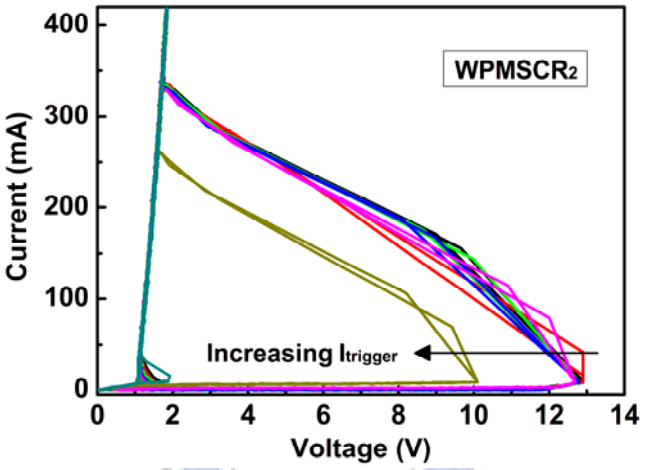


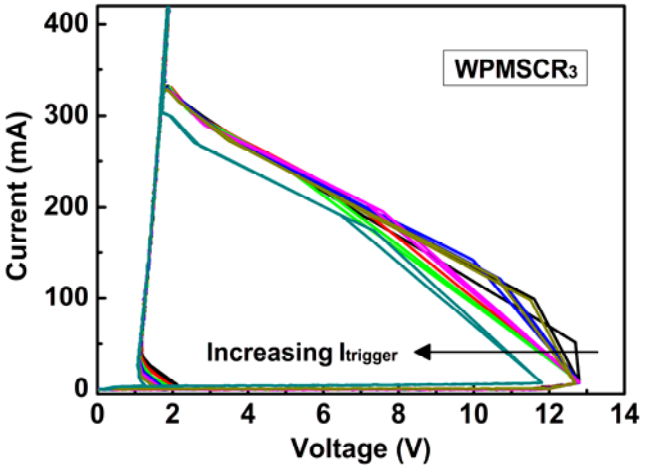
Fig. 3.11. Measurement setup to find the dc I-V curves of each WPMSCR devices under different trigger currents.



(a)



(b)



(c)

Fig. 3.12. The dc I-V curves of (a) $WPMSCR_1$, (b) $WPMSCR_2$, and (c) $WPMSCR_3$, under different trigger currents.

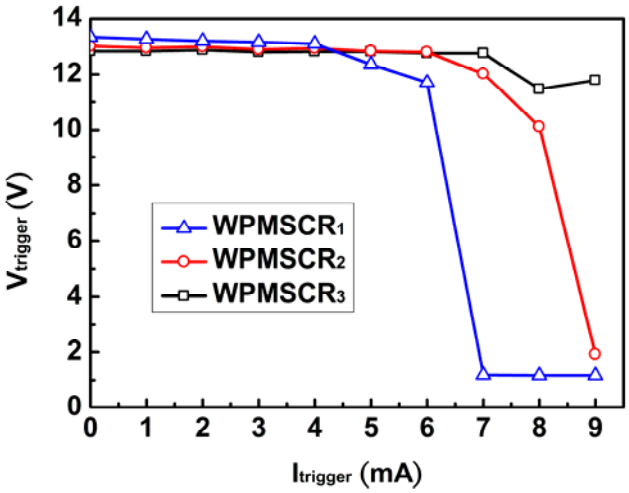


Fig. 3.13. Dependences of the trigger voltages of WPMSCR devices on the trigger current.

The measurement setup and experimental results of dc I-V curves of the base-emitter junction diode of the WPMSCR are shown in Figs. 3.14 and 3.15, respectively. The trigger voltage of the WPMSCR can be significantly reduced as long as the base-emitter junction diode of the NPN transistor is turned on. If the trigger current is continually increased, the trigger voltage of each WPMSCR devices will be reduced to a value close to their holding voltages. With large enough trigger current, the SCR can be readily turned on to clamp the voltage across its anode and cathode. Before the SCR is turned on, the P-well resistance of each WPMSCR can be extracted as the reciprocal of the slope of each curve in Fig. 3.15.

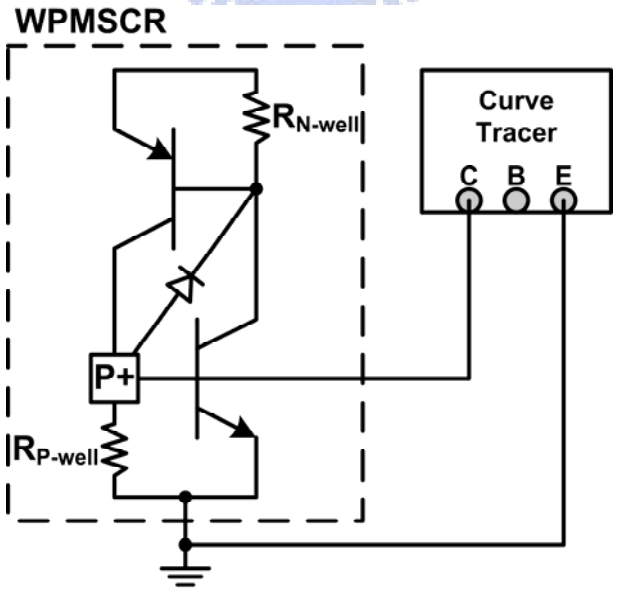


Fig. 3.14. Measurement setup to find the dc I-V curves of the base-emitter junction diode of WPMSCRs.

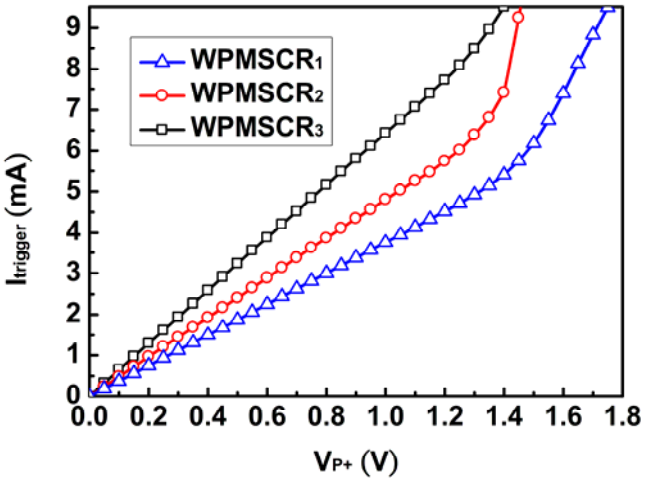


Fig. 3.15. The dc I-V curves of the base-emitter junction diode of WPMSCRs.

3.3.6. Turn-On Speed

In order to investigate the turn-on speed of the WPMSCR devices with different trigger diffusion areas, the experimental setup to measure the required turn-on times of the WPMSCR devices is illustrated in Fig. 3.16. A 5-V voltage bias was connected to the anode of a WPMSCR device through a 10-Ω resistance, which was used to limit the sudden large transient current from power supply when the WPMSCR is turned on. The cathode of the SCR was grounded. The turn-on time of the WPMSCR is defined as the time for the WPMSCR to enter its low-voltage holding region. The turn-on time of WPMSCR should be relative to the rise time of the trigger pulse. In this case, we use the pulse with 10-ns rise time to simulate the WPMSCR under HBM/MM ESD stresses. The pulse with amplitude of 5 V, rise time of 10 ns, and pulse width of 100 ns was applied to the trigger node. The measured voltage waveforms on the trigger nodes and anodes, and the turn-on times for three WPMSCR devices with different trigger diffusion areas are shown in Figs. 3.17(a) - 3.17(c). The turn-on times of WPMSCR devices are 10.9 ns, 11.4 ns, and 15.3 ns, respectively. The turn-on time is reduced when the WPMSCR is drawn with a smaller trigger diffusion area. The measured turn-on times and the measured $R_{P\text{-well}}$ of the three WPMSCR devices under different trigger diffusion areas are compared in Fig. 3.18. The too much trigger diffusion in WPMSCR will decrease the FOM (V_{MM}/C_{ESD}) and degrade the turn-on speed. Therefore, the most suitable trigger diffusion area is found in the $WPMSCR_1$.

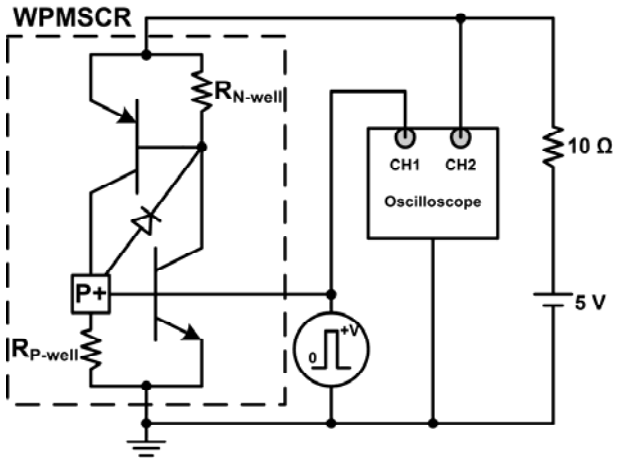


Fig. 3.16. Measurement setup to find the turn-on time of WPMSCR devices under different voltage pulses.

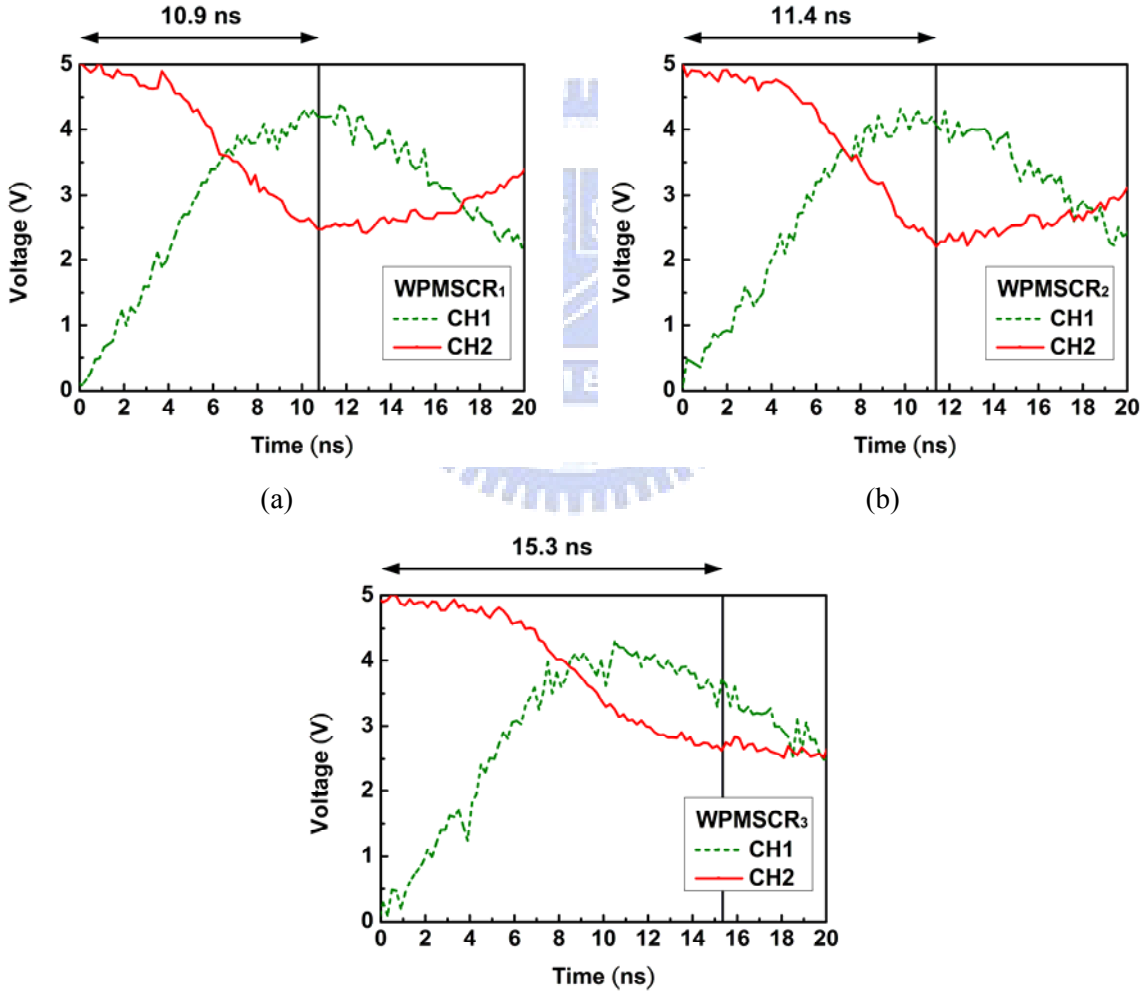


Fig. 3.17. The measured voltage waveforms on the anode of (a) $WPMSCR_1$, (b) $WPMSCR_2$, and (c) $WPMSCR_3$, while the WPMSCR is triggering by the 5-V pulse into the trigger node.

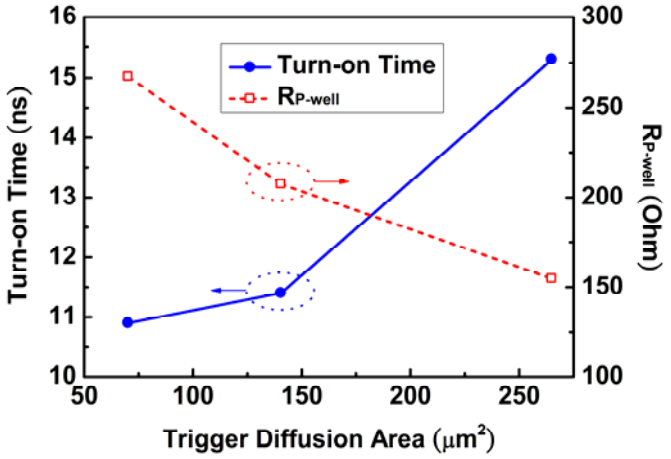


Fig. 3.18. Dependence of the turn-on time and the $R_{P\text{-well}}$ of WPMSCRs on the different trigger diffusion area.

3.3.7. Discussion

According to the experimental results of SCR devices with different layout structures, the SCR devices with waffle layout structures have the better ESD robustness under the same parasitic capacitance. In other words, the parasitic capacitance of each SCR device in waffle layout has been reduced under the same ESD robustness. The proposed WSCR and WPMSCRs are more suitable for RF ESD protection because of the reduced parasitic capacitance. For faster turn-on speed, the trigger voltage of the WPMSCRs can be further reduced by additional trigger circuit to effectively protect the RF circuits against ESD damages. A low-parasitic-capacitance ESD detection and trigger circuit should be developed to enhance the turn-on speed of the proposed waffle SCR for ESD protection in RF ICs.

3.4. Summary

The proposed SCR devices with waffle layout structure had been successfully verified in a 0.18-μm CMOS process. As compared with the conventional stripe SCR devices, the proposed WSCR and WPMSCR have been demonstrated to improve ESD robustness under the same parasitic capacitance. The FOM (V_{MM}/C_{ESD}) of the proposed WPMSCR under positive ESD stresses has an increase of about 25%, as compared to the conventional SPMSCR. Although the FOM is decreased with the increased trigger diffusion area, the trigger voltage can be reduced to effectively protect the RF circuits against ESD damages. The FOM of stripe and waffle SCR under negative ESD stresses are almost the same in this study. The trigger voltage of WPMSCR can be further reduced by injecting trigger current to the P+ trigger diffusion. The dependences of the trigger voltage of WPMSCR on the trigger

current had also been investigated. Besides, the dependence of turn-on time on trigger diffusion area had been investigated. With the investigation on trigger current and turn-on time, the ESD detection circuit can be properly designed to quickly trigger on the WPMSCR under ESD stress conditions.

Chapter 4

ESD Protection Design on An Ultra-Wideband Power Amplifier With Waffle-Structured SCR

With the smaller layout area and parasitic capacitance under the same electrostatic discharge (ESD) robustness, silicon-controlled rectifier (SCR) has been used as an effective on-chip ESD protection device in radio-frequency (RF) IC. The low-capacitance waffle-structured SCR is applied to an UWB RF power amplifier (PA). The PA co-designed with the waffle-structured SCR has been designed and fabricated in a 130-nm CMOS process. Before ESD stress, the RF performances of the ESD-protected PA are as well as that of the unprotected PA. After ESD stress, the unprotected PA is seriously degraded, whereas the ESD-protected PA still keeps the performances well. The measurement results verify that low-capacitance ESD protection strategy with the waffle-structured SCR indeed provides excellent ESD robustness.

4.1. Background

Silicon-controlled rectifier (SCR) device had been reported as an useful RF ESD protection element [67], [68]. With the smaller device size and the excellent ESD robustness, using SCR as ESD protection device introduces less parasitic capacitance. To further reduce the parasitic capacitance, the SCR device in waffle layout structure has been studied. The waffle-structured SCR devices have the minimized ratio of parasitic capacitance to ESD robustness. With the minimized parasitic capacitance, the variation of the parasitic capacitance within ultra-wide band (UWB, 3.1-10.6 GHz) frequencies can also be minimized. SCR device with the minimized ratios of parasitic capacitance to ESD robustness and capacitance variation to ESD robustness is more suitable for the UWB RF applications.

4.2. UWB Distributed Power Amplifier Basics

4.2.1. Conventional Architecture of UWB Class-AB PA

The distributed amplifier is an elegant way to overcome the limitation of maximum gain-bandwidth product [73]. This architecture achieves a gain-delay trade-off without the penalty on bandwidth. Theoretically, this architecture can provide possibly infinite bandwidth with arbitrary gain. Therefore, ultra-wideband amplification can be accomplished.

Fig. 4.1 is the conventional distributed amplifier architecture. Each G_m-cell acts as a transconductor to provide a certain amount of output current corresponding to the input driving voltage signal. While the input driving voltage signal propagates down the input line, each G_m-cell is being excited in succession, producing the output current equal to the transconductance (G_m) of each G_m-cell multiplied by the input driving voltage signal. One half of the output current signals from each G_m-cell propagate backward to the output line termination resistor R_t and are absorbed. The other half of the output current signals ultimately sum in time coherence if the delays of the input and output lines are matched. Therefore, the output current waves sum up coherently in constructive superposition manner.

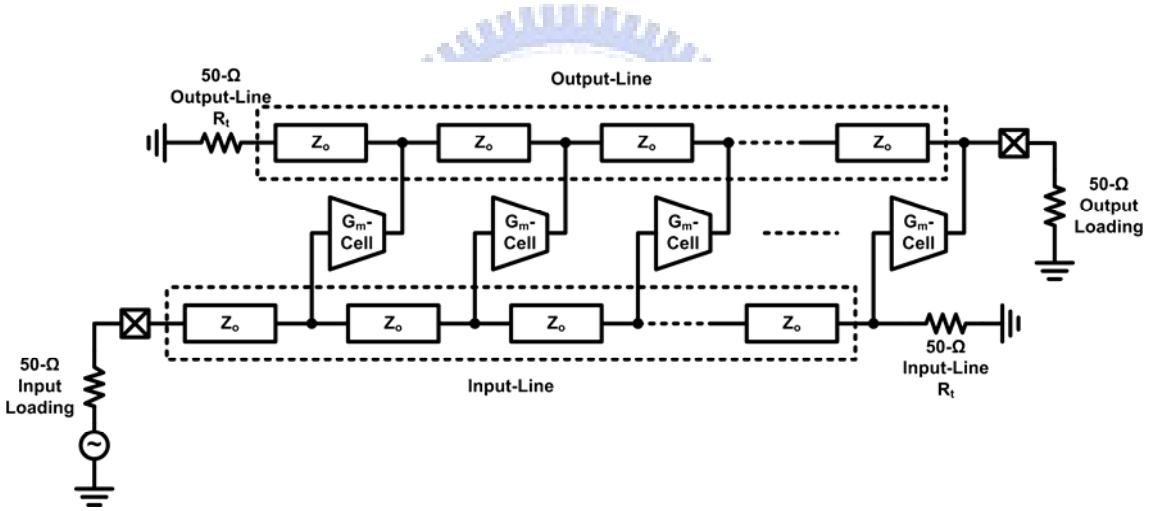


Fig. 4.1. Conventional distributed amplifier architecture.

4.2.2. Load-line Design of Each G_m-Cell

Fig. 4.2 is a typical circuit implementation of this architecture. The cascode topology provides good voltage gain and good isolation. The input and output lines can be synthesized by lumped passive devices, exhibiting a transmission line characteristic impedance of Z_o.

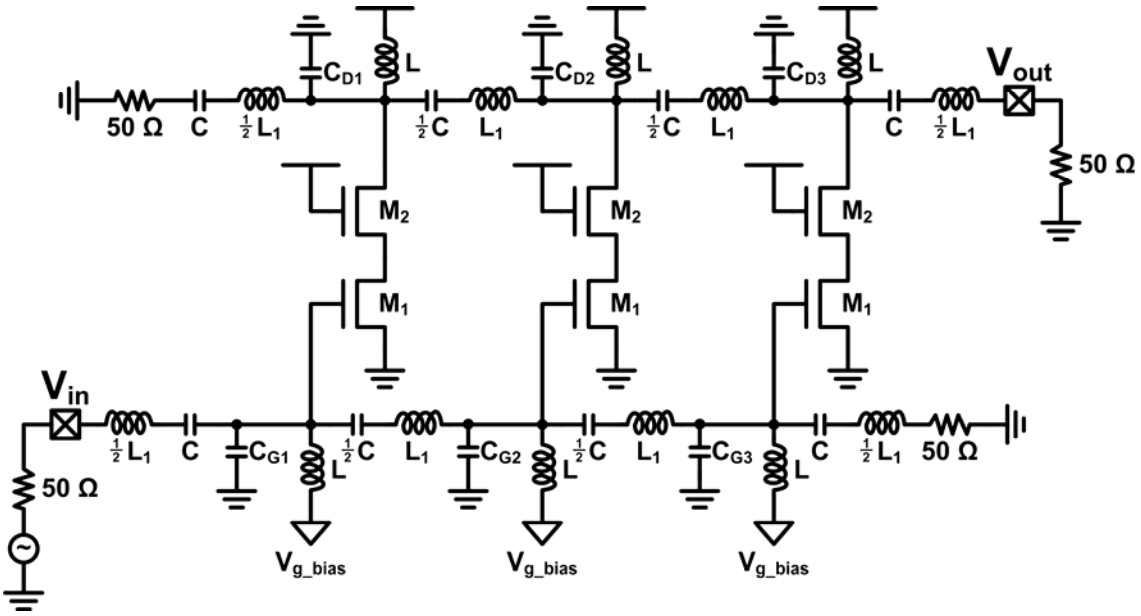


Fig. 4.2. Typical circuit implementation of the conventional distributed amplifier architecture.

Fig. 4.3 shows the loading condition of each G_m-cell. The active device output is loaded with a characteristic impedance of Z_o in both directions. Equivalently, each Gm-cell is loaded with $Z_o/2$. Therefore, it is easy to show that the voltage gain, A_v, of the distributed amplifier is governed by

$$A_V = \frac{1}{2} n \cdot G_m \cdot Z_o \tag{4.1}$$

where n denotes the number of G_m-cell in the distributed amplifier.

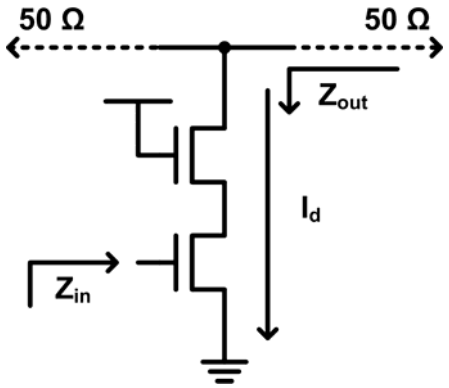


Fig. 4.3. Loading condition of each G_m-cell.

The distributed amplifier architecture provides the capability to achieve simultaneously 50-Ω conjugate match and load-line match. Since each direction seen by the active device output is designed to be 50-Ω for minimum signal reflection, the total loading seen by the

active device output is 25-Ω as the 50-Ω output matching condition. If each G_m-cell is also designed to be with a 25-Ω optimal load-line R_L, as shown in Fig. 4.3, 50-Ω conjugate match and optimal load-line match is simultaneously achieved. Therefore, minimum output signal reflection and PA maximum output power efficiency can be accomplished at the same time. Note that this is impossible in the case of narrowband class-AB PA, which must trade the output 50-Ω matching and the PA maximum output power efficiency, since the optimal load-line impedance is usually much smaller than 50-Ω.

Finally, each output power of each G_m-cell (P_{out_each}) and the total output power appear at the output port (P_{out_total}) can be derived as

$$P_{out\_each} = \frac{1}{2} \cdot \frac{[(V_{MAX} - V_{knee})/2]^2}{R_L} \tag{4.2}$$

and

$$P_{out\_total} = \frac{1}{2} \cdot n \cdot P_{out\_each} . \tag{4.3}$$

4.2.3. Input and Output Line Design

Fig. 4.4 is the distributed amplifier architecture whose input and output lines are synthesized by lumped devices. In such manner, the input and output lines are named as the artificial lines.

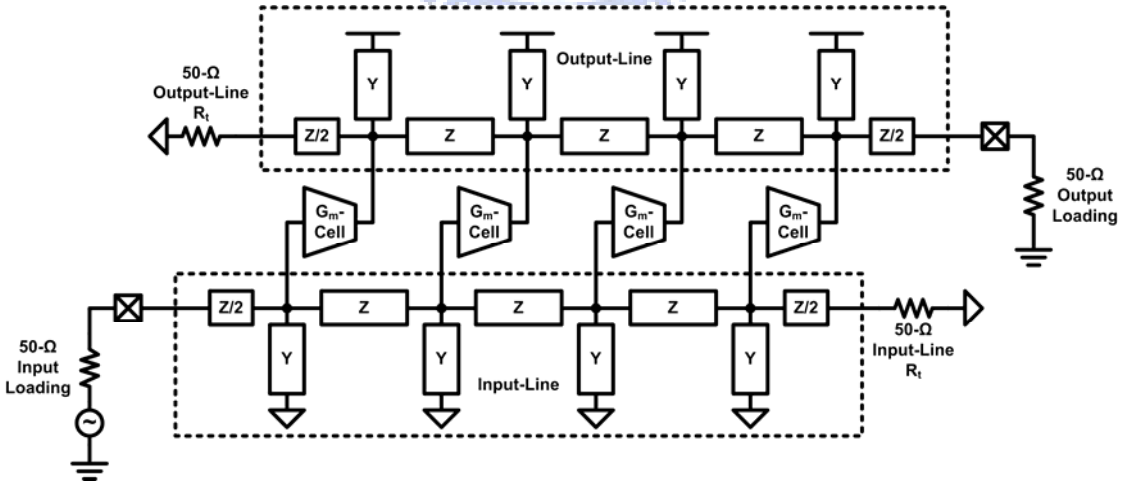


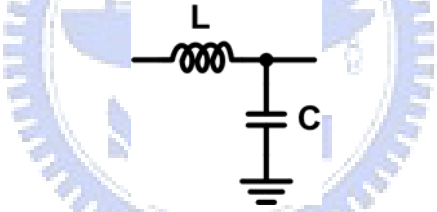
Fig. 4.4. Distributed amplifier with artificial line.

From Fig. 4.4, the characteristic impedance of Z_o of the line is

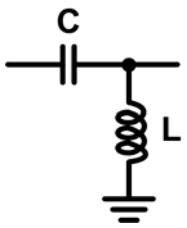
$$Z_o = \frac{Z}{2}\left(1 \pm \sqrt{1 + \frac{4}{Z \cdot Y}}\right) \approx \sqrt{\frac{Z}{Y}},\ if\ \ \frac{4}{Z \cdot Y} >> 1\,. \tag{4.4}$$

To achieve 50-Ω matching, the characteristic impedance Z_o of the line is designed to be 50-Ω. The terminal resistor R_t at the end of the line is also 50-Ω to ensure no signal reflection back to the input and output port.

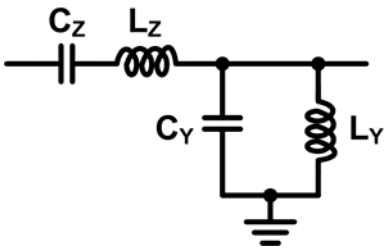
There are three configurations for the artificial lines (Z and Y), namely low-pass line, high-pass line, and band-pass line, as shown in Fig. 4.5. From Fig. 4.4, it can be observed that the overcome of the bandwidth limitation of this architecture comes from the fact that the input and output parasitic capacitances of the G_m-cell are actually parts of the shunt Y devices. That is, the parasitic capacitances are absorbed into the input and output line, causing entirely no degradation on the circuit operation speed. Therefore, until the cutoff frequency of the line itself is approached, the input and output impedance remains constant and equal to Z_o, and the overall operation bandwidth is controlled solely by the input and output lines. It is obvious that the band-pass line structure is the most convenient way to control the overall band-pass type bandwidth.



(a)



(b)



(c)

Fig. 4.5. Detailed artificial line structure and corresponding design equations of (a) low-pass line, (b) high-pass line, and (c) band-pass line.

4.2.4. Design Principle of the UWB Distributed Amplifier

First of all, the optimal load-line (R_L) condition of each G_m-cell is designed as the 25-Ω, as shown in Fig. 4.3. In this case, conjugate matching condition and maximum output power efficiency condition can be simultaneous achieved. Therefore, minimum signal reflection and excellent power efficiency can be guaranteed.

Once the optimal load-line R_L is set, the size and bias of the active devices is set. Also, the output power of each G_m-cell is defined, as shown in (4.2). Therefore, the input and output impedance of the active devices is defined. With the information of the input and output capacitances, along with the bandwidth specification, the input and output artificial line can be designed, according to Fig. 4.5.

Finally, from the output power specification, the number of stages can be defined, according to (4.3), and the ultra-wideband distributed amplifier is ready to work.

4.3. ESD-Protected PA With Waffle-Structured SCR

4.3.1. UWB Class-AB Distributed PA Design

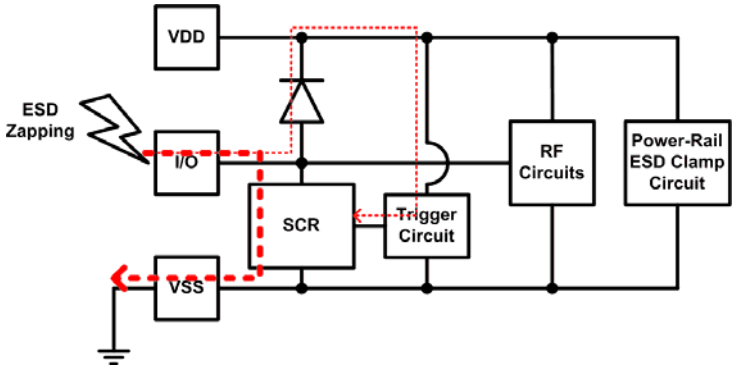
This section presents a fully integrated UWB class-AB PA co-designed with ESD protection circuit. The PA with and without the ESD protection circuit are designed and fabricated in a 130-nm CMOS process. The presented UWB RF PA is a three-stage distributed amplifier (DA). The UWB applications cover the frequency band from 3.1 GHz to 10.6 GHz. The DA is intrinsically suitable for this bandwidth and widely used for PA [74]. The circuit schematic of the PA has been shown in Fig. 4.2. The active core devices (M_1 and M_2) of each stage are in cascode topology. The cascode topology provides good voltage gain and good isolation. It also prevents drain overstress since the voltage swing may approach 2 x VDD at the output node. The device size and voltage/current bias of the cascode pair is designed to produce a particular current that gives the active core device with a 50-Ω loading for its optimal load-line resistance within its operational dynamic range. With such a manner, the DA can simultaneously satisfy a 50-Ω conjugate match and optimal load-line match.

4.3.2. ESD Protection Design

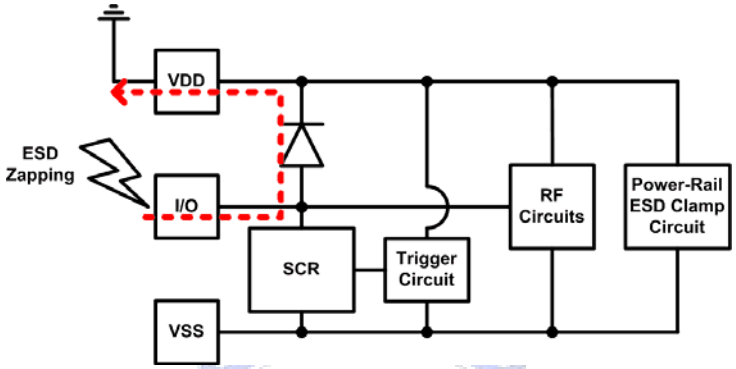
In order to build the trigger circuit to trigger SCR device without increasing the I/O loading capacitance, the new ESD protection strategy for RF ICs is shown in Fig. 4.6. The ESD protection devices are composed of a diode from I/O to VDD and a waffle-structured

SCR from I/O to VSS. The trigger circuit of the waffle-structured SCR between VDD and VSS is separated from the I/O port and not adding the I/O loading. Fig. 4.6(a) shows the discharging path under positive-to-VSS mode (PS-mode) ESD zapping, which is a worse case of ESD events [8]. During PS-mode ESD stress, ESD current will first pass through the diode to VDD, and the trigger circuit will trigger SCR. The major ESD current will be discharged by SCR from the I/O pad to VSS. Under other ESD stress modes, including positive-to-VDD (PD-mode), negative-to-VSS (NS-mode), and negative-to-VDD (ND-mode), the new ESD protection circuit also provides the corresponding current discharging paths with good ESD robustness, which are also shown by the dashed lines in Fig. 4.6. The discharging path for this circuit under NS-mode ESD stresses was the P-well/N-well diodes in SCR. For ND-mode stress, the discharging path was the SCR in series with a diode.

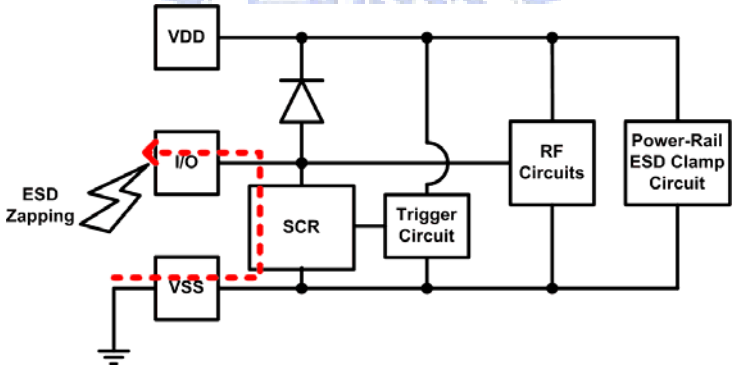
To demonstrate the function of the fast turn-on design on SCR devices under PS-mode stress, the experimental setup to measure the TLP I-V characteristics of the waffle-structured SCR with trigger the circuit is shown in Fig. 4.7. The trigger circuit was composed of a 20-pF capacitance and a 20-kΩ resistance. The RC time constant of the trigger circuit was designed in the order of 10^{-6} - 10^{-7} seconds to detect ESD events. Under normal circuit operation, the trigger port of the SCR was biased at VSS to be kept off. When the ESD pulse was zapping, the trigger port was coupled to high potential by the ESD energy. Therefore, the trigger current will be injected into the trigger port by the CR trigger circuit, and the SCR will be quickly turned on. The TLP-measured I-V curve for CR-triggered SCR is shown in Fig. 4.8. The turn-on voltage of the CR-triggered SCR was reduced to about 5.5 V. The 5.5-V turn-on voltage of CR-triggered SCR is much lower than the breakdown voltage of the gate oxide in the given CMOS process, so the fast turn-on design is proved to be feasible.



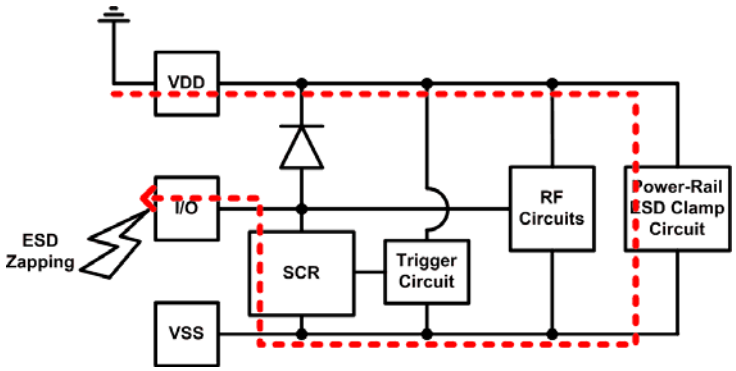
(a)



(b)



(c)



(d)

Fig. 4.6. Application of the waffle-structured SCR device in on-chip ESD protection design for RF ICs with low-capacitance consideration, and the discharging current path under (a) PS-mode, (b) PD-mode, (c) NS-mode, and (d) ND-mode ESD zapping.

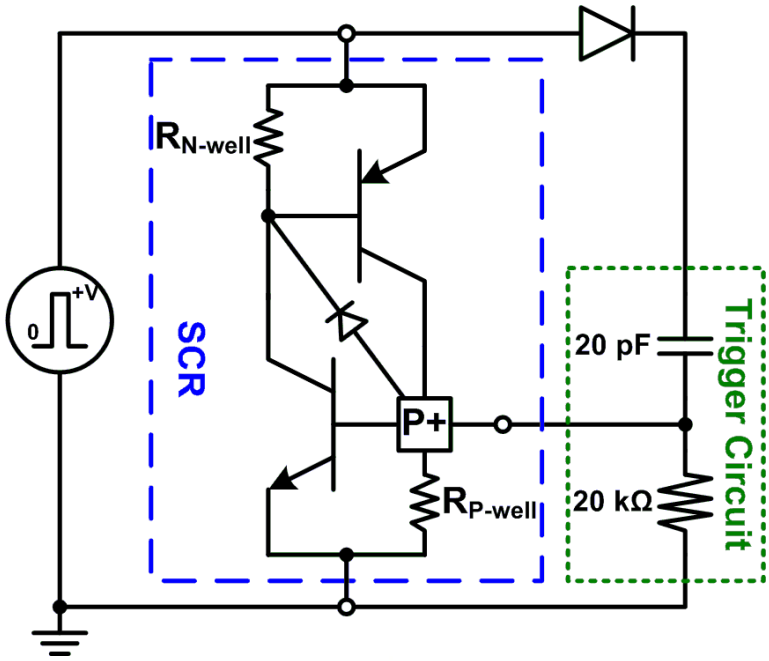


Fig. 4.7. Measurement setup to find I-V characteristics of CR-triggered SCR.

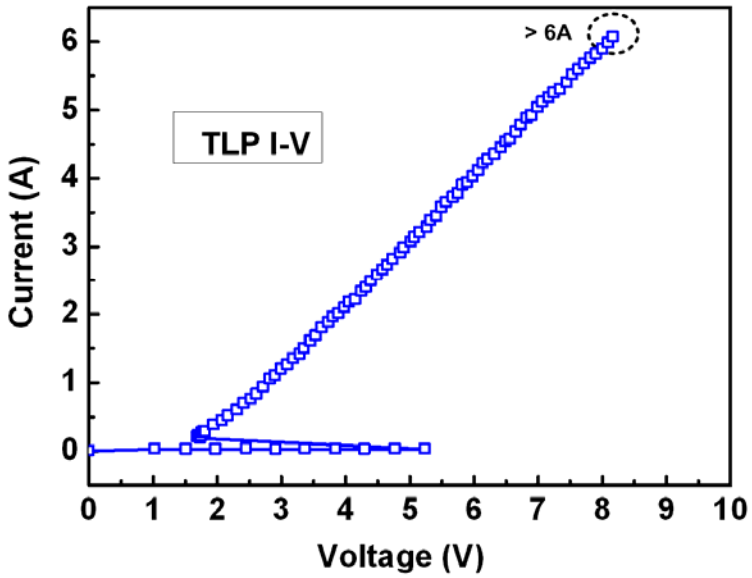


Fig. 4.8. TLP-measured I-V characteristics of SCR with trigger circuit.

4.3.3. PA With ESD Protection

The UWB RF PA with the new ESD protection circuit is shown in Fig. 4.9. It contains a waffle-structured diode string from output (O/P) to VDD, and a waffle-structured SCR from O/P to VSS with a RC-inverter as a trigger circuit. The diode string can avoid the signals leak from O/P to VDD since the voltage swing may approach 2 x VDD (VDD = 1.2 V in a

130-nm CMOS process) at the output node. Besides, another set of RC-inverter-triggered SCR acts as the power-rail ESD clamp circuit to provide the discharging path between VDD and VSS. The RC time constants of the trigger circuits were designed in the order of 10^{-6} - 10^{-7} seconds to detect ESD events. The capacitor of each trigger circuit was composed of a MOS capacitor and was in the area of about 1700 μm^2. Under normal circuit operation, ESD protection circuits were all kept off. During PS-mode ESD stress, with ESD pulses zapping to O/P of the protected PA, ESD current will first flow through the diodes to VDD, and then flow into the RC-inverter to trigger the SCR. The ESD current will be discharged by the SCR from the O/P to VSS. Therefore, the ESD protection ability can be significantly improved.

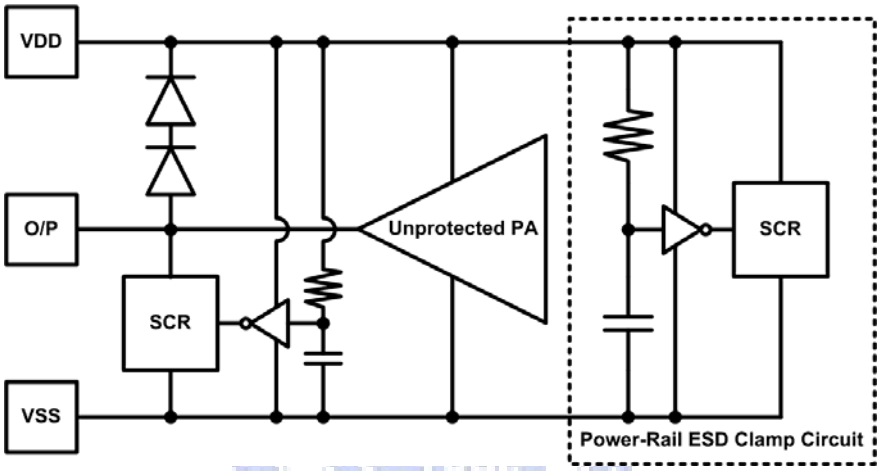
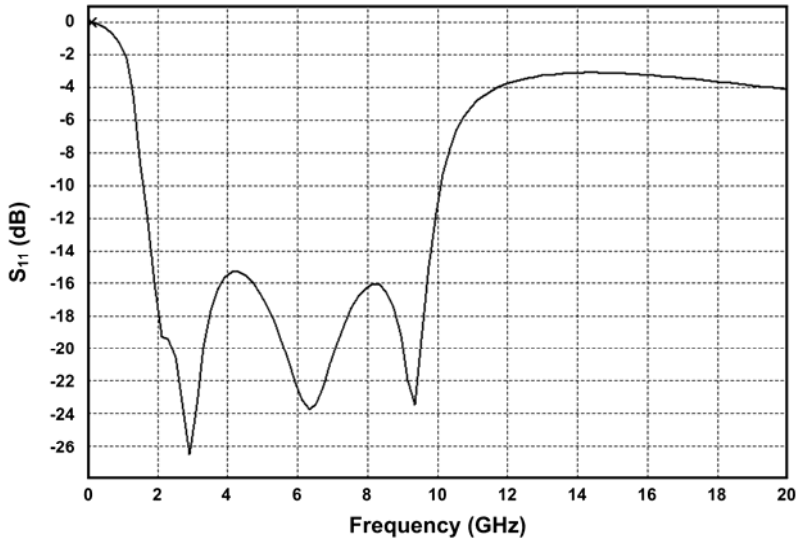


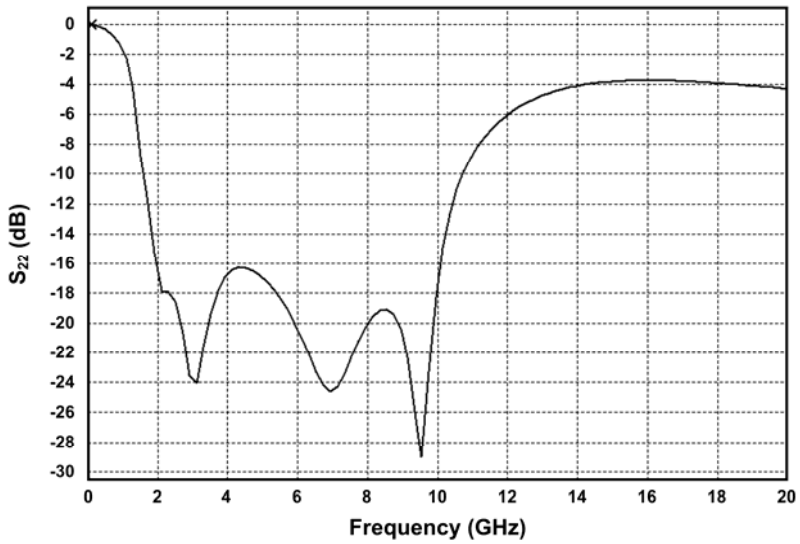
Fig. 4.9. Equivalent circuit of UWB RF PA with the new ESD protection circuit (ESD-protected PA).

The parasitic capacitances contributed by the ESD protection circuit were extracted by a layout parasitic extraction (LPE) CAD tool. Then the extracted capacitances can be incorporated to run the post-layout simulation, and the effects of the ESD protection circuit on the DA can be obtained.

The post-layout simulation of the unprotected DA is shown in Figs. 4.10, 4.11, and 4.12. Fig. 4.10 is the matching situations of the unprotected PA. Fig. 4.11 is the forward and reverse power transmission of the unprotected PA. Fig. 4.12 is the gain and OP1dB versus frequency of the unprotected PA. The post-layout simulation of the ESD-protected PA is illustrated in Figs. 4.13, 4.14, and 4.15. Fig. 4.13 is the matching situations of the DA. Fig. 4.14 is the forward and reverse power transmission of the ESD-protected PA. Fig. 4.15 is the gain and OP1dB versus frequency of the ESD-protected PA. These results are also organized in Table 4.1.

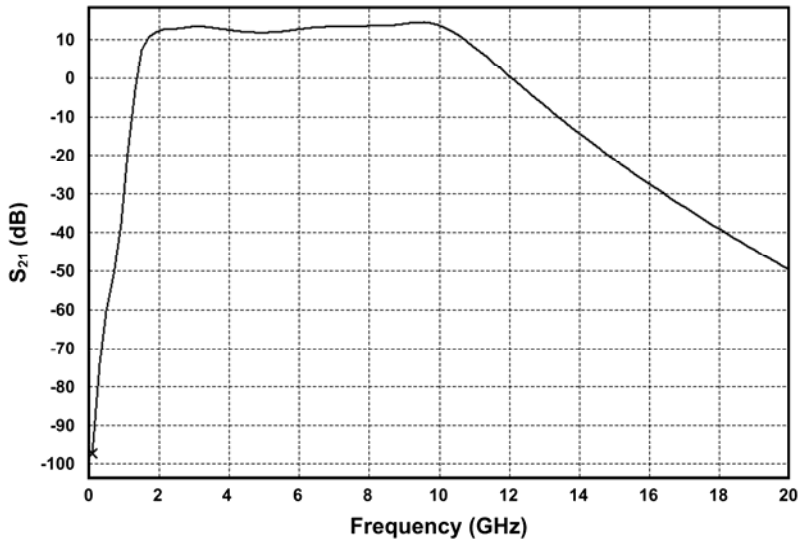


(a)

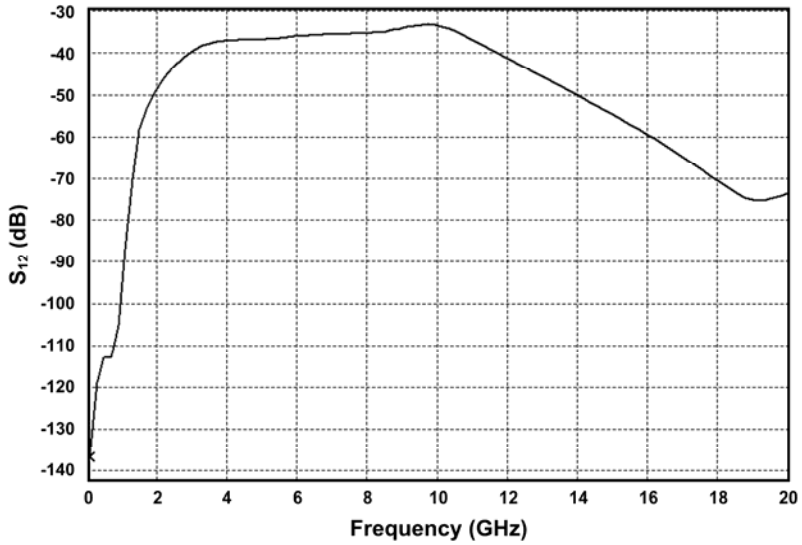


(b)

Fig. 4.10. Post-layout simulation on matching situations of (a) S_{11}, and (b) S_{22}, of the unprotected PA.

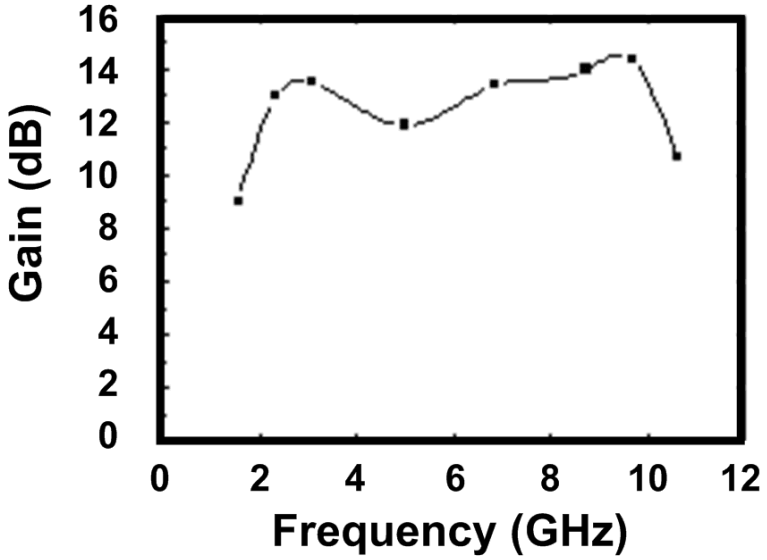


(a)

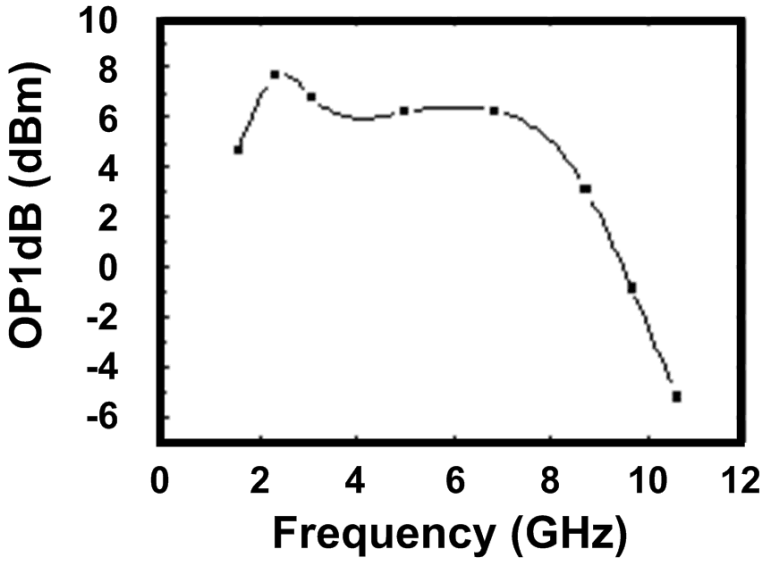


(b)

Fig. 4.11. Post-layout simulation on power transmission of (a) S_{21}, and (b) S_{12}, of the unprotected PA.

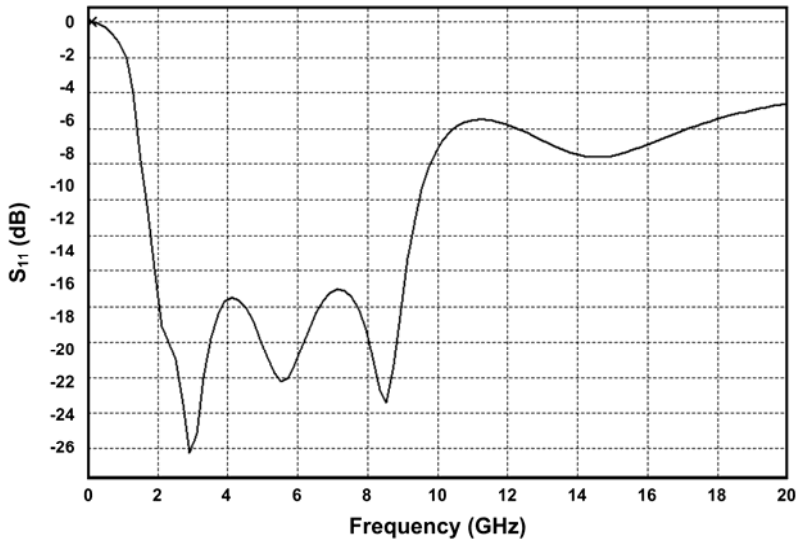


(a)

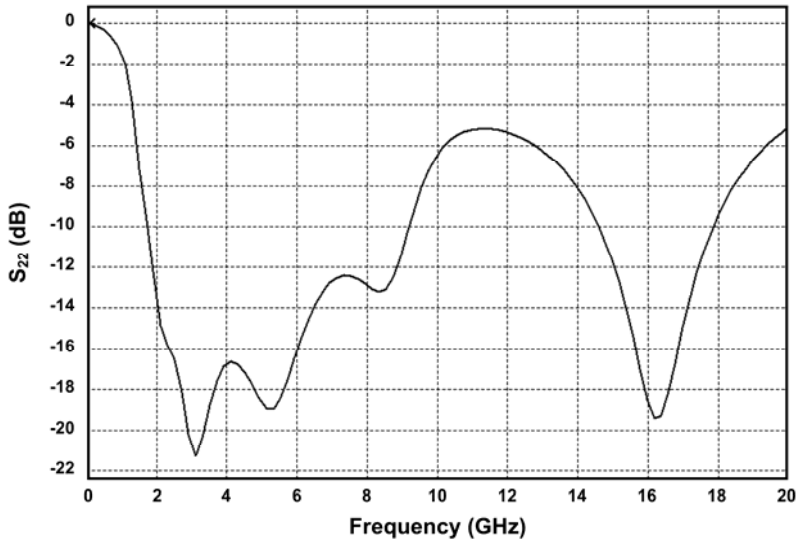


(b)

Fig. 4.12. Post-layout simulation results of (a) gain, and (b) OP1dB, vs. frequency of the unprotected PA.

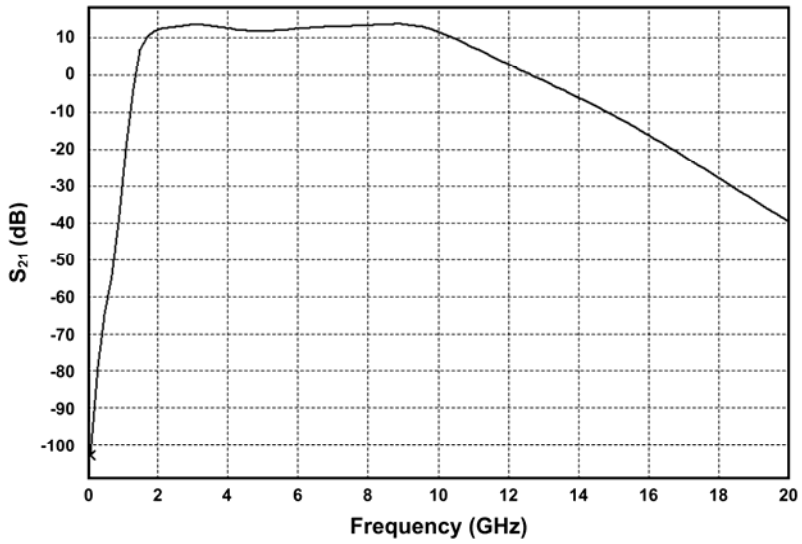


(a)

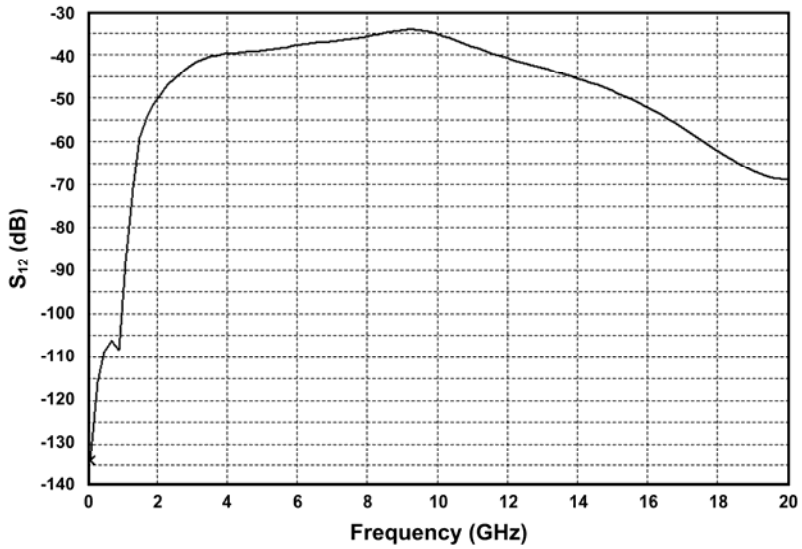


(b)

Fig. 4.13. Post-layout simulation on matching situations of (a) S_{11}, and (b) S_{22}, of the ESD-protected PA.

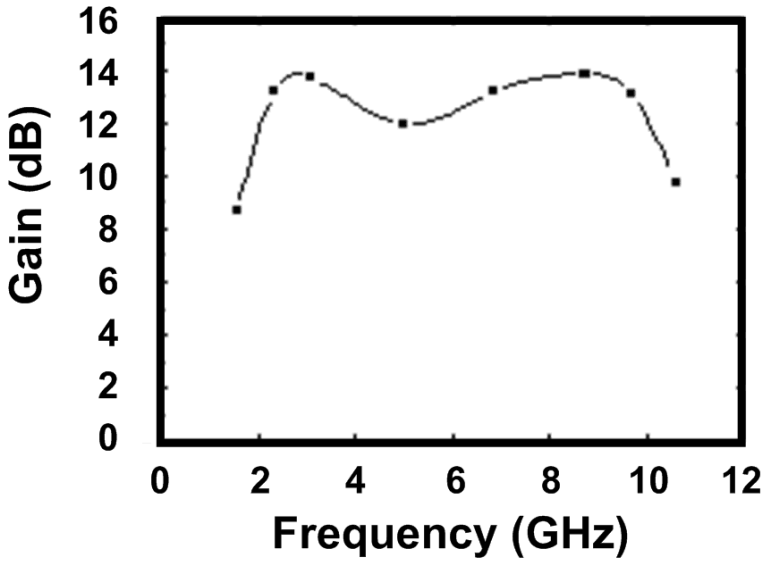


(a)

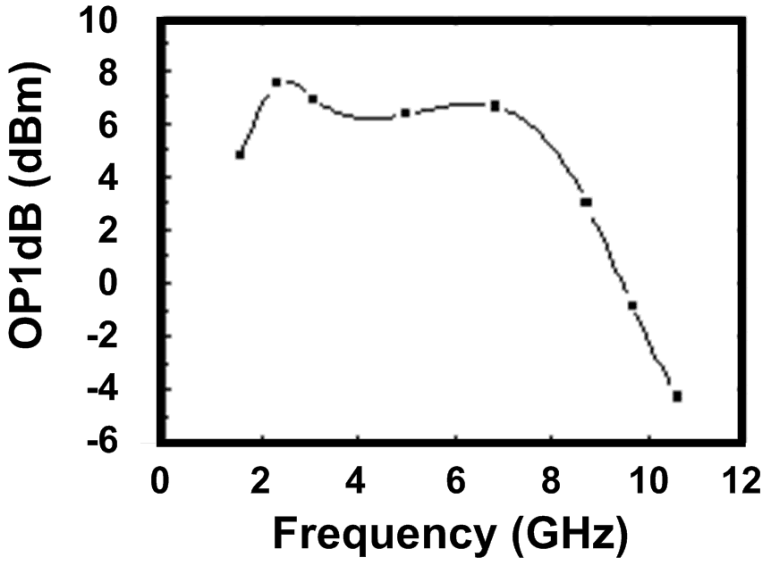


(b)

Fig. 4.14. Post-layout simulation on power transmission of (a) S_{21}, and (b) S_{12}, of ESD-protected PA.



(a)



(b)

Fig. 4.15. Post-layout simulation results of (a) gain, and (b) OP1dB, vs. frequency of ESD-protected PA.

Table 4.1

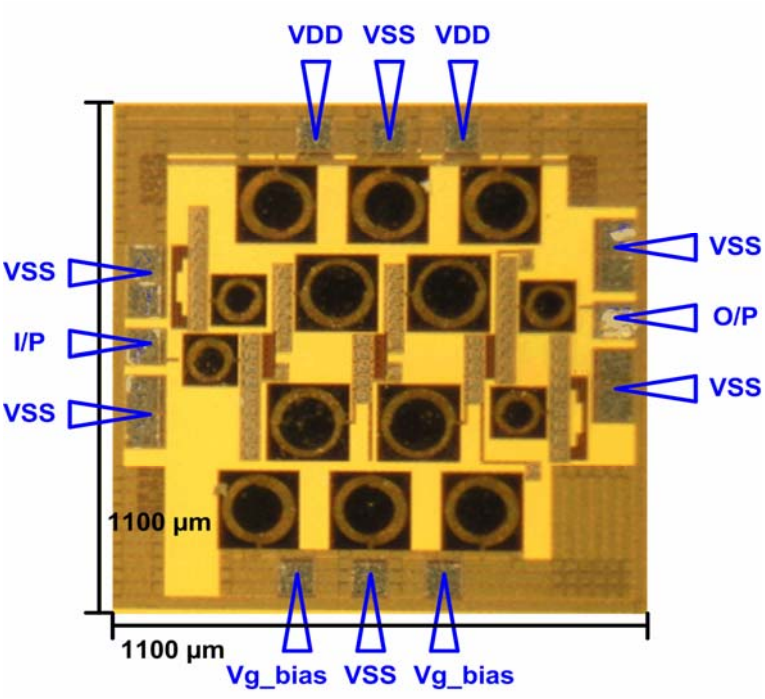
Summary of RF Performance of 3-GHz 0-dBm Narrowband Class-AB PA Before ESD Testing

		Bandwidth	S_{21}	S_{22}	Gain	OP1dB
Specification		3.1-10.6 GHz				0 dBm
Pre-Layout Simulation	W/O ESD	1.9-10.9 GHz	13.1-15.5 dB	< -15.2 dB	13.9 dB	6.3 dBm
Post-Layout Simulation	W/O ESD	1.9-10.4 GHz	11.8-14.4 dB	< -17.1 dB	13.2 dB	5.6 dBm
	With ESD	1.94-10 GHz	11.9-13.7 dB	< -6.4 dB	12.4 dB	5.8 dBm
Measurement Results	W/O ESD	1.85-9.7 GHz	6.4-16 dB	< -2.2 dB	12.4 dB	4.9 dBm
	With ESD	1.7-8.9 GHz	8.2-15.2 dB	< -3.2 dB	10.7 dB	3.3 dBm

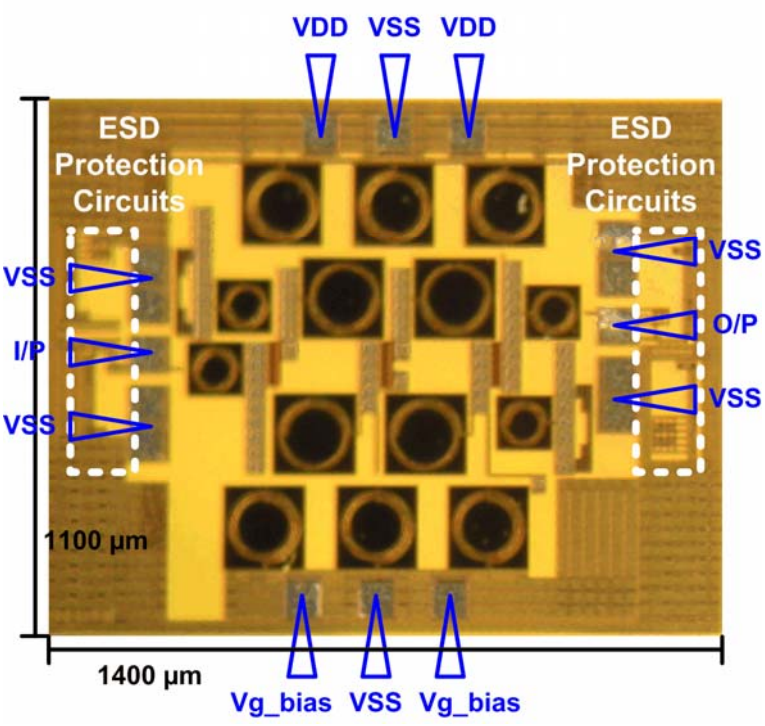
The test chip has been fabricated in 130-nm CMOS process. The die photos of the fabricated chips of the unprotected PA and ESD-protected PA are shown in Figs. 4.16(a) and 4.16(b), respectively.

4.4. Measured RF Performance After ESD Zapping

The S-parameters of the UWB RF PA were measured by using the Agilent E8364B PNA. An Agilent E4448A spectrum analyzer and an Agilent E8257D signal generator were used to evaluate the large signal characteristics of the PA. To compare the ESD protection capability between the PA with and without ESD protection circuit, the RF performance of PA was measured again after each HBM ESD zapping.



(a)

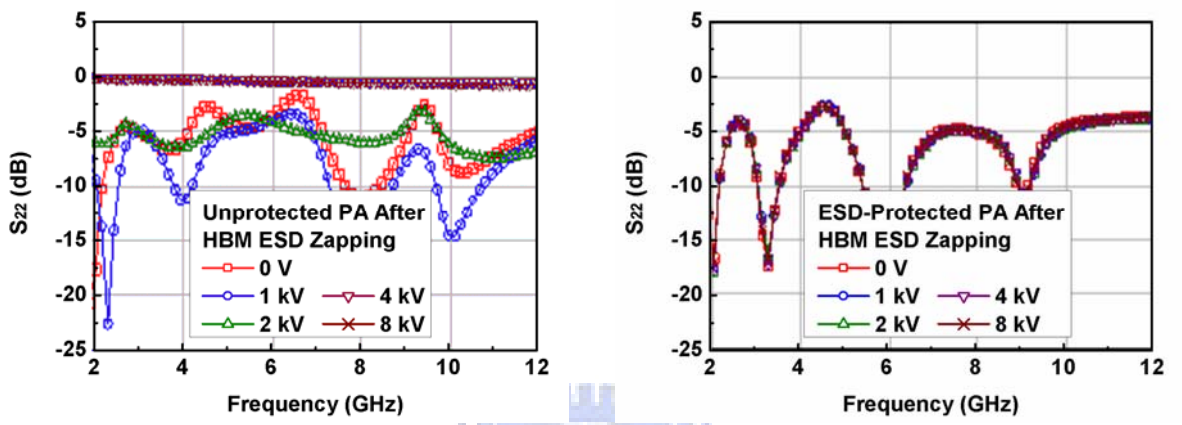


(b)

Fig. 4.16. Die photos of the fabricated (a) unprotected PA and (b) ESD-protected PA.

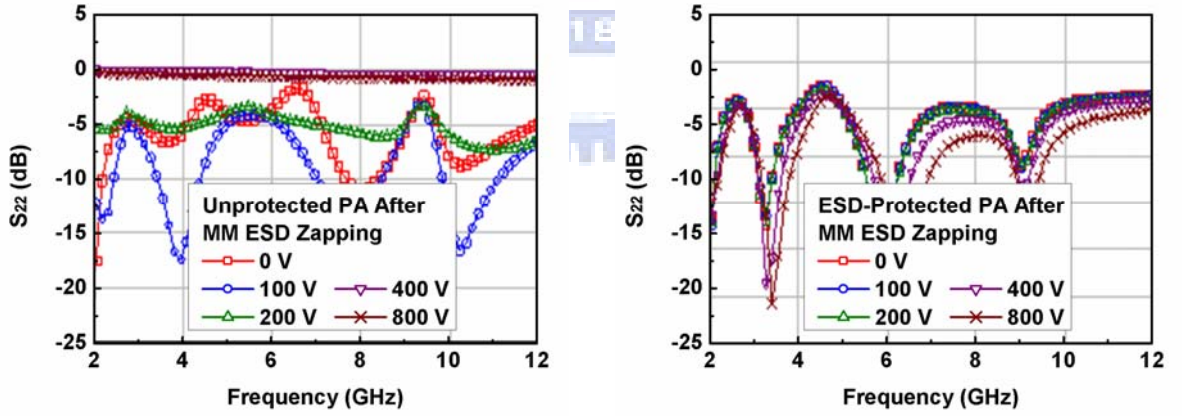
The measured results of the S_{22} from 2 to 12 GHz of the PA without ESD protection circuit (unprotected PA) and that of the PA with ESD protection circuit (ESD-protected PA) are shown in Figs. 4.17 and 4.18. The measured results of the S_{21} are shown in Figs. 4.19 and

4.20. The unprotected PA was severely degraded after HBM or MM ESD zapping. On the contrast, the ESD-protected PA still well performed even if the 8-kV HBM or 800-V MM ESD test was stressed. The bandwidths of the unprotected and ESD-protected PA after each HBM ESD zapping are summarized in Table 4.2. The bandwidths of ESD-protected PA are kept at ~9 dB, even if there are some variations among the test chips.



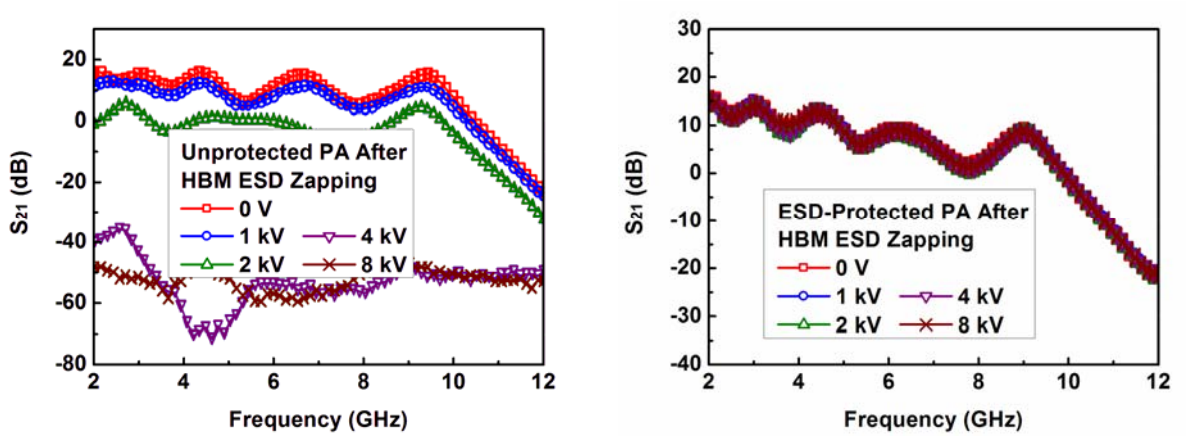
(a) (b)

Fig. 4.17. Measured results on S_{22}-parameter of (a) unprotected PA, and (b) ESD-protected PA, after each HBM ESD zapping.



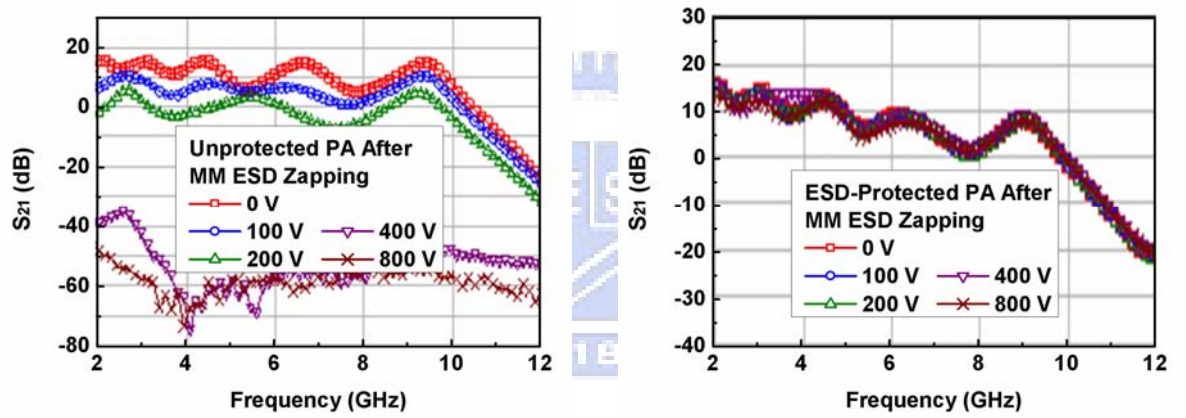
(a) (b)

Fig. 4.18. Measured results on S_{22}-parameter of (a) unprotected PA, and (b) ESD-protected PA, after each MM ESD zapping.



(a) (b)

Fig. 4.19. Measured results on S_{21}-parameter of (a) unprotected PA, and (b) ESD-protected PA, after each HBM ESD zapping.



(a) (b)

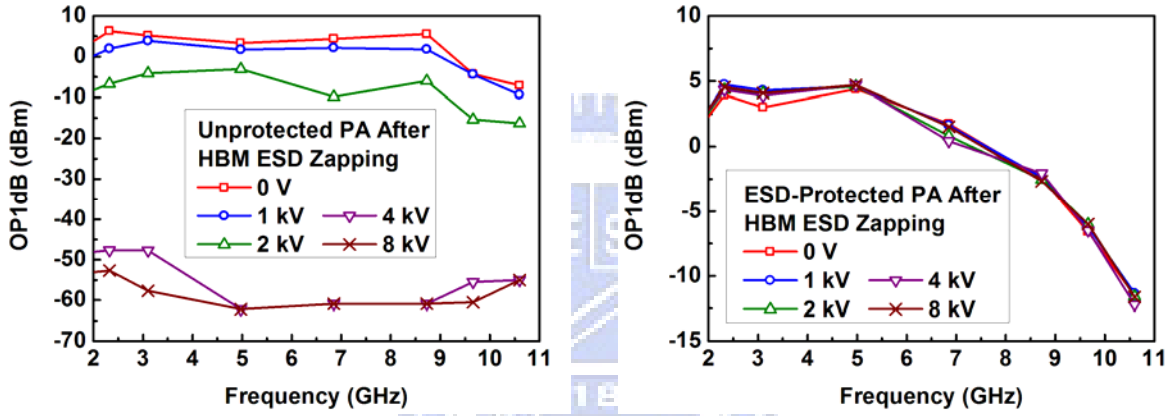
Fig. 4.20. Measured results on S_{21}-parameter of (a) unprotected PA, and (b) ESD-protected PA, after each MM ESD zapping.

Table 4.2

Bandwidth and Gain of UWB RF PA After HBM ESD Zapping

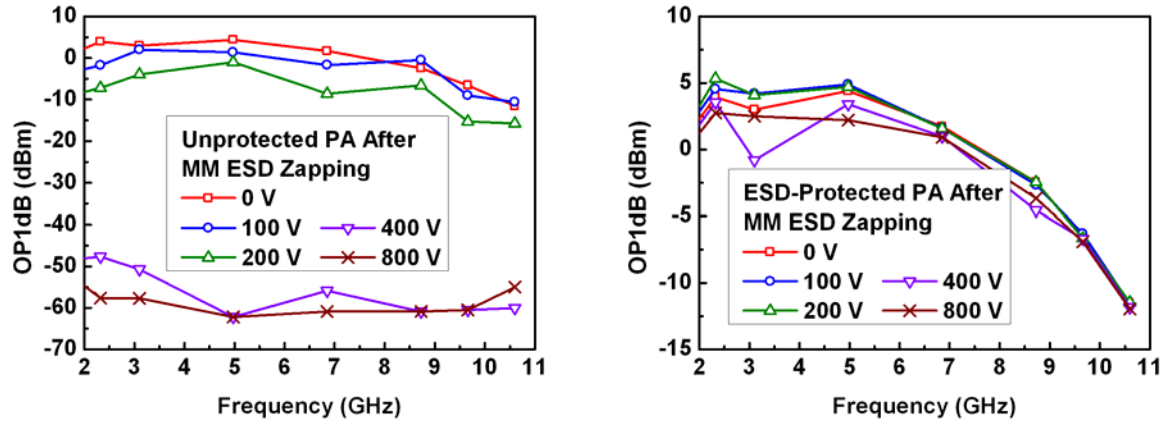
HBM ESD Zapping	Bandwidth		Averaged Gain (3.1-10.6 GHz)	
	Unprotected PA	ESD-Protected PA	Unprotected PA	ESD-Protected PA
0 V	7.8 GHz	7.3 GHz	12.4 dB	9.8 dB
1 kV	7.7 GHz	7.4 GHz	8.9 dB	9.3 dB
2 kV	8.2 GHz	7.3 GHz	-0.4 dB	9.2 dB
4 kV	0 GHz	7.4 GHz	-51.8 dB	8.5 dB
8 kV	0 GHz	7.3 GHz	-55.3 dB	9.5 dB

The averaged large signal power gain of the unprotected and ESD-protected PA within 3.1-10.6 GHz after each HBM ESD zapping are also listed in Table 4.2. According to the measured data, both the bandwidth and the averaged large signal gain of the ESD-protected PA are kept fine after each HBM ESD stress, while those of the unprotected PA are seriously degraded. When the output power increases, the output swing would be compressed. The output power at 1-dB compression point (OP1dB) can be treated as the maximum linear output power capability of the PA. Figs. 4.21 and 4.22 show the measured results on the OP1dB of the unprotected and ESD-protected PA. The OP1dB of the unprotected PA was seriously degraded after HBM or MM ESD zapping. The OP1dB of the ESD-protected PA was not degraded even after 8-kV HBM or 800-V MM ESD test.



(a) (b)

Fig. 4.21. Measured results of OP1dB of (a) unprotected PA, and (b) ESD-protected PA, after each HBM ESD zapping.



(a) (b)

Fig. 4.22. Measured results of OP1dB of (a) unprotected PA, and (b) ESD-protected PA, after each MM ESD zapping.

4.5. Summary

The low-capacitance ESD device is a waffle-structured SCR with trigger circuit incorporated in the whole-chip ESD protection architecture which utilizes an upward diode string to divert part of the ESD current to the power-rail and activate the detection circuit, trigger circuit, and the power-rail ESD clamp. The SCR and the diodes are in waffle-structured layout style which can maximize the discharging peripheral within a given layout area. Therefore, the waffle-structured layout style can provide maximum ESD protection capability but contributing minimum parasitic capacitance. This ESD protection strategy is designed and fabricated in a standard 130-nm CMOS process. A 3-to-10-GHz 0-dBm ultra-wideband class-AB distributed amplifier is designed and acts as the protected RF PA. The waffle-structured SCR and diodes are plugged to RF PA to provide ESD protection. Unprotected PA and ESD-protected PA are tested to understand the influence of ESD zapping. The measurement results prove that an unprotected PA cannot survive any ESD zapping. The gain and output power capability of an unprotected PA are largely degraded ever since a 1-kV HBM test. It can be concluded that an unprotected RF PA may not survive any single ESD zapping; RF PA circuitry is in urgent need of ESD protection.

Besides, the measurement results verify the low-capacitance ESD protection strategy and reveal the truth that this ESD protection technique indeed provides excellent ESD robustness. The RF performance degradation can be minimized by using ESD protection design with the waffle-structured SCR.

Chapter 5

Modeling Parasitic Capacitance for Matching Network Co-Designed in RF ICs

ESD protection design for RF circuits is one of the key challenges to implement RF circuits in CMOS technology. Conventional on-chip ESD protection circuits at the I/O pads often cause performance degradations to RF circuits. The performance degradations are much serious for the RF circuits applied to higher frequency band. Therefore, ESD protection circuits must be designed with minimum negative impact to the RF circuits and to sustain high enough ESD robustness. In this chapter, ESD protection design considerations and matching network co-designed in RF ICs are presented and discussed. In section 5.2, the small-signal model of SCR in RF frequency band is presented firstly. With the matching network co-design between SCR device and RF circuits, the parasitics of the SCR device can be cancelled. In section 5.3, the low-capacitance and low-loss bond pad is studied in CMOS technologies for RF ESD applications. Besides, some ESD protection design techniques for RF applications in standard CMOS processes are overviewed in section 5.4.

5.1. Background

ESD protection design on RF circuits applied to higher frequency band is a popular topic. For example, WirelessHD is the recent technology that operates near the 60-GHz range. To apply the ESD protection devices to such RF circuits, the RF performance degradations caused by the ESD protection devices should be characterized carefully. The implementations of low-capacitance ESD protection device and low-capacitance bond pad are required for RF ICs. Besides, during the RF circuit design, the simulation on RF performances must be performed to acquire preliminary insight into the impacts of ESD protections on RF performance. If all device models of ESD protection device and bond pad in the desired RF frequency band can be obtained, the input/output matching for RF circuits can be well designed. Thus, the circuit simulation models of ESD protection devices have strongly requested by IC industry [75], [76].

SCR has been reported as the useful ESD protection device in RF ICs due to its high ESD robustness within a small layout area and low parasitic capacitance. The macro model of SCR has been reported to simulate its turn-on mechanism during ESD stress [63], [64]. However, the small-signal model of SCR in RF circuit operation condition is scarce. In the RF circuits with SCR-based ESD protection, the lack of SCR device model will introduce the unexpected results, such as the operating frequency shift. To correctly predict the performances of RF circuit with SCR-based ESD protection, it is essential for RF circuit design with accurate model of SCR device. With such a small-signal model, the parasitic capacitance from ESD protection device can be well co-designed with RF circuits.

5.2. Modeling Parasitic Capacitance on Waffle-Structured SCR

5.2.1. Waffle-Structured SCR Design

Waffle-structured SCR device has been studied to lower the parasitic capacitance for RF applications. For such an waffle-structured SCR, its layout top view is shown in Fig. 5.1(a). The anode of SCR was connected to the inside N+ and P+ diffusions, which were formed in N-well. On the contrary, the cathode of SCR was connected to the outside N+ and P+ diffusions, which were formed in P-well. To implement the waffle-structured SCR for experiment, the test devices have been designed and fabricated in a 0.18-μm CMOS process. The dimension of inside P+ (labeled as S_A) is kept at 29.12 μm in layout of this work. The spacing between the inside P+ and the outside N+ is labeled as S_{AC}, which is drawn as 2 μm or 4 μm to study this capacitance. The size of outside N+ and P+ (labeled as S_C) is kept at 14.25 μm. The device cross-sectional view and the small-signal circuit model of waffle-structured SCR is shown in Fig. 5.1(b). The parasitic capacitance of inside P+/N-well junction is labeled as C_A. The resistances from the anode to the fringe of N-well are labeled as R_A and R_{AS}. The parasitic capacitance of N-well/P-well junction, including N-well/P-substrate junction, is labeled as C_S. The resistances from the fringe of N-well to the cathode are labeled as R_{CS} and R_C. The parasitic capacitance of outside P-well/N+ junction is labeled as C_C. The total impedance from anode to cathode of SCR is

$$Z_{SCR} = \frac{1}{2}\left(\frac{R_A}{1 + j\omega C_A R_A} + R_{AS} + \frac{1}{j\omega C_S} + R_{CS} + \frac{R_C}{1 + j\omega C_C R_C} \right) \tag{5.1}$$

where ω is the operation angle frequency (2πf, f is the operation frequency). In general, the resistances of R_A, R_{AS}, R_{CS}, and R_C have the same order of 100 Ω, which are estimated from the design kit. For the capacitances of C_A, C_S, and C_C, even if they are with different bias

conditions, they have the same order of 100 fF. To simplify the calculation, the resistances and the capacitances are replaced by the symbols of R and C. The admittance from anode to cathode of SCR can be expressed as

$$Y_{SCR} = \frac{8\omega^2C^2R + 4\omega^4C^4R^3}{1 + 21\omega^2C^2R^2 + 4\omega^4C^4R^4} + j\omega\left(\frac{2C + 6\omega^2C^3R^2}{1 + 21\omega^2C^2R^2 + 4\omega^4C^4R^4}\right). \quad (5.2)$$

Therefore, the parasitic capacitance of SCR in high frequency can be found as

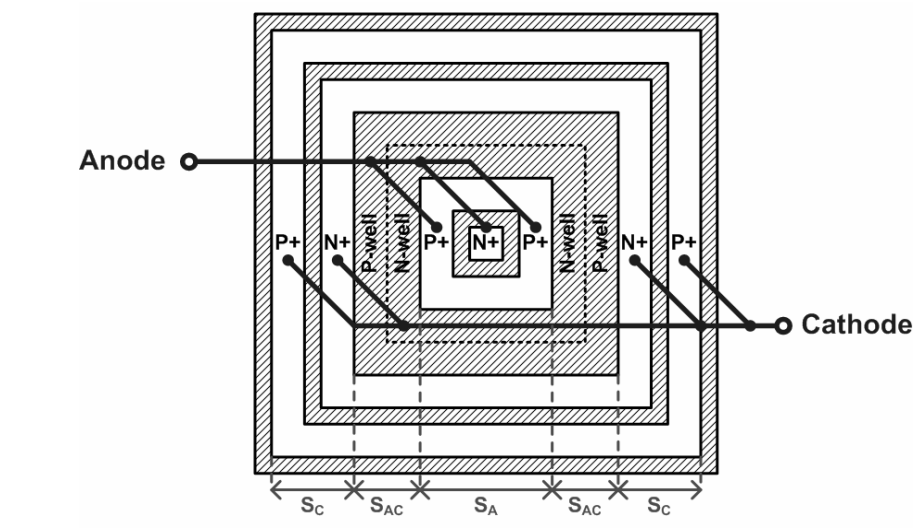
$$C_{SCR} = \frac{2C + 6\omega^2C^3R^2}{1 + 21\omega^2C^2R^2 + 4\omega^4C^4R^4} \cong \frac{3}{2\omega^2CR^2}. \quad (5.3)$$

To further reduce the parasitic capacitance of waffle-structured SCR, increasing R and the spacing between the anode and the cathode (S_{AC}) is a layout solution. For our test SCR devices, the dimensions of components used in the small-signal model are listed in Table 5.1. The layout size of each SCR device is kept at about 60 x 60 μm^2.

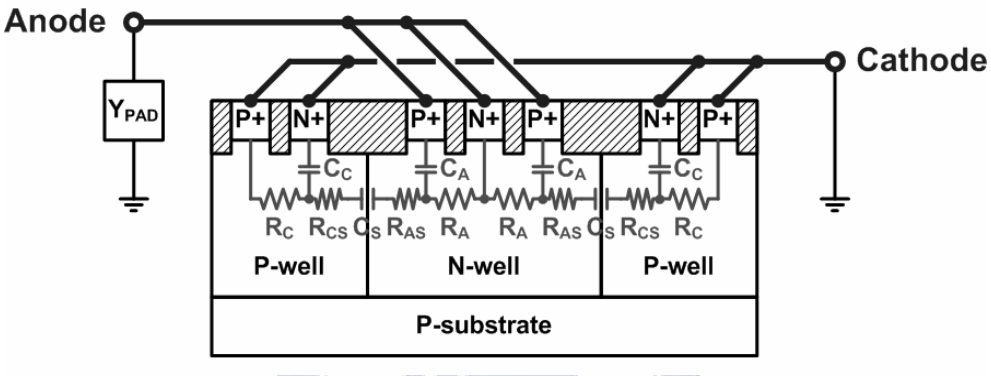
Table 5.1

Dimension of Components Used in Small-Signal Model of Waffle-Structured SCR and Comparison on Measured Characteristics Under Different Device Spacing

	Parameter	S_{AC} = 2 μm	S_{AC} = 4 μm
Small-Signal Model	C_S	85 fF	95 fF
	C_A	100 fF	100 fF
	C_C	150 fF	180 fF
	R_A	500 Ω	500 Ω
	R_C	450 Ω	420 Ω
	R_{AS}	90 Ω	120 Ω
	R_{CS}	70 Ω	100 Ω
Measured Characteristics	C_{SCR}@2.4GHz	80.23 fF	77.17 fF
	C_{SCR}@5GHz	61.19 fF	57.22 fF
	V_{HBM}	> 8 kV	> 8 kV
	V_{MM}	1.30 kV	1.53 kV
	V_{t1}	15.2 V	16.2 V
	R_{on}	0.8 Ω	1.0 Ω
	I_{t2}	> 6 A	> 6 A



(a)



(b)

Fig. 5.1. Waffle-structured SCR: (a) layout top view and (b) device cross-sectional view and small-signal model.

5.2.2. Experimental results

The high-frequency characteristics of waffle-structured SCR can be obtained from the measurement of S-parameters. During the S-parameter measurement, the anode of SCR was biased at 0.9 V, which is VDD/2 in the given 0.18-μm CMOS process. Then, the Y_{11}-parameter can be obtained from the measured two-port S-parameters. The parasitic effects of bond pads (Y_{PAD} in Fig. 5.1(b)) have been removed by using de-embedding technique to extract the intrinsic device characteristics. The intrinsic capacitances and the simulated results within 0~20 GHz of the waffle-structured SCR with shorter and longer spacing (S_{AC}) are shown in Fig. 5.2. The measured parasitic capacitances well agree with the simulated capacitances. Thus, the small-signal model of SCR is appropriate to simulate the parasitics of SCR. Comparing between the test patterns, the parasitic capacitance of SCR at 2.4 or 5 GHz (for 802.11 applications) is decreased with the increased S_{AC}, which is

summarized in Table 5.1. Beside this waffled-structured SCR, the proposed small-signal model can be modified and used to model the other SCR-based ESD protections.

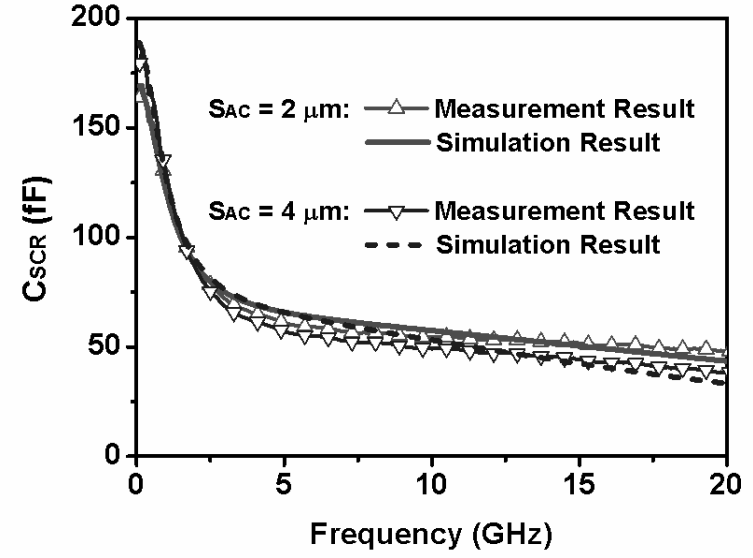


Fig. 5.2. Measured and simulated parasitic capacitance (C_{SCR}) of the waffle-structured SCR devices.

HBM and MM ESD robustness of our SCR patterns have been evaluated by ESD simulator. HBM ESD levels (V_{HBM}) of all SCR exceed 8 kV (8-kV is the maximum limitation of ESD simulator), and MM ESD levels (V_{MM}) are increased from 1.30 kV to 1.53 kV with the increased S_{AC}. The ratios of parasitic capacitance to MM ESD robustness (C_{SCR}/V_{MM}) of SCR with longer S_{AC} has a decrease of about 30 %, as compared with that of SCR with shorter S_{AC}. The turn-on voltage (V_{t1}), secondary breakdown current (I_{t2}), and turn-on resistance in the holding region (R_{on}) of SCR were obtained by the transmission line pulsing (TLP) system. These measurement results are also listed in Table 5.1.

5.3. Low-Capacitance and Low-Loss Bond Pad Design for RF ESD Applications in CMOS Technologies

The semiconductor nature of silicon substrate introduces the undesired parasitic capacitance between the substrate and the bond pad, which will disturb the high frequency signals, induce RC delay in the signal path, and cause performance degradation on the RF circuits. Besides, in a mixed-signal IC, the crosstalk will be coupled across the RF and digital circuits through the parasitic capacitance between the bond pad and silicon substrate [23]. Therefore, the parasitic capacitance at the bond pad must be minimized. For a 5-GHz

low-noise amplifier in an RF receiver, the typical specification on the total input loading capacitance is in the order of 100 fF, including the bond pad and input ESD protection devices [65]. The specification is even stricter for the RF circuits applied to higher frequency band. However, the dimensions of ESD protection devices and bond pad can not be shrunk in advanced CMOS process due to the considerations of reliability and bondability; namely, the parasitic effects of ESD protection devices and bond pad can not be reduced with the shrinking process. Therefore, the implementations of low-capacitance bond pad and low-capacitance ESD protection device are strongly requested by RF ICs.

There are several techniques reported to reduce the bond pad capacitance [77]-[80]. The first approach to reduce the parasitic capacitance is to modify the fabrication process. A bond pad using semi-insulating porous silicon to reduce the bond pad capacitance had been presented [77]. In the low-capacitance bond pad designs by process solutions, chip fabrication cost will be increased due to additional process steps. Another approach to reduce the parasitic capacitance is to realize the bond pad with special layout patterns, which had been demonstrated with smaller bond pad capacitance [78]. Another bond pad with depletion-insulation structure to improve crosstalk isolation and quality factor had been reported [79]. However, layout solution often has small amount of capacitance reduction. The third approach to reduce the parasitic capacitance is implemented by circuit design technique. A low-capacitance bond pad with stacked inductor embedded under the bond pad had been reported [80]. The capacitance can be resonated by inserting the stacked inductor, and the equivalent capacitance can be even reduced to zero at a selected frequency band. However, the bond-pad insertion loss may increase significantly in some layout patterns with embedded inductors, which will loss the signals through the bond pad. Therefore, the low-capacitance bond pad with embedded inductor must be further optimized to lower the insertion loss.

5.3.1. Optimization on Low-Capacitance Bond Pad

The low-capacitance bond pad with embedded inductor is illustrated in Fig. 5.3. The equivalent circuit model of the bond pad is also shown in Fig. 5.3. The circuit model for the bond pad consists of three parts, which are the parasitic capacitance between the support metal and the overlapped substrate, the coupling effect between the support metal and stacked inductor, and the stacked inductor model. In the first part, the parasitic capacitance between the support metal and overlapped substrate is denoted as C_P (45 fF for a pad size of 57 μm × 70 μm). In the second part, the coupling effect between the support metal and stacked

inductor is modeled by C_{C1} (232 fF), C_{C2} (10 fF), R_1 (220 Ω), and R_2 (250 Ω). In the third part, the stacked inductor model is represented by L_S (8.695 nH), C_F (21 fF), R_S (53 Ω), C_{OX1} (27.5 fF), C_{OX2} (74 fF), C_{SUB} (480 fF), and R_{SUB} (16.42 Ω). L_S and R_S represent the inductance and series resistance of the stacked inductor, respectively. C_F is the parasitic capacitance between the metal layers in the stacked inductor. C_{OX1} and C_{OX2} are the capacitances between the stacked inductor and the substrate. C_{SUB} and R_{SUB} represent the parasitic effects of the substrate.

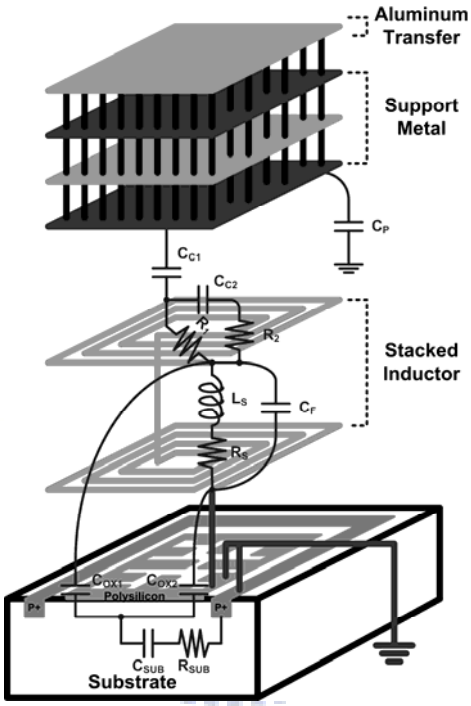


Fig. 5.3. Low-capacitance bond pad with stacked inductor.

Since the insertion loss increases up to 1 dB in some patterns with stacked inductors, the low-capacitance bond pad must be carefully designed to prevent the signal loss through the bond pad. The effects of each component in the bond pad model are investigated first in this work. The dimensions of each component vary from half to double, and the variations result in the changes of insertion loss. S-parameter simulations are performed on these bond pads by using the microwave circuit simulator ADS to find the insertion loss. The loss of the original bond pad model is 0.48 dB at 5-GHz frequency. As each component in bond pad model is half-sized/double-sized, the simulated insertion loss is compared to the 0.48 dB and denoted as Δ Loss. The simulation results on the Δ Loss as each component in the bond pad model varied from double to half are summarized in Table 5.2. In order to lower the insertion

loss of the low-capacitance bond pad, some possible solutions are to decrease C_{C1}, increase R_1, or increase C_F. A simple approach for this goal is to realize the embedded inductor under the bond pad with the lower metal layers. The bond pad with the lower-metal-layer inductor is implemented to reduce the insertion loss from that with the higher-metal-layer inductor.

Table 5.2

Simulation Results on Insertion Loss as Each Component in Bond Pad Model Varied from Double to Half

Component	$2 \cdot C_P$ / $\frac{1}{2} \cdot C_P$	$2 \cdot C_{C1}$ / $\frac{1}{2} \cdot C_{C1}$	$2 \cdot C_{C2}$ / $\frac{1}{2} \cdot C_{C2}$	$2 \cdot R_1$ / $\frac{1}{2} \cdot R_1$	$2 \cdot R_2$ / $\frac{1}{2} \cdot R_2$	$2 \cdot L_S$ / $\frac{1}{2} \cdot L_S$
Δ Loss (dB)	0.004 / 0.001	0.013 / -0.134	0.019 / -0.008	-0.223 / 0.299	0.001 / 0.000	-0.030 / 0.002
Component	$2 \cdot C_F$ / $\frac{1}{2} \cdot C_F$	$2 \cdot R_S$ / $\frac{1}{2} \cdot R_S$	$2 \cdot C_{OX1}$ / $\frac{1}{2} \cdot C_{OX1}$	$2 \cdot C_{OX2}$ / $\frac{1}{2} \cdot C_{OX2}$	$2 \cdot C_{SUB}$ / $\frac{1}{2} \cdot C_{SUB}$	$2 \cdot R_{SUB}$ / $\frac{1}{2} \cdot R_{SUB}$
Δ Loss (dB)	-0.112 / -0.055	-0.051 / 0.026	0.019 / -0.041	0.000 / 0.001	-0.003 / 0.005	0.001 / 0.000

5.3.2. Implementation on Low-Capacitance Bond Pad

In this study, a 65-nm one-poly ten-metal (1P10M) CMOS process is used. The reference pad without embedded inductor is implemented with the top three metal layers (metal 8~10), and the corresponding lower metal layers (metal 1~7) are removed to reduce the bond-pad capacitance. Other bond pads with three kinds of inductors, which are whole-metal-layer inductor (metal 1~7), higher-metal-layer inductor (metal 5~7), and lower-metal-layer inductor (metal 1~5), were implemented in the same silicon chip for comparison. The effective thickness of the inductors in these bond pads are about 1.4 μm, 0.7 μm, and 0.9 μm, respectively. All inductors are drawn with 4-μm track width, 2-μm track spacing, and three turns. The polysilicon layer as the patterned ground shield is used to reduce the energy dissipation in substrate and increase quality factor of the inductor [81]. All the inductors are implemented within the region of bond pad, and each bond pad occupies silicon area of 52 μm × 64 μm. One-port ground-signal-ground (G-S-G) pads are adopted to facilitate on-wafer RF measurement. The layout top view of one test pattern used to measure the s-parameter is shown in Fig. 5.4.

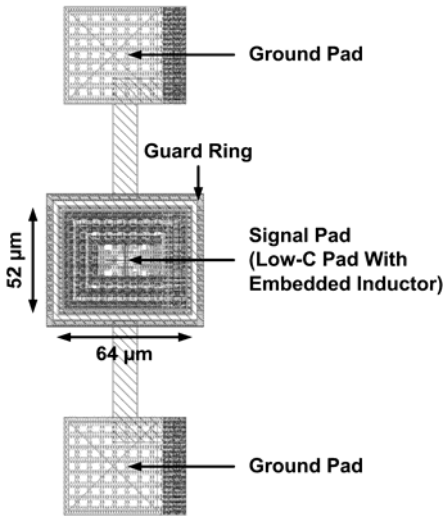


Fig. 5.4. Layout top view of one test pattern for low-C pad with embedded inductor with one-port G-S-G pads.

The s-parameters of all fabricated bond pads are measured by using Cascade Air Coplanar G-S-G microwave probe and Agilent E8364B PNA network analyzer. The capacitance and insertion loss of each bond pad can be extracted by following equations [72]

$$Capacitance = \frac{\mathrm{Im}(Y)}{2\pi f} = \frac{\mathrm{Im}\left(\frac{1}{Z_0}\cdot\frac{1-S}{1+S}\right)}{2\pi f} \tag{5.4}$$

and

$$Insertion\ Loss = \left|\frac{2}{2+Y\cdot Z_0}\right| = \left|\frac{2}{2+\frac{1-S}{1+S}}\right| \tag{5.5}$$

where f denotes the frequency, Z_0 is the 50-Ω termination resistance, S denotes the measured s-parameter, and Y is the extracted y-parameter.

Figs. 5.5 and 5.6 show the extracted capacitance and insertion loss among the fabricated bond pads under different frequencies. All the low-capacitance bond pads have very small capacitance around the specific frequency band. The optimized bond pad with M1-M5 (metal 1~5) inductor has the least loss among the low-capacitance bond pads with embedded inductors, and the lower loss is more tolerable at RF frond-ends. Therefore, the optimized low-capacitance bond pad is much suitable for RF applications. The frequency at which the capacitance of the bond pad is minimum can be shifted by adjusting the resonant frequency of inductance and capacitance, which can be achieved by changing the track width, spacing, turn numbers, or other layout dimensions of the embedded inductor.

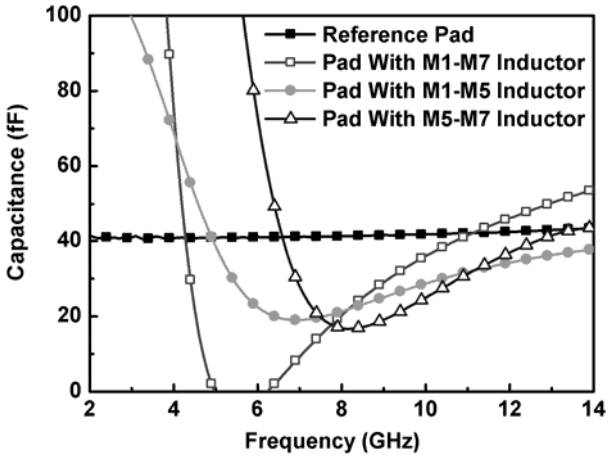


Fig. 5.5. Extracted bond pad capacitance of each fabricated bond pad under different frequencies.

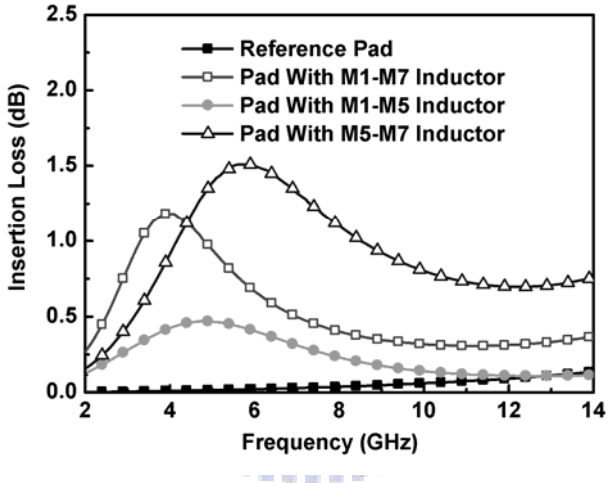


Fig. 5.6. Extracted insertion loss of each fabricated bond pad under different frequencies.

5.4. Summary

The small-signal circuit model of waffle-structured SCR has been presented and proved in silicon. The measured parasitic capacitances well agree with the simulated capacitances. The RF circuits can be well co-designed with the presented small-signal model to eliminate the negative impacts from ESD protection SCR on RF performances.

With optimized design on the embedded inductor under the bond pad, the bond pad can perform both low parasitic capacitance and low insertion loss. The experimental results in a 65-nm CMOS process have proven that the bond pad capacitance and insertion loss can be successfully reduced in a specific frequency band by the optimized bond pad structure. Therefore, the optimized bond pad is very suitable for the narrowband RF applications. The

optimized bond pad can be realized in any bulk CMOS technology without additional process steps for RF applications. Besides, the small-signal model of the optimized bond pad can be used in the RF-circuit-design phase to well co-design with the RF circuits, which can eliminate the negative impacts from bond pad on RF performances.

Chapter 6

High-Voltage-Tolerant ESD Clamp Circuit With Low Standby Leakage in Nanoscale CMOS Process

To fully integrate the RF frond-end and baseband circuits into a single chip, I/O circuits with low-voltages devices must drive or receive high-voltage signals to communicate with other circuit blocks. With the consideration of low standby leakage in nanoscale CMOS processes, a new 2×VDD-tolerant ESD clamp circuit by using only 1×VDD devices was presented in this chapter. The new ESD clamp circuit had a high-voltage-tolerant ESD detection circuit to improve the turn-on efficiency of the SCR-based ESD clamp device, so the ESD clamp circuit had the high ESD robustness. This design had been successfully verified in a 65-nm CMOS process. The leakage current of this ESD clamp circuit under normal circuit operating condition was only in the order of 100 nA. The test patterns with 25-μm and 50-μm SCR-based ESD clamp devices can achieve 2.6-kV and 4.8-kV HBM ESD robustness, respectively. Such high-voltage-tolerant ESD clamp circuit by using only low-voltage devices with very low standby leakage current and high ESD robustness was very suitable for mixed-voltage I/O interfaces in nanoscale CMOS processes.

6.1. Background

In advanced CMOS technologies, the thickness of gate oxide has been scaled down to improve circuit performances with the decreased power supply voltage for low-power applications. However, for the system-on-a-chip (SoC) applications, the I/O buffers with low-voltage devices will drive or receive high-voltage signals to communicate with other ICs in the microelectronic systems or subsystems. Therefore, the I/O buffers must be designed with the consideration of high-voltage tolerance to prevent overstress voltage on the thinner gate oxide of the devices in I/O buffers. To avoid this gate-oxide-reliability issue without using additional thick-gate-oxide devices, the stacked NMOS configuration has been widely used in the mixed-voltage I/O buffers [82]-[84]. Without the thick-gate-oxide devices in low-voltage processes, the process steps can be reduced, the fabrication yield can be

increased, and the chip cost can be lowered. However, the stacked NMOS configuration usually has a lower ESD robustness and slow turn-on speed of the parasitic lateral n-p-n device, as compared with the single NMOS [85]-[87]. Therefore, additional ESD protection design must be provided to protect the stacked NMOS in the mixed-voltage I/O buffer.

The ESD protection scheme with ESD bus and high-voltage-tolerant ESD clamp circuit for a SoC with mixed-voltage I/O interfaces has been presented [88], [89]. The high-voltage-tolerant ESD clamp circuits realized with only 1×VDD devices have been reported [90]-[92]. However, in nanoscale CMOS technologies, the leakage current must be considered during the circuit design [93], [94]. Therefore, the high-voltage-tolerant power-rail ESD clamp circuit must be designed with the consideration of low standby leakage current in nanoscale CMOS processes.

6.2. ESD Protection Scheme With On-Chip ESD Bus for High-Voltage-Tolerant Mixed-Voltage I/O Buffer

To receive the input signals with n×VDD voltage level, the traditional ESD protection design with direct diode connection from I/O pad to 1×VDD line is forbidden. To improve ESD robustness of the mixed-voltage I/O interfaces, the ESD protection circuit with on-chip ESD bus is used. The ESD protection scheme with ESD bus and high-voltage-tolerant ESD clamp circuit for a SoC with mixed-voltage I/O interfaces has been presented [88], [89]. With the consideration on gate-oxide reliability, the ESD protection scheme with on-chip ESD bus for high-voltage-tolerant mixed-voltage I/O buffer is shown in Fig. 6.1. The ESD protection scheme is realized with ESD diodes (D_P, D_N, and D_1), ESD bus, 1×VDD ESD clamp circuit, and high-voltage-tolerant ESD clamp circuit.

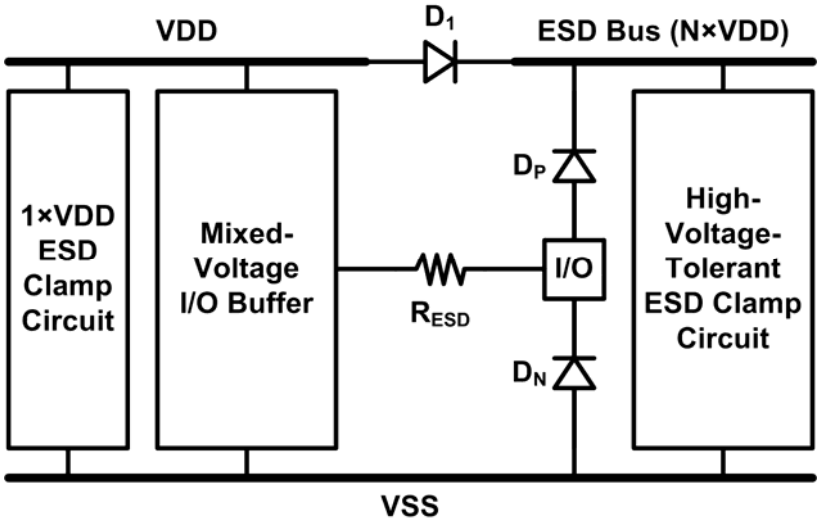


Fig. 6.1. ESD protection scheme with on-chip ESD bus for high-voltage-tolerant mixed-voltage I/O buffer.

While positive ESD charges stress to I/O pad with grounded ESD bus, the ESD currents can be discharged through the diode D_P in forward-biased condition. As positive ESD charges stress to I/O pad with grounded VSS, the ESD currents can be discharged through the diode D_P to the ESD bus and then through the high-voltage-tolerant ESD clamp circuit to VSS. Once positive ESD charges stress to I/O pad with grounded VDD, the ESD currents can be discharged through D_P, ESD bus, high-voltage-tolerant ESD clamp circuit, VSS line, and 1×VDD ESD clamp circuit.

While negative ESD charges stress to I/O pad with grounded VSS, the ESD currents can be discharged through the diode D_N in forward-biased condition. As negative ESD charges stress to I/O pad with grounded ESD bus, the ESD currents can be discharged through D_N to the floating VSS line, and then through the high-voltage-tolerant ESD clamp circuit to the ESD bus. Once negative ESD charges stress to I/O pad with grounded VDD, the ESD currents can be discharged through D_N to the floating VSS line, and then through the 1×VDD ESD clamp circuit to VDD.

As positive ESD charges stress to VDD with grounded ESD bus, the ESD currents can be discharged through the diode D_1. Once negative ESD charges stress to VDD with grounded ESD bus, the ESD currents can be discharged through the 1×VDD ESD clamp circuit, VSS line, and high-voltage-tolerant ESD clamp circuit. Each mode of ESD stresses at the mixed-voltage I/O pad, ESD bus, VDD, or VSS line has the corresponding well-designed ESD discharging path in this ESD protection scheme.

6.3. Traditional Designs of High-Voltage-Tolerant ESD Clamp Circuits

Some high-voltage-tolerant ESD clamp circuits realized with only 1×VDD devices have been reported. Fig. 6.2 shows a 2×VDD-tolerant design. Under ESD stress conditions, the ESD current will discharge through M1 and M2. Under normal circuit operating conditions, the voltage divider (M3 and M4) will keep the node 1×VDD at half of the 2×VDD voltage. Therefore, all gate-to-source and gate-to-drain voltages stay below 1×VDD voltage in the long term. It should be noted that the gate-to-bulk voltage across M5 is greater than 1×VDD voltage at steady state. However, since the conductive channel is induced under the gate of M5, the voltage across the gate oxide of such a device is not more than 1×VDD voltage. Therefore, all low-voltage devices prevent from gate-oxide reliability concern.

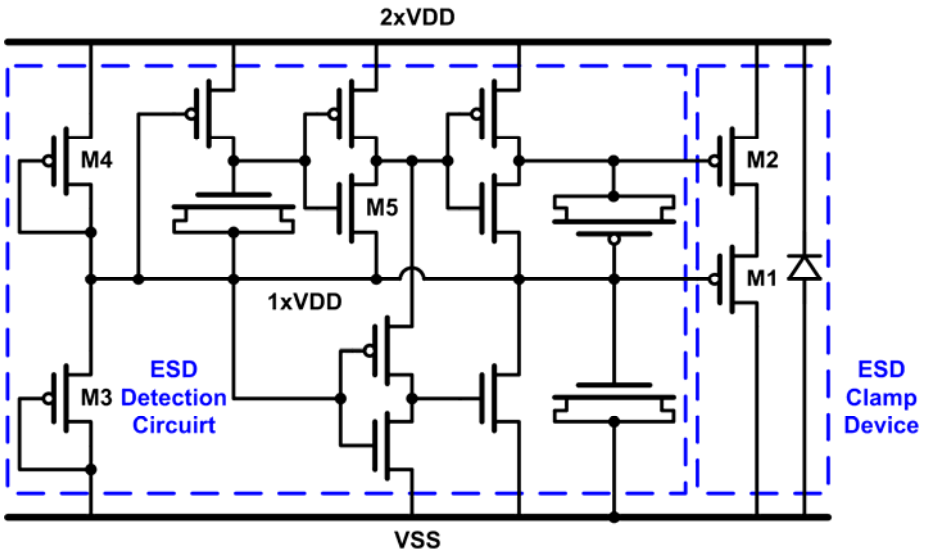


Fig. 6.2. Traditional design of 2×VDD-tolerant ESD clamp circuit.

A 3×VDD-tolerant ESD clamp circuit operated under 3.3-V bias with 1.2-V low-voltage devices is shown in Fig. 6.3. The ESD clamp device is realized by a substrate-triggered SCR (STSCR) with three diodes in series. Under normal circuit operating conditions, the diode-connected PMOS (M1, M2, and M3) are used as the voltage divider to bias the ESD detection circuit. The nodes 1 and 2 in the ESD detection circuit are biased at 1.1 V and 2.2 V, respectively. The node 3 is biased to 1.2-V VDD through the resistor R1. The M5 is turned off, so there is no trigger current generated from the ESD detection circuit into the SCR device. All devices in this ESD detection circuit are free from gate-oxide reliability issue.

During ESD stress to ESD bus with VSS grounded, the capacitor Mc2 will couple some

ESD charge to node 2 to turn on M7. The RC delay of R2 and Mc1 in the ESD detection circuit will keep the gate of M6 (node 4) at lower voltage level. The VDD is initially floating with 0 V as ESD stress to ESD bus. The gate of M5 and M6 are initially at low voltage level, so the M5 and M6 can be quickly turned on to generate the substrate-triggered current into the substrate of SCR device. Then, the SCR device can be turned on to discharge ESD current from ESD bus to VSS.

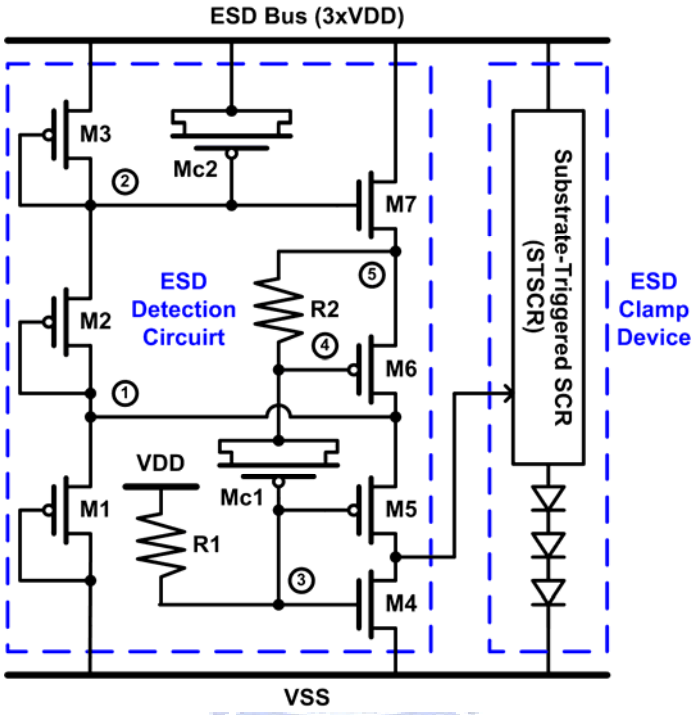


Fig. 6.3. Traditional design of 3×VDD-tolerant ESD clamp circuit.

The other 3×VDD-tolerant power-rail ESD clamp circuit is shown in Fig. 6.4. The 3×VDD-tolerant power-rail ESD clamp circuit is also realized with 1.2-V low-voltage devices to operate at 3.3 V without the risk of gate-oxide reliability. The ESD clamp device is realized by STSCR with two diodes in series. Under normal circuit operating conditions, the nodes 2 and 3 in the ESD detection circuit are biased at 1.1 V and 2.2 V, respectively. The gate voltage of M7 (node 1) is biased at 0.6 V, so that M7 is turned on and the node 9 is biased at 1.1 V. The gate-to-source voltage of M10 is 0 V, and therefore M10 is turned off. There is no trigger current generated from the ESD detection circuit into the ESD clamp device. In the ESD detection circuit, the gate voltage of M3 and M12 is biased at 3.3 V through the resistor R1. Therefore, the M3 and M12 are kept in off state. Owing to the turned-off M3, there is no current path from ESD bus through the PMOS M3, M2, and M1 to

VSS, so that M2 is kept at off state. Therefore, the source-to-gate voltage of M2 is less than the threshold voltage of the 1.2-V PMOS transistor (V_{tp}), so the voltage level of node 5 is kept between 2.2 V and 2.2+|V_{tp}| V. With the same reason, M1 is also kept at off state, and the gate voltage of M5 and M8 (node 4) is kept between 1.1 V and 1.1+|V_{tp}| V, so that M5 and M8 are both at on state, and therefore the voltage level of nodes 6 and 10 are biased at 2.2 V. The gate-to-source voltages of M4, M6, and M11 are nearly 0 V, so these transistors are all at off state. In this situation, all 1.2-V devices are free from gate-oxide reliability issue under normal circuit operating conditions.

When ESD voltage is conducted to the ESD bus with VSS grounded, the RC delay of R1 and Mc1 in the ESD detection circuit keeps the gates of M3 and M12 (node 7) at low voltage level, as compared with the ESD bus. The M3 and M12 can be turned on, and therefore, the voltage levels at nodes 5 and 10 rise rapidly. The voltage levels at nodes 2 and 3 are initially floating with 0 V, so the M2 and M11 can be turned on, and the voltage levels at nodes 4 and 9 also rise rapidly. The M7 is in on state, and the voltage level at node 2 will rise with the voltage level at node 9. However, the RC delay keeps the node 2 in a low voltage level to ensure that M10 is in the turned-on state during ESD stress event. Moreover, the gate voltage of M4 (node 4) is higher than its source voltage (node 2). Therefore, M4 is turned on to keep the voltage level at node 6 in a low voltage level. The gate-to-drain voltage of M6 is ~0 V. The voltage level at node 3 is one threshold voltage higher than the voltage level at node 6. Furthermore, the gate voltage of M8 (node 4) is as high as its source voltage (node 10), so that M8 is in off state to ensure that the voltage level at node 3 can be kept in a low voltage level, as compared with node 10. Therefore, the M10, M11, and M12 can be quickly turned on to generate the substrate-triggered current into the trigger node (node 8) of the SCR under ESD stress conditions.

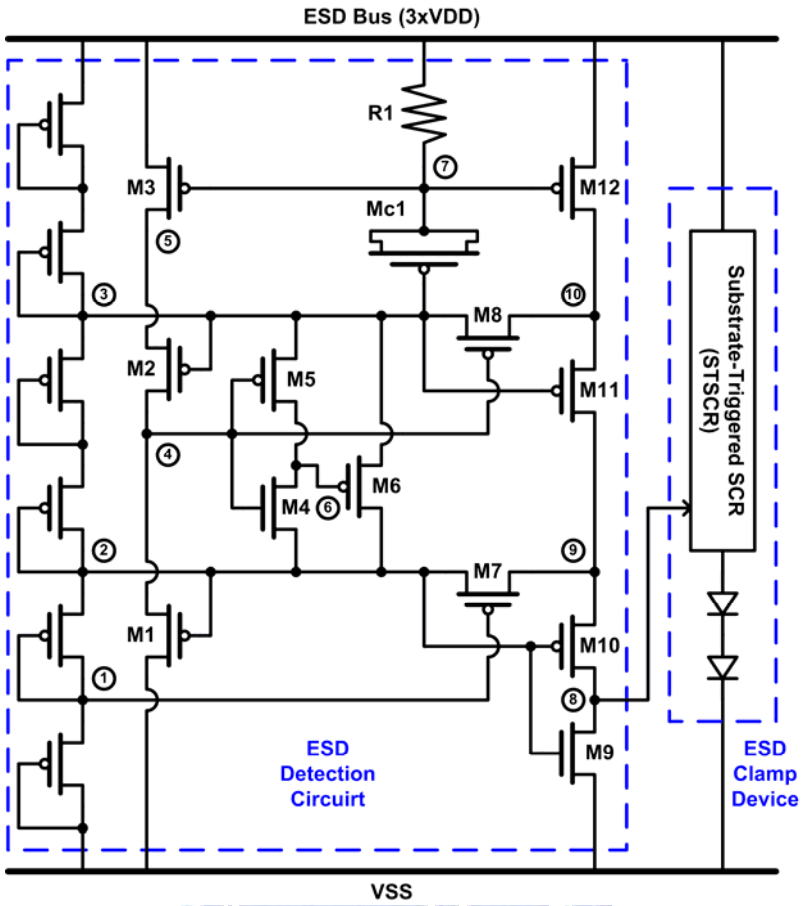


Fig. 6.4. Another traditional design of 3×VDD-tolerant ESD clamp circuit.

The other 2.5-V-tolerant ESD clamp circuit by using 1.2-V devices is shown in Fig. 6.5. The ESD clamp device has a stacked NMOS (STNMOS) with a substrate-triggered design. The STNMOS is formed by stacked NMOS transistors (M4 and M5) with a 1.2-V gate oxide in a 0.13-μm CMOS process. The gate of M5 is biased at the 1.2-V VDD through a resistor to avoid the gate-oxide reliability issue, and the gate of M4 is connected to the VSS to ensure the off state of the STNMOS during normal circuit operating conditions. Therefore, STNMOS will be kept off without gate-oxide reliability during normal circuit operating conditions.

With a 1.2-V VDD power supply voltage, the ESD bus could be charged up to 2.5 V by the 2.5-V input signals at the I/O pad. With a maximum voltage level of 2.5 V on the ESD bus, the gate of M3 will be biased at 2.5 V through resistor R1, and the gate of M1 and M2 will be biased at 1.2 V through a resistor. Therefore, M2 and M3 are kept off, and M1 is turned on to bias the substrate of STNMOS at VSS. There is no trigger current generated from the ESD detection circuit into the STNMOS, so STNMOS is guaranteed to be kept off under normal circuit operating conditions. The source-to-gate voltage of M2 is less than the

threshold voltage of the 1.2-V PMOS transistor (Vtp), so the source voltage of M2 is kept between VDD and VDD+|Vtp|. In this situation, all 1.2-V devices are free from the gate-oxide reliability issue under normal circuit operating conditions.

Under positive ESD stresses at ESD bus with VSS grounded, the gate of M3 is kept at a low voltage due to the RC delay of R1 and Mc1 in the ESD detection circuit. VDD is initially floating with 0 V. The gate of M2 is kept at a low voltage level to keep M2 at the on state. Therefore, M2 and M3 can be quickly turned on by ESD energy to generate the substrate-triggered current into the substrate of STNMOS. After the base-emitter voltage of the lateral npn BJT in the STNMOS is greater than its cut-in voltage, the STNMOS will be triggered into its snapback region. Therefore, the ESD current can be discharged from the ESD bus through the lateral npn BJT in the STNMOS to VSS.

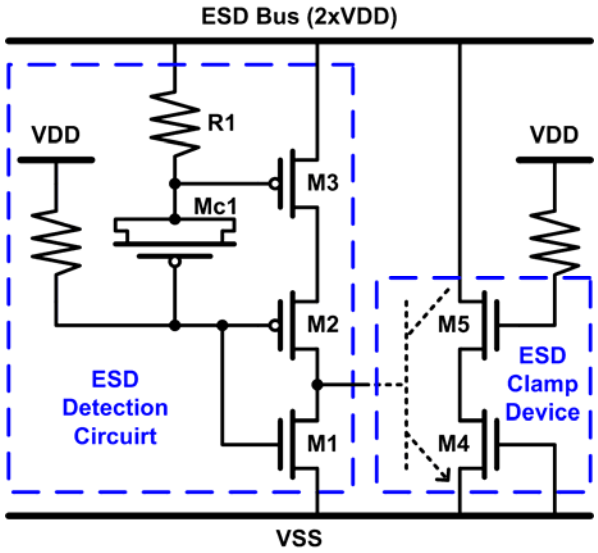


Fig. 6.5. Another traditional design of 2×VDD-tolerant ESD clamp circuit.

6.4. New Design of High-Voltage-Tolerant ESD Clamp Circuit

In nanoscale CMOS technologies, new design of the high-voltage-tolerant ESD clamp circuit must be developed to reduce standby leakage current.

6.4.1. Circuit Topology

The new ESD clamp circuit has an n×VDD-tolerant ESD detection circuit to improve the turn-on efficiency of the n×VDD-tolerant ESD clamp device, as shown in Fig. 6.6. The n×VDD-tolerant ESD detection circuit is composed of n low-leakage ESD detection circuits to divide n×VDD voltage into 1×VDD voltage by their self. Even if there is the process

variation, each low-leakage ESD detection circuit is expected to have almost the same variation due to the symmetry between these low-leakage ESD diction circuits. Thus, each low-leakage ESD diction circuit still sustains ~1×VDD voltage. In other words, this design prevents from gate-oxide overstress issue as all low-voltage devices sustain only 1×VDD voltage. Besides, the initial-on PMOS devices (Mt1, …, and Mtn) [95] exist in each low-leakage ESD detection circuits to effectively trigger the ESD clamp device under ESD stress conditions. The main ESD current discharging path is n×VDD-tolerant ESD clamp device, which consists of the SCR-based ESD clamp device. The SCR device, which is composed of cross-coupled p-n-p and n-p-n BJTs with regenerative feedback loop, can sustain high ESD level within a small silicon area in CMOS process. To improve the turn-on speed of SCR device under ESD stress conditions, the trigger currents can be absorbed from the base terminal of p-n-p BJT, and be injected to the base terminal of n-p-n BJT in SCR device. Besides, the SCR device has high enough holding voltage to prevent from latchup issue in nanoscale CMOS processes. Moreover, the SCR device without poly gate layer has good immunity against the gate-oxide overstress and gate-leakage problems.

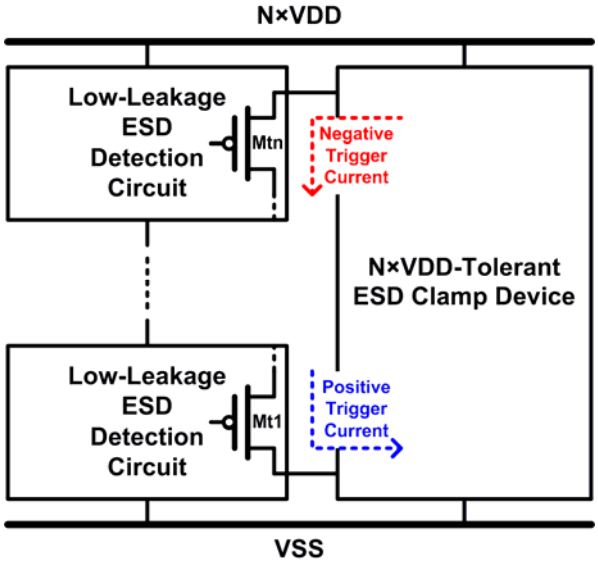


Fig. 6.6. New ESD clamp circuit with n×VDD-tolerant ESD detection circuit to trigger n×VDD-tolerant ESD clamp device.

6.4.2. 1×VDD-Tolerant ESD Detection Circuit

Fig. 6.7 shows a 1×VDD-tolerant ESD detection circuit of the n×VDD-tolerant ESD detection circuit. The 1×VDD-tolerant ESD detection circuit consists of the RC timer, inverters, feedback PMOS Mp4, and trigger PMOS Mt1. The RC timer is typically used to

enable the clamp during fast-edge ESD event and to isolate it from the power supply during normal power-on condition. Under normal circuit operating condition, the voltage of node 5 is biased at logic high, and no trigger current is generated in the trigger PMOS Mt1. In the mean time, the feedback PMOS Mp4 can lower the voltage drop across the RC timer, because the voltage of node 1 can be decreased as the voltage of node 5 is biased at logic high. Therefore, the voltage drop and gate-leakage current of the MOS capacitor under the normal circuit operating condition can be reduced. Fig. 6.8 shows the Hspice-simulated results of the 1×VDD-tolerant ESD detection circuit under normal circuit operating conditions. The node 2 voltage is only ~0.2 V. In other word, the voltage across MOS capacitor is only ~0.2×VDD, which is much lower than that in the traditional RC-based ESD detection circuits. Therefore, the gate-leakage current through the MOS capacitor can be significantly reduced, and the total leakage current can be reduced to ~0.15 μA at room temperature.

When a positive fast-transient ESD voltage is applied to the VDD line with VSS grounded, the trigger currents will pass through the initial-on PMOS Mt1 to trigger the ESD clamp device. In the mean time, the voltage of node 5 is still floating, so the voltage of node 1 can be charged through the PMOS Mp4 to logic high to turn on the NMOS Mn3. The RC delay keeps the voltage of node 2 at logic low, the voltage of node 3 at logic high, and the voltage of node 4 at logic low. Therefore, the voltage of node 5 can be kept at logic low through the turned-on NMOS Mn3, and the trigger PMOS Mt1 can continuously generate the trigger currents. Finally, the ESD clamp device can be fully turned-on into holding state to discharge ESD currents from VDD to VSS.

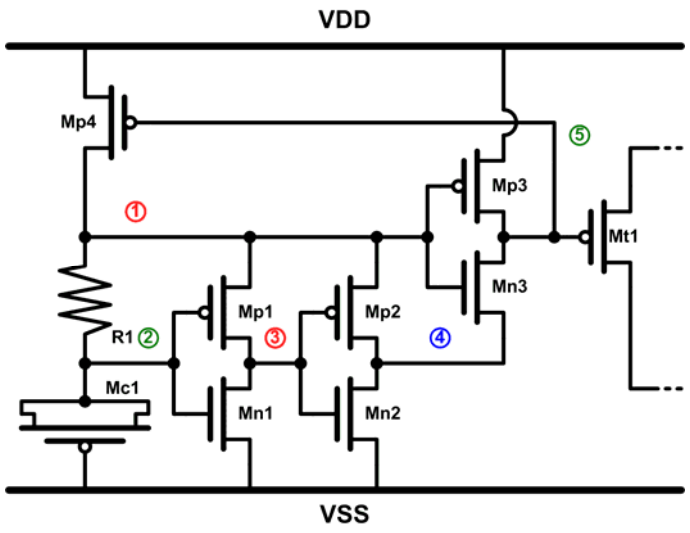


Fig. 6.7. Implementation of 1×VDD-tolerant ESD detection circuit.

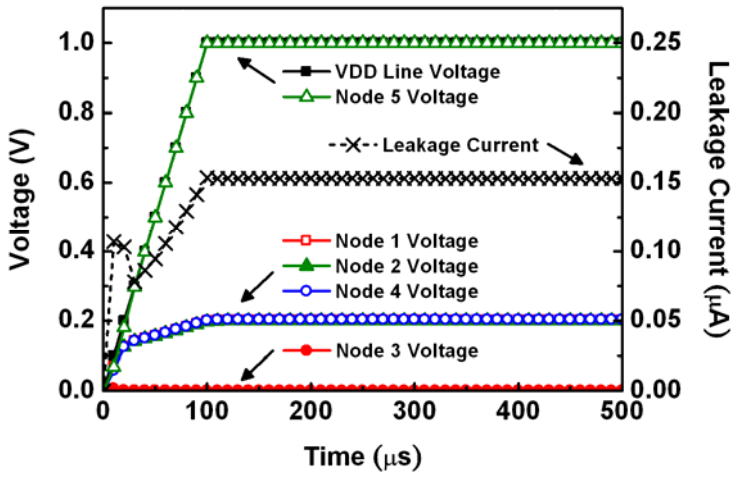


Fig. 6.8. Hspice-simulated results of 1×VDD-tolerant ESD detection circuit under normal power-on condition.

6.4.3. High-Voltage-Tolerant ESD Clamp Circuit

Fig. 6.9 shows the test circuit of the 2×VDD-tolerant ESD clamp circuit. The main ESD current discharging path consists of the double-triggered SCR (DTSCR) with a diode in series (DTSCR+diode). Although there is a parasitic SCR path in the DTSCR+diode structure, the parasitic SCR has the higher holding voltage due to the parasitic N-well resistor in the parasitic SCR path. Therefore, the DTSCR+diode structure has high enough holding voltage to prevent from latchup issue. The SCR device and the forward biased diode can sustain high ESD level within a small silicon area in CMOS process. Fig. 6.10(a) shows the Hspice-simulated results of the 2×VDD-tolerant ESD clamp circuit under normal circuit operating conditions. Under simulations, the ESD clamp device in Fig. 6.9 is replaced by two 100-Ω resistors, which are between the trigger PMOS Mt2 (Mt1) and VDD (VSS), to simplify the simulation. With 2-V 2×VDD and grounded VSS, node B (1×VDD) of the circuit in Fig. 6.9 is 1 V. In other words, all low-voltage devices sustain only 1 V. Therefore, all low-voltage devices prevent from gate-oxide overstress issue. The total leakage current is only ~0.15 μA at 25 °C. As the temperature varies from 25 °C to 100 °C, Fig. 6.10(b) summarizes the simulated results under normal circuit operating conditions. The node B (1×VDD) voltage is exactly at 1 V, even if the temperature varies from 25 °C to 100 °C.

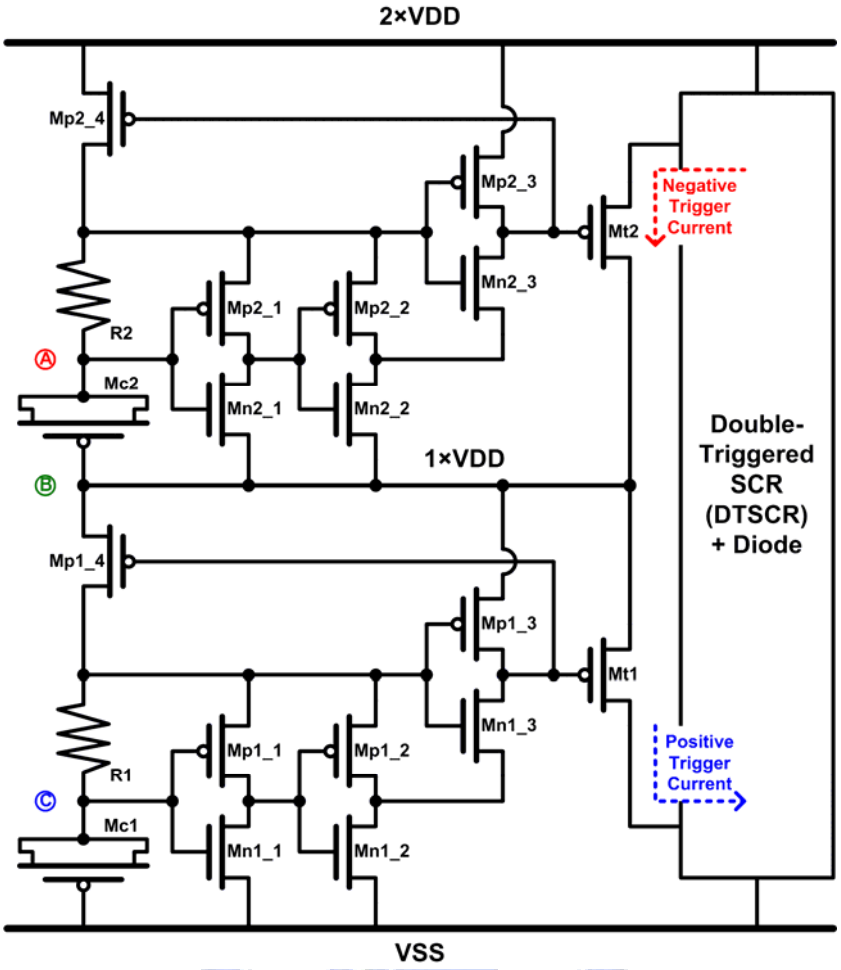
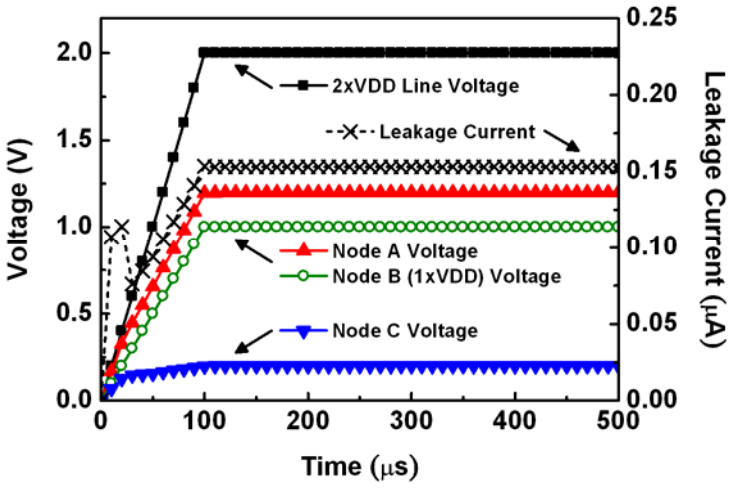
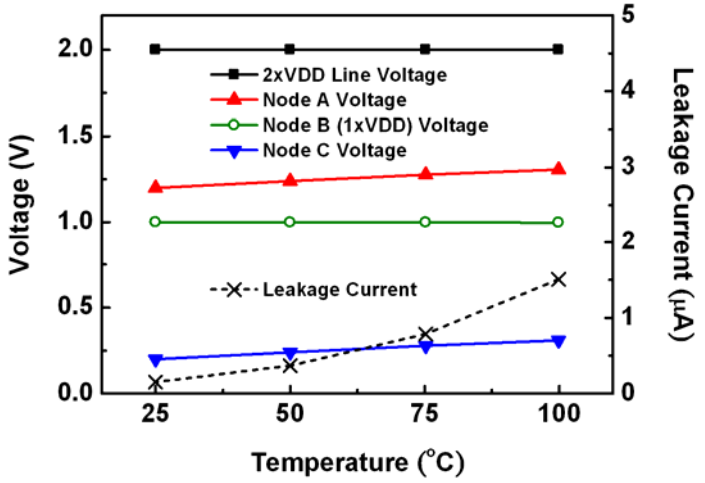


Fig. 6.9. Implementation of 2×VDD-tolerant ESD clamp circuit with 2×VDD-tolerant ESD detection circuit and SCR-based ESD clamp device.

Fig. 6.11 shows the simulated transient responses of the 2×VDD-tolerant ESD clamp circuit. With the voltage disturbance on 2×VDD line, the ESD detection circuit is accidentally turned-on under normal circuit operating condition. However, the MOS capacitors can be restored to logic high to turn off the trigger currents. Therefore, this design can prevent from latch events.



(a)



(b)

Fig. 6.10. Hspice-simulated results of 2×VDD-tolerant ESD clamp circuit under normal power-on condition: (a) at 25 °C, and (b) summary within 25 °C and 100 °C.

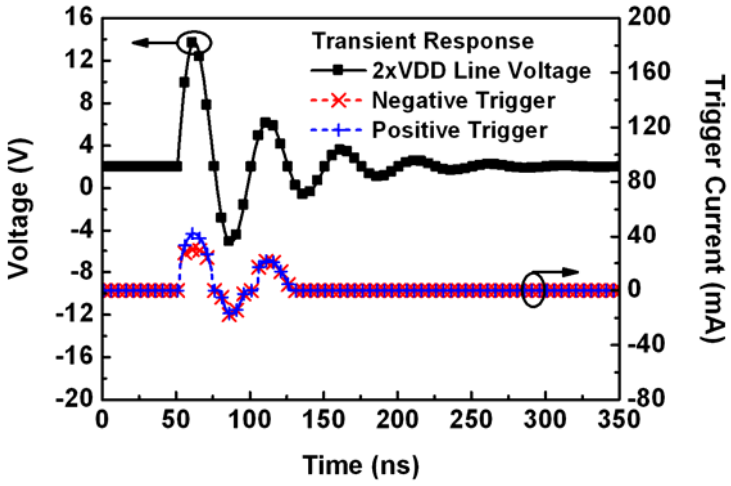
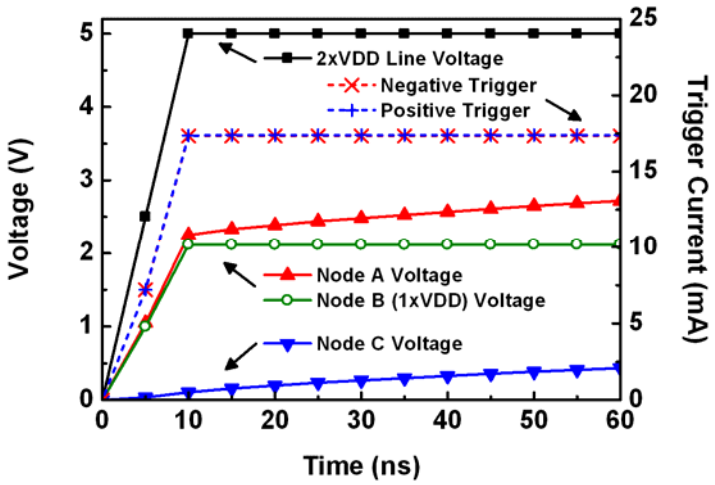
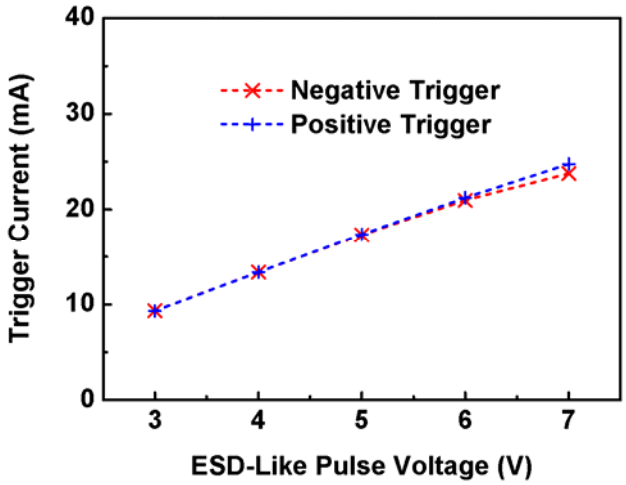


Fig. 6.11. Hspice-simulated transient responses of 2×VDD-tolerant ESD clamp circuit.

When a positive fast-transient ESD voltage is applied to 2×VDD line with VSS grounded, the trigger currents will pass through the initial-on PMOS (Mt1 and Mt2) to trigger the DTSCR device. The RC delay keeps the trigger PMOS (Mt1 and Mt2) turned-on to continuously generate the trigger currents. Finally, the DTSCR device can be fully turned-on into holding state to discharge ESD currents from 2×VDD line to VSS. Fig. 6.12(a) shows the simulation results of the ESD detection circuit under 5-V ESD-like pulse zapping to simulate the fast transient voltage of human-body-model (HBM) ESD events, and Fig. 6.12(b) summarizes that under different voltage pulse zapping. The trigger currents can be successfully generated.



(a)



(b)

Fig. 6.12. Hspice-simulated results of 2×VDD-tolerant ESD detection circuit under ESD-like pulse zapping: (a) 5-V pulse, and (b) summary of different voltage pulse.

The 2×VDD-tolerant ESD clamp devices with and without the ESD detection circuit have been fabricated in a 1-V 65-nm CMOS process. The size of ESD clamp devices are design to pass the general requirement of 2-kV (4-kV) HBM ESD level, so the size of DTSCR and diode are all selected to be 25 μm (50 μm). Besides, Mt1 and Mt2 of ESD detection circuit are also selected to be 25 μm (50 μm). The layout top view of one test pattern with the high-voltage-tolerant ESD clamp circuit is shown in Fig. 6.13.

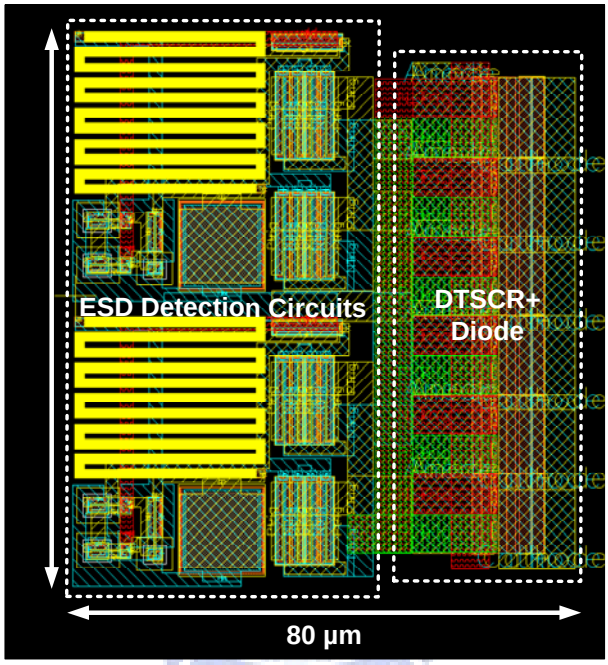


Fig. 6.13. Layout top view of one test pattern with high-voltage-tolerant ESD clamp circuit.

6.4.4. Experimental Results

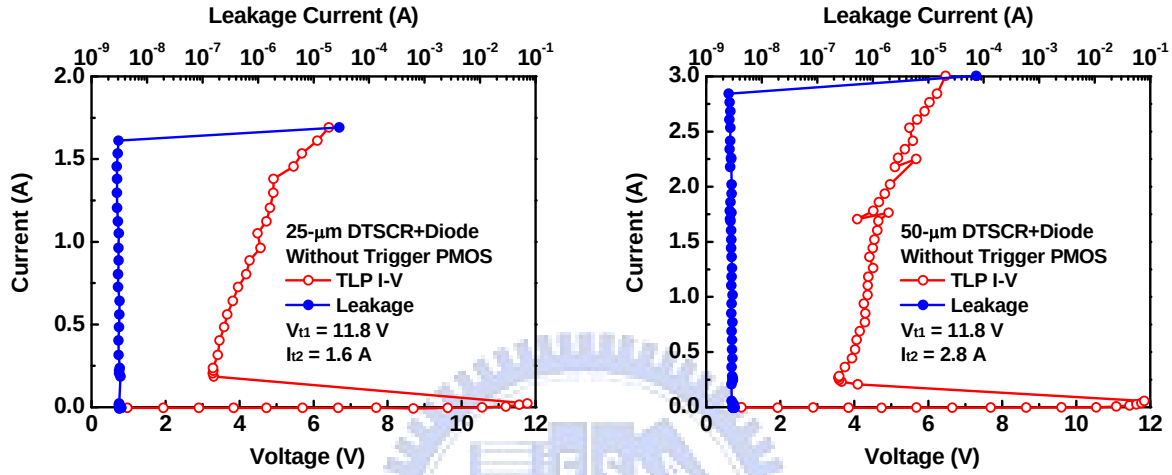
The I-V characteristics of the circuits are measured by using transmission line pulsing (TLP) system with 10-ns rise time and 100-ns pulse width. Figs. 6.14, 6.15, and 6.16 show the TLP-measured I-V curves of the ESD clamp circuits.

Fig. 6.14 shows the TLP-measured I-V curves of the stand-alone ESD clamp devices without the ESD detection circuit. The trigger voltages (V_{t1}) of each stand-alone ESD clamp devices without the ESD detection circuit are 11.8 V. The secondary breakdown currents (I_{t2}) of ESD clamp devices are 1.6 A and 2.8 A, respectively.

Fig. 6.15 shows the TLP-measured I-V curves of the ESD clamp circuits with the 25-μm trigger PMOS (Mt1 and Mt2). The trigger voltages (V_{t1}) of the ESD clamp circuits with 25-μm and 50-μm DTSCR are reduced to 6.7 V and 7.3 V, respectively. The secondary

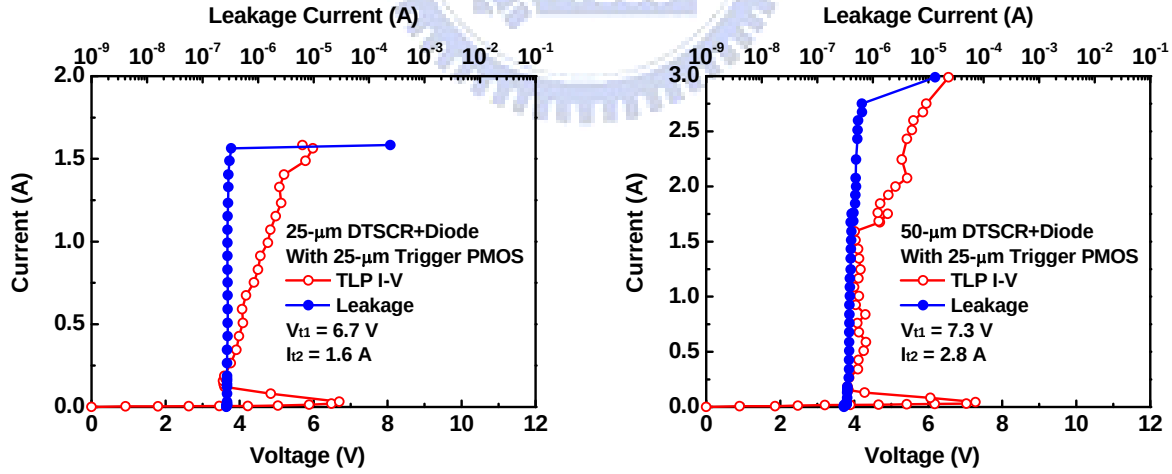
breakdown currents (I_{t2}) of ESD clamp devices are kept 1.6 A and 2.8 A, respectively.

Fig. 6.16 shows the TLP-measured I-V curves of the ESD clamp circuits with the 50-μm trigger PMOS (Mt1 and Mt2). The trigger voltages (V_{t1}) of the ESD clamp circuits with 25-μm and 50-μm DTSCR are reduced to 6 V and 6.5 V, respectively. The secondary breakdown currents (I_{t2}) of ESD clamp devices are 1.6 A and 2.9 A, respectively. These data are summarized in Table 6.1.



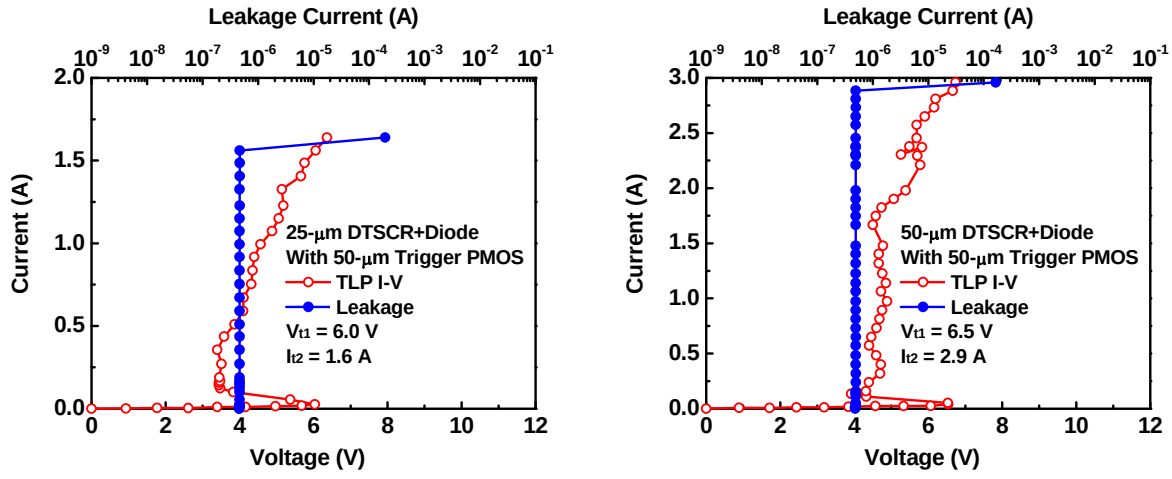
(a) (b)

Fig. 6.14. TLP I-V curves of (a) 25-μm and (b) 50-μm DTSCR+diode without trigger PMOS.



(a) (b)

Fig. 6.15. TLP I-V curves of (a) 25-μm and (b) 50-μm DTSCR+diode with 25-μm trigger PMOS.



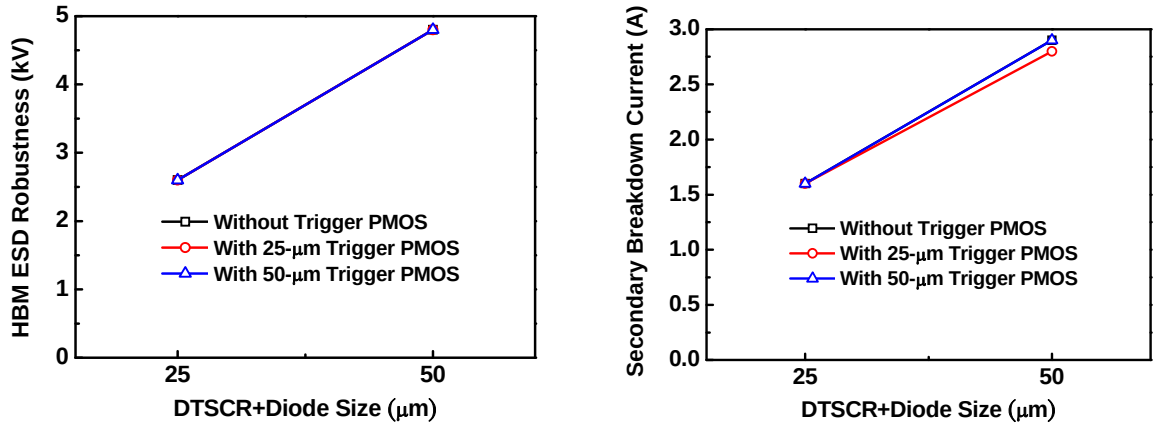
(a) (b)

Fig. 6.16. TLP I-V curves of (a) 25-μm and (b) 50-μm DTSCR+diode with 50-μm trigger PMOS.

The HBM ESD robustness of the fabricated ESD clamp circuits are evaluated by the ESD simulator. Fig. 6.17(a) shows the HBM ESD robustness of all ESD clamp circuits, and Fig. 6.17(b) summarizes the I_{t2} levels of all ESD clamp circuits. All ESD clamp devices with 25-μm (50-μm) size can achieve 2.6-kV (4.8-kV) HBM ESD robustness. These data are also summarized in Table 6.1.

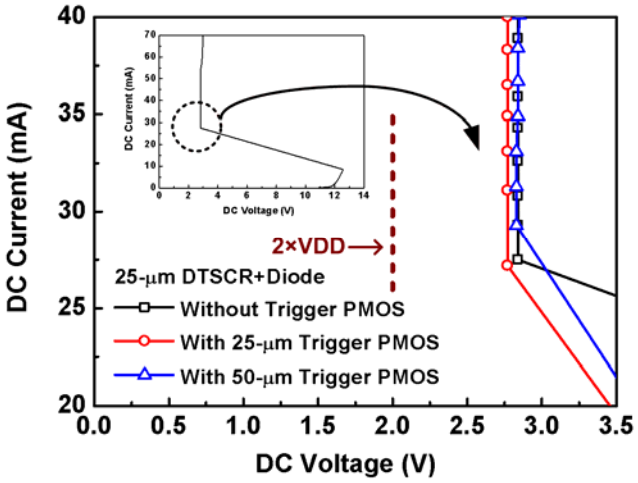
The dc I-V characteristics of ESD clamp circuits are measured by using Tek370 curve tracer. The measured dc holding voltages (V_{hold}) of all ESD clamp circuits under room temperature are ~2.8 V, as shown in Fig. 6.18. All the dc holding voltages exceed 2×VDD (2 V) with 0.8-V margin, which is very safe from latchup event under normal circuit operating condition.

The standby leakage current of the stand-alone 25-μm (50-μm) DTSCR in series with diode under 2-V bias at room temperature is only 4 nA (5 nA). Even if the 25-μm trigger PMOS is applied to the 25-μm (50-μm) DTSCR in series with diode, the standby leakage current under 2-V bias at room temperature is 148 nA (170 nA). As the 50-μm trigger PMOS is applied to the 25-μm (50-μm) DTSCR in series with diode, the standby leakage current under 2-V bias at room temperature is 264 nA (293 nA). Although the leakage current is increased with the insert of ESD detection circuit, the trigger voltage can be significantly reduced to effectively protect the core circuits. Therefore, the ESD clamp circuit of this work can provide the excellent ESD robustness with low standby leakage current by using only low-voltage devices.

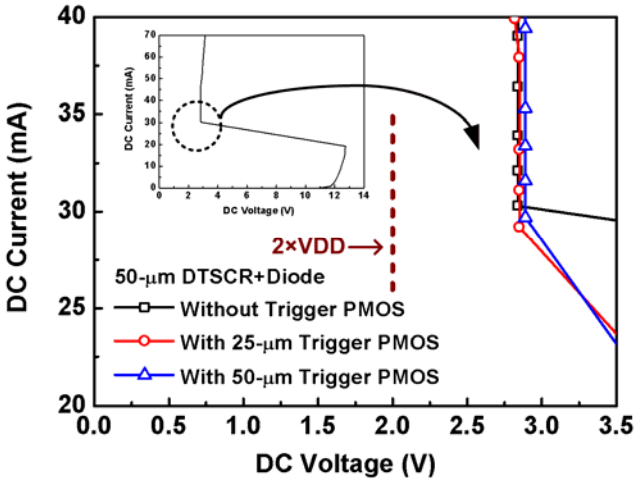


(a) (b)

Fig. 6.17. (a) HBM ESD robustness and (b) secondary breakdown current of ESD clamp circuits.



(a)



(b)

Fig. 6.18. Measured dc holding voltages of ESD clamp circuits with (a) 25-μm and (b) 50-μm ESD clamp devices under room temperature.

Table 6.1

Comparison Among ESD Clamp Circuits

ESD Detection Circuits	ESD Clamp Devices	TLP V_{t1} (V)	TLP I_{t2} (A)	HBM ESD (kV)	DC V_{hold} @ 25°C (V)	I_{Leak} @ 25°C / 2V (nA)	I_{Leak} @ 50°C / 2V (nA)	I_{Leak} @ 100°C / 2V (nA)
None	25-μm DTSCR + Diode	11.8	1.6	2.6	2.8	4	4	6
	50-μm DTSCR + Diode	11.8	2.9	4.8	2.8	5	6	8
With 25-μm Trigger PMOS	25-μm DTSCR + Diode	6.7	1.6	2.6	2.8	148	349	1304
	50-μm DTSCR + Diode	7.3	2.8	4.8	2.8	170	368	1480
With 50-μm Trigger PMOS	25-μm DTSCR + Diode	6.0	1.6	2.6	2.8	264	571	2807
	50-μm DTSCR + Diode	6.5	2.9	4.8	2.9	293	871	3115

6.5. Summary

The new 2×VDD-tolerant ESD clamp circuit by using only low-voltage devices with low standby leakage current and high ESD robustness for SoC applications with mixed-voltage I/O interfaces has been successfully designed and verified in a 65-nm CMOS process. The 2×VDD-tolerant ESD clamp circuit can operate without gate-oxide reliability issue, and the leakage current is only in the order of 100 nA under normal circuit operating condition. The HBM ESD robustness of the test patterns with 25-μm and 50-μm ESD clamp devices can achieve 2.6 kV and 4.8 kV, respectively. In addition, the new ESD detection circuit shows significant help on increasing the turn-on speed of ESD clamp device. With trigger currents generated from the ESD detection circuit, the trigger voltage of the SCR-based ESD clamp device can be reduced as compared with the stand-alone SCR device. The TLP-measured trigger voltage of the ESD clamp device with the ESD detection circuit is ~6 V. Besides, the holding voltage of each ESD clamp circuits is ~2.8 V, which is much greater than 2×VDD voltage (2 V). Therefore, there is no latchup concern in this design. The new ESD clamp circuit by using only low-voltage devices with very low standby leakage current and high ESD robustness is the useful circuit solution for on-chip ESD protection design with mixed-voltage I/O interfaces in SoC applications.

Chapter 7

Conclusions and Future Works

This chapter summarizes the main results and contributions of this dissertation. Future works for the fields of SCR-based ESD protection designs for RF circuits in fully silicided CMOS process are also provided in this chapter.

7.1. Main Results of This Dissertation

The nanoscale CMOS processes are attractive to implement RF circuits. With the evolution of CMOS technology, ESD protection design in nanoscale CMOS processes becomes more challenging. In this dissertation, a cross-coupled-SCR ESD protection scheme for differential input pads is presented to protect the differential LNA. Experimental results have shown that this ESD protection circuit co-designed with the input matching network of the LNA can achieve excellent ESD robustness and good RF performance. Besides using SCR for ESD protection on LNA, the optimized layout structure on SCR device with low capacitance is studied. The waffle-structured SCR with low parasitic capacitance is suitable for on-chip ESD protection in RF ICs. This waffle-structured SCR has been applied to an UWB RF power amplifier. The measurement results verify that low-capacitance ESD protection strategy with the waffle-structured SCR indeed provides excellent ESD robustness. Besides the low-capacitance SCR, the small-signal model of SCR in RF frequency band is presented. The RF circuits can be well co-designed with the presented small-signal model to eliminate the negative impacts from ESD protection SCR on RF performances. As the operating frequencies of RF front-end circuits are increased, on-chip ESD protection designs for RF applications are more challenging, and they should be designed more carefully.

To reduce the parasitic effects of ESD devices connected to the I/O pad, the efficient power-rail ESD clamp circuit must be included into the RF ICs. With the consideration of low standby leakage in nanoscale CMOS processes, a new 2×VDD-tolerant ESD clamp circuit by using only 1×VDD devices was presented. The new ESD clamp circuit by using only low-voltage devices with very low standby leakage current and high ESD robustness is

the useful circuit solution for on-chip ESD protection design in SoC applications. The contributions of each chapter in this dissertation are presented in the following.

In chapter 2, the pin-to-pin ESD protection design on a 5-GHz differential LNA is proposed. The 5-GHz differential LNA is implemented in a 130-nm CMOS process. The reference differential LNA without ESD protection has 16.2-dB power gain and 2.16-dB noise figure at operating frequency. The conventional double-diode ESD protection scheme is realized for the differential LNA, which has 2.5-kV HBM and 200-V MM ESD robustness. The differential LNA with double-diode ESD protection has 17.9-dB power gain and 2.43-dB noise figure at operating frequency. The ESD protection design using cross-coupled SCR devices between the differential input pads is also proposed. Besides providing ESD protection for a single input pad, pin-to-pin ESD protection is also achieved without adding any extra devices. This ESD protection scheme achieves 3.5-kV HBM and 300-V MM ESD levels, respectively. The power gain and noise figure of this differential LNA are 17.2 dB and 3.58 dB at operating frequency, respectively. All of the fabricated differential LNAs consume 10.3 mW from the 1.2-V power supply.

SCR has been used as an effective on-chip ESD protection device in CMOS technology due to the highest ESD robustness in nanoscale ICs. In chapter 3, SCR realized in waffle layout structure is proposed to improve ESD current distribution efficiency for ESD protection and to reduce the parasitic capacitance. The waffle layout structure of SCR can achieve smaller parasitic capacitance under the same ESD robustness. With smaller parasitic capacitance, the degradation on RF circuit performance due to ESD protection devices can be reduced. The proposed waffle SCR with low parasitic capacitance is suitable for on-chip ESD protection in RF ICs. Besides, the desired current to trigger on the SCR device with waffle layout structure and its turn-on time has also been investigated in silicon chip.

With the reduced parasitic capacitance, the waffle-structured SCR co-designed with PA was investigated in chapter 4. The waffle-structured SCR is designed with ESD detection and trigger circuit to provide the best ESD protection capability while contributing minimum parasitic capacitance to the RF PA. The measurement results have verified the effectiveness of the proposed ESD protection strategy and proved that this ESD protection technique indeed provides excellent ESD robustness of up to 8kV HBM ESD level and 800V MM ESD level.

In chapter 5, the small-signal circuit model of waffle-structured SCR has been presented and proved in silicon. The measured parasitic capacitances well agree with the simulated capacitances. The RF circuits can be well co-designed with the presented small-signal model

to eliminate the negative impacts from ESD protection SCR on RF performances. Besides, the optimized design of the bond pad for RF applications was also investigated. The experimental results in a 65-nm CMOS process have proven that the bond pad capacitance and insertion loss can be successfully reduced by the optimized bond pad structure. The small-signal circuit model of the optimized bond pad has also been presented for RF circuit designs.

In chapter 6, the new 2×VDD-tolerant ESD clamp circuit by using only low-voltage devices with low standby leakage current and high ESD robustness for SoC applications with mixed-voltage I/O interfaces has been successfully designed and verified in a 65-nm CMOS process. The 2×VDD-tolerant ESD clamp circuit can operate without gate-oxide reliability issue, and the leakage current is only in the order of 100 nA under normal circuit operating condition. Besides, there is no latchup concern in this design. The new ESD clamp circuit by using only low-voltage devices with very low standby leakage current and high ESD robustness is the useful circuit solution for on-chip ESD protection design with mixed-voltage I/O interfaces in SoC applications.

7.2. Future Works

The designs for RF circuits applied to higher frequency band is a popular topic in advanced CMOS technology. The V band occupied from 40 to 75 GHz frequency band. The V band is primarily used for high capacity and short distance communication systems. For example, WirelessHD is the recent technology that operates near the 60-GHz range. To achieve successful ESD protection design for such high-frequency RF circuits, precise modeling of ESD protection devices is necessary. Hence, modeling of ESD protections in such high frequency bands is needed.

In an fully integrate SoC chip with RF frond-end and baseband circuits, the larger die size for SoC applications and the thinner gate oxide in nanoscale CMOS transistors will become the design concerns. With the larger die size and the thinner gate oxide, nanoscale CMOS ICs are very sensitive to charged-device model (CDM) ESD events. Therefore, the efficient CDM ESD protections should be designed in nanoscale CMOS process.

Inductors are often used to compensate the parasitic capacitance of ESD protection devices in RF bands. Besides, the inductor can act like the conductive path under ESD stress conditions, which can be used as the ESD detection circuit for the trigger design on SCR devices. Thus, developing inductor-based ESD detection circuit for SCR devices in RF

circuits is promising in the future.

References

[1] S. Voldman, *ESD: Circuits and Devices*, John Wiley & Sons, 2006.

[2] S. Voldman, *ESD: RF Technology and Circuits*. John Wiley & Sons, 2006.

[3] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, John Wiley & Sons, 2002.

[4] S. Dabral and T. Maloney, *Basic ESD and I/O Design*. John Wiley & Sons, 1998.

[5] *Electrostatic Discharge (ESD) Sensitivity Testing—Human Body Model (HBM)*, EIA/JEDEC Standard Test Method 5.1, 2001.

[6] *Electrostatic Discharge (ESD) Sensitivity Testing—Machine Model (MM)*, EIA/JEDEC Standard Test Method 5.2, 1999.

[7] M.-D. Ker, W.-Y. Lo, C.-M. Lee, C.-P. Chen, and H.-S. Kao, "ESD protection design for 900-MHz RF receiver with 8-kV HBM ESD robustness," in *Proc. IEEE Radio Freq. Integrated Circuit Symp.*, 2002, pp. 427-430.

[8] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173-183, Jan. 1999.

[9] C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini, "Investigation on different ESD protection strategies devoted to 3.3 V RF applications (2 GHz) in a 0.18um CMOS process," in *Proc. EOS/ESD Symp.*, 2000, pp. 251-259.

[10] M.-D. Ker and C.-M. Lee, "Interference of ESD protection diodes on RF performance in giga-Hz RF circuits," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2003, pp. 297-300.

[11] K. Gong, H. Feng, R. Zhan, and A. Wang, "A study of parasitic effects of ESD protection on RF ICs," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 393-402, Jan. 2002.

[12] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998.

[13] G. Boselli, J. Rodriguez, C. Duvvury, and J. Smith, "Analysis of ESD protection components in 65-nm CMOS technology: scaling perspective and impact on ESD design windows," in *Proc. EOS/ESD Symp.*, 2005, pp. 43-52.

[14] P. Leroux, M. Steyaert, V. Vassilev, and G. Groeseneken, "A 1.3dB NF CMOS LNA for GPS with 3kV HBM ESD-protection," in *Proc. Eur. Solid-State Circuits Conf.*, 2002, pp. 335-338.

[15] M.-D. Ker, T.-Y. Chen, and C.-Y. Chang, "ESD protection design for CMOS RF integrated circuits," in *Proc. EOS/ESD Symp.*, 2001, pp. 346-354.

[16] M.-D. Ker and C.-Y. Chang, "ESD protection design for CMOS RF integrated circuits using polysilicon diodes," *J. Microelectron. Reliab.*, vol. 42, no. 6, pp. 863-872, Jun. 2002.

[17] X. Jin, L. Tse, K. Tsai, G. Chien, and S. Wei, "Methods and apparatus for improving high frequency input/output performance," U.S. Patent 6911739, Jun. 2005.

[18] X. Jin, L. Tse, K. Tsai, G. Chien, and S. Wei, "Methods and apparatus for improving high frequency input/output performance," U.S. Patent 6977444, Dec. 2005.

[19] X. Jin, L. Tse, K. Tsai, G. Chien, and S. Wei, "Methods and apparatus for improving high frequency input/output performance," U.S. Patent 6987326, Jan. 2006.

[20] X. Jin, L. Tse, K. Tsai, G. Chien, and S. Wei, "Methods and apparatus for improving high frequency input/output performance," U.S. Patent 7009308, Mar. 2006.

[21] S. Hyvonen, S. Joshi, and E. Rosenbaum, "Comprehensive ESD protection for RF inputs," *J. Microelectron. Reliab.*, vol. 45, no. 2, pp. 245-254, Feb. 2005.

[22] S. Hyvonen and E. Rosenbaum, "Diode-based tuned ESD protection for 5.25-GHz CMOS LNAs," in *Proc. EOS/ESD Symp.*, 2005, pp. 9-17.

[23] T. Tsukada, Y. Hashimoto, K. Sakata, H. Okada, and K. Ishibashi, "An on-chip active decoupling circuit to suppress crosstalk in deep-submicron CMOS mixed-signal SoCs," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 67-79, Jan. 2005.

[24] M.-D. Ker, C.-M. Lee, and W.-Y. Lo, "Electrostatic discharge protection device for giga-Hz radio frequency integrated circuits with varactor-LC tanks," U.S. Patent 6885534, Apr. 2005.

[25] M.-D. Ker, C.-M. Lee, and T.-Y. Chen, "Electrostatic discharge protection designs with parallel LC tank for giga-Hz RF integrated circuits," U.S. Patent 7009826, Mar. 2006.

[26] M.-D. Ker, C.-M. Lee, and T.-Y. Chen, "ESD protection designs with parallel LC tank for giga-Hz RF integrated circuits," U.S. Patent 7023677, Apr. 2006.

[27] M.-D. Ker, C.-M. Lee, and T.-Y. Chen, "ESD protection designs with parallel LC tank for giga-Hz RF integrated circuits," U.S. Patent 7023678, Apr. 2006.

[28] M.-D. Ker, C.-I. Chou, and C.-M. Lee, "A novel LC-tank ESD protection design for giga-Hz RF circuits," in *Proc. IEEE Radio Freq. Integrated Circuit Symp.*, 2003, pp. 115-118.

[29] C. Yue, S. Wong, D. Su, and W. McFarland, "System for providing electrostatic discharge protection for high-speed integrated circuits," U.S. Patent 6509779, Jan.

2003.

[30] C. Yue, S. Wong, D. Su, and W. McFarland, "System for providing electrostatic discharge protection for high-speed integrated circuits," U.S. Patent 6593794, Jul. 2003.

[31] C. Yue, S. Wong, D. Su, and W. McFarland, "System for providing electrostatic discharge protection for high-speed integrated circuits," U.S. Patent 6597227, Jul. 2003.

[32] J. Leete, "Electrostatic protection circuit with impedance matching for radio frequency integrated circuits," U.S. Patent 6771475, Aug. 2004.

[33] B.-S. Huang and M.-D. Ker, "New matching methodology of low-noise amplifier with ESD protection," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2006, pp. 4891-4894.

[34] J. Zerbe, V. Stojanovic, M. Horowitz, and P. Chau, "Input/output circuit with on-chip inductor to reduce parasitic capacitance," U.S. Patent 7005939, Feb. 2006.

[35] A. Rofougaran, "Radio frequency integrated circuit electro-static discharge circuit," U.S. Patent 7010279, Mar. 2006.

[36] D. Linten, S. Thijs, M. Natarajan, P. Wambacq, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Donnay, and S. Decoutere, "A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1434-1442, Jul. 2005.

[37] P. Leroux and M. Steyaert, "A 5 GHz CMOS low-noise amplifier with inductive ESD protection exceeding 3 kV HBM," in *Proc. Eur. Solid-State Circuits Conf.*, 2004, pp. 295-298.

[38] J. Borremans, S. Thijs, P. Wambacq, D. Linten, Y. Rolain, and M. Kuijk, "A 5 kV HBM transformer-based ESD protected 5-6 GHz LNA," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2007, pp. 100-101.

[39] S. Galal and B. Razavi, "Broadband ESD protection circuits in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2334-2340, Dec. 2003.

[40] M. Kossel, C. Menolfi, J. Weiss, P. Buchmann, G. von Bueren, L. Rodoni, T. Morf, T. Toifl, and M. Schmatz, "A T-coil-enhanced 8.5Gb/s high-swing source-series-terminated transmitter in 65nm bulk CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2008, pp. 110-111.

[41] D. Linten, S. Thijs, J. Borremans, M. Dehan, D. Tremouilles, M. Scholz, M. Natarajan, P. Wambacq, and G. Groeseneken, "T-diodes - a novel plug-and-play wideband RF circuit ESD protection methodology," in *Proc. EOS/ESD Symp.*, 2007, pp. 242-249.

[42] B. Kleveland and T. Lee, "Distributed ESD protection device for high speed integrated circuits," U.S. Patent 5969929, Oct. 1999.

[43] B. Kleveland, T. Maloney, I. Morgan, L. Madden, T. Lee, and S. Wong, "Distributed ESD protection for high-speed integrated circuits," *IEEE Electron Device Lett.*, vol. 21, no. 8, pp. 390-392, Aug. 2000.

[44] C. Ito, K. Banerjee, and R. Dutton, "Analysis and design of distributed ESD protection circuits for high-speed mixed-signal and RF ICs," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1444-1454, Aug. 2002.

[45] M.-D. Ker and B.-J. Kuo, "Decreasing-size distributed ESD protection scheme for broadband RF circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 582-589, Feb. 2005.

[46] M.-D. Ker, B.-J. Kuo, and Y.-W. Hsiao, "Optimization of broadband RF performance and ESD robustness by π-model distributed ESD protection scheme," *J. Electrostatics*, vol. 64, no. 2, pp. 80-87, Feb. 2006.

[47] M.-D. Ker and C.-M. Lee, "ESD protection circuits with impedance matching for radio-frequency applications," U.S. Patent 2006/0256489 A1, Nov. 2006.

[48] D. Cassan and J. Long, "A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 427-435, Mar. 2003.

[49] C.-H. Liao and H.-R. Chuang, "A 5.7-GHz 0.18-μm CMOS gain-controlled differential LNA with current reuse for WLAN receiver," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 12, pp. 526-528, Dec. 2003.

[50] W. Zhuo, X. Li, S. Shekhar, S. Embabi, J. Pineda de Gyvez, D. Allstot, and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 12, pp. 875-879, Dec. 2005.

[51] R. Salerno, M. Tiebout, H. Paule, M. Streibl, C. Sandner, and K. Kropf, "ESD-protected CMOS 3-5GHz wideband LNA+PGA design for UWB," in *Proc. Eur. Solid-State Circuits Conf.*, 2005, pp. 219-222.

[52] A. Bevilacqua, C. Sandner, A. Gerosa, and A. Neviani, "A fully integrated differential CMOS LNA for 3-5-GHz ultrawideband wireless receivers," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 3, pp. 134-136, Mar. 2003.

[53] T. Chang, J. Chen, L. Rigge, and J. Lin, "ESD-protected wideband CMOS LNAs using modified resistive feedback techniques with chip-on-board packaging," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 8, pp. 1817-1826, Aug. 2008.

[54] Y. Cao, V. Issakov, and M. Tiebout, "A 2kV ESD-protected 18GHz LNA with 4dB NF in 0.13μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2008, pp.

194-195.

[55] A. Wang, *On-Chip ESD Protection for Integrated Circuits*. Kluwer, 2002.

[56] M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD protection design on analog pin with very low input capacitance for high-frequency or current-mode applications," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1194-1199, Aug. 2000.

[57] Y.-W. Hsiao and M.-D. Ker, "An ESD-protected 5-GHz differential low-noise amplifier in a 130-nm CMOS process," in *Proc. Custom Integrated Circuits Conf.*, 2008, pp. 233-236.

[58] D. Shaeffer and T. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745-759, May 1997.

[59] M.-D. Ker and K.-C. Hsu, "Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits," *IEEE Trans. Device Mater. Reliab.*, vol. 5, no. 2, pp. 235-249, Jun. 2005.

[60] W. Soldner, M.-J. Kim, M. Streibl, H. Gossner, T. Lee, and D. Schmitt-Landsiedel, "A 10GHz broadband amplifier with bootstrapped 2kV ESD protection," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. papers*, 2007, pp. 550-551.

[61] M.-D. Ker and C.-Y. Lin, "Low-capacitance SCR with waffle layout structure for on-chip ESD protection in RF ICs," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, pp. 1286-1294, May 2008.

[62] M.-D. Ker and C.-Y. Wu, "Modeling the positive-feedback regenerative process of CMOS latchup by a positive transient pole method-Part I: theoretical derivation," *IEEE Trans. Electron Devices*, vol. 42, no. 6, pp. 1141-1148, Jun. 1995.

[63] Y. Zhou, J. Hajjar, A. Righter, and K. Lisiak, "Modeling snapback of LVTSCR devices for ESD circuit simulation using advanced BJT and MOS models," in *Proc. EOS/ESD Symp.*, 2007, pp. 175-184.

[64] P. Juliano and E. Rosenbaum, "A novel SCR macromodel for ESD circuit simulation," in *IEDM Tech. Dig.*, 2001, pp. 319-322.

[65] M. Natarajan, D. Linten, S. Thijs, P. Jansen, D. Tremouilles, W. Jeamsaksiri, T. Nakaie, M. Sawada, T. Hasebe, S. Decoutere, and G. Groeseneken, "RFCMOS ESD protection and reliability," in *Proc. IEEE Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2005, pp. 59-66.

[66] M.-D. Ker and C.-M. Lee, "ESD protection design for giga-Hz RF CMOS LNA with novel impedance-isolation technique," in *Proc. EOS/ESD Symp.*, 2003, pp. 204-213.

[67] J.-H. Lee, Y.-H. Wu, K.-R. Peng, R.-Y. Chang, T.-L. Yu, and T.-C. Ong, "The embedded

SCR NMOS and low capacitance ESD protection device for self-protection scheme and RF application," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2002, pp. 93-96.

[68] K. Higashi, A. Adan, M. Fukumi, N. Tanba, T. Yoshimasu, and M. Hayashi, "ESD protection of RF circuits in standard CMOS process," in *RFIC Symp. Dig.*, Jun. 2002, pp. 31-34.

[69] M.-D. Ker and K.-H. Lin, "ESD protection design for I/O cells with embedded SCR structure as power-rail ESD clamp device in nanoscale CMOS technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2329-2338, Nov. 2005.

[70] W. Wu, S. Lam, and M. Chan, "Effects of layout methods of RFCMOS on noise performance," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2753-2759, Dec. 2005.

[71] S. Dabral and K. Seshan, "Diode and transistor design for high speed I/O," US Patent 7012304, Mar. 2006.

[72] D. Pozar, *Microwave Engineering*, 2nd ed. New York: Wiley, 1998.

[73] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004.

[74] B. Ballweber, R. Gupta, and D. Allstot, "A fully integrated 0.5-5.5 GHz CMOS distributed amplifier," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 231-239, Feb. 2000.

[75] J. Li, S. Joshi, R. Barnes, and E. Rosenbaum, "Compact modeling of on-chip ESD protection devices using Verilog-A", *IEEE Trans. Computer-Aided Design Integrated Circuits Systems*, vol. 25, no. 6, pp. 1047-1063, Jun. 2006.

[76] V. Vassilev, G. Groeseneken, S. Jenei, R. Venegas, M. Steyaert, H. Maes, "Modelling and extraction of RF performance parameters of CMOS electrostatic discharge protection devices," in *Proc. EOS/ESD Symp.*, 2002, pp. 111-118.

[77] K. Chong and Y. Xie, "Low capacitance and high isolation bond pad for high-frequency RFICs," *IEEE Electron Device Lett.*, vol. 26, no. 10, pp. 746-748, Oct. 2005.

[78] M.-D. Ker, H.-C. Jiang, and C.-Y. Chang, "Design on the low-capacitance bond pad for high-frequency I/O circuits in CMOS technology," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2953-2956, Dec. 2001.

[79] S. Lam, P. Mok, P. Ko, and M. Chan, "High-isolation bonding pad design for silicon RFIC up to 20 GHz," *IEEE Electron Device Lett.*, vol. 24, no. 9, pp. 601-603, Sep. 2003.

[80] Y.-W. Hsiao and M.-D. Ker, "Bond pad design with low capacitance in CMOS

technology for RF applications," *IEEE Electron Device Lett.*, vol. 28, no. 1, pp. 68-70, Jan. 2007.

[81] T. Cheung and J. Long, "Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1183-1200, May 2006.

[82] D. Seo, H. Dabag, Y. Guo, M. Mishra, and G. McAllister, "High-voltage-tolerant analog circuits design in deep-submicrometer CMOS technologies," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 54, no. 10, pp. 2159-2166, Oct. 2007.

[83] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Overview and design of mixed-voltage I/O buffers with low-voltage thin-oxide CMOS transistors," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 53, no. 9, pp. 1934-1945, Sep. 2006.

[84] B. Serneels, T. Piessens, M. Steyaert, and W. Dehaene, "A high-voltage output driver in a 2.5-V 0.25-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 576- 583, Mar. 2005.

[85] T. Suzuki, M. Kojima, J. Iwahori, T. Morita, N. Isomura, K. Hashimoto, and N. Yokota, "A study of ESD robustness of cascoded NMOS driver," in *Proc. EOS/ESD Symp.*, 2007, pp. 403-407.

[86] T. Tang, S. Chen, S. Liu, M. Lee, C. Liu, M. Wang, and M. Jeng, "ESD protection for the tolerant I/O circuits using PESD implantation," *J. Electrostatics*, vol. 54, no. 3-4, pp. 293-300, Mar. 2002.

[87] W. Anderson and B. Krakauer, "ESD protection for mixed-voltage I/O using NMOS transistors stacked in a cascode configuration," in *Proc. EOS/ESD Symp.*, 1998, pp. 54-62.

[88] M.-D. Ker and W.-J. Chang, "ESD protection design with on-chip ESD bus and high-voltage-tolerant ESD clamp circuit for mixed-voltage I/O buffers," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1409-1416, Jun. 2008.

[89] L. Avery, "ESD protection for overvoltage friendly input/output circuits," U.S. Patent 5708550, Jan. 1998.

[90] M.-D. Ker and C.-T. Wang, "Design of high-voltage-tolerant ESD protection circuit in low-voltage CMOS processes," *IEEE Trans. Device Mater. Reliab.*, vol. 9, no. 1, pp. 49-58, Mar. 2009.

[91] S. Poon and T. Maloney, "New considerations for MOSFET power clamps," in *Proc. EOS/ESD Symp.*, 2002, pp. 1-5.

[92] M.-D. Ker, W.-J. Chang, C.-T. Wang, and W.-Y. Chen, "ESD protection for

mixed-voltage I/O in low-voltage thin-oxide CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2006, pp. 546-547.

[93] C.-T. Wang and M.-D. Ker, "Design of power-rail ESD clamp circuit with ultra-low standby leakage current in nanoscale CMOS technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 956-964, Mar. 2009.

[94] Y. Lin, C. Wu, C. Chang, R. Yang, W. Chen, J. Liaw, and C. Diaz, "Leakage scaling in deep submicron CMOS for SoC," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 1034-1041, Jun. 2002.

[95] S.-H. Chen and M.-D. Ker, "Implementation of initial-on ESD protection concept with PMOS-triggered SCR devices in deep-submicron CMOS technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1158-1168, May 2007.

Vita

姓　　名：林群祐 (Chun-Yu Lin)

性　　別：男

出生日期：民國 73 年 7 月 28 日

出 生 地：花蓮市

住　　址：花蓮市光復街 18-1 號

學　　歷：國立交通大學電子工程學系畢業 (91 年 9 月–95 年 1 月)

國立交通大學電子研究所碩士班 (95 年 2 月–95 年 8 月)

國立交通大學電子研究所博士班 (95 年 9 月入學)

論文名稱：全金屬矽化物互補式金氧半製程之矽控整流器及其在射頻電路之靜電放電防護設計與應用

SCR-Based ESD Protection Designs for Radio-Frequency Integrated Circuits in Fully Silicided CMOS Process

Publication List

(A) Referred Journal Papers:

[1] M.-D. Ker and **Chun-Yu Lin**, "Low-capacitance SCR with waffle layout structure for on-chip ESD protection in RF ICs," *IEEE Trans. Microwave Theory and Techniques*, vol. 56, no. 5, pp. 1286-1294, May 2008.

[2] **Chun-Yu Lin**, M.-D. Ker, and G.-X. Meng, "Low-capacitance and fast turn-on SCR for RF ESD protection," *IEICE Trans. Electronics*, vol. E91-C, no. 8, pp. 1321-1330, Aug. 2008.

[3] **Chun-Yu Lin** and M.-D. Ker, "Optimization on low-capacitance bond pad for RF applications in CMOS technology," submitted to *IEEE Microwave and Wireless Components Letters*.

[4] **Chun-Yu Lin** and M.-D. Ker, "High-voltage-tolerant ESD clamp circuit by using only low-voltage devices with low standby leakage in nanoscale CMOS process," submitted to *IEEE Trans. Electron Devices*.

[5] **Chun-Yu Lin**, M.-D. Ker, and Y.-W. Hsiao, "ESD protection design for differential low-noise amplifier with cross-coupled SCR," submitted to *IEEE Electron Device Letters*.

[6] **Chun-Yu Lin** and M.-D. Ker, "Modeling parasitic capacitance on ESD protection SCR for matching network co-designed in RF ICs," submitted to *IET Electronics Letters*.

(B) International Conference Papers:

[1] M.-D. Ker and **Chun-Yu Lin**, "Test structure on SCR device in waffle layout for RF ESD protection," in *Proc. IEEE International Conference on Microelectronic Test Structures*, 2007, pp.196-199.

[2] **Chun-Yu Lin** and M.-D. Ker, "Low-capacitance SCR with waffle layout structure for on-chip ESD protection in RF ICs," in *Proc. IEEE Radio Frequency Integrated Circuit Symposium*, 2007, pp. 749-752.

[3] **Chun-Yu Lin** and M.-D. Ker, "ESD protection design for RF circuits in CMOS technology with low-C implementation," in *Proc. International Semiconductor Technology Conference*, 2008, pp. 70-75.

[4] M.-D. Ker, **Chun-Yu Lin**, and G.-X. Meng, "ESD protection design for fully

integrated CMOS RF power amplifiers with waffle-structured SCR," in *Proc. IEEE International Symposium on Circuits and Systems*, 2008, pp. 1292-1295.

[5] **Chun-Yu Lin** and M.-D. Ker, "Optimization on SCR device with low capacitance for on-chip ESD protection in UWB RF circuits," in *Proc. IEEE International Symposium on Physical and Failure Analysis of Integrated Circuits*, 2008, pp. 58-61.

[6] **Chun-Yu Lin** and M.-D. Ker, "Co-design strategy with low-C consideration for on-chip ESD protection in RF ICs," in *Proc. International PhD Student Workshop on SOC*, 2008.

[7] **Chun-Yu Lin** and M.-D. Ker, "Low-capacitance and low-loss bond pad design using LC-resonator structure in CMOS technology for RF and high-speed applications," in *Proc. International Conference on Solid State Devices and Materials*, 2009, *in press*.

(C) Local Conference Papers:

[1] Y.-W. Hsiao, **Chun-Yu Lin**, and M.-D. Ker, "Design and realization of ultra low-capacitance bond pad with inductive compensation for RF circuits in CMOS technology," in *Proc. VLSI Design/CAD Symposium*, 2007, pp. 1-4.

(D) Patents:

[1] M.-D. Ker, **Chun-Yu Lin**, and C.-T. Wang, "SCR layout to achieve low parasitic capacitance with high ESD robustness for RF applications," U.S. and R.O.C. patent pending.

[2] M.-D. Ker, **Chun-Yu Lin**, and C.-T. Wang, "Uniform turn-on design on multi-finger SCR," U.S. and R.O.C. patent pending.

[3] M.-D. Ker, **Chun-Yu Lin**, and F.-Y. Tsai, "ESD protection circuit with merged triggering mechanism," U.S. and R.O.C. patent pending.

[4] **Chun-Yu Lin**, M.-D. Ker, and F.-Y. Tsai, "High-voltage-tolerant power-rail ESD clamp circuits in low-voltage CMOS processes," U.S. and R.O.C. patent pending.

[5] M.-D. Ker, **Chun-Yu Lin**, and C.-T. Wang, "ESD protection design against CDM ESD events," U.S. and R.O.C. patent pending.

[6] M.-D. Ker and **Chun-Yu Lin**, "Inductor-triggered SCR with ultra low capacitance," U.S. and R.O.C. patent pending.