國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

應用於視網膜療程之植入式人工視網膜

與其電源控制電路

A CMOS IMPLANTABLE RETINAL CHIP WITH SOLAR CELL POWER SUPPLY CONTROL CIRCUIT FOR RETINA PROSTHESES

研 究 生 ： 萬謎

指導教授 ： 吳重雨 教授

林伯剛 醫師

中華民國九十七年四月

A CMOS IMPLANTABLE RETINAL CHIP WITH SOLAR CELL POWER SUPPLY CONTROL CIRCUIT FOR RETINA PROSTHESES

應用於視網膜療程之植入式人工視網膜與其電源控制電路

研 究 生： 萬諶　　Student : Chen Wan

指導教授： 吳重雨 教授　　Advisor Prof. Chung-Yu Wu

林伯剛 醫師　　Dr. Po-Kang Lin

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics
College of Electrical and Computer Engineering
National Chiao-Tung University
in Partial Fulfillment of the Requirements
for the Degree of Master
in
Electronics Engineering
April 2008
Hsin-Chu, Taiwan, Republic of China

中華民國九十七年四月

應用於視網膜療程之植入式人工視網膜與其電源控制電路

學生: 萬諶 指導教授: 吳重雨 教授

林伯剛 醫師

國立交通大學

電子工程學系 電子研究所碩士班

ABSTRACT (CHINESE)

本篇論文中描述一個應用於下視網膜療程中的人工矽視網膜晶片設計。包含光電池架構的設計、晶片時脈產生器的設計、基本像素的設計與電能控制系統的設計。在光電池供電系統中，我們提出新的光電池架構並將電路系統與光電池同時整合在CMOS積體電路晶片上的設計也經由許多相關的測試元件與設計改良驗證其使用特性。我們並且初步設計並實作由感光二極體陣列構成之視網膜晶片的體外生物實驗，成功的驗證視網膜晶片刺激視網膜細胞的生物反應。而晶片時脈系統經過設計、模擬、量測後驗證爲一超低功率時脈產生器，此振盪器可在**3.6mW/cm^2**的光照強度下產生**1.632KHz**的震盪其電路消耗功率僅爲**5.2nW**。此植入式人工視網膜晶片使用了由生物特性啓發而得的電能控制系統，所以在下視網膜療程中的電能使用效益上有所改善。在應用此分區供電的架構下，此晶片可以產生約三倍的有效輸出電流已提供視網膜細胞所需要的電性刺激。此晶片在**3.6mW/cm^2**的光照強度下可以得到約略**844nA**的電流輸出、在**5.06mW/cm^2**的光照強度下可以得到約略**1.72μA**的電流輸出。在台灣積體電路製造股份有限公司與國家晶片系統中心的幫助下，此視網膜晶片將以**0.18**微米製程實現。基於上述特性，此光電池架構、視網膜晶片與電源控制系統對下視網膜療程中的人工矽視網膜晶片設計上有相當程度的貢獻。

A CMOS IMPLANTABLE RETINAL CHIP WITH SOLAR CELL POWER SUPPLY CONTROL CIRCUIT FOR RETINA PROSTHESES

Student: Chen Wan Advisor: Prof. Chun-Yu Wu
Dr. Po-Kang Lin
Department of Electronics Engineering & Institute of Electronics
National Chiao-Tung University

ABSTRACT (ENGLISH)

In this thesis, a retinal chip has been designed, analyzed, and fabricated to improve the power efficiency of the sub-retinal prostheses. The preliminary in vitro experiment of the silicon retina chip which composed of micro photodiode array has also been designed and verified. The silicon retina with MPA can successfully trigger the retina cell and the electrical-response is similar to the light-response in retina cell. The feasibility of on-chip solar cell supply system which integrated with circuit system in CMOS technology has been verified in the work. An ultra-low power clock generator is also designed and verified in this work. This clock generator can generate a clock signal with 1.632KHz under 3.6mW/cm^2 incident light intensity with only 5.2nW power consumption. A three times output stimulating current is achieved by taking advantage of the bio-inspired divisional power supply architecture. The stimulating output current is approximately 844nA under the illumination of 3.6mW/cm^2 light intensity and 1.72μA under the illumination of 5.06mW/cm^2 light intensity. The retinal chip fabricated with a standard 0.18μm tsmc CMOS process demonstrate good mimic of electrical behavior of human retina with low-power consumption. Because of its characteristic, the proposed power management system could be considered as one of the highly integrated solutions for the sub-retinal implant chips.

ACKNOWLEDGEMENTS

悠悠風城中，兩年的時光晃眼即過，彷彿回首我仍是剛進到竹湖畔的新鮮人。於此時此景即將要離開交通大學，心中實有萬分不捨與傷感。在這裡，我首先要感謝吳重雨老師從我還是大學時到此時此刻所給予我循序漸進的教誨，使我得以獲得許多積體電路設計的專業知識，更在此過程中學習到面對壓力與挑戰困難的精神，解決問題的方法。另外也要特別感謝林伯剛醫師在醫學領域與焦傳金老師在細胞電生理領域的指導與協助，讓這份跨領域的研究能夠順利完成。

在這段求學的過程中，奈米晶片與系統實驗室的給予了我完善的硬體及軟體資源，讓我能夠順利的完成學業，感謝學長姐們努力經營實驗室，讓實驗室如同我第二個家。更感謝實驗室學長姐，林俐如，楊文嘉，王文傑，陳勝豪，虞繼堯，陳旻珓，黃祖德，蔡夙勇，王資閔，羅怡凱，松諭、巧玲、黃董、宗裕、188、Taka、Hakko、野獸、神童、維德、國忠以及順哥等的細心指導；感謝實驗室同儕們的陪伴，讓我這段實驗室的歲月過的不僅充實也很溫馨有趣。另外也感謝及助理卓慧貞小姐與李清音小姐給予我在研究上的資源及行政上的幫助，讓我完成學業。

接著要感謝的是一起打拼的同學們，蒙國軒、吳國維、宅帥、小帆、紹岐、世範、帥哥邦、北鴨、塔哥、胖哥、歐陽、區威、小恩恩、建名、科科、筱妘。大家一起複習歷史，努力修課、熬夜趕工，出遊玩樂，讓我的碩士生活充滿歡樂；互相扶持，加油打氣讓我能充電再繼續努力。謝謝你們一直以來的陪伴與關懷。

最後我要致上萬分的感謝給予我的父親 萬昭明先生，以及我的母親 劉意君女士，由於他們一直以來的關心、支持與無微不至的照顧，並細心的栽培我讀書，進而讓我擁有了今天的成就。最後祝福我的師長、家人、朋友及學弟妹們事事順心、身體健康。我在撰寫的過程中，雖力求嚴謹，然誤謬之處，在所難免，尚祈各位讀者賜予寶貴意見，使本論文能更加完善。

萬謎

誌於 風城交大

九十七年 初春

CONTENTS

TABLE CAPTIONS

CHAPTER 3

CHAPTER 4

FIGURE CAPTIONS

CHAPTER 1

CHAPTER 2

CHAPTER 3

CHAPTER 4

CHAPTER 1 Introduction

1.1 BACKGROUND

Vision is one of the most important sensory organs and thus losing vision can bring one endless torments. Currently, over 10,000,000 people worldwide are blind because of photoreceptor loss or other cells loss in the retina [1]. Although medicine and ophthalmology today is well developed, some of the retinal degenerative diseases cannot be treated yet, such as retinitis pigmentosa (RP) and advanced age-related macular degeneration (AMD). Retinitis Pigmentosa has an incidence of 1 in 4000 live births, whereas 200,000 eyes are blinded each year by age-related macular degeneration. Thus, to restore vision with artificial retinal prosthesis draws considerable attention [2].On the other hand, the operation underlying early visual processing has been studied for many years. A large number of well-studied mathematical algorithms for the early visual processing have been proposed [3]-[21].

The vertebrate retina is a tiny sheet of neural tissue that locates at the back of the vertebrate eye chamber as shown in Fig. 1.1. It can perform two functions. Firstly, the photoreceptor is able to transducer the information of the optical image into neural signals. Secondly, the neural circuitry is able to abstract certain features of the visual world form the large number of photoreceptor signals and pass this information on to the brain via the optic nerve fibers.

All the retinal prostheses are based on a hypothesis that light perception can be elicited by electrical stimulations of neuronal tissues such as bipolar and/or ganglion cells of a retina. Fortunately the hypothesis has been verified via animal and human subject [2]. Critical question relating to the hypothesis include how many stimulations are required, and what are the electrical stimulus parameters (amplitude, duration, waveform, frequency) needed for each pixel in order to meet the safety and effectiveness constrains of the prosthesis. Answers to these questions greatly facilitate the optimal design, fabrication, fixation, and integration of and electrode array in a retinal prosthesis system and the power requirement of the prosthesis.

Based on the well development of silicon retina circuits and the verified hypothesis that light perception can be elicited by electrical stimulation of neural tissues, the artificial retinal prosthesis by implantable circuits can be developed and used to restore the vision of the blindness. There are two approaches for retinal implants, namely epi-retinal and sub-retinal implants. In epi-retinal prosthesis, the prosthetic device is attached to the inner retinal surface so that the electrical signal directly stimulates the inner retina first. On the other hand, sub-retinal prosthesis places the implant in a space between neurosensory retinal and retinal pigment epithelium so that the electrical signal stimulates the outer retina first. The main advantage of the epi-retinal approach is to keep most of the electronics off the retinal space, in the vitreous cavity which greatly helps in dissipating the heat generated by the electronics. While the sub-retinal implant has the advantage of placing the electrodes closer to the bipolar

cells and thus has a potential of reducing the stimulus threshold. Many individual research teams have now published an extensive body of reports detailing the progress achieved with both these approaches. (Epi-retinal implants:[22-29];sub-retinal implants:[30-35]).

1.2 REVIEW ON THE RETINAL PROSTHESES

1.2.1 Epi-Retinal Prosthesis

The idea of epi-retinal prosthesis resembles that of the cochlear implant, which converts sound into electrical impulses to stimulate the auditory nerve in the inner ear. Fig.1.2 shows a conceptual prosthetic system. The epi-retinal implant acquires images from a camera positioned outside the eye. These images are preprocessed in a computer and stimulation by the energy source; they can be received through the epi-retinal implant and understood by the brain following transmission via the optic nerve. In principle, therefore, the epi-retinal implant model represents a contact structure for reading preprocessed visual information into the human optical system. Experience to date has indicated that fixing such structures to the retinal surface is a major problem. Nevertheless, suitable fixation techniques have been successfully developed in the interim and this state of affairs has thus been improved. As a result, the fixation of epi-retinal implants can now be achieved in a manner that ensures long-term biocompatibility and has few complications [36]. Similar results have also been reported by a team in USA following implantation of stimulation arrays epi-retinally in four dogs [37]. Long-term biocompatibility in these studies was verified using visual evoked potentials (VEP) or Electroretinography (ERG).

Although long-term biocompatibility was consistently demonstrated initially only for electrically inactive implants, a functional chronic epi-retinal prosthesis has now been implanted for the first time by Humayun [38]. In the first 10 weeks after the implantation, the completely blind test subject was able to see perception light (phosphenes) after stimulation of an electrode array (4x4 pixels) interfacing with the retina. The subject was thus able to detect the presence or absence of ambient light or motion, and to recognize simple shapes. The stimulation energies used were below those expected on basis of acute studies in humans. This has positive implications for the development and success of epi-retinal implants [39]. Reliable and reproducible responses to retinal electro-stimulation have therefore been obtained with the epi-retinal implant in studies in humans. Because only small numbers of electrodes have so far been used, it is planned that their number will be markedly increased for the next generation of epi-retinal implants in order to offer more complex stimulation patterns so that the capabilities of these visual prostheses can be assessed [39].

The epi-retinal prosthesis usually possesses a common framework: an external signal-processing unit for biological sense information (sound, image, etc), a bi-directional

telemetry unit, an internal signal processing unit, a stimulus generator/driver, and electrode array for interfacing to tissue or nerves. Fig. 1.3 shows the typically functional implantable microsystem [40]. A miniature video camera supplies visual information to an image processing unit. The processor collects, compresses, and formats the data for the implanted stimulator. The processor produces a serial data stream and clock which are encoded. The encoded signal is used to modulate an amplifier that drives the primary coil of the inductively coupled link. The above components are mounted on glasses to be worn by the patient. Typically implanted in the eyeball are the secondary coil, power and data recovery components, stimulus circuits, and the electrode array. The signal produced by the secondary coil is rectified and filtered to produce a DC supply voltage for the implanted circuits.

One great concern of epi-retinal prosthesis is affixing the chip to the retina and protecting the chip. The harsh environment inside the eye could cause the chip to disintegrate or malfunction. Another great challenge is the huge heat generated by the antennal system. The great heat may damage the normal retinal cells and result in worse vision.

1.2.2 Sub-Retinal Prosthesis

As long ago as 1956, Tassiker in Australia described in a patent a retinal prosthesis that consisted of a light-sensitive selenium cell placed behind the retina of a blind patient [41]; this transiently restored the patient's ability to perceive light. In the ensuing period, however, greater successes were reported with cortical implants [42], although spatial resolution and the fading of excitation were still unresolved problems. These techniques have subsequently been taken to their most sophisticated form by Normann who has developed an intracortical array comprising 100 individual "needle" electrodes [43].

By the early 1990s the efforts of many research teams finally came to concentrate on the retina. In particular, more sophisticated developments in the field of microelectronics and the successful use of the cochlear implant to replace lost auditory function suggested that the possible development of a functional retinal implant was within reach. After these early prototypes had been developed and implanted, experimental animal work was performed to define the electrical stimulation parameters for the retina. In this context the capacity of the human eye to adapt to large brightness and contrast variances plays a decisive role.

Before thoughts could turn to a corresponding series of experiments in humans, the appropriate surgical techniques for the reliable insertion and attachment of these implants first had to be developed. As a rule this work was performed in animal models because these are apparently suitable for answering the specific questions raised in this context. In addition, it was of crucial importance first to establish which patients appeared best suited to receive prosthesis of this type.

Currently, the research conducted by teams in Germany, the USA and Japan into epi-retinal and sub-retinal implants has reached the stage where clinical trials can now be

performed with the devices that have been developed.

The fundamental concept of the Sub-retinal approach is that electrical charge generated by the micro-photodiode array (MPA) in response to a light stimulus may be used to artificially alter the membrane potential of neurons in the remaining retinal layers in a manner to produce formed images [44]. The MPA functions in solar cell mode, that is, it operates without power supply. Fig. 1.4 shows the sub-retinal implant [45]. This approach would theoretically allow the remaining intact retinal circuits of the inner retina to process this signal in a near-normal fashion and transmit this signal to the brain. In addition, the sampling density of a sub-retinal device could be designed to match that of the remaining photoreceptor or bipolar cell matrix, thereby providing a potentially high-resolution input to the retina.

Although the current sub-retinal implants have less circuit complexity, they suffer from the problem that the pn junction diode in solar cell mode cannot provide enough photovoltaic power supply to the retinal chip. Therefore, it is important to improve the efficiency of the pn junction diode in solar cell mode in sub-retinal implants.

1.3 REVIEW ON POWER SUPPLY ISSUE IN ARTIFICIAL RETINA PROSTHESES

It is medically infeasible to have permanent wired connections pass through the eyeball wall because the wire would do quick damage to the eyes. Laying the wires and connecting the nodes entails extensive incisions, a potentially hazardous surgery. Therefore, the power issue is a great challenge for implanted retinal circuit.

Owing to lower stimulus level, sub-retinal chip usually consists of photodiode and electrode array which provides stimulus of low energy [46]. Thus sub-retinal chip requires no power supply. However, this kind of artificial retinal prosthesis can only replace the photoreceptor, a cell converting light into electrical signal. If more than the damage of photoreceptor causes blindness, the typical sub-retinal chip cannot restore the vision.

A common way to provide the implanted retinal circuit power is utilization of RF telemetry [2], [40]. This kind of implanted device consists of an extraocular and intraocular unit. The implantable component receiver power and a data signal via a telemetric inductive link between the two units. The extraocular unit includes a video camera and video processing board, a telemetry protocol encoder chip, and an RF amplifier and primary coil. The intraocular unit consists of a secondary coil, a rectifier and regulator, a retinal chip with a telemetry protocol decoder, a stimulus signal generator, and an electrode array. The major difficulty for this telemetry technique is tissue heating associated with electromagnetic power deposition in the tissues and power dissipation in the microchip collectively.

The proposed method to supply power to implanted retinal chip is using solar cells. When the circuit is designed as low-power circuit, solar cells can provides enough energy to the implanted circuit. Two advantages of solar cell are described below. Firstly, when there is no light and therefore human cannot see and the solar cells supply no power to the implanted

circuit. It clearly reduces some power dissipation and tissue heating. Secondly, solar cell is compatible with intraocular unit. Therefore, there is no equipments need to carry with the blind.

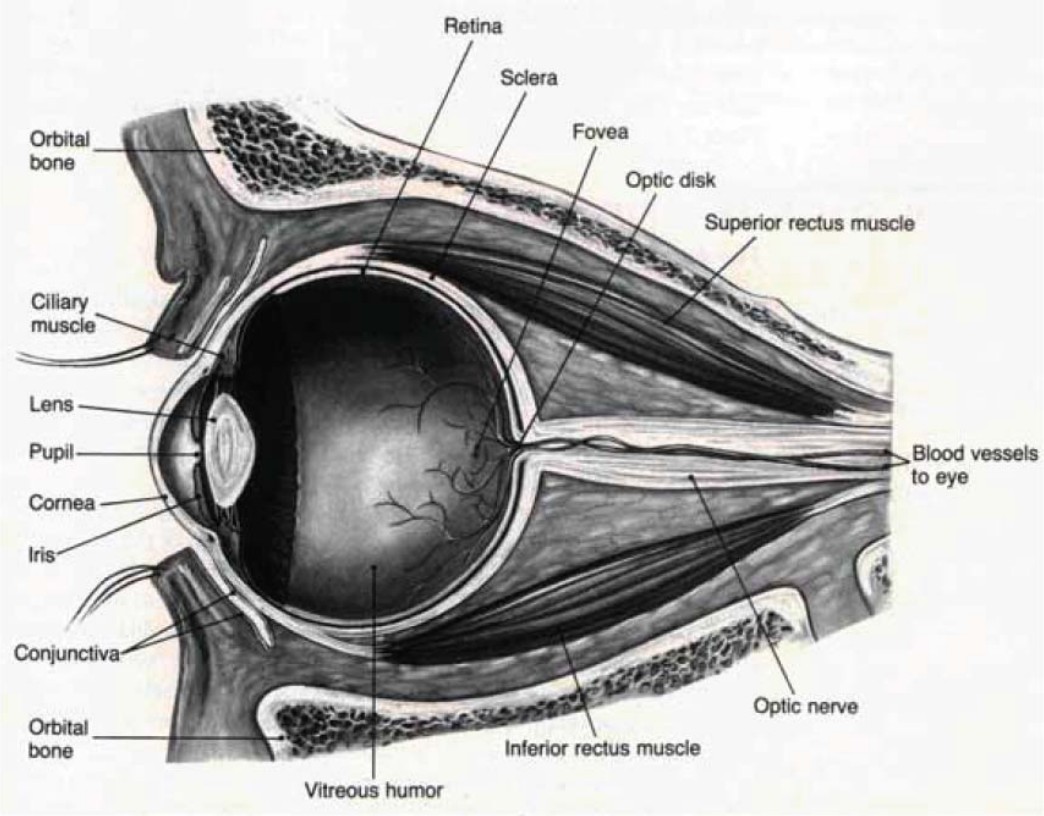


Figure. 1.1 The Human Eye. *Reprinted from "Foundations of Physiological Psychology," by Neil R. Carlson, 1988, p.134.*

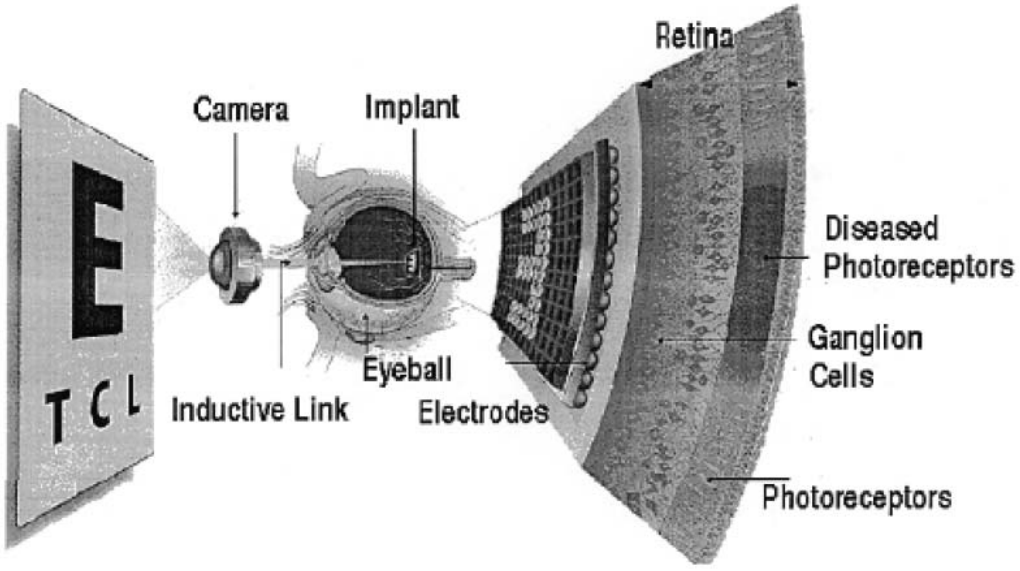


Figure. 1.2 A Conceptual Epi-Retinal Prosthetic System. *Reprinted form "A Neuro-Stimulus Chip with Telemetry Unit for Retinal Prosthetic Device," by Wentai Liu, and etc, 2000.*

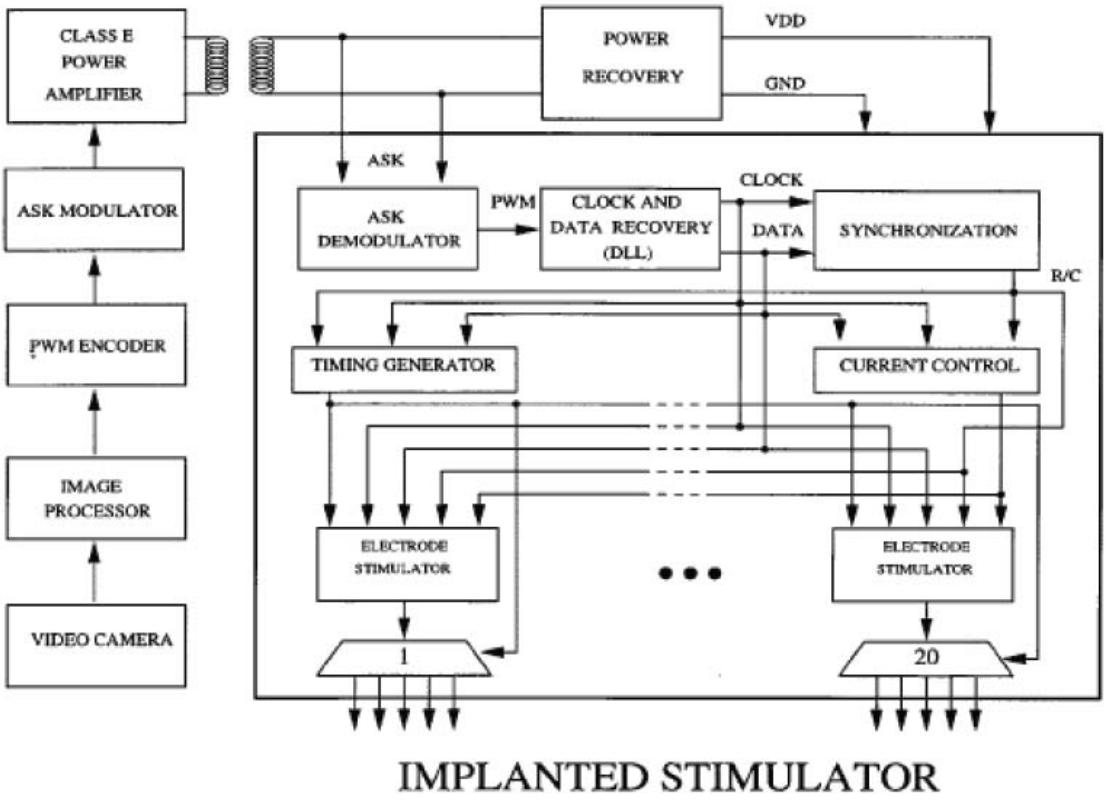


Figure. 1.3. The Typically Functional Implantable Epi-Retinal Microsystem. *Reptinted from "A Neuro-Stimulus Chip with Telemetry Unit for Retinal Prosthesis Device" by Wentai Liu, and etc., 2000.*

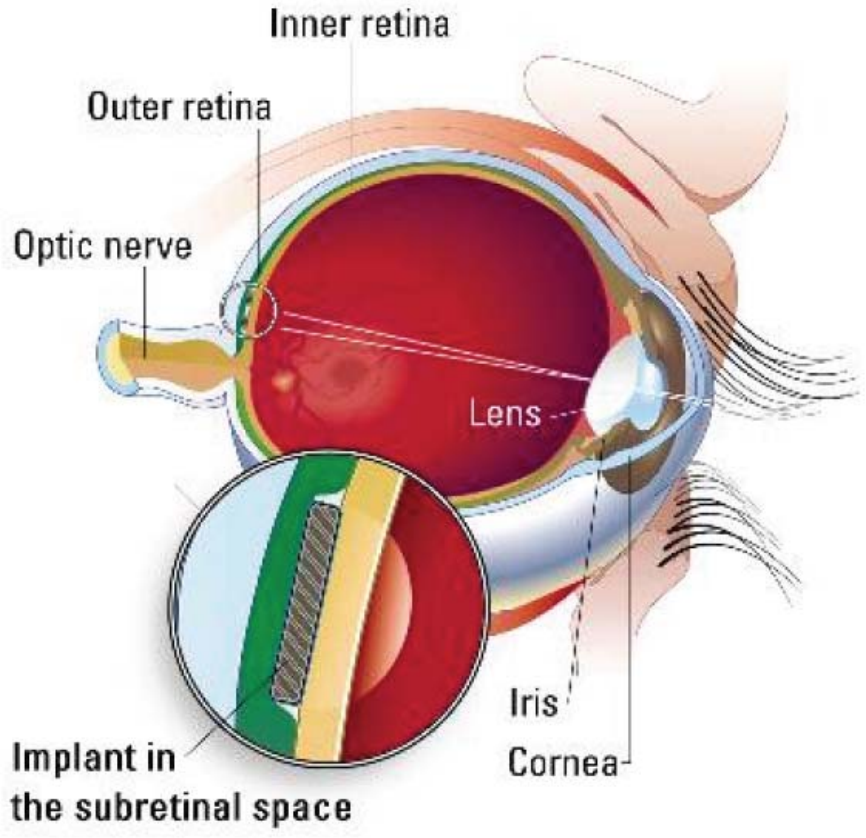


Figure. 1.4. The Sub-Retinal Implant. Reprinted from the internet: "http://www.optobionics.com/theeye.htm" by Mike Zang.

1.4 MOTIVATIONS

1.4.1 Solar cell structure.

In modern CMOS imager design, the silicon-based phototransduction has been studied in several different aspects. We will show the relation between layout structure and phototransduction efficiency in this section. One of the important sensors for digital imaging is PN junction photodiode because it is easy to fabricate in CMOS technology, which is inexpensive and widely available. When the light irradiates a diode's junction, electron-hole pairs are generated due to the light illumination. Inside the depletion region, Electrons and holes generated will be swept into the adjacent N and P regions, respectively, due to the electric field across the junction. In addition, electrons and holes generated in the adjacent P and N regions may diffuse into the depletion region and be swept into the other side. Photogenerated carriers swept into the across junction layer may be detected either as photocurrent or as photovoltage. The photodiode can be operated in two basic modes: photoconductive mode and photovoltaic mode. The equivalent circuit for both modes of operation is shown in Fig. N, where I_{ph} represents photocurrent, D_0 is a diode, R_s is the series resistance, R_j is the load resistance, and V is the reverse bias voltage. If the incident light power is P_{ph}, the photocurrent I_{ph} corresponding to the current source in Fig. 1.5 is

$$I_{ph} = \frac{q\eta P_{ph}}{\hbar\omega}$$

where η is the quantum efficiency if the photodiode and ω is the angular frequency of the incident light. In short-circuit photoconductive mode, the voltage across the photodiode is zero and the external current is I_{ph}. The photoconductive mode is also known as photo-sensing mode which is widely applied in CMOS imager design. In photovoltaic mode, the carriers swept through the depletion layer build up a potential across the PN junction. The photovoltaic mode is also known as solar cell power supply mode which is widely used in on-chip solar power supply system. In this work, we will use these two different modes to build up a CMOS imager and retina stimulator with on-chip solar power supply system. [48]

There are several different layout methodologies of the CMOS photodiode. The N+/P-substrate photodiode, which is shown in Fig .1.6, is the most popular layout structure in APS (active pixel sensor) imager design. But the photodiode structure above can't be applied in solar cell power supply system because the p-substrate in CMOS circuit must be connected to ground. Thus the N+/P-substrate structure can only provide negative voltage level and the p-substrate can't be connected as the VDD of the CMOS circuit because the NMOS in the circuit will operate under high body voltage condition that the V_t (threshold voltage) will increase. In order to provide a positive voltage level to the circuit, the P+/N-well photodiode structure is proposed as shown in Fig. 1.7. The solar cell with this structure can provide the positive voltage level as an on-chip power supply.

There are two solar cells connected in series to provide the voltage power supply in the

beginning of the solar cell power supply design. The retinal chip is powered by on-chip solar cell which can be measured individually. The measurement environment is shown in Fig. 1.8. The measurement result is shown in Fig. 1.9. The characteristic I-V curve of the solar cells, which are connected in series, has a strange curve within 0V to 1V voltage-sweep range. In compassion with ideal curve, the measured curve seems to be a compound of ideal solar cell I-V curve and ideal solar BJT I-V curve. The top view and cross-section view of the solar cell supply system is shown in Fig. 1.10. We suppose there is a parasitic BJT in the solar cell power supply system as shown in Fig. 1.11. Due to the p-substrate is connected to ground; the junction between n-well and p-substrate is under reverse bias and the junction between p+ and n-well is foreword bias. Therefore the parasitic BJT is turn on and the I-V curve of the solar cell supply system is change to the I-V curve of the photo-BJT (parasitic BJT). With this parasitic structure, we create a new simulation model of the solar cell supply system as shown in Fig. 1.12. This model is based on experimental results of the solar cell supply system. The simulation result of the new solar cell supply system is shown in upper box of the Fig. 1.14. The comparison between the simulation result and the measurement result can verify the cause of the strange I-V curve of the solar cell supply system.

In addition, if there is only one solar cell to provide the on-chip power supply, the problem we face above still has in the parasitic effect. On the measuring of another testkey with same p+/n-well diode structure, the connection condition of p-substrate has tremendous influence on the efficiency of the solar cell. The testkey with same p+/n-well diode structure is surrounded by the n-well guard-ring and p-substrate guard-ring. The top view layout of this testkey is shown in Fig. 1.14. The measurement results of the single solar cell testkey above are shown in Fig. 1.15. Four different lines represent the different connection of the n-well and p-substrate individually. NW:O: the n-well is connected to VDD; NW:X: the n-well is floating. Psub:O: the p-substrate is connected to ground; Psub:X: the p-substrate is floating. As we can see in this figure, the connection of the n-well has strongly effect on the efficiency of the solar cell, but has no influence on the Voc of the solar cell, which is very important for a power supply. In another hand, the connection of the p-substrate has a great influence on both efficiency and Voc of the solar cell. First, the red dashed line and black solid line have shown the same characteristic which measured in above solar cell supply system. Therefore the problem of the p-substrate connection, which happened in solar cells connected in series, still can be found in this single solar cell testkey. The connection effect of the n-well is not usually seen but the p-substrate connection problem will happen in any NMOS in normal CMOS design. As a result, we propose several layout methodologies in next Chapter to prevent the problem of parasitic BJT.

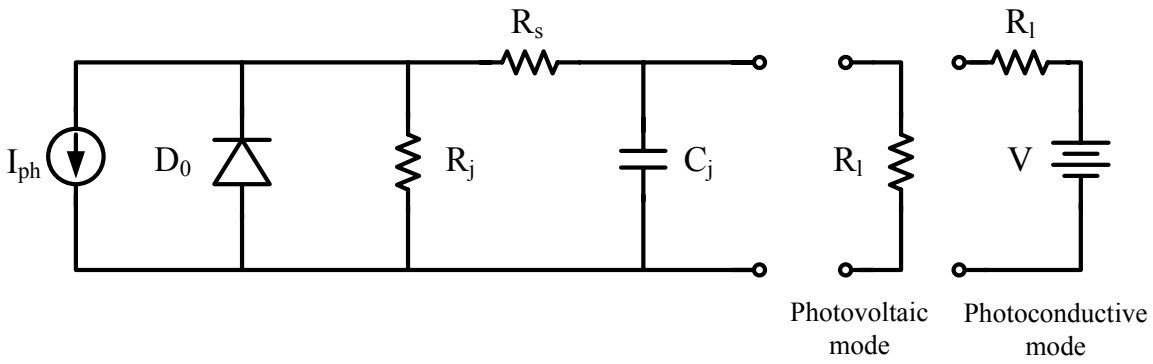


Figure 1.5. Equivalent circuit for a photodiode. Iph represents photocurrent, D0 is a diode, Rs is the series resistance, Rj is the load resistance, and V is the reverse bias voltage.

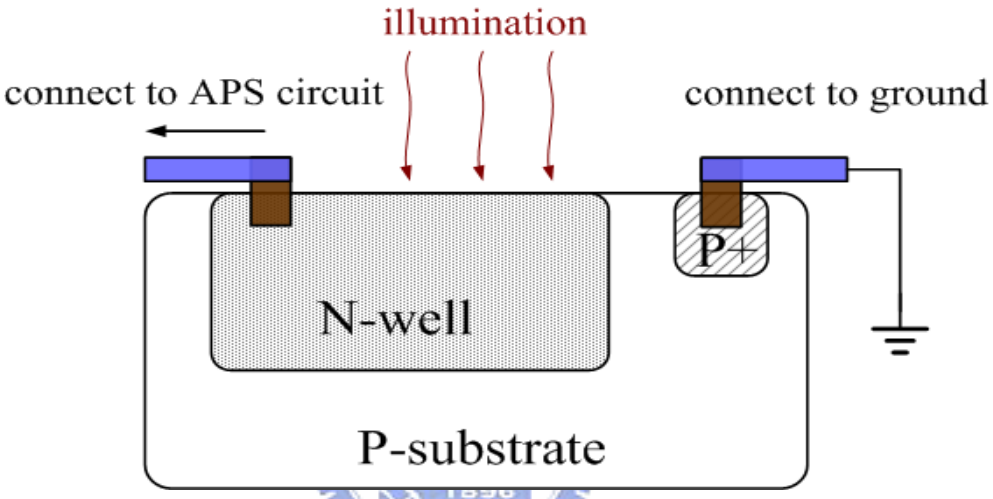


Figure 1.6 .the cross-section view of the n-well/p-substrate photodiode which is widely used in CMOS imager design.

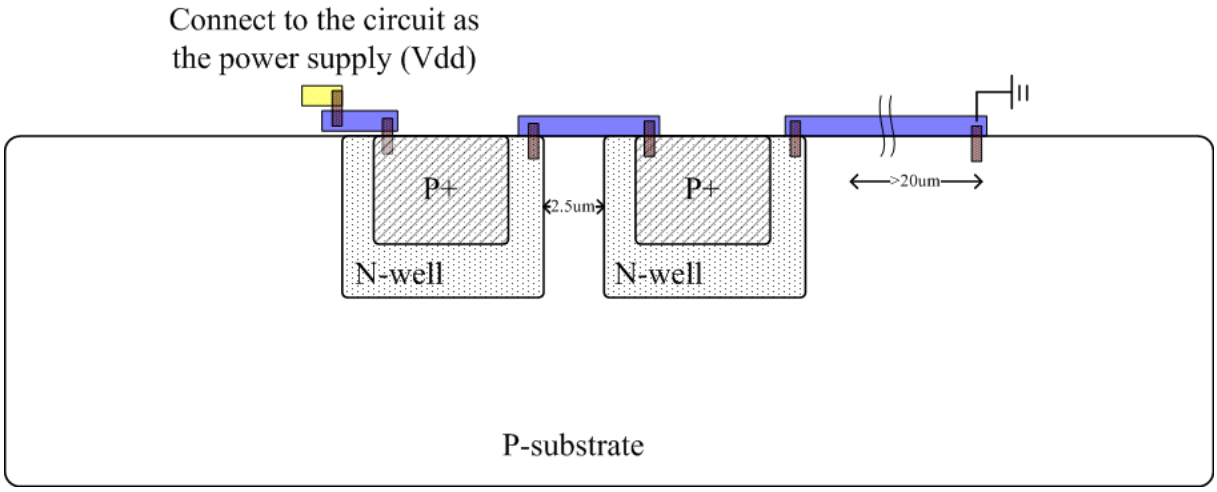


Figure 1.7. the solar cell power supply system with two solar cells in series which can provide sufficient positive voltage supply.

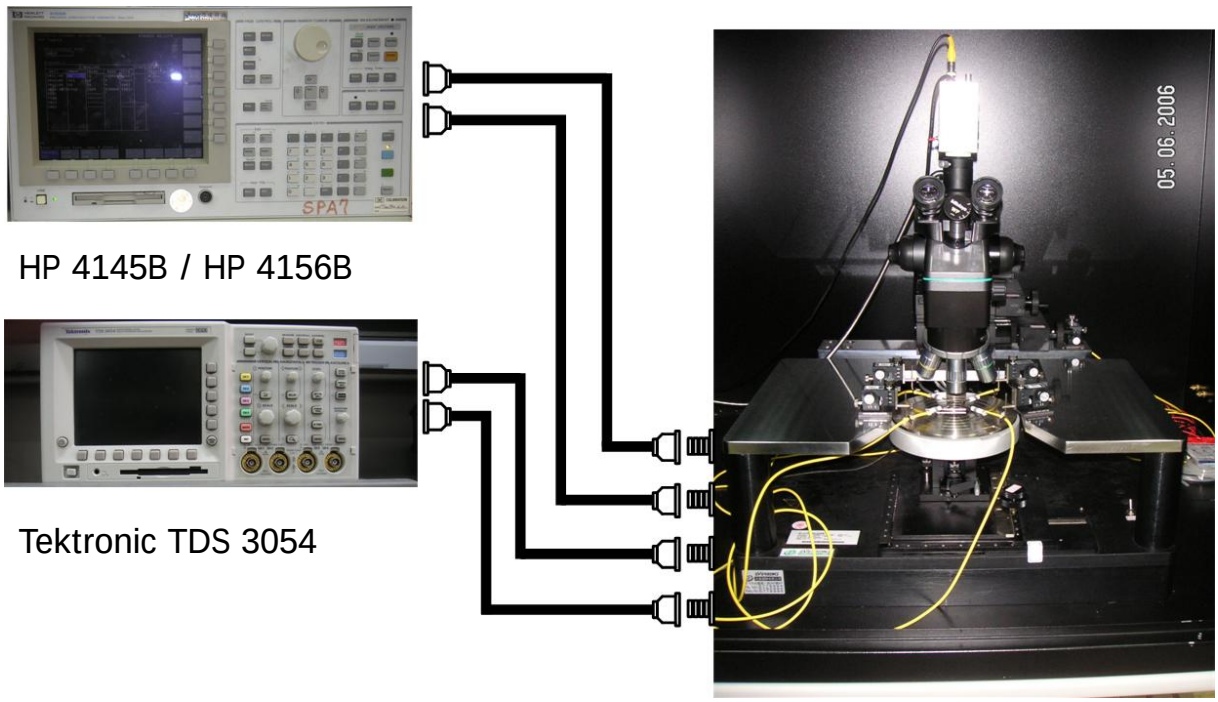


Figure 1.8. the measurement environment of the solar cell testkey and solar cell powr supply system. The right box is the probe station with four recording channel.

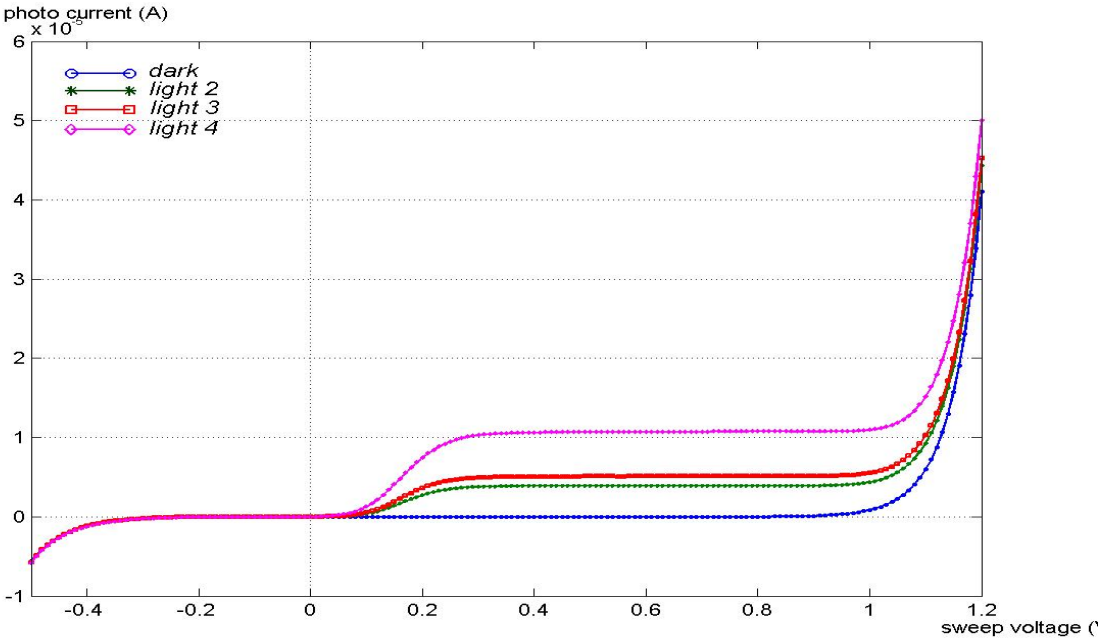


Figure 1.9. the measurement results of the solar cell power supply which has two solar cells connected in series. The curve light2 is under 400lux illumination, curve light3 is under 1000lux illumination, and light4 is under 1500lux illumination.

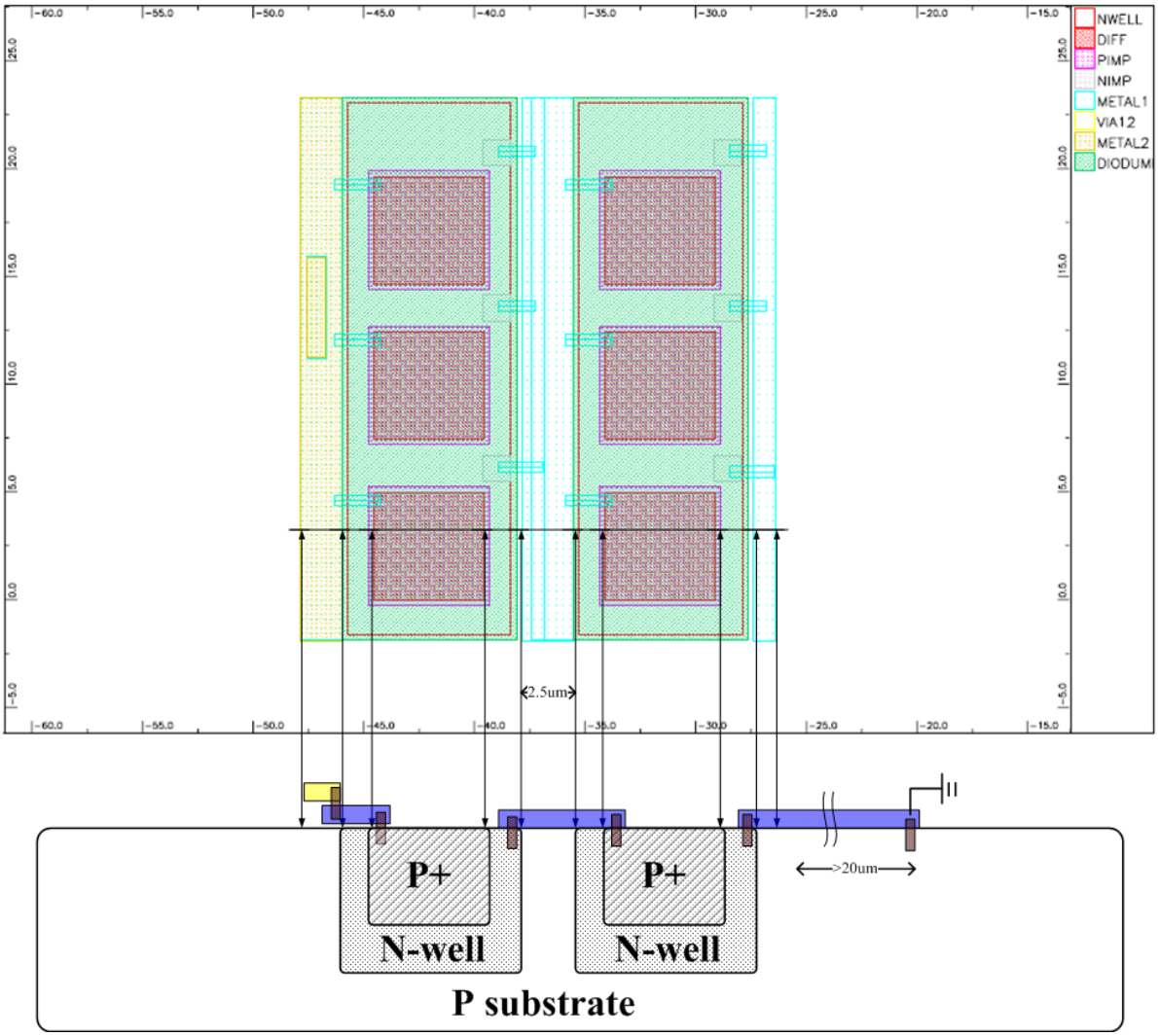


Figure 1.10. the top view and cross-section view of the solar cell power supply system. .

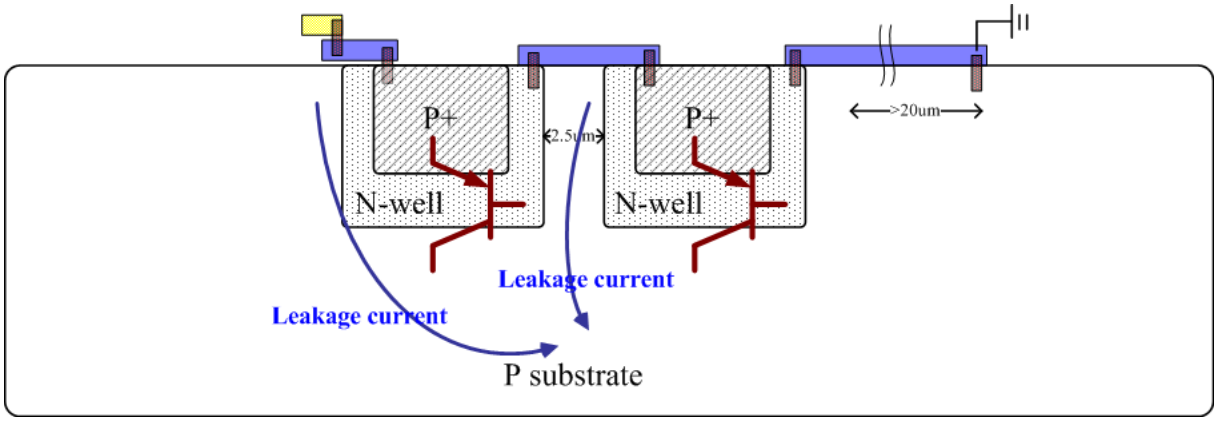


Figure 1.11. the parasitic BJT of the solar cell supply system. The leakage current through the BTJ result in the strange I-V curve we measured.

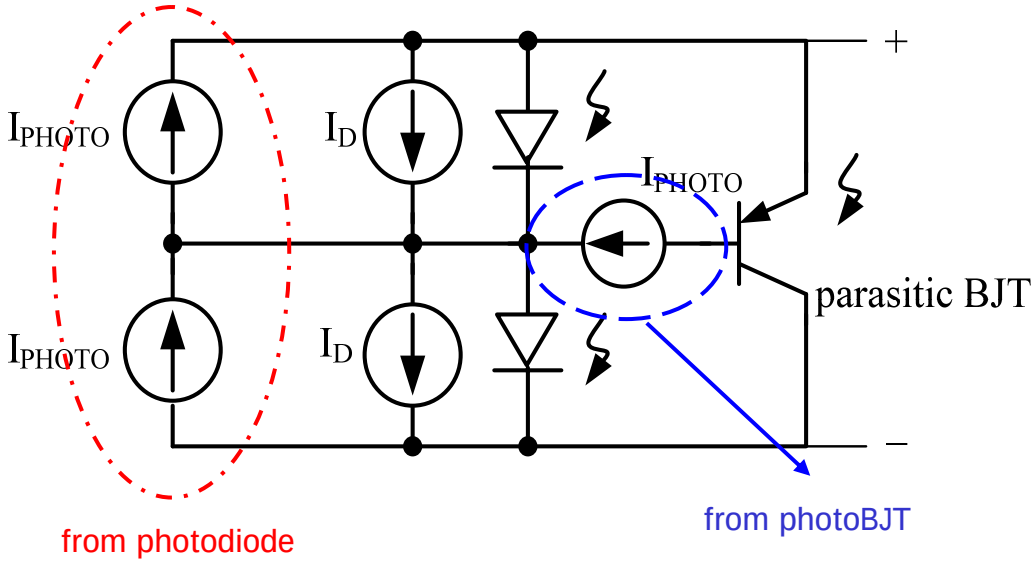


Figure 1.12. new simulation model of the solar cell supply system with parasitic BJT. both parasitic BJT and solar cell have phototransduction current. This model is based on experimental resluts of the solar cell supply system.

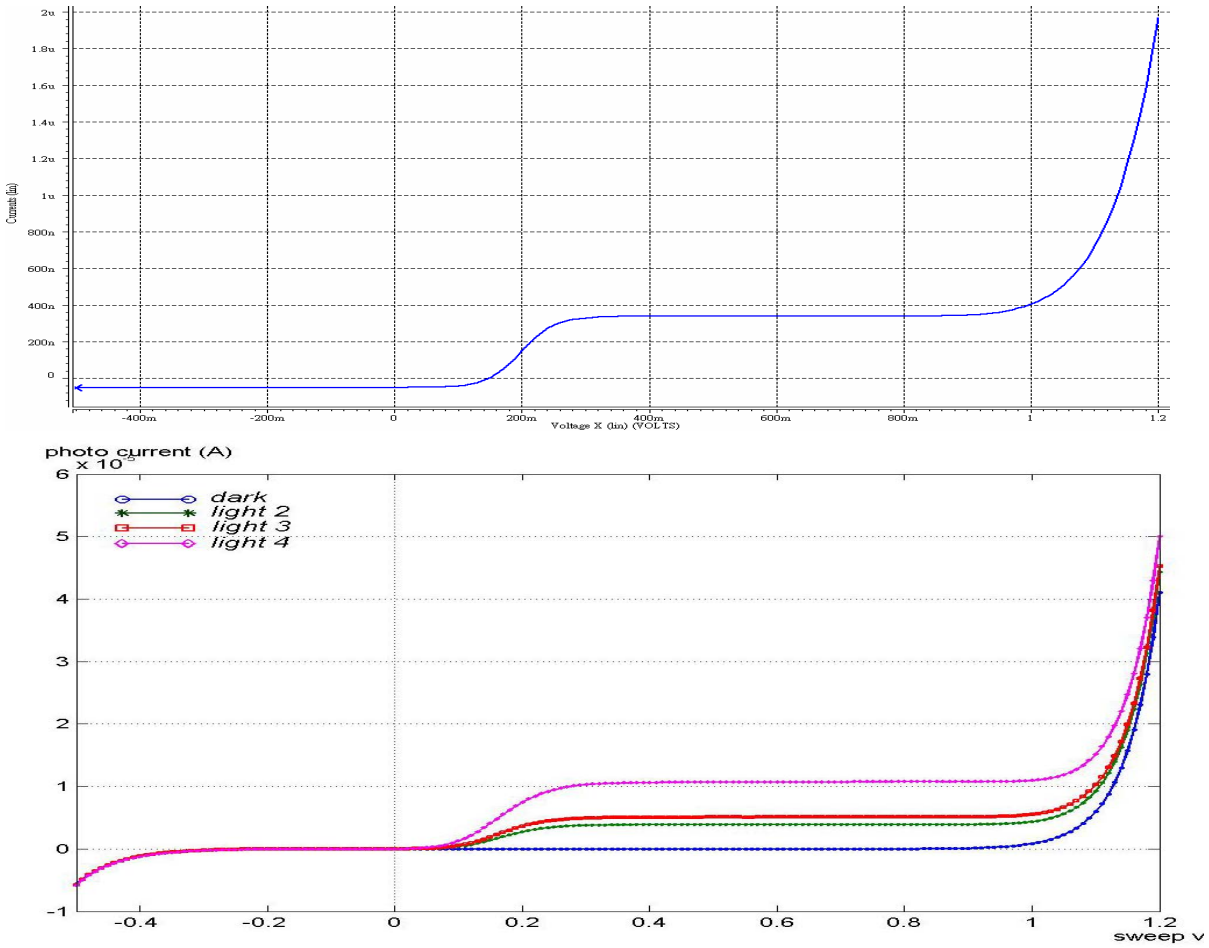


Figure 1.13. the comparsion between the simulation results and experimental results. Upper box: the simulation result of the new solar cell supply system. Lower box: the experimental results of the solar cell supply system.

Figure 1.14. the top view of the layout of the single solar cell test key.

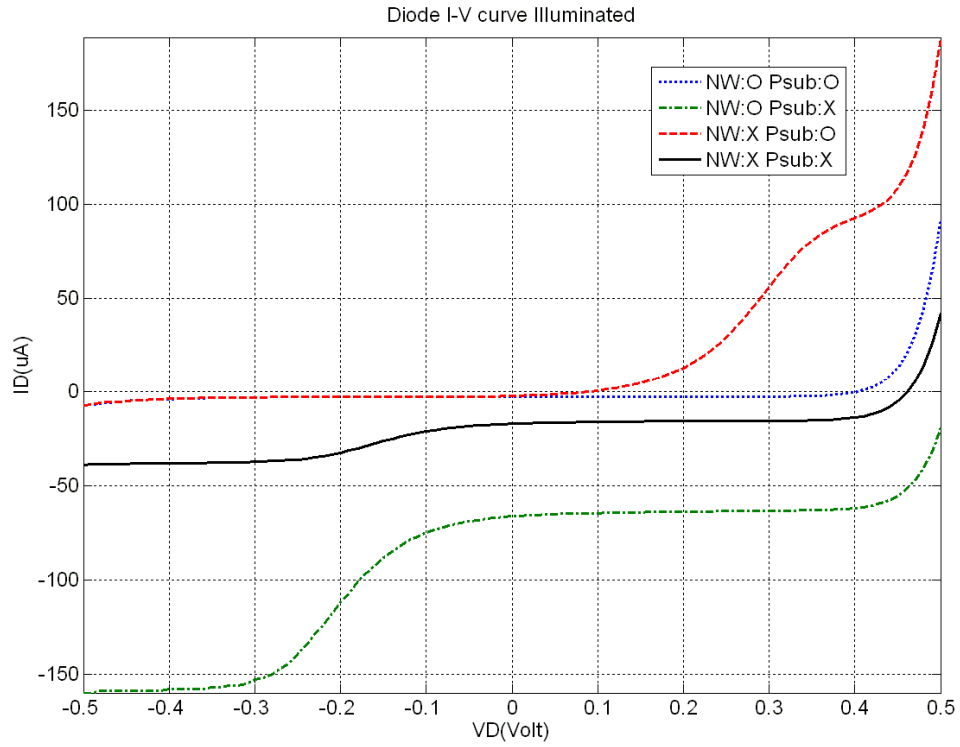


Figure 1.15. the measurement results of the single solar cell test key. Four different lines represent the different connection of the n-well and p-substrate individually. NW:O: the n-well is connected to VDD; NW:X: the n-well is floating. Psub:O: the p-substrate is connected to ground; Psub:X: the p-substrate is floating. As we can see in this figure, the connection of the n-well has strongly effect on the efficiency of the solar cell, but has no influence on the Voc of the solar cell, which is very important for a power supply. in another hand, the connection of the p-substrate has a great influence on both efficiency and Voc of the solar cell. Therefore the problem of the p-substrate connection, which happened in solar cells connected in series, still can be found in this single solar cell testkey.

1.4.2 Power issue

In CMOS solar cell power supply design, the photovoltaic efficiency is limited to the chip fabrication foundry and the total supplied power is in proportional to the layout area of the solar cells. Therefore the power supply design of the retinal chip is mainly focus on the power saving policy.

Persistence of vision is the phenomenon of the eye by which even nanoseconds of exposure to an image result in milliseconds of reaction (sight) from the retina to the opitic nerves. This is because persistence of vision depends on chemical transmission of nerve responses, and this biochemical hysteresis is much slower than the light transmission. A typical explanation of persistence of vision went something like this: when the human eye is presented with a rapid succession of slightly different images, there is a brief period during which each image, after its disappearance, persists upon the retina, allowing that image to blend smoothly with the next image. [47] Therefore the retinal chip needs not to stimulate the retinal cell continuously but stimulate the retinal cell with a more discrete method. As we know that the maximum frame rate which can be distinguished by human is about 60Hz, namely, we can stimulate the retinal cell every 16ms or less and the retina still consider the discrete stiulus as a continuous stimulus.

By applying the technique of divisional power supply architecture to exploit the characteristic mentioned above, an three times output current could be achieved. The details are in the followings. We divide the pixel array into four blocks whole outputs are controlled by four control signals generated by power control unit. The blocks will be activated in turn to send out their stimulating signals. The time interval between neighboring activation of the same block must be much smaller than biochemical hysteresis of the cell. Only one of the blocks is activated at the same time and the power from whole chip, which is supplied by solar cells, is provide to that block to increase the output stimulating current. In contrast to the conventional MPA design, the output power is much greater and the discrete stimulus won't cause any misinterpret in the retina but still provide continuous signals to the brain.

1.5 MAIN RESULTS

In this thesis, a retinal chip has been designed, analyzed, and fabricated to improve the power efficiency of the sub-retinal prostheses. The feasibility of on-chip solar cell supply system which integrated with circuit system in CMOS technology has been verified in the work. According to the experiment data, the preliminary in vitro experiment of the silicon retina chip which composed of micro photodiode array has been designed and verified. According to the experiment data, the silicon retina with MPA can successfully trigger the retina cell and the electrical-response is similar to the light-response in retina cell. A three times output stimulating current is achieved by taking advantage of the bio-inspired divisional power supply architecture. The stimulating output current is approximately 844nA under the illumination of 3.6mW/cm^2 light intensity and 1.72μA under the illumination of 5.06mW/cm^2 light intensity. The retinal chip fabricated with a standard 0.18μm tsmc CMOS process demonstrate good mimic of electrical behavior of human retina with low-power consumption.

CHAPTER 2 Solar Cell Design in CMOS Technology

2.1 THE NOVEL STRUCTURE OF SOLAR CELL

The new layout methodologies for the solar cell supply system are proposed in this section to solve the problem we faced in above section. We propose three different layout methodologies for the new solar cell supply system. First, we found that some of the solar cells in previous testkey can still have proper characteristic as a power supply. In comparison with other solar cells and other on-chip solar cell power supply system, the distance between p-substrate pick-up and solar cell seems to be a key factor to this problem. The p+/n-well solar cell can maintain the same characteristic while the distance between p-substrate pick-up and solar cell is greater than 50μm. Therefore, we can use same p+/n-well diode structure to build up an on-chip solar cell supply system. But in order to maintain the characteristic of the solar cells, the required layout area is increasing dramatically due to the distance between p-substrate pick-up and solar cells. We propose other solar cell structures to provide the solar cell power supply. In order to keep the p-substrate floating to prevent the leakage problem in p+/n-well solar cell, we use deep-n-well to isolate the solar cells or NMOS in the circuit as shown in Fig. 2.1. One of the layout structures is shown in top block of Fig. 2.1: the NMOS is isolated by the deep-n-well and the p-substrate pick-up is connected to p-well within deep-n-well. Therefore the p+/n-well solar cell can maintain the characteristic with the floating p-substrate. Another layout structure is shown in bottom block of Fig.2.1 the solar cell is isolated by the deep-n-well and the deep-n-well is floating that the solar cell within the deep-n-well can still maintain the power supply characteristic. The layout of the NMOS in the circuit is still the same as conventional design. The layout view of these two different structures is also shown in Fig. 2.2

In the retinal chip design, the amount of the solar cells is many times more than the NMOS in the circuit. The solar cells embedded in deep-n-well have to occupy large layout area due to the layout design rules and the total amount of the solar cells. In another hand, the NMOS embedded also have to occupy large layout area, but the amount of the NMOS is much less than solar cell. Therefore considering the layout area efficiency of the retinal chip the layout methodology in the top block of the Fig. 2.1 is chosen to achieve the on-chip solar power supply system for the retinal chip.

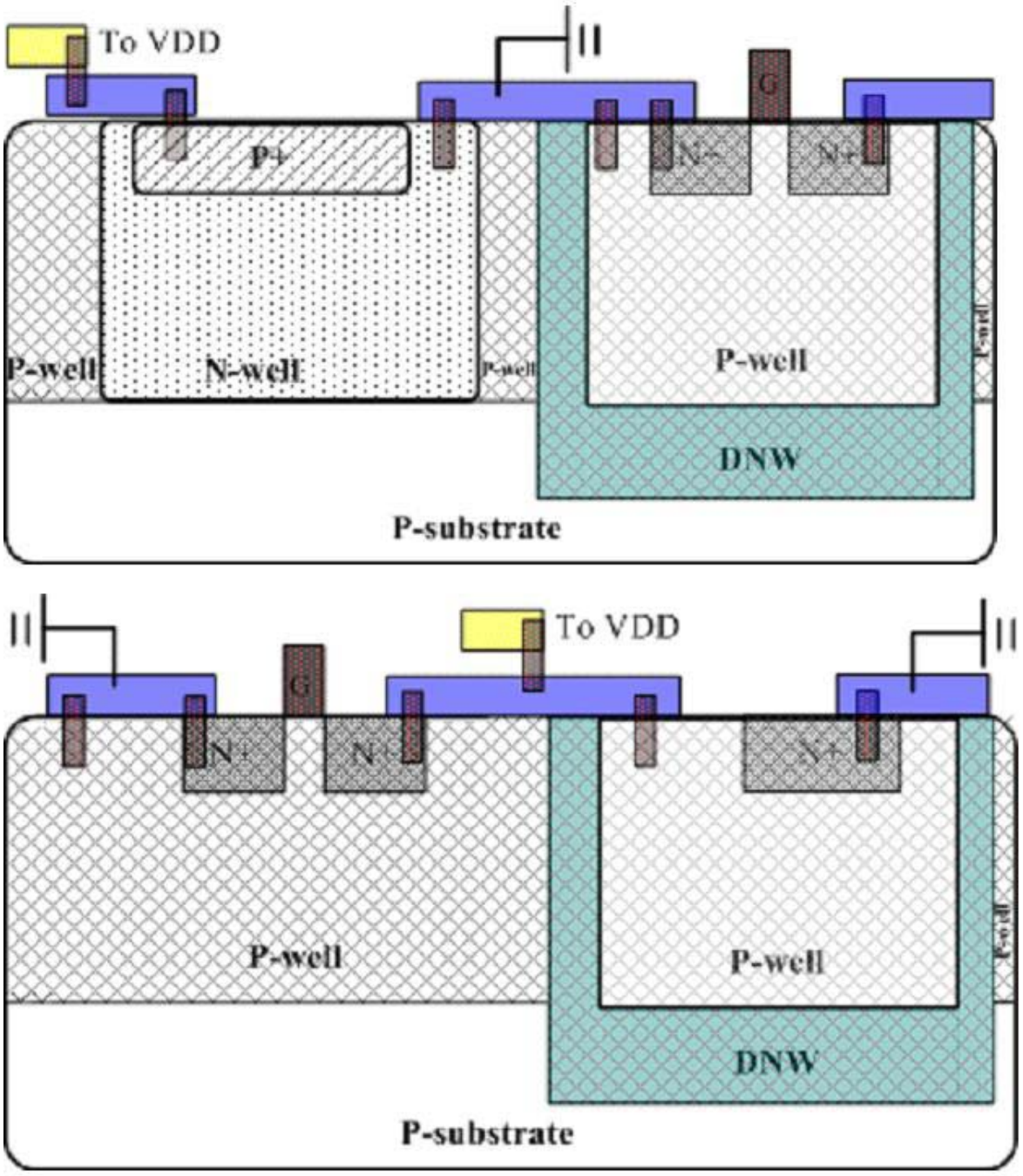


Figure 2.1. the cross-section view of two different layout methodology. Top: the NMOS is isolated by the deep-n-well and the p-substrate pick-up is connected to p-well within deep-n-well. Therefore the p+/n-well solar cell can maintain the characteristic with the floating p-substrate. Bottom: the solar cell is isolated by the deep-n-well and the deep-n-well is floating that the solar cell within the deep-n-well can still maintain the power supply characteristic. The layout of the NMOS in the circuit is still the same as conventional design.

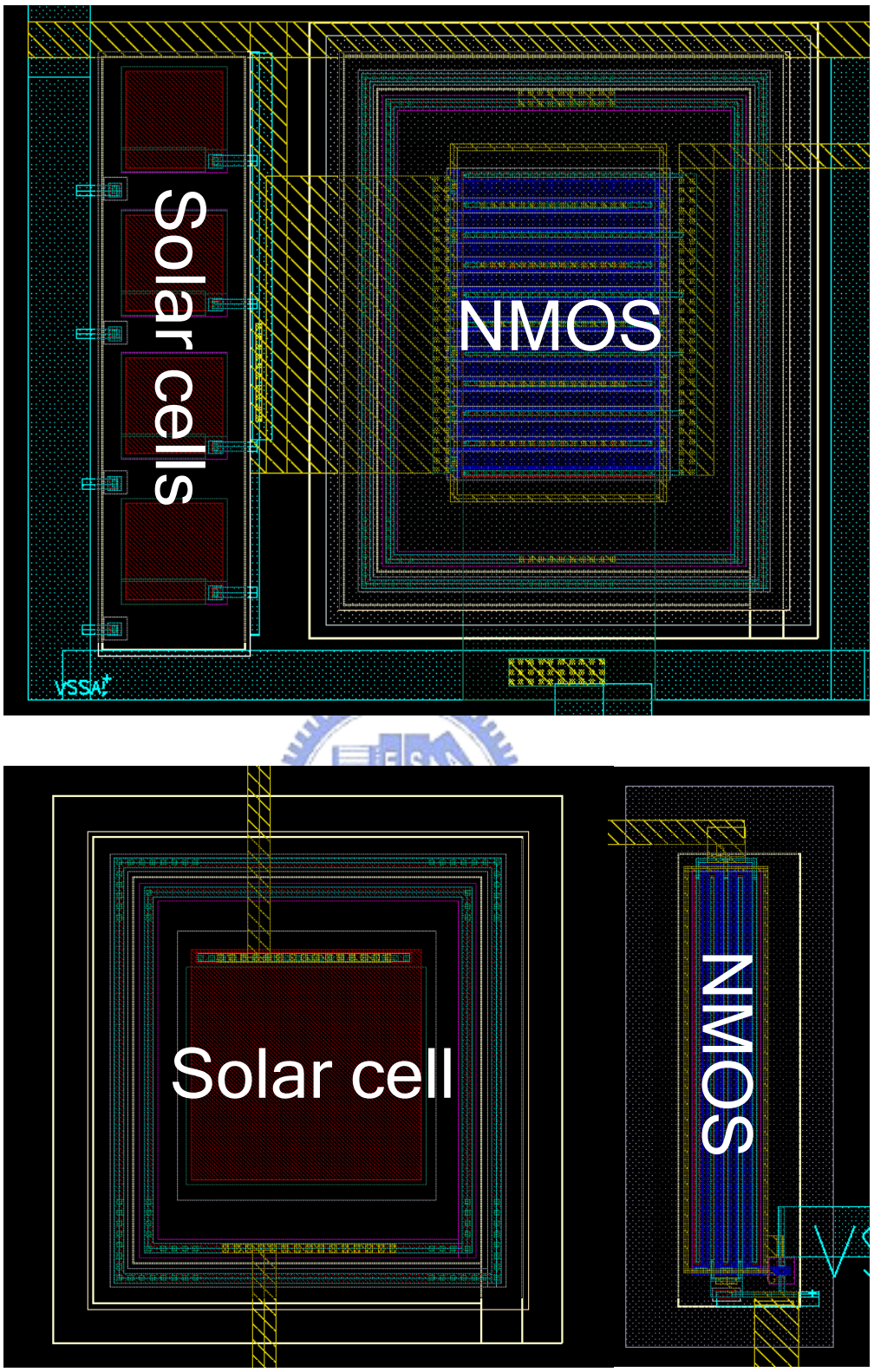


Figure 2.2 the top view of two different layout methodology. Top: the NMOS is isolated by the deep-n-well and the p-substrate pick-up is connected to p-well within deep-n-well. Therefore the p+/n-well solar cell can maintain the characteristic with the floating p-substrate. Bottom: the solar cell is isolated by the deep-n-well and the deep-n-well is floating that the solar cell within the deep-n-well can still maintain the power supply characteristic. The layout of the NMOS in the circuit is still the same as conventional design.

2.2 EXPERIMENTAL RESULTS OF SOLAR CELL

The measurement results of the solar cells which have same layout configuration of top block of Fig. 2.1 is shown in Fig. 2.3 and the measurement results of the solar cells which have same layout configuration of bottom block of Fig. 2.1 is shown in Fig. 2.4. we can see that both of the solar cell structures can function as a power supply with the CMOS technology and the photocurrent is in proportional to the irradiation intensity and the photovoltage is about 0.4V to 0.6 V (most of the Voc fall in the 0.4V to 0.5V interval). According to the Fig. 2.3 and Fig. 2.4, the total effective area of the solar cell testkey is the same but the phototransduction efficiency of each testkey is different. The p-well/n+ solar cell has better phototransduction efficiency than the p+/n-well solar cell due to the high doping concentration of n+ can prevent the contaminated atoms to diffuse into Si in N+ OD area (active region). Therefore the effective photocurrent in n+/p-well solar cell is larger than p+/n-well solar cell. [49] The experiment results of the testkey which composed of two p-well/n+ solar cells connected in series is shown in Fig.2.5. We can see that there is a huge current leakage compared with Fig. 2.4. The current leakage is due to the parasitic PNP and NPN structure around two solar cells. But we can sure that the p-well/n+ structure can be applied in higher supply voltage on-chip solar cell supply system. As a result, the further design of the silicon retina can use regular supply voltage, such as 3.3V for 0.35 um process and 1.8V for 0.18um process.

Further more, we proposed another set of the solar cell testkey which is in order to verify the relation between phototransduction efficiency and distance between active two parallel active regions. The layout top view and cross section view are shown in Fig. 2.6 which the distance between the neighboring active regions is 2um, 4um, 8um and 16um respectively to block A, B, C and D of bottom block. The measurement result is shown in Fig. 2.7. The displacement between two neighboring active regions has great effect on the phototransduction efficiency due to the n-well region increasing with the displacement increasing. The n-well generate a lot of electron-hole pairs while the light irradiating on it and the electron-hole pairs will be swept into the depletion region becoming the photocurrent. Therefore, the larger n-well size induces bigger photocurrent but the photocurrent will be saturated due to the distance between electron-hole pair and metal contact is too far to pass electrons or holes. As we can see in the Fig. 2.7, the photocurrent saturate at the displacement of 10um and this measurement data can provide a layout guideline for the future solar cell supply system research.

In summary, The feasibility of on-chip solar cell supply system which integrated with circuit system in CMOS technology has been verified in the work and the feasibility of high voltage power supply system with only solar cell is also been verified.

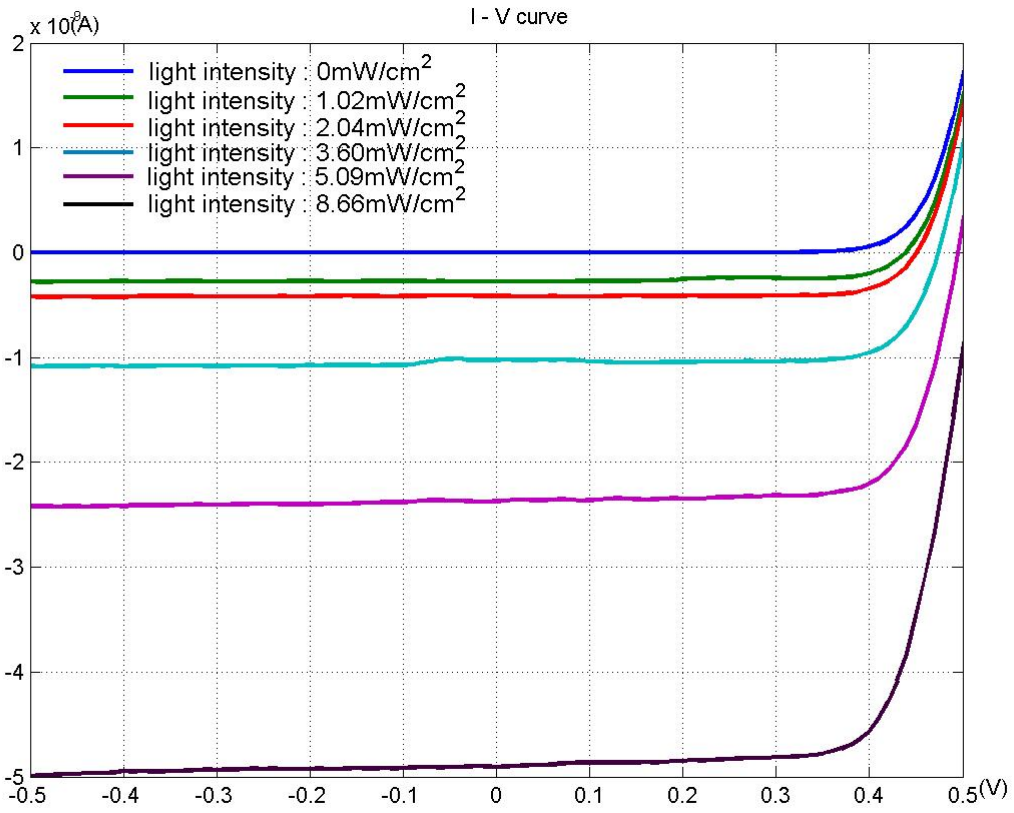


Figure 2.3 the measurement results of the p+/n-well solar cell with the floating p-substrate under varying light intensities. The solar cell testkey which measured is somposed of four 5um x 5um solar cells connected in parallel.

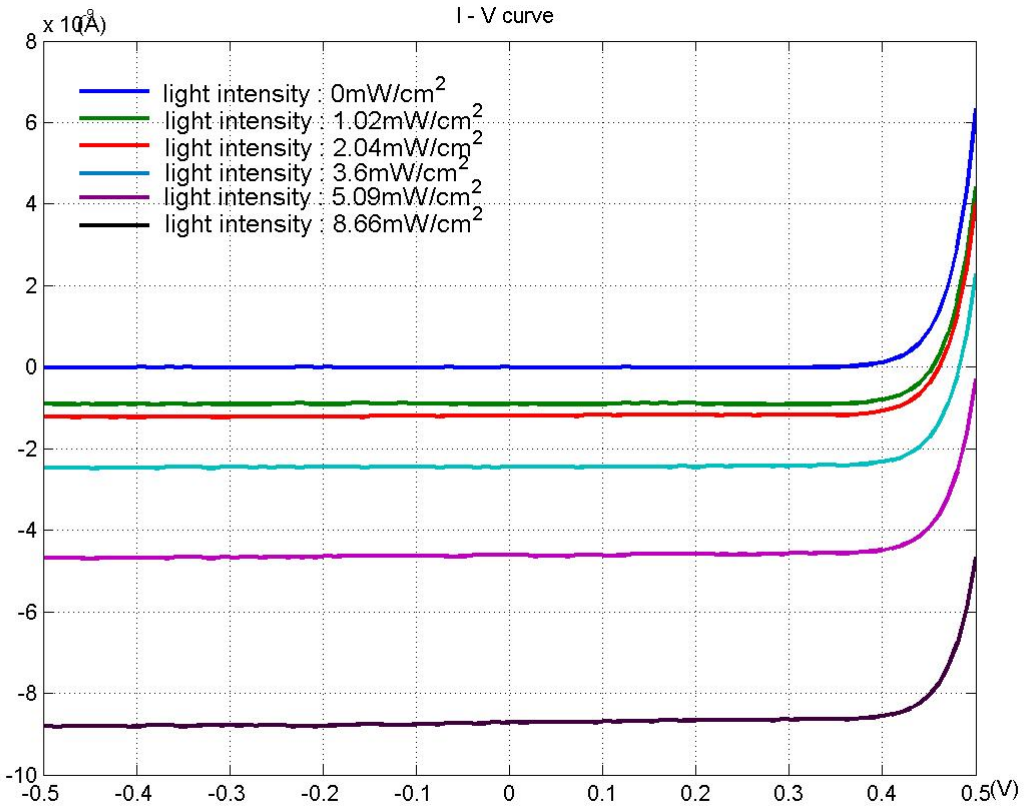


Figure 2.4 the measurement results of the p-well/N+ solar cell with the deep-n-well under varying light intensities. The solar cell testkey which measured is composed of one 10um x 10um solar cell.

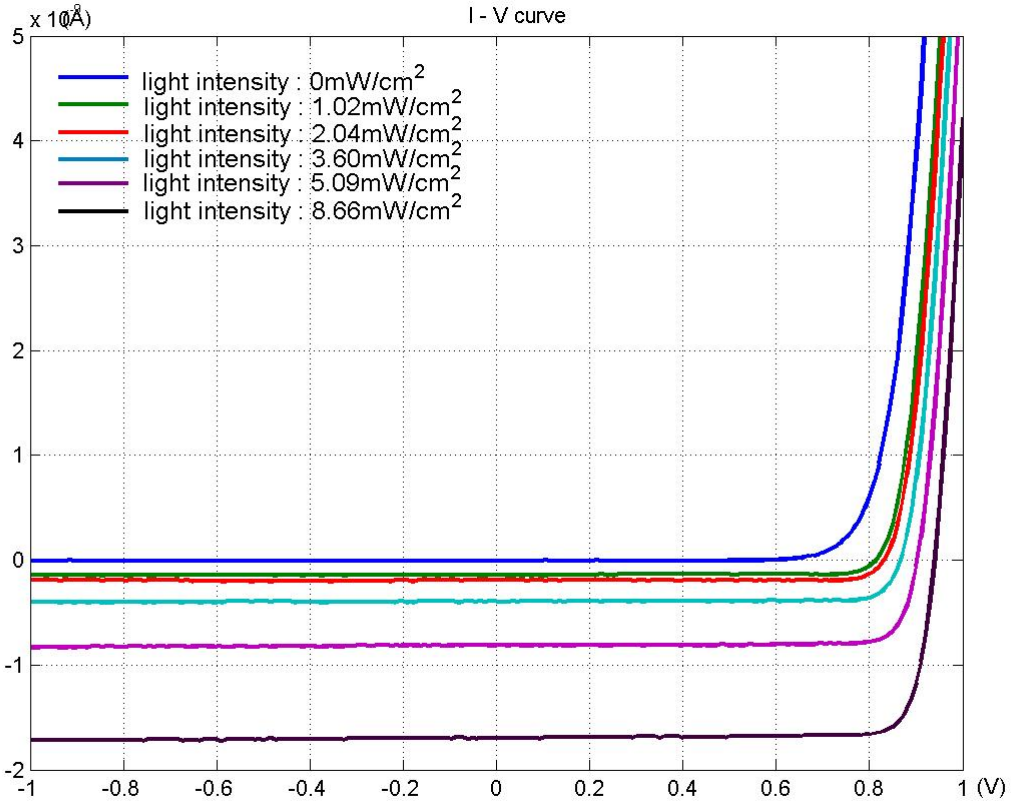


Figure 2.5 the measurement results of two p-well/n+ solar cells with the deep-n-well which connected in series under varying light intensities. The solar cell testkey which measured is composed of one 10um x 10um solar cell.

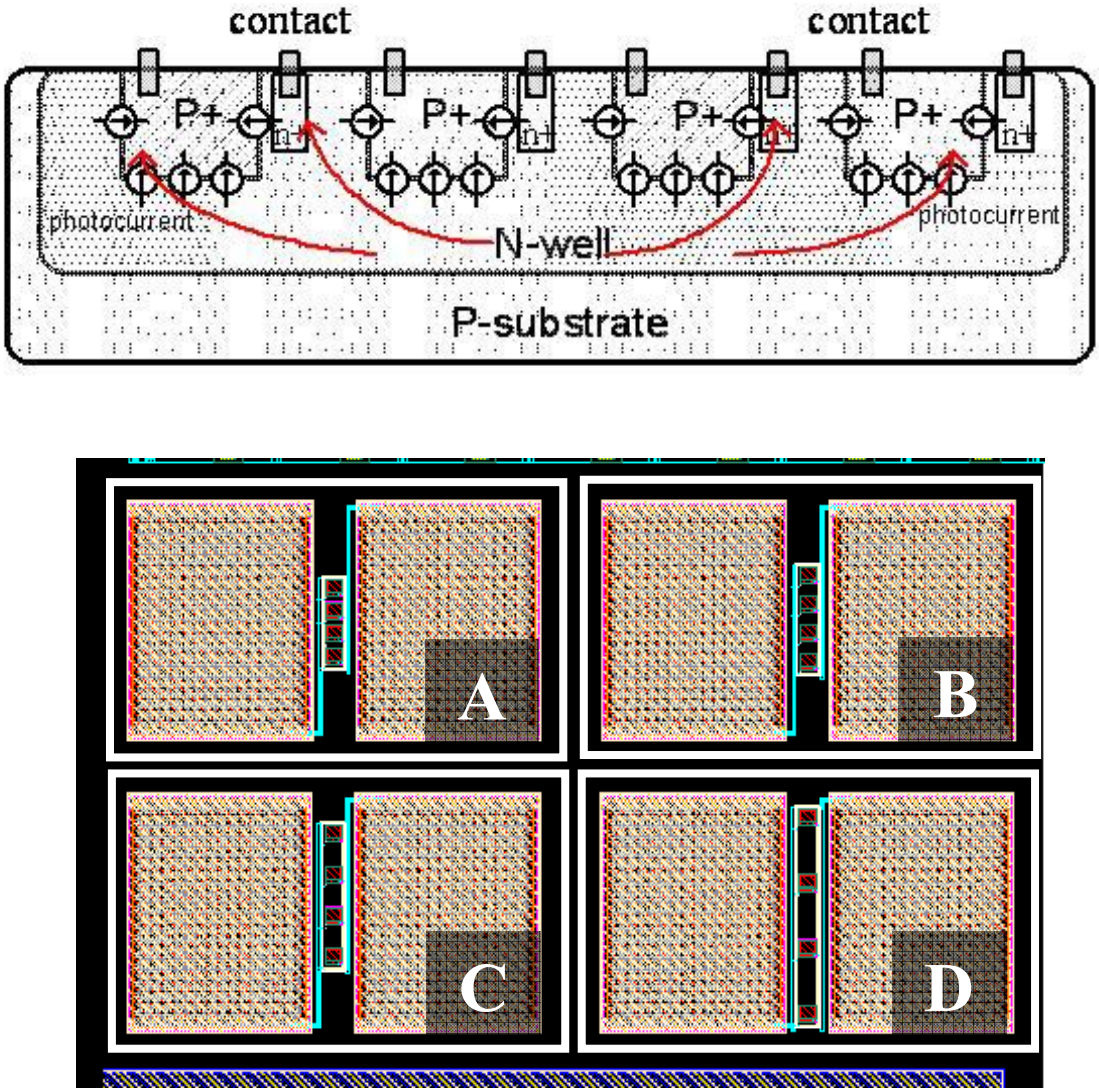


Figure 2.6 Top: cross section view of the solar cells. Bottom: the four testkeys which is composed of four 5um x 5um solar cells connected in parallel and the distance between the neighboring active regions is 2um, 4um, 8um and 16um respectively to block A, B, C and D.

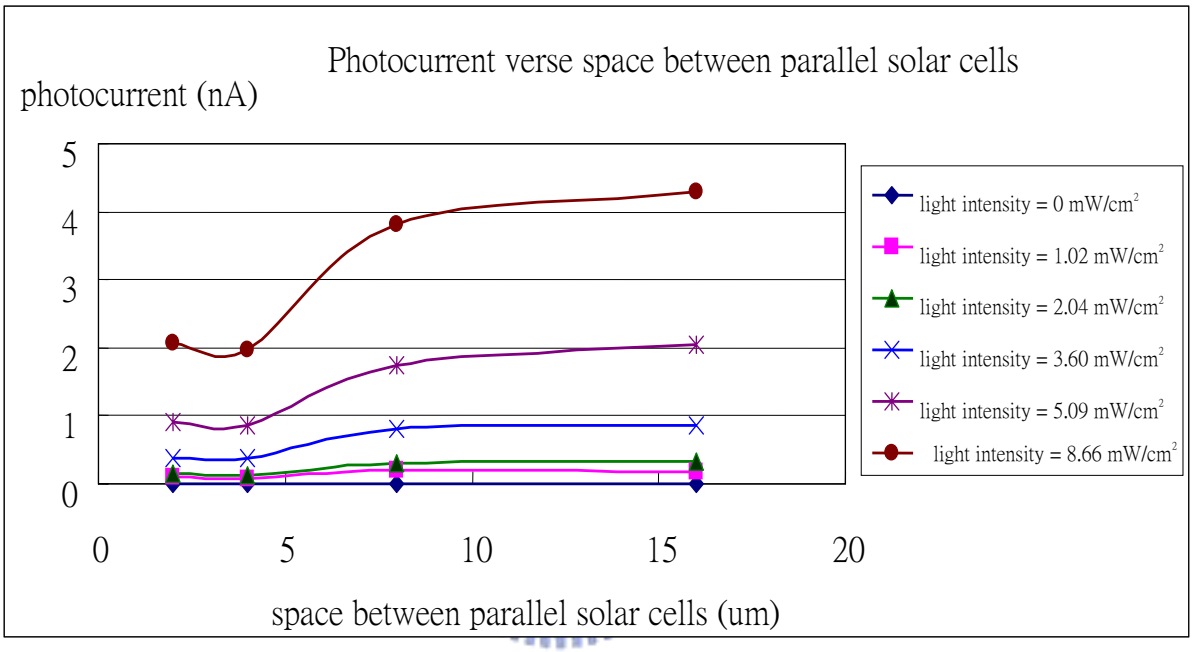


Figure 2.7 the four testkeys which is composed of four 5um x 5um solar cells connected in parallel and the distance between the neighboring active regions is 2um, 4um, 8um and 16um respectively to block A, B, C and D.

CHAPTER 3 In Vitro Experiment of Photodiode Array

3.1 CHIP STRUCTURE

As mentioned in previous chapter, we proposed the novel structure of the solar cell in CMOS technology. In the conventional silicon retina design, the micro-photodiode-array, MPA, is one of the most popular designs. [44, 46] The solar cells in the MPA which Allen Chow proposed is composed of P+/N-well solar cell and the P+ is connected to the retinal tissue and N-well is floating. The solar cell in the design is under open circuit condition and the cross-junction voltage is in proportion with the incident light strength. Therefore the stimulation in [44, 46] is positive voltage stimulus. In our study, we found that the current stimulus can mimic the cell stimulation better. The silicon retina with MPA in this work is composed of P+/N-well solar cell with P+ connected to retinal tissue and N-well connected to ground which function as a return of the solar cell circuit as shown in Fig. 3.1. The stimulus is a photocurrent which flow from N to P of the solar cell PN junction and the current amplitude is in proportion with incident light strength.

The layout view of the pixel in MPA is shown in Fig. 3.2. The red block is the output electrode and the orange block within the red block is a 10μm x 10μm passivation window which really contact to the retinal tissue. The green block is the solar cell and the blue and yellow lines are the routing paths. The chip view of the MPA is shown in Fig. 3.3. The dark spot on the chip is the exposure electrodes and the large electrode on the right-bottom side is the common ground of the MPA which all the N-well ends are connected here to provide a return path to the MPA. The chip view under the immersion microscope which used in the in vitro experiment is shown in Fig. 3.4. The specification of the chip is shown in table I.

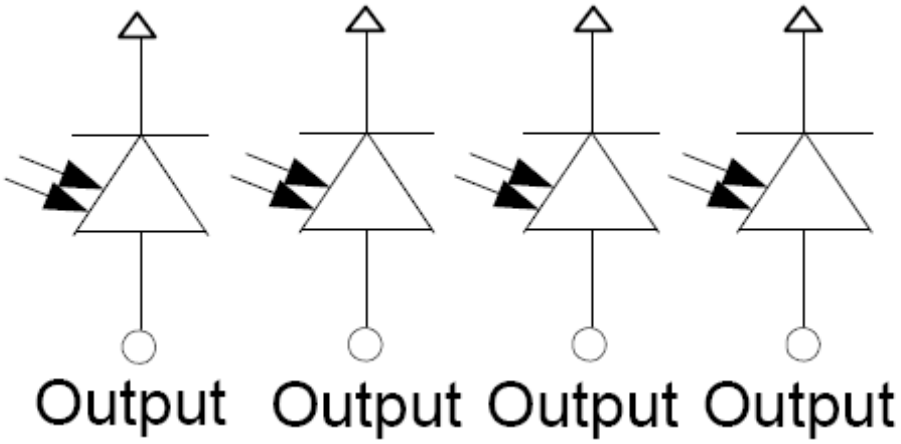


Figure 3.1 The P+/N-well solar cell with P+ connected to retinal tissue and N-well connected to ground which function as a return of the solar cell circuit.

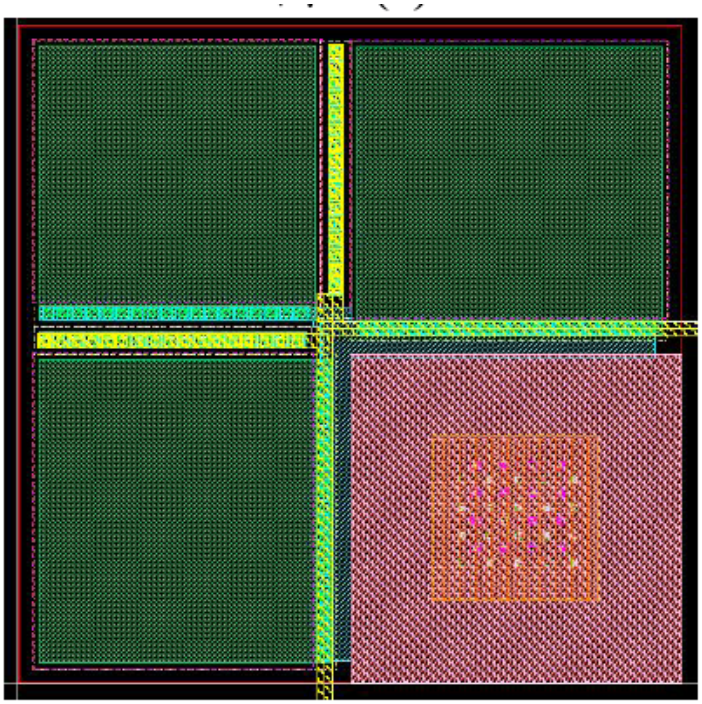


Figure 3.2 The layout view of the pixel in MPA. The red block is the output electrode and the orange block within the red block is a 10μm x 10μm passivation window which really contact to the retinal tissue. The green block is the solar cell and the blue and yellow lines are the routing paths.

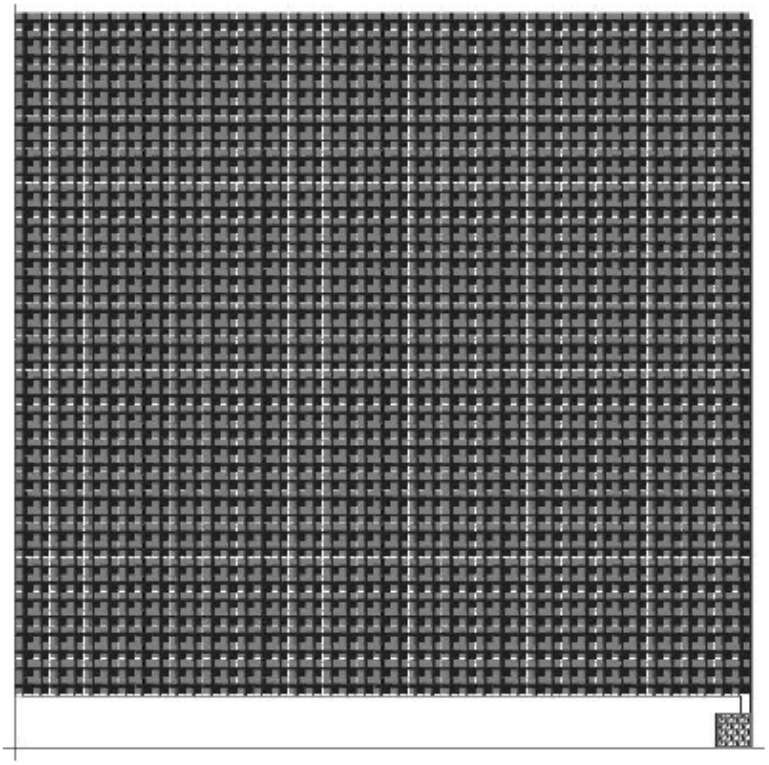


Figure 3.3 The chip view of the MPA. The dark spot on the chip is the exposure electrodes and the large electrode on the right-bottom side is the common ground of the MPA which all the N-well ends are connected here to provide a return path to the MPA.

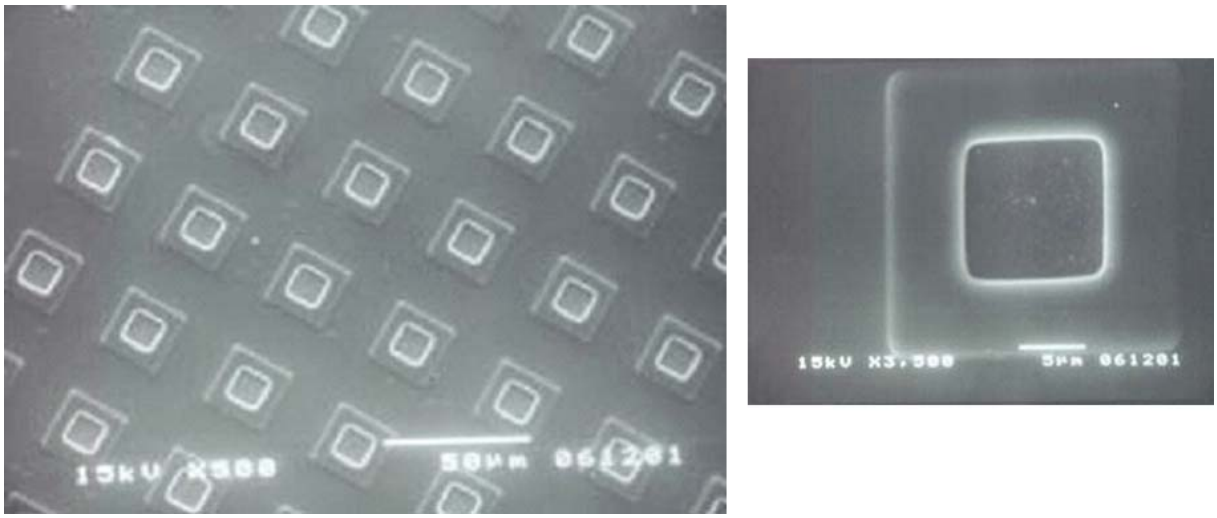


Figure 3.4 The chip view under the immersion microscope which used in the in vitro experiment.

TABLE I. SPECIFICATION OF THE IMPLANTABLE MPA

SPECIFICATION	
Power supply voltage	No external power supply
Pixel number	45 x 44 cells
Array size	1.7644x1.8mm^2
Exposured electrode size	10 x 10 μm^2
Photosensing area size	3 x 16.7 μm x 15.7 μm
Stimulation type	Current output

3.2 IN VITRO EXPERIMENT ENVIRONMENT SETUP

3.2.1 Retina preparation

This study will use retina tissues from adult New Zealand White rabbits (1-2 kg). The animal will be anesthetized with an intramuscular injection of 1:1 mixture of ketamine (50mg/ml) and xylazine (20mg/ml). A local anesthetic (proparacaine hydrocholoride; 2-3 drops) will be applied to the eye before intraocular injection of 4', 6-diamidino-2-phenylindole (DAPI, 2μg; Sigma, St. Louis, MO). The animal will be allowed to recover. One day after DAPI injection, the animal will be dark-adapted for at least one hour before dissection. The animal will be deeply anesthetized again for isolating the retina. Each eye will be removed and hemi-sected in oxygenated (95% O_2 and 5% CO_2) Ames' medium. The retina will be dissected out from the sclera and carefully peeled off the pigment epithelium. A small piece of the ventral retina (5×8 mm) will be cut off and placed flat on the silicon retina mentioned above as in Fig. 3.5. This tissue will be pressed down by weights with nylon netting for getting a good contact. This preparation will be moved to a custom-made recording chamber attached to a microscope stage of a fluorescence microscope (Axioskop 2 FS Plus, Zeiss, Germany) and superfused at rate of 1.5-2.5 ml/min with oxygenated Ames' medium at 34-37°C. All procedures will be carried out under dim red illumination. The deeply anesthetized animal will be euthanized with overdose of anesthetic or 100% CO_2.

3.2.2 Electrophysiological recording

Membrane potentials will be recorded extracellularly from individual ganglion cell bodies with a tungsten-in-glass electrode (tip size, 30-40μm; resistance, ~1 MΩ). Signals will be amplified, filtered, and fed into a differential amplifier (ISO-80, WPI). The analog inputs will be converted into digital signals using a PC computer equipped with the data acquisition (DAQ) device (National Instrument, Texas, USA). The signals will also be displayed on an oscilloscope for observation and fed into an audio amplifier for monitoring spikes. The operation of extracellular recording will be controlled by a custom-written software (LabView). Off-line analysis will be carried out using the Matlab (The MathWorks). The retina will be closely attached on the MPA with cell-tak (a preparation of barnacle glue shown to increase attachment of tissue and cells: BioPolymers. Inc.. Farmington, CT).

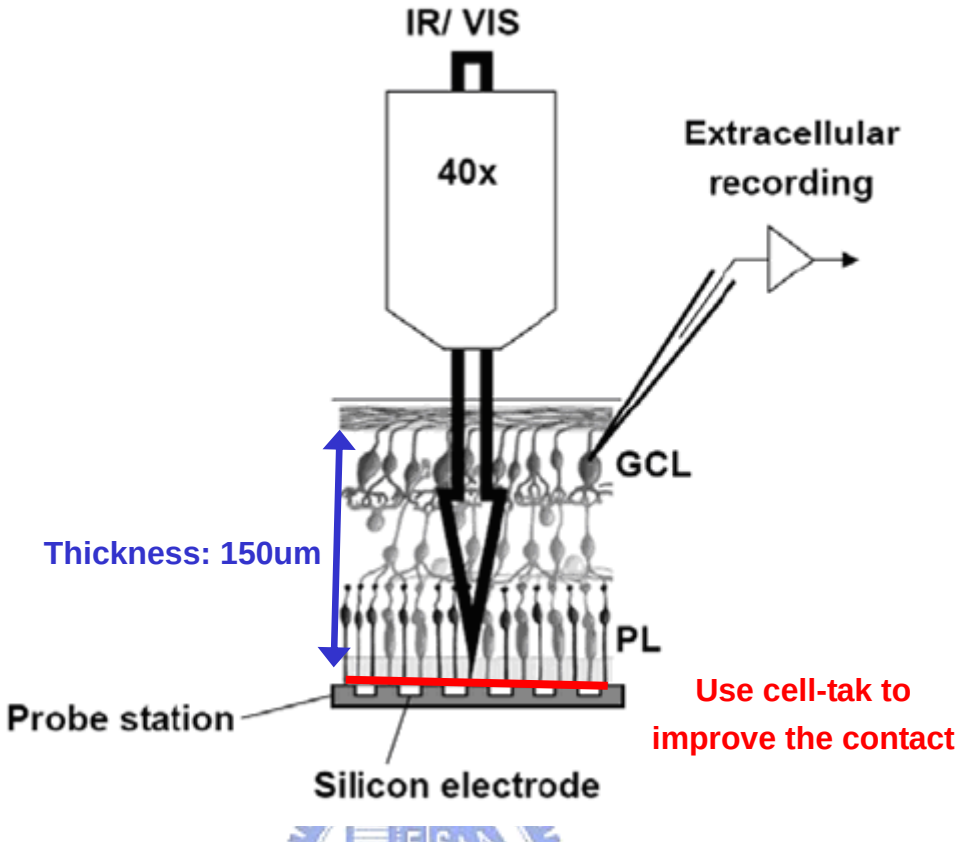


Figure 3.5 Top: the schematic of the measurement environment. Bottom: the setup view of the measurement environment.

3.3 IN VITRO EXPERIMENT RESULTS

The main purpose of this in vitro experiment is to verify the electrical stimulation of the retinal chip and we provide the light-response experiment and electrical-response which the electrical simulation is from the retinal chip which is triggered by IR. In compare with the light-response and electrical-response, the light intensity of the CRT light stimulation (visible light) is too low to trigger the retinal chip and the waveform recorded is almost the pure light-response of the ganglion cell, and the IR stimulation won't trigger the normal ganglion cell due to that IR is not visible light and recorded waveform is definitely not from the light-response of ganglion cell but from the electrical stimulation of the retinal chip which triggered by IR. The ganglion cell used in this in vitro experiment is shown in Fig. 3.6. Fig. 3.7 shows the extra-cellular signal which recorded under varying light intensity of IR stimulus. Fig. 3.8 shows the zooming of the extra-cellular signals above. There is a spike with latency shown after the IR stimulation while the IR intensity is over 400mW. This spike is a strong evidence to prove the retina cell is triggered by the MPA. Fig. 3.9 shows the comparison between electrical stimulation and light-response. With the same experiment environment, including chip, retina, probe position and temperature, two responses from two different stimulations are recorded individually. Left block shows the signal which recorded while silicon retina was triggered by IR irradiation. Right block shows the ganglion cell response while the visible light triggers the retina. Despite the artifact, the latency response of both signals has some in common. This data shows that the sub-retinal prosthesis with silicon retina which powered by solar cell is able to trigger the retina and may replace the functionalities of outer-plexiform layer of the retina.

In order to compare with the Fig.3.6, Fig. 3.10 shows the extra-cellular signal which recorded under varying light intensity of IR stimulus but the retina is removed. As shown in Fig.3.11, with the same experiment environment, including chip, IR stimulation, probe position and temperature, two signals are recorded individually. Left block shows the signal which the retina is still attach on the silicon retina. Right block shows the signal while the retina is removed from the chip. Under the same IR stimulation, the right block show some artifacts which is induced by the silicon retina. The same artifact is also shown in left block, but the spike with latency is clearly shows the feasibility of the silicon retina which can generate effective stimulation under IR stimulation. The Fig.3.12 shows the threshold of the retinal cell in this experiment is the stimulating current while MPA is under 400mW IR illumination and 400mW IR illumination on the MPA can induce about 42uA photocurrent. Therefore the threshold of the off α ganglion cell in this experiment is about 42uA. Further more, we carry on the same experiment with the on α ganglion cell. We can also record the cell response to verify the feasibility of the on α ganglion cell and the threshold of the on α ganglion cell is about 18uA. These experiment results can ensure that the silicon retina can

trigger the retina in the sub-retinal prosthesis. As a preliminary in vitro experiment of the silicon retina, the feasibility of the sub-retinal silicon retina is verified and the experiment data can provide some useful information to the future work.

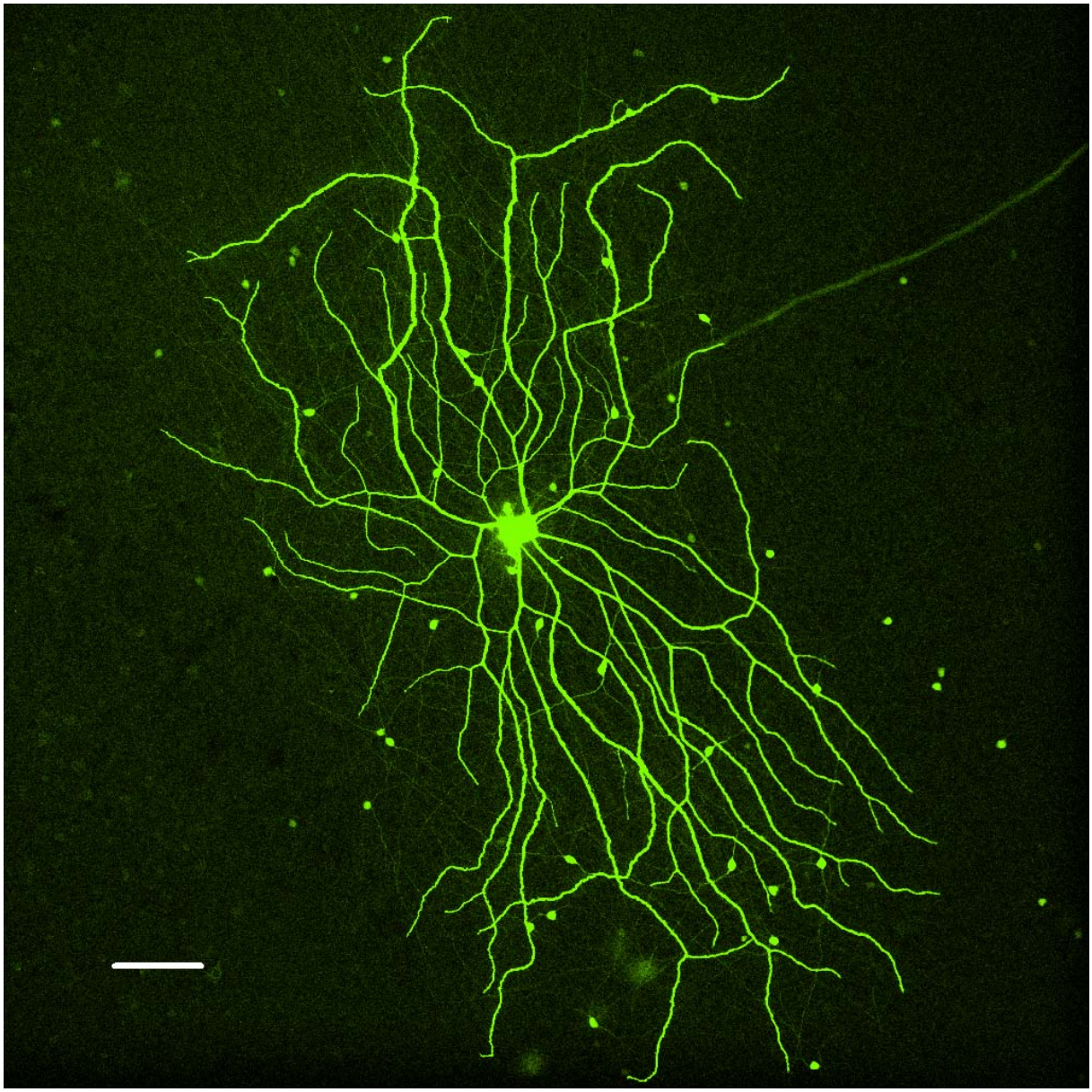


Fig. 3.6 the ganglion cell used in this in vitro experiment. White bar represent 100um and the size of this ganglion cell is about 1.2mm. This picture is reprinted from NTHU Y.T. Yang.

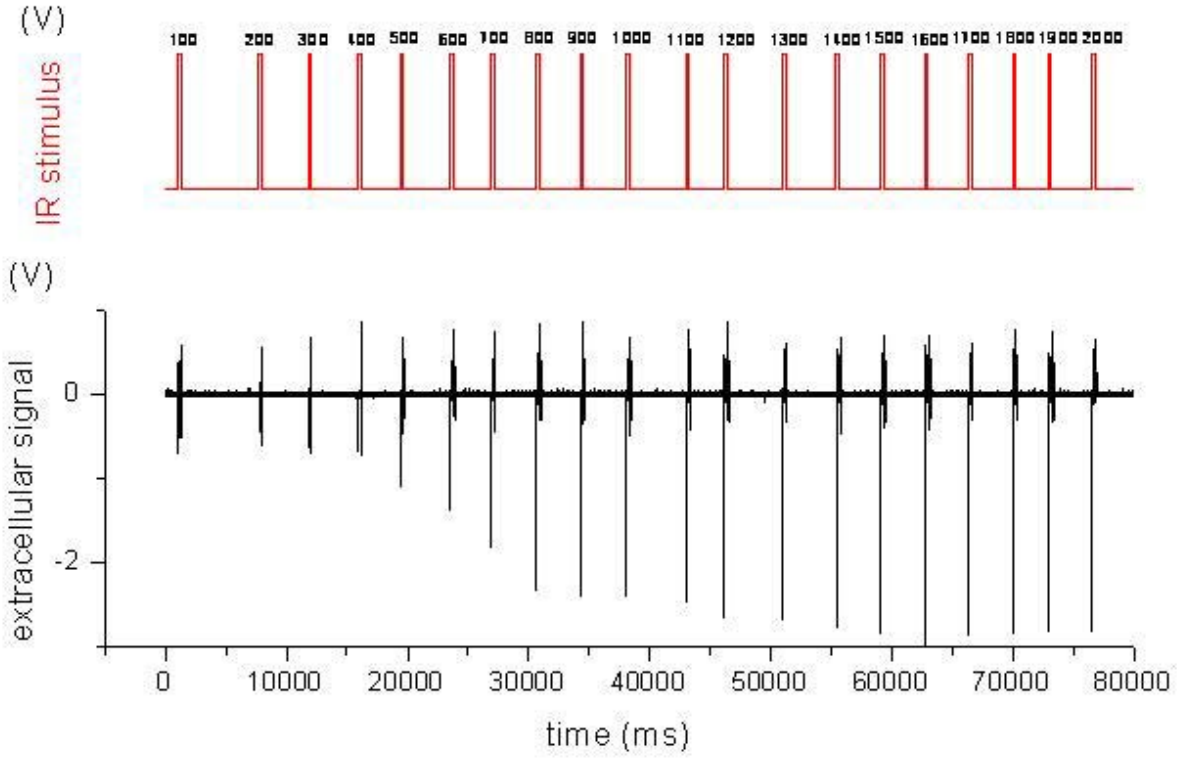


Fig. 3.7. The extra-cellular signal recorded under varying light intensity of IR stimulus. The IR intensity vary from 100mW to 2000mW.

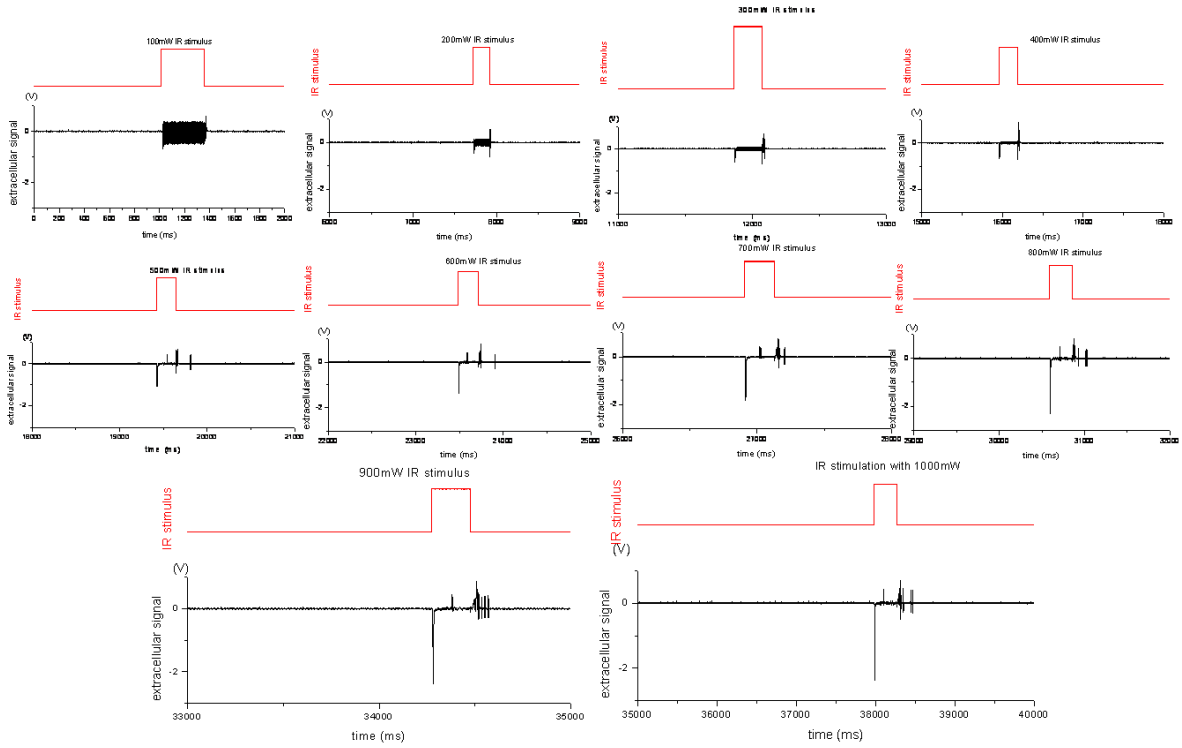


Fig. 3.8. The extra-cellular signal recorded under varying light intensity of IR stimulus. The IR intensity vary from 100mW to 2000mW. Each block is the zooming figure of Fig. 3.7. The spike with latency represents the cell's response to the silicon retina's trigger.

IR stimulus with1000mW and CRT stimulus

(electrical response and light response)

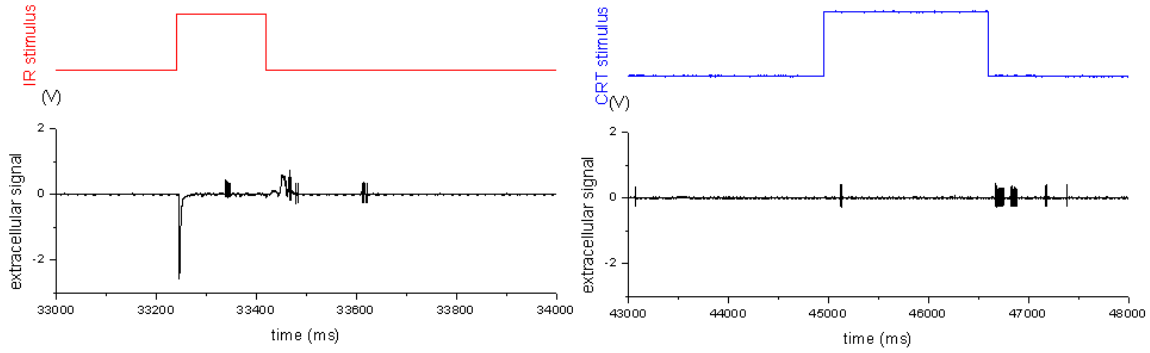


Fig. 3.9 The comparison between electrical stimulation and visible light stimulation. With the same experiment environment, including chip, retina, probe position and temperature, two responses from two different stimulations are recorded individually. Left block shows the signal which recorded while silicon retina was triggered by IR irradiation. Right block shows the ganglion cell response while the visible light triggers the retina. Despite the artifact, the latency response of both signals has some in common.

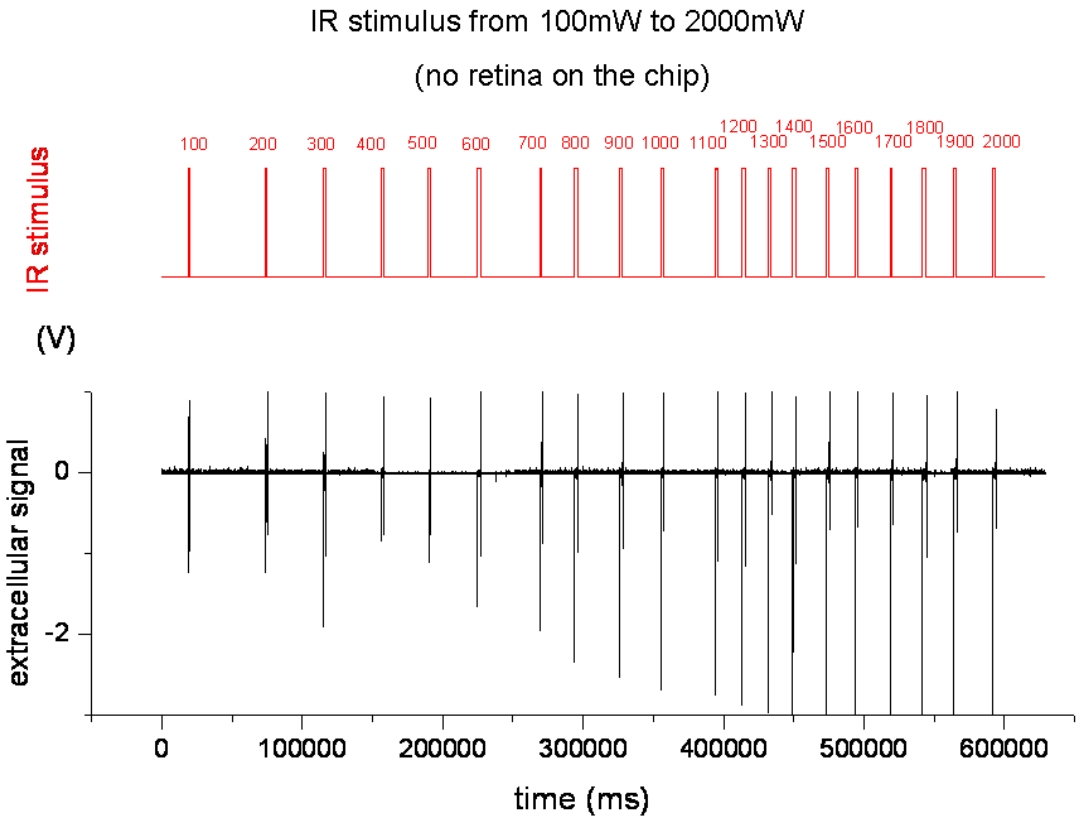


Fig. 3.10 The signal recorded under varying light intensity of IR stimulus with no retina on the chip. The IR intensity vary from 100mW to 2000mW.

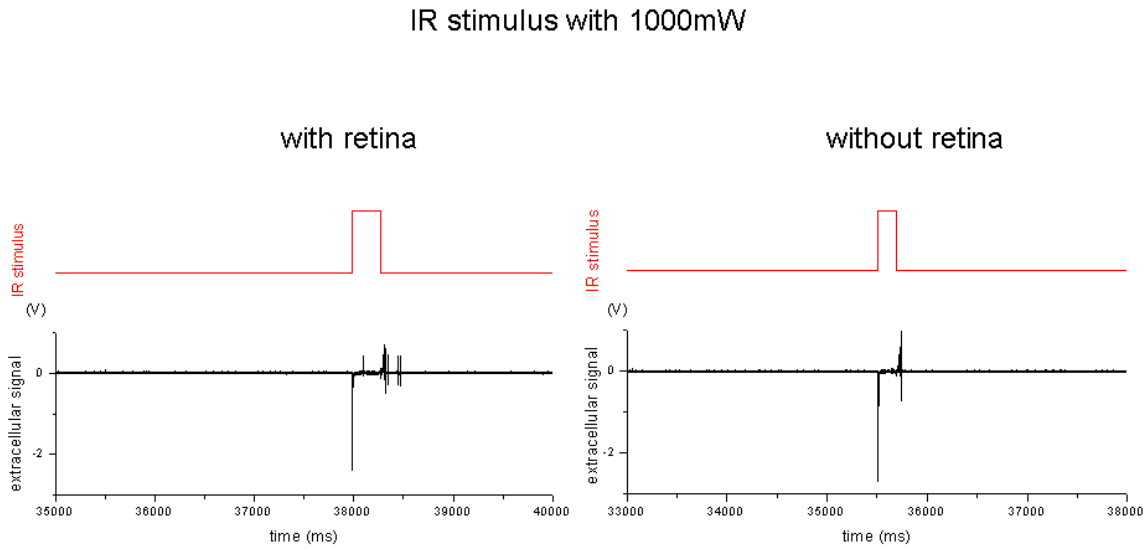


Fig. 3.11 The comparison between cell response and silicon retinal artifact. With the same experiment environment, including chip, IR stimulation, probe position and temperature, two signals are recorded individually. Left block shows the signal which the retina is still attach on the silicon retina. Right block shows the signal while the retina is removed from the chip. Under the same IR stimulation, the right block show some artifacts which is induced by the silicon retina. The same artifact is also shown in left block, but the spike with latency is clearly shows the feasibility of the silicon retina which can generate effective stimulation under IR stimulation. This experiment result can ensure that the silicon retina can trigger the retina in the sub-retinal prosthesis.

■ **Threshold estimation of electrical stimulation**

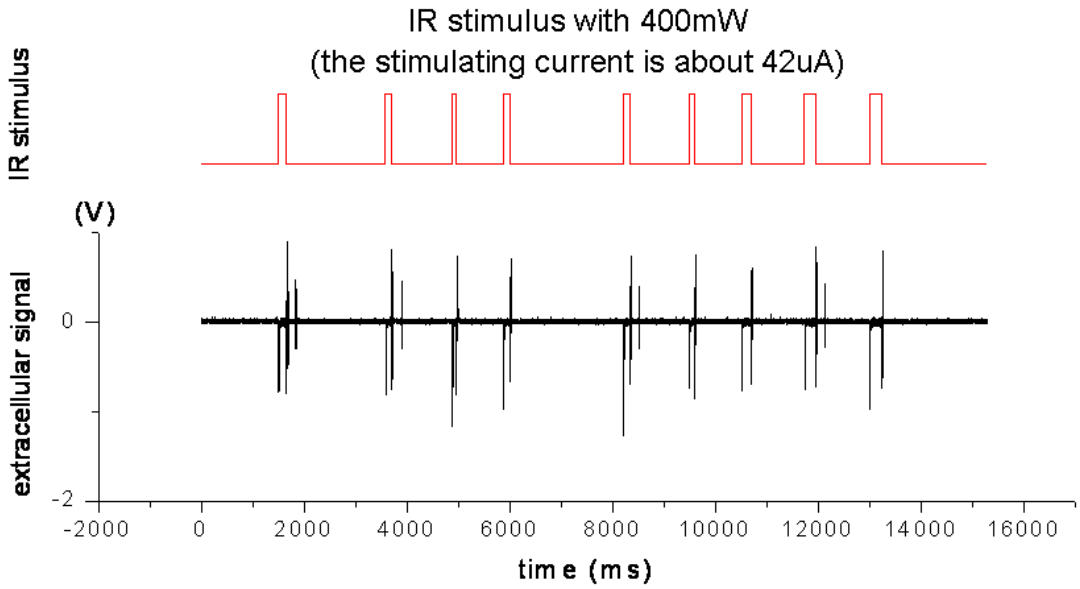


Fig. 3.12 the threshold estimation of the in vitro experiment. As we can see in this figure, the cell response is recorded occasionally. This means the threshold of the retinal cell is about this light intensity (or stimulating current).

3.4 DISCUSSIONS

As we can see in Fig. 3.7 – 3.11 , the retina cell is triggered by the MPA silicon retina is verified and the feasibility silicon retinal chip for sub-retinal prosthesis is also verified. We also carry on the same experiment with the on α ganglion cell and the threshold is about 300mW IR irradiation which means the stimulating current is about 18uA. In compare with the experiment in [48], the Fig. 3.13 and table II shows the comparison results and the experiment environment of the experiment mentioned in [48]. As we can see in the table II, both experiment animal are rabbits and the stimulation site are the same (PR side). According to Humayun's report in [48], the electrode size has significant effect on the stimulus threshold. The smaller electrode size has higher stimulation threshold. According to the table, the threshold measured in our in vitro experiment is very reasonable and the threshold is slightly higher due to the small electrode used in this experiment. But in the real application of the retina prosthesis, the IR stimulus with over 400mW is too large to destroy some eye tissue and the safety limit of the IR irradiation which applied in eye relative prosthesis is 10 sun light intensity which is about 100~200mW. Therefore the next generation silicon retina must solve this solar cell power issue.

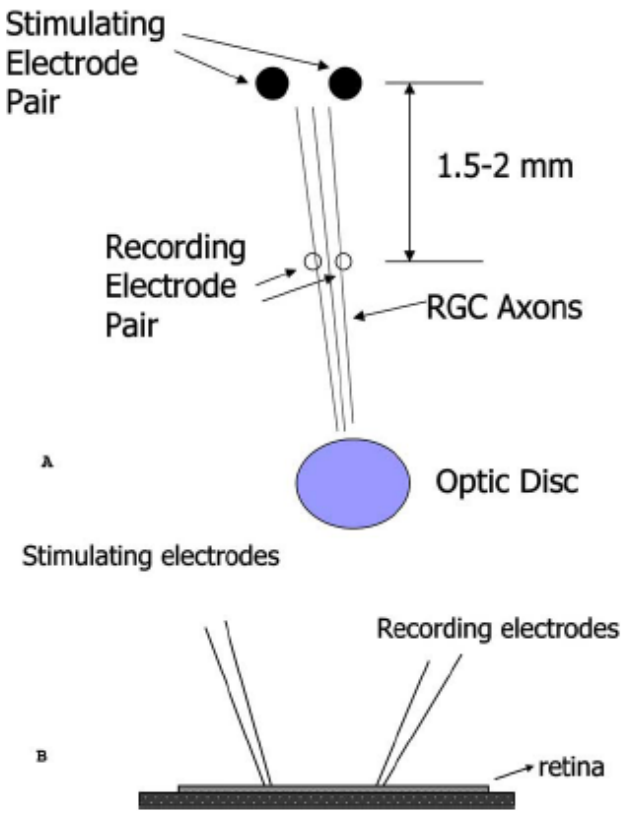


Fig. 3.13 The experiment schematic of the in vitro experiment which mentioned in M. Humayun in 2006.[48] Stimulus and recording electrodes were positioned to record retinal ganglion cell action potentials from axons projecting from the stimulus site. Stimulating electrodes were platinum disks, either 25 or 125 _m in diameter. Two tungsten microwires were used as a differential recording electrode pair. (a) Top view of the isolated retina chamber. (b) Schematic cross section of recording chamber. Retinal ganglion cell (RGC). Both stimulating and recording electrodes were positioned using manual micromanipulators. Since the stimulating electrodes could not penetrate the retina, the location of the stimulating electrodes (GC or PR) determined which side of the retina was placed face up in the chamber. Recording electrodes were positioned first. When stimulating PR, the PR side faced up and the recording electrodes penetrated through the retina to the GC nerve fiber layer. When stimulating GC, the GC side faced up and the recording electrodes were inserted slightly into the GC nerve fiber layer.

TABLE II. the comparison of this work and M.Humayun in 2006 [48]

	This work		Mark S. Humayun,2006 [48]	
Animal	**New Zealand Rabbits**		**Dutch Belted Rabbits**	
Target cell	**OFF α GC**	**ON α GC**	**GC (type not mentioned)**	
Stimulating type	**current level**		**current pulse**	
Stimulating site	**PR**	**PR**	**PR**	**PR**
Electrode size	**10x10um^2 square electrode**		**25um diameter circle electrode**	**125um diameter circle electrode**
Threshold current	**42uA**	**20uA**	**17.1±5uA**	**6.7±4uA**

CHAPTER 4 Design and Analysis of Retinal Chip

4.1 CLOCK GENERATOR AND POWER CONTROL UNIT

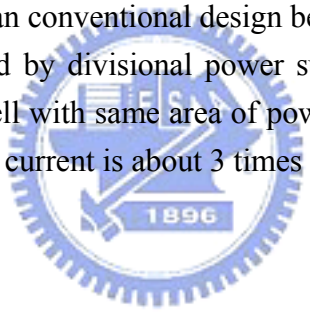
Persistence of vision is the phenomenon of the eye by which even nanoseconds of exposure to an image result in milliseconds of reaction (sight) from the retina to the optic nerves. This is because persistence of vision depends on chemical transmission of nerve responses, and this biochemical hysteresis is much slower than the light transmission. A typical explanation of persistence of vision went something like this: when the human eye is presented with a rapid succession of slightly different images, there is a brief period during which each image, after its disappearance, persists upon the retina, allowing that image to blend smoothly with the next image. [47] Therefore the retinal chip needs not to stimulate the retinal cell continuously but stimulate the retinal cell with a more discrete method. As we know that the maximum frame rate which can be distinguished by human is about 60Hz, namely, we can stimulate the retinal cell every 16ms or less and the retina still consider the discrete stimulus as a continuous stimulus.

By applying the technique of divisional power supply architecture to exploit the characteristic mentioned above, a three times output current could be achieved. The details are in the followings. We divide the pixel array into four blocks whole outputs are controlled by four control signals generated by power control unit. The blocks will be activated in turn to send out their stimulating signals. The time interval between neighboring activation of the same block must be much smaller than biochemical hysteresis of the cell. Only one of the blocks is activated at the same time and the power from whole chip, which is supplied by solar cells, is provide to that block to increase the output stimulating current. In contrast to the conventional MPA design, the output current is much greater and the discrete stimulus won't cause any misinterpret in the retina but still provide continuous signals to the brain.

The architecture of the chip is shown in Fig. 4.1. The block diagram of the power control unit is marked in the upper box of Fig. 4.1. The whole power control unit is only power supplied by on-chip solar cells. There are three main components in the unit, an oscillator, two frequency dividers, and combinational logic part. The schematics of the clock generator and frequency divider in power control unit are shown in Fig. 4.2. A ring oscillator is used to generate the reference clock. This structure is the same as the one in [50] which only on chip solar cell is acquired. The cross section view of the clock generator is shown in Fig.4.4. The on-chip solar cell system is the only supply of the clock generator and the NMOS is isolated to avoid the parasitic BJT causing the leakage current which result in the clock generator out of function. In order to generate the quadrature phase signal, a D flip-flop frequency divider shown in Fig. 4.4 is chosen to provide two synchronous signals with the half and quarter clock frequency. Two frequency dividers are required in this design because the clock signal from the clock generator is not in a square waveform. A clear square waveform with relatively short

rise time and fall time is required for the combinational logic circuit. Therefore we use two frequency dividers to provide two synchronous square-wave signals with the half and quarter clock frequency. We choose the conventional static cross-coupled NAND structure to implement the D flip flop of the frequency divider as shown in Fig. 4.5. The operating frequency of the frequency divider is about 1KHz to 10KHz which is much lower than the radio-frequency application. Therefore the modern dynamic D flip flop design which will result in charge leakage problem is not suitable for this work. The static design can operate in low voltage supply and also has lower power consumption. In the last stage, the combinational logic circuits consisted of NAND and INV gates synthesizes the final quadrature control signals. The logic gates mention above are powered individually by on-chip solar cell which each gate has six solar cells as the power supply. The schematic of the combinational logic circuit is shown in Fig. 4.6. The circuit schematic of the NAND gates and INV gates are shown in Fig. 4.7. The sizes of the MOSFETs in each block are shown in table III.

In the design of the retinal chip with on-chip solar cell supply, the total power generated by the solar cell is in proportion to the area of the solar cell. Therefore some layout area on the retinal chip is occupied by the power control unit. In other words, the power generated by solar cell in this work will smaller than conventional design because some layout area is occupied by control unit. The power saved by divisional power supply system is much higher than the power generated by the solar cell with same area of power control unit. The simulation results also show the output simulating current is about 3 times of the conventional one.



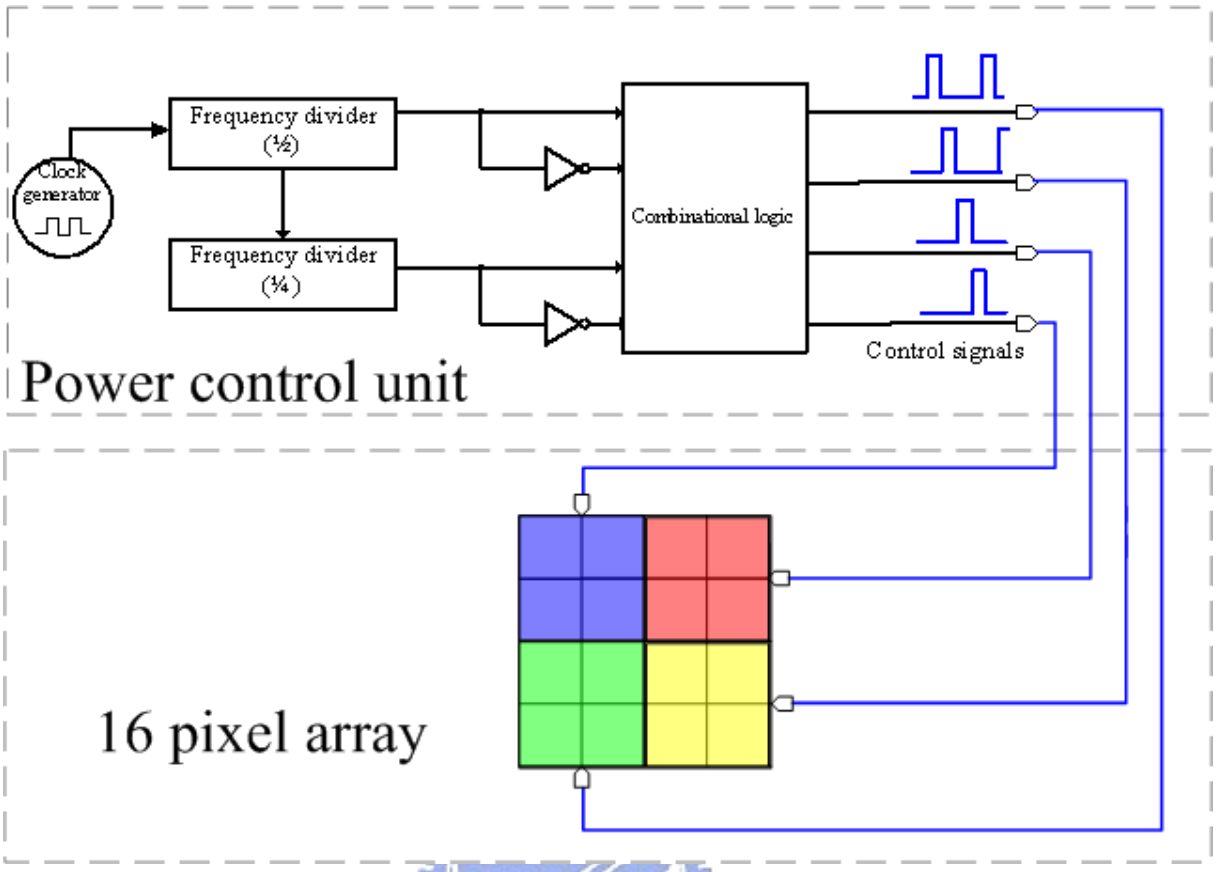


Figure 4.1. The block diagram of the retinal chip. The control circuit which provides quadrature phase control signals to pixel array is composed of pulse generator, frequency dividers, and combinational logic.

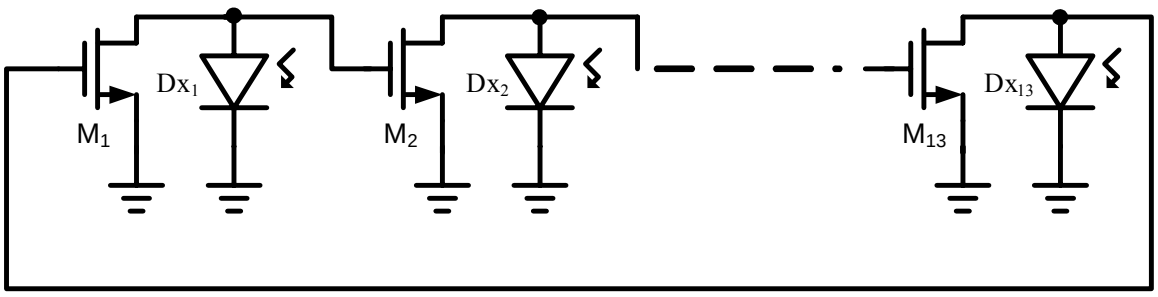


Figure 4.2. The schematic of ring oscillator provides the reference clock signal to control unit.

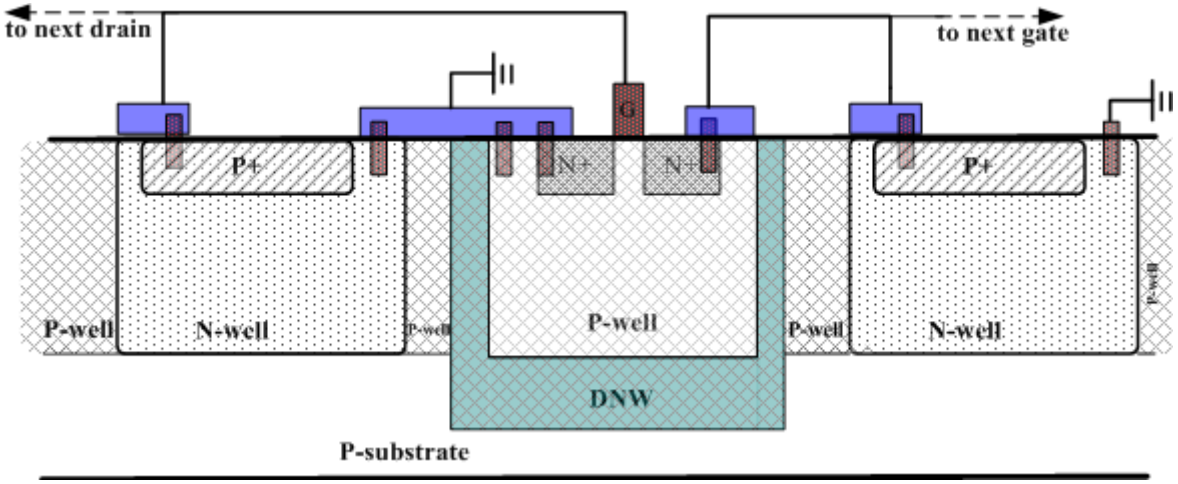


Figure 4.4. part of the cross section of the clock generator. We use the deep-n-well to isolate to NMOS from the leakage current of parasitic BJT.

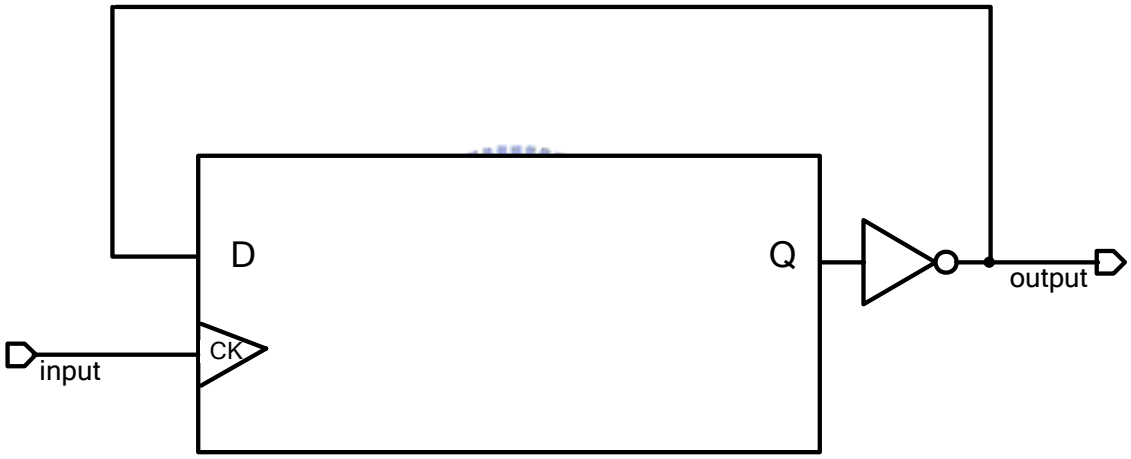


Figure 4.4. The schematic of the frequency divider.

.

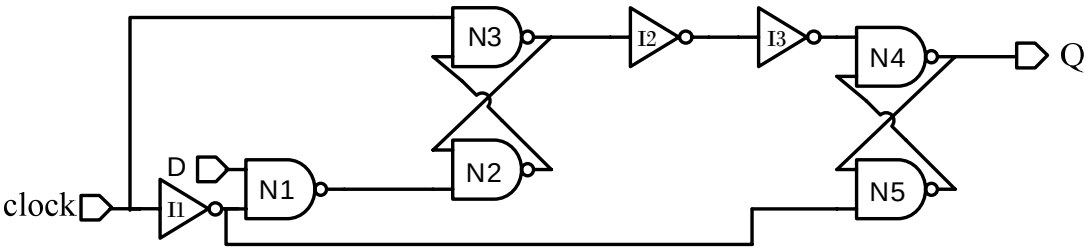


Figure 4.5. The schematic of the frequency divider.

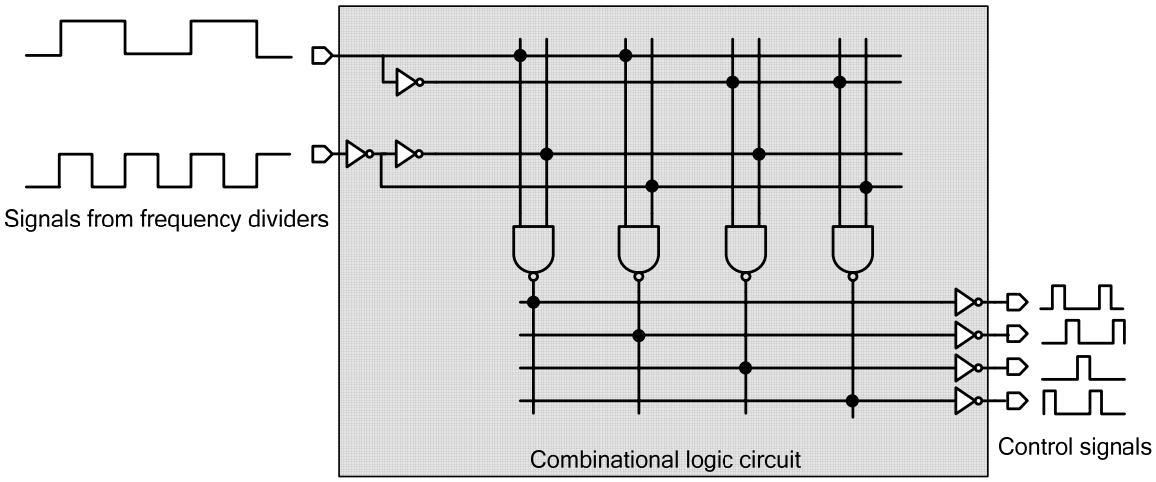


Figure 4.6. The schematic of the combinational logic circuit.

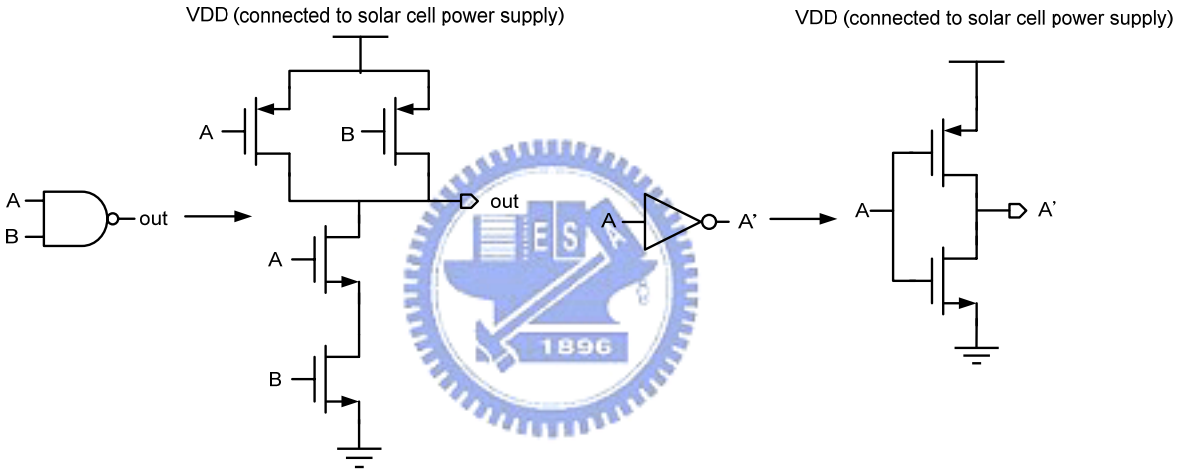


Figure 4.7. The circuit schematic of the NAND gates and INV gates.

TABLE III. sizes of the MOSFETs of each block

clock generator		D flip-flop		combinational logic	
NMOS (μm)		PMOS/NMOS (μm /μm)		PMOS/NMOS (μm /μm)	
M1	100/1	N1	P: 1/0.5	NAND gates	P: 1/0.5
M2	100/1		N: 1/0.5		N: 1/0.5
M3	100/1	N2	P: 1/0.5	INV gates	P: 1/0.5
M4	100/1		N: 1/0.5		N: 0.5/0.35
M5	100/1	N3	P: 1/0.5		
M6	100/1		N: 1/0.5		
M7	100/1	N4	P: 1/0.5		
M8	100/1		N: 1/0.5		
M9	100/1	N5	P: 1/0.5		
M10	100/1		N: 1/0.5		
M11	100/1	I1	P: 1/0.5		
M12	100/1		N: 0.5/0.35		
M13	100/1	I2	P: 0.8/1.6		
			N: 0.4/1.6		
		I3	P: 0.8/1.6		
			N: 0.4/1.6		

4.2 IMPLANTABLE RETINAL CHIP

The architecture of the chip is shown in Fig. 4.1. The power control unit generates quadrature phase pulse signals to activate the four blocks in the pixel array in turn. The whole chip is only power supplied by on chip solar cells to prevent the external wiring from hurting the eye ball. The quadrature signals mentioned previously control the activation of the blocks in the pixel array as shown in lower box of Fig. 4.1. According to the report of the artificial retina prostheses [2], we chose 16 pixels resolution in this chip. There are 16 pixels in the array which is divided into four blocks, and thus each block contains four pixels. The pixel circuitry is shown in Fig. 4.8. Diodes D2, which have 306 solar cells (photodiodes) in parallel connection, as the solar cell are the power supply of a single pixel. All the solar cells in the pixel array are connected in parallel to provide the global power supply to the whole array. Photodiodes D1, which have 6 photodiodes in parallel connection, are the photo-sensor for each pixel whose photocurrent is amplified 200 times through current mirror for stimulating output. In order to provide large output stimulating current, we roughly estimate that each pixel should has at least 300 solar cells to produce at least 500nA output stimulating current under 1200lux illumination. In the prototypical design of the pixel circuit, there has only one photo-sensing diode. But that will induce another problem that the one stage current mirror, which is shown in Fig. 4.8 as M1 and M2, can't afford more than 1000 times amplification and the mirror ratio will has mismatch. Therefore the amount of the photo-sensor photodiode D1 is chosen as 6 to keep the amplification ratio of current mirror in 200. The amount of diodes in D2 is chosen as 306 because there will be quiescent current in 6 diodes of D1 under the light illumination. 306 solar cells in D2 can ensure the photo-current induced by D1 be amplified 200 times. The output stimulating current is controlled by the M3 with the control signal from power control unit. The amplified current will be sent out for stimulating the retina tissue via the in-pixel electrode if the block is activated. When one block is activated, four pixels in this block receive the power from the parallel solar cells of all the blocks while the pixels in the other blocks consume almost no power because their output paths are cut off. Therefore, the output stimulating current will be approximately three times of the conventional MPA design.

In this work, about five thousand solar cells are connected parallel as the on-chip solar cell power supply. Four blocks are activated in turn that power wasted in refractory period is saved to be added to another blocks for more effective stimulation. The simulation results also show the power efficiency is elevated by the divisional power supply system.

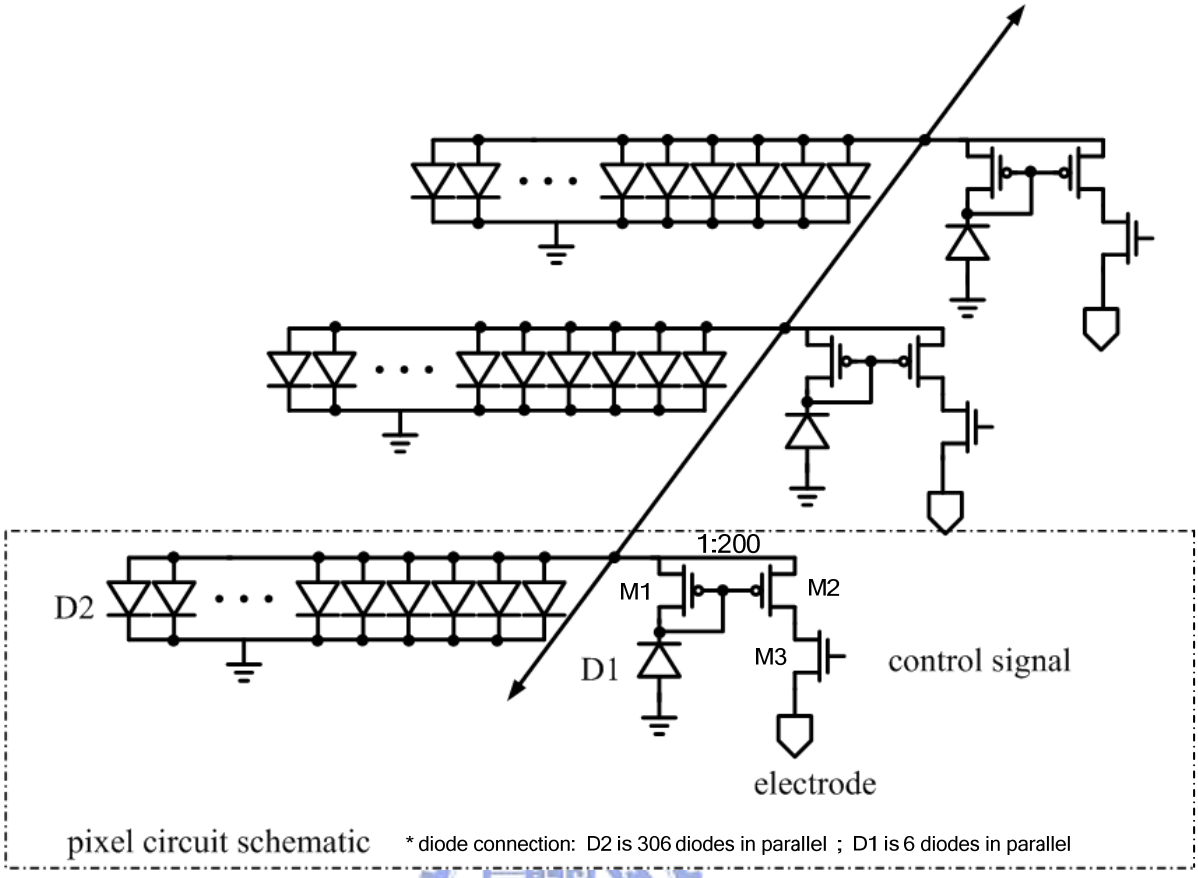


Figure 4.8. The schematic of pixel circuit and array connection. The output electrode is controlled by the NMOS switch with the control signal from power control unit.

4.3 SIMULATION RESULTS AND LAYOUT DESCRIPTION

4.3.1 Simulation results

The simulation model of each photodiode in the circuit is established based on the measurement results shown in the previous section. The simulation model is shown in Fig. 4.9. E1 is the voltage-control voltage source and F1 is the current-control current source, which present two kinds of characteristic of the photodiode: current source and passive component. The photodiode will operate in 4th quadrant of I-V characteristic curve as a solar cell power supply while illumination, and operate in 3rd quadrant as a photo-sensor. The magnitude of the photocurrent Iph in the model is chosen according to the measurement results of the testkey.

The photocurrent is assumed to be proportional to the area of the diode. All simulation results are based on device models of 0.18μm CMOS technology. We simulate two different ambient illuminations of 2.04mW/cm^2 light intensity and 3.6mW/cm^2 light intensity. Photocurrent of D1 and D2 in Fig. 3 are 0.5nA and 1nA per each photodiode under two different ambient illuminations. The transient simulation results of the ring oscillator, two synchronous square-wave signals with the half and quarter clock frequency and control signals under different ambient illumination are shown in Fig. 4.10, 4.11, 4.12 and 4.14. The

simulation results of the output stimulating current are shown in Fig. 4.14 and 4.15. The time interval between neighboring activation is less than 3ms and output stimulating current is about 580nA, 1uA per pixel. As shown in the figure above, the stimulating frequency is varying with the light strength of illumination because the oscillating frequency of ring oscillator in clock generator is controlled by the photocurrent which is almost in proportion of the strength of illumination. Under the high intensity illumination, the time interval between neighboring activation will much less than refractory period. Therefore the stimulation is the waste of the power during the refractory period, but this retinal chip still save some waste power consumption and enhances the power efficiency in comparison with the conventional retinal chip. The whole chip power consumption is 1.1μW including 0.1μW from the control unit under 2.04mW/cm^2 illumination light intensity and 1.6μW including 0.2μW from the control unit under 3.6mW/cm^2 illumination light intensity. The estimated output power of the conventional MPA design with the same area as the proposed chip including pixel array and control unit is 1.2μW which can produce 190nA output current per pixel under 2.04mW/cm^2 illumination light intensity. The total power is slightly greater than this work is due to some layout area is used to realize the power control unit and pixel circuit in this work. The output stimulating current is in proportion to the photodiode area in each pixel which has same area as this work. Therefore, a three time output stimulating current is achieved in the proposed chip.

4.3.2 Layout description

The layout of the whole chip is shown in Fig. 4.16. The layout methodology of the solar cell is a key issue of this retinal chip design as shown in previous section. In order to keep the p-substrate floating, all the NMOS in this retinal chip is located in the deep N-well. With the twin-well technology, the P-pick up (body) of the NMOS can connect to the P-well within the deep N-well as shown in top block of Fig.2.12. The floating p-substrate can ensure the performance of the solar cell and preventing the current leakage by the parasitic lateral BJT. In addition to the leakage problem, there is a silicide layer procedure, which will result in serious photoelectric effect problem of the retinal chip, in the tsmc CMOS 0.18μm technology. A silicide is a compound that has silicon with more electropositive elements, such as titanium silicide ($TiSi_2$). The problem is that the light penetrability of the silicide is very low. Therefore the Incident light of both the solar cells and photodiodes is insufficient to provide the supply power and photocurrent. The silicide blocking procedure is required to prevent the light penetrability problem in this retinal chip. the layout of individual solar cell and photodiode is alnoe with the RPO layer (SAB layer in umc technology) to block the silicide on the diffusion region and avoid the efficiency loss in the photoelectric effect.

There are three main blocks in proposed retinal chip. First, the power control unit, which can produce the quadrature control signals for the retinal chip, is shown in Fig. 4.17. The power control unit's layout dimension is 600μm x 120μm which almost equal to the area of three pixels. Each logic component in both D flip-flop and combinational logic circuit is

powered by six solar cells individually. Therefore the power consumption of each logic component won't interfere with each other. Second, the pixel array with four by four resolutions, which mimic the photo-receptor cell of the retina, can generate the stimulus for retina according to the incident light strength as show in Fig. 4.18. The layout dimension is 700μm x 700μm and each pixel's size is 170μm x 170μm. There are 306 solar cells and 6 photodiodes in a pixel. The layout methodology of the NMOS in the pixel is as shown in top block of Fig.2.12. The output electrodes are shown as the top block of Fig. 4.16. Third, the testkey which contain testkey of the power control unit, solar with different layout configurations, is shown in Fig. 4.19. There are several characteristics need to be confirmed through theses testkey. For instance, the phototransduction efficiency of solar cell with different layout configuration is one most concerned issue of the solar cell design in CMOS technology which is mentioned in Chapter 2. We need to measure the performance of each part's functionality of the power control unit. Therefore we also design a testkey, which is identical to the power control unit in retinal chip, for the measurement usage that we can obtain the detail information of the power control unit. The retinal chip specification is shown in table IV.

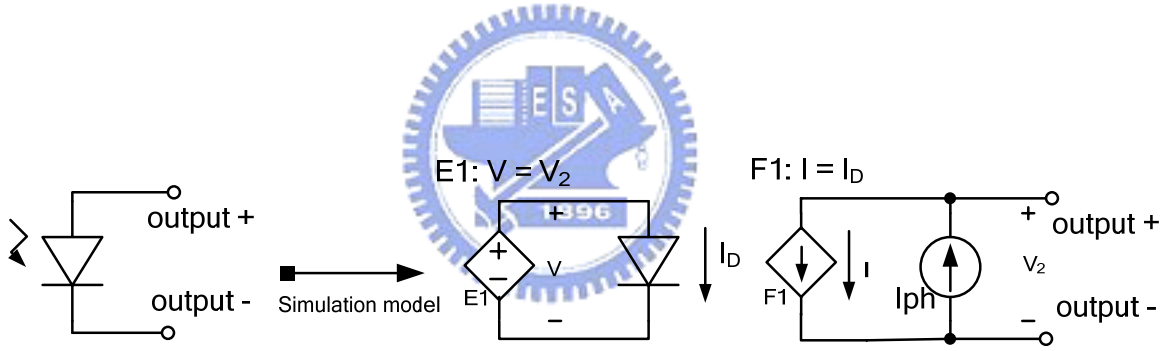


Figure 4.9. the simulation model of each solar cell.

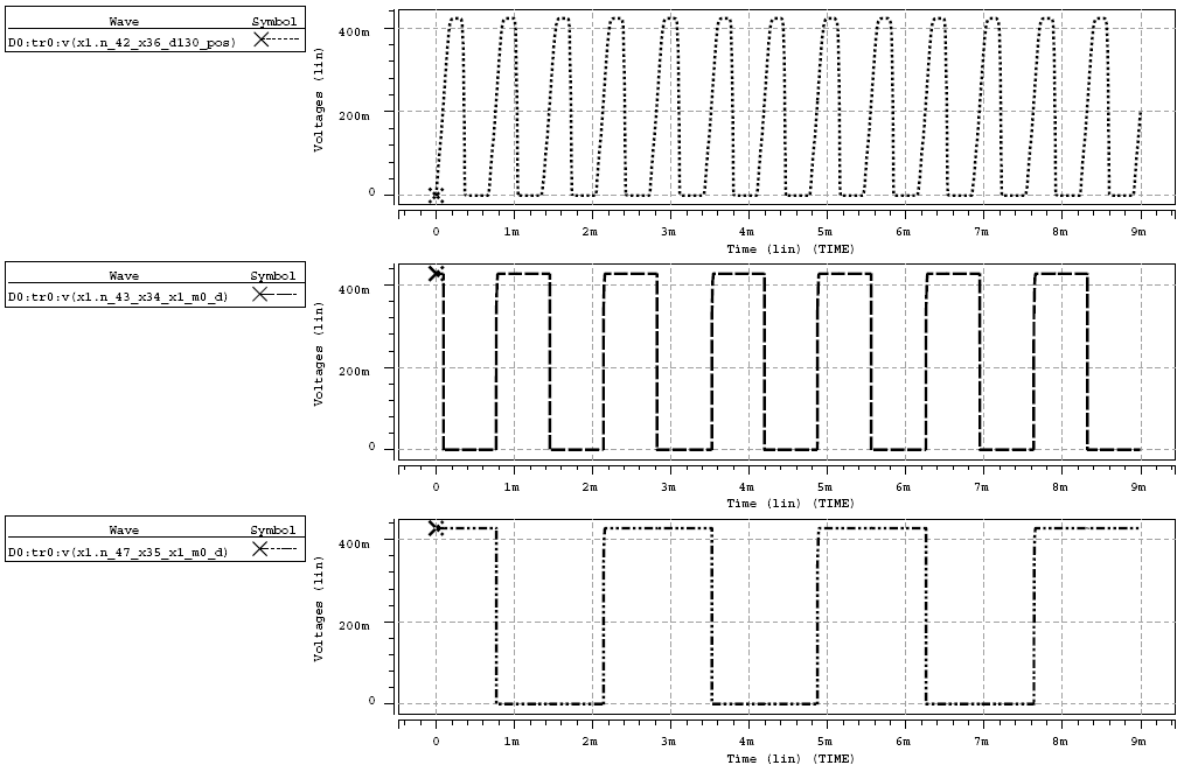


Figure 4.10. The simulation results of the clock generator and frequency divider with 0.5nA photocurrent under 2.04mW/cm^2 light intesity.

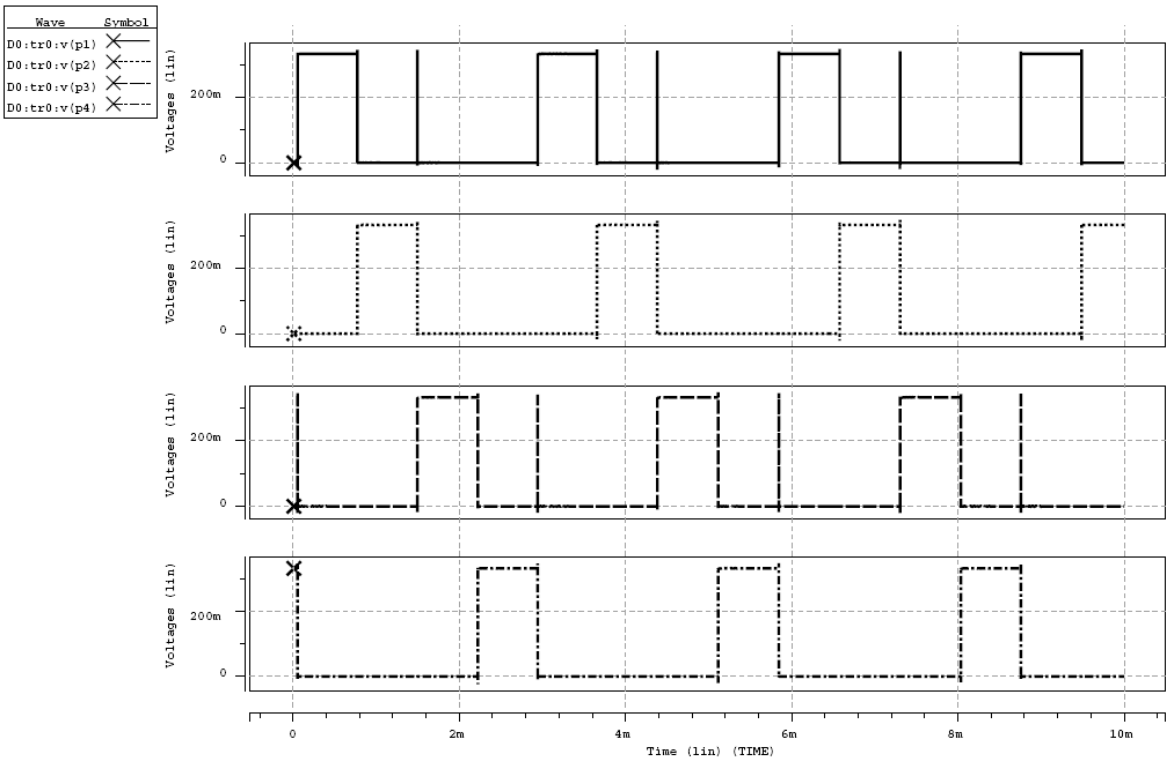


Figure 4.11. The simulation results of the qudrature phase control signals with 0.5nA photocurrent under 2.04mW/cm^2 light intesity.

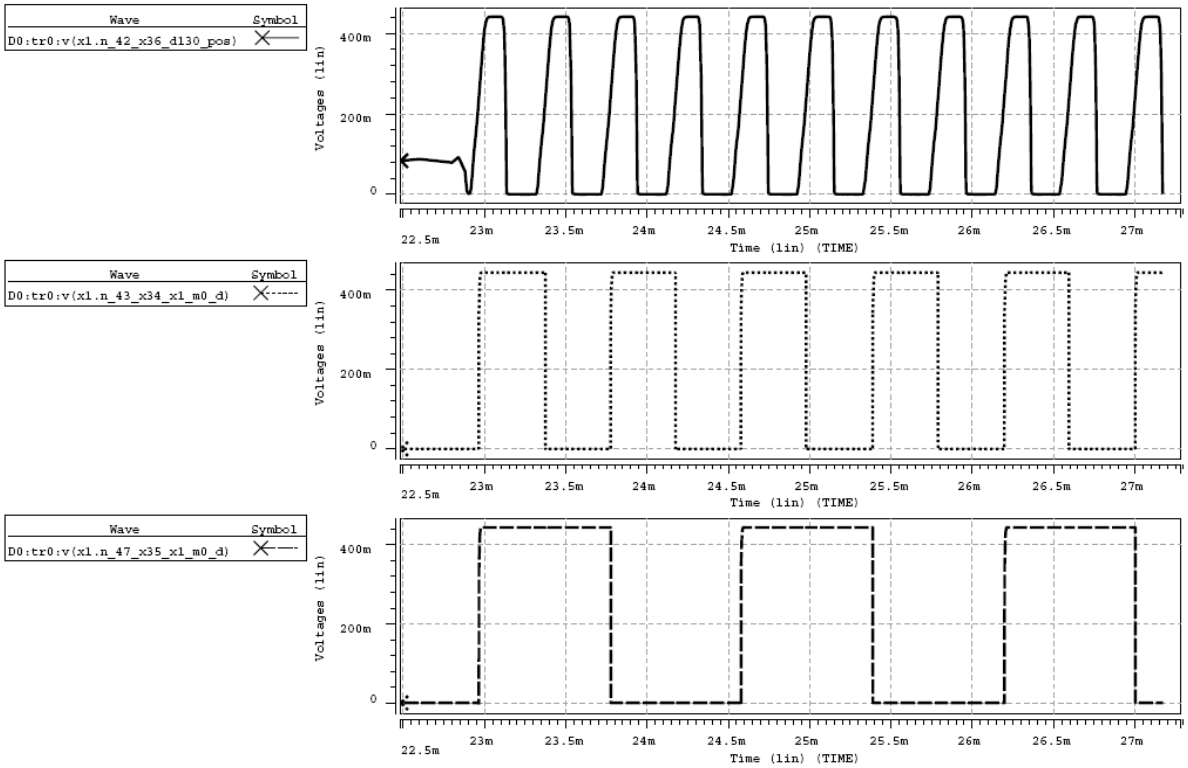


Figure 4.12. The simulation results of the clock generator and frequency divider with 1nA photocurrent under 3.6mW/cm^2 light intesity..

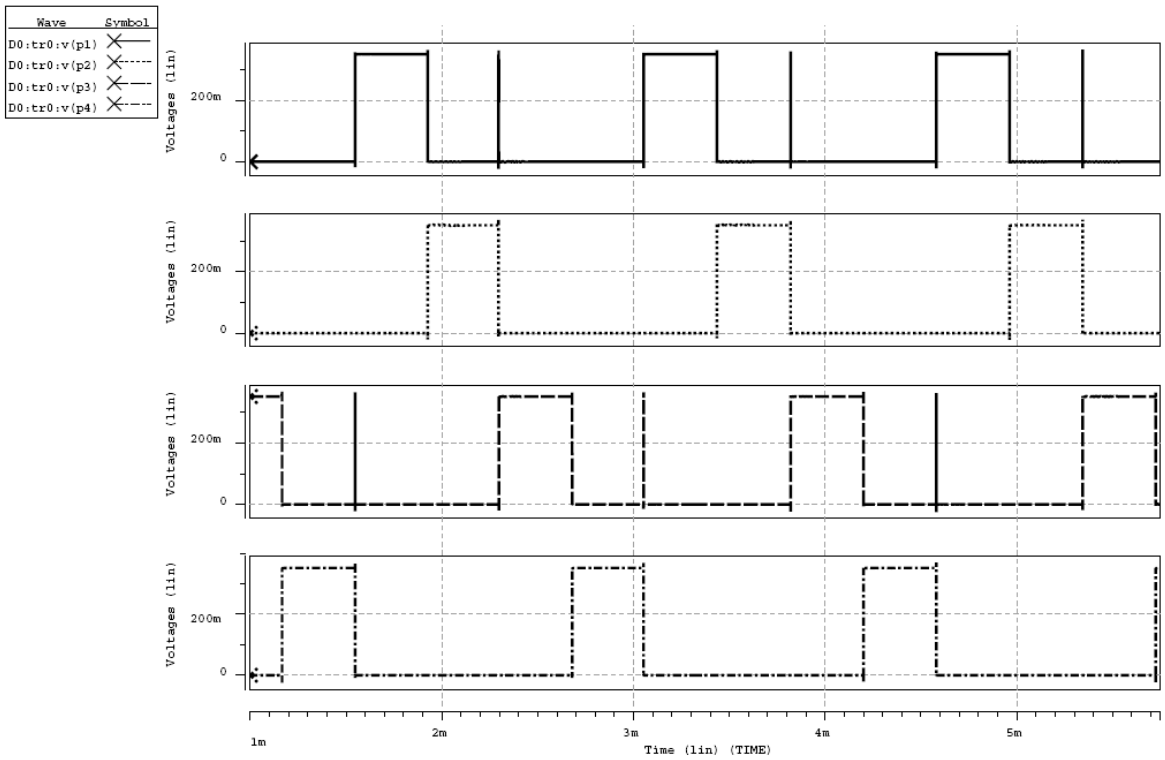


Figure 4.13. The simulation results of the qudrature phase control signals with 1nA photocurrent under 3.6mW/cm^2 light intesity..

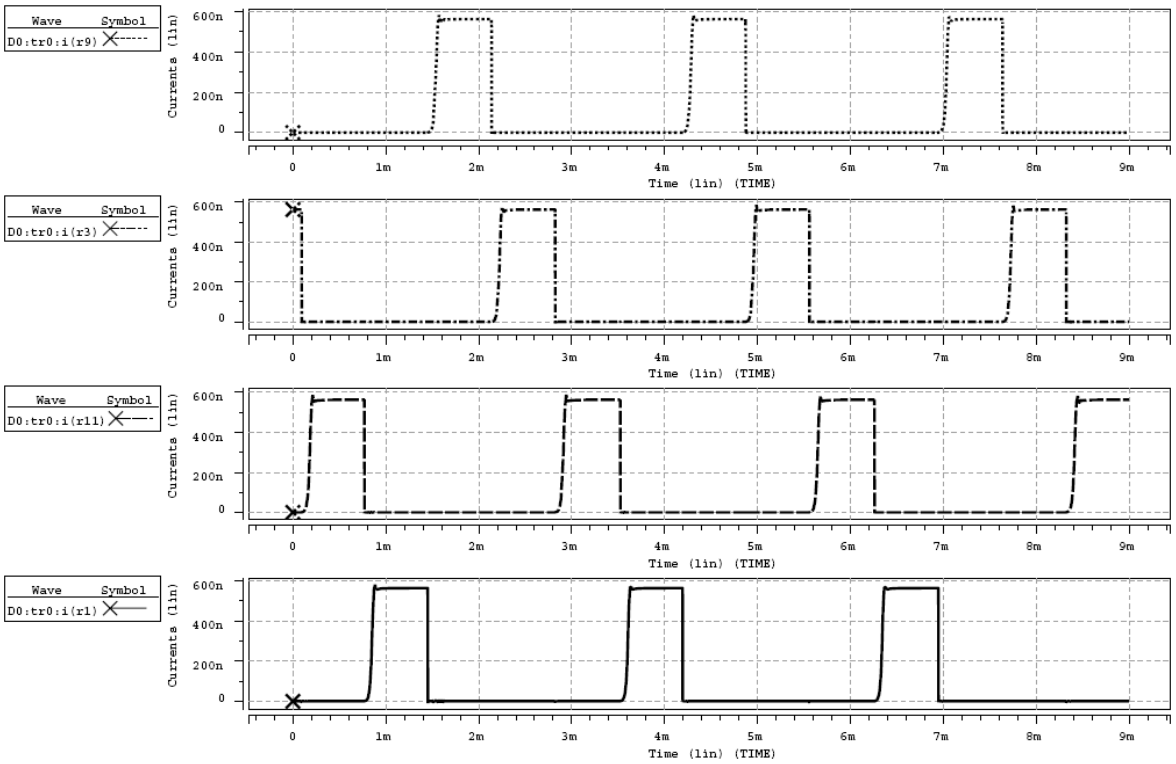


Figure 4.14. The simulation results of the output stimulating current with 0.5nA photocurrent under 2.04mW/cm^2 light intesity. The magnitude of the current is approximately 580nA.

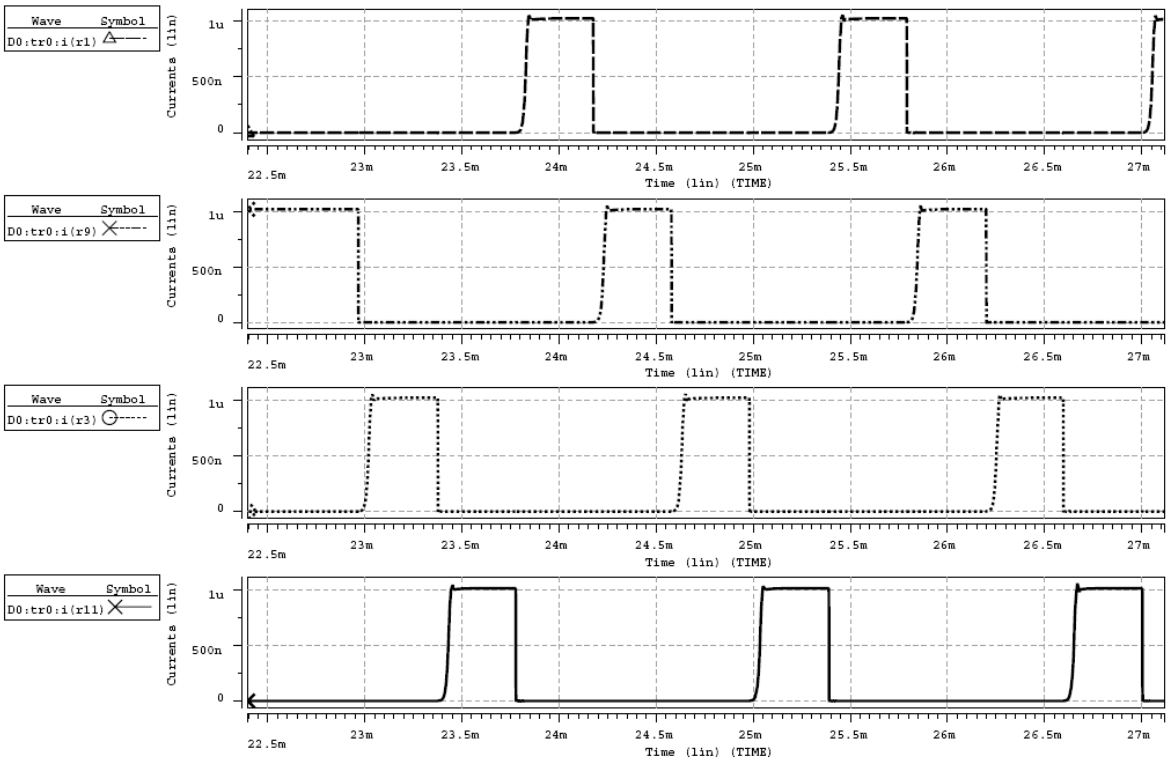


Figure 4.15. The simulation results of the output stimulating current with 1nA photocurrent under 3.6mW/cm^2 light intesity. The magnitude of the current is approximately 1020nA.

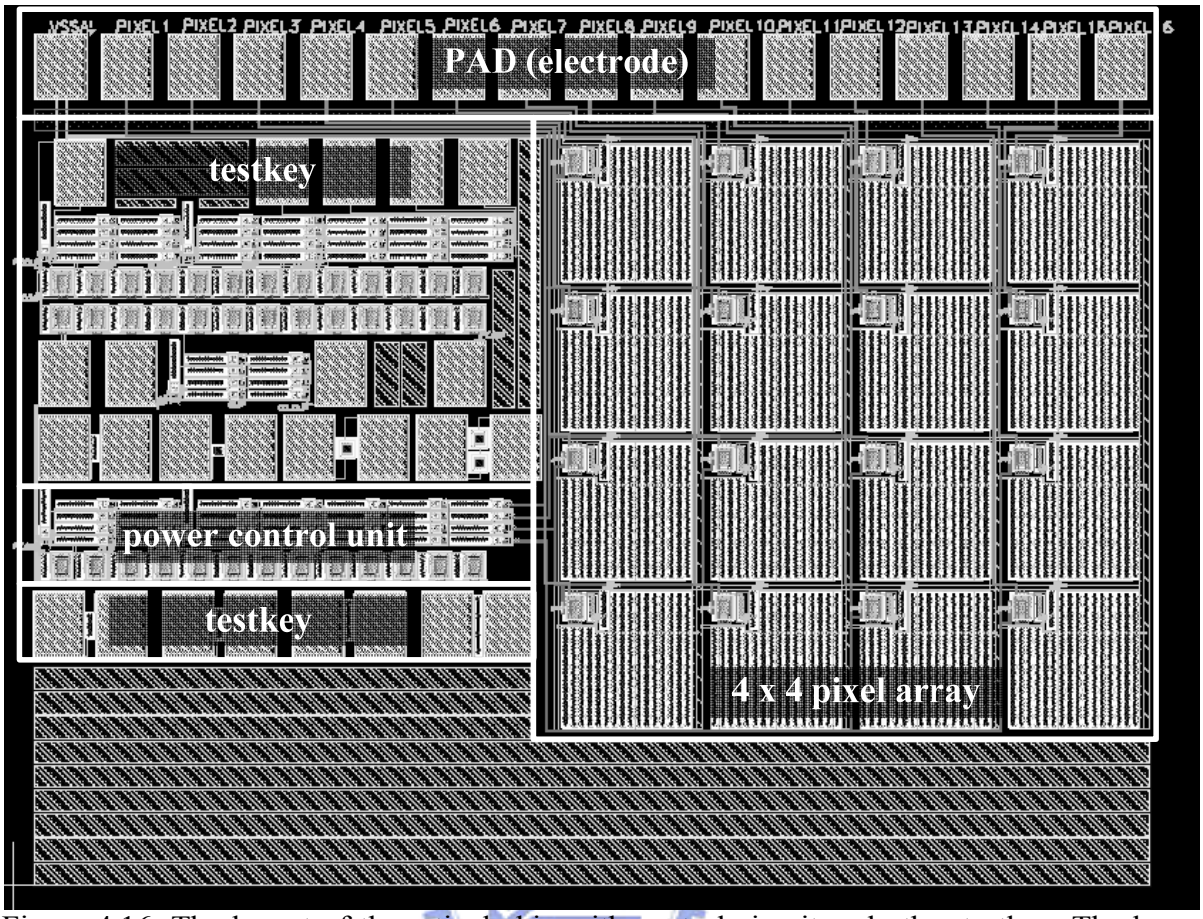


Figure 4.16. The layout of the retinal chip with control circuit and other testkey. The layout dimension is 1400μm x 1000μm.

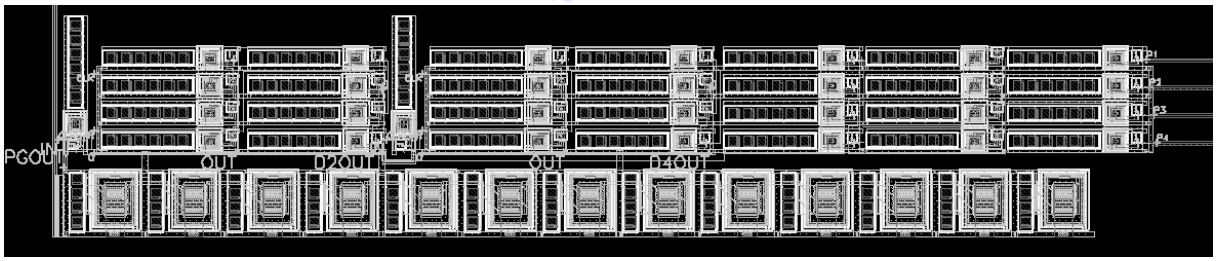


Figure 4.17. The layout of the power control unin. The layout dimension is 600μm x 120μm which almost equal to the area of three pixels.

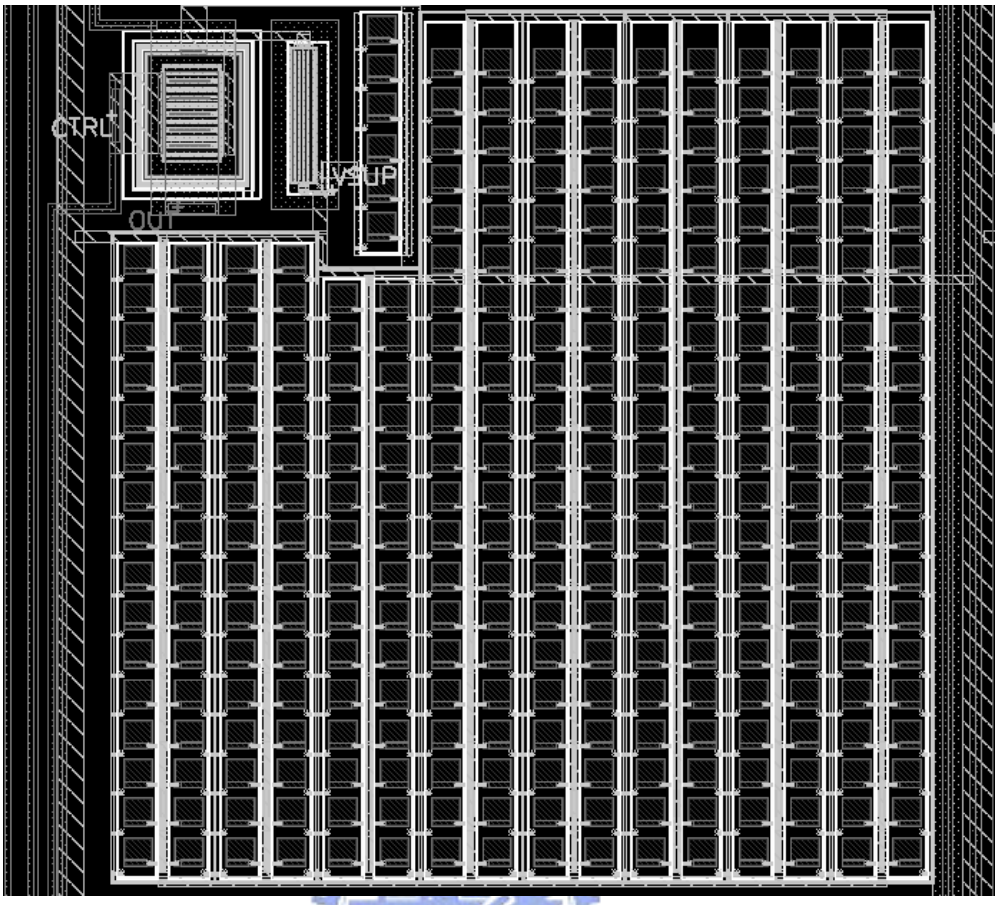


Figure 4.18. The layout of the pixel array. The layout dimension is 700μm x 700μm and each pixel's size is 170μm x 170μm. The output electrodes are shown as the top block of Fig. 4.16.

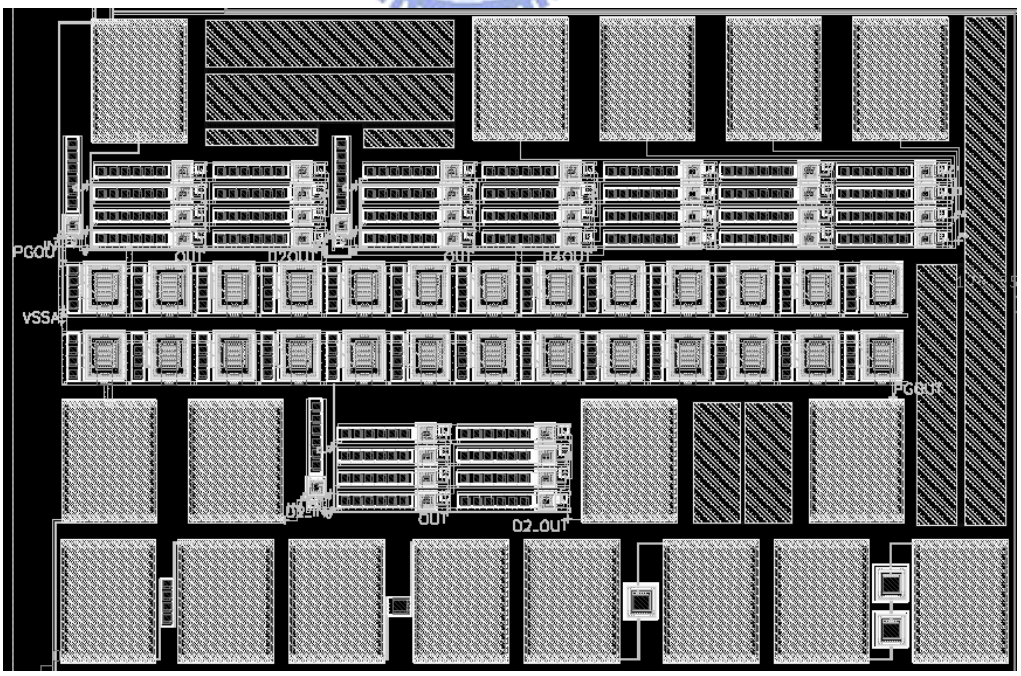


Figure 4.19. The layout of the testkey. Including testkey of power control unit and testkey of solar cells with different layout configuration.

TABLE IV. the specification of the retinal chip

SPECIFICATION	
Power supply	No external power supply
Pixel number	4 x4 cells
Chip dimension	1.4x1.5mm^2
Exposured electrode size	50 x 50 μm^2 (within the pixel)
Pixel area	150 μm x 150 μm
Output stimulating current	900nA (3.60 mW/cm^2) 1.75uA (5.06 mW/cm^2)

4.4 MEASUREMENT RESULTS

Fig.4.20 and 4.21 show the measurement environment of the retina chip. We use the probe station and HP 4156B (parameter meter) to get the I – V curve of the solar cell to ensure the function of the solar cell supply system which has been described in chapter 2. The oscilloscope (TDS 3054) is used to observe the output waveform which is buffered through the unit gain buffer composed of OpAmp with negative feedback.

Fig.4.22 shows the measurement results of the clock generator under varying light intensities. Fig. 4.23 shows the post-layout simulation result of the clock generator with and without output loading (4pF capacitor and 1TΩ resistor) with 1nA photocurrent. Fig. 4.24 shows the comparison between the simulation result and measurement result and the function of the clock generator is verified in this work.

Fig. 4.25 shows the measurement result of the output waveform of power control unit. The output waveform of the power control unit is not as what we expected and the outputs of the pixel array also not provide the divisional output stimulating current due to the fail control signals.

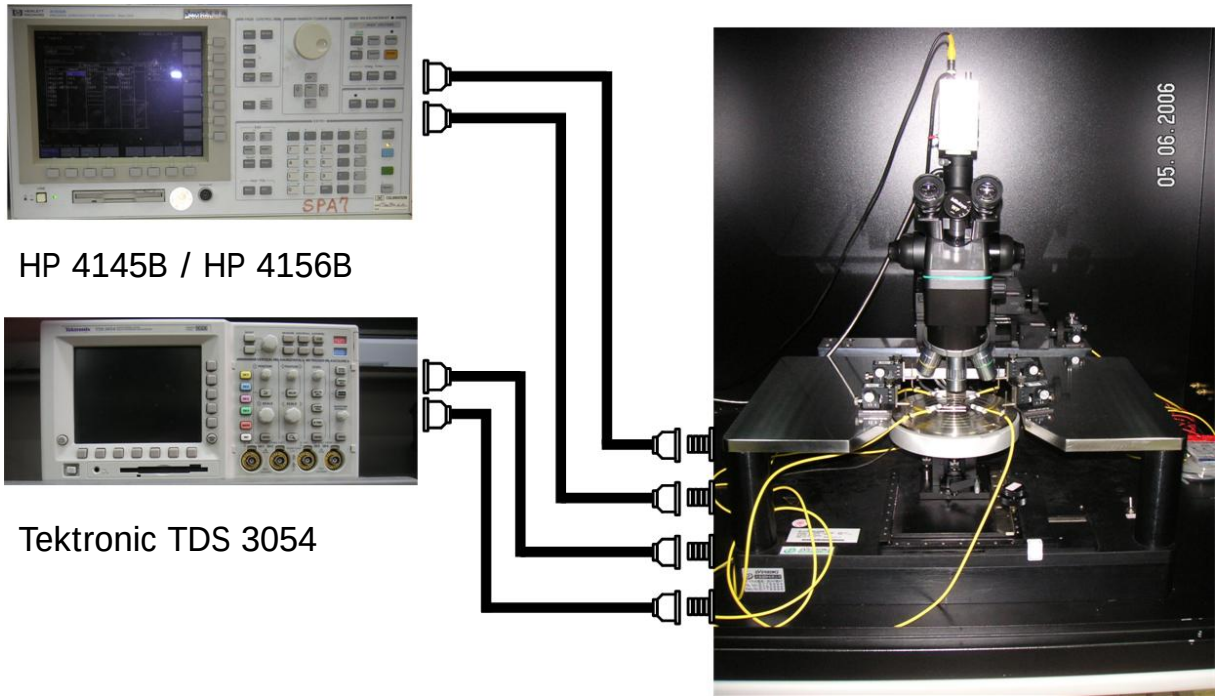
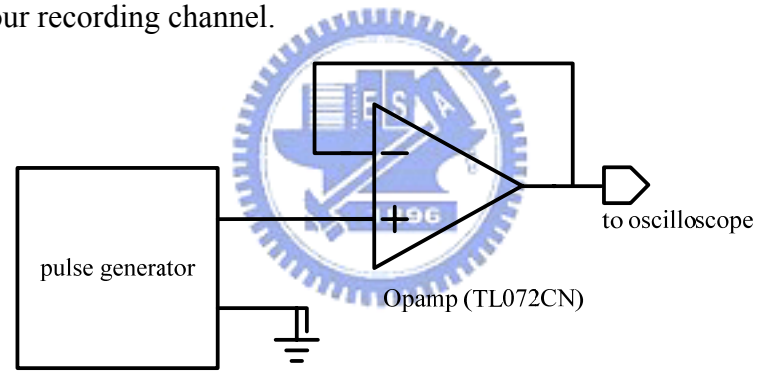


Figure 4.20. the measurement environment of the retinal chip. The right box is the probe station with four recording channel.



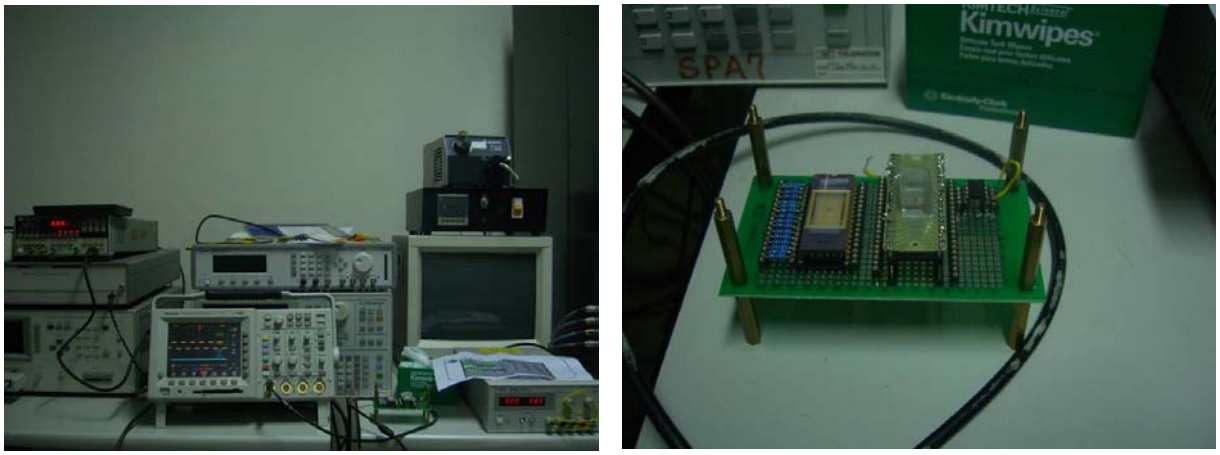


Figure 4.21. the measurement environment of the retinal chip. The top block is the schematic of the external unit gain buffer.

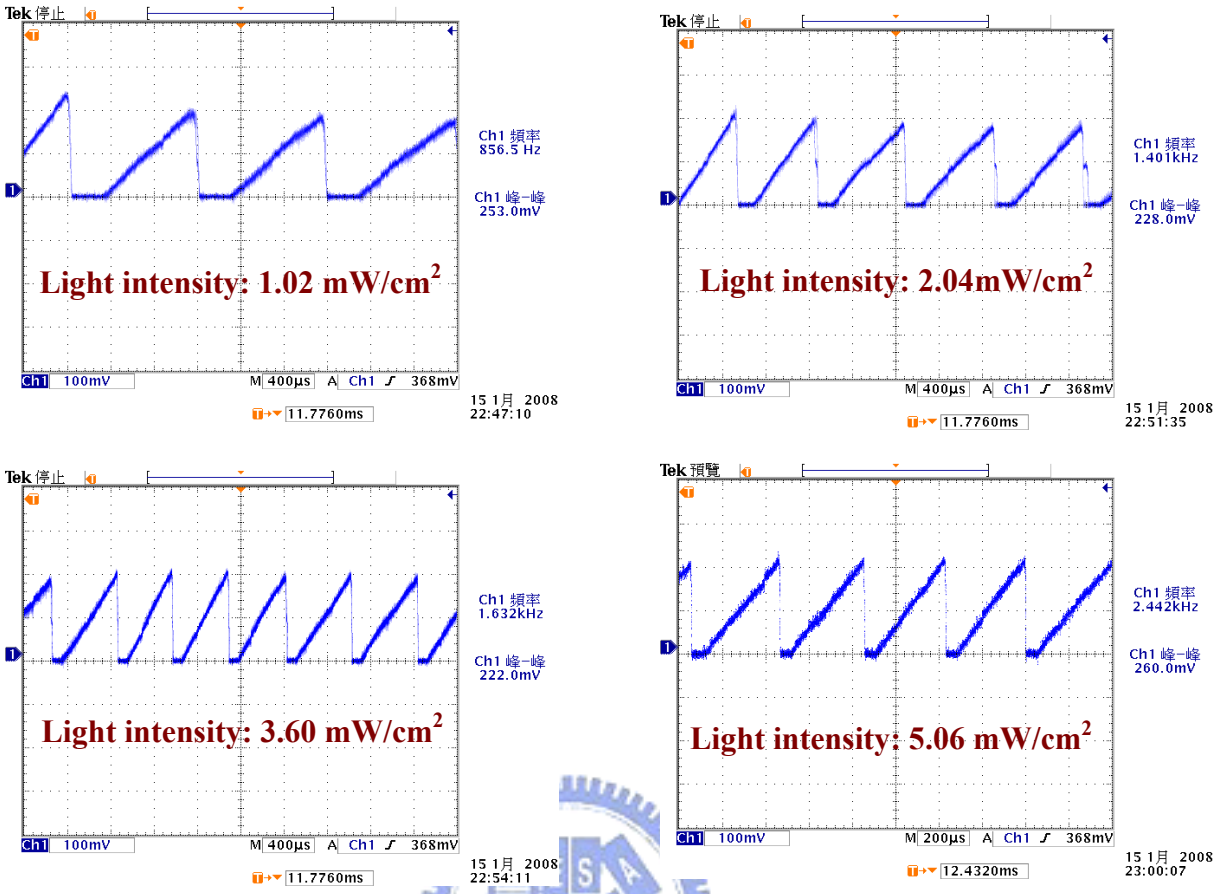


Figure 4.22. measurement results of the clock generator under varying light intensities.

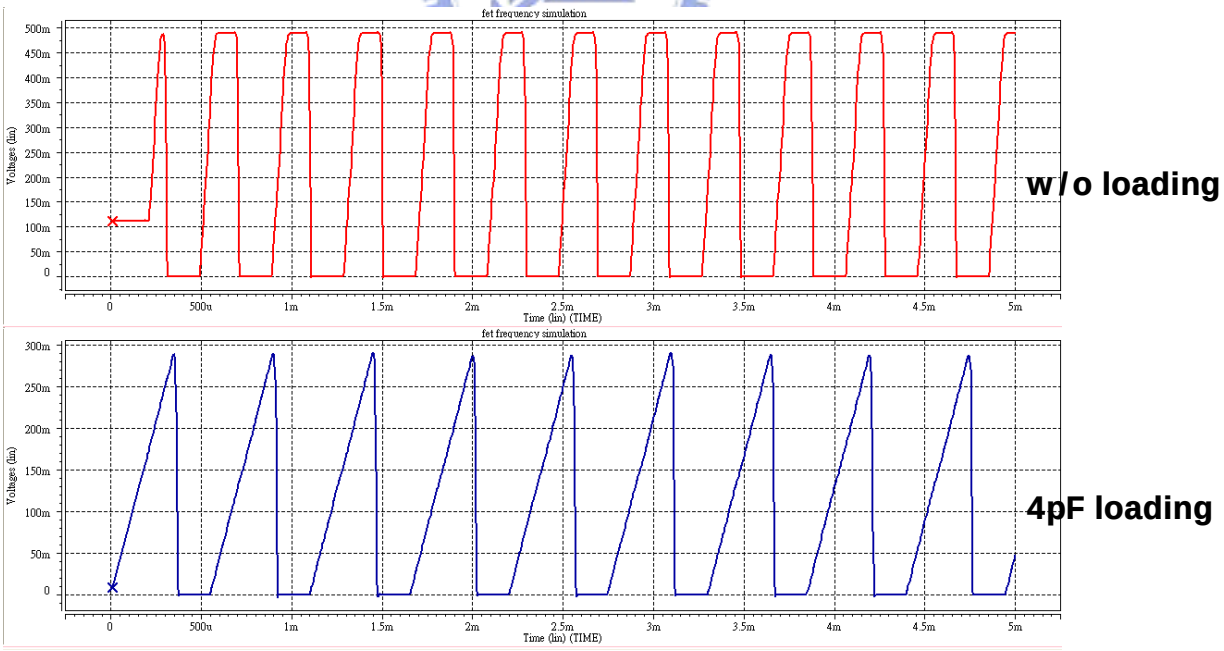


Figure 4.23. the post-layout simulation result of the clock generator with and without output loading (4pF capacitor and 1TΩ resistor) with 1nA photocurrent (3.6mW/cm^2 light intensity).

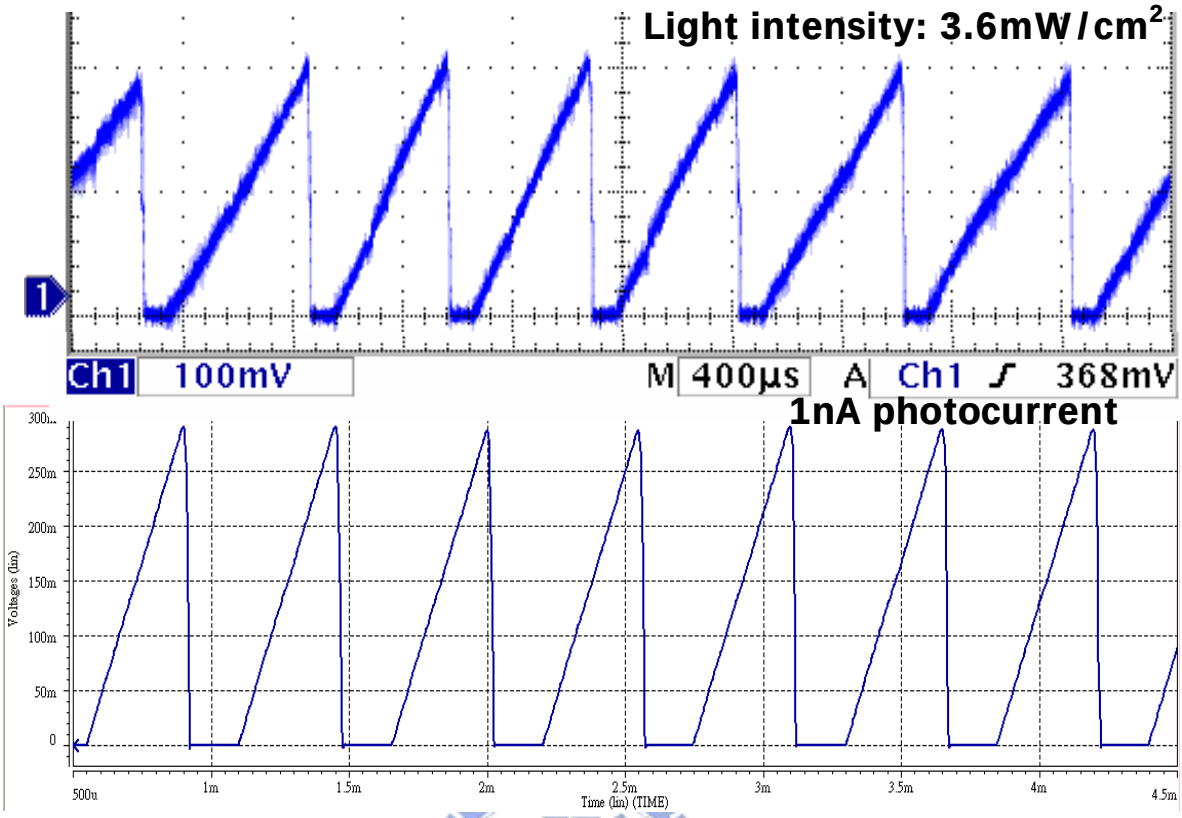


Figure 4.24. the comparison between the simulation result and measurement result with 1nA photocurrent (3.6mW/cm^2 light intensity)

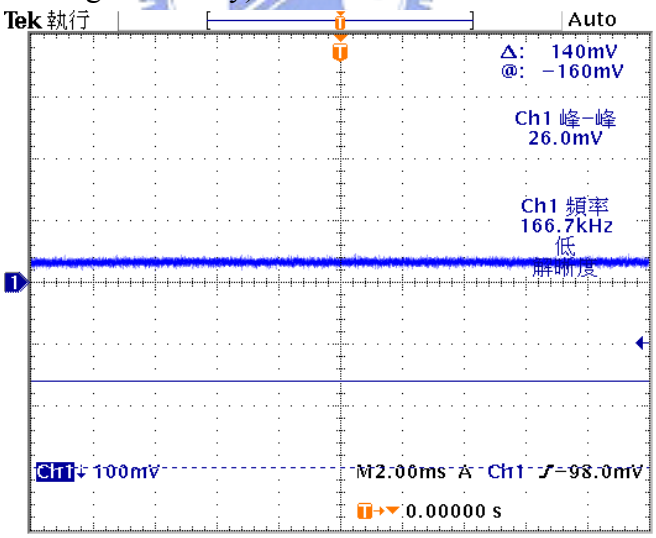


Figure 4.25. the measurement result of the output waveform of power control unit. The output waveform of the power control unit is not as what we expected due to the negligence of the Vt variation in the subthreshold logic design. Therefore the output current of the pixel array also not function properly.

4.5 DISCUSSION

Though the clock generator is designed and verified with only on-chip solar cell supply, there is still a big problem within this clock generator structure: the clock frequency is in proportional to the light intensity. This characteristic will result in the stimulating frequency of the retinal chip is uncertain while the chip is activated to stimulate the retina. As we can see in the Fig. 4.22, the clock frequency varies from 800Hz to 2.5KHz while the light intensity is varying from 1mW/cm2 to 5mW/cm2 which means the stimulating frequency is about 250Hz to 600Hz. With the extrapolation of the measurement data, the 60Hz stimulating frequency will be approximately related to the irradiation intensity of 0.5mW/cm^2. According to the theory of the persistence of vision, the stimulating frequency should greater than 60Hz. As a result, the clock generator which can be used in this experiment should be irradiated with the light which's intensity is greater than 0.5mW.

The Vt, width and length variations have a great effect to the VTC (voltage transfer curve) of the logic gate in the subthreshold logic design and therefore we suspect that the Vt, width and length variations are the major problems to the power control unit. Then we put the proposed circuit under the Monte Carlo simulation with 5% Vt variation and compare it with the measurement result as shown in Fig. 4.26. The VTC of the inverter which powered only by on-chip solar cell in the Monte Carlo simulation with 5% Vt variation is shown in Fig.4.27. The VTC has a large varying range due to the Vt variation which result in the wrong function between each logic gates. Furthermore, the output waveform at each stage in Monte Carlo simulation is shown in Fig. 4.28. We can sure that the problem which result in the power control unit function fail is the Vt variation issue.

The problem of the Vt variation in the subthreshold logic design is one of most popular research issue in the modern EECS. The specification of the performance in this work is relatively low compared with other subthreshold logic design. Therefore, the solution to this problem is seemed to be relatively simple. The I_D in the subthreshold region can be describing as:

$$I_D = \frac{W}{L} \bullet I_t \bullet e^{\frac{V_{GS}-V_t}{nV_T}} \bullet (1 - e^{-\frac{V_{DS}}{V_T}})$$

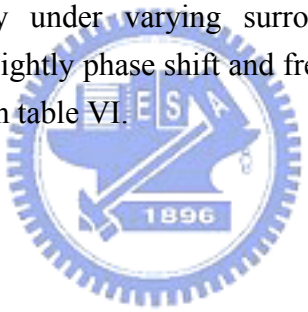
,which the $I_t \rightarrow D_{nnpo}$ which depends on process parameters (e.g., 20nA) and the deviation of Vt variation is:

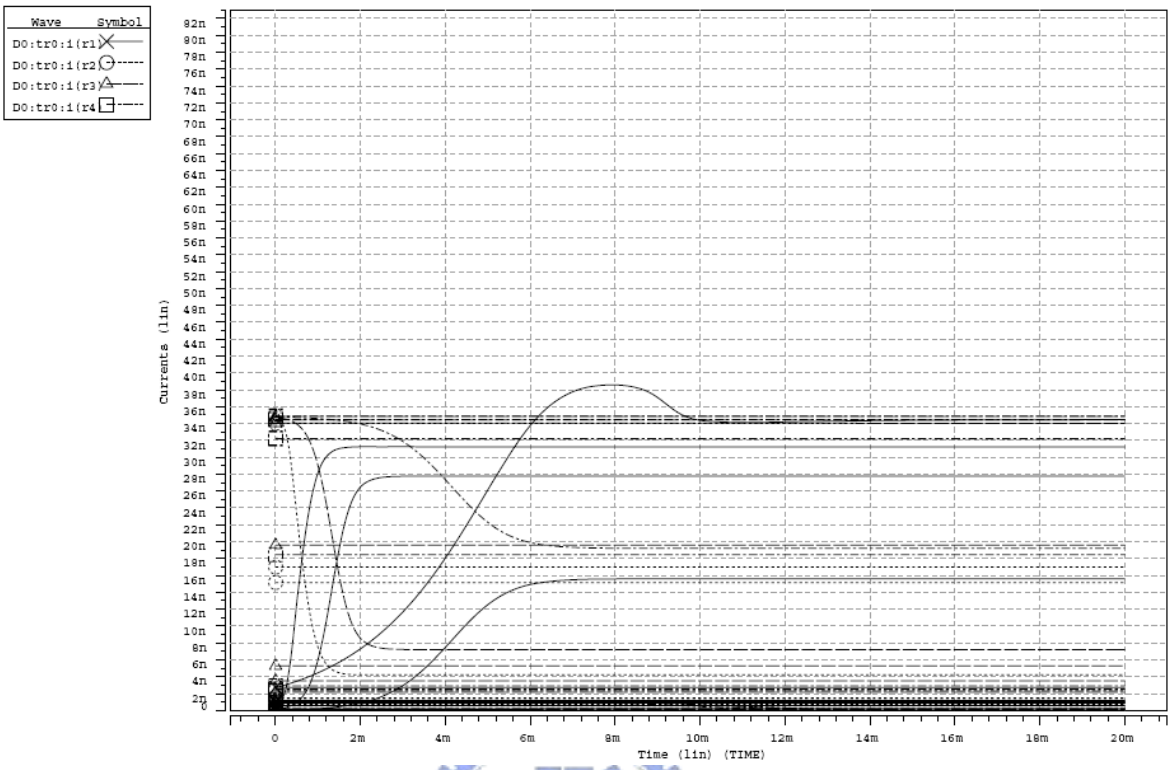
$$\sigma_{V_t} = \frac{f_{V_t}}{\sqrt{W \bullet L}}$$

, which f_{Vt} is a constant describing the influence of the area and periphery fluctuation. [51] Therefore, we carry on following two methods to improve the Vt variation in this modification design. 1. Improve the immunity to Vt variation (mismatch) through increasing the width and length of each logic which is almost minimum size in the previous design. 2. Reorganize the

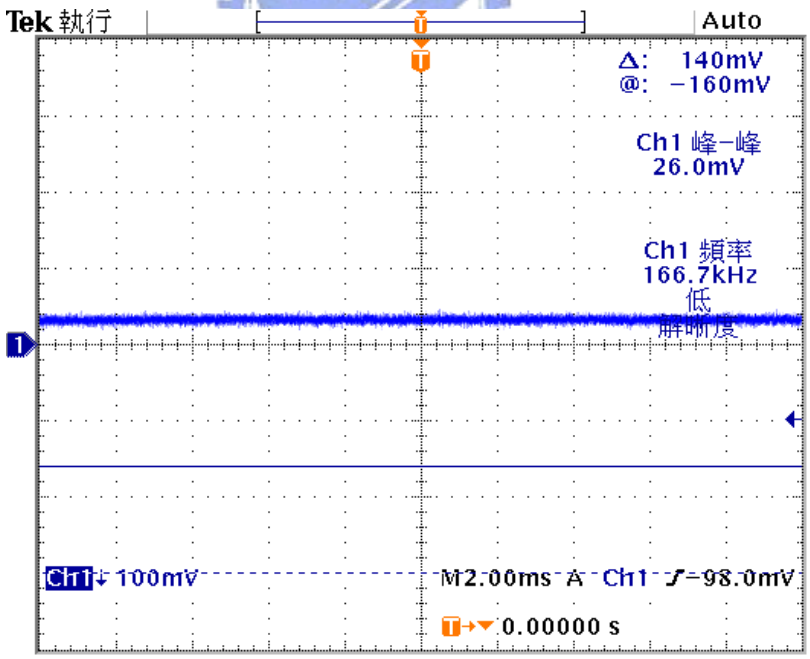
layout floor plan to put all MOS which belonged to related logic gates together which can avoid the large Vt variation on the VTC form gate to gate. The size of each MOS in the modified design is shown in table V. Fig. 4.29 shows the VTC of the modified inverter which powered only by on-chip solar cell in the Monte Carlo simulation with 5% Vt variation and Fig. 4.30 shows the output waveform at each stage in Monte Carlo simulation with 5% Vt variation. The Monte Carlo simulation results of the pixel array outputs are shown in Fig. 4.31 which we can see that the mismatch problem is greatly reduced compared with Fig. 4.26.

The modified chip layout view is shown in Fig. 4.32 and the layout and schematic of the testkey of power control unit which is for measurement usage is shown in Fig. 4.33. The output of the power control unit testkey is buffered by two on-chip inverter buffers which are supplied by external power supply. The post-layout simulations of the modified retina chip with 3.6mW/cm^2 and 5.06mW/cm^2 illumination (1nA and 2nA photocurrent) are shown in Fig. 4.34 and 4.35 and the output waveform of the power control unit testkey is shown in Fig. 4.36. The time interval between neighboring activation is less than 3ms and output stimulating current is about 844nA, 1.72uA per pixel. Also the temperature variation simulation of the retinal chip is shown in Fig. 4.37. The figure shows that the divisional output stimulating current still function properly under varying surrounding temperature and the output stimulating current only has a slightly phase shift and frequency variation. The specification of modified retinal chip is shown in table VI.





(A)



(B)

Figure 4.26.. Monte Carlo simulation with 5% Vt variation and compare it with the measurement result. (A) Simulation results with 5% Vt variation and 6KΩ output loading. (B) measurement results with 6 KΩ output loading under 3.6mW/cm^2 light intensity.

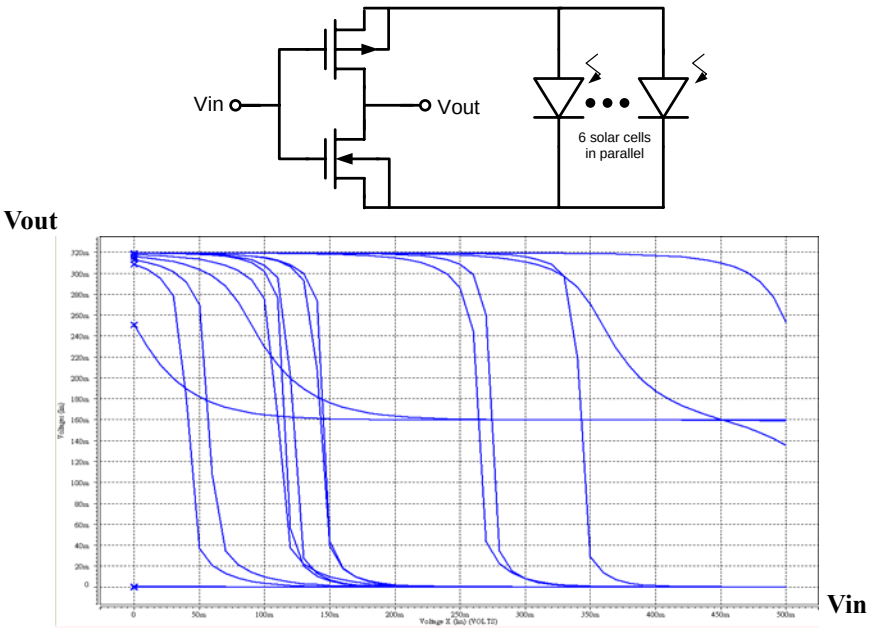


Figure 4.27. The VTC (voltage transfer curve) of the inverter which powered only by on-chip solar cell in the Monte Carlo simulation with 5% Vt variation.

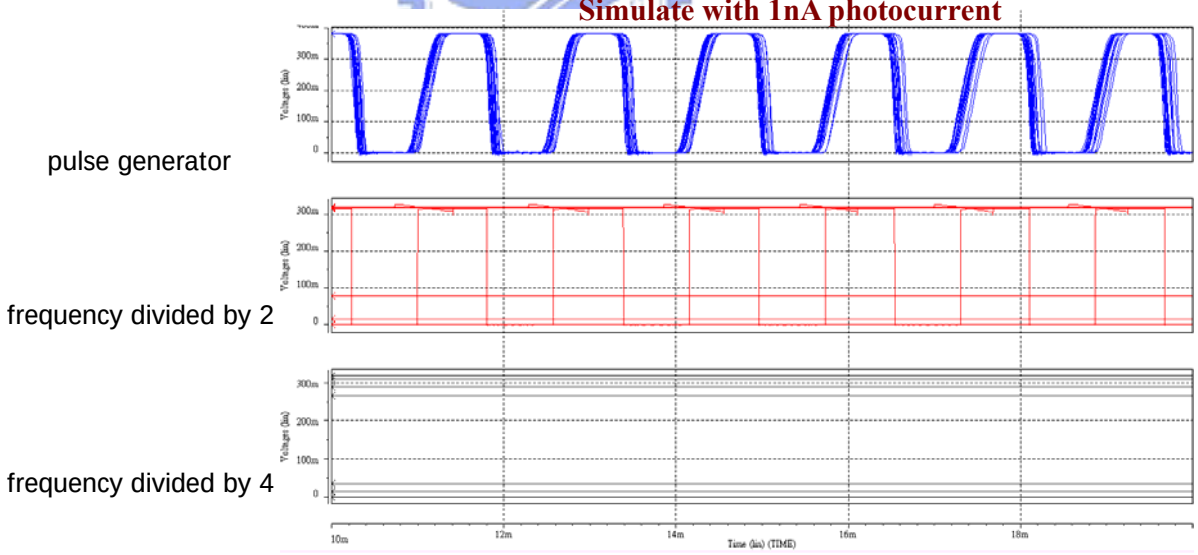


Figure 4.28. the output waveform at each stage in Monte Carlo simulation with 5% Vt variation.

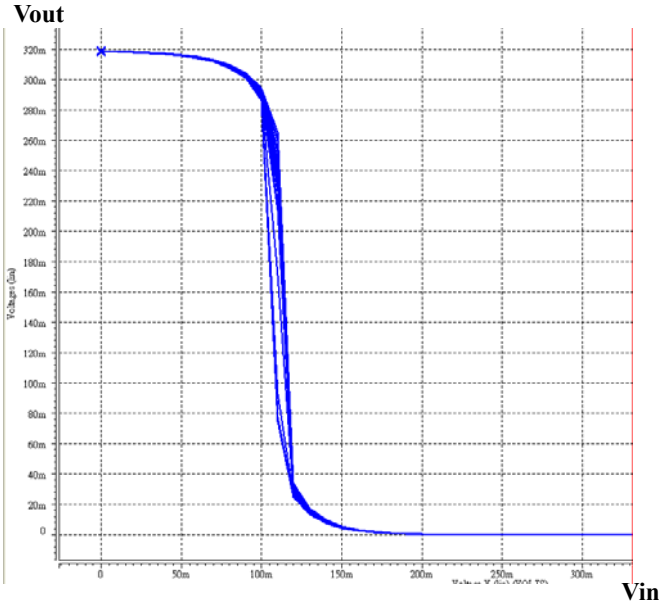


Figure 4.29. the VTC of the modified inverter which powered only by on-chip solar cell in the Monte Carlo simulation with 5% Vt variation..

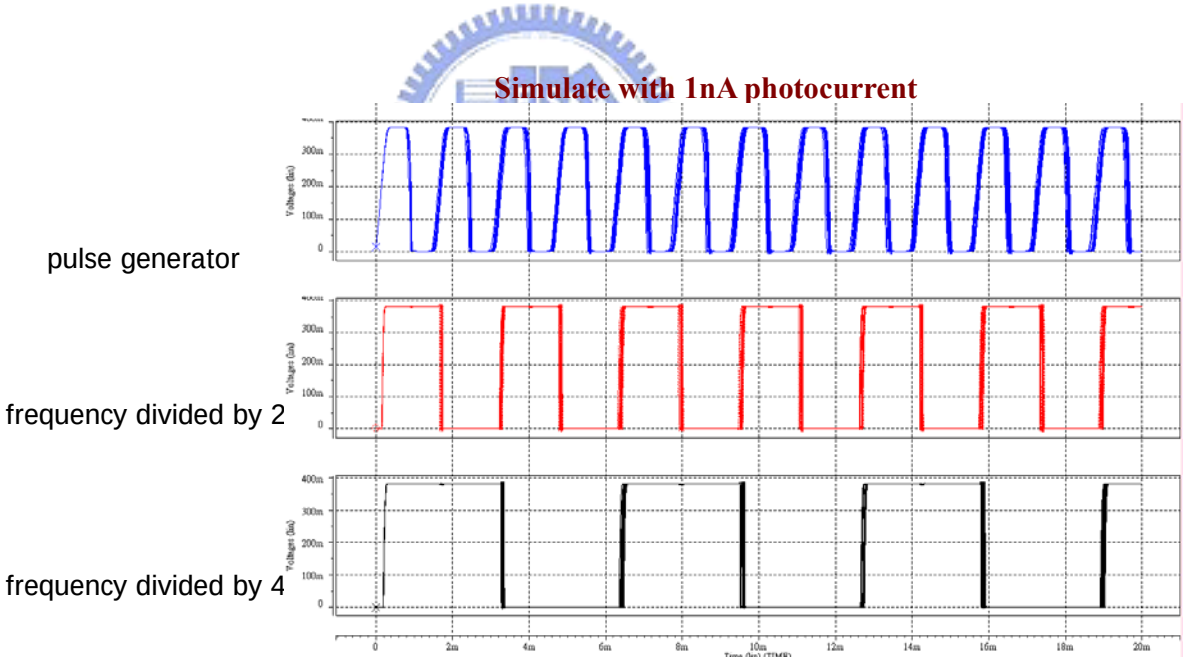


Figure 4.30. the output waveform at each stage in Monte Carlo simulation with 5% Vt variation.

Output loading: R = 6KΩ , C =20pF

Photocurrent = 1 nA (Monte Carlo)

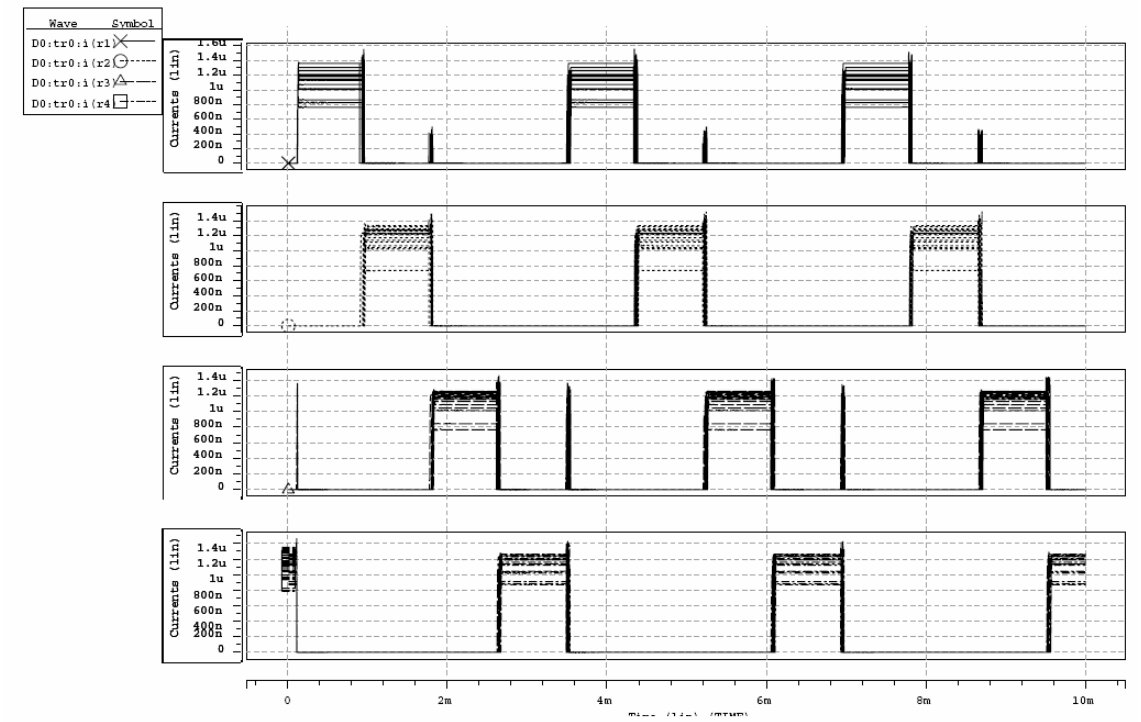


Figure 4.31. The Monte Carlo simulation results of the pixel array outputs under 3.6mW/cm^2 light intensity with 5% Vt variation.

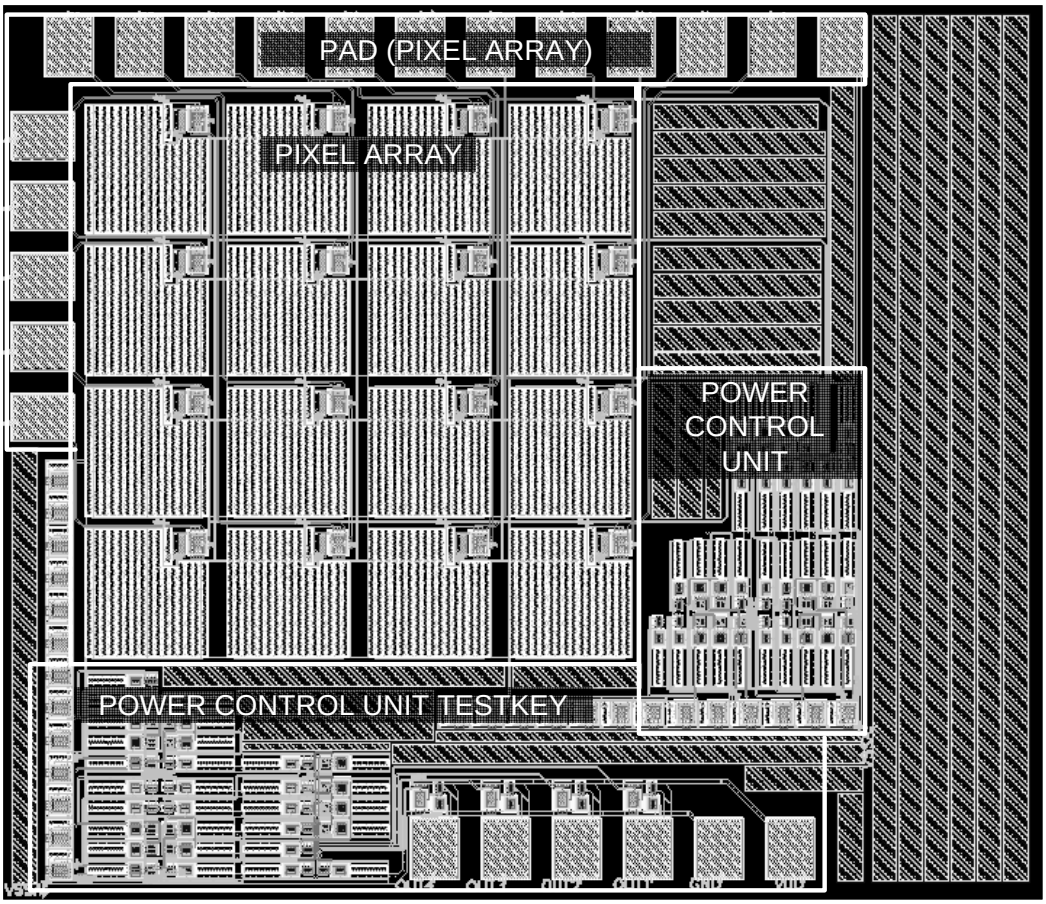


Figure 4.32. The modified retinal chip layout view.

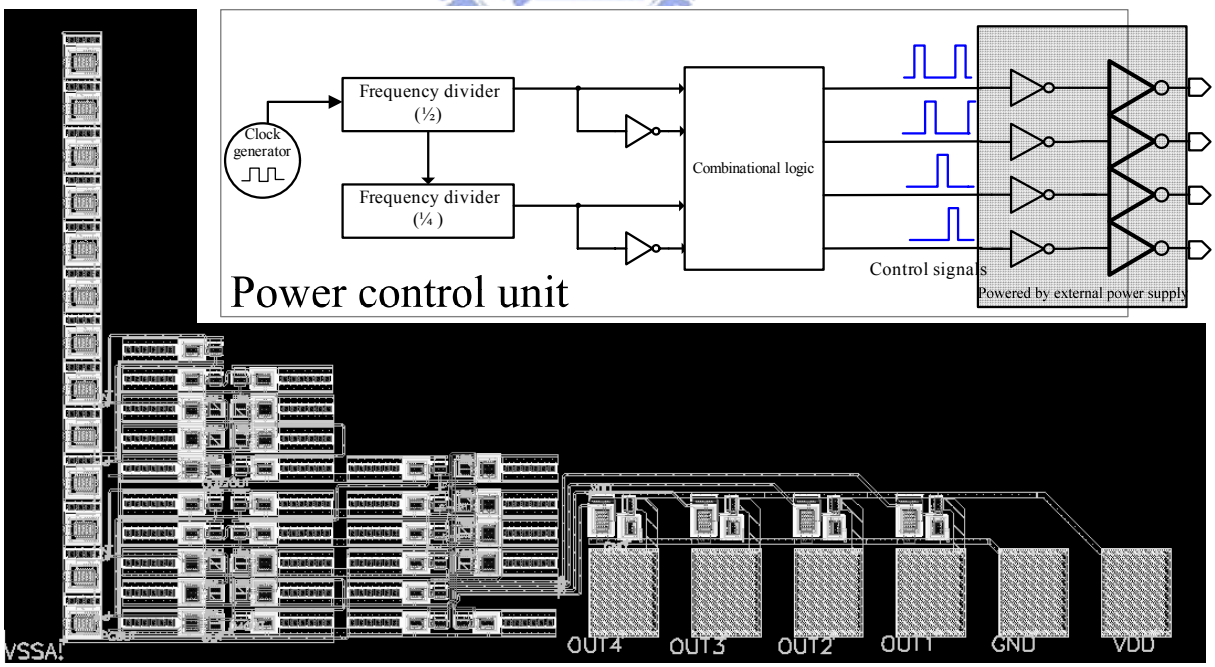


Figure 4.33. the layout and schematic of the testkey of power control unit which is for measurement usage.

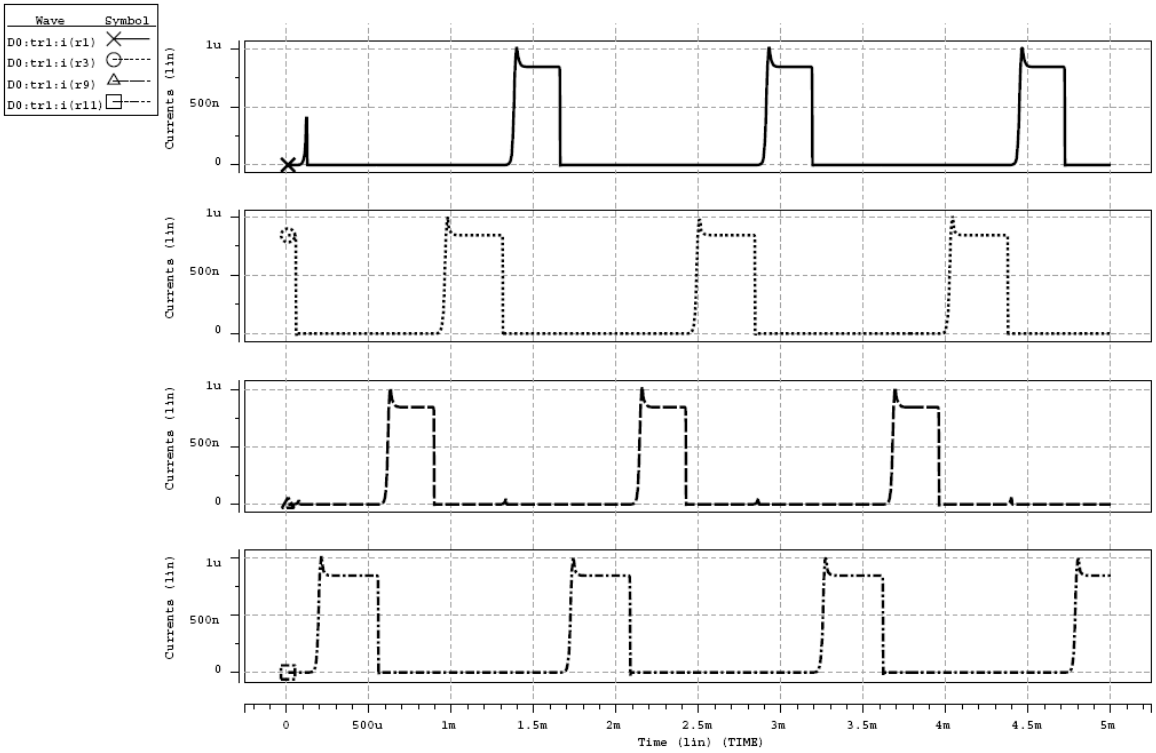


Figure 4.34. The post-layout simulations of the modified retina chip with 3.6mW/cm^2 light intensity (1nA photocurrent). Each row represent a pixel's current output.

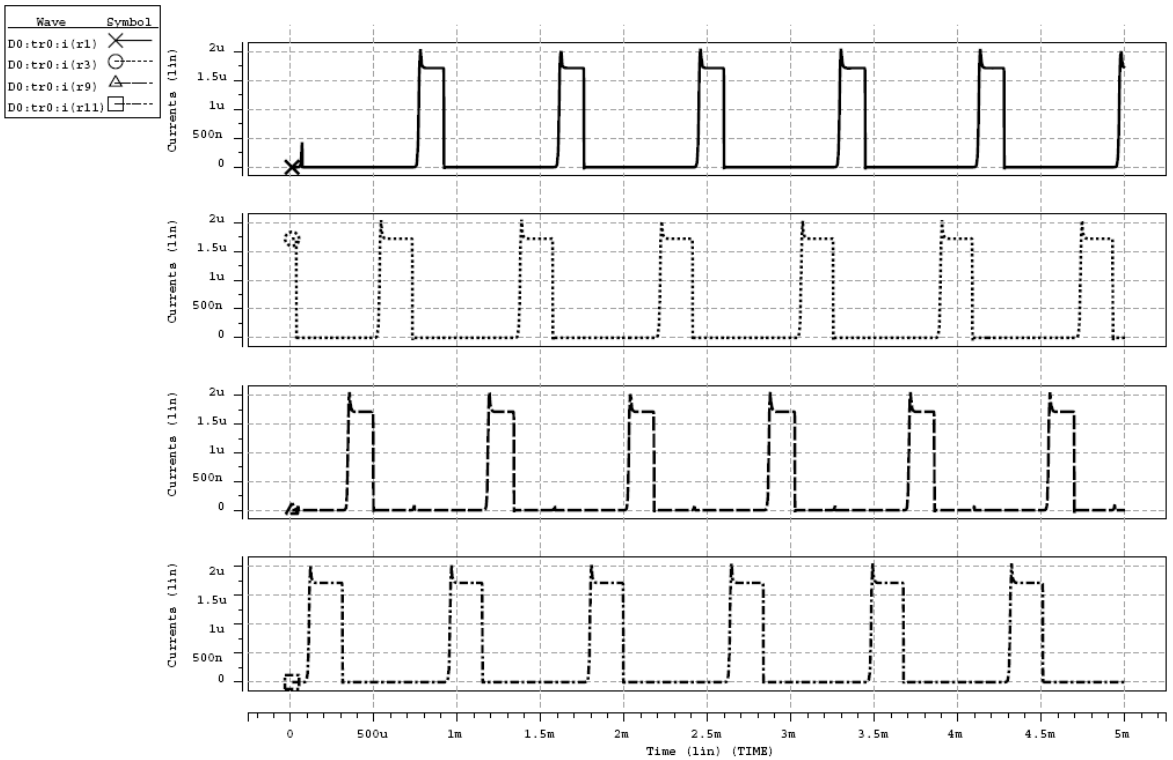


Figure 4.35. The post-layout simulations of the modified retina chip with 5.06mW/cm^2 light intensity (2nA photocurrent). Each row represent a pixel's current output.

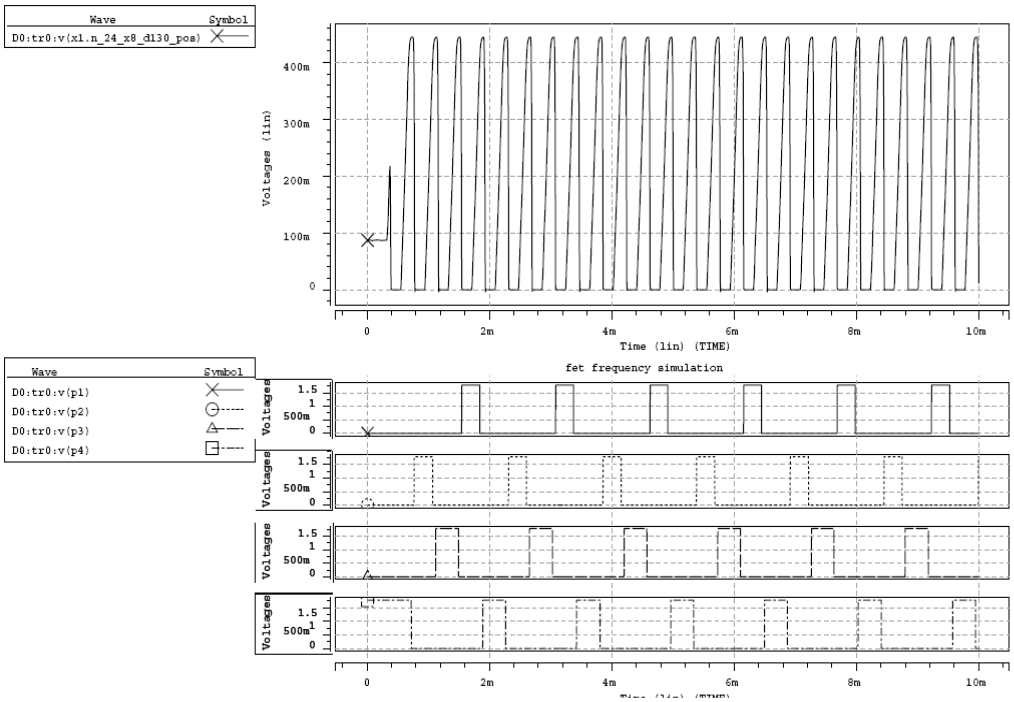


Figure 4.36. the post-layout simulation waveform of clock generator and the power control signals. Because the external powered buffer, the power control signal's voltage level can reach approximately 1.8 V.

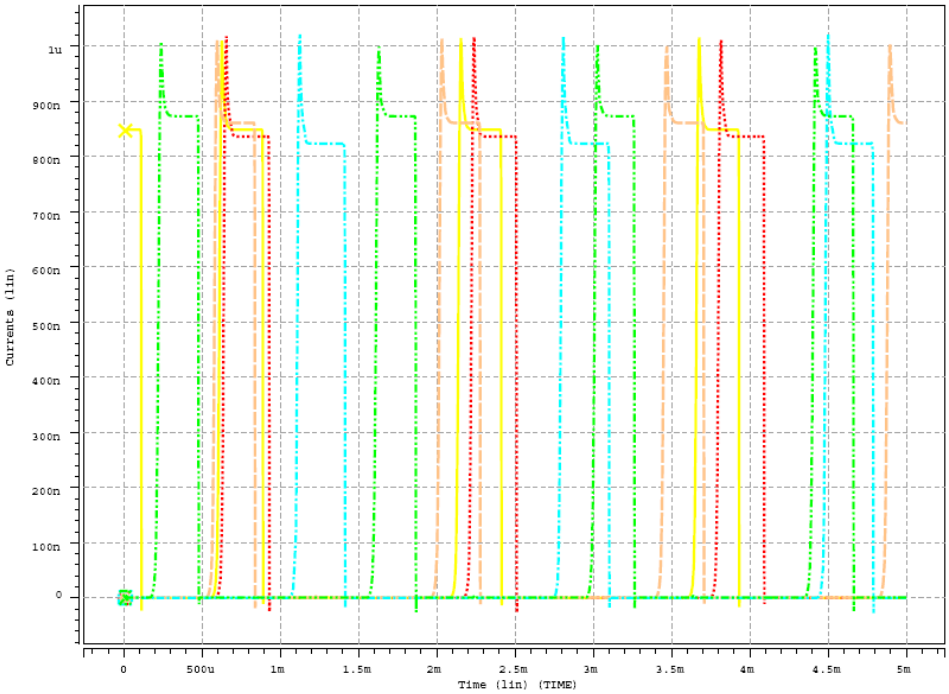


Figure 4.37. the post-layout simulation waveform of single pixel's output under varying surrounding temperature (20℃ ~ 60℃) with 3.6mW/cm^2 light intensity (1nA photocurrent).

TABLE V. sizes of the MOSFETs of each block in modified desgin

clock generator		D flip-flop		combinational logic	
NMOS (μm)		PMOS/NMOS (μm /μm)		PMOS/NMOS (μm /μm)	
M1	100/1	N1	P: 10/5 N: 10/5	NAND gates	P: 10/5 N: 10/5
M2	100/1				
M3	100/1	N2	P: 10/5 N: 10/5	INV gates	P: 10/5 N: 10/5
M4	100/1				
M5	100/1	N3	P: 10/5 N: 10/5		
M6	100/1				
M7	100/1	N4	P: 10/5 N: 10/5		
M8	100/1				
M9	100/1	N5	P: 10/5 N: 10/5		
M10	100/1				
M11	100/1	I1	P: 10/5 N: 10/5		
M12	100/1				
M13	100/1	I2	P: 10/5 N: 10/5		
		I3	P: 10/5 N: 10/5		

TABLE VI. the specification of the retinal chip

SPECIFICATION	
Power supply	No external power supply
Pixel number	4 x4 cells
Chip dimension	1.3x1.2mm^2
Exposured electrode size	50 x 50 μm^2 (within the pixel)
Pixel area	150 μm x 150 μm
Output stimulating current	844nA (3.60 mW/cm^2) 1.72uA (5.06 mW/cm^2)

4.6 SUMMARY

The clock generator in this work is only supplied by on-chip power supply but the oscillation frequency is in proportion with the illumination light intensity. This property can be applied to the optical communication as a modulator/de-modulator. The clock generator can not only function as a clock but also a pulse stimulation generator which can also apply to sub-retinal prosthesis as a stimulus source, which other work need a lot efforts to transmit a pulse signal to the retinal chip.[2]

The Vt variation is one of key issues which greatly influence the feasibility and stability of the circuit design, especially in subthreshold circuit design. In the design of the clock generator, power control unit and pixel circuit, the limited on-chip power supply system has greatly limited the circuit design feasibility and all the MOSFET on the chip is operated in the subthreshold region (weak inversion region) which result in the wrong output function of the power control unit. Therefore we should carry on a wider range Monte Carlo simulation in our future design, such as 10% mismatch in subthreshold region, to ensure the functionality. In all, the output stimulating current of the modified retinal chip is about 844nA, 1.72uA per pixel which is almost three times larger than conventional design [44]. The summary table is shown in table VII.

TABLE VII. the summary of the retinal chip

<table>
<tr><th colspan="3"></th><th colspan="2">Clock generator</th><th colspan="2">Implantable retinal chip</th></tr>
<tr><td colspan="3">Power supply</td><td colspan="2">Solar cell supply</td><td colspan="2">Solar cell supply</td></tr>
<tr><td rowspan="2">Power consumption
two different light intensity</td><td>3.60mW/cm2</td><td colspan="2">5.2nW</td><td colspan="2">2.04uW</td></tr>
<tr><td>5.06mW/cm2</td><td colspan="2">10.5nW</td><td colspan="2">4.1uW</td></tr>
<tr><td rowspan="2">Output
two different light intensity</td><td>3.60mW/cm2</td><td rowspan="2">Clock frequency</td><td>1.632KHz</td><td rowspan="2">Output current</td><td>0.844uA</td></tr>
<tr><td>5.06mW/cm2</td><td>2.442KHz</td><td>1.724uA</td></tr>
<tr><td colspan="3">Compared with conventional design</td><td colspan="2">Ultra low-power design
Required no external power.</td><td colspan="2">Three times output stimulating current.</td></tr>
<tr><td colspan="3">Application</td><td colspan="2">Silicon retinal chip.
Optical communication.</td><td colspan="2">Sub-retinal prosthesis.</td></tr>
</table>

CHAPTER 5 Conclusions and Future Work

5.1 CONCLUSIONS

In this thesis, a retinal chip has been designed, analyzed, and fabricated to improve the power efficiency of the sub-retinal prostheses. The preliminary in vitro experiment of the silicon retina chip which composed of micro photodiode array has been designed and put to practice. In this early in vitro experiment, we can sure that the retinal chip can send the stimulation signal to the retina during the IR illumination and we can use the IR with lower output power to verify the retinal response form light and electric stimulation in further experiment. The feasibility of on-chip solar cell supply system which integrated with circuit system in CMOS technology has been verified in the work. An ultra-low power clock generator is also designed and verified in this work. A three times output stimulating current is achieved by taking advantage of the bio-inspired divisional power supply architecture. The stimulating output current is approximately 844nA under the illumination of 3.6mW/cm^2 light intensity and 1.72μA under the illumination of 5.06mW/cm^2 light intensity. The retinal chip fabricated with a standard 0.18μm tsmc CMOS process demonstrate good mimic of electrical behavior of human retina with low-power consumption. Because of its characteristic, the proposed power management system could be considered as one of the highly integrated solutions for the sub-retinal implant chips.

5.2 FUTURE WORK

The next steps of the retinal chip research are to fabricate and verify the modified retinal chip via electrical experiments, in vitro and in vivo experiments. Though, the power control system can provide a solution to the problem which the solar cell area occupied large area that reduces the resolution of the artificial retina. The area of solar cell as supply is still to large compared to the photo-sensing photodiode area. Solar cells with higher efficiency are required while the SOI technology and GeAs technology might be applied to future retinal chip. Further more, the layout floor plan of the power control unit could be reorganized to surround the retinal pixel array which can prevent the power control unit from failure while the light is focus on the pixel array and there is no light irradiation on the power control unit.

This silicon retina can be used as optical signal receiver and retina stimulator while working with the external optical device which can capture the real-world image and project the processed light signals to the implanted silicon retina. The power control unit can only divide the power into four blocks in this work which can approximately increase three times output stimulating current but the next generation power control unit might divide the power into 16 or 64 blocks by elevating the clock frequency and more frequency dividers to increase the output stimulating current dramatically.

REFERENCES

[1] W. Liu, E. McGucken, K. Vitchiechom and M. Clements, "Dual Unit Visual Intraocular Prosthesis," Proc. IEEE/EMBS Annual International Conference of the IEEE ,Volume: 5 ,30 Oct.-2 Nov. 1997.

[2] W. Liu, "Retinal Implant: Bridgin Engineering and Medicine," *IEDM Digest*, pp.492-495, Dec. 2002

[3] D. Marr, *Vision*, San Francisco, CA: W. H. Freeman, 1982.

[4] D. Marr and E. Hildreth, "Theory of Edge Detection," *Proc. Royal Soc. London B.*, 207, pp. 187-217,1980

[5] J. Babaud, A. P.Withkin, M. Baudin, and R. O. Duda, "Uniqueness of the Gaussian Kernel for Scale-Space Filtering," *IEEE Trans. Pattern Anal. And Mach. Intell.*, Vol. PAMI-8, pp. 26-33, Jan.1986.

[6] P. Perona and J. Malik, "Scale-Space and Edge Detection Using Anisotropic Diffusion," *IEEE Trans. on Pattern Analysis and Machine Intelligence*, vol. 12, No. 7, pp.629-639, July, 1990.

[7] A. Rosenfeld and M. Thurston, " Edge and Curve detection for Visual Scene Analysis," *IEEE Trans. Comput.*, vol. C-20, pp. 562-569, May, 1971.

[8] A. Yuille and T. Poggio, "Scaling Theorems for Zero Crossings," *IEEE Trans Pattern Anal. Machine Intell.*, vol. PAMI-8, Jan., 1986.

[9] A. Witkin, "Scale-Space Filtering," *in Int., Joint Conf. Artificial Intelligence*, Karlsruhe, West Germany, pp. 1019-1021, 1984.

[10] A. Hummel, "Representations Based on Zero-Crossings in Scale-Space," *in Proc. IEEE Computer Vision and Pattern Recognition Conf.*, pp. 204-209, June, 1986.

[11] J. F. Canny, "Finding Edges and Lines in Images," *Artificial Intelligence Lab.Memo*, No. 720, MIT, Cambridge, 1984.

[12] T. Poggio, H. Voorhees, and A. Yuille, "Regularizing Edge Detection," *Artificial Intelligence Lab. Memo*, No.776, MIT, Cambridge, 1984.

[13] T. Poggio and V. Torre, "I11-posed Problems and Regularization Analysis in Early Vision," *Artificial Intelligence Lab. Memo*, No.773, MIT, Cambridge, 1984.

[14] T. Poggio V. Torre and C.Koch, "Computational Vision and Regularization Theory," *Nature*, vol. 317, No.6035, pp. 314-319, 1985..

[15] M. I. Sezan and R. L. Lagendijk, *Motion Analysis and Image Sequence Processing*, Kluwer Academic Publishers, 1994.

[16] B. K. Horn and B. G. Schunck, "Determining Optical Flow," *Artificial Intellighence*, Vol. 17, pp.185-203, 1981.

[17] A. D. Bimbo, P. Nesi, and J. L. C. Sanz, "Analysis of Optical Flow Constraints," *IEEE Trans. Image Processing*, Vol. 4, pp. 460-469,1995.

[18] F. Hildreth, " The Computation of the Velocity Field," *in Proc. Royal Soc. London B.*,

1984, Vol.221, pp.189-220

[19] E. H. Adelson and J.R. Bergen, “Spatiotemporal Energy Models for the Perception of Motion,” *J. Opt. Soc. Amer. A*, Vol. 2, pp.284-299. Feb. 1985

[20] A. Verri, and T. Poggio, “Motion Field and Optical Flow: Qualitative Properties,” *IEEE Trans. Patt. Anal. Machine Intell*., Vol. 11, pp.490-498, May 1989.

[21] A. Verri, F. Girosi and V. Torre, “Differential Techniques for Optical Flow,” *J. Opt. Soc. Amer. A*, Vol. 7, pp. 912-922, May 1990.

[22] Hesse L, Schanze T, Wilms M, Eger M (2000) Implantation of retina stimulation electrodes and recording of electrical stimulation responses in the visual cortex of the cat. Graefes Arch Clin Exp Ophthalmol 238:840 – 845

[23] Humayun MS, De Juan EJ (1998) Artificial vision. Eye 12:605 – 607

[24] Humayun MS, Propst RH, De Juan EJ, McCormick K, Hickingbotham D (1994) Bipolar surface electrical stimulation of the vertebrate retina. Arch Ophthalmol 112:110 – 116

[25] Humayun MS, De Juan EJ, Weiland JD, Greenberg R (1999a) An implantable neuro-stimulator device for a retinal prosthesis. IEEE International Solid- State Circuits TP 12.7 (Abstract)

[26] Humayun MS, Weiland JD, De Juan EJ (1999b) Electrical stimulation of the human retina. In: Hollyfield JG, Anderson RE, LaVail MM (eds) Retinal degenerative diseases and experimentaltherapy. Plenum, New York, pp 479 – 485

[27] Humayun MS, De Juan EJ, Weiland JD, Dagnelie G, Katona S, Greenberg R, Suzuki S (1999c) Pattern electrical stimulation of the human retina. Vision Res 39:2569 – 2576

[28] Rizzo JF, Wyatt JL (2000) Retinal prosthesis. In: Berger J, Fine SL, Maguire MG (eds) Age-related macular degeneration. Mosby, St. Louis, pp. 413 – 432

[29] Wyatt J, Rizzo JF, Grumet A, Edell D, Jensen RJ (1994) Development of a silicon retinal implant: epiretinal stimulation of retinal ganglion cells in the rabbit. Invest Ophthalmol Vis Sci 35:1380 (Abstract)

[30] Chow AY, Chow VY (1997) Subretinal electrical stimulation of the rabbit retina. Neurosci Lett 225:13 – 16

[31] Peyman G, Chow AY, Liang C, Chow VY, Perlman JI, Peachey NS (1998) Subretinal semiconductor microphotodiode array. Ophthalmic Surg Lasers 29:234 – 241

[32] Schwahn HN, Gekeler F, Sachs H, Kobuch K, K_hler M, Jakob W, Gabel V-P, Zrenner E (2000) Evoked cortical responses following multifocal electrical stimulation in the subretinal space of rabbit and micropig. Invest Ophthalmol Vis Sci 41:S102 (Abstract)

[33] Zrenner E. (2002) Will retinal implants restore vision? Science 295:1022 – 1025

[34] Zrenner E, Miliczek K-D, Gabel V-P, Graf HG, Guenther E, Haemmerle H, Hoefflinger B, Kohler K, Nisch W, Schubert M, Stett A, Weiss S (1997) The development of subretinal microphotodiodes for replacement of degenerated

photoreceptors. Ophthalmic Res 29:269 – 280

[35] Zrenner E, Gekeler F, Gabel V-P, Graf HG, Graf M, Guenther E, Haemmerle H, Hoefflinger B, Kobuch K, Kohler K, Nisch W, Sachs H, Schlosshauer B, Schubert M, Schwahn H, Stelzle M, Stett A, Troeger B, Weiss S (2001) Subretinales Mikrophotodioden-Array als Ersatz f_r degenerierte Photorezeptoren [Subretinal microphotodiode array as replacement for degenerated photoreceptors?]. Ophthalmologe 98:357 – 363

[36] Walter P, Szurman P, Vobig M, Berk H, L_dtke-Handjery H-C, Richter H, Mittermayer C, Heimann K, Sellhaus B (1999) Successful long-term implantation of electrically inactive epiretinal microelectrode arrays in rabbits. Retina 19:546 – 552

[37] Majji AB, Humayun MS, Weiland JD, Suzuki S, D' Anna SA, De Juan E Jr (1999) Long-term histological and electrophysiological results of an inactive epiretinal electrode array implantation in dogs. Invest Ophthalmol Vis Sci 40:2073 – 2081

[38] Humayun MS, Weiland JD, Fujii GY, Greenberg R, Williamson R, Little J, Mech B, Cimmarusti V, Van Boemel G, Dagnelie G, De Juan E Jr (2003) Visual perception in a blind subject with a chronic microelectronic retinal prosthesis. Vision Res 43:2573 – 2581

[39] Humayun MS, Weiland JD, Fujii GY, Greenberg R, Williamson R, Little J, Mech B, Cimmarusti V, Van Boemel G, Dagnelie G, De Juan E Jr (2003) Visual perception in a blind subject with a chronic microelectronic retinal prosthesis. Vision Res 43:2573 – 2581

[40] W. Liu, K. Vichienchom, M. Clements, S.C. DeMarco, C. Hughes, E. McGucken, M. S. Humayun, E. de Juan, J. D. Weiland, and R. Greenberg, "A Neuro-Stimulus Chip with Telemetry Unit for Retinal Prosthesis Device," IJSSC, vol. 35, No. 10, October 2000.

[41] Tassiker GE (1956) US Patent 2,760,483

[42] Dobelle WH, Mladejovsky WG (1974b) Phosphenes produced by electrical stimulation of human occipital cortex, and their application to the development of a prosthesis for the blind. J Physiol 243:553 – 576

[43] Normann RA, Warren DJ, Ammermuller J, Fernandez E, Guillory S (2001) High-resolution spatio-temporal mapping of visual pathways using multi-electrode arrays. Vision Res 41:1261 – 1275

[44] A. Y. Chow, T. Pradue, J. I. Perlman, and etc, "Subretinal Implantation of Semiconductor-Based Photodiodes: Durability of novel implant designs," Journal of rehabilitation Research and Development, Vol.39, No.3, pp.313-322, 2002.

[45] http://www.optobionics.com/theeye.htm

[46] A. Y. Chow, T. Pradue, J. I. Perlman, and etc, "Subretinal Implantation of Semiconductor-Based Photodiodes: Durability of novel implant designs," Journal of rehabilitation Research and Development, Vol.39, No.3, pp.313-322, 2002.

[47] Coltheart M. "The persistences of vision." *Philos Trans R Soc Lond B Biol Sci.* 1980 Jul 8.

[48] Jeng-Shyong Shyu, Mauricio Maia, James D. Weiland, Thomas O'Hearn, Shih-Jen Chen, Eyal Margalit, Satoshi Suzuki, and Mark S. Humayun," Electrical Stimulation in Isolated Rabbit Retina" IEEE TRANSACTIONS ON NEURAL SYSTEMS AND REHABILITATION ENGINEERING, VOL. 14, NO. 3, SEPTEMBER 2006

[48] Orly Yadid-Pecht and Ralph Etienne-Cummings, "CMOS Imagers-from phototransduction to image processing". 2004 Kluwer Academic Publishers, Boston.

[49] C.D. Chang, C.H. Liao, Y.C. Lin, D.E. Lin, S.L. Pang, Y.J. Chu, "The Chamber memory Effect Induces P+ Junction Leakage and EEPROM Tunneling Oxide Degradation". 1999 IEEVCPMT Int'l Electronics Manufacturing Technology Symposium

[50] Chunyan Wang, "ELETRICAL-SUPPLY-FREE MOS INTEGRATED CIRCUIT", US patent 6680468.

[51] Trond Ytterdal, Yuhua Cheng, Tor A. Fjeldly, "Device Modeling for Analog and RF CMOS Circuit Design", Copyright 2003 John Wiley & Sons, Ltd.

[52] C. Y. Wu, Felice Cheng, C. T. Chiang, and P. K. Lin "A Low-Power Implantable Pseudo-BJT-based Silicon Retina With Solar Cells For Artificial Retinal Prosthesis," in ISCAS, pp.IV 37-40, 2004.

簡歷

VITA

姓 名：萬謎

學 歷：

國立武陵高中 (88年9月~91年6月)

國立交通大學電子工程學系 (91年9月~95年2月)

國立交通大學電子研究所碩士班 (95年2月~97年4月)

永久地址：桃園市民光東路45巷7號

Email：dcfox.ee91@nctu.edu.tw

m9411411@alab.ee.nctu.edu.tw

論文名稱：

應用於視網膜療程之植入式人工視網膜與其電源控制電路

A CMOS IMPLANTABLE RETINAL CHIP WITH SOLAR CELL POWER SUPPLY CONTROL CIRCUIT FOR RETINA PROSTHESES