國立交通大學

電子工程學系 電子研究所

博士論文

研究半導體和高介電絕緣體之介面以獲得高性能之鍺及三五族金氧半場效電晶體

Improvement of High Dielectric Materials and Semiconductor-Insulator Interfaces for Ge and III-V High Performance MOSFETs

研究生： 鄭兆欽

指導教授： 張俊彥 院士
簡昭欣 教授

中華民國 九十八 年 六 月

研究半導體和高介電絕緣體之介面以獲得高性能之鍺及三五族金氧半場效電晶體

Improvement of High Dielectric Materials and Semiconductor-Insulator Interfaces for Ge and III-V High Performance MOSFETs

研究生：鄭兆欽　　Student: Chao-Ching Cheng

指導教授：張俊彥 院士　　Advisors: Dr. Chun-Yen Chang
簡昭欣 教授　　Dr. Chao-Hsin Chien

國立交通大學
電子工程學系 電子研究所
博士論文

A Dissertation
Submitted to the Institute of Electronics
College of Electrical Engineering and Computer Science
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in Electronics Engineering
June 2009
Hsinchu, Taiwan, Republic of China

中華民國九十八年六月

研究半導體和高介電絕緣體之介面以獲得高性能之鍺及三五族金氧半場效電晶體

研究生：鄭兆欽　　　　　　　　　指導教授：張俊彥 院士
簡昭欣 教授

國立交通大學

電子工程學系 電子研究所

摘要

此論文中，我們廣泛地研究各種高介電(high-*k*)薄膜—包含氮氧化鉿(HfO_xN_y)、三氧化二鋁(Al_2O_3)及三氧化二釓(Gd_2O_3)—在塊材鍺(Ge)及砷化鎵(GaAs)基板上的沉積及元件特性。首先，我們提出兩種表面鈍化方法，氨氣電漿處理及超薄矽批覆，來改善氮氧化鉿濺鍍膜在純鍺基板上；而我們確實看到在經過不管是表面氮化或矽覆蓋製程後，僅少量氧化鍺(GeO_x)存在介電層接面、抑制鍺擴散至上層氮氧化鉿以及較少的氧化層電荷捕獲。我們推測這些改善現象是由於減少氧化鍺的揮發及提升高介電層/鍺接面熱穩定性的結果。

我們接續研究原子層沉積(atomic-layer-deposited)三氧化二鋁在純鍺基板上的材料及電特性。發現提升沉積溫度確實改善三氧化二鋁本身的密度及當量化(stoichiometry)；但沉積溫度超過200度將造成三氧化二鋁介電層與氧化鍺接面層的混合，也就是形成氧化鍺鋁中間層($Ge_xAl_{1-x}O$ intermediate layer)，這將導致白金

/三氧化二鋁/鍺($Pt/Al_2O_3/Ge$)電容元件出現較大漏電流及接面缺陷密度(interfacial state density)高達 10^{13} $cm^{-2}eV^{-1}$ 以上。另一方面，進一步採用氫氣氮氣混合之熱退火(forming gas annealing)來改善低溫(100 度)三氧化二鋁沉積在鍺上的特性，結果發現在靠近能帶中間(midgap)之接面缺陷密度可以下降至約 6×10^{11} $cm^{-2}eV^{-1}$ 左右，連遲滯(hysteresis)現象也獲得改善。此外，我們結合電容元件實驗與 MEDICI 模擬軟體，進一步證實具有高本質載子濃度(intrinsic carrier concentration)的純鍺在透過基板內部缺陷(bulk trap)的產生結合(generation/recombination)或擴散(diffusion)機制，是導致在高頻率下($>10^3$ Hz)會觀察到低頻電容曲線及無電壓相依性之反轉電導(gate-independent inversion conductance)的主因。我們透過電導-電壓(conductance-voltage)特性評估出在低摻雜濃度鍺基板內的缺陷密度約為$(2\text{-}4)\times10^{15}$ cm^{-3} 左右。阿瑞尼士之基板電導圖(Arrhenius-dependent substrate conductance)也指出在鍺基板內比起在矽基板內有高達 10^4 倍的能量損耗(energy loss)，的確反應出具有較快速的次要載子反應速度(minority-carrier response rate)。

論文中，另一研究主題為改善濕式化學清潔(wet-chemical cleaning)及硫化氨處理[$(NH_4)_2S$ treatment]對於高介電層/砷化鎵之電特性影響。實驗證明，採用氨水鹼性溶液(NH_4OH alkaline solution)並搭配 80 度的硫化氨水溶液[$(NH_4)_2S\text{-}H_2O$]可有效地抑制砷化鎵原生氧化層(GaAs native oxides)及接面附近砷原子(elemental As)的形成，進而改善費米能階釘扎效應(Fermi level pinning effect)對電特性的影響。所製造的三氧化二釓/砷化鎵($Gd_2O_3/GaAs$)電容元件經過最佳化硫化處理後，在電容等效厚度(capacitance-equivalent-thickness)約 20 埃及閘極電壓在平帶電壓加 1 伏特[$V_g = (V_{FB}+1)$ V]條件下，可表現出漏電流僅約 1.5×10^{-5} A/cm^2；已足以匹配他人之前文獻使用超薄矽/鍺鈍化(ultrathin Si/Ge interfacial passivation)之二氧化鉿/砷化鎵電容元件的優越電性表現。而原子層沉積之三氧化二鋁/砷化鎵($ALD\text{-}Al_2O_3/GaAs$)電容元件在經過硫化後，也表現出較高的氧化層電容值、較小

的頻率離散(frequency dispersion)、微縮的遲滯現象及較低的接面缺陷密度及漏電流成果。且進一步將硫化氨的溶劑(solvent)從水換成丁醇(C_4H_9OH)將可看到更大幅度的電特性改善，不僅明顯壓抑表面砷原子及氧化砷(AsO_x)的量，也形成更多穩定硫鍵結在砷化鎵基板上。另一方面，後續熱退火氣體環境的採用，氧氣及氮氣，對原子層沉積三氧化二鋁/砷化鎵電容元件特性影響，已可透過了解背後熱化學反應機制來理解。此外，我們也注意另一有趣現象，原子層沉積之三氧化二鋁在砷化鎵基板上傾向於高溫(300 度)成長，剛好跟它在鍺基板上傾向於低溫(低於 200 度)成長是相反趨勢。

最後，我們成功地製作出搭配原子層沉積三氧化二鋁高介電層之反轉式(inversion-mode)純鍺 P 型/N 型場效電晶體。純鍺 P 型電晶體(寬度/長度 = 100 µm/4 µm)呈現載子遷移率峰值(peak mobility)及電流開關比(on-off ratio)分別為 225 $cm^2V^{-1}s^{-1}$ 及大於 10^3；相對地，純鍺 N 型電晶體(寬度/長度 = 100 µm/9 µm)的載子遷移率峰值及電流開關比分別低於 100 $cm^2V^{-1}s^{-1}$ 及 10^3。而我們認為相對劣等的 N 型電晶體特性主要跟具有較大的源極/汲極(source/drain)阻值、較嚴重的接面缺陷散射效應以及較低的基板濃度有所關聯性。後續使用 300 度的氫氣氮氣混合之熱退火不但可以提升驅動電流(on current)、降低能帶缺陷密度以及改善負偏壓熱不穩定性(negative bias temperature instability)可靠度。但提升溫度至 400 度將會極劇增加 N 型電晶體的關電流(off current)，這是由於源極/汲極的磷摻雜發生嚴重向外擴散所導致的結果。在此論文中，我們亦調查純鍺接面二極體特性及漏電流路徑，我們得到純鍺 P^+N 及 N^+P 接面二極體整流特性比分別可超過 10^3 及 10^4(電壓範圍為±1 伏特)，所對應的漏電流為接近 10^{-2} and 10^{-4} A/cm^2。至於漏電流到底是由表面周圍(surface perimeter)或接面面積(junction area)大小所主宰，發現熱製程(摻雜活化或氫氣氮氣混合之熱退火)的使用乃是主要關鍵角色。另一方面，我們也展示具有原子層沉積三氧化二鋁高介電層之空乏式(depletion-mode)砷化鎵 N 型場效電晶體，在搭配硫化氨-丁醇表面處理後的轉換(transfer)及輸出(output)電特

性。在閘極電壓高於臨界電壓 4.8 伏特以及汲極電壓為 4 伏特($V_g – V_{th} = 4.8$ V, $V_d =$ 4 V)條件下，汲極電流(I_d)約為 250 mA/mm。但所萃取出來的電子遷移率峰值僅僅只有 336 cm^{2}V^{-1}s^{-1}之多，顯示高介電層/砷化鎵接面品質仍需進一步最佳化。

Improvement of High Dielectric Materials and Semiconductor-Insulator Interfaces for Ge and III-V High Performance MOSFETs

Student: Chao-Ching Cheng **Advisors: Dr. Chun-Yen Chang**
Dr. Chao-Hsin Chien

Department of Electronics Engineering and Institute of Electronics
National Chiao Tung University

Abstract

In this thesis we have extensively investigated the deposition of various high-*k* dielectric films—including HfO_xN_y, Al_2O_3, and Gd_2O_3—onto the bulk Ge and GaAs substrates and the electrical characteristics of the devices with these developed high-*k* dielectric films. At first, two surface passivation methods, i.e., the NH_3 plasma pretreatment and the ultrathin Si capping, were employed to improve the quality of the sputtered HfO_xN_y films on the Ge substrates. Not only the severe incorporation of Ge species into the overlying HfO_xN_y was eliminated, but also the smaller amount of GeO_x remained at the dielectric interface and the less oxide trapped charge were observed after undergoing surface nitridation or Si capping processes. These improvements can be attributed to the reduced GeO_x volatilization and also enhanced thermal stability of the high-*k*/Ge interface.

We subsequently studied the material and electrical properties of atomic-layer-deposited (ALD) Al_2O_3 thin films on the Ge substrates. It was found that an increase in the deposition temperature did improve both the density and stoichiometry of the Al_2O_3 films; nevertheless, temperatures exceeding 200 °C caused the intermixing of top Al_2O_3 and interfacial GeO_2 layers, i.e., the formation of a $Ge_xAl_{1-x}O$ intermediate layer. It led to the consequence of an increasing gate leakage (J_g) and a higher interface state density (D_{it}, $>10^{13}$ $cm^{-2}eV^{-1}$) in the Pt/Al_2O_3/Ge capacitors. On the other hand, for improving the quality of low-temperature (100 °C) Al_2O_3 films on the Ge, the forming gas annealing (FGA) at 300 °C was conducted further; the value of the D_{it} close to midgap was evidently lowered to ca. 6×10^{11} $cm^{-2}eV^{-1}$ accompanying with the reduced hysteresis width. In addition, we combined these device experiments with MEDICI simulations and thus validated that a high value of intrinsic carrier concentration (n_i) in Ge, via the bulk-trap generation/recombination as well as the diffusion from the bulk substrate, were responsible for the presence of low frequency *C*-*V* curves in the kHz regime and the gate-independent inversion conductance. The density of the bulk trap was estimated to be ca. $(2\text{–}4) \times 10^{15}$ cm^{-3} in the low-doped Ge in terms of their conductance-voltage (*G*-*V*) characteristics. The plot of the Arrhenius-dependent substrate conductance (G_{sub}) also indicated a larger energy loss occurring in Ge than in Si by at least four orders of magnitude, reflecting the fast minority-carrier response rate.

We also, afterward, presented the study of the effects of alterant wet-chemical clean and $(NH_4)_2S$ treatment on the electrical characteristics of high-*k*/GaAs devices. Through analysis of the surface chemistry, it was evident that employing the NH_4OH alkaline solution and then $(NH_4)_2S$-H_2O passivation at 80 °C effectively suppressed the formation of GaAs native oxides and elemental As close to dielectric interface, thereby abating the “Fermi level (E_f) pinning” effect on the electrical performance. With undergoing the optimized sulfidization processes, the fabricated Gd_2O_3/GaAs capacitors exhibited the J_g of ca. 1.5×10^{-5} A/cm^2 @ $V_g = (V_{FB} + 1)$ V with the capacitance-equivalent-thickness of ca. 20 Å, which is comparable to the earlier study of high-performance HfO_2/GaAs system with an ultrathin Si/Ge interfacial passivation. Also, the sulfidized ALD-Al_2O_3/GaAs capacitors can reveal the resultant higher oxide capacitance, the smaller frequency dispersion, the decreased hysteresis width, the reduced D_{it}, and the smaller J_g, respectively. Further replacing the $(NH_4)_2S$ solvent from H_2O to C_4H_9OH indicated a higher electrical improvement, in which an obvious suppression of elemental As and AsO_x surface species was found with an increasing sulfur bonds on the GaAs substrates. On the other hand, the influences of post annealing ambient, O_2 and N_2, adopted in the Al_2O_3/GaAs capacitor were investigated and we clarified the characteristic differences by identifying the underlying thermochemical mechanisms. In our studies, another interesting feature was noticed that the deposition of the ALD-Al_2O_3 films on GaAs favored to at the higher temperature, 300 °C, which is opposite to the behavior that those on Ge favored to at low temperatures (<200 °C).

Finally, we have successively demonstrated the device characteristics of the inversion-mode Ge p- and n-MOS field-effect-transistors (FETs) with the ALD-Al_2O_3 gate dielectrics, respectively. The respective peak mobility and on/off ratio was ca. 225 cm^2 V^{-1} s^{-1} and >10^3 for Ge p-FET (W/L = 100 μm/4 μm), while these values were less than 100 cm^2 V^{-1} s^{-1} and ca. 10^3, respectively, for Ge n-FET (W/L = 100 μm/9 μm). The inferior n-FET device performance can be mainly correlated to the larger source/drain (S/D) contact resistance, the severe D_{it} scattering, and the lower level of substrate doping. Subsequently performing FGA at 300 °C can enhance the driving on-current, decrease the D_{it} at the Al_2O_3–Ge interface, and improve the negative bias temperature instability (NBTI) reliability. A higher FGA temperature of 400 °C led to a dramatic increase in the off-current of the n-FET, arising from the severe out-diffusion of phosphorous dopant from S/D. Herein, the characteristics of Ge junction diodes and their reverse leakage paths were also examined in more details. The magnitudes of the rectifying ratios for the Ge p^+n and n^+p junctions exceeded three and four orders of magnitude (in the voltage range of ±1 V), respectively, with the values of reverse junction leakage of ca. 10^{-2} and 10^{-4} A/cm^2, respectively. The site of the primary leakage path, at either the surface periphery or junction area, was determined by (i) the thermal budget during dopant activation and (ii) whether FGA was employed or not. Furthermore, the transfer and output characteristics of the depletion-mode ALD-Al_2O_3/GaAs n-FET with the $(NH_4)_2S$-C_4H_9OH chemical passivation were also presented. The maximum I_d was 250 mA/mm measured at V_g–V_{th} = 4.8 V, V_d = 4 V. However, the extracted peak electron mobility was only 336 cm^{2}V^{-1}s^{-1}, indicating that optimization of the dielectric/GaAs interface was still required.

誌　謝

首先，我要向指導教授張俊彥院士致上最高謝意與敬意。在這些年的學習生涯中給予極大的研究空間及支持，讓我順利完成博士學位，也習得許多待人處世及應對進退之道。而老師在學術專業上的創新遠見不僅讓我受益無窮，其對知識追求的積極態度更令我敬佩。且在學術領域上也能一再受到海內外給予最高榮譽肯定，不啻對台灣半導體，更對國家高等教育與經營管理上都有卓越貢獻。

其次很想感謝的人是簡昭欣教授。從碩班一直拉拔我長大，人最怕就是犯錯時，還自己渾然不知，簡博在這方面指點我相當多，很感謝他的點悟!實驗研究的帶領自然不在話下，其對人生觀的寬闊胸襟也是我學習的對象，提的起放的下，而簡博真的做到了，讓我打從心裡佩服!而從他身上也學到許多，實在無法一一言表，以衷心祝福來感謝他長久以來的照顧。另外，想謝謝羅廣禮博士，對我來說，他就像是個亦師亦友的角色，不僅在熱烈討論過程中，學到很多，還可以一起聊天搞笑，這才是做實驗嘛!很感謝他每次在實驗上總是二話不說就給予幫助，不知該做些啥回報，羅博我只有腿特長，不知可以幫上啥忙~哈哈~，未來兆欽還有很多需要您多多照顧的地方，再麻煩您了!

再來想感謝我大學的啟蒙老師-倪澤恩老師，真的可以說沒有他的鼓勵與提攜，沒有今日的兆欽。雖然今日只是得到一個博士學位，但

想跟倪老師說:想與您一起分享我的喜悅，感謝您。另外也感謝長庚的好伙伴-暉堂學長及人正學弟，快點畢業阿!鐵三角的約定!

而當初指導我入門最重要的四位學長-王丁勇學長、陳經緯學長、彭辭修學長、陳怡誠學長。感謝他們全心全意的傾囊相授，讓我獲益良多，怡誠學長-我不會忘記我們一起炒X的回憶，雖然人生有各自的旅程要走~Hovever~We~Have~Brother~Watch~Right?.^_^.。另外很幸運還有很多很棒的學長姊們，像紹明學長、世璋學長、宗熺學長、土撥學長、漢譽學長、小懿學長、慶宗學長、心卉學姐、凱立學長、宗霖學長、文政學長、永俊學長，還有很多一起經歷酸甜苦辣的戰友及學弟們，有立偉、昭正、哲榮、緯仁、弘斌、家豪、勝杰、Joner、吱吱、勾勾楊、賽哥、師父、詩國、彥廷、效諭、宣凱還有好多學長學弟，一時也想不起來，如果忘記了，可要原諒我阿~一併感謝你們，對了，還有最棒的兩位助理-伊喬公主及秋梅美女，感恩阿~。

再來要非常感激NLD的明瑞學長、世祿學長、志彥學長、仕強學長、楊君惠小姐、沈奕伶小姐等在實驗樣品與分析的製備協助。也感謝台積電的柯誌欣博士給予的幫助以及超寬容體諒，讓我得以順利完成這篇論文。而一路走來，也帶領過很多屆的學弟，從第一屆的哲弘，第二屆的小劉、阿國、競之，第三屆的欣哲、弘森、敬倫、登偉、春瑀，到現在的第四屆宗佑跟政庭，沒有你們，我根本無法畢業，太感

謝你們了，希望你們每個人都可以大展鴻圖，這樣我才可以跟你們攀交情~嘿嘿~也祝福宗佑跟政庭能順利考過資格考加博班畢業~等給你們兩個請客。

另一方面，我想謝謝陪我度過充滿無限快樂的交大國標社及中華國標社的朋友們~真的~我愛你們~每個人親手寫的卡片都讓我很感動，也給我一個很棒的生日驚喜[一大堆派]及超讚的送舊派對，還有也謝謝京橋在跳舞給予很大的啟示，希望你在跳舞領域也要拿到博士等級喔，我才能把你最心愛的宛姍正妹嫁給你喔~哈哈~而對我來說，最重要的是陪我跳舞很久的雲雲，一起教舞編舞、考執照、出國遊玩、到處表演和比賽，這些回憶，forever，將永生難忘，my best partner。

而在我人生路途上，一直無怨無悔陪伴著我的女友積頤，不管是甜是苦，感謝妳，妳永遠不離不棄，希望未來一直有妳的陪伴~愛你~最後，萬分感謝父母從小含辛茹苦的扶養與對我教育的重視，無虞匱乏的支持鼓勵，成就我今天的小小成就，希望我最愛的爸爸媽媽身體健康，每天開開心心的、我老哥工作順遂、大嫂佳雯未來生產順利，謹將這份成果獻給我摯愛的家人及朋友們。

鄭兆欽

於新竹交通大學

2009 年 07 月 12 日

Contents

Chapter 1

Introduction and Research Motivation

Chapter 2

Sputtered HfO_xN_y Dielectric Films on Bulk Ge Substrates

Chapter 3

Atomic-Layer-Deposited Al_2O_3 Dielectric Films on Bulk Ge Substrates

Chapter 4

E-gun Evaporated Gd_2O_3 Dielectric Films on GaAs Substrates

Chapter 5

Atomic-Layer-Deposited Al_2O_3 Dielectric Films on GaAs Substrates

Chapter 6

Inversion-Mode Ge p- and n-MOSFETs and Depletion-Mode GaAs n-MOSFET with Atomic-Layer-Deposited Al_2O_3 Gate Dielectrics

Chapter 7

Conclusions and Suggestions for Future Work

Table Captions

Chapter 1

Chapter 4

Chapter 5

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

Chapter 1

Introduction and Research Motivation

1.1 Overview of Transistor Research Roadmap and Device Scaling Issues

The rapid advancement of complementary metal oxide semiconductor (CMOS) integrated circuit technologies during the past few decades has forced the Si-based microelectronics industry to face several huge technological challenges and to test some theoretical limits. R. Chau, Intel Corporation, has even demonstrated the scaling roadmap in the progress of the Si MOS field-effect-transistors (FETs), as displayed in **Fig. 1.1**. It was found that within the next two decades, the lateral dimensions of the transistor will approach the physical limits and finally consist of only a few atoms. Accordingly, several device issues emerged in the nanoscale MOSFETs, as the scheme presented in **Fig. 1.2**. The first issue is the poor device electrostatics and we need to maintain the gate control ability within the channel. One solution is the use of the double- and triple-gates to improve the electrostatics, but, it also implies that the additional process challenges emerged in such new device architecture. Second, the channel transport characteristic is also degraded, leading to the decrease of device on-current (I_{on}). Employment of new channel materials possessing the higher carrier mobility and injection velocity is conceivable to solve this channel issue, even if these materials possibly bring other integration issues in Si device platform. Third, it is expect that the impact of the source/drain (S/D) resistance on the reduction of I_{on} is an increasing importance with the dimension scaling. It was suggested that the replacement of the ion implantation with the in-situ doping in the S/D region, i.e., implantation-free S/D, or the use of metal Schottky S/D is the possible solution to reduce the effect of the extrinsic resistance. The fourth and fifth issues are an exponential increase in the gate leakage current of an ultra-thin SiO_2 and the poly depletion effect, respectively. Even up to now, these two well-known issues are of intense discussion. Of course, the adoption of the metal-gate/high-*k* dielectric stack is the optimum solution to solve these two issues.

In fact, at the early stage of the 90-nm node, substrate engineering and uniaxial strain technologies—e.g., pseudomorphic SiGe channels grown on the Si substrates for p-FETs [1] and strained Si channels on the relaxed graded SiGe buffer layers for n-FETs [2]—have been developed to enhance the carrier mobility in the channel. With further scaling down to the 45-nm node, high-*k* materials are also introduced as alternative gate dielectrics—in place of ultra-thin conventional SiO_2 or oxynitrides—in light of leakage concerns and reliability issues. Many novel device structures and materials are continuously proposed and explored eagerly in an effort to alleviate the tremendous scaling pressure required to improve device performances. Various kinds of non-planar tri-gate architectures, carbon nanotubes, nanowires, and high-mobility materials catch an increasing attention in recent years. Among above intense researches, the feasibility of integrating various prevailing high-*k* dielectrics with high mobility substrates is of much interest due to the advanced progress in the development of high-*k* dielectrics in Si-based MOSFET applications. Through the **Table 1.1**, we can compare the material properties of bulk Si, Ge, GaAs, and InAs at 300 K [3]. As seen, since Ge possesses the higher electron (3×) and hole (4×) mobilities than those in Si, therefore, Ge is considered new potential candidate to be p- and n-channel materials for high-performance logic devices. While GaAs and InAs, relative to Si, have the advantages of much higher enhancements in electron mobility and velocity; in consequence, III-V materials are suitable to be n-channel MOSFET. Up to date, the promising device characteristics of Ge [4], [5], (In)GaAs [6], and InSb [7] channels with either HfO_2 or Al_2O_3 high-*k* dielectrics have been continually demonstrated, and their performance even surpassed the traditional Si transistors at the sub-micro gate length [8]. Therefore, it is believed that the MOS capacitor and device properties integrating various high-*k* dielectric materials onto Ge and GaAs substrates are worthy to study in this dissertation. Accordingly, the device challenges and process difficulties in use of the high-mobility channels/substrates are of importance to describe more details. We will describe these subjects in the following **Session 1.2**.

1.2 Device and Process Challenges in High Mobility Substrates

As discussed in the previous section, great progress in the deposition of high-*k* materials enables renewed interest in high-mobility substrates being as a transport channel in combination with various high-*k* dielectrics. In other words, the first challenge is how to realize the high interface quality between the deposited dielectric films and either Ge or III-V semiconductors. The absence of thermodynamically stable insulators on these two high-mobility substrates has probably become the foremost bottleneck to them rivaling or exceeding the properties of Si MOSFETs. This actually leads to the onset of high interfacial state density (D_{it}), thereby causing a Fermi level (E_{f}) pinning effect and casting some doubts on the anticipated performance [9]. In fact, for the studies of the dielectric/III-V interface, especially the (In)GaAs substrate, numerous efforts have been devoted for more than four decades in intensively questing the competitive, high interface quality insulators and efficient passivation methods, respectively. Except for SiO_2 and Si_3N_4, $(Gd,Ga)_2O_3$ and atomic-layer-deposited (ALD) Al_2O_3 [10], HfO_2 [11] high-*k* dielectrics are of particular interest; meanwhile, the sulfur chemical treatment [12], and Si and Ge [13] as the interfacial passivation layers are currently active approaches to protect the III-V surface prior to the dielectric deposition. Namely, Ge also requires the surface protection, like employing the thermal annealing in NH_3 [14] or SiH_4 [15] ambient, in order to reduce the value of the D_{it} as low as possible, e.g, $<10^{11}$ cm^{-2}eV^{-1}.

Another important subject is the fabrication of high-performance S/D junction in Ge and III-V MOSFETs. At first, for the Ge p^+n junction, fortunately, the boron is a highly activated dopant without the need of higher annealing temperature (just in the range 450–550 °C), and the retarded diffusion behavior of boron dopant is also observed [16]. However, almost the opposed results are characterized in the corresponding n^+p junction. Not only a higher thermal budget (in the range 550–650 °C) is required during n-type dopant activation, but also more rapid dopant diffusion (either out of the surface or into the substrate) and lower electrical activation are generally observed [17], [18]. It has been reported previously that the amounts of P dopant loss were ca. 40% and >60% after RTA at 500 and 600 °C, respectively [19]. The resultant surface concentration also influenced the variation of the contact resistance [20]. Therefore, how to obtain the n^+p shallow junction having an acceptable leakage current is critical to obtaining high-performance Ge n-FETs. It should be noted that the feature of small bandgap in Ge and other III-V materials (except GaAs) is likely to give rise to high band-to-band tunneling (BTBT) leakage current and hence large static power dissipation.

On the other hand, the III-V junction diodes have been widely investigated because of the optoelectronic applications, but, we still need to consider two essential issues in fabricating the III-V n^+p junction for the n-FET application. One is that the dopant activation temperature, in general, is also higher, e.g, in the range 750–850 °C for (In)GaAs-based materials, which in turn possibly degrades the characteristic of the dielectric/III-V interface. Another is III-V materials that usually possess the lower values of solid solubility of n-type dopants and the density of states (DOS), as shown in **Table 1.1**. For example, in GaAs the maximum Si solubility and the DOS are merely $(4\text{-}6) \times 10^{18}$ and 4.7×10^{17} cm^{-3}, respectively, which are ca. 1.5 and 2 orders of magnitude lower than those in Si. In consequence, these inherent material issues certainly contribute the more S/D resistance in device and hence limit the maximum I_{on}, acting the obstacle in outperforming the Si device performance of deep sub-100nm region [21].

Other device issues and process difficulties, like the work function of gate metals, the metal germanide technology in S/D, wet-chemical cleaning processes, and wet/dry etching, are still significant. Most importantly, the subject of heterogeneous integration of these Ge and III-V materials onto the traditional Si platform, i.e., the heteroepitaxy technique, will be quite critical in developing these oncoming nanoscale CMOS technologies.

1.3 Scope and Organization of the Thesis

Two promising high-mobility substrate materials, Ge and GaAs, are investigated in this dissertation. We devoted our efforts to the effects of wet-chemical clean, surface passivation, and thermal processing on the physical and electrical properties of various alternative high-*k* gate dielectrics on these two substrates. This dissertation is divided into seven chapters and organized as follows:

In **Chapter 1**, a brief overview of the background and motivation is described. We reviewed the MOSFET scaling roadmap and the possible challenges emerged in the nanoscale devices. Next, we discussed the significance of high mobility substrates in further application of the advanced CMOS technologies; meanwhile, the process difficulties and material issues in the accomplishment of the Ge and GaAs III-V devices were brought up.

In **Chapter 2**, we performed the physical and electrical analyses to systematically examine the HfO_xN_y thin films sputtered on Ge substrates and the admittance properties of their MIS capacitors. Both the NH_3 plasma treatment and Si_2H_6 thermal annealing are proposed in an attempt to improve the properties of HfO_xN_y high-*k* films on Ge substrates. We observed that not only the out-diffusion of Ge substrate and charge trapping phenomenon of entire HfO_xN_y/Ge gate stack are relieved, but also the thermal stability is enhanced after these two passivation methods.

In **Chapter 3**, we investigated the structural and electrical properties of Al_2O_3 thin films grown through ALD system on Ge substrates. It was observed that variation of the substrate temperature strongly influenced the Al_2O_3 film qualities on Ge, including the density, stoichiometry, and the degree of the Al_2O_3-GeO_2 intermixing. Such a temperature effect on the interface, capacitor, and gate leakage characteristics of the Al_2O_3/Ge structures is examined as well. Furthermore, we explored the minority-carrier response behavior of Ge MOS capacitors through MEDICI simulations and device experiments, and further compare their electrical differences with those in traditional Si MOS capacitors.

In **Chapter 4**, we modified the wet-chemical clean and $(NH_4)_2S$ sulfidizing treatment on GaAs substrate and characterized the effects of the surface modification on the interfacial and electrical improvements of the e-gun evaporated Gd_2O_3/GaAs MOS capacitors. In addition, we further compared the gate leakage characteristics of the fabricated Gd_2O_3/GaAs structures to the reported performance of various high-*k* dielectric materials on GaAs substrates.

In **Chapter 5**, the deposition of ALD-Al_2O_3 gate dielectrics on GaAs substrates was studied. Next, the impact of interfacial $(NH_4)_2S$ treatment integrating with different sulfidizing solvents was investigated through analyses of the surface chemistry and capacitor characteristics of the Al_2O_3/GaAs structure. In the following, we performed the post-deposition annealing in O_2 and N_2 ambient to understand the changes of the structural and electrical properties; the differences were clarified in terms of identifying the underlying thermochemical mechanisms.

In **Chapter 6**, both the inversion-mode Ge p- and n-MOSFETs and the depletion-mode GaAs n-MOSFET with the ALD-Al_2O_3 gate dielectrics were fabricated. Herein, we studied effects of the forming gas annealing on the Ge junction and device properties; the correlation between the n-type dopant activation and the origins of n^+p junction leakage and source/drain resistance is also analyzed in more details. On the other hand, the transfer and output characteristics of ALD-Al_2O_3/GaAs n-MOSFET were demonstrated and we employed the $(NH_4)_2S$-C_4H_9OH chemical passivation to improve the GaAs device performance further.

In **Chapter 7**, we summarized the experimental results in the thesis and gave the conclusions and the suggestions for future studies.

References (Chapter 1)

[1] C.-W. Chen, C.-H. Chien, Y.-C. Chen, S.-L. Hsu, and C.-Y. Chang, "Deep sub-micron strained $Si_{0.85}Ge_{0.15}$ channel p-channel metal-oxide-semiconductor field-effect transistors (pMOSFETs) with ultra-thin N_2O-annealed SiN gate dielectric," *Jpn. J. Appl. Phys.*, vol. **44**, p. L278, 2005.

[2] N. Sugii, D. Hisamoto, K. Washio, N. Yokoyama, and S. Kimura, "Performance enhancement of strained-Si MOSFETs fabricated on a chemical-mechanical-polished SiGe substrate," *IEEE Trans. Electron Devices*, vol. **49**, p. 2237, 2002.

[3] M. Levinshtein, S. Rumyantsev, and M. Shur, *Handbook Series on Semiconductor Parameters Volume 1: Si, Ge, C(diamond), GaAs, GaP, GaSb, InAs, InP, InSb*, World Scientific, Singapore, 1996.

[4] D. Kuzum, A. J. Pethe, T. Krishnamohan, and K. C. Saraswat, "Ge (100) and (111) n- and p-FETs with high mobility and low-T mobility characterization," *IEEE Trans. Electron Devices*, vol. **56**, p. 648, 2009.

[5] G. Nicholas, B. De Jaeger, D. P. Brunco, P. Zimmerman, G. Eneman, K. Martens, M. Meuris, and M. M. Heyns, "High-performance deep submicron Ge pMOSFETs with halo implants," *IEEE Trans. Electron Devices*, vol. **54**, p. 2503, 2007.

[6] H.-C. Chin, M. Zhu, Z.-C. Lee, X. Liu, K.-M. Tan, H. K. Lee, L. Shi, L.-J. Tang, C.-H. Tung, G.-Q. Lo, L.-S. Tan, and Y.-C. Yeo, "A new silane-ammonia surface passivation technology for realizing inversion-type surface-channel GaAs n-MOSFET with 160 nm gate length and high-quality metal-gate/high-*k* dielectric stack," *Tech. Dig. Int. Electron Devices Meet.*, p. 383, 2008.

[7] N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov, R. Kambhampati, M. Yakimov, Y. Sun, P. Pianetta, C.K. Gaspe, M.B. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai, "Addressing the gate stack challenge for high mobility $In_xGa_{1-x}As$ channels for

nFETs," *Tech. Dig. Int. Electron Devices Meet.*, p. 363, 2008.

[8] M. Radosavljevic, T. Ashley, A. Andreev, S. D. Coomber, G. Dewey, M. T. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, M. K. Hudait, R. Jefferies, T. Martin, R. Pillarisetty, W. Rachmady, T. Rakshit, S. J. Smith, M. J. Uren, D. J. Wallis, P. J. Wilding and R. Chau, "High-performance 40nm gate length InSb p-channel compressively strained quantum well field effect transistors for low-power (Vcc=0.5V) logic applications," *Tech. Dig. Int. Electron Devices Meet.*, p. 727, 2008.

[9] T. H. Chiang, W. C. Lee, T. D. Lin, D. Lin, K. H. Shiu, J. Kwo, W. E. Wang, W. Tsai, and M. Hong, "Appoaching Fermi level unpinning in oxide-$In_{0.2}Ga_{0.8}As$," *Tech. Dig. Int. Electron Devices Meet.*, p. 375, 2008.

[10] H.-L. Lu, L. Sun, S.-J. Ding, M. Xu, D. W. Zhang, and L.-K. Wang, "Characterization of atomic-layer-deposited Al_2O_3/GaAs interface improved by NH_3 plasma pretreatment," *Appl. Phys. Lett.* vol. **89**, p. 152910, 2006.

[11] M. Zhu, C.-H. Tung, and Y.-C. Yeo, "Aluminum oxynitride interfacial passivation layer for high-permittivity gate dielectric stack on gallium arsenide," *Appl. Phys. Lett.* vol. **89**, p. 202903, 2006.

[12] M.-K. Lee, C.-F. Yen, J.-J. Huang, and S.-H. Lin, "Electrical characteristics of postmetallization-annealed MOCVD-TiO_2 films on ammonium sulfide-treated GaAs," *J. Electrochem. Soc.* vol. **153**, p. F266, 2006.

[13] H.-S. Kim, I. Ok. M. Zhang, T. Lee, F. Zhu, L. Yu, and J. C. Lee, "Metal gate-HfO_2 metal-oxide-semiconductor capacitors on n-GaAs substrate with silicon/germanium interfacial passivation layers," *Appl. Phys. Lett.* vol. **89**, p. 222903, 2006.

[14] T. Maeda, M. Nishizawa, Y. Morita, and S. Takagi, "Role of germanium nitride interfacial layers in HfO_2/germanium nitride/germanium metal-insulator-semiconductor structures," *Appl. Phys. Lett.*, vol. **90**, p. 072911, 2007.

[15] N. Wu, Q. Zhang, D. S. H. Chan, N. Balasubramanian, and C. Zhu, "Gate-first Germanium nMOSFET with CVD HfO_2 gate dielectric and silicon surface passivation," *IEEE Electron Devices Lett.*, vol. **27**, p. 479, 2006.

[16] Y. S. Suh, M. S. Carroll, R. A. Levy, G. Bisognin, D. D. Salvador, M. A. Sahiner, and C. A. King, "Implantation and activation of high concentrations of boron in germanium," *IEEE Trans. Electron Devices,* vol. **52**, p. 2416, 2005.

[17] M. Posselt, B. Schmidt, W. Anwand, R. Grotzschel, V. Heera, A. Mucklich, C. Wundisch, W. Skorupa, H. Hortenbach, S. Gennaro *et al.*, "P implantation into preamorphized germanium and subsequent annealing: solid phase epitaxial regrowth, P diffusion, and activation," *J. Vac. Sci. Technol. B,* vol. **26**, p. 430, 2008.

[18] A. Satta, E. Simoen, R. Duffy, T. Janssens, T. Clarysse, A. Benedetti, M. Meuris, and W. Vandervorst, "Diffusion, activation, and recrystallization of high dose P implants in Ge," *Appl. Phys. Lett.*, vol. **88**, p. 162118, 2006.

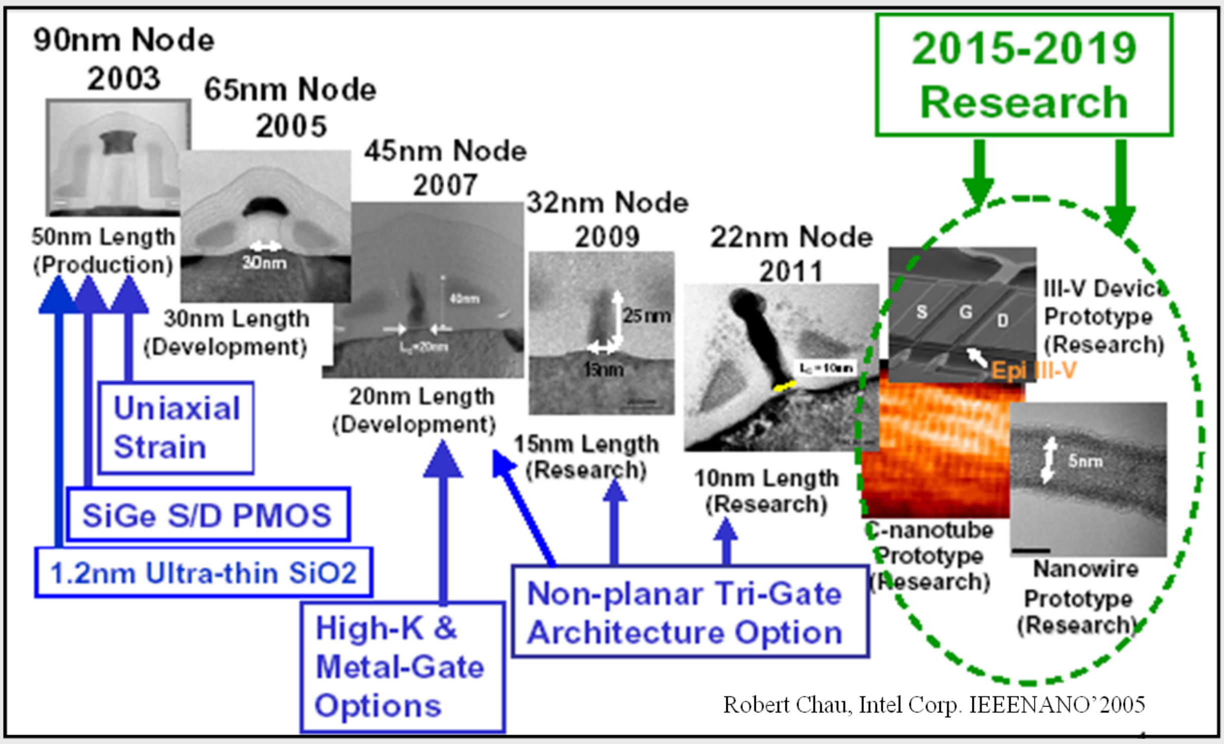
[19] A. Satta, T. Janssens, T. Clarysse, E. Simoen, M. Meuris, A. Benedetti, I. Hoflijk, B. D. Jaeger, C. Demeurisse, and W. Vandervorst, "P implantation doping of Ge: diffusion, activation, and recrystallization," *J. Vac. Sci. Technol. B,* vol. **24**, p. 494, 2006.

[20] C.-C. Cheng, C.-H. Chien, G.-L. Luo, C.-L. Lin, H.-S. Chen, J.-C. Liu, C.-C. Kei, C.-N. Hsiao, and C.-Y. Chang, "Junction and Device Characteristics of Gate-Last Ge p- and n-MOSFETs with ALD-Al_2O_3 Gate Dielectric," *IEEE Trans. Electron Devices*, (accepted).

[21] M. V. Fischetti, L. Wang, B. Yu, C. Sachs, P. M. Asbeck, Y. Taur, and M. Rodwell: 'Simulation of electron transport in high-mobility MOSFETs: density of states bottleneck and source starvation', *Int. Electron Devices Meet. Tech. Dig.*, p. 109, 2007.

Material	Lattice constant (Å)	E_g (eV)	Intrinsic carrier concentration n_i (cm^{-3})	Conduction band density of states Nc (cm^{-3})	Dopant type	Dopant act. limit (cm^{-3})	Electron velocity v_e (cm^2/s)	Electron mobility μ_e (cm^2/V-s)	Hole mobility μ_h (cm^2/V-s)
Si	5.431	1.12	9.6E9	2.8E19	P	(1-2)E20	2.3E7	1350	480
Ge	5.646	0.66	2.4E13	1.04E19	P	(4-6)E19	3.1E7	3900	1900
GaAs	5.653	1.42	2.1E6	4.7E17	Si	(4-6)E18	4.4E7	8500	400
InAs	6.058	0.35	1.0E15	8.7E16	Si	(1-3)E18	7.7E7	33000	460

Table. 1.1 Material properties of Si, Ge, GaAs, and InAs at 300 K.

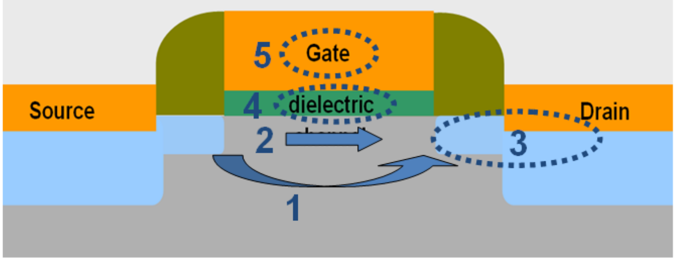


Robert Chau, Intel Corp. IEEENANO'2005

Fig. 1.1 Transistor scaling and research roadmap demonstrated by R. Chau, Intel Corp.

Problem 4: Gate leakage increased
Solution – High-K dielectrics
- Reduced gate leakage

Problem 5: poly-gate depletion
-> increased EOT
Solution – Metal gate
- High drive current



Problem 1: Poor Electrostatics
-> increased I_{off}
Solution - Double Gate
- Retain gate control over channel
- Minimize off-state S/D leakage

Problem 3: S/D Parasitic Resistance
-> decreased I_{on}
Solution – Metal Schottky S/D
- Reduced extrinsic resistance

Problem 2: Poor Channel Transport -> decreased I_{on}
Solution – High Mobility III-V Channel
- High mobility/ injection velocity
- High drive current and low intrinsic delay

Fig. 1.2 Scheme of device issues in the nanoscale MOSFETs.

Chapter 2

Sputtered HfO_xN_y Dielectric Films on Bulk Ge Substrates

2.1 Introduction

Recently, Ge-channel devices—including bulk Ge [1], [2], strained Ge [3], and Ge-on-insulator (GOI) [4] systems—integrated with high-*k* gate dielectrics have attracted considerable research interest. Although transistors were originally fabricated on Ge substrates, the lack of a stable Ge native oxide has been an obstacle in complementary metal-oxide-semiconductor (CMOS) device realization with Ge. Therefore, silicon has been used in CMOS technology for many decades because of the better qualities of its native oxide, such as a low leakage current, low interface state density, and good thermal stability. With the further scaling of device and gate oxide dimensions down to the nanometer range, however, the leakage current density in SiO_2 has become much higher than 2 mA/cm^2, which is the maximum concession for low power applications [5]. Consequently, higher dielectric-constant materials with a thicker physical thickness are introduced to suppress the concern of excessive gate leakage while maintaining the equivalent-oxide-thickness (EOT) of the scaled devices.

Presently, hafnium-based oxides or oxynitrides, e.g., HfO_2, HfON, and HfSiON, are the uppermost candidates for application among all of the potential high-*k* dielectrics. Both Si and SiGe MOSFETs integrated with Hf-based gate dielectrics exhibit admirable properties [6]-[8], but they also reveal undesirable surface carrier mobility degradation behavior [9], [10]. Changing the substrate from Si to Ge might be a possible solution to this problem because Ge has a higher carrier mobility relative to that of Si. From recent advances in the deposition of high-*k* materials, Ge MOSFETs incorporating high-*k* gate dielectrics have exhibited some promising performance [11], [12]. In this session, we investigated the physical and electrical characteristics of HfO_xN_y sputtered films on bulk Ge substrates and then determined the impact of thermal annealing processing on the entire capacitor structure. Meanwhile, recent reports have described that annealing a cleaned Ge substrate in a NH_3 [13] or SiH_4 [14] gas ambient, prior to deposition of a high-*k* dielectric, further improves the MOS properties on Ge. Here, we proposed the NH_3 plasma pretreatment to passivate a Ge substrate and investigated the passivation efficiency. Actually, the overall MOS structures had higher thermal stability and showed the improved electrical characteristics. On the other hand, we also speculate that the incorporation of nitrogen atoms may lead to incomplete passivation of the dangling bonds on the Ge surface; such a surface would not fully inhibit the growth of GeO_x because of the lower thermal stability of Ge–N bonds [15]. Therefore, we also attempted to adopt the Si_2H_6 passivation onto Ge surfaces, in which several monolayers of Si exist between the gate dielectric and Ge substrate, for inhibiting the formation of GeO_x and suppressing hysteresis phenomena in high-*k*/Ge MOS capacitors; we also presented an energy band diagram to explain the charge trapping model.

2.2 Experimental Procedures

N-type Ge substrates, which were doped with Sb dopant at a concentration of ca. 1×10^{14} cm^{-3} (resistivity ~ 8–12 Ω·cm), were precleaned through a cyclic rinse involving a diluted HF dip and deionized water. After wet cleaning, the NH_3 plasma exposure on the Ge surface of some samples was performed in the plasma-enhanced chemical vapor deposition (PECVD). HfO_xN_y thin films were subsequently deposited through reactive sputtering in a $Ar+N_2$ ambient with a pure Hf target, followed by annealing in a N_2 atmosphere containing residual oxygen. In an attempt to suppress any additional oxidation, which can help to minimize the thickness of interfacial layer (IL), the post-deposition annealing (PDA) was performed in an N_2 ambient rather than an O_2 ambient to convert HfN into HfO_xN_y. Various

PDA temperatures (500 and 600 °C) and durations (30 s and 5 min) were employed. Next, a platinum (Pt) dot was deposited using electron beam evaporation through a shadow mask. For evaluating the thermal stability of the Pt/high-*k*/Ge structures, the post-metallization annealing (PMA) with the same temperature conditions were performed.

For experiments of the ultrathin Si capping, the cleaned Ge substrates underwent thermal desorption at 550 °C for 10 min through ultrahigh-vacuum chemical vapor deposition (UHVCVD) to remove the native GeO_x, followed by *in situ* passivation of a Si capping layer upon annealing under a Si_2H_6 ambient at the same substrate temperature; the thicknesses—evaluated using angle-resolved x-ray photoelectron spectroscopy (AR-XPS)—were ca. 8 Å and ca. 13 Å for annealing duration of 1 and 2 min, respectively. After the following deposition of high-*k* film and metallization process, the Pt/HfO_xN_y/Ge MOS capacitor structure can be obtained.

Transmission electron microscopy (TEM) and secondary ion mass spectroscopy (SIMS) were employed to investigate the entire structure and Ge incorporation behavior after these two pretreatments, respectively. In addition, we carried out *ex-situ* XPS measurements using an Al $K\alpha$ source (1486.6 eV) to examine the effects of surface plasma nitridation on the dielectric-substrate interface and evaluate the Ge contamination level within the top high-*k* films. In electrical characterization, the capacitance–voltage (C–V) and conductance–voltage (G–V) curves were measured using an HP4284 LCR meter, while the current–voltage (I–V) characteristics were measured using a Keithley 4200 semiconductor analyzer system. We further extracted the series resistance and external inductance or capacitance in measurements and then applied as a correction to the measured capacitance and conductance [16], [17]. The value of the effective trapped charge density (N_{eff}) was determined quantitatively by measuring the hysteresis width at flat-band voltage (V_{FB}) in the bidirectional C–V sweeps [18]. The interface state density (D_{it}) was estimated from both high-low frequency capacitance method [19] and the G–V characteristics using Hill's method [20].

2.3 Effects of Postdeposition Annealing and NH_3 Plasma Pretreatment

2.3.1 Structure and Composition Analyses

Figure 2.1 shows cross-sectional TEM image of as-deposited Pt/HfO_xN_y/Ge structure. We characterized that the thicknesses of the HfO_xN_y bulk film and the IL were ca. 73 Å and ca. 19 Å, respectively. When HfO_xN_y/Ge system undergoes high-temperature process, of primary interest is the resultant germanium diffusion in the overlying HfO_xN_y films. As the SIMS depth profiles illustrated in **Fig. 2.2**, we observed a large Hf tail—a known SIMS artifact—at the end of the HfO_xN_y layer, and ion yield enhancements of both Ge and Hf at the beginning of the Ge substrate. Discarding these artificial phenomena, a U-shaped distribution of Ge did exist inside the overlying HfO_xN_y layer. From the concentration levels, we suggest that the higher thermal annealing indeed enhanced the incorporation of Ge, relative to the concentration in low-temperature processed sample. Assuming that the composition is the mixture of HfO_xN_y and GeO_xN_y, we evaluated the amount of incorporated Ge quantitatively through XPS measurements because of the lack of sputtering yield information for Ge in the HfO_xN_y layer. Considering the respective atomic sensitivity factors of the Ge 2p3, Hf 4f, O 1s, and N 1s core levels, we estimated an average Ge concentration of ca. 12(±1.4) at.% in their overlying high-*k* layers for the 400 °C-processed sample, with the values increasing to ca. 19.3(±2) at.% after 500 °C PDA for 5 min. Such a low-temperature annealing has led to severe Ge incorporation into the HfO_xN_y dielectric film. Note that the maximum sampling depth is ca. 45 Å in Ge 2p3 spectrum, and it exactly involves in a U-shaped distribution of Ge within the high-*k* films, therefore, we use an average value for evaluating the Ge contamination. These Ge atoms are incorporated in the form of GeO_x through both external and internal contamination mechanisms. A higher surface concentration of Ge oxide in the SIMS analyses has been identified as arising from gaseous GeO species diffusing out from the substrate and downward into the high-*k* layer via airborne transportation; the contamination depth has been estimated to be ca. 20 Å—at least for high-*k* thin films deposited on Ge substrates [21]. This kind of surface contamination, however, can be further suppressed by capping a thick SiO_2 layer onto the back side of the Ge substrate prior to performing the annealing process. In addition, bulk contamination of GeO_x may result from the desorption of a defective GeO_x-containing IL and/or the oxidation of the Ge substrate due to residual oxygen existing in a N_2 ambient [22].

2.3.2 Capacitance and Conductance Characteristics

Figure 2.3 displays multi-frequency C–V characteristics of Pt/HfO_xN_y/Ge capacitors before and after performing the 500 °C PDA and PMA, respectively. It should be pointed out that the sweep direction in all of the curves presented here is from strong accumulation to strong inversion and they seem not to reach fully saturation in the accumulation regimes. This phenomenon can be reasonably understood in term of fast detrapping of the trapped charges during the C–V sweep; on the contrary, when the voltage is swept from inversion to accumulation, the normal saturation behavior in C–V curves can be seen, as the results shown in Fig. 6. Here, we extracted the capacitance-equivalent-thickness (CET) at a value of V_g of +2 V in the C–V curves was ca. 28 Å for as-deposited sample; it decreased to ca. 27 Å and ca. 26 Å after PDA and PMA, respectively. Extending the annealing duration to 5 min leads to further CET reduction of ca. 23 Å (not shown here), and it partly arises from the shrinkage of the IL [22] due to the fact that Ge does not prefer to form the germinate $HfGeO_4$ [23], [24]—unlike Si, which readily forms $HfSiO_4$—through reaction with Hf. In addition, we observed that the C–V stretch-out behavior with the hump emerged in depletion for all samples, indicating the existence of a large density of interface states at the dielectric interface. Considering the frequency dependence of the interface properties, the deviation of the 10 kHz curve with respect to the 1 MHz curve was obviously abated by performing subsequent annealing processes. In particular, the PMA-processed sample revealed a deeper “dip” in depletion, indicative of its improved interface quality. The quantitative analyses of the D_{it} showed that the as-deposited HfO_xN_y/Ge gate stack revealed a large value of D_{it} of ca. 8×10^{12} $cm^{-2} \cdot eV^{-1}$ and it reduced to the value of D_{it} of ca. 3.5×10^{12} and ca. 1.4×10^{12} $cm^{-2} \cdot eV^{-1}$ for the PDA and PMA samples, respectively. Interface traps and dangling-bond defects existing in near-interfacial Ge oxide or Ge oxynitride have been characterized in HfO_2/Ge system [25]. Recently, C. O. Chui *et al*. also examined that the level of D_{it} was quite high and still on the order of 10^{12} $cm^{-2} \cdot eV^{-1}$ for GeO_xN_y/Ge gate stack even though receiving forming-gas anneal (FGA) [26]. As a result, we believe that a higher value of D_{it} presented at the HfO_xN_y/Ge interface should be associated with poor quality of the defective GeO_x IL.

Figure 2.4 presents the corresponding *G–V* curves of Pt/HfO_xN_y/Ge gate stacks measured at 100 kHz; the result of Pt/HfO_xN_y/Si control sample is also shown for comparison. The *G–V* traces obviously exhibit an interface loss peak, corresponding to the hump observed in *C–V* depletion. The PMA process reduced the conductance peak that emerged in the *G–V* curve of the as-deposited sample to a greater extent than did the PDA process, which is consistent with the examination of D_{it}. Another noteworthy feature is that we measured a high value of conductance in inversion and it displayed gate-bias independence; this finding is rare for traditional Si MOS capacitors [27]. Generally, the equivalent parallel conductance passes through a peak in weak inversion and drops immediately to a very low value in strong inversion; in other words, an exponential decline of the conductance values should occur, like Si case shown here. In contrast, we observed gate-bias-independent conductance in inversion in our case, suggesting that the minority carriers in the Ge substrate, formed either through the generation/recombination via midgap trap levels or through a diffusion mechanism—do indeed contribute an energy loss in inversion and compete with interface-state loss in depletion [28]. Y. Fukuda *et al*. have investigated the GeO_xN_y/Ge interface properties through the conductance method [29] and they also simultaneously explored the identical inversion conductance [30]. We have observed the anomalous *G–V* characteristics on low-doped (~10^{14} cm^{-3}) Ge substrate for both types; this behavior can be minimized by increasing dopant concentration. C. O. Chui *et al.* characterized the gate-bias-independent conductance in inversion for MOS capacitors with GeO_xN_y dielectric thin film on n-type (ca. 10^{16} cm^{-3}) Ge substrate, but not on p-type (ca. 5×10^{17} cm^{-3}) Ge substrate [26]. We suggest that the onset of this strange behavior in Ge capacitor is strongly dependent on the substrate doping level because this in turn determines the amount of minority carrier and corresponding response time. Moreover, we noticed that the measured capacitance and conductance rose after different thermal processes, which are a typical characteristic of the increased number of bulk traps, presumably caused by impurity atoms introduced during high-temperature annealing. These induced bulky defects in Ge, with energy levels near the midgap, not only contribute to greater bulk trap loss but also enhance the supply of minority carriers to the inversion layer, incurring the low-frequency-like behavior in the 10-kHz *C–V* curves. We suggest that both thermal mechanisms are significant in Ge because of a large intrinsic carrier concentration (ca. 2×10^{13} cm^{-3}) since they obviously affect the room-temperature *C–V* characteristics measured at high frequencies—even as high as 1 MHz [31].

2.3.3 Flatband Voltage Shift and Gate Leakage Characteristics

As indicated in **Fig. 2.5**, we examine the variation of the V_{FB} shift (the left-hand axis) and the gate leakage current J_g (the right-hand axis) with respect to the annealing temperature. It can be seen that the value of V_{FB} for the as-deposited sample (ca. 0.35 V) is lower than the value of the ideal work-function difference (ca. 0.9 eV) between a Pt gate and n-Ge substrate, implying that a substantial number of positive charges have been introduced into the gate dielectric/IL bi-layer. High temperature annealing caused the positive shift of the V_{FB} and increased the J_g considerably to 1×10^{-3} A/cm^2 at (V_{FB} + 1) V after 600 °C PDA; these behaviors are possibly correlated with the degree of GeO volatilization. As far as the positive V_{FB} shift after thermal annealing is concerned, the desorption process of GeO is believed to generate additional negative charges and leads to charge neutralization. W. P. Bai *et al*. have examined that an increase of PMA temperature made the value of V_{FB} shift positively and they interpreted this phenomenon in terms of the out-diffusion of GeO_x from Ge substrate [32]. Another result demonstrated further by N. Wu *et al*. was that the thicker the Si layer capping onto Ge substrate is, the smaller the amount of Ge out-diffusion is. Accordingly, a less positive V_{FB} shift was found owing to the reduction of these negative charges [33]. Furthermore, more severe out-diffusion of GeO was seen upon increasing annealing temperature; this in turn caused the high-*k*/Ge interface degradation [23]. This tendency is obviously different from that observed in the Pt/HfO_xN_y/Si capacitors which depict the reduction in J_g upon increasing PDA temperature. We thus suggest that the GeO_x incorporation into the overlying HfO_xN_y bulk film may form the leakage path and contribute to gate leakage current, especially after annealing at 600 °C.

2.3.4 Influence of NH_3 Plasma Passivation

Most studies have demonstrated that the gate leakage current in high-*k*/Ge systems decreases significantly after receiving surface thermal-annealing in a NH_3 ambient, especially prior to the deposition of HfO_2 dielectric films [34]. We observed similar effects after NH_3 plasma, as presented in the inset of **Fig. 2.6**. The gate leakage was lower after higher-temperature PDA for the NH_3–treated sample relative to that of the HF-last sample. Moreover, plasma treatment reduced the hysteresis loop in the bidirectional *C*–*V* curves measured at 1 MHz (**Fig. 2.6**); reduction of the interface state density to the order of 10^{11} $cm^{-2} \cdot eV^{-1}$ was also achieved. We obtained a corresponding value of N_{eff} of ca. 4.8×10^{12} cm^{-2} for HF-last sample and it decreased to ca. 2.5×10^{12} cm^{-2} after surface nitridation. It was believed that sub-stoichiometric oxide may create a high-density of charge-trapping sites at the dielectric-substrate and they could induce charge trapping and detrapping. The formation of Ge–N chemical bonds and the inhibited growth of GeO_x ($x \leqq 2$) may be responsible for the resulting improved electrical performance. The interposed GeO_xN_y IL may behave as a diffusion barrier and suppress the volatilization of GeO out-diffusion from Ge substrate; therefore, causing a less significant increase in J_g after NH_3 plasma pretreatment.

On the other hand, in order to obtain a deeper insight into the origin of the hysteresis behavior, we separately extended the inversion and accumulation biases in the C–V sweeps and found that the increased inversion bias did lead to an increased hysteresis width, but the increased accumulation bias did not, as is evident in **Fig. 2.7**. This fact implies that hole trapping is the dominant mechanism; the scheme of a charge trapping model for a $Pt/HfO_xN_y/GeO_x/Ge$ gate stack has been proposed in other studies [35]. We conclude that the minority carriers (in this case, holes for n-type Ge) tunnel from the Ge substrate and become trapped at the inner-interface and/or inside the deficient GeO_x interlayer. This process causes the C–V curve to shift negatively with the deviation of the V_{FB} when the sweeping bias is started further from the negative side, i.e, more inversion charges are trapped. In contrast, the C–V curve exhibits its own value of V_{FB} without being trapped when the voltage is swept from accumulation to inversion.

2.3.5 HfO_xN_y/Ge Interface Chemistry

In **Fig. 2.8** and **Fig. 2.9** we investigate the distribution of GeO species in entire structures through analyses of the Ge 2p3 and Ge 3p core levels—a broad band consisting of Ge dioxides and suboxides and elemental Ge. We compared the spectra of these two Ge photoemissions because they allow sampling at significantly different depths. We employed mixed Gaussian–Lorentzian line shapes to reproduce these two Ge core levels from three components—Ge, GeO, and GeO_2. From the high-surface-sensitivity Ge 2p3 spectrum (**Fig. 2.8**), a quite high intensity ratio of the GeO_2 and GeO to the Ge substrate was found for both samples; this feature arose primarily from the surface contamination of GeO_x ($x \leqq 2$). The average Ge concentration estimated within the top of high-*k* bulk layer is ca. 12(±1.4) at.% for HF-last sample; with the value can be reduced to ca. 4.8 at.% providing that the Ge substrate receives surface pretreatment of NH_3 plasma. Subsequently annealing the NH_3 sample at 600 °C for 30 s causes the Ge concentration increasing to the value of ca. 14 at.%. From the concentration levels, we found that NH_3 pretreatment did assist to minimize Ge incorporation behavior during annealing with respect to the result obtained in HF-last sample that the Ge contamination was up to ca. 19.3(±2) at.% after annealing at 500 °C for 5 min. However, we suggest that the finite improvements in characteristics of NH_3-treatment samples as compared to the literatures [14], [33] using another passivation technique—the Si interlayer on Ge—can be attributed to the incomplete passivation of the dangling bonds on the Ge surface; such a surface would not fully diminish the formation of GeO_x. Lower dissociated temperature (ca. 500 °C) of Ge–N bonds [15] is a major cause to result in a still higher concentration of Ge observed after high-temperature processing.

In contrast, the Ge 3p spectrum (**Fig. 2.9**) clearly demonstrated that the intensity from the GeO_x ($x \leqq 2$) was lower than that from the substrate after NH_3 plasma nitridation, especially for inhibiting a large amount of Ge suboxides; these phenomena are the opposite of that observed for the non-nitrided high-*k*/Ge sample. Our explanation for this experimental finding is that the Ge 3p core level is capable of examining the amount of Ge oxide existing at the high-*k*/Ge interface since it possesses a higher sampling depth (ca. 80 Å) relative to that (ca. 34 Å) of the Ge 2p3 spectrum [36]. Accordingly, such a low oxide/substrate emission ratio after performing the nitridation process is a direct result of NH_3 plasma pretreatment diminishing the number of GeO_x ($x \leqq 2$) defects at the interface; in other words, the reduced charge trapping centers is achieved. These results also imply that surface nitridation does indeed assist in enhancing the thermal stabilities of Pt/HfO_xN_y/Ge MOS structures.

2.4 Passivation of Ultrathin Si Capping Layer

2.4.1 Composition and Interfacial Physical Analyses

Figure 2.10 displays the SIMS depth profiles of the chemical species present in the HfO_xN_y films on the Ge substrates (a) in the absence and (b) presence of the Si capping layer. We estimate that the overall thicknesses of the bulk HfO_xN_y and IL were ca. 90 Å and >100 Å before and after Si passivation, respectively; the probable chemical composition is also identified. An important feature of the HfO_xN_y layer was that the distribution profile of Ge was U-shaped; the subsequent PDA process enhanced the incorporation behavior, provided that Si_2H_6 passivation was not performed. The amount of incorporated Ge was reduced ca. fourfold after capping with the ca. 8-Å-thick Si layer; further retardation of Ge chemical species into the overlying high-*k* dielectric was achieved after subsequent annealing under the same conditions. This finding provides strong evidence that employing a Si capping layer on a Ge substrate improves the thermal stability of HfO_xN_y/Ge gate stacks.

Figure 2.11(a) displays the Si 2*p* and Ge 2*p* core-level XPS spectra of the Ge substrate having the Si capping layer both before and after deposition of Pt/HfO_xN_y bi-layers. Prior to deposition, two well-resolved peaks—originating from the signals of the Si capping layer and the Ge substrate, respectively—appeared in corresponding core-level spectra; i.e., the native oxide was absent. After completing the entire MIS fabrication process, most of the Si atoms had transformed into Si dioxide and Hf-silicate, with some nitrogen-related bonds formed;

meanwhile, GeO_x ($x \leqq 2$) emerged at the top surface and also in the bulk of the high-*k* layer. Next, in **Fig. 2.11(b)**, we compared the relative intensities of the Ge 2*p* levels of the four SIMS samples investigated in **Figs. 2.10(a) and 2.10(b)**, respectively; because of the lack of sputtering yield information for Ge in the HfO_xN_y layer, we performed XPS analyses to evaluate the amounts of incorporated Ge. We estimate Ge concentrations of ca. 13% and ca. 4.3% for the non-annealed samples lacking and containing the Si capping layer, respectively, with these values increasing to ca. 19.6% and ca. 6.1%, respectively, after dielectric annealing. The non-annealed high-*k* dielectric sample lacking the surface passivation layer exhibited a severe degree of Ge diffusion into the top HfO_xN_y film even when post-metallization annealing (PMA) was performed at only 400 °C. Because the Ge 2*p* core level displays higher surface sensitivity [36], the GeO_x species detected in the Ge 2*p* spectrum arose possibly through one of two incorporation mechanisms: (a) out-diffusion of gaseous GeO species from the substrate and downward into the high-*k* layer through airborne transportation [21]; (b) GeO volatilization from the IL and top surface of the Ge substrate. From the viewpoint that the same GeO desorption rate would be expected for mechanism (a), it is reasonable to attribute the obvious increase in the GeO_x intensity of the sample lacking the Si capping layer, with respect to that of the sample containing one, to contamination of GeO in the bulk of the high-*k* layer; this hypothesis is in agreement with the SIMS data.

2.4.2 Capacitance Characteristics and Charge Trapping Model

Figure 2.12 displays the bidirectional sweep (1 MHz) C–V curves of the Pt/HfO_xN_y/Ge gate stacks lacking and containing Si capping layers. We found that increasing the capping layer thickness suppressed the hysteresis width dramatically; its value reduced to ca. 20 mV upon increasing the thickness of the Si capping layer to ca. 13 Å. This tendency is quite consistent with the recent results reported by N. Wu *et al* [33]. Moreover, the V_{FB} returned to the work-function difference of ca. 0.8 eV between the Pt gate and the n-Ge substrate or undoped Si layer, indicating that the addition of the Si capping layer also eliminated the fixed positive charges in the gate dielectric. Our explanation for these phenomena is that it is more likely that SiO_x and its silicate will form, rather than GeO_x, after deposition and annealing when the Si capping layer is present because Si–O bonds have larger Gibbs free energies and higher thermodynamical stabilities [37]. Therefore, the formation of GeO at the interface and its out-diffusion are suppressed significantly upon increasing the thickness of the Si layer. Also, we believe that the exacerbated hysteresis width might be due to the high-density of charge-trapping sites at the high-k/GeO_x interface and/or within the defective GeO_x IL. We found that the increased inversion bias did lead to an increased hysteresis width, but the increased accumulation bias did not (not shown), implying that the hole trapping mechanism was dominant. **Fig. 2.13** displays our proposed charge trapping model for the Pt/HfO_xN_y/GeO_x/Ge gate stack; the energy bandgaps of each material and their corresponding electron affinities are literature data [38]-[41]. As seen in **Fig. 2.13(a)**, the minority carriers (in this case, holes for n-type Ge) tunnel from the Ge substrate and become trapped at the inner-interface and/or within the deficient GeO_x interlayer. This phenomenon causes the C–V curve to shift negatively, and the value of V_{FB} to deviate, when the voltage was swept further toward the negative side. In contrast, the C–V curve exhibited its own value of V_{FB} without being trapped when the voltage was swept from accumulation to inversion. These results were further confirmed by the larger gate leakage current observed in the accumulation regime, with respect to that in the inversion regime, because of the higher probability of Fowler–Nordheim (F–N) tunneling and thermionic emission occurring, as indicated in **Fig. 2.13(b)**.

2.5 Conclusions

In Chapter 2, we first studied the thermal stability of the as-deposited HfO_xN_y thin films on the Ge substrate by employing rapid thermal annealing. After undergoing high temperature processing, we observed several interesting physical and electrical features presented in the HfO_xN_y/Ge system, including a large Ge out-diffusion (> 15 at.%) into high-*k* films, positive V_{FB} shift, severe charge trapping, and increased leakage current. These phenomena are closely related to the existence of GeO_x defective layer and the degree of resultant GeO volatilization. We abated these undesirable effects, especially for reducing the amount of Ge incorporation (< 5 at.%) and the sub-stoichiometric oxide at dielectric-substrate interface, through performing NH_3 plasma pretreatment on the Ge surface. These improvements can be interpreted in terms of a surface nitridation process that enhanced the thermal stability of the high-*k*/Ge interface. Moreover, we also adopted the Si_2H_6 thermal pretreatment to relieve Ge out-diffusion in HfO_xN_y/Ge capacitors. It was found that capping an ultrathin Si layer onto a Ge substrate retarded GeO volatilization and suppressed oxide charge trapping in the MIS structures and, thus, enhanced the thermal stabilities of entire HfO_xN_y/Ge MIS structures. We provide herein a schematic energy band diagram to explain the resultant charge trapping behavior in these systems.

References (Chapter 2)

[1] R. Li, S. J. Lee, H. B. Yao, D. Z. Chi, M. B. Yu, and D. L. Kwong, “Pt-germanide Schottky source/drain germanium p-MOSFET with HfO_2 gate dielectric and TaN gate electrode,” *IEEE Electron Device Lett*., vol. **27**, p. 476, 2006.

[2] Y.-L. Chao and J. C. S. Woo, “Reduction of parasitic resistance of self-aligned copper germanide for germanium p-MOSFETs,” *Ext. Abst. Int. Conf. on Solid State Devices and Materials* (*SSDM*), p. 1052, 2006.

[3] A. Ritenour, S. Yu, M. L. Lee, N. Lu, W. Bai, A. Pitera, E. A. Fitzgerald, D. L. Kwong, and D. A. Antoniadis, “Epitaxial strained germanium p-MOSFETs with HfO_2 gate dielectric and TaN gate electrode,” *Tech. Dig. Int. Electron Devices Meet*., p. 433, 2003.

[4] C. H. Huang, M. Y. Yang, A. Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, “Very low defects and high performance Ge-on-insulator p-MOSFETs with Al_2O_3 gate dielectrics,” *Tech. Dig. VLSI Symp*., p. 119, 2003.

[5] *The International Technology Roadmap for Semiconductors (ITRS)*, http://public.itrs.net, 2004.

[6] O. Weber, F. Andrieu, M. Cass, T. Ernst, J. Mitard, F. Ducroquet, J.-F. Damlencourt, J.-M. Harmann, D. Lafond, A.-M. Papon, L. Militaru, L. Thevenod, K. Romanjek, C. Leroux, F. Martin, B. Guillaumot, G. Ghibaudo, and S. Deleonibus, “Experimental determination of mobility scattering mechanisms in Si/HfO_2/TiN and SiGe:C/HfO_2/TiN surface channel n- and p-MOSFETs,” *Tech. Dig. Int. Electron Devices Meet*., p. 867, 2004.

[7] C. S. Kang, H.-J. Cho, K. Onishi, R. Choi, R. Nieh, S. Gopalan, S. Krishnan, and J. C. Lee, “Improved thermal stability and device performance of ultra-thin (EOT<10 Å) gate dielectric MOSFETs by using hafnium oxynitride (HfO_xN_y),” *Tech. Dig. VLSI Symp*., p. 146, 2002.

[8] H. C.-H. Wang, C.-W. Tsai, S.-J. Chen, C.-T. Chan, H.-J.Lin, Y. Lin, H.-J. Tao, S.-C. Chen, C. H. Diaz, T. Ong, A. S. Oates, M.-S. Liang, and M.-H. Chi, “Reliability of

HfSiON as gate dielectric for advanced CMOS technology," *Tech. Dig. VLSI Symp.*, p. 170, 2005.

[9] A. L. P. Rotondaro, M. R. Visokay, J. J. Chambers, A. Shanware, R. Khamankar, H. Bu, R. T. Laaksonen, L. Tsung, M. Douglas, R. Kuan, M. J. Bevan, T. Grider, J. Mcpherson, L. Colombo, "Advanced CMOS transistors with a novel HfSiON gate dielectric," *Tech. Dig. VLSI Symp.*, p. 148, 2002.

[10] T. Yamaguchi, R. Iijima, T. Ino, A. Nishitama, H. Satake, and N. Fukushima, "Additional scattering effects for mobility degradation in Hf-silicate gate MISFETs," *Tech. Dig. Int. Electron Devices Meet.*, p. 621, 2002.

[11] M. Houssa, T. Conard, F. Bellenger, G. Mavrou, Y. Panayiotatos, A. Sotiropoulos, A. Dimoulas, M. Meuris, M. Caymax, and M. M. Heynsa, "Electrical properties of atomic-beam deposited $GeO_{1-x}N_x/HfO_2$ gate stacks on Ge," *J. Electrochem. Soc.*, vol. **153**, p. G1112, 2006.

[12] S. Zhu, R. Li, S. J. Lee, M. F. Li, A. Du, J. Singh, C. Zhu, A. Chin, and D. L. Kwong, "Germanium pMOSFETs with Schottky-barrier germanide S/D, high-*k* gate dielectric and metal gate," *IEEE Electron Device Lett.*, vol. **26**, p. 81, 2005.

[13] N. Lu, W. Bai, A. Ramirez, C. Mouli, A. Ritenour, M. L. Lee, D. Antoniadis, and D. L. Kwong, "Ge diffusion in Ge metal oxide semiconductor with chemical vapor deposition HfO_2 dielectric," *Appl. Phys. Lett.*, vol. **87**, p. 051922, 2005.

[14] N. Wu, Q. Zhang, C. Zhu, D. S. H. Chan, A. Du, N. Balasubramanian, M. F. Li, A. Chin, and J. K. O. Sin, "A TaN-HfO_2-Ge pMOSFET with novel SiH_4 surface passivation," *IEEE Electron Device Lett.*, vol. **25**, p. 631, 2004.

[15] K. Prabhakaran and T. Ogino, "Selective bond-breaking and bond-making in oxynitride of Si and Ge: a case of chemical bond manipulation," Surf. Sci., vol. **387**, p. L1068, 1997.

[16] W. H. Wu, B. Y. Tsui, Y. P. Huang, F. C. Hsieh, M. C. Chen, Y. T. Hou, Y. Jin, H. J. Tao, S.

C. Chen, and M. S. Liang, "Two-frequency C-V correction using five-element circuit model for high-*k* gate dielectric and ultrathin oxide," *IEEE Electron Device Lett*., vol. **27**, p. 399, 2006.

[17] H.-T. Lue, C.-Y. Liu, and T.-Y. Tseng, "An improved two-frequency method of capacitance measurement for $SrTiO_3$ as high-k gate dielectric," *IEEE Electron Device Lett*., vol. **23**, p. 553, 2002.

[18] M.-K. Lee, C.-F. Yen, J.-J. Huang, and S.-H. Lin, "Electrical characteristics of postmetallization-annealed MOCVD-TiO_2 films on ammonium sulfide-treated GaAs," *J. Electrochem. Soc*., vol. **153**, p. F266, 2006.

[19] D. K. Schroder, *Semiconductor Material and Device Characterization*, 2*nd* ed., pp. 368–378, John Wiley & Sons, Inc., New York, 1998.

[20] W. A. Hill and C. C. Coleman, "A single-frequency approximation for interface-state density determination," *Solid-State Electron*., vol. **23**, p. 987, 1980.

[21] Q. Zhang, N. Wu, D. M. Y. Lai, Y. Nikolai, L. K. Bera, and C. Zhu, "Germanium incorporation in HfO_2 dielectric on germanium substrate," *J. Electrochem. Soc*., vol. **153**, p. G207, 2006.

[22] C.-C. Cheng, C.-H. Chien, C.-W. Chen, S.-L. Hsu, C.-H. Yang, and C.-Y. Chang, "Effects of postdeposition annealing on the characteristics of HfO_xN_y dielectrics on germanium and silicon substrates," *J. Electrochem. Soc*., vol. **153**, p. F160, 2006.

[23] C.-C. Cheng, C.-H. Chien, J.-H. Lin, C.-Y. Chang, G.-L. Luo, C.-H. Yang, and S.-L. Hsu, "Thermochemical reaction of $ZrO_x(N_y)$ interfaces on Ge and Si substrate," *Appl. Phys. Lett*., vol. **89**, p. 012905, 2006.

[24] P. M. Lambert, "Hafnium germanate from a hydrous hafnium germanium oxide gel," *Inorg. Chem.,* vol. **37**, p. 1352, 1998.

[25] V. V. Afanas'ev, Y. G. Fedorenko, and A. Stesmans, "Interface traps and dangling-bond defects in (100)Ge/HfO_2," *Appl. Phys. Lett*. vol. **87**, p. 032107, 2005.

[26] C. O. Chui, F. Ito, and K. C. Saraswat, “Nanoscale germanium MOS dielectrics—Part I: Germanium oxynitrides,” *IEEE Trans. Electron Devices*, vol. **53**, p. 1501, 2006.

[27] D. Flandre, F. Campabadal, J. Esteve, E. Lora-Tamayo, and F. V. D. Wiele, “ac capacitance and conductance measurements of two-terminal metal-oxide-semiconductor-oxide-semiconductor capacitors on silicon-on-insulator substrates,” *J. Appl. Phys.*, vol. **70**, p. 5111, 1991.

[28] E. H. Nicollian and J. R. Brews, *MOS* (*Metal Oxide Semiconductor*) *Physics and Technology*, John Wiley & Sons, Inc., New York, 1982.

[29] Y. Fukuda, T. Ueno and S. Hirono, “Electrical behavior of germanium oxide/germanium interface prepared by electron-cyclotron-resonance plasma oxidation in capacitance and conductance measurements,” *Jap. J. Appl. Phys.*, vol. **44**, p. 7928, 2005.

[30] Y. Fukuda, T. Ueno, S. Hirono and S. Hashimoto, “Electrical characterization of germanium oxide/germanium interface prepared by electron-cyclotron-resonance plasma irradiation,” *Jap. J. Appl. Phys.*, vol. **44**, p. 6981, 2005.

[31] A. Dimoulas, G. Vellianities, G. Mavrou, E. K. Evangelou, and A. Sotiropoulos, “Intrinsic carrier effects in HfO_2–Ge metal–insulator–semiconductor capacitors,” *Appl. Phys. Lett.*, vol. **86**, p. 223507, 2005.

[32] W. P. Bai, N. Lu, and D.-L. Kwong, “Si interlayer passivation on germanium MOS capacitors with high-*k* dielectric and metal gate,” *IEEE Electron Device Lett.*, vol. **26**, p. 378, 2005.

[33] N. Wu, Q. Zhang, D. S. H. Chan, N. Balasubramanian, and C. Zhu, “Gate-first germanium nMOSFET with CVD HfO_2 gate dielectric and silicon surface passivation,” *IEEE Electron Device Lett.*, vol. **27**, p. 479, 2006.

[34] N. Wu, Q. Zhang, C. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, B. J. Cho, A. Chin, D.-L. Kwong, A. Y. Du, C. H. Tung, and N. Balasubramanian, “Effect of surface NH_3 anneal on the physical and electrical properties of HfO_2 films on Ge substrate,” *Appl.*

Phys. *Lett*., vol. **84**, p. 3741, 2004.

[35] C.-C. Cheng, C.-H. Chien, G.-L. Luo, C.-H. Yang, M.-L. Kuo, J.-H. Lin, and C.-Y. Chang, “Ultrathin Si capping layer suppresses charge trapping in HfO_xN_y/Ge metal-insulator-semiconductor capacitors,” *Appl*. *Phys*. *Lett*., vol. **90**, p. 012905, 2007.

[36] *NIST Electron Inelastic-Mean-Free-Path Database 71 (v. 1.1)*, National Institute of Standards and Technology, 2000.

[37] I. Barin and O. Knacke, *Thermochemical Properties of Inorganic Substances* (Berlin, Springer, 1977).

[38] W.-J. Zhu, T.-P. Ma, T. Tamagawa, J. Kim, and Y. Di, “Current transport in metal/hafnium oxide/silicon structure,” *IEEE Electron Device Lett*. vol. **23**, p. 97, 2002.

[39] V. V. Afanas’ev and A. Stesmans, “Energy band alignment at the (100)Ge/HfO_2 interface,” *Appl. Phys. Lett*. vol. **84**, p. 2319, 2004, and references 3, 14, and 15 cited within.

[40] K.-L. Seo, P. C. Mclntyre, S. Sun, D.-L. Lee, P. Pianetta, and K. C. Saraswat, “Chemical states and electronic structure of a HfO_2/Ge(001) interface,” *Appl. Phys. Lett*. vol. **87**, p. 042902, 2005.

[41] M. Liu, Q. Fang, G. He, L. Li, L. Q. Zhu, G. H. Li, and L. D. Zhang, “Effect of post deposition annealing on the optical properties of HfO_xN_y films,” *Appl. Phys. Lett*. vol. **88**, p. 192904, 2006.

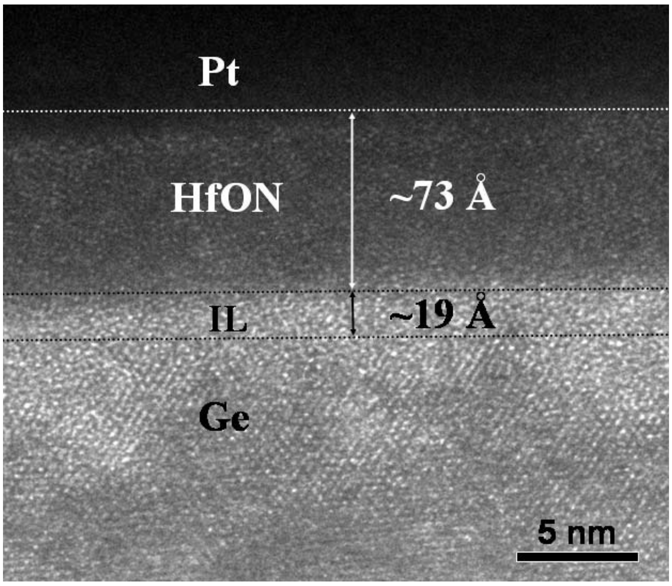


Fig. 2.1 Cross-sectional TEM image of as-deposited Pt/HfO$_x$N$_y$/Ge gate stack.

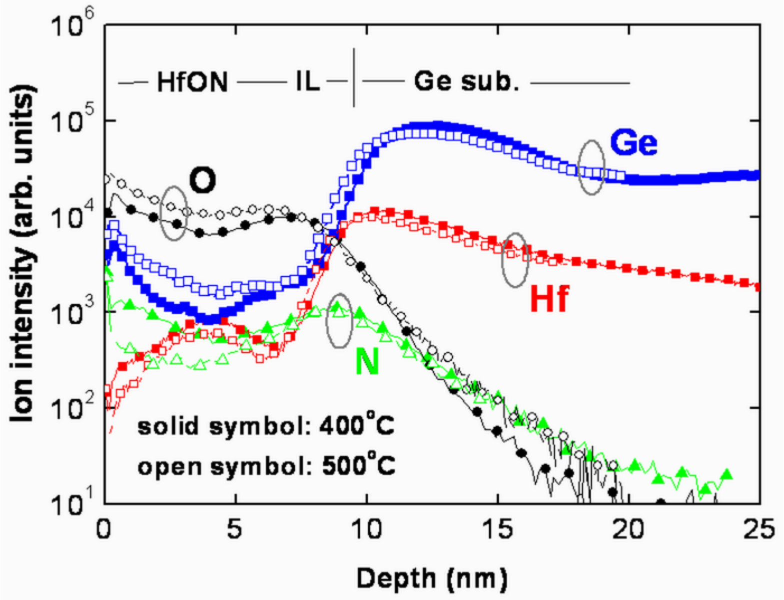


Fig. 2.2 SIMS profiles of as-deposited HfO$_x$N$_y$/Ge gate stack after two different annealing conditions: (a) 400 °C, 30 s; (b) 500 °C, 5 min.

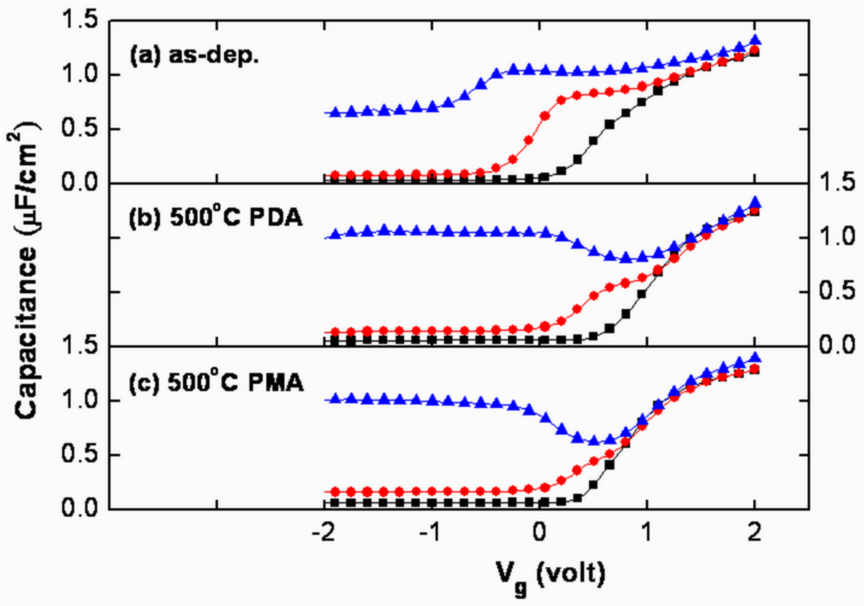


Fig. 2.3 Multi-frequency *C*–*V* curves of Pt/HfO$_x$N$_y$/n-Ge capacitors measured at 10 kHz (▲), 100 kHz (●), and 1MHz (■): (a) as-deposited; (b) 500 °C PDA, 30 s; (c) 500 °C PMA, 30 s.

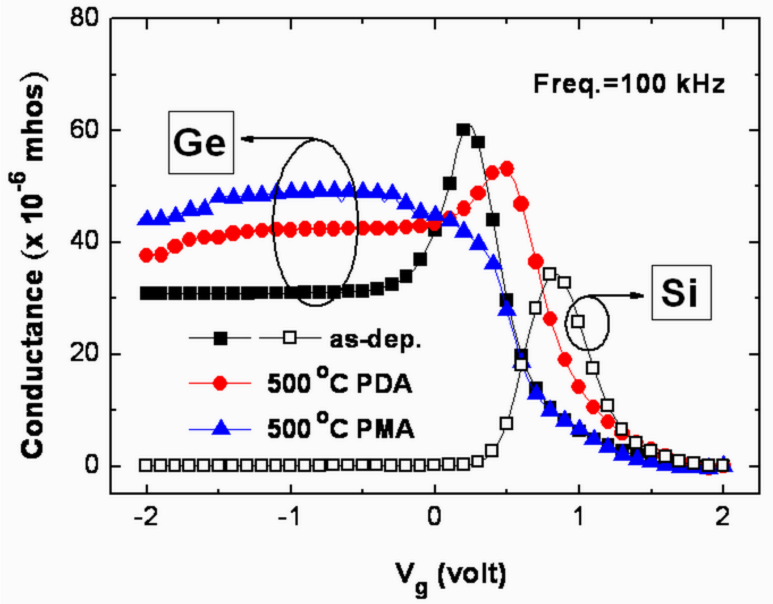


Fig. 2.4 Typical 100-kHz *G*–*V* curves of as-deposited and annealed Pt/HfO$_x$N$_y$/n-Ge capacitors (solid symbols); the annealing duration is 30 s for these two thermal processes. Note that the *G*–*V* curve of as-deposited Pt/HfO$_x$N$_y$/n-Si capacitor (open squares) is added for comparison.

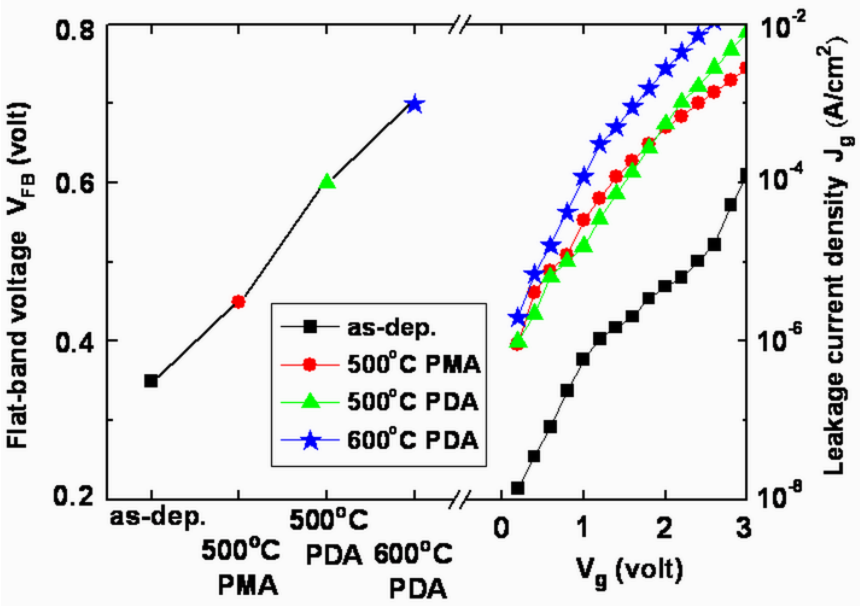


Fig. 2.5 The V_{FB} shift (the left y-axis) and I–V characteristics (the right y-axis) of Pt/HfO$_x$N$_y$/n-Ge capacitors subjected to different thermal processing.

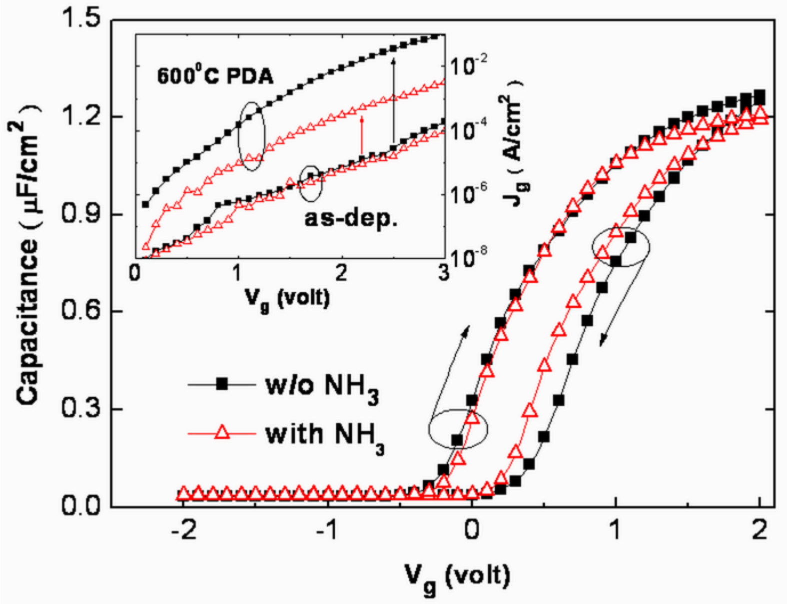


Fig. 2.6 Bidirectional sweep (1 MHz) C–V curves of Pt/HfO$_x$N$_y$/n-Ge capacitors prepared without (■) and with (△) NH$_3$ nitridation. The inset displays the corresponding plots of J_g versus V_g before and after PDA at 600 °C.

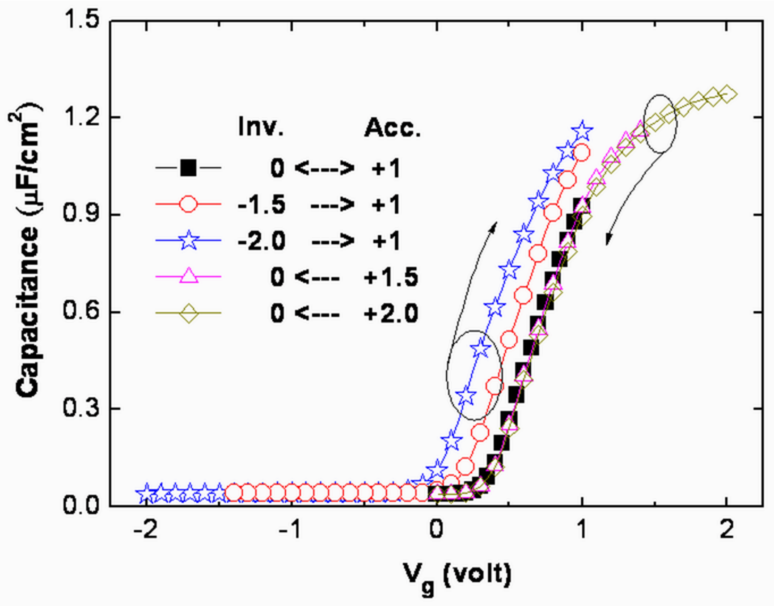


Fig. 2.7 Dependence of the hysteresis width in *C*–*V* (1 MHz) sweep on the starting accumulation and inversion gate biases; the absence of the hysteresis behavior in the gate-bias ranged from 0 to 1 V.

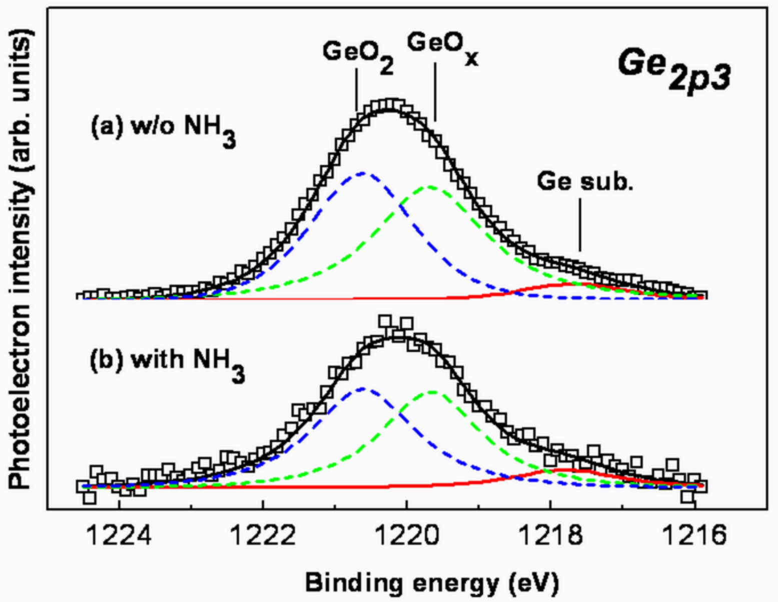


Fig. 2.8 Ge 2p3 XPS spectra of Pt/HfO_xN_y/Ge capacitors prepared without and with NH_3 nitridation. Three components were extracted: Ge, GeO_x, and GeO_2.

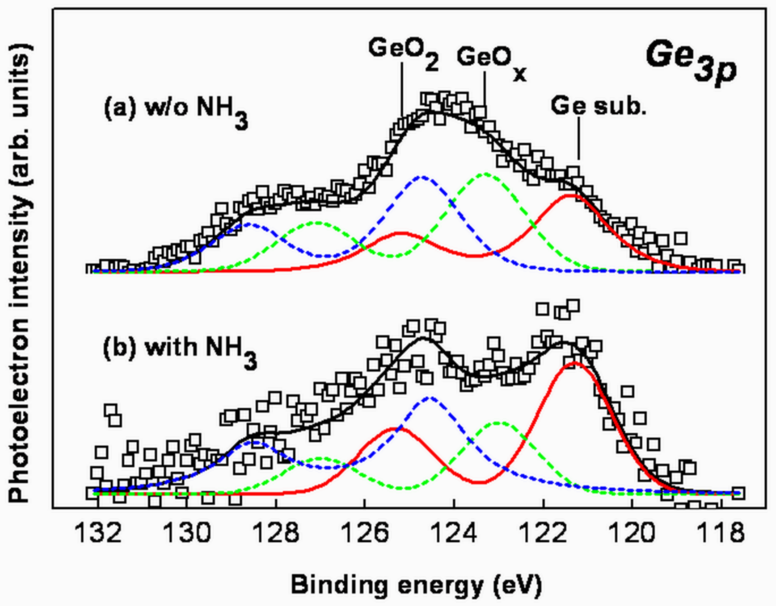


Fig. 2.9 Ge 3p XPS spectra of Pt/HfO_xN_y/Ge capacitors prepared without and with NH_3 nitridation. Three components were extracted: Ge, GeO_x, and GeO_2.

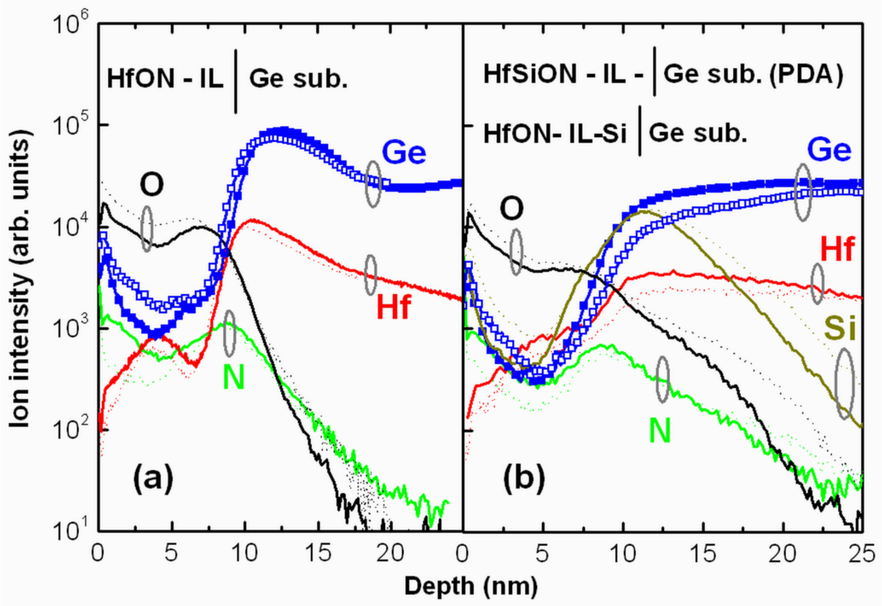


Fig. 2.10 SIMS profiles of HfO_xN_y thin films deposited on Ge substrates (a) without and (b) with Si passivation. The solid lines (—) and solid squares (■) refer to the as-deposited samples; the dotted lines (---) and open squares (□) refer to the annealed samples (500 °C, 5 min).

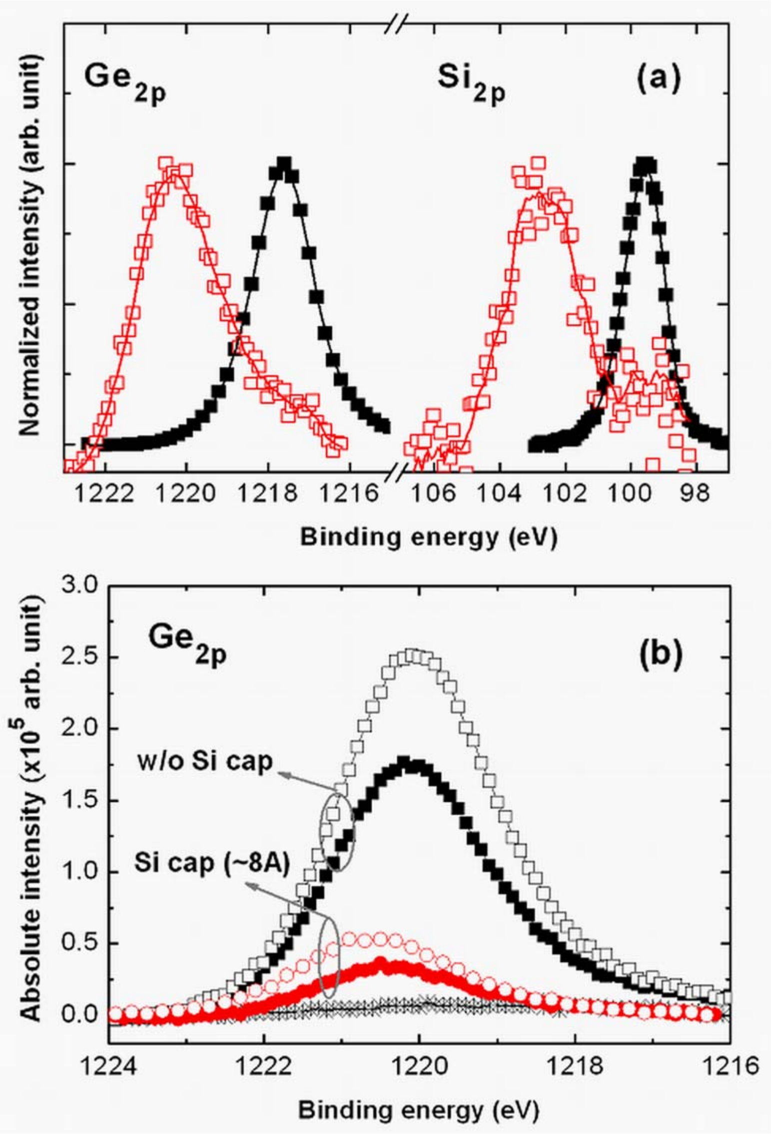


Fig. 2.11 (a) XPS spectra displaying the Si 2*p* and Ge 2*p* core levels for Ge samples capped with a Si layer (ca. 8 Å) before (■) and after (□) deposition of the HfO$_x$N$_y$ high-*k* film. (b) Ge 2*p* spectra of Pt/HfO$_x$N$_y$/Ge gate stacks before (solid symbols) and after (open symbols) dielectric annealing at 500 °C for 5 min. Note that the lowest curve (∗) indicates that no Ge was incorporated into the high-*k* film when thermal processing—PDA and PMA—was not undertaken.

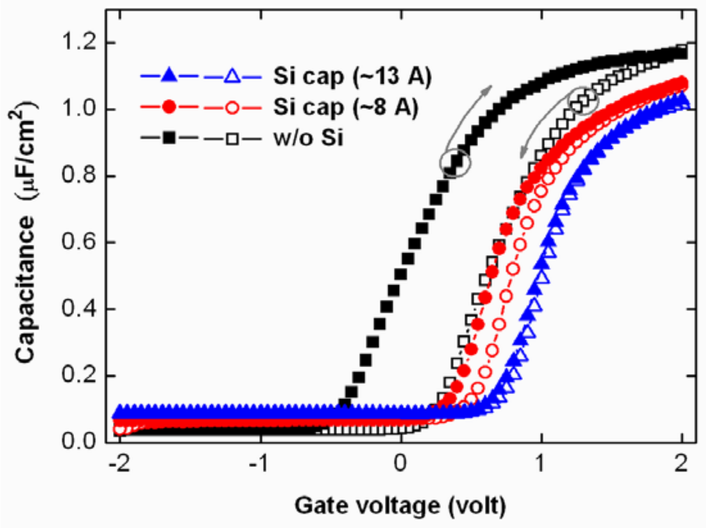


Fig. 2.12 Bidirectional sweep (1 MHz) *C–V* curves of Pt/HfO_xN_y/Ge gate stacks lacking and containing a Si capping layer. HfO_xN_y was the as-deposited thin film and the capacitors were only subjected to 400 °C PMA.

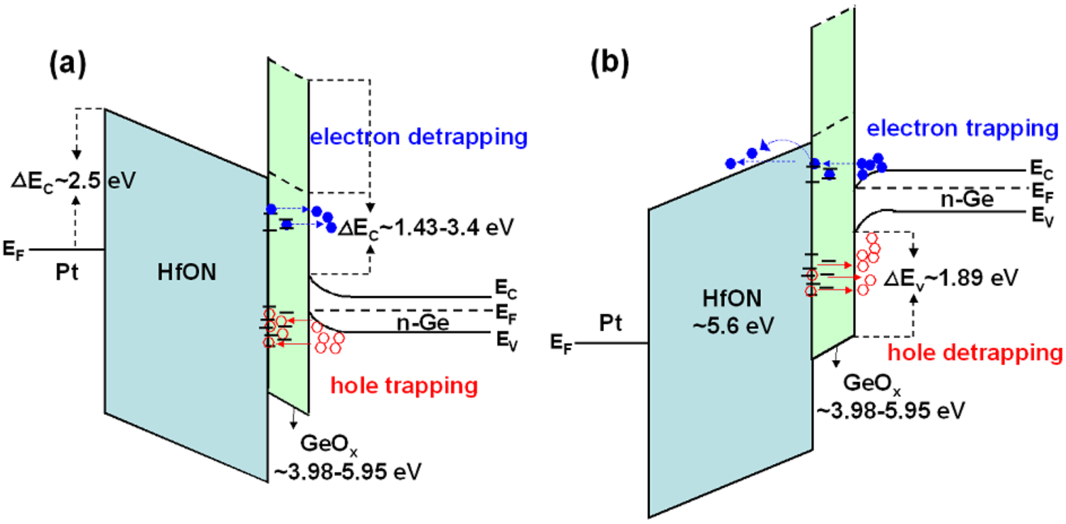


Fig. 2.13 Schematic energy band diagram displaying the charge trapping model for a Pt/HfO_xN_y/GeO_x/Ge gate stack upon (a) sweeping from the inversion bias ($V_g = V_{FB} - 1$ V) and (b) sweeping from the accumulation bias ($V_g = V_{FB} + 1$ V). Note that the value of V_{FB} was ca. 0.5 V.

Chapter 3

Atomic-Layer-Deposited Al_2O_3 Dielectric Films on Bulk Ge Substrates

3.1 Introduction

High-*k* Al_2O_3 is considered a potential alternative gate dielectric material on Si substrates for application to metal oxide semiconductor field effect transistors (MOSFETs) because of its wide bandgap energy (ca. 8.8 eV), large conduction/valance band offsets, and high thermodynamic stability. Nevertheless, there are several drawbacks affecting the deposition of Al_2O_3 on Si, relative to SiO_2, including the low crystallization temperature, the high thermal expansion coefficient, and the high densities of negative fixed charges and interface states (D_{it}). Recent progress in the deposition of high-*k* materials—e.g., the use of deposition techniques such as atomic layer deposition (ALD)—has meant that some of these problems can be overcome [1]. Several reports have described the characteristics of ALD-Al_2O_3 dielectric films grown on Si using trimethylaluminum [TMA, $Al(CH_3)_3$] as the precursor and H_2O as the oxidant because of the excellent ALD mechanism and broad process window [2], [3]. In recent years, many investigators have studied the deposition of ALD-HfO_2 high-*k* layers on high-mobility Ge substrates [4] using a variety of oxidants [5] in efforts aimed at enhancing the driving current in MOSFETs. Meanwhile, various surface preparation techniques—e.g., the incorporation of ultra-thin Si [6], [7], AlN_x, and GeON dielectric interlayers [8], [9], plasma treatment with NH_3 or PH_3 [10], [11], and chemical passivation with $(NH_4)_2S$ [12]—have been developed to enhance the electrical performance of Ge capacitors and transistors [13] because the primary obstacle affecting the fabrication of high-*k*/Ge structures is the presence of GeO_x native oxides and their thermal desorption, which debase the Ge device characteristics, e.g., to provide a high value of D_{it}, a large gate leakage current, and severe charge trapping.

In this chapter, we analyzed the composition and interfacial chemistry of ALD-Al_2O_3 dielectrics deposited on bulk Ge substrates at temperatures in the range of 50–300 °C; subsequent thermal processing strongly influenced the structural stability and electrical properties of the Al_2O_3/Ge system. Interestingly, an uncommon electrical characteristic—fast minority carrier response—has been manifested during electrical measurements of Ge MOS capacitors; its variation with respect to the interface state response is also a noteworthy issue that requires clarification. In fact, many years ago, Nicollian and Brews [14] foresaw that it would be possible to observe a low-frequency (LF) C–V curve for a narrow-gap material, such as Ge, at the standard high-frequency (HF) used for traditional Si because of the higher intrinsic carrier concentration (n_i). Such minority carrier characteristics for capacitors deposited on Si substrates have been established, correlated to the effects of the temperature, doping concentration, and impurity contamination, but similar studies using Ge substrates remain rare [15]–[17]. The influences of the doping concentration and the substrate type on this anomalous C–V behavior have been discovered in high-k/Ge MOS capacitors [9], [18]; the fundamental mechanisms were clarified through fitting of MOS equivalent circuit models [15], [16] and measurements of Arrhenius-dependent conductance properties [17], respectively. In the second part, we utilized a two-dimensional MEDICI numerical simulator, accompanied by theoretical calculations, to investigate the minority carrier response comprehensively—as functions of the doping concentration, measured frequency, and temperature—in terms of the electrical properties of Ge and Si MOS capacitors. We have also examined the underlying mechanistic differences through practical admittance measurements of ALD-Al_2O_3 thin films on both types of Ge substrates.

3.2 Experimental Procedures and MEDICI Simulation Program

3.2.1 ALD-Al_2O_3 Growth and Capacitor Fabrication

The p-Ge substrate had a doping concentration of ca. 2 × 10^{15} cm^{-3} (resistivity ca. 2 Ω·cm). All wafers were pre-cleaned through a cyclic rinse with dilute hydrofluoric acid and deionized water. The Al_2O_3 thin films were grown on the bulk Ge at substrate temperatures of 50, 100, 200, and 300 °C, respectively, while maintaining the chamber pressure at 10 torr in the ALD system. $Al(CH_3)_3$ and H_2O were chosen as the Al metal source and oxidant, respectively; they were pulsed alternately into the reactor for 1 s per pulse, separated by a N_2 purge of 10 s to remove redundant reactants. Next, a 700-Å-thick layer of Pt was deposited using a sputtering system to pattern the capacitor electrode through the shadow mask. Two post-thermal processes were tested: (i) rapid thermal annealing (RTA) at 400 or 600 °C in a N_2 ambient for 30 s and (ii) forming gas annealing (FGA) at 300 °C in a H_2/N_2 (10%) mixed ambient for 30 min. Finally, a thermal coater Al was deposited as the backside contact. Optical microscopy revealed that the gate capacitance area was ca. 4 × 10^{-4} cm^2.

Physical analyses—high-resolution transmission electron microscopy (HRTEM), secondary ion mass spectroscopy (SIMS), grazing-incidence x-ray reflectivity (GI-XRR), and x-ray photoelectron spectroscopy (XPS)—were performed to investigate the as-deposited Al_2O_3/Ge structure and its compositional variation after thermal annealing. The GI-XRR system employed parallel collimated and monochromatic beams (Cu Kα radiation; $\lambda = 1.5406$ Å) and a scanned angle ranging from 0 to 7600 arc-seconds. The reflected X-ray signal was analyzed using a commercial Bede REFS Mercury software package based on the four-layered stack model; the available data in experiments were applied to minimize the cost function χ^2 and more accurately extract all the parameters during curve fitting. For XPS analysis, an Al Kα excitation source operating at 1486.6 eV was employed to collect the photoelectrons at a take-off angle of 60° with respect to the surface horizontal. These measurements allowed us to examine not only the density and stoichiometry of the Al_2O_3 dielectric films but also the interfacial GeO_x chemistry and thermal diffusion behavior within the high-*k* dielectric. For electrical characterization, the parallel capacitance–voltage (*C*–*V*), parallel conductance–voltage (*G*–*V*), and gate leakage (*I*–*V*) behavior of Pt/ALD-Al_2O_3/p-Ge MOS structures were measured. Nicollian and Goetzberger's conductance method considering the fluctuation of surface band bending was used to determine the value of D_{it} [14].

For understanding the minority-carrier behavior in Ge MOS capacitors, we prepared p- and n-type Ge wafers that were doped with Ga and Sb dopants at levels of ca. 2×10^{15} and ca. 1×10^{14} cm^{-3}, respectively. The Si wafer having a standard doping concentration of ca. 1×10^{16} cm^{-3} was also studied for comparison. All wafers were pre-cleaned through a cyclic rinse with dilute hydrofluoric acid and deionized water. Here, the ALD-Al_2O_3 high-*k* layer was deposited at 100 °C, in which the physical thickness was ca. 64(±2) Å according to the established growth rate of ca. 1.06 Å/cycle. Pt and Al metals were deposited as the top and bottom capacitor electrodes, respectively. In final, the entire MOS structure underwent 300 °C FGA for 30 min. The parallel-mode *C*–*V* and *G*–*V* characteristics were measured and they were corrected by excluding the series resistance and parasitic components [19]. The temperature- and frequency-dependent electrical curves in depletion and weak inversion were investigated to explore the minority carrier response mechanisms.

3.2.2 MEDICI Simulator

The computer simulation program MEDICI has been employed to predict the semiconductor device properties of several electronic structures, including HEMTs [20], MOSFETs [21], silicon oxide high-*k* oxide silicon (SOHOS) [22], photo-detectors [23], and junction diodes [24]. By solving the Poisson equation and the continuity equations self-consistently in MEDICI, we can simulate the admittance properties of MOS structures containing SiO_2 (30 Å) and Al gates to examine the minority carrier characteristics in Si and Ge. In addition, MEDICI makes it possible to perform simulations at relatively high frequencies and low temperatures by providing the appropriate physical models and parameters. Most importantly, the contributions of the interface states to both the capacitance and conductance loss at depletion can be omitted, which is beneficial to the analysis of admittance-voltage data in the inversion region. Apart from a large difference in the value of the energy bandgap for these two substrates, both the carrier lifetime and mobility, which are dependent on the carrier concentration and temperature, are critical in determining the minority carrier generation behavior. Moreover, the bulk trap level at midgap was assumed for both substrates.

3.3 Temperature-Dependent Growth of ALD-Al_2O_3/Ge Films

3.3.1 Temperature-Dependent Al_2O_3 Thicknesses

The TEM images in **Figs. 3.1(a)–(d)** reveal that the thicknesses of as-deposited Al_2O_3 thin films on Ge substrate were dependent on the deposition temperature (T_{dep}); they were ca. 53, 62, 70, and 48 Å after 60 deposition cycles at values of T_{dep} of 50, 100, 200, and 300 °C, respectively. The Al_2O_3 exhibited an amorphous phase in these samples, but we did not observe the existence of an obvious interfacial layer; nevertheless, the oxygen atoms are likely to react with the Ge substrate surface during deposition, probably in the form of GeO_x species, because Ge is readily oxidized. A blurred oxide–substrate interface became apparent upon increasing the value of T_{dep} to above 200 °C, presumably correlating with the interfacial GeO_x desorption; the detailed surface chemistry is discussed in the following sections describing the XRR and XPS analyses. **Fig. 3.2** displays a plot of the corresponding

ALD-Al_2O_3 deposition rate on Ge determined in this study, together with those on Si as reported by Ott *et al.* [2] and Groner *et al.* [3]; the results indicate similar ALD growth behavior with respect to the value of T_{dep}. Meanwhile, these experimental data were simulated well using our proposed ALD model [25], suggesting that the growth mechanism was mainly determined by the activation energy in Al_2O_3 chemical reactions at low temperatures and by the adsorption coverage of AlOH* or $Al(CH_3)$* reactive species at high temperatures. These two effects ensured that the growth rate achieved a maximum at a critical temperature (T_{max}); in our case, the value of T_{max} was ca. 170 °C, close to the value (ca. 175 °C) reported by Ott *et al.*, but higher than that (ca. 125 °C) observed by Groner *et al.* The resultant shift of the value of T_{max} was correlated to differences in the chemisorption energy required for Al_2O_3 deposition as well as the desorption rate of formed surface species; further details of this behavior are described elsewhere [25].

3.3.2 Composition Analyses

Fig. 3.3(a) compares the XRR curves of Al_2O_3/Ge samples deposited at 50 and 300 °C. The four-layer model of the $Al_2O_3/Ge_xAl_{1-x}O/GeO_2$/Ge gate stack fit the measured curve nearly perfectly; note that the presence of a $Ge_xAl_{1-x}O$ interlayer—arising from intermixing of Al_2O_3 and GeO_2—had to be considered into the model for accomplishing an excellent fit to the curve. The oscillation frequency is determined primarily by the thickness of the overlying Al_2O_3 film, and the oscillation amplitude is very sensitive to the variation in roughness between the top surface and the deposited interface. The 300 °C-Al_2O_3 on Ge substrate exhibited a slower oscillation frequency with a higher amplitude variation, reflecting its thinner Al_2O_3 film and rougher Ge interface, with respect to those of the substrate prepared at 50 °C. Note that the top surface roughness (<3 Å) was similar in all samples. We also observed that the peak positions of the maxima shifted with the incident angle in these two samples, a typical effect of the Al_2O_3 density changing with the value T_{dep}. Indeed, the film density increased from ca. 3.3 g cm^{-3} to ca. 3.7 g cm^{-3} [**Fig. 3.3(b)**]. Compared with the high density (3.97 g cm^{-3}) of crystalline α-Al_2O_3 [26], the density of each as-deposited Al_2O_3 film was indeed closer to those reported for γ-Al_2O_3 or amorphous alumina (3.5–3.7 g cm^{-3}) [26], [27]. The lower densities of the Al_2O_3 films observed upon decreasing the value of T_{dep} arose mainly from the thermally activated reaction kinetics dominating at lower temperatures—especially because we used TMA and H_2O in the ALD process, which caused an increase in the levels of H, OH, and C impurities in films. Using forward recoil spectrometry (FReS), the hydrogen concentration in ALD-Al_2O_3 has been observed to increase upon decreasing the value of T_{dep} from 175 to 35 °C [3]. SIMS analyses (**Fig. 3.4**) provided further evidence for a relatively large carbon concentration within the main Al_2O_3 prepared at temperatures below T_{max}, i.e., <200 °C. When excess O atoms or the C/H contaminants were present within the Al_2O_3—probably in the form of aluminum hydroxide [$Al(OH)_3$] and aluminum oxy-hydroxide, the densities of which are 2.42 and 3.44 g cm^{-3}, respectively [28]—the film density was lowered accordingly.

Figure 3.3(c) depicts the respective thicknesses of main Al_2O_3, mixed Al_2O_3–GeO_2, and interfacial GeO_2 layers after 60 deposition cycles as a function of T_{dep}; at first, the overall XRR thicknesses were close to the TEM observations. Interestingly, as the value of T_{dep} increased from 50 to 300 °C, the thickness of the underlying GeO_2 layer decreased gradually from ca. 5 Å to below 1 Å, whereas that of the intermediate $Ge_xAl_{1-x}O$ layer increased dramatically from ca. 1 Å to ca. 14 Å, accompanied by increased roughness between the GeO_2 layer and Ge substrate. These structural degradations became severe at temperatures above 200 °C, implying that, during ALD deposition, the poorly oxidized GeO_x species at the surface were less stable and probably diffused into the top Al_2O_3 at higher values of T_{dep}, leading to more severe dielectric intermixing and degraded interfacial roughness. Seo *et al*. speculated that similar behavior occurred during the growth of HfO_2 thin films on Ge substrates using molecular beam epitaxy (MBE) [29]; they observed that the surface GeO_x species possibly dissolve in HfO_2 at a growth temperature of 360 °C.

Next, we examined the relevance of the Al 2*p* and O 1*s* photoemission spectra, in particular their peak energy spacing; **Fig. 3.5(a)** provides an example for the as-deposited Al_2O_3/Ge. The value of the energy spacing was ca. 456.95 eV, close to the value of 457 eV for sapphire, but we did not observe a correlation between the energy spacing and the deposition temperature because the chemical shift was within 1 eV. Therefore, we further investigated the stoichiometry of the temperature-dependent grown Al_2O_3 before and after rapid thermal processing [**Fig. 3.5(b)**]. Two noteworthy features are that (i) the O/Al composition ratio gradually achieved the ideal value of 1.5 upon increasing the value of T_{dep} to 200 °C, but it increased to 1.65 at 300 °C, and (ii) a more-stoichiometric film was formed after subsequent RTA. We can explain the variation of the O/Al composition ratio reasonably in terms of the controlled growth mechanism. As we mentioned earlier, raising the value of T_{dep} led to redundant oxygen-based radicals being expelled from the deposited films, which in turn suppressed the oxygen content and, thus, improved the Al_2O_3 stoichiometry. Above T_{max} (ca. 185 °C), the deposition process relies strongly on the presence of AlOH* or $Al(CH_3)$* reactive sites because of the lower adsorption rate. In other words, a relatively higher H_2O concentration exists close to the surface at higher T_{dep}, presumably leading to the oxygen-excessive Al_2O_3 film observed when T_{dep} was 300 °C. Similar tendency was also characterized in the electrical permittivity that are ca. 5.1, 6.2, 7.9, and 5.8 for as-deposited Al_2O_3 films grown at T_{dep} of 50, 100, 200, and 300 °C, respectively; a relatively higher value was obtained at 200 °C. Furthermore, we suggest that high-temperature annealing provides additional thermal energy, acting as an external driving force, to return these as-deposited Al_2O_3 samples to their stable, stoichiometric phase.

On the other hand, GeO_x out-diffusion after thermal annealing is a critical issue in the preparation of high-*k*/Ge structures. Surface-sensitive Ge $2p_{3/2}$ spectroscopy [**Fig. 3.6(a)**] revealed that no Ge oxides diffused into the top of the Al_2O_3 dielectric after 400 °C RTA, but the bulk-sensitive Ge 3*d* spectrum (inset) revealed an increased GeO_x/Ge intensity ratio, indicative of GeO_2 growth near the lower interface. When we increased the RTA temperature to 600 °C, we detected a small peak corresponding to GeO_2 in the Ge $2p_{3/2}$ spectrum along with a reduced GeO_x/Ge ratio in the Ge 3*d* spectrum. We speculate that the balance between two competing processes—oxide growth and oxide desorption, which are strongly dependent on both the temperature and oxygen concentration—determines the amount of residual Ge oxide and its distribution. Because we used a N_2 ambient as the feed gas, oxide desorption (rather than oxide growth) should dominate the thermal reaction mechanism. Together with the finding that the critical temperature of GeO desorption was in the range of 360–425 °C [30], [31], it is probable that GeO_2 continued to grow at ca. 400 °C due to the presence of some residual oxygen in the N_2 ambient, but it most likely desorbed at the higher temperature of 600 °C. In **Fig. 3.6(b)**, the Al_2O_3/Ge deposited at a lower temperature of 50 °C exhibited results similar to that deposited at 100 °C after RTA; moreover, the higher-temperature Al_2O_3 samples appeared to display lower resistivity in GeO_x incorporation. Note that the calculated value of the GeO_2 atomic concentration in Al_2O_3—based on a standard sampling depth of ca. 30 (±4) Å for the Ge $2p_{3/2}$ spectrum—might be affected by different Al_2O_3 overlaying thicknesses in these samples. Here, the GeO_2 concentration remained low (<1.0 at.%) in all cases. In view of the earlier XRR examination, the as-deposited Al_2O_3/Ge structures displayed an increased $Ge_xAl_{1-x}O$ intermixing phenomenon, especially at temperatures up to 200 °C. Therefore, we conclude that high-temperature annealing is likely to cause interfacial GeO_x volatilization on the bottom of the Al_2O_3 dielectric with a small degree of Ge incorporation. It was suspected that Al_2O_3/Ge capacitors undergoing RTA at 600 °C might suffer from resultant dielectric intermixing, as in the case of the high-T_{dep} systems (≥200 °C); indeed, both the interface quality and the leakage current characteristics deteriorated (data not shown). These experimental findings agree with those of previous studies suggesting that the volatilization of gaseous GeO into high-*k* layers degrades the insulator properties [6], [32].

3.3.3 Effect of Forming Gas Annealing on Electrical Characteristics

The physical analyses described above suggested that Al_2O_3 ALD films grown on p-Ge substrates at the T_{dep} range of 100–200 °C should exhibit improved dielectric and interfacial qualities. Thus, we studied the electrical properties of Ge MOS capacitors incorporating Al_2O_3 deposited at 100 °C; **Fig. 3.7(a)** depicts the multi-frequency *C–V* curves recorded before and after FGA at 300 °C. Note that the *C–V* sweep direction presented here was from strong inversion to strong accumulation, and that the as-deposited Al_2O_3 thickness increased to ca. 80 Å in this case. For the as-deposited sample, we observed *C–V* stretch-out behavior along with humps that emerged in the depletion and weak inversion regimes, arising from the onset of surface slow states. Subsequent FGA processing improved the quality of the Al_2O_3–Ge interface, such that the *C–V* curves reached full accumulation saturation with a deeper "dip" in depletion, i.e., the deviation of the 1 kHz curve was diminished with respect to that of the 1 MHz curve. Another noticeable phenomenon is the significant frequency dispersion in the strong inversion region, which is consistent with a high intrinsic carrier concentration and a large density of bulk traps close to the midgap in Ge; consequently, fast accumulation of minority carriers could occur at the Ge surface [17]. Vanhellemont and Simoen reported that metal impurities—in particular Fe and Ni—are responsible for these deep levels, with a trap energy of ca. 0.3 eV within the bandgap [33]. From electrical characterization, the trap density was estimated to be ca. 10^{15}–10^{16} cm^{-3} in the bulk Ge substrate [16]. **Fig. 3.7(b)** provides a comparison of the *I–V* characteristics; the inset presents the bi-directional sweep of the *C–V* curves. At a similar value of the capacitance equivalent thickness (CET), the value of J_g and the degree of charge trapping were both reduced after FGA; we attribute these improvements to the resultant passivation of the interfacial traps.

The common approaches toward extracting the value of D_{it} for Si MOS capacitors—namely the Terman [34], high–low frequency capacitance [35], and conductance [12] methods—cannot be fully applied to Ge devices because carrier exchange between the interface states and the minority-carrier band edge influences the D_{it} extraction in the weak inversion regime [16]. Here, the statistical conductance model was utilized to evaluate the energy distribution of D_{it} only within the limited gate biases. **Fig. 3.8(a)** provides a plot of the conductance (G_p/w) as a function of the measured frequency (f_m) for the as-deposited Al_2O_3/Ge capacitor under gate biases ranging from 0.2 to 0.7 V, i.e., where the device biased from depletion to weak inversion. During the D_{it} extraction, only the conductance peak having the shoulder near the higher frequency side was fitted well. Most importantly, two interesting features appeared upon increasing the positive gate bias: (i) the G_p/w peak increased in intensity gradually and moved to lower frequency and (ii) the plateau in the range 1–10 kHz had higher magnitude. As it is well known, two main physical mechanisms are responsible for the onset of the ac conductance loss peak: (i) the carrier transition between the interface states near the Fermi level and the majority-carrier band edge, which certainly dominates at gate bias in depletion, and (ii) the dark current of the minority carriers that charge the inversion layer; they arise not only from the bulk traps within the depletion layer but also from the diffusion current from the bulk semiconductor. Based on the observation that the generation and recombination of the bulk traps over the diffusion mechanism contributed to the main minority-carrier current at temperatures below ca. 45 °C [17], we suppose that in the weak inversion region the competition between bulk trap loss and interface state loss is intense. The resultant shift of the gate bias-dependent G_p/w peak reflected the fact that charging and discharging of the interface traps should dominate these energy losses. On the other hand, as for the conductance plateau observed on the lower frequency side (1–10 kHz), Evangelou *et al.* successively simulated this anomalous behavior using the continuum D_{it} model accompanying the tunneling effect of the majority carriers from the semiconductor surface to the bulk oxide defects [35]. We suspect, however, that the insensitive conductance loss should be strongly related to the intrinsic properties of Ge; studies of temperature- and doping concentration-dependences are currently under investigation.

In terms of the frequency-dependent conductance peaks, **Fig. 3.8(b)** reveals the change in D_{it} after thermal processing. The value of D_{it} of the as-deposited sample was ca. 4×10^{12} cm^{-2} eV^{-1}; it increased to ca. 2×10^{13} cm^{-2} eV^{-1} after RTA at 600 °C, but decreased to ca. 5×10^{11} cm^{-2} eV^{-1} after FGA at 300 °C, indicating that the low-temperature FGA did help to repair the high-*k*–Ge interface [36]. The in-diffused hydrogen possibly filled the existed defects inside poor-quality GeO_x between high-*k*/Ge interface [37]. In addition, as is evident in **Fig. 3.8(c)**, the employed value of T_{dep} was also a determining factor affecting the quality of the interface between the grown Al_2O_3 and Ge. Apparently, the value of D_{it} increased to greater than 10^{13} cm^{-2} eV^{-1} when T_{dep} was 200 and 300 °C, showing consistency with the results of appreciable interfacial dielectric intermixing. In other words, it is essential to protect the Ge devices from GeO_x formation and volatilization under either higher-temperature deposition or higher-temperature post-thermal processing to achieve the optimal electrical performance.

3.4 Minority Carrier Response Behavior of Ge MOS Capacitors

3.4.1 Equivalent Circuit Model and Concept of Conductance Method

Measurements of the MOS device can be modeled using the equivalent circuit presented in **Fig. 3.9(a)**, where C_{ins} is the insulator capacitance and C_{acc}, C_{dep}, and C_{inv} are the semiconductor capacitances in accumulation, depletion, and inversion, respectively. This model also incorporates the effects of interface traps located between the insulator and semiconductor. Because interface traps follow the Shockley–Read–Hall (SRH) model, the kinetics of the generation/recombination (*g*-*r*) of interface states are represented by the associated conductances, G_{cit} and G_{vit}, connected to the respective conduction- and valance-band edges in p-type materials. In addition to the energy loss associated with the capture and emission of carriers, there is a capacitance (C_{it}) that is proportional to the interface state density (D_{it}). In depletion, G_{vit} would be greater than G_{cit} in the weak depletion of a p-type material because of the neglected contribution of minority carriers to the charging/discharging of D_{it}. Based on the assumption that only majority-carrier density effects are important in depletion, the complete equivalent circuit can be simplified to the equivalent circuit presented in **Fig. 3.9(d)**. For analyses, we have modified such a single-level trap model into a more realistic case of a continuous and random distribution of D_{it} within the bandgap.

Figure 3.9(e) displays the simplified equivalent circuit for the MOS device when entering the inversion regime. In contrast to the depletion region, the bulk traps, the *g*-*r*, and the diffusion of minority carriers all contribute to the dark current that charges the inversion layer. The value of G_{inv} is the equivalent conductance of the parallel combination of *g*-*r* conductance (G_{gr}) and diffusion conductance (G_{diff}), where G_{gr} is due to the finite *g*-*r* within the depletion layer through bulk traps and G_{diff} is due to the diffusion current of minority carriers from the bulk to the edge of the depletion region. At lower temperatures, G_{gr} is more significant [14], [38] and can be expressed using the equation

$$\frac{G_{gr}}{A} = \frac{q}{\phi_S}\frac{n_i}{1}\frac{w}{\tau_T} \tag{3.1}$$

where ϕ_S and w are the surface potential and depletion layer width in inversion, respectively, and τ_T is the SRH lifetime determined by the density of *g*-*r* centers and the capture coefficients for electrons and holes, respectively. As the temperature increases further, G_{diff} becomes dominant because of the increasing function of n_i^2 [14], [38], as revealed by the following equation:

$$\frac{G_{diff}}{A} = \frac{q^2}{kT}\frac{n_i^2}{N_{maj}}\frac{L_{mir}}{\tau_{mir}} = \frac{q\,N_{mir}\,\mu_{mir}}{L_{mir}} \qquad (3.2)$$

where N_{maj} is the substrate doping concentration and L_{maj} (τ_{mir}) and μ_{mir} are the diffusion length (lifetime) and mobility of minority carriers in the bulk material, respectively. To correctly observe the temperature dependence of the minority-carrier response behavior, all of the parameters are a function of the temperature in calculations, except for τ_T, because of the weakly temperature dependence. Note that the equivalent circuit biased in strong inversion is often simplified for the Si case in terms of $wC_{\text{inv}} >> G_{\text{inv}}$, but this assumption cannot be fully adopted for Ge; the details are discussed below.

The conductance technique is suitable for evaluating the characteristics of interface and bulk traps in depletion and inversion; identical equivalent circuits were found: the semiconductor admittance consists of the C_{dep} shunted by the series combination of one capacitance and one conductance. Therefore, in depletion, $\tau_{it} = C_{\text{it}}/G_{\text{it}}$ is defined as the time constant related to the trap-to-band communications; in inversion, $\tau_{inv} = C_{\text{inv}}/G_{\text{inv}}$ is the minority carrier response time. Moreover, the commonly used parallel equivalent circuit is converted into the equivalent circuit in **Fig. 3.9(b)** by subtracting the reactance of the insulator capacitor C_{ins} to analyze the semiconductor admittance directly. Through a plot of G_{sub}/f versus log f for various gate biases, we can examine the interfacial and bulk properties from the changes of maximum position and height of the G_{sub}/f peak.

3.4.2 MEDICI-Simulated and Measured Electrical Characteristics

Figures 3.10 and **3.11** present the simulated *C–V* and *G–V* characteristics of Al/SiO_2 gate stacks on p-Si and p-Ge substrates at various temperatures. It was observed that the dielectric on Si [**Fig. 3.10(a)**] obviously presented the LF *C–V* curves only when raising the temperature up to 400 K and reducing the frequency to as low as 100 Hz. In contrast, such LF curves occurred readily at 300 K for Ge systems in which the doping concentrations were 10^{16} and 10^{14} cm^{-3} [**Figs. 3.10(b)** and **3.10(c)**, respectively]. We observed the minority carrier behavior even at higher frequencies, e.g., 1 MHz, in the low-doped Ge. On the contrary, the complete HF C–V curves appeared only in the high-doped Ge at temperatures as low as 250 K. By examining the simulated conductance G_{mea} in the Si case [**Fig. 3.11(a)**], the inversion conductance G_{inv} revealed a frequency independence up to 100 kHz; the values increased by ca. two orders of magnitude as we increased the temperature from 300 to 400 K. From **Figs. 3.11(b)** and **3.11(c)**, the Ge counterpart reveals two distinct features: the G_{inv} characteristics measured at low temperature (250 K) were identical to those in Si at high temperature (400 K); upon increasing the temperature to 350 K, the value of G_{inv} became proportional to the square of the angular frequency ω, similar to the curves observed in accumulation [**Fig. 3.9(c)**]. The resultant w^2-dependence of G–V curves implied the similar equivalent operation circuits in both accumulation and inversion for Ge MOS capacitors at higher temperatures, e.g., >300 K. The electrical differences in inversion between Ge and Si are dependent on the values of G_{mea}, which are dominated by either of the terms G_{inv} or ωC_{inv}, which are strongly correlated to the measured temperature, frequency, and properties of the substrate material. We will understand the minority-carrier conductance loss further through theoretical calculations of these two components, together with the following experimental findings. Note that the absence of interface states was assumed in simulation; hence, they did not contribute to the energy loss, thereby causing the onset of a deeper “dip” in depletion.

Figures 3.13 and **3.14** display the measured C–V and G–V characteristics of Pt/ALD-Al_2O_3 gate stacks deposited on p-Ge and n-Ge substrates, respectively (the measured curves of the p-Si MOS capacitor in **Fig. 3.12** were used as a reference). First, as illustrated in **Figs. 3.13(a)–(c)** and **3.14(a)–(c)**, the minority carrier response occurred in C–V inversion for both types of Ge. Through plots of the temperature dependence of 1-MHz C–V curves [**Figs. 3.15(a)** and **3.15(b)**], we observe that increasing the measured temperature to 100 °C accelerated the overall response rate pronouncedly. Besides, the low-doped (10^{14} cm^{-3}) n-Ge also exhibited a faster rate with respect to p-Ge (2×10^{15} cm^{-3}), which we attribute to the resultant high minority-carrier concentration. On the other hand, unlike the exponential decline of the conductance curves in inversion for Si MOS capacitors, **Figs. 3.13(d)–(f)** and **3.14(d)–(f)** display gate-bias-independent values of G_{inv} in Ge with a more severe frequency dispersion upon increasing the measured temperature. Meanwhile, the temperature-dependent G–V curves in **Figs. 3.15(c)** and **3.15(d)** indicate that the values of G_{inv} increased upon raising the temperature up to 60–70 °C, but then they deceased again. We attribute this phenomenon to the effects of the external conductance G_{ext} at higher temperatures, resulting in the lower values of G_{inv}.

3.4.3 Minority Carrier Response Characteristics

Figure 3.16(a) provides an analysis of the simulated Arrhenius-dependent substrate conductance G_{sub} in Si and Ge at various dopant concentrations (10^{14} and 10^{16} cm^{-3}), plotted with experimental data obtained from this and previous studies. The simulated values of G_{sub} in inversion, i.e., G_{inv}, can be divided into two stages: one dominated by G_{diff} at high temperatures and the other by G_{gr} at low temperatures. Most importantly, the values of G_{inv} of the dielectric on Ge were larger than those on Si by at least four orders of magnitude, indicative of a larger energy loss occurring in Ge. Both our data for Al_2O_3/p-Ge and those reported for HfO_2/n-Ge are in agreement with the simulation results for the SiO_2/p-Ge structure. Using eqs. (3.1) and (3.2), we evaluated the respective components of G_{gr} and G_{diff} in G_{inv} for these two substrates. We assumed a high bulk trap volume density (N_{T}) of 10^{15} cm^{-3} in Ge, relative to a value of 10^{14} cm^{-3} in Si, because Ge wafer quality has not yet developed to a satisfactory level. **Fig. 3.16(b)** reveals that the crossover temperature (T_C) at which the transition is made from the *g*-*r* mechanism dominating to the diffusion-controlled process was ca. 330 K for p-Ge, close to the value of ca. 318 K characterized for high-*k*/n-Ge (N_D = ca. 7×10^{14} cm^{-3}) [17]. Relative to the value of T_C of ca. 442 K for its Si counterpart, we ascribe the lower value for Ge to its higher value of n_i. Here, deviations in the values of the G_{inv} evaluated via the MEDICI simulations and the theoretical calculation arose from the adopted material parameters, e.g., the N_{T} value. We also calculated the magnitude of the wC_{inv} term, where C_{inv} is defined using Eq. (3.3) [14], for comparison with the values of G_{inv} in these two substrates.

$$C_{inv} = \frac{\varepsilon_S\, \varepsilon_o}{\sqrt{2}L_D} \frac{n_i}{N_{maj}} exp(\frac{-q\,\phi_S}{2kT}) \tag{3.3}$$

where ε_S is the substrate dielectric constant, L_D is the Debye length, and ϕ_S is equal to $2\phi_B$ at the threshold inversion point (ϕ_B is the bulk potential). The calculations revealed that $wC_{\mathrm{inv}} >> G_{\mathrm{inv}}$ for the Si case at temperatures up to ca. 400 K; thus, the equivalent inversion circuit in **Fig. 3.9(e)** is often simplified further so that the depletion capacitance C_{dep} changes in parallel only with the G_{inv} term. This conclusion is only suitable for the Ge counterpart when the temperatures decrease below ca. 250 K; meanwhile, the opposite behavior, $wC_{\mathrm{inv}} << G_{\mathrm{inv}}$, occurs at temperatures above ca. 350 K. That is to say, at intermediate temperatures (250–350 K), the minority carrier response in Ge MOS capacitors is strongly dependent on the measured temperature and frequency.

Here, we define the effective transition frequency f_{tran}—at which the capacitance in inversion is midway between C_{ins} and the HF capacitance C_{hf}—as marking the onset of the LF *C*–*V* behavior. Our experimental data for f_{tran} observed in Al_2O_3/p-Ge (**Fig. 3.13**) were within the MEDICI-simulated predictions in **Fig. 3.17(a)**. The fast response rates in the Ge capacitors corresponded to higher values of f_{tran}: ca. 5 and 200 kHz at RT for Ge doped at 10^{16} and 10^{14} cm^{-3}, respectively. Higher degrees of substrate doping and lower measured temperatures lowered the order of f_{tran} accordingly, due to abatement of minority carrier disturbance. From these studies, we conclude that two energy loss mechanisms, G_{gr} and G_{diff}, are responsible for the supply of minority carriers to the inversion layer, providing LF-like *C–V* properties in the kilohertz regime. Previously, Bai *et al*. reported an interesting phenomenon in HfO_2/p-Ge [9]: an increase in the degree of substrate doping from 10^{15} to 4×10^{17} cm^{-3} reduced the value of f_{tran} from greater than 100 kHz to less than 10 kHz. Upon increasing the Ge concentration to 3×10^{18} cm^{-3}, however, the value of f_{tran} increased again to greater than 1 MHz, which is opposite to the trend that we expected. To explain this anomalous behavior, we correlated the value of f_{tran} to the changes in G_{inv} using the following equation [14]:

$$f_{tran} = \frac{G_{inv}}{2\pi C_{ins}}\left(1 - \frac{C_{hf}}{C_{ins}}\right) \tag{3.4}$$

using a value of C_{ins} of 1.11 μF/cm^2 as in our Al_2O_3/Ge cases, i.e., corresponding to the capacitance-equivalent-thickness (CET) of 30 Å, and with the assumption that the number of bulk traps was proportional to the dopant concentration. We observe in **Fig. 3.17(b)** that Ge doped at 10^{18} cm^{-3} exhibited a relatively high value of f_{tran} with respect to that of the low-doped Ge. Considering that values of N_T ranging from ca. 10^{14} to 10^{16} cm^{-3} have been reported for an intrinsic Ge epitaxial film [16] and low-doped Ge substrates [33], [39], together with a maximum solid solubility of ca. 10^{19} cm^{-3} for p-type dopants, we suspect that the highly doped p-Ge wafer might contain a large number of mid-gap traps (e.g., 10^{17}–10^{19} cm^{-3}) inside the depletion layer, possibly arising from high degrees of Fe and Ni metal impurities [33], dopant precipitation, and/or metal-dopant combined defects. In reality, the density of bulky defects is governed not only by the wafer type and contamination by impurities but also by the device's fabrication [18], [40], in particular the dielectric–Ge interface, which in turn influences the degree of minority carrier response on the measured frequency. In other words, the magnitude of G_{gr} is probably comparable with that of G_{diff}—possibly even exceeding it at higher temperatures—but G_{diff} still immediately rules the inversion conductance G_{inv} as the temperature increases further.

3.4.4 Interfacial State Response Characteristics

On the other hand, because the device equivalent circuit in inversion is similar to that in depletion, it is essential to explore the differences between the minority-carrier-induced loss and the interface-state loss with respect to the measured frequency. Thus, we calculated the temperature dependence of the interface-state response frequency (f_{it}) as a function of the surface potential using the following equation [14]:

$$f_{it} = \frac{v_{th}\,\sigma_{cap}\,n_i}{\pi} exp(\frac{-q\,\phi_S}{kT}) \tag{3.5}$$

where v_{th} is the thermal velocity and σ_{cap} is the capture cross section. Supposing that the standard measured frequency in the range 10^3–10^6 Hz, as depicted in **Fig. 3.18(a)**, we can detect D_{it} close to the midgap in Ge only at values of f_{it} greater than 10^5 Hz, quite different from the D_{it} response observed as low as 10^3 Hz in Si. This conflicting behavior can be understood in terms of the results of the MOS experiments presented in **Figs. 3.12–3.14**, where we observe depletion bumps at frequencies of 1–100 kHz for the Al_2O_3/p-Si capacitors and at 50–1000 kHz for the Al_2O_3/p-Ge capacitors. In contrast, we did not observe any such bump for the corresponding n-Ge case because of the intense minority-carrier loss. The calculated results in **Figs. 3.18(b)–(c)** suggest that continuously decreasing the temperature from 300 to 100 K is a practical means of extracting the overall distribution of D_{it} within the Ge bandgap. Such a temperature-dependent conductance method is discussed in detail in a recent literature review by Martens *et al.* [15].

Figures 3.19(a)–(f) display the G_{sub}/f versus log f characteristics for both types of Ge under gate biases ranging from the mid-gap to the inversion. We employed the statistical conductance model to estimate values of the mid-gap D_{it} for p-Ge and n-Ge of ca. 7 (±1) × 10^{11} and 1.5 (±0.5) × 10^{12} cm^{-2} eV^{-1}, respectively. An interesting trend appeared for the devices biased into the inversion conditions: the G_{sub}/f peak gradually moved to lower frequency, accompanied by an increased intensity, and upon raising the temperature; as a consequence, the overall conductance spectra shifted to higher frequency. Because of the presence of a high minority carrier density, this phenomenon reveals that we must consider the communication of interface traps not only with majority carriers but also with minority carriers in Ge MOS capacitors. Even so, we still believe that such a shift in the frequency-dependent conductance peaks is correlated mainly to the G_{inv} loss within the substrate itself, overwhelming the D_{it}-induced energy loss in inversion. We rationalize this behavior by considering the following observations. First, from the viewpoint of the f_{it} calculation, the G_{sub}/f peaks appear far below 10^5 Hz, which is irrational for the D_{it} response in Ge devices close to RT. Next, assuming that the transition of surface minority carriers with D_{it} dominates the conductance peaks in inversion, the resultant shorter lifetime in the charging/discharging of D_{it} should shift them to higher frequency, rather than lower frequency, upon increasing the inversion biases. In fact, a Λ-shaped distribution in the trap time constant across the overall Ge bandgap was observed under a quite low temperature of 80 K when employing a full conductance measurement [15], in which the G_{sub}/f peaks shifted initially to lower frequency and subsequently to higher frequency with respect to the gate bias. In addition, according to the classical bulk trap model proposed by Nicollian and Brews [14], the resultant frequency of the G_{sub}/f maximum should coincide with the value of f_{tran} observed in the C–V curves. Indeed, we observed that the conductance peaks (and values of the f_{tran}) for p-Ge capacitors were located at ca. 4 kHz (3 kHz), 20 kHz (15 kHz), and 100 kHz (130 kHz) at 20, 40, and 60 °C, respectively, when V_g was equal to 1 V. The trends were also consistent for the n-Ge cases. In addition, we estimated the effective values of N_T simply from the corresponding magnitudes of G_{sub}/f by evaluating the depletion width swept out by a 2-kT band bending; the resulting values of N_T for p-Ge and n-Ge were ca. 3.9×10^{15} and 2.5×10^{15} cm^{-3}, respectively, reflecting high levels of bulky defects existing in these particular Ge wafers.

3.5 Conclusions

In Chapter 3, we describe the structural and electrical properties of ALD-Al_2O_3 thin films onto Ge substrates over a wide deposition temperature range (50–300 °C). From GI-XRR and XPS, we found that increasing the deposition temperature improved the Al_2O_3 film density and its dielectric stoichiometry; nevertheless, dielectric intermixing between main Al_2O_3 and interfacial GeO_2 appeared at temperatures above 200 °C, along with degradation of the GeO_2/Ge interface. Accordingly, a relatively large J_g and a high density of D_{it} ($>10^{13}$ cm^{-2} eV^{-1}) were observed as a result of deterioration of the entire Al_2O_3/Ge structure at higher deposition temperatures. In addition, although subsequent high-temperature processing at 600 °C in a N_2 ambient could relieve the oxygen-excessive behavior further, i.e., to provide a more stoichiometric film, the accompanying GeO_x volatilization close to the dielectric interface caused greater damage to the electrical performance. Only low-temperature 300 °C FGA improved the C–V characteristics of the Pt/Al_2O_3/Ge structure, in terms of providing a lower value of D_{it} (ca. 6×10^{11} cm^{-2} eV^{-1}), a lower value of J_g, and reduced hysteresis width.

Furthermore, we also present MEDICI simulations of the admittance-voltage properties of Ge and Si MOS devices, including analyses of the substrate conductance G_{sub} and high–low transition frequency f_{tran}, to explore differences in the minority-carrier response. The Arrhenius-dependent G_{sub} characteristics revealed that a larger energy loss—by at least four orders of magnitude—occurs in Ge than in Si, reflecting the fast minority-carrier response rate, i.e., a higher value of f_{tran}. We confirmed that the higher intrinsic carrier concentration in Ge, through the generation/recombination of mid-gap trap levels as well as the diffusion mechanism, resulted in the onset of LF C–V curves in the kHz regime, accompanying the gate-independent inversion conductance. Experimental data obtained from Al_2O_3/Ge MOS capacitors were consistent with the values of G_{sub} and f_{tran} obtained from the MEDICI predictions and theoretical calculations. In addition, upon increasing the inversion biases, we observed shifts in the G_{sub}/f conductance peaks to low frequencies that arose mainly from the transition of minority carriers with bulk traps in the depletion layer. Meanwhile, we estimated that bulky defects of ca. (2–4) × 10^{15} cm^{-3} exist in present-day low-doped Ge wafers.

References (Chapter 3)

[1] S. K. Kim, S. W. Lee, C. S. Hwang, Y.-S. Min, J. Y. Won, and J. Jeong, “Low temperature (<100 °C) deposition of aluminum oxide thin films by ALD with O_3 as oxidant,” *J. Electrochem. Soc.* vol. **153**, p. F69, 2006.

[2] A. W. Ott, J. W. Klaus, J. M. Johnson, and S. M. George, “Al_2O_3 thin film growth on Si(100) using binary reaction sequence chemistry,” *Thin Solid Films* vol. **292**, p. 135, 1997.

[3] M. D. Groner, F. H. Fabreguette, J. W. Elam, and S. M. George, “Low-temperature Al_2O_3 atomic layer deposition,” *Chem. Mater.* vol. **16**, p. 639, 2004.

[4] C. O. Chui, H. Kim, D. Chi, P. C. McIntyre, and K. C. Saraswat, “Nanoscale germanium MOS dielectrics—Part II: high-*k* gate dielectrics,” *IEEE Trans. Electron Devices*, vol. **53**, p. 1509, 2006.

[5] S. Spiga, C. Wiemer, G. Tallarida, G. Scarel, S. Ferrari, G. Seguini, and M. Fanciulli, “Effects of the oxygen precursor on the electrical and structural properties of HfO_2 films grown by atomic layer deposition on Ge,” *Appl. Phys. Lett.* vol. **87**, p. 112904, 2005.

[6] W. P. Bai, N. Lu, and D.-L. Kwong, “Si interlayer passivation on germanium MOS capacitors with high-*k* dielectric and metal gate,” *IEEE Electron Device Lett.* vol. **26**, p. 378, 2005.

[7] N. Wu, Q. Zhang, C. Zhu, D. S. H. Chan, A. Du, N. Balasubramanian, M. F. Li, A. Chin, J. K. O. Sin, and D.-L. Kwong, “A TaN-HfO_2-Ge pMOSFET with novel SiH_4 surface passivation,” *IEEE Electron Device Lett.* vol. **25**, p. 631, 2004.

[8] F. Gao, S. J. Lee, J. S. Pan, L. J. Tang, and D.-L. Kwong, “Surface passivation using ultrathin AlN_x film for Ge–metal–oxide–semiconductor devices with hafnium oxide gate dielectric,” *Appl. Phys. Lett.* vol. **86**, p. 113501, 2005.

[9] W. Bai, N. Lu, P. Ritenour, M. L. Lee, D. A. Antoniadis, and D.-L. Kwong, “The electrical properties of HfO_2 dielectric on germanium and the substrate doping effect,”

IEEE Trans. Electron Devices, vol. **53**, p. 2551, 2006.

[10] C.-C. Cheng, C.-H. Chien, G.-L. Luo, C.-H. Yang, M.-L. Kuo, J.-H. Lin, C.-K. Tseng, and C.-Y. Chang, "Study of thermal stability of HfO_xN_y/Ge capacitors using postdeposition annealing and NH_3 plasma pretreatment," *J. Electrochem. Soc.* vol. **154**, p. G155, 2007.

[11] S. J. Whang, S. J. Lee, F. Gao, N. Wu, C. X. Zhu, J. S. Pan, L. J. Tang, and D. L. Kwong, "Germanium p- and n-MOSFETs fabricated with novel surface passivation (plasma PH_3 and thin AlN) and TaN/HfO_2 gate stack," *Tech. Dig. Int. Electron Devices Meet.* p. 307, 2004.

[12] M. M. Frank, S. J. Koester, M. Copel, J. A. Ott, V. K. Paruchuri, H. Shang, and R. Loesing, "Hafnium oxide gate dielectrics on sulfur-passivated germanium," *Appl. Phys. Lett.* vol. **89**, p. 112905, 2006.

[13] N. Wu, Q. Zhang, N. Balasubramanian, D. S. H. Chan, and C. Zhu, "Characteristics of self-aligned gate-first Ge p- and n-channel MOSFETs using CVD HfO_2 gate dielectric and Si surface passivation," *IEEE Electron Device Lett.* vol. **54**, p. 733, 2007.

[14] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982.

[15] K. Martens, C. O. Chui, G. Brammertz, B. D. Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, "On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates," *IEEE Trans. Electron Devices*, vol. **55**, p. 547, 2008.

[16] P. Batude, X. Garros, L. Clavelier, C. Le Royer, J. M. Hartmann, V. Loup, P. Besson, L. Vandroux, Y. Campidelli, S. Deleonibus, and F. Boulanger, "Insights on fundamental mechanisms impacting Ge metal oxide semiconductor capacitors with high-*k*/metal gate stacks," *J. Appl. Phys.*, vol. **102**, p. 034514, 2007.

[17] A. Dimoulas, G. Vellianitis, G. Mavrou, E. K. Evangelou, and A. Sotiropoulos, "Intrinsic

carrier effects in HfO_2-Ge metal–insulator–semiconductor capacitors," *Appl. Phys. Lett.*, vol. **86**, p. 223507, 2005.

[18] C. O. Chui, F. Ito, and K. C. Saraswat, "Nanoscale germanium MOS dielectrics—Part I: Germanium oxynitrides," *IEEE Trans. Electron Devices*, vol. **53**, p. 1501, 2006.

[19] C.-C. Cheng, C.-H. Chien, G.-L. Luo, J.-C. Liu, Y.-C. Chen, Y.-F. Chang, S.-Y. Wang, C.-C. Kei, C.-N. Hsiao, and C.-Y. Chang, "Five-element circuit model using linear regression method to correct the admittance measurement of MOS capacitor", *J. Vac. Sci. Technol. B*, vol. **27**, p. 130, 2009.

[20] J.-C. Lin, P.-Y. Yang, and W.-C. Tsai, "Simulation and analysis of metamorphic high electron mobility transistors," *Microelectron. J.*, vol. **38**, p. 251, 2007.

[21] M. Zhu, P. Chen, R. K. Y. Fu, W. Liu, C. Lin, and P. K. Chu, "Simulation of suppression of floating-body effect in partially depleted SOI MOSFET using a $Si_{1-x}Ge_x$ dual source structure," *Mater. Sci. Eng. B*, vol. **114–115**, p. 264, 2004.

[22] Y. N. Yeo, Y. Q. Wang, S. K. Samanta, W. J. Yoo, G. Samudra, D. Gao, and C. C. Chong, "Simulation of trapping properties of high-*k* material as the charge storage layer for flash memory application," *Thin Solid Films*, vol. **504**, p. 209, 2006.

[23] N. V. Sochinskii, M. Lozano, G. Pellegrini, and M. Ullan, "Simulation of CdTe:Ge crystal properties for nuclear radiation detectors," *Nucl. Instrum. Methods Phys. Res., Sect. A*, vol. **568**, p. 451, 2006.

[24] N. Keskitalo, A. Hallen, F. Masszi, and J. Olsson, "Simulation of forward bias injection in proton irradiated silicon pn-junctions," *Solid-State Electon.*, vol. **39**, p. 1087, 1996.

[25] C.-C. Cheng, J.-C. Liu, C.-H. Chien, G.-L. Luo, C.-C. Kei, C.-N. Hsiao, and C.-Y. Chang, (unpublished).

[26] D. R. Lide, *CRC Handbook of Chemistry and Physics: A Ready-Reference Book of Chemical and Physical Data* (84th ed.), CRC Press, 2003.

[27] D. E. Grey, *American Institute of Physics Handbook*, American Institute of Physics, New

York, 1982.

[28] Y.-S. Min, Y. J. Cho, and C. S. Hwang, “Atomic layer deposition of Al_2O_3 thin films from a 1-methoxy-2-methyl-2-propoxide complex of aluminum and water,” *Chem. Mater.* vol. **17**, p. 626, 2005.

[29] J. W. Seo, Ch. Dieker, J.-P. Locquet, G. Mavrou, and A. Dimoulas, “HfO_2 high-*k* dielectrics grown on (100)Ge with ultrathin passivation layers: Structure and interfacial stability,” *Appl. Phys. Lett.* vol. **87**, p. 221906, 2005.

[30] K. Prabhakaran, F. Maeda, Y. Watanabe, and T. Ogino, “Distinctly different thermal decomposition pathways of ultrathin oxide layer on Ge and Si surfaces,” *Appl. Phys. Lett.* vol. **76**, p.2244, 2000.

[31] K. Prabhakaran and T. Ogino, “Selective bond-breaking and bond-making in oxynitride of Si and Ge: a case of chemical bond manipulation,” *Surf. Sci.* vol. **387**, p. L1068, 1997.

[32] C.-C. Cheng, C.-H. Chien, C.-W. Chen, S.-L. Hsu, C.-H. Yang, and C.-Y. Chang, “Effects of postdeposition annealing on the characteristics of HfO_xN_y dielectrics on germanium and silicon substrates,” *J. Electrochem. Soc.* vol. **153**, p. F160, 2006.

[33] J. Vanhellemont and E. Simoen, “Brother silicon, sister germanium,” *J. Electrochem. Soc.* vol. **154**, p. H572, 2007.

[34] J. J.-H. Chen, N. A. Bojarczuk, Jr., H. Shang, M. Copel, J. B. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, “Ultrathin Al_2O_3 and HfO_2 gate dielectrics on surface-nitrided Ge,” *IEEE Trans. Electron Devices* vol. **51**, p. 1441, 2004.

[35] E. K. Evangelou, G. Mavrou, A. Dimoulas, and N. Konofaos, “Rare earth oxides as high-*k* dielectrics for Ge based MOS devices: An electrical study of $Pt/Gd_2O_3/Ge$ capacitors,” *Solid-State Electron.* vol. **51**, p. 164, 2007.

[36] T. Maeda, M. Nishizawa, Y. Morita, and S. Takagi, “Role of germanium nitride interfacial layers in HfO_2/germanium nitride/germanium metal-insulator-semiconductor structures,” *Appl. Phys. Lett.* vol. **90**, p. 072911, 2007.

[37] V. V. Afanas'ev, Y. G. Fedorenko, and A. Stesmans, "Interface traps and dangling-bond defects in (100)Ge/HfO_2," *Appl. Phys. Lett.* vol. **87**, p. 032107, 2005.

[38] Y. Nemirovsky and l. Bloom, "Admittance measurements of metal-insulator-semiconductor devices in p-type HgCdTe," *J. Vac. Sci. Technol. A,* vol. **6**, p. 2710, 1988.

[39] E. Simoen, C. Claeys, S. Sioncke, J. V. Steenbergen, M. Meuris, S. Forment, J. Vanhellemont, P. Clauws, and A. Theuwis, "Lifetime and leakage current considerations in metal-doped germanium," *J. Mater. Sci.: Mater. Electron.*, vol. **18**, p. 799, 2007.

[40] A. Dimoulas, D. P. Brunco, S. Ferrari, J. W. Seo, Y. Panayiotatos, A. Sotiropoulos, T. Conard, M. Caymax, S. Spiga, M. Fanciulli, Ch. Dieker, E. K. Evangelou, S. Galata, M. Houssa, and M. M. Heyns, "Interface engineering for Ge metal-oxide-semiconductor devices," *Thin Solid Films*, vol. **515**, p. 6337, 2007.

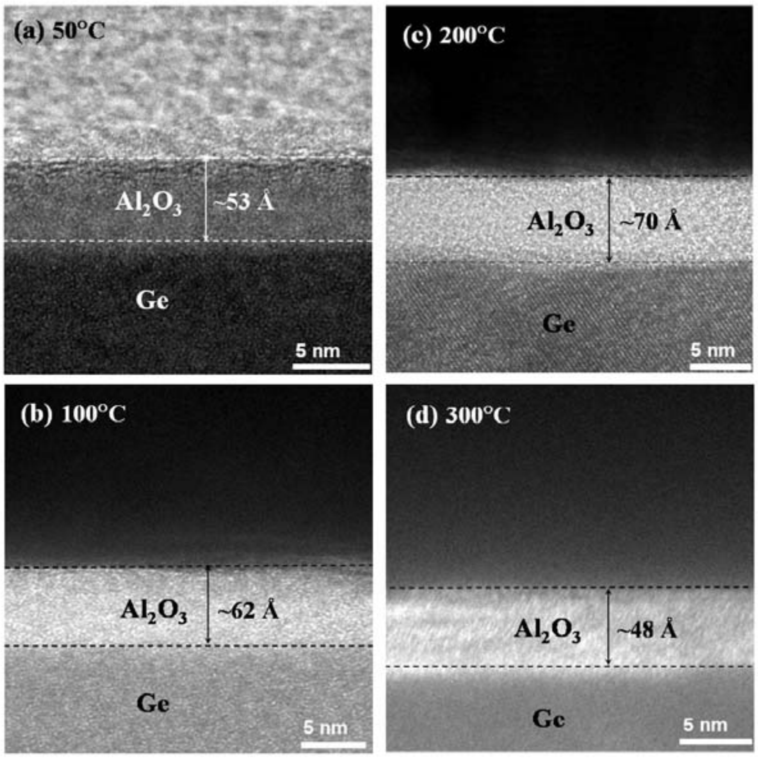


Fig. 3.1 TEM images of the as-deposited Pt/ALD-Al_2O_3/Ge structure after 60 deposition cycles under different values of T_{dep}.

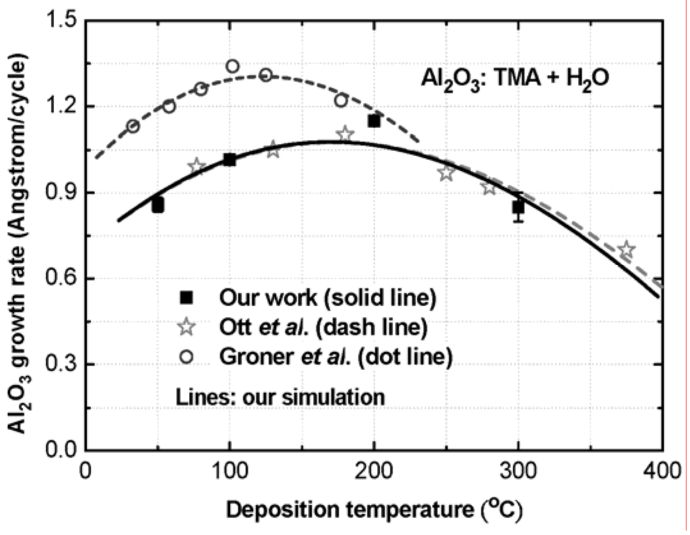


Fig. 3.2 Growth rates of ALD-Al_2O_3 films plotted against the value of T_{dep} for both this and previously studies (by Ott *et al*. and Groner *et al*.). Solid lines represented the simulation of our proposed ALD model [25].

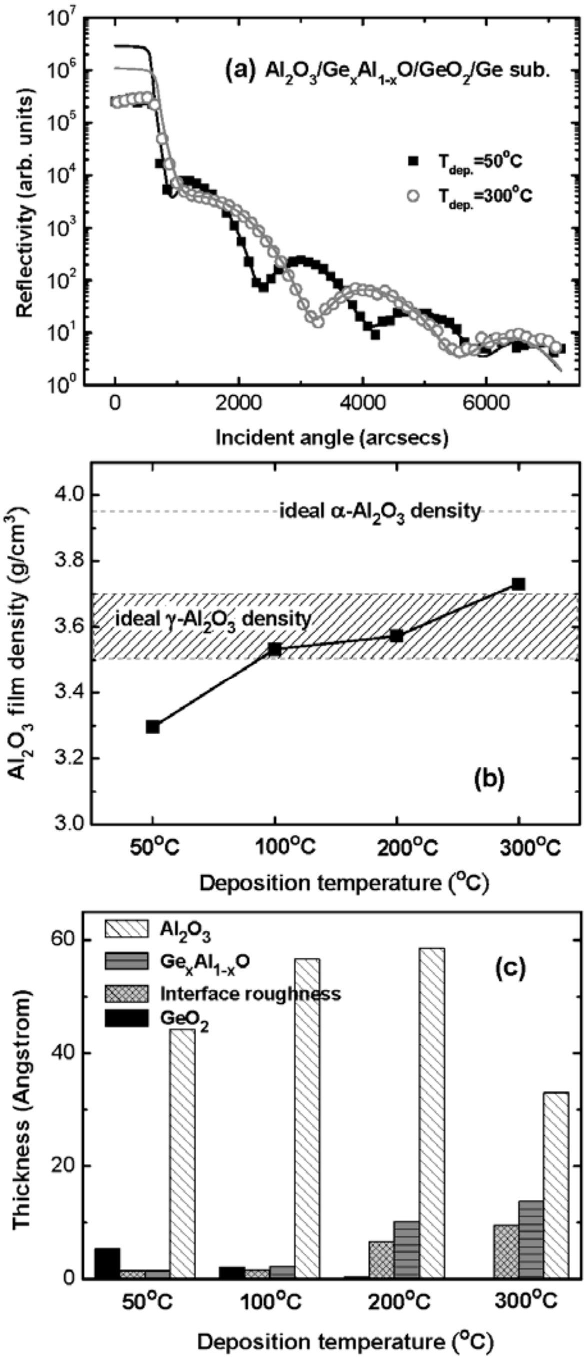


Fig. 3.3 (a) Measured and simulated GIXRR curves of the as-deposited Al_2O_3 (60 cycles)/Ge structures at values of T_{dep} of 50 and 300 °C. (b) Extracted Al_2O_3 film densities plotted with respect to the value of T_{dep}. (c) Extracted thicknesses of each layer and GeO_2/Ge interface roughness plotted against the value of T_{dep}. Note that the modeled XRR structure is the $Al_2O_3/Ge_xAl_{1-x}O/GeO_2$/Ge gate stack.

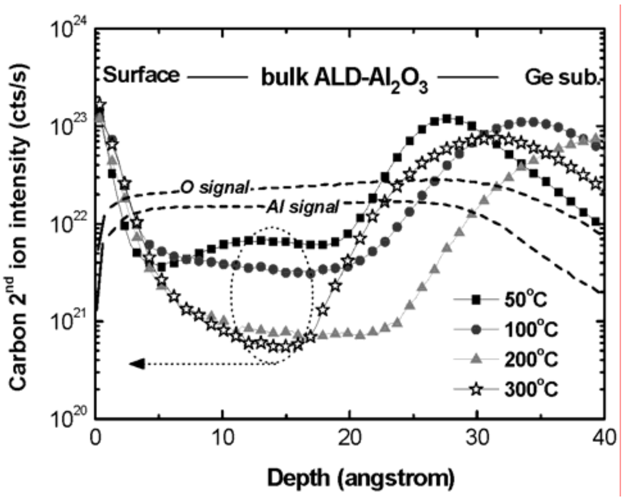


Fig. 3.4 SIMS depth profiles of carbon second-ion intensity within ALD-Al_2O_3 (60 cycles) on Ge substrate deposited at various values of T_{dep}. The Al and O second-ion intensities of the Al_2O_3 (T_{dep} = 300 °C)/Ge sample are labeled as a reference of the relative depth.

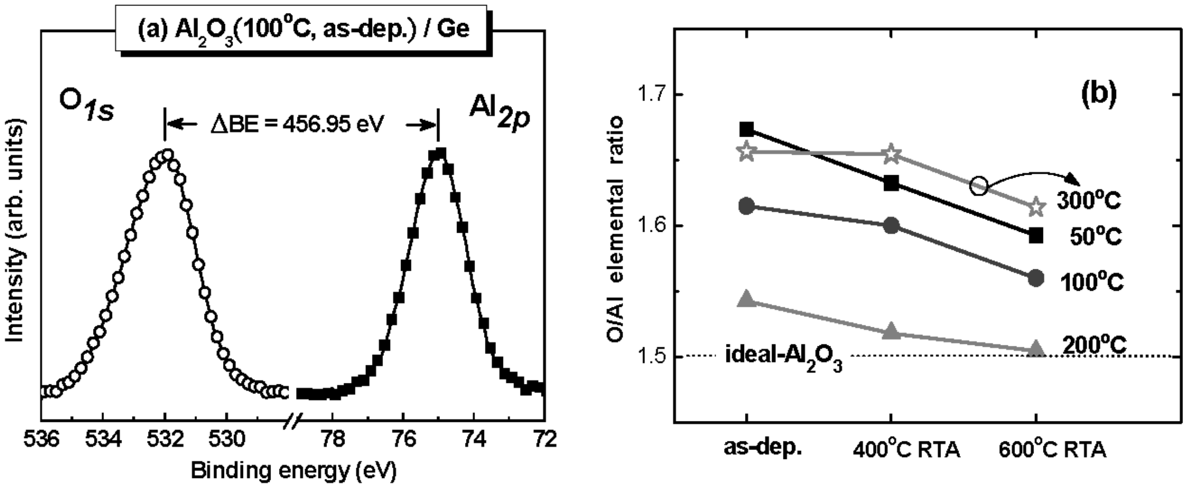


Fig. 3.5 (a) Binding energy difference between the peak positions of Al 2*p* and O 1*s* core levels for the as-deposited Al_2O_3 (T_{dep} = 100 °C)/Ge structure. (b) Oxygen-to-aluminum elemental ratios estimated from the respective photoemissions of the Al_2O_3 (T_{dep} = 50–300 °C)/Ge samples subjected to RTA at 400 and 600 °C, respectively.

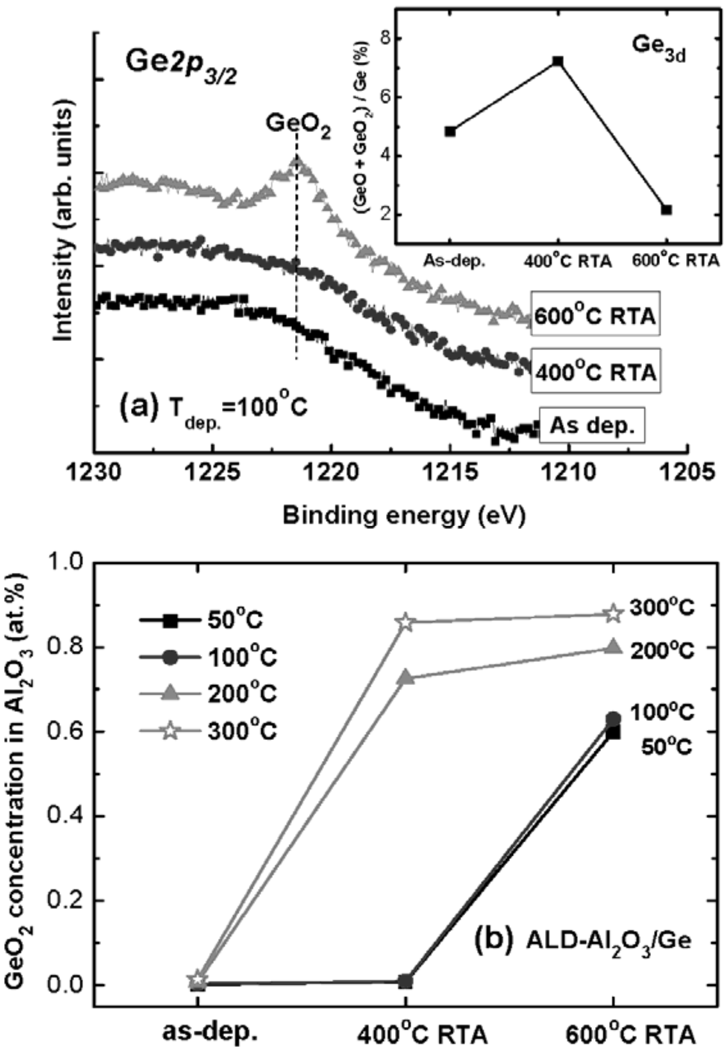


Fig. 3.6 (a) Ge $2p_{3/2}$ core level spectra of the Al_2O_3 (T_{dep} = 100 °C)/Ge structure before and after RTA. Inset: Emission ratio of Ge oxides to substrate extracted from the Ge 3*d* core level. (b) Calculated GeO_2 atomic concentration within Al_2O_3 high-*k* dielectric (T_{dep} = 50–300 °C) grown on Ge substrate before and after RTA.

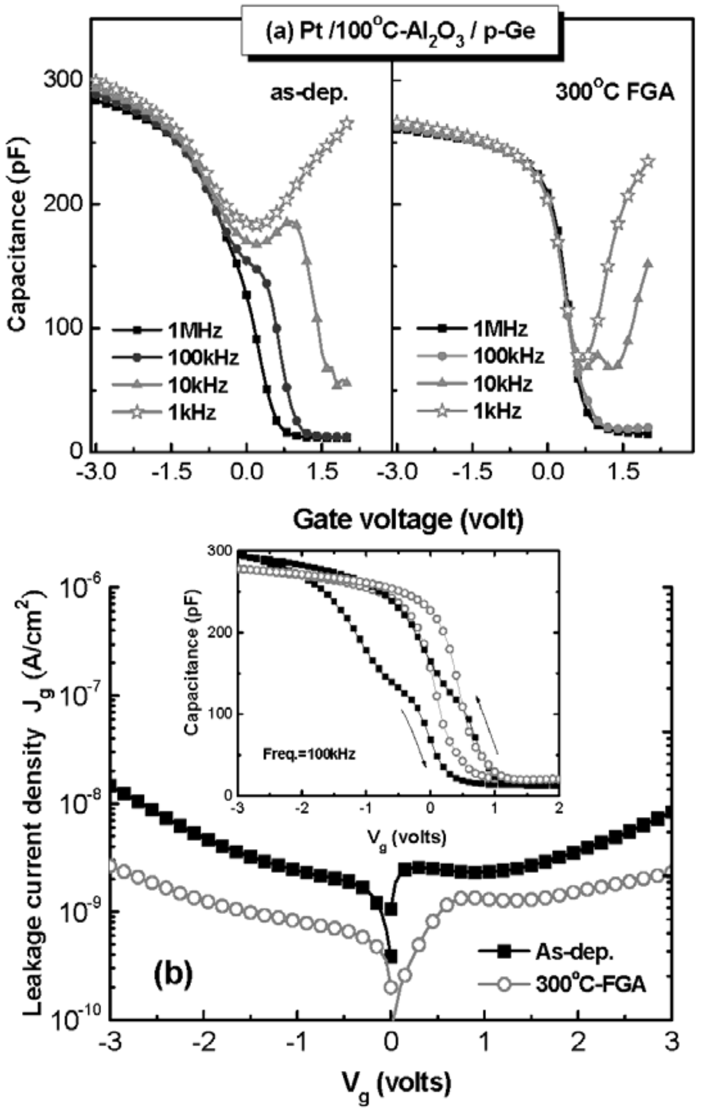


Fig. 3.7 (a) Multi-frequency *C–V* and (b) *I–V* characteristics of the Pt/Al_2O_3 (T_{dep} = 100 °C)/p-Ge MOS capacitors before and after FGA at 300 °C. Inset: Bidirectional *C–V* curves measured at 100 kHz.

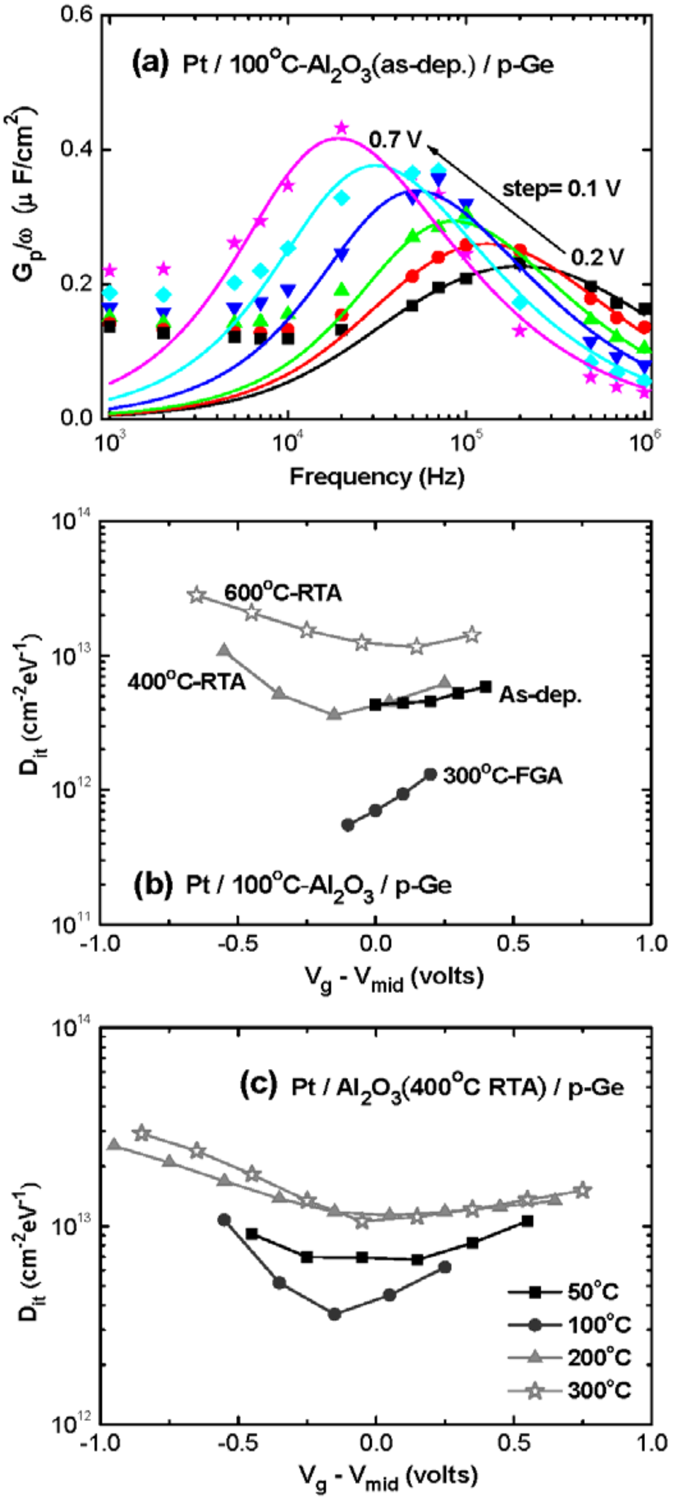


Fig. 3.8 (a) Plot of G_p/ω versus the log frequency curves for the as-deposited Pt/Al_2O_3 (T_{dep} = 100 °C)/p-Ge structure under various gate biases. Energy distribution of D_{it} for Pt/Al_2O_3/p-Ge samples (b) subjected to different thermal processing and (c) grown at values of T_{dep} from 50 to 300 °C.

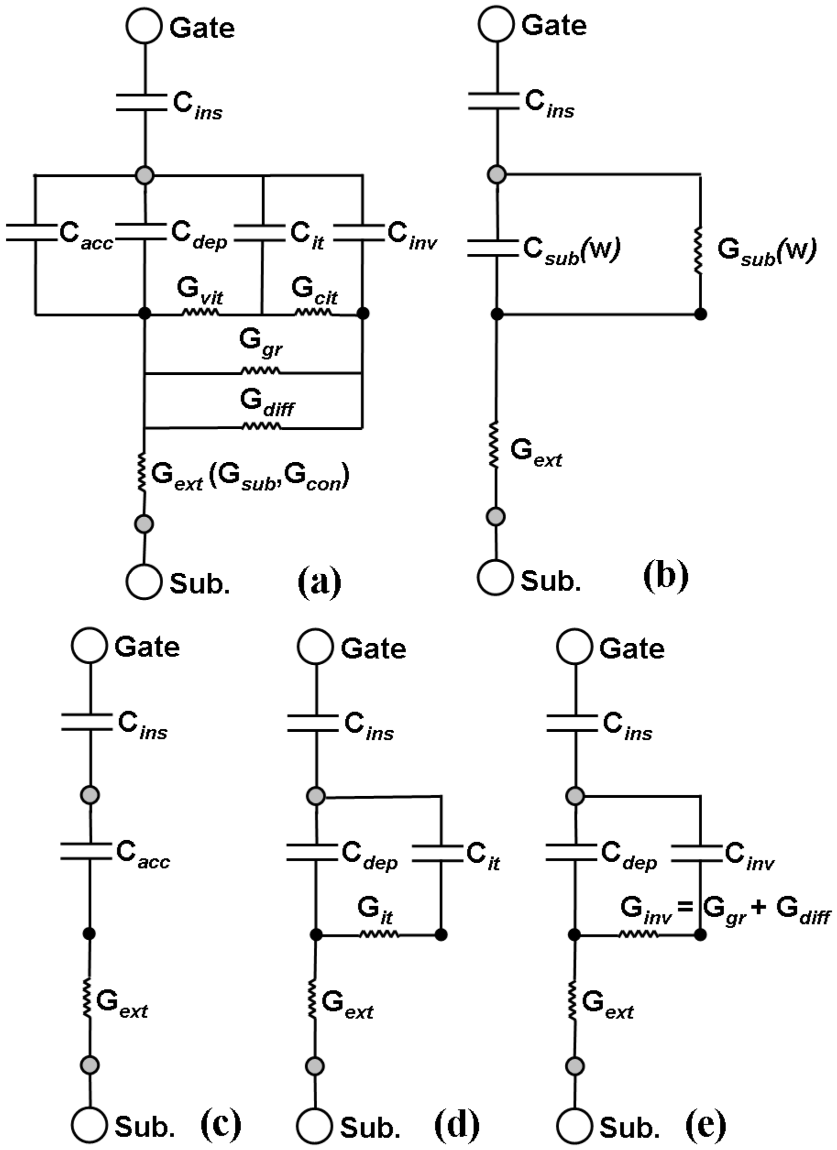


Fig. 3.9 (a) Equivalent circuit of a p-type MOS device, incorporating the effects of interface states and minority-carrier dart current, which can be characterized by (b) a parallel circuit mode with a frequency-dependent substrate capacitance $C_{\mathrm{sub}}(w)$ and conductance $G_{\mathrm{sub}}(w)$. Simplified MOS device circuits biased in (c) strong accumulation, (d) depletion, and (e) strong inversion.

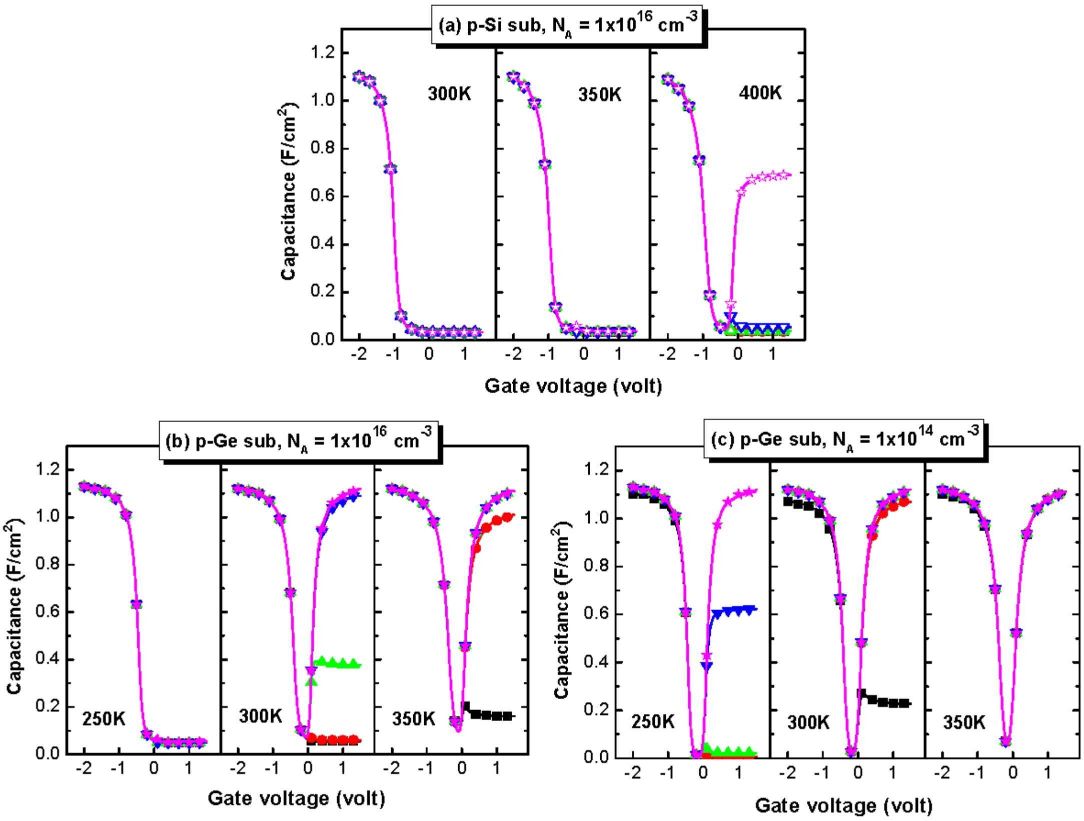


Fig. 3.10 MEDICI-simulated *C*–*V* curves of Al/SiO$_2$ gate stacks on Si and Ge substrates under measured temperatures ranging from 250 to 400 K: (a) p-Si, 10^{16} cm^{-3}; (b) p-Ge, 10^{16} cm^{-3}; (c) p-Ge, 10^{14} cm^{-3}. Note that the measured frequencies are labeled by solid symbols: square (■, 1 MHz), circle (●, 100 kHz), up-triangle (▲, 10 kHz), down-triangle (▼, 1 kHz), and star (★, 100 Hz).

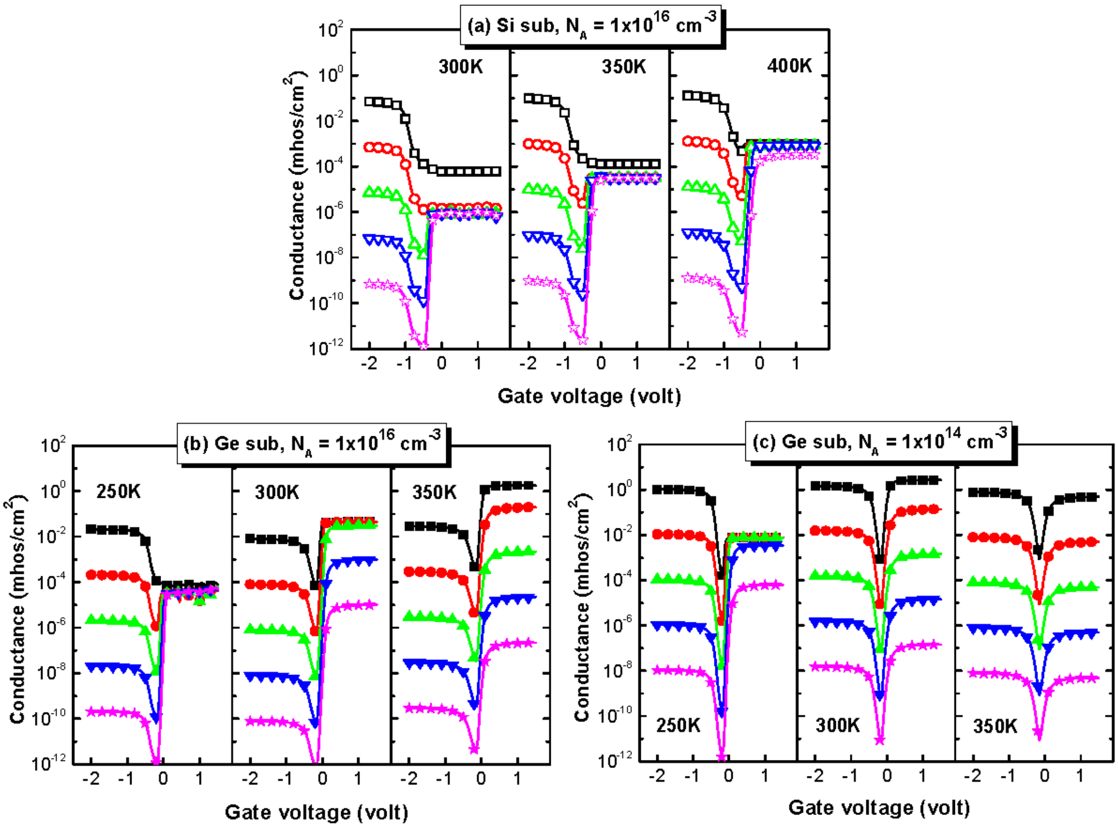


Fig. 3.11 MEDICI-simulated *G*–*V* curves of Al/SiO$_2$ gate stacks on Si and Ge substrates under measured temperatures ranging from 250 to 400 K: (a) p-Si, 10^{16} cm^{-3}; (b) p-Ge, 10^{16} cm^{-3}; (c) p-Ge, 10^{14} cm^{-3}. Note that the measured frequencies are labeled by solid symbols: square (■, 1 MHz), circle (●, 100 kHz), up-triangle (▲, 10 kHz), down-triangle (▼, 1 kHz), and star (★, 100 Hz).

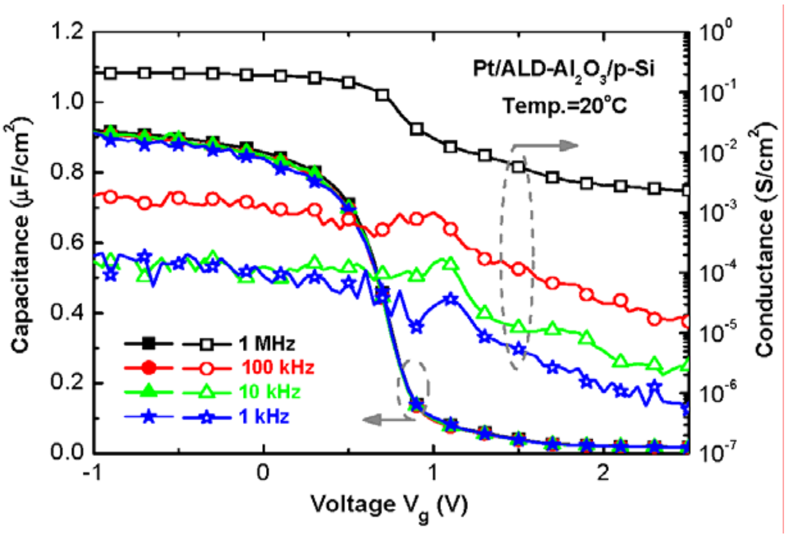


Fig. 3.12 Measured *C–V* (left-hand *y*-axis) and *G–V* (right-hand *y*-axis) curves of Pt/ALD-Al$_2$O$_3$/p-Si MOS capacitors.

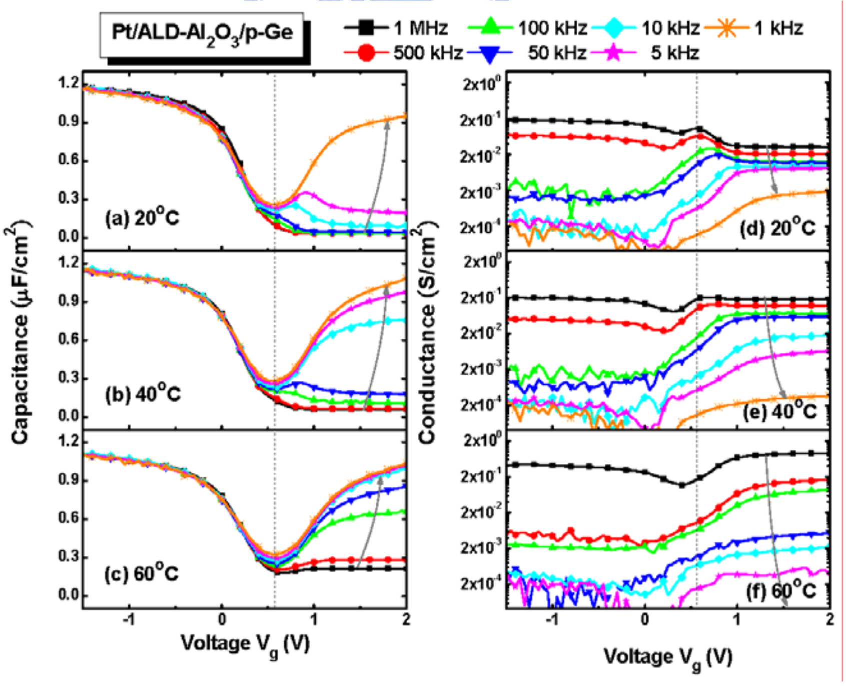


Fig. 3.13 Measured *C–V* (left-hand *y*-axis) and *G–V* (right-hand *y*-axis) curves of Pt/ALD-Al$_2$O$_3$/p-Ge MOS capacitors.

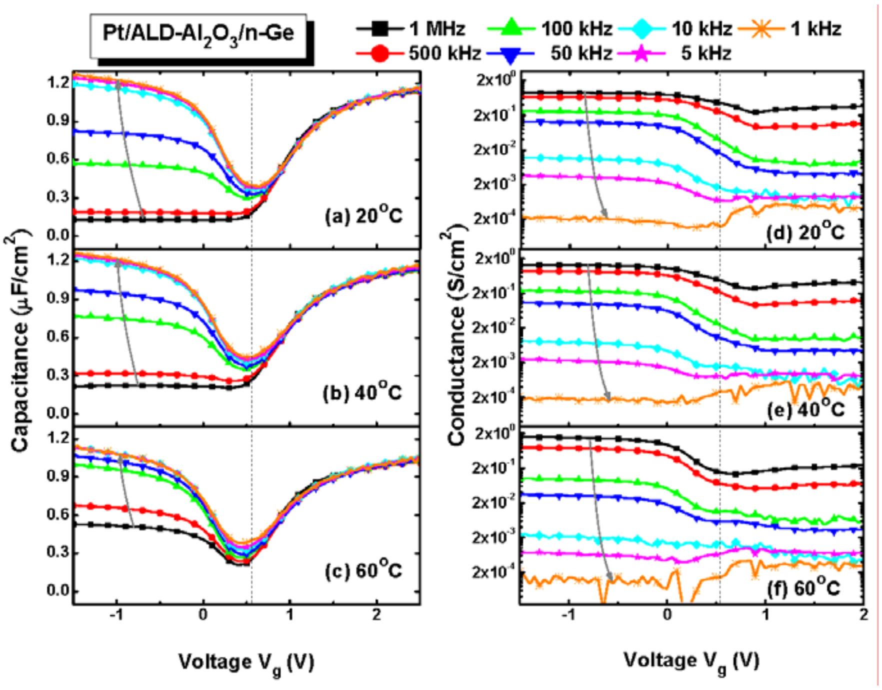


Fig. 3.14 (a)–(c) *C*–*V* and (d)–(f) *G*–*V* curves of Pt/ALD-Al_2O_3/p-Ge MOS capacitors measured at temperatures of 20, 40, and 60 °C, respectively.

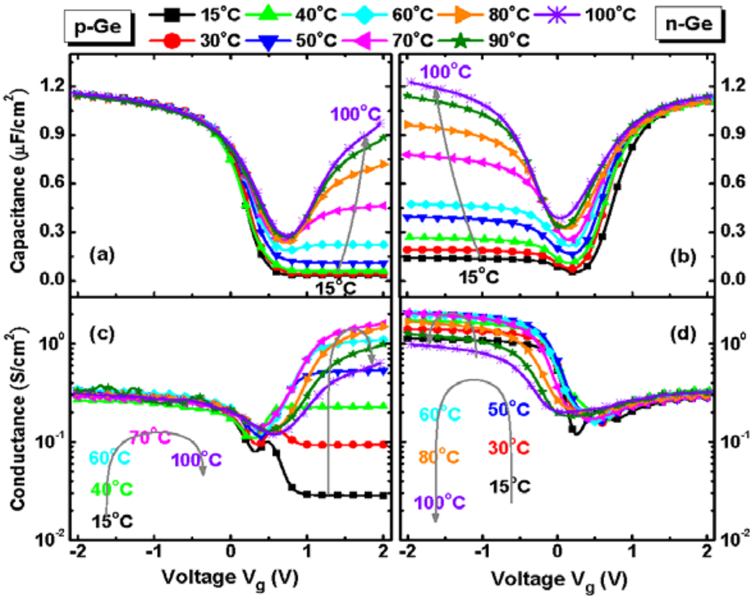


Fig. 3.15 (a)–(b) *C*–*V* and (c)–(d) *G*–*V* curves (1 MHz) of Pt/ALD-Al_2O_3 gate stacks on p-Ge and n-Ge MOS capacitors, measured at temperatures ranging from 15 to 100 °C.

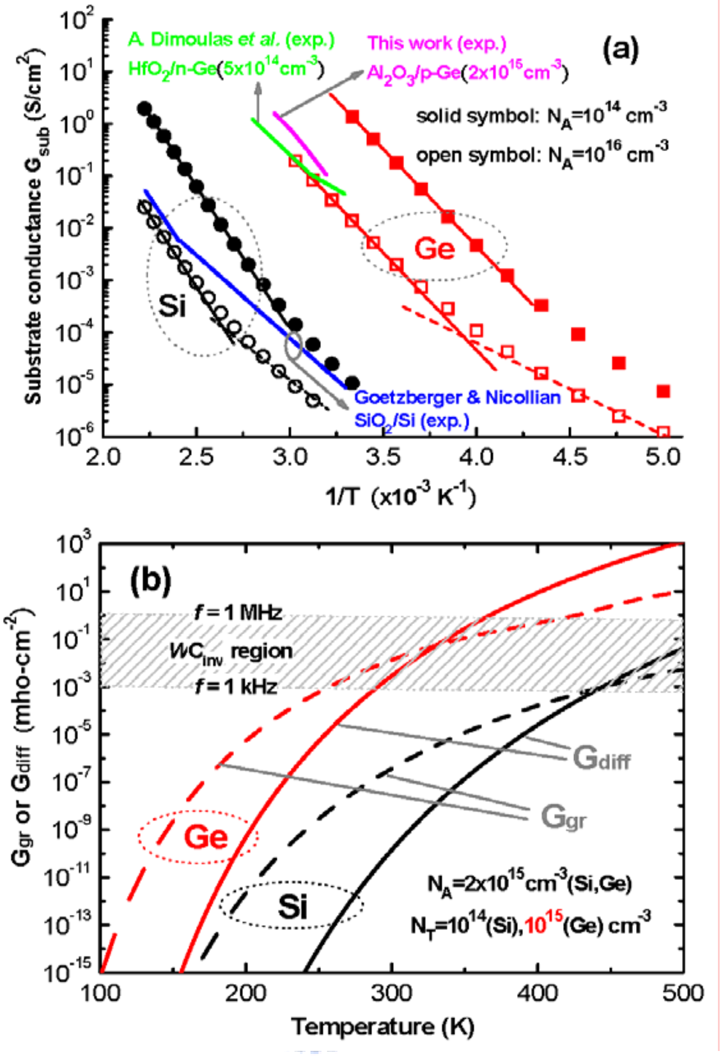


Fig. 3.16 (a) Simulated Arrhenius-dependent substrate conductances G_{sub} in Si and Ge at two dopant concentrations (10^{14} and 10^{16} cm^{-3}), plotted with the experimental data obtained in this and previous studies [14], [17]. The simulated G_{sub} data can be fitted by the diffusion conductances G_{diff} (solid lines) and *g-r* conductances G_{gr} (dashed lines), respectively. (b) Calculations of temperature-dependent G_{diff} and G_{gr} in Si and Ge substrates having dopant concentrations of 2×10^{15} cm^{-3}. The values of N_{T} were 10^{14} and 10^{15} cm^{-3} in Si and Ge, respectively. The values of the wC_{inv} term were also calculated in terms of the frequency range 1 kHz–1 MHz.

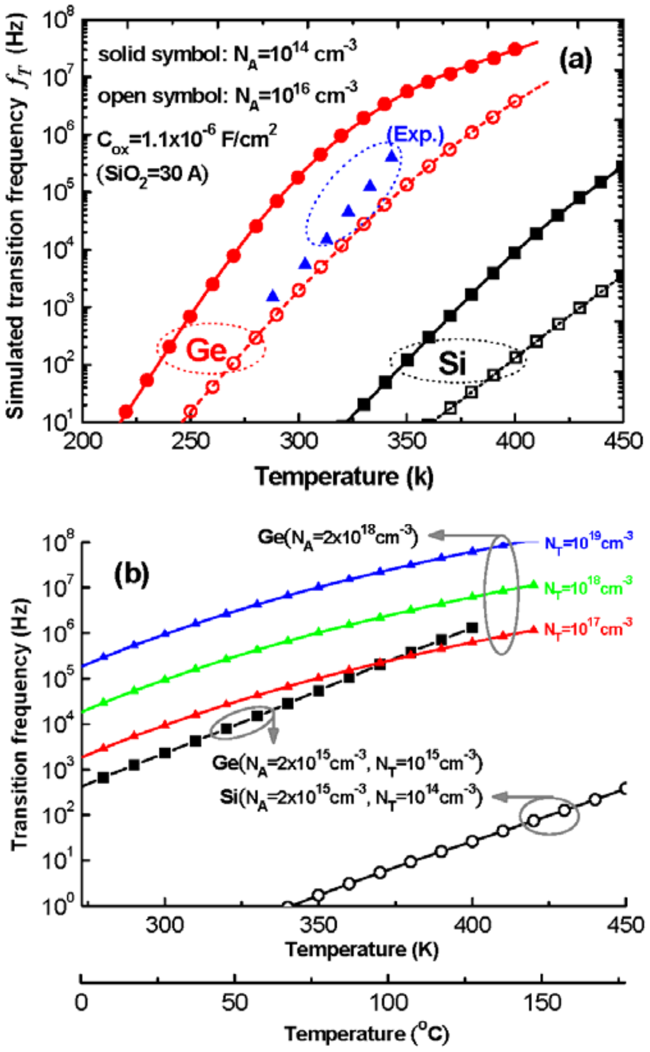


Fig. 3.17 (a) Simulated temperature-dependent transition frequencies f_{tran} in Si and Ge at two dopant concentrations (10^{14} and 10^{16} cm^{-3}), plotted along with our experimental data from Figs. 3.13 and 3.16. (b) Calculated temperature-dependent transition frequencies f_{tran} in Si and Ge substrates, determined according to the material parameters in Fig. 3.19. Different values of N_T (10^{17}–10^{19} cm^{-3}) were assumed for our highly doped Ge system.

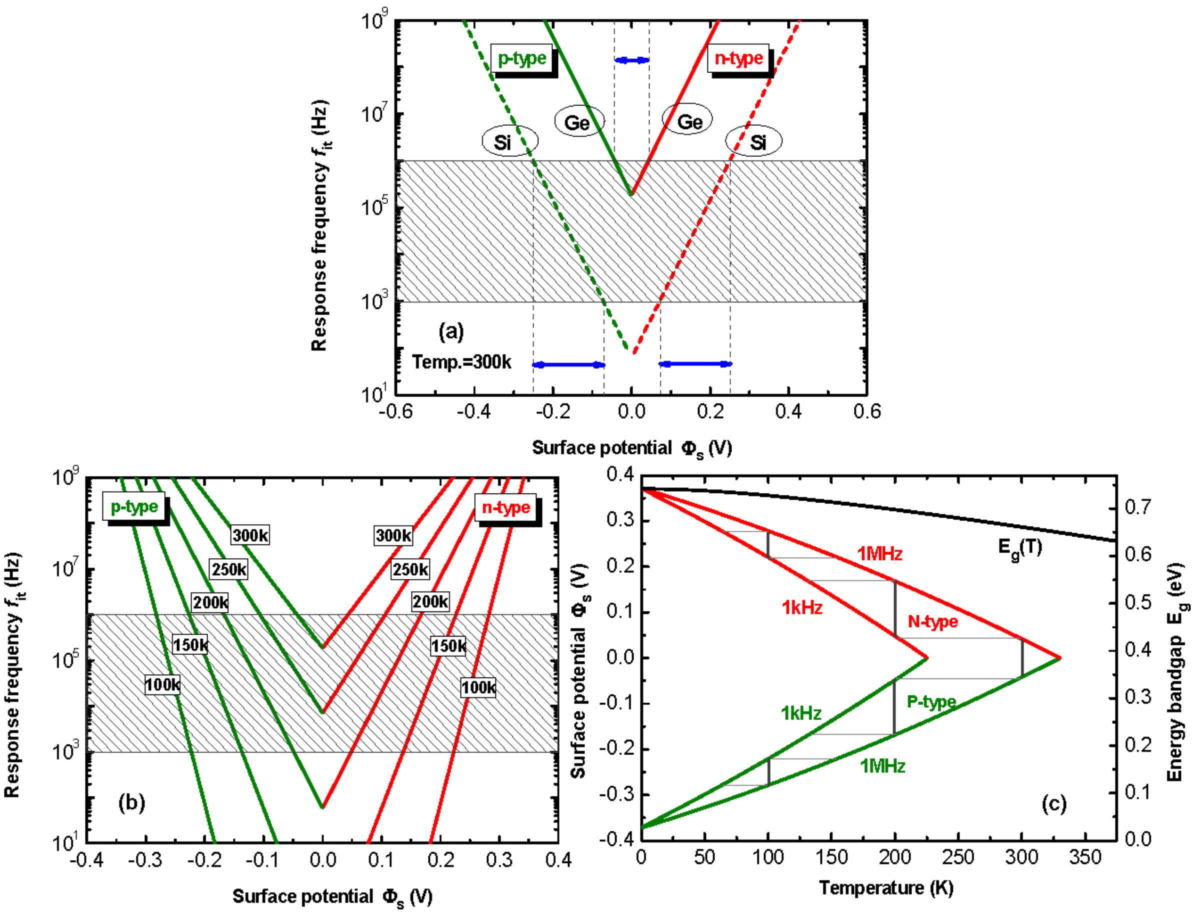


Fig. 3.18 (a) Calculated response frequency f_{it} of interface states plotted as a function of the surface potential ϕ_S for Si and Ge capacitors at RT. (b) Temperature dependence of the plots of f_{it} versus the ϕ_S for the Ge capacitor. The shadow region represents the standard frequency range 1 kHz–1 MHz used for measurements. (c) Plot of the ϕ_S dependence of observable D_{it} in the Ge bandgap at various measured temperatures (within the standard frequency range). For comparison, the temperature dependence of the Ge bandgap is presented on the right-hand *y*-axis.

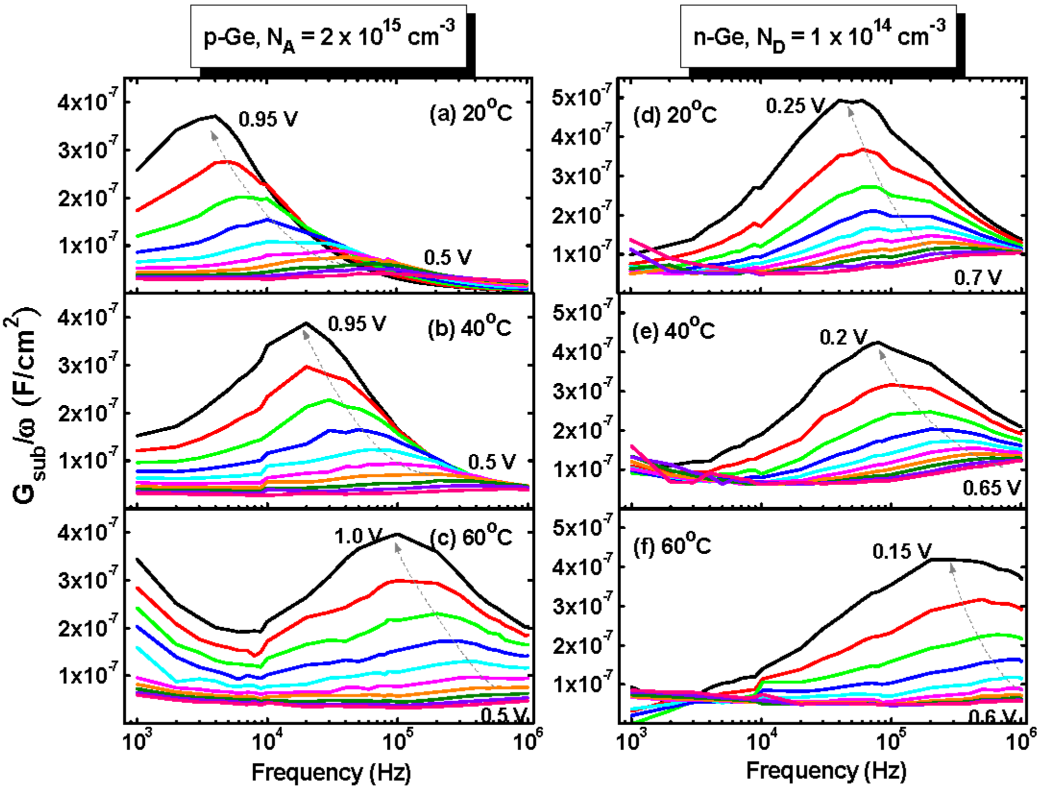


Fig. 3.19 Measured values of G_{sub}/w plotted with respect to the log frequency for Pt/ALD-Al_2O_3 gate stacks on (a)–(c) p-Ge and (d)–(f) n-Ge substrates at temperatures of 20, 40, and 60 °C, respectively.

Chapter 4

E-gun Evaporated Gd_2O_3 Dielectric Films on GaAs Substrates

4.1 Introduction

GaAs metal-oxide-semiconductor (MOS) devices with different high-*k* gate dielectrics have been of more interest in recent years. Examples of these include the well-known Gd_2O_3 [1], Al_2O_3 [2], TiO_2 [3], and Hf-based oxides [4], [5], respectively. The primary bottleneck of these high-*k*/GaAs structures in realizing the practical devices is a large density of interfacial states, which causes significant Fermi-level pinning effects, e.g., the low modulation of surface potential and other poor electrical properties. The carbon contamination, the native oxides, and, in particular, the arsenic element segregation are commonly detected species on the GaAs surface [6]. In other words, understanding the chemical bonding configuration at the dielectric/GaAs interface is of the utmost importance and its quality also determines the device performance since the GaAs surface is likely to debase during the dielectric deposition and thermal anneal processing. Several groups have demonstrated several promising capacitor and transistor characteristics by performing various surface preparation techniques, mainly comprising three aspects of the wet-chemical cleaning, interface passivation, and thermal treatment, respectively. Numerous acidic or basic wet solutions have been extensively studied; it was found that the amount of impurity contamination and residual components strongly depended on the entire cleaning procedures [7]-[9]. Prior to the deposition of the gate dielectrics, the passivations of GaAs surface—the sulfide-based immersion [10], [11], the silicon/germanium interfacial layer [12]-[14], and the coverage of lattice-matched dielectric thin-film [15]—also have been reviewed again in recent years. Additionally, thermal desorption in the high vacuum system especially for the molecular beam epitaxy (MBE) is another widely used approach to clean III-V deposited surface [16], [17]. In this session, we modified the wet-chemical cleaning and sulfide passivation processes to improve the electrical performance of Gd_2O_3 dielectric thin film deposited on the n-GaAs substrate. Low gate leakage, diminutive hysteresis and reduced interface state density can be achieved in the fabricated Gd_2O_3/GaAs structures.

4.2 Experimental Procedures

MOS structures were fabricated on the highly-doped (~1 x 10^{18} cm^{-3}) n-type GaAs substrates. A series of wet-chemical cleaning processes (WCPs) were applied and listed in Table I. Both the HCl and NH_4OH aqueous solutions with the same diluted concentration (acid or alkaline/H_2O, 1:10) was used in GaAs surface clean. Subsequently, the samples were dipped into aqueous ammonium sulfide solution [$(NH_4)_2S$/DI water, 1:100] at two different processing temperatures of RT and 80 °C, respectively, with the fixed immersion time of 5 min for studying the sulfur bonding states as well as the efficiency of oxide removal. After undergoing these WCPs, we measured the roughness variation of GaAs surface morphology within the scanning area of 1×1 μm^2 by the atomic force microscopy (AFM). Meanwhile, we employed x-ray photoelectron spectroscopy (XPS) that Al $K\alpha$ ($h\nu$=1486.6 eV) was used as an excitation source and the take-off angle was fixed at 60º in order to understand the surface chemistry. High surface-sensitive As $2p_{3/2}$ and Ga $2p_{3/2}$ core level spectra, after subtraction of the Shirley background, were analyzed by least-squares fitting method—the contributed components comprised a Gaussian line shape convoluted with a Lorentzian broadening function. In addition, for examining the impact of the WCPs on the properties of the resultant capacitor, we deposited the Gd_2O_3 thin film as gate dielectric using electron beam evaporation with pure Gd_2O_3 ingot, followed by performing the post-deposition annealing (PDA) at 500

°C for 10 s in Ar/O_2 mixed ambient for further condensation. Most importantly, the distribution of $(Ga,As)_2O_x$ oxides and GaAs-related defects into the high-*k* dielectric after thermal processing was examined. A 600-Å-thick layer of sputtered Pt was patterned as circular capacitor electrode via a specific shadow mask; while the backside Ohmic contact was formed by e-beam evaporation of In/Pt (300/300 Å) bilayer. The capacitance–voltage (*C*–*V*) and the gate leakage (*I*-*V*) characteristics for the fabricated Pt/Gd_2O_3/GaAs MOS structures were measured using an HP4284 LCR meter and a Keithley 4200 semiconductor analyzer system, respectively. The level of fast interface states was evaluated by frequency-dependent conductance method, while the capacitance-equivalent-thickness (CET) was determined by the value of accumulation capacitance (10-kHz) at gate voltage $V_g = 3$ V.

4.3 Modified Wet-Chemical Clean and Sulfidization Processes

4.3.1 Surface Chemistry and Morphology of Cleaned GaAs Substrates

Figures 4.1 and 4.2 show the respective As $2p_{3/2}$ and Ga $2p_{3/2}$ photoemission spectra of the GaAs surface after four WCPs and all the deconvoluted peaks; the fitting results are summarized in **Table I**. It was seen in **Fig. 4.1(a)**, as compared to the others, that more As oxides as well as amorphous As preferred to accumulate on the GaAs surface subject only to HCl acidic solution etching. The chlorine ion intends to attack the GaAs surface forming soluble gallium chloride [18] and the simultaneously produced As-rich overlayer can then be partly oxidized to form As_2O_3 and As_2O_5 species on the outmost surface. From the viewpoint of thermodynamics, the Ga atoms are more easily oxidized because the Gibbs energy of the formation of Ga_2O_3 (ca. -999 kJ/mol) at RT is lower than that of As_2O_3 (ca. -576 kJ/mol) [19]. However, our experimental observation is obviously contradictory to this prediction. This is due to the fact that Gibbs energy is not the sole determining factor but the constituent distribution as well as the oxidized probability also play a big role in the real oxidation processing [7]. We, thus, suggest that excess As atoms possibly block the access of chlorine to underlying gallium atoms during HCl clean, which also act as a passivation layer to hinder the interfacial gallium oxidation. This result is similar to what observed in the previous studies in which the GaAs substrate was cleaned by the acid HF [20], [21].

Subsequently performing $(NH_4)_2S$ immersion at RT was found, as shown in **Fig. 4.1(b)**, to effectively diminish the oxidized As species; raising the temperature up to 80 °C lessened them further. As reported, wet sulfide solution comprising $(NH_4)_2S$ or Na_2S agent are capable of suppressing these undesirable species on GaAs by forming sulfur-related chemical bonds, where the outer oxide will be etched away and then reactive sulfur starts to create bonds with surface atoms [22]. The dissolution of ammonium sulfide produces both the weak acid HS^- ions and H_2S molecules adsorbed onto the GaAs, which is closely correlated to the electrostatic interaction and surface dipole moment [23]. We suppose that the solution temperature affects both the rate of oxide removal and the creation of sulfur bonds mainly in terms of their activation energies; also, it determines the dissociation of $(NH_4)_2S$ solution. The higher removal efficiency at increased temperature may be ascribed to the enhanced migration of etching agent into oxide layer [24] and the increasing solubility of As oxides [25].

In **Fig. 4.1(c)** and **4.1(d)**, another interesting feature was noticed that increasing the sulfide-treated temperature and adding the NH_4OH clean caused the rearrangement of the sulfur bonding state, i.e., more Ga-S bonds did emerge relative to the reduced As-S bonds. Such a surface bonding reconstruction was attributed to the following conversion mechanisms: (a) AsS_x sulfidized compounds transfer into highly stable GaS_x species by reacting with GaAs surface [26]. (b) since As-S chemical bond easily breaks at temperature as low as 200 °C [27]-[29], indicative of the lower bonding strength, the loose sulfur atoms thus prefer to create the strong Ga-S bonds [24]. Furthermore, the NH_4OH alkaline solution was critical in abating these surface components compared to the results obtained in the untreated samples; we characterized that the NH_4OH rinse obviously decreased the content of not only As-O and As-As species but also Ga-O species. Here, we can only have speculation regarding the underlying mechanism since the explicit role of NH_4^+ and OH^- ions in the dissolution of GaAs surface components are still in controversy [25]. Two kinds of surface cleaning mechanism, to our knowledge, have been conjectured: one is that OH^- ions directly react with either Ga or As chemical species forming the soluble compounds such as GaO_3^{3-} and AsO_2^- with the participation of free holes from the semiconductor [29]; another is that the former reaction initially produces the hydroxides in the form of $Ga(OH)_3$/$As(OH)_3$, which are transformed into the soluble complexes like hydroxygallate aggregates $NH_4Ga(OH)_4$ and $(NH_4)_3AsO_4$, via the assistant of free NH_4^+ agent [25]. Irrespective of the detailed dissolution procedure, the resultant defect suppression can then expected being able to promote the interface quality between Gd_2O_3 deposited film and GaAs substrate, thereby achieving the better insulator properties. This claim was first supported by the improved surface morphology after the WCP modulation, as displayed in **Fig. 4.3**. The root-mean-square (RMS) roughness of HCl-etched GaAs surface can be reduced from ca. 0.35 nm to ca. 0.25 nm by rinsing in either $(NH_4)_2S$ at 80 °C or NH_4OH aqueous solution.

4.3.2 Physical and Electrical Characteristics of Gd_2O_3/GaAs Structures

Figures 4.4(a) and **4.4(b)** display the capacitor characteristics of Pt/Gd_2O_3/n-GaAs structures subjected to different WCPs. In the following discussion we denoted the MOS capacitor—underwent the HCl and $(NH_4)_2S$ two processes—without and with the NH_4OH clean as the “HS-sample” and “HNS-sample”, respectively. The bidirectional *C-V* curves in **Fig. 4.4(a)** showed that the HNS-sample relative to the HS-sample had a high value of the accumulation capacitance. However, they still presented the anti-clockwise hysteresis loop, which could be eliminated by increasing the sulfidized temperature up to 80 °C. From the variation of $(NH_4)_2S$ concentration level, an increase in sulfide concentration from 1% to 10% plainly degraded the overall accumulation capacitance. In addition, since the poor insulator-substrate interface leads to a remarkable shift of the flatband voltage (V_{FB}), i.e., the large frequency dispersion at the accumulation/depletion region, in frequency–dependent *C-V* curves, hence, we qualitatively examined the Fermi level (E_f) pinning effect through variations of the $\triangle C$ and $\triangle V$ that were defined as follows:

$$\triangle C(@V_g = 3\text{ V}) = 1 - C_{acc}(@1\text{ MHz}) / C_{acc}(@1\text{ kHz}) \tag{4.1}$$

$$\triangle V(@C_{FB}) = V_g(@1\text{ kHz}) - V_g(@100\text{ kHz}), \tag{4.2}$$

where $\triangle C$ is the deviation of the accumulation capacitance measured at 1-kHz and 1-MHz for the V_g of 3 V, while $\triangle V$ is the voltage difference between 1-kHz and 100-kHz *C-V* curves achieving the value of the flatband capacitance (C_{FB}). In **Fig. 4.4(b)**, the respective $\triangle C$ and $\triangle V$ were ca. 64% and ca. 2.2 V for the HS sample; with both the values could be reduced to ca. 38% and to ca. 1.4 V providing that we added the NH_4OH clean with the sulfidization at 80 °C. These improvements confirmed that the WCP optimization further unpinned the interface Fermi level. Due to a high density of surface states formed by segregated As atoms, the E_f at GaAs (100) surface being pinned at ca. 0.8 V below the conduction band (E_c) minimum was demonstrated [30], [31]. The possible energy-level models, basically, based on the framework of a donor state near the midgap with an acceptor state close to the valence band (E_v) edge, also have been proposed [32]. It seems that the lower surface states induced by sulfide passivation can cause a movement of the E_f back toward the E_c [10], [33]. However, this conclusion is not confirmative since some other previous experimental findings that the E_f moved toward the E_v by ca. 0.2 eV were also illustrated [34], [35]. We suggest that the movement of surface Fermi level is related to the actual sulfidation procedure and the resulting sulfur adsorption; the E_f intends to shift back to E_c provided that more Ga-S bonds form at the interface [36], for example, which can be obtained after high-temperature annealing. On the as-treated sample the formation of less stable As-S bonds compared to Ga-S ones has been deduced to induce the extra gap states [37]; this consequence directly affects the shift behavior of the E_f in experiments. In our case, since the interfacial state density (D_{it}) reduced from the order of 10^{13} $cm^{-2}eV^{-1}$ to that of 10^{12} $cm^{-2}eV^{-1}$, we believe that the improved WCP, along with a relatively more GaS_x formation, did facilitate to lessen the overall surface recombination centers, in particular for donors induced by As_{Ga} anti-sites. Evidently, it promotes the carrier population at the dielectric interface at high frequency of 1 MHz, coinciding with the consequence of △C and △V reduction.

Figure 4.5 shows the corresponding *I-V* characteristics and the inset displays the comparison of gate leakage J_g at $V_g = (V_{FB} + 1)$ V for all samples with different WCPs. The result clearly indicated that the WCP—[HCl + NH_4OH + sulfide(1%, 80 °C)] certainly led to the better leakage performance that the J_g could be reduced to ca. 1.5×10^{-5} A/cm^2 at $V_g = (V_{FB} + 1)$ V; however, either increasing the concentration to 10% or lowering the temperature to RT caused J_g to increase considerably. Our explanations for these experimental findings are given below: in the course of performing $(NH_4)_2S$ immersion, one or two GaAs sulfide monolayers were formed until the bonding saturation, and then sulfur ions remained to reside on the outer surface, probably in the form of either molecules or complex compound. Excess sulfur contamination might be induced by the increased concentration; we evidenced this consequence by the AFM images that the 1%-sulfide could flatten the morphology of HCl-etched surface, whereas an increased roughness was seen after 10%-sulfide due to the presence of small particles (not shown here). Subsequent annealing-induced diffusion toward the Gd_2O_3 thin film possibly induced the leakage path and/or behaves as the leaky defect, causing the gate leakage degradation with an increased equivalent-oxide-thickness (EOT). In addition, as we mentioned earlier, more As-S bonds formed at RT than at 80 °C, and they would be reduced to the elemental arsenic since kinetics naturally drives the reaction below [26].

$$GaAs + AsS_x \rightarrow GaS_x + 2As \tag{4.3}$$

The higher sulfidized temperature, i.e. at 80 °C, reduced the As suboxides and arsenic accumulation at high-*k*/GaAs interface, therefore, resulting in the lowered J_g and less severe charge trapping. This fact also implies that forming the stable Ga-S chemical bonds at the interface will be indispensable in the pursuit of high-performance high-*k* gate dielectric and interface on GaAs substrate. **Fig. 4.6** shows the XPS spectra for these samples after 500 °C PDA. It was found that both Ga and As oxide components had been incorporated into the annealed Gd_2O_3 films. The estimated concentration of Ga_2O_x is 13, 6, and 4% with that of As_2O_x below 3% for the respective samples. The enrichment in the Ga-O relative to As-O species in bulk Gd_2O_3 can be reasonably understood by the following heat reaction,

$$GaAs + As_2O_3 \rightarrow Ga_2O_3 + 4As, \tag{4.4}$$

and this chemical transformation is thermodynamically favorable at RT. We did observe a relatively high Ga_2O_3 concentration in the HS sample, which was accompanied with the serious desorption of the interfacial arsenic into high-*k* dielectric film. As a result, we think that it is a direct attribute of J_g increase and other degraded electrical properties.

Figure 4.7 plots the characteristic of J_g versus the CET or EOT along with the previously published data [3], [5], [13]-[15], [38], [39]. Apparently, we observed that the Gd_2O_3/n-GaAs capacitors through WCP optimization did exhibit the excellent insulating properties as compared to HfO_2 dielectrics reported on the n-GaAs in combination with Si or Ge interfacial passivation layers. A lower CET of ca. 20 Å with a reduced J_g of ca. 10^{-5} A/cm^2 at $(V_{FB} + 1)$ V was accomplished. The continuously optimized interface quality via process modification is expected to further improve the Gd_2O_3/GaAs electrical performance, which thus be considered as a promising MOS device structure.

4.5 Conclusions

In Chapter 4, we demonstrated the improved electrical characteristics of the Gd_2O_3

dielectric thin films on the n-GaAs substrate by manipulating the wet-chemical clean and $(NH_4)_2S$ passivation. With the XPS analysis, the HCl-cleaned GaAs surface was characterized to possess the oxide species mainly in the form of As_2O_x near the outmost surface and Ga_2O_x with elemental arsenic close to the interface. These undesirable components could be suppressed through rinsing in NH_4OH alkaline solution and then performing the sulfidization at 80 °C, as a result, alleviating the E_f pinning effect on the Gd_2O_3/GaAs capacitor performance. The higher oxide capacitance and alleviated frequency dispersion at the accumulation/depletion regimes were achieved, accompanied by the negligible charge trapping (<100 mV). Accordingly, the gate leakage J_g was lowered to ca. 10^{-5} A/cm^2 at gate voltage $V_g = (V_{FB} + 1)$ V, which was comparable to the recently reported performance of HfO_2/GaAs structure with an ultra-thin Si/Ge interfacial layer. We attributed the electrical improvements to the enhanced stabilization of high-*k*/sulfur-terminated GaAs interface due to abatement of the native oxides and excess arsenic segregation.

References (Chapter 4)

[1] C. P. Chen, Y. J. Lee, Y. C. Chang, Z. K. Yang, M. Hong, J. Kwo, H. Y. Lee, and T. S. Lay, “Structural and electrical characteristics of $Ga_2O_3(Gd_2O_3)/GaAs$ under high temperature annealing,” *J. Appl. Phys*. vol. **100**, p. 104502, 2006.

[2] H.-L. Lu, L. Sun, S.-J. Ding, M. Xu, D. W. Zhang, and L.-K. Wang, “Characterization of atomic-layer-deposited $Al_2O_3/GaAs$ interface improved by NH_3 plasma pretreatment,” *Appl. Phys. Lett.* vol. **89**, p. 152910, 2006.

[3] M.-K. Lee, C.-F. Yen, J.-J. Huang, and S.-H. Lin, “Electrical characteristics of postmetallization-annealed MOCVD-TiO_2 films on ammonium sulfide-treated GaAs,” *J. Electrochem. Soc.* vol. **153**, p. F266, 2006.

[4] M. H. Zhang, M. Oye, B. Cobb, F. Zhu, H. S. Kim, I. J. Ok, J. Hurst, S. Lewis, A. Holmes, J. C. Lee, S. Koveshnikov, W. Tsai, M. Yakimov, V. Torkanov, and S. Oktyabrsky, “Importance of controlling oxygen incorporation into $HfO_2/Si/n$-GaAs gate stacks,” *J. Appl. Phys.* vol. **101**, p. 034103, 2007.

[5] M. H. Zhang, I. J. Ok, H. S. Kim, F. Zhu, T. Lee, G. Thareja, L. Yu, and J. C. Lee, “Characteristics of sputtered $Hf_{1-x}Si_xO_2/Si/GaAs$ gate stacks,” *Appl. Phys. Lett.* vol. **89**, p. 042902, 2006.

[6] J. T. Wolan, W. S. Epling, and G. B. Hoflund, “Characterization study of GaAs(001) surfaces using ion scattering spectroscopy and x-ray photoelectron spectroscopy,” *J. Appl. Phys.* vol. **81**, p. 6160, 1997.

[7] J. S. Song, Y. C. Choi, S. H. Seo, D. C. Oh, M. W. Cho, T. Yao, and M. H. Oh, “Wet chemical cleaning process of GaAs substrate for ready-to-use,” *J. Crystal Growth* vol. **264**, p. 98, 2004.

[8] G. C. Desalvo, C. A. Bozada, J. L. Ebel, D. C. Look, J. P. Barrette, C. L. A. Cerny, R. W. Dettmer, J. K. Gillespie, C. K. Havasy, T. J. Jenkins, K. Nakano, C. I. Pettiford, T. K. Quach, J. S. Sewell, and G. D. Via, “Wet chemical digital etching of GaAs at room

temperature," *J. Electrochem. Soc.* vol. **143**, p. 3652, 1996.

[9] A. Saletes, J. Massies, and J. P. Contour, "Residual carbon and oxygen surface contamination of chemically etched GaAs (001) substrates," *Jap. J. Appl. Phys.* vol. **25**, p. L48, 1986.

[10] J.-K. Yang, M.-G. Kang, and H.-H. Park, "Chemical and electrical characterization of Gd_2O_3/GaAs interface improved by sulfur passivation," *J. Appl. Phys.* vol. **96**, p. 4811, 2004.

[11] V. N. Bessolov, E. V. Konenkova, and M. V. Lebedev, "Solvent effect on the properties of sulfur passivated GaAs," *J. Vac. Sci. Technol.* B vol. **14**, p. 2761, 1996.

[12] F. Zhu, S. Koveshnikov, I. Ok, H. S. Kim, M. Zhang, T. Lee, G. Thareja, L. Yu, J. C. Lee, W. Tsai, V. Tokranov, M. Yakimov, and S. Oktyabrsky, "Depletion-mode GaAs metal-oxide-semiconductor field-effect transistor with amorphous silicon interface passivation layer and thin HfO_2 gate oxide," *Appl. Phys. Lett.* vol. **91**, p. 043507, 2007.

[13] D. Shahrjerdi, M. M. Oye, A. L. Holmes, Jr., and S. K. Banerjee, "Unpinned metal gate/high-*k* GaAs capacitors: fabrication and characterization," *Appl. Phys. Lett.* vol. **89**, p. 043501, 2006.

[14] H.-S. Kim, I. Ok. M. Zhang, T. Lee, F. Zhu, L. Yu, J. C. Lee, "Metal gate-HfO_2 metal-oxide-semiconductor capacitors on n-GaAs substrate with silicon/germanium interfacial passivation layers," *Appl. Phys. Lett.* vol. **89**, p. 222903, 2006.

[15] M. Zhu, C.-H. Tung, Y.-C. Yeo, "Aluminum oxynitride interfacial passivation layer for high-permittivity gate dielectric stack on gallium arsenide," *Appl. Phys. Lett.* vol. **89**, p. 202903, 2006.

[16] A. G.-Cervantes, Z. R.-Alvarez, M. L.-Lopez, E. L.-Luna, and I. H.-Calderon, "GaAs surface oxide desorption by annealing in ultra high vacuum," *Thin Solid Film* vol. **373**, p. 159, 2000.

[17] M. Yamada and Y. Ide, "Anomalous behaviors observed in the isothermal desorption of

GaAs surface oxides," *Surf. Sci.* vol. **339**, p. L914, 1995.

[18] V. L. Alperovich, O. E. Tereshchenko, N. S. Rudaya, D. V. Sheglov, A. V. Latyshev, and A. S. Terekhov, "Surface passivation and morphology of GaAs(100) treated in HCl-isopropanol solution," *Appl. Surf. Sci.* vol. **235**, p. 249, 2004.

[19] D. R. Lide, *CRC handbook of chemistry and physics: a ready-reference book of chemical and physical data*, 84th ed., CRC Press, 2003.

[20] K. Menda, E. Kanda, and T. Yokoyama, "ARXPS analysis on As-passivated GaAs surfaces by HF dipping method," *Jap. J. Appl. Phys.* vol. **29**, p. L391, 1990.

[21] S. Adachi and D. Kikuchi, "Chemical etching characteristics of GaAs(100) surfaces in aqueous HF solutions," *J. Electrochem. Soc.* vol. **147**, p. 4618, 2000.

[22] S. Arabasz, E. Bergignat, G. Hollinger, and J. Szuber, "XPS study of surface chemistry of epiready GaAs(100) surface after $(NH_4)_2S_x$ passivation," *Vacuum* vol. **80**, p. 888, 2006.

[23] V. N. Bessolov, E. V. Konenkova, and M. V. Lebedev, "Sulfidization of GaAs in alcoholic solutions: A method having an impact on efficiency and stability of passivation," *Mater. Sci. and Eng.* B vol. **44**, p. 376, 1997.

[24] S. Arabasz, E. Bergignat, G. Hollinger, and J. Szuber, "XPS analysis of surface chemistry of near surface region of epiready GaAs(100) surface treated with (NH4)(2)S-x solution," *Appl. Surf. Sci.* vol. **252**, p. 7659, 2006.

[25] C. Bryce and D. Berk, "Kinetics of GaAs dissolution in H_2O_2-NH_4OH-H_2O solutions," *Ind. Eng. Chem. Res.* vol. **35**, p. 4460, 1996.

[26] Yu. V. Medvedev, "Thermodynamic stability of GaAs sulfur passivation," *Appl. Phys. Lett.* vol. **64**, p. 3458, 1994.

[27] T. Scimeca, Y. Muramatsu, M. Oshima H. Oigawa and Y. Nannichi, "Temperature-dependent changes on the sulfur-passivated GaAs (111)*A*, (100), and (111)*B* surfaces," *Phys. Rev.* B vol. **44**, p. 12927, 1991.

[28] H. Sik, Y. Feurprier, C. Cardinaud, G. Turban, and A. Scavennec, “Reduction of recombination velocity on GaAs surface by Ga-S and As-S bond-related surface states from $(NH_4)_2S$ treatment,” *J. Electrochem. Soc.* vol. **144**, p. 2106, 1997.

[29] D. Paget, J. E. Bonnet, V. L. Berkovits, P. Chiaradia, and J. Avila, “Sulfide-passivated GaAs(001). I. Chemistry analysis by photoemission and reflectance anisotropy spectroscopies,” *Phys. Rev.* B vol. **53**, p. 4604, 1996.

[30] W. E. Spicer, P. W. Chye, P. R. Skeath, C. Y. Su, and I. J. Linden, “New and unified model for Schottky barrier and III–V insulator interface states formation,” *J. Vac. Sci. Technol.* A vol. **16**, p. 1422, 1979.

[31] M. Passlack, E. F. Schubert, W. S. Hobson, M. Hong, N. Moriya, S. N. G. Chu, K. Konstadinidis, J. P. Mannaerts, M. L. Schnoes, and G. J. Zydzik, “Ga_2O_3 films for electronic and optoelectronic applications,” *J. Appl. Phys.* vol. **77**, p. 686, 1995.

[32] C. J. Spindt and W. E. Spicer, “Sulfur passivation of GaAs surfaces: A model for reduced surface recombination without band flattening,” *Appl. Phys. Lett.* vol. **55**, p. 1653, 1989.

[33] T. Simonsmeier, A. Ivankov, and W. Bauhofer, “Sulfidic photochemical passivation of GaAs surfaces in alcoholic solutions,” *J. Appl. Phys.* vol. **97**, p. 084910, 2005.

[34] H. Sugahara, M. Oshima, H. Oigawa, H. Shigekawa, and Y. Nannichi, “Synchrotron radiation photoemission analysis for $(NH_4)_2S_x$-treated GaAs,” *J. Appl. Phys.* vol. **69**, p. 4349, 1991.

[35] L. Koenders, M. Blomacher, and W. Monch, “Electronic properties of sulfur adsorbed on cleaved GaAs surfaces,” *J. Vac. Sci. Technol.* B vol. **6**, p. 1416, 1988.

[36] P. Moriarty, B. Murphy, L. Roberts, A. A. Cafolla, G. Hughes, L. Koenders, and P. Bailey, “Photoelectron core-level spectroscopy and scanning-tunneling-microscopy study of the sulfur-treated GaAs(100) surface,” *Phys. Rev.* B vol. **50**, p. 14237, 1994.

[37] Y. Dong, X. M. Ding, X. Y. Hou, Y. Li, and X. B. Li, “Sulfur passivation of GaAs metal-semiconductor field-effect transistor,” *Appl. Phys. Lett.* vol. **77**, p. 3839, 2000.

[38] H.-S. Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, and J. C. Lee, "Gate oxide scaling down in HfO_2–GaAs metal-oxide-semiconductor capacitor using germanium interfacial passivation layer," *Appl. Phys. Lett.* vol. **91**, p. 042904, 2007.

[39] S. I. Park, I. Ok, H.-S. Kim, F. Zhu, M. Zhang, J. H. Yum, Z. Han, and J. C. Lee, "Optimization of electrical characteristics of TiO_2-incorporated HfO_2 *n*-type doped gallium arsenide metal oxide semiconductor capacitor with silicon interface passivation layer," *Appl. Phys. Lett.* vol. **91**, p. 082908, 2007.

	As $2p_{3/2}$ & Ga $2p_{3/2}$				
	As-As/As_{tot}	As_2O_x/As_{tot}	Ga_2O_x/Ga_{tot}	As-S/As_{tot}	Ga-S/Ga_{tot}
HCl only	15.4 %	45.6 %	27.8 %	—	—
HCl+Sulf.(RT)	14.9 %	34.8 %	27.6 %	5.4 %	7.3 %
HCl+NH_4OH+Sulf.(RT)	12.8 %	28.1 %	23.5 %	3.5 %	11.7 %
HCl+NH_4OH+Sulf.(80°C)	12.3 %	22.9 %	23.2 %	2.6 %	12.5 %

Table. 4.1 Chemical ratios of As $2p_{3/2}$ and Ga $2p_{3/2}$ spectra for the cleaned GaAs surface after different WCPs.

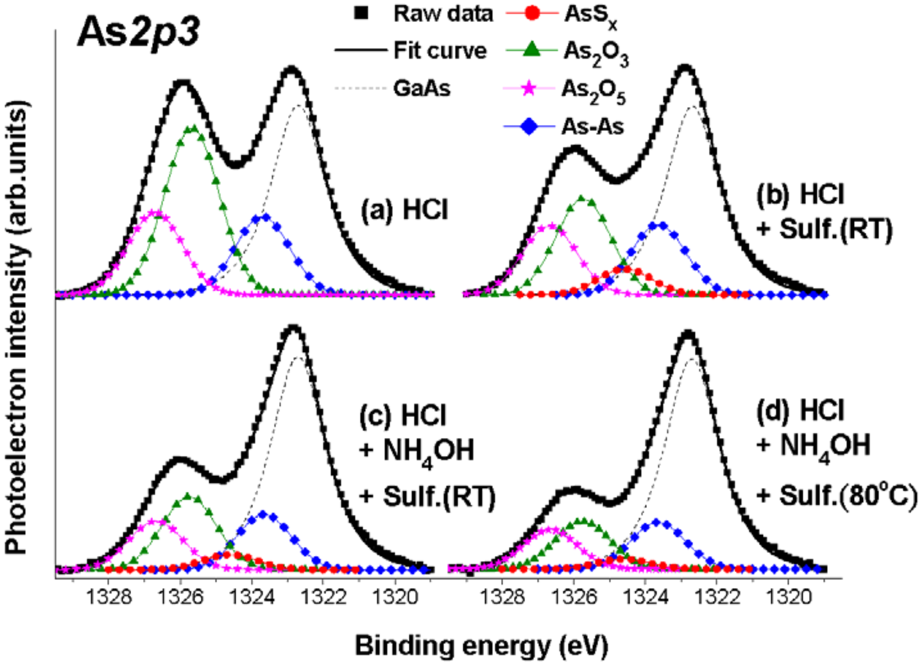


Fig. 4.1 As $2p_{3/2}$ XPS spectra of clean GaAs substrate subjected to four different WCPs. Five components were extracted: GaAs, AsS_x, As_2O_3, As_2O_5, and elemental As.

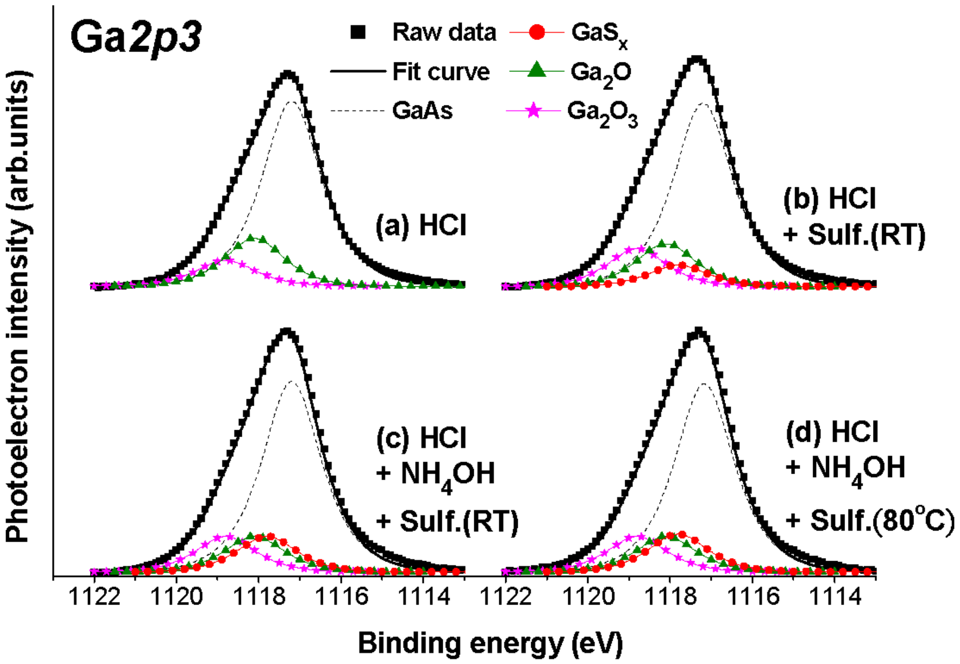


Fig. 4.2 Ga $2p_{3/2}$ XPS spectra of clean GaAs substrate subjected to four different WCPs. Four components were extracted: GaAs, GaS_x, Ga_2O, and Ga_2O_3.

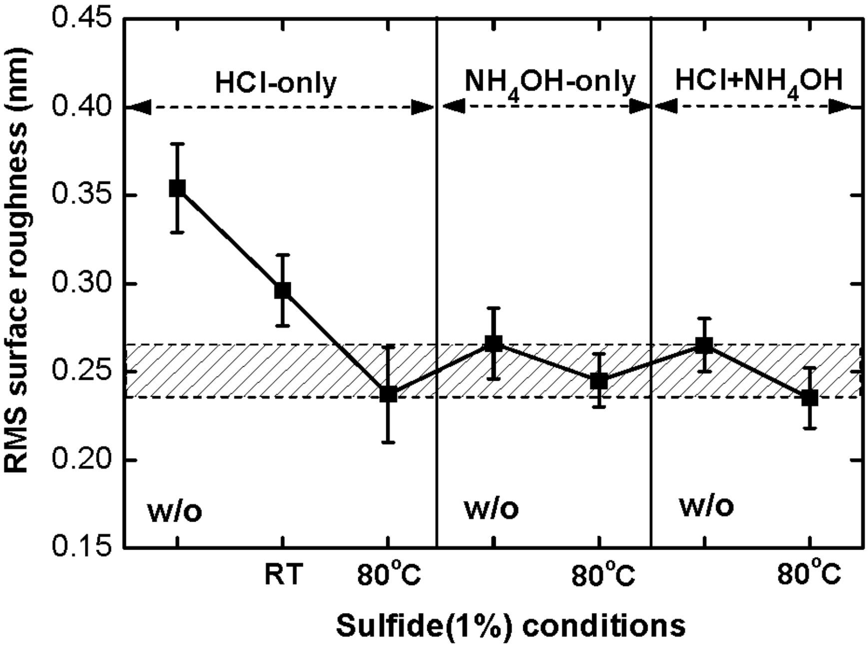


Fig. 4.3 RMS surface roughness of clean GaAs substrate subjected to different WCPs.

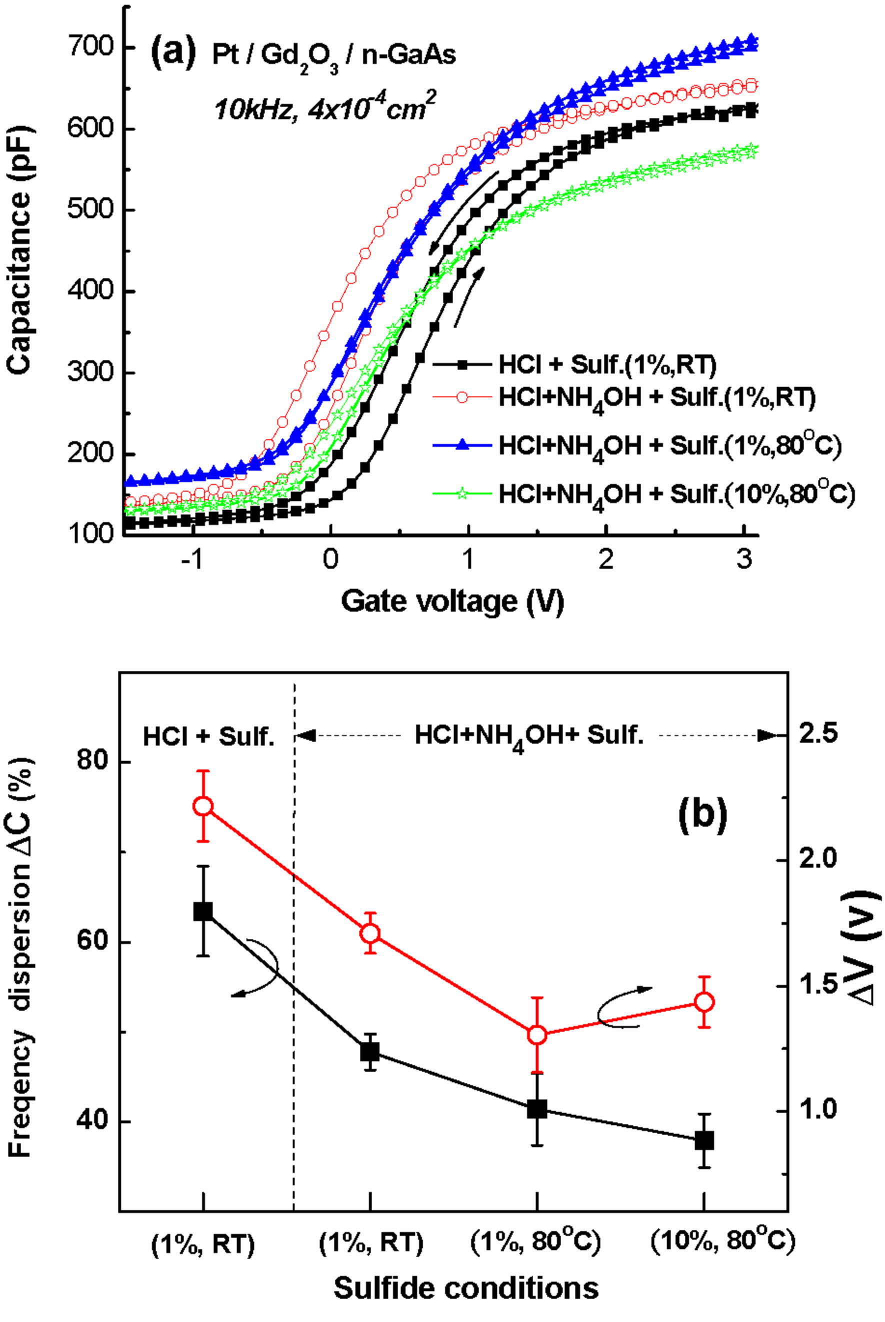


Fig. 4.4 (a) Bidirectional sweep (10 kHz) *C–V* curves; (b) the frequency response of △C and △V values for Pt/Gd_2O_3/n-GaAs capacitors with four kinds of WCPs.

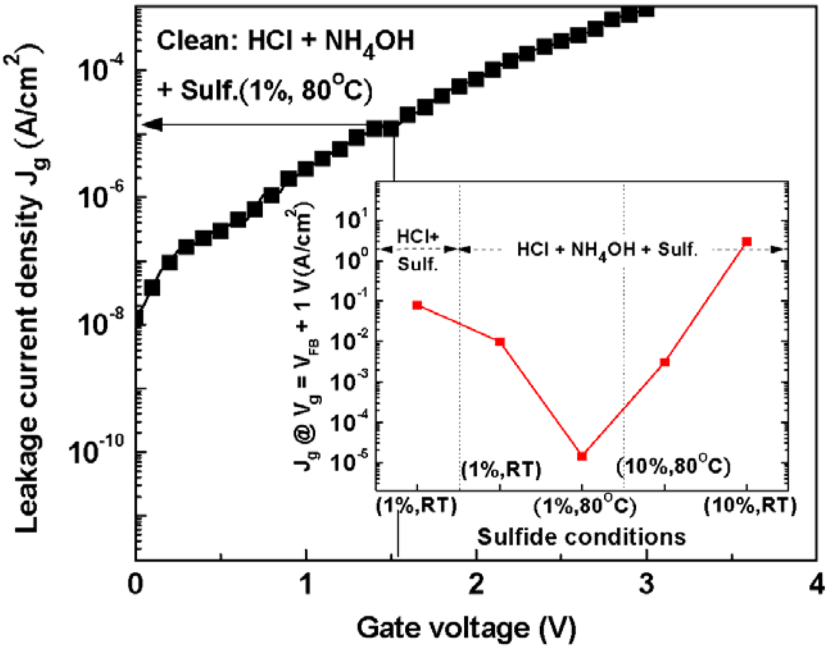


Fig. 4.5 The *I–V* characteristics of Pt/Gd_2O_3/n-GaAs capacitor with the WCP — HCl + NH_4OH + Sulfide (1%, 80 °C). The inset displays the plot of J_g @ V_g = (V_{FB} + 1) V versus the WCP conditions.

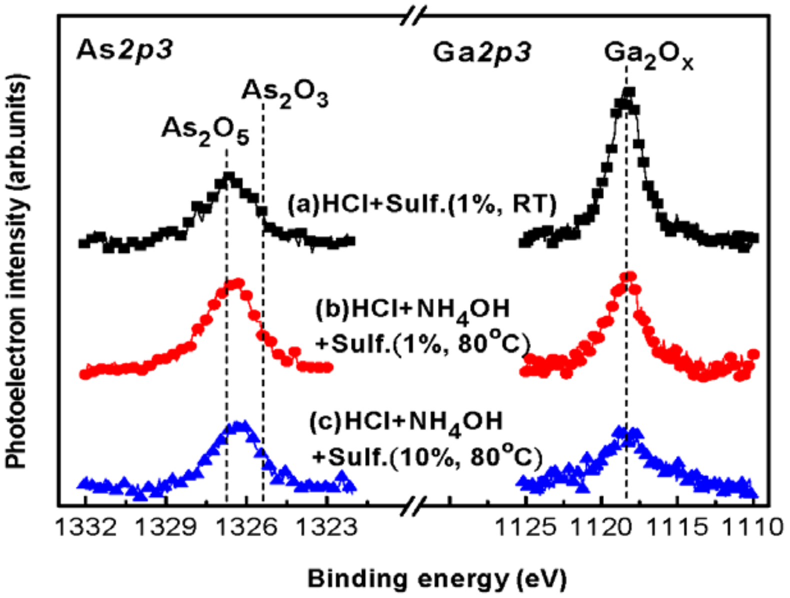


Fig. 4.6 As $2p_{3/2}$ and Ga $2p_{3/2}$ XPS spectra of the Pt/Gd_2O_3/GaAs structures investigated in Figs. 4.4 and 4.5.

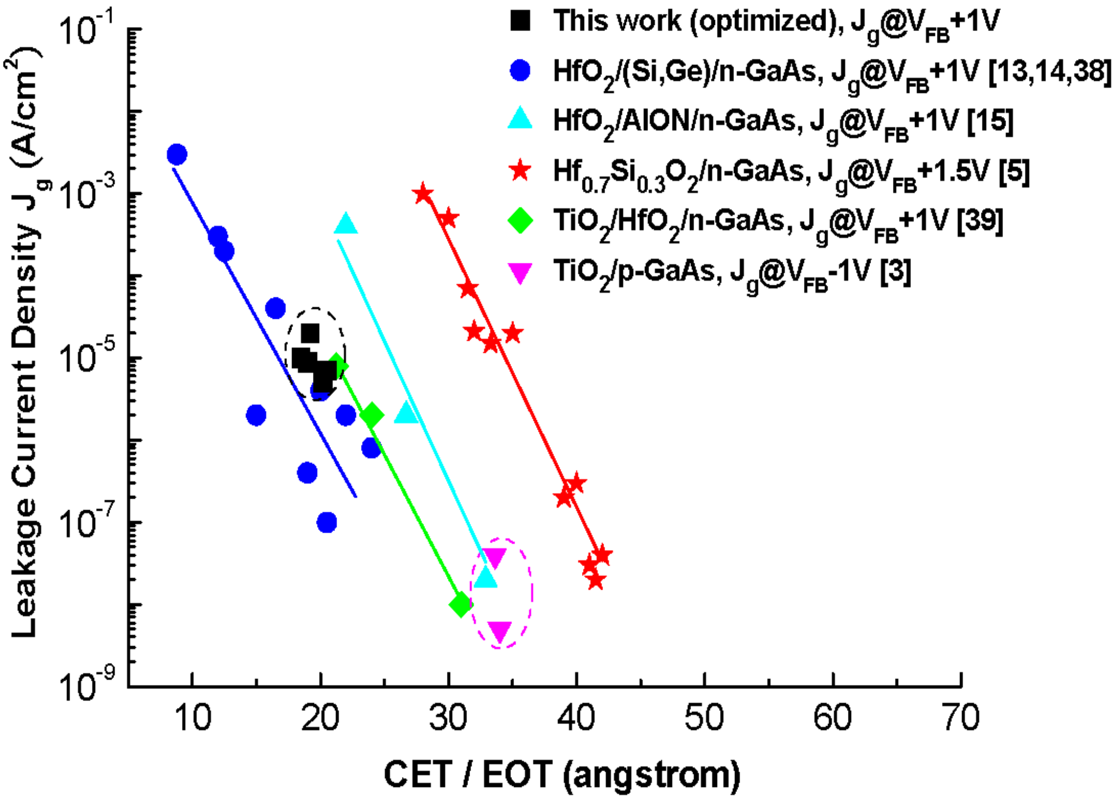


Fig. 4.7 Comparison of J_g versus CET or EOT characteristics for Pt/Gd$_2$O$_3$/n-GaAs capacitors with other's published data [3], [5], [13]-[15], [38], [39].

Chapter 5

Atomic-Layer-Deposited Al_2O_3 Dielectric Films on GaAs Substrates

5.1 Introduction

Presently, GaAs materials are used widely in such applications as optoelectronic devices, photodiodes, high-electron-mobility transistors (HEMTs), and other high-frequency devices. In attempts to obtain superior performance rivaling or exceeding that of transistors on traditional Si-based substrates, various high-*k* gate dielectrics have been examined on high-mobility III–V substrates, especially GaAs- and InSb-based compound materials [1], [2]. Studies into competitive insulators on compound semiconductors and efficient passivation methods have been performed for more than four decades; the poor quality of the insulator–substrate interface has been the foremost obstacle hindering the realization of III–V metal oxide semiconductor (MOS) devices. In addition to SiO_2 and Si_3N_4 [3], atomic-layer-deposited (ALD) Al_2O_3 [4], $(Gd,Ga)_2O_3$ [5], and HfO_2 high-*k* dielectrics [6] are also potential candidates for use on GaAs substrates. Surface sulfide treatment and the use of ultra-thin Si or Ge interfacial passivation layers are both practical techniques for improving electrical characteristics. The passivation of GaAs surfaces with Na_2S or ammonium sulfide $[(NH_4)_2S]$ prior to deposition of the gate dielectric has been reviewed comprehensively [7], [8]; the improvement in the device performance depends strongly on the sulfide treatment procedure [9]. The *in situ* deposition of several Si or Ge monolayers on GaAs [10], [11] can reduce the interfacial state density to ca. 10^{10}–10^{11} cm^{-2} eV^{-1}; this passivation technique has received renewed interest in recent years [12].

Subsequent thermal annealing can further improve the quality of insulator films deposited on GaAs [13]. Meanwhile, during high-temperature processing it is important to inhibit the loss of As within the GaAs substrate and also suppress the formation and subsequent incorporation of native oxides; these processes lead directly to electrical deterioration in GaAs MOS capacitors [14]. The impact of rapid thermal annealing on the properties of various high-*k*/GaAs structures has been studied previously [15]; the gas used in the annealing process influences the thermochemical mechanism as well as the interfacial quality [16]. Nevertheless, correlations between these thermal reactions and the MOS performance have not been established in detail. In this session, we examined the material and electrical characteristics of ALD-Al_2O_3 thin films deposited on an $(NH_4)_2S$-treated GaAs surface and then monitored the impact of thermal annealing processing. The nature of the annealing environment also affected the electrical properties; this behavior could be interpreted by considering the latent thermodynamic mechanisms, which we identified from the physical analyses. Furthermore, in order to increase the effectiveness of sulfur passivation [17], different alcohols with a lower dielectric constant, e.g., C_4H_9OH, can be used as solvents, in which the improvement of surface quality has been evidenced by an increase in photoluminescence intensity [17], [18], lower surface band bending [19], and reduced surface barrier height [20] of GaAs substrates. Nevertheless, the effects of the alcoholic solutions of $(NH_4)_2S$ on the practical electrical characteristics are still rare. Consequently, we also investigated the effects of the $(NH_4)_2S$-C_4H_9OH chemical passivation on the interface and capacitor properties of the ALD-Al_2O_3/GaAs structure. Our experimental findings verified the replacement of H_2O with C_4H_9OH as sulfidizing solvent that assisted to obtain the better electrical performance.

5.2 Experimental Procedures

n-Type GaAs substrates having a doping concentration of ca. 1×10^{18} cm^{-3} (resistivity < 0.01 Ω·cm) were first rinsed in acetone (ACE) and deionized (DI) water for 1 and 5 min, respectively. Subsequently, dilute HCl solution (HCl/DI water, 1:10) was used to etch the surface native oxides. After wet chemical cleaning, the samples were dipped into aqueous ammonium sulfide solution [$(NH_4)_2S$/DI water, 1:50] with different immersion durations, e.g., 30 s or 30 min, to passivate the GaAs surfaces prior to deposition of the dielectric. The Al_2O_3 films were deposited in ALD system at substrate temperatures of 100 and 300°C. Trimethylaluminum [$Al(CH_3)_3$] and H_2O were chosen as the metal source and oxidant, respectively; they were pulsed alternately into the reactor for 1 s per pulse, separated by a N_2 purge of 10 s to remove redundant reactants. The deposition rate was ca. 1.0–1.1 Å s^{-1}. For comparison, the as-deposited Al_2O_3 dielectric films were subjected to post-deposition annealing (PDA) at 600 °C in either a N_2 or O_2 ambient. The RTA system was purged cyclically by pumping down to 25 torr and refilling the feed gas; the chamber pressure was then maintained at 1 atm during annealing after flushing the gas. The top Pt gate electrode was formed via shadow mask sputtering; thermal evaporation of Al formed the backside contact; the capacitance area of the formed Pt was ca. 4×10^{-4} cm^2, measured using an optical microscope. In addition, post-metallization annealing (PMA) was performed at 400 °C for one sample to evaluate the thermal stability of the fabricated Pt/Al_2O_3/GaAs structures. On the other hand, for examining effects of the solvent used in GaAs sulfidization, we also applied a series of ammonium sulfide treatments, as listed in **Table 5.1**. Here, two kinds of solvents, DI water and C_4H_9OH, were used to dilute the $(NH_4)_2S$ solution, in which the treated temperatures were set at room temperature (RT) and 60 °C, respectively, and the soak time was kept at 1 min.

The surface morphology of GaAs after the DI water rinse was characterized by the atomic force microscopy (AFM). High-resolution transmission electron microscopy (HRTEM) was used to characterize the variations in thickness of the deposited Al_2O_3 film after processing under the two different annealing environments. The respective structural composition, sulfur bonding configuration, and oxide removal efficiency were examined using the secondary ion mass spectrometry (SIMS) and x-ray photoelectron spectroscopy (XPS) with an Al Kα radiation source (1486.6 eV). To extract each chemical component from the photoemission spectra, a rigorous fitting process was adopted: after the peak positions had been ascertained, they were applied to reconstruct the original spectra and then to extract each respective contribution. During the deconvolution of the spectra, the peak areas were varied while maintaining the full width at half maximum and the ratio of the Gaussian to Lorentzian distribution constant. In addition, we measured the frequency-dependent capacitance–voltage (C–V) and current–voltage (I–V) characteristics using an HP4284 LCR meter and a Keithley 4200 system, respectively, to determine the quality of the Al_2O_3–GaAs interface. The interface state density (D_{it}) was calculated using the conductance method [21] based on the measured conductance–voltage (G–V) curves.

5.3 Temperature-Dependent Growth of ALD-Al_2O_3/GaAs Films

The frequency-dependent and bidirectional C–V curves of Pt/100°C-Al_2O_3/n-GaAs MOS capacitors are shown in **Figs. 5.1(a)** and **5.1(b)**, respectively. As seen, the as-deposited sample apparently showed C–V stretch-out behavior accompanying with the lower oxide capacitance; the clockwise hysteresis width was also presented. Even though annealing the sample at 600 °C in an O_2 ambient exhibited the higher accumulation capacitance, it also caused a large flat-band voltage (V_{FB}) shift with respect to the measured frequency, implying the generation of slow states at and/or close to the interface. As the $(NH_4)_2S$ treatment was further employed, the highest accumulation capacitance with steep C–V slope presented; meanwhile, the smaller hysteresis behavior was also found. We suggested that the sulfide passivation can improve the interface quality between Al_2O_3 high-k dielectric and GaAs substrate due to the native oxide suppression and enhanced thermal stability.

Figure 5.2 shows the corresponding I–V characteristics. It was noticed that high-temperature PDA obviously increased the gate leakage current (J_g) by more than two orders, at gate bias V_g above 2 V. From XPS analysis (not shown), we found that a small amount of As metal and both native oxides have been incorporated into bulk Al_2O_3 during annealing; the resultant contamination are believed to be responsible for a huge increase in J_g.

The quality of Al_2O_3 deposited at 300 °C on GaAs are examined in **Fig. 5.3(a)**; the inset shows the Weibull plot of J_g distribution at V_g = 2V. The $(NH_4)_2S$-treated sample relative to the HCl-last sample exhibited the higher oxide capacitance and smaller C–V frequency dispersion, which is similar to the examination in ALD-Al_2O_3 at 100 °C. The corresponding J_g seemed to be slightly lower than that in the sample without sulfide process, but, with the broad distribution in the Weibull plot, reflecting the fact that the distribution of sulfur bonding is an important role in gate leakage performance. Besides, as illustrated in **Fig. 5.3(b)**, all 300°C-Al_2O_3 samples were found to show the better J_g performance, where the nearly four orders of magnitude reduction in J_g at the capacitance-equivalent-thickness (CET) of 40 Å, with respect to the 100°C-Al_2O_3 samples.

5.4 Effect of Interfacial Sulfidization

5.4.1 Surface Chemistry of Sulfidized GaAs Surface

Figure 5.4 displays As $2p_{3/2}$ and Ga $2p_{3/2}$ photoemission spectra of the as-deposited Al_2O_3/GaAs bilayer with and without $(NH_4)_2S$ interfacial passivation; the thickness of the overlying Al_2O_3 thin film after 60 deposition cycles was ca. 63 (±3) Å. Thus, we employed the high surface sensitivity of this technique (maximum sampling depths of ca. 31 and ca. 55 Å for the As $2p_{3/2}$ and Ga $2p_{3/2}$ spectra, respectively) to characterize the content of

GaAs-related chemical species diffused into the high-*k* layer [22]. In accordance with the Ga $2p_{3/2}$, As $2p_{3/2}$, Al 2*p*, and O 1*s* core levels, we evaluated the average concentration of existed GaAs oxides and the stoichiometric ratio of O to Al, based on the mixture of Ga_2O_x and As_2O_x in the Al_2O_x bulk layer. As indicated in **Table 5.2**, the concentrations of both the Ga and As oxide species were much less than 0.5%. So that, we infer that both kinds of native oxides, As_2O_x and Ga_2O_x, in the forms of their stoichiometric oxides and suboxides more likely formed close to oxide-substrate interface. But, we cannot rule out the possibility that a tiny amount of As oxides diffused into the Al_2O_3 high-*k* film during deposition at substrate temperature up to 300 ^oC. Besides, the formation of these oxides, in particular the gallium oxides, could be suppressed by forming Ga- and As-related sulfur bonds at the dielectric interface. Interestingly, it appears that, the stoichiometry of Al_2O_x in the deposited film may correlate with the degree of GaAs oxides formed nearby the interface. Provided that Al_2O_3 was directly deposited on GaAs, the O/Al chemical ratio was as high as 1.75, i.e., an oxygen-enriched Al_2O_x dielectric film; long-term sulfide immersion could return this value to a nearly ideal stoichiometric ratio of 1.57 as a result of the enhanced surface stability.

The As 3*d* and Ga 3*d* core level spectra in **Fig. 5.5** allowed us to characterize the interfacial composition close to the substrate, because the inelastic mean free paths (IMFPs) were above 25 Å. We found that an amorphous As layer was present on the bulk GaAs; moreover, its content could be decreased upon chemical treatment with $(NH_4)_2S$. We suggest that these interfacial As atoms could have arisen through two mechanisms: (a) the dilute HCl solution used to clean the GaAs might have led to the formation of elemental As atoms covering the GaAs surface [23]; (b) thermal transformation of the surface As oxides might have occurred through reactions with the GaAs substrate [24]. The As suboxides can desorb at ca. 150–200 °C, and the As_2O_x species having higher oxidization states ($x = 3$ or 5) will sublime at temperatures of ca. 250–300 °C [24]-[26]. This ready thermal desorption indicates that mechanism (b) probably occurred during ALD deposition at 300 °C. We also calculated the relative contributions of elemental As and the As_2O_x and Ga_2O_x components in the respective As 3*d* and Ga 3*d* spectra (**Table 5.3**). Evidently, the sulfur-terminated GaAs surface successfully decreased the content of the As-rich layer and its chemical oxides.

The O 2*s* photoelectron signal observed at 23.4 eV, which mostly originated from the overlying Al_2O_3 thin film, overlapped with the Ga 3*d* core level. The content of Ga–O oxide species existing near the Al_2O_3–GaAs interface decreased after sulfidization. According to the literature [27], [28], the Ga–S chemical bond, relative to the As–S bond, has the higher bond strength up to 400 °C, thereby effectively restraining the growth of Ga_2O_x. These sulfur species are not readily identified in a S 2*p* spectrum because of partial overlap with the signal of bulk Ga 3*s*, but a small number of GaS_x bonds were detectable at a peak position of ca. 162.2 eV (not shown here) [29]. Along with the high stabilization of the Ga_2O_3 stoichiometric oxide, these features taken together reasonably explain the absence of the Ga–O signal in the Ga $2p_{3/2}$ spectra after surface sulfidization. In view of the improved behavior, we believe that the sulfur-terminated GaAs substrate enhanced the deposition quality and dielectric stoichiometry of the ALD-Al_2O_3 thin films.

5.4.2 Capacitor and Gate Leakage Characteristics

Figure 5.6 displays the *C*–*V* and *I*–*V* characteristics of the various samples. The $(NH_4)_2S$-treated sample displayed a higher oxide capacitance accompanying a decreased *C*–*V* frequency dispersion, relative to those of the untreated sample; a reduction in hysteresis width and J_g were also achieved [**Figs. 5.6(b)** and **5.6(c)**]. These results are indicative of the abatement of the Fermi level pinning effect in the capacitor properties; in other words, modulation of the surface potential and carrier manipulation was enhanced. As stated above, sulfide pretreatment suppressed the amounts of unstable As–As and As–O species, which are believed to be a source of high-density interfacial traps. The value of D_{it} close to the midgap was estimated to be ca. 1×10^{13} cm^{-2} eV^{-1} for the untreated sample; subsequent sulfide passivation reduced this value to ca. 7×10^{12} cm^{-2} eV^{-1}. Previous studies have found that sulfidized GaAs improved the MOS characteristics as a result of eliminating As-related surface defects [30], [31]. The subsequent PMA at 400 °C, however, not only caused a larger frequency dispersion and broadened hysteresis width at the depletion region but also increased the value of J_g by nearly four orders of magnitude. The underlying mechanisms responsible for the PMA-induced gate leakage degradation are discussed below.

5.5 Effect of Postdeposition Annealing Ambient

5.5.1 Structure Analysis

To explore the degradation of the electrical characteristics that were due to N_2 annealing, we first compared HRTEM images of the Pt/Al_2O_3 bilayers deposited on the sulfide-treated GaAs after post-deposition annealing under N_2 and O_2 atmospheres [**Figs. 5.7(a)–(c)**]. We did not observe the existence of the interfacial layer (IL); the deposited Al_2O_3 also exhibited an amorphous phase after PDA at 600 °C. Most importantly, the O_2-processed sample revealed a bright Al_2O_3 thin film and an interface that was indistinct with respect to the upper Pt metal and GaAs substrate, whereas the N_2-processed sample revealed a relatively dark, thick Al_2O_3 film possessing a sharp interface. We believe that the O_2 used as the feed gas was effective in densifying the ALD-Al_2O_3 gate dielectric and repairing the inner bond imperfections, e.g., dangling bonds and oxygen vacancies. Meanwhile, a great degree of inter-diffusion occurred at the dielectric–substrate interface, which can be attributed to the relatively high probability of oxygen diffusing into the GaAs substrate [32], resulting in the blurred interface for the O_2-processed system.

5.5.2 Capacitor and Gate Leakage Characteristics

Next we examined the impact of thermal annealing on the multi-frequency *C*–*V* curves, as illustrated in **Figs. 5.8(a)** and **5.8(b)**; each inset displays the *C*–*V* hysteresis width measured at 100 kHz. For both deposition conditions, the O_2-annealed samples exhibited higher oxide capacitance and decreased hysteresis phenomena with respect to the N_2-annealed samples; we attribute this finding mainly to the highly improved dielectric quality and the thinner film thickness. We also found that electron trapping was responsible for the clockwise hysteresis loop [16], where the hysteresis widths after O_2 and N_2 PDA were ca. 0.3 and ca. 0.4 V, respectively. This situation reflected the smaller density of slow traps that resided around the dielectric interface after performing O_2 annealing. In contrast, the *I*–*V* characteristics in **Fig. 5.9** are remarkably different: N_2 PDA severely deteriorated the J_g characteristics, as in the PMA case in **Fig. 5.6(c)**, whereas the O_2 ambient alleviated the degradation phenomenon. From a plot of the J_g (at V_g = 2 V) versus the CET, the value of J_g at a CET of 40 Å was reduced by nearly three orders of magnitude after replacing N_2 with O_2 as the annealing gas (inset to **Fig. 5.9**). We ascribe the dramatically increased value of J_g to one or both of the following mechanisms: (a) the elemental As overlayer that acted as a metallic contamination source nearby the oxide–bulk interface increased the surface recombination velocity, with fast diffusion resulting in poor insulator properties; (b) high-temperature processing caused the generation of surface pits or holes within the GaAs substrate, thus increasing the surface roughness [24]. Excess As atoms might have been produced during either the decomposition of GaAs itself or the chemical transformation of oxide species through reactions with the bulk GaAs; meanwhile, the inhomogeneous voids formed also deteriorated the surface morphology. We expected a relatively low density of formed voids after annealing because of the coverage of an amorphous Al_2O_3 film on GaAs substrate. Thus, we inferred that the N_2-annealed Al_2O_3/GaAs structures suffered from relatively severe desorption and transformation of the As_2O_x and Ga_2O_x mixed oxides; in addition, more As atoms were segregated at the interface. In light of this behavior, we would expect degradation of the gate leakage characteristics to be accelerated after N_2 annealing. To support our hypothesis, we performed a dielectric reliability test (**Fig. 5.10**) with regard to this degradation behavior. The Pt/ALD-Al_2O_3/GaAs capacitors were stressed under the constant V_g of 5 V and a constant oxide electrical field (E_{ox}) of 8.5 MV·cm^{-1}. Irrespective of the dielectric stress method employed, we found that the sulfidization procedure improved the dielectric reliability. The sulfidized sample that underwent subsequent O_2 annealing possessed superior dielectric reliability, relative to that which underwent N_2 annealing, in accordance with the slower rate of increase in the value of J_g. These findings indicate that the annealing environment is a crucial factor in determining the electrical performance of high-*k*/GaAs structures. The degraded quality of the N_2-annealed sample with respect to the O_2-annealed one shall be closely linked to severe As_2O_x desorption and the extent is not so drastic to cause the increase of the interface roughness. This is because a relatively low temperature of 600 °C annealing was employed as compared to the previous observation reported by M. Passlack *et al.* that the Ga_2O_3/GaAs interface is very smooth after annealing below 700 °C and severely degrades with 780 °C annealing [15].

5.5.3 Thermochemical Reactions and Composition Analysis

Table 5.4 provides a comprehensive list of the accessible solid state reactions involved in the Ga–As–O phase diagram [33], [34] to aid us in determining the transformation phenomena that occurred during annealing. The critical temperature T_c is defined as the temperature at which the reaction becomes thermodynamically favorable, i.e., where the Gibbs free energy of formation ($\triangle G_f$) is less than zero; we obtained the values of T_c from experimental results reported in the literatures [24]-[26], [37]. We also calculated the value of $\triangle G_f$ for each of these stoichiometric equations [35], [36]. If $\triangle G_f$ is greater than zero, the chemical reaction will not proceed; for example, the mechanisms associated with Ga_2O formation are inhibited at RT, but an increase in temperature enhances the driving kinetics of the reaction. Because various kinds of GaAs chemical products desorb and/or transform during high-temperature processing, we performed XPS and SIMS analyses to better characterize the electrical differences.

The As 2$p_{3/2}$ and Ga 2$p_{3/2}$ spectra in **Fig. 5.11** indicate that the diffusion of GaAs chemical species was enhanced within the Al_2O_3 gate dielectric after thermal annealing; we extracted the contribution of each chemical component. In the following discussion we denote the N_2-annealed capacitor that underwent sulfide treatment as the “SN-sample” and denote the O_2-annealed capacitors without and with sulfide treatment as the “O-sample” and “SO-sample,” respectively. The As 2$p_{3/2}$ spectra revealed an increased incorporation of arsenic oxides, including As_2O_5, As_2O_3, and AsO_x, relative to their content in the as-deposited Al_2O_3 film. We observed similar behavior in the Ga 2$p_{3/2}$ spectra: both the Ga_2O_3 and GaO_x oxides were slightly enriched after annealing, with the SN-sample having relative higher concentrations. From the atomic quantification, **Table 5.5** indicates that the amount of diffused arsenic oxides was larger, by about one order of magnitude, than that of the gallium oxides in the annealed Al_2O_3; this behavior is similar to that of the oxide layer formed during thermal oxidation of a GaAs surface [39]. In addition, only the O-sample after annealing at 600 °C presented an oxygen-enriched Al_2O_x film; we attribute this finding to a portion of the sulfur atoms filling a number of vacancies inside the high-*k* gate dielectric, thereby avoiding over-oxidization in the sulfidized samples during PDA.

Table 5.4 (part A) indicates that the value of T_c for the desorption of arsenic oxides ranges from 150 to 350 °C; these transformations are thermodynamically favorable at RT. In contrast, the higher thermal stability of the Ga-based oxide compounds inhibits the reduction of nonvolatile Ga_2O_3 into Ga_2O (**Table 5.4, part D**); consequently, its value of T_c is higher (400–600 °C). Because of the low sublimation point of the oxides of arsenic, volatile As_2O_3 oxide first reacts with either the GaAs substrate or interstitial Ga atoms to form a Ga_2O_3 layer and segregated As close to the interface. It is possible that the highly stable Ga_2O_3 oxide also reacts with the substrate again to produce non-stoichiometric Ga_2O along with the As co-products under high-temperature annealing at 600 °C. Most of these As species—in the form of elemental As and/or gaseous As_4—are oxidized during the desorption event and then trapped inside the dielectric film. Note that Ga_2O_3 formation can arise through several transformation paths; for example: $As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4As$ or As_4. Because the O_2 environment provides additional reaction paths (**Table 5.4, part B**), the content of chemical products is likely to be somewhat different to that in the N_2 annealing case. This situation can be explained in terms of the chemical reaction principle that kinetics naturally drive several oxidation mechanisms—e.g., the oxidation of GaAs, As, and As_4—resulting in a deceleration of the rate of transformation of As_2O_x compounds as well as the generation of As defects in the O_2 ambient [41]. In addition, even if molecular oxygen prefers to react with Ga atoms over As atoms, the As species will still have a higher probability of oxidation because they are more readily desorbed [42]. When the content of arsenic oxides increases in the upper area of the dielectric film they can act as a block, which in turn hinders the diffusion of oxygen into the dielectric–substrate region. These phenomena result in our observation of an enriched amount of As_2O_x with a low Ga_2O_x concentration for both the SO- and O-samples, a finding that is opposite to the behavior of the SN-sample. Another interesting phenomenon visible in the $2p_{3/2}$ spectra is that PDA under N_2 resulted in the formation of some metallic As, whereas some elemental Ga appeared after PDA under O_2. This finding provides direct evidence of the fast generation of As species in the N_2 ambient. On the other hand, as far as the source of these Ga atoms is concerned, we speculate that the oxidation of the Al_2O_3/GaAs interface and decomposition of the GaAs substrate are responsible for the supply of free Ga atoms [26], [41]. It should be pointed out that as regarding the reactions related to Al and these in-diffused Ga or As oxides, most possible reaction we presume is the reaction of Al_2O_3 with Ga_2O_3, due to the higher thermal stability relative to As_2O_3. However, in our study the highest RTA temperature is 600 °C, probably not enough to make Al react with Ga oxides [43]; these thermal processes are excluded here and still need further investigation.

Figure 5.12 presents the highly bulk-sensitive As 3*d* and Ga 3*d* photoemissions; **Table 5.6** provides the chemical bonding ratio of the contributed chemical components for convenient characterization. We observe that annealing at 600 °C further decreased the percentage of interfacial As presented in the overall As 3*d* spectra, with respect to that in the as-deposited Al_2O_3/GaAs structures (**Fig. 5.5**, **Table 5.3**). Even though the desorption event contributed to the formation of either As or As_4, most of the As atoms escaped into the atmosphere or were further oxidized into various oxidation states. A substantial amount of Ga_2O_x oxides was generated accordingly through chemical transformation. We also observed that the additional sulfide pretreatment of the SO-sample made it (relative to the O-sample) more highly resistant to the growth of these undesirable components. **Fig. 5.13** illustrates the respective SIMS depth profiles; the thickness of the Al_2O_3 thin film, which was deposited at 300 °C for 50 cycles, was ca. 50 (±3) Å after PDA at 600 °C. Of primary interest is the distribution of the As, Ga, and S species in the overlying Al_2O_3 high-*k* film. We found that a higher concentration of As was presented around the bottom of the Al_2O_3 bulk film, coinciding with the diffusion of As-enriched oxides and the interfacial arsenic layer. Another feature is the observation of a small tails of Ga species at a depth of ca. 10–30 Å for the SO- and O-samples only, probably related to a trace of out-diffused Ga elements, the detailed mechanism of which requires further investigation. On the other hand, the S signal detected in the O-sample was due to mass interference of molecular oxygen in the SIMS analysis of the oxide film. We believe that the S atoms did exist even after high-temperature processing, as determined after subtracting the induced signal of the mass interference used as the baseline background. The corresponding XPS analysis in Table IV indicates that the sulfidized samples were relatively less oxygen-excessive (Al/O ratio = 1.78) with respect to the HCl-last sample (Al/O ratio = 2.2). Meanwhile, the smaller *C*–*V* hysteresis width after sulfidization is indicative of less charge trapping in the Al_2O_3 dielectric (not shown here). Thus, we conclude that most of the S atoms diffused into the high-*k* film and probably occupied either the vacancy sites or pre-existing defects; as a result, this process facilitated the improvement in the quality of the Al_2O_3 gate dielectrics as well as their electrical performance.

5.6 Effect of $(NH_4)_2S$ Sulfidization Solvent

5.6.1 Surface Chemistry and Morphology Analysis

Figure 5.14 shows the Ga $2p_{3/2}$ and As $2p_{3/2}$ photoemission spectra of GaAs substrates subjected to the $(NH_4)_2S$-C_4H_9OH sulfidizing treatments with different concentrations and temperatures, respectively. As seen, the deconvoluted peaks of Ga-S, Ga_2O, and Ga_2O_3 were observed in Ga $2p_{3/2}$ spectra at the respective binding energy of 0.65, 1.0, and 1.6 eV above the GaAs substrate. While the As $2p_{3/2}$ spectra also presented the signals of As-As, As-S, As_2O_3, and As_2O_5 at the respective binding energy of 1.0, 1.7, 2.95, and 3.95 eV above the GaAs substrate. **Table 5.1** summarizes the signal ratios of these surface chemical species on GaAs. It was found that the NH_4OH rinse decreased the content of As-As species and native oxides obviously, as compared to the results presented in the DIW-rinsed sample. Subsequent immersion of $(NH_4)_2S$-based solution can make the amount of As-related species reduce continuously. Here, we are of more interest in the surface modification of GaAs by replacing H_2O with C_4H_9OH as sulfidizing solvent; evidently, not only the removal efficiency of AsO_x species accelerated but also more sulfur ions bonded to GaAs with either raising the concentration to 10% and/or the temperature to 60 °C. These observations can be attributed to the stronger electrostatic interaction between the sulfur ion and the GaAs surface by decreasing the solvent dielectric constant ε from 80.1 (H_2O) to 12.5 (C_4H_9OH). Even if V. N. Bessolov *et al.* [17] brought up that the change of the alcoholic solvents in $(NH_4)_2S$ solution, relative to that in Na_2S solution, had a minor enhancement on the sulfur passivation on GaAs, a higher degree of the sulfur coverage was actually observed from XPS analysis as a result of the increased chemical activity in sulfidized solution. As compared to the results in the RT case, a remarkable feature was the amount of As-As species that increased slightly from 8.4% to 10.9% at higher temperature of 60 °C. Such an increase in the elemental As on GaAs surface did lead to severe leakage degradation of the ALD-Al_2O_3 deposited film (not shown here). In general, the resultant suppression of GaAs defects is able to boost the interface and film qualities of the deposited insulator. As the AFM images displayed in **Fig. 5.15**, the flatter morphology of GaAs surface was observed with the help of the sulfidized immersion, giving the evidence of the interface improvement. The root-mean-square (RMS) roughness of NH_4OH-cleaned GaAs surface was ca. 0.28 nm and then reduced to ca. 0.22 nm by rinsing in $(NH_4)_2S$-C_4H_9OH solution (10%) at 60 °C.

Figure 5.16 presents the TEM image of as-deposited Pt/ALD-Al_2O_3/GaAs capacitor, in which the thickness of Al_2O_3 film is ca. 62 Å for 60 deposition cycles. We did not observe the existence of an obvious IL between the Al_2O_3 and the GaAs, which should be correlated to the self-cleaning of GaAs native oxides at the initial stage of ALD deposition [44], [45]. Such behavior of the bonding replacement between ALD metal precursor and $As_2O_x(Ga_2O_x)$ has been also manifested in the recent studies of ALD-HfO_2/GaAs growth [46], [47].

5.6.2 Capacitor and Gate Leakage Characteristics

Furthermore, the impact of the sulfidizing solvent and PDA on the capacitor characteristics was examined. As the frequency–dependent *C-V* curves shown in **Figs. 5.17(a)** and **5.17(b)**, the alcoholic-$(NH_4)_2S$ solution increased the value of accumulation capacitance, and subsequent O_2 PDA improved the *C-V* dispersion further. For the NH_4OH-cleaned GaAs capacitor, the capacitance-equivalent-thickness (CET) extracted at 1 kHz was ca. 3.78 nm and its values were reduced to ca. 3.54 and 3.75 nm for the sulfidized GaAs samples before and after 600 °C thermal annealing, respectively. We qualitatively inspected the improvement of capacitor characteristics through variations of the $\triangle$C and $\triangle$V that were defined as follows:

$$\triangle C(@V_g = 4\ \mathrm{V}) = 1 - C_{acc}(@100\ \mathrm{kHz}) / C_{acc}(@1\ \mathrm{kHz}) \tag{5.1}$$

$$\triangle V(@C_{FB}) = V_g(@1\ \mathrm{kHz}) - V_g(@100\ \mathrm{kHz}), \tag{5.2}$$

where $\triangle$C is the deviation of the accumulation capacitance measured at 1-kHz and 100-kHz for the V_g of 4 V, while $\triangle$V is the voltage difference between 1-kHz and 100-kHz *C-V* curves achieving the value of the flatband capacitance (C_{FB}). As the results plotted in **Fig. 5.17(c)**, both values of $\triangle$C and $\triangle$V showed the decrement with the C_4H_9OH solvent used, an increased sulfidizing concentration, and in particular the implement of post thermal annealing. The lowest values of $\triangle$C and $\triangle$V obtained were 13.6% and 0.69 V, respectively, by performing 10% $(NH_4)_2S$-C_4H_9OH interfacial treatment with 600 °C O_2 PDA; a corresponding D_{it} value of 5×10^{12} cm^{-2}eV^{-1} was evaluated.

Figure 5.18(a) displays the J_g characteristics and the results indicate that the sulfur passivation is effective to suppress the dielectric leakage current and the alcoholic-$(NH_4)_2S$ solution can boost the thermal stability further. The treatment of 10% $(NH_4)_2S$-C_4H_9OH apparently led to the better leakage performance that the respective values of J_g at $V_g = (V_{FB} + 1)$ V were ca. 7×10^{-7} and 1×10^{-5} A/cm^2 before and after 600 °C PDA in O_2 ambient. By plotting the J_g versus CET, as shown in **Fig. 5.18(b)**, the fabricated ALD-Al_2O_3/GaAs capacitors exhibited the comparable J_g characteristics to the previous studies of the sputtered $Hf_xSi_{1-x}O$/n-GaAs [2] and HfO_xN_y/p-GaAs [48] structures, respectively. However, the capacitor performance was inferior than the results of ALD-Al_2O_3 [49], -HfAlO [50], -HfO_2 [6] films and metal-organic chemical vapor deposition HfO_2 film [51] on GaAs substrates from other research groups, indicating that the film quality of the deposited Al_2O_3 itself still needs the growth optimization.

5.7 Conclusions

In Chapter 5, the ALD-Al_2O_3 films deposited on GaAs substrate at 300°C relative to that at 100°C showed the nearly four orders of magnitude reduction in gate leakage current at the capacitance-equivalent-thickness of 40 Å. Next, we examined the interfacial chemistry of the Al_2O_3/GaAs and the impact of sulfidization and thermal annealing on the properties of the resultant capacitor. It was observed that sulfidized passivation actually improved the effect of the E_F pinning on the electrical characteristics, thereby providing a higher oxide capacitance, smaller frequency dispersion, and reduced surface states, as well as decreased interfacial charge trapping and gate leakage current. Photoemission analysis indicated that the $(NH_4)_2S$-treated GaAs improved the quality of the as-deposited Al_2O_3 thin film and preserved the stoichiometry of the dielectric during subsequent high-temperature annealing. This behavior was closely correlated to the diminution of GaAs native oxides and elemental-As defects and their unwanted diffusion. In addition, thermal processing under an O_2 atmosphere, relative to that under N_2, decreased the thickness of the Al_2O_3 gate dielectric and relieved the J_g degradation induced by metallic arsenic; as a result, superior dielectric reliability was attained. We discussed the underlying thermochemical reactions that account for these experimental observations. Furthermore, it was also found that degreasing GaAs into $(NH_4)_2S$ solution with C_4H_9OH used as solvent clearly reduced the amount of As-As and AsO_x surface species and formed more sulfur bondings to GaAs; the flatter surface morphology was also characterized. A higher electrical improvement was indeed presented by replacing H_2O with C_4H_9OH as sulfidizing solvent, again thanks to the elimination of more As-related defects as well as the higher sulfur coverage on GaAs. It is believed that the $(NH_4)_2S$-C_4H_9OH treatment can be adopted on the InGaAs/InSb substrates or integrates with other passivation methods to provide the better surface quality for realizing high-performance high-*k*/III-V devices.

References (Chapter 5)

[1] S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, “85nm gate length enhancement and depletion mode InSb quantum well transistors for ultra high speed and very low power digital logic applications,” *Tech. Dig. Int. Electron Device Meet.*, p. 783, 2005.

[2] M. H. Zhang, I. J. Ok, H. S. Kim, F. Zhu, T. Lee, G. Thareja, L. Yu, and J. C. Lee, “Characteristics of sputtered $Hf_{1-x}Si_xO_2$/Si/GaAs gate stacks,” *Appl. Phys. Lett.* vol. **89**, p. 042902, 2006.

[3] J. Reed, Z. Fan, G. B. Gao, A. Botchkarev, and H. Morkoc, “GaAs metal insulator semiconductor capacitors and high transconductance metal insulator semiconductor field effect transistors,” *Appl. Phys. Lett.* vol. **64**, p. 2706, 1994.

[4] H.-L. Lu, L. Sun, S.-J. Ding, M. Xu, D. W. Zhang, and L.-K. Wang, “Characterization of atomic-layer-deposited Al_2O_3/GaAs interface improved by NH_3 plasma pretreatment,” *Appl. Phys. Lett.* vol. **89**, p. 152910, 2006.

[5] C. P. Chen, Y. J. Lee, Y. C. Chang, Z. K. Yang, M. Hong, J. Kwo, H. Y. Lee, and T. S. Lay, “Structural and electrical characteristics of $Ga_2O_3(Gd_2O_3)$/GaAs under high temperature annealing,” *J. Appl. Phys.* vol. **100**, p. 104502, 2006.

[6] M. Zhu, C.-H. Tung, Y.-C. Yeo, “ Aluminum oxynitride interfacial passivation layer for high-permittivity gate dielectric stack on gallium arsenide,” *Appl. Phys. Lett.* vol. **89**, p. 202903, 2006.

[7] S. Arabasz, E. Bergignat, G. Hollinger, and J. Szuber, “ XPS study of surface chemistry of epiready GaAs(100) surface after $(NH_4)_2S_x$ passivation,” *Vacuum* vol. **80**, p. 888, 2006.

[8] V. N. Bessolov, E. V. Konenkova, and M. V. Lebedev, “ Solvent effect on the properties of sulfur passivated GaAs,” *J. Vac. Sci. Technol. B* vol. **14**, p. 2761, 1996.

[9] Y. Dong, X. M. Ding, X. Y. Hou, Y. Li, and X. B. Li, “Sulfur passivation of GaAs

metal-semiconductor field-effect transistor," *Appl. Phys. Lett*. vol. **77**, p. 3839, 2000.

[10] D. S. L. Mui, D. Biswas, J. Reed, A. L. Demirel, S. Strite, and H. Morkoc, "Investigations of the Si_3N_4/Si/n-GaAs insulator-semiconductor interface with low interface trap density," *Appl. Phys. Lett*. vol. **60**, p. 2511, 1992.

[11] Z. Chen and D. Gong, "Physical and electrical properties of a Si_3N_4/Si/GaAs metal–insulator–semiconductor structure," *J. Appl. Phys*. vol. **90**, p. 4205, 2001.

[12] D. Shahrjerdi, M. M. Oye, A. L. Holmes, Jr., and S. K. Banerjee, "Unpinned metal gate/high-*k* GaAs capacitors: fabrication and characterization," *Appl. Phys. Lett*. vol. **89**, p. 043501, 2006.

[13] A. Jaouad, V. Aimez, C. Aktik, K. Bellatreche, and A. Souifi, "Fabrication of $(NH_4)_2S$ passivated GaAs metal-insulator-semiconductor devices using low-frequency plasma-enhanced chemical vapor deposition," *J. Vac. Sci. Technol*. A vol. **22**, p. 1027, 2004.

[14] M.-K. Lee, C.-F. Yen, J.-J. Huang, and S.-H. Lin, "Electrical characteristics of postmetallization-annealed MOCVD-TiO_2 films on ammonium sulfide-treated GaAs," *J. Electrochem. Soc*. vol. **153**, p. F266, 2006.

[15] M. Passlack, J. K. Abrokwah, Z. Yu, R. Droopad, C. Overgaard, H. Kawayoshi, "Thermally induced oxide crystallinity and interface destruction in Ga_2O_3–GaAs structures," *Appl. Phys. Lett*. vol. **82**, p. 1691, 2003.

[16] M. H. Zhang, M. Oye, B. Cobb, F. Zhu, H. S. Kim, I. J. Ok, J. Hurst, S. Lewis, A. Holmes, J. C. Lee, S. Koveshnikov, W. Tsai, M. Yakimov, V. Torkanov, and S. Oktyabrsky, "Importance of controlling oxygen incorporation into HfO_2/Si/*n*-GaAs gate stacks," *J. Appl. Phys*. vol. **101**, p. 034103, 2007.

[17] V. N. Bessolov, E. V. Konenkova, and M. V. Lebedev, "Sulfidization of GaAs in alcoholic solutions: A method having an impact on efficiency and stability of passivation," *Mat. Sci. Engineer.* vol. **B44**, p. 376, 1997.

[18] V. N. Bessolov, M. V. Lebedev, N. M. Binh, M. Friedrich, and D. R. T. Zahn, "Sulphide passivation of GaAs: the role of the sulphur chemical activity," *Semicond. Sci. Technol.* vol. **13**, p. 611, 1998.

[19] V. N. Bessolov, M. V. Lebedev, A. F. Ivankov, W. Bauhofer, and D. R. T. Zahn, "Electronic properties of GaAs(100) surface passivated in alcoholic sulfide solutions," *Appl. Surf. Sci.* vol. **133**, p. 17, 1998.

[20] V. N. Bessolov, M. V. Lebedev, and D. R. T. Zahn, "Raman scattering study of surface barriers in GaAs passivated in alcoholic sulfide solutions," *J. Appl. Phys.* vol. **82**, p. 2640, 1997.

[21] W. A. Hill and C. C. Coleman, "A single-frequency approximation for interface-state density determination," *Solid State Electron*. vol. **23**, p. 987, 1980.

[22] *NIST Electron Inelastic-Mean-Free-Path Database 71 (v. 1.1)*, National Institute of Standards and Technology, 2000.

[23] K. W. Frese and S. R. Morrison, "Passivation and interface state studies on n-GaAs," *Appl. Surf. Sci*. vol. **8**, p. 266, 1981.

[24] A. G.-Cervantes, Z. R.-Alvarez, M. L.-Lopez, E. L.-Luna, and I. H.-Calderon, "GaAs surface oxide desorption by annealing in ultra high vacuum," *Thin Solid Film* vol. **373**, p. 159, 2000.

[25] J. P. Contour, J. Massies, H. Fronius, and K. Ploog, "An XPS study of the passivating oxide layer produced on GaAs (001) substrate by heating in air above 200 °C," *Jpn. J. Appl. Phys*. vol. **27**, p. L167, 1988.

[26] M. Yamada and Y. Ide, "Anomalous behaviors observed in the isothermal desorption of GaAs surface oxides," *Surf. Sci*. vol. **339**, p. L914, 1995.

[27] H. Sugahara, M. Oshima, H. Oigawa, H. Shigekawa, and Y. Nannichi, "Synchrotron radiation photoemission analysis for $(NH_4)_2S_x$-treated GaAs," *J. Appl. Phys*. vol. **69**, p. 4349, 1991.

[28] H. Sik, Y. Feurprier, C. Cardinaud, G. Turban, and A. Scavennec, “Reduction of recombination velocity on GaAs surface by Ga-S and As-S bond-related surface states from $(NH_4)_2S_x$ treatment,” *J. Electrochem. Soc.* vol. **144**, p. 2106, 1997.

[29] M. V. Lebedev, T. Mayer, and W. Jaegermann, “Sulfur adsorption at GaAs(100) from solution: role of the solvent in surface chemistry,” *Surf. Sci.* vol. **547**, p. 171, 2003.

[30] J.-K. Yang, M.-G. Kang, and H.-H. Park, “Chemical and electrical characterization of Gd_2O_3/GaAs interface improved by sulfur passivation,” *J. Appl. Phys.* vol. **96**, p. 4811, 2004.

[31] L. J. Huang, W. M. Lau, S. Ingrey, D. Landheer, and J.-P. Noel, “Metal-insulator-semiconductor capacitors on cleaved GaAs(110),” *J. Appl. Phys.* vol. **76**, p. 8192, 1994.

[32] B. R. Chakraborty, N. Dilawar, S. Pal, and D. N. Bose, “SIMS characterization of GaAs MIS devices at the interface,” *Thin Solid Films* vol. **411**, p. 240, 2002.

[33] Yu. V. Medvedev, “Thermodynamic stability of GaAs sulfur passivation,” *Appl. Phys. Lett.* vol. **64**, p. 3458, 1994.

[34] C. D. Thurmond, G. P. Schwartz, G. W. Kammlott, and B. Schwartz, “GaAs oxidation and the Ga-As-O equilibrium phase diagram,” *J. Electrochem. Soc.* vol. **127**, p. 1366, 1980.

[35] D. R. Lide, *CRC Handbook of Chemistry and Physics: a Ready-Reference Book of Chemical and Physical Data*, 84th ed., CRC Press, 2003.

[36] O. Knacke, O. Kubaschewski, and K. Hesselmann, *Thermochemical Properties of Inorganic Substances*, Springer, Berlin, 1991.

[37] K. Tone, M. Yamada, Y. Ide, and Y. Katayama, “Characterization of oxidized GaAs (001) surfaces using temperature programed desorption and x-ray photoelectron spectroscopy,” *Jap. J. Appl. Phys. Part.* 2 vol. **31**, p. L721, 1992.

[38] G. W. Smith, A. J. Pidduck, C. R. Whitehouse, J. L. Glasper, A. M. Keir, “Surface

topography changes during the growth of GaAs by molecular beam epitaxy," *Appl. Phys. Lett*. vol. **59**, p. 3282, 1991.

[39] S. C. Ghosh, M. C. Biesinger, R. R. LaPierre, and P. Kruse, "X-ray photoelectron spectroscopic study of the formation of catalytic gold nanoparticles on ultraviolet-ozone oxidized GaAs(100) substrates," *J. Appl. Phys*. vol. **101**, p. 114322, 2007.

[40] S. C. Ghosh, M. C. Biesinger, R. R. LaPierre, and P. Kruse, "The role of proximity caps during the annealing of UV-ozone oxidized GaAs," *J. Appl. Phys*. vol. **101**, p. 114321, 2007.

[41] D. A. Allwood, S. Cox, N. J. Mason, R. Palmer, R. Young, and P. J. Walker, "Monitoring epiready semiconductor wafers," *Thin Solid Films* vol. **412**, p. 76, 2002.

[42] J. S. Song, Y. C. Choi, S. H. Seo, D. C. Oh, M. W. Cho, T. Yao, and M. H. Oh, "Wet chemical cleaning process of GaAs substrate for ready-to-use," *J. Cryst. Growth* vol. **264**, p. 98, 2004.

[43] M. Takahashi, T. Nakatani, S. Iwamoto, T. Watanabe and M. Inoue, "Effect of modification by alkali on the gamma-Ga_2O_3-Al_2O_3 mixed oxides prepared by the solvothermal method," *J. Phys.: Condens. Matter.* vol. **18**, p. 5745, 2006.

[44] C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. A.-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, "GaAs interfacial self-cleaning by atomic layer deposition," *Appl. Phys. Lett.* vol. **92**, p. 071901, 2008.

[45] M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, H. C. Kim, E. M. Vogel, J. Kim, and R. M. Wallace, "Half-cycle atomic layer deposition reaction studies of Al_2O_3 on $(NH_4)_2S$ passivated GaAs(100) surfaces," *Appl. Phys. Lett.* vol. **93**, p. 252905, 2008.

[46] J. C. Hackley, J. D. Demaree, and T. Gougousi, "Interface of atomic layer deposited HfO_2 films on GaAs (100) surfaces," *Appl. Phys. Lett.* vol. **92**, p. 162902, 2008.

[47] C. Y. Kim, S. W. Cho, M.-H. Cho, K. B. Chung, C.-H. An, H. Kim, H. J. Lee, and D.-H.

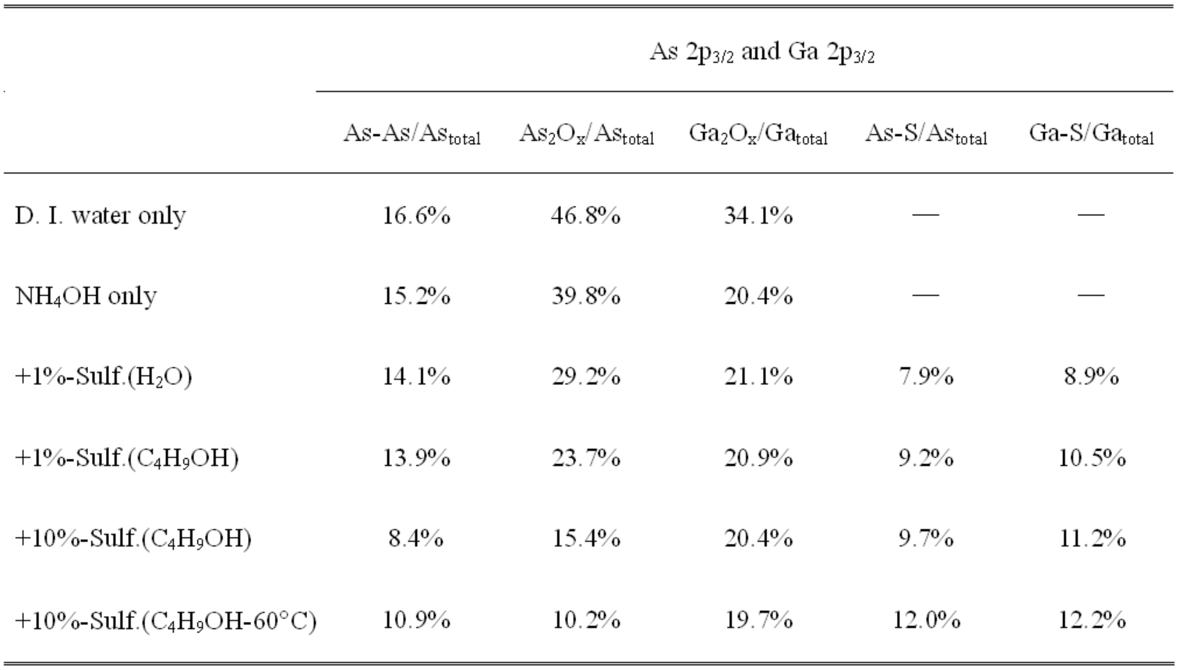
Ko, “Interfacial reaction of atomic-layer-deposited HfO_2 film as a function of the surface state of an n-GaAs (100) substrate,” *Appl. Phys. Lett.* vol. **93**, p. 192902, 2008.

[48] G. K. Dalapati, A. Sridhara, A. S. W. Wong, C. K. Chia, and D. Z. Chi, “HfO_xN_y gate dielectric on p-GaAs,” *Appl. Phys. Lett.* vol. **94**, p. 073502, 2009.

[49] D. Shahrjerdi, E. Tutuc, and S. K. Banerjee, “Impact of surface chemical treatment on capacitance-voltage characteristics of GaAs metal-oxide-semiconductor capacitors with Al_2O_3 gate dielectric,” *Appl. Phys. Lett.* vol. **91**, p. 063501, 2007.

[50] R. Suri, B. Lee, D. J. Lichtenwalner, N. Biswas, and V. Misra, “Electrical characteristics of metal-oxide-semiconductor capacitors on p-GaAs using atomic layer deposition of ultrathin HfAlO gate dielectric,” *Appl. Phys. Lett.* vol. **93**, p. 193504, 2008.

[51] M. Zhu, H.-C. Chin, C.-H. Tung, and Y.-C. Yeo, “In situ silane passivation of gallium arsenide and deposition of high-permittivity gate dielectric for MOS applications,” *J. Electrochem. Soc.*, vol. **154**, p. H879, 2007.



	As $2p_{3/2}$ and Ga $2p_{3/2}$				
	As-As/As_{total}	As_2O_x/As_{total}	Ga_2O_x/Ga_{total}	As-S/As_{total}	Ga-S/Ga_{total}
D. I. water only	16.6%	46.8%	34.1%	—	—
NH_4OH only	15.2%	39.8%	20.4%	—	—
+1%-Sulf.(H_2O)	14.1%	29.2%	21.1%	7.9%	8.9%
+1%-Sulf.(C_4H_9OH)	13.9%	23.7%	20.9%	9.2%	10.5%
+10%-Sulf.(C_4H_9OH)	8.4%	15.4%	20.4%	9.7%	11.2%
+10%-Sulf.(C_4H_9OH-60°C)	10.9%	10.2%	19.7%	12.0%	12.2%

Table. 5.1 Chemical ratios of As $2p_{3/2}$ and Ga $2p_{3/2}$ spectra for the GaAs substrate after undergoing different wet-chemical procedures. Note that the surface of all samples has been exposed to air for ca. 10 min prior to chemical analysis.

	Ga	As	Al	O	O/Al ratio
Control (HCl/H_2O, 1:10)	0.2%	0.2%	36.3%	63.3%	1.75
$(NH_4)_2S_{aq}$ (2%, 30 s)	0%	0.1%	36.9%	63.0%	1.70
$(NH_4)_2S_{aq}$ (2%, 30 min)	0%	0.05%	38.8%	61.15%	1.57

Table. 5.2 Calculated relative concentrations of GaAs oxides and stoichiometric O-to-Al ratios in as-deposited ALD-Al_2O_3 thin films before and after chemical treatment with $(NH_4)_2S$. Note that the As 2$p_{3/2}$, Ga 2$p_{3/2}$, Al 2p, and O 1s core levels were used by considering the atomic sensitivity factor.

	As 3*d* and Ga 3*d*		
	As-As/As_{Total}	As_2O_x*/As_{Total}	Ga_2O_x**/Ga_{Total}
Control (HCl/H_2O, 1:10)	18.5%	5%	17.70%
$(NH_4)_2S_{aq}$ (2%, 30 s)	13.4%	0%	9.84%
$(NH_4)_2S_{aq}$ (2%, 30 min)	12.8%	0%	8.86%

*The As_2O_x chemical species include As_2O_5, As_2O_3, and As suboxides.

**The Ga_2O_x chemical species include Ga_2O_3 and Ga suboxides.

Table. 5.3 Chemical bonding ratios of As 3*d* and Ga 3*d* core levels determined by fitting the XPS data from Fig. 5.5. Note that the contribution of the O 2*s* emission has been excluded.

	T_c (°C)	$\triangle G_f$ (kJ mol^{-1})
A. Transformation reactions:[a]		
(I) $4AsO_x(s) \rightarrow 4As(s)$ or $As_4(g)\uparrow + xO_2(g)$	150–200 °C	—
(II) $As_2O_3(s) + 2GaAs(s) \rightarrow Ga_2O_3(s) + 4As(s)$ or $As_4(g)\uparrow$	290–350 °C	–280/–225 (@300 K) & –277/–233 (@600 K)
(III) $As_2O_3(s) + 4Ga(s,l) \rightarrow Ga_2O_3(s) + 2GaAs(s)$	—	–564 (@300 K) & –521 (@600 K)
(IV) $As_2O_3(s) + 2Ga(s,l) \rightarrow Ga_2O_3(s) + 2As(s)$ or $As_2(g)\uparrow$	—	–422/–347 (@300 K) & –399/–403 (@600 K)
(V) $Ga(s,l) + As(s) \rightarrow GaAs(s)$	—	–70 (@300 K) & –50 (@900 K)
B. Oxidation reactions:[b]		
(I) $2GaAs(s) + 3/2O_2(g) \rightarrow As_2O_3(s) + 2Ga(s,l)$	—	–435 (@300 K) & –376 (@600 K)
(II) $2Ga(s,l) + 3/2O_2(g) \rightarrow Ga_2O_3(s)$	—	–999 (@300 K) & –896 (@600 K)
(III) $2As(s) + 3/2O_2(g) \rightarrow As_2O_3(s)$	—	–576 (@300 K) & –497 (@600 K)
(IV) $As_2O_3(s) + O_2(g) \rightarrow As_2O_5(s)$	—	–207 (@300 K) & –141 (@600 K)

Table. 5.4 Solid state chemical reactions of Ga–As–O associated systems. All these equations are separated into four parts.

	T_c (°C)	$\triangle G_f$ (kJ mol^{-1})
C. GaAs decomposition/As vaporization reactions (inhibited at room temperature):[c]		
(I) $2As(s) \rightarrow As_2(g)$	300 °C	139 (@300 K) & 48 (@875 K)
(II) $4As(s) \rightarrow As_4(g)$	300 °C	76 (@300 K) & –81 (@875 K)
(III) $4GaAs(s) \rightarrow 4Ga(s,l)$ + $4As(s)$ or $As_4(g)\uparrow$	500–600 °C	280/379 (@300 K) & 200/195 (@900 K)
D. Ga_2O[d] formation reactions (inhibited at room temperature):[e]		
(I) $As_2O_3(s) + 6GaAs(s) \rightarrow$ $3Ga_2O(s) + 8As(s)$ or $2As_4(g)\uparrow$	—	6/202 (@300 K) & << 6 (@600 K)
(II) $Ga_2O_3(s) + 4Ga(s,l) \rightarrow 3Ga_2O(s)$	500–600 °C	7 (@300 K) & << 7 (@900 K)
(III) $Ga_2O_3(s) + 4GaAs(s) \rightarrow$ $3Ga_2O(s) + 4As(s)$ or $As_4(g)\uparrow$	400–500 °C	287/385 (@300 K) & << 287 (@900 K)

[a]Ref. 25,26,40, [b]ref. 41, and [c]ref. 26, 36.

[d]The standard molar Gibbs free energy of formation ($\triangle G_f$) for $Ga_2O(s)$ was assumed to be –330 kJ mol^{-1}, based on the standard molar enthalpy of formation ($\triangle H_f$) of –356 kJ mol^{-1} at 300 K (ref. 35).

[e]Ref. 26,38,40.

Table. 5.4 (Conti.) Solid state chemical reactions of Ga–As–O associated systems. All these equations are separated into four parts.

	Ga	As	Al	O	O/Al ratio
Sulfide + N_2 600 °C PDA	0.3%	2.0%	34.8%	62.9%	1.80
Sulfide + O_2 600 °C PDA	0.11%	2.94%	35.1%	61.8%	1.76
O_2 600 °C PDA only	0.24%	3.87%	30.0%	65.8%	2.19

Table. 5.5 Calculated relative concentration of GaAs oxides and stoichiometric O-to-Al ratios in the N_2- and O_2-annealed ALD-Al_2O_3 thin films with and without $(NH_4)_2S$ surface passivation.

	As 3*d* & Ga 3*d*		
	As–As/As_{Total}	As_2O_x*/As_{Total}	Ga_2O_x**/Ga_{Total}
Sulfide + N_2 PDA at 600 °C	10.6%	20.6%	17.4%
Sulfide + O_2 PDA at 600 °C	6.2%	26.0%	16.8%
O_2 PDA at 600 °C only	9.2%	30.8%	27.6%

*The As_2O_x chemical species include As_2O_5, As_2O_3, and As suboxides.

**The Ga_2O_x chemical species include Ga_2O_3 and Ga suboxides.

Table. 5.6 Chemical bonding ratios of As 3*d* and Ga 3*d* core levels determined by fitting the XPS data from Fig. 5.12. Note that the contribution of the O 2*s* emission has been excluded.

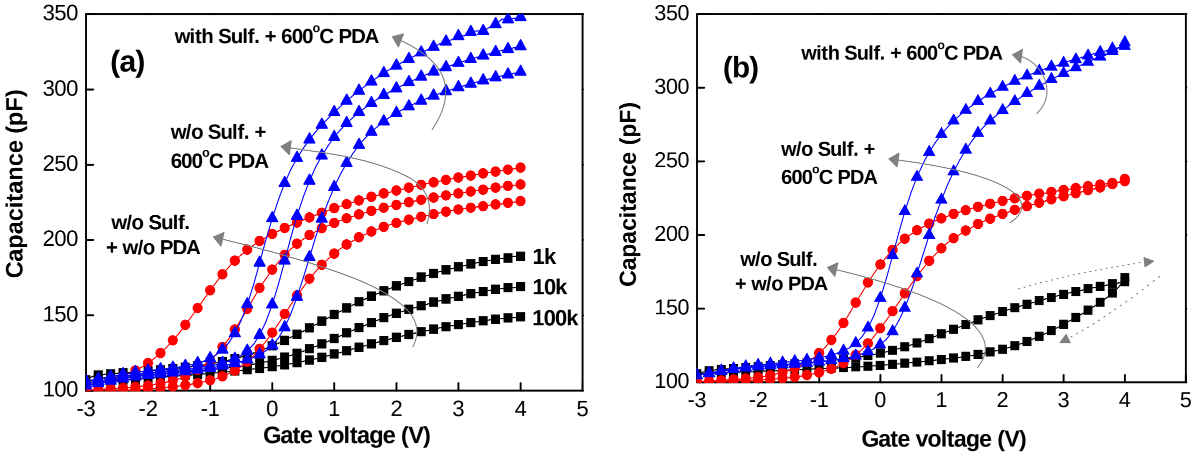


Fig. 5.1 (a) Multi-frequency *C-V* and (b) bidirectional *C-V* (10 kHz) curves of Pt/ALD-Al_2O_3/n^+-GaAs capacitors with different cleaning preparation and annealing processes. The Al_2O_3 films were deposited at 100 °C for 60 cycles.

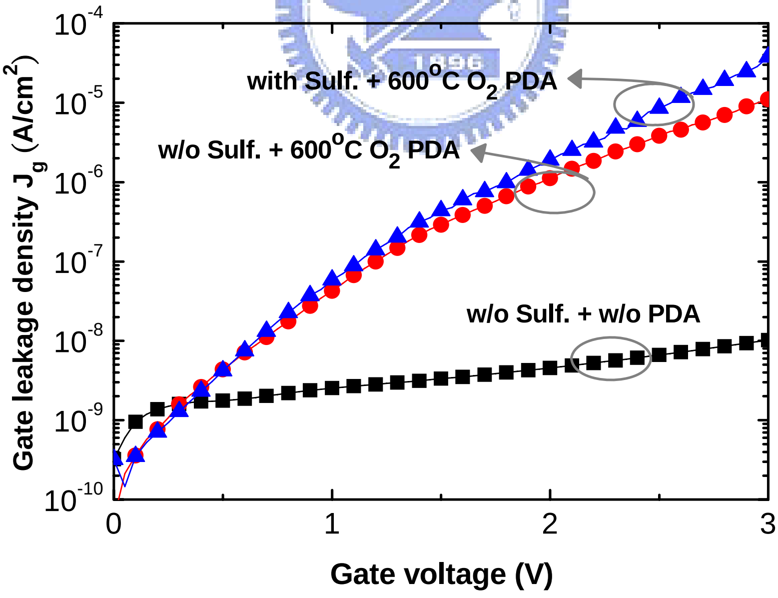


Fig. 5.2 Gate leakage current J_g characteristics of Pt/Al_2O_3/n-GaAs capacitors. The Al_2O_3 thin films were deposited at 100 °C for 60 cycles.

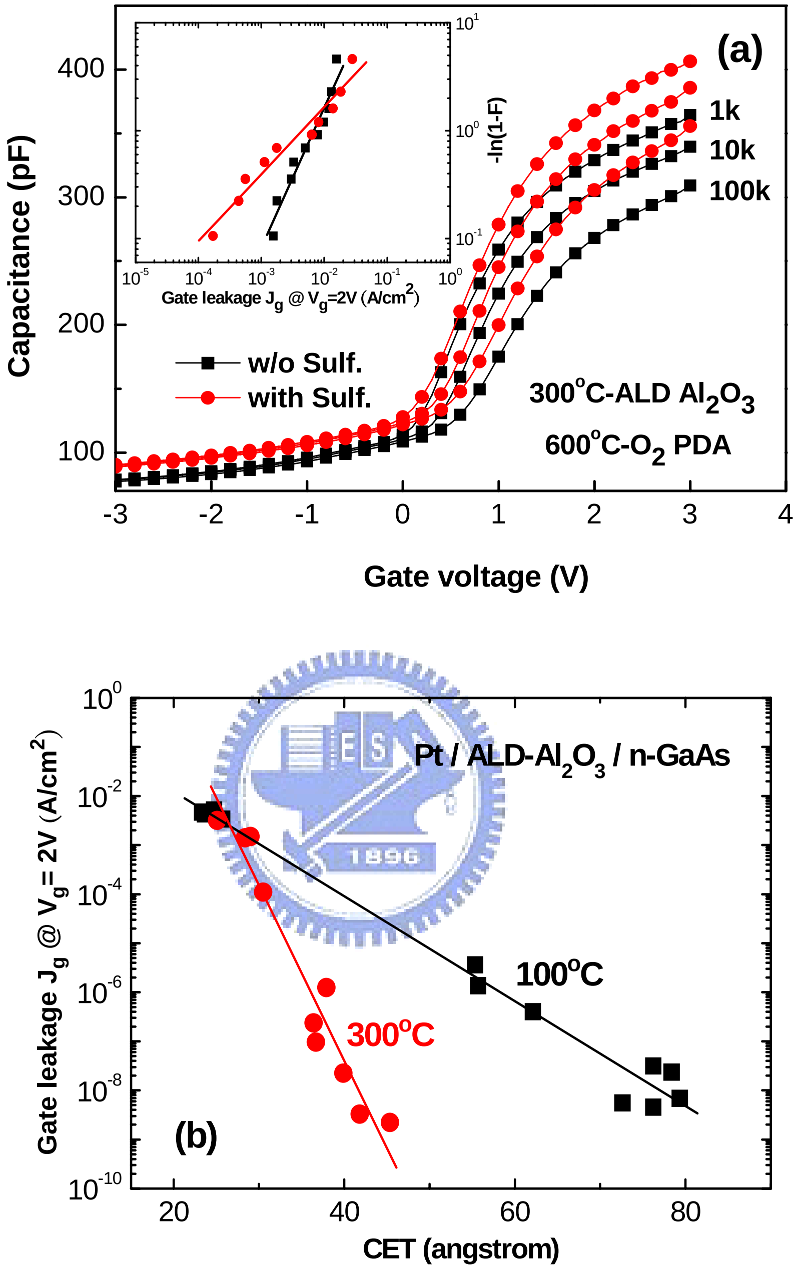


Fig. 5.3 (a) *C*-*V* curves of GaAs MOS capacitors with ALD-Al$_2$O$_3$ deposited at 300°C for 60 cycles and (b) Comparison of J$_g$ versus CET characteristics of ALD-Al$_2$O$_3$/GaAs capacitors deposited at 100 and 300 °C with different surface preparation and annealing processes.

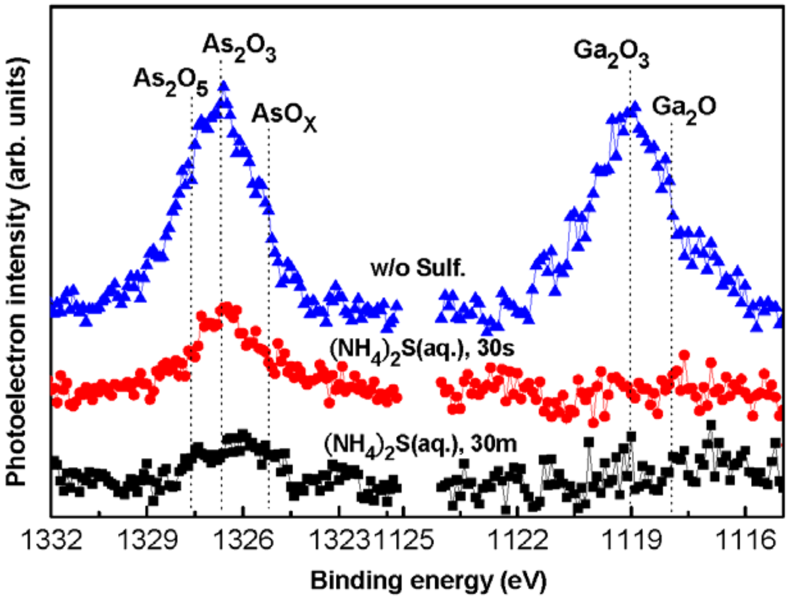


Fig. 5.4 As 2$p_{3/2}$ and Ga 2$p_{3/2}$ XPS spectra of as-deposited ALD-Al_2O_3 thin films on GaAs substrates without and with $(NH_4)_2S$ sulfide passivation.

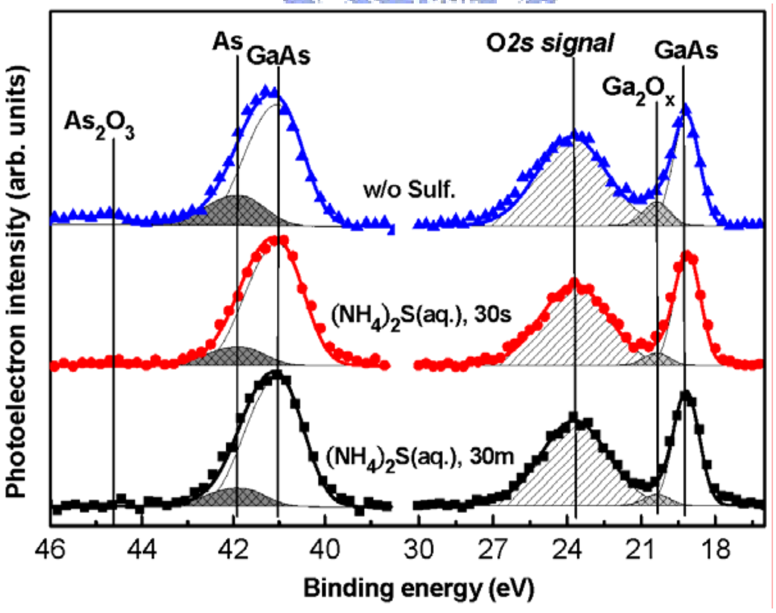


Fig. 5.5 As 3*d* and Ga 3*d* XPS spectra of as-deposited ALD-Al_2O_3 thin films on GaAs substrates with and without $(NH_4)_2S$ sulfide passivation.

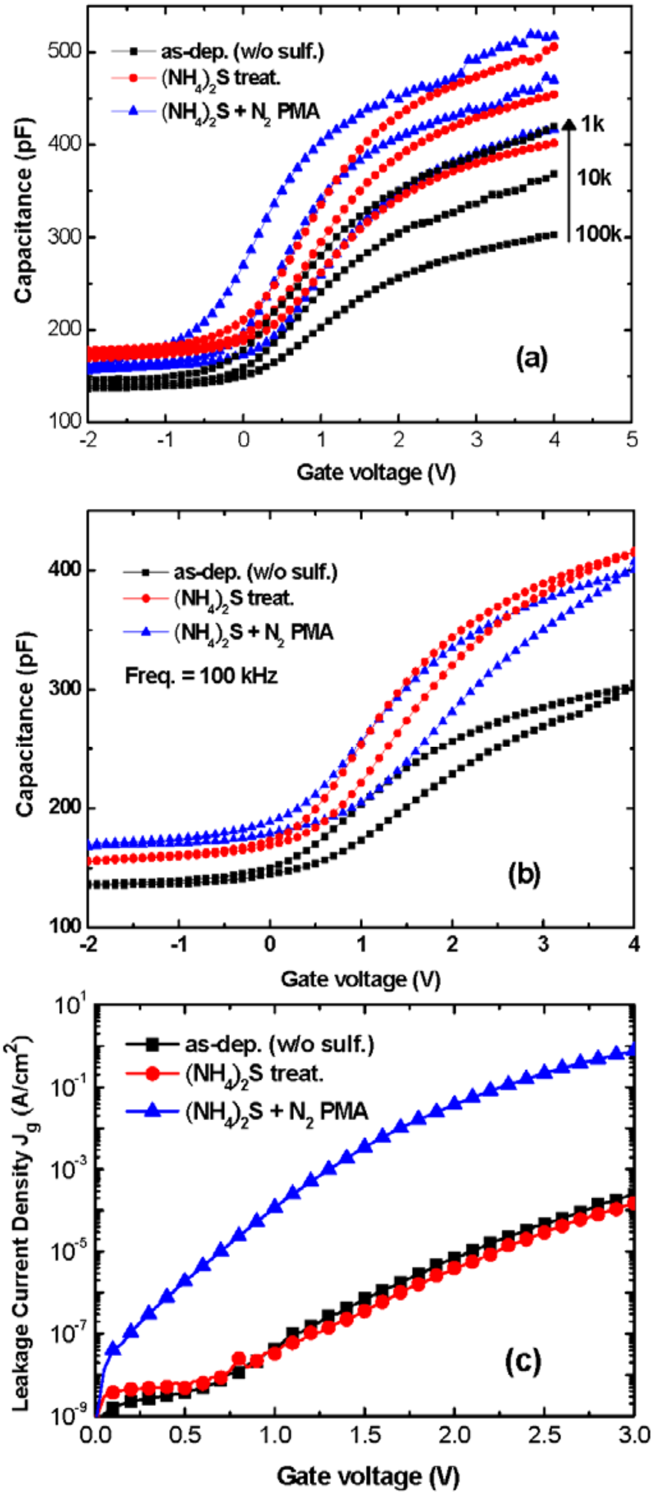


Fig. 5.6 (a) Multi-frequency and (b) bi-directional *C*–*V* characteristics and (c) gate leakage current (*I*–*V*) curves of GaAs MOS capacitors with as-deposited Al_2O_3 thin films after $(NH_4)_2S$ passivation and PMA at 400 °C.

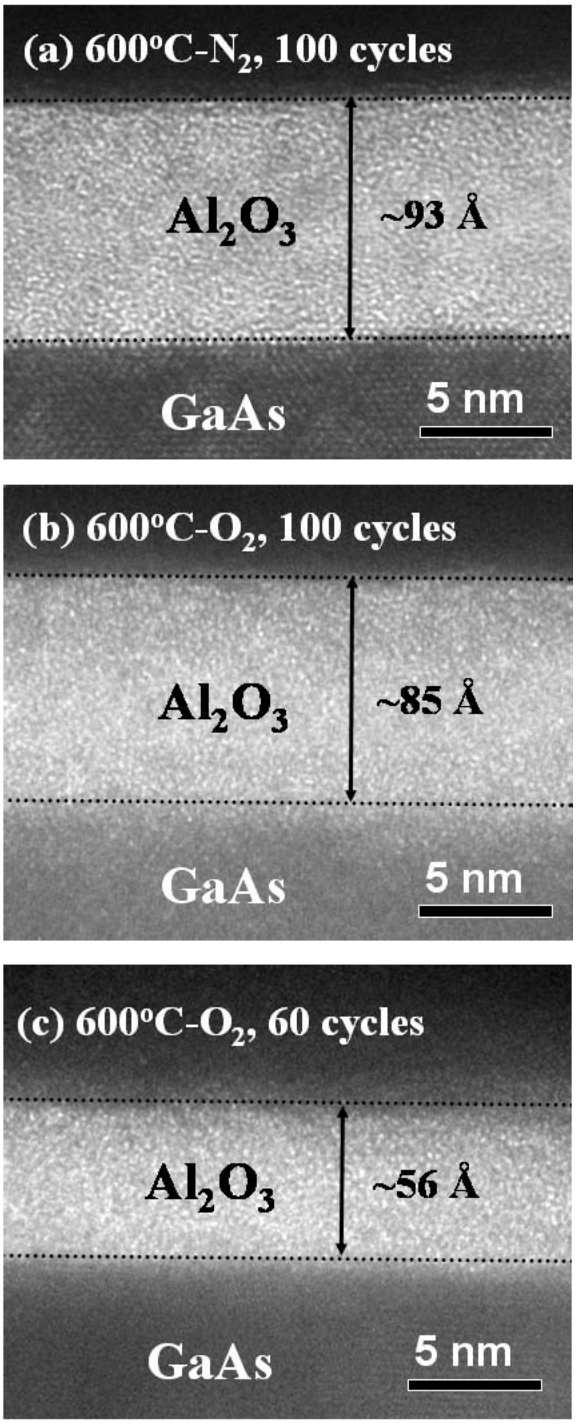


Fig. 5.7 HRTEM images of Pt/Al_2O_3/sulfidized-GaAs structures with different deposition cycles and PDA conditions: (a) 100 cycles, N_2 PDA; (b) 100 cycles, O_2 PDA; (c) 60 cycles, O_2 PDA. PDA temperature: 600 °C.

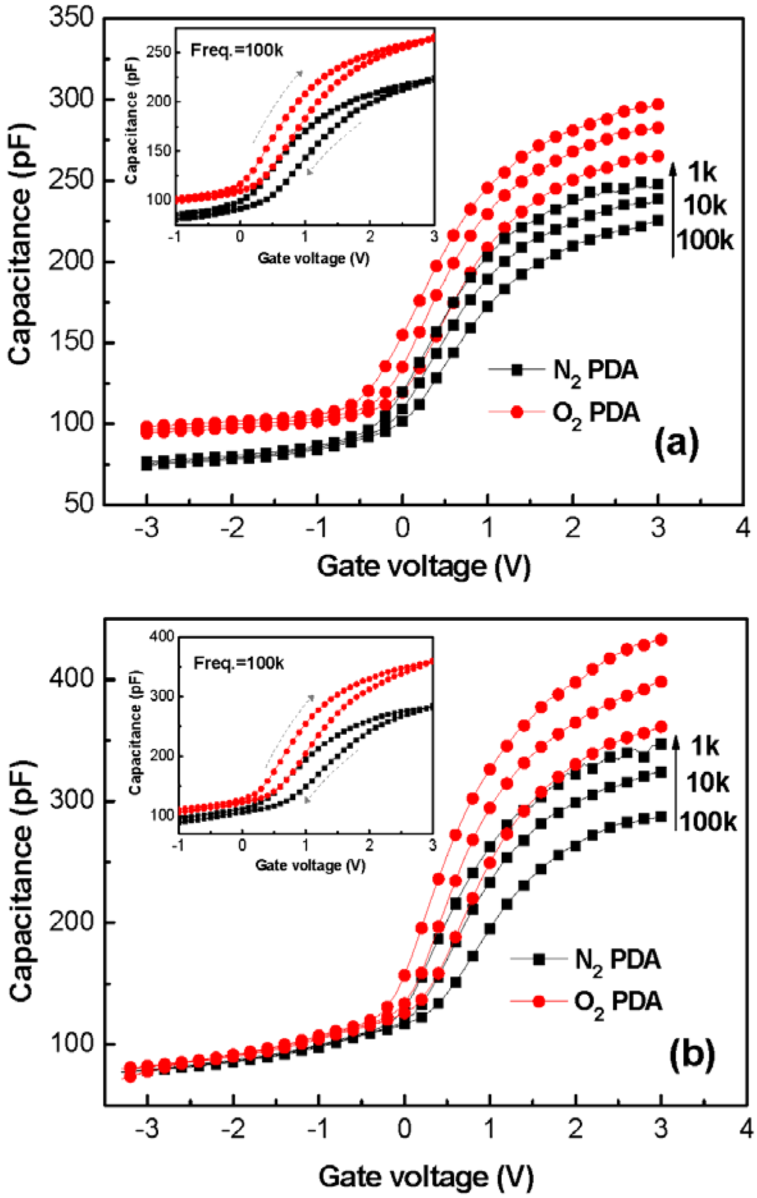


Fig. 5.8 Multi-frequency *C*–*V* curves of sulfidized-GaAs MOS capacitors with Al_2O_3 thin films annealed for (a) 100 and (b) 60 deposition cycles. Each inset displays the respective *C*–*V* hysteresis measured at 100 kHz.

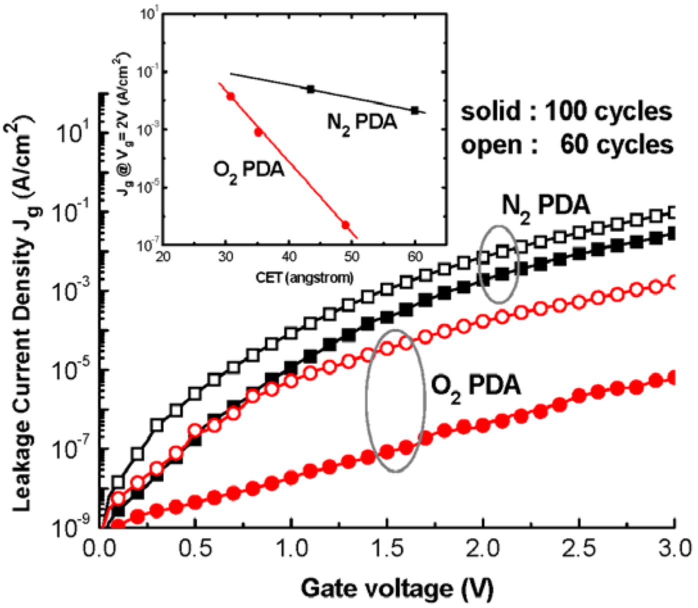


Fig. 5.9 *I–V* Characteristics of the MOS capacitors analyzed in Fig. 5.8. Inset: Plot of J_g (at V_g = 2 V) versus CET.

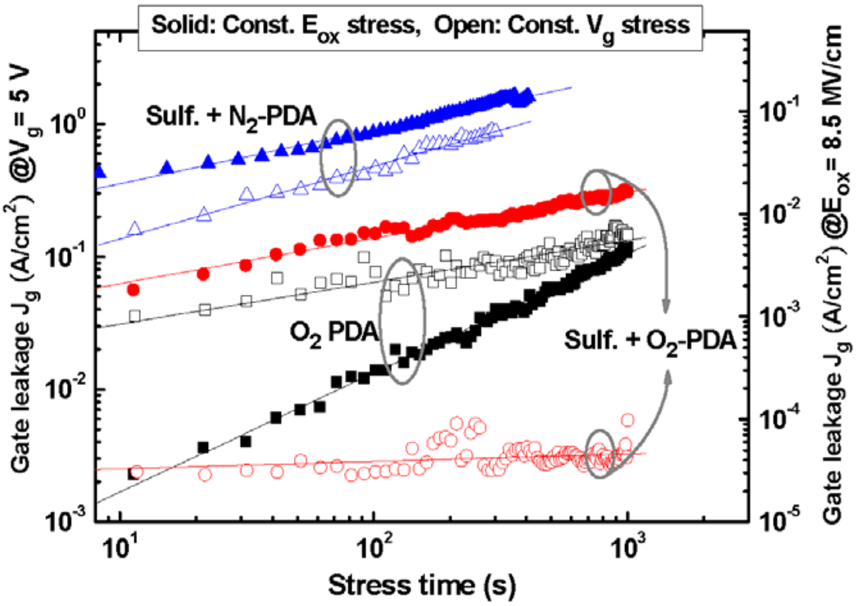


Fig. 5.10 Stress time dependence of the gate leakage J_g for Pt/ALD-Al$_2$O$_3$/GaAs MOS capacitors under a constant V_g stress of 5 V (at the left *y*-axis) and a constant E_{ox} stress of 8.5 MV cm^{-1} (at the right *y*-axis), respectively.

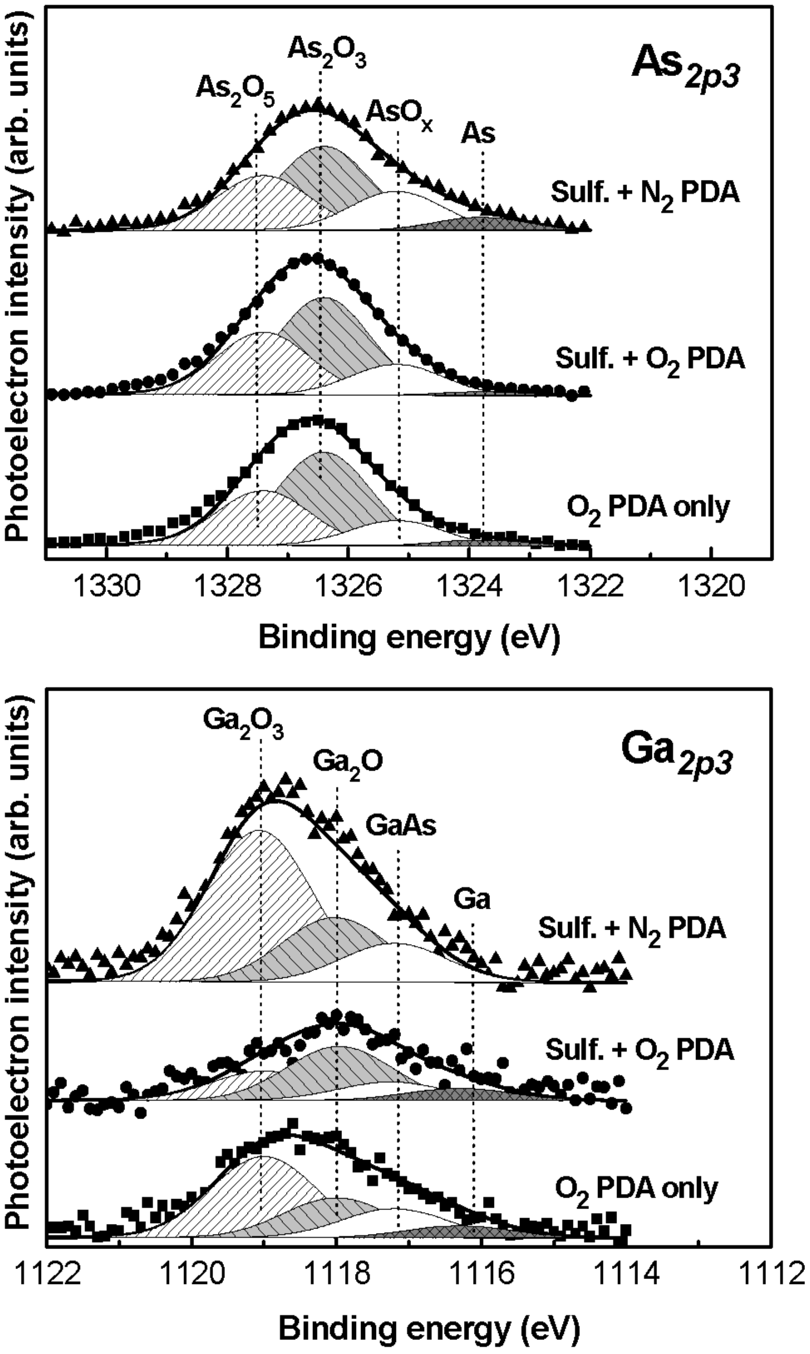


Fig. 5.11 As $2p_{3/2}$ and Ga $2p_{3/2}$ XPS spectra of 600 °C-annealed Al_2O_3 thin films on the sulfidized GaAs substrate. The contributing chemical components were extracted and are displayed in the respective spectra.

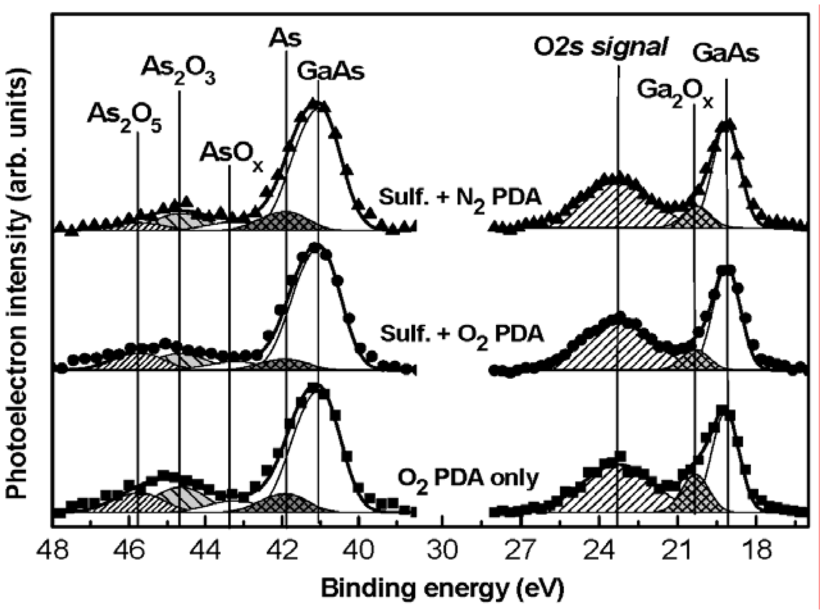


Fig. 5.12 As 3*d* and Ga 3*d* XPS spectra of 600 °C-annealed Al_2O_3 thin films on the sulfidized GaAs substrate. The contributed chemical components were extracted and are displayed in the respective spectra.

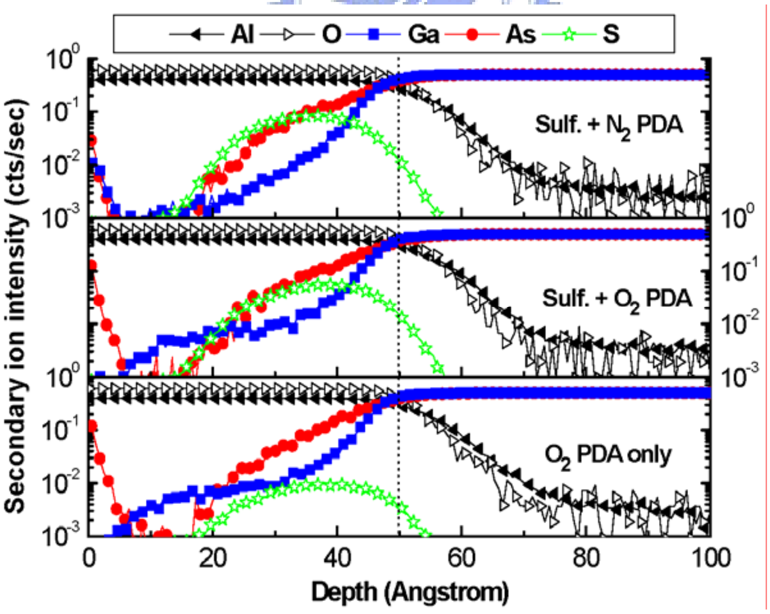


Fig. 5.13 SIMS depth profiles of the Al_2O_3/GaAs samples analyzed in Fig. 5.12. The diffusion of As- and Ga-related chemical species into overlying high-*k* film was observed.

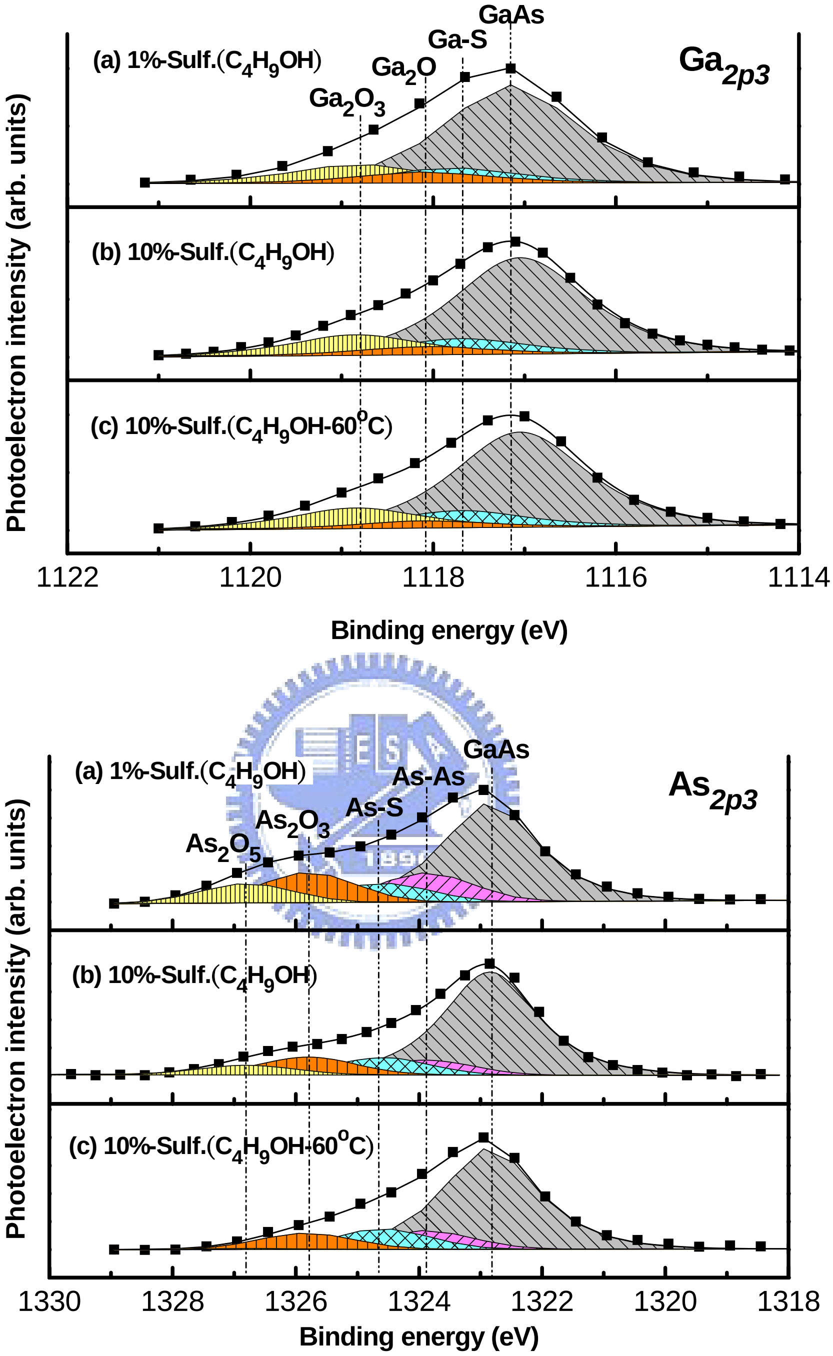


Fig. 5.14 Ga $2p_{3/2}$ and As $2p_{3/2}$ XPS spectra of GaAs substrate subjected to different wet-chemical procedures. Four components were extracted in Ga $2p_{3/2}$ spectra: GaAs, GaS_x, Ga_2O, and Ga_2O_3, while five components were extracted in As $2p_{3/2}$ spectra: GaAs, elemental As, AsS_x, As_2O_3, and As_2O_5.

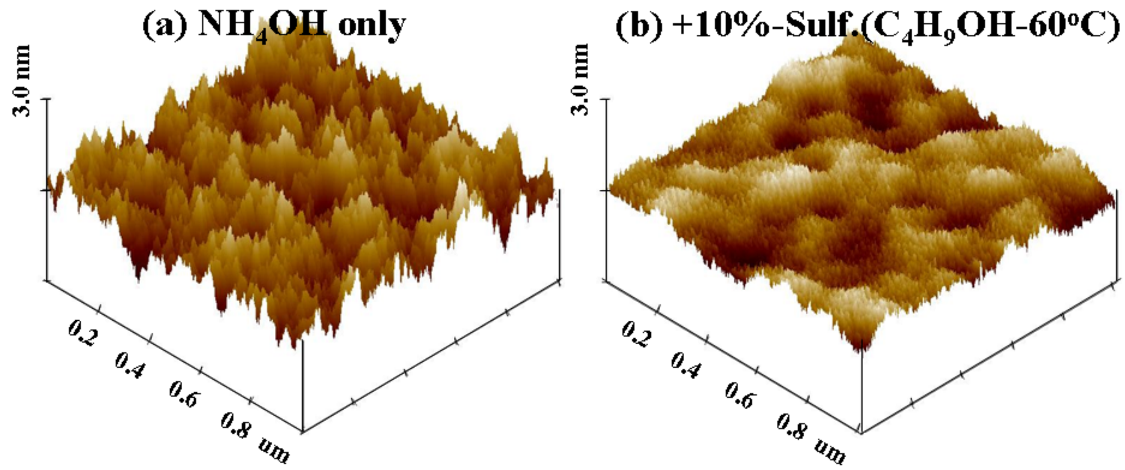


Fig. 5.15 AFM images of the NH_4OH-cleaned GaAs substrates (a) before and (b) after receiving $(NH_4)_2S$-C_4H_9OH(10%, 60 °C) chemical treatment, respectively.

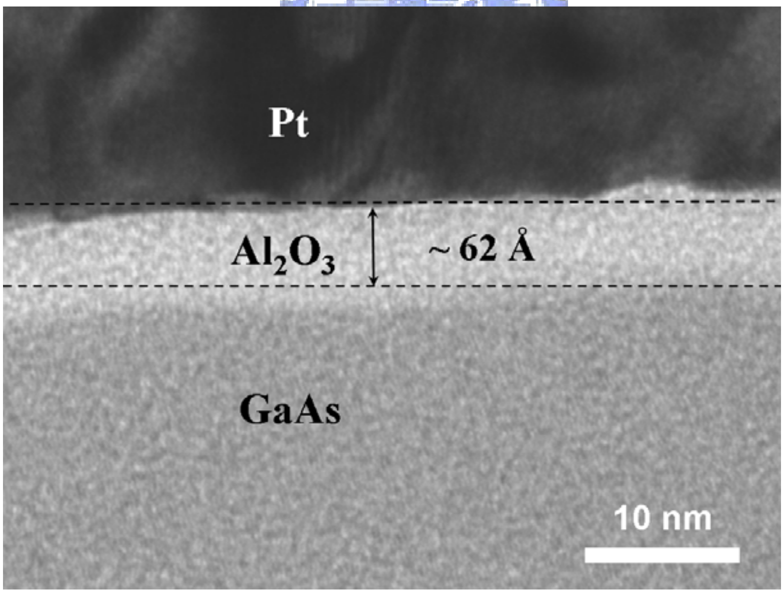


Fig. 5.16 TEM image of the as-deposited Pt/ALD-Al_2O_3(60 deposition cycles)/GaAs MOS structure with $(NH_4)_2S$-C_4H_9OH(10%, RT) chemical treatment.

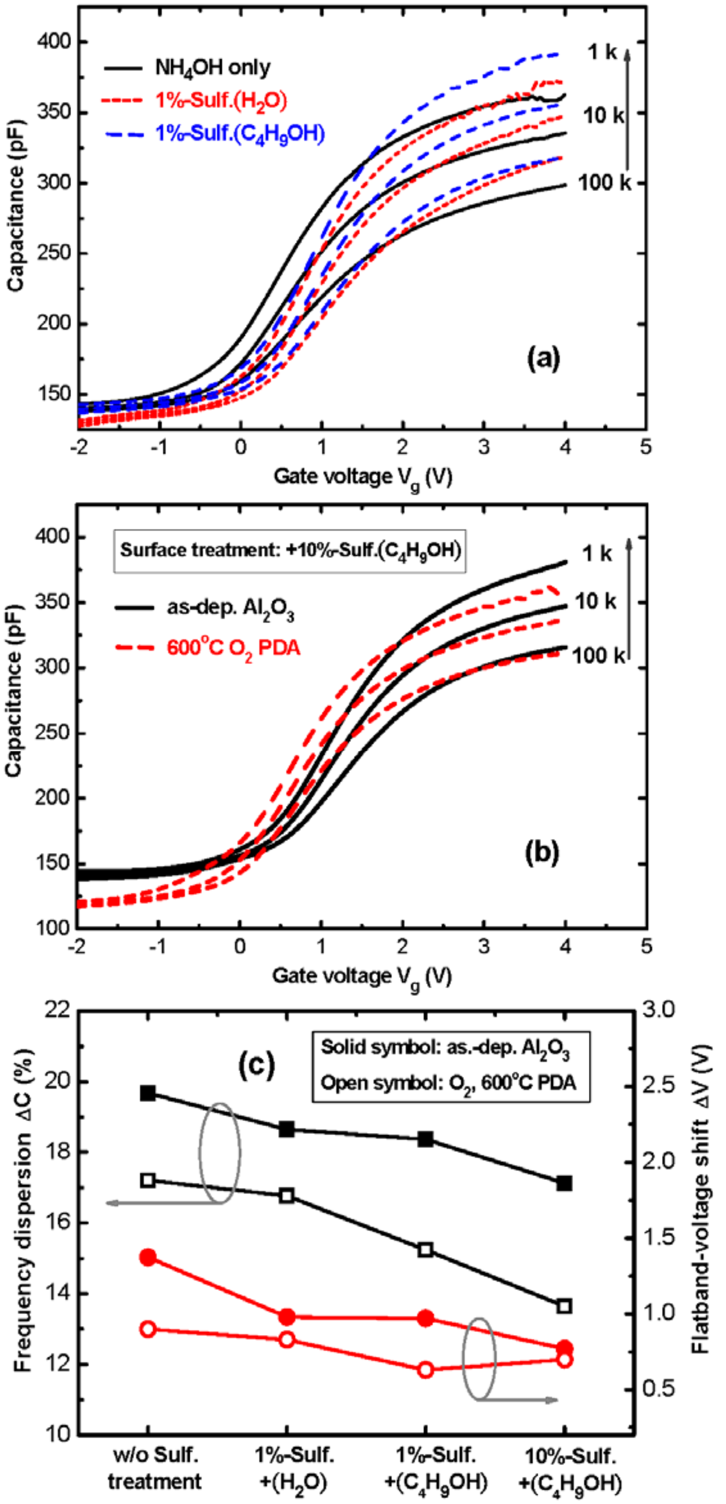


Fig. 5.17 Multi-frequency *C*–*V* curves of Pt/Al_2O_3/n-GaAs capacitors (a) with different wet-chemical procedures; (b) before and after 600 °C PDA. (c) Variations of the frequency response of △C and △V values.

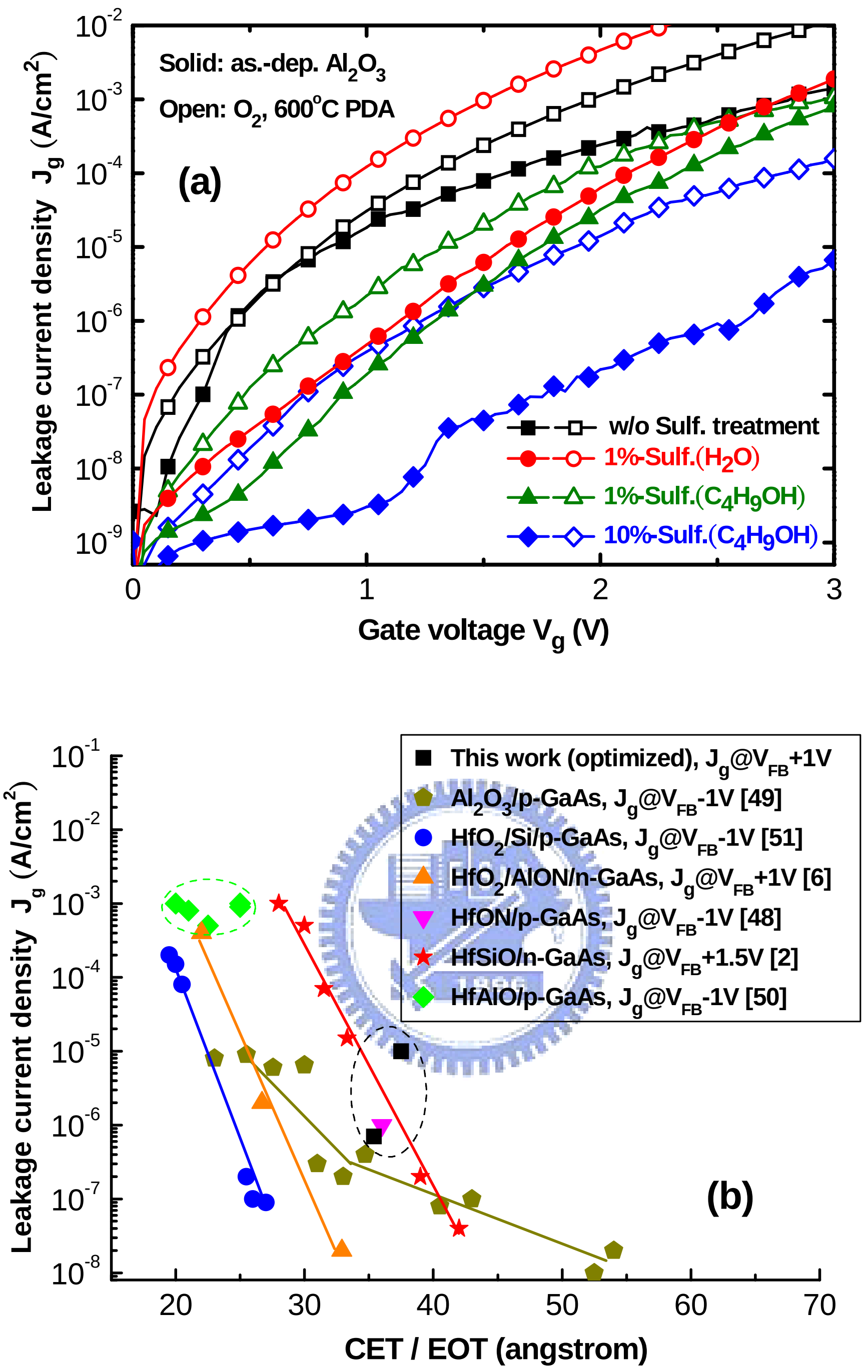


Fig. 5.18 (a) The I–V characteristics of Pt/Al_2O_3/n-GaAs capacitors with various sulfidizing conditions (solid symbols) before and (open symbols) after 600 °C PDA in O_2 ambient, respectively. (b) Comparison of J_g versus CET or EOT characteristics for our work with other's published data [2], [6], [48]-[51].

Chapter 6

Inversion-Mode Ge p- and n-MOSFETs and Depletion-Mode GaAs n-MOSFET with Atomic-Layer-Deposited Al_2O_3 Gate Dielectrics

6.1 Introduction

When Si complementary metal-oxide-semiconductor (CMOS) technologies gradually approximate to 22 nm node, the field of high mobility semiconductor materials is renewed in MOS field effect transistor (MOSFET) applications to pursue much higher device performance. In particular, Ge- and III-V-based channels featuring various prevailing gate dielectrics are promising structures to use in place of conventional Si MOSFETs. Nevertheless, several formidable challenges remain if we are to realize state-of-the-art Ge devices. The first bottleneck is the water-solubility and poor thermal stability of its native oxide. Even though GeO_2–Ge interfaces can be prepared with excellent quality [1], subsequent thermal processing is likely to degrade the gate stack integrity. Fortunately, recent developments in high-*k* material deposition and surface pretreatment methods—e.g., thermal annealing in SiH_4 ambient [2] and atomic N radical plasma [3]—have expanded the possibilities in this field. Other key obstacles are the smaller band gap of Ge and the higher intrinsic carrier concentration (ca. 10^{13} cm^{-3}; cf. ca. 10^{10} cm^{-3} in Si), which lead to larger junction leakage currents [4]. In addition, because a higher thermal budget is required during n-type dopant activation, more rapid dopant diffusion (either out of the surface or into the substrate) and lower electrical activation are generally observed. A shallow source/drain (S/D) junction possessing an acceptable off-state current, within the range from 10^{-4} to 10^{-7} A cm^{-2} [5], will be required if we are to achieve higher device performance.

Although superior high-*k*/Ge p-FET characteristics have been reported recently [6], [7], the fabrication of promising Ge n-FETs remains challenging because of the resulting low electron mobility. Such n-FET degradation behavior can be explained in terms of the asymmetrical distribution of interface states, the surface Fermi level (E_F) pinning, and the junction issues mentioned above. On the other hand, still several promising n-FET device characteristics based on (In)GaAs- and InSb-based III-V channels have been continually demonstrated [8]-[10], and their performance even surpassed the strained-Si transistor at the sub-micro gate length [10]. In fact, for obtaining the superior III-V device performance, it is essential to achieve the unpinned oxide/substrate interface. Such a E_F pinning effect—arising from the onset of high interfacial state density (D_{it})—actually casts some doubts on the anticipated performance [11]. Even up to date, this pinning issue is still of interest and more challenging for the dielectrics on GaAs substrate, relative to on InGaAs, because of having a larger energy difference between the charge neutrality level and the conductance band edge [12]. Various kinds of the modified wet-chemical procedures and passivation methods, such as acid-alcohol solution [13], hydrogen clean [14], Si capping layer [15], [16], silane-ammonia [17], and sulfur treatment [18], are adopted to eliminate the native oxides and other surface defects.

From several literatures, it was found that the deposition of Al_2O_3 or the incorporation of Al into HfO_2 dielectrics on Ge substrates can improve the device characteristics—e.g., decreased intermixing [19] and lower D_{it} [20], [21]—relative to those of the system in which HfO_2 is applied directly onto the Ge substrate. Hence, the characteristics of atomic-layer-deposited (ALD) Al_2O_3 gate dielectrics on either Ge channels or substrates are worth studying in more detail. Herein, we firstly focused on the structural and electrical characteristics of Ge junction diodes—in particular, the n^+p junction. We also analyzed the underlying leakage paths and mechanisms. We adopted gate-last processes when fabricating the Ge devices to avoid degradation of the Al_2O_3–Ge interface during the high-temperature treatment required for S/D activation. Moreover, we also investigated the effects of forming gas annealing (FGA) on the Ge junction and device properties—including the reverse leakage current, dielectric interface quality, subthreshold swing, and on/off ratio. We also succeeded to fabricate the depletion-mode (D-mode) GaAs n-MOSFETs with ALD-Al_2O_3 gate dielectrics on the molecular beam epitaxy (MBE) GaAs structures.

6.2 Experimental Procedures

6.2.1 Fabrication of Ge N^+P Junction Diodes

Gallium-doped (ca. 2×10^{15} cm^{-3}) Ge UMICORE substrates were used to study the Ge n^+p diodes through a two-mask processing layout. We used plasma-enhanced chemical vapor deposition (PECVD) to deposit a SiO_2 isolation layer having a thickness of 420 nm to define the P implantation regions, which were implanted at doses of 2×10^{14} and 1×10^{15} cm^{-2} at 30 and 60 keV, respectively. Subsequent rapid thermal annealing (RTA) in a N_2 ambient was performed at temperatures ranging from 500 to 700 °C and for lengths of time ranging from 30 to 90 s. During dopant activation, a PECVD-SiO_2 layer (50 nm) was deposited as the capping layer to examine the improvement in the junction. Finally, a 500-nm-thick layer of Al metal was deposited and then defined as gate and substrate contacts using a lift-off process. Secondary ion mass spectrometry (SIMS) was used to analyze the P dopant profile (note that surface oxide layer was removed prior to analysis).

6.2.2 Fabrication of Gate-Last Ge p- and n-MOSFETs

This fabrication step employed n- and p-type (100) Ge wafers that had been doped with

Sb and Ga dopants at levels of 1 × 10^{14} and 2 × 10^{15} cm^{-3}, respectively. These two substrates were pre-cleaned through cyclic rinsing with dilute hydrofluoric acid and deionized water, and then they were capped with a 420-nm-thick layer of SiO_2 that acted as the field oxide. The source/drain (S/D) junction region was then opened, followed by implantation of the B (1 × 10^{15} cm^{-2}, 60 keV) and P (1 × 10^{15} cm^{-2}, 30 keV) dopants into the respective n-Ge and p-Ge substrates. In the N_2-RTA split conditions, the annealing temperatures were studied in the range 500–650 °C for the B dopant and 650–700 °C for the P dopant. The annealing time was maintained at 30 s for all devices. In addition, considering the onset of severe P out-diffusion during activation, the deposition of a SiO_2 capping layer was required for the n-FET. The SiO_2 was subsequently removed from the active region and then the Al_2O_3 high-*k* gate dielectric was deposited at 170 °C for 100 cycles in ALD. After excavating the S/D contact holes, Al metallization was performed with patterning to define the metal pads; the substrate contact was prepared directly through thermal evaporation of Al onto the Ge backside. The overall MOSFET structures were subjected to FGA in a H_2/N_2 (10%) mixed ambient at a temperature of 300, 350, or 400 °C for 30 min.

6.2.3 Fabrication of Depletion-Mode GaAs n-MOSFET

We employed the MBE system to grow the GaAs stack structure for fabrication of the D-mode MOSFET, as the scheme displayed in **Fig. 6.1**. We did the mesa isolation and then opened the n-GaAs channel region by etching in a solution of $H_3PO_4:H_2O_2:H_2O$ = 60:20:1500 (the etching rate ~0.785 nm/s). The ALD-Al_2O_3 of 120 deposition cycles was deposited as gate dielectric with the following metallization of Al gate. Subsequently, the tri-layer of Au(200-nm)/Ge(70-nm)/Ni(30-nm) was deposited at the S/D region by using e-beam system and lift-off process, followed by PDA at 400 °C for 1 min to form Ohmic contact. Transmission electron microscopy (TEM) was used to characterize the capacitor and device structures; while the element depth profiles of the AuGeNi alloy were analyzed via Auger electron spectroscopy (AES) using Ar^+ ion sputtering.

For these fabricated junction and devices, current–voltage (I–V), capacitance–voltage (C–V), and conductance–voltage (G–V) characteristics were measured using a Keithley 4200 semiconductor analyzer system and an HP4284 LCR meter, respectively.

6.3 Effect of Forming Gas Annealing on Ge p-MOSFET Characteristics

6.3.1 P$^+$N Ge Junction Characteristics

Figure 6.2 displays the effects of FGA on the junction characteristics of Ge p-FETs that had been subjected to dopant activation at 500 °C. The reverse leakage current density (J_R) for the as-activated junction was 2×10^{-2} A cm^{-2} at -1 V. A gradual increase in J_R occurred for temperatures above 500 °C (not shown), possibly because of a rougher surface morphology or a smaller dopant loss [22]. We suspect that the value of J_R obtained in this case arose mainly from the contribution of the generation current, which is dependent on not only the level of substrate doping but also the extent of residual metal contamination after surface cleaning [23] or device fabrication processing. A larger resultant depletion width for a substrate having lower levels of doping and metal contamination will obviously lead to more defects—including both bulky defects in the Ge substrate and on the surface states at the isolation region—residing inside the depletion region; in turn, this phenomenon will result in a larger generation current. Because the doping level of the substrate used here was as low as 1×10^{14} cm^{-3}, we believe that, rather than metal contamination, defects arising from Ge wafer manufacturing and our employed isolation techniques were the primary culprits for the observed high leakage current [24]. Using previously reported equations for calculating the diffusion (J_{diff}) and generation (J_{gr}) current densities in a diode [14], we estimated the values of J_{diff} and J_{gr} to be ca. 2.8×10^{-4} and 1×10^{-2} A cm^{-2}, respectively, for our low-doped (10^{14} cm^{-3}) n-Ge substrate—assuming the presence of a bulk trap density (N_{T}) of 10^{15} cm^{-3} and a capture cross-section of 10^{-15} cm^{-2} [4], [26], [27]. Consistent with our experimental results, the value of J_{gr} prevailed over that of J_{diff} to dominate the junction leakage. This behavior is consistent with a recent report in which the value of J_{R} increased significantly in a Ge $\mathrm{p^{+}n}$ junction when the substrate doping was as low as ca. 10^{15} cm^{-3}, due to the enhanced rate of generation of thermally activated electron/hole pairs in the depletion layer [28]. Using a MEDICI simulator, those authors predicted this substrate dopant-level dependence of the Ge junction leakage, which was not observed in the Si counterpart. As a result, we think that the density of the defects in the Ge substrate shall be indispensably eliminated in order to obtain better electrical property of the diode.

We found that performing the FGA process mainly impacted the degree of reverse leakage and slightly enhanced the forward current of the diode. The inset to **Fig. 6.2** presents the Weibull plots of the values of J_{R} at a reverse bias (V_{R}) of –1 V. Performing FGA at a low temperature of 300 °C decreased the value of J_{R} to 10^{-2} A cm^{-2}, whereas it increased continuously to 3×10^{-2} and 10^{-1} A cm^{-2} at FGA temperatures of 350 and 400 °C, respectively. We suspect that the FGA process induced junction degradation as a result of the increased roughness around the contact hole periphery that accompanied bulk-trap generation during Al-germanide formation. Similar phenomena, either the presence of voids of different sizes [29] or metal-induced deep traps inside Ge [30], have been characterized during the formation of Ni- and Co-germanides. Scanning electron microscopy (SEM) images (not shown) did not reveal the formation of any voids after FGA at 400 °C; we did, however, observe an increase in morphological damage of the S/D metal pads, but not in the gate and channel regions.

6.3.2 Device, Reliability, and Mobility Characteristics

Several studies have demonstrated that FGA or pure H_2 annealing can result in improved high-*k*/Ge interfaces [3], [7], [31]. Using the conductance method and charge pumping measurements, we did indeed obtain a lower value of D_{it} of 8×10^{11} cm^{-2} eV^{-1} for the MOS capacitors after performing FGA at 300 °C. Hence, we anticipated that the fabricated p-FETs would exhibit enhanced performance as a result of improvements to both the p^+n junction and the dielectric interface. **Figs. 6.3(a)** and **6.3(b)** display the respective I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics of the p-FETs fabricated with and without FGA. Not surprisingly, the devices subjected to FGA at 300 °C exhibited superior performance: a higher drive current (ca. 1.8×), a better on-off current ratio (greater than three orders of magnitude), a lower leakage current, and a reduced subthreshold swing (S_S) of ca. 185 mV $decade^{-1}$.

Negative bias temperature instability (NBTI) is an important reliability issue for high-*k* dielectrics on Si, and also on Ge. **Figs. 6.4(a)–(d)** present results for device degradation in terms of changes in the values of I_{sat}, the transconductance maximum (G_m), and S_S and the V_{th} shift under NBTI stress. We applied two stress biases (–3.0 and –3.2 V) to the Ge p-FET samples. In the absence of hydrogen passivation, we detected severe electrical deterioration after applying the stress for 10^3 s, notably a value of $\Delta I_d/I_d$ of 23–35%, a value of $\Delta G_m/G_m$ of ca. 10%, rapid degradation in the value of S_S, and a large negative V_{th} shift (>250 mV). Because the mechanisms occurring during the NBTI degradation for high-*k* gate dielectrics are similar to those observed in SiO_2 [32], we suspected that subsequent FGA might aid in effectively repairing dangling bonds and defects inside the GeO_x IL, in turn boosting the dielectric quality and interfacial reliability. **Fig. 6.5** presents a plot of the extracted channel hole mobility with respect to the effective electric field, together with data reported in two previous publications [7], [33]. Our ALD-Al_2O_3/Ge p-FET exhibited superior mobility behavior over the Si hole universal curve. The peak mobility was ca. 225 cm^2 V^{-1} s^{-1}, an improvement of ca. 25%. This value is comparable with that for an NH_3-nitrided HfO_2/Ge structure, but poorer than that for a reported HfO_2/Ge structure that had been subjected to Si passivation. As a result, we believe that adopting an ultra-thin Si capping layer—the thickness of which needs optimization—should further improve the channel mobility [34], [35]. In addition, the techniques employed for deposition and Ge surface preparation are critical in determining the quality of this Si IL and the resultant improvement in mobility in the Ge devices.

6.4 Effect of Dopant Activation on N^+P Ge Junction Characteristics

6.4.1 N^+P Ge Junction Characteristics

The presence of an n^+p shallow junction having an acceptable leakage current is critical to obtaining high-performance Ge n-FETs. Previous studies of P ion implantation in Ge [36], [37] have revealed that an RTA temperature above 500 °C is essential to achieving sufficient dopant activation and full recrystallization of the amorphous Ge region. In this study, we found that an annealing temperature of 500 °C was insufficient to repair all of the implant-induced damage, as indicated in **Fig. 6.6(a)**. Raising the temperature to 700 °C decreased the value of J_R to 3.5×10^{-4} A cm^{-2}, a reduction of more than two orders of magnitude relative to the value obtained for the sample prepared at 500 °C case, even though the value of J_F had deteriorated. After capping with a 50-nm-thick SiO_2 layer, we observed an improvement (increase) in the value of J_F upon increasing the RTA temperature [**Fig. 6.6(b)**]. A difference of up to five decades was achieved between the J_F and J_R curves after RTA at 700 °C; the value of J_R was ca. 2.1×10^{-4} A cm^{-2}, close to the calculated value of J_{diff} of 1.4×10^{-4} A cm^{-2} for an ideal Ge n^+p diode. After extending the annealing time to 60 s, the value of J_R remained unchanged, irrespective of the implantation energy [30 or 60 keV; **Fig. 6.6(c)**]. In contrast, annealing for 90 s led to a severe increase in leakage, by at least one order of magnitude. We interpret these characteristic differences in terms of variations in surface resistance, with further evidence supplied by SIMS analyses and electrical measurements.

6.4.2 Phosphorous Dopant Diffusion Characteristics

Figures 6.7(a)–(c) display the respective SIMS depth profiles of the n^+p diodes discussed in Fig. 5. For the lower implantation case (2×10^{14} cm^{-2}, 30 keV) in **Fig. 6.7(a)**, annealing at 500 °C for 30 s led only to flattening in the high-concentration region without any significant junction diffusion, revealing a box-shaped chemical profile. **Fig. 6.7(b)** reveals a similar “box profile” for the higher implanted case (1×10^{15} cm^{-2}, 30 keV) after RTA at 600 °C for 30 s. Taking a close look at these two sets of results, it was clear that the P diffusion rate was much faster at a concentration level of $\geqq 1 \times 10^{19}$ cm^{-3}, indicative of concentration-enhanced inner diffusion of P in Ge [36]–[38]. In contrast, we detected no significant movement of the P dopant profile at low implantation concentrations (e.g., $< 1 \times 10^{19}$ cm^{-3}) [38]. In addition, unlike the “box profile” features observed at annealing temperatures below 600 °C, an increase in temperature to 700 °C caused strong P diffusion and resulted in a complementary error function profile. This difference correlated to the surface P dopant concentration under intrinsic or extrinsic diffusion conditions, i.e., it was dependent on the value of the so-called “intrinsic carrier concentration” (n_{in}) during activation; more details are available elsewhere [39]. Furthermore, **Fig. 6.7(c)** displays evidence for P pile-up at a distance of 20 nm from the top surface, with peak concentrations of up to $(5–7) \times 10^{19}$ cm^{-3} after SiO_2 passivation. It has been reported previously [38] that the amounts of P dopant loss were ca. 40% and >60% after RTA at 500 and 600 °C, respectively; therefore, it is very likely that severe out-diffusion occurred in our system at a temperature of 700 °C. We speculate that the resultant surface P concentration influenced the contact resistance, thereby affecting the n^+p forward junction characteristics in the samples prepared with and without a

SiO_2 capping layer.

6.4.3 Diode Resistance Analysis

To confirm our suspicions, we examined the magnitudes of the resistance components in the test structure. **Fig. 6.8(a)** displays the test structure, which allowed current transport between two metal pads within the P-implanted region. We obtained the overall contact resistance ($2R_{cont}$) by subtracting the value of the transport resistance (R_{tran}) from the total resistance (R_{total}). Here, the value of R_{total} was extracted from the slope of the measured I–V curve, while the value of R_{tran} was the product of the measured sheet resistance and the constant L/W ratio of 1.6. **Fig. 6.8(b)** summarizes our results. Upon increasing the RTA temperature (from 500 to 700 °C), a larger resistance increase (from 285 to 650 Ω), contributed mostly by the value of R_{cont}, occurred in the uncapped samples as a result of significant dopant out-diffusion. With SiO_2 capping, we observed a considerable reduction in the values of R_{total} (<270 Ω), reaching an especially low value of ca. 150 Ω after RTA at 700 °C. Therefore, we conclude that a suppressed dopant loss (and, hence, an enhanced surface active P concentration) was responsible for the resulting improved junction characteristics, even though different implantation conditions were employed in the two cases. Again, further extending the annealing time to 90 s caused a slight increase in resistance. Returning to the corresponding SIMS profile [**Fig. 6.7(c)**], we also explored the continuous surface P segregation with the deeper in-diffused junction. Its accumulation concentration already exceeded the allowed activation level of $(5–6) \times 10^{19}$ cm^{-3} in Ge, possibly forming inactive precipitates that functioned as the leakage current path [37]. We suspect that these concurrent events were responsible for the degraded junction leakage after longer annealing times, as observed in **Fig. 6.6(c)**.

6.4.4 Reverse Leakage Current Analysis

In principle, two leakage components contribute to the value of J_R in a diode, namely the perimeter current density (J_P) and the area current density (J_A), as represented schematically in the inset to **Fig. 6.9(c)**. Using Eq. (6.1), we determined the origin of the junction leakage by designing diodes having various area (A)-to-perimeter (P) ratios,

$$I_R = J_A \cdot A + J_P \cdot P \tag{6.1}$$

where J_A represents the generation-recombination centers in the depletion region as well as resulting carrier diffusion, while J_P represents the surface states existing at the isolated-oxide/substrate interface. Interestingly, **Figs. 6.9(a)** and **6.9(b)** reveal a transition for the dominant term from J_P to J_A upon changing the RTA temperature from 600 to 700 °C, presumably because RTA at 700 °C decreased the contribution of the J_P term dramatically, as indicated in the extracted results in **Fig. 6.9(c)**. In particular, for the uncapped samples we observed a reduction in J_P of three orders of magnitude, from ca. 10^{-3} to 10^{-6} A cm^{-1}; a similar decrease occurred for the value of J_P in the capped samples. This behavior indicates that high-temperature annealing decreased the surface recombination velocity at the SiO_2–Ge interface, although determining the details of the repair mechanism will require further investigation. In addition, the increase in the values of J_P for annealing times greater than 30 s provides evidence of surface perimeter leakage degradation for the longer thermal budget.

6.5 Effect of Forming Gas Annealing on Ge n-MOSFET Characteristics

Figures 6.10(a) and **6.10(b)** present the I_{ds}–V_{gs} and I_{ds}–V_{ds} curves of the Ge n-FETs before and after FGA at 300 °C, respectively. For the control sample, the on/off current ratio approximated three orders of magnitudes, with values of S_S and D_{it} of ca. 489 mV decade^{-1}

and 4.7 × 10^{12} cm^{-2} eV^{-1}, respectively. Subsequent FGA treatment decreased the value of D_{it} to 1.9 × 10^{12} cm^{-2} eV^{-1}, which was still higher than that (8 × 10^{11} cm^{-2} eV^{-1}) obtained for the p-FETs. This difference appears to correlate to the typical characteristics of an asymmetric energy distribution of D_{it}—a higher value of D_{it} exists in the upper half of the Ge bandgap [40]. From the I_{ds}–V_{ds} curves, we observed a 6.5 (±0.5)-fold enhancement in I_{sat} after performing FGA at 300 °C, due to a decrease in the value of R_{sd} from 385 to 124 Ω that was caused by decreasing the Schottky barrier height [41]. Nevertheless, the on/off ratio was degraded by only two orders of magnitude. Almost complete loss of the Ge n-FET transfer characteristics occurred in the device subjected to FGA at 400 °C (not shown here). Such acute degradation in the n-FETs, but not in the p-FETs, probably arose from the severe P dopant loss and the rougher morphology of the Al S/D metal. In other words, the negligible diffusion of the B dopant in Ge was probably the major cause of the lack of serious p-FET junction degeneration.

Figure 6.11 reveals that the extracted channel mobility in the n-FET device was lower than that in the p-FET device—and far below the published values for electron mobility [33], [42], [43]. Apart from the relatively high level of D_{it} playing a significant scattering role, the lower electron mobility in our n-FET devices most likely resulted from other two factors: (i) because of a severe E_F pinning effect, the higher value of R_{sd} limited the drive on-current capacity and, hence, the value of G_m; (ii) because the doping level of p-Ge substrate was relatively low (ca. 10^{15} cm^{-3}), more acceptor-like states could be filled to prevent efficient inversion during the operation of the n-MOS device [44]. In fact, even if Si passivation had been performed with these Ge n-FETs, the exhibited electron mobility remained far below the Si electron universal curve. Considering this issue from the viewpoint of Ge-based devices, the emerging concept of integrating InGaAs n-MOS and Ge p-MOS devices on the chip has been attracting much attention recently. From the viewpoints of material film integration and device process technology, however, understanding the bonding configuration and the role of possible intrinsic defects at the dielectric–Ge interface remains imperative, requiring either the first-principle calculations or Monte Carlo simulations.

6.6 Characteristics of GaAs n-MOSFET Characteristics

Since forming a good Ohmic contact is essential to achieve the excellent performance of D-mode GaAs nMOSFET, therefore, the AES depth profiles of alloyed Au/Ge/Ni tri-layer on GaAs were analyzed in **Figs. 6.12(a)** and **6.12(b)**, respectively. Alloying at 400 °C caused extensive interdiffusion between metal layer and GaAs substrate with respect to the as-deposited profile. Both Ge and Ni diffused onto the top surface and also interacted with GaAs severely. Further from the TEM image in **Fig. 6.13(b)**, Ni and Ge reacted with each other not only forming a NiGe compound (in the ratio of 1:1) in the upper layer but also causing pits inside the GaAs substrate. Some traces of Ga and As were also detected in the upper metal alloys. These findings showed the similar behavior to the several reported studies [45]-[47], and the reaction mechanism was also widely investigated [46], [47]. With the analysis of transfer length method (TLM), the measured specific contact resistivity was $2.9 \times 10^{-5}\ \Omega\cdot\text{cm}^2$, acting a good Ohmic contact. **Fig. 6.13(a)** shows the TEM image of the overall GaAs n-MOSFET structure. The average distance between the Al gate and the AuGeNi S/D was ca. 3 um and also the rough morphology of AuGeNi alloy was observed at the S/D region. From the zoom in picture of the Al/ALD-Al_2O_3/n-GaAs in **Fig. 6.13(c)**, the physical dielectric thickness was 12.5(±0.5) nm, which corresponded to have the CET value of 5.4 nm.

Figure 6.14(a) illustrates the I_d–V_g transfer characteristics in the linear and saturations for D-mode ALD-Al_2O_3/GaAs n-FET with $(NH_4)_2S$-C_4H_9OH interfacial passivation. For device with the gate length/width of 5/100 μm, the values of V_{th} was -3.8 V and the values of G_m at V_d = 1.1/3.1 V were 43/59 mS/mm, respectively. In addition, well saturation and pinch-off characteristics were presented in the I_d–V_d curves [**Fig. 6.14(b)**] with the gate overdrive V_g-V_{th} ranging from -1.2 to 4.8 V in steps of 1 V. The maximum I_d was 250 mA/mm measured at V_g-V_{th} = 4.8 V, V_d = 4 V. The extracted peak electron mobility was only 336 $cm^2V^{-1}s^{-1}$, higher than the value of 212 $cm^2V^{-1}s^{-1}$ for the non-sulfidized GaAs device (not shown here). But, the device properties are still not comparable to the reported performance of D-mode HfO_2/GaAs devices with α-Si interfacial passivation layer [48]. This may be correlated to a higher D_{it} still existed at the dielectric-GaAs interface. Further modulation of the ALD film deposition as well as optimization of the wet-chemical clean and PDA processes are required. Here, we want to reassert that executing the sulfidization with the solvents of lower dielectric constant, e.g., $(NH_4)_2S$ + C_4H_9OH, is relatively effective to improve the quality of GaAs surface prior to high-*k* deposition. It is also possible to implant this chemical treatment along with other passivation methods in pursuit of superior high-performance high-*k*/III-V n-MOSFET.

6.7 Conclusions

In Chapter 6, we investigated the characteristics of Ge junction diodes and gate-last p- and n-MOSFETs with the ALD-Al_2O_3 gate dielectrics. The magnitudes of the rectifying ratios for the Ge p^+n and n^+p junctions exceeded three and four orders of magnitude (in the voltage range of ±1 V), respectively, with accompanying reverse leakages of ca. 10^{-2} and 10^{-4} A cm^{-2}, respectively. It was also found that the origin of the leakage path, governed by surface perimeter or junction area, was mainly dependent on the thermal budgets adopted in devices (i.e., dopant activation and FGA). In addition, performing FGA at 300 °C boosted the device on-current, decreased the Al_2O_3/Ge interface states to 8×10^{11} cm^{-2} eV^{-1}, and improved the reliability of bias temperature-instability. The peak mobility and on/off ratio reached as high as 225 cm^2 V^{-1} s^{-1} and $>10^3$, respectively, for the p-FET (W/L = 100 μm/4 μm), while these values were less than 100 cm^2 V^{-1} s^{-1} and ca. 10^3, respectively, for the n-FET (W/L = 100 μm/9 μm). The relatively inferior n-FET performance resulted from the larger S/D contact resistance, higher surface states scattering, and lower substrate doping concentration.

In accordance with the studies of $(NH_4)_2S$-C_4H_9OH chemical passivation on GaAs substrate in Chapter 5, herein, we employed such an alcoholic sulfide treatment to fabricate the D-mode GaAs n-MOSFETs and successively demonstrated their transfer and output characteristics. The maximum I_d was 250 mA/mm measured at V_g-V_{th} = 4.8 V, V_d = 4 V. The extracted peak electron mobility was only 336 $cm^2V^{-1}s^{-1}$, indicative of the more optimization in the dielectric/GaAs interface quality. Perhaps, the $(NH_4)_2S$-C_4H_9OH treatment can be adopted on the InGaAs/InSb substrates or integrates with other passivation methods to provide the better surface quality for realizing high-performance high-k/III-V devices.

References (Chapter 6)

[1] H. Matsubara, T. Sasada, M. Takenaka, and S. Takagi, "Evidence of low interface trap density in GeO_2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation," *Appl. Phys. Lett.*, vol. **93**, p. 032104, 2008.

[2] N. Wu, Q. Zhang, D. S. H. Chan, N. Balasubramanian, and C. Zhu, "Gate-first Germanium nMOSFET with CVD HfO_2 gate dielectric and silicon surface passivation," *IEEE Electron Devices Lett.*, vol. **27**, p. 479, 2006.

[3] T. Maeda, M. Nishizawa, Y. Morita, and S. Takagi, "Role of germanium nitride interfacial layers in HfO_2/germanium nitride/germanium metal-insulator-semiconductor structures," *Appl. Phys. Lett.*, vol. **90**, p. 072911, 2007.

[4] J. Vanhellemont and E. Simoen, "Brother silicon, sister germanium," *J. Electrochem. Soc.*, vol. **154**, p. H572, 2007.

[5] E. Simoen, A. Satta, M. Meuris, T. Janssens, T. Clarysse, C. Demeurisse, B. Brijs, I. Hoflijk, W. Vandervorst, and C. Claeys, "Defect removal, dopant diffusion and activation issues in ion-implanted shallow junctions fabricated in crystalline germanium substrates," *Solid State Phenom.*, vol. **108–109**, p. 691, 2005.

[6] D. Kuzum, A. J. Pethe, T. Krishnamohan, and K. C. Saraswat, "Ge (100) and (111) n- and p-FETs with high mobility and low-T mobility characterization," *IEEE Trans. Electron Devices*, vol. **56**, p. 648, 2009.

[7] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L.-A. Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M. M. Heyns, "High performance Ge pMOS devices using a Si-compatible process flow," in *Tech. Dig. Int. Electron Device Meet.*, p. 655, 2006.

[8] H.-C. Chin, M. Zhu, Z.-C. Lee, X. Liu, K.-M. Tan, H. K. Lee, L. Shi, L.-J. Tang, C.-H. Tung, G.-Q. Lo, L.-S. Tan, and Y.-C. Yeo, "A new silane-ammonia surface passivation technology for realizing inversion-type surface-channel GaAs n-MOSFET with 160 nm

gate length and high-quality metal-gate/high-*k* dielectric stack," *Tech. Dig. Int. Electron Devices Meet.*, p. 383, 2008.

[9] N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov, R. Kambhampati, M. Yakimov, Y. Sun, P. Pianetta, C.K. Gaspe, M.B. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai, "Addressing the gate stack challenge for high mobility $In_xGa_{1-x}As$ channels for nFETs," *Tech. Dig. Int. Electron Devices Meet.*, p. 363, 2008.

[10] M. Radosavljevic, T. Ashley, A. Andreev, S. D. Coomber, G. Dewey, M. T. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, M. K. Hudait, R. Jefferies, T. Martin, R. Pillarisetty, W. Rachmady, T. Rakshit, S. J. Smith, M. J. Uren, D. J. Wallis, P. J. Wilding and R. Chau, "High-performance 40nm gate length InSb p-channel compressively strained quantum well field effect transistors for low-power (Vcc=0.5V) logic applications," *Tech. Dig. Int. Electron Devices Meet.*, p. 727, 2008.

[11] T. H. Chiang, W. C. Lee, T. D. Lin, D. Lin, K. H. Shiu, J. Kwo, W. E. Wang, W. Tsai, and M. Hong, "Approaching Fermi level unpinning in oxide-$In_{0.2}Ga_{0.8}As$," *Tech. Dig. Int. Electron Devices Meet.*, p. 375, 2008.

[12] P. D. Ye, "Main determinants for III–V metal-oxide-semiconductor field-effect transistors (invited)," *J. Vac. Sci. Technol. A.,* vol. **26**, p. 697, 2008.

[13] A. Saletes, J. Massies, and J. P. Contour, "Residual carbon and oxygen surface contamination of chemically etched GaAs (001) substrates," *Jpn. J. Appl. Phys.* vol. **25**, p. L48, 1986.

[14] S. Goto, M. Yamada, and Y. Nomura, "Surface cleaning of Si-doped/undoped GaAs substrates," *Jpn. J. Appl. Phys.* vol. **34**, p. L1180, 1995.

[15] F. Zhu, H. Zhao, I. Ok, H. S. Kim, J. Yum, J. C. Lee, N. Goel, W. Tsai, C. K. Gaspe, and M. B. Santos, "Effects of anneal and silicon interface passivation layer thickness on device characteristics of $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors," *Electrochem. Solid-State Lett.*, vol. **12**, p. H131, 2009.

[16] H.-C. Chin, M. Zhu, G. S. Samudra, and Y.-C. Yeo, "n-channel GaAs MOSFET with TaN/HfAlO gate stack formed using in situ vacuum anneal and silane passivation," *J. Electrochem. Soc.*, vol. **155**, p. H464, 2008.

[17] H.-C. Chin, M. Zhu, X. Liu, H.-K. Lee, L. Shi, L.-S. Tan, and Y.-C. Yeo, "Silane–ammonia surface passivation for gallium arsenide surface-channel n-MOSFET," *IEEE Electron Device Lett.*, vol. **30**, p. 110, 2009.

[18] C.-C. Cheng, C.-H. Chien, G.-L. Luo, C.-H. Yang, C.-K. Tseng, H.-C. Chiang, and C.-Y. Chang, "Improved electrical properties of Gd_2O_3/GaAs capacitor with modified wet-chemical clean and sulfidization procedures," *J. Electrochem. Soc.*, vol. **155**, p. G56, 2008.

[19] F. Bellenger, M. Houssa, A. Delabie, V. Afanasiev, T. Conard, M. Caymax, M. Meuris, K. D. Meyer, and M. M. Heyns, "Passivation of Ge(100)/GeO_2/high-*k* gate stacks using thermal oxide treatments," *J. Electrochem. Soc.*, vol. **155**, p. G33, 2008.

[20] M. S.-Mathur, Y.-C. Perng, J. Lu, H.-O. Blom, J. Bargar, and J. P. Chang, "The effect of aluminum oxide incorporation on the material and electrical properties of hafnium on Ge," *Appl. Phys. Lett.*, vol. **93**, p. 233501, 2008.

[21] J. J.-H. Chen, N. A. Bojarczuk, J. H. Shang, M. Copel, J. B. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, "Ultrathin Al_2O_3 and HfO_2 gate dielectrics on surface-nitrided Ge," *IEEE Trans. Electron Devices*, vol. **51**, p. 1441, 2004.

[22] Y. Kamata, Y. Kamimuta, T. Ino, R. Iijima, M. Koyama, and A. Nishiyama, "Influences of annealing temperature on characteristics of Ge p-channel metal oxide semiconductor field effect transistors with ZrO_2 gate dielectrics," *Jpn. J. Appl. Phys.*, vol. **45**, p. 5651, 2006.

[23] Y. Kamata, T. Ino, M. Koyama, and A. Nishiyama, "Improvement in *C–V* characteristics of Ge metal-oxide semiconductor capacitor by H_2O_2 incorporated HCl pretreatment," *Appl. Phys. Lett.*, vol. **92**, p. 063512, 2008.

[24] A. Satta, G. Nicholas, E. Simoen, M. Houssa, A. Dimoulas, B. D. Jaeger, J. V. Steenbergen, and M. Meuris, “Impact of germanium surface passivation on the leakage current of shallow planar p–n junctions,” *Mater. Sci. Semi. Proc.*, vol. **9**, p. 716, 2006.

[25] E. Simoen, S. Sonde, C. Claeys, A. Satta, B. De Jaeger, R. Todi, and M. Meuris, “Processing factors impacting the leakage current and flicker noise of germanium p$^+$n junctions on silicon substrates,” *J. Electrochem. Soc.*, vol. **155**, p. H145, 2008.

[26] P. Batude, X. Garros, L. Clavelier, C. Le Royer, J. M. Hartmann, V. Loup, P. Besson, L. Vandroux, Y. Campidelli, S. Deleonibus, and F. Boulanger, “Insights on fundamental mechanisms impacting Ge metal oxide semiconductor capacitors with high-*k*/metal gate stacks,” *J. Appl. Phys.*, vol. **102**, p. 034514, 2007.

[27] E. Simoen, C. Claeys, S. Sioncke, J. V. Steenbergen, M. Meuris, S. Forment, J. Vanhellemont, P. Clauws, and A. Theuwis, “Lifetime and leakage current considerations in metal-doped germanium,” *J. Mater. Sci.: Mater. Electron.*, vol. **18**, p. 799, 2007.

[28] G. Eneman, M. Wiot, A. Brugère, O. S. I. Casain, S. Sonde, D. P. Brunco, B. D. Jaeger, A. Satta, G. Hellings, K. D. Meyer, C. Claeys, M. Meuris, M. M. Heyns, and E. Simoen, “Impact of donor concentration, electric field, and temperature effects on the leakage current in germanium p$^+$/n junctions,” *IEEE Trans. Electron Devices*, vol. **55**, p. 2287, 2008.

[29] D. P. Brunco, K. Opsomer, B. D. Jaeger, G. Winderickx, K. Verheyden, and M. Meuris, “Observation and suppression of nickel germanide overgrowth on germanium substrates with patterned SiO$_2$ structures,” *Electrochem. Solid-State Lett.*, vol. **11**, p. H39, 2008.

[30] K. Opsomer, E. Simoen, C. Claeys, K. Maex, C. Detavernier, R. L. V. Meirhaeghe, S. Forment, and P. Clauws, “A deep-level transient spectroscopy study of Co- and Ni-germanided n-type germanium,” *Mater. Sci. Semi. Proc.*, vol. **9**, p. 554, 2006.

[31] C.-C. Cheng, C.-H. Chien, G.-L. Luo, J.-C. Liu, C.-C. Kei, D.-R. Liu, C.-N. Hsiao, C.-H.

Yang, and C.-Y. Chang, “Characteristics of atomic-layer-deposited Al_2O_3 high-k dielectric films grown on Ge substrates,” *J. Electrochem. Soc.*, vol. **155**, p. G203, 2008.

[32] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F.Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, “Review on high-κ dielectrics reliability issues,” *IEEE Trans. Device Mater. Rel.*, vol. **5**, p. 5, 2005.

[33] N. Wu, Q. Zhang, N. Balasubramanian, D. S. H. Chan, and C. Zhu, “Characteristics of self-aligned gate-first Ge p- and n-channel MOSFETs using CVD HfO_2 gate dielectric and Si surface passivation,” *IEEE Trans. Electron Devices*, vol. **54**, p. 733, 2007.

[34] N. Taoka, M. Harada, Y. Yamashita, T. Yamamoto, N. Sugiyama, and S.-I. Takagi, “Effects of Si passivation on Ge metal-insulator-semiconductor interface properties and inversion-layer hole mobility,” *Appl. Phys. Lett.*, vol. **92**, p. 113511, 2008.

[35] D. P. Brunco, B. D. Jaeger, G. Eneman, A. Satta, V. Terzieva, L. Souriau, F. E. Leys, G. Pourtois, M. Houssa, K. Opsomer, *et al.*, “Germanium: the past and possibly a future material for microelectronics,” *ECS Trans.*, vol. **11**, p. 479, 2007.

[36] M. Posselt, B. Schmidt, W. Anwand, R. Grotzschel, V. Heera, A. Mucklich, C. Wundisch, W. Skorupa, H. Hortenbach, S. Gennaro *et al.*, “P implantation into preamorphized germanium and subsequent annealing: solid phase epitaxial regrowth, P diffusion, and activation,” *J. Vac. Sci. Technol. B,* vol. **26**, p. 430, 2008.

[37] A. Satta, E. Simoen, R. Duffy, T. Janssens, T. Clarysse, A. Benedetti, M. Meuris, and W. Vandervorst, “Diffusion, activation, and recrystallization of high dose P implants in Ge,” *Appl. Phys. Lett.*, vol. **88**, p. 162118, 2006.

[38] A. Satta, T. Janssens, T. Clarysse, E. Simoen, M. Meuris, A. Benedetti, I. Hoflijk, B. D. Jaeger, C. Demeurisse, and W. Vandervorst, “P implantation doping of Ge: diffusion, activation, and recrystallization,” *J. Vac. Sci. Technol. B,* vol. **24**, p. 494, 2006.

[39] S. Brotzmann and H. Bracht, “Intrinsic and extrinsic diffusion of phosphorus, arsenic, and antimony in germanium,” *J. Appl. Phys.*, vol. **103**, p. 033508, 2008.

[40] R. Xie, N. Wu, C. Shen, and C. Zhu, "Energy distribution of interface traps in germanium metal-oxide-semiconductor field effect transistors with HfO_2 gate dielectric and its impact on mobility," *Appl. Phys. Lett.*, vol. **93**, p. 083510, 2008.

[41] M. Kobayashi, A. Kinoshita, K. Saraswat, H.-S. P. Wong, and Y. Nishi, "Fermi-level depinning in metal/Ge Schottky junction and its application to metal source/drain NMOSFET," *Tech. Dig. VLSI Symp.*, p. 54, 2008.

[42] Q. Zhang, J. Huang, N. Wu, G. Chen, M. Hong, L. K. Bera, and C. Zhu, "Drive-current enhancement in Ge n-channel MOSFET using laser annealing for source/drain activation," *IEEE Electron Devices Lett.*, vol. **27**, p. 728, 2006.

[43] S. J. Whang, S. J. Lee, F. Gao, N. Wu, C. X. Zhu, J. S. Pan, L. J. Tang, and D. L. Kwong, "Germanium p- & n-MOSFETs fabricated with novel surface passivation (plasma-PH_3 and thin AlN) and TaN/HfO_2 gate stack," *Tech. Dig. Int. Electron Device Meet.*, p. 307, 2004.

[44] A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E. K. Evangelou, "Fermi-level pinning and charge neutrality level in germanium," *Appl. Phys. Lett.*, vol. **89**, p. 252110, 2006.

[45] L. David, B. Kovacs, I. Mojzes, B. Pecz, and J. Labar, "Electrical and microstructure analysis of Ni/Ge/n-GaAs interface," *Thin Solid Films*, vol. **323**, p. 212, 1998.

[46] H. R. Kawata, T. Oku, A. Otsuki, and M. Murakami, "NiGe-based ohmic contacts to n-type GaAs. II. Effects of Au addition," *J. Appl. Phys.* vol. **75**, p. 2530, 1994.

[47] H. S. Lee, M. W. Cole, R. T. Lareau, S. N. Schauer, D. C. Fox, D. W. Eckart, R. P. Moerkirk, W. H. Chang, K. A. Jones, S. Elagoz, W. Vavra, and R. Clarke, "The microstructure and electrical properties of nonalloyed epitaxial Au-Ge ohmic contacts to n-GaAs," *J. Appl. Phys.* vol. **72**, p. 4773, 1992.

[48] F. Zhu, S. Koveshnikov, I. Ok, H. S. Kim, M. Zhang, T. Lee, G. Thareja, L. Yu, J. C. Lee, W. Tsai, V. Tokranov, M. Yakimov, and S. Oktyabrsky, "Depletion-mode GaAs metal-oxide-semiconductor field-effect transistor with amorphous silicon interface

passivation layer and thin HfO_2 gate oxide," *Appl. Phys. Lett.* vol. **91**, p. 043507, 2007.

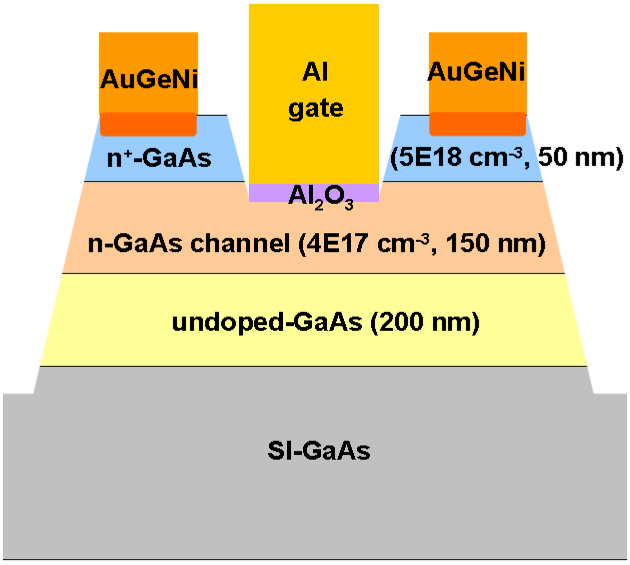


Fig. 6.1 Scheme of the depletion-mode GaAs n-MOSFET structure.

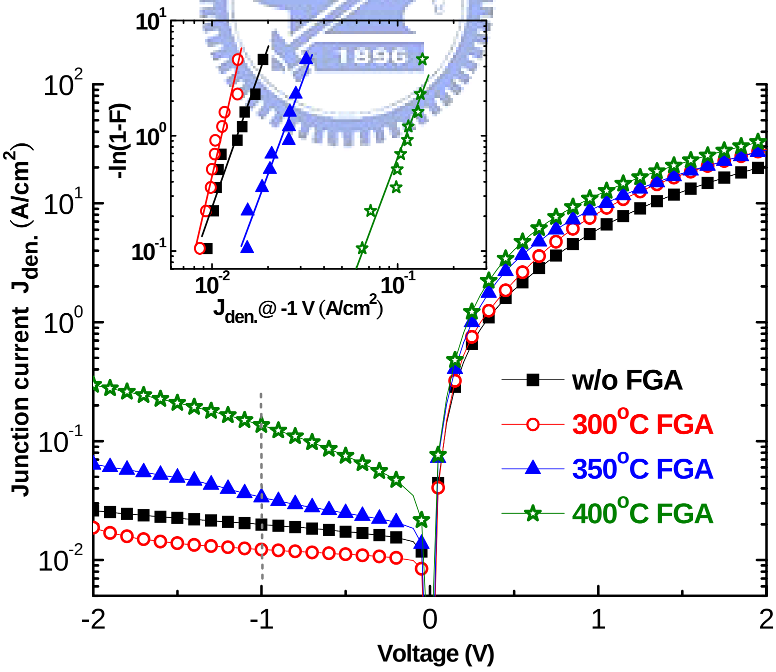


Fig. 6.2 *I*–*V* characteristics of p^+n junctions activated at 500 °C, before and after performing FGA. Inset: Weibull plot of the value of J_R at $V_R = -1$ V.

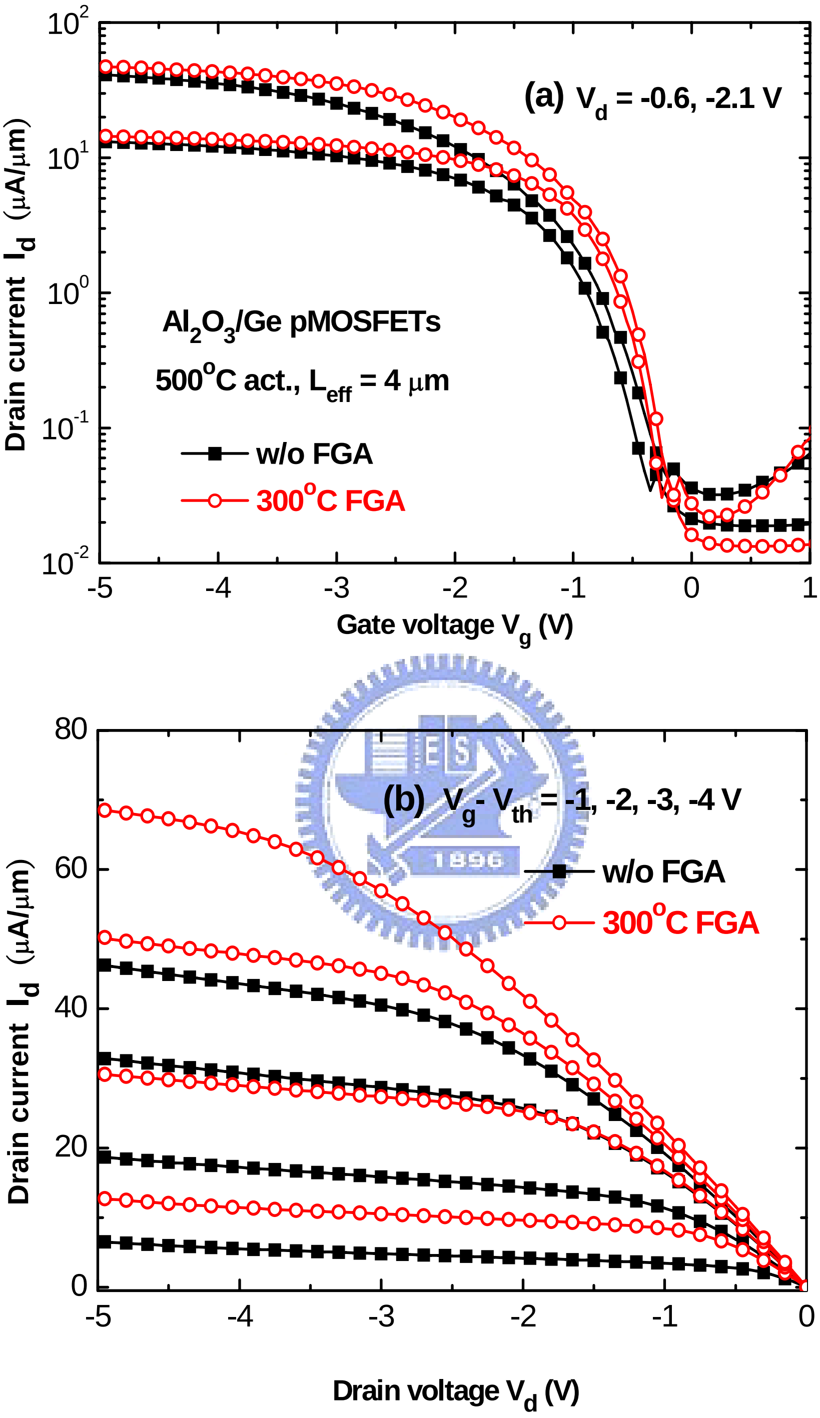


Fig. 6.3 Effects of FGA at 300 °C on the (a) I_{ds}–V_{gs} and (b) I_{ds}–V_{ds} characteristics of ALD-Al$_2$O$_3$/Ge p-FETs (W/L = 100 μm/4 μm).

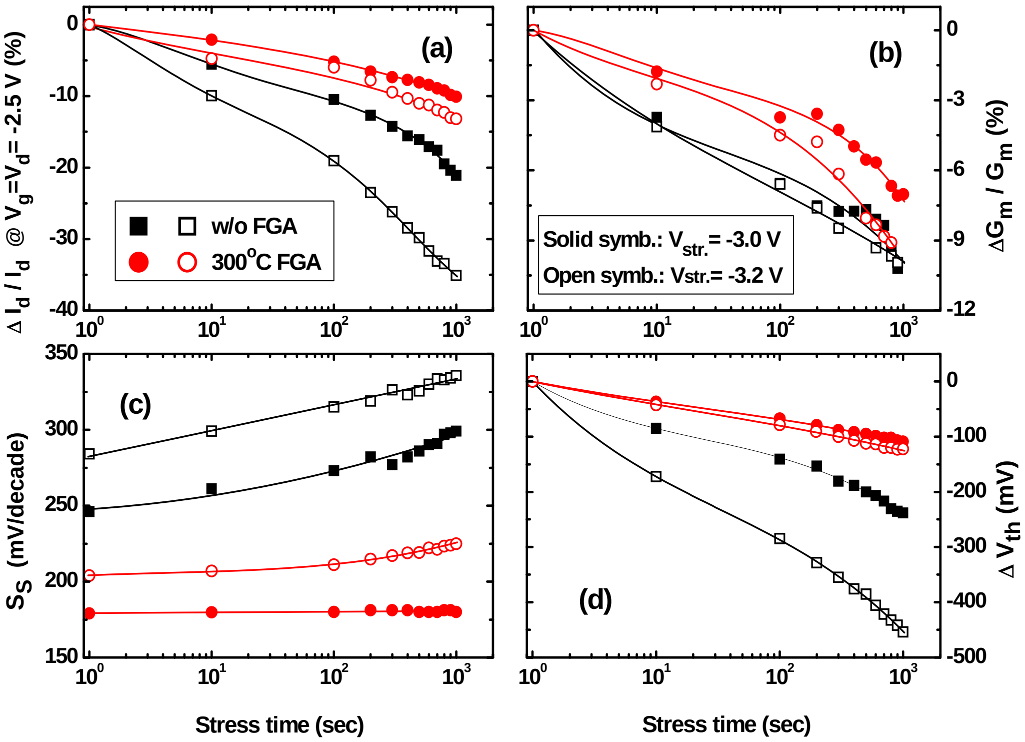


Fig. 6.4 NBTI characteristics of ALD-Al_2O_3/Ge p-FETs prepared with and without FGA at 300 °C.

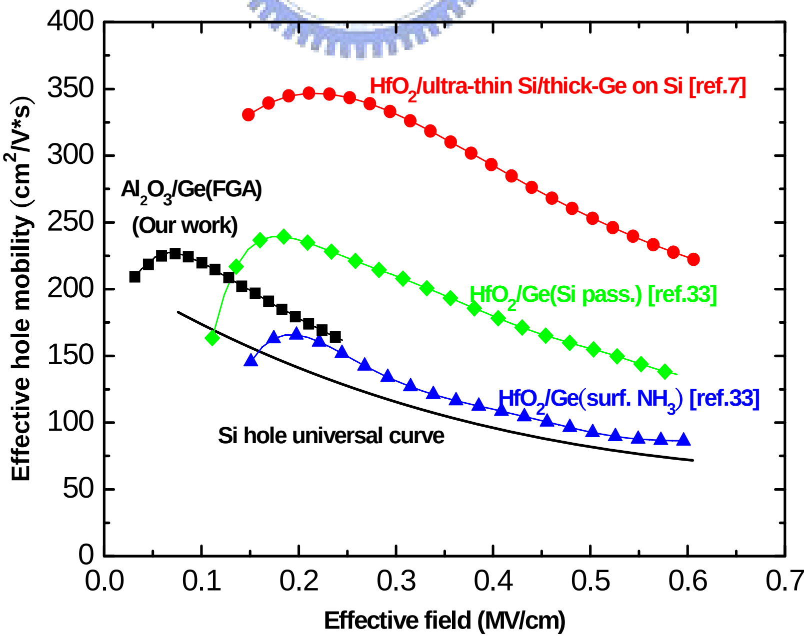


Fig. 6.5 Effective hole mobility of ALD-Al_2O_3/Ge p-FETs plotted with respect to the effective field; published mobility data are also presented [7], [33].

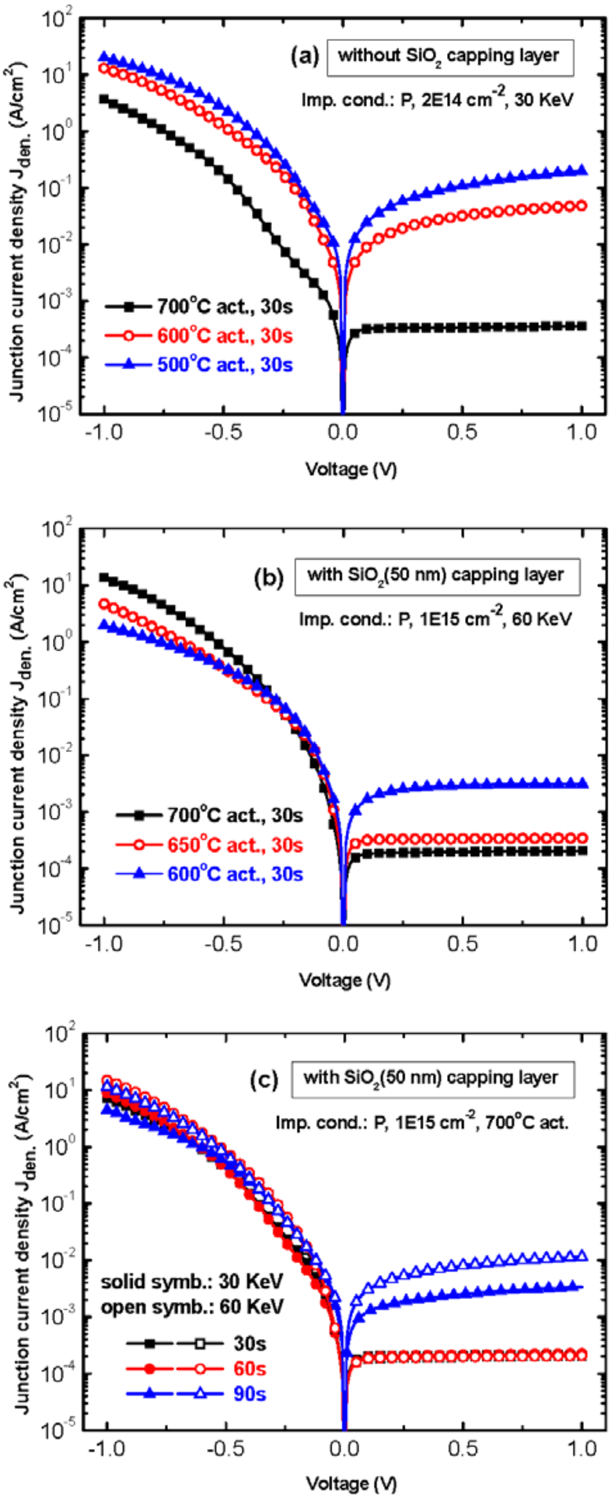


Fig. 6.6 Effects of activation conditions and SiO$_2$ capping layer on the n$^+$p junction characteristics: (a) 500–700 °C, 30 s, without SiO$_2$; (b) 600–700 °C, 30 s, with SiO$_2$; (c) 700 °C, 30–90 s, with SiO$_2$.

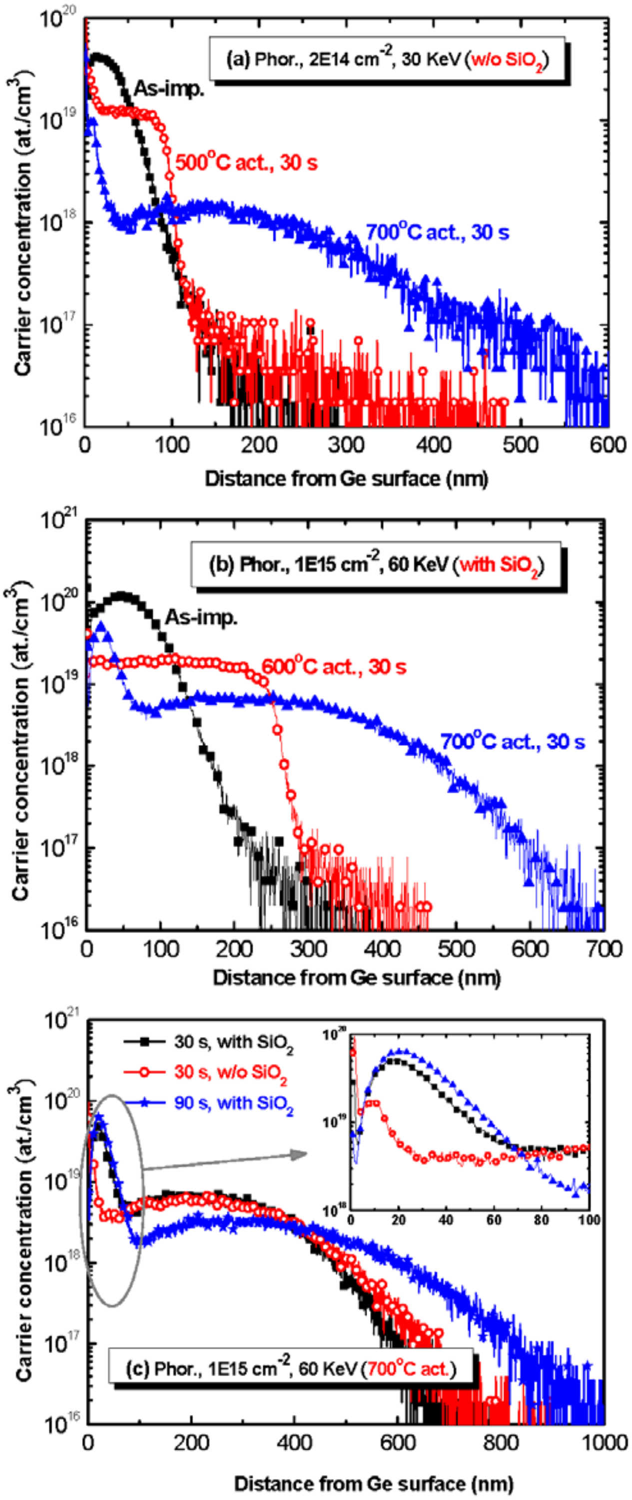


Fig. 6.7 SIMS depth profiles of the P-implanted Ge junctions discussed in Fig. 5: (a) 500–700 °C, without SiO$_2$; (b) 600–700 °C, with SiO$_2$; (c) 30–90 s, with and without SiO$_2$. Inset: Expanded image of the SIMS profile at the surface region (<100 nm).

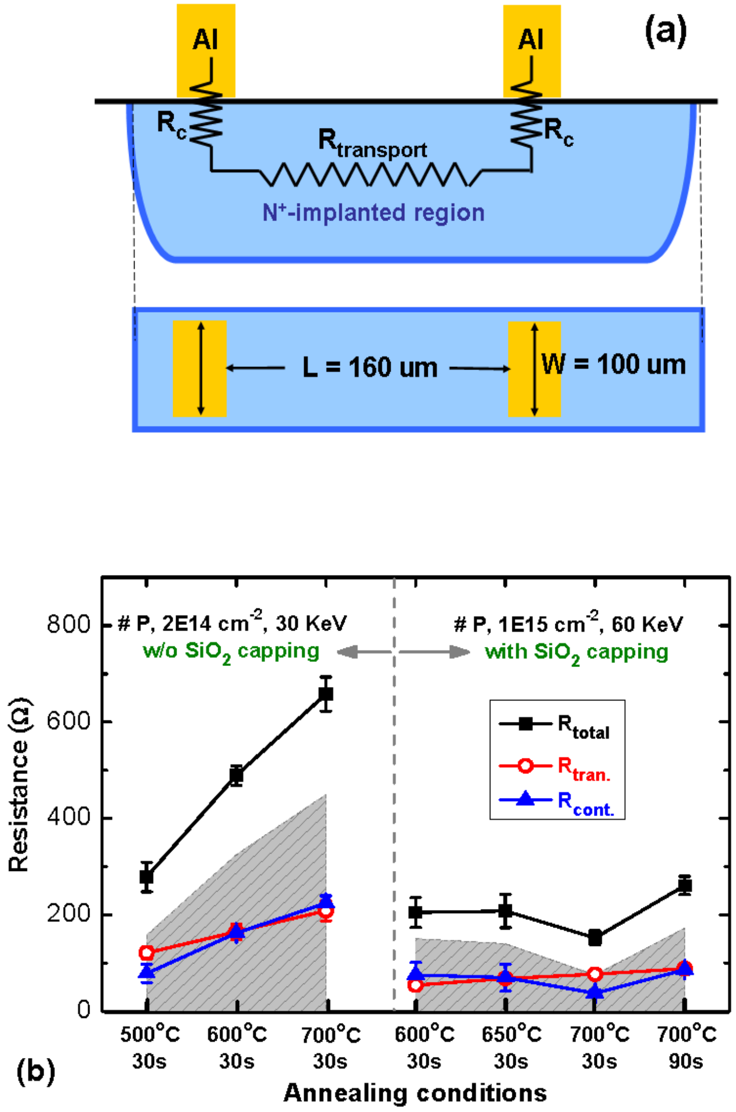


Fig. 6.8 (a) Schematic representation of the contact and transport resistances between two Al metal pads within the same P-implanted region. (b) Extraction of the values of R_{total}, R_{tran}, and R_{cont} under various activation conditions and SiO_2 capping effects. The gray region labels are values equal to two times the respective values of R_{cont} (i.e., $2R_{\text{cont}}$).

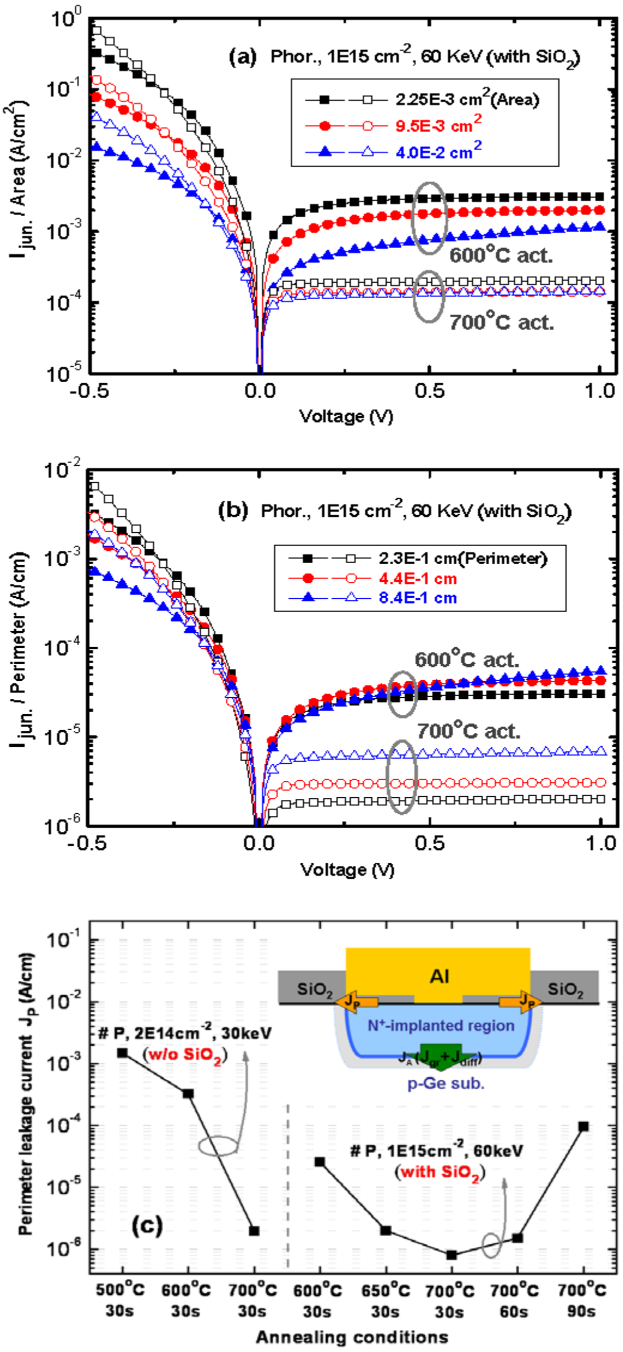


Fig. 6.9 Characteristics of n$^+$p junction currents normalized by the (a) diode area and (b) diode perimeter. (c) Extraction of the perimeter leakage component J_p as functions of the activation conditions and SiO$_2$ capping effects. Inset: Schematic representation of the two main leakage paths (J_p and J_A) at the S/D contact region; J_A comprises the generation-recombination current (J_{gr}) and diffusion current (J_{diff}).

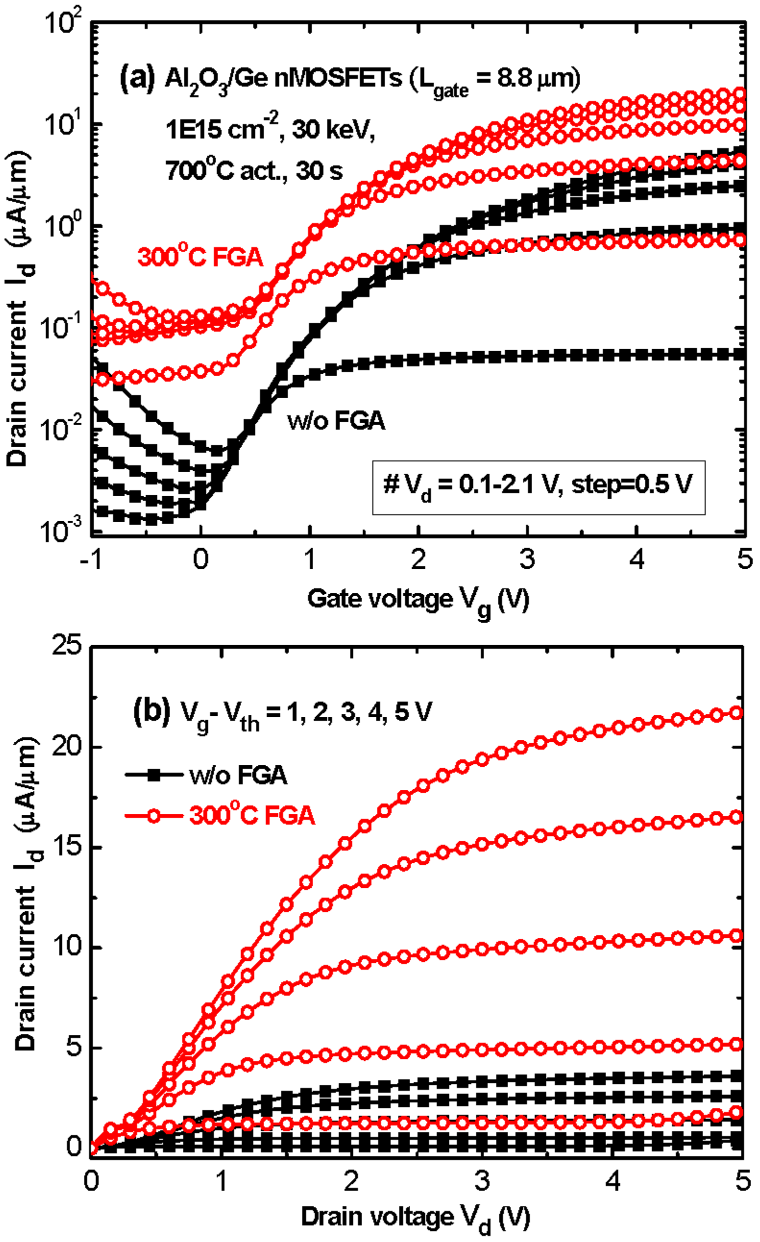


Fig. 6.10 Effects of FGA at 300 °C on the (a) I_{ds}–V_{gs} and (b) I_{ds}–V_{ds} characteristics of ALD-Al_2O_3/Ge n-FETs (W/L = 100 μm/8.8 μm).

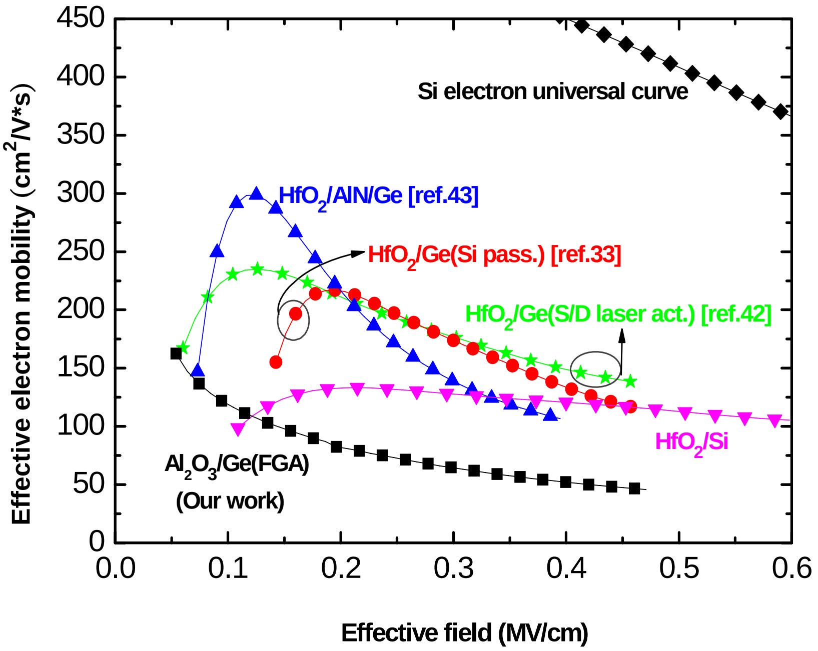


Fig. 6.11 Effective electron mobility of ALD-Al_2O_3/Ge n-FETs plotted with respect to the effective field; published mobility data are also presented [33], [42], [43].

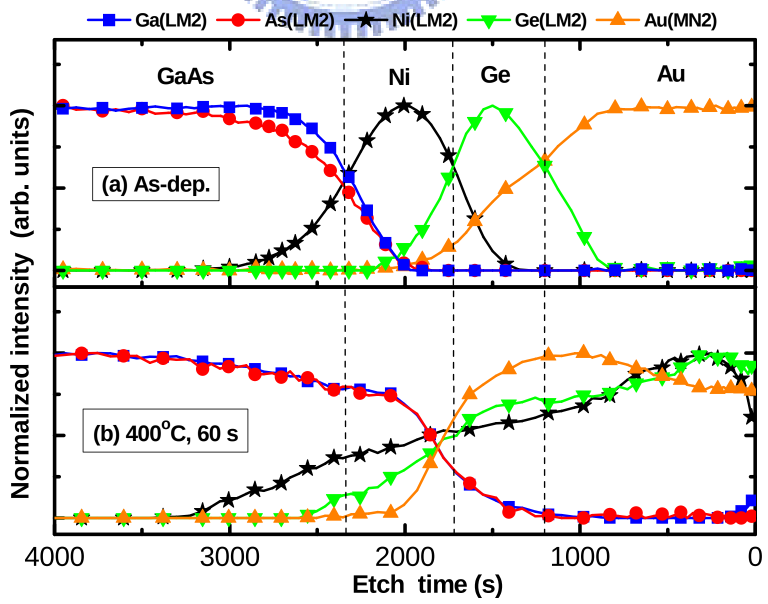


Fig. 6.12 AES depth profiles of the Au/Ge/Ni S/D Ohmic contact (a) before and (b) after 400 °C for 1 min, respectively.

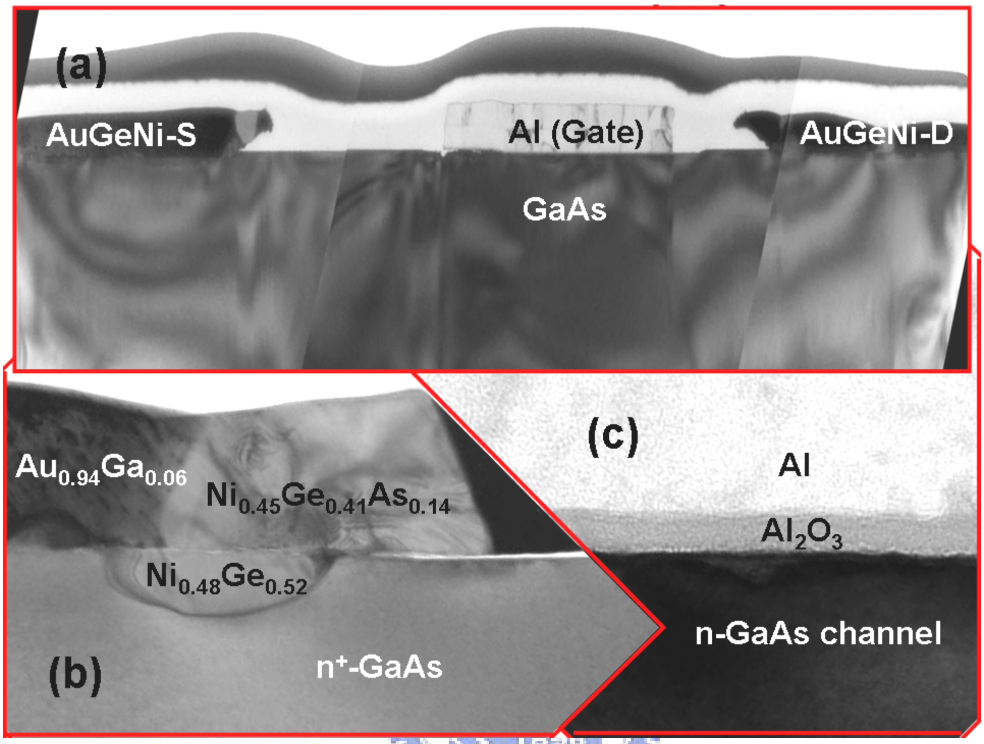


Fig. 6.13 TEM images of (a) the D-mode GaAs n-MOSFET structure; (b) alloyed Ni/Ge/Au S/D Ohmic contact after 400 °C for 1 min; (c) Al/ALD-Al_2O_3/GaAs channel, respectively.

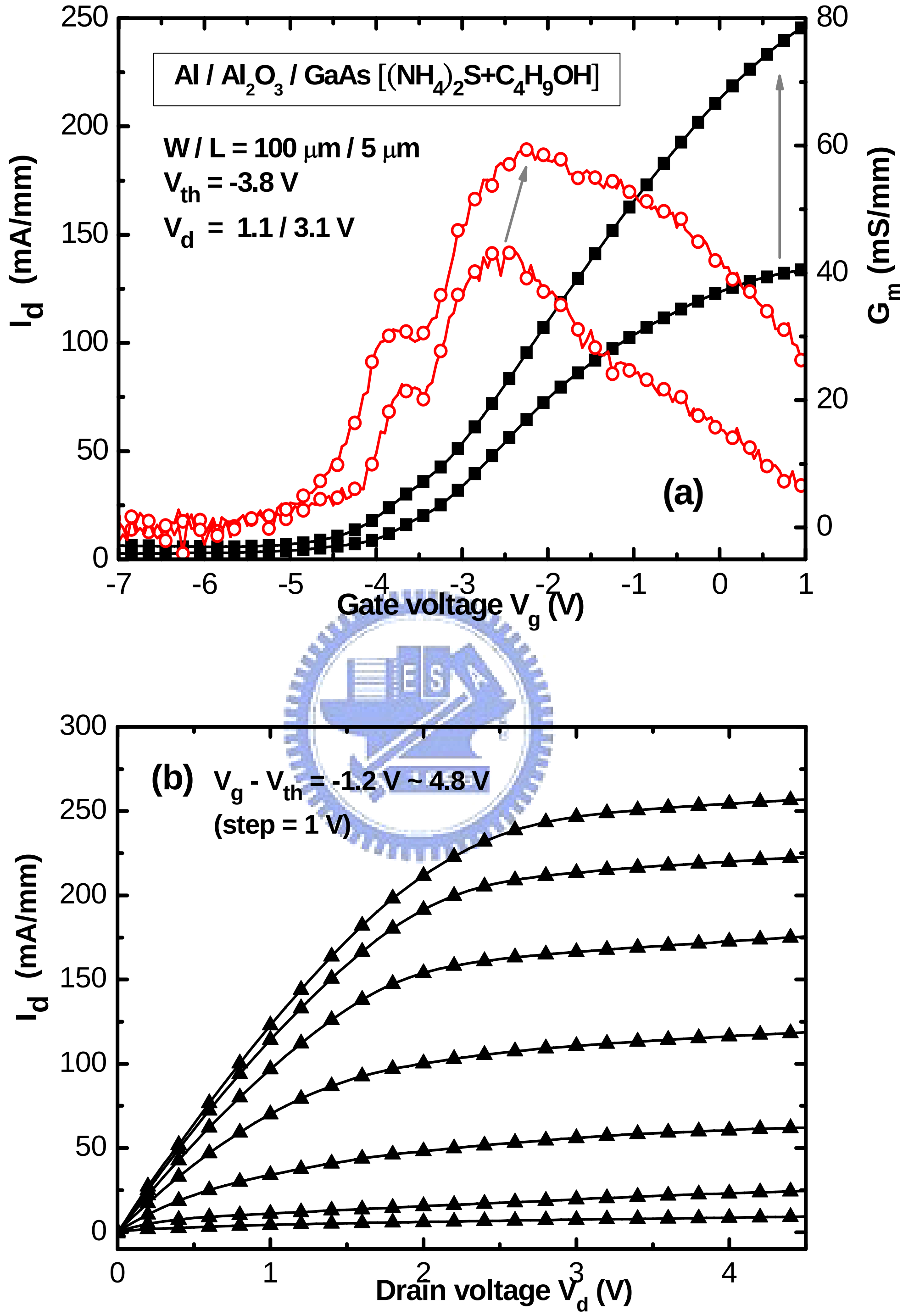


Fig. 6.14 (a) I_d–V_g and (b) I_d–V_d characteristics of the D-mode ALD-Al_2O_3/GaAs n-MOSFET with $(NH_4)_2S$-C_4H_9OH chemical treatment, respectively.

Chapter 7

Conclusions and Suggestions for Future Work

7.1 Conclusions of this study

In this thesis, we have studied the deposition of various high-*k* dielectric films, including HfO_xN_y, Al_2O_3, and Gd_2O_3, onto the bulk Ge and GaAs substrates and systematically investigated their capacitor and device characteristics. We first adopted two surface passivation methods—the NH_3 plasma and the Si_2H_6 thermal annealing—to improve the high-*k*/Ge capacitor characteristics, while also deeply examined the effects of $(NH_4)_2S$ chemical treatment on the electrical improvements of high-*k*/GaAs MOS capacitors. In the following, various kinds of thermal processing, like post-deposition annealing (PDA), post-metallization annealing (PMA), and forming-gas annealing (FGA), were employed to further improve the Ge and GaAs device properties. Finally, we also successively demonstrated the characteristics of inversion-mode Ge p- and n-MOSFETs and depletion-mode GaAs n-MOSFET with the atomic-layer-deposited Al_2O_3 gate dielectrics, respectively. Herein, we summarized the experimental results as follows:

For the HfO_xN_y sputtered films on Ge substrates, we observed a U-shaped distribution of Ge atoms into the overlying HfO_xN_y dielectric and an increased Ge incorporation (>17 at.%) after higher thermal processing. Although high-temperature annealing did improve the interface qualities, they also caused a positive shift of the V_{FB}, severe charge trapping, and increased gate leakage current (J_g) considerably; which are closely related to the existence of GeO_x defective layer and the degree of resultant GeO desorption. These problems could be relieved after performing NH_3 plasma pretreatment on the Ge surface; in particular, suppressing the amount of Ge incorporation (<5 at.%) and the sub-stoichiometric oxide at dielectric-substrate interface. Evidently, capping the Ge substrate with an ultrathin Si layer also efficiently inhibited the incorporation of Ge into the HfO_xN_y bulk dielectric, thereby diminishing the oxide charge trapping. We suggested that both surface nitridation and Si capping processes actually diminished the volatilization of gaseous GeO and enhanced the thermal stability of the high-*k*/Ge interface.

Next, we employed the ALD system to deposit the Al_2O_3 thin films on Ge over the wide deposition temperatures. Physical analyses revealed that an increase in the deposition temperature can enhance the Al_2O_3 film density and its dielectric stoichiometry, but temperatures above 200 °C led to formation of a $Ge_xAl_{1-x}O$ intermediate layer, which in turn caused an increasing J_g and a higher interface state density (D_{it}, $>10^{13}$ cm^{-2} eV^{-1}). Furthermore, although N_2 RTA at 600 °C abated the resultant oxygen-excessive behavior, i.e., providing a more stoichiometric film, interfacial GeO_x volatilization still caused the greater electrical degradation. In contrast, FGA at 300 °C improved the $Pt/Al_2O_3/Ge$ capacitor properties, including lower values of D_{it} (ca. 6×10^{11} cm^{-2} eV^{-1}) and J_g and reduced hysteresis width. Interestingly, we attempted to explore the minority-carrier response behavior of Ge MOS capacitors through MEDICI simulations and device experiments, and further compare their electrical differences with those in traditional Si MOS capacitors. The plot of the Arrhenius-dependent substrate conductance (G_{sub}) indicated a larger energy loss occurring in Ge than in Si by at least four orders of magnitude, corresponding to the fast minority-carrier response rate. All experimental findings showed almost consistent with the MEDICI prediction. We validated that a high value of intrinsic carrier concentration (n_i) in Ge, via the bulk-trap generation/recombination as well as the diffusion from the bulk substrate, caused the onset of low frequency capacitance-voltage (*C*-*V*) curves in the kHz regime and the gate-independent inversion conductance. From the conductance-voltage (*G*-*V*) characteristics, the density of the bulk trap was estimated to be ca. (2–4) × 10^{15} cm^{-3} in the low-doped Ge.

Another main topic in the thesis is the understanding of modified wet-chemical clean and $(NH_4)_2S$ treatment on the electrical characteristics of the high-*k*/GaAs structures. It was found that employing the NH_4OH alkaline solution and then $(NH_4)_2S$-H_2O passivation at 80 °C suppressed the formation of GaAs native oxides and elemental As coverage close to dielectric interface, thereby improving the electrical performance. The higher oxide capacitance with reduced *C*-*V* frequency dispersion was shown, which was a direct evidence of abating the “Fermi level (E_f) pinning” effect; also, the diminutive hysteresis (<100 mV) was achieved. Here, the fabricated Gd_2O_3/GaAs capacitor after the optimized sulfidization processes can exhibit the J_g of ca. 1.5 × 10^{-5} A/cm^2 @ $V_g = (V_{FB} + 1)$ V with the CET of ca. 20 Å, which was comparable to the report of high-performance HfO_2/GaAs system with an ultrathin Si/Ge interfacial layer. We suspected that the inhibited formation of elemental As and native oxides at high-*k*/sulfur-passivated GaAs interface were responsible for these electrical improvements.

Also, the well-established ALD-Al_2O_3 dielectric films were deposited on the sulfidized GaAs substrates to investigate the interface and capacitor properties. In accordance, the sulfidized Al_2O_3/GaAs capacitors can display the higher oxide capacitances, smaller frequency dispersions, decreased hysteresis widths, reduced interfacial state densities, and smaller gate leakages, respectively. Moreover, a higher electrical improvement was observed by replacing sulfidizing solvent from H_2O to C_4H_9OH; a significant reduction of elemental As and AsO_x surface species was indeed characterized with an increasing sulfur bonds on GaAs substrate. For the Al_2O_3/GaAs capacitors undergoing thermal annealing processes, the use of an O_2 ambient, relative to N_2, was found to densify the Al_2O_3 thin film further, alleviate charge trapping, and decrease the amount of metallic As generated, thereby enhancing the dielectric reliability. We have clarified these phenomena in terms of identifying the latent thermochemical mechanisms. On the other hand, we also noticed another interesting feature that the ALD-Al_2O_3 film deposited at 300 °C relative to that at 100 °C showed the nearly four orders of magnitude reduction in J_g at the CET of 40 Å; this finding is opposed to the advantages of low-temperature ALD-Al_2O_3 films on Ge substrates.

Accompanying above these experiences in high-*k*/Ge capacitors, we successively demonstrated the device characteristics of the inversion-mode Ge p- and n-FETs featuring ALD-Al_2O_3 gate dielectrics. The peak mobility and on/off ratio reached as high as 225 $cm^2\ V^{-1}\ s^{-1}$ and $>10^3$, respectively, for the p-FET (W/L = 100 μm/4 μm), while these values were less than 100 $cm^2\ V^{-1}\ s^{-1}$ and ca. 10^3, respectively, for the n-FET (W/L = 100 μm/9 μm). The inferior device performance of the n-FETs, relative to the p-FETs, correlated mainly to the greater source/drain (S/D) contact resistance, the higher value of D_{it} scattering, and the lower level of substrate doping. Moreover, subsequently performing FGA at 300 °C enhanced the driving on-current, decreased the density of Al_2O_3–Ge interface states, and improved the negative bias temperature instability (NBTI) reliability. A higher FGA temperature of 400 °C led to a dramatic increase in the off current of the n-FET as a result of severe out-diffusion of the P dopant. Herein, we also examined that the dominance of the surface perimeter leakage or junction area leakage in Ge reverse n^+p junctions was dependent mainly on the thermal processing adopted in devices (i.e., dopant activation and FGA). On the other hand, we also presented the transfer and output characteristics of depletion-mode ALD-Al_2O_3/GaAs n-MOSFET accompanying the $(NH_4)_2S$-C_4H_9OH chemical passivation. The maximum I_d was 250 mA/mm measured at V_g–V_{th} = 4.8 V, V_d = 4 V. However, the extracted peak electron mobility was only 336 $cm^2V^{-1}s^{-1}$, indicating that optimization of the dielectric/GaAs interface was still required. Even so, it is still possible that the $(NH_4)_2S$-C_4H_9OH treatment with the process optimization can be adopted onto the InGaAs or InSb substrates or integrates with other passivation methods to provide the better surface quality for realizing high-performance high-*k*/III-V devices.

7.2 Suggestions for Future Work

In terms of our experimental observations and several reported studies, it is concluded that the characteristic of an asymmetric energy distribution of D_{it}, which is higher in the upper half of the Ge bandgap, causes the device degradation of Ge n-FET. Even to date, the best records of peak electron mobility are ca. 400 and 550 $\mathrm{cm^2V^{-1}s^{-1}}$ for the respective (100) and (111) n-FETs, but, these results are still below the Si universal curves (ca. 600 $\mathrm{cm^2V^{-1}s^{-1}}$) at the effective field of 0.1 MV/cm. By contrast, as high as 2–3 times improvement is characterized in mobility characteristic of Ge p-FET. In consequence, it seems to be indispensable to search a new n-FET candidate and probably III-V materials having much higher electron mobility are the suitable selection. It is suggested that such an emerging concept of combining Ge p-MOS and (In)GaAs (or other III-V) n-MOS devices on the same chip, perhaps, is the practical strategy in the prospect of the CMOS future. Of course, this novel technique brings several challenges from the viewpoints of material film integration and device process technology. Therefore, we adumbrate that the heteroepitaxy of high-quality and dislocation-free Ge and III-V materials on the conventional Si platform is worthy to study in future work.

On the other hand, the intrinsic issues of the smaller density of states (DOS) and lower solid solubility of n-type dopant in III-V-based devices also can be relieved by studying the topic of the IV/III-V heteroepitaxy. This is because that the epitaxial structure of the III-V channel MOSFET having the IV-group S/D is capable of tackling the resistance problem and hence boosting the current drive capability. Such a nanoscale MOSFET integrates the advantages of III-V n-channel with higher electron mobility and thermal velocity, and the advantages of IV-group S/D with higher DOS and n-type dopant concentration. Moreover, the IV-group S/D can facilitate the integration of silicide and germanide technologies to reduce the resistance effect further. For example, the lattice-matched Ge/GaAs epitaxial system is the excellent and promising candidate; in addition, the SiGe S/D provides the tensile strain within the GaAs channel, further assisting to enhance the driving current. It is believed that these research topics in the heteroepitaxy technique and device fabrication are worthy of more detailed investigation.

簡　歷

姓　　名：鄭兆欽

性　　別：男

出生年月日：民國 70 年 1 月 8 日

籍　　貫：台灣省台南市

住　　址：台南市中區青年路53號

學　　歷：

私立長庚大學電子工程學系學士	**(88.09 – 92.06)**
國立交通大學電子研究所碩士班	**(92.09 – 94.06)**
國立交通大學電子研究所博士班	**(94.09 – 98.06)**

碩士論文題目：

含鉿之閘極介電層於鍺基板之電物性研究

The Electrical and Material Characterization of Hafnium-family Gate Dielectric on Ge Substrate

博士論文題目：

研究半導體和高介電絕緣體之介面以獲得高性能之鍺及三五族金氧半場效電晶體

Improvement of High Dielectric Materials and Semiconductor-Insulator Interfaces for Ge and III-V High Performance MOSFETs

Publication List

A. Journal Papers

1. Guang-Li Luo, Shih-Chiang Huang, Chih-Hsin Ko, Clement H. Wann, Cheng-Ting Chung, Zong-You Han, **Chao-Ching Cheng**, Chun-Yen Chang, Hau-Yu Lin, and Chao-Hsin Chien, "The annihilation of threading dislocations in the germanium epitaxially grown within the silicon nanoscale trenches", *J. Electrochem. Soc.*, vol.156, pp. H703-H706, 2009.
2. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Ching-Lun Lin, Hung-Sen Chen, Jun-Cheng Liu, Chi-Chung Kei, Chien-Nan Hsiao, and Chun-Yen Chang, "Junction and Device Characteristics of Gate-Last Ge p- and n-MOSFETs with ALD-Al_2O_3 Gate Dielectric", (accepted by *IEEE Trans. Electron Devices*).
3. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Yu-Ting Ling, Ruey-Dar Chang, Chi-Chung Kei, Chien-Nan Hsiao, Jun-Cheng Liu, and Chun-Yen Chang, "Effects of Minority-Carrier Response Behavior on Ge MOS Capacitor Characteristics: Experimental Measurements and Theoretical Simulations", *IEEE Trans. Electron Devices*, vol.56, pp.1118-1127, 2009.
4. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Jun-Cheng Liu, Yi-Cheng Chen, Yao-Feng Chang, Shin-Yuan Wang, Chi-Chung Kei, Chien-Nan Hsiao, and Chun-Yen Chang, "Five-Element Circuit Model Using Linear Regression Method to Correct the Admittance Measurement of MOS Capacitor", *J. Vac. Sci. Technol. B*, vol. 27, pp. 130-133, 2009.
5. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Jun-Cheng Liu, Chi-Chung Kei, Da-Ren Liu, Chien-Nan Hsiao, Chun-Hui Yang, and Chun-Yen Chang, "Characteristics of atomic-layer-deposited Al_2O_3 high-k dielectric films grown on Ge substrates", *J. Electrochem. Soc.*, vol.155, pp. G203-G208, 2008.
6. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Chun-Hui Yang, Chih-Kuo Tseng, Hsin-Che Chiang, and Chun-Yen Chang, "Improved electrical properties of Gd_2O_3/GaAs capacitor with modified wet-chemical clean and sulfidization procedures", *J. Electrochem. Soc.*, vol.155, pp. G56-G60, 2008.
7. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Chun-Hui Yang, Ching-Chih Chang, Chun-Yen Chang, Chi-Chung Kei, Chien-Nan Hsiao, and Tsong-Pyng Perng, "Effects of interfacial sulfidization and thermal annealing on the electrical properties of an atomic-layer-deposited Al_2O_3 gate dielectric on GaAs substrate", *J. Appl. Phys.*, vol.103, p.074102, 2008.
8. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Ching-Chih Chang, Chi-Chung Kei, Chun-Hui Yang, Chien-Nan Hsiao, Tsong-Pyng Perng, and Chun-Yen Chang, "Electrical and material characterization of atomic-layer-deposited Al_2O_3 gate dielectric on ammonium sulfide treated GaAs

substrates", J. Phys.: Conf. Series, vol.100, p.042002, 2008.

9. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Chun-Hui Yang, Mei-Ling Kuo, Je-Hung Lin, Chih-Kuo Tseng, and Chun-Yen Chang, "Study of Thermal Stability of HfO_xN_y/Ge Capacitors Using Post-deposition Annealing and NH_3 Plasma Pretreatment", *J. Electrochem. Soc.*, vol.154, pp. G155-G159, 2007.
10. Guang-Li Luo, Yen-Chang Hsieh, Edward Yi Chang, M. H. Pilkuhn, Chao-Hsin Chien, Tsung-Hsi Yang, **Chao-Ching Cheng**, and Chun-Yen Chang, "High-speed GaAs metal gate semiconductor field effect transistor structure grown on a composite Ge/Ge_xSi_{1-x}/Si substrate", *J. Appl. Phys.*, vol.101, p.084501, 2007.
11. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Chun-Hui Yang, Mei-Ling Kuo, Je-Hung Lin, and Chun-Yen Chang, "Ultrathin Si capping layer suppresses charge trapping in HfO_xN_y/Ge metal-insulator-semiconductor capacitors", *Appl. Phys. Lett.*, vol.90, p.012905, 2007.
12. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Je-Hung Lin, Shih-Lu Hsu, Chun-Hui Yang, and Chun-Yen Chang, "Thermochemical reaction of $ZrO_x(N_y)$ interfaces on Ge and Si substrates", *Appl. Phys. Lett.*, vol.89, p.012905, 2006.
13. **Chao-Ching Cheng**, Chao-Hsin Chien, Ching-Wei Chen, Shih-Lu Hsu, Chun-Hui Yang, and Chun-Yen Chang, "Effects of Postdeposition Annealing on the Characteristics of HfO_xN_y Thin Films on Germanium and Silicon Substrates", *J. Electrochem. Soc.*, vol.153, pp. F160-F168, 2006.
14. Tzer-En Nee, Ya-Fen Wu, **Chao-Ching Cheng**, Hui-Tang Shen, "Carrier dynamics study of the temperature- and excitation-dependent photoluminescence of InAs/GaAs quantum dots", *J. Appl. Phys.*, vol. 99, p. 013506, 2006.
15. Tzer-En Nee, Jen-Cheng Wang, Hui-Tang Shen, **Chao-Ching Cheng**, and Ray-Ming Lin, "Optical investigation of the interdot carrier transfer process in InAs/GaAs quantum-dot heterosystems", *J. Vac. Sci. Technol. B*, vol. 24, pp. 1-4, 2006.
16. Guang-Li Luo, **Chao-Ching Cheng**, C.-Y. Huang, Shih-Lu Hsu, Chao-Hsin Chien, W.-X. Ni, and Chun-Yen Chang, "Suppressing phosphorus diffusion in germanium by carbon incorporation", *Electron. Lett.*, vol.41, pp. 1354-1355, 2005.
17. **Chao-Ching Cheng**, Chao-Hsin Chien, Ching-Wei Chen, Shih-Lu Hsu, Ming-Yi Yang, Chien-Chao Huang, Fu-Liang Yang, and Chun-Yen Chang, "Impact of post-deposition-annealing on the electrical characteristics of HfO_xN_y gate dielectric on Ge substrate", *Micro. Engineering*, vol. 80, pp. 30-33, 2005.
18. Y.-F. Wu, H.-T. Shen, Y.-H Lin, **C.-C. Cheng**, R.-M. Lin, T.-E. Nee, and N.-T Yeh, "Intersublevel relaxation dependence of carrier hopping in self-organized InAs quantum dot heterostructures", *Solid. State. Phen.* vol. 99-100, pp. 41-48, 2004.

19. Ray-Ming Lin, **Chao-Ching Cheng**, Hui-Tang Shen, and Tzer-En Nee, "Study of lateral-carrier transport in InAs quantum-dot heterostructures by optical spectroscopy", *J. Vac. Sci. Technol. A*, vol. 22, pp. 891-893, 2004.
20. Tzer-En Nee, **Chao-Ching Cheng**, and Ray-Ming Lin, "Phonon-Assisted Auger Recombination Processes in InGaAs/GaAs Single-Quantum-Well Lasers", *Jap. J. Appl. Phys*. vol. 43, pp. 890-893, 2004.

B. Conferences

1. Cheng-Ting Chung, Shih-Chiang Huang, Guang-Li Luo, Chih-Hsin Ko, Clement H. Wann, Hau-Yu Lin, Zong-You Han, **Chao-Ching Cheng**, Chun-Yen Chang, and Chao-Hsin Chien, "Achievement of the dislocation-free Ge/Si heterostructure by employing nanoscale epitaxial growth method", *2009 Int. Conf. on Solid State Devices and Materials (SSDM 2009)*, Sendai, Japan, October 7-9, 2009.
2. Zong-You Han, Guang-Li Luo, Shih-Chiang Huang, Chih-Hsin Ko, Clement H. Wann, Hau-Yu Lin, Cheng-Ting Chung, **Chao-Ching Cheng**, Chun-Yen Chang, and Chao-Hsin Chien, "Heteroepitaxy of Si_xGe_{1-x} ($x < 5\%$) source/drain on GaAs substrates for the application of III-V MOSFETs", *2009 Int. Conf. on Solid State Devices and Materials (SSDM 2009)*, Sendai, Japan, October 7-9, 2009.
3. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Hsin-Che Chiang, Hung-Sen Chen, Ching-Lun Lin, Chi-Chung Kei, Chien-Nan Hsiao, and Chun-Yen Chang, "Minority carrier response characteristics in Germanium MOS capacitor", *2008 Int. Conf. on Solid State Devices and Materials (SSDM 2008)*, Ibaraki, Japan, September 24-26, 2008.
4. Hsin-Che Chiang, Chao-Hsin Chien, **Chao-Ching Cheng**, Ching-Lun Lin, Chung-Sen Chen, Guang-Li Luo, Yi-Ling Shen, Chi-Chung Kei, and Chien-Nan Hsiao, "Improved electrical characteristics of atomic-layer-deposited Al_2O_3/GaAs MOS capacitors with $(NH_4)_2S$-C_4H_9OH sulfide treatment", *2008 Int. Conf. on Solid State Devices and Materials (SSDM 2008)*, Ibaraki, Japan, September 24-26, 2008.
5. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Chih-Kuo Tseng, Hsin-Che Chiang, Chun-Hui Yang, and Chun-Yen Chang, "Improved electrical characteristics of Pt/Gd_2O_3/GaAs MOS capacitors with surface preparation procedures", *2007 Int. Conf. on Solid State Devices and Materials (SSDM 2007)*, Ibaraki, Japan, September 18-21, 2007.
6. **Chao-Ching Cheng**, Chao-Hsin Chien, Guang-Li Luo, Ching-Chih Chang, Chi-Chung Kei, Chun-Hui Yang, Chien-Nan Hsiao, Tsong-Pyng Perng, and Chun-Yen Chang, "Electrical and material characterization of atomic-layer-deposited Al_2O_3 gate dielectric on ammonium sulfide treated GaAs substrates", *17th Int. Vacuum Congress/13th Int. Conf. on Surf. Sci. and Int. Conf.*

on Nano Sci. and Tech. (IVC-17/ICSS-13 and ICN+T2007), Stockholm, Sweden, July 2-6, 2007.

7. Jun-Cheng Liu, Chao-Hsin Chien, Guang-Li Luo, Chi-Chung Kei, **Chao-Ching Cheng**, Chien-Nan Hsiao, Tsong-Pyng Perng, Chun-Hui Yang, and Chun-Yen Chang, "Characterization of interface states of Ge-MOSCAPs with atomic-layer-deposited Al_2O_3 dielectrics by conductance-voltage (G-V) method", *Symposium on Nano Device Technology (SNDT 2007)*, Hsinchu, Taiwan, May 10-11, 2007.
8. Jun-Cheng Liu, Chao-Hsin Chien, Chi-Chung Kei, Guang-Li Luo, **Chao-Ching Cheng**, Chien-Nan Hsiao, Tsong-Pyng Perng, and Chun-Yen Chang, "Al_2O_3 high-*k* dielectric films grown by atomic layer deposition on Ge substrate", *AVS 6th Int. Conf. On Atomic Layer Deposition*, Seoul, Korea, July 24-26, 2006.
9. **Chao-Ching Cheng**, Chao-Hsin Chien, Ching-Wei Chen, Shih-Lu Hsu, Ming-Yi Yang, Chien-Chao Huang, Fu-Liang Yang, and Chun-Yen Chang, "Impact of post-deposition-annealing on the electrical characteristics of HfO_xN_y gate dielectric on Ge substrate", *Insulating Films on Semiconductors (INFOS)*, Leuven, Belgium, June 22-24, 2005.
10. J.-C. Lee, Y.-F. Wu, **C.-C. Cheng**, H.-T. Shen, J.-C. Wang, R.-M. Lin, and T.-E. Nee, "Temperature Dependence of Carrier Dynamics in InAs/GaAs Quantum Dot Heterostructures", *12th Canadian Semiconductor Technology Conference (CSTC)*, Ottawa, Canada, August 16-19, 2005.
11. **Chao-Ching Cheng**, Hui-Tang Shen, Ray-Ming Lin, Tzer-En Nee, Ya-Fen Wu, Tung-Po Hsieh, Nien-Tze Yeh "Lateral Hot-Carrier Transport in InAs Quantum Dot Heterostructures by Optical Spectroscopy", *11th Canadian Semiconductor Technology Conference (CSTC)*, Ottawa, Canada, August 18-22, 2003.
12. Hui-Tang Shen, Jen-Cheng Wang, Yung-Hsiang Lin, **Chao-Ching Cheng**, Ray-Ming Lin, Tzer-En Nee, and Nien-Tze Yeh, "Thermally enhanced lateral carrier transfer characteristics in InAs/GaAs quantum dot heterosystem", *European Materials Research Society* (EMRS), Fall Meeting, Warsaw, Poland, September 15- 19, 2003.
13. Hui-Tang Shen, Ya-Fen Wu, Yung-Hsiang Lin, **Chao-Ching Cheng**, Ray-Ming Lin, Tzer-En Nee, and Nien-Tze Yeh, "Intersublevel Relaxation Dependence of Carrier Hopping in self-organized InAs Quantum Dot Heterostructures", *European Materials Research Society* (EMRS), Fall Meeting, Warsaw, Poland, September 15- 19, 2003.
14. **C.-C. Cheng**, C.-E. Huang, T.-F. Liu, R.-M. Lin, T.-E. Nee, Nien-Tze Yeh, "Observations of Hot-Hole Processes in InGaAs/GaAs Single-Quantum-Well Lasers", *Intl. Electron Devices and Materials Symposium (IEDMS)*, Taipei, Taiwan, 2002.

15. **Chao-Ching Cheng**, C.-E. Huang, T.-F. Liu, R.-M. Lin, T.-E. Nee, “Observation of Auger Recombination Processes in the InGaAs/GaAs Single Quantum Well Lasers”, *4th International Conference on Low Dimensional Structures and Devices*(LDSD), Fortaleza - Ceará, Brazil, December 8-13, 2002.