國立交通大學

電子工程學系電子研究所

博士論文

高效能慢波特性傳輸線及去除嵌入技巧的改善

High-Performance Slow-Wave Transmission lines and Improved De-embedding Techniques

研究生：卓秀英 Hsiu-Ying Cho

指導教授：吳重雨 Chung-Yu Wu

中華民國九十九年二月

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博士論文

A Dissertation

Submitted to Department of Electronics Engineering &

Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

in

Electronics Engineering

Feb. 2010

Hsin-Chu, Taiwan, Republic of China

中華民國九十九年二月

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摘要

當我們在設計接地的遮蔽層時，我們必需注到它是否能夠提升品質因數。從未有任何有關於對於浮動條狀遮蔽層的條狀長度、浮動條狀之間的距離、及浮動條狀遮蔽層所在金屬層的位置可以調整波長、衰減耗損、及特徵阻抗的研究可作參考。一般而言，對於曾經發表的等效電路去除嵌入技巧中所提出的假設，只有在元件的長度遠比二埠的距離短時才成立。然而，如果元件的尺寸比較長時，去除嵌入技巧的正確性就會降低。因此，本文所提出的去除嵌入技巧就可以將正確性提高。連線及堆疊通孔寄生效應隨著操作頻率變高而變得日益重要。然而，目前提出的去除嵌入技巧並沒有有效去除堆疊通孔寄生效應。本論文分別闡述高效能傳輸線及去除嵌入技巧的改善。引入慢波特性概念來設計高效能傳輸線元件同時縮減元件尺寸。對於電路設計而言，一個能精確描述高頻元件的理論模型扮演著關鍵的影響，因此本文提出新穎的去除嵌入技巧以便建立更正確的元件理論模型。

利用浮動條狀遮蔽層配合尺寸最佳化設計在先進半導體製程中製作具慢波特性的傳輸線。傳輸線下方的週期性浮動條狀遮蔽層可以用來提供遮蔽基板及縮減波長，此研究是第一個提出藉由改變浮動條狀遮蔽層的條狀長度、

浮動條狀之間的距離、及浮動條狀遮蔽層所在金屬層的位置可以調整波長、衰減耗損、及特徵阻抗。將波長變短必須同時綜合考量慢波特性及衰減耗損。根據模擬分析浮動條狀遮蔽層的條狀長度、條狀之間的距離、及條狀遮蔽層所在金屬層的位置，發現最小的條狀遮蔽層條狀長度可以得到最佳的結果。設計電路的準則可以使電路設計者選擇最適合的浮動條狀遮蔽層，達到最佳化的電路設計。待測的傳輸線元件以 45 nm 先進半導體製程製作而成。量測及模擬都到達頻率 50 GHz。傳輸線的長度常常用在半波長或四分之一波長，藉由最佳浮動條狀遮蔽層的設計可以使波長變短，慢波共平面波導傳輸線可以達到67%的面積用地節省。實驗結果顯示，比起傳統傳輸線，可以增加九倍的有效相對介電常數及增加六倍的品質因數。

在傳輸線去除嵌入技巧的改善中，利用長度分別為一倍以及二倍的傳輸線就可以直接得到左邊及右邊的地-訊號-地探針銲墊（ GSG probe pads ）。額外的直通（ through ）結構，用來去除堆疊通孔的寄生效應是目前去除嵌入技巧獨一無二的設計結構。此建議方法有五個優點，分別是需要的用地面積變小、解決銲墊及連線的不連續、解決基板耦合及接觸效應、採用去除堆疊通孔寄生效應、以及解決傳統去除嵌入技巧多扣除寄生效應的問題。這個新方法是高頻去除嵌入技巧的一大突破，使得射頻元件模型更加精確。對於串聯去除嵌入技巧有關去除堆疊通孔寄生效應，此方法最適用於具慢波同軸波導傳輸線結構。實驗結果顯示改變浮動條狀遮蔽層的密度及浮動條狀遮蔽層所在金屬層的位置，可以調整衰減耗損及波長。藉由同軸波導上層及下層浮動條狀遮蔽最佳化設計，可以使波長變短而達到66%的面積用地節省。

High-Performance Slow-Wave Transmission lines and Improved De-embedding Techniques

Student：Hsiu-Ying Cho Advisor：Chung-Yu Wu

Department of Electronics Engineering and
Institute of Electronics
National Chiao Tung University

Abstract

The patterned ground shield (PGS) must be well designed; otherwise they may not at all able to improve the quality factor. Investigations into different strip length, strip spacing and metal layer positions of the slot-type floating shields for wavelength, attenuation loss, and characteristic impedance, which have not yet been conducted before, are performed in this work. In general, the assumption for lumped-equivalent-circuit-model-based techniques is valid only if the lengths of the DUT devices are much smaller than the distances between two ports. However, this is not always true for larger DUT devices and may result in over de-embedding when intrinsic device performance is involved. Therefore, the proposed de-embedding technique can address the problem of over de-embedding. The contribution of the interconnection and the via stack becomes important as the frequencies increase. Unfortunately, currently existing techniques do not account

for via stack parasitic contributions. In this dissertation, high-performance transmission lines and improved de-embedding techniques are presented. The slow-wave concept has been used in order to design high-performance transmission lines and reduce the size of the transmission lines. Accurate models that describe the behavior of RF devices are critical for the circuit designs, and improved parasitic de-embedding techniques are proposed as to achieve accurate device characterization.

A novel slow-wave transmission line with optimized slot-type floating shields in advanced CMOS technology is presented. Periodical slot-type floating shields are inserted beneath the transmission line to provide the substrate shield and shorten the electromagnetic propagation wavelength. This is the first study that demonstrates how the wavelength, attenuation loss, and characteristic impedance can be adjusted by changing the strip length, the strip spacing, and the metal layer positions of the slot-type floating shields. Wavelength shortening needs to be achieved with a trade-off between the slow-wave effect and the attenuation loss. The slot-type floating shields with different strip lengths, strip spacings and metal layer positions are analyzed. It is concluded that the minimum strip length provides the most optimal result. A design guideline can be established that enables circuit designers to achieve the most appropriate slot-type floating shields for optimal circuit performance. Transmission line test structures were fabricated by using 45 nm CMOS process technology. Both measurement and electro-magnetic (EM) wave simulation were performed up to 50 GHz. Transmission lines are frequently

used at a length of half- or quarter-wavelength. With a shortened wavelength, a saving in silicon area of more than 67% can be achieved by using optimized slot-type floating shields. Experimental results demonstrated a higher effective relative permittivity value, improved by a factor of more than 9, and a better quality factor, improved by a factor of more than 6, as compared to conventional transmission lines.

A novel transmission line de-embedding technique is presented. With this technique, the left- and right-side ground-signal-ground (GSG) probe pads can be extracted directly using two transmission line test structures of length L and 2L. An additional through structure is designed using via stack de-embedding, which is unique amongst current de-embedding methods. The advantages of the proposed method include the following: (1) a smaller silicon area; (2) the consideration for discontinuity between the pad and interconnect; (3) the consideration for substrate coupling and contact effects; (4) the employment of via stack de-embedding; and (5) the solution to the over de-embedding. The proposed novel methodology could be considered as a breakthrough in the area of ultra-high frequency de-embedding and should enable more accurate RF models to be developed. In the proposed methodology, intrinsic slow-wave coplanar waveguide (CPW) transmission line structures are placed on the inter-level metallization layers, as they are the most appropriate RF device for a cascade-based de-embedding method involving the via stack de-embedding technique. Experimental results have demonstrated that attenuation loss and wavelength can be optimized by changing the metal density

and the metal layer positions of the floating shields. With a shortened wavelength, a reduction in silicon area of more than 66% can be achieved by using optimized slot-type floating shields located both above and below the CPW structure.

Acknowledgements

首先，我要感謝我的指導教授吳重雨，多年來耐心及嚴謹的指導，讓我了解面對困難及解決問題的正確態度，老師的身教時時流露著做人及做學問的道理，老師以身作則，常常犧牲假日休息時間來指導學生，這些做事認真不馬虎的態度，都讓學生受益良多。平常或是言教或是身教的做人做事道理，對我們在人生未來的旅途上都很大的幫助，誠心的謝謝您。

接著，我要感謝台積電劉莎莉處長的支持與指導，讓我有機會把事情做的更好更完整，同時讓我漸漸喜歡上做踏實的研究，也由於莎莉處長的開闊心胸，讓我們勇敢說實話，紮實的把事情做更好，從不吝惜給我們指導，磨練我們成為能夠獨立解決問題的工程師，誠心的謝謝您。

在這段求學的過程，我要感謝所有台積電的長官及同事還有交大307實驗室的夥伴們，一路上有你們的扶持，讓我在面對挫折時有更大的韌性一一克服困難，誠心的謝謝您們。

最後，我要致上最深的感謝給我的家人及朋友，沒有你們無怨無悔的付出，就不會有今日的我，願你們永遠幸福平安，誠心的謝謝您們。

卓秀英

中華民國九十九年二月

Contents

1 Review of Transmission Line Structures and De-embedding Methodologies

1.1 Transmission line design challenges in silicon technology

Advanced communication applications, such as cellular telephones, wireless networks, satellite broadcasting and fiber-optic communication rely on continuous improvements in increased speed and reduced size. In other words, a trend toward increasing the speed of information transmission and miniaturizing the integrated circuits that provide various relevant communication functions is inevitable. However, as system designers look toward using higher frequencies in the range of tens of gigahertz (GHz), as well as the miniaturization of the integrated circuits, a number of conventional components that in the past were considered inapplicable continue to become indispensable. Consequently, a common design challenge involves identifying new components that can be implemented in integrated circuits to achieve faster operations and smaller chip areas.

The size of the interconnections and parasitic loss in silicon IC technologies are common design challenges in millimeter wave integrated circuits (MMICs). Passive devices with low parasitic loss that can be isolated from other circuit sub-blocks are required in order to complement the gain-bandwidth of silicon transistors for microwave applications. Unfortunately, the parasitic contribution of RF on-chip passive components cannot be scaled as readily as the parasitic that

accompanies active devices, such as transistors. Until more efficient components are developed, circuit designs will be constrained by the limitations related to the interconnections and passive components surrounding the active devices.

In most circuit designs, the direct application of traditional transmission lines is not realistic because the electromagnetic wavelength is too long. For example, the electromagnetic wavelength in SiO_2 dielectric material is 3000 um at 50 GHz, which is area-consuming when applied to impedance matching networks for quarter-wavelength long transmission lines. Furthermore, the increased ohmic and substrate loss of transmission lines is another barrier to the design of fully integrated high-frequency circuits. Current crowding at high frequencies also causes high ohmic conductor loss. Each type of metal has its own skin depth, which is a function of frequency, as illustrated in Fig. 1-1. The exact skin depth at certain frequencies is listed in Table 1-1 for reference. The skin depth of copper at 50 GHz is 0.3 um, which negates some of the advantages of a thick top metal layers or increased metal width. If the transmission lines are of a coplanar waveguide type, the lateral sidewalls still help in reducing loss. Coplanar waveguide transmission lines also suffer from substrate loss as a result of using highly conductive substrates in most CMOS processes.

Enhanced silicon system-on-a-chip (SOC) designs continue to enable improved technologies for the future generations of low-cost portable multimedia wireless devices. With the continuous scaling of CMOS technology, devices with a higher cut-off frequency are now being manufactured, so integrated circuits in the

millimeter wavelength range will be considered more seriously in the coming years. However, these devices cannot yet be efficiently integrated into microwave circuits, mainly because of significant transmission line loss and unacceptable line lengths. This study investigates the evolution in the design of the transmission lines, and, therefore, coplanar waveguide (CPW) and microstrip (MS) line transmission line structures are studied in relation to the field of low loss and high quality factors.

CPW transmission lines are often used in (MMICs) [1] as they are uniplanar, which allows the easy connection of shunt and series circuit elements without the need for via hole arrays, as shown in Fig. 1-2(a). CPW transmission lines are commonly referred to as an asymmetric configuration. The arrangement of two ground lines surrounding the center signal conductor serves to confine the electric field in the dielectric material between the signal and the ground lines, thereby creating a conduit through which the wave can propagate. To achieve the proposed characteristic impedance, CPW transmission lines allow a variety of signal line width to be used and the adjustable spacing between the signal and the ground lines. However, CPW transmission lines generally suffer from limited impedance ranges. This is due to the fact that CPW transmission line loss tends to increase at high and low characteristic impedance extremes. CPW transmission lines have an inherent disadvantage in having no shield between the signal line and the underlying substrate. Moreover, low-loss CPW structures on a silicon substrate have been designed and optimized by using either a thick dielectric layer [2] or a micromachining process [3]-[5]. However, the CPW structures mentioned above

are not fully compatible with advanced CMOS processes. It is expected that a standard CPW transmission line can be combined with substrate shields to create competitive passive components for MMIC chips.

Microstrip (MS) line structures are composed of a signal line and a ground plane underneath such that there is no dependency on substrate properties due to the shielding by the ground plane [6], as shown in Fig. 1-2(b). The signal line and the ground plane for MS lines are separated by only a few microns of SiO_2 dielectric material as a result of the continuous scaling of CMOS technology, resulting in a relatively large capacitance. Consequently, a 50 Ω MS line has a relatively narrow signal width. To achieve the proposed characteristic impedance, the ohmic loss is higher because of the narrow signal width, which limits the flexible tuning in characteristic impedance performance. Since the ground plane is treated as both the return path and the substrate shields, the thin ground plane used in current CMOS processes also results in high ohmic loss. Lowing the resistance of the ground plane can be achieved by connecting the two bottom layers.

Several substrate shield methods for passive devices, such as transmission lines, inductors and transformers, have been developed in order to minimize the amount of lost radio-frequency (RF) energy that is coupled to the substrate. Substrate shields can be either a patterned ground shield (PGS) [7]-[17] or a floating shield [18]. The PGS must be well designed; otherwise they may not be able to improve the quality factor, as in [7]-[8]. According to Faraday's and Lenz's laws, an electric field is magnetically induced for every electrical-current-carrying

segment, resulting in both substrate and conductor eddy-current loss [19]-[21]. The interactions and correlations of conductor eddy-current loss on slot-type floating shields [18] have not been investigated previously. The eddy-current loss plays a major role at high frequencies, and it is worth mentioning that the eddy-current loss in conductors is roughly proportional to the square of the frequency [21]. The majority of earlier research [9]-[12] covers frequencies less than 20 GHz, at which there is no enough eddy-current loss on the PGS to significantly degrade the quality factor of the devices. At a frequency of 20 GHz or above, the quality factor of devices with PGS can be degraded further to be even lower than that of unshielded devices. In practice, it is also difficult to implement an on-chip ground reference that does not suffer from some level of voltage variation due to the parasitic inductance and capacitance coupled with the neighboring interconnections of both circuits and packages. When an AC variation exists on the grounded shields, energy is again lost to the silicon, thereby degrading the shielding ability. However, floating shields do not suffer from voltage variations, since no source is connected to the isolated floating shields.

In conventional transmission lines, the phase velocity Vp is controlled only by the dielectric material and can be expressed as:

$$Vp = f \cdot \lambda = \frac{c_0}{\sqrt{\mu_r \cdot \varepsilon_r}} \tag{1}$$

where c_0 is the velocity of light, μ_r is the effective relative permeability, and ε_r is the effective relative permittivity. Generally, a reduction in phase velocity

results in a corresponding reduction in wavelength and an increase in the effective relative permittivity of the dielectric material at a given operating frequency. Thus the wavelength is not adjustable. But a reduced wavelength in the transmission line can be achieved by adding periodical shields that decelerate the propagation EM waves in a guided medium. This is called the slow-wave phenomenon. The slow-wave theory in the microwave range has been investigated with most grounded slow-wave structures [22]-[34]. However, investigations into floating metal coverage density and floating metal layer positions for substrate shields and wavelength reduction, which have not yet been conducted, are performed in this work.

1.2 De-embedding Methodologies

The extreme importance of accurate on-wafer parasitic de-embedding techniques to RF device characterization has already been established. In general, the parasitic contributions of DUT structures mainly arise from the probe pads, the interconnection lines connected to the intrinsic on-chip DUT structure, and the silicon substrate. The intrinsic device performance can be obtained by removing the parasitic contributions of an RF device under test (DUT) structure is defined as the de-embedding, as shown in Fig. 1-3. De-embedding techniques can be classified as two groups. The first group is called the lumped-equivalent-circuit-model-based technique [35]-[43]. An equivalent circuit model for the RF DUT structure and the parasitic components is illustrated in Fig.

1-4. A conventional open/short (OS) de-embedding technique is popularly used in the industry, and the accuracy is recognized for the frequencies below 20 GHz. However, the accuracy is not enough for the frequencies above 20 GHz, and more developed de-embedding techniques, which involve a more complicated extraction and a larger chip in advanced CMOS processes, are needed to obtain accurate results. In this group, an extra grounded metal strip, which adds resistance and inductance to the short structure, is used as a connection between the two ports, as shown in Fig. 1-5. The parasitic contribution of the extra grounded metal strip, resulting in over de-embedding, cannot be ignored if the frequencies are high or if the DUT structures are large. In general, the short structure for lumped-equivalent-circuit-model-based techniques does not account for via stack parasitic contributions exactly if the intrinsic DUT structures are placed on the inter-level metallization layers, as illustrated in Fig. 1-6.

The second group involves a cascade-based de-embedding technique [44]-[49] which enables the extraction of interconnection parameters using through structures. To obtain the most practical test-key design, the metal interconnection from the probe pad to the intrinsic DUT structure should be around 20 um to 40 um. It is important to design a good “through” structure where the left and right pads are effectively uncoupled and do not suffer from the effects of an extra grounded metal strip. Therefore, cascade-based techniques are suitable for larger DUT structures, such as transmission lines, inductors, or MOSFETs with larger widths. In situations where real silicon is involved, RF DUT structures are

connected to the probe pad using low- to high-level metallization, and the cascade sequence is first metallization, then stacked metallization connected through via holes, and finally top metallization. The contribution of the interconnection and the proposed methodology becomes important as the frequencies increase. Unfortunately, currently existing techniques do not account for via stack parasitic contributions.

1.3 Research Motivation and Main Results

The patterned ground shield (PGS) must be well designed; otherwise they may not at all able to improve the quality factor [7]-[8]. Therefore, further study into the optimization of the shields is necessary. According to Faraday's and Lenz's laws, an electric field is magnetically induced to create eddy-current loss both on substrate and grounded shields [19]-[21]. The interactions and correlations of attenuation loss on slot-type floating shields have not been investigated previously. Moreover, investigations into different strip length, strip spacing and metal layer positions of the slot-type floating shields for wavelength, attenuation loss, and characteristic impedance, which have not yet been conducted before, are performed in this work.

A slow-wave CPW transmission line, combining the advantages of both CPW transmission lines and MS lines, is proposed to create high-performance passive components for MMIC chips. Periodical slot-type floating shields are used to achieve a slow-wave phenomenon enabling a reduction in chip area while still

maintaining high performance. Slot-type floating shields can also enhance the immunity of slow-wave CPW transmission lines from AC noise. The optimization of slot-type floating shields plays a key role in creating a high performance slow-wave CPW. Investigations into floating metal coverage density and floating metal layer positions for substrate shields and wavelength reduction, which have not yet been conducted before, are performed in this work. It was found from the experimental results that the currently prevalent concept that highest-density shields are the best choice [8] is simply not always true. Instead, either a lower density coverage or a lower metal layer position of the slot-type floating shields can exhibit a higher quality factor as frequencies increase. Moreover, the wavelength and attenuation loss can be adjusted by changing the strip length (SL), the strip spacing (SS), or the metal layer position of the slot-type floating shields while retaining the same area. As compared with conventional transmission lines, the proposed slow-wave CPW has a higher effective relative permittivity value of up to 51 at 50 GHz, which is an improvement by a factor of more than 9, and a better quality factor of 17 at 33 GHz has been obtained, which is an improvement by a factor of more than 6. Moreover, a wavelength as short as 0.85 mm at 50 GHz has been obtained, which is a reduction by a factor of more than 3 and results in a saving in silicon area of more than 67%.

In general, the assumption for lumped-equivalent-circuit-model-based techniques is valid only if the lengths of the DUT devices are much smaller than the distances between two ports. However, this is not always true for larger DUT

devices and may result in over de-embedding when intrinsic device performance is involved. The lumped-equivalent-circuit-model-based techniques may suffer from other disadvantages, which are that the model used may become invalid when the electrical properties of a network cannot be modeled using an appropriate equivalent circuit such as the complicated substrate network, and that an accurate equivalent circuit would be difficult to be obtained or used if interconnect or transmission lines lengths become too long or the operating frequency becomes too high. For simplification, lumped equivalent-circuit model may ignore some effects, which may be significant at high frequencies, and this will degrade the de-embedding accuracy. The contributions of the interconnection and the via stack become important as the frequencies increase. Unfortunately, currently existing techniques do not account for via stack parasitic contributions exactly if the intrinsic DUT structures are placed on the inter-level metallization layers.

A novel transmission line de-embedding method, which requires two transmission line structures of length L_1 and L_2 and one additional through structure, is proposed to create a more accurate RF device characterization. Investigations into methodologies using via stack de-embedding, which have not been conducted previously, are performed in this work. Two transmission line structures are created to achieve direct extraction of the left- and right-side of GSG pads. One additional through structure is designed to solve the bottleneck resulting from via stack de-embedding and the uncertainty associated with direct measurement. Based on the experiment and simulation results from this work, it

can be concluded that direct extraction of the left- and right-side GSG pads and the via stack de-embedding method are the best options. When compared with conventional de-embedding methods, the advantages of the proposed method include the following: (1) a smaller silicon area; (2) the consideration for discontinuity between the pad and interconnect; (3) the consideration for substrate coupling and contact effects; (4) the employment of via stack de-embedding; and (5) the solution to the over de-embedding.

Coaxial transmission lines offer significant advantages for the design of integrated millimeter-wave circuits when compared to those offered by microstrip or coplanar waveguide transmission lines [50]-[51]. Since coaxial transmission lines are shielded, lines and components can be closely spaced and they can even pass over each other with minimal crosstalk, allowing for complex and compact signal routing. A slow-wave coplanar waveguide (CPW) transmission line structure, where floating shields are both above and below the CPW structure, can be regarded as a rectangular coaxial transmission line structure. Moreover, the design and performance of coaxial transmission lines are independent of any substrate. As demonstrated in the coaxial transmission line study, attenuation loss and wavelength can also be adjusted by changing the metal density and the position of the floating shields on the metal layers. An optimization index of the slow-wave coaxial transmission lines has been developed to enable circuit designers to determine expediently the most appropriate slot-type floating shields to meet design specifications. The proposed floating slow-wave coaxial

transmission line has a better quality factor of 15 at 50 GHz and a shorter wavelength, which results in a reduction in silicon area of more than 66% when compared to that of conventional CPW transmission lines.

Frequency (Ghz)	1	10	20	30	40	50
Skin depth of Copper (um)	2.07	0.66	0.46	0.38	0.33	0.29
Skin depth of Aluminum (um)	2.57	0.81	0.58	0.47	0.41	0.36
Skin depth of Silicon (um)	5030.00	1590.63	1124.74	918.35	795.31	711.35

Table 1-1. The skin depth for different metal materials

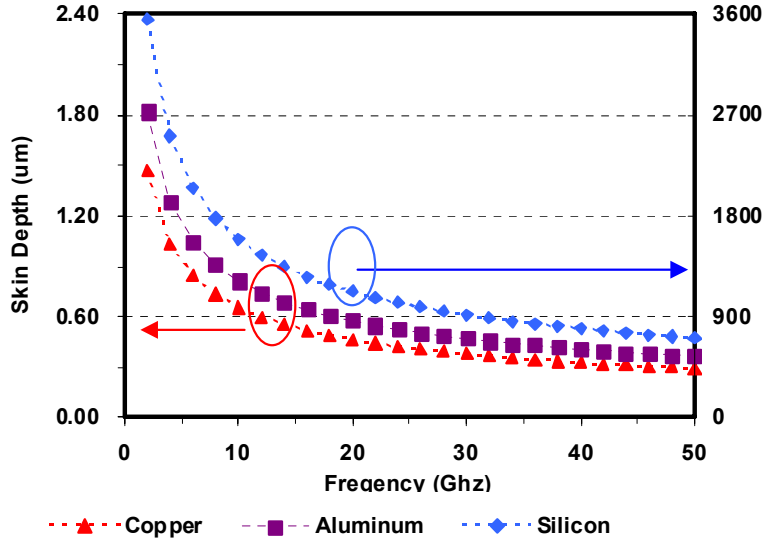
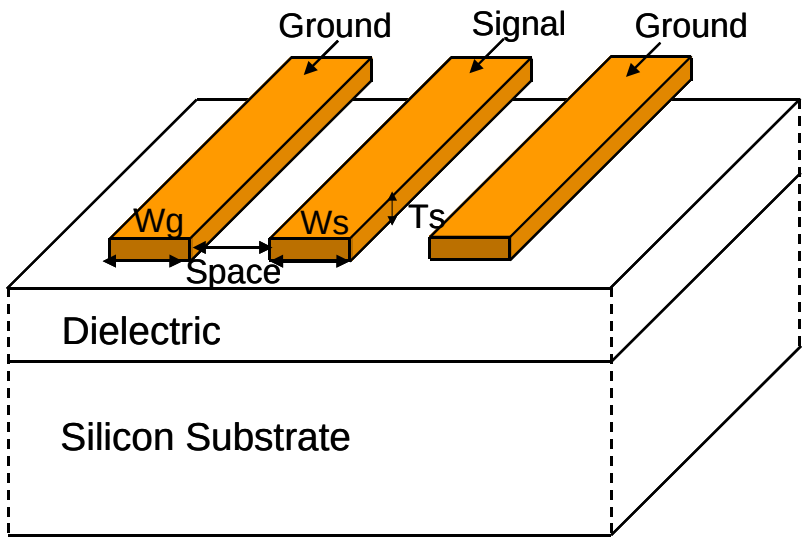
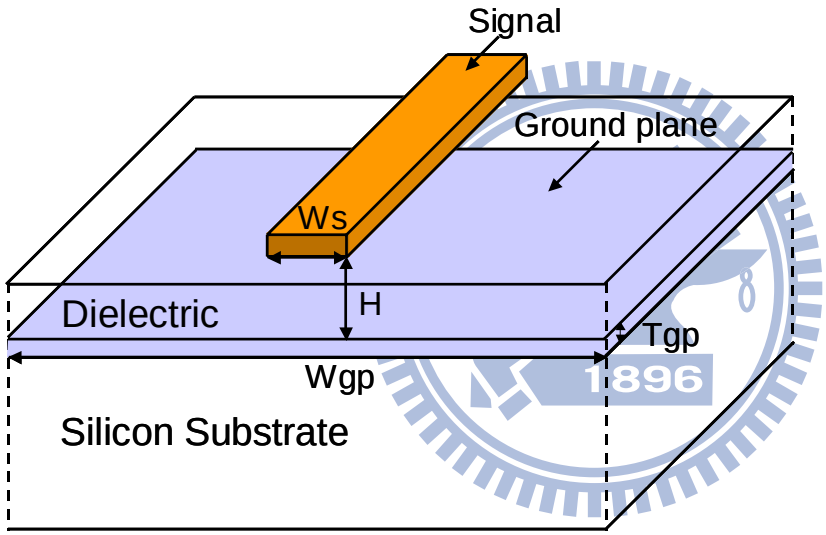


Fig. 1-1. The skin depth for copper, aluminum, and silicon for frequencies up to 50 GHz.



(a)



(b)

Fig. 1-2. A schematic view of the transmission line structures. (a) Coplanar waveguide. (b) Microstrip line.

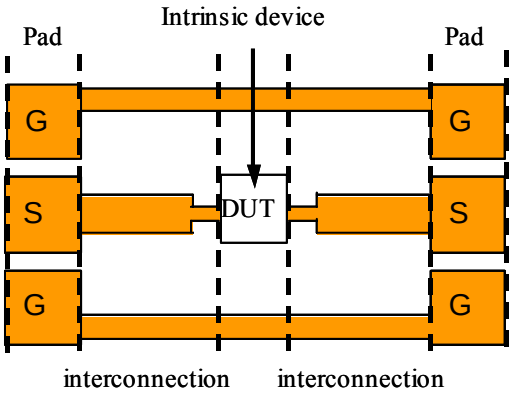


Fig. 1-3. A top view for the RF DUT structure and the parasitic components.

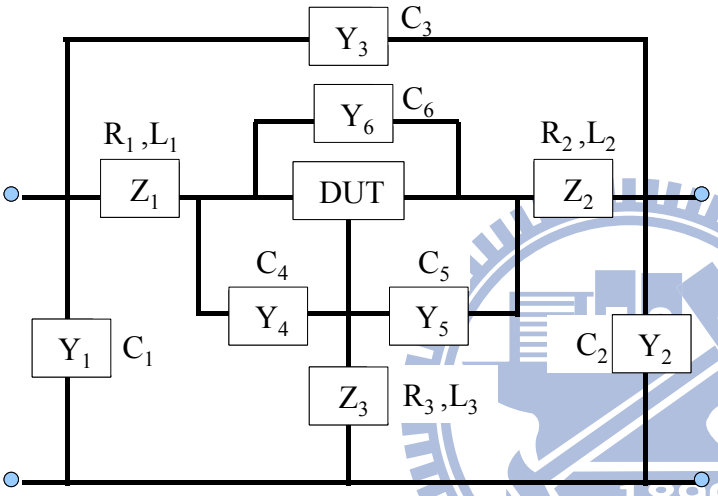
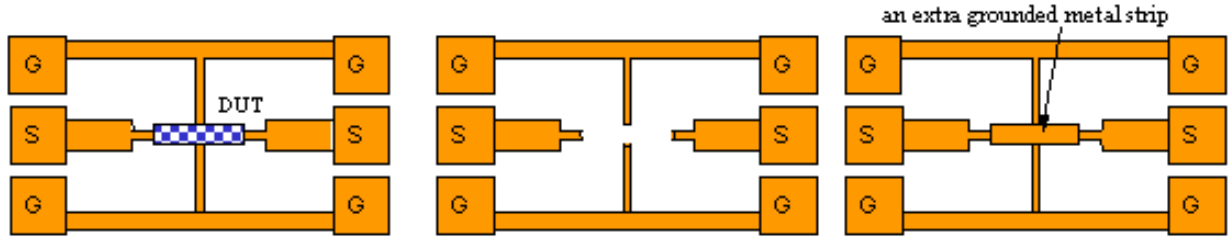
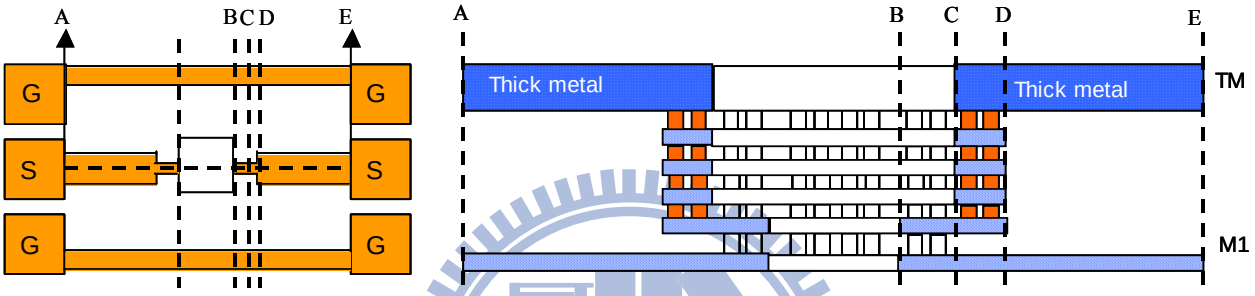


Fig. 1-4. An equivalent circuit model for the RF DUT structure and the parasitic components.



(a) (b) (c)

Fig. 1-5. A long and thin structure. (a) The RF DUT structure. (b) The open structure. (c) The short structure.



(a) (b)

Fig. 1-6. The short structure. (a) The top view structure, and (b) The cross-sectional view along the A- E cut.

2 High-Performance Slow-Wave Transmission Lines with Optimized Slot-Type Floating Shields

2.1 The analysis of transmission lines

2.1.1 Measured and simulated calibration

A simulation of transmission line performance up to 50 GHz was carried out using a commercial electromagnetic EM simulator, Ansoft HFSS, in order to fit the simulated data to the measured data by slightly adjusting the process parameters, such as the substrate conductivity, the metal conductivity and the relative dielectric constant. The process parameters were then calibrated using the measured data. After determining the appropriate process parameters to fit the real silicon process, the EM simulator can provide simulation results very close to the observed measurements. Consequently, we can conduct further characteristic analysis based on the simulation results. The silicon layout was designed based on the optimized simulation results. The CPW transmission line structures both with and without the floating metal strip shields were chosen to be used as calibration sets. The CPW transmission line without a floating shield is a signal line width of 2 um and a space of 4.5 um between the signal and the ground lines. However, the CPW with a floating shield has the same width and space, but contains a 1 um metal strip shield width and a 0.5 um metal strip shield space between each strip. Figs. 2-1(a),

(b), (c), and (d) show the transmission line performance results, such as the attenuation loss, the quality factor, the relative permittivity, and the wavelength, as functions of frequency, and a good agreement between the measured and the simulated performance results was demonstrated. Consequently, the optimization of slot-type floating shields is further conducted using the HFSS simulation results.

2.1.2 Coplanar Waveguide (CPW)

An electromagnetic (EM) simulation of transmission lines for frequencies up to 50 GHz was carried out using a commercial EM simulator, Ansoft HFSS, in order to design an optimized transmission line. EM field distribution and non-linear behavior can then be conducted through full field analysis, which cannot be measured from the silicon experiment. In the EM simulation, transmission line performance versus the dimensions of the CPW transmission line structures and MS line structures are investigated, respectively. This saves the silicon cost and research time for transmission line development.

The performance of a transmission line can be characterized by the characteristic impedance, the attenuation loss, the effective relative permittivity, the wavelength, and the quality factor, and the detail explanation is included in the following. A 2x2 transmission (ABCD) matrix is a powerful network matrix that can be used for each two-port network. An ABCD matrix for the cascaded connection of two or more two-port networks can be easily found by multiplying the ABCD matrices of the individual two-ports. A two-port transmission line

device under test (DUT) structure can be decoupled into a cascade of three two-port networks, including two GSG pads and an intrinsic transmission line. After subtracting the parasitics of the pads from the transmission line DUT structure, the intrinsic transmission line characteristics can be obtained through parameter extraction. The ABCD matrix of a lossy transmission line of length *l* can be represented as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh \gamma l & Z_c \sinh \gamma l \\ \frac{1}{Zc} \sin \gamma l & \cosh \gamma l \end{bmatrix} \tag{2}$$

The characteristic impedance (Z_C) and the propagation constant (γ) can be obtained through the manipulation of ABCD:

$$Zc = \sqrt{\frac{B}{C}}\ (\Omega) \quad \text{and} \quad \gamma = \frac{1}{l}\cosh^{-1} A\ (m^{-1}) \tag{3}$$

The line parameters, such as resistance (R), inductance (L), conductance (G), and capacitance (C) are used to characterize a transmission line directly from material used to fabricate a transmission line and the various transmission line dimension. These line parameters are often used in the equivalent circuit for further analysis, and the slow-wave phenomenon will be discussed later. The relevant transmission line performances used in this thesis are the attenuation loss per unit length (α), the phase constant per unit length (β), the effective relative permittivity (ε_r), the wavelength (λ), and the quality factor (Q), which can be expressed as:

$\alpha = real(\gamma)$ $(Neper/m)$, $\beta = imag(\gamma)$ (rad/m), $\varepsilon_r = 9 \cdot 10^{16} \cdot (\frac{\beta}{\omega})^2$, $\lambda = \frac{2\pi}{\beta}$ (m), and

$$Q = \frac{\beta}{2\alpha} \tag{4}$$

where ω is the angular frequency, and γ is the propagation constant [52]. Firstly, the attenuation loss α represents the loss as the wave propagates, which indicates the amplitude of the wave is decreased as α increases. Secondly, the phase constant β denotes that for each wavelength distance traveled, a wave undergoes a phase change of 2π radians. Another important characterizing parameter of the transmission line is the effective relative permittivity, which is the particular physical characteristic of the transmission line, indicating a given medium in which a wave propagates. The wavelength provides the key index of the slow-wave phenomenon, and is inversely proportional to the phase constant. Finally, the quality factor is regarded as a ratio of the maximum energy stored in the system to the total energy lost by the system in a given time period. In other words, a system that has a large quality factor is a significantly preferred because of the relatively small energy loss.

From the circuit design point of view, transmission line performance, such as the attenuation loss and the quality factor, are calculated. The simulated characteristics for both the attenuation loss and the quality factor versus the signal line width, the spacing between the signal line and the ground lines, and the signal line thickness, respectively, are shown in Fig. 2-2. As can be observed in Fig. 2-2(a), initially, the attenuation loss and the quality factor performance obviously improves as the width of the signal line increases, which is a result of reduced ohmic loss. Once the optimized width value, which is 7 um, as shown in Fig. 2-2(a)

is reached, the energy loss to the substrate increases and even degrades the quality factor performance. Similarly, Fig. 2-2(b) reveals that, initially, the attenuation loss and the quality factor performance obviously improve as the thickness of the signal line increases, which is a result of reduced ohmic loss. Once the optimized thickness value is reached, which is 1 um, the attenuation loss and the quality factor performance shows less improvement, which is a result of saturated ohmic loss. It is worthwhile noting from Fig. 2-2(c) that the loss increases when the spacing between the signal and the ground lines is in both a narrower and a wider range. If the space is narrower, the signal line with a surrounding dielectric material of a few micrometers suffers from a high conductor loss due to high field intensities. If the space is wider than the dielectric thickness from the CPW to the substrate, the coupling loss to the substrate is bigger, which can be explained from the electric field analysis. The electric field intensity coupled to the substrate is stronger as the space is wider, which can be observed from the electric field intensity in the substrate, as shown in Fig. 2-3. The CPW transmission line shown in Fig. 2-3(a) a signal line width of 30 um and a space of 5 um between the signal and the ground lines, suffers from a higher substrate loss than that shown in Fig. 2-3(b) a signal line width of 30 um and a space of 2 um space between the signal and the ground lines. To achieve the proposed characteristic impedance, relatively wide signal lines, and their accompanying larger spaces, suffer from a high attenuation loss and a low quality factor.

2.1.3 Microstrip (MS) Line

The simulated characteristics for both the attenuation loss and the quality factor versus the ground plane width, the ground plane thickness, and the height between the signal line and the ground plane, respectively, are shown in Fig. 2-4. Fig. 2-4(a) reveals that the width of the ground plane, which acts as a substrate shield, is typically much wider than that of the signal line, and a width more than three times greater is suggested in order to minimize the attenuation loss. As expected, the loss increases rapidly once the ground plane thickness becomes less than the skin depth for copper metal, which is 0.3 um at 50 GHz, as illustrated in Fig. 2-4(b). The thickness of the metal layers will be reduced in advanced CMOS processes as a result of scaling trends. An effectively thicker metal can be manufactured by combining two or more metal layers connected by via hole arrays. Fig. 2-4(c) demonstrates that if the height between the signal line and the ground plane is smaller, the MS line suffers from high conductor loss as a result of high field intensities.

In summary, it is suggested that a top metal layer is used as the signal line, while a combination of the first and second metal layer connected by via arrays is used as the ground plane, allowing an increased height between the signal line and the ground plane.

2.1.4 Transmission line Structures with floating shields

Each distinct conventional transmission line suffers from its own unique type

of loss as a result of structural limitations. Since there are no shields between the CPW and the highly conductive substrate, the dominant loss is the energy coupled to the substrate. In contrast, substrate-induced losses are not critical to the MS lines as a result of the ground plane that exists under the signal line. As the scaling of backend processes continues to trend downward, the height between the signal line and the ground plane becomes significantly reduced, which results in the need for a narrower signal line to achieve the desired characteristic impedance. Therefore, ohmic losses in MS lines are increased significantly. Following investigations, a CPW transmission line using periodical floating shields combining the advantages of both CPW transmission lines and MS lines is proposed, as shown in Fig. 2-5, where the SL is the strip length and the SS is the strip spacing. The concept of floating shields is adopted in order to shield the silicon substrate and achieve a compact transmission line structure. Passive devices with substrate shields that can be isolated from other circuit sub-blocks are required for the high-frequency circuit design.

To observe and estimate the substrate loss of a transmission line, the EM simulator is first adopted to evaluate electric field distribution in the substrate. The energy loss to the substrate from CPW transmission lines and slow-wave transmission lines is estimated by integrating the electric energy density $\frac{1}{2}\varepsilon(\vec{E}\cdot\vec{E}^*)$ within the substrate volume as $\frac{1}{2}\varepsilon\int_v(\vec{E}\cdot\vec{E}^*)dV$, and the result is summarized in Table 2-1, where ε is the absolute permittivity, and $\vec{E}$ is the electric field intensity. As expected, the energy loss to the substrate is increased as

the width of the signal line or the space between the signal line and the ground lines increases. Moreover, the substrate loss of a CPW without floating shields is higher than that of a CPW with floating shields. In summary, a CPW with substrate shields illustrates that the presence of the shield can minimize the energy being coupled to the substrate, thereby reducing the attenuation loss. As can easily be observed from the Table 2-1, the substrate loss is higher if the SS is wider in floating shield design.

2.2 The Optimization of Slot-Type Floating Shields

A schematic view of a slow-wave CPW transmission line structure with slot-type floating shields is shown in Fig. 2-6(a), where the SL is strip length and the SS is strip spacing. The advantage of using slot-type floating shields is that slow-wave transmission lines have a lower electric field leakage to the substrate and a lower conductor eddy-current loss, especially at high frequencies. Fig. 2-6(b) shows the electric field distributions from a 3D EM simulation of slot-type floating shields. The electric field starts from the signal line, couples to the floating shields, and finally terminates on the coplanar ground conductors. Therefore, the effective dielectric thickness of devices with floating shields is larger than that of devices with grounded shields. Thus both capacitance and electric field intensity of devices with floating shields are smaller than those of devices with grounded shields, which leads to lower conductor eddy-current loss. Generally, lower attenuation loss and higher effective relative permittivity are required to achieve a high

performance transmission line and a compact size is desired. Consequently, the incorporation of floating shields into transmission lines as an alternative approach for better performance at high frequencies can be considered.

If the length of the periodical structure is short compared to the wavelength, each segment of the signal line can be modeled by an inductance and capacitance lumped-element equivalent circuit, as shown in Fig. 2-7(a), where inductance (L) and capacitance (C) are the series inductance and the shunt capacitance per unit length, respectively. The density, R, of the slot-type floating shields is defined as:

$$R = \frac{SL}{SL + SS} \tag{5}$$

Segment I, on top of the open slot, can be modeled by a series inductance L(1-R)(Δz) and a shunt capacitance C(1-R)(Δz). While Segment II, on top of the shield metal line, can be modeled by a series inductance L(RΔz) and an increased shunt capacitance (nC)(RΔz) where n represents the increased ratio in the capacitance as a result of coupling to the slot-type shields, and Δz denotes the differential unit length. When two segments are cascaded together, the combined equivalent circuit can be condensed as shown in Fig. 2-7(b). It should be noted that the equivalent circuit shown in Fig. 2-7(b) is valid only when n is >> 1. Consequently, the phase velocity Vp with the slow-wave effect can be expressed as:

$$Vp = \frac{c_0}{\sqrt{\mu_r \cdot \varepsilon_r}} = \frac{1}{\sqrt{LC * (nR)}} \tag{6}$$

The slow-wave phenomenon can be explained by equation (6), which shows the

phase velocity is decelerated by a factor of $\sqrt{nR}$.

An optimization of the slot-type floating shields was performed in order to reduce the attenuation loss and also increase the slow-wave features. Both wavelength and attenuation loss can be adjusted by changing both the SL and the SS of the slot-type floating shields while retaining the same area. Optimization analysis of the SL and SS was conducted by evaluating the EM simulation results for structures with a variety of SL and SS dimensions while retaining the same area. An semi-empirical equation is derived to relate the effective relative permittivity ε_r to R and SL,

$$\varepsilon_r = 52 \cdot (R^{0.47} \cdot SL^{-0.167}) + 0.582 \tag{7}$$

The correlation coefficient of the semi-empirical equation in (7) is around 0.91, as shown in Fig. 2-8, which is valuable for predicting the optimized relative permittivity. The calculated values approximate well to the simulation results at 50 GHz, as illustrated in Fig. 2-9(a), which exemplifies the slow-wave equation (6) that predicts that a higher density of slot-type floating shields results in a higher effective relative permittivity. Furthermore, Fig. 2-9(a) indicates that a higher effective relative permittivity is obtained when the SL is smaller. The parameter SL has been explicitly introduced into equation (7). When the attenuation loss performance is taken into consideration, it becomes even more obvious that a minimized SL is the best choice for slot-type floating shield design, as illustrated in Fig. 2-9(a). Though the high-density shields minimize the exposure of the signal line to the substrate, field leakage to the substrate can be reduced. However, the

consequence of using high-density shields is that the conductor eddy-current loss is high, and this in turn increases the attenuation loss. In contrast, the opposite is true when the density of the slot-type floating shields is low. There is a trade-off between the slow-wave effect and the attenuation loss in slow-wave CPW transmission lines; namely, that while the wavelength is reduced to facilitate the implementation of smaller devices, greater attenuation loss may be induced by the eddy-current loss on the slot-type floating shields. The optimization index of the slot-type floating shields is defined as $\varepsilon_r \cdot \alpha^{-1}$ in mm/dB, and Fig. 2-9(b) shows that the optimized performance is achieved when the density R is equal to 0.2 where the SL=1.2 um and the SS=4.8 um. If the specification requirement for the attenuation loss is first determined, then the density of the slot-type floating shields can be calculated. Consequently, the effective relative permittivity can be predicated from the minimum SL and the density of the slot-type floating shields.

2.3 Experiment Results

Five types of transmission lines were fabricated by using CMOS technology, as listed in Tables 2-2 and 2-3, including (1) a CPW transmission line without shields (CPW), (2) five slow-wave CPW transmission lines with slot-type floating shields (FSCPW1, FSCPW2, FSCPW3, FSCPW4, and FSCPW5), (3) a slow-wave CPW transmission line with slot-type grounded shields (GSCPW1), (4) an MS transmission line with plane grounded shields (MS), and (5) four slow-wave MS transmission lines with slot-type grounded shields (SMS1, SMS2, SMS3, and

SMS4). A slow-wave CPW transmission line with slot-type floating shields was designed with slot-type floating shields located periodically beneath the CPW structure, and the slot-type floating shields are oriented transversely to the CPW structure. For all transmission lines listed in Table 2-1, the signal line is formed on the tenth (M10) metal layer and the slot-type shields are created on either the ninth (M9) or eighth (M8) metal layer. The CPW part of the structure has a signal/ground line width of 30 um/10 um, with a 30 um space between the signal and the ground lines. In the slot-type floating shields, the SL is at the minimum length allowed by the design rules to achieve a high performance with a minimized eddy-current loss. The minimum length on M8 is 0.07 um and on M9 is 0.4 um for 45 nm CMOS technology. The slot-type floating shields are designed with the following dimension splits: (1) the SL on M8 is 0.07 um and the accompanying SS is 0.07 um, and (2) the SL on M9 and M8 is 0.4 um and the accompanying SS varies between 0.4 um, 1.6 um, and 3.2 um. For the grounded slow-wave CPW transmission line, it is designed with a similar structure to the slow-wave CPW transmission line with floating shields as described above, but with the slot-type shields connected to the ground. This grounded slow-wave CPW is included for the comparison purpose. A CPW with the same signal/ground line structure but without shields is also included for comparison. The slow-wave MS transmission lines with slot-type grounded shields have a similar structure to the conventional MS lines, but the slot design is used on the ground plane. Similarly, an MS line with the same signal structure but plane shields is also included for comparison.

The backend metal scheme is a dual-damascene copper process with dielectric SiO_2 material that has an effective relative dielectric constant of around 5.4 used as insulator layers. All test structures have the same length of 400 um and width of 120 um to ensure a fair comparison between the different designs. The S-parameters of the transmission line test structures were measured up to 50 GHz using an Agilent 8510C network analyzer.

Fig. 2-10(a) shows that the attenuation loss of a CPW with slot-type floating shields is lower than the CPW without shields. It also shows that at frequencies above 50 GHz, slot-type floating shields on M8 is needed as it has the least amount of eddy-current loss on the floating shields. Among the CPW designs with slot-type floating shields, in the 30-50 GHz frequency range, the attenuation loss of an SL of 0.4 um and an SS of 0.4 um on M8 is less than that on M9, because the dielectric thickness between the signal line on M10 and the floating shields on M8 is 3.2 um, which is thicker than the dielectric thickness between the signal line on M10 and the floating shields on M9 (0.74 um). By now, it can be concluded that the smaller the SL, the wider the SS, and the greater the thickness between the signal line and the floating shields, the lower the attenuation loss will be induced.

Fig. 2-10(b) compares the effective relative permittivity constants of different CPW designs, both with and without floating shields. In slow-wave CPW transmission lines with slot-type floating shields, a reduction in wavelength results in a corresponding increase in both the phase constant and the effective relative permittivity, pursuant to the relationship $\beta = \frac{2\pi}{\lambda}$ and $\varepsilon_r = 52 \cdot (R^{0.47} \cdot SL^{-0.167}) + 0.582$.

The effective relative permittivity increases to 51 at 50 GHz, for the CPW with shields on M9 where SL = 0.4 um and SS = 0.4 um. This is an improvement by a factor of more than 9 compared to a conventional CPW transmission line. As expected, the wider the SS and the greater the dielectric thickness between the signal line and the floating shields, the lower the effective relative permittivity will be obtained. Conventional passive devices in RF circuit design do not gain as much benefit from CMOS scaling as active devices. Passive devices play the role of a bottleneck in area reduction and performance improvement. Since the SL and the SS can be adjusted along technology scaling, a scaled slow-wave CPW can continue to offer lower attenuation loss and higher effective relative permittivity, a significant advantage for future technology scaling, which is a great breakthrough for RF circuit design.

An optimized design requires a good quality factor, $Q = \frac{\beta}{2\alpha}$ where β is the phase constant and α is the attenuation loss. Therefore, the quality factor should be used to judge an overall trade-off between attenuation loss and effective relative permittivity. Guidelines for designing a transmission line with a high quality factor are illustrated in Fig. 2-10(c). The crossover of the quality factor is around frequencies of 30 GHz, so the appropriate choice for designs operating at frequencies below 30 GHz is to create floating shields on M9 with an SL of 0.4 um and an SS of 0.4 um. At frequencies in the range of 30 to 50 GHz, floating shields on M9 with an SL of 0.4 um and a variety of SS values is preferred. As a result, a quality factor of 18 can be achieved at 40 GHz, which is more than 6 times that of

a conventional CPW transmission line, whose value is around 2.8. At significantly higher frequencies above 50 GHz, floating shields on M8 are strongly recommended. The wider the SS, the lower the attenuation loss will be obtained, but the corresponding effective relative permittivity will also be lower. As discussed above and as demonstrated in the experiments, the designers must weigh among SL and SS dimensions, as well as metal layer positions, to design a proper slow-wave CPW with slot-type floating shields with a good quality factor to achieve a functional circuit at the operating frequency.

Fig. 2-10(d) shows that the characteristic impedance can be tuned by changing the SL, the SS, and the metal layer position of the slot-type floating shields. A low characteristic impedance can be achieved by increasing slot-type floating shield density or higher metal layer position. Characteristic impedance tuning by changing the metal density and metal layer position in the slot-type floating shields is also a new design approach.

Furthermore, the wavelength of a transmission line indicates if the transmission line design is compact in size. The wavelengths of transmission lines with a variety of slot-type floating shield design are compared in Fig. 2-10(e), which indicates that the best choice is FSCPW1 with floating shields on M9, SL = 0.4 um and SS = 0.4 um. The wavelength of FSCPW1 is reduced to 0.85 mm, i.e., is by a factor of more than 3 as compared to a conventional CPW transmission line, whose wavelength is 2.63 mm. The reduction in chip area and wavelength for FSCPW1, FSCPW2, FSCPW3, FSCPW4, FSCPW5, and GSCPW1 in terms of

percentage and wavelength are illustrated in Fig. 2-11. A saving in silicon area of more than 67% can be achieved for FSCPW1, which demonstrates that this approach could have extremely high potential for MMIC applications.

A slow-wave CPW transmission line with slot-type grounded shields is shown in Fig. 2-12(a). The slot-type shields are connected to ground by two parallel conductors added at the two ends of the slot-type shields. When the shields are grounded, the electric field starts from the signal line and terminates directly on the grounded shields, as illustrated in Fig. 2-12(b). In Fig. 2-13(a), the measured capacitance of the devices with grounded shields is higher than that of the devices with floating shields, which implies that the effective dielectric thickness of the devices with grounded shields is smaller than that of the devices with floating shields. Consequently, the electric field intensity of the devices with grounded shields is larger than that of the devices with floating shields, resulting in the eddy-current loss induced by increased voltage variation at extreme high frequency. As the signal frequencies increase, the number of voltage variations between the positive and the negative potential in unit time increases, resulting in an increase in eddy-current loss on the grounded shields and the eddy-current loss on the conductors is proportional to the square of the frequency. Since the presence of the grounded shields increases the slow-wave feature as compared to floating shields, the wavelength of the grounded slow-wave transmission line is shorter than that of the floating slow-wave transmission line, as illustrated in Fig. 2-13(b). Although the increase in the slow-wave feature facilitates the fabrication of relatively smaller

devices, higher electric field intensity will enhance the eddy-current loss on the grounded shields.

The optimization index of the slot-type floating shields is defined as $\varepsilon_r \cdot \alpha^{-1}$ in mm/dB, and Fig. 2-14 shows that the optimized performance is achieved when the density R is equal to 0.2 where the SL=0.4 um and the SS=1.6 um. If the specification requirement for the attenuation loss is first determined, then the density of the slot-type floating shields can be calculated. Consequently, the effective relative permittivity can be predicated from the semi-empirical equation in (7) related to minimum SL and the density of the slot-type floating shields. Then, the transmission line length can be calculated, which is useful information for circuit designers.

A slow-wave MS transmission line with slot-type grounded shields is shown in Fig. 2-15. The slot-type technique is designed on the plane ground and two parallel conductors are added to the two ends of the slot-type shields. The flexible characteristic impedance range can be obtained by adjusting the distance between the two substantially identical parallel conductors. The characteristic value varies with the different inductance return paths. The measured results show that a 218% improvement in characteristic impedance at 50 GHz (from 34.91Ω to 76.37Ω) is achieved through an adjustment of the strip width to 66 um, as illustrated in Fig. 2-16(a). Flexible characteristic impedance can be easily obtained by adjusting the strip shield width or SS. If the strip shield width between the parallel conductors is increased, a larger inductance return loop will be created, resulting in higher

characteristic impedance. In contrast, the opposite is true when the strip shield width is decreased. Also, a smaller capacitance can be obtained if the SS is increased, resulting in higher characteristic impedance. Similarly, the opposite is true if the SS is decreased. Accordingly, the desired characteristic impedance can be obtained by adjusting either the position of the two parallel conductors or the SS value. Another significant improvement is a 42.5% saving in silicon area with the wavelength reduced from 2.03 mm to 1.16 mm) at 50 GHz when the strip width is increased to 66 um, as indicated in Fig. 2-16(b). Thus, the wavelength can be reduced to facilitate implementation in smaller devices.

2.4 Conclusion

High performance slow-wave transmission lines with optimized slot-type floating shields have been analyzed. It has been shown that the wavelength, attenuation loss, and characteristic impedance can be adjusted by the SL, the SS, and the metal layer position of the slot-type floating shields while retaining the same area. A semi-empirical equation that can predict a rough value for the effective relative permittivity has been presented. An optimization index of the floating slow-wave CPW transmission lines has been developed to enable circuit designers to expediently determine the most appropriate slot-type floating shields to meet design specifications. The designers must weigh among SL and SS dimensions, as well as metal layer positions, to design a proper slow-wave CPW with slot-type floating shields with a good quality factor to achieve a functional

circuit at the operating frequency. The proposed floating slow-wave CPW transmission line has a higher effective relative permittivity value of up to 51 at 50 GHz, and a better quality factor of 17 at 33 GHz as compared to conventional CPW transmission lines. Moreover, a wavelength as short as 0.85 mm at 50 GHz has been obtained, which results in a saving in silicon area of more than 67%.

Transmission Line Type	Width	Space	Strip Length (SL)	Strip Space (SS)	Substrate Loss (joul)
CPW	10um	30um	No strip shields		4.35E-13
CPW	20um	30um			5.61E-13
CPW	30um	20um			5.54E-13
CPW	30um	30um			6.33E-13
Slow-wave CPW	30um	30um	1.2um	0.3um	6.28E-14
Slow-wave CPW	30um	30um	1.2um	0.6um	6.74E-14
Slow-wave CPW	30um	30um	1.2um	9.6um	1.16E-13

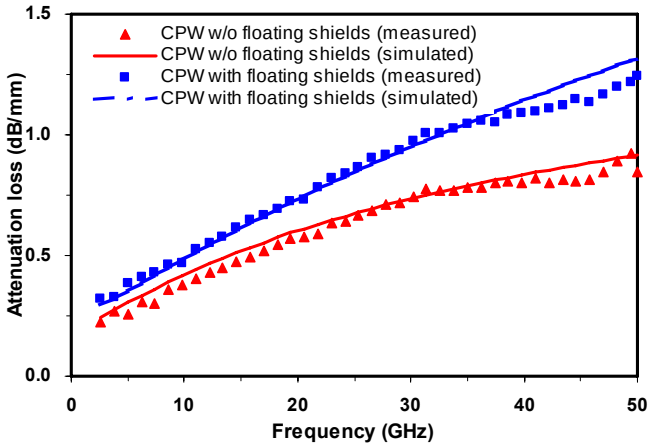
Table 2-1. The energy loss to the substrate

Name	Transmission Line Type	Metal Shield Layer	Strip Width (SL)	Strip Space (SS)	Shield Type
CPW	CPW	No strip shields			
FSCPW1	Floating slow-wave CPW	M9	0.4 um	0.4 um	floating
FSCPW2	Floating slow-wave CPW	M9	0.4 um	1.6 um	floating
FSCPW3	Floating slow-wave CPW	M9	0.4 um	3.2 um	floating
FSCPW4	Floating slow-wave CPW	M8	0.4 um	0.4 um	floating
FSCPW5	Floating slow-wave CPW	M8	0.07 um	0.07 um	floating
GSCPW1	Grounded slow-wave CPW	M8	0.07 um	0.07 um	grounded

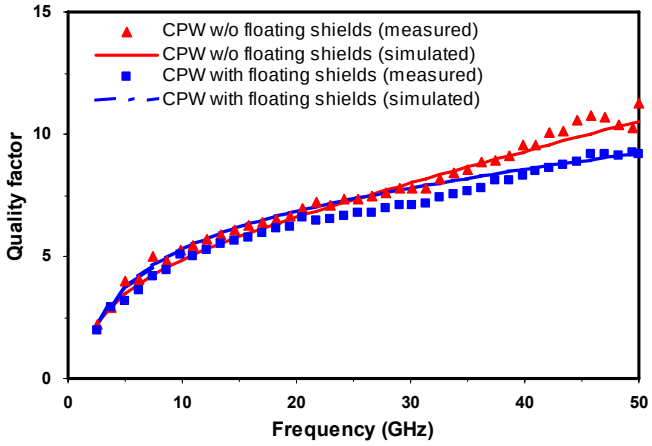
Table 2-2. CPW-type transmission line structures

Name	Transmission Line Type	Metal Signal Layer	Metal Shield Layer	Strip Shield Width
MS	MS line	M9	M8	48um
SMS1	Slow-wave MS line	M9	M8	12um
SMS2	Slow-wave MS line	M9	M8	24um
SMS3	Slow-wave MS line	M9	M8	48um
SMS4	Slow-wave MS line	M9	M8	66um

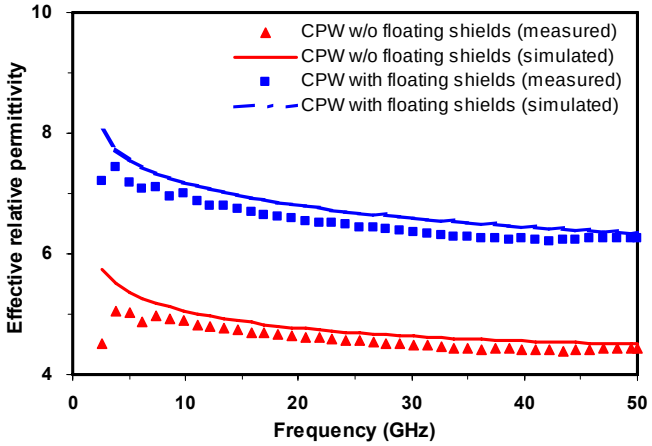
Table 2-3: MS-type transmission line structures


CPW w/o floating shields (measured)
CPW w/o floating shields (simulated)
CPW with floating shields (measured)
CPW with floating shields (simulated)
Attenuation loss (dB/mm)
1.5
1.0
0.5
0.0
0
10
20
30
40
50
Frequency (GHz)

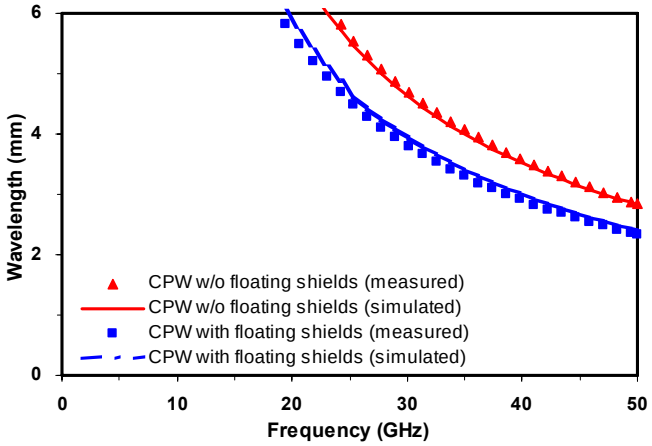
(a)


CPW w/o floating shields (measured)
CPW w/o floating shields (simulated)
CPW with floating shields (measured)
CPW with floating shields (simulated)
Quality factor
15
10
5
0
0
10
20
30
40
50
Frequency (GHz)

(b)

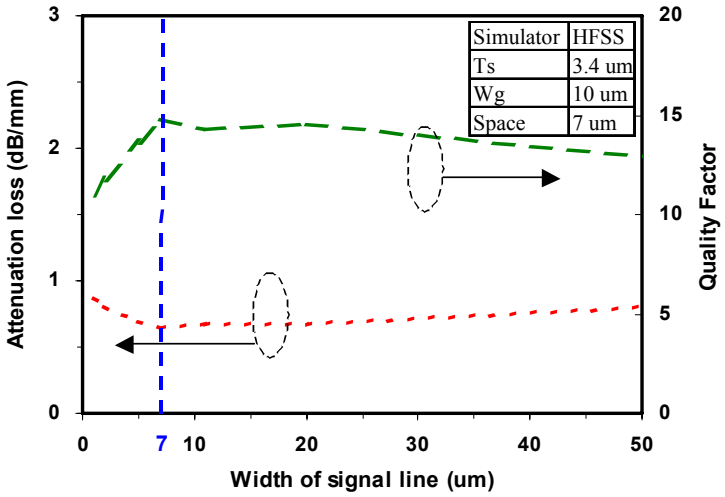

CPW w/o floating shields (measured)
CPW w/o floating shields (simulated)
CPW with floating shields (measured)
CPW with floating shields (simulated)
Effective relative permittivity
10
8
6
4
0
10
20
30
40
50
Frequency (GHz)

(c)

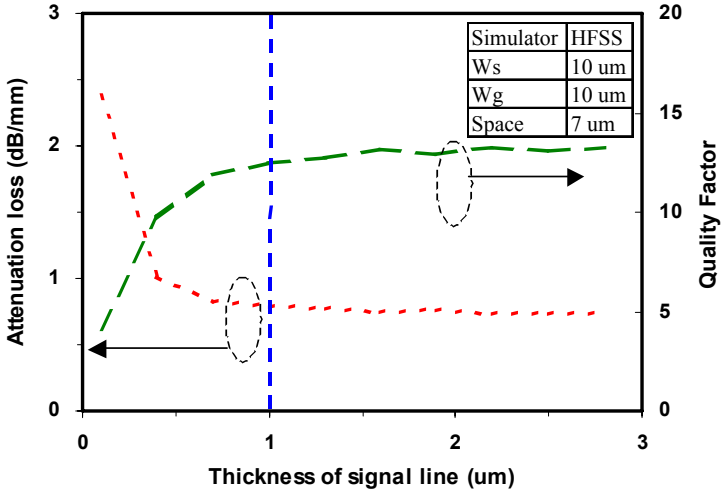


(d)

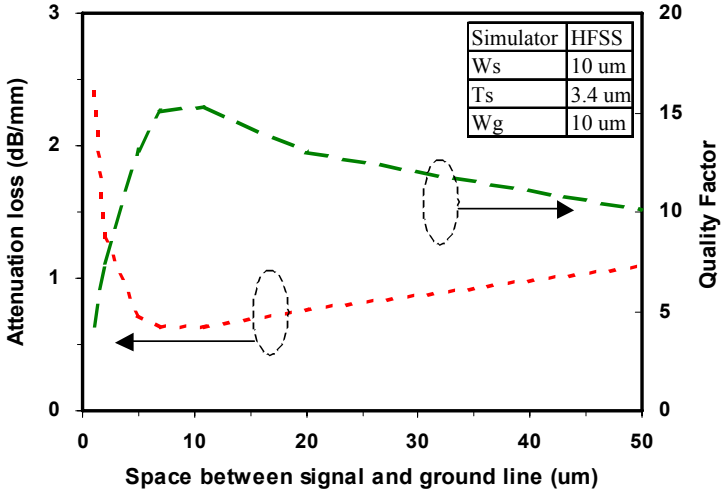
Fig. 2-1. The comparison of the measured and the simulated transmission line performance. (a) Attenuation loss versus frequency. (b) Quality factor versus frequency. (c) Effective relative permittivity versus frequency. (d) Wavelength versus frequency.



(a)

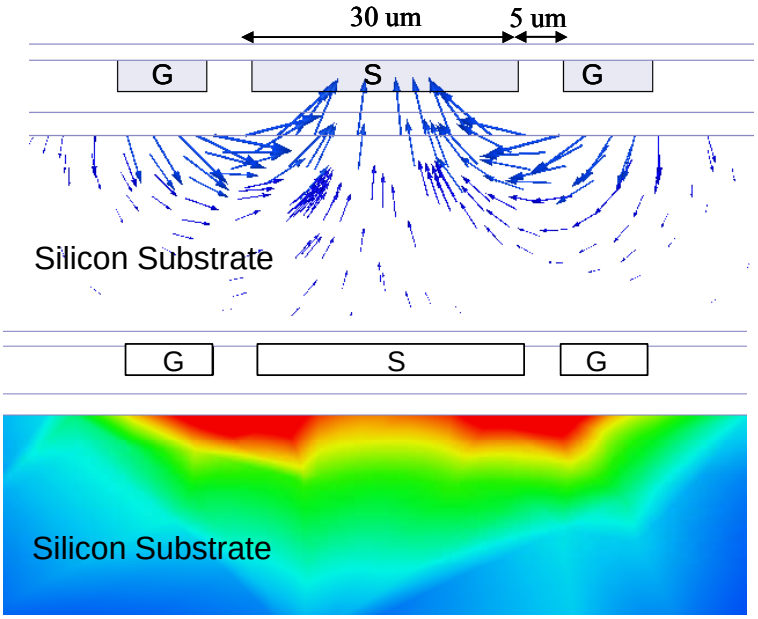


(b)

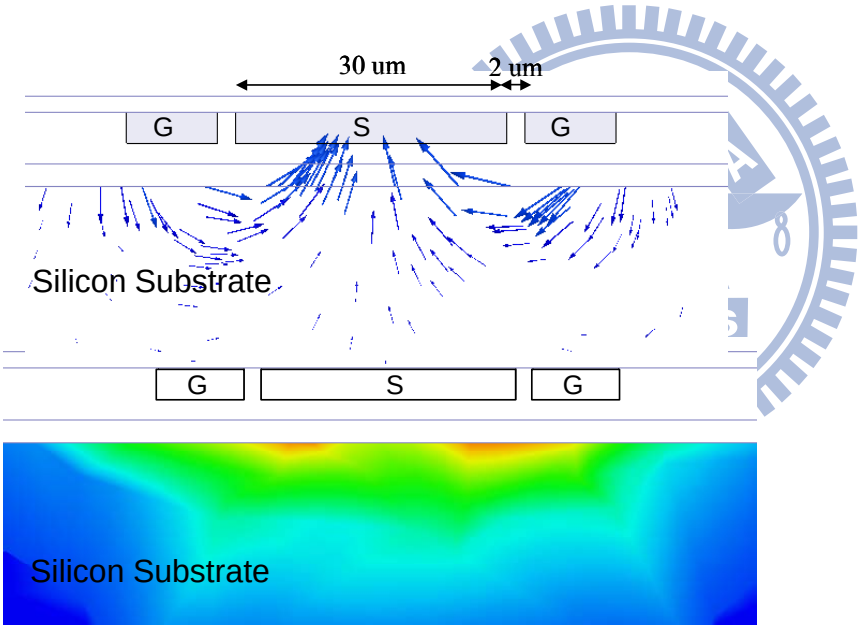


(c)

Fig. 2-2. The simulated CPW performance. (a) Attenuation loss and quality factor versus the width of the signal line. (b) Attenuation loss and quality factor versus the thickness of the signal line. (c) Attenuation loss and quality factor versus the space between the signal and the ground lines.

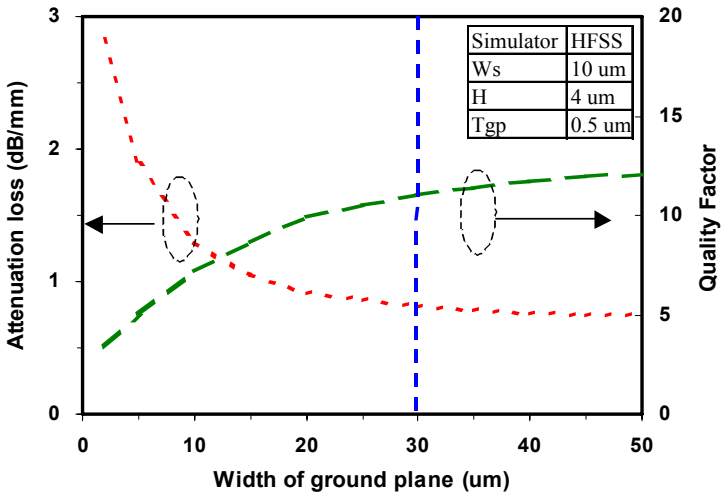


(a)

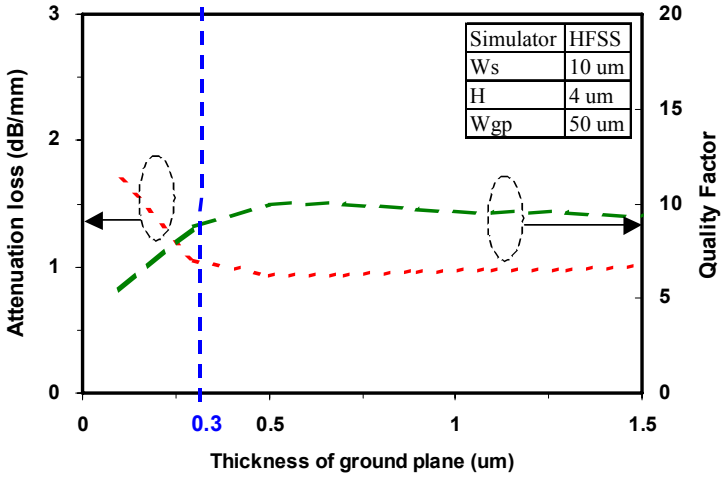


(b)

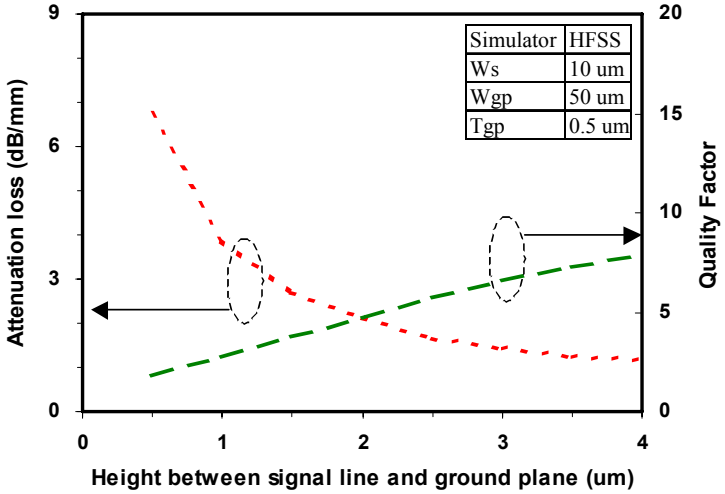
Fig. 2-3. The electric field intensity of the CPW transmission line for different spacings between the signal line and the ground line. (a) A signal line width of 30 um with a space of 5 um between the signal and the ground lines. (b) A signal line width of 30 um with a space of 2 um space between the signal and the ground lines.



(a)



(b)



(c)

Fig. 2-4. The simulated MS line performance. (a) Attenuation loss and quality factor versus the width of the ground plane. (b) Attenuation loss and quality factor versus the thickness of the ground plane. (c) Attenuation loss and quality factor versus the height between the signal line and the ground plane.

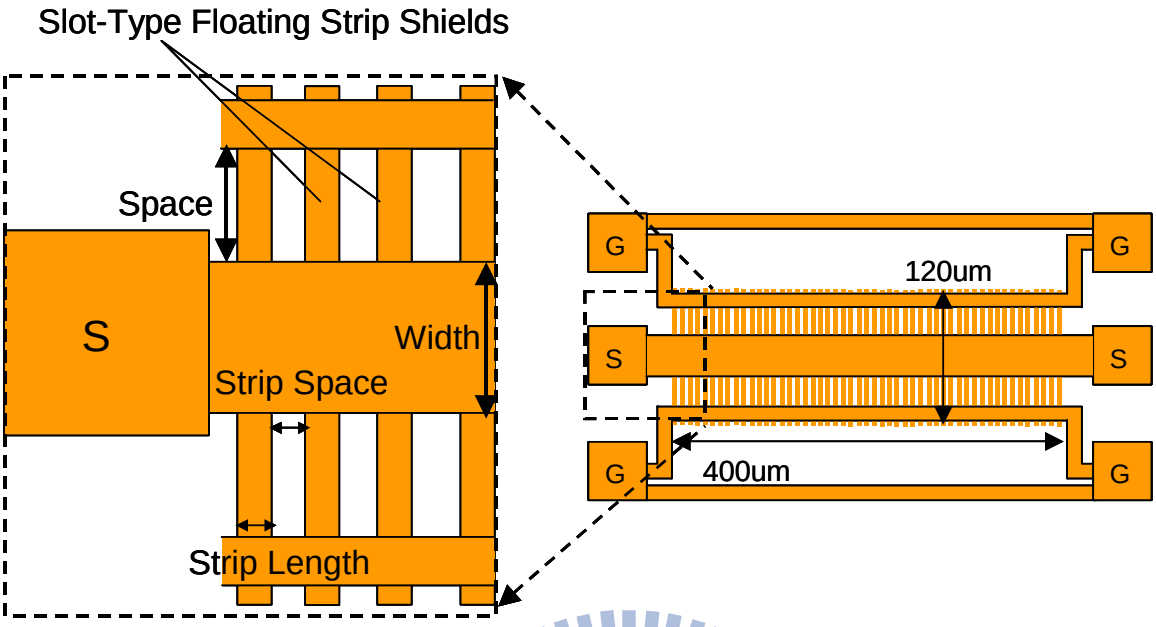
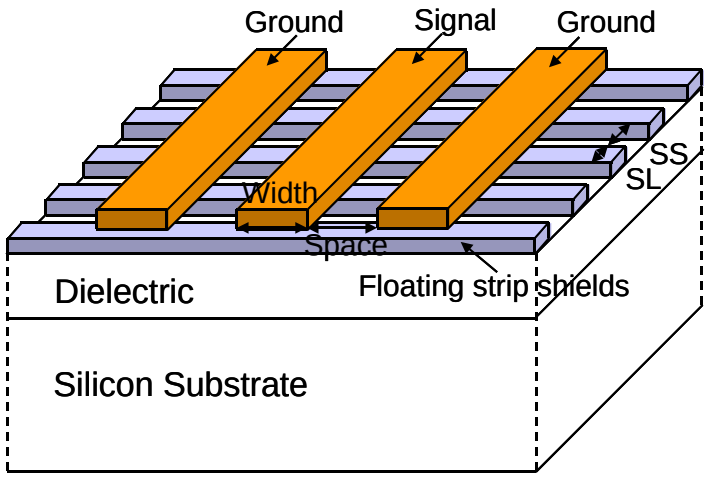
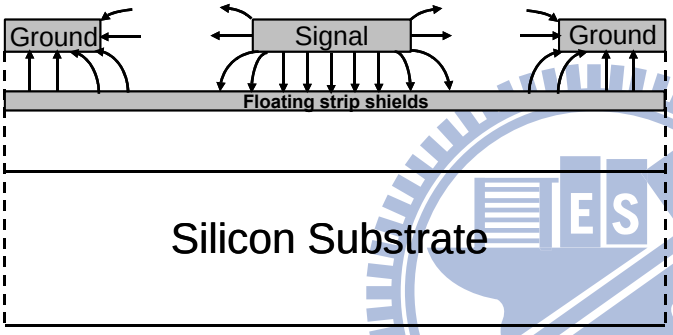


Fig. 2-5. The top view of a slow-wave CPW transmission line structure with slot-type floating shields.

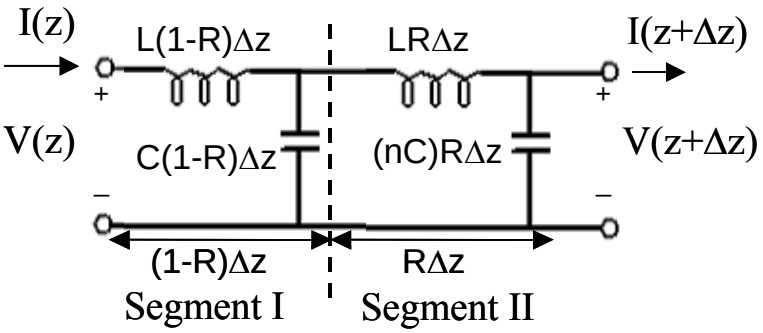


(a)

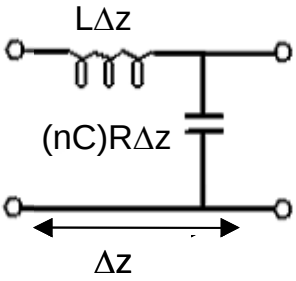


(b)

Fig. 2-6. A slow-wave CPW transmission line structure with slot-type floating shields. (a) A schematic view. (b) Electric field distribution from 3D EM simulation.



(a)



(b)

Fig. 2-7. The equivalent circuits for a slow-wave CPW transmission line. (a) The inductance and capacitance lumped-element equivalent circuit. (b) The cascaded equivalent circuit.

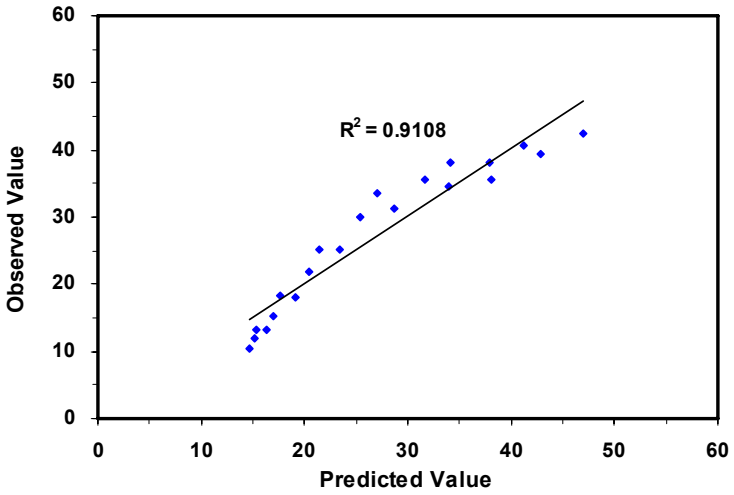
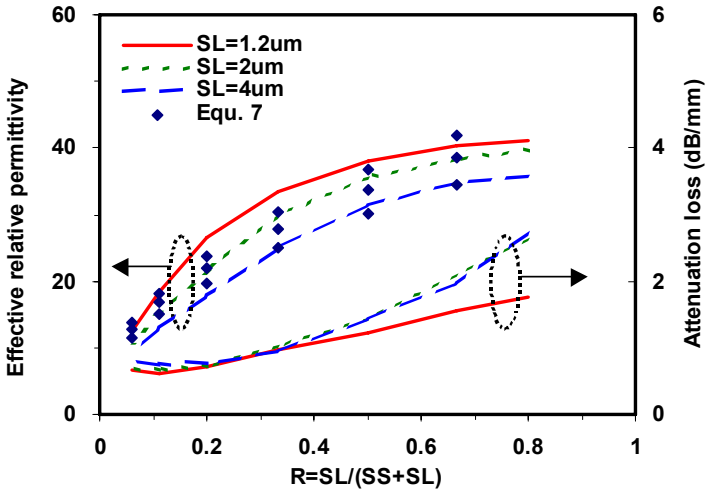
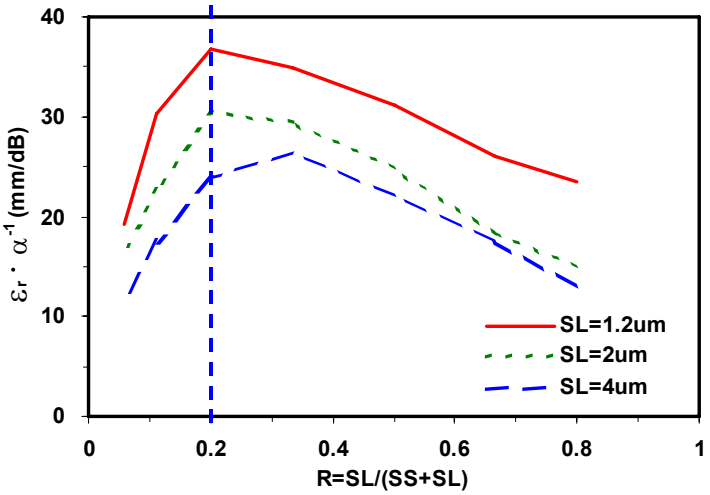


Fig. 2-8. A correlation of the semi-empirical equation.

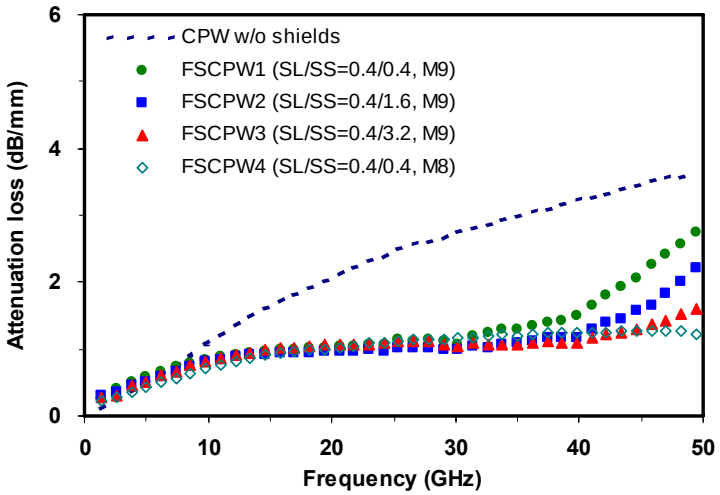


(a)

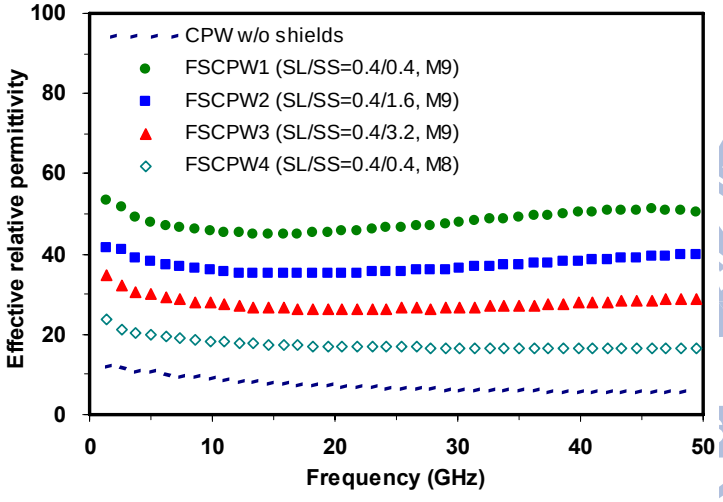


(b)

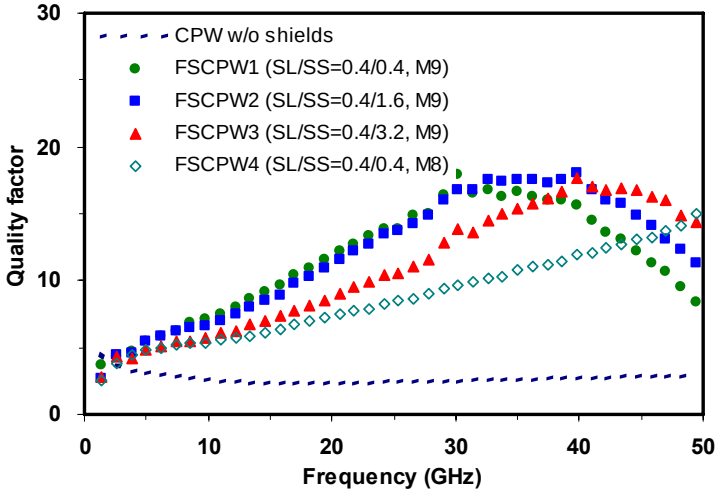
Fig. 2-9. The simulated slow-wave CPW transmission line performance versus parameter R with different SL values at a signal frequency of 50 GHz. (a) Effective relative permittivity and attenuation loss. (b) Optimization index value of $\varepsilon_r \cdot \alpha^{-1}$.


CPW w/o shields
FSCPW1 (SL/SS=0.4/0.4, M9)
FSCPW2 (SL/SS=0.4/1.6, M9)
FSCPW3 (SL/SS=0.4/3.2, M9)
FSCPW4 (SL/SS=0.4/0.4, M8)
Attenuation loss (dB/mm)
Frequency (GHz)
0
2
4
6
0
10
20
30
40
50

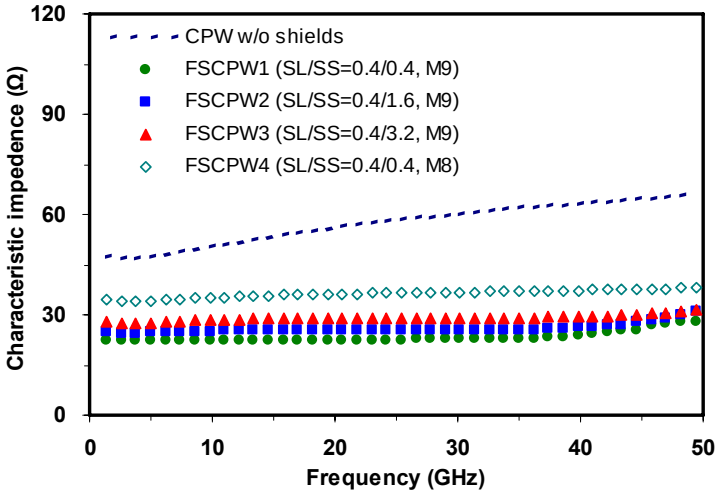
(a)


CPW w/o shields
FSCPW1 (SL/SS=0.4/0.4, M9)
FSCPW2 (SL/SS=0.4/1.6, M9)
FSCPW3 (SL/SS=0.4/3.2, M9)
FSCPW4 (SL/SS=0.4/0.4, M8)
Effective relative permittivity
Frequency (GHz)
0
20
40
60
80
100
0
10
20
30
40
50

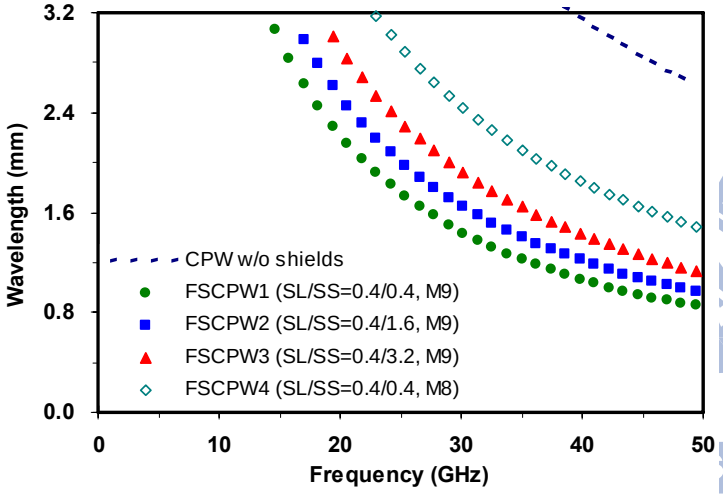
(b)


CPW w/o shields
FSCPW1 (SL/SS=0.4/0.4, M9)
FSCPW2 (SL/SS=0.4/1.6, M9)
FSCPW3 (SL/SS=0.4/3.2, M9)
FSCPW4 (SL/SS=0.4/0.4, M8)
Quality factor
Frequency (GHz)
0
10
20
30
0
10
20
30
40
50

(c)



(d)



(e)

Fig. 2-10. A comparison of the measured transmission line performance for different floating shields. (a) Attenuation loss versus frequency. (b) Effective relative permittivity versus frequency. (c) Quality factor versus frequency. (d) Characteristic impedance versus frequency. (e) Wavelength versus frequency.

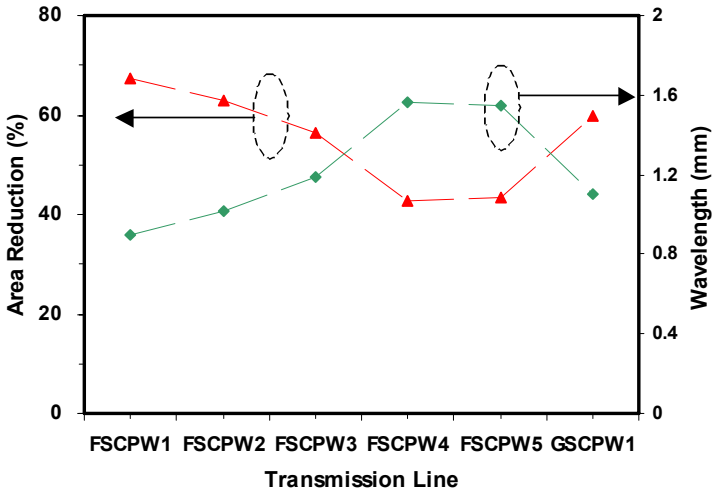
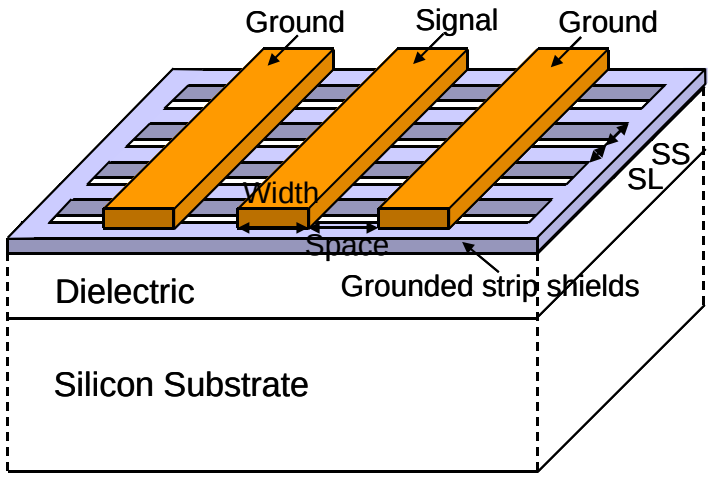
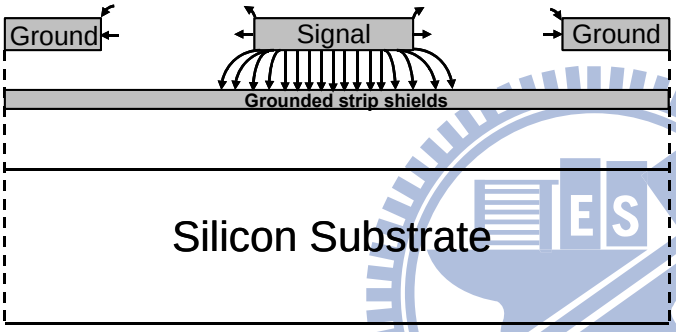


Fig. 2-11. The measured transmission line performance at 50GHz for each transmission line structure versus area reduction and wavelength.

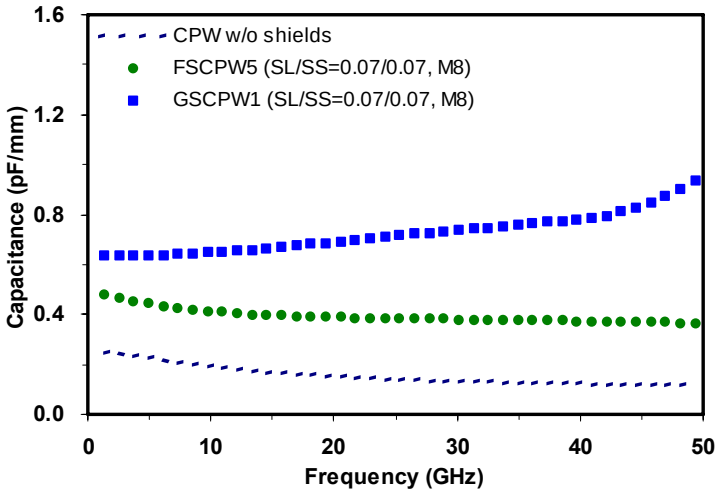


(a)

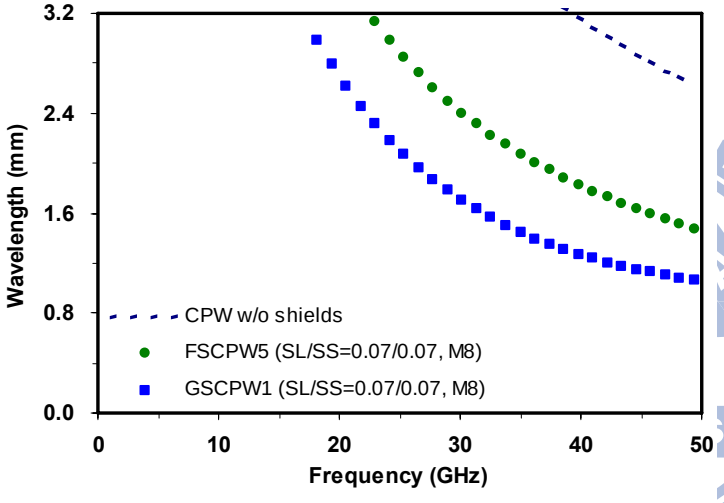


(b)

Fig. 2-12. A slow-wave CPW transmission line structure with slot-type grounded shields. (a) A schematic view. (b) Electric field distribution from 3D EM simulation.



(a)



(b)

Fig. 2-13. A comparison of the measured transmission line performance for floating shields and grounded shields. (a) Capacitance versus frequency. (b) Wavelength versus frequency.

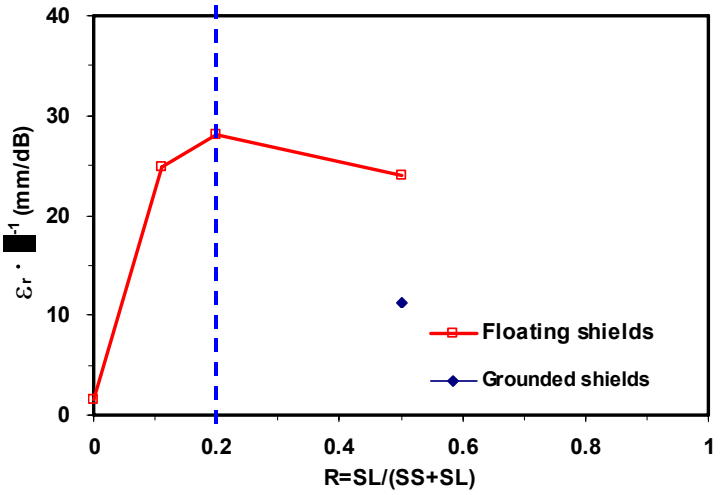


Fig. 2-14. The optimization index value of $\varepsilon_r \cdot \alpha^{-1}$ of the measured slow-wave CPW transmission line performance versus parameter R at a signal frequency of 50 GHz.

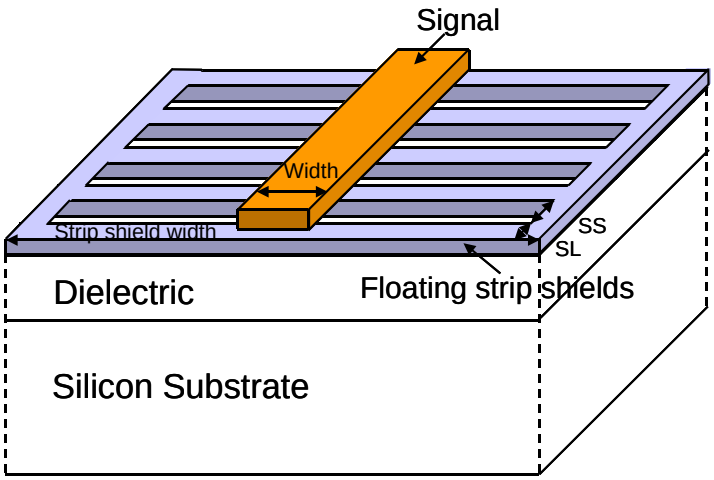
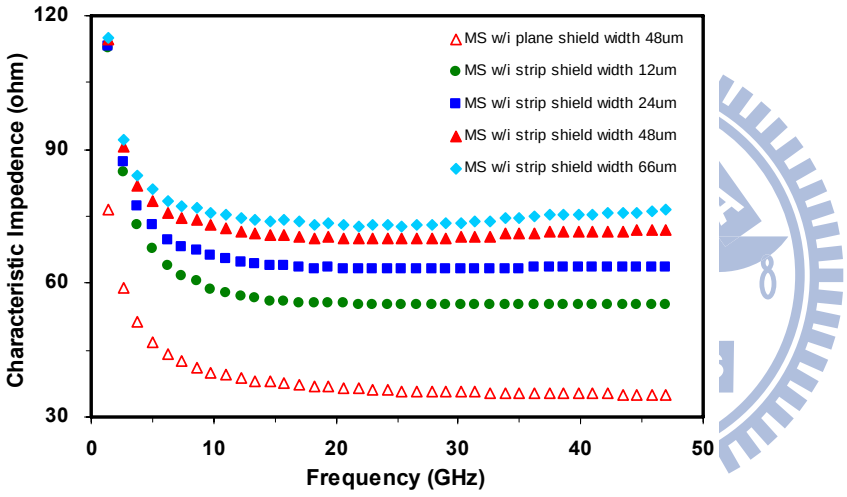
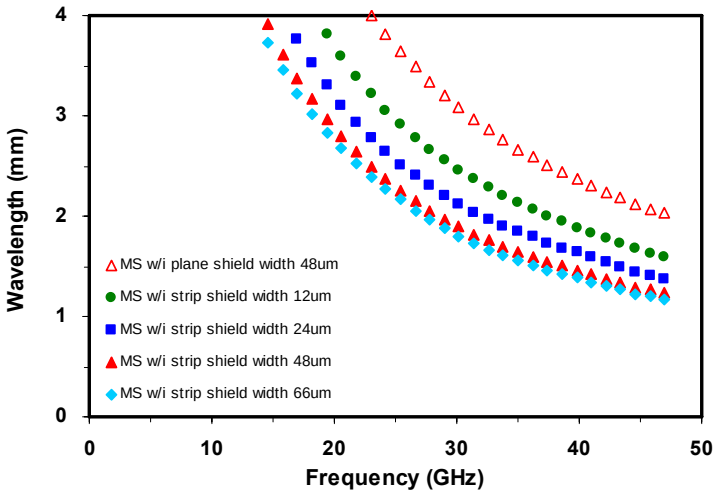


Fig. 2-15. A schematic view of a slow-wave MS transmission line structure



(a)



(b)

Fig. 2-16. A comparison of the measured transmission line performance using different strip shield widths. (a) Characteristic impedance versus frequency. (b) Wavelength versus frequency.

3 A Novel Transmission Line De-Embedding Technique for RF Device Characterization

3.1 The proposed de-embedding technique

A novel transmission line de-embedding technique is presented in this thesis. With this technique the left- and right-side ground-signal-ground (GSG) probe pads can be extracted directly using two transmission line test structures of length L and 2L. An additional through structure is designed using via stack de-embedding, which is unique amongst current de-embedding methods. The advantages of the proposed method include the following: (1) a smaller silicon area; (2) the consideration for discontinuity between the pad and interconnect; (3) the consideration for substrate coupling and contact effects; (4) the employment of via stack de-embedding; and (5) the solution to the over de-embedding. The proposed novel methodology is a great breakthrough in the area of ultra-high frequency de-embedding and should enable more accurate RF models to be developed.

3.1.1 Left- and right- GSG pad extraction

Figs. 3-1(a) and (b) illustrate the proposed de-embedding test structures. Two transmission lines of length L_1 and L_2 are designed in a GSG configuration. The discontinuity between the pad and interconnect is combined with that of the left- and right-side GSG pads. The transmission line structure is de-coupled into a series cascade of three two-port networks, including the left- and right-side GSG pads,

together with the intrinsic transmission line. If the length is properly designed as $L_1 = 2*L_2$, the multiplication sum of ABCD matrix $[P_{LEFT}]$ and $[P_{RIGHT}]$, can be extracted using the following:

$$[TL_{l_1}] = [P_{LEFT}][M_{l_1}][P_{RIGHT}] = [P_{LEFT}][M_{l_2}][M_{l_2}][P_{RIGHT}] \tag{8}$$

$$[TL_{l_2}] = [P_{LEFT}][M_{l_2}][P_{RIGHT}] \tag{9}$$

$$[P_{LEFT}][P_{RIGHT}] = [TL_{l_2}][TL_{l_1}]^{-1}[TL_{l_2}] = \begin{bmatrix} A_{LR} & B_{LR} \\ C_{LR} & D_{LR} \end{bmatrix} \tag{10}$$

where

$[P_{LEFT}]$ and $[P_{RIGHT}]$ are the ABCD matrices for the left- and right-side GSG pads.

$[TL_{l_1}]$ and $[TL_{l_2}]$ are the ABCD matrices for the transmission line structures of lengths L_1 and L_2.

$[M_{l_1}]$ and $[M_{l_2}]$ are the ABCD matrices for the intrinsic transmission line structures of lengths L_1 and L_2.

The left- and right-GSG pad structures are symmetrical and the equivalent circuit is illustrated in Fig 3-2. By definition [31], $[P_{LEFT}]$ and $[P_{RIGHT}]$ can be represented as:

$$[P_{LEFT}][P_{RIGHT}] = \begin{bmatrix} 1 & 1/Y_2 \\ Y_1 & 1+Y_1/Y_2 \end{bmatrix}\begin{bmatrix} 1+Y_1/Y_2 & 1/Y_2 \\ Y_1 & 1 \end{bmatrix} \tag{11}$$

$$\begin{bmatrix} 1 & 1/Y_2 \\ Y_1 & 1+Y_1/Y_2 \end{bmatrix}\begin{bmatrix} 1+Y_1/Y_2 & 1/Y_2 \\ Y_1 & 1 \end{bmatrix} = [TL_{l_2}][TL_{l_1}]^{-1}[TL_{l_2}] = \begin{bmatrix} A_{LR} & B_{LR} \\ C_{LR} & D_{LR} \end{bmatrix} \tag{12}$$

$$\begin{bmatrix} 1+2Y_1/Y_2 & 2/Y_2 \\ 2Y_1(1+Y_1/Y_2) & 1+2Y_1/Y_2 \end{bmatrix} = \begin{bmatrix} A_{LR} & B_{LR} \\ C_{LR} & D_{LR} \end{bmatrix} \tag{13}$$

Therefore, $[P_{LEFT}]$ and $[P_{RIGHT}]$ can be obtained using the following:

$$[P_{LEFT}] = \begin{bmatrix} 1 & B_{LR}/2 \\ C_{LR}/(1+(A_{LR}+D_{LR})/2) & 1+B_{LR}C_{LR}/2(1+(A_{LR}+D_{LR})/2) \end{bmatrix} \quad (14)$$

$$[P_{RIGHT}] = \begin{bmatrix} 1+B_{LR}C_{LR}/2(1+(A_{LR}+D_{LR})/2) & B_{LR}/2 \\ C_{LR}/(1+(A_{LR}+D_{LR})/2) & 1 \end{bmatrix} \quad (15)$$

After extracting $[P_{LEFT}]$ and $[P_{RIGHT}]$, the performance of both the transmission lines of lengths L_1 and L_2 can be extracted using the following, allowing for additional extraction data:

$$[M_{l_1}] = [P_{LEFT}]^{-1}[TL_{l_1}][P_{RIGHT}]^{-1} \quad (16)$$

$$[M_{l_2}] = [P_{LEFT}]^{-1}[TL_{l_2}][P_{RIGHT}]^{-1} \quad (17)$$

The detail matrix manipulation for equations (16) and (17) is shown in Figs. 3-3 and 3-4, respectively.

Since $[P_{LEFT}]$, $[P_{RIGHT}]$, $[M_{l_1}]$ and $[M_{l_2}]$ can be extracted, more variable combinations can be further cascaded to create more flexible de-embedding dummy structures, which can also lead to the creation of an additional through structure.

3.1.2 Via Stack De-embedding

The intrinsic DUT structure can be connected to the probe pads using either the high-level metallization layer or the low- to high-level metallization layer. Fig. 3-5(a) is a top view of the ABCD matrix $[A']$ of a DUT structure where the ABCD matrices $[Thru_{LEFT}]$ and $[Thru_{RIGHT}]$ are the left- and right-side interconnections. If the intrinsic DUT structure is placed on the top-level metallization layer, the RF DUT structure is connected to the probe pad using

high-level metallization. Top metallization are included along the B-E cut, as illustrated in Fig. 3-5(b). If the intrinsic DUT structure is placed on the inter-level metallization layer, Fig. 3-6(a) is a top view of the ABCD matrix $[A']$ of a DUT structure and the RF DUT structure is connected to the probe pad using low- to high-level metallization. First metallization, stacked metallization connected through via holes, and top metallization are included along the B-E cut, as illustrated in Fig. 3-6(b), using the proposed via stack de-embedding technique. An estimation based on resistance performance is obtained from EM simulation, and the resistance of the B-D cut over the B-E cut is around 40%, as illustrated in Fig. 3-7. It was proved that the parasitic contribution of the interconnection and via, etc., cannot be ignored, especially in the high-frequency range. The ratio would be higher if either low-level metallization M1 or a shorter length D-E is involved. Since the minimum interconnect length between two ports is around 40um, probe-to-probe coupling with such short interconnect could be a potential limitation. For medium or large devices, or small-cascaded devices, the distance between two ports in Fig. 3-6(a) is above 100 um. Therefore, it is necessary to design a good "through" test structure in order to obtain stable measurement results. The top view of one additional through structure is designed as Fig. 3-8(a), and the cross-sectional view is designed as Fig. 3-8(b) and Fig. 3-9(b), respectively, if the intrinsic DUT is connected to the probe pads using the high-level metallization layer or the low- to high-level metallization layer. The ABCD matrix of the additional through structure $[THRU]$ is equal to $[TL_{LEFT}][Thru_{LEFT}][Thru_{RIGHT}][P_{RIGHT}]$,

where the ABCD matrix $[TL_{LEFT}]$ is the left-side transmission line of length L_2 and is equal to $[TL_{l_2}][P_{RIGHT}]^{-1}$, as shown in Fig. 3-10(c). The optimized length of L_2 is designed based on two criteria: (1) The maximum length cannot be too long because the parasitics of interest will represent a smaller faction of the measured structure, and (2) The minimum length cannot be so short as to decrease probe-to-probe coupling.

$[Thru_{LEFT}][Thru_{RIGHT}]$ can be extracted from the following equation and the corresponding explanation is illustrated in Fig. 3-10:

$$[Thru_{LEFT}][Thru_{RIGHT}] = [TL_{LEFT}]^{-1}[THRU][P_{RIGHT}]^{-1} \tag{18}$$

Using equations (14) and (15), the matrices $[Thru_{LEFT}]$ and $[Thru_{RIGHT}]$ can be calculated, respectively. The length of $[Thru_{LEFT}]$ and $[Thru_{RIGHT}]$ cannot be too long in order to maintain the validity of the de-embedding technique when high frequencies are involved. After determining $[P_{LEFT}]$, $[Thru_{LEFT}]$, $[Thru_{RIGHT}]$, and $[P_{RIGHT}]$, the ABCD matrix $[A]$ of the intrinsic DUT structure can be extracted using equation (12) through the matrix manipulation of the ABCD matrix $[A']$ of the DUT structure with the left- and right-side interconnections and the left- and right-side GSG pad, as shown in Fig. 3-10(a). The proposed de-embedding method can also be used with asymmetrical DUT structures by designing another through dummy structure:

$$[A] = [P_{LEFT}]^{-1}[Thru_{LEFT}]^{-1}[A'][Thru_{RIGHT}]^{-1}[P_{RIGHT}]^{-1} \tag{19}$$

3.1.3 De-embedding procedure

The proposed de-embedding procedure involves the following steps:

1) Measurement of the scattering matrices of the transmission lines of lengths L_1 and L_2, the one additional through structure, and the DUT structure, as shown in Figs. 3-1(a), 3-1(b), 3-10(b), and 3-5(a), respectively.

2) Conversion of the scattered matrices of the transmission lines of lengths L_1 and L_2, the one additional through structure, and the DUT structure to their ABCD matrices $[TL_{l_1}], [TL_{l_2}], [THRU]$, and $[A']$, respectively.

3) Calculation of the ABCD matrices of the left- and right-side GSG pads $[P_{LEFT}]$ and $[P_{RIGHT}]$, respectively, using (8)-(15).

4) Calculation of the ABCD matrices of the left- and right-side through $[Thru_{LEFT}]$ and $[Thru_{RIGHT}]$, respectively, using (18), and (14)-(15).

5) Calculation of the ABCD matrix $[A]$ of the intrinsic DUT structure using (19).

3.1.4 Simulation Results

A capacitor device is chosen as the subject of a study to compare with and without via stack de-embedding methods. The schematic view of the capacitor structure is designed as Fig. 3-11(a), and the cross-sectional view is illustrated as Fig. 3-11(b), where the intrinsic capacitor is connected to the probe pads using the low- to high-level metallization layer. The B-E cut is de-embedded using the via

stack technique, while the D-E cut is de-embedded without the via stack technique. As the ideal de-embedded data are known, the comparative results based on the 40% resistance ratio of the B-D cut over B-E cut are shown in Fig. 3-12. It can be seen that there is an obvious improvement in accuracy and capacitance performance using the via stack de-embedding method.

3.2 Experimental Results

3.2.1 Comparative results of de-embedding techniques

One open, one short, and two microstrip transmission lines of lengths L_1=1000 um and L_2=500 um were designed. The S-parameters of the transmission line DUT structures were measured up to 50 GHz using an Agilent 8510C. The proposed test structures were fabricated using 65nm RF-CMOS technology. The results of a comparison of the proposed technique denoted as De-embedding_L2L, the Mangan's method [49] denoted as De-embedding_LS, an open-short de-embedding technique denoted as De-embedding_OS, and an EM simulation are shown in Fig. 3-13. Less resistance and inductance values remain after the conventional open-short de-embedding is performed. An extra grounded metal strip of the short structure results in over de-embedding. The over de-embedding phenomenon in both the x and y direction in the short dummy structure, as illustrated in Figs 3-14 and 3-15, cannot be ignored, especially for large RF devices. The transmission line suffers from over de-embedding significantly in the x

direction, as proven in Fig. 3-13, which reveals an adequate agreement between the proposed de-embedding technique and EM simulation.

In general, the assumption for lumped-equivalent-circuit-model-based techniques is valid only if the lengths of the DUT devices are much smaller than the distances between port1 and port2. However, this is not always true for larger DUT devices and may result in over de-embedding when intrinsic device performance is involved. Therefore, the proposed de-embedding technique can address the problem of over de-embedding. Moreover, it can be considered to be the best choice when larger DUT devices are involved, such as transmission lines, inductors, and MOSFETs with larger widths. As the left- and right-side GSG pads are extracted directly, in addition to substrate coupling and contact effects provided by a four-step de-embedding method [36], the proposed method accounts for the discontinuity between the pad and interconnect.

3.2.2 The applications for the proposed de-embedding method and slow-wave CPW transmission lines

Intrinsic slow-wave CPW transmission line structures with above and below slot-type floating shields are placed on the inter-level metallization layers, as shown in Fig. 3-16. They are the most appropriate RF device for the proposed de-embedding methods involving the via stack de-embedding technique.

Two types of transmission lines were fabricated, as listed in Table 3-1, including (1) a coplanar waveguide transmission line without shields (CPW) and (2)

three slow-wave CPW transmission lines with slot-type floating shields (FSCPW1, FSCPW2, and FSCPW3), as shown in Fig. 3-17. A slow-wave CPW transmission line was designed where slot-type floating shields are located periodically both above and below the CPW structure, and they are oriented transversely to the CPW structure. For all the transmission lines listed in Table 3-1, the CPW structure is formed on the eighth (M8) metal layer and the lower slot-type shields are created on either the seventh (M7) or second (M2) metal layer. The CPW part has a signal/ground line width of 10 um/10 um, with a 20 um space between the signal and ground lines. The upper floating shields are formed on the ninth (M9) metal layer with a fixed strip length (SL) of 2 um and a fixed strip space (SS) of 2 um. The SL of lower floating shields is designed to be the minimum length required to achieve a high performance with minimal eddy-current loss. The lower slot-type floating shields are designed with the following dimension splits: (1) the SL on M7 is 0.1 um and the accompanying SS is either 0.1 um or 0.9 um, and (2) the SL on M2 is 0.1 um and the accompanying SS is 0.1 um.

The experimental results are obtained using the proposed de-embedding technique. Fig. 3-18(a) shows that the attenuation loss of FSCPW3 is lower than that of FSCPW1, because the dielectric thickness between the signal line on M8 and the floating shields on M2 is greater than the dielectric thickness between the signal line on M8 and the floating shields on M7. These results indicate that the currently prevalent opinion that highest-density shields are the best choice [9] is not always true. As frequencies increase, lower density coverage FSCPW2 exhibits

a lower attenuation loss than FSCPW1. In summary, the smaller the SL, and the greater the thickness between the signal line and the floating shields, the lower the induced attenuation loss will be obtained.

Fig. 3-18(b) shows that lower characteristic impedance can be achieved by increasing floating shield density or by raising the position of the metal layer. Characteristic impedance tuning by changing the metal density and the position of the metal layer in the slot-type floating shields offers a new design approach.

The wavelength of a transmission line indicates whether or not the transmission line design is compact. Therefore, the wavelengths of transmission lines with a variety of slot-type floating shield designs are compared in Fig. 3-18(c). From this, it can be seen that the best choice is FSCPW1 whose wavelength is reduced to 1.19 mm; that is, by a factor of more than 3 when compared to that of a conventional CPW transmission line with a wavelength of 3.58 mm. As a result, a reduction in silicon area of more than 66% can be achieved, which demonstrates that this approach is potentially highly attractive for MMIC applications.

An optimized design requires a good quality factor, such as $Q = \frac{\beta}{2\alpha}$ where β is the phase constant and α is the attenuation loss, and it should be used to judge an overall trade-off between attenuation loss and wavelength. Guidelines for designing a transmission line with a high quality factor are illustrated in Fig. 3-18(d). It can be seen from this that FSCPW1 is the most appropriate choice for designs operating at frequencies below 50 GHz. As discussed above and

demonstrated in the experiments, the lower the attenuation loss, the longer the wavelength is usually obtained. Therefore, a designer must weigh up the pros and cons between SL and SS dimensions together with metal layer positions in order to design a suitable slow-wave CPW to achieve a functional circuit at the desired operating frequency.

3.2.3 Optimized simulation for slot-type floating shields in transmission lines

The optimization of slot-type floating shields to reduce simultaneously attenuation loss and wavelength is performed. Optimization analyses on SL, SS, and the position of floating shields are conducted by analyzing the EM simulation results. The density, *R*, of the slot-type floating shields is defined as follows:

$$R = \frac{SL}{SL + SS}$$

Fig. 3-19(a) indicates that a higher effective relative permittivity is achieved with a smaller *SL*, higher density *R*, and smaller dielectric thickness between the signal line and the floating shields. When the attenuation loss is taken into consideration, a minimized *SL* is the best choice for both effective relative permittivity and attenuation loss performance. The optimization index of the slot-type floating shields is defined as $\varepsilon_r \cdot \alpha^{-1}$ in mm/dB, and Fig. 3-19(b) shows that an optimized performance is achieved when the density R is equal to 0.33 (SL=1 um and SS=2 um) on M7. The optimized floating shields include a minimized SL, medium density R, and high metal layer position. After the specification

requirements for the attenuation loss is determined, the density of the slot-type floating shields can be calculated. Consequently, the effective relative permittivity can be predicted from the minimized SL and the density of the slot-type floating shields. Since both SL and the SS can be adjusted in accordance with technology scaling, a scaled slow-wave CPW can continue to offer lower attenuation loss and higher effective relative permittivity.

3.3 Conclusion

Conventional de-embedding methods suffer from an over de-embedding problem to which the proposed method offers a solution. In addition to the substrate coupling and contact effects provided by existing four-step de-embedding methods, the proposed method also accounts for the discontinuity between the pad and interconnect. Current de-embedding techniques do not de-embed via stack parasitic and the contribution of the proposed method becomes more important as frequency increases. As $[P_{LEFT}]$,$[P_{RIGHT}]$, $[M_{l_1}]$ and $[M_{l_2}]$can be extracted, more flexible de-embedding dummy structures can be created. Therefore, an additional through structure can be designed to perform via stack de-embedding. The proposed de-embedding method can be extended to other RF devices and, this will allow for more accurate RF device characterization. Intrinsic slow-wave CPW transmission line structures are placed on the inter-level metallization layers as they are the most appropriate RF device for cascade-based de-embedding methods involving the via stack de-embedding technique. The proposed floating slow-wave

CPW transmission line where slot-type floating shields are located periodically both above and below the CPW structure has a better quality factor of 15 at 50 GHz and a shorter wavelength, which results in a reduction of silicon area of more than 66% when compared to that of conventional CPW transmission lines. In short, a significant advantage for future technology scaling and RF circuit designing is made available through the use of more suitable SL and SS dimensions.

Name	Transmission Line Type	Metal Shield Layer	Strip Length (SL)	Strip Space (SS)	Shield Type
CPW	CPW	No strip shields			
FSCPW1	Floating slow-wave CPW	M9, M7	0.1um	0.1um	floating
FSCPW2	Floating slow-wave CPW	M9, M7	0.1um	0.9um	floating
FSCPW3	Floating slow-wave CPW	M9, M2	0.1um	0.1um	floating

Table 3-1. CPW-type transmission line structures

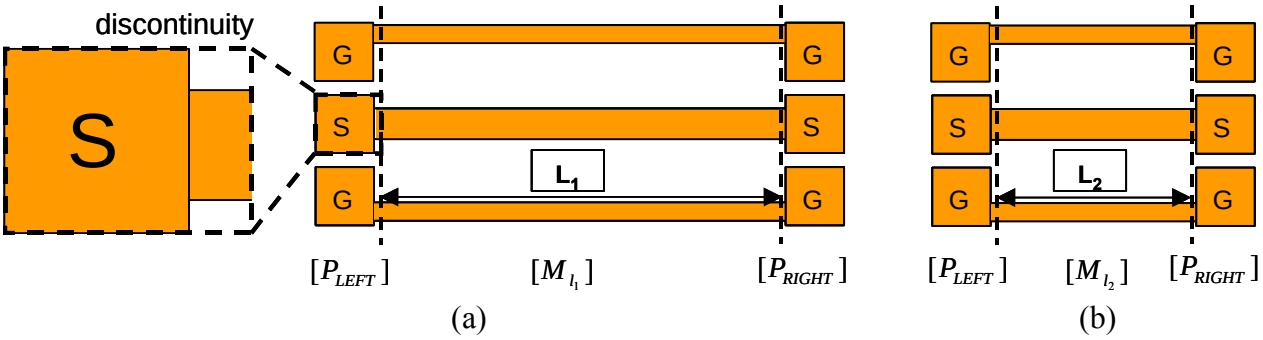


Fig. 3-1. Two transmission lines of lengths L_1 and L_2 are designed in a GSG configuration.. (a) A transmission line of length L_1 $[TL_{l_1}]$, and (b) A transmission line of length L_2.

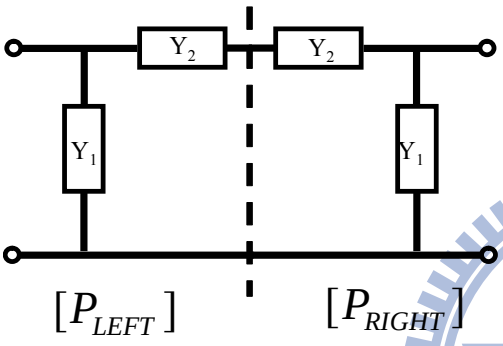
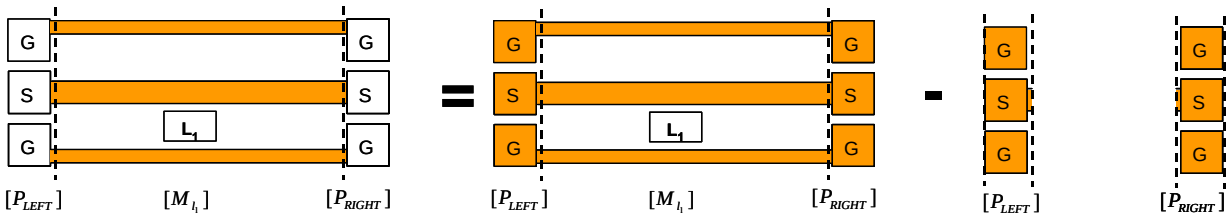
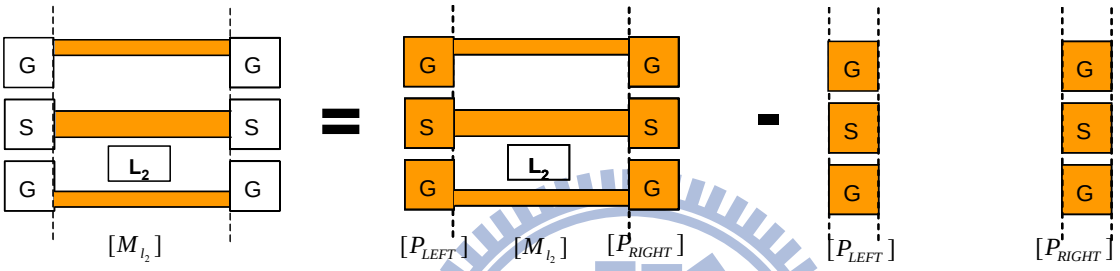


Fig. 3-2. An equivalent representation of a symmetrical structure.



(a) (b) (c)

Fig. 3-3. The matrix manipulation for a transmission line of length L_1 in conjunction with two GSG pads, $[P_{LEFT}]$ and $[P_{RIGHT}]$ (a) An intrinsic transmission line of length L_1 (b) A transmission line of length L_1 (c) Two GSG pads.



(a) (b) (c)

Fig. 3-4. The matrix manipulation for a transmission line of length L_2 in conjunction with two GSG pads, $[P_{LEFT}]$ and $[P_{RIGHT}]$ (a) An intrinsic transmission line of length L_2 (b) A transmission line of length L_2 (c) Two GSG pads.

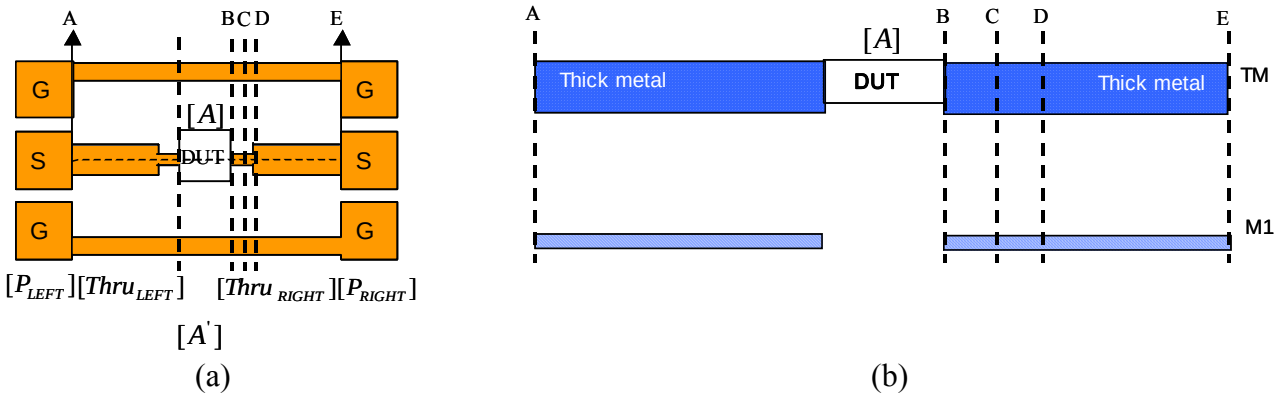


Fig. 3-5. The connection using the high-level metallization layer. (a) The top view of the ABCD matrix $[A']$ of the DUT structure, and (b) The cross-section along the A- E cut.

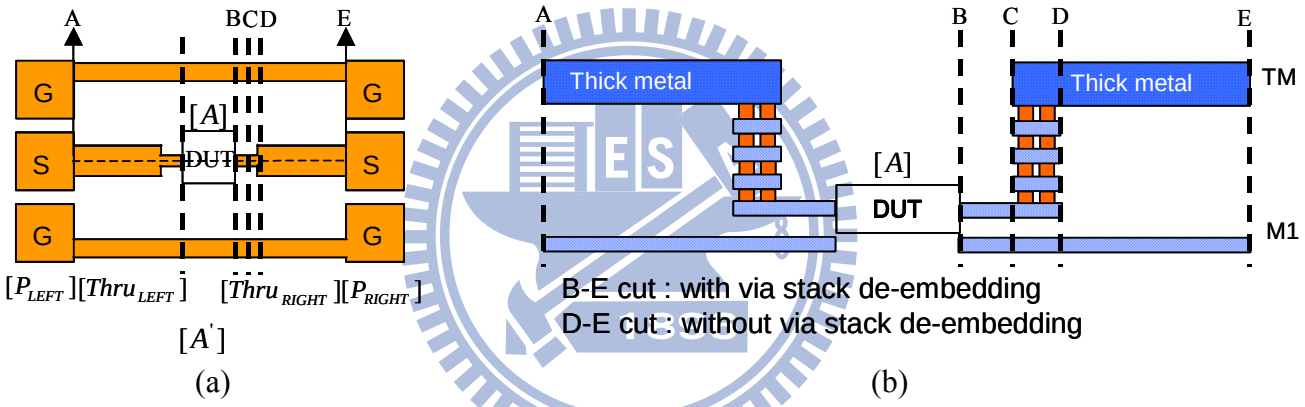


Fig. 3-6. The connection using the low- and high-level metallization layers. (a) The top view of the ABCD matrix $[A']$ of the DUT structure, and (b) The cross-section along the A- E cut.

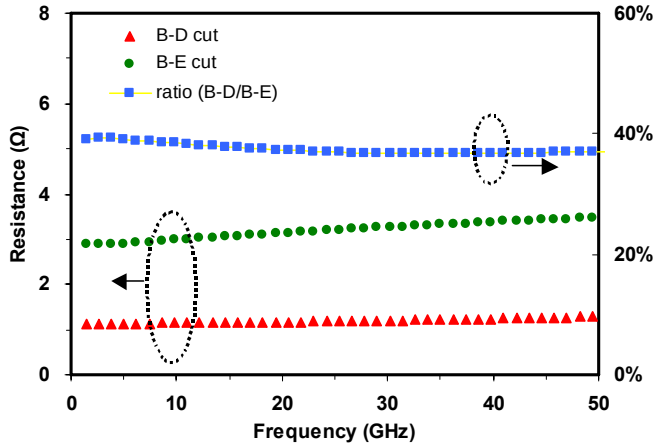


Fig. 3-7 An estimation of the resistance ratio of B-D cut to the B-E cut using EM simulation.

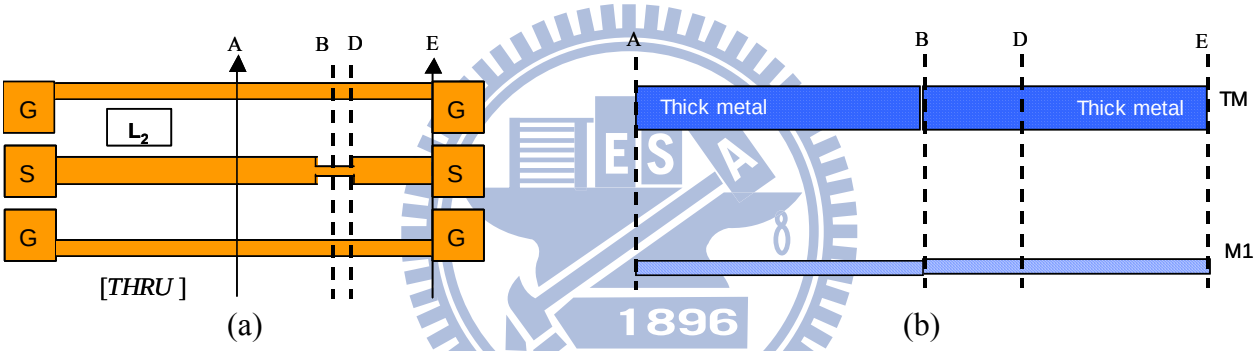


Fig. 3-8. The connection using high-level metallization layers. (a) The top view of the through structure, and (b) The cross-sectional view along the A- E cut.

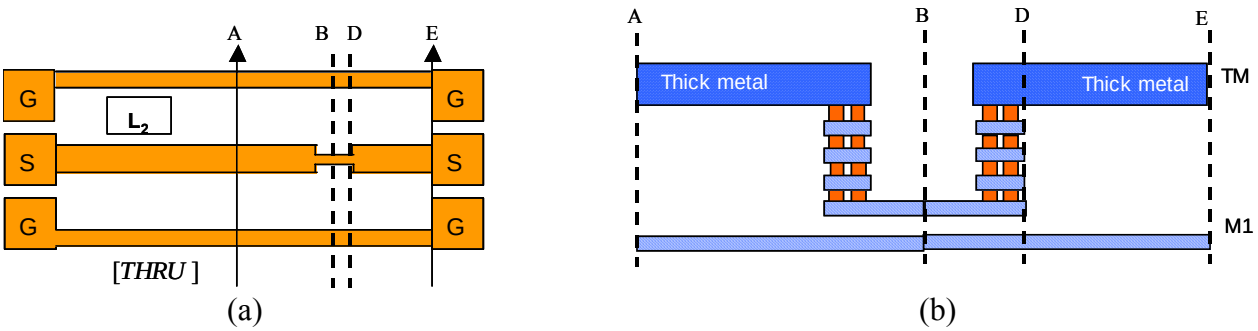


Fig. 3-9. The connection between the low- and high-level metallization layers. (a) The top view of the DUT structure, and (b) The cross-sectional view along the A- E cut.

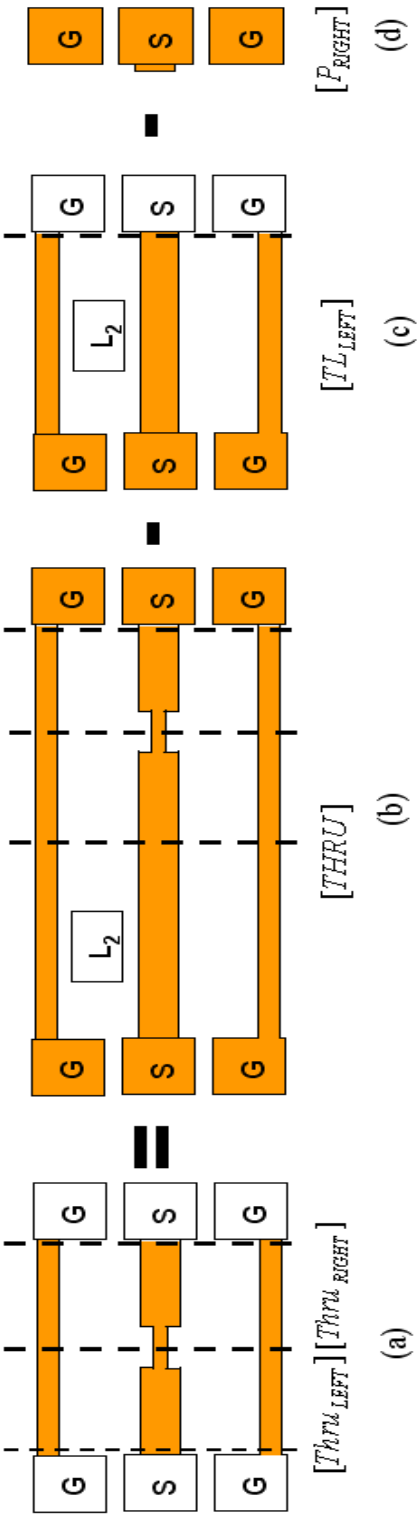
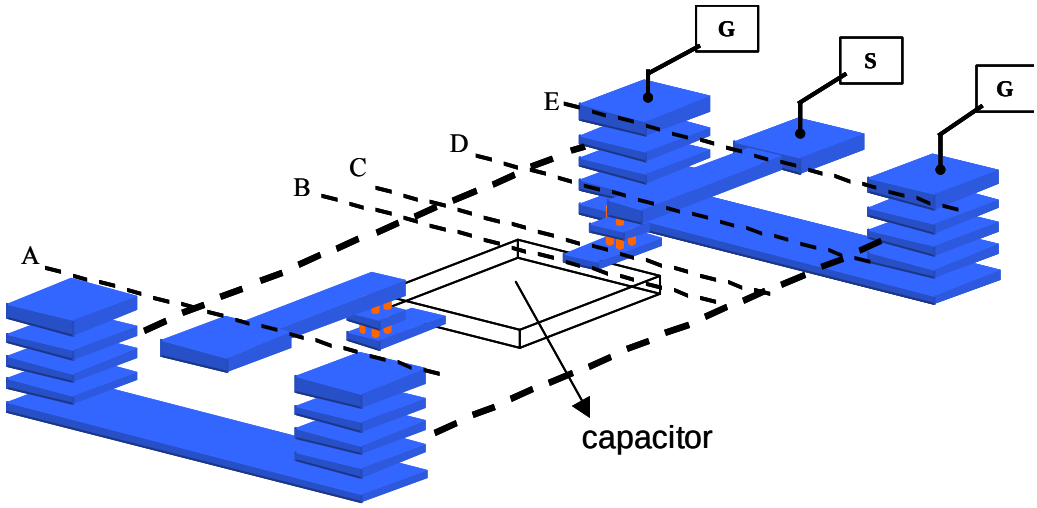
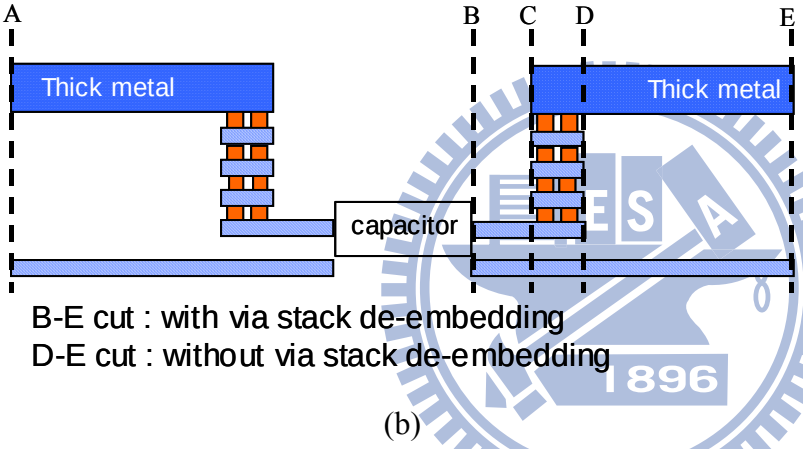


Fig. 3-10. The matrix manipulation for the series cascade of $[Thru_{LEFT}][Thru_{RIGHT}]$ with $[THRU]$, $[TL_{LEFT}]$, and $[P_{RIGHT}]$. (a) The cascade of $[Thru_{LEFT}][Thru_{RIGHT}]$, (b) One additional through structure $[THRU]$, (c) The left-side transmission line of length L_2 $[TL_{LEFT}]$, and (d) The right-side GSG pad $[P_{RIGHT}]$.

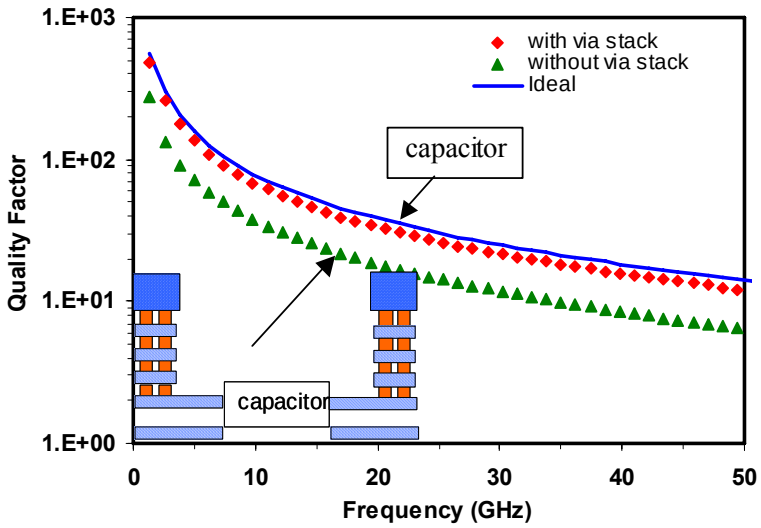


(a)

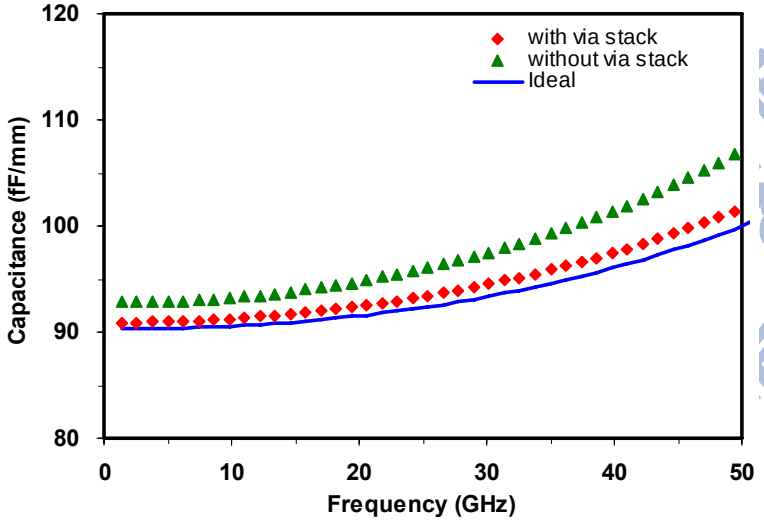


(b)

Fig. 3-11. The connection between the low- and high-level metallization layers. (a) The schematic view of the a capacitor structure, and (b) The cross-sectional view along the A- E cut.

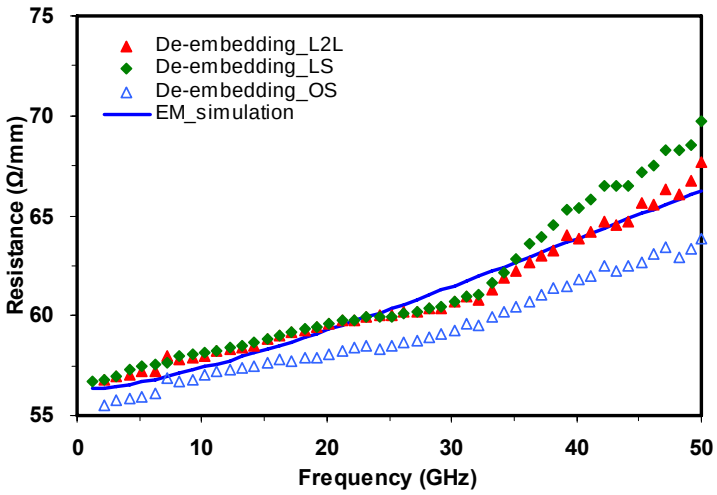


(a)

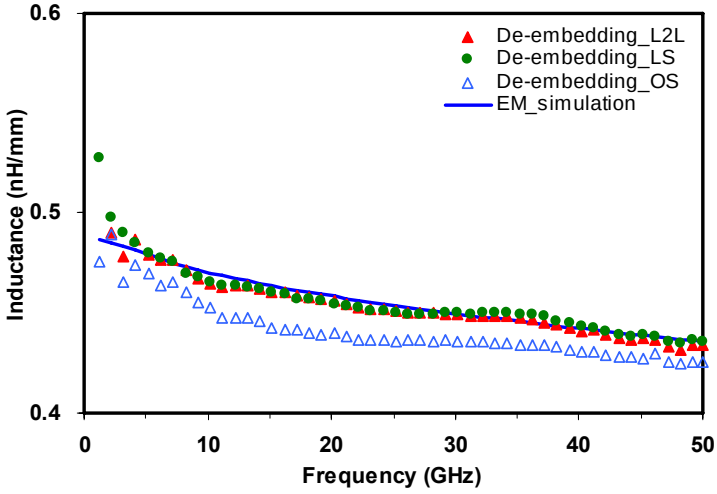


(b)

Fig. 3-12. A comparison of the simulated capacitor performances for via stack de-embedding with and without via stack de-embedding (a) Quality factor versus frequency, and (b) Capacitance versus frequency.

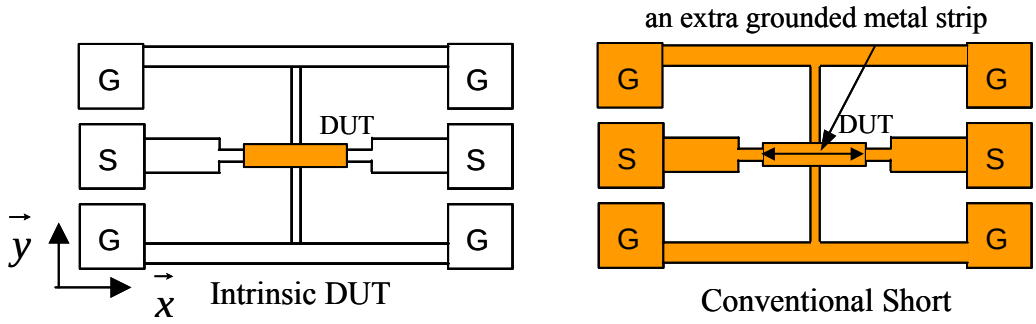


(a)



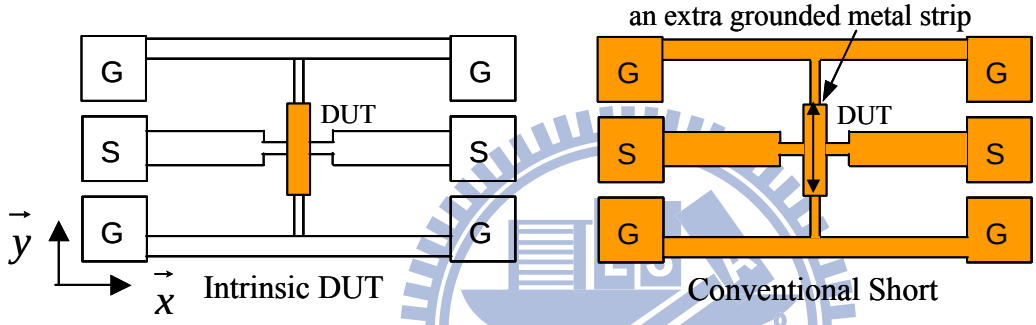
(b)

Fig. 3-13. A comparison of the measured transmission line performances for De-embedding_L2L, De-embedding_LS [14], De-embedding_OS, and EM simulation with(a) Resistance versus frequency, and (b) Inductance versus frequency.



(a) (b)

Fig. 3-14. A long and thin structure in the x direction. (a) The RF DUT structure. (b) The conventional short structure.



(a) (b)

Fig. 3-15. A long and thin structure in the y direction. (a) The RF DUT structure. (b) The conventional short structure.

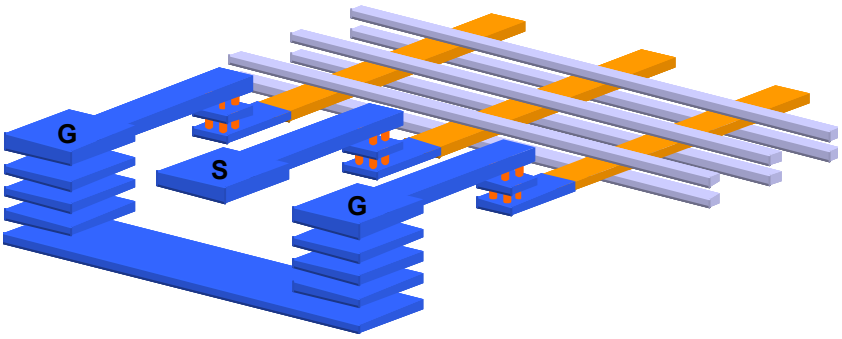


Fig. 3-16: A schematic view of a slow-wave CPW transmission line with above and below slot-type floating shields.

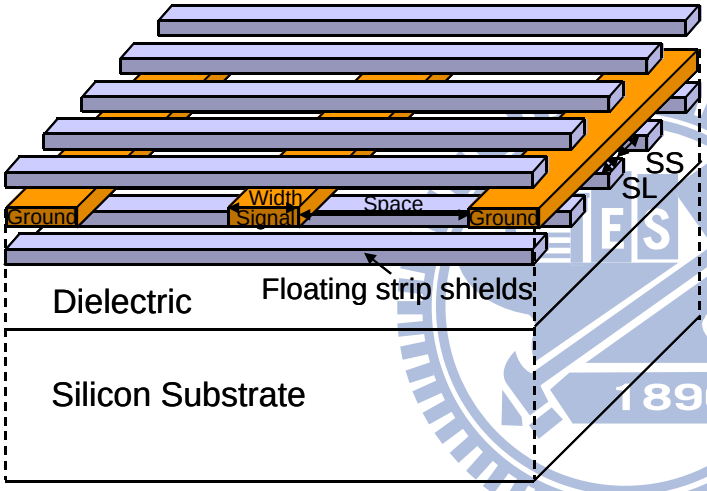
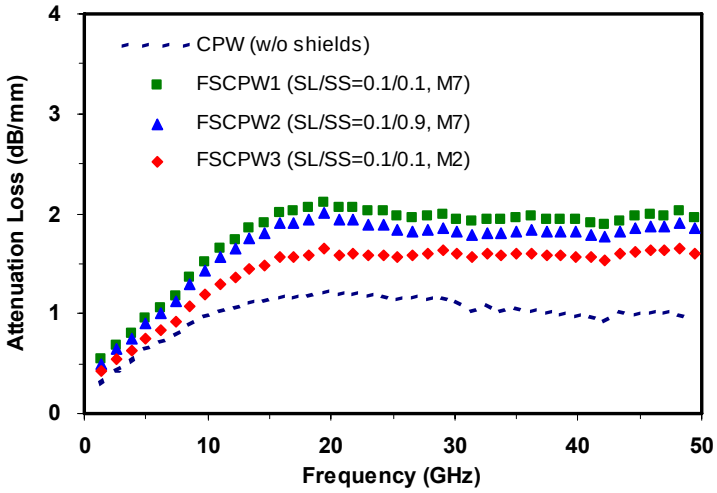
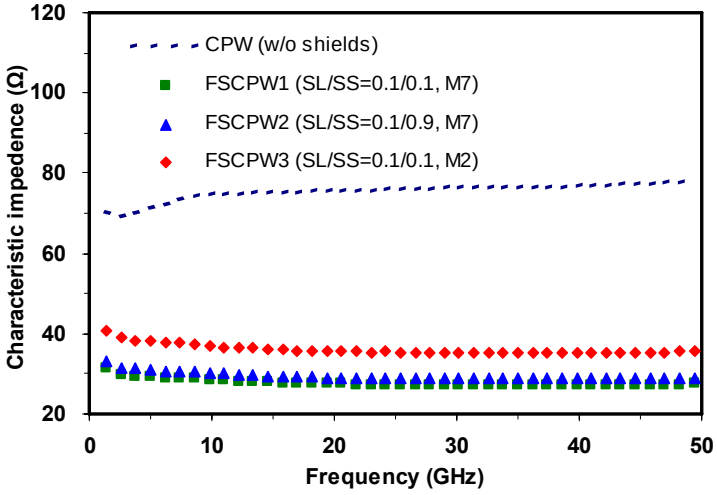


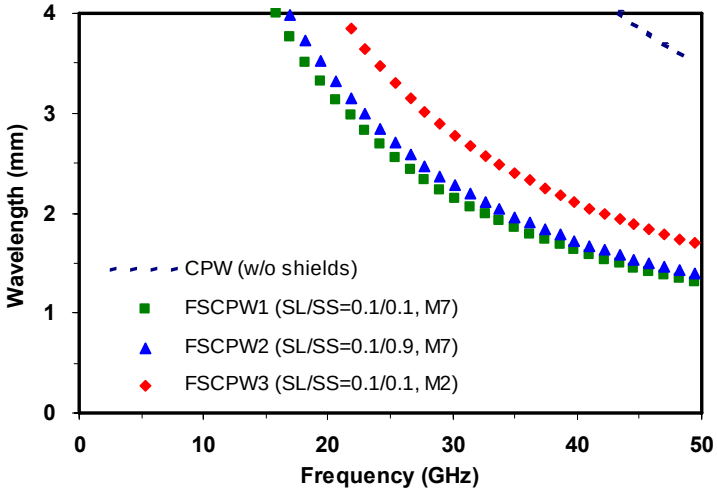
Fig. 3-17: A schematic view of a slow-wave CPW transmission line with above and below slot-type floating shields.


CPW (w/o shields)
FSCPW1 (SL/SS=0.1/0.1, M7)
FSCPW2 (SL/SS=0.1/0.9, M7)
FSCPW3 (SL/SS=0.1/0.1, M2)
Attenuation Loss (dB/mm)
Frequency (GHz)
0
1
2
3
4
0
10
20
30
40
50

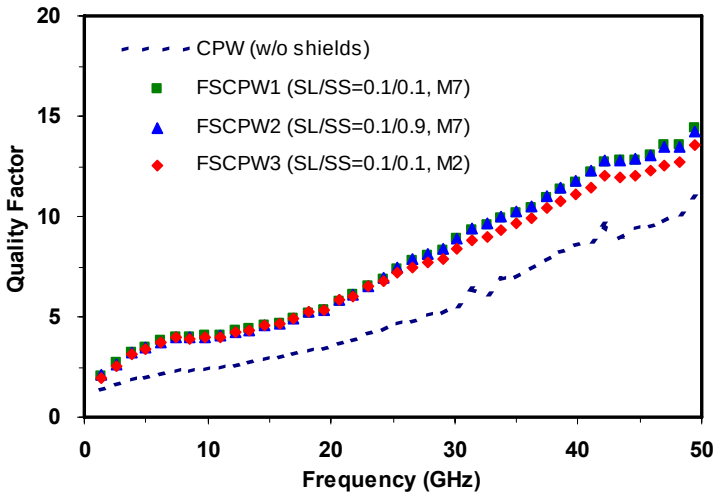
(a)


CPW (w/o shields)
FSCPW1 (SL/SS=0.1/0.1, M7)
FSCPW2 (SL/SS=0.1/0.9, M7)
FSCPW3 (SL/SS=0.1/0.1, M2)
Characteristic impedence (Ω)
Frequency (GHz)
20
40
60
80
100
120
0
10
20
30
40
50

(b)

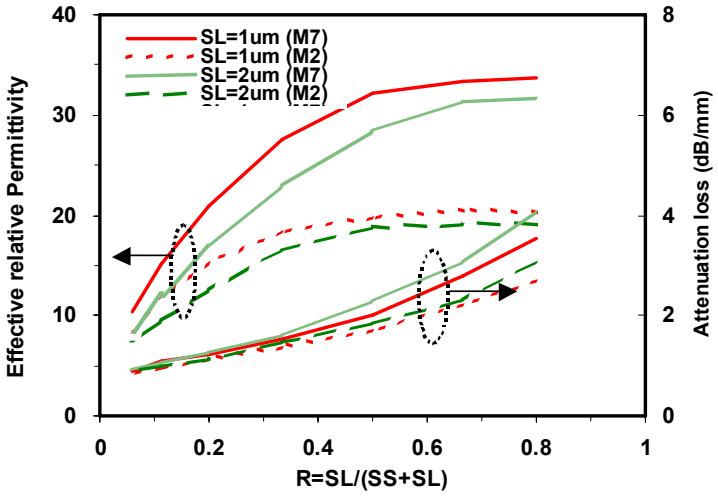

CPW (w/o shields)
FSCPW1 (SL/SS=0.1/0.1, M7)
FSCPW2 (SL/SS=0.1/0.9, M7)
FSCPW3 (SL/SS=0.1/0.1, M2)
Wavelength (mm)
Frequency (GHz)
0
1
2
3
4
0
10
20
30
40
50

(c)

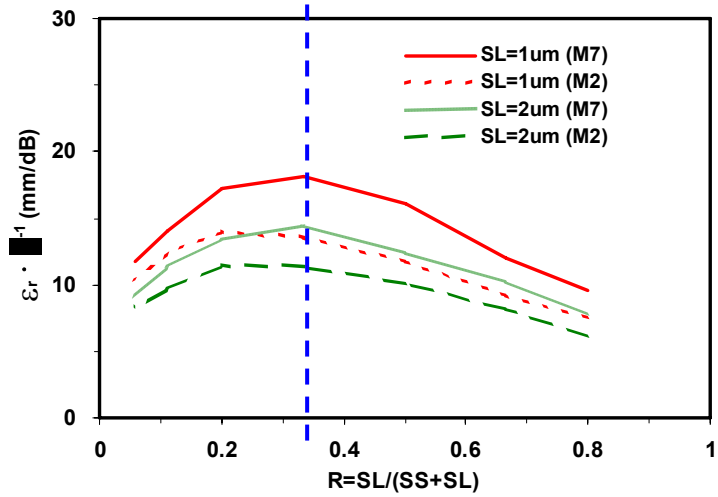


(d)

Fig. 3-18: A comparison of the measured transmission line performances for different floating shields. (a) Attenuation loss versus frequency, (b) Characteristic impedance versus frequency, (c) Wavelength versus frequency, and (d) Quality factor versus frequency.



(a)



(b)

Fig. 3-19: The simulated slow-wave CPW transmission line performance versus parameter R with different SL and metal layer positions at a signal frequency of 50 GHz. (a) Effective relative permittivity and attenuation loss, and (b) Optimization index value of $\varepsilon_r \cdot \alpha^{-1}$.

4 Conclusion and Future work

4.1 Conclusion

High performance slow-wave transmission lines with optimized slot-type floating shields have been analyzed. It has been shown that the wavelength, attenuation loss, and characteristic impedance can be adjusted by the SL, the SS, and the metal layer position of the slot-type floating shields while retaining the same area. A semi-empirical equation that can predict a rough value for the effective relative permittivity has been presented. An optimization index of the floating slow-wave CPW transmission lines has been developed to enable circuit designers to expediently determine the most appropriate slot-type floating shields to meet design specifications. The designers must weigh among SL and SS dimensions, as well as metal layer positions, to design a proper slow-wave CPW with slot-type floating shields with a good quality factor to achieve a functional circuit at the operating frequency. The proposed floating slow-wave CPW transmission line has a higher effective relative permittivity value of up to 51 at 50 GHz, and a better quality factor of 17 at 33 GHz as compared to conventional CPW transmission lines. Moreover, a wavelength as short as 0.85 mm at 50 GHz has been obtained, which results in a saving in silicon area of more than 67%.

Conventional de-embedding methods suffer from an over de-embedding problem to which the proposed method offers a solution. In addition to the

substrate coupling and contact effects provided by existing four-step de-embedding methods, the proposed method also accounts for the discontinuity between the pad and interconnect. Current de-embedding techniques do not de-embed via stack parasitic and the contribution of the proposed method becomes more important as frequency increases. As $[P_{LEFT}]$,$[P_{RIGHT}]$, $[M_{l_1}]$ and $[M_{l_2}]$ can be extracted, more flexible de-embedding dummy structures can be created. Therefore, an additional through structure can be designed to perform via stack de-embedding. The proposed de-embedding method can be extended to other RF devices and this will allow for more accurate RF device characterization. Intrinsic slow-wave CPW transmission line structures are placed on the inter-level metallization layers as they are the most appropriate RF device for cascade-based de-embedding methods involving the via stack de-embedding technique. The proposed floating slow-wave CPW transmission line where periodically slot-type floating shields are located both above and below the CPW structure has a better quality factor of 15 at 50 GHz and a shorter wavelength which results in a reduction of silicon area of more than 66% when compared to that of conventional CPW transmission lines. In short, a significant advantage for future technology scaling and RF circuit designing is made available through the use of more suitable SL and SS dimensions.

4.2 Future Work

Measurement and simulation can be carried out for the frequency up to 110 GHz. The eddy-current loss plays a major role at high frequencies, and it is worth

mentioning that the eddy-current loss in conductors is roughly proportional to the square of the frequency. Therefore, it can be expected that the attenuation loss will increase obviously, better optimization for the slot-type floating shields is needed for the frequencies above 50 GHz.

Further investigations into optimized passive performance and accurate de-embedding techniques are critical to RF circuit design. Transmission lines are important elements in microwave circuit applications as these devices provide the interconnection between active and passive devices in microwave circuits, and are also utilized as impedance matching elements. The CPW structures and MS line structures suffer from incomplete shields, and a significant portion of the electromagnetic field is confined to the dielectric region between the signal and the ground. However, the loss will be induced if the shields are not complete or the shield design is not optimized. The coaxial transmission line includes a signal line and, a top and a bottom slot-type shield surrounding the signal line and therefore. Since the shields are complete, the signal line can be isolated from the external environment and any unwanted crosstalk will be reduced, as shown in Fig. 4-1. Therefore, the coaxial transmission line will show a better dummy metal immunity and a lower attenuation loss compared to incomplete shielded transmission lines. Usually, the inter metal dielectric thickness is constrained by CMOS technologies, and the characteristic impedance range is controlled mainly by the limited height from the signal metal to the shield metal layer. Therefore, coaxial transmission lines with the tunable characteristic impedance and the slow-wave feature are

designed. A strip metal shield creates the slow-wave feature, while an adjustment of the position of the two parallel conductors allows the characteristic impedance range to be tuned. In addition, the formation of the coaxial transmission lines is highly compatible with existing CMOS processes. However, further investigations into optimized coaxial transmission structures with slot-type floating shields and slot-type grounded shields are needed before they can be considered for practical applications. Optimization can be achieved by the strip length, the strip space, and the metal layer position of the top and bottom slot-type shields while retaining the same area. Moreover, more investigations and developments on novel transmission line structures are required to meet the circuit design applications.

The proposed de-embedding technique is developed to overcome the shortcomings of the current lumped-equivalent-circuit-based de-embedding methods. Since the assumption in the additional through structure design limits the applications to all kinds of RF DUT layout style, further investigation on de-embedding techniques is needed to obtain accurate intrinsic device performance for frequencies up to 110 GHz or higher. If the left-side transmission line of length L $[TL_{LEFT}]$, and the right-side transmission line of length L $[TL_{RIGHT}]$, as showin in Fig. 4-2(c), is calculated without any assumption restrictions, it would be helpful to obtain more accurate RF device characterization. The reduction in the parasitic contribution to the surrounding parasitics on intrinsic devices in on-wafer RF DUT structures becomes increasingly important because the intrinsic capacitance, resistance, or inductance may be reduced with the continuous downscaling of the

intrinsic device dimensions. Since the parasitics exist in terms of capacitance, resistance, or inductance, the design of the minimum parasitics for de-embedding dummy structures is necessary in order to improve de-embedding accuracy, and this is the general design guideline for proper dummy structures. After designing the proper dummy structures, small device de-embedding techniques can be further conducted.

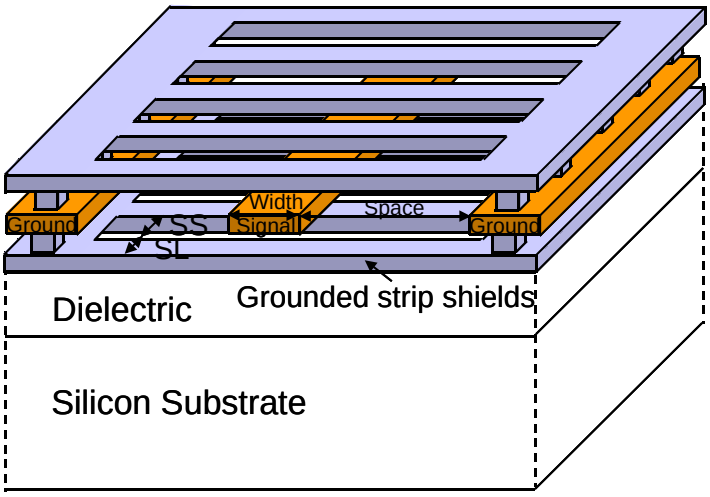


Fig. 4-1: A schematic view of a slow-wave CPW transmission line with slot-type grounded shields.

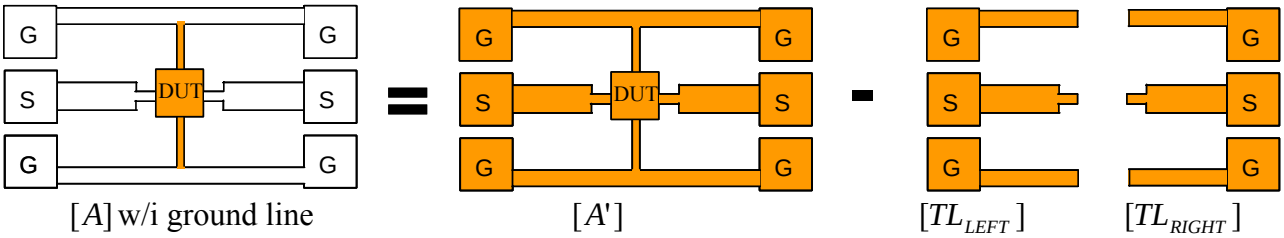


Fig. 4-2. The matrix manipulation for the cascaded-based de-embedding techniques. (a) The intrinsic DUT structure $[A]$ with the ground line parasitic, (b) The RF DUT structure $[A']$, (c) The left-side transmission line of length L $[TL_{LEFT}]$, and the right-side transmission line of length L $[TL_{RIGHT}]$

Figure Captions

Table captions

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Vita

Hsiu-Ying Cho received a M.S. degree in electronic engineering from National Tsing Hua University, Hsinchu, Taiwan. She worked toward the Ph.D. degree in electronics engineering from the National Chiao-Tung University, Hsinchu, Taiwan. from 2001 to 2009. She joined TSMC as an engineer of Process Integration in 1999 and moved onwards to SPICE Modeling Department in 2003. Her current research activity is focused on development of high-frequency device characterization, and device modeling and simulation.

PUBLICATION LIST

(A) JOURNAL PAPERS

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