國立交通大學

電子工程學系　電子研究所

博士論文

具高介電常數閘極絕緣層的低溫多晶矽薄膜電晶體之研究

Investigation on Low-Temperature Polycrystalline-Silicon Thin-Film Transistor with High-κ Gate Dielectric

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摘要

在本論文中，我們詳細地探討高性能之具二氧化鉿（HfO_2）的低溫薄膜電晶體之元件特性。本論文首先特別針二氧化鉿（HfO_2）與多晶矽薄膜之間所產生的介面層（interfacial layer），對於低溫多晶矽薄膜電晶體的特性影響上作了仔細的分析，特別是二氧化鉿的介面層對於 N 型與 P 型通道之低溫薄膜電晶體的影響。此外，為了更進一步研究與加強二氧化鉿之低溫薄膜電晶體的特性，氧氣電漿表面處理也被使用來改善多晶矽通道的表面品質與鈍化缺陷，可增加載子遷移率與降低表面粗糙散射（surface roughness scattering）。另外，氮氣和氨氣電漿表面處理可個別地明顯地增加二氧化鉿之低溫薄膜電晶體的載子遷移率約 74.4 和 108.5 個百分比。而且，氮氣和氨氣電漿表面處理也可降低表面粗糙散射來增加在高的閘極偏壓下之載子遷移率，可個別地提升二氧化鉿之低溫薄膜電晶體的驅動電流約 217 和 219.6 個百分比。

另外，我們也詳細地探討高性能之具二氧化鉿（HfO_2）的低溫薄膜電晶體之可靠度機制。施加多種偏壓與溫度的應力條件以用於釐清陷阱密度能態（trap

density states）的分佈與機制。藉由施予閘極正偏壓應力（PBS）與閘極正偏壓高溫應力（PBTI）在二氧化鉿之低溫薄膜電晶體上，可以觀察到等效介面層之深層陷井能態的產生、多晶矽晶界之淺層陷井能態的產生、以及二氧化鉿之電子捕捉。而閘極負偏壓應力（NBS）與閘極負偏壓高溫應力（NBTI）施予在二氧化鉿之低溫薄膜電晶體可以觀察到等效介面層之深層與淺層陷井能態的產生。

除了電漿表面處理之外，氟與氮離子佈植法配以固態低溫活化法也可達到高性能的二氧化鉿之低溫薄膜電晶體。對於氟離子佈植法而言，二次離子質譜儀的分析展現了與過往研究中不同的氟離子分佈，造成約有百分之 25 的晶界缺陷陷阱被氟離子鈍化且導致漏電電流降低約十倍。另外，熱載子效應對於臨界電壓不穩定度也有了改善。具二氧化鉿之低溫多晶矽薄膜電晶體配以氟離子佈植法可達到低臨界電壓約 1.32 V、優異的次臨界斜率約 0.141 V/decade、和高開關電流比 1.98 x 10^7。然而對於氮離子佈植法而言，二次離子質譜儀的分析展現了氮離子在佈植後的退火過程中，將會聚集在多晶矽通道與絕緣層的介面處，對於 N 型低溫多晶矽薄膜電晶體而言，將會造成百分之 54.9 的驅動電流增加量，然而對於 P 型低溫多晶矽薄膜電晶體而言，將會造成百分之 16.7 的驅動電流增加量。因此，對具二氧化鉿之低溫多晶矽薄膜電晶體配以氮離子佈植法可達到低臨界電壓：N 型約為 1.05 V，P 型約為−0.8 V、優異的次臨界斜率：N 型為 0.213 V/decade，P 型為 0.123 V/decade、以及較高的載子遷移率：N 型為 37.80 cm2/V-s，P 型為 64.14 cm2/V-s。這些具二氧化鉿之低溫多晶矽薄膜電晶體的改善，均歸功於較高的閘極電容密度以及氟與氮離子對於多晶矽薄膜缺陷的鈍化。

最後，此論文也展示了利用金屬側向誘發結晶法配以氮化鉭/二氧化鉿（TaN/HfO_2）結構之 P 型通道低溫薄膜電晶體。低臨界電壓約 0.095 V、優異次臨界斜率約 83 mV/decade、和超高載子遷移率 240 cm^2/V-s 可被實現而不需要任何的缺陷鈍化處理。此明顯的電性改善主要是來自於利用金屬側向誘發結晶法所產生的通道薄膜以及非常高的閘極電容密度。

Investigation on Low-Temperature Polycrystalline-Silicon Thin-Film Transistor with High-κ Gate Dielectric

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Abstract

In this dissertation, the impacts of HfO_2 interfacial layer on n- and p-channel LTPS-TFTs are specified. In order to enhance the characteristics of HfO_2 LTPS-TFT further, oxygen plasma surface treatment is employed to improve the interface quality and passivate the defects of channel grain boundaries, resulting in increasing the carrier mobility and reducing the surface roughness scattering. Moreover, significant field effect mobility μ_{FE} improvement ~ 74.4 % and 108.5 % are observed for LTPS-TFTs with HfO_2 gate dielectric after N_2 and NH_3 plasma surface treatments, respectively. In addition, the N_2 and NH_3 plasma surface treatments can also reduce the surface roughness scattering to enhance the field effect mobility μ_{FE} at high gate bias voltage V_G, resulting in 217.0 % and 219.6 % improvement in driving current, respectively.

In addition, a comprehensive study of the reliability mechanisms of the high performance low-temperature poly-Si thin-film transistor (LTPS-TFT) with HfO_2 gate dielectric is also demonstrated. Various bias and temperature stress conditions, which correspond to positive bias stress (PBS), positive bias temperature instability (PBTI), negative bias stress (NBS), negative bias temperature stability (NBTI), and hot carrier stress, are used to differentiate the distribution and mechanism of trap density states. The generation of deep trap states of the effective interfacial layer, tail trap states of poly-Si grain boundaries, and electrons trapping of the HfO_2 gate dielectric are observed for the PBS and PBTI of the HfO_2 LTPS-TFT. In addition, both the deep and tail trap states of the effective interfacial layer are generated under NBS and NBTI of the HfO_2 LTPS-TFT. Moreover,

In addition to the plasma surface treatment, fluorine and nitrogen ion implantation with low temperature solid-phase crystallized activation scheme is used to obtain a high performance HfO_2 LTPS-TFT. For fluorine ion implantation of LTPS-TFT, the SIMS analysis shows a different fluorine profile compared to that annealed at high temperature. About one order current reduction of I_{min} is achieved due to 25 % grain-boundary traps are passivated by fluorine implantation. In addition, the threshold voltage instability of hot carrier stress is also improved with the introduction of fluorine. The LTPS-TFT with HfO_2 gate dielectric and fluorine pre-implantation can simultaneously achieve low V_{TH} ~ 1.32 V, excellent S.S. ~ 0.141 V/decade, and high I_{on}/I_{min} current ratio ~ 1.98 x 10^7. For nitrogen ion implantation of LTPS-TFT, the SIMS analysis shows the nitrogen atoms would pile up near the surface of poly-Si channel film after SPC process. For n-channel LTPS-TFT, a ~ 54.9 % driving current I_{Dsat} improvement is found. For p-channel LTPS-TFT, a ~ 16.7 % driving current I_{Dsat} improvement is found. Finally, a high performance CMOS

LTPS-TFTs with threshold voltage V_{THn} ~ 1.05 V, V_{THp} ~ –0.8 V, subthreshold swing $S.S._n$ ~ 0.213 V/dec., $S.S._p$ ~ 0.123 V/dec., field effect carrier mobility μ_{nFE} ~ 37.80 cm^2/V-s and μ_{pFE} ~ 64.14 cm^2/V-s are derived. The performance improvements of LTPS-TFTs after NII treatment are due to the defect passivation near the surface channel by nitrogen atoms.

Finally, high-performance low-temperature poly-Si (LTPS) p-channel thin-film transistor (TFT) with metal-induced lateral crystallization (MILC) channel layer and TaN/HfO_2 gate stack is demonstrated. Devices of low threshold voltage V_{TH} ~ 0.095 V, excellent subthreshold swing S.S. ~ 83 mV/dec., and high field effect mobility μ_{FE} ~ 240 cm^2/V-s are achieved without any defect passivation methods. These significant improvements are due to the MILC channel film and the very high gate capacitance density provided by HfO_2 gate dielectric with the effective oxide thickness (EOT) of 5.12 nm.

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Chapter 1

Introduction of Low-Temperature Polycrystalline-Silicon Thin-Film Transistor

1.1 Background of Silicon Channel Thin-Film Transistors

Silicon channel thin-film transistors (TFTs) have been widely investigated for the application of pixel driving device of active matrix liquid crystal display (AMLCD) [1.1]-[1.3]. The liquid crystal of LCD can show different polarization to make the incident white light reveal different colors. In order to control the polarization of liquid crystal, a switch device of liquid crystal is required to make the liquid crystal act as a display monitor. Therefore, the switch devices must be embedded in the glass panel to control the polarization of liquid crystal. The fabrication processes of switch devices are limited by the melting point of glass panel because the fabrication of switch devices is not separating from glass panel. Amorphous-silicon channel TFTs are generally chosen to be the switch device of AMLCD in LCD industry. However, the driving current of amorphous-Si TFT is very low because the amorphous-silicon film is less conductive, which is corresponding to very low field effect carrier mobility μ_{EF} about several cm^2/V-s. With the development of large-size display panel, high driving current of switch device of liquid crystal is urgently needed to drive amount of pixels and enhance the respond time of liquid crystal. Low-temperature polycrystalline-silicon (LTPS) thin-film transistors have been studied instead of amorphous silicon [1.4]-[1.8]. This is because the field effect carrier mobility μ_{EF} in polycrystalline silicon is significantly higher (by one ~ two orders of magnitude) than that in amorphous silicon [1.9], so that the switch devices of liquid crystal with reasonably high drive currents can be achieved in polycrystalline silicon.

In addition to the switch device of liquid crystal pixel, the functional electronic circuits of LCD are wanted to be integrated on the panel, which is named system-on-panel (SOP). Recently, the topic of SOP is attracting much attention to realize [1.6]. In order to achieve high functional integrated circuits, high-performance TFTs with high driving current, low gate leakage current, low threshold voltage V_{TH} and low subthreshold swing S.S. are required urgently for high-speed display driving circuits.

Beside the application of display industry, the device structure of silicon-channel TFT is the same as the silicon-on-insulator (SOI) device of microelectronics. The difference of TFT and SOI device is the crystal phase of silicon channel film that amorphous- and polycrystalline-silicon channel are usually referred to TFT and the single-crystalline silicon channel film is referred to SOI device. SOI device exhibits ultra-high performance characteristics to be applied in very large scale integrated circuits (VLSI) technology. However, the cost of SOI device is very expensive. In recent years, TFTs device have been studied for the application of Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM) in the back-end fabrication process of VLSI technology [1.10][1.11]. The three-dimension integration of integrated circuits technology has been paid much attention to realize because the chip area of integrated circuits can be reduced and the cost of TFT device is much cheaper than single-crystalline MOSFETs and SOI devices. Therefore, the idea of system-on-panel and three-dimension integration would be a novel development of semiconductor industry.

1.2 Electrical Characteristics of Polycrystalline-Silicon

Fig. 1-1 shows the device structure of polycrystalline-silicon thin-film transistors.

The performance of TFT is limited by the electrical characteristics of polycrystalline-silicon channel film. Therefore, the studies of electrical characteristics of polycrystalline-silicon are very important.

1.2.1 Seto's model

John Y. W. Seto proposed a model to describe the electrical properties of polycrystalline silicon thin-film in 1975 [1.12]. Seto's model has some assumptions as shown below:

Assumption:

1. Polycrystalline-silicon is composed of identical crystallites having a grain size of L cm.
2. There is only one type of impurity atom present, the impurity atoms are totally ionized, and uniformly distributed with a concentration of N cm^{-3}.
3. The single-crystalline silicon energy band structure is assumed to be applicable inside the crystallites.
4. The grain boundary is of negligible thickness compared to L and contains Q_t cm^{-2} of traps located at energy E_t with respect to the intrinsic Fermi-level.
5. The traps are assumed to be initially neutral and become charged by trapping a carrier.
6. Abrupt depletion approximation.

I. Potential barrier derivation

As shown in Fig. 1-2 that indicates the grain size L, dopant concentration N, and the depletion width 2(L/2 – h). From Poisson's equation:

$$\frac{d^2V}{dx^2} = \frac{-qN}{\varepsilon}, \quad h < |x| < \frac{1}{2}L \quad (1)$$

$$\rightarrow \quad \frac{dV}{dx} = \frac{-qN}{\varepsilon}x + C_1 \quad (2)$$

and $\left.\frac{dV}{dx}\right|_{x=h} = 0$

$$\rightarrow \quad C_1 = \frac{qNh}{\varepsilon} \quad \rightarrow \quad \frac{dV}{dx} = \frac{qN}{\varepsilon}(h-x)$$

$$\rightarrow \quad V_{(x)} = \frac{qN}{2\varepsilon}(x-h)^2 + V_0, \quad h < |x| < \frac{1}{2}L \quad (3)$$

V_0 is the potential of the conduction band edge at the corner of the crystallite.

E_{Fi} is taken to be at zero energy

a. for $LN < Q_t$ → $h = 0$

$$\rightarrow \quad V_{(x)} = \frac{qN}{2\varepsilon}x^2 + V_0, \quad |x| < \frac{1}{2}L \quad (4)$$

so that the potential barrier $V_B = V_{(L/2)} - V_{(0)} = \frac{qL^2N}{8\varepsilon}$ (5)

We define the average carrier concentration of polycrystalline-silicon thin-film is P_a and the Boltzmann statistics $P_{(x)}$ is valid,

$$P_{(x)} = N_c \exp\{\frac{-[qV_{(x)} - E_F]}{KT}\} \quad (6)$$

$$P_a = \frac{1}{L}\int_{-L/2}^{L/2} P_{(x)}\ dx = \frac{n_i}{Lq}\left(\frac{\pi 2\varepsilon KT}{N}\right)^{1/2} \exp\left(\frac{E_B + E_F}{KT}\right) erf\left[\frac{qL}{2}\left(\frac{N}{2\varepsilon KT}\right)^{1/2}\right] \quad (7)$$

$$E_B = qV_B, \quad n_i = N_c \exp\left(\frac{-E_g}{2KT}\right),$$

According to the number of carriers trapped to the total number of trapping states which are occupied, we can obtain

$$LN = \frac{Q_t}{1 + 2\exp[\frac{E_t - E_F}{KT}]}$$

$$\rightarrow \quad E_F = E_t - KT\ln\left(\frac{\frac{Q_t}{LN} - 1}{2}\right) \quad (8),$$

Therefore, we can derive the P_a if N, L, Q_t and E_t are given.

b. for $LN > Q_t$ → $h > 0$

$$\rightarrow \quad V_B = \frac{qQ_t^{\,2}}{8\varepsilon N} \qquad (9)$$

From the results of equations (5) and (9), we can derive the relation between the potential barrier V_B and the doping concentration N of the polycrystalline-silicon thin-film as shown in Fig. 1-3. When the doping concentration of the polycrystalline-silicon N is less than Q_t/L, the V_B would be higher if the N increased, resulting in the less conductive of polycrystalline-silicon thin-film. When N is higher than Q_t/L, the V_B would be reduced if the N increased, resulting in the more conductive of polycrystalline-silicon thin-film.

In the non-depletion region:

$$P_b = N_c \exp[\frac{-(E_c - E_F)}{KT}]$$

→ The average carrier concentration P_a:

$$P_a = \frac{1}{L}\int_{-L/2}^{L/2} P_{(x)}\ dx = P_b\{(1-\frac{Q_t}{LN}) + \frac{1}{Lq}(\frac{\pi 2\varepsilon KT}{N})^{1/2} erf[\frac{qQ_t}{2}(\frac{1}{2\varepsilon KTN})^{1/2}] \qquad (10)$$

II. Current transport derivation

The resistance of polycrystalline-silicon thin-film can be divided into two parts: grain boundary region and bulk of crystallite, and dominated by the grain boundary region. The current transport mechanisms of polycrystalline-silicon thin-film are thermionic emission and tunneling current. When the carrier energy is higher than the barrier height E_B, thermionic emission dominates. On the contrary hand, tunneling current dominates the conduction current when the carrier energy is higher than the barrier height E_B. In addition, if the barrier height E_B is narrow and high, tunneling current would dominate the conduction current. In polycrystalline-silicon thin-film, the potential is highest when the barrier width is the widest. For highly doped polycrystalline-silicon, potential barrier E_B is very small and the tunneling current can be neglected. From the thermionic emission current density equation J_{th}:

$$J_{th} = qP_a\left(\frac{KT}{2m^*\pi}\right)^{1/2} \exp\left(\frac{-qV_B}{KT}\right)\left[\exp\left(\frac{qV_a}{KT}\right)-1\right] \quad (11)$$

J_{th}: thermionic emission current

V_a: applied voltage

By neglecting collisions within the depletion region and the carrier concentration in the crystallite was assumed to be independent of the current flow, so that it is applicable only if the number of carriers which take part in the current transport is small compared to the total number of carriers in the crystallite. This condition restricts the V_B > KT.

For $qV_a << KT$,

$$J_{th} = q^2 P_a\left(\frac{1}{2m^*\pi KT}\right)^{1/2} \exp\left(\frac{-qV_B}{KT}\right)V_a \quad (12)$$

$$\rightarrow \quad \sigma = Lq^2 P_a\left(\frac{1}{2\pi m^* KT}\right)^{1/2} \exp\left(\frac{-qV_B}{KT}\right)$$

$$\rightarrow \quad \sigma \propto \exp\left[\frac{-1}{KT}\left(\frac{Eg}{2} - E_F\right)\right], \text{ if } LN < Q_t$$

$$\sigma \propto T^{-1/2} \exp\left(\frac{-E_B}{KT}\right), \text{ if } LN > Q_t$$

In addition, $\sigma = qn\mu$

$$\rightarrow \quad \mu_{eff} = Lq\left(\frac{1}{2\pi m^* KT}\right)^{1/2} \exp\left(\frac{-E_B}{KT}\right) \quad (13)$$

When E_B reach maximum, the minimum μ_{eff} is obtained. Therefore, the μ_{eff} is a function of doping concentration.

Summary of Seto's model

Physical parameters of model are grain size L, trap charge density Q_t, and trap energy level E_t.

L: obtained from TEM

Q$_t$: $V_B = \frac{qQ_t^{\ 2}}{8\varepsilon N}$ (14)

$$\mu_{eff} = Lq(\frac{1}{2\pi m^* KT})^{1/2}\exp(\frac{-E_B}{KT})$$

$$\rightarrow \quad \ln\mu_{eff} = \ln(Lq) - \frac{1}{2}\ln(2\pi m^* KT) - \frac{E_B}{KT} \quad (15)$$

From the curve of equation (15), E$_B$ can be extracted by the slope of ln(μ$_{eff}$)–1/KT plot. Finally, Q$_t$ can be derived.

E$_t$: From equations (7) and (8), E$_t$ can be extracted.

1.2.2 Baccarani's model

After John Y. W. Seto proposed a model to describe the electrical properties of polycrystalline silicon thin-film in 1975 [1.13], G. Baccarani modified Seto's model in 1978 to propose a modified grain-boundary trapping model as follows:

Modifying the equation (11) by replacing P$_a$ with N$_a$:

$$J_{th} = q^2 N_a(\frac{1}{2m^*\pi KT})^{1/2}\exp(\frac{-qV_B}{KT})V_a \quad (16)$$

$$N_a = N_c\exp[\frac{-(\frac{E_g}{2} - E_F)}{KT}] = n_0 \quad (17)$$

$$\rightarrow \quad J_{th} = \frac{q^2 N_c v_c}{KT}\exp(\frac{-\frac{E_g}{2} + E_B - E_F}{KT})V_a \quad (18), \quad v_c = (\frac{KT}{2\pi m^*})^{1/2}$$

$$\rightarrow \quad \sigma = \frac{q^2 L N_c v_c}{KT}\exp[\frac{-(\frac{E_g}{2} + E_B - E_F)}{KT}] \quad (19)$$

$$= \frac{q^2 L n_0 v_c}{KT}\exp(\frac{-E_B}{KT})$$

The energy levels are referred to the intrinsic Fermi-level at the neutral region.

G. Baccarani assumed that the grain boundary traps consisted of Q$_t$ acceptor states with energy E$_t$ referred to the intrinsic Fermi-level at the interface.

$$\rightarrow \quad 2N_D(\frac{L}{2}-h)=\frac{Q_t}{1+\frac{1}{2}\exp(\frac{E_t+E_B-E_F}{KT})} \qquad (20)$$

$$E_B=\frac{q^2(\frac{L}{2}-h)^2 N_D}{2\varepsilon} \qquad (21)$$

N_D: doping concentration of polycrystalline-silicon thin-film

N_D^*: charge density trapped by the grain boundaries

A. When $N_D = N_D^*$ → $h=0$

$$\rightarrow \quad 2N_D^*\frac{L}{2}=\frac{N_t}{1+\frac{1}{2}\exp[\frac{1}{KT}(E_t-E_F+\frac{q^2L^2N_D^*}{8\varepsilon})]}$$

$$\rightarrow \quad N_D^*=\frac{8\varepsilon}{q^2L^2}\{E_F-E_t+KT\ln[2(\frac{N_t}{N_D^*L})-1]\} \qquad (22)$$

For small N_t and L → $N_D^* \propto L^{-1}$.

For large N_t and L → $N_D^* \propto L^{-2}$.

B. When $N_D < N_D^*$

$$E_B=\frac{q^2L^2N_D}{8\varepsilon},$$

$$N_DL=\frac{N_t}{1+\frac{1}{2}\exp\frac{(E_t+E_B-E_F)}{KT}} \qquad (23)$$

$$\rightarrow \quad E_F=E_t+E_B-KT\ln[2(\frac{N_t}{LN_D}-1)] \qquad (24)$$

In addition, from equation (19),

$$\begin{aligned}\sigma &= \frac{q^2LN_cv_c}{KT}\exp[\frac{-(\frac{E_g}{2}+E_B-E_F)}{KT}] \qquad (25)\\ &= \frac{q^2LN_cN_Dv_c}{2KT(N_t-LN_D)}\exp(\frac{-E_a}{KT})\end{aligned}$$

$$E_a = \frac{E_g}{2} - E_t \quad (26)$$

C. When $N_D > N_D^*$

$$2N_D(\frac{L}{2} - h) = \frac{N_t}{1 + \frac{1}{2}\exp(\frac{E_t + E_B - E_F}{KT})} \quad (27)$$

and $E_B = \dfrac{q^2(\frac{L}{2} - h)^2 N_D}{2\varepsilon}$

$$\rightarrow \quad h = \frac{L}{2} - \sqrt{\frac{2\varepsilon E_B}{q^2 N_D}} \quad (28)$$

$$\rightarrow \quad 2N_D\sqrt{\frac{2\varepsilon E_B}{q^2 N_D}} = \frac{N_t}{1 + \frac{1}{2}\exp(\frac{E_t + E_B - E_F}{KT})}$$

$$\rightarrow \quad E_B = E_F - E_t + KT\ln\{2[\frac{qN_t}{\sqrt{8\varepsilon N_D E_B}} - 1]\} \quad (29)$$

From equation (29), E_B would linearly increase with N_D as $N_D < N_D^*$. When $N_D > N_D^*$, there are two different situations as follows:

1. when $E_F - E_t - E_B >> KT \quad \rightarrow \quad 2N_D(\frac{L}{2} - h) \cong N_t \quad \rightarrow \quad \sqrt{\frac{8\varepsilon N_D E_B}{q^2}} = N_t$

$$\rightarrow \quad E_B \cong \frac{q^2 N_t^{\ 2}}{8\varepsilon N_D} \propto \frac{1}{N_D} \quad (30)$$

2. when $E_t + E_B - E_B >> KT \quad \rightarrow \quad N_D \approx n_0 = N_c \exp[\frac{-(\frac{E_g}{2} - E_F)}{KT}]$

$$\rightarrow \quad 2N_D(\frac{L}{2} - h) = 2N_c \exp[\frac{-(\frac{E_g}{2} - E_F)}{KT}]\sqrt{\frac{2\varepsilon E_B}{q^2 N_D}} = \frac{2N_t}{\exp(\frac{E_t + E_B - E_F}{KT})}$$

$$\rightarrow E_B = \frac{E_g}{2} - E_t + KT\ln\left[\frac{qN_D{}^{1/2}N_t}{N_c(2\varepsilon E_B)^{1/2}}\right] \quad (31)$$

Finally, a modified grain-boundary trapping model is derived and the relation between E_B and N_D can be plotted in Fig. 1-4.

1.2.3 J. Levinson's current equation of polycrystalline-silicon thin-film transistor

After John Y. W. Seto and G. Baccarani proposed the physics of polycrystalline-silicon in 1975 and 1978, respectively, J. Levinson proposed the basic current equation of polycrystalline-silicon thin-film transistor at small drain bias based on the Seto and Baccarani's model in 1982 [1.14].

According thermionic emission equation:

When $qV_d << KT$, V_d is the voltage drop of a poly-grain

$$J_{th} = q^2 n_0 \left(\frac{v_c}{KT}\right) V_d \exp\left(\frac{-E_B}{KT}\right) \quad (32)$$

$$v_c = \left(\frac{KT}{2\pi m^*}\right)^{1/2}$$

If the number of grain regions is N and the drain voltage is V_D → $V_d = V_D/N$,

For $N_D < N_D{}^*$ as shown in equation (19)

$$\sigma = \frac{q^2 L N_c v_c}{KT}\exp\left[\frac{-\left(\frac{E_g}{2} + E_B - E_F\right)}{KT}\right], \quad E_B = \frac{q^2 L^2 N_D}{8\varepsilon}$$

For $N_D > N_D{}^*$ as shown in equation (19)

$$\sigma = \frac{q^2 L n_0 v_c}{KT}\exp\left(\frac{-E_B}{KT}\right)$$

$$\rightarrow \quad \sigma = q n_0 \mu_0 \exp\left(\frac{-E_B}{KT}\right) \quad (33)$$

$$\mu_0 = \frac{q L v_c}{KT} \quad (34)$$

when $E_F - E_t - E_B >> KT$ → $E_B \cong \frac{q^2 N_t^{\ 2}}{8\varepsilon N_D}$

For the completed description of mobility, the carrier scattering would also occurred at the grain boundaries except the effect of potential barrier. Therefore, the mobility relation should be modified as:

$$\frac{1}{\mu_b} = \frac{1}{\mu_0} + \frac{1}{\mu_s} \qquad (35)$$

μ_0: effect of the potential barrier

μ_s: scattering at grain boundaries

$$\rightarrow \quad \rho = \rho_G + \rho_B = \frac{1}{q\mu_G n_0} + \frac{1}{q\mu_b n_0 \exp(\frac{-E_B}{KT})} \qquad (36)$$

Equation (36) is valid when the mean free path of carrier is less than the grain size.

ρ_G: grain region term

ρ_B: grain boundaries term

$$\rightarrow \quad \frac{1}{\mu} = \frac{1}{\mu_G} + \frac{1}{\mu_b \exp(\frac{-E_B}{KT})} \qquad (37)$$

In general, $\mu_G >> \mu_b$

$$\rightarrow \quad \mu \cong \mu_b \exp(\frac{-E_B}{KT}) \qquad (38)$$

$$\rightarrow \quad I_L = wtqN_D \mu_b (\frac{V_D}{l}) \exp(\frac{-E_B}{KT}) \qquad (39)$$

w: channel width

l: channel length

$n_0 \sim N_D$

t: inversion layer thickness (~ film thickness)

L_c: thickness of the induced channel

$$E_B \cong \frac{q^2 N_t^{\ 2}}{8\varepsilon N_D}$$

N_G: gate induced charge density (cm^{-2})

$$\rightarrow \quad N_{D(V_G)} = N_D + \frac{N_G}{L_c}$$

$$\rightarrow \quad I_D = wq\mu_b (N_D L_c + N_G) \frac{V_D}{l} \exp\{-[\frac{q^2 N_t^{\ 2} L_c}{8\varepsilon KT(N_D L_c + N_G)}]\} \qquad (40)$$

When $V_G = 0V$, equation (40) = equation (39).

If the dopant is not completely ionized, $N_D \rightarrow \eta N_D$. η:effective doping efficiency

When V_D is very small, $\rightarrow \quad qN_G = C_{ox}(V_{GS} - V_T)$

This chapter describes the physical mechanism of polycrystalline-silicon and thin-film transistor. In order to similar to the device physics of single-crystalline metal-oxide-semiconductor field effect transistor (MOSFET), the impacts of defects and grain boundaries on the carrier transport of polycrystalline-silicon are attributed to the mobility parameter which is modified by the potential barrier height and carrier scattering with grain boundaries. Therefore, a lot of carriers are required to lower the potential barrier height to enhance the current transport, resulting in a large operation voltage of polycrystalline-silicon thin-film transistor. Hence, many studies of high performance low-temperature polycrystalline-silicon thin-film transistor focus on the several ways to enhance the driving current of LTPS-TFT. Enlarging grain size to decrease the grain boundaries is a popular way to enhance the performance of LTPS-TFT, like low-temperature solid-phase crystallization (SPC), excimer layer annealing (ELA), metal-induced crystallization (MIC), and metal-induced lateral crystallization (MILC). Another method to improve the characteristics of LTPS-TFT is the passivation of defects in the polycrystalline-silicon thin-film, like H_2, NH_3, CF_4 and O_2 plasma passivation, to inactive the trap states of defects. In addition to these two main methods, the enhancement of gate capacitance density is a novel idea instead of additional fabrication process in recent years due to the development of high-κ gate dielectric. A comprehensive investigation of LTPS-TFT with HfO_2 high-κ gate dielectric is proposed in this dissertation.

1.3 Dissertation Organization

In Chapter 1, an introduction about the background of silicon channel thin-film transistors is described. In addition, the physical model of the polycrystalline-silicon thin-film is also addressed to clarify the impacts of defects and grain boundaries on the electrical characteristics of thin-film transistors. According to the physical model of polycrystalline-silicon, many effective methods which can improve the performance of thin-film transistors are illustrated for the development of thin-film transistors.

In Chapter 2, a detail study about the impacts of the interfacial layer, which is formed natively at the interface of poly-Si and HfO_2 gate dielectric, on the electrical characteristics of HfO_2 LTPS-TFT is performed. Both n-channel and p-channel LTPS-TFT with HfO_2 gate dielectric are fabricated to comprehensively characterize the property of HfO_2/poly-Si interfacial layer. In addition to the characteristics of HfO_2/poly-Si interfacial layer, O_2, N_2 and NH_3 plasma surface treatment are also used to analyze and enhance the performance of both n-channel and p-channel LTPS-TFT with HfO_2 gate dielectric.

In Chapter 3, the effects of the adopting of HfO_2 high-κ gate dielectric on the low-temperature polycrystalline-silicon thin-film transistor are proposed. In addition, a comprehensive study on the reliability mechanisms of HfO_2 LTPS-TFT is also performed by the way of different stress conditions, such as negative-bias stress, negative-bias temperature instability, positive-bias stress, positive-bias temperature instability, hot-carrier stress and high-temperature hot-carrier stress, to distinguish the degradation mechanisms of HfO_2 thin-film transistor.

In Chapter 4, fluorine ion implantation before solid phase crystallization and nitrogen ion implantation after solid phase crystallization of the amorphous-silicon channel film are employed to passivate the defects of channel film. The fluorine ion implantation results in reducing the leakage current and improving the reliability of LTPS-TFT with HfO_2 gate dielectric. Different behavior of fluorine ion implantation from other groups' reports is observed for low temperature solid phase activation of fluorine ion implantation. The nitrogen ion implantation results in the improvements of threshold voltage V_{TH}, subthreshold swing S.S., field effect carrier mobility μ_{FE} and driving current I_{Dsat} of CMOS LTPS-TFTs with HfO_2 gate dielectric.

In Chapter 5, a novel crystallization method: metal-induced lateral crystallization with TaN/HfO_2 gate stack structure is demonstrated for LTPS-TFT. Excellent device performance which can be compared with single-crystalline MOSFET is observed to reveal the possibility of SOP realization.

Finally, conclusions of this dissertation and recommendations for further research are presented in Chapter 6.

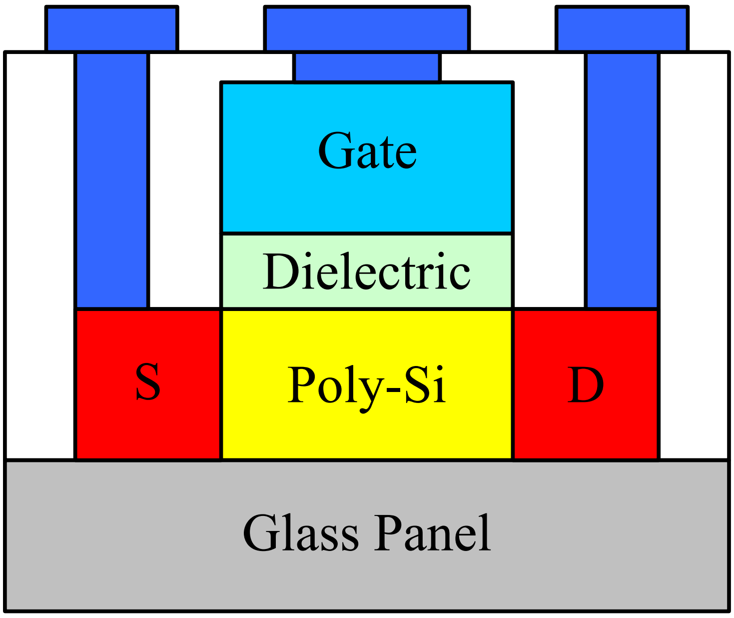


Fig. 1-1. The cross-section view of polycrystalline-silicon thin-film transistor.

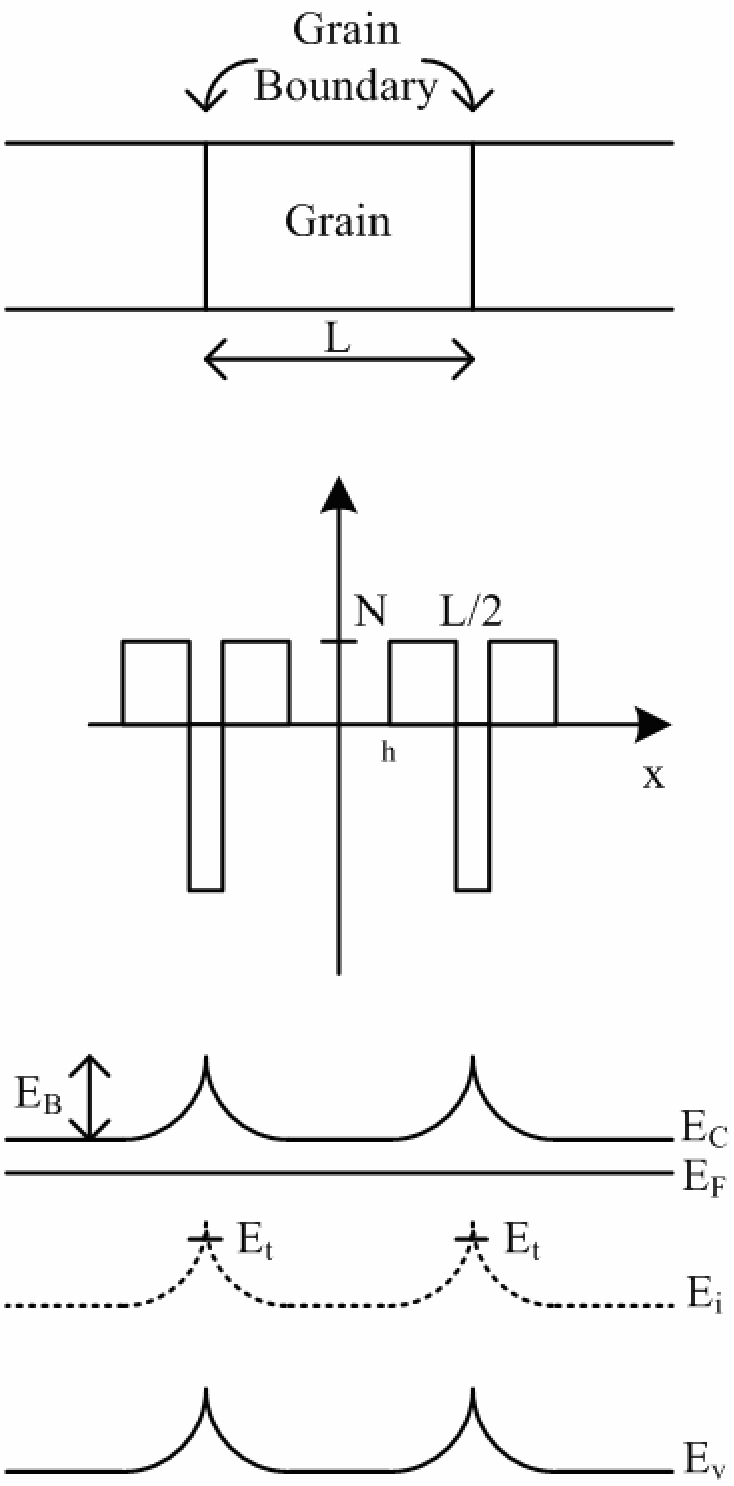


Fig. 1-2. Sketch of the band diagram in polycrystalline-silicon thin-film.

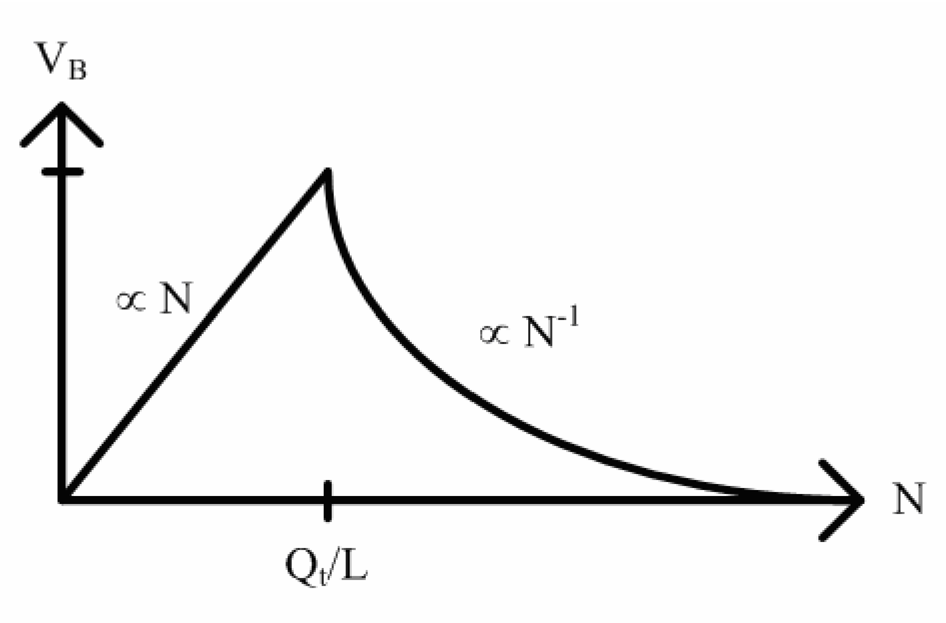


Fig. 1-3. Barrier height versus impurity concentration.

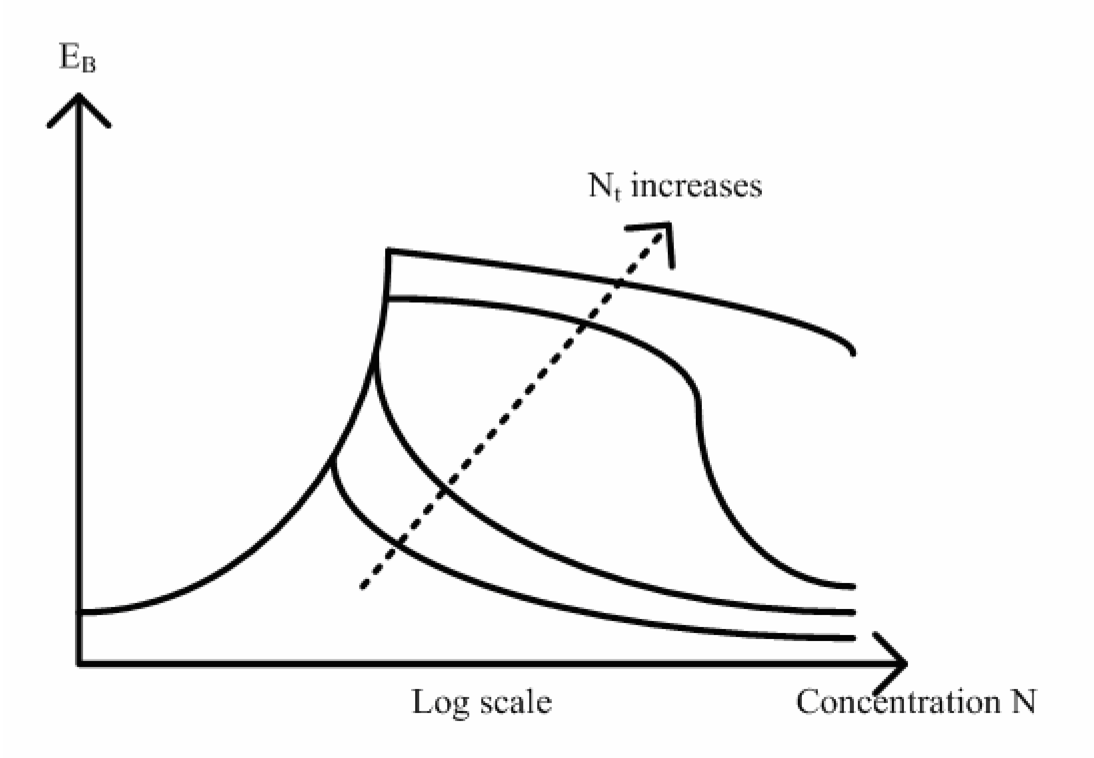


Fig. 1-4. Barrier height versus impurity concentration.

Chapter 2

Investigation of HfO_2/Poly-Si Interfacial Layer on CMOS Low-Temperature Polycrystalline-Silicon Thin-Film Transistor, Including O_2, N_2, NH_3 Plasma Surface Treatment

2.1 Impacts of HfO_2/Poly-Si Interfacial Layer on CMOS Low-Temperature Polycrystalline-Silicon Thin-Film Transistor with HfO_2 Gate Dielectric

2.1.1 Introduction

As mentioned in Chapter 1.1, low-temperature polycrystalline silicon thin-film transistors (LTPS-TFTs) have been used for active-matrix liquid crystal displays (AMLCDs) and system-on-panel (SOP) on glass substrate as pixel switch devices and driving integrated circuits instead of amorphous silicon [2.1]-[2.6] due to that the field effect mobility μ_{EF} in polycrystalline silicon is significantly higher (by two orders of magnitude) than that in amorphous silicon [2.6]. So that complementary metal-oxide-semiconductor (CMOS) devices with reasonably high drive currents can be achieved in polycrystalline silicon. However, the highest temperature of TFTs manufacture process for the application of SOP is limited to the melting point of glass substrate. Consequently, it is difficult to develop high-performance LTPS-TFTs with low threshold voltage V_{TH}, low subthreshold swing S.S. and high driving current I_{Dsat} to drive the liquid crystal of large area panel. Therefore, high-performance TFTs with high driving current I_{Dsat}, low gate leakage current I_G, low threshold voltage V_{TH} and subthreshold swing S.S. are required urgently. In order to enhance the driving current of TFTs and break through this challenge, a thin gate oxide must be used to increase the gate capacitance density. However, a higher gate leakage current would be introduced when the thickness of gate oxide becomes thinner. In addition, low quality deposited low-temperature SiO_2 (like plasma enhanced chemical vapor deposition or PECVD-SiO_2) is generally employed as the gate dielectric of the conventional LTPS-TFT. Comparing with low quality deposited low-temperature SiO_2, low temperature deposited high-κ gate dielectric could have better quality and be more suitable for the replacement of the conventional low temperature SiO_2. Many high-κ dielectrics have been used to reduce gate leakage current and to increase transconductance G_m [2.7]-[2.14]. Among these dielectric materials, HfO_2 is the most promising candidate of future high-κ gate dielectric material due to its high permittivity (~ 25) and thermal stability with poly-Si [2.11]-[2.14]. In this Chapter, a high performance LTPS-TFT with HfO_2 gate dielectric is demonstrated.

For the application of system-on-panel (SOP) and three-dimension circuit integration, complementary metal-oxide-semiconductor (CMOS) LTPS-TFTs should be studied simultaneously. In this Chapter, the CMOS LTPS-TFTs with HfO_2 gate dielectric are demonstrated. In addition, the growth of a SiO_2-like interfacial layer (IL) at high-κ/poly-Si interface is observed while the high-κ materials are deposited on the poly-Si surface [2.8]-[2.12]. In this Chapter, the impacts of the IL on the electrical characteristics of LTPS-TFT are specified and compared with conventional CMOS LTPS-TFTs.

In addition to the employment of HfO_2 gate dielectric, the oxygen plasma treatment has been proposed to improve the electrical characteristics of TFTs [2.15][2.16]. The improvements of TFTs are due to the defects passivation of grain boundaries and good quality of the oxide grown by oxidizing the poly-Si surface by oxygen plasma [2.15][2.16]. In this Chapter, the oxygen plasma is also used to study the impact of IL on CMOS LTPS-TFTs.

2.1.2 Fabrication Process

The fabrication of devices started by depositing a 50-nm undoped amorphous Si (α-Si) layer at 550°C in a low-pressure chemical vapor deposition system on Si wafers capped with a 500-nm thermal oxide layer. Then the 50-nm α-Si layer was recrystallized by solid-phase crystallization process at 600°C for 24-h in a N_2 ambient. Then a 500-nm plasma-enhanced chemical vapor deposition oxide (PECVD-SiO_2) was deposited at 300°C for device isolation. The device active region was formed by patterning and etching the isolation oxide. As shown in Fig. 2-1(a), the source and drain regions (S/D) in the active device region was implanted with phosphorus (15 keV at 5 x 10^{15} cm^{-2}) and boron (10 keV at 5 x 10^{15} cm^{-2}) for N- and P-channel LTPS-TFT, respectively. The S/D was activated at 600°C for 24-h annealing in a N_2 ambient. Then oxygen plasma surface treatment was performed for 0, 5, and 15 min at 300°C with a power density of 1.6-mW/cm^2 in O_2, NH_2 and NH_3 gas as shown in Fig. 2-1(b). The flow-rate was 100-sccm at pressure of 67 Pa. A 50-nm HfO_2 with effective oxide thickness EOT ~ 10.8-nm was deposited by electron-beam evaporation system at room temperature. In addition, a 49.3-nm PECVD-SiO_2 was deposited at 300°C as the gate dielectric of conventional CMOS LTPS-TFTs, which are used to compare with CMOS LTPS-TFTs with HfO_2 gate dielectric. After the patterning of S/D contact holes, aluminum was deposited by thermal evaporation system as the gate electrode and S/D contact pad. Finally, the TFT devices were completed by the contact pad definition as shown in Fig. 2-1(c). Devices with gate length (L) and width (W) of 10 and 100 μm are measured. The threshold voltage $|V_{TH}|$ is defined as the gate voltage at which the drain current reaches 10 nA x W/L and $|V_D|$ = 0.1 V. The field effect mobility μ_{FE} is extracted from the maximum transconductance (G_m).

2.1.3 Discussion of Impacts of Interfacial Layer on LTPS-TFT with HfO_2 Gate Dielectric, Including O_2 Plasma Surface Treatment

Figure 2-2 shows the transfer characteristics (I_D-V_G and field effect mobility μ_{FE}) of CMOS HfO_2 LTPS-TFTs without oxygen plasma surface treatment. Some important parameters of CMOS HfO_2 LTPS-TFTs without oxygen plasma surface treatment and conventional CMOS LTPS-TFTs with SiO_2 gate dielectric are all listed in Table 2-I. The threshold voltage $|V_{TH}|$ and subthreshold swing S.S. are reduced significantly while the SiO_2 gate dielectric is replaced by HfO_2. Larger gate capacitance density, which is achieved by replacing SiO_2 gate dielectric by HfO_2 due to higher relative dielectric constant of HfO_2, can attract more carriers with a smaller gate voltage to turn on the LTPS-TFTs. In addition, CMOS LTPS-TFTs with HfO_2 gate dielectric have higher electron and hole field effect mobility μ_{FE} than CMOS LTPS-TFTs with SiO_2 gate dielectric. It indicates that the native growth of a SiO_2-like IL between the HfO_2 and poly-Si has better interface quality than deposited-SiO_2/poly-Si interface [2.9]-[2.12]. Because the poly-Si channel film has a rough Si surface and lots of dangling bonds and strain bonds in the surface of poly-Si channel film, the native growth SiO_2-like IL of HfO_2 LTPS-TFT can terminate these defects and lead to better performance of LTPS-TFT.

For the characteristics of CMOS LTPS-TFTs with HfO_2 gate dielectric as shown in Table 2-I and Fig. 2-2, the hole field effect mobility μ_{FE} is higher about 130.4 % than electron field effect mobility μ_{FE}, which is different from the conventional CMOS LTPS-TFTs with SiO_2 gate dielectric that the hole field effect mobility μ_{FE} is lower about 24.1 % than electron field effect mobility μ_{FE}. It means that the IL of

HfO_2/IL/poly-Si has different characteristics from deposited-SiO_2/poly-Si. It is well known that the field effect carrier mobility μ_{FE} is dominated by the trap states near band tail region [2.17]. Higher hole field effect mobility μ_{FE} than electron field effect mobility μ_{FE} for HfO_2 LTPS-TFTs indicates that there are less tail trap states near the valence band than tail trap states near conduction band. It implies that the native growth SiO_2-like IL of HfO_2/poly-Si interface can terminate both tail state traps density near conduction band and valence band, and more traps density near valence band are terminated than traps density near conduction band. Figure 2-3 shows the output characteristics (the I_D-V_D curve) of CMOS LTPS-TFTs with HfO_2 gate dielectric. Significant higher driving current of P-channel HfO_2 LTPS-TFT than N-channel HfO_2 LTPS-TFT is obtained, which consists with the behavior of field effect mobility μ_{FE} of HfO_2 LTPS-TFTs. It indicates that P-channel LTPS-TFT is more suitable for the driving device of display pixel than N-channel LTPS-TFT if HfO_2 material is used as the gate dielectric of LTPS-TFT.

In addition to the intrinsic characteristics of LTPS-TFTs with HfO_2 gate dielectric, oxygen plasma surface treatment is employed to study the impacts of growth-SiO_2 by oxygen plasma on the CMOS LTPS-TFT with HfO_2 gate dielectric. Figures 2-4 and 2-5 show the transfer characteristics (I_D-V_G and field effect mobility μ_{FE}) of N-channel and P-channel HfO_2 LTPS-TFTs, respectively, with and without oxygen plasma surface treatment. Some important parameters of CMOS HfO_2 LTPS-TFTs with and without oxygen plasma surface treatment are also listed in Table 2-II. The electron field effect mobility μ_{FE} is enhanced with the increase of oxygen plasma time, which indicates the tail trap states near conduction band of HfO_2/poly-Si interface are passivated to enhance the electron field effect mobility μ_{FE} about 46.0 % and 92.4 % for 5-min and 15-min oxygen plasma time, respectively. However, the hole field effect mobility μ_{FE} is reduced while the oxygen plasma is performed for 5 min, which indicates the tail trap states near valence band of HfO_2/poly-Si interface are generated after oxygen plasma surface treatment. When the oxygen plasma is performed for 15-min, the hole field effect mobility μ_{FE} is higher than the hole field effect mobility μ_{FE} of 5-min oxygen plasma treatment. It indicates different effects of oxygen plasma surface treatment. While the oxygen plasma surface treatment is initially performed for a short time, the oxygen diffused slowly and reacted with poly-Si to form a Si-O rich interfacial layer of HfO_2/SiO_2/poly-Si [2.16][2.18][2.19]. While the oxygen plasma treatment is performed for a long time, the oxygen atom can diffuse into the poly-Si channel to passivate the defects of grain boundaries [2.15][2.16]. Therefore, the impact of oxygen plasma surface treatment could be deduced that the effect of interfacial layer growth is dominant for the first 5-min oxygen plasma step. It results in the elimination of tail trap states of HfO_2/poly-Si interface near the conduction band and the generation of tail trap states of HfO_2/poly-Si interface near the valence band to enhance the electron field effect mobility μ_{FE} and reduce the hole field effect mobility μ_{FE}. After a long time of oxygen plasma treatment, the defects passivation of poly-Si channel is dominant, resulting in both electron and hole field effect mobility μ_{FE} are enhanced simultaneously.

Figures 2-6 and 2-7 show the I_D-V_D curve of N-channel and P-channel HfO_2 LTPS-TFTs with and without oxygen plasma surface treatment. From Fig. 2-7, the drain current at $|V_D| = 4V$ of P-channel HfO_2 LTPS-TFT with 5-min oxygen plasma surface treatment is lower than the HfO_2 LTPS-TFT without oxygen plasma surface treatment at $|V_G - V_{TH}| \le 3V$. However, the drain current at $|V_D| = 4V$ of P-channel HfO_2 LTPS-TFT with 5-min oxygen plasma surface treatment is higher than the HfO_2 LTPS-TFT without oxygen plasma surface treatment at $|V_G - V_{TH}| \ge 4V$ even the hole field effect mobility μ_{EF} of P-channel HfO_2 LTPS-TFT with 5-min oxygen plasma surface treatment is lower than HfO_2 LTPS-TFT without oxygen plasma surface treatment. The same trend could be observed for P-channel HfO_2 LTPS-TFT with 15-min oxygen plasma surface treatment that the drain current at $|V_D| = 4V$ of P-channel HfO_2 LTPS-TFT with 15-min oxygen plasma surface treatment is lower than HfO_2 LTPS-TFT without oxygen plasma surface treatment at $|V_G - V_{TH}| \leq 2V$ and higher at $|V_G - V_{TH}| \geq 3V$. We define the saturation current $I_{D(sat)}$ as the drain current at $|V_G - V_{TH}| = |V_D| = 4V$ as shown in Table 2-II. The P-channel LTPS-TFT with oxygen plasma treatment shows a lower drain current at small $|V_G|$ and a higher drain current at large $|V_G|$ as shown in Fig. 2-7. Figures 2-8 and 2-9 show the normalized field effect mobility μ_{EF} of N-channel and P-channel HfO_2 LTPS-TFTs, respectively. It is noted that the field effect mobility μ_{EF} reduction is improved after the oxygen plasma treatment at high $|V_G|$. As described above, the oxygen plasma can passivate the defect trap states of poly-Si channel film and improve the interface quality of HfO_2/poly-Si interface, resulting in the reduction of phonon scattering. Therefore, the drain current of P-channel LTPS-TFT with oxygen plasma treatment is lower at small $|V_G|$ due to lower μ_{EF} and higher at large $|V_G|$ due to the improvement of phonon scattering.

2.1.4 Summary

CMOS LTPS-TFTs with HfO_2 gate dielectric are demonstrated in this Chapter. The effects of HfO_2/poly-Si interfacial layer on the electrical characteristics of CMOS LTPS-TFTs are also specified. In addition, the impacts of oxygen plasma surface treatment on CMOS LTPS-TFTs with HfO_2 gate dielectric are investigated. Not only the change of interfacial layer characteristics, but also the defects passivation of poly-Si channel film is observed. In conclusion, oxygen plasma surface treatment can improve the driving current of CMOS LTPS-TFTs with HfO_2 gate dielectric due to the passivation of interface trap states and grain boundaries of poly-Si channel film. The combination of HfO_2 gate dielectric and oxygen plasma surface treatment would be very suitable for the application of three-dimension circuit integration and SOP.

2.2 Characteristics of HfO_2/Poly-Si Interfacial Layer with N_2 and NH_3 Plasma Surface Treatment on Low-Temperature Polycrystalline-Silicon Thin-Film Transistor with HfO_2 Gate Dielectric

2.2.1 Introduction

After the discussion of Chapter 2.1, characteristics of the native-growth HfO_2/poly-Si interfacial layer of HfO_2 LTPS-TFT have been studied comprehensively. However, the trap states still exist among the polycrystalline-silicon in spite of the employment of high-κ gate dielectrics without any defects passivation methods. The NH_3 plasma post-treatment is the most general method to passivate the trap states of the polycrystalline-silicon channel film for conventional TFTs [2.20][2.21]. Hence, the impacts of NH_3 plasma treatment on LTPS-TFT with high-κ gate dielectric would be worth to study. In order to distinguish the passivation effects of hydrogen H and nitrogen N, N_2 plasma surface treatment would also be done to compare with NH_3 plasma surface treatment. In this Chapter the HfO_2 gate dielectric LTPS-TFT with N_2 and NH_3 surface plasma treatment is demonstrated.

2.2.2 Discussion of Impacts of N_2 and NH_3 Plasma Surface Treatment on Low-Temperature Polycrystalline-Silicon Thin-Film Transistor with HfO_2 Gate Dielectric

The device fabrication process with N_2 and NH_3 plasma surface treatment has described in section 2.1.2. Figures 2-10 and 2-11 show the transfer characteristics (I_D-V_G and transconductance G_m) of LTPS-TFT with HfO_2 gate dielectric after N_2 and NH_3 plasma surface treatment for 5-min and 15-min, respectively. The important device parameters of LTPS-TFTs are listed in the Table 2-III. The subthreshold swing S.S. of device shows an improvement of 8.6 % and 9.6 % with N_2 plasma surface treatment for 5-min and 15-min, respectively. Moreover, field effect mobility μ_{FE} of device also show an increase of 36.1 % and 74.4 % with N_2 plasma surface treatment for 5-min and 15-min, respectively. It is known that subthreshold swing S.S. and field effect mobility μ_{FE} are related to the dangling-bond deep trap states and the strain-bond tail trap states of the polycrystalline-silicon channel [2.17], respectively. The significant increase on field effect mobility μ_{FE} indicates that nitrogen has better passivation effect on strain-bond tail trap states than on dangling-bond deep trap states. On the other hand, devices show 9.1 % and 21.2 % subthreshold swing S.S. improvement with NH_3 plasma surface treatment for 5-min and 15-min, respectively. In addition, 5-min and 15-min NH_3 plasma surface treatment show 50.0 % and 108.5 % field effect mobility μ_{FE} improvement, respectively. It is found that the improvement of subthreshold swing S.S. is on the same level by either 5-min N_2 or NH_3 plasma treatment. This implies hydrogen from NH_3 has no significant contribution to the improvement of subthreshold swing S.S. for such a short 5-min. On the contrary, devices with a longer 15-min NH_3 plasma exhibit more subthreshold swing S.S. improvement, indicating that more passivation effect on the dangling-bond deep trap states due to the contribution of hydrogen. Devices with either 15-min N_2 or

NH_3 plasma show significant field effect mobility μ_{FE} improvement, indicating good passivation on strain-bond tail states can be achieved by both plasma treatments. Figures 2-12 and 2-13 show the output characteristics (I_D-V_D) of LTPS-TFT with HfO_2 gate dielectrics after N_2 and NH_3 plasma surface treatment for 5-min and 15-min, respectively. For 5-min, N_2 plasma and NH_3 plasma show 165.0 % and 91.3 % driving saturation current I_{D_sat} enhancement at $V_G - V_{TH} = 4V$ and $V_D = 5V$ as shown in Table 2-III and Fig. 2-12. The 5-min N_2 plasma surface treatment shows a smaller field effect mobility μ_{FE} improvement and higher I_{D_sat} enhancement than 5-min NH_3 plasma surface treatment.

Figures 2-14 and 2-15 show the normalized μ_{EF} of HfO_2 LTPS-TFTs with N_2 and NH_3 plasma surface treatment. It is noted that the μ_{EF} reduction rate after the peak is improved using surface plasma treatment at high V_G. This improvement is due to the reduced surface roughness scattering [2.22]. N_2 plasma surface treatment has more improvement on surface roughness scattering than NH_3 plasma, resulting in a higher driving saturation current I_{D_sat} for 5-min. The surface roughness scattering are improved further, leading to 217.0 % and 219.6 % improvement in driving saturation current for 15-min N_2 and NH_3 plasma surface treatment, respectively.

High performance LTPS-TFT with low threshold voltage V_{TH} ~ 0.45 V, excellent subthreshold swing S.S. ~ 0.179 V/decade and high field effect mobility μ_{FE} ~ 51.25 $cm^2/V\text{-}s$ is obtained by using HfO_2 gate dielectric and 15-min N_2 plasma surface treatment. In addition, high performance LTPS-TFT with low threshold voltage V_{TH} ~ 0.33 V, excellent subthreshold swing S.S. ~ 0.156 V/decade and high field effect mobility μ_{FE} ~ 61.25 $cm^2/V\text{-}s$ is also obtained by using HfO_2 gate dielectric and 15-min NH_3 plasma surface treatment.

2.2.3 Summary

In this Chapter, high performance LTPS-TFT with HfO_2 gate dielectric has been fabricated. In order to enhance the performance of LTPS with high-κ gate dielectric, two kinds of plasma, N_2 and NH_3, are employed. Subthreshold swing S.S., field effect mobility μ_{FE} and driving saturation current are all significantly improved after N_2 and NH_3 plasma surface treatment.

Table 2-I. Important parameters of CMOS HfO_2 LTPS-TFTs without oxygen plasma surface treatment and conventional CMOS LTPS-TFTs with SiO_2 gate dielectric.

Type	**Gate Oxide**	**V_{TH} (V)**	**S.S. (V/dec.)**	**G_m (μS)**	**EOT (nm)**	**μ_{FE} (cm^2/V-s)**	**$I_{D(sat)}$ (mA)**
N-channel	**SiO_2**	**6.8**	**1.41**	**1.08**	**49.3**	**15.43**	**0.024**
	HfO_2	**0.34**	**0.198**	**9.2**	**10.8**	**28.75**	**0.226**
P-channel	**SiO_2**	**-13.3**	**1.60**	**0.82**	**49.3**	**11.71**	**0.014**
	HfO_2	**-1.22**	**0.144**	**21.2**	**10.8**	**66.25**	**0.718**

Table 2-II. Important parameters of CMOS HfO_2 LTPS-TFTs with and without oxygen plasma surface treatment.

Type	**Gate Oxide**	**Treatment**	**V_{TH} (V)**	**S.S. (V/dec.)**	**G_m (μS)**	**EOT (nm)**	**μ_{FE} (cm^2/V-s)**	**$I_{D(sat)}$ (mA)**
N-channel	**HfO_2**	**Control**	**0.34**	**0.198**	**9.2**	**10.8**	**28.75**	**0.226**
		O_2 5min	**0.62**	**0.225**	**12.8**	**11.3**	**41.97**	**0.453**
		O_2 15min	**0.52**	**0.202**	**15.1**	**12.6**	**55.31**	**0.689**
P-channel	**HfO_2**	**Control**	**-1.22**	**0.144**	**21.2**	**10.8**	**66.25**	**0.718**
		O_2 5min	**-1.8**	**0.165**	**18**	**11.3**	**59.02**	**0.727**
		O_2 15min	**-1.72**	**0.178**	**17.7**	**12.6**	**64.84**	**0.854**

Table 2-III. Important device parameters of LTPS-TFT with HfO_2 gate dielectric after N_2 and NH_3 plasma surface treatment for 5-min and 15-min, respectively.

HfO_2-TFT	**V_{TH} (V)**	**S.S. (V/dec.)**	**G_m (μS)**	**μ_{FE} (cm^2/V-s)**	**I_{D_sat} (mA)**
Control	**0.33**	**0.198**	**9.4**	**29.38**	**0.311**
N_2 5min	**0.5**	**0.181**	**12.8**	**40.00**	**0.824**
NH_3 5min	**0.28**	**0.180**	**14.1**	**44.06**	**0.595**
N_2 15min	**0.45**	**0.179**	**16.4**	**51.25**	**0.986**
NH_3 15min	**0.33**	**0.156**	**19.6**	**61.25**	**0.994**

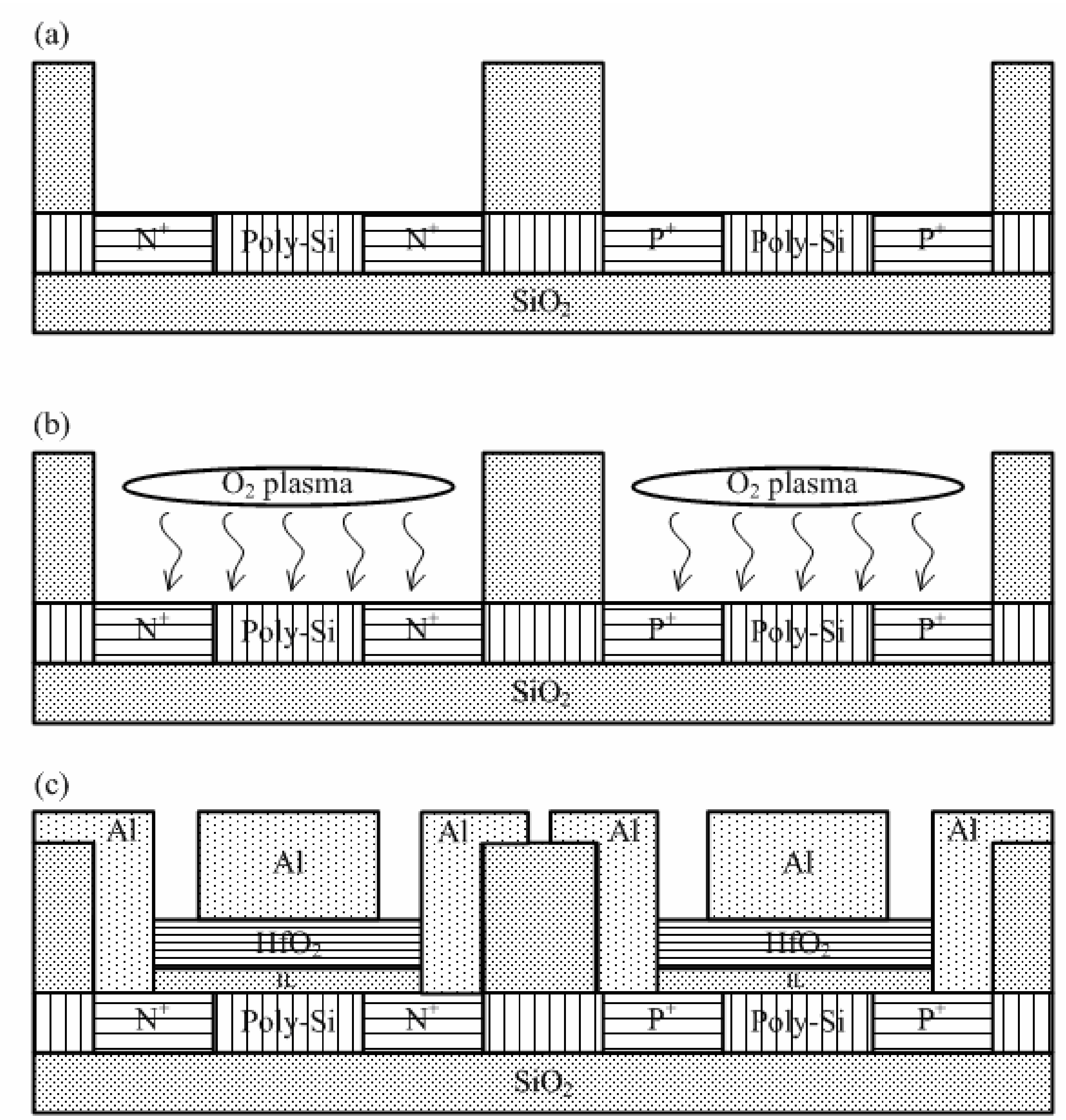


Fig. 2-1. The cross-sectional view of CMOS LTPS-TFTs with HfO_2 gate dielectric and oxygen plasma surface treatment.

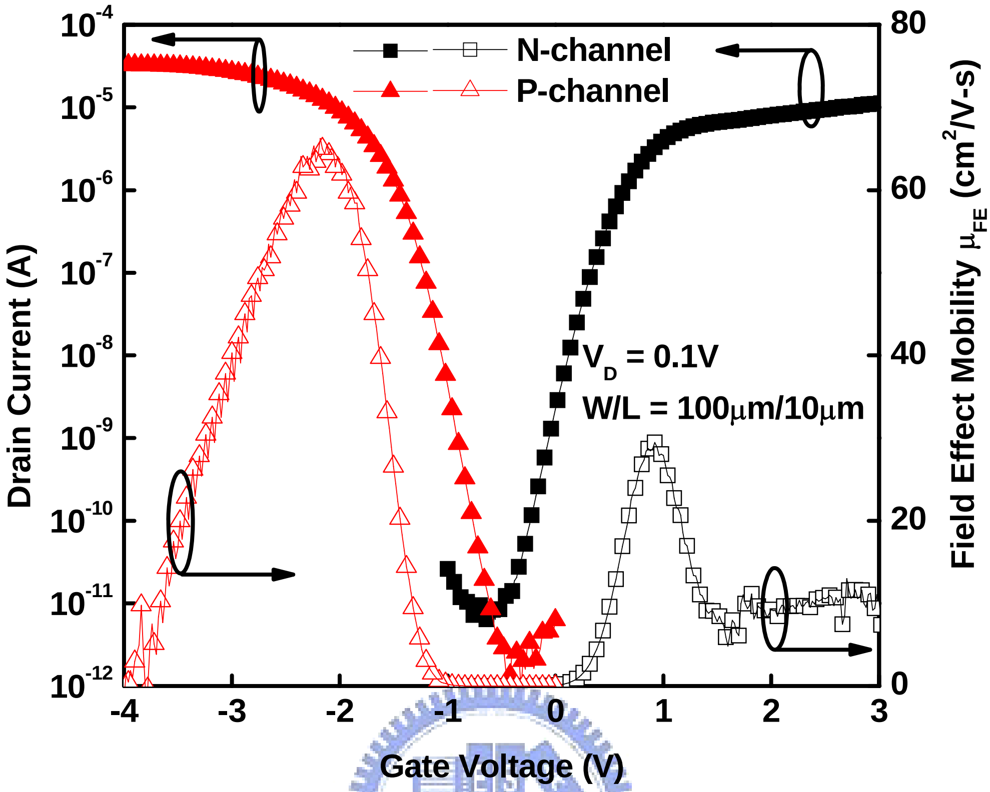


Fig. 2-2. The transfer characteristics (I_D-V_G and field effect mobility μ_{FE}) of CMOS HfO_2 LTPS-TFTs without oxygen plasma surface treatment.

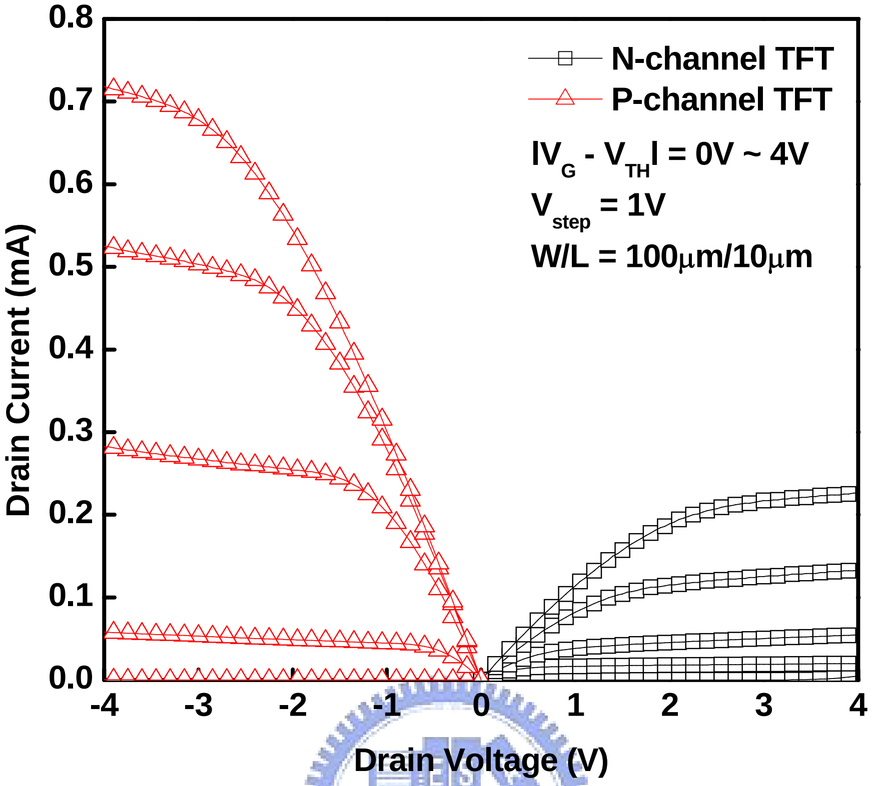


Fig. 2-3. The output characteristics (the I_D-V_D curve) of CMOS LTPS-TFTs with HfO_2 gate dielectric.

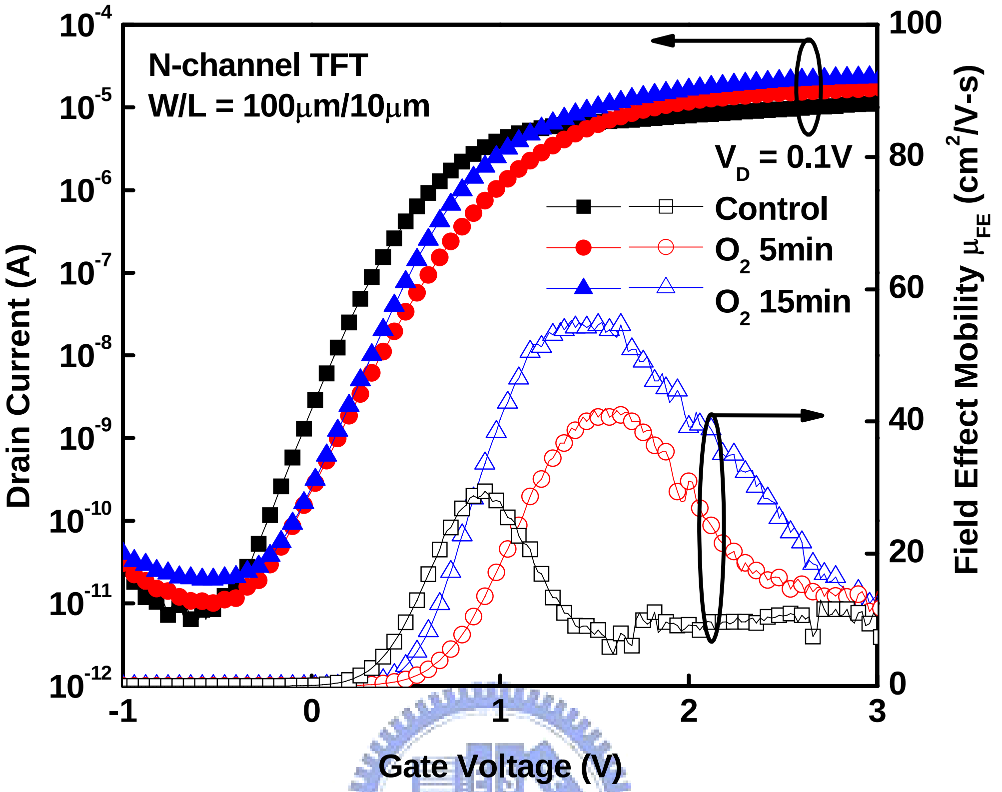


Fig. 2-4. The transfer characteristics (I_D-V_G and field effect mobility μ_{FE}) of N-channel with and without oxygen plasma surface treatment.

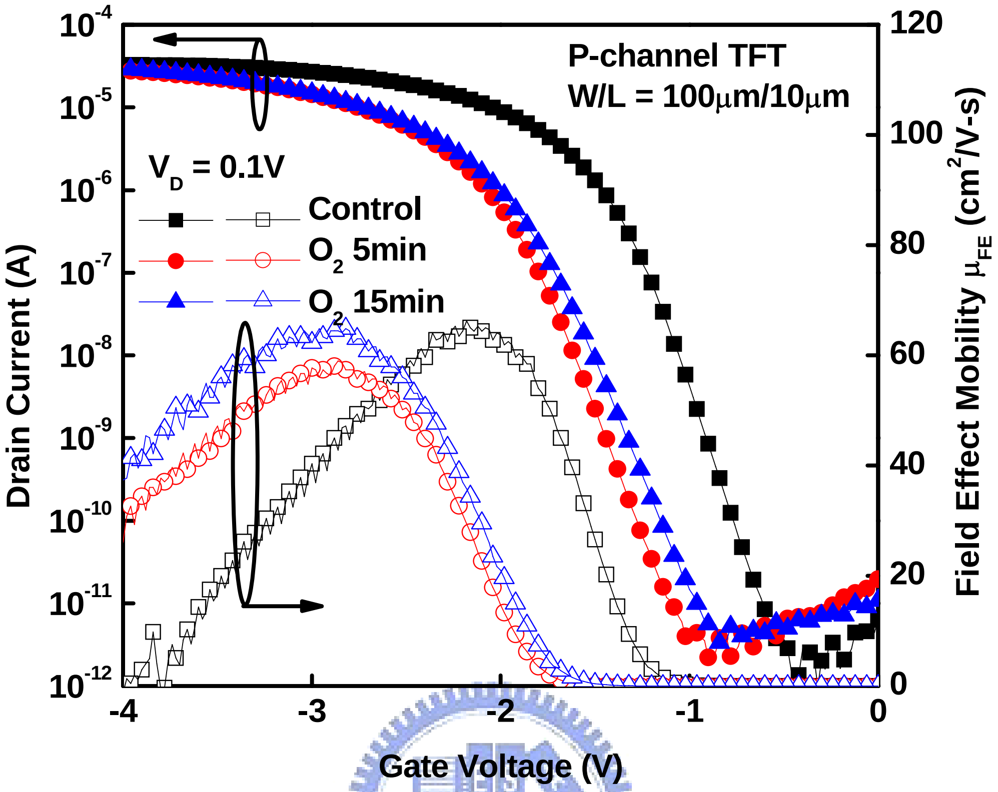


Fig. 2-5. The transfer characteristics (I_D-V_G and field effect mobility μ_{FE}) of P-channel with and without oxygen plasma surface treatment.

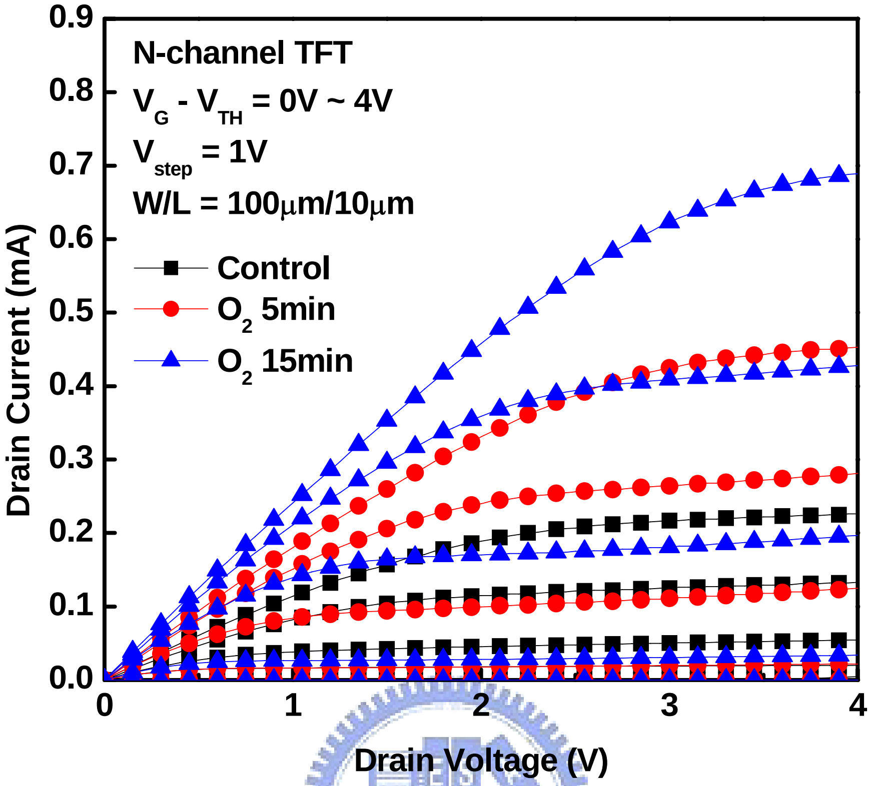


Fig. 2-6. The I_D-V_D curve of N-channel HfO_2 LTPS-TFTs with and without oxygen plasma surface treatment.

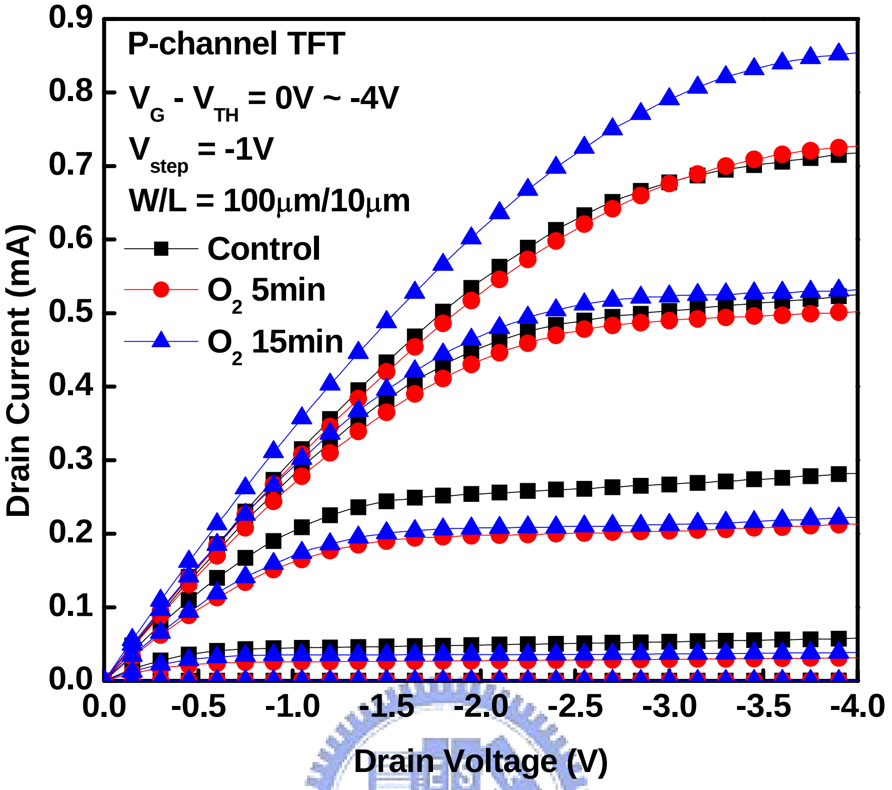


Fig. 2-7. The I_D-V_D curve of P-channel HfO_2 LTPS-TFTs with and without oxygen plasma surface treatment.

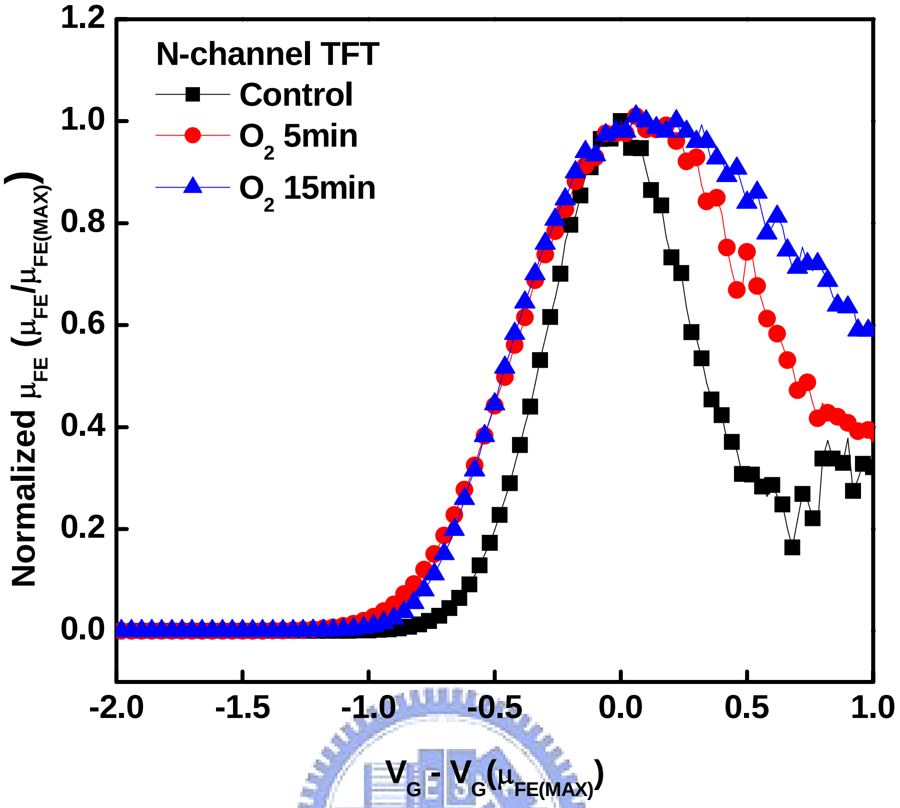


Fig. 2-8. The normalized field effect mobility μ_{EF} of N-channel HfO_2 LTPS-TFTs.

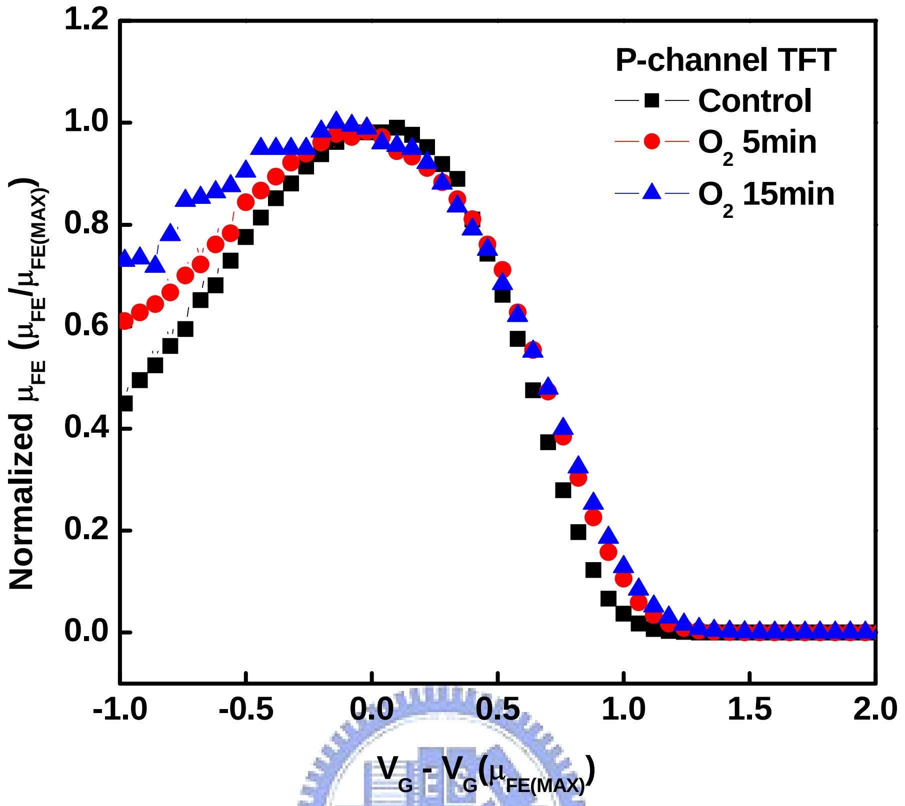


Fig. 2-9. The normalized field effect mobility μ_{EF} of P-channel HfO_2 LTPS-TFTs.

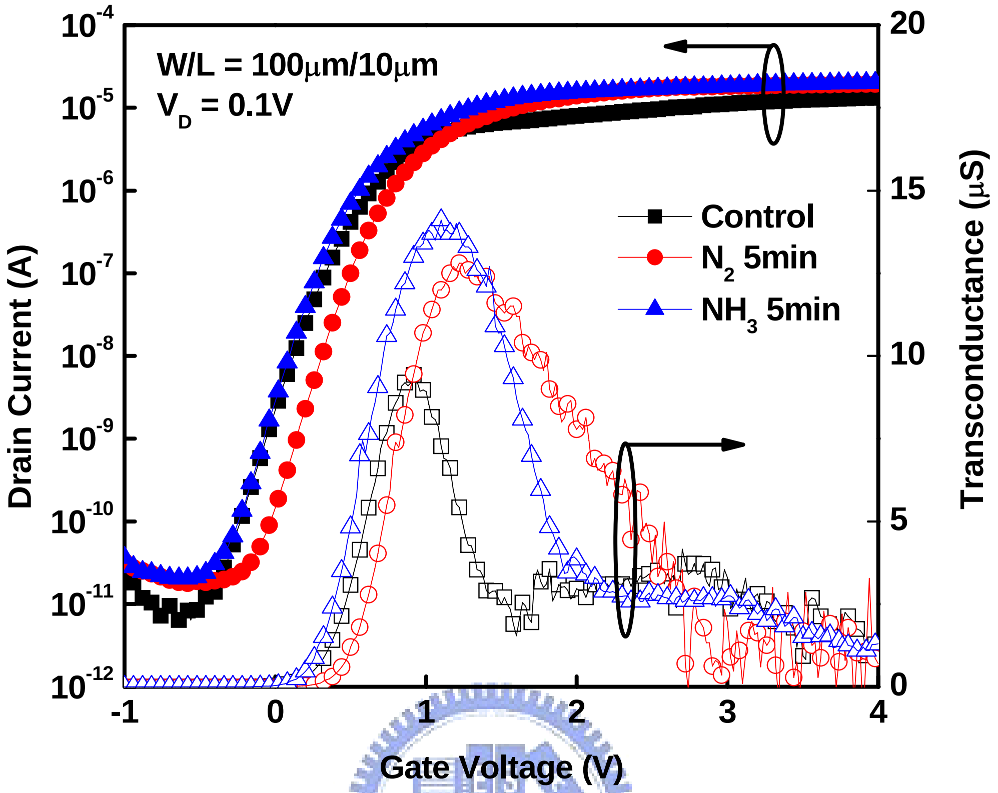


Fig. 2-10. The transfer characteristics (I_D-V_G and transconductance G_m) of LTPS-TFT with HfO_2 gate dielectric after N_2 and NH_3 plasma surface treatment for 5-min.

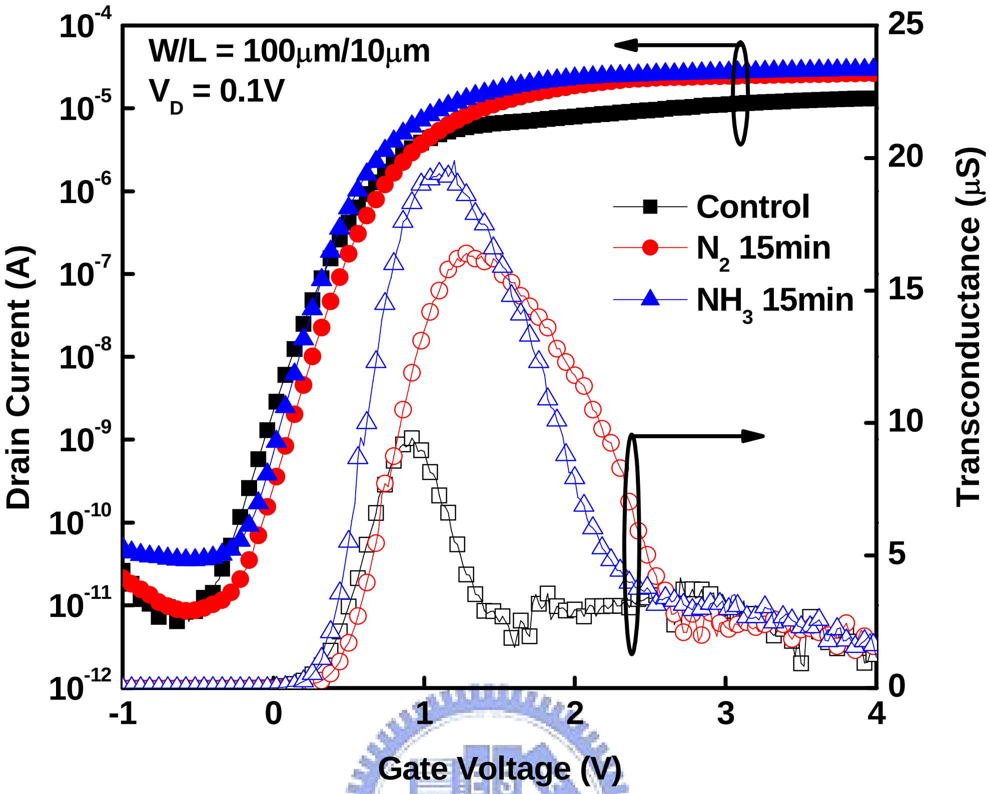


Fig. 2-11. The transfer characteristics (I_D-V_G and transconductance G_m) of LTPS-TFT with HfO_2 gate dielectric after N_2 and NH_3 plasma surface treatment for 15-min.

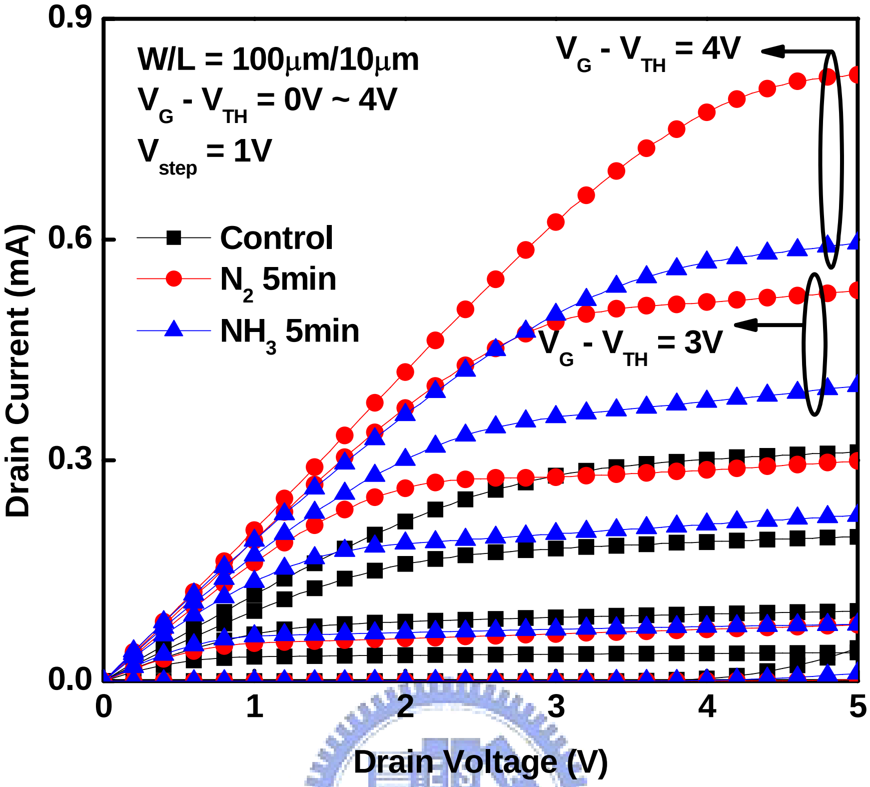


Fig. 2-12. The output characteristics (I_D-V_D) curve of LTPS-TFT with HfO_2 gate dielectric after N_2 and NH_3 plasma surface treatment for 5-min.

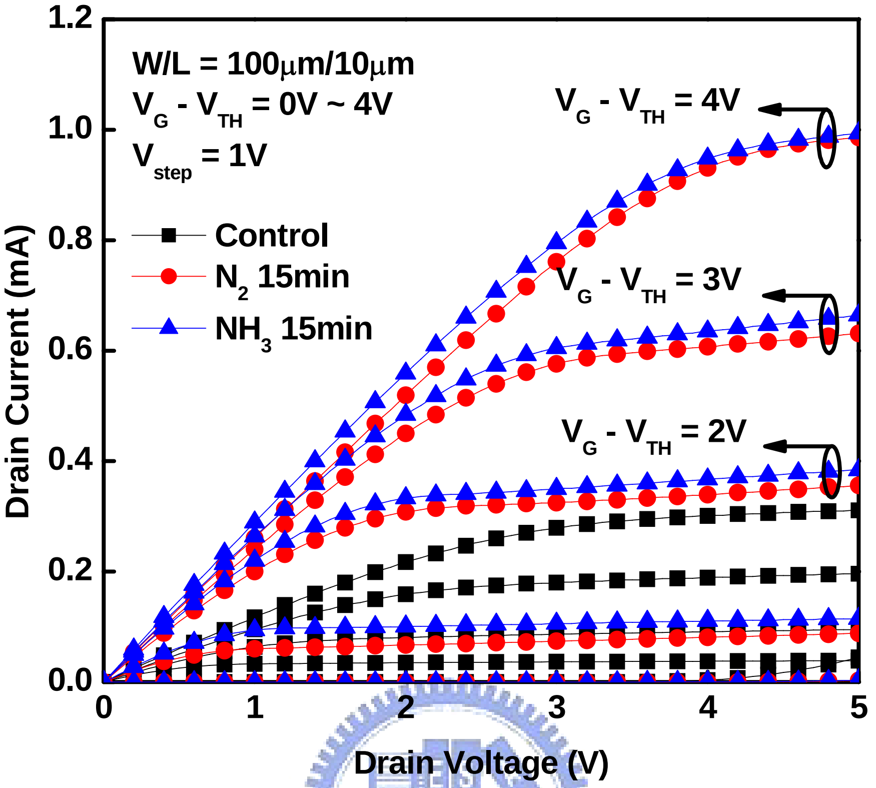


Fig. 2-13. The output characteristics (I_D-V_D) curve of LTPS-TFT with HfO_2 gate dielectric after N_2 and NH_3 plasma surface treatment for 15-min.

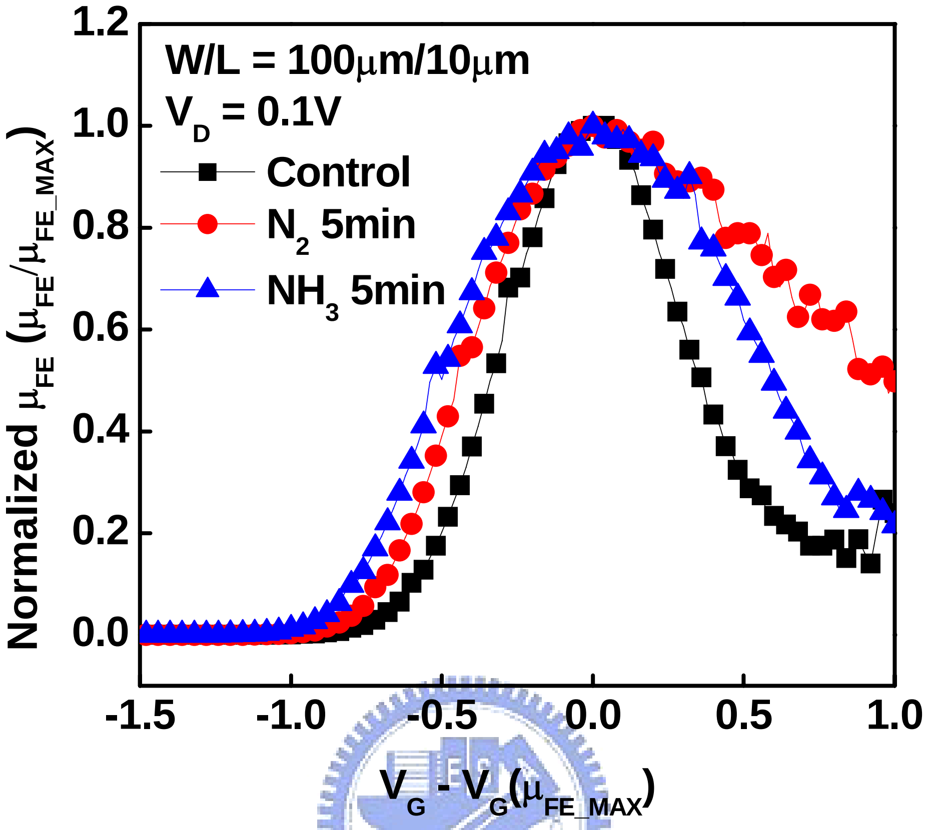


Fig. 2-14. The normalized field effect mobility μ_{EF} of LTPS-TFT with HfO_2 gate dielectric after N_2 and NH_3 plasma surface treatment for 5-min.

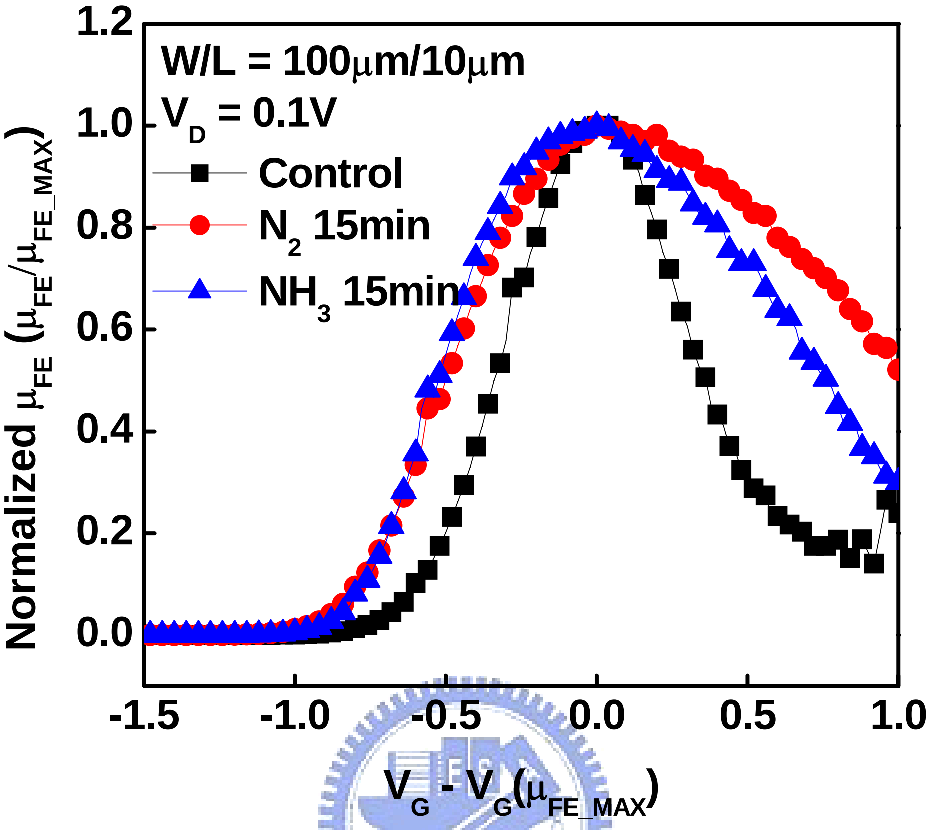


Fig. 2-15. The normalized field effect mobility μ_{EF} of LTPS-TFT with HfO_2 gate dielectric after N_2 and NH_3 plasma surface treatment for 15-min.

Chapter 3

The Adoption of HfO_2 Gate Dielectric for the Low-Temperature Polycrystalline-Silicon Thin-Film Transistor: Performance and Reliability Mechanism

3.1 Introduction of the Reliability of Low-Temperature Polycrystalline-Silicon Thin-Film Transistor with HfO_2 Gate Dielectric

As described in the previous Chapter, high performance low-temperature polycrystalline-silicon thin-film transistors (LTPS-TFTs) are required urgently for the application of three-dimension devices integration and the driving integrated circuits on glass panel [3.1]-[3.3]. In order to achieve high performance characteristics of LTPS-TFTs with low threshold voltage $\left|V_{TH}\right|$, high field effect mobility μ_{FE}, and low subthreshold swing S.S., hydrogen-related plasma treatment is usually used to passivate the defects of poly-Si channel film and SiO_2/poly-Si interface [3.4]-[3.6]. Unfortunately, the introduction of hydrogen would result in the reliability issue of LTPS-TFTs [3.6][3.7]. The employment of high-κ materials as the gate dielectric of LTPS-TFTs would be an effective way to improve the electrical characteristics of LTPS-TFTs without any defect passivation methods as demonstrated in Chapter 2.

In addition, the main limitation of LTPS-TFTs for the application of SOP is their reliability issue which is associated with the trap states in the grain boundaries of poly-Si channel film, interface of gate-oxide/poly-Si channel film, and gate oxide film. Numerous degradation analyses, such as the carrier injection into the gate oxide, degradation of the channel interface, and the increase of trap states in the grain boundaries of the poly-Si channel film, have been proposed to explain the observed device degradation behavior [3.8]-[3.15]. However, a comprehensive investigation of the reliability mechanism for LTPS-TFTs with HfO_2 gate dielectric has not been studied yet.

In this Chapter, various gate and drain bias stress conditions are applied to study the instability of LTPS-TFTs with HfO_2 gate dielectric. In addition, two measurements and bias stress temperatures of 25°C and 125°C are also employed to distinguish the degradation impacts of the effective interfacial layer and the grain boundaries of poly-Si channel film. These bias and temperature stress conditions could correspond to the positive-bias stress (PBS), positive-bias temperature instability (PBTI), negative-bias stress (NBS), negative-bias temperature instability (NBTI) and hot carrier stress (HCS). Finally, a completed reliability mechanisms of LTPS-TFT with HfO_2 gate dielectric are investigated.

3.2 Fabrication Process

The fabrication of devices started by depositing a 50-nm undoped amorphous Si (α-Si) layer at 550°C in a low-pressure chemical vapor deposition system on Si wafers capped with a 500-nm thick thermal oxide layer. Then, the α-Si layer was recrystallized by solid-phase crystallization (SPC) process in furnace at 600°C for 24-h in a N_2 ambient. A 500-nm thick plasma-enhanced chemical vapor deposition oxide was deposited at 300°C for device isolation. The oxide was then patterned and etched to define the active region of device. The source and drain regions in the active device region was implanted with phosphorus (15 keV at 5×10^{15} cm^{-2}) and activated at 600°C for 24-h annealing in a N_2 ambient. Then, a 75-nm HfO_2 was deposited in vacuum ambient without any gas flow by electron-beam evaporation system at room temperature. An O_2 treatment in furnace was applied to improve the gate oxide quality at 400°C for 30-min. A 75-nm HfO_2 with effective oxide thickness 14.7-nm is measured to indicates a high permittivity about 20 for HfO_2. In addition, a ~ 3-nm interfacial layer (IL) was also observed from the transmission electron microscopy micrograph of HfO_2 gate dielectric LTPS-TFT which is not shown here. After the patterning of contact holes, aluminum was deposited by thermal evaporation system and patterned as the probe pads to complete the TFT devices.

Devices of gate length and width of 10 and 100 μm were measured. The V_{TH} is defined as the V_G at which the I_D reaches 100 nA x W/L and $V_D = 0.1$ V. Different gate and drain bias stresses are performed at 25°C and 125°C, as shown in Fig. 3-1. Stress of $V_G = -5V, -4.1V, 5.9V$ and 10.9V represent $V_G - V_{FB} = -5V$, $V_G - V_{TH} = -5V, 5V$ and 10V, respectively. The flat-band voltage V_{FB} is defined as the gate voltage that yields the minimum drain-current from the transfer characteristic [3.16]. The field effect mobility μ_{FE} is extracted from the maximum transconductance G_m.

3.3 High-Performance LTPS-TFT with HfO_2 Gate Dielectric

Figure 3-2 shows the transfer characteristics of the HfO_2 LTPS-TFT without any passivation treatment. High performance HfO_2 LTPS-TFT with low threshold voltage V_{TH} ~ 0.9 V, excellent subthreshold swing S.S. ~ 0.147 V/decade, and high I_{on}/I_{min} current ratio ~ 2.19×10^6 is demonstrated to be suitable for the applications of AMLCD and SOP. Some important parameters are listed in Table 3-I. Compared with conventional LTPS-TFT with thick SiO_2 gate dielectric as shown in Table 3-I [3.17]-[3.20], obviously the LTPS-TFT with high-κ gate dielectric can lower the threshold voltage V_{TH}, reduce the subthreshold swing S.S., and increase the I_{on}/I_{min} current ratio without any hydrogen-related plasma treatment. The highly improved performance characteristics of LTPS-TFT with high-κ gate dielectric can be attributed to the employment of high-κ gate dielectric which can provide much higher gate capacitance density with thicker dielectric thickness and smaller gate leakage current.

3.4 Reliability Mechanisms of High-Performance LTPS-TFT with HfO_2 Gate Dielectric

In order to study the reliability mechanisms of HfO_2 LTPS-TFT, we divided the HfO_2 LTPS-TFT into three parts to discuss as shown in Fig. 3-1. They are: gate dielectric film, effective interfacial layer of HfO_2/poly-Si, and poly-Si channel film. Because the defects in the HfO_2/poly-Si interface is correlated with the defects in the poly-Si grain boundaries of the conduction channel near the HfO_2/poly-Si interface, we define the effective interfacial layer as the combination of the HfO_2/poly-Si interface and the grain boundaries of poly-Si near the surface conduction channel which is about several nano-meters below the HfO_2/poly-Si interface. Then, the distribution and mechanisms of the defects and trap states generation will be discussed as follows according to the electrical properties of the HfO_2 LTPS-TFT such as threshold voltage V_{TH}, transconductance G_m, gate leakage current, subthreshold swing S.S., and drain leakage current I_{min}.

Based on the proposed degradation mechanisms, the generation of the fixed oxide charge in the gate dielectric film would affect the threshold voltage V_{TH} and gate leakage current due to the variance in the potential of gate dielectric [3.21]. The subthreshold swing S.S. would depend on the defects in the effective interfacial layer. The deep trap states existing in the grain boundaries of the effective interfacial layer has been demonstrated to degrade mainly the subthreshold swing S.S. and much less the transconductance G_m [3.5][3.16][3.22]. Moreover, the tail trap states existing in the grain boundaries of the effective interfacial layer would mainly contribute to the degradation of the transconductance G_m and much less to the subthreshold swing S.S. [3.5][3.16][3.22]. In addition, the grain boundaries traps in the channel film would also result in the drain leakage current I_{min} [3.5][3.23]. Therefore, it is obvious that the electrical properties after stress could be used to clarify the generation and distribution of defects and trap states of the LTPS-TFTs. These proposed reliability mechanisms are summarized on the Table 3-II.

Figure 3-3 shows the I_D-V_G characteristic of HfO_2 LTPS-TFT before and after negative bias stress (NBS) and positive bias stress (PBS) with V_G = –5V, –4.1V, 5.9V and $V_D = V_S$ = 0V for 1000 seconds at T = 25°C. The threshold voltage shift ΔV_{TH} of PBS is more significant than the ΔV_{TH} of NBS. Both the subthreshold swing S.S. degradation and the fixed oxide charge generation, which is due to carrier injection, could result in the threshold voltage shift ΔV_{TH}. Figure 3-4 shows the subthreshold swing S.S. and the transconductance G_m of the HfO_2 LTPS-TFT before and after NBS and PBS, which indicates that more subthreshold swing S.S. degradation of PBS is observed than that of NBS, resulting in more threshold voltage shift ΔV_{TH} of PBS than NBS. In addition to the different subthreshold swing S.S. degradation of NBS and PBS, the flat-band voltage shifts ΔV_{FB} of NBS and PBS also show different behavior. The NBS shows a slight increase of flat-band shift ΔV_{FB} and PBS shows a significant increase of flat-band shift ΔV_{FB}. It indicates that more negative fixed charges are produced by PBS than NBS, which means that more electrons are injected into HfO_2 from channel film during PBS than electrons injection from gate during NBS. Electrons trapping in HfO_2 would raise the electron potential of HfO_2 to reduce the tunneling of electrons, resulting in the decrease of gate leakage current. Figure 3-5 shows the gate leakage current of the HfO_2 LTPS-TFT before and after NBS and PBS. A more significant gate leakage current reduction after PBS is observed than one after NBS, which consists with the results of flat-band shift ΔV_{FB} which is due to the electrons trapping in HfO_2. Therefore, the threshold voltage shifts ΔV_{TH} of PBS and NBS are mainly attributed to both the subthreshold swing S.S. degradation and electrons trapping in the HfO_2, and both the subthreshold swing S.S. degradation and electrons trapping of PBS are more serious than NBS, resulting in more threshold voltage shift ΔV_{TH} of PBS than NBS. Therefore, we can deduce that both PBS and NBS would produce the deep trap states in the effective interfacial layer because of the subthreshold swing S.S. degradation. In addition, the PBS degrades the device much more than NBS does. In addition to the threshold voltage shift ΔV_{TH} and the subthreshold swing S.S. degradation, Fig. 3-4 shows a similar transconductance degradation ΔG_m of PBS and NBS. Although the transconductance degradation ΔG_m of PBS and NBS are similar, the mechanisms of transconductance degradation ΔG_m of PBS and NBS are completely different and will be distinguished in terms of negative bias temperature stability (NBTI) and positive bias temperature instability (PBTI) and discussed as follows.

Figure 3-6 shows the I_D-V_G characteristic of HfO_2 LTPS-TFT before and after NBTI and PBTI with V_G = –5V, 5.9V and $V_D = V_S$ = 0V for 1000 seconds at T = 125°C. Similar subthreshold swing S.S. degradation and threshold voltage shift ΔV_{TH} are observed for PBTI and NBTI. However, much more serious transconductance degradation G_m of NBTI is observed than that of PBTI as shown in Figs. 3-6 and 3-7. In addition, the drain leakage current I_{min} also shows the remarkably different behavior that PBTI has a significant drain leakage current I_{min} degradation and NBTI shows a nearly invariant drain leakage current I_{min} as shown in Fig. 3-6, which indicates that the mechanism of NBTI is quite different from one of PBTI. The drain leakage current I_{min} can be attributed to two sources, one is coming from the gate leakage current and the other is coming from the junction leakage current of drain-side [3.23]. In this case, the gate leakage current as shown in Fig. 3-8 has been shown too low to contribute the drain leakage current I_{min} of devices. Therefore, we can conclude that the drain leakage current I_{min} degradation is coming from the junction leakage of drain-side, close to surface. In PBTI device, the highest drain leakage current I_{min} increase indicates the most serious grain damage in the channel film, resulting in significant increase of the drain leakage current I_{min}. Therefore, we can deduce that the PBTI would attract electrons from the channel film to inject into the HfO_2 gate dielectric. During positive bias stress, electrons would be accelerated by positive gate voltage and move toward the interface of HfO_2/poly-Si as shown in Fig. 3-9(a). The accelerated electrons would collide with the weak bond of the grain boundaries and damage the poly-Si channel film and the effective interfacial layer to generate the trap states to increase the drain leakage current I_{min}, subthreshold swing S.S., and reduce the transconductance G_m.

In addition to the PBTI, the NBTI would merely damage the effective interfacial layer to generate the trap states, increasing the subthreshold swing S.S. and reducing the transconductance G_m. Although the PBTI would degrade the grain boundaries of the channel film much more than the NBTI, the NBTI shows the most serious degradation of transconductance G_m. Therefore, the damage of NBTI would be in the effective interfacial layer which is less dependent on the drain leakage current I_{min}. Hydrogen diffusion-controlled model, which is the electrochemical reactions between the holes and the hydrogen species, has been proposed to be the degradation mechanism of the LTPS-TFTs after NBTI [3.10][3.15]. When a negative bias stress is performed, holes will accumulate at the oxide/Si interface and react with the hydrogen species which are weakly bound to Si atoms as shown in Fig. 3-9(b). The dissociation of hydrogen will then generate the interface trap states, and this is more important for high-κ gate dielectric devices due to their high density of trap states. A significant subthreshold swing S.S. degradation and transconductance G_m reduction indicates that both deep trap states and tail trap states are generated after NBTI stress.

The degradation model of LTPS-TFT under NBTI stress can be described by the following [3.15]:

$$[\equiv\mathrm{Si}-\mathrm{H}]\ (\text{interface}) + [\equiv\mathrm{Si}-\mathrm{O}-\mathrm{Si}\equiv]\ (\text{interfacial oxide})$$

$$\rightarrow [\mathrm{Si}\bullet]\ (\text{interface}) + [\equiv\mathrm{Si}^{+}] + [\equiv\mathrm{Si}-\mathrm{OH}]\ (\text{interfacial oxide}) + e^{-}.$$

The hydrogen atoms are weakly bonded to the Si atoms at the interface of the poly-silicon channel film. Under NBTI stress, hydrogen atoms react with holes from the inversion layer and dissociate from the Si atoms. The release of hydrogen atoms results in the generation of interface defects to form the deep trap states and tail trap states and degrade the subthreshold swing S.S. and transconductance G_m, respectively.

Furthermore, a 5V drain bias is applied during NBS and PBS to investigate the impacts of the drain bias stress. Figure 3-10 shows that more serious transconductance G_m and subthreshold swing S.S. degradation of NBS with V_D = 5V than V_D = 0V is observed. Contrary to the NBS with drain bias stress, PBS with V_D = 5V shows a slight improvement of the transconductance G_m and subthreshold swing S.S. degradation compared with PBS with V_D = 0V. In addition, NBTI and PBTI with V_D = 5V at T = 125°C are also studied as shown in Fig. 3-11. The same trend of the transconductance G_m and subthreshold swing S.S. degradation is also observed compared with NBS and PBS with drain bias applying. However, for the PBTI case, the drain leakage current is decreased with V_D = 5V compared with V_D = 0V as shown in Fig. 3-6. It is because that the applying of a drain bias would make the vertical electric field near the drain side be lower and improve the drain leakage current I_{min} slightly. When a larger drain bias was applied during PBTI, the vertical electric field of the channel film would be decreased in further. As shown in Fig. 3-12, applying a drain bias would decrease the vertical field near the drain side and result in less junction damage. Therefore, the large drain bias would make the device have less drain leakage current I_{min} degradation, and a hump in transfer characteristic of the device is observed as shown in Fig. 3-13. For the NBTI case, applying a drain bias would increase the vertical field near the drain side as shown in Fig. 3-12 and result in more serious transconductance G_m and subthreshold swing S.S. degradation. This appearance of asymmetry damage of source/drain junction region is also observed in the previous study [3.10][3.11]. In addition, the transconductance G_m of the HfO_2 LTPS-TFT would be decreased as the drain bias increasing after V_D = 10V to indicate that impact ionization effect of hot carrier stress [3.11] is appearing as shown in Fig. 3-13. Therefore, the stress of vertical electric field is more important than the stress of lateral electrical field for the HfO_2 LTPS-TFT before the occurring of hot carrier stress, and the impact ionization of the HfO_2 LTPS-TFT dominates the degradation when the large drain bias stress is applying.

The electron trapping in the gate dielectric and the trap states generation of channel film and interface regions are observed for both HfO_2 LTPS-TFT and the conventional thick SiO_2 LTPS-TFT after PBS stresses [3.14][3.18]. In addition, the significant subthreshold swing S.S. degradation of HfO_2 LTPS-TFT and SiO_2 LTPS-TFT after NBS stresses are observed [3.9][3.10][3.18]. However, the location of traps generation in interface or channel film is difficult to determine after PBS and NBS stresses. The mechanism of NBTI of LTPS-TFT proposed by Chen *et al.* would be adopted to explain the behavior of NBS [3.15]. Therefore, the reliability mechanisms of positive gate bias stress and negative bias stress can be systematically analyzed by studying the electrical characteristics of LTPS-TFT after NBS, PBS, NBTI and PBTI stresses.

Comparing the stresses of HfO_2 LTPS-TFT with the conventional thick SiO_2 LTPS-TFT, the effective electric field of stress E_{eff} in the channel film ($E_{eff} = V_G/t_{dielectric} \times \varepsilon_{dielectric}/\varepsilon_{silicon}$) is quite different. The $t_{dielectric}$, $\varepsilon_{dielectric}$, and $\varepsilon_{silicon}$ are defined as the gate dielectric thickness, gate dielectric permittivity, and silicon permittivity, respectively. The stress field of HfO_2 LTPS-TFT would be higher than that of conventional thick SiO_2 LTPS-TFT. Large gate bias stress at high temperature can accelerate the degradation to distinguish between positive gate bias stress and negative bias stress. The remarkable I_{min} degradation behavior after PBTI is not observed in previous works [3.9][3.10][3.14][3.18] due to higher vertical stress field of HfO_2 LTPS-TFT. In addition, the hole trapping in gate dielectric after PBS and PBTI is not found in our work. It could be due to the characteristic of high-κ gate dielectric in which electron trapping is easier than hole trapping. Moreover, the stress of vertical electric field is the dominant factor for the hot carrier stress of HfO_2 LTPS-TFT, which is completely different with previous report [3.14]. It would be due to the characteristic of high-κ gate dielectric that the ability of charge trapping is more significant than SiO_2.

So far we have analyzed the reliability mechanisms of LTPS-TFT with HfO_2 gate dielectric. The employment of high-κ gate dielectric gives an effective way to keep the performance of LTPS-TFT at low operation voltage. In addition, many defect passivation methods have been proposed to improve the reliability of LTPS-TFT [3.24][3.25]. High performance and reliability LTPS-TFT with high-κ gate dielectric will be one of the most possible solutions to realize the target of system-on-panel.

3.5 Summary

A comprehensive investigation of the reliability mechanisms of high performance LTPS-TFT with HfO_2 gate dielectric is studied in this Chapter. Various stress conditions, including PBS, PBTI, NBS, NBTI and hot carrier stress, are performing to differentiate the degradation mechanisms. For PBS and PBTI, it is found that serious subthreshold swing S.S. degradation is due to the deep trap states of the effective interfacial layer; transconductance G_m decrease with the drain leakage current I_{min} increase is due to the tail trap states of poly-Si grain boundaries, and gate leakage current reduction is due to electrons trapping of the HfO_2 gate dielectric. For NBS and NBTI, significant subthreshold swing S.S. and transconductance G_m degradation without the drain leakage current I_{min} increase are observed to show that the effective interfacial layer is the main damage region that both deep and tail trap states are generated after NBS and NBTI. Remarkable drain leakage current I_{min} increase of PBTI and almost invariant drain leakage current I_{min} degradation of NBTI show that PBTI and NBTI are attributing to different mechanisms. The carrier collision and injection model is employed to explain the mechanism of PBS and PBTI, and the hydrogen diffusion model is employed to explain the mechanism of NBS and NBTI. In addition, the drain bias applying during stress is also studied, and the results show that the applied of drain bias would affect the vertical electric field near the drain side of LTPS-TFT, resulting in the less degradation for PBS and PBTI, and more serious degradation for NBS and NBTI. Moreover, the degradation of LTPS-TFT due to impact ionization will dominate the degradation mechanism if a large drain bias stress is applied.

Table 3-I. Device parameter comparison of the HfO_2 gate dielectric TFTs. Other gate dielectric TFTs are also listed for comparison.

Parameters	HfO_2	$AlLaO_3$ [3.19]	Al_2O_3 [3.20]	LPCVD Oxide [3.17]	PECVD Oxide [3.18]
V_{TH} (V)	0.9	1.2	3	5.6	8.14
EOT (nm)	14.7	8.7	19.5	80	60
S.S. (V/dec.)	0.147	0.31	0.44	1.4	1.97
I_{on}/I_{min} (10^6)	2.19	1.5	0.3	0.35	0.297

Table 3-II. Degradation of experimental electrical characteristics and corresponding possible degradation mechanisms

Defect location	**Impacts of electrical characteristics**	**Cause**
Gate dielectric film	**1. Threshold voltage V_{TH} (V)** **2. Flat-band voltage V_{FB} (V)** **3. Gate leakage current (A)**	**Fixed oxide charge**
Effective interfacial layer of HfO_2/poly-Si	**1. Subthreshold Swing (S.S.)** **2. Threshold voltage V_{TH} (V)** **3. Transconductance G_m (S)**	**1. deep trap states** **2. deep trap states** **3. tail trap states**
Poly-Si channel film	**1. Transconductance G_m (S)** **2. Drain leakage current I_{min} (A)**	**1. tail trap states** **2.deep & tail states**

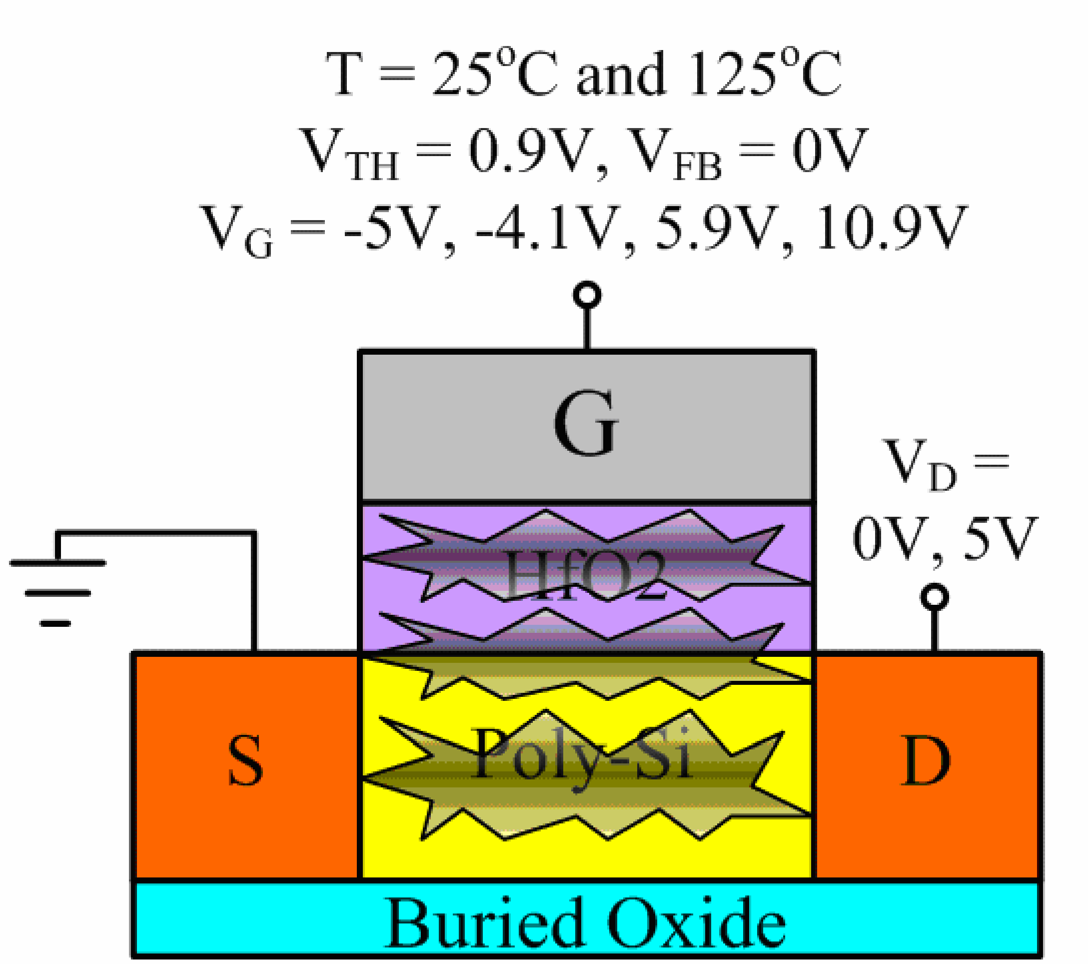


Fig. 3-1. The cross-section structure of Al/HfO_2/poly-Si n-channel LTPS-TFT with different V_G and V_D stress bias for 1000-s. The locations of stress damage are also indicated.

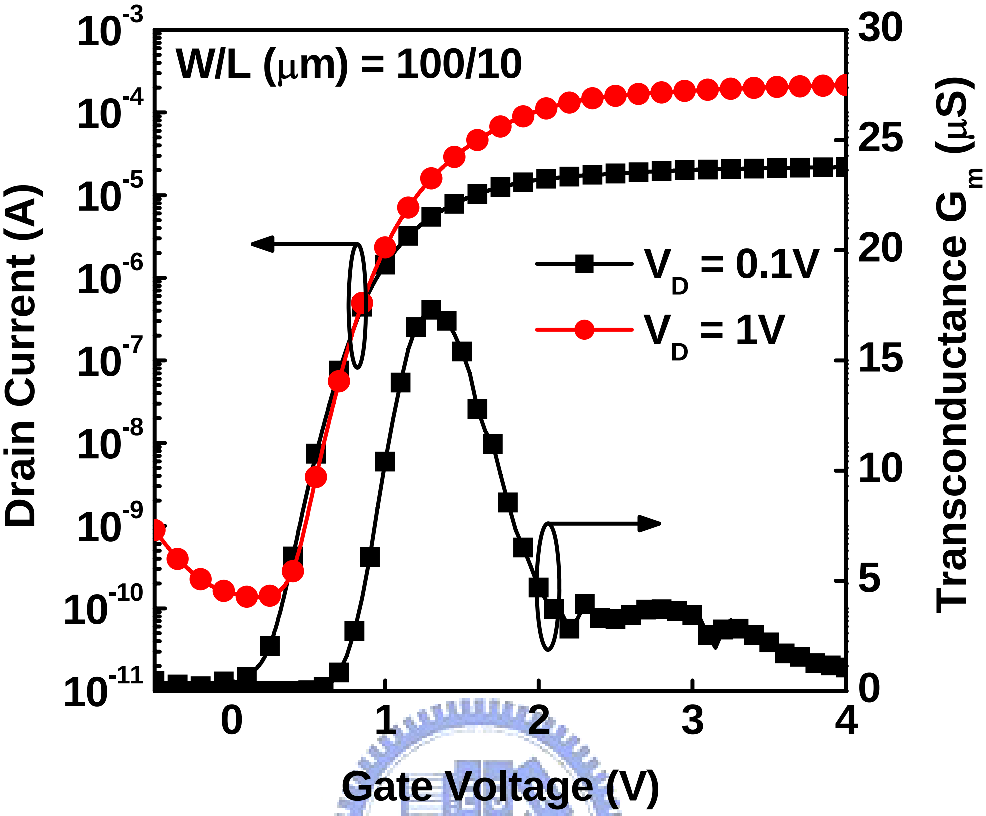


Fig. 3-2. The I_D-V_G and transconductance G_m characteristics of the HfO_2 LTPS-TFT with W/L = 100 μm/10 μm.

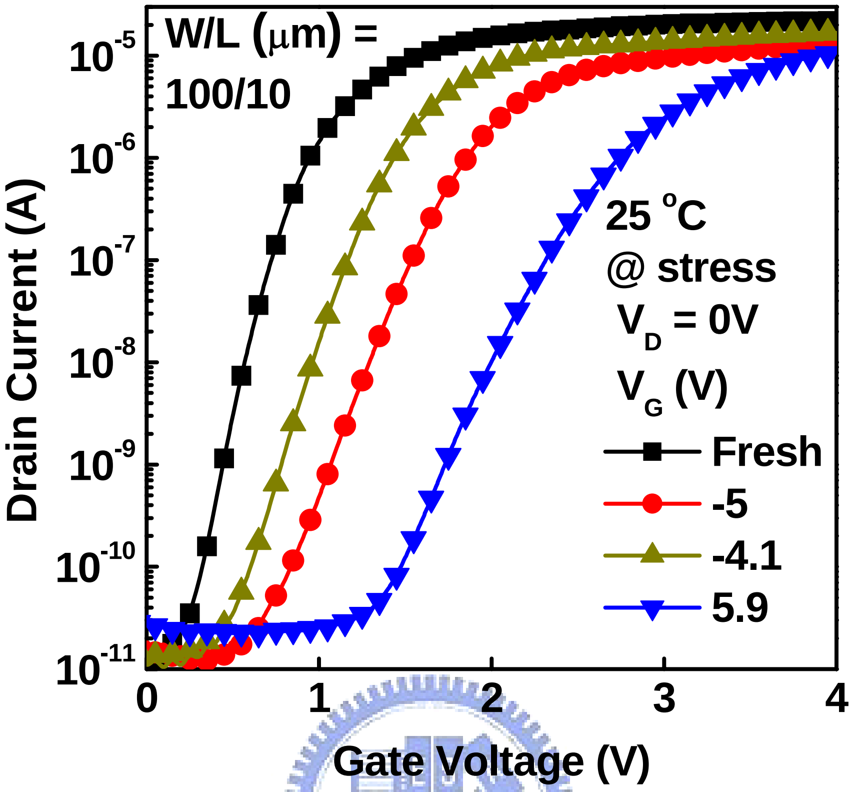


Fig. 3-3. The I_D-V_G characteristics of the HfO_2 LTPS-TFT before and after different gate bias stresses with fixed V_D = 0V for 1000-s at 25°C.

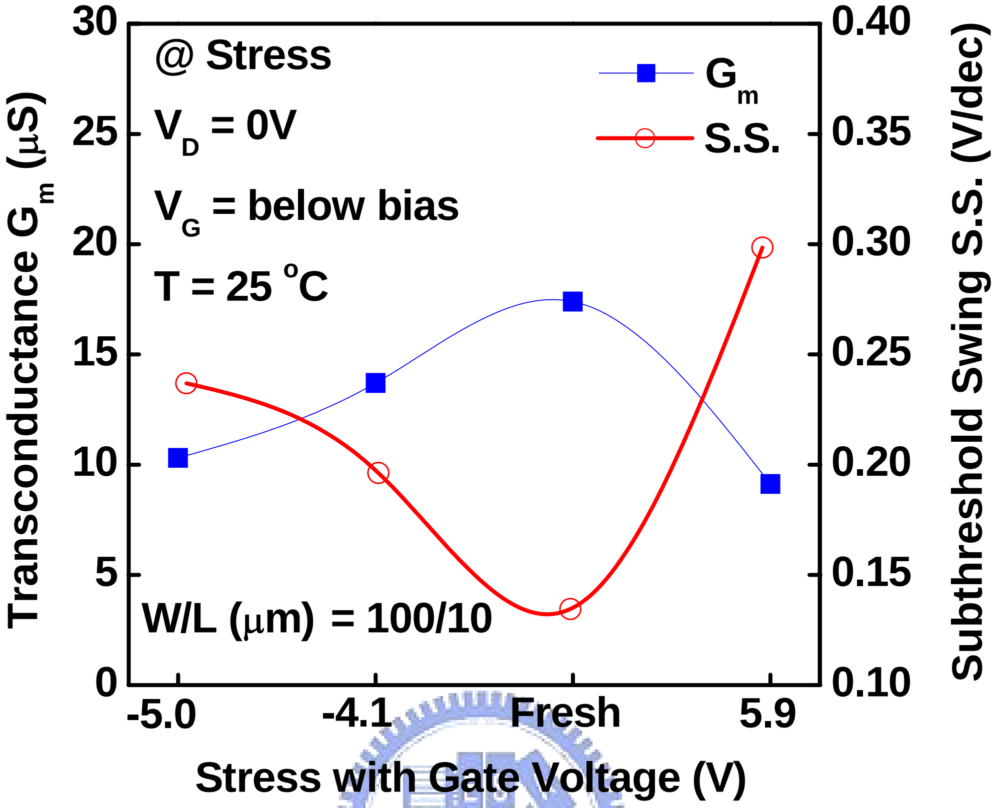


Fig. 3-4. The transconductance G_m and subthreshold swing S.S. of the HfO_2 LTPS-TFT before and after different gate bias stresses with fixed V_D = 0V for 1000-s at 25°C.

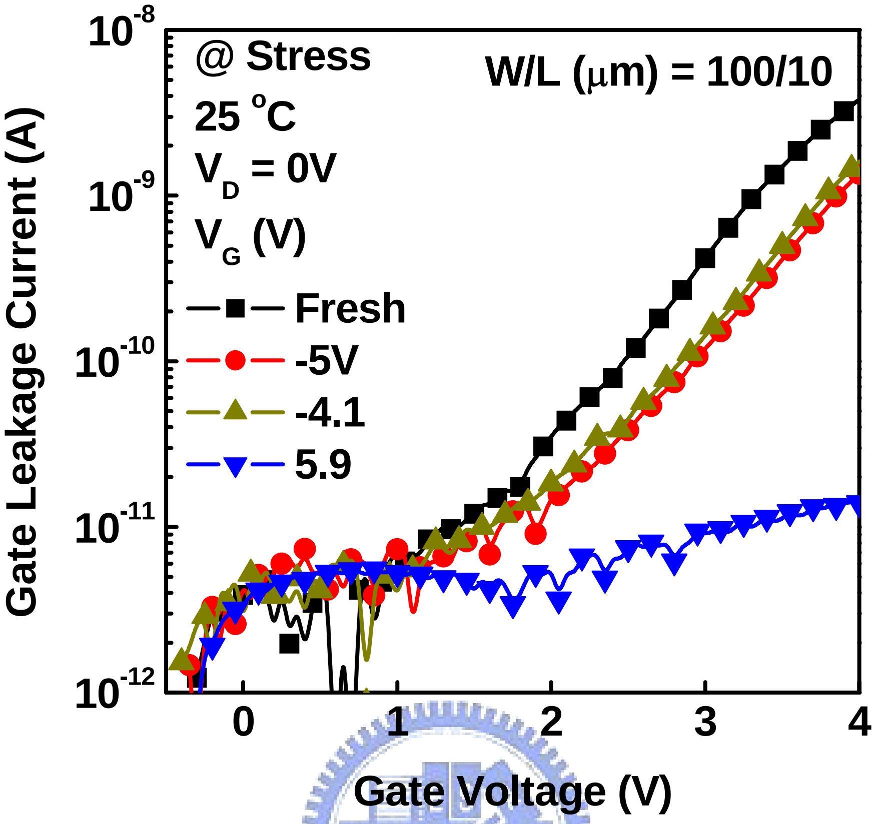


Fig. 3-5. The gate leakage current of the HfO_2 LTPS-TFT before and after different gate bias stresses with fixed V_D = 0V for 1000-s at 25°C.

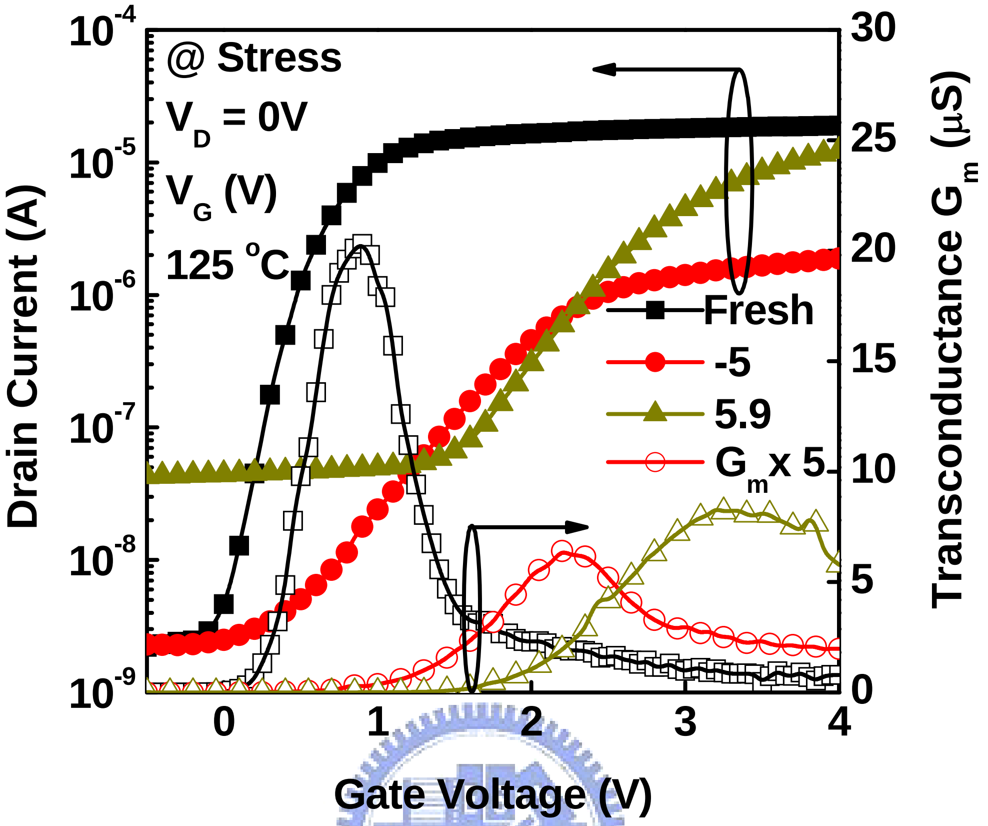


Fig. 3-6. The I_D-V_G and transconductance G_m characteristics of the HfO_2 LTPS-TFT before and after different gate bias stresses with fixed V_D = 0V for 1000-s at 125°C.

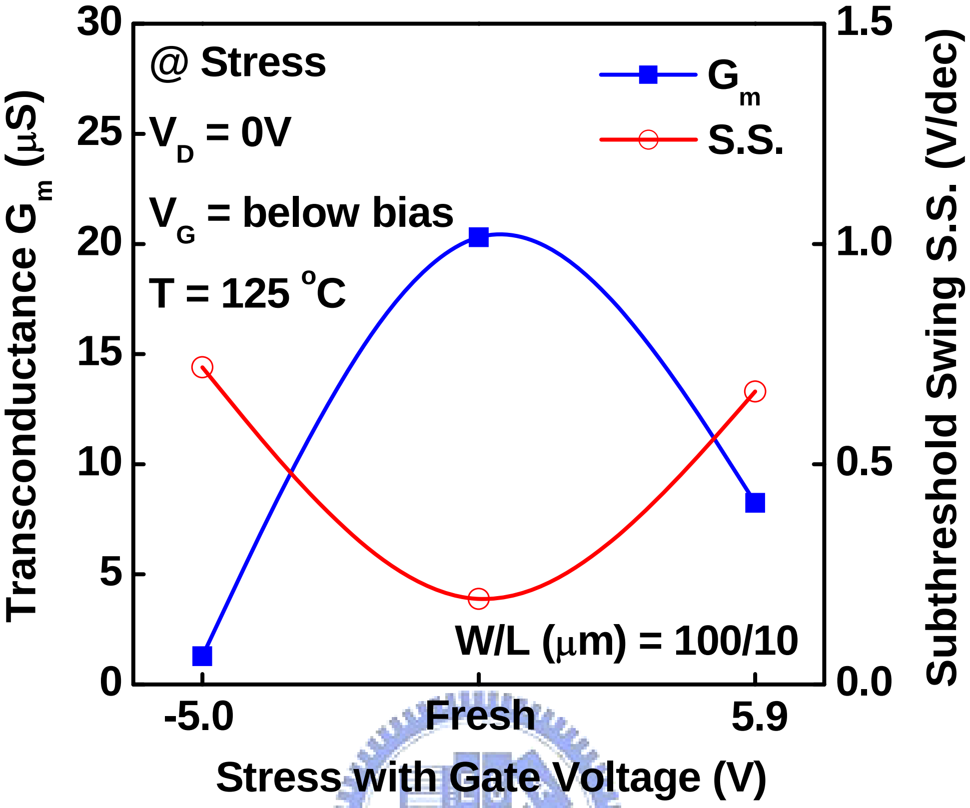


Fig. 3-7. The transconductance G_m and subthreshold swing S.S. characteristics of the HfO_2 LTPS-TFT before and after different gate bias stresses with fixed V_D = 0V for 1000-s at 125°C.

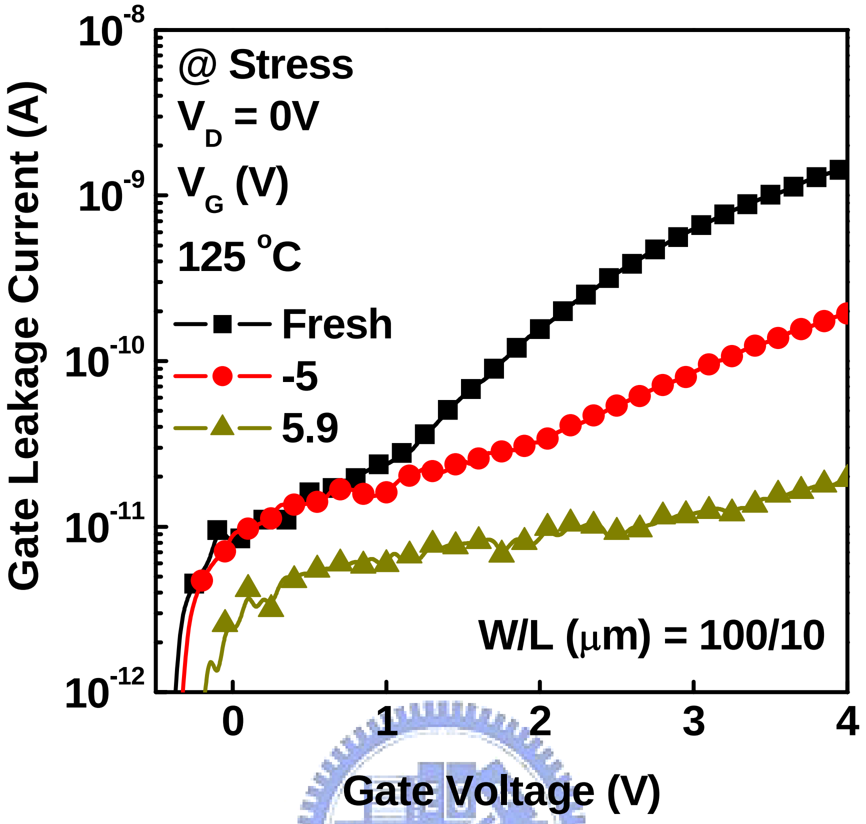
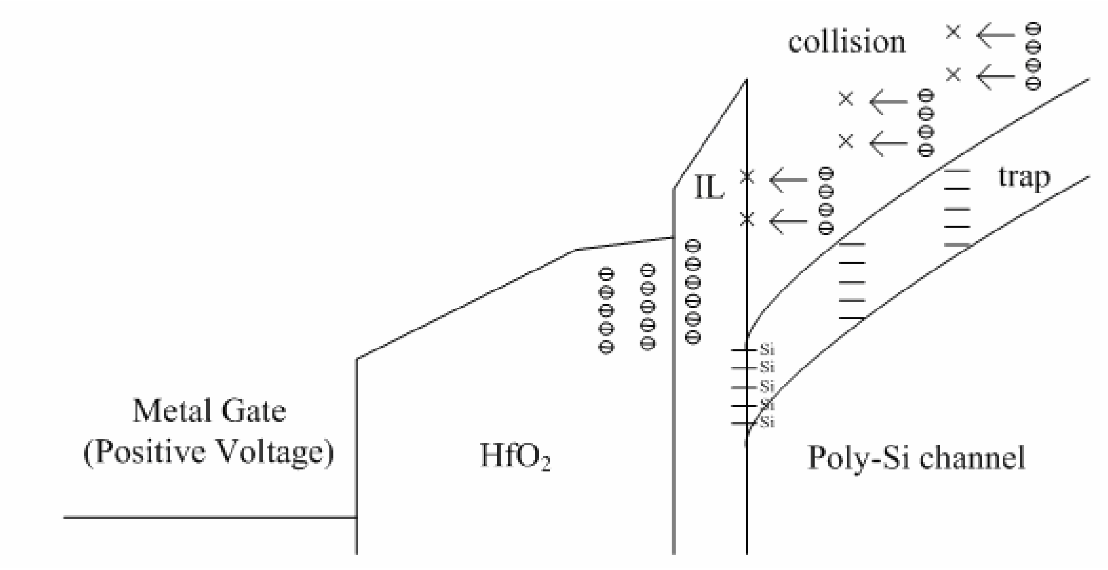
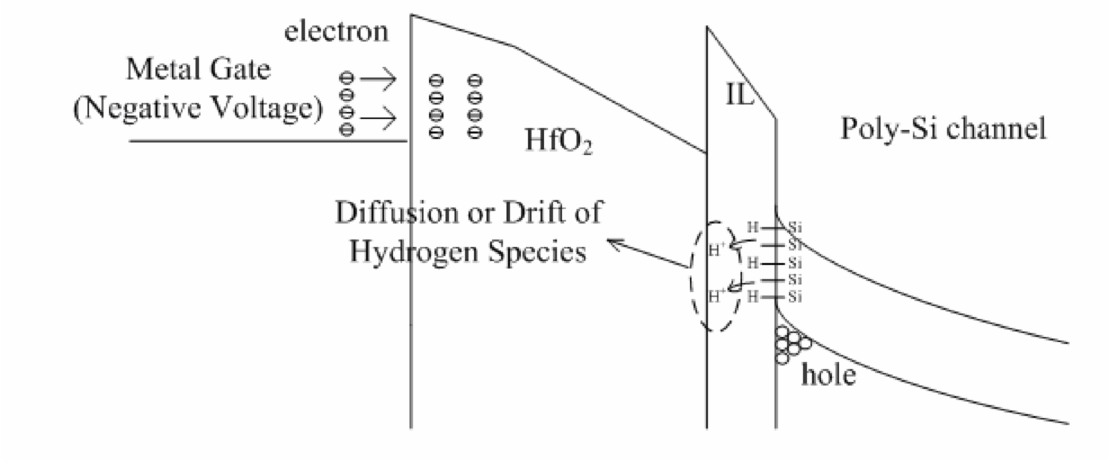


Fig. 3-8. The gate leakage current of the HfO_2 LTPS-TFT before and after different gate bias stresses with fixed V_D = 0V for 1000-s at 125°C.



(a)



(b)

Fig. 3-9. Energy band diagram of the HfO_2 LTPS-TFT under (a) PBTI and (b) NBTI stress.

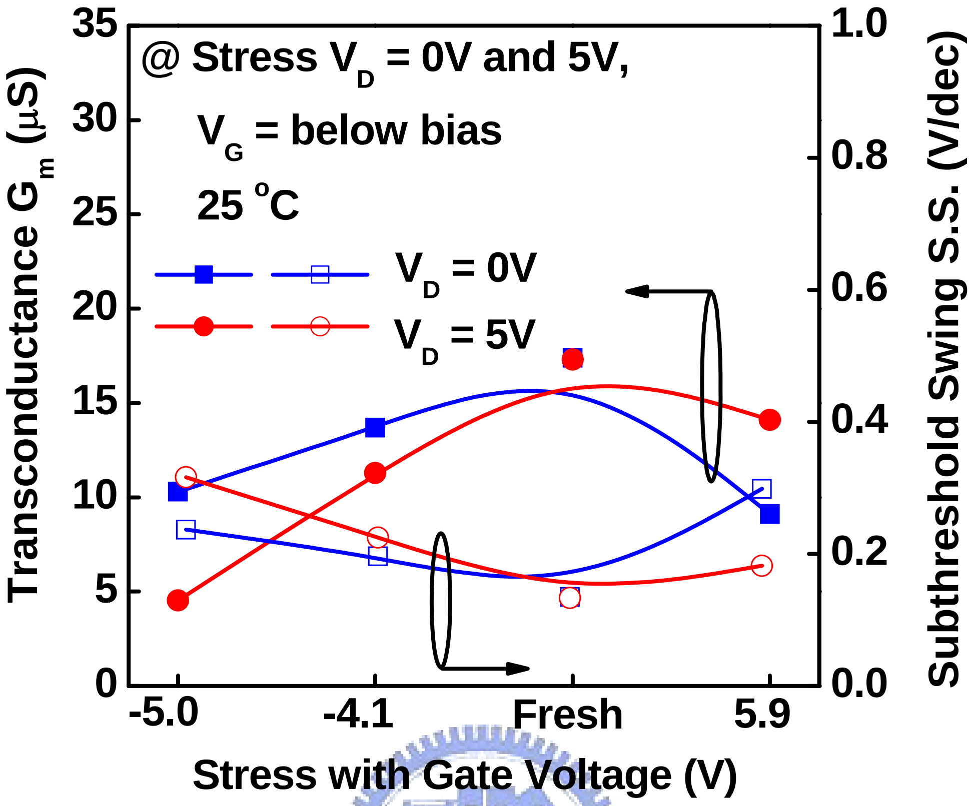


Fig. 3-10. The transconductance G_m and subthreshold swing S.S. characteristics of the HfO_2 LTPS-TFT before and after different gate bias stresses with fixed V_D = 0V and V_D = 5V for 1000-s at 25°C.

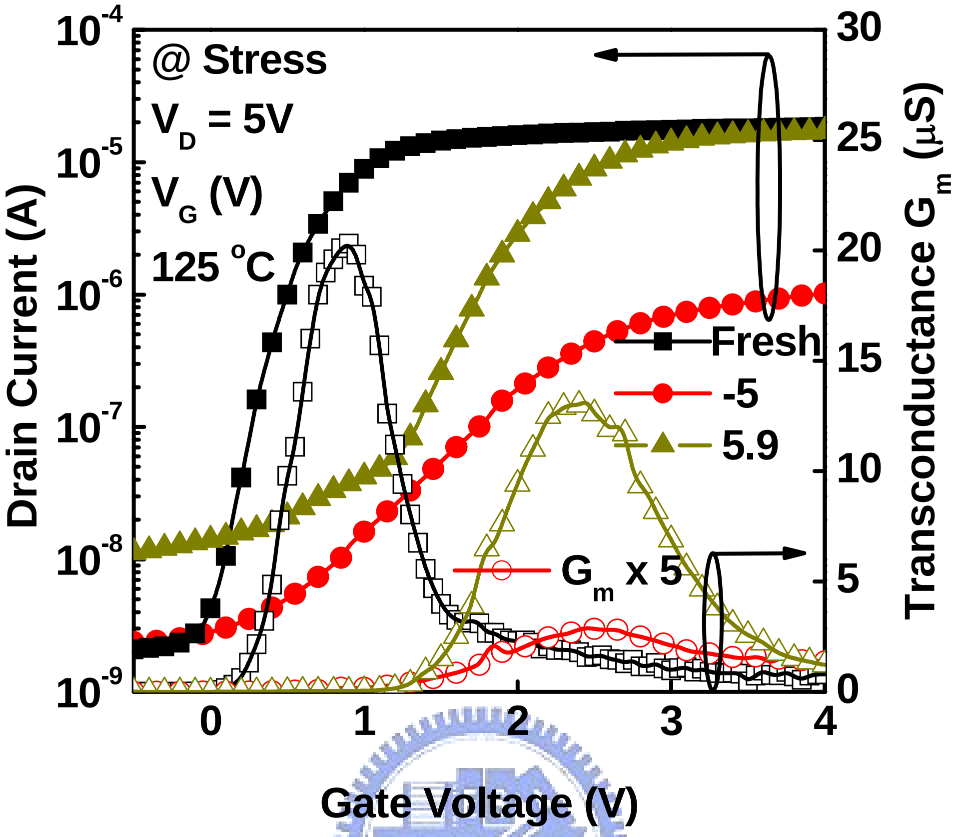


Fig. 3-11. The I_D-V_G and transconductance G_m characteristics of the HfO_2 LTPS-TFT before and after different gate bias stresses with fixed V_D = 5V for 1000-s at 125°C.

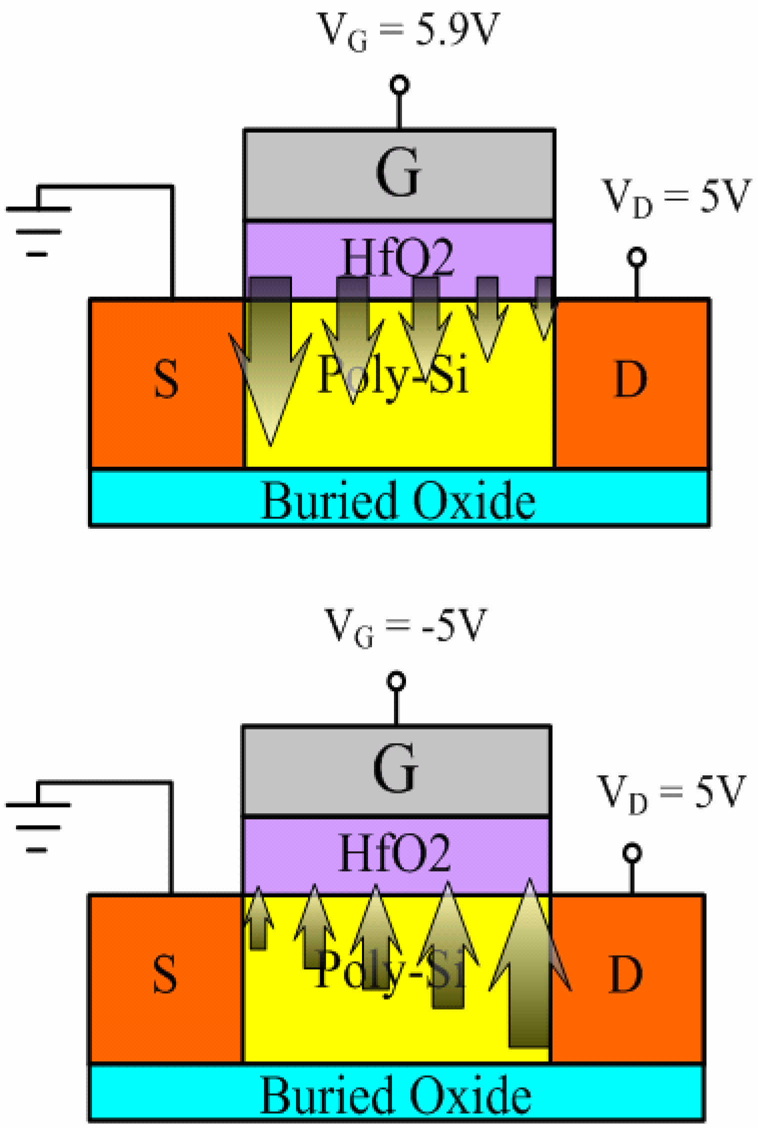


Fig. 3-12. The cross-section structure of Al/HfO_2/poly-Si n-channel LTPS-TFT with drain bias stress for 1000-s. The magnitudes of vertical electric field are also indicated.

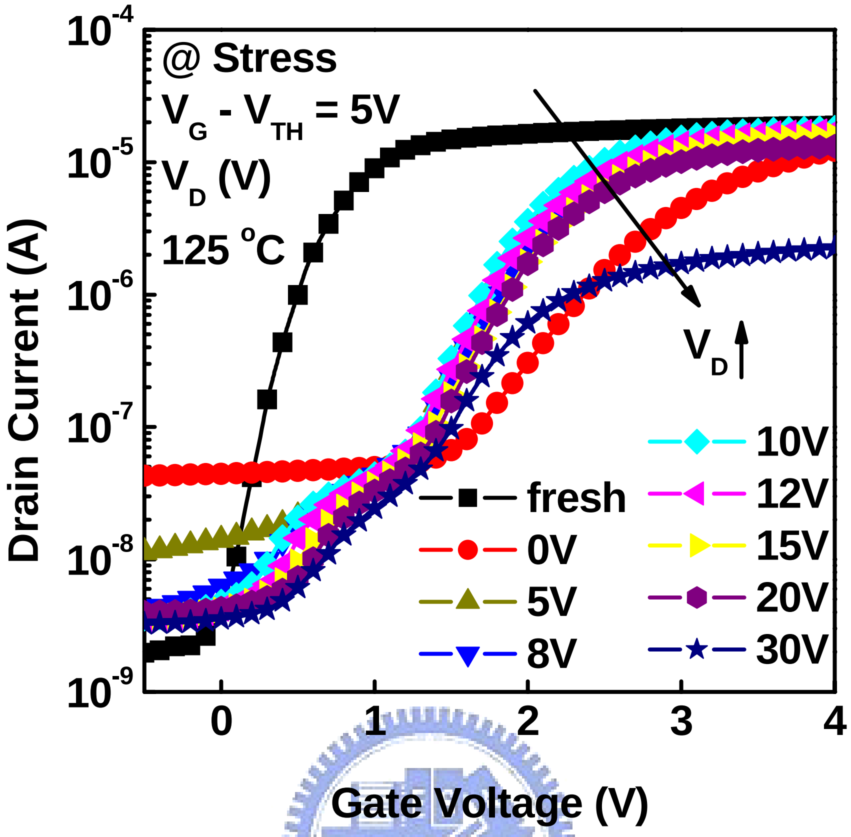


Fig. 3-13. The I_D-V_G characteristics of the HfO_2 LTPS-TFT before and after different drain bias stresses with fixed $V_G – V_{TH}$ = 5V for 1000-s at 125°C.

Chapter 4

Impacts of Fluorine and Nitrogen Ion Implantation on Low-Temperature Polycrystalline-Silicon Thin-Film Transistor with HfO_2 Gate Dielectric

4.1 The Fluorine Ion Implantation Before Solid Phase Crystallization

4.1.1 Introduction

As mention in the Chapter 1, there are many defects at the grain boundary of poly-Si channel film, resulting in the degradation of performance of low-temperature polycrystalline-silicon thin-film transistors (LTPS-TFTs) [4.1]. In order to make the channel be more conductive, grain traps of the poly-Si channel film must be passivated. Therefore, a large operation voltage was needed for the conventional LTPS-TFTs without any defects passivation [4.2]-[4.6]. The grain defects of the poly-Si channel film would result in poor subthreshold swing (S.S.), high minimum drain-current (I_{min}) and large threshold voltage (V_{TH}).

The adopting of high-κ gate dielectric is one of effective ways to improve the performance of LTPS-TFTs [4.7]-[4.9] as shown in Chapters 2 and 3. A larger gate capacitance with the same physical thickness by using high-κ gate dielectric instead of SiO_2 gate oxide can attract more carriers with a smaller voltage to turn on the LTPS-TFTs. In spite of the employment of high-κ gate dielectrics, the defects of the poly-Si channel film still exist that contribute to high drain leakage current [4.1]. Therefore, defects passivation is necessary to improve the drain leakage current and

I_{on}/I_{min} current ratio. Hydrogen plasma treatment is the most popular approach used to passivate defects and reduce the leakage current [4.10]-[4.12]. However, the introduction of hydrogen would degrade the reliability due to the weak Si-H bonds [4.13][4.14]. In Chapter 2, we have demonstrated the defects passivation methods by the employment of O_2, N_2, and NH_3 plasma surface treatment. However, the plasma treatment would have some process issues. The concentration of plasma species, like O, N and H, is difficult to control. In addition, the time of plasma treatment would significantly affect the electrical characteristics of LTPS-TFTs. To solve this problem, fluorine ion implantation is a promising alternative to create strong Si-F bonds [4.2]-[4.6] to enhance the performance and reliability of LTPS-TFTs. High temperature subsequent processes (≧700°C) after fluorine implantation have been used for the deposition of TEOS gate dielectric layer and passivation layer in 700°C over 3hr [4.3][4.4], and the growth of thermal oxide and dopant activation in 850°C [4.5][4.6], resulting in fluorine ions diffuse to the interfaces of gate-oxide/poly-Si and poly-Si/buried-oxide and pile up in the interfaces. However, fluorine implantation with a low temperature solid-phase crystallized activation (≦600°C) has not been studied yet. In this Chapter, we found that the distribution of fluorine ions is totally different from that at high temperature, and the electrical performance can be significantly improved.

4.1.2 Fabrication Process

The fabrication of devices started by depositing a 50-nm undoped amorphous Si (α-Si) layer at 550°C in a low-pressure chemical vapor deposition system on Si wafers capped with a 500-nm thick thermal oxide layer. Then, the fluorine atoms were implanted at energy of 11 keV to a dosage of 5×10^{14} cm^{-2}. The α-Si layer was recrystallized by solid-phase crystallization (SPC) process in furnace at 600°C for

24-h in a N_2 ambient. A 500-nm thick plasma-enhanced chemical vapor deposition oxide was deposited at 300°C for device isolation. The oxide was then patterned and etched to define the active region of device. The source and drain regions in the active device region was implanted with phosphorus (15 keV at 5 x 10^{15} cm^{-2}) and activated at 600°C for 24-h annealing in a N_2 ambient. Then, a 75-nm HfO_2 was deposited by electron-beam evaporation system. An O_2 treatment in furnace was applied to improve the gate oxide quality at 400°C for 30-min. After the patterning of contact holes, aluminum was deposited by thermal evaporation system and patterned as the probe pads to complete the TFT devices. There is not any high temperature processes (≧600°C) during device fabrication.

Figure 4-1 shows the cross-sectional transmission electron microscopy (TEM) micrograph of HfO_2 gate dielectric TFT structure. The measured device has gate length and width of 10 and 100 μm, respectively. The V_{TH} is defined as the gate voltage at which the drain current reaches 100 nA x W/L under V_D = 0.1 V. The field effect mobility μ_{FE} is extracted from the maximum transconductance (G_m).

4.1.3 Discussion

Figure 4-2 shows the secondary ion mass spectrometer (SIMS) spectrum of HfO_2 LTPS-TFT with fluorine implantation. We can observe that fluorine ions after post-implanted low temperature SPC activation are merely piling up at the poly-Si/buried-oxide interface and not observed in the HfO_2/poly-Si interface. This distribution of fluorine ions is different from the results of high temperature annealing that fluorine ions would pile up at the interfaces of both gate-oxide/poly-Si and poly-Si/buried-oxide [4.3]-[4.6]. This implies that SPC activation of α-Si with fluorine pre-implantation would not affect the upper part of the channel film. The impacts of fluorine pre-implantation with low temperature SPC activation on the performance of HfO_2 LTPS-TFTs are shown in Fig. 4-3. High performance characteristics of HfO_2 LTPS-TFT with low V_{TH} ~ 1 V, excellent subthreshold swing (S.S.) ~ 0.147 V/decade, high mobility ~ 74.5 cm^2/V-s, and high I_{on}/I_{min} current ratio ~ 2.19 x 10^6 is observed without any treatment. After fluorine implantation, we can observe that the I_{min} is reduced significantly from 9.78 pA to 1.09 pA at V_D = 0.1 V. The I_{min} can be attributed to the junction leakage current which is dominated by the grain-boundary trap-state densities (N_{trap}) of poly-Si channel film [4.1]. The effective grain-boundary trap-state densities (N_{trap}) with and without fluorine implantation are also estimated by Levinson and Proano method [4.15][4.16]. Figure 4-4 exhibits the plots of ln [$4.I_{DS}/(V_{GS} - V_{FB})$] versus $1/(V_{GS} - V_{FB})^2$ curves at V_{DS} = 1 V and high V_{GS}, where the flat-band voltage (V_{FB}) is defined as the gate voltage that yields the minimum drain-current from the transfer characteristic. From Fig. 4-4, it is apparent that the effective grain-boundary trap-state densities decrease from 3.530 x 10^{12} cm^{-2} to 2.624 x 10^{12} cm^{-2} after fluorine passivation. This indicates that about 25.6 % reduction in the effective grain-boundary trap-state densities is achieved due to the passivation of the grain-boundary trap-state densities in the lower part of the channel film. The important parameters of LTPS-TFTs are listed in the table 4-I. A slight increase of V_{TH} from 1.01 V to 1.32 V is observed after fluorine implantation. This is because that lots of fluorine ions are incorporated in the buried oxide to form the negative fixed oxide charges to affect the channel film [4.17]. This sub-gate effect would make the channel less conductive thus increase the V_{TH} [4.5]. However, the behaviors of significant I_{min} reduction and a slight V_{TH} increase of the fluorinated n-channel TFTs can not be found in the previous reports [4.3]-[4.6].

In addition to the performance enhancement of HfO_2 LTPS-TFT, the reliability of the devices under hot carrier stress with $V_D = 2(V_G – V_{TH})$ = 10 V for 1000 second is also studied as shown in Fig. 4-3. The behavior of about one order reduction of I_{min} in the fluorinated TFT still maintains and shows a better threshold voltage instability ΔV_{TH} from 1.02 V to 0.89 V. It also demonstrates that the treatment method of fluorine pre-implantation with low temperature SPC activation would improve the reliability of LTPS-TFTs as the previous reports [4.3]-[4.6]. Hydrogen treatment can also reduce the I_{min} effectively. However, the introduction of hydrogen would seriously degrade the reliability of LTPS-TFTs and easily release during mediate temperature process (≧500°C) [4.13][4.14].

In addition to the stress condition of hot carrier stress with $V_D = 2(V_G - V_{TH}) = 10$ V for 1000 second, other stress conditions are also performed to study. Because the operation voltage of LTPS-TFTs with TaN/HfO_2 gate stack structure was within 3 V, we employee the hot carrier stress with $V_{GS} - V_{TH} = V_{DS} = 5$ V for 1000 seconds instead of $V_{GS} = V_{DS} = 5$V because that different hot carrier stability is observed under different V_{GS} and constant V_{DS} [4.18]. The threshold voltage stability ($\Delta V_{TH} = V_{THf} - V_{THi}$) was improved from 1.6 V to 1.22 V of the threshold voltage shift after 1000 seconds hot carrier stress as shown in the Fig. 4-5. Positive voltage shifts of threshold voltage indicate that the electrons were trapped by the gate dielectric HfO_2 under hot carrier stress. The fluorine implanted device shows a smaller threshold voltage shift indicates that fewer electrons were trapped in HfO_2 after fluorine passivation. Figure 4-6 shows the gate leakage current of LTPS-TFT with and without fluorine ion implantation. A smaller reduction rate of gate leakage current of the fluorine-implanted device under hot carrier stress was observed, which shows a smaller electron trapping rate than the device without fluorine ion implantation.

Figure 4-7 shows the transconductance G_m degradation of the LTPS-TFT with and without fluorine ion implantation. For the device without fluorine ion implantation, a suddenly high degradation rate of transconductance G_m was happened within 50 seconds of hot carrier stress, and then a saturation behavior was observed.

For the fluorine-implanted device, the suddenly high degradation rate region of transconductance G_m was within 20 seconds. In addition, the degradation of transconductance G_m after 1000 seconds of hot carrier stress was more serious for the LTPS-TFT with fluorine ion implantation. In the short stress time regime, the degradation of G_m for the fluorine-implanted device is smaller than that of the device without fluorine implantation. Because the grain boundaries and the high-κ/poly-Si interface of the fluorine-implanted device were passivated by the strong Si–F bonds, the device was less degraded as the stress was initially performed. As stress time increases, the fluorine-implanted device shows a larger degradation rate in G_m than the one without fluorine implantation. We attributed the severe degradation of the fluorine-implanted device to the more strict stress current, and this can be further explained from Fig. 4-8, which shows the time dependence of the driving current under hot carrier stress.

It is worth noting that the fluorine-implanted device shows a larger driving current through all the stress time. The degradation improvement of driving current is attributed to the defects passivation by fluorine. *Chern et al.* have proposed that the fluorine can passivate uniformly the band tail-states, which are produced due to strain bond, and midgap deep-states, which are produced due to dangling bond, within the poly-Si channel film [4.6]. Fluorine can break the strain bond of channel film, like Si-Si and Si-O-Si bond, to relax the local strain and also passivate the dangling bonds in grain boundaries and HfO_2/polysilicon interface [4.19]-[4.21]. Therefore, hot carrier immunity is enhanced due to the strong Si-F bond.

Finally, a high performance LTPS-TFT with low threshold voltage ~ 1.38 V, ultra-low subthreshold swing 0.132 V/decade, high I_{on}/I_{min} current ratio 1.21×10^7, and strong hot carrier immunity is derived. Consequently, the metal-gate/high-κ LTPS-TFTs with fluorine implantation is demonstrated for the first time.

4.1.4 Summary

High-performance LTPS-TFT with HfO_2 gate dielectric and fluorine pre-implantation has been demonstrated. Low temperature SPC activation of fluorine ions is reported for the first time and it also provide an improved electrical characteristics and reliability.

4.2 The Nitrogen Ion Implantation After Solid Phase Crystallization

4.2.1 Introduction

In addition to the fluorine ion implantation to create strong Si-F bonds, nitrogen ion implantation (NII) is also another promising method to create strong Si-N bonds to enhance the performance and reliability of LTPS-TFTs [4.22]-[4.23]. Nevertheless, the NII treatment of LTPS-TFT with low temperature SPC process has not been reported yet. In this Chapter, we demonstrate the high performance CMOS LTPS-TFT with the employment of high-κ gate dielectric HfO_2 and the treatment of NII after SPC process.

4.2.2 Fabrication Process

The fabrication of devices started by depositing a 50-nm undoped amorphous Si (α-Si) layer at 550°C in a low-pressure chemical vapor deposition system on Si wafers capped with a 500-nm thick thermal oxide layer. Then, the α-Si layer was recrystallized by SPC process in furnace at 600°C for 24-h in a N_2 ambient. After the crystallization of channel film, the nitrogen atoms were implanted with energy of 10 keV and a dosage of 1×10^{14} cm^{-2} and 5×10^{14} cm^{-2}. After NII, a 500-nm thick plasma-enhanced chemical vapor deposition oxide was deposited at 300°C for device isolation. The oxide was then patterned and etched to define the active region of device. The source and drain regions in the active device region was implanted with phosphorus (15 keV at 5 x 10^{15} cm^{-2}) and boron (10 keV at 5 x 10^{15} cm^{-2}) and activated at 600°C for 24-h SPC annealing in a N_2 ambient. Then, a 45-nm HfO_2 was deposited by electron-beam evaporation system. An O_2 treatment in furnace was applied to improve the gate oxide quality at 400°C for 30-min. After the patterning of contact holes, aluminum was deposited by thermal evaporation system and patterned as the probe pads to complete the TFT devices. There is not any high temperature processes (> 600°C) during device fabrication.

The measured device has gate length and width of 10 and 100 μm, respectively. The V_{TH} is defined as the gate voltage at which the drain current reaches 10 nA x W/L under V_D = 0.1 V. The μ_{FE} is extracted from the maximum transconductance (G_m).

4.2.3 Discussion

Figures 9 and 10 show the transfer characteristics (I_D-V_G and G_m) of n-channel and p-channel LTPS-TFTs with HfO_2 gate dielectric and NII treatment. The important parameters of intrinsic n-channel and p-channel LTPS-TFTs without any treatment are listed in Tables II and III, respectively, which conventional LTPS-TFTs with thick SiO_2 gate dielectric and other's work are included. The significant performance improvements of LTPS-TFTs are observed as shown in Tables II and III when the SiO_2 gate dielectric is replaced by the HfO_2 gate dielectric. For n-channel LTPS-TFT, the threshold voltage V_{TH} and subthreshold swing S.S. are significantly reduced from 6.8 V and 1.41 V/dec. to 1.13 V and 0.248 V/dec., respectively. For p-channel LTPS-TFT, the threshold voltage V_{TH} and subthreshold swing S.S. are significantly reduced from –13.3 V and 1.60 V/dec. to –0.93 V and 0.143 V/dec., respectively. The improvements of threshold voltage V_{TH} and subthreshold swing S.S. are attributed to the high gate capacitance density [4.7]-[4.9]. In addition, the field effect carrier mobility μ_{FE} improvement of LTPS-TFTs with high-κ gate dielectric is due to the native-growth of SiO_2-like interfacial layer between the high-κ and poly-Si interface, resulting in the elimination of trap states of the effective interfacial layer [4.7]-[4.9]. In addition to the employment of HfO_2 gate dielectric, Figs. 9 & 10 and Table I & II also show the electrical characteristics of n-channel and p-channel LTPS-TFTs with and without NII treatment. Further performance improvements of LTPS-TFTs are observed, including threshold voltage V_{TH}, subthreshold swing S.S. and field effect carrier mobility μ_{FE}. Figures 11 and 12 show the output characteristics (I_D-V_D) of n-channel and p-channel LTPS-TFTs with HfO_2 gate dielectric and NII treatment. For n-channel LTPS-TFT, a ~ 54.9 % driving current I_{Dsat} improvement is found, which the driving current I_{Dsat} is defined as the drain current at $V_G - V_{TH} = 3V$ and $V_D = 4V$. For p-channel LTPS-TFT, a ~ 16.7 % driving current I_{Dsat} improvement is found. The performance improvements of LTPS-TFTs after NII treatment are due to the defect passivation near the surface channel by nitrogen atoms. Figure 4-13 shows the secondary ion mass spectrometer (SIMS) of poly-Si channel film after NII treatment. It shows the nitrogen atoms would pile up near the surface of poly-Si channel film after SPC process. The effective interface-trap-state density (N_{it}) near the interface of HfO_2/poly-Si can be extracted from the subthreshold swing S.S. [4.24]:

$$N_{it} = [(\frac{S.S.}{\ln 10})(\frac{q}{KT}) - 1](\frac{C_{gate\_dielectric}}{q}) \quad (1)$$

In addition, the effective grain boundary trap state density (N_{trap}) with and without NII treatment are estimated by Levinson and Proano methods [4.15][4.16]. Figures 4-14 and 4-15 exhibit the plot of $\ln[I_D/(V_G - V_{FB})]$ versus $1/(V_G - V_{FB})^2$ curves at $V_D = 0.1$ V and high V_G, where the flat-band voltage (V_{FB}) is defined as the gate voltage that yields the minimum drain current from the transfer characteristic. The effective interface-trap-state density N_{it} and the effective grain boundary trap state density N_{trap} parameters are also listed in the Tables II and III. It is found that the effective interface-trap-state density N_{it} of n-channel LTPS-TFT is reduced from 8.09 x 10^{12} cm^{-2} to 6.59 x 10^{12} cm^{-2}, and the effective interface-trap-state density N_{it} of p-channel LTPS-TFT is reduced from 3.58 x 10^{12} cm^{-2} to 2.72 x 10^{12} cm^{-2}. In addition, the effective grain boundary trap state density N_{trap} of n-channel LTPS-TFT is reduced from 56.62 x 10^{12} cm^{-2} to 4.60 x 10^{12} cm^{-2} after 5 x 10^{14} cm^{-2} NII treatment and the effective grain boundary trap state density N_{trap} of p-channel LTPS-TFT is reduced from 5.20 x 10^{12} cm^{-2} to 4.44 x 10^{12} cm^{-2} after 5 x 10^{14} cm^{-2} NII treatment, resulting in the subthreshold swing S.S. improvement of n-channel LTPS-TFT from 0.248 V/dec. to 0.213 V/dec. and the field effect carrier mobility μ_{FE} enhancement from 27.56 cm^2/V-s to 37.80 cm^2/V-s, and also resulting in the subthreshold swing S.S. improvement of p-channel LTPS-TFT from 0.143 V/dec. to 0.123 V/dec. and the field effect carrier mobility μ_{FE} enhancement from 55.60 cm^2/V-s to 64.14 cm^2/V-s. Finally, a high performance CMOS LTPS-TFTs with threshold voltage V_{THn} ~ 1.05 V, V_{THp} ~ –0.8 V, subthreshold swing $S.S._n$ ~ 0.213 V/dec., $S.S._p$ ~ 0.123 V/dec., field effect carrier mobility μ_{nFE} ~ 37.80 cm^2/V-s and μ_{pFE} ~ 64.14 cm^2/V-s are derived. The combination of HfO_2 gate dielectric and NII treatment would be a promising technology for the application of high resolution display and SOP.

4.2.4 Summary

A high performance p-channel LTPS-TFT with HfO_2 gate dielectric and NII treatment is demonstrated for the application of AMLCD and SOP. The very low threshold voltage V_{THn} ~ 1.05 V, V_{THp} ~ –0.8 V, excellent subthreshold swing $S.S._n$ ~ 0.213 V/dec., $S.S._p$ ~ 0.123 V/dec. and high field effect carrier mobility μ_{nFE} ~ 37.80 cm^2/V-s, μ_{pFE} ~ 64.14 cm^2/V-s are obtained due to the high gate capacitance density provided by HfO_2 gate dielectric and the defect passivation by NII treatment.

Table 4-I. The important parameters of the HfO_2 LTPS-TFT without and with fluorine pre-implantation.

	V_{TH} (V)	**S.S. (V/dec.)**	**I_{min} (pA)**	**I_{on} (μA)**	**I_{on}/I_{min} (10^6)**	**N_{trap} (10^{12} cm^{-2})**	**ΔV_{TH} (V)**
w/o F-implant	**1.01**	**0.147**	**9.78**	**21.4**	**2.19**	**3.530**	**1.02**
with F-implant	**1.32**	**0.141**	**1.09**	**21.6**	**19.82**	**2.624**	**0.89**

Table 4-II. The important parameters of the n-channel LTPS-TFT with HfO_2 gate dielectric and NII treatment, which conventional LTPS-TFT with thick SiO_2 gate dielectric and other's work are included.

n-channel	**HfO_2**	**HfO_2 + NII $1x10^{14}$**	**HfO_2 + NII $5x10^{14}$**	**SiO_2**	**AlLaO3 [4.8]**
V_{TH} (V)	**1.13**	**1.11**	**1.05**	**6.8**	**1.2**
S.S. (V/dec.)	**0.248**	**0.226**	**0.213**	**1.41**	**0.31**
EOT (nm)	**8.4**	**8.4**	**8.4**	**49.3**	**8.7**
G_m (μS)	**11.3**	**12.6**	**15.5**	**1.08**	**--**
μ_{FE} (cm^2/V-s)	**27.56**	**30.73**	**37.80**	**15.43**	**40**
D_{it} (10^{12} cm^{-2})	**8.09**	**7.15**	**6.59**	**--**	**--**
Q_{trap} (10^{12} cm^{-2})	**6.62**	**5.21**	**4.60**	**--**	**--**
I_{off} (pA)	**19.2**	**51.2**	**185.3**	**--**	**--**
I_{Dsat} (μA/μm)	**2.75**	**3.34**	**4.26**	**--**	**--**

Table 4-III. The important parameters of the p-channel LTPS-TFT with HfO_2 gate dielectric and NII treatment, which conventional LTPS-TFT with thick SiO_2 gate dielectric and other's work are included.

p-channel	**V_{TH} (V)**	**S.S. (V/dec.)**	**EOT (nm)**	**μ_{FE} (cm^2/V-s)**	**N_{it} (cm^{-2})**	**N_{trap} (cm^{-2})**	**I_{Dsat} (μA/μm)**
$HfSiO_x$ [4.9]	**-0.91**	**0.37**	**25.5**	**27.45**	**--**	**--**	**--**
SiO_2	**-13.3**	**1.60**	**49.3**	**11.71**	**--**	**--**	**--**
HfO_2	**-0.93**	**0.143**	**8.4**	**55.60**	**$3.58x10^{12}$**	**$5.20x10^{12}$**	**7.83**
HfO_2 + NII $1x10^{14}$	**-0.86**	**0.132**	**8.4**	**59.26**	**$3.11x10^{12}$**	**$4.78x10^{12}$**	**8.42**
HfO_2 + NII $5x10^{14}$	**-0.80**	**0.123**	**8.4**	**64.14**	**$2.72x10^{12}$**	**$4.44x10^{12}$**	**9.14**

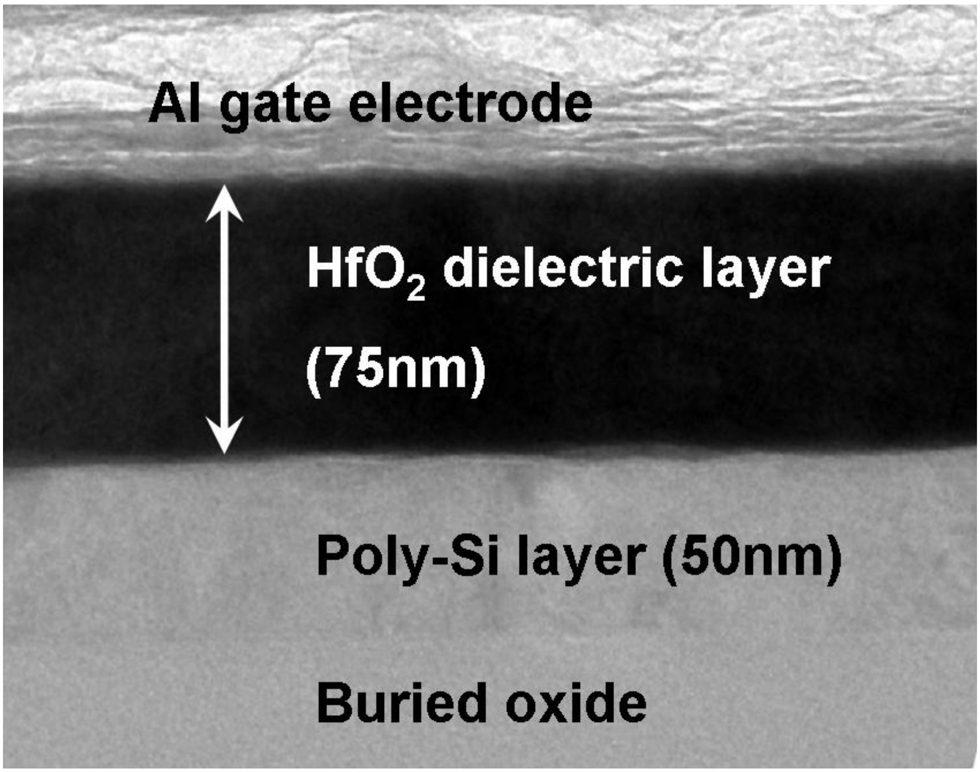


Fig. 4-1. The cross-sectional transmission electron microscopy (TEM) micrograph of the HfO_2 gate dielectric TFT structure.

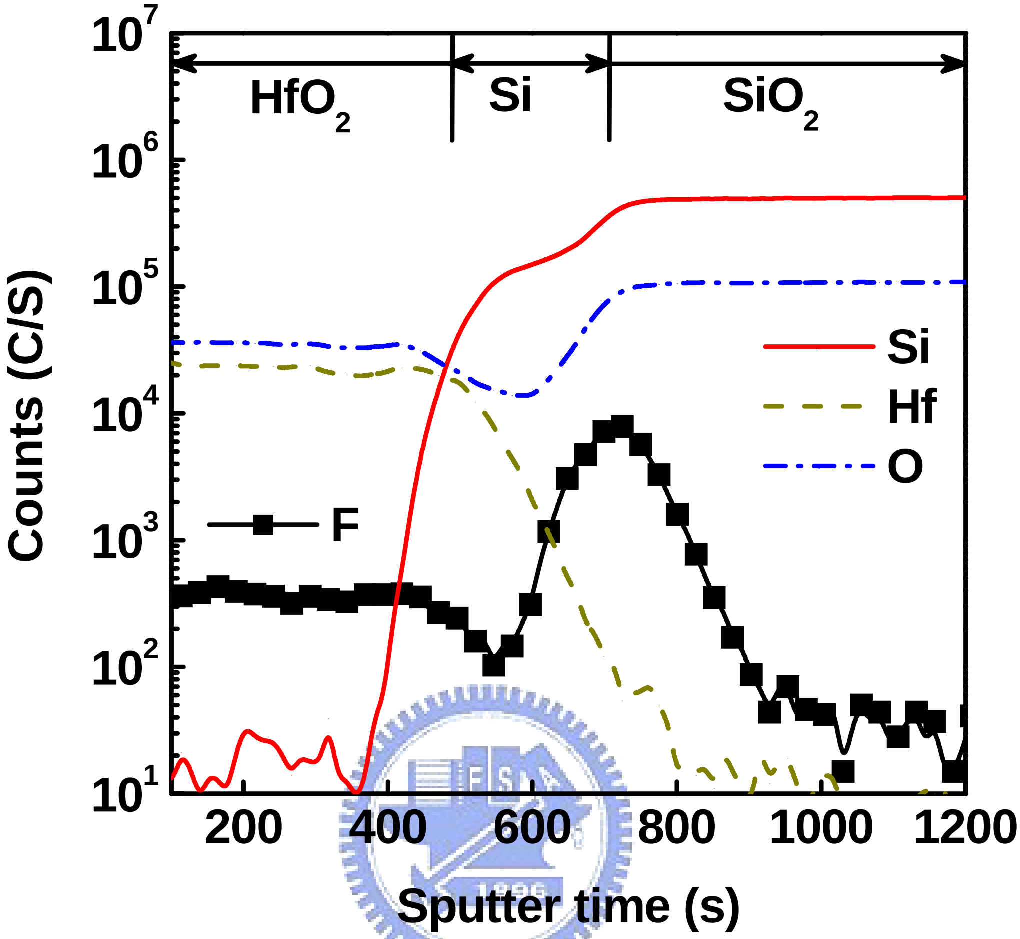


Fig. 4-2. The SIMS analysis of the HfO_2 LTPS-TFT with fluorine pre-implantation.

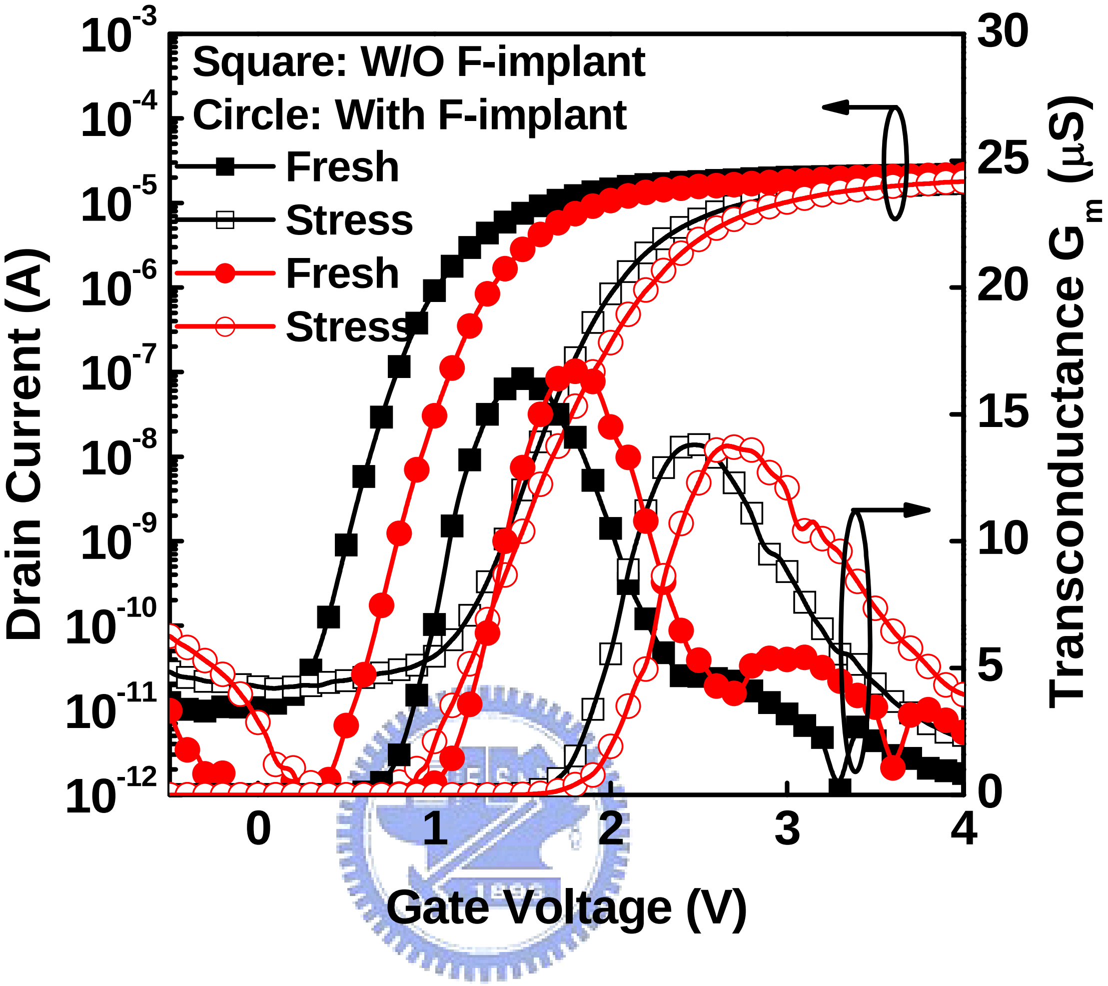


Fig. 4-3. Transfer characteristics (I_D-V_G and G_m) of the HfO_2 LTPS-TFT at V_D = 0.1 V without and with fluorine pre-implantation before and after hot carrier stress $V_G - V_{TH} = V_D$ = 5V for 1000 seconds.

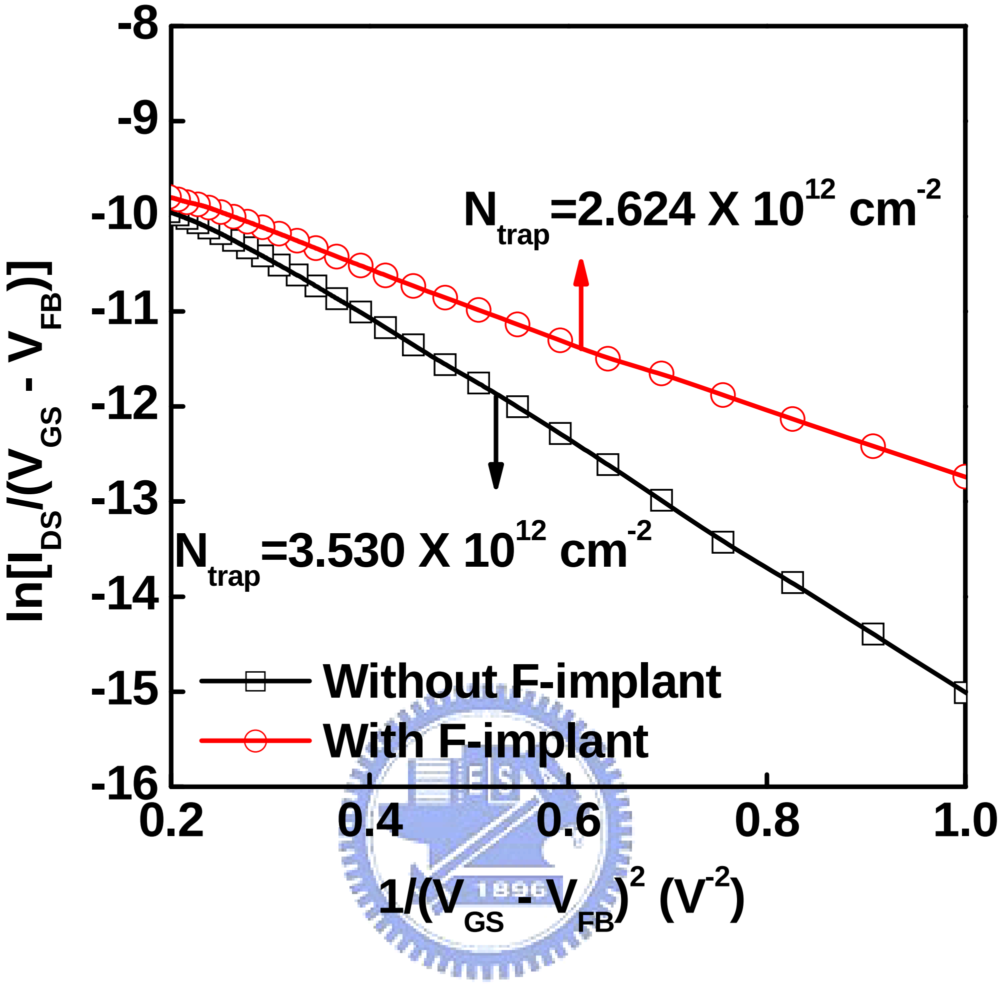


Fig. 4-4. The plots of ln [I_{DS}/(V_{GS} - V_{FB})] versus 1/(V_{GS} - V_{FB})^2 curves at V_{DS} = 1 V and high V_{GS}.

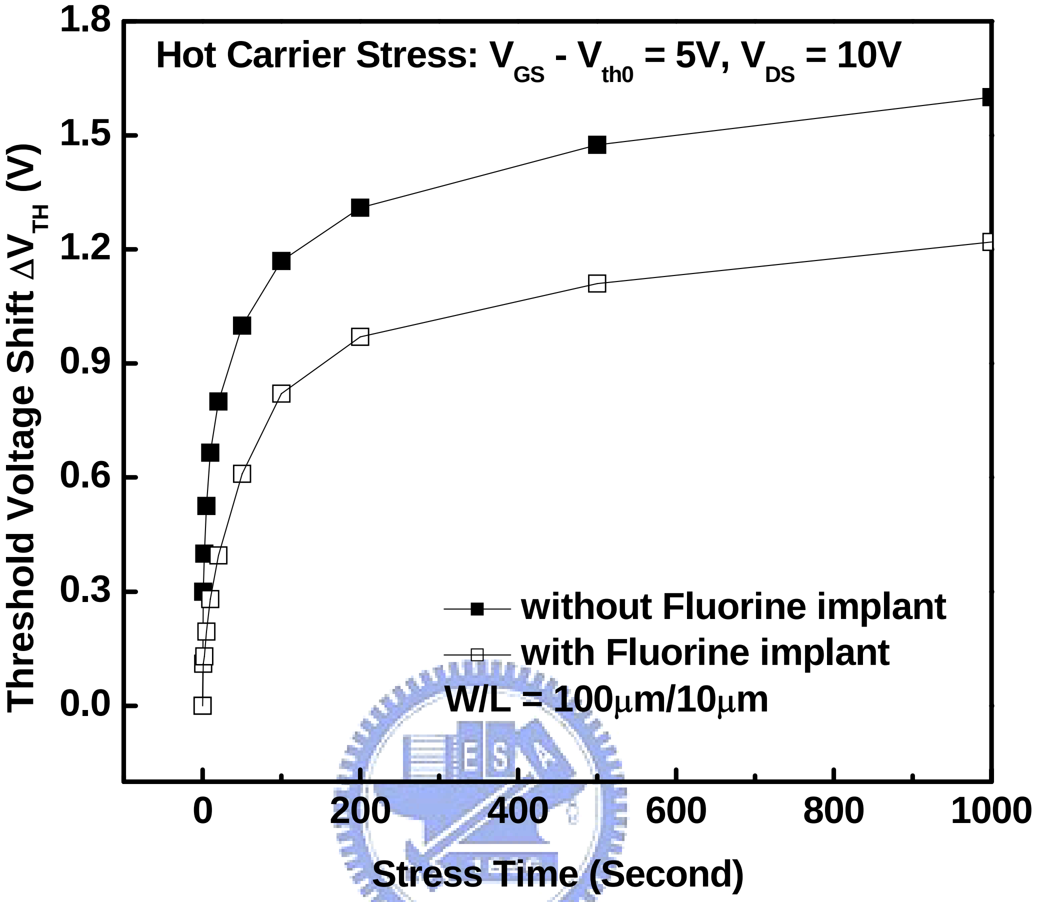


Fig. 4-5. The threshold voltage shift ΔV_T of TaN/HfO_2 LTPS-TFTs with and without fluorine implantation after 1000-s hot carrier stress $V_G - V_{TH}$ = 5V, V_D = 10V.

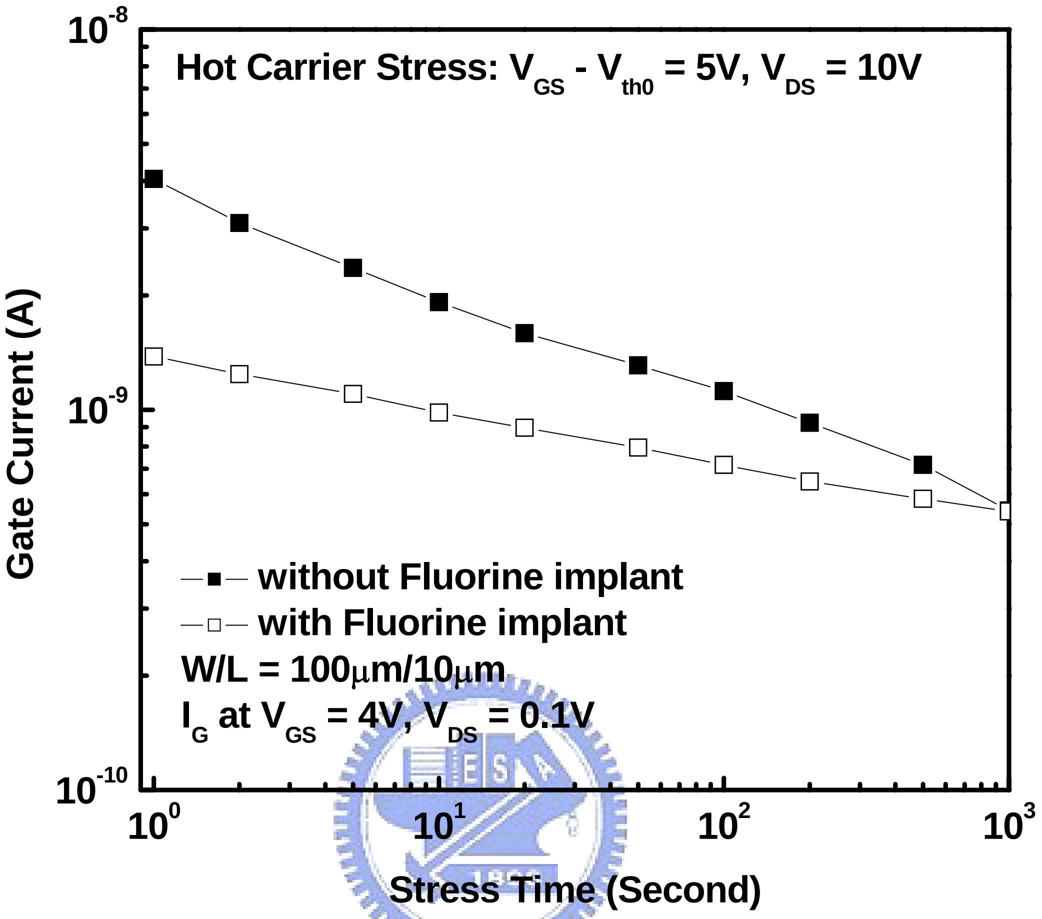


Fig. 4-6. The gate leakage current of TaN/HfO_2 LTPS-TFTs with and without fluorine implantation during the hot carrier stress $V_G - V_{TH}$ = 5V, V_D = 10V.

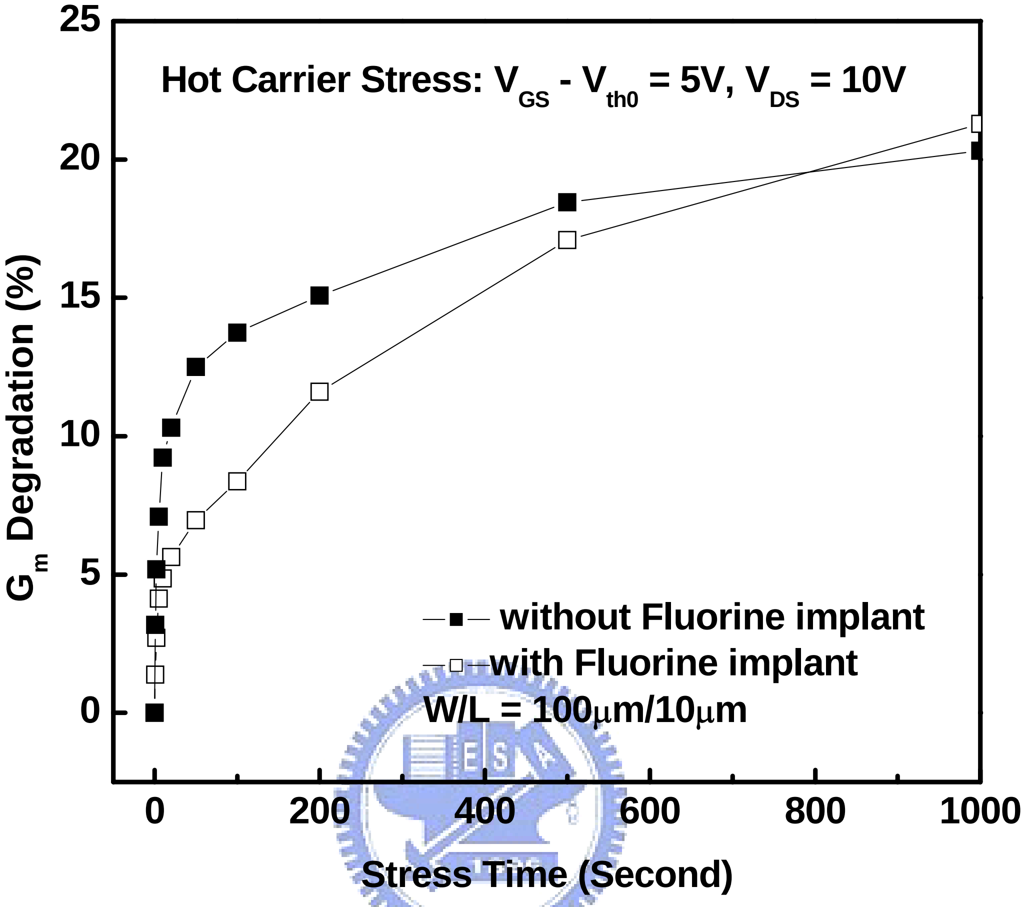


Fig. 4-7. The transconductance G_m degradation of TaN/HfO_2 LTPS-TFTs with and without fluorine implantation during 1000-s hot carrier stress $V_G - V_{TH} = 5V$, $V_D = 10V$.

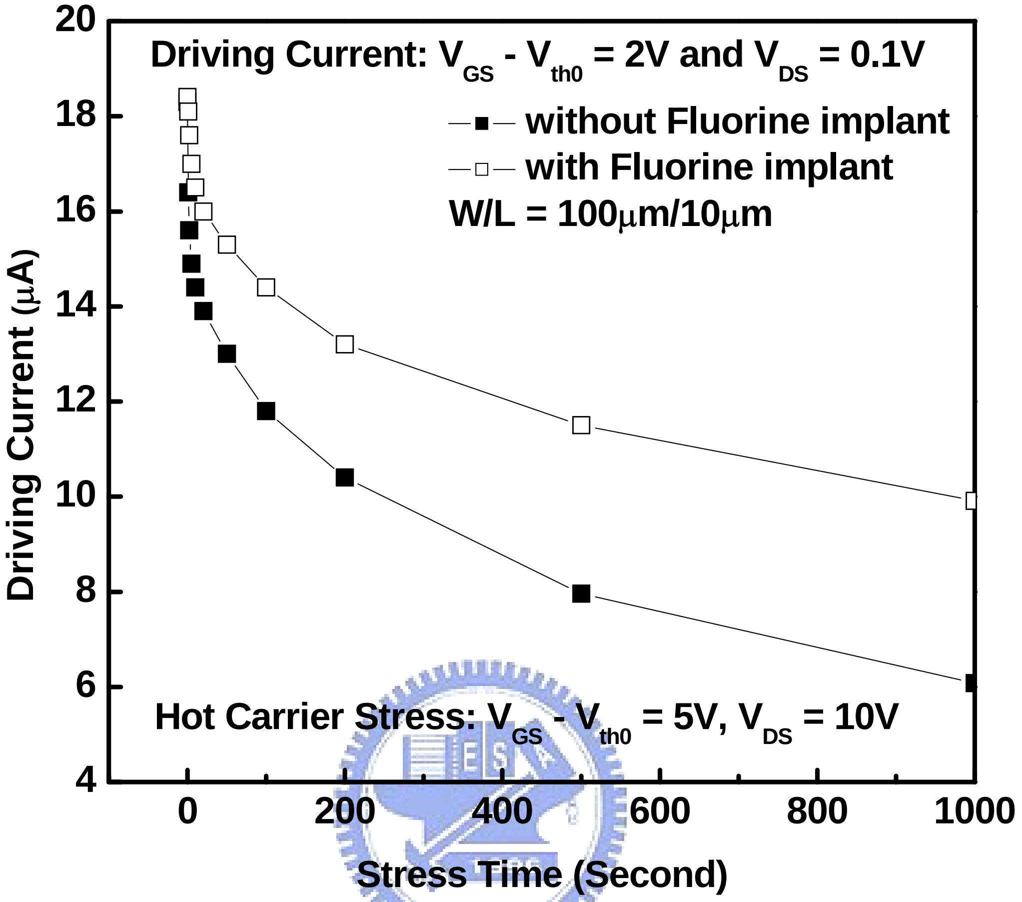


Fig. 4-8. The driving current of TaN/HfO_2 LTPS-TFTs with and without fluorine implantation during 1000-s hot carrier stress $V_G - V_{TH}$ = 5V, V_D = 10V.

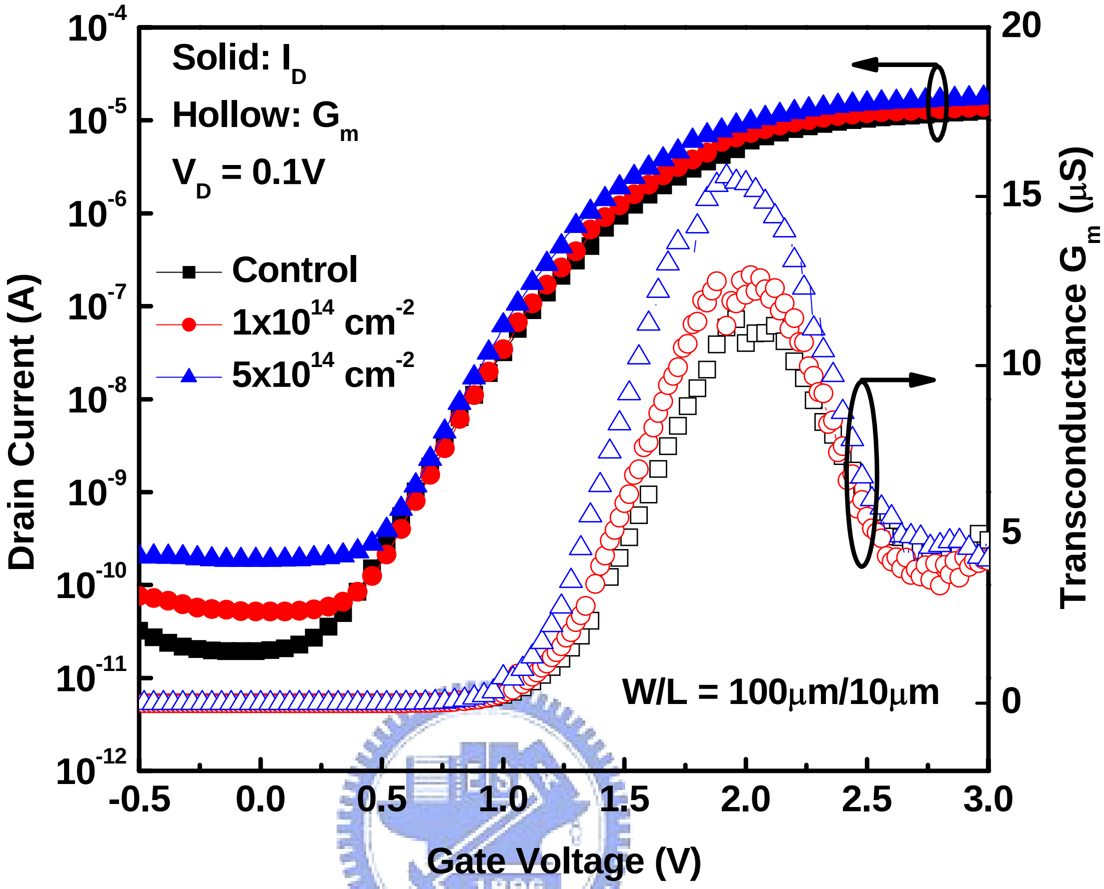


Fig. 4-9. The transfer characteristics (I_D-V_G and G_m) of n-channel LTPS-TFT with HfO_2 gate dielectric and NII treatment.

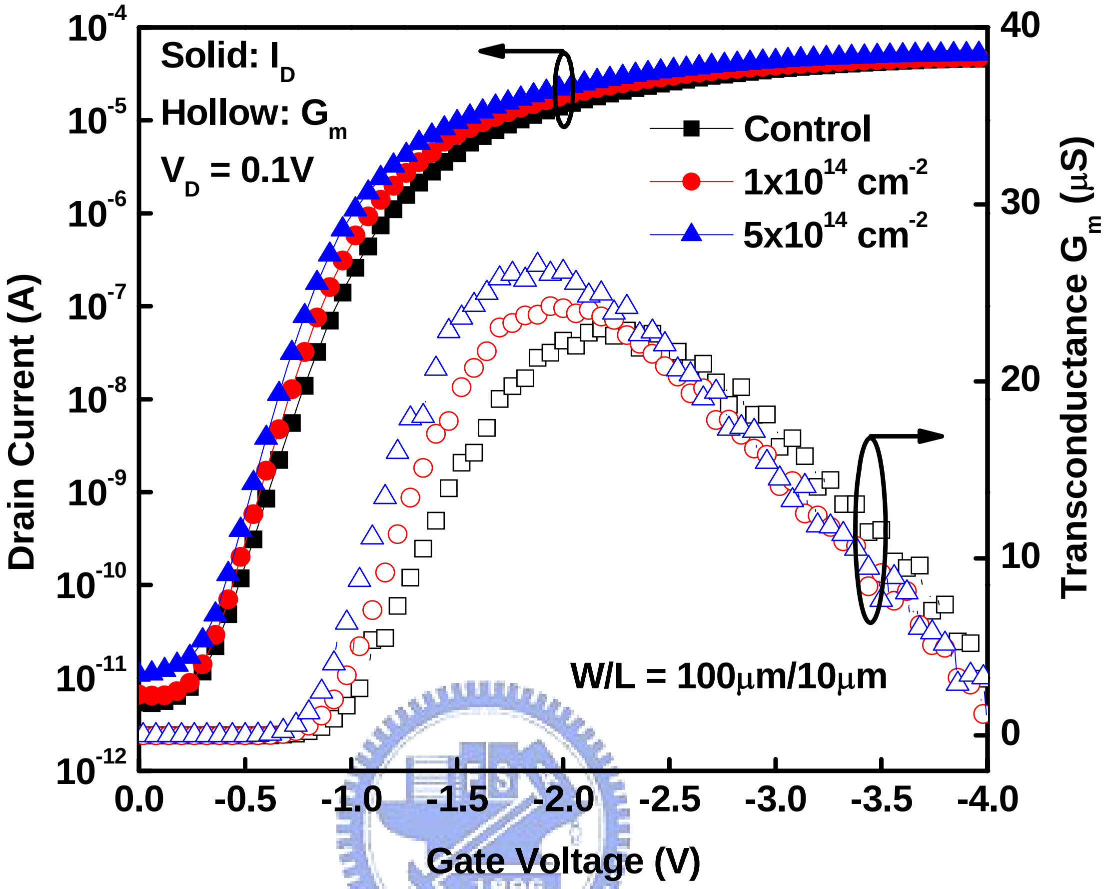


Fig. 4-10. The transfer characteristics (I_D-V_G and G_m) of p-channel LTPS-TFT with HfO_2 gate dielectric and NII treatment.

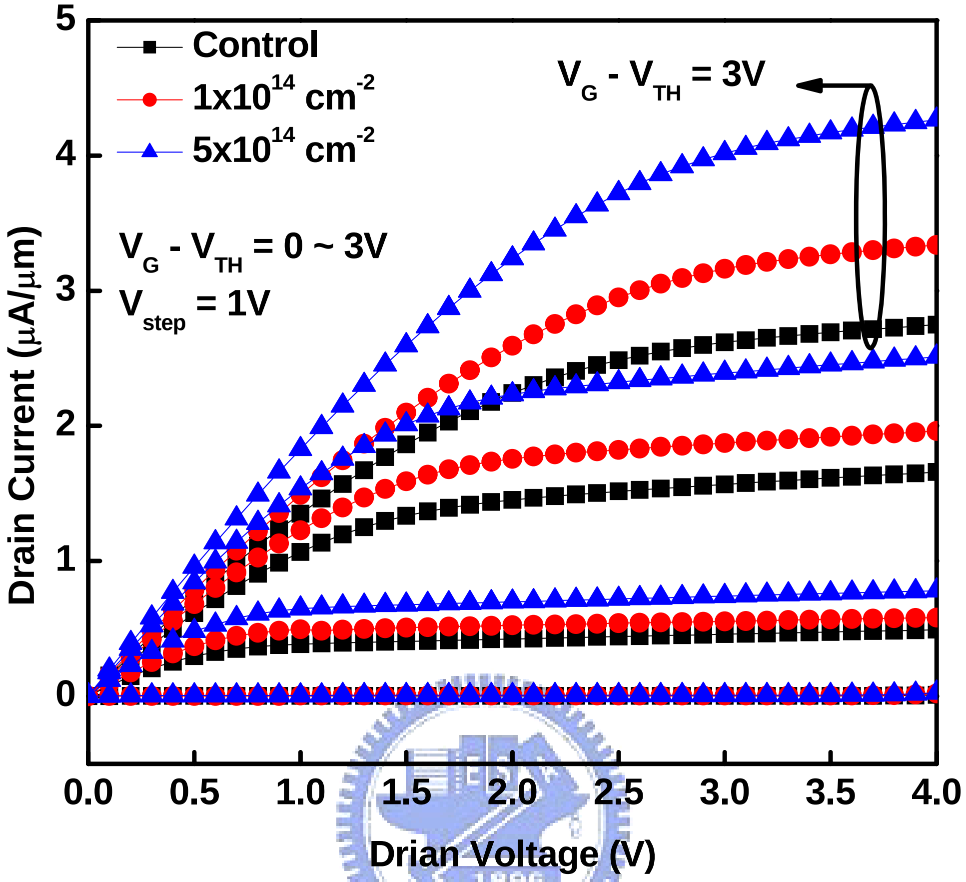


Fig. 4-11. The output characteristics (I_D-V_D) of n-channel LTPS-TFT with HfO_2 gate dielectric and NII treatment.

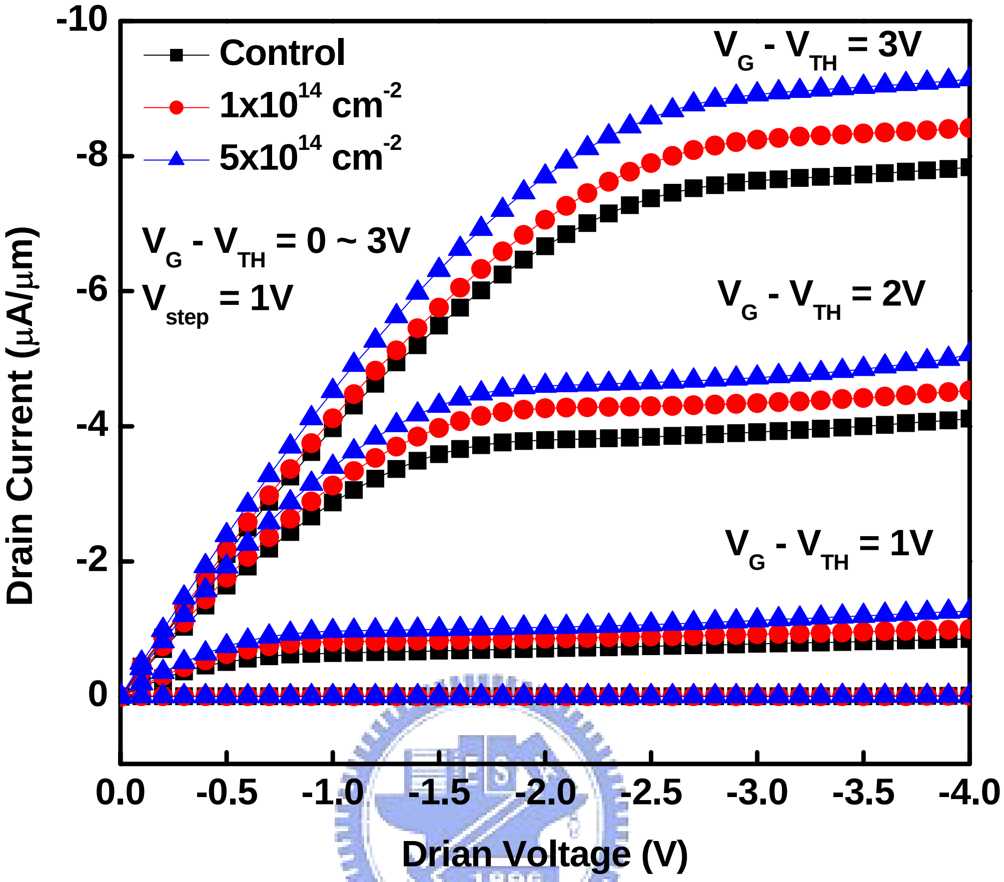


Fig. 4-12. The output characteristics (I_D-V_D) of p-channel LTPS-TFT with HfO_2 gate dielectric and NII treatment.

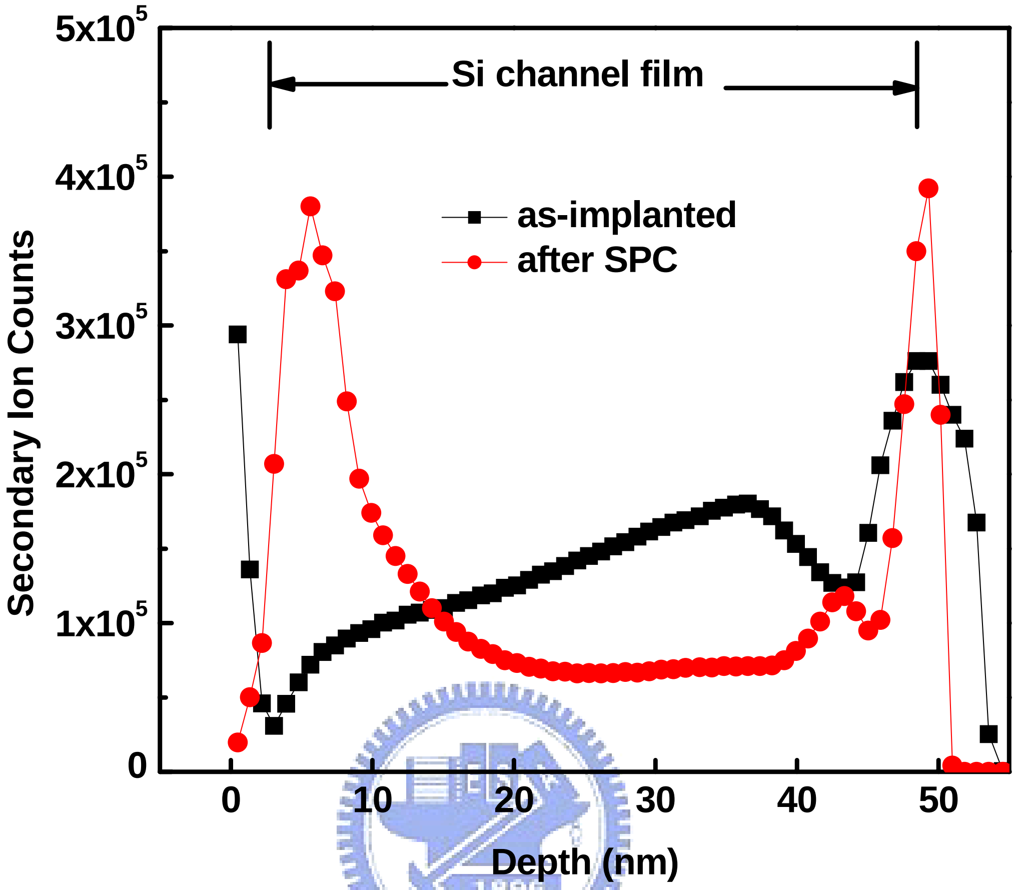


Fig. 4-13. The secondary ion mass spectrometer (SIMS) of poly-Si channel film after NII treatment.

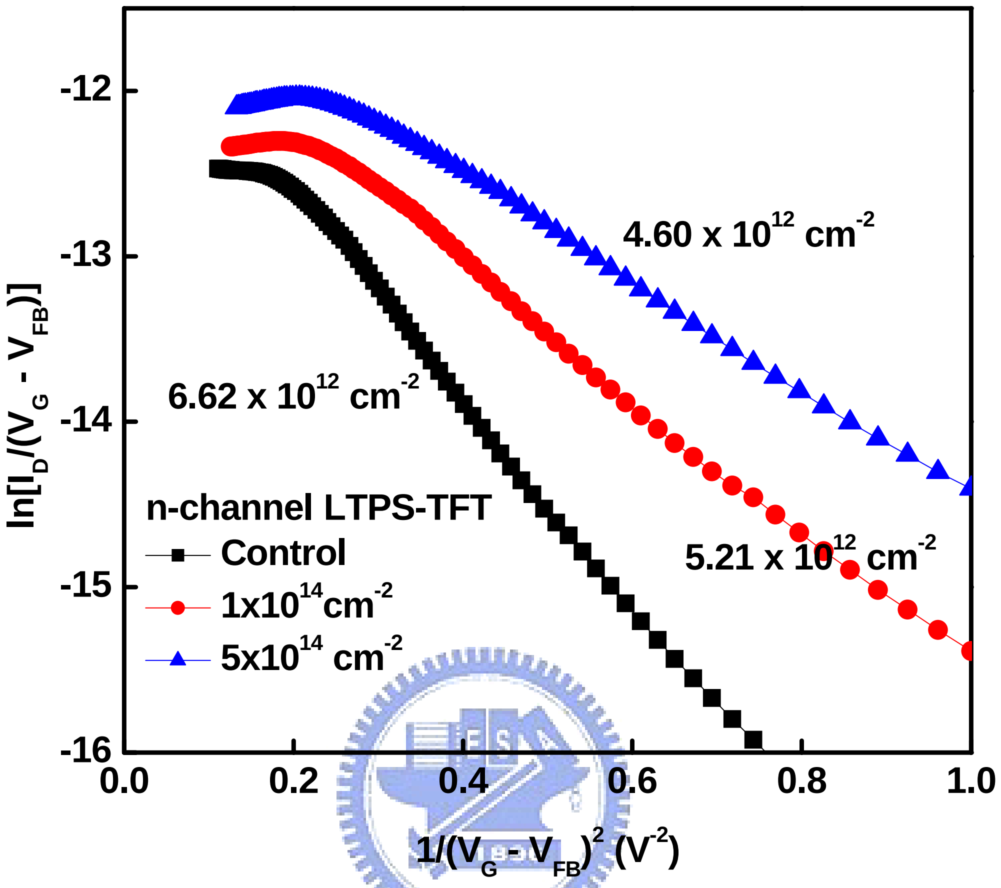


Fig. 4-14. The plot of ln[I_D/(V_G – V_{FB})] versus 1/(V_G – V_{FB})^2 curves at V_D = 0.1 V and high V_G of n-channel LTPS-TFT.

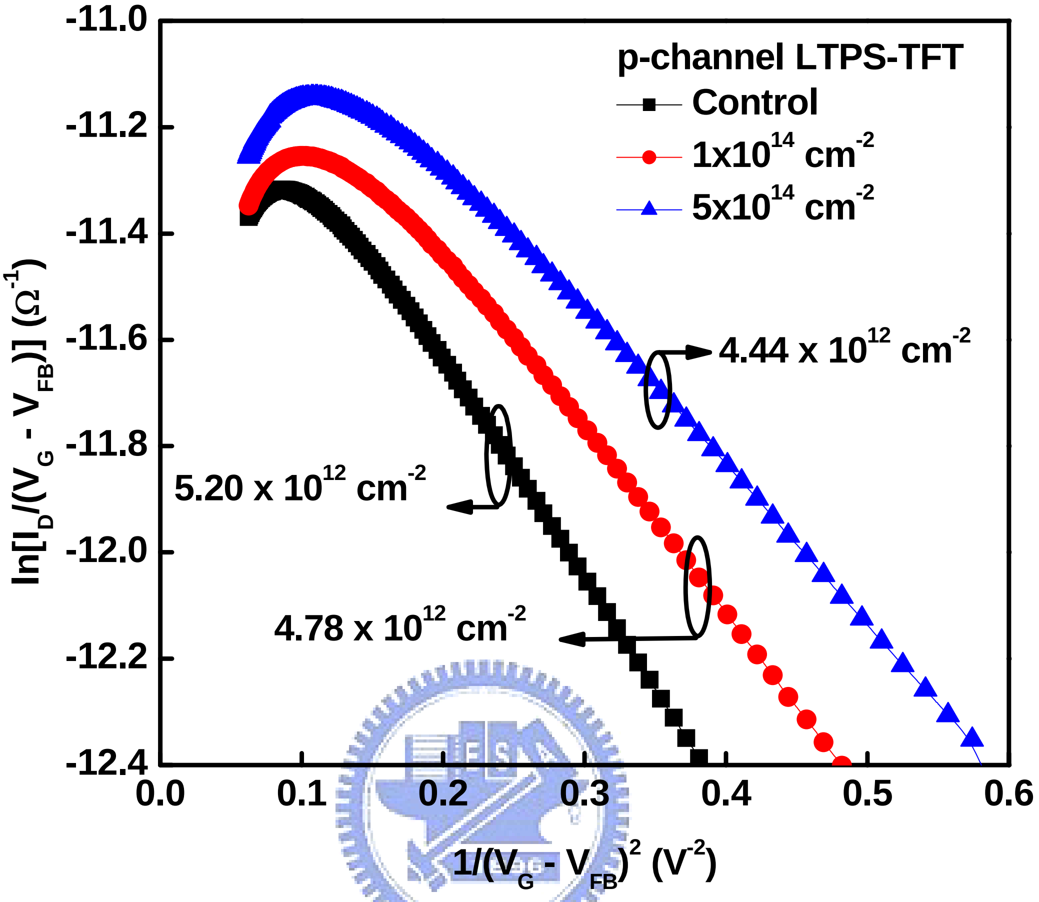


Fig. 4-15. The plot of $\ln[I_D/(V_G - V_{FB})]$ versus $1/(V_G - V_{FB})^2$ curves at $V_D = 0.1$ V and high V_G of p-channel LTPS-TFT.

Chapter 5

High Performance Metal-Induced Lateral Crystallized Polycrystalline Silicon P-Channel Thin-Film Transistor with TaN/HfO_2 Gate Stack Structure

5.1 Introduction

As described in previous Chapter, high performance low temperature poly-Si thin-film transistors (LTPS-TFTs) have been intensively investigated for the application of the active matrix liquid phase crystal displays [5.1] and the three-dimension (3-D) circuit integration elements such as SRAM's and DRAM's [5.2][5.3]. However, the poly-Si channel film would still have many grain boundaries which degrade the subthreshold swing S.S., threshold voltage V_{TH}, and field effect mobility μ_{FE} and results in a large operation voltage [5.4]-[5.6]. Hydrogen-related plasma is generally used to passivate these grain boundaries in the poly-Si channel film to have a lower operation voltage of LTPS-TFTs [5.7]-[5.9]. Nevertheless, the introduction of hydrogen would also result in the degradation of the reliability of LTPS-TFTs [5.10][5.11]. In addition, high-κ materials such as $HfSiO_x$, HfO_2, $LaAlO_3$ and Al_2O_3 have been used as the gate dielectric of LTPS-TFTs to enhance the gate capacitance density, resulting in the improvement of the subthreshold swing S.S. and threshold voltage V_{TH} without any hydrogen-related plasma treatments [5.12]-[5.15].

Improvement of the subthreshold swing S.S., threshold voltage V_{TH}, and field effect mobility μ_{FE} of devices with high-κ gate dielectrics is still not high enough for the application of system-on-panel (SOP) or 3-D circuit integration. Compared with solid-phase-crystallization (SPC) method, excimer laser crystallization (ELC) method is capable of producing poly-Si film with low defect densities and higher field effect mobility μ_{FE} [5.16]. However, ELC suffers from high initial cost and high process complexity. Metal-induced lateral crystallization (MILC) method is another batch process with low cost to achieve high field effect mobility μ_{FE} of LTPS-TFTs due to its large grain size and longitudinal grain boundaries [5.17]-[5.21].

In this Chapter, we demonstrate the p-channel LTPS-TFT with TaN gate, HfO_2 gate dielectric, and MILC poly-Si channel film. High-performance LTPS-TFTs of very low threshold voltage V_{TH}, excellent subthreshold swing S.S., and very high field effect mobility μ_{FE} can be obtained, which is very promising for the realization of SOP and 3-D circuit integration.

5.2 Fabrication Process

The fabrication of devices started by depositing a 50-nm undoped amorphous Si (α-Si) layer at 550°C in a low-pressure chemical vapor deposition system on Si wafers capped with a 500-nm thermal oxide layer. A 5-nm Ni was deposited by electron-beam evaporation system at room temperature and patterned by lift-off process as a seed layer to crystallize the α-Si as shown in Fig. 5-1(a). Seok-Woon Lee *et al* and Man Wong *et al* have shown that a very thin thickness of Ni within 5 nm is enough for MILC process [5.17]-[5.21]. Then the 50-nm α-Si layer was recrystallized by metal induced lateral crystallization process at 550°C for 24-h in a N_2 ambient as shown in Fig. 5-1(b). After the residual Ni was removed by $H_2SO_4 + H_2O_2$, a 500-nm plasma-enhanced chemical vapor deposition oxide was deposited at 300°C for device isolation. The device active region was formed by patterning and etching the isolation oxide. The source and drain (S/D) regions in the active device region were implanted with boron (10 keV at 5×10^{15} cm^{-2}) and activated at 600°C for 24-h annealing in a N_2 ambient as shown in Fig. 5-1(c). A 25-nm HfO_2 was deposited by electron-beam evaporation system at room temperature. Then 200-nm TaN gate electrode was deposited by sputter at room temperature and patterned by reactive ion etching. After the patterning of source/drain contact holes, Al was deposited by thermal evaporation system as the gate and source/drain contact pad. Finally, the TFT devices were completed by the contact pad definition. The cross-section view of the TaN/HfO_2 gate stack structure LTPS-TFT with MILC channel film was shown in Fig. 5-1(d).

Device with gate length (L) and width (W) of 2-μm and 1-μm were measured. The V_{TH} was defined as the V_G at which the drain current reaches 100 nA x W/L and V_{DS} = 0.1 V. The μ_{FE} was extracted from the maximum transconductance (G_m).

5.3 Discussion

Figure 5-2 shows the transfer characteristics (I_D-V_G and transconductance G_m) of LTPS-TFT with TaN/HfO_2 gate stack structure and MILC poly-Si channel film. A very low threshold voltage V_{TH} ~ 0.095V and ultra sharp subthreshold current curve is observed which indicates an excellent subthreshold swing S.S. ~ 83 mV/dec. that can be comparable with single crystalline silicon channel. A very high gate capacitance density which corresponds to a very low effective oxide thickness EOT ~ 5.12-nm is obtained from the capacitance-voltage curve of TaN/HfO_2 on P-type single crystalline silicon substrate to extract the gate capacitance density of TaN/HfO_2 LTPS-TFT as shown in inset of Fig. 5-2. Therefore, the high field effect mobility μ_{FE} ~ 240 cm^2/V-s can be calculated from the maximum transconductance G_m. The high performance electrical characteristics of LTPS-TFT is attributed to both the low defect density of poly-Si channel film crystallized by MILC and high gate capacitance density provided by high-κ gate dielectric HfO_2. Some important electrical parameters of LTPS-TFT are listed in Table 5-I and compared with others' works. Compared with conventional SPC-TFT with thick SiO_2 gate dielectric, we can observe that the conventional

MILC-TFT with thick SiO_2 gate dielectric shows a significant improvement on field effect mobility μ_{FE} as shown in Table 5-I. It is due to that MILC channel film has low defect density in poly-Si [5.21]. However, the subthreshold swing S.S. of conventional MILC-TFT is still too high to reduce operation voltage of LTPS-TFT [5.17]-[5.21]. Replacement of thick SiO_2 gate dielectrics by high-κ gate dielectrics can provide a large gate capacitance density to attract more carriers with a smaller gate voltage to fill up the traps and lower the potential barrier height in the poly-Si channel film [5.22]. This makes the LTPS-TFTs turn on within several voltages, resulting in the reduction of the subthreshold swing S.S. and the operation voltage. As shown in Table 5-I, the threshold voltage V_{TH} and subthreshold swing S.S. can be obviously reduced without any hydrogen-related plasma treatments as high-κ gate dielectrics are used. In addition, the mobility of TaN/HfO_2 MILC-TFT is much larger than conventional MILC-TFT. It can be attributed to small device's length and width that less grain boundaries exist in the channel film.

However, the drain leakage current of LTPS-TFT with TaN/HfO_2 gate stack structure and MILC poly-Si channel film is higher than conventional MILC and SPC LTPS-TFT, resulting in a degradation of the I_{on}/I_{min} current ratio. The high drain leakage current is attributed to the poor grain boundaries of SPC/MILC interface in S/D junction region. Because the longitudinal grain boundaries of MILC channel film would be not continuous in the S/D junction region which is activated by SPC. The SPC poly-Si has a columnar grain structure with grain boundaries randomly oriented with respect to the longitudinal grain boundaries of MILC channel film, resulting in poor grain boundaries of the S/D and channel interface. The process flow of S/D ion-implantation before MILC process may improve this drawback. However, the S/D ion-implantation will affect the MILC length. The modified process of metal-gate/high-κ MILC TFT is under studying.

Figure 5-3 shows the output characteristic I_D-V_D of MILC LTPS-TFT with TaN/HfO_2 gate stack structure, and indicates a very high driving current within -2 V of gate and drain voltages. The high driving current would be very suitable for the application of SOP and 3-D circuit integration.

5.4 Summary

The combination of high-κ gate dielectric and MILC poly-Si channel film has been proposed for the first time. The p-channel LTPS-TFT with TaN/HfO_2 gate stack structure and MILC polycrystalline channel film can achieve high field effect mobility μ_{FE} ~ 240 cm^2/V-s, low threshold voltage V_{TH} ~ 0.095V and excellent subthreshold swing S.S. ~ 83 mV/decade. simultaneously. The combination of TaN/HfO_2 gate stack structure and MILC poly-Si channel would be very promising for the application of system-on-panel.

Table 5-I. The important parameters of the TaN/HfO_2 gate stack structure LTPS-TFT with MILC channel film. Others' works are also listed for compare.

	MILC P-TFT with HfO_2	**MILC P-TFT with SiO_2 [5.19]**	**SPC P-TFT with $HfSiO_x$ [5.12]**	**SPC P-TFT with SiO_2 [5.12]**
W/L (μm/μm)	**1/2**	**10/5**	**5/10**	**5/10**
V_{TH} (V)	**0.095**	**-4.2**	**-0.91**	**-6.85**
S.S. (V/decade)	**0.083**	**1.0**	**0.37**	**1.06**
EOT (nm)	**5.12**	**100**	**25.5**	**46.5**
μ_{FE} (cm^2/V-s)	**240**	**98**	**27.45**	**15.82**
I_{on}/I_{min}	**4.09×10^5**	**3.4×10^7**	**4.12×10^6**	**3.56×10^6**

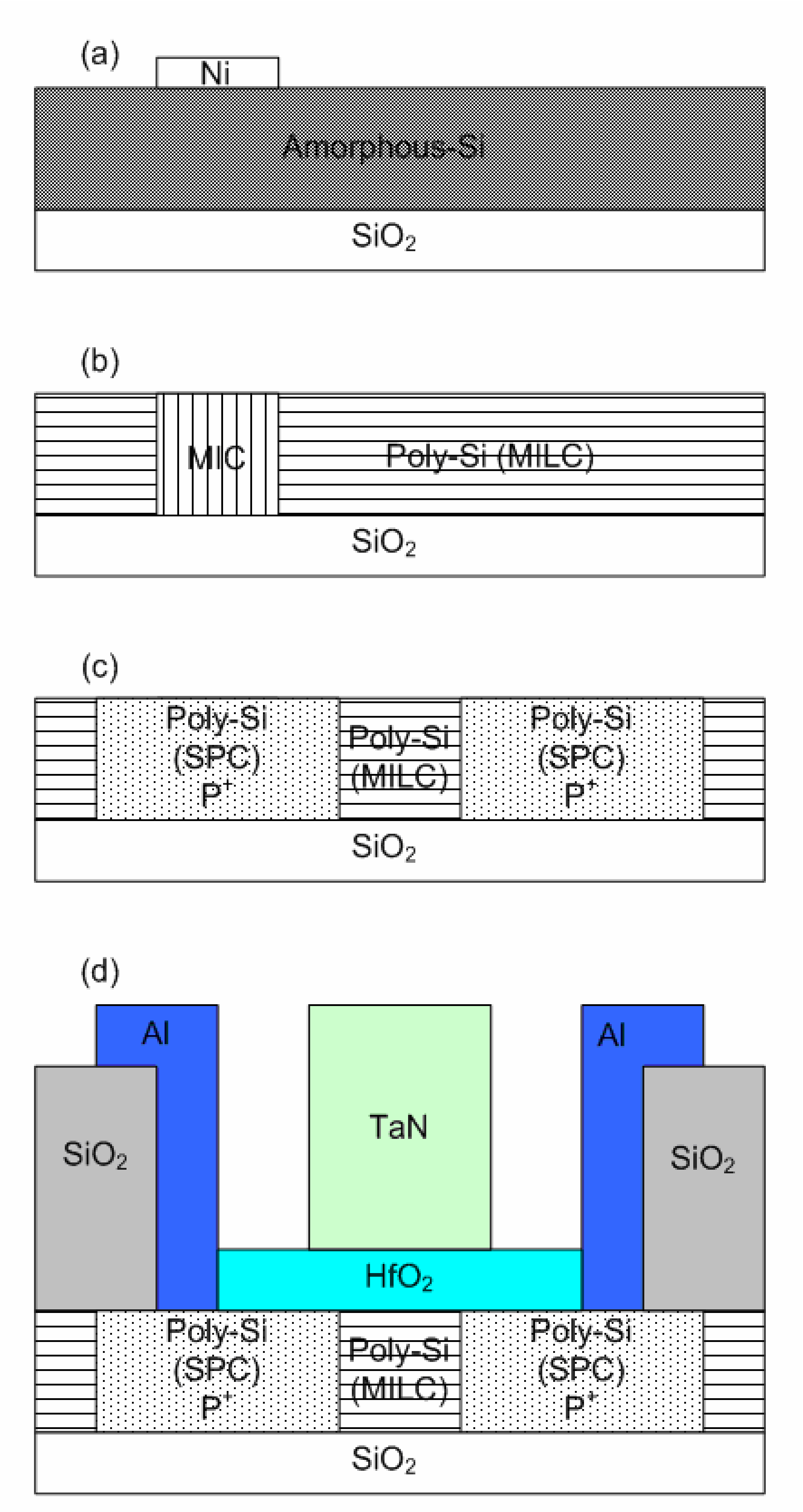


Fig. 5-1. The cross-section view and process flow of the TaN/HfO_2 gate stack structure LTPS-TFT with MILC channel film.

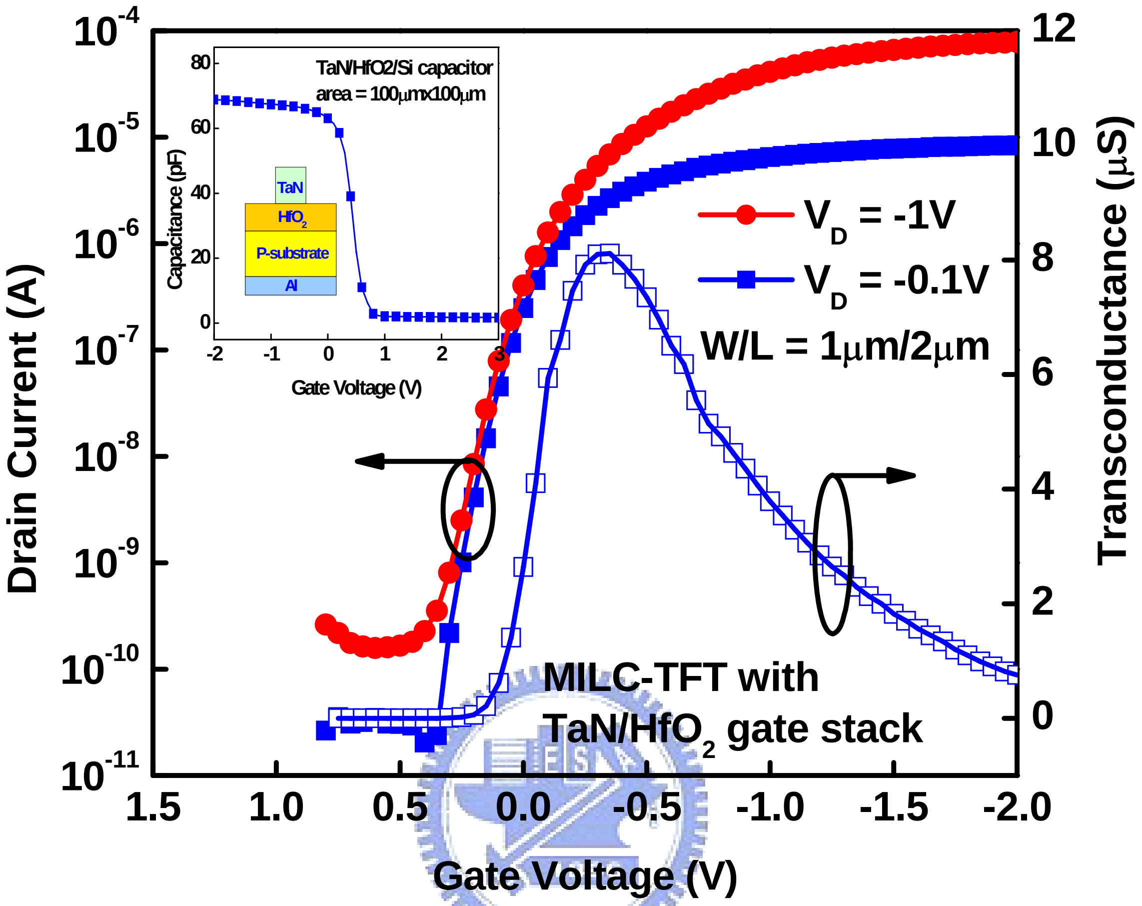


Fig. 5-2. The transfer characteristics (I_D-V_G and transconductance G_m) of LTPS-TFT with TaN/HfO_2 gate stack structure and MILC polycrystalline silicon channel film. The inserted figure is the C-V curve of TaN/HfO_2 capacitor.

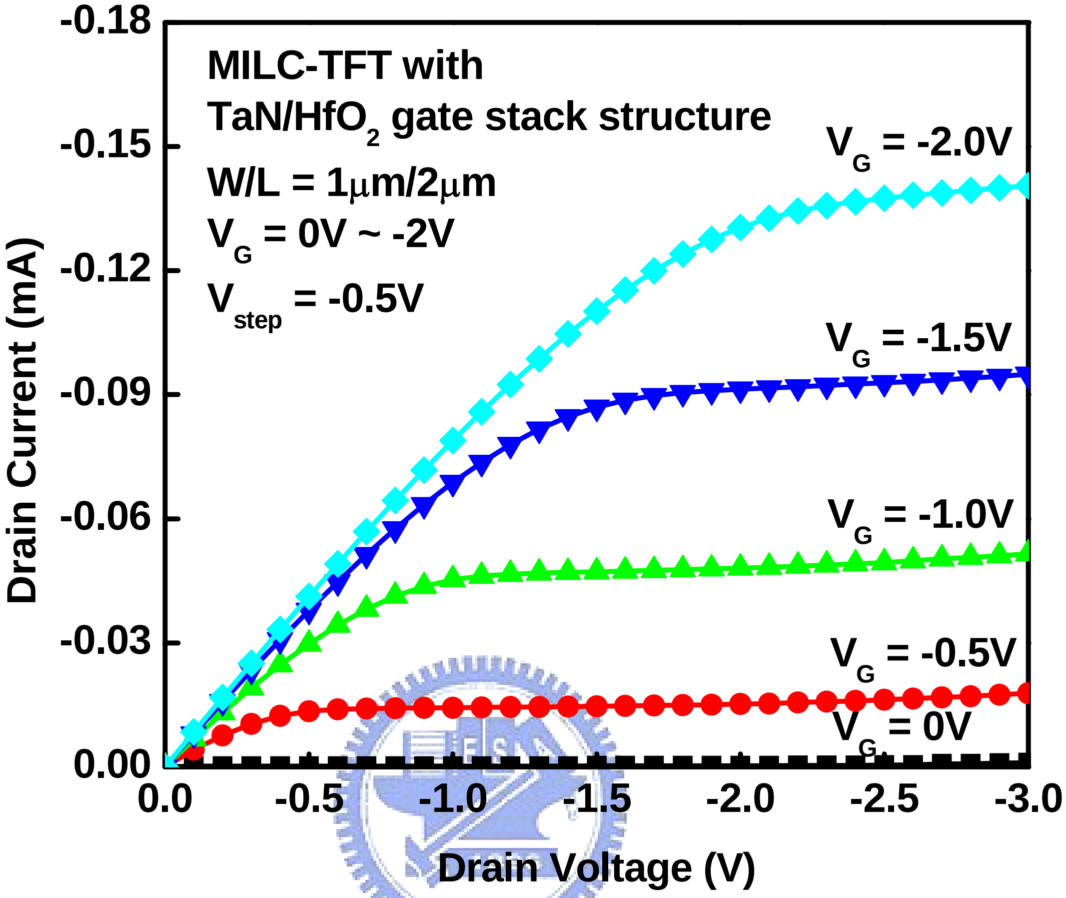


Fig. 5-3. The output characteristic I_D-V_D of MILC LTPS-TFT with TaN/HfO_2 gate stack structure.

Chapter 6

Conclusions and Recommendations for Future Research

6.1 Conclusions

In conclusion, this dissertation involves the effects of HfO_2 high-κ dielectric as gate insulator of low-temperature polycrystalline-silicon thin-film transistor (LTPS-TFT), including the performance enhancement and the reliability mechanisms. In addition to the demonstration of LTPS-TFT with the employment of HfO_2 gate dielectric, the characteristics of the native growth interfacial layer are also comprehensively analyzed. Many plasma surface treatments are used to study the interface properties of the HfO_2/poly-Si. Moreover, fluorine and nitrogen ion implantation are also utilized to passivate the defects of polycrystalline-silicon channel film to improve the performance and reliability of HfO_2 LTPS-TFT. Finally, TaN metal gate and HfO_2 gate dielectric are demonstrated on the metal-induced lateral crystallization (MILC) LTPS-TFT.

First, CMOS LTPS-TFTs with HfO_2 gate dielectric are fabricated and analyzed simultaneously. The effects of HfO_2/poly-Si interfacial layer on the electrical characteristics of CMOS LTPS-TFTs are also specified. In addition, the impacts of oxygen plasma surface treatment on CMOS LTPS-TFTs with HfO_2 gate dielectric are investigated. Not only the change of interfacial layer characteristics, but also the defects passivation of poly-Si channel film is observed. In conclusion, oxygen plasma surface treatment can improve the driving current of CMOS LTPS-TFTs with HfO_2 gate dielectric. In order to further enhance the performance of LTPS with high-κ gate dielectric, another two kinds of plasma, N_2 and NH_3, are also employed. Subthreshold swing S.S., field effect mobility μ_{FE} and driving saturation current are all significantly improved after N_2 and NH_3 plasma surface treatment.

Second, a comprehensive investigation of the reliability mechanisms of high performance LTPS-TFT with HfO_2 gate dielectric is demonstrated. Various stress conditions, including PBS, PBTI, NBS, NBTI and hot carrier stress, are performing to differentiate the degradation mechanisms. For PBS and PBTI, it is found that serious subthreshold swing S.S. degradation is due to the deep trap states of the effective interfacial layer; transconductance G_m decrease with the drain leakage current I_{min} increase is due to the tail trap states of poly-Si grain boundaries, and gate leakage current reduction is due to electrons trapping of the HfO_2 gate dielectric. For NBS and NBTI, significant subthreshold swing S.S. and transconductance G_m degradation without the drain leakage current I_{min} increase are observed to show that the effective interfacial layer is the main damage region that both deep and tail trap states are generated after NBS and NBTI. Remarkable drain leakage current I_{min} increase of PBTI and almost invariant drain leakage current I_{min} degradation of NBTI show that PBTI and NBTI are attributing to different mechanisms. The carrier collision and injection model is employed to explain the mechanism of PBS and PBTI, and the hydrogen diffusion model is employed to explain the mechanism of NBS and NBTI. In addition, the drain bias applying during stress is also studied, and the results show that the impact ionization will dominate the degradation mechanism if a large drain bias stress is used.

Third, high-performance LTPS-TFTs with HfO_2 gate dielectric and fluorine pre-implantation, nitrogen post-implantation are demonstrated. Low temperature SPC activation of fluorine and nitrogen ions is proposed and it also provides an improved electrical characteristics and reliability.

Finally, the combination of high-κ gate dielectric and MILC poly-Si channel film is proposed. The p-channel LTPS-TFT with TaN/HfO_2 gate stack structure and MILC polycrystalline channel film can achieve high μ_{FE} ~ 240 cm^2/V-s, low V_{TH} ~ 0.095V and excellent S.S. ~ 83 mV/dec. simultaneously. The combination of TaN/HfO_2 gate stack structure and MILC poly-Si channel would be very promising for the application of system-on-panel.

6.2 Recommendations for Future Research

There are some topics that are suggested for future works. The technology combination of defects passivation methods and high-κ gate dielectric employment is demonstrated on the LTPS-TFT with solid-phase crystallization method. However, the employment of high-κ gate dielectric has not been demonstrated on the LTPS-TFT with excimer laser annealing (ELA) crystallization method. Therefore, the impacts of the native growth interfacial layer HfO_2/poly-Si on ELA and MILC CMOS LTPS-TFT can be investigated in the future. Moreover, many passivation methods, like plasma treatment and ion implantation treatment, can also be employed on ELA and MILC CMOS LTPS-TFT with the adoption of high-κ gate dielectric. The reliability mechanisms of high-κ LTPS-TFT by ELA, MILC and SPC crystallization method can be studied simultaneously and clarified the difference. According to the study of electrical characteristics of high-κ LTPS-TFT with different crystallization technologies and defect passivation methods, the best performance and reliability LTPS-TFTs can be chosen for different applications. Flash memory of LTPS-TFT is a potential research topic in the future. In addition, three-dimension integration can be demonstrated in the future. The consisted elements of circuit can be fabricated on different inter-metal layer (IML) in back-end fabrication process. The realization of three-dimension integration can solve the scaling down limit of very large scale integration (VLSI) device. The driving current can be arbitrarily increased by increasing the width of device because the device area is not the concern if devices can be fabricated on IML. For display industrial, large size glass panel could provide a free space to design different functional circuits to realized SOP. In conclusion, high performance and reliability low-temperature polycrystalline-silicon thin-film transistors and its application would be the most potential research in the future.

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PUBLICATION LIST

A. International Journal:

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D. Local Conference [會議]:

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具高介電常數閘極絕緣層的低溫多晶矽薄膜電晶體之研究

Investigation on Low-Temperature Polycrystalline-Silicon Thin-Film Transistor with High-κ Gate Dielectric