國立交通大學

電子工程學系　　電子研究所

博士論文

應用於系統面板之各種薄膜電晶體元件結構之研究

Study on the Thin Film Transistors with Various Device Structures for System-on-Panel Applications

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中華民國九十八年八月

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摘要

在此論文中，分別針對汲極、閘極與通道等三項工程提出不同改善結構與技術以提昇低溫多晶矽薄膜電晶體之電特性。除此之外，為使系統面板能更具多元化，我們也開發以低溫多晶矽薄膜電晶體技術為基礎之非揮發性記憶體與場發射元件。

首先，針對低溫多晶矽薄膜電晶體汲極工程的開發，有別於傳統須複雜製程或額外光罩來製做的降電場結構，我們提出僅需簡單選擇性蝕刻法與臨場真空封裝技術製作出具有真空腔洞之T型閘極低溫多晶矽薄膜電晶體，利用製做出的偏移區域(offset region)與真空腔洞可有效降低其汲極端之大電場，因而可大幅降低漏電流、提高開關電流比、降低紐結電流(kink current)、與改善可靠度問題。

其次，針對低溫多晶矽薄膜電晶體閘極工程的開發，我們提出一種簡單且低成本的方式來製作新穎環繞式閘極與多重奈米通道之複晶矽薄膜電晶體。利用簡單間隙壁技術(spacer technique)來製作高寬比趨近於一之奈米通道，而不需先進微影技術。並利用蝕刻犧牲氧化層來讓奈米通道懸空以至於能被閘極完全包覆形成環繞閘極結構。製作出的具環繞閘極與多重奈米通道之複晶矽薄膜電晶體和傳統的元件比較起來有相當良好的電特性。該元件擁有較高載子移動率、較低的臨界電壓、較高開關電流比、與極佳之短通道效應之抑制能力。這些改善主要可歸功於環繞閘極增強閘極之控制能力、奈米線中

的三個尖端與較少的缺陷量。

針對通道工程的改善，我們提出兩種新穎製程方式可製作具高結晶性矽奈米線之多晶矽薄膜電晶體。第一種為控制最佳準分子雷射能量，直接對奈米線做結晶，由於利用前敘之隙壁技術會造成奈米線區域之非晶矽較薄，而汲/源區域較厚，故在雷射照射下，可控制晶種分別由汲/源區域兩區域成長過來，因而可達成只有一個晶界之奈米線，利用該法製作出的環繞式閘極薄膜電晶體擁有 273 cm^2/V-s 之場效載子移動率。另一種，則利用奈米尺寸之氮化矽隙壁(nitride spacer)當硬光罩直接蝕刻定義奈米線在連續側向固化結晶法(sequential-lateral-solidification)之大晶粒多晶矽薄膜上，由於奈米線尺寸遠小於大矽晶粒的尺寸，故可製作出幾乎是單晶的矽奈米線，利用該法製作出的環繞式閘極薄膜電晶體擁有 **596** cm^2/V-s 之場效載子移動率與極陡之次臨界擺幅(101 mV/decade) ，因此非常適用於未來系統面板(system-on-panel)的應用。

針對非揮發性記憶體開發，我們提出利用隙壁直接造成的三個尖端之電場增強式奈米線，使有效的提高 SONOS (silicon-oxide-nitride-oxide-silicon)記憶體之寫入/抹除效率。除此之外，我們也第一次提出將穿隧氧化層置換成真空之 SONVAS (silicon-oxide-nitride-vacuum-silicon)結構，由於穿隧層為為最低介電係數之真空，所以亦可進一步將穿隧層之電場提高，因而可進一步提高記憶體之寫入/抹除效率；且穿隧層為真空，可以降低傳統因多次寫入/抹除對穿隧氧化層造成的傷害，因而也可大幅提升其耐久(endurance)可靠度。

針對場發射顯示開發，我們也利用以低溫多晶矽為基礎之隙壁技術(spacer technique)製作兩種場發射元件，使其有機會能直接整合於系統面板上而取代傳統液晶顯示器。第一種為直接以隙壁矽奈米線之尖端當成場發射源，其導通電場為 2.06 V/μm。此外，我也利用前敘之環繞式電極直接當成陽極，懸空之三個尖端隙壁奈米線當成陰極，直接由 E-Gun 沉積的二氧化矽封成真空，利用該法製作出場發元件，導通電壓僅 0.14 V，為目前最低的導通電壓。

最後，該論文結論與針對未來系統面板研究可著重的工作方向亦討論之。

Study on the Thin Film Transistors with Various Device Structures for System-on-Panel Applications

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ABSTRACT

In this thesis, various structures and techniques are studied for the fabrication of high-performance low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) through drain, gate, and channel engineering. In addition, for further versatile system-on-panel (SOP) applications, the novel nonvolatile memories and field emitters based on LTPS technology are developed as well.

At first, for drain engineering, the T-shaped-gate (T-Gate) LTPS TFTs with symmetric vacuum gaps have been proposed and fabricated simply only with a selective-etching technique and an *in-situ* vacuum encapsulation. Due to the great reduction of electric field near the drain junction by the resulting offset region and vacuum gap, the fabricated T-Gate LTPS TFTs exhibit ultra low leakage current, high on/off current ratio, reduced kink current, and high reliability.

Secondly, for gate engineering, the novel gate-all-around (GAA) poly-Si TFTs with multiple nanowire channels (MNCs) have been, for the first time, fabricated using a simple process to demonstrate high performance electrical characteristics and high immunity to short channel effects (SCEs). The nanowire channel with high body thickness-to-width ratio,

approximately equals to one, is realized only with a sidewall-spacer formation. Moreover, the unique suspending MNCs are also achieved to build the GAA structure. The resultant GAA-MNC TFTs show outstanding three-dimensional gate controllability and excellent electrical characteristics, which reveal a high on/off current ratio, a low threshold voltage, a steep subthreshold swing, a near-free drain-induced barrier lowering, as well as an excellent SCE suppression.

For channel engineering, two types of novel processes are subsequently demonstrated for fabricating high-crystallinity Si-nanowire LTPS TFTs. The one is to utilize the previously proposed sidewall-spacer nanowire structure to control the lateral grain growth from the thicker S/D pads to the center of thinner nanowire channel. Due to the necking effect in such nanowire structure, only-one grain boundary exists in the middle nanowire channel. LTPS TFTs with field-effect mobility of 273 cm^2/V-s have been fabricated by using this method. The other is to utilize spacer lithography to directly transfer the nanowire pattern onto the large-grain sequential-lateral-solidification (SLS) poly-Si thin film. In term of probability, the nanowire pattern (8 nm) is much smaller than the SLS grain width (0.8 μm), which makes the nanowire locate within a single grain, thus the resulting nanowire can be performed like a single-crystal simply. Due to the high-crystallinity formed in the nanowire channel, the nanowire TFT exhibits an excellent mobility of **596** cm^2/V-s and steeper subthreshold slope of 101 mV/decade. As a result, it is very suitable for future system-on-panel (SOP) applications.

For nonvolatile memory development, a field-enhanced nanowire (FEN) LTPS-TFT silicon-oxide-nitride-oxide-silicon (SONOS) memory with a gate-all-around (GAA) structure has been proposed to improve the program and erase (P/E) performance. Each nanowire inherently has three sharp corners fabricated simply by sidewall spacer formation to obtain high local electric fields. The field-enhanced carriers tunneling via such a structure lead to faster P/E speed and wider memory window for the FEN SONOS as compared to the conventional planar (CP) counterpart. The FEN LTPS TFT SONOS device exhibits a V_{th} shift of 2.71 V and 2.11 V at V_{GS} = +15/-15 V in 1 ms for FN programming and erasing (P/E) operations, respectively. Other than FEN structure, a vacuum counterpart is further as a substitute for tunneling oxide to perform the novel silicon-oxide-nitride-vacuum-silicon (SONVAS) structure, for the first time. Due to the further electric field enhancement from the vacuum introduction in tunneling layer, the FEN SONVAS exhibits larger V_{th} shifts of 3.17V and 2.68V at V_{GS} = +15/-15V in 1 ms for FN P/E operations, correspondingly. Besides, due to the empty property of vacuum, there are less dangling bonds and tunneling-oxide traps produced during P/E cycles, so that FEN SONVAS exhibits much improved endurance reliability as well.

For field emitter development, spacer technique are applied on two types of LTPS-based field emitters for the possibilities of the replacement of LCD display elements in terms of system integration and image performance. For spacer nanowire field emitters, the F-N characteristics with turn-on field of 2.06 V/um have been performed. For the triple-corner nanowire emitter *in-situ* vacuum-encapsulated by the surrounding silicon dioxide, the F-N characteristics have been performed with a turn-on voltage of 0.14 V, which is the lowest one in the record to date.

Finally, conclusions as well as prospects for further research are also summarized.

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Contents

Chapter 3 Novel Gate-All-Around Polycrystalline Silicon Thin Film Transistors with Multiple Nanowire Channels…………………48

Chapter 6 Novel Polycrystalline Silicon Nanowire Field Emitters….……135

Table Lists

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

Chapter 1

Introduction

1.1 Overview of Low Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

During the last three decades, low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have been increasingly used in active matrix displays, such as active matrix liquid crystal displays (AMLCDs) [1.1]-[1.7] and active matrix organic light emitting displays (AMOLEDs) [1.8]-[1.14]. In 1980s, polycrystalline silicon (poly-Si) thin film transistors (TFTs) fabricated using a maximum temperature below 600 °C commenced to study. The original motivation of this concept was to replace expensive quartz substrate with low-cost glass for active matrix display applications. This would make large-area high-resolution active matrix displays more practical and cost-effective.

In the initial stage of active matrix liquid crystal displays (AMLCDs), hydrogenated amorphous silicon (a-Si:H) TFTs were predominantly applied as the pixel switching device. The major advantages of a-Si:H TFT technology are low processing temperature compatible with large-area glass substrate as well as its low leakage current due to the high off-state impedance. However, the low electron field-effect mobility (typically less than 1 $cm^2V^{-1}s^{-1}$) of a-Si:H TFTs confines their application to the switching elements only. Integration of driver circuitry with display panel on the same substrate is very desirable not only to reduce the module cost but also to improve the system reliability. Thus, poly-Si becomes a very attractive alternative material for the active elements of AMLCDs.

Essentially, the effective carrier mobilities in poly-Si are significantly higher (by two orders of magnitude) than those in a-Si, so that transistors with reasonably high drive currents can be achieved in poly-Si [1.15]. The higher drive current allows smaller TFTs to be used as the pixel-switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance [1.16]. In addition, the capability to realize complementary metal-oxide-semiconductor (CMOS) circuits allows low-power driver circuitry to be integrated with the active-matrix elements, for reduced display-module cost and improved reliability [1.17].

Previously, poly-Si TFT technology was primarily applied on small, high-definition LCD panels for projection display systems, because the required high processing-temperature made it incompatible with commercially available large-area glass substrates and necessitated the use of high-cost quartz substrates. In recent years, rapid progress of poly-Si has been made in the development of fabrication processes which are compatible with glass substrates and also in the improvement of process-module throughput, so that the cost-effective manufacture of LTPS TFT AMLCDs and AMOLEDs on large-area substrates increasingly flourishes.

1.2 Key Fabrication Processes of LTPS TFTs

As compared to modern complementary metal-oxide-semiconductor field-effect transistor (CMOS FET) process technology, the processes of LTPS TFTs technology only can be performed at relative low temperatures which are compatible with glass substrates. As a result, some maturely developed semiconductor fabrication processes in CMOS-FET technology cannot be applied to LTPS TFTs technology, especially on the high-temperature oxidation and dopant activation. Large-area glass substrates used in LTPS TFTs technology also make precise lithography difficult, including fine critical dimension (CD) definition and layer-to-layer registration. Basically, all kinds of processes in the fabrication of LTPS TFTs would affect the resulting TFT performance. Other than poor crystallinity of poly-Si by nature, there are still some unique processes profoundly affecting the LTPS TFT characteristics, including crystallization of amorphous silicon (a-Si) thin films, dopant activation, defect passivation, and deposition of gate dielectric.

In the following sections, more detailed information about fabrication processes, electrical characteristics, device architectures, and applications of LTPS TFTs is introduced to give an overall concept of LTPS TFT technology.

1.3 Channel Engineering: Crystallization of Amorphous Silicon (a-Si) Thin Films

Due to the crystallized poly-Si thin films always served as channel in the poly-Si TFTs, the quality of poly-Si active layer places a profound influence on the performance of poly-Si TFTs. A good-quality poly-Si thin film always results in good electrical characteristics of poly-Si. Thus, crystallization of a-Si thin films has been considered the most important process in the fabrication of LTPS TFTs. The defect density is generally a gauge for assessing the quality of poly-Si. In polycrystalline material, most of defects are always generated in the grain boundaries and intra-grain defects. Essentially, enlarging grain size can reduce the quantity of grain boundaries. Hence, enlarging grain size can effectively promote the quality of poly-Si. It is desirable that reducing defect density in poly-Si to approach the quality of single-crystalline to obtain the excellent performance comparable to that of silicon-on-insulator (SOI) device.

Various technologies have been proposed for a-Si crystallization. They can be classified into two groups: solid phase crystallization and liquid phase crystallization.

In solid phase crystallization, thermal annealing provides the energy required for grain nucleation and growth. In general, intrinsic solid phase crystallization needs a long duration to fully crystallize a-Si at low temperature, and large defect density always exists in crystallized poly-Si. In liquid phase crystallization, a laser is usually employed to melting the silicon thin film.

In the following, three kinds of low temperature crystallization methods, which have been most widely studied, are roughly reviewed, including solid phase crystallization (SPC), and liquid phase crystallization.

1.3.1 Solid Phase Crystallization

Solid phase crystallization (SPC) of a-Si is a simple and effective method to acquire poly-Si thin film with large grains [1.18]. In the SPC furnace annealing, the a-Si film is annealed in a furnace for as long as 24 hours at temperatures as high as 600°C. SPC of a-Si thin films involves two distinct processes, namely the nucleation of seeds (formation of clusters of crystalline silicon) and their growth to polycrystalline films [1.19]. The transformation in the a-Si annealing proceeds after an apparent incubation period via nucleation and dendritic-like growth of crystal domain within the amorphous matrix [1.20]. The nucleations of the crystals likely occur through the thermal reaction of crystal clusters. The rate-limiting step of the crystallization process is the rate of nucleation of seeds, which has an activation energy of about 5 eV [1.20]. The rate of the crystal growth has an activation energy of about 2.7 eV [1.20], [1.21].

Final grain size is known to be large when the nucleation rate is low and the grain growth rate is high [1.20]. Many alternatives to enlarge grain size of the annealed poly-Si thin film are to modify the structure disorder of the starting a-Si or poly-Si thin film. Previous studies indicated that the grain size was enlarged up to a few micrometers by means of solid-state crystallization of a-Si produced by self-ion bombarded polycrystalline or amorphous films deposited by LPCVD. It is possible that ion-bombardment amorphizes the embryo of crystallines which pre-exist at the interface of the as-deposited amorphous thin films so that the incubation period of nucleation is lengthened [1.22]-[1.24]. On the other hand, it has also been reported that the grain size of the recrystallized films formed from disilane (Si_2H_6) is larger than that formed from silane (SiH_4) [1.25]-[1.28]. The average grain size of the poly-Si thin film resulting from the crystallization of a film deposited in the amorphous phase by thermal decomposition of disilane, is a increasing function of the deposition rate, while as a function of the deposition temperature it exhibits a maximum at certain temperature (about 470°C) [1.29]. This can be attributed to the minimum nucleation rate resulting from the maximum structural disorder of the Si network. For deposition temperature higher than 470°C, the as-deposited silicon thin films have higher structural order (in the form of crystal-like clusters) which results in higher nucleation rate and thus small grain size; whereas at lower deposition temperature the higher structural disorder of the as-deposited film (or equivalently, the higher free energy) provides a driving force for accelerating the nucleation process. The increase in the grain size can also be obtained by increasing the deposition rate of the film [1.29]. Deposition rate also affects the structural order of the as-deposited film. A-Si thin films deposited at higher rates have higher structural disorder which results in lower nucleation rate during crystallization and thus larger grain size. Therefore, crystallization of a-Si thin films deposited by thermal decomposition of disilane yield very large grain size.

On the other hand, a number of researchers have examined the introduction of metal impurities during the SPC process, which is so called metal induced crystallization (MIC). In some case, this has enhanced the crystallization of the a-Si thin films at lower temperature. When a certain metal, for example, Al [1.30], Cu [1.31], Au [1.32], Ag [1.33], Pd [1.34], or Ni

[1.35], is deposited on a-Si, the a-Si crystallizes to poly-Si at a lower temperature than its SPC temperature. The reaction between a metal and a-Si occurs at an interlayer by diffusion and its lowers the crystallization temperature. Such enhancement of crystallization is due to an interaction of the free electrons from the metal with covalent Si bonds near the growing interface. Considering the metal-Si eutectic temperature, an a-Si thin film can be crystallized at below 500°C. A grain size up to 4-5 um has been achieved. However, with this method, the metal contamination is still an issue.

1.3.2 Liquid Phase Crystallization (Laser Crystallization)

Presently, a widely used method to prepare poly-Si on glass substrates is laser crystallization. Laser crystallization is a much faster process than SPC and MIC and can produce large grained poly-Si with a low dislocation density. The basic principle of laser crystallization is the transformation from amorphous to crystalline silicon by melting the silicon for a very short time. Poly-Si with large grains results from the subsequent solidification [1.36]. Strictly speaking, laser crystallization is not a low temperature process as the silicon is heated well above 1200 °C. However, the high temperatures are only sustained for a very short time. Due to the short time scale the thermal strain on the low-temperature substrates does not lead to severe damage or destruction of these substrates.

Laser crystallization of amorphous silicon has been a subject of intense research for a considerable time. Laser crystallization of a-Si can be performed using a variety of lasers and different techniques [1.37]-[1.40]. However, excimer laser crystallization (ELC) is by far the most widely used method at the moment [1.41], [1.42]. The principal advantage of excimer lasers is the strong absorption of UV light in silicon. In consequence, most of the laser energy is deposited close to the surface of the thin film and the thermal strain on the substrate is much lower than in case of lasers with longer wavelength. The basic transformation processes for excimer laser crystallization are divided into three crystallization regimes depending on the applied laser fluences and are relatively well understood [1.43], [1.44].

1.3.3 Defect Passivation

Other than mentioned crystallization, the incorporation of hydrogen into the channel layer (also called hydrogenation) to passivate the defect states is effective and essential for attaining good device performance and also for improving the uniformity of device performance. The electrical behavior of a poly-Si TFT is dominated by the effects of defect states within the poly-Si thin film. The high density of defect states result in poor device performance, such as low field-effect mobility, large leakage current, large threshold voltage, and large subthreshold swing. Because significant hydrogen diffusion occurs at temperatures above 350°C, the defects passivation process must be performed after all the high-temperature-processing steps in the poly-Si TFT fabrication processes. On the other hand, it has been reported that TFTs exposed to hydrogen plasma suffer from poor hot carrier endurance and a low thermal stability due to the weak Si-H bond [1.45]. NH_3 and N_2 have also been proposed instead of H_2. Better hot carrier endurance has been shown as the Si-N bond is stronger than Si-H bond [1.45], [1.46]. Alternative approach, which generates high-density plasma, such as ECR and TCP, may result in equivalent performance with high throughput [1.47].

1.4 Drain Engineering

For switching devices applications, the off-state leakage current of LTPS TFTs is the major concern. Although the field effect mobility of poly-Si TFTs is much higher than that of amorphous TFTs, the higher anomalous off-state leakage current in poly-Si TFTs is still an issue. The leakage currents can be reduced by either decreasing the trap state density or reducing the high electric field near the drain junction. For the driving circuit applications, the hot carriers phenomena are likely to occur in poly-Si TFTs, where supply voltages can be relatively high in the range 10-30 V [1.48]. As well known in crystalline Si (c-Si) MOSFET's, hot carrier phenomena are strongly depended upon the maximum electric field near the drain junction [1.49]. It is worth pointing out that in poly-Si TFTs, due to the high density of trap states localized at the grain boundaries, it is possible to achieve high electric fields, even at moderate biases. Moreover, poly-Si TFTs also suffer from floating body effect due to impact ionization occurring in the high electric field region at the drain end of the channel. This effect results in an increase of the output conductance, and it is responsible for degradation of the device characteristics both in digital and in analog applications such as noise margins and available voltage gain loss [1.50].

All these undesirable effects, including off-state leakage currents, hot carrier reliability, kink effect are all related to the high electric field near the drain junction.

Drain-field-relief structures are widely adopted to solve these undesirable effects. Lightly doped drain (LDD) and offset gate are commonly used structures for reducing leakage current. However, although the high resistivity of LDD and offset regions can effectively reduce the leakage current, unfortunately, the driving capability of TFTs is also degraded thereby. The resistivity of LDD regions depends on the length of LDD and the dose in LDD. In order to reduce leakage current without degrading driving current significantly and to get a maximum on/off current ratio, the length and dose of LDD should be carefully determined. As well as LDD structure, the length of offset region of offset gate structure should be carefully determine to keep the driving capability. Recently, advanced field-relief-structure such as field induced drain (FID) [1.51], [1.52] and gate-overlapped LDD (GOLDD) structure has been adopted to suppress the high drain field effects for improving device reliability and reducing leakage current while a high on-state current remains. In FID structures, the offset region is coupled by a sub-gate. The sub-gate is biased to induce inversion carriers in the offset region when the TFTs operate in the on state, so that the inversion carriers contribute to a lower resistivity in on state. In GOLDD structures, the LDD region is overlapped under gate edge. As well as FID structures, the surface of LDD region is inverted to a lower resistivity current path when the TFTs operate in the on state. A high on/off ratio can be achieved by such those advanced application because reducing leakage current while a high on-state current remains. However, the formation of FID or GOLDD structure generally requires an additional lithography step or complex fabrication process. Besides increasing fabrication cost, the misalignment in layer registration can result in asymmetrical characteristics of TFT and poor uniformity of TFT performance, especially for large-area glass substrates.

1.5 Gate Engineering

For the consideration of low power consumption, high speed and high packing density in system on a panel, there is a need to scale down poly-Si TFTs' device geometries However, scaling down the channel length will leads to undesirable short-channel effects. It will result in the threshold voltage roll-off, degradation in drain breakdown and severe kink effect. Comparing with single-crystalline Si MOSFET, poly-Si TFTs show more seriously short channel effect due to the presence of rich defect in the grain boundaries which enhance the impact ionization effects [1.53]. Since the defect traps play an intense influence on the electrical characteristics of poly-Si TFTs, one effective approach is to reduce the defects by improving the quality of poly-Si thin film. The other method is to enhance gate controllability to suppress the large filed near drain by modifying the device structures. Recently, for single-crystalline-Si MOSFETs, lots of efforts on non-planar device structures have been developed for better gate electrostatic control of the channel potential, such as double-gated, triple-gated, Π-gated, Ω-gated, nanowire channel, and GAA [1.54]-[1.58]. Among those, GAA FETs together with the nanowire channel have been reported to be the best structure for extreme geometry scaling [1.56]-[1.58].

1.6 System on a Panel (SOP) Issues

The advantages of integrating poly-Si TFTs circuits in the panel are not only it can allow pixel pitch to go beyond the bonding pitch of IC chips, but also permit to integrate a variety of circuitry not merely drivers [1.59]. However, the poly-Si TFT LCD module still costs a lot and consumes much power since it needs high driving speed and a wide voltage range analog interface [1.60]. If the TFT driver achieves full digital interface of transistor to transistor logic (TTL) or a lower voltage level, the cost of LCD module will be reduced and power consumption will be decreased.

1.6.1 Concept of System on a Panel

In short, the meaning of system on panel can be defined as the entire system integration on a single substrate including active matrix displays, integrated peripheral circuits, memory circuits, and controller circuits [1.60]-[1.63]. The first system on panel prototype was proposed by Sharp Corp. and Semiconductor Energy Laboratory Co. in 2004, which realizes the integration of CPU, an audio circuit, a graphic controller, and memories on the liquid crystal display by continuous grain silicon (CGS) technology. CG silicon fabricated in low temperature by catalyst assists solid phase crystallization, which doesn't subject to the effects of variations in laser density [1.64]. This crystallization method offers superior reliability and uniformity. The 8-bit CPU contains about thirteen thousand TFTs and operates at 3MHz with 5V voltage supply.

Various kinds of voltage or signal losses come into existence in the module because the system has to transfer enormous data between the large scale circuits at high frequency [1.60]. If the large scale circuits can be entirely integrated in the same substrate without sacrificing functional properties, the total performance will be improved and the power consumption will be diminished theoretically. More importantly, the size, weight, and cost of the system will be cut down which is beneficial to the consumers.

There are two main considerations to achieve the goal of system on panel. First, the properties of poly-Si TFTs must be improved such as better mobility (larger than 400 cm^2/Vs), shorter channel device (less than 1 μm), lower sub-threshold swing (~0.1 V/dec), lower threshold voltage(~±0.7 V), higher on/off current ratio (~10^9) are needed. Second, the circuit interconnection technique needs to be promoted. When shrinking the transistor size, excellent uniformity and reliability are critically required for the development of SOP.

1.7 Motivation

Low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have received much attention in recent years because of their increasing use in active matrix displays, such as active matrix liquid crystal displays (AMLCDs) [1.1]-[1.7] and active matrix organic light emitting displays (AMOLEDs) [1.8]-[1.14], and potential for 3-dimension ICs' applications [1.65]. The ability of fabricating high-performance LTPS TFTs enables their use in further applications of SOPs. Therefore, there is great interest in improving the performance of LTPS TFTs. Considering the issues of system on panel (SOP) mentioned in former section, both the LTPS TFT performance and the added-value functionality need to be further promoted and developed. For the further development, high versatile circuits and systems need to be fully integrated to achieve system-on-panel (SOP). As performance and complexity requirements increase, there is a need to scale down device geometries to achieve higher speeds and packing densities. Unfortunately, those undesirable effects in the electrical characteristics that mentioned above become particularly important as the channel length and gate insulator thickness are reduced. Those all are increased with the higher drain electric field near the drain junction. These undesirable effects prohibit the use of poly-Si TFTs in many high-performance circuit applications. Therefore, the drain-field-relief structure plays an essential role for the future prospection. However, those structures often required complicated process (such as, spacer and damascene processes), or additional mask step which may raise the mis-alignment problem. In chapter 2, a novel and simple process was introduced to fabricate T-shaped gate (T-Gate) structures.

Especially for high-speed and low-power applications, the scaled-down LTPS TFTs with high performance are required. Unfortunately, several short-channel effects are known to aggravate with reducing device dimension, such as threshold voltage roll-off, higher subthreshold swing, larger drain-induced barrier lowering (DIBL), and acuter kink effect. The short-channel effects seriously restrict these applications. Recently, for single-crystalline MOSFETs, lots of efforts on non-planar device structures have been developed for better gate electrostatic control of the channel potential, such as double-gated, triple-gated, Π-gated, Ω-gated, NW fin-channel, and gate-all-around (GAA). Among those structures, the GAA structure with nanowire channels is proposed to be the best structure to provide the immunity of short-channel effects. Additionally, the poly-Si TFTs suffer more serious short-channel effects than SOI devices due to the presence of grain boundary and intra-grain defects in channel region. However, there are few works presented such structures on poly-Si TFTs so far. In chapter 3, the gate-all-around poly-Si TFTs with multiple nanowire channels, for the first time, are proposed by using simple process sequence to achieve high electrical performance and effectively suppress the short-channels effects.

Since the quality of poly-Si active layer places a profound influence on the performance of poly-Si TFTs, crystallization of a-Si thin films becomes the most important process issue in the fabrication of high-performance LTPS TFTs. A good-quality poly-Si thin film always results in good electrical characteristics of poly-Si. Various crystallization technologies have been propose to create high-quality poly-Si thin films on foreign substrates at low temperature, however, most of them are still complex and not easy to control. As a result, in chapter 4, two types of simple process sequences were demonstrated for fabricating gate-all-around LTPS TFTs with high-crystallinity Si nanowire (NW) channels. The one is the excimer-laser-crystallized (ELC) nanowire TFT, in which the nanowire structure features only-one grain boundary. The other is the spacer-patterned nanowire TFT based on large-grain poly-Si thin film prepared with sequential-lateral-solidification (SLS) crystallization, in which the nanowire can be controlled to be approximated single-crystalline.

In addition to promoting the device performance of basic LTPS TFTs, for system-on-panel (SOP) developments, other added-value functional elements based on poly-Si TFT technology, such as memory and display elements are also needed to develop to fully integrate on the same display panel. In chapter 5, we utilized the spacer technique to promote nonvolatile memory performance on SONOS NVM for SOP applications. In chapter 6, we further applied this technique on two types of field emitters for the opportunity of replacement of LCD display elements in terms of system integration and image performance.

1.8 Thesis Organization

In this thesis, various structures and techniques are studied for the fabrication of high-performance low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) through drain, gate, and channel engineering. In addition, for diversified SOP application, the SONOS memory, field emitters and flexible electronics are developed. The outline of thesis organization is shown in Fig. 1-2.

In chapter 2, a novel and simple process was introduced to fabricate T-shaped gate (T-Gate) structures.

In chapter 3, the gate-all-around poly-Si TFTs with multiple nanowire channels are proposed by using simple process sequence to achieve high electrical performance and effectively suppress the short-channels effects.

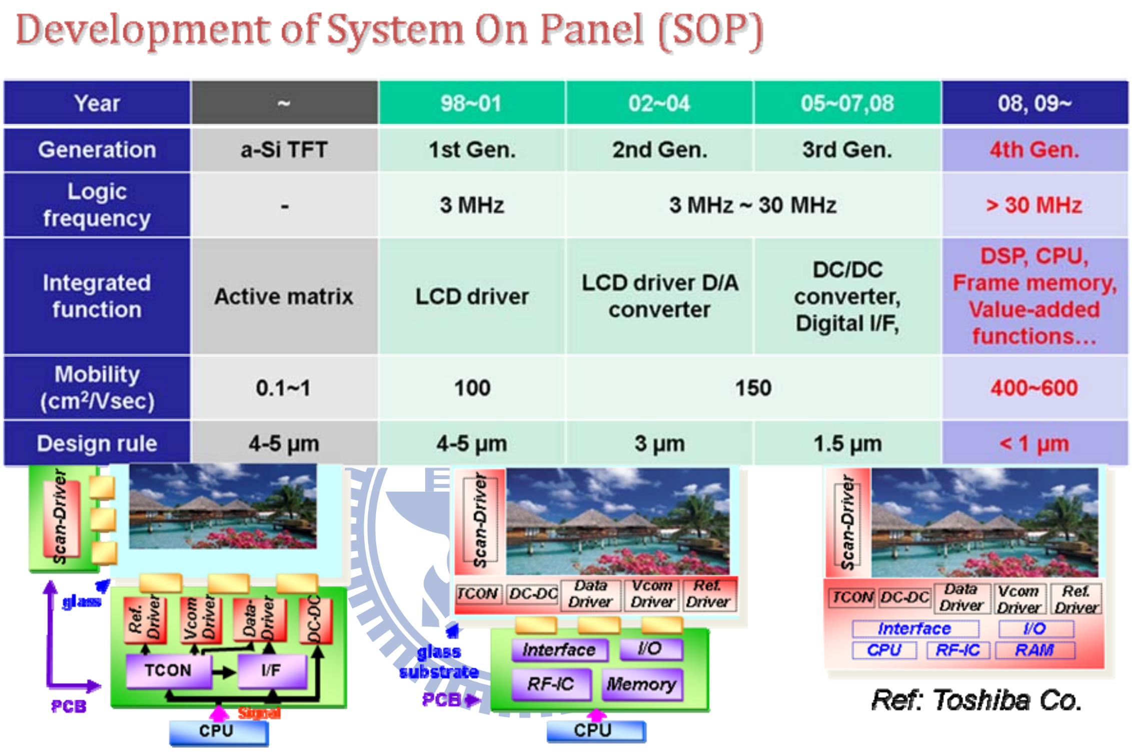
In chapter 4, two types of novel and simple processes were demonstrated for fabricating high-crystallinely Si nanowire LTPS TFTs with gate-all-around structures for channel engineering development.

In chapter 5, based on previous proposed gate-all-around structure, two kinds of trapping-charge memory devices with field-enhanced nanowire and/or silicon-oxide-vacuum-oxide-silicon (SONVAS) structures were proposed for the first time to improve the memory performance and reliability with a simple process sequence for SOP applications.

In chapter 6, we further applied this technique on two types of field emitters for the opportunity of replacement of LCD display elements in terms of system integration and image performance.

Finally, summary and conclusions as well as recommendation for further research are given in chapter 7 and chapter 8, respectively.

Figures

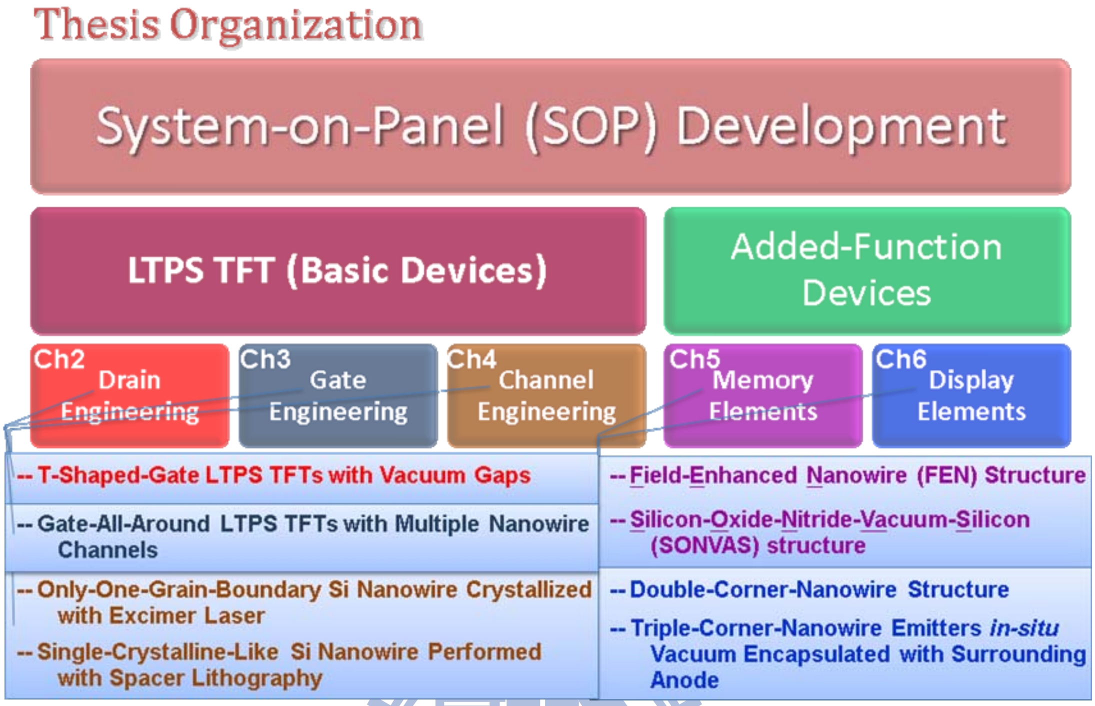


Development of System On Panel (SOP)

Year	~	98~01	02~04	05~07,08	08, 09~
Generation	a-Si TFT	1st Gen.	2nd Gen.	3rd Gen.	4th Gen.
Logic frequency	-	3 MHz	3 MHz ~ 30 MHz		> 30 MHz
Integrated function	Active matrix	LCD driver	LCD driver D/A converter	DC/DC converter, Digital I/F,	DSP, CPU, Frame memory, Value-added functions…
Mobility ($cm^2/Vsec$)	0.1~1	100	150		400~600
Design rule	4-5 μm	4-5 μm	3 μm	1.5 μm	< 1 μm

Ref: Toshiba Co.

Fig. 1-1 Development of system on panel (SOP)



Thesis Organization

System-on-Panel (SOP) Development

LTPS TFT (Basic Devices)

Added-Function Devices

Ch2 Drain Engineering

Ch3 Gate Engineering

Ch4 Channel Engineering

Ch5 Memory Elements

Ch6 Display Elements

-- T-Shaped-Gate LTPS TFTs with Vacuum Gaps

-- Gate-All-Around LTPS TFTs with Multiple Nanowire Channels

-- Only-One-Grain-Boundary Si Nanowire Crystallized with Excimer Laser

-- Single-Crystalline-Like Si Nanowire Performed with Spacer Lithography

-- Field-Enhanced Nanowire (FEN) Structure

-- Silicon-Oxide-Nitride-Vacuum-Silicon (SONVAS) structure

-- Double-Corner-Nanowire Structure

-- Triple-Corner-Nanowire Emitters *in-situ* Vacuum Encapsulated with Surrounding Anode

Fig. 1-2 Outline of thesis organization.

Chapter 2

Novel T-Shaped-Gate Polycrystalline Silicon Thin Film Transistors with *in-situ* Embed Vacuum

2.1 Introduction

Poly-Si thin film transistors (TFTs) have been widely applied as switching elements in active matrix liquid crystal displays (AMLCDs), and active matrix organic light emitting diodes (AMOLEDs) [2.1]-[2.5]. Unlike the conventional amorphous silicon TFTs, poly-Si TFTs exhibit higher driving current. For further SOP development, high versatile circuits and systems need to be fully integrated on the display panel substrate [2.6], [2.7]. Unfortunately, conventional poly-Si TFTs suffer from anomalous off-state leakage current, serious kink effect, and hot-carrier instability, which are all related to the high electric field near the drain junction. Those undesirable effects prohibit the use of poly-Si TFTs in many high-performance and low-standby-power circuit applications. The dominant off-state leakage current is due to the field emission via grain boundary traps induced by the high electric field in the drain depletion region [2.8], [2.9]. It has been widely reported that the offset-gated and lightly doped drain (LDD) poly-Si TFTs can effectively reduce the maximum drain electric field in the channel. However, the offset-gated poly-Si TFTs cause a high parasitic resistance in the offset region which severely decreases the on-current [2.10], [2.11]. Besides, in LDD structure, the device degradations due to the additional n- implant damage caused by low-temperature activation of dopants (< 600 ˚C) and difficulty in doping control at the grain boundaries are also serious problems [2.12]. Recently, the offset-gated poly-Si TFTs with sub-gate structures together with thicker dielectrics below sub-gate, which have lower off-state leakage current, while maintain high turn-on characteristics, as well as free from LDD implant damage, have been reported [2.13]-[2.15]. However, those structures often required complicated process (such as spacer and damascene processes), or additional mask step which may raise the mis-alignment problem [2.16].

In this chapter, a T-shaped-gated (T-Gate) poly-Si thin-film transistor with self-aligned sub-gates and *in-situ* embed vacuum is proposed and fabricated only with a simple selective side-etching process and without any additional photo-lithography step. Besides, novel vacuum (the lowest permittivity of k=1 in nature) gaps embedded in this T-Gate structure are *in-situ* created via capping the SiH_4-based passivation oxide in plasma enhanced chemical vapor deposition (PECVD) system [2.17].

The schematic figure of the proposed T-Gate TFTs and its equivalent structure were shown in Figs. 2-1(a) and (b), respectively. The vacuum gaps can reduce the vertical electric field near the drain due to its lowest permittivity of k=1. The vacuum gaps serve as an equivalent thicker oxide. Due to the relative static permittivity SiO_2 of 3.9, the equivalent oxide thickness of the vacuum gap is as high as 3.9 times [2.18]-[2.20]. The poly-Si region under vacuum gaps can be considered as the offset region and the gate edge over the vacuum cavity serves as a field plate connected with the main gate, so that the proposed TFT operates similar as the field induced drain (FID) TFTs.

2.2 Electrical Simulations for T-Gate LTPS TFTs with Vacuum Gaps

Device simulation is first carried out to compare the electric field distributions of T-Gate

TFTs with different vacuum-gap thickness (T_{vac}) and length (L_{vac}) which are followed by the experimental details of device fabrication. The 2-D numerical simulation was carried out using ISE which is a commonly used numerical simulator for device analysis [2.21]. Figs. 2-2 (a) and (b) display the simulated potential contours of the proposed T-Gate and the conventional poly-Si TFTs at V_{GS} = 1.5 V and V_{DS} = 20 V, respectively. It can be seen evidently that in the T-Gate LTPS TFT, the electrostatic potential contours at channel surface near the drain can be relaxed remarkably by the additional offset region and vacuum gap, as compared with that in the conventional device. Under higher negative gate bias, the effective thicker gate insulator resulting from the extra vacuum gap can make less gate voltage couple to the drain junction [2.22]-[2.24]. Thus, not only the maximum lateral electric field (E_{ML}) but also the maximum vertical electric field (E_{MV}) can be effectively reduced for the proposed T-Gate poly-Si TFT.

Figs. 2-2 (a) and (b) show the 2-D electrical potential distribution of the conventional and T-Gate TFTs, respectively. The dense equi-potential lines near the drain region in conventional TFTs can be significantly relaxed in the T-Gate TFTs, indicating that electric field is consequently reduced by T-Gate structure. Figs. 2-3 (a) and (b) shows the corresponding simulated lateral and vertical electric field distributions along the channel surface near the drain junction for T-Gate TFTs with various T_{vac} and L_{vac}, respectively. The maximum lateral and vertical electric field decreases with increasing T_{vac} and L_{vac} in the T-Gate TFT. The reduction of vertical electric field is dominated by the vacuum-gap height (T_{vac}), while reduction of lateral electric field is dominated by the offset length (i.e. the side-etching length, L_{vac}).

Thus, the maximum electric field near the drain can be effectively decreased by applying the T-Gate structure.

2.3 Experiments

2.3.1 Fabrication Sequence of T-Gate Poly-Si TFTs with Vacuum Gaps

The detailed process flow of device fabrication is shown in Figs. 2-4 (a)-(k). At first, a buffer layer that composed of 50nm-thick SiN and 130nm-thick SiO_2 thin films was deposited by plasma-enhanced chemical vapor deposition (PECVD) system on the glass substrate. Then, a 50 nm amorphous silicon (a-Si) thin film was deposited by PECVD system on buffer layer. Before excimer laser crystallization, dehydrogenation at 500 °C for 15 minutes was carried out to prevent the hydrogen explosion during laser irradiation. The a-Si thin film was transferred into poly-Si by 308-nm XeCl excimer laser with laser energy density of 257 mJ/cm^2 and shot overlapping of 99%. After defining the active layer, a 40 nm or 80 nm-thick SiO_2 was deposited as gate insulator by PECVD system at 420 °C. A 50 or 100 nm-thick indium tin oxides (ITO) and a 200 nm-thick Mo films were deposited by sputter system at room temperature sequentially. The stacked Mo/ITO films were simultaneously etched to pattern as the gate electrode. An oxalic acid, $(COOH)_2 \cdot 2H_2O$, solution was then used to selectively etch the ITO layer without harming Mo layer to form the T-shaped structure. Different side etching lengths of ITO thin film were carefully controlled to 250 and 500 nm confirmed by the scanning electron microscope (SEM) analyses. A self-aligned phosphorous implantation was carried out to form source and drain regions with the implantation energy and dosage of 15 keV and 2×10^{14} cm^{-2}, respectively. Then, a 500-nm-thick inter-layer dielectric of silane (SiH_4)-based SiO_2 was deposited by PECVD system. It should be noted that the vacuum gaps were *in-situ* formed during the inter-layer dielectric deposition by PECVD due to the active chemical properties of silane-based (SiH_4) free radicals [2.25]. Then, the dopants were activated through rapid thermal annealing (RTA) at 620 °C for 30 seconds.

After standard contact hole opening, 500-nm-thick Al was deposited and patterned as interconnect metal. Finally, some TFTs were subjected to the NH_3 plasma treatment at 300 °C for 1 hour to passivate the dangling bonds at the poly-Si/SiO_2 interface and the trap-states within the poly-Si film. For the purpose of comparison, the conventional poly-Si TFTs without side-etching process shown in Fig. 2-11(l) were also fabricated with the same process sequence. For all T-Gate devices, the channel length (L) is defined as the length of the patterned Mo gate electrode, the height of vacuum gap (labeled as T_{vac}) is determined by the thickness of deposited ITO, and the length of vacuum gap (labeled as L_{vac}) is determined by the length of side-etched ITO. The split conditions of various T_{vac} and L_{vac} were designed and listed in Table 2-1. The corresponding SEM images of the fabricated T-Gate and the conventional TFTs are shown in Figs. 2-5 and 2-6, respectively.

2.4 Results and Discussion

2.4.1 Method of Electrical Parameter Extraction

In the whole thesis, all the electrical characteristics of LTPS TFTs were measured by HP 4156C semiconductor parameter analyzer. Extraction methods of all the electrical parameters mentioned in this thesis, including the threshold voltage (V_{th}), subthreshold swing (S.S.), maximum on-current (I_{on}), minimum off-current (I_{off}) and the on/off current ratio, are introduced.

Threshold Voltage (V_{th})

The method to determine the threshold voltage in this thesis is the constant drain current method, that is, defined as the gate voltage required to achieve a normalized drain current of $I_D = (W/L)\times 10^{-8}$ A at $|V_{DS}| = 0.1V$.

Field effect mobility (μ)

The field effect mobility is extracted from the maximum transconductance in the linear region of I_{DS}-V_{GS} characteristics at $|V_{DS}| = 0.1V$ using the formula:

$$\mu^* = \frac{g_m}{C_{ox}(\frac{W}{L})V_{DS}}(@V_{DS} = 0.1V) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

, where C_{ox} is the gate oxide capacitance per unit area, and the transconductance (g_m) is defined as:

$$g_m = \frac{\partial I_D}{\partial V_g}|_{V_{DS}=0.1V} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(2)$$

Field effect mobility is an important parameter for carrier transport; it describes how strong the motion of an electron or hole is influenced by the applied electric field.

Subthreshold swing (S.S.)

Substhreshold swing (SS) is defined as:

$$\mathrm{SS} = \min\left(\frac{\partial \log(I_D)}{\partial V_G}\right)^{-1} @V_{DS} = 0.1V \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots(3)$$

It is a typical parameter to describe the control ability of gate toward channel.

Maximum on-current and Maximum leakage-current

In this chapter, on-current is defined as the drain current measured at V_{GS}= 15V, V_{DS}= 3V. Maximum leakage current is defined as the drain current measured at V_{GS} = -15V, V_{DS} = 3V.

On/off current ratio

The on/off current ratio is defined as the ratio of maximum drain current over minimum drain current at $|V_{DS}| = 3$ V.

A high performance poly-Si TFT should not only provides high on-state driving current but low off-state leakage current. High on-state driving current means the pixel capacitances could be charged more efficiently during a line access time. Sufficiently low off-state leakage current represents the charged capacitance could remain stable during the much longer frame time. Therefore, on/off current ratio is obviously a more appropriate evaluation parameter compared with on-state or off-state current alone.

2.4.2 Electrical Characteristics of T-Gate TFTs with Vacuum Gaps

Fig. 2-7 shows the transfer characteristics of T-Gate LTPS TFTs with different T_{vac} and fixed L_{vac}; while Fig. 2-8 shows those with different L_{vac} and fixed $T_{vac.}$ All T-Gate LTPS TFTs are with channel length of 5 µm and channel width of 10 µm, and gate oxide thickness of 400 Å. It is shown that the leakage current of T-Gate LTPS TFTs could be remarkably suppressed without degrading on current significantly. It is attributed to the drain field relief via the offset region and vacuum gap to reduce the leakage current at the off state, and the low series resistance via field plate assistance to maintain the on current at the on state. The leakage current of T-Gate LTPS TFTs could also be further reduced by increasing the T_{vac} or L_{vac} due to the more vertical or lateral drain-field reduction, respectively, which is consistent with previous simulated results. For the T-Gate TFTs with $T_{vac} = 100$ nm and $L_{vac} = 500$ nm, the leakage current could be suppressed to below 1 pA at $V_{DS} = 3$V and $V_{GS} = -15$V, which is about three-order reduction as compared to conventional one, and the maximum on/off current ratio could be promoted to beyond 10^9. Table 2-2 lists the typical electrical characteristics of these devices.

In order to verify the symmetry of self-aligned ITO side etching process, the forward-mode and reverse-mode measurement were carried out, whose corresponding measurement is illustrated in Fig. 2-9. Fig. 2-10 shows the transfer characteristics of the fabricated T-Gate LTPS TFT under forward and reverse modes. There is almost no difference between these two modes, indicating that the ITO side-etching from the two sides of the patterned gate is symmetry and self-aligned.

Fig. 2-11 shows the output characteristics of T-Gate and conventional LTPS TFTs. It is shown that T-Gate LTPS TFT exhibits a reduced kink effect, while conventional LTPS TFT suffers from a severe kink at high drain biases. It is believed that the moderate kink in T-Gate LTPS TFT is mainly due to a relative low electric field near the drain junction. For conventional LTPS TFT, the severe kink at high drain biases is a result of the exaggerated avalanche multiplication near drain junction caused by the high drain field and the large amount of traps [2.26].

2.4.3 Effect of Gate Oxide Thickness

T-Gate TFTs with two different oxide thicknesses of 40 nm and 80 nm were performed to discuss the effect of gate oxide thickness. The transfer characteristics of these two kinds of T-Gate TFTs are shown in Figs. 2-12 and 2-13, respectively. The channel width and channel length were 10 μm and 5 μm. T_{vac} and L_{vac} were fixed at 100 nm and 250 nm, respectively. The leakage current as well as the driving current at large gate bias (i.e. at V_{GS} = -15 V and 15 V) are listed at Table 2-3. A better outcome of leakage current reduction is observed in the T-Gate TFTs with thinner gate insulator (40 nm) in comparison with the thicker one (80 nm).

Figs. 2-14 and 2-15 are the schematic illustrations of the equivalent structure of T-Gate TFTs in which the thickness of gate oxide are 40 and 80 nm, respectively. The equivalent oxide thickness at the gate edge of T-Gate TFTs with 40 nm gate oxide is 440 nm in which is 11 times the thickness of the conventional TFTs. As to the T-Gate TFTs with 80-nm-thick gate oxide, only 6 times is observed.

2.4.4 Oxide Breakdown Characteristics of T-Gate LTPS TFTs with Vacuum Gaps

Due to the low-temperature process of PECVD, the gate oxide used in LTPS TFTs usually exhibits poorer physical and electrical qualities, such as low density, high gate leakage current, and low breakdown field characteristics as compared to those high-temperature thermal grown oxide used in MOSFET technology. And, the protruded silicon surface caused from the ELA crystallization further worsens the breakdown field characteristics. To overcome this unavoidable problem, gate dielectric thin films have to be thicker to improve the poor oxide breakdown characteristics, however reducing TFT driving ability.

The gate breakdown characteristics of T-Gate and conventional TFTs with 40-nm-thick gate insulators are shown in Fig. 2-16. T-Gate TFTs with T_{vac} = 100 nm and L_{vac} = 500 nm has an excellent breakdown voltage of about 36.4 V while the conventional one has a poorer one of about 24.8 V. This is because the maximum vertical electric field between the gate edge and S/D are relaxed by the embedded vacuum in such T-Gate structure. That is, the T-Gate TFTs have a higher gate-voltage operation range than the conventional TFTs.

2.4.5 Drain Avalanche Hot Carrier (DAHC) Stress on T-Gate LTPS TFTs with Vacuum Gaps

Figs. 2-17 (a)-(c) show the transfer characteristics of conventional and T-Gate TFTs before and after drain avalanche hot carrier stress at $V_{DS} = 10$ V, $V_{GS} = 1.5$ V from 0 to 1000 seconds, respectively. Less degradation on transconductance, on-current and threshold voltage shift are revealed for T-Gate TFTs, while there is a serious degradation is in the conventional one. The shifts of threshold voltage, transconductance and I_{ON} were extracted in Fig. 2-18(a)-(c), respectively. Those demonstrated obviously that the T-Gate TFTs have a better immunity on drain avalanche hot carrier stress as compared to conventional one.

2.5 Summary

In this chapter, we have demonstrated high performance and high reliability T-Shaped-Gate polycrystalline silicon thin-film transistors fabricated by a low-cost process. High-performance T-Gate TFTs with on/off ratio exceeding 10^9 have been demonstrated. The maximum leakage current (i.e. the drain current at $V_{GS} = -15$ V and $V_{DS} = 3$ V) was distinctly improved more than three orders by applying T-Gate structure. In addiction, the alleviation of kink effect was also observed due to the lower impact ionization from the proposed structure.

T-Gate LTPS TFTs with thinner oxide have better field-relief efficiency as compare to those with thicker ones. It is because the vacuum contributes more weighting in the effective oxide thickness for the thinner oxide case.

The symmetry of electrical characteristics was performed to verify that ITO side etching step was a self-aligned process. Additionally, the oxide breakdown field can be promoted from 24.8 V to 36.4 V by adopting the T-Gate TFTs with 100-nm-thick vacuum gaps. Moreover, T-Gate LTPS TFTs have been demonstrated to a better immunity to drain avalanche hot carrier stress.

To sum up, T-Gate structure with vacuum gaps was attractive, especially for the thin oxide devices. The characteristics of T-Gate LTPS TFTs with vacuum gaps exhibited excellent on/off current ratio. The leakage current can be decreased dramatically while the driving can be maintained. Besides, the improvement of oxide breakdown characteristics can enlarge the operation range of the gate bias. Furthermore, the proposed T-Gate TFTs have much superior immunity to the hot carrier degradation as compared with the conventional ones.

Tables

Table 2-1 Split conditions with different vacuum gap height (T_{vac}), side etching length (L_{vac}).

	T_{vac} (nm)	L_{vac} (nm)
0	0	0
1	50	250
2	100	250
3	100	500

Table 2-2 Measured electrical characteristics of conventional and T-Gate TFTs. On current is defined as the drain current measured at V_{GS} = 15V, V_{DS} = 3V. Leakage-current is defined as the drain current measured at V_{GS} = -15V, V_{DS} = 3V.

	Leakage Current (A) @V_{GS}= -15 V; V_{DS}= 3 V	Min. Leakage Current (A) @V_{DS}= 3 V	On current (A) @V_{GS}= 15 V; V_{DS}= 3 V	Max. I_{on}/I_{off} @V_{DS}= 3 V	V_{th} (V)	S.S. (mV/dec)
Conventional	1.81×10^{-8}	2.59×10^{-12}	4.89×10^{-4}	1.89×10^{8}	-0.393	192
T_{vac}=50 nm L_{vac}=250 nm	2.83×10^{-9}	1.23×10^{-12}	3.7×10^{-4}	3.01×10^{8}	-0.379	201
T_{vac} =100 nm L_{vac} =250 nm	7.45×10^{-11}	1.4×10^{-13}	3.21×10^{-4}	2.29×10^{9}	-0.249	238
T_{vac} =100 nm L_{vac} =500 nm	8.6×10^{-13}	7.2×10^{-14}	1.27×10^{-4}	1.76×10^{9}	-0.228	350

Table 2-3 Extraction of the leakage current and the on current at large gate bias (at V_{GS} = -15 V and 15 V, respectively) with different gate oxide thickness. Notice that the leakage current reduction efficiency abruptly decreased while the gate oxide thickness increased.

T_{ox}	Structure	Leakage current (A) @V_{GS} = -15 V ; V_{DS} = 3 V		On current (A) @V_{GS} = 15 V ; V_{DS} = 3 V	
40 nm	T-Gate TFTs	7.45E-11	X (1/4116)	3.21E-4	X 0.65
	Conv. TFTs	1.81E-8		4.89E-4	
80 nm	T-Gate TFTs	1.77E-11	X (1/26)	2.06E-4	X 0.71
	Conv. TFTs	4.72E-10		2.9E-4	

Figures

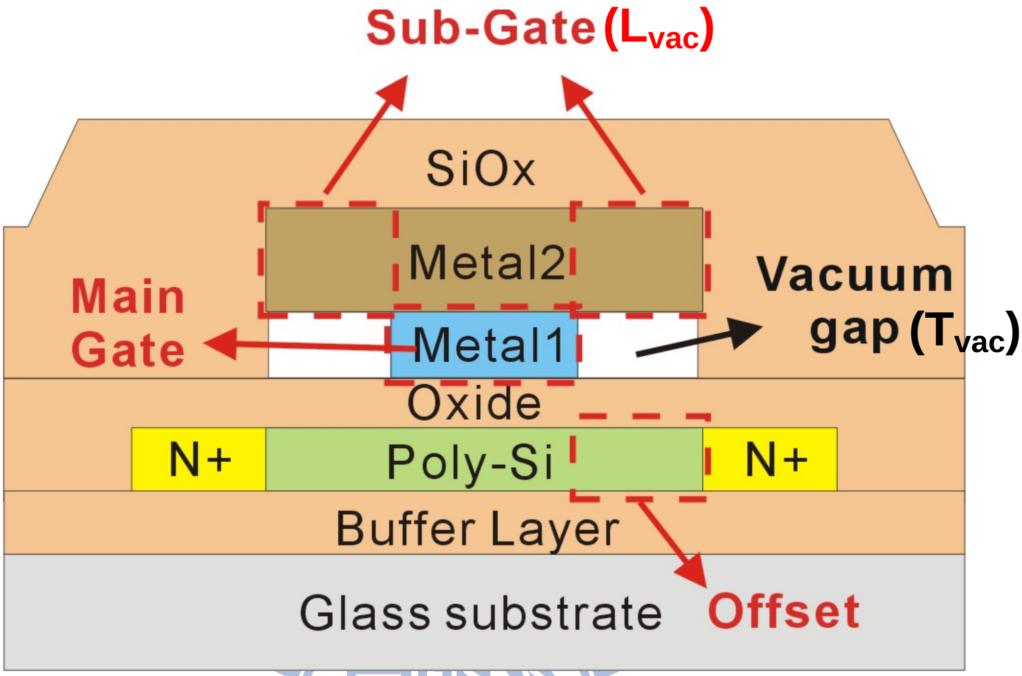


Fig. 2-1(a) The device structure of proposed T-Gate LTPS TFTs with vacuum gaps

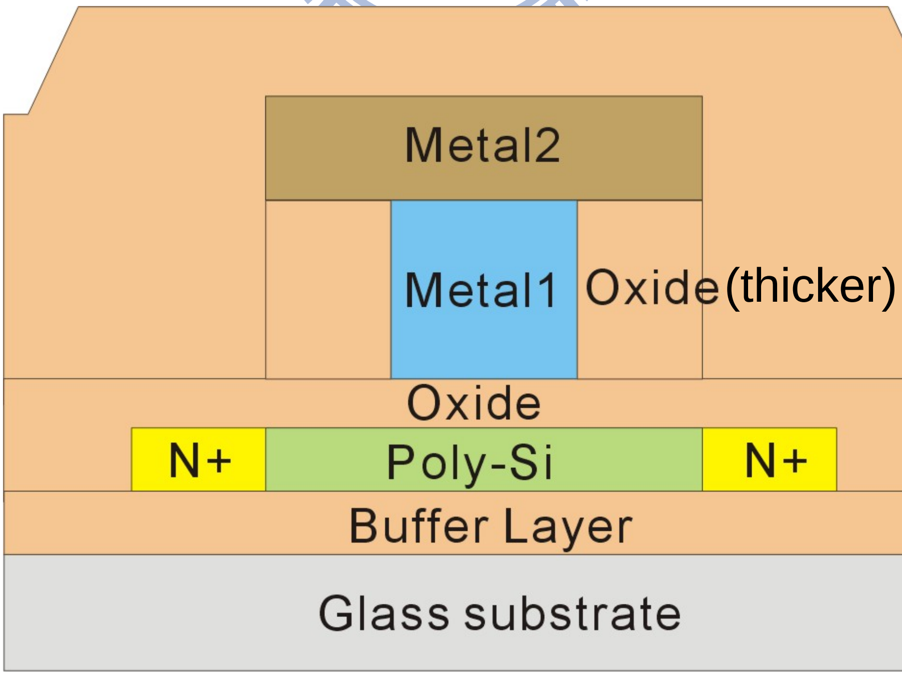


Fig. 2-1(b) The schematic illustration of the equivalent device structure of the proposed T-Gate LTPS TFTs with vacuum gaps

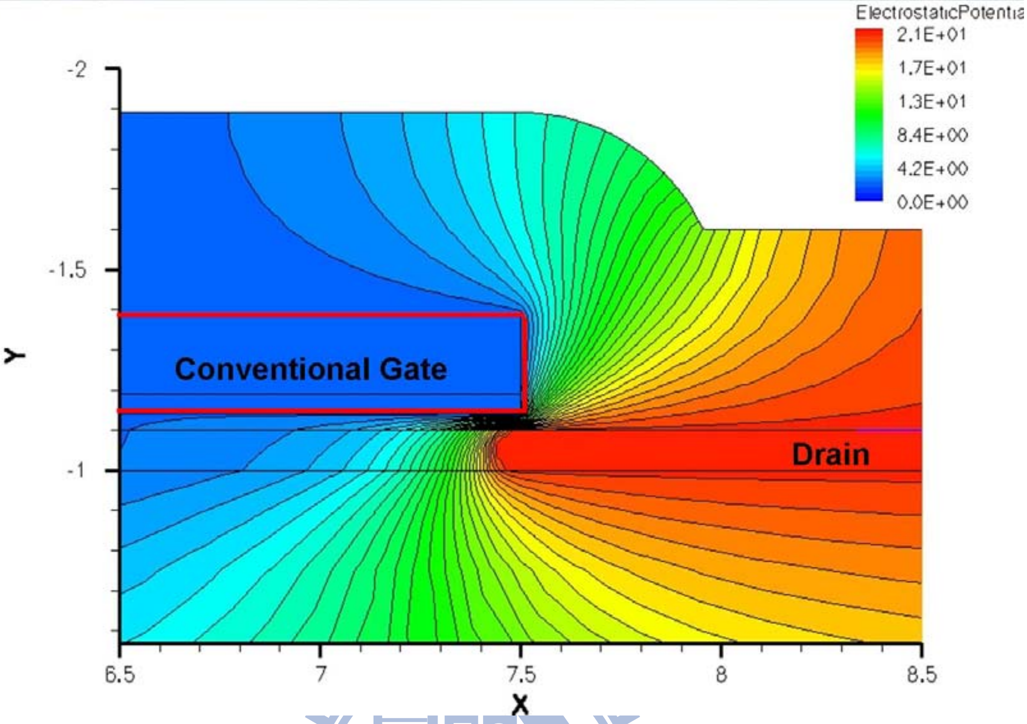


Fig. 2-2(a) The 2-D electrical potential distribution of the conventional TFTs.

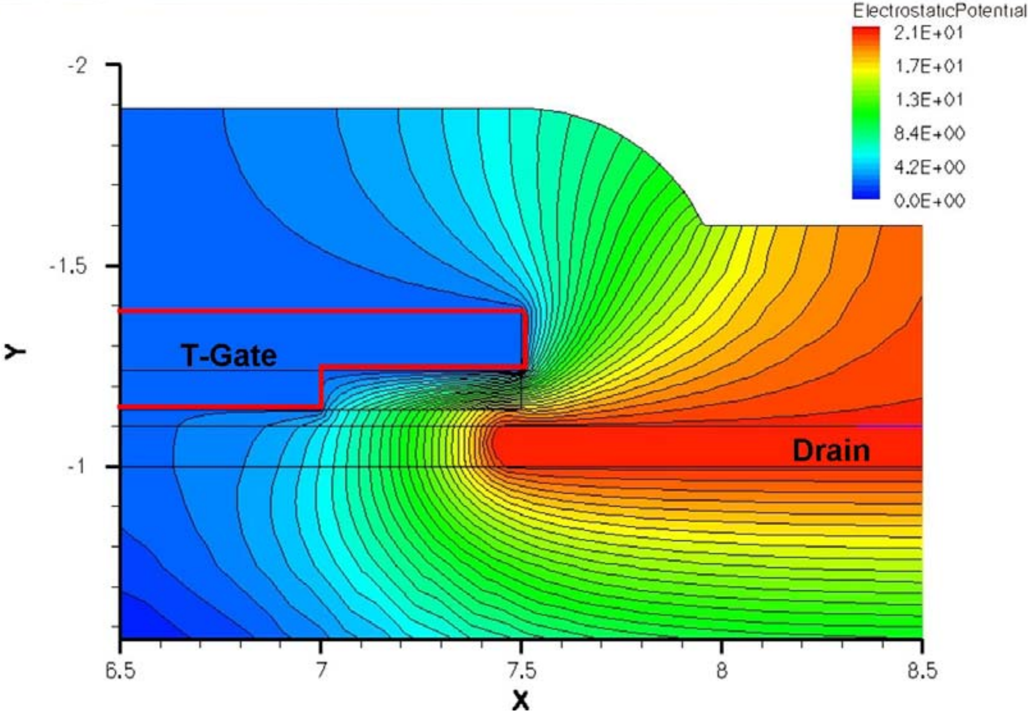


Fig. 2-2(b) The 2-D electrical potential distribution of the T-Gate TFTs.

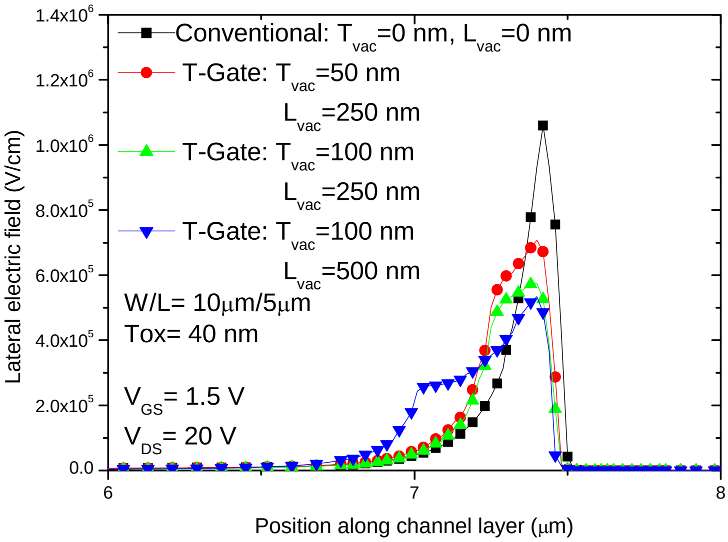


Fig. 2-3(a) The lateral electric fields under positive gate bias along channel layer of the conventional and T-Gate TFTs with different T_{vac} and L_{vac}.

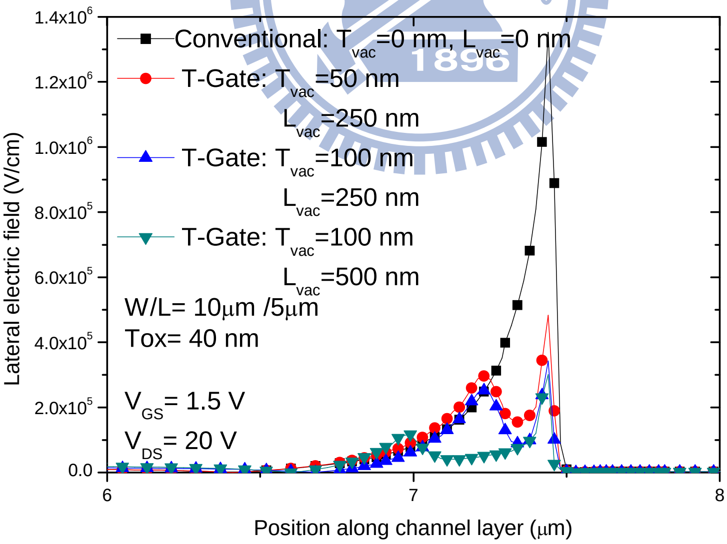


Fig. 2-3(b) The vertical electric fields under positive gate bias along channel layer of the conventional and T-Gate TFT with different T_{vac} and L_{vac}.

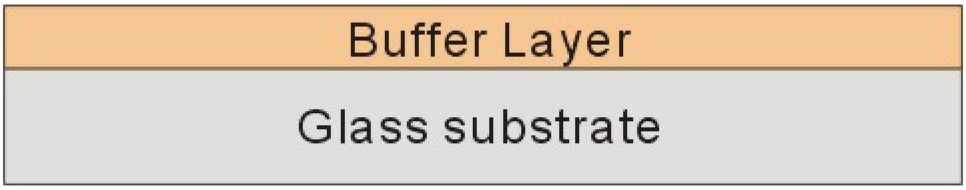


Fig. 2-4 (a) Buffer layer deposition on the glass substrate

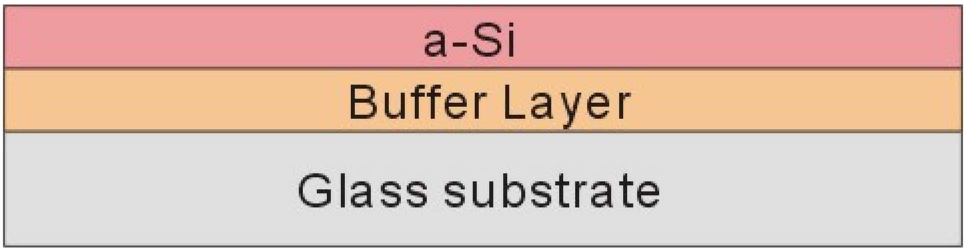


Fig. 2-4 (b) Amorphous Silicon layer deposition by PECVD system

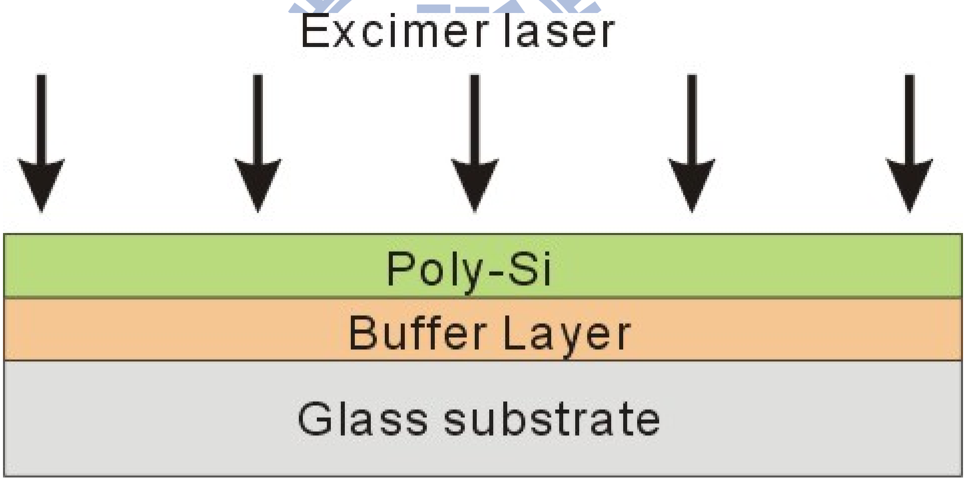


Fig. 2-4 (c) Crystallization of the amorphous-Si film using excimer laser irradiation

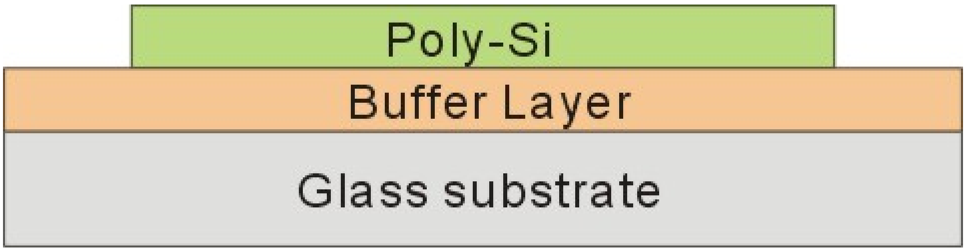


Fig. 2-4 (d) Definition of active region

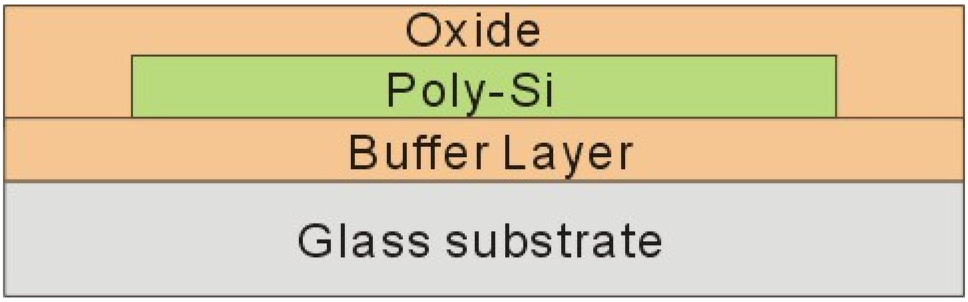


Fig. 2-4 (e) Gate oxide deposition by PECVD system at 300°C

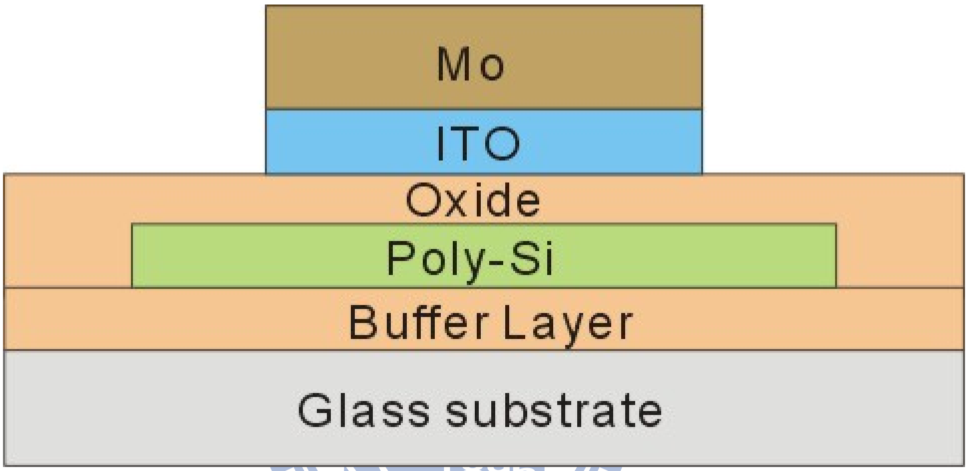


Fig. 2-4 (f) The stacked ITO/Mo layer deposition followed by patterning as the gate electrode

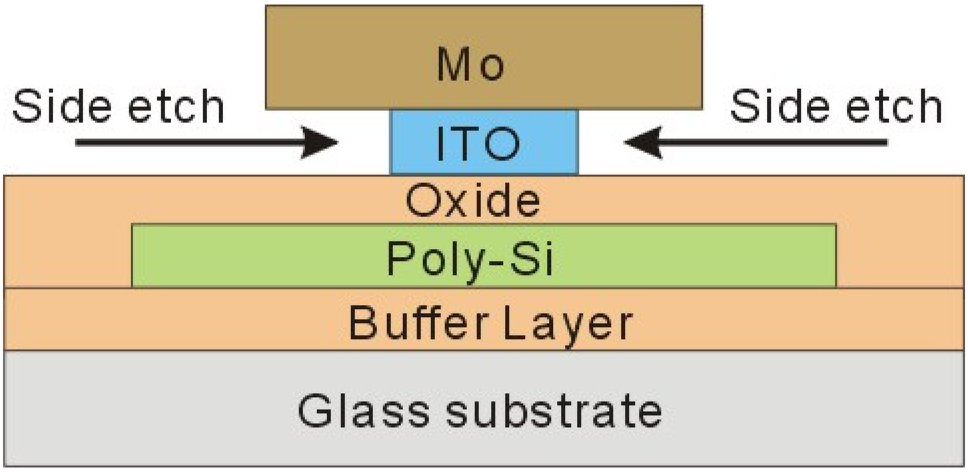


Fig. 2-4 (g) Selective side etching of the ITO layer to form the T-shape gate electrode structure

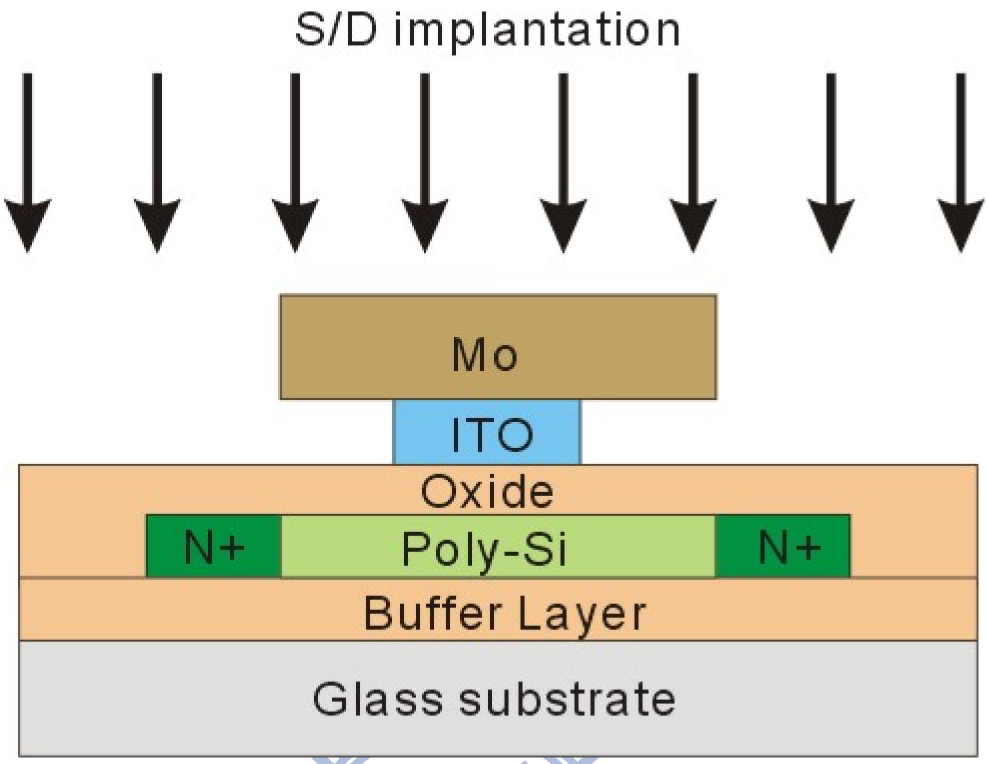


Fig. 2-4 (h) Self-aligned source and drain implantation to form source and drain region

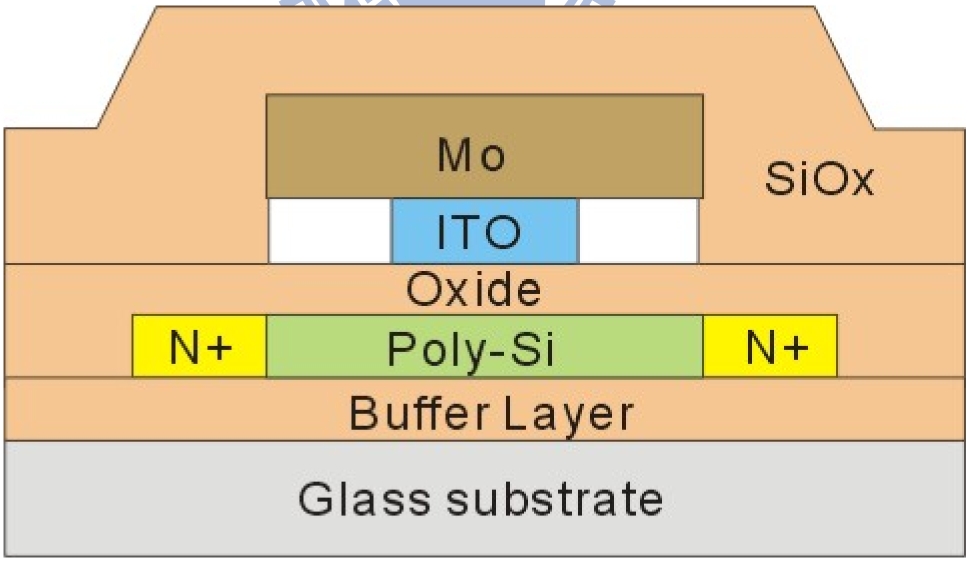


Fig. 2-4 (i) Silane-base SiO_x passivation layer deposition by PECVD system resulting in the in-situ vacuum gaps and then dopant activation by RTA system

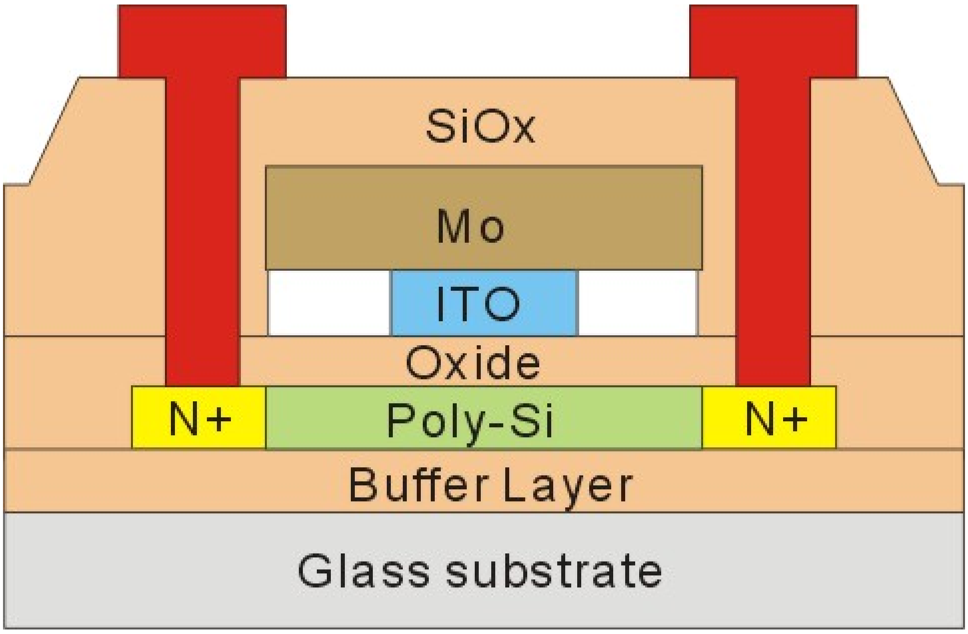


Fig. 2-4 (j) Contact-hole opening and metallization

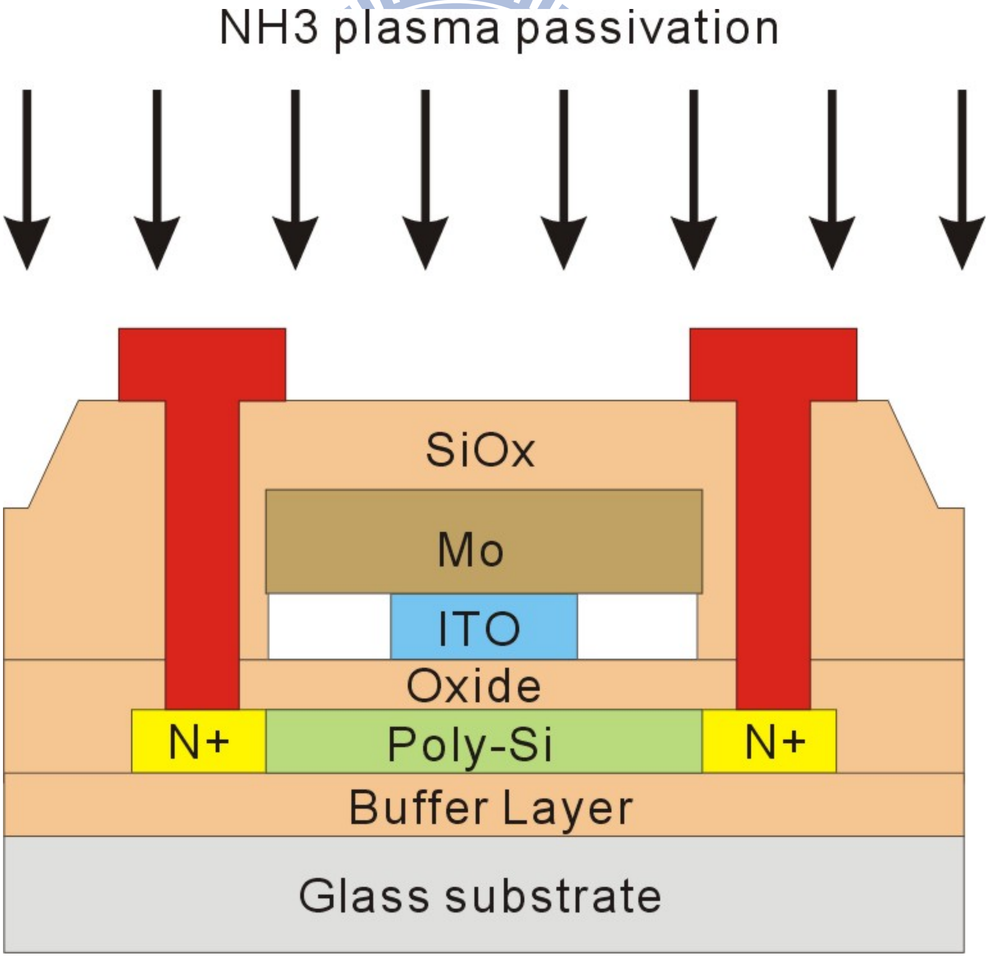


Fig. 2-4 (k) NH_3 plasma passivation

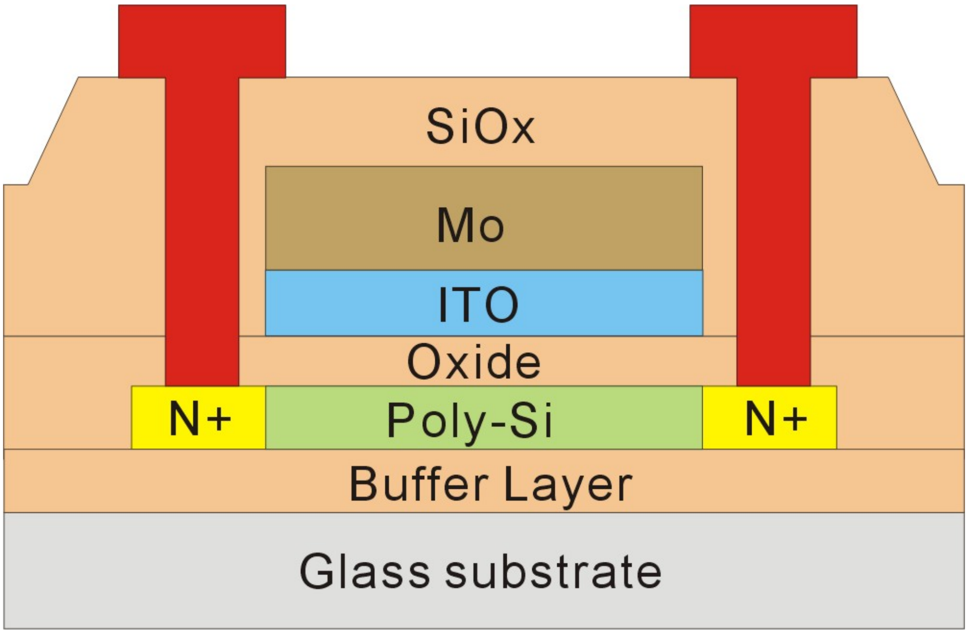


Fig. 2-4(l) The conventional structure

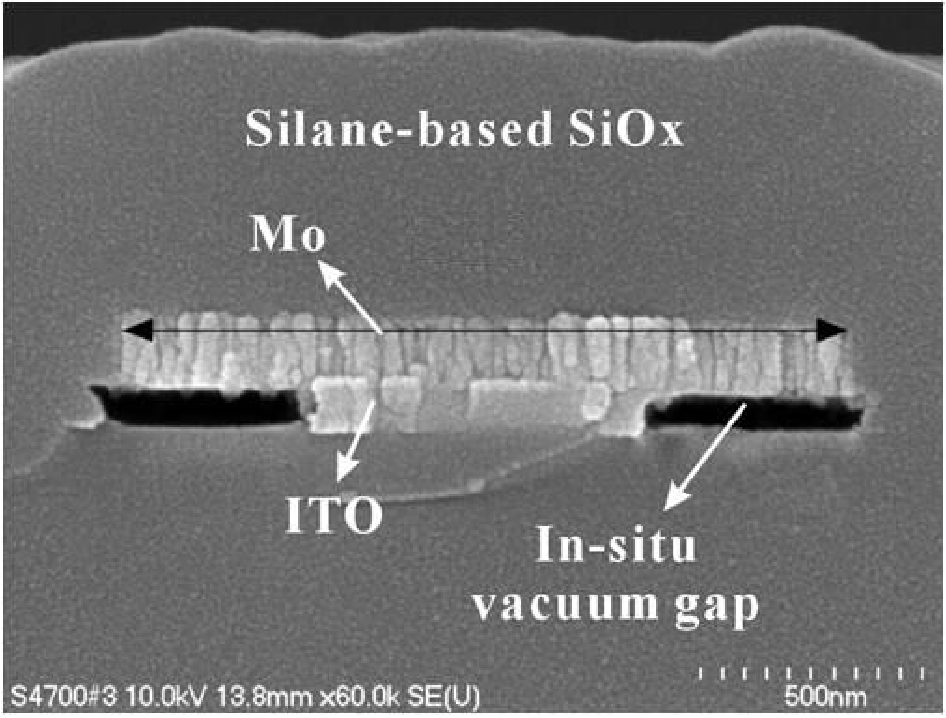


Fig. 2-5 The SEM image of the fabricated T-Gate structure.

($T_{vac} = 100$ nm, $L_{vac} = 500$ nm)

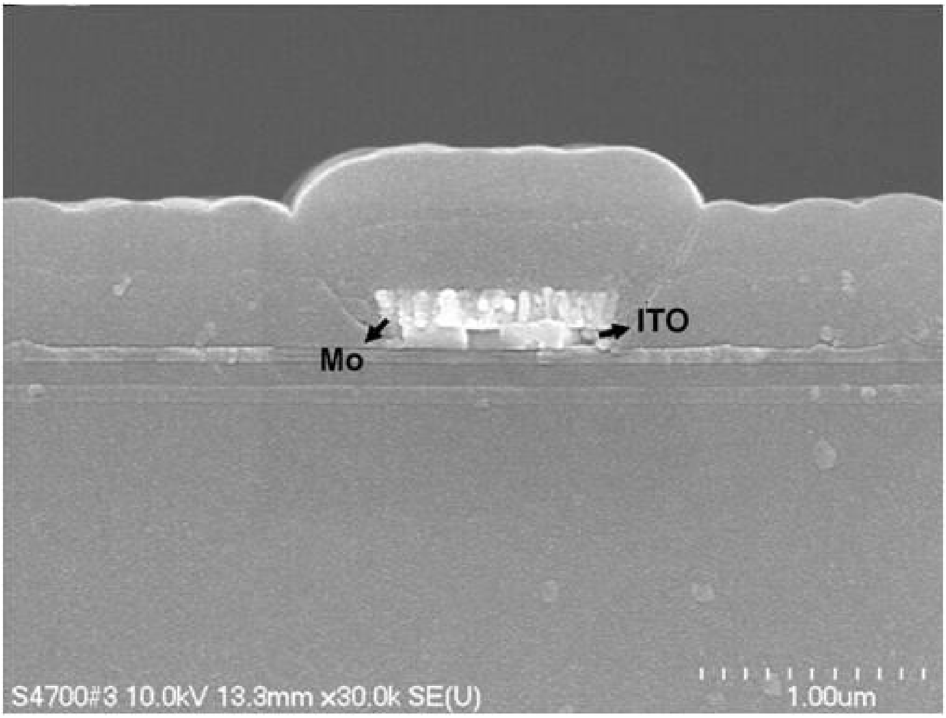


Fig. 2-6 The SEM image of the conventional gate electrode structure. (T_{vac} = 0 nm, L_{vac} = 0 nm)

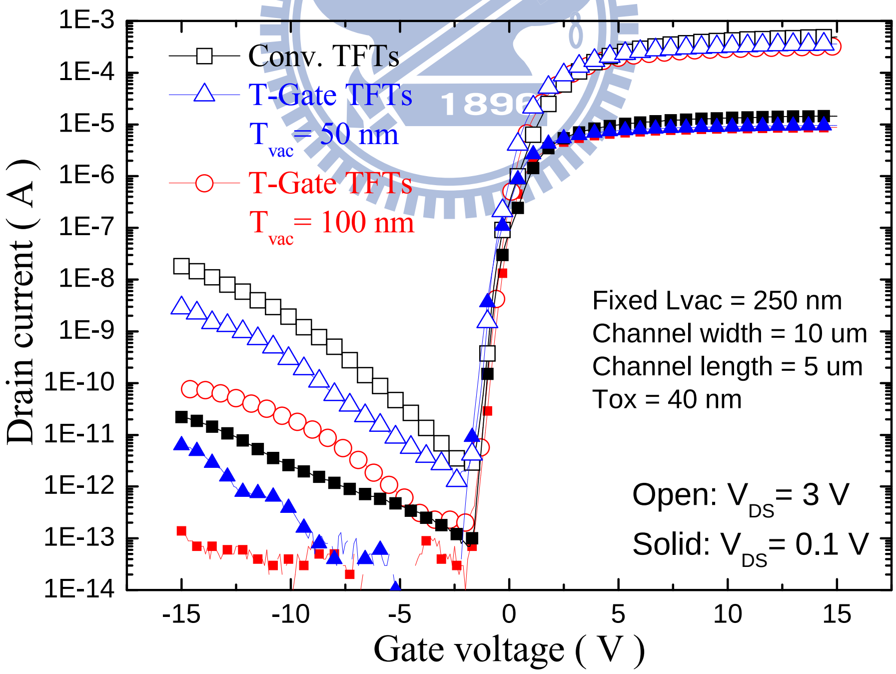


Fig. 2-7 Transfer Characteristics of T-Gate LTPS TFTs with different T_{vac} and fixed L_{vac}, in which channel length is 5 µm, channel width is 10 µm, and the thickness of gate oxide is 40 nm.

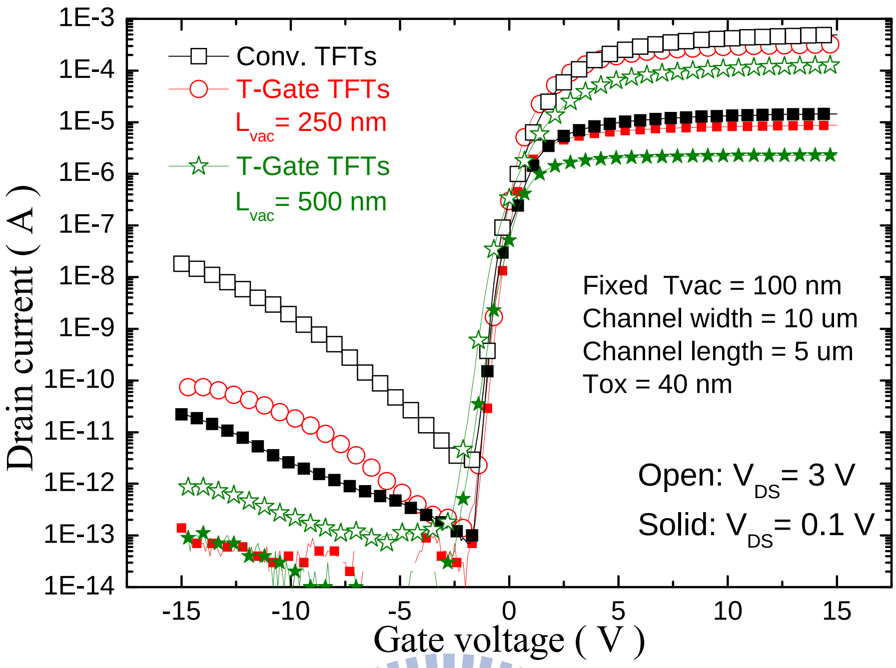


Fig. 2-8 Transfer Characteristics of T-Gate LTPS TFTs with different L_{vac} and fixed T_{vac}, in which channel length is 5 μm, channel width is 10 μm, and the thickness of gate oxide is 40 nm.

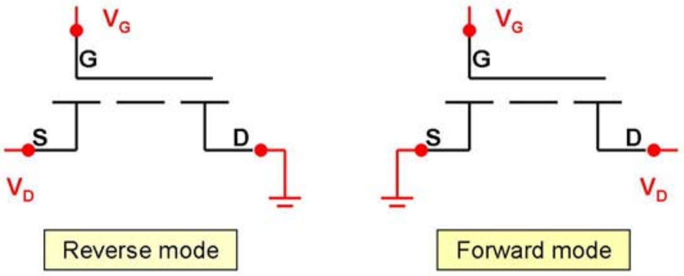


Fig. 2-9 The schematic illustration of the forward mode and reverse mode measurement.

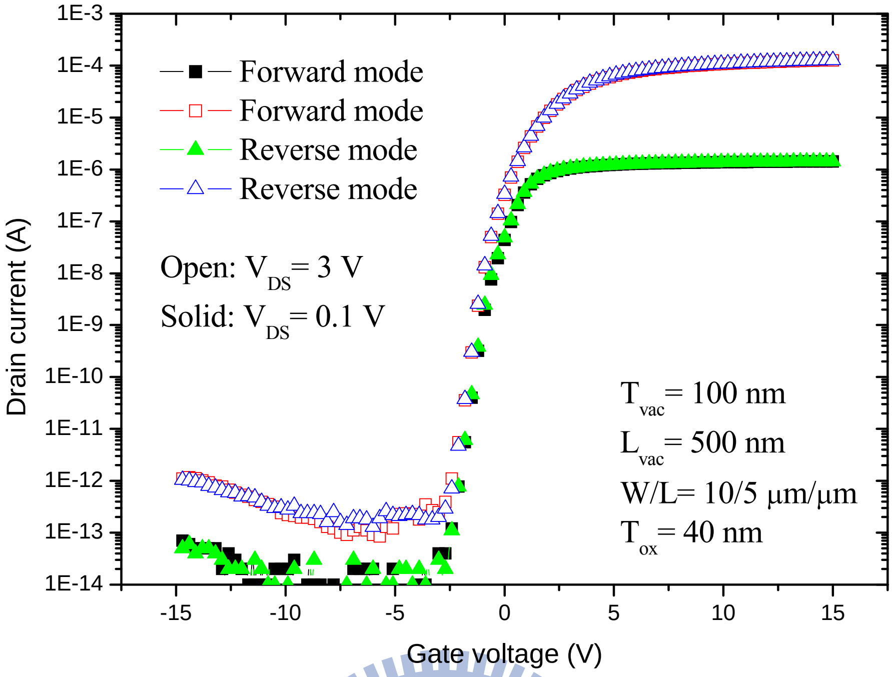


Fig. 2-10 Symmetry transfer characteristics of T-Gate TFTs (T_{vac} = 100 nm and L_{vac} = 500 nm)

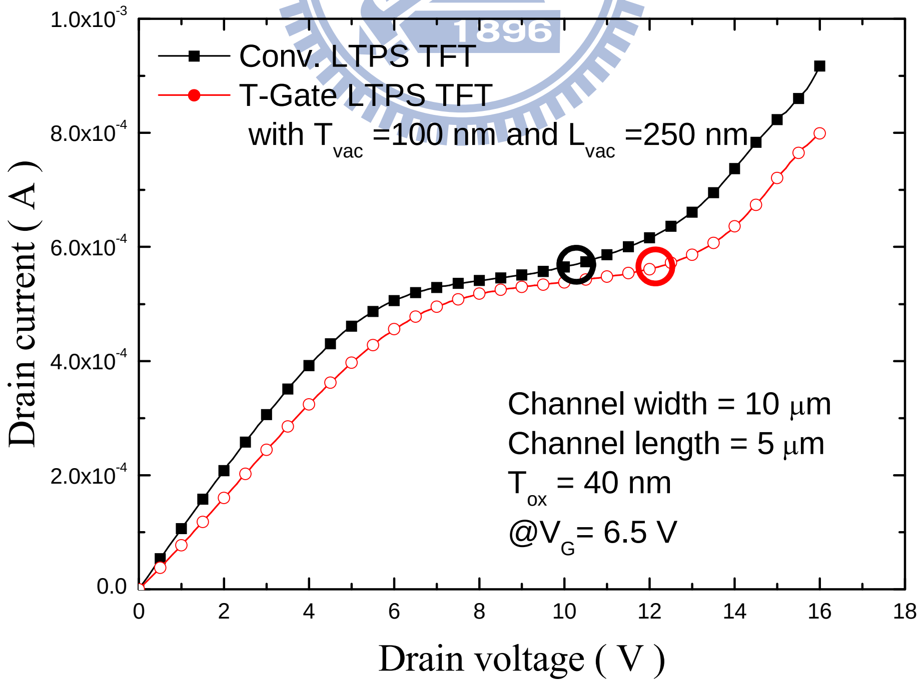


Fig. 2-11 Output characteristics of conventional and T-Gate LTPS TFTs, in which channel length is 5 μm, channel width is 10 μm, and the thickness of gate oxide is 40 nm.

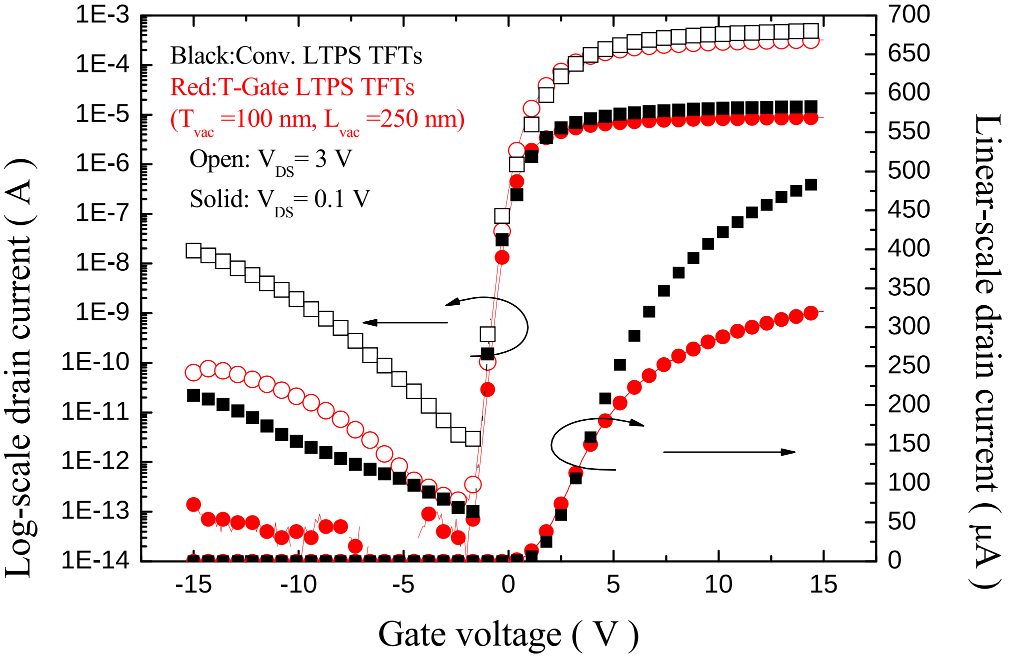


Fig. 2-12 Transfer characteristics of T-Gate LTPS TFTs with channel length of 5 μm and channel width of 10 μm, in which the thickness of gate oxide is 40 nm.

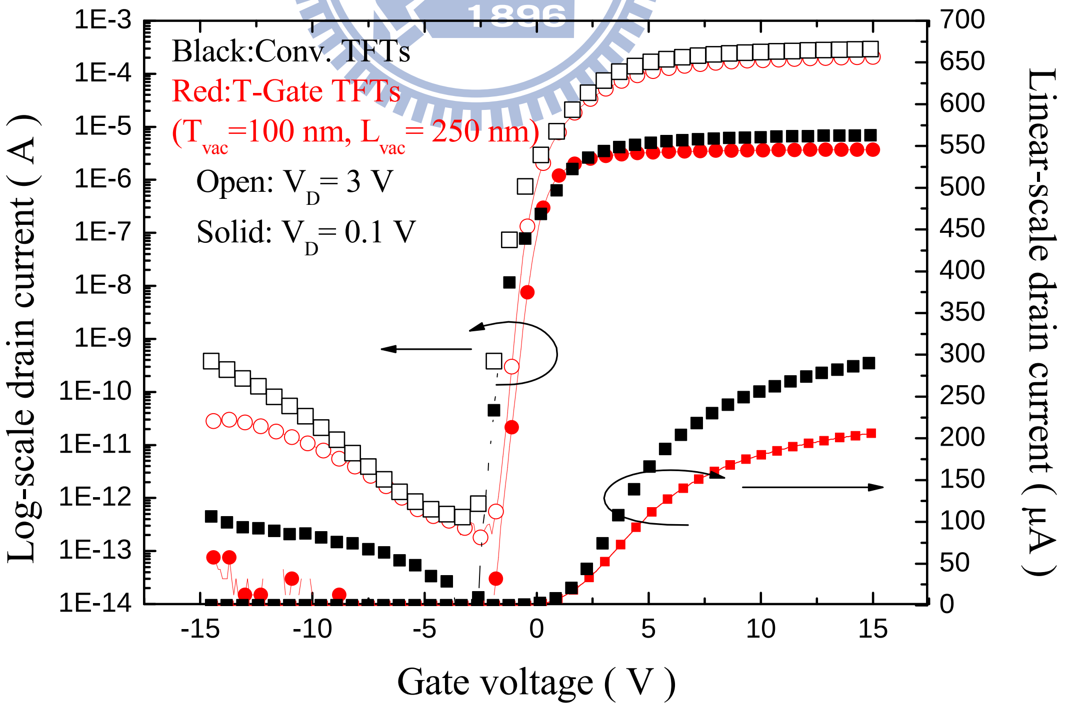


Fig. 2-13 Transfer characteristics of T-Gate LTPS TFTs with channel length of 5 μm and channel width of 10 μm, in which the thickness of gate oxide is 80 nm.

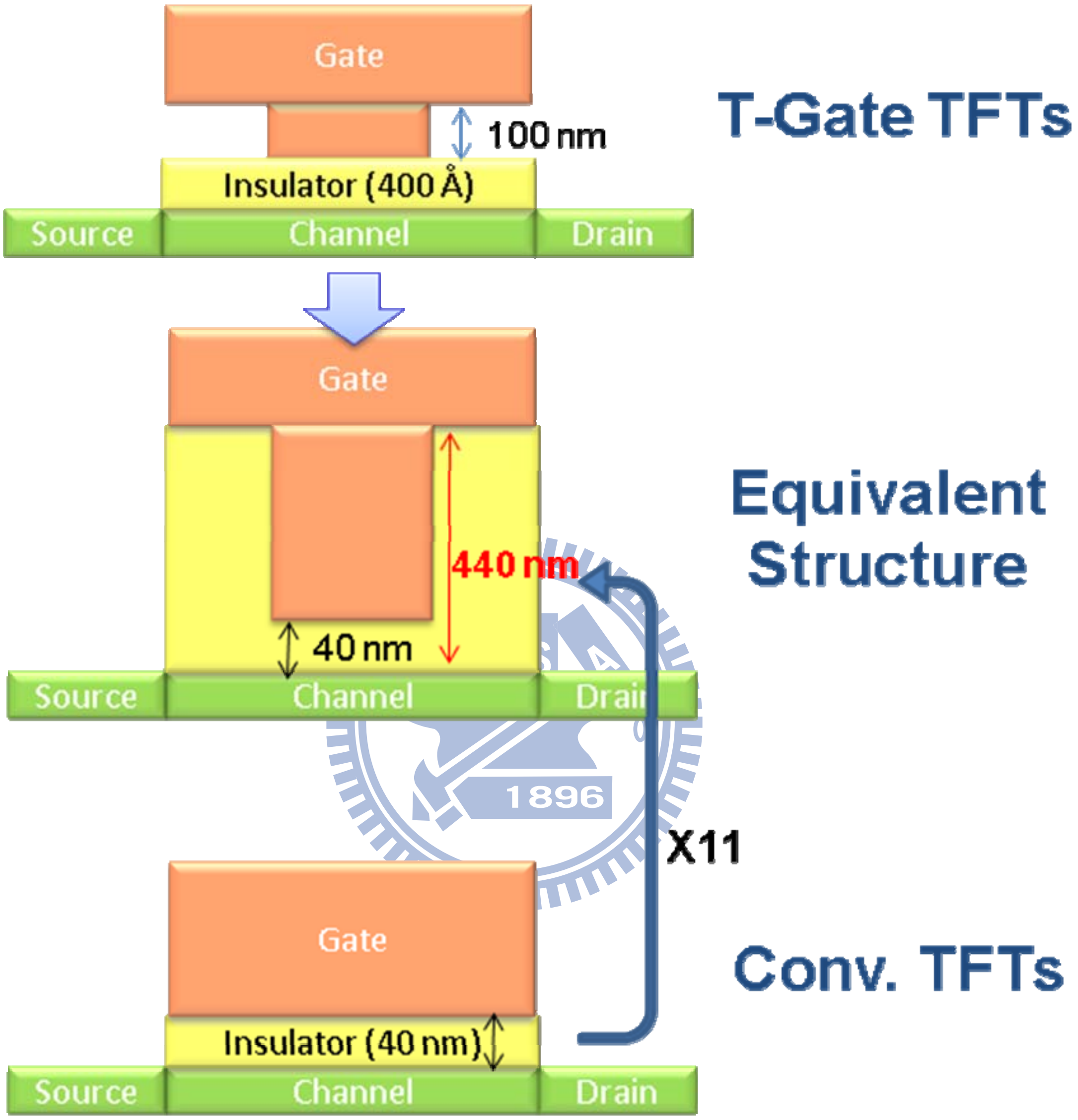


Fig. 2-14 The schematic illustration of the equivalent structure of T-Gate TFTs compared to conventional TFTs in which the thickness of gate oxide is 40 nm.

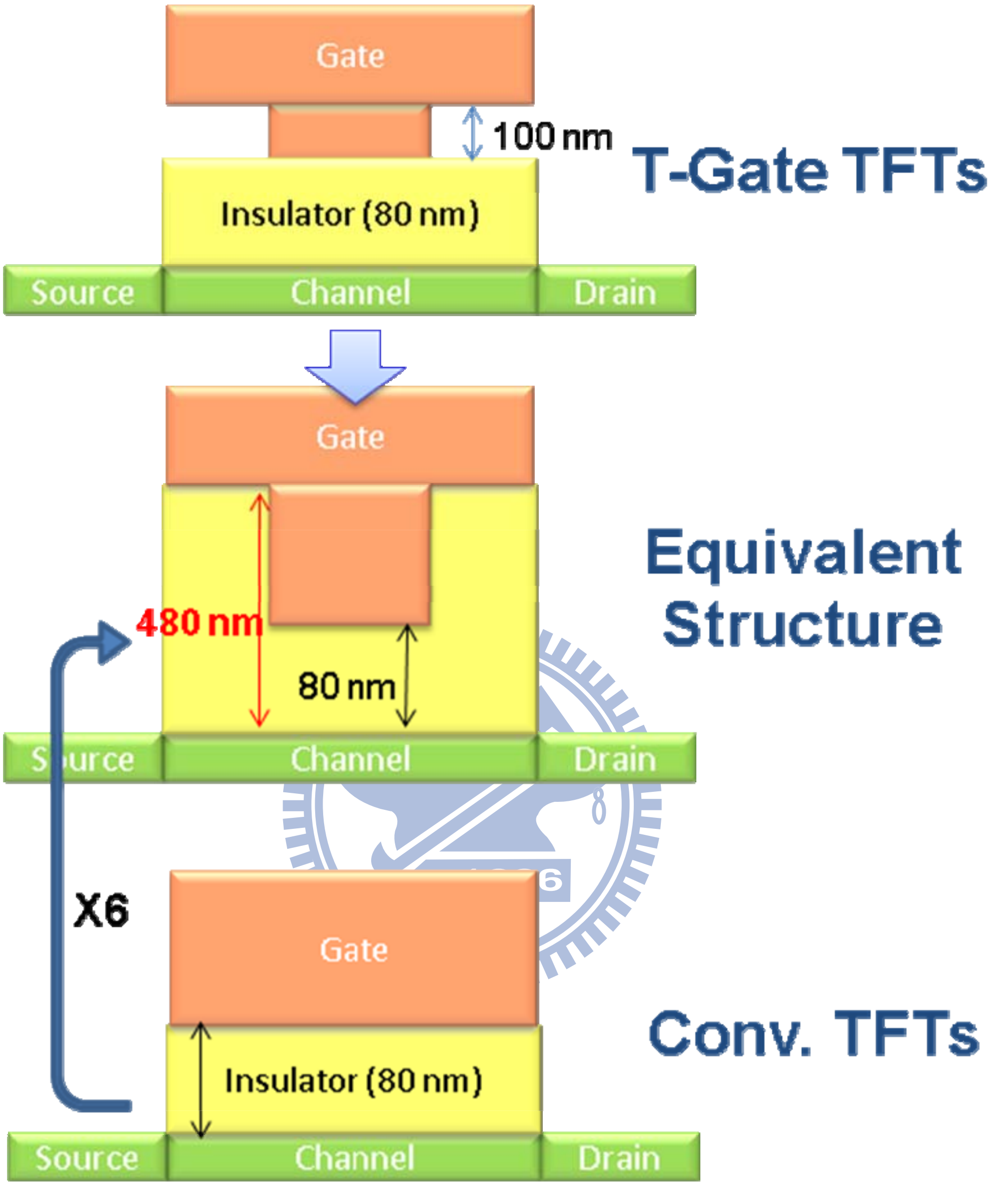


Fig. 2-15 The schematic illustration of the equivalent structure of T-Gate TFTs compared to conventional TFTs in which the thickness of gate oxide is 80 nm.

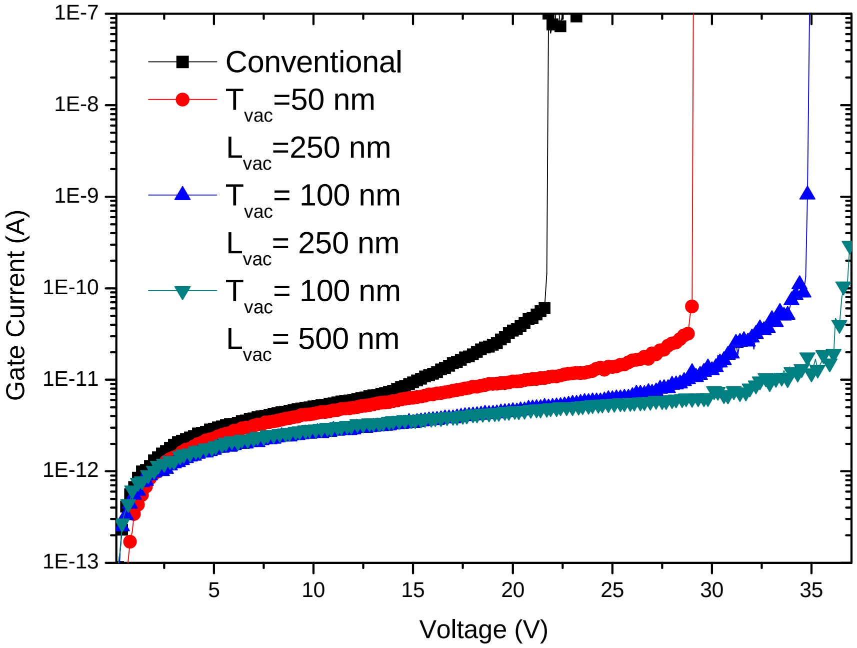


Fig. 2-16 Gate oxide breakdown characteristics of various T-Gate and conventional TFTs.

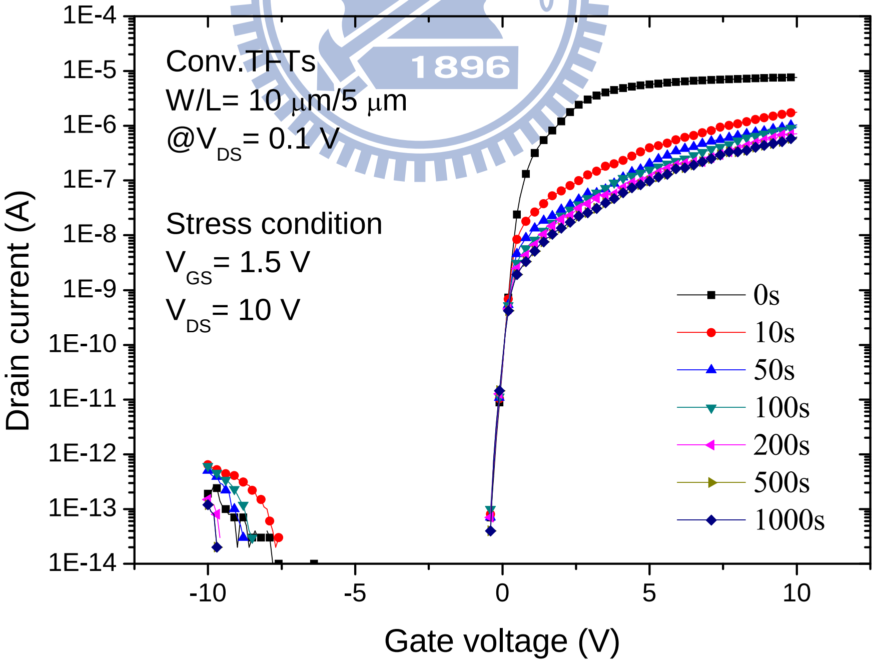


Fig. 2-17(a) Degraded transfer characteristics of the conventional TFTs before and after drain avalanche hot carrier stress at V_{DS} = 10 V and V_{GS} = 1.5 V from 0 to 1000 seconds.

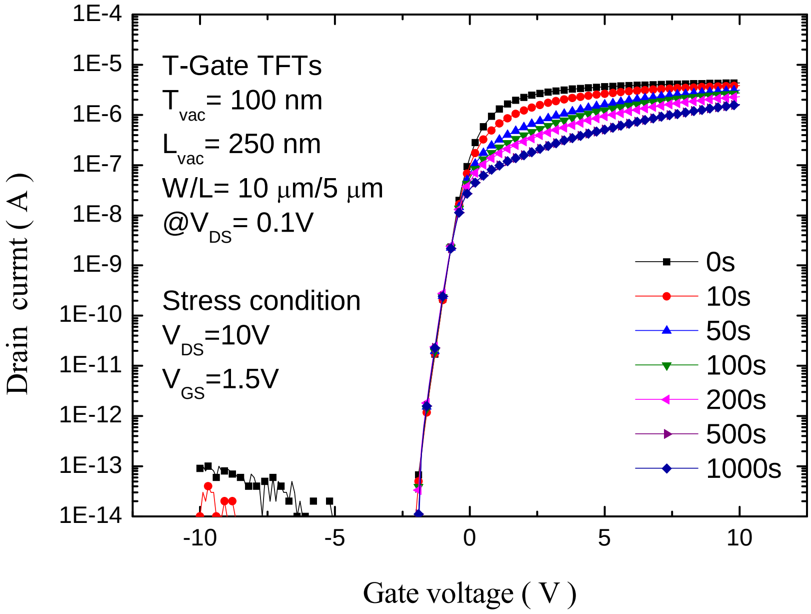


Fig. 2-17(b) Degraded transfer characteristics of the T-Gate TFTs (T_{vac}=100 nm, L_{vac}=250 nm) before and after drain avalanche hot carrier stress at V_{DS} = 10 V and V_{GS} = 1.5 V from 0 to 1000 seconds.

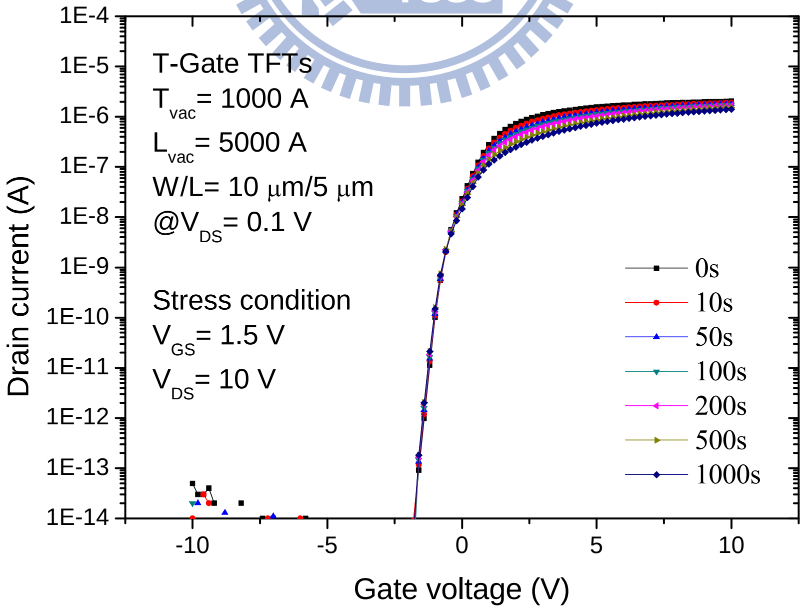


Fig. 2-17(c) Degraded transfer characteristics of the T-Gate TFTs (T_{vac}=100 nm, L_{vac}=500 nm) before and after drain avalanche hot carrier stress at V_{DS} = 10 V and V_{GS} = 1.5 V from 0 to 1000 seconds.

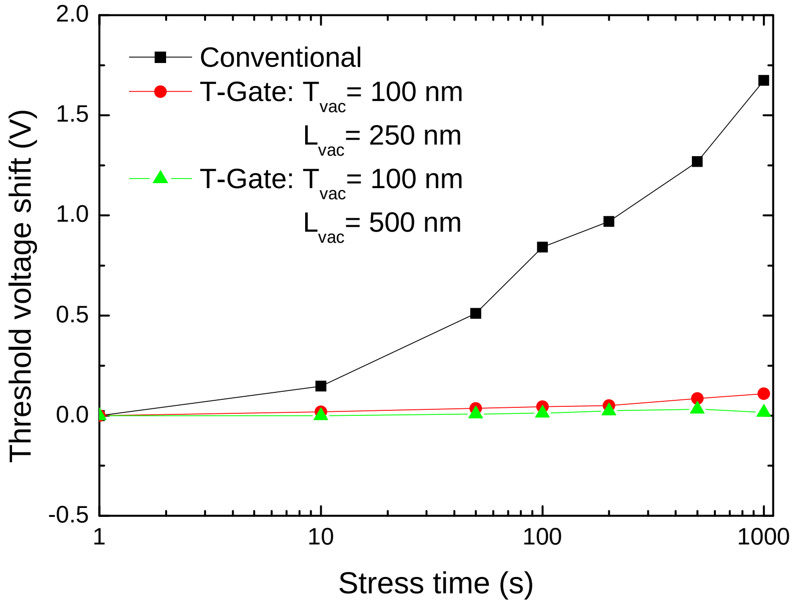


Fig. 2-18(a) Threshold voltage shift of T-Gate and conventional TFTs after drain avalanche hot carrier stress at V_{DS} = 10 V and V_{GS} = 1.5 V from 0 to 1000 seconds.

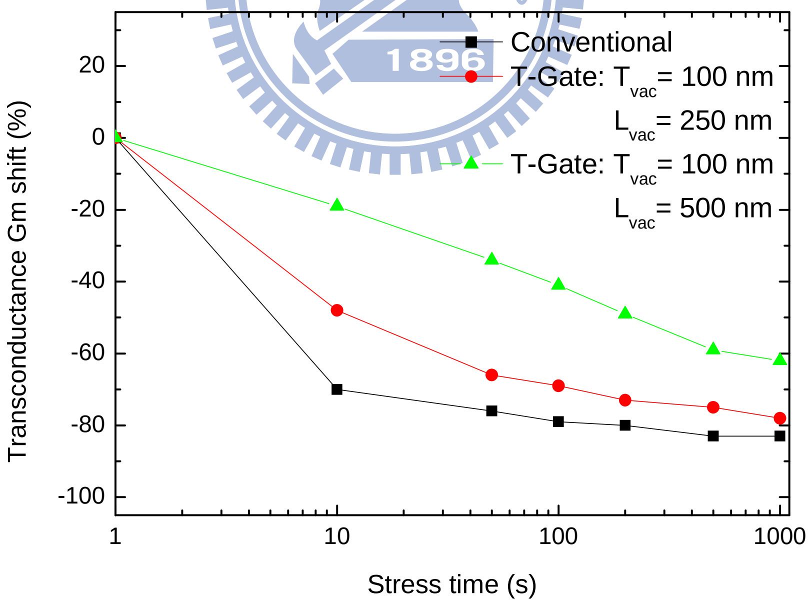


Fig. 2-18(b) Transconductance shift of T-Gate and conventional TFTs after drain avalanche hot carrier stress at V_{DS} = 10 V and V_{GS} = 1.5 V from 0 to 1000 seconds.

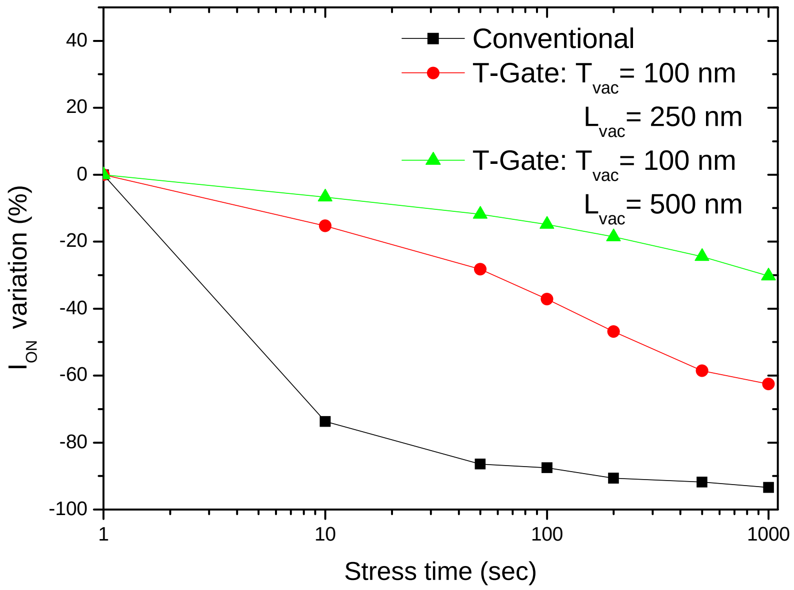


Fig. 2-18(c) I_{ON} variation of T-Gate and conventional TFTs after drain avalanche hot carrier stress at $V_{DS} = 10$ V and $V_{GS} = 1.5$ V from 0 to 1000 seconds.

Chapter 3

Novel Gate-All-Around Polycrystalline Silicon Thin Film Transistors with Multiple Nanowire Channels

3.1 Introduction

Low-temperature polycrystalline silicon thin film transistors (LTPS TFTs) have been widely used as switching elements in active matrix displays. For the further SOP and 3D circuit applications with high versatile circuits and systems integration, there is a need to scale down poly-Si TFTs' device geometries to achieve higher speeds and packing densities [3.1], [3.2]. Unfortunately, it has been shown that conventional planar short-channel poly-Si TFTs suffer from several undesirable SCEs in the electrical characteristics, including threshold-voltage (V_{th}) roll-off, poor subthreshold swing (SS), and large drain-induced barrier lowering (DIBL) which greatly retard their applications [3.3], [3.4]. Recently, for single-crystalline-Si MOSFETs, lots of efforts on non-planar device structures have been developed for better gate electrostatic control of the channel potential, such as double-gated, triple-gated, Π-gated, Ω-gated, nanowire channel, and GAA [3.5]-[3.9]. Among those, GAA FETs together with the nanowire channel have been reported to be the best structure for extreme geometry scaling [3.7]-[3.9]. It is well-known that the poly-Si TFTs serve more pronounced SCEs than single-crystalline-Si MOSFETs due to the rich defects in poly-Si thin films [3.3], [3.4]. However, few works demonstrated such structures on poly-Si TFTs, [3.10]-[3.12]. In this chapter, the gate-all-around (GAA) poly-Si TFTs with multiple nanowire channels (MNCs), for the first time, are proposed by a simple process sequence to improve the device performance and suppress the SCEs and narrow width effects (NWEs).

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3.2 Experiments

3.2.1 Fabrication Sequence of Gate-All-Around Polycrystalline Silicon Thin Film Transistors with Multiple Nanowire Channels

The fabrication steps of the GAA-MNC poly-Si TFTs are schematically illustrated in Fig. 3-1. At First, a 50-nm-thick Si_3N_4 and a 300-nm-thick SiO_2 served as the etch-stop layer and the sacrificial layer were deposited on the oxidized wafer by the low-pressure chemical vapor deposition furnace (LPCVD) at 780 and 700 ˚C, respectively. The sacrificial SiO_2 layer was patterned as several strips by standard optical lithography and then etched anisotropically with 100 nm in-depth by the reactive ion etching (RIE) to form the step profile as shown in Figs. 3-1(a) and (b) in the tilted and cross-section views, accordingly. After a 100-nm-thick a-Si conformal deposition by LPCVD at 550 ˚C, only the photo-resists (PRs) for the source/drain (S/D) pads were patterned to overlap on the two edges of those oxide strips by standard optical lithography. Subsequently, a reactive ion etch (RIE) with a slow etching rate of 2 nm/sec was used to remove the a-Si; meanwhile, a couple of spacer nanowire channels were *in-situ* resided with a self-aligned manner against the sidewall of each oxide strip and naturally connected to the source/drain (S/D) pads as shown in Figs. 3-1(c) and 3-1(d) in the tilted and cross-section views, respectively. It should be noted that the nano-scale dimension of the nanowire channels can be defined only by controlling the RIE time without any advanced lithography [3.11]-[3.13], as well as the MNCs can be designed with patterning several oxide strips (n strips × 2 wires/strip = 2n wires). After the release of S/D-pad PRs, a solid-phase crystallization at 600 °C in N_2 ambient for 24 hours was performed to transform the a-Si into poly-Si. Then, the unique suspending MNCs were constructed after the dummy oxide-strips were etched out (down to the SiN etch-stop layer) by diluted HF etchant as shown in Figs. 3-1(e) and 3-1(f) in the tilted and cross-section views, respectively. Then, the 25-nm-thick TEOS SiO_2 and the 200-nm of phosphorous *in-situ* doped poly-Si (with a doping level of 5×10^{19} cm^{-3}) were conformally deposited by LPCVD system at 700 and 550 °C as gate insulator and gate electrode, respectively. After gate patterning, a self-aligned phosphorous S/D implantation was performed (as shown in Figs. 3-1(g) and 3-1(h) in the tilted and cross-section views, respectively) and a 300-nm-thick passivation oxide layer was deposited, followed by an activation at 600 °C in N_2 ambient for 10 hours. Contact opening formation, metallization, and NH_3-plasma passivation for 1 hour at 300 °C was carried out [3.14]. For the purpose of comparison, the conventional planar (CP) poly-Si TFTs were also fabricated with the same process run.

3.2.2 Material Analyses for Gate-All-Around Poly-Si TFTs with Multiple Nanowire Channels

Figs. 3-2(a) and 3-2(b) display the SEM images before and after the removal of oxide strips by HF acid, respectively. And, Figs. 3-2(c) and 3-2(d) show their corresponding schematic images. Fig. 3-3(a) further demonstrates the tiled-view SEM image of the multiple nanowire channels after HF etching. The corresponding process schematic image is demonstrated in Fig. 3-3(b). It shows clear that the suspending spacer nanowire channel was braced by S/D pads, and an empty space was between the suspending nanowire channel and the etch-stop SiN layer. Different channel width can be easily designed by adjusting the number of SiO_2 strips. The structure of suspending channels is displayed in the cross-section view in the SEM image of Fig. 3-4(a). The corresponding process step is demonstrated in Fig. 3-4(b). The multiple nanowire channels are suspended in the air with a height of 200 nm above the Si_3N_4 etch-stop layer and joined to the source and drain pads. With the aid of the suspending nanowire channels, the gate oxide and gate electrode deposited by LPCVD can surround the channel to form the GAA structure. Fig. 3-5(a) shows the top view SEM graph after patterning gate. The corresponding process step is demonstrated in Fig. 3-5(b). The multiple channels are surrounded by *in-situ* doped poly gate. Fig. 3-6 shows its corresponding tilted-view SEM graph.

Fig. 3-7 shows the cross-sectional transmission electron microscopy (TEM) image of each GAA-MNC, the good step-coverage is observed on GAA structure both for TEOS gate oxide and phosphorous *in-situ* doped poly gate, and the vertical sidewall thickness (T_{Fin}), the horizontal width (W_{Fin}) and the bevel length of each nanowire channel are about 85, 85, and 130 nm, respectively. Thus the total surrounding width of each nanowire channel is 300 nm. The aspect ratio T_{Fin}/W_{Fin} of each nanowire channel in GAA-MNC TFT (approximately equals to one) is much larger than that in CP TFT and thus features like a fin structure [3.6], [3.14].

3. 3 Results and Discussion

3.3.1 Electrical Characterization of Gate-All-Around Poly-Si TFTs with Multiple Nanowire Channels

It should be noted that the channel width of GAA-MNC TFT is defined as 0.6n μm, where the n is the designed number of oxide strip. That is, W = n strips × 2 wires/strip × 300 nm/wire = 0.6n μm. The surrounding width of each nanowire channel is 300 nm as shown in Fig.3-7. The subthreshold swing (SS) is determined from the subthreshold region of I_{DS}-V_{GS} curve at V_{DS} = 0.1 V.

In this section, devices with channel length of 2 μm and channel width of 3 μm are characterized, where the W of GAA-MNC TFTs are defined by 5-oxide-strip structure (i.e. 5 strips × 2 wires/strip × 300 nm/wire = 3 μm).

Fig. 3-8 demonstrates the comparison of transfer characteristics between GAA-MNC and conventional TFTs, while the comparison of output characteristics is demonstrated in Fig. 3-9. Those figures display that the GAA-MNC TFTs exhibit excellent electrical performance as compared to conventional TFTs. The mobility increases from 26 to 33 cm^2/V-s, the threshold voltage V_{th} decreases from 2.31 to 1.31 V, the subthreshold swing (SS) decreases from 0.64 to 0.37 V/decade, minimum I_{Off} decreases from 3.69×10^{-12} to 3.33×10^{-13} A, maximum I_{ON} increases from 3.81×10^{-5} to 4.17×10^{-5} A, I_{On}/I_{Off} increases from 1.03×10^{7} to 1.25×10^{8}, and DIBL decreases from 0.29 to 0.04 V/V.

In the subthreshold and on-state region, the GAA-MNC TFTs demonstrate lower threshold voltage (V_{th}), lower DIBL, stepper subthreshold swing (SS), higher on current, and higher mobility. These performance improvements can be explained by the effects of surrounding gate, sharp corner, and nano-scale dimension.

I. Surrounding-Gate Effect

Gate-all-around transistors have been reported to significantly enhance gate controllability [3.14]. With the multiple gates, the channel potential can be effectively controlled. Thus, the GAA-MNC TFTs can turn on easily and result in shaper subthreshold swing, lower threshold voltage, and higher mobility [3.20]-[3.21]. Also, the higher gate electric field can suppress the lateral electric field in drain and reduce the influence caused from drain bias such as DIBL and kink effects.

II. Sharp Corner Effect

The three sharp corners in such nanowire further enhance the gate electric field and then provide more inversion carriers during on state. This phenomenon is further explained by a simulated analysis of ISE-DESSIS. Fig. 3-10 shows the cross-section simulation of GAA-MNC TFTs. It shows that the three sharp corners inverse more electrons than other region, the electron density increase from 10^{18} to 10^{20} cm^{-2}.

III. Nano Dimension

Fewer intra- and inter- grain defects exist in the nanowire channels owing to the high surface-to-volume ratio and small volume of nanowire body in the GAA-MNC TFTs. The higher surface-to-volume ratio indicates that the GAA-MNC TFTs have less volume defects than conventional TFTs in the same surface width.

The leakage currents of GAA-MNC and conventional TFTs are specifically shown in Fig. 3-11. In the off-state region, the mechanisms of leakage current can be explained under three different gate-bias regions. The leakage current mechanisms are displayed in Fig. 3-12. In low electric field region, the electrons are thermally excited from the valence band into the trap states and then jumping into the conduction band. The phenomenon is called thermionic emission which contributes the low electric field off-state leakage current. The number of excited electrons in thermionic emission strongly depends on the quantity of the defects and traps in channel.

In medium electric field region, the electrons are thermally excited from the valence band into the trap states and then tunneling into the conduction band by the gate-drain electric field. This mechanism is known as thermionic-filed emission and depends on both the trap states and electric field.

In high electric field region, the band diagram is bent strongly under high gate-drain electric field in the gate/drain overlapped region. The electrons tunnel directly from the valence band to the conduction band. This is called as the band-to-band tunneling and cause high leakage current in gate-drain junction which is also known as gate-induced drain leakage (GIDL). The GIDL current highly depends on the gate-to-drain electric field and becomes more serious with the assistance of traps.

The GAA-MNC TFTs shows lower leakage current at the low gate electric field region as compared to conventional TFTs. It is because there is less volume defects in GAA-MNC TFTs' channel resulting in the reduction of thermionic emission. However, at the high gate electric field region, the GIDL current is more significant in the GAA-MNC TFTs. The higher GIDL current comes from the higher gate electric field as a result of surrounding gate and sharp corners. The related simulation results are shown in Fig. 3-13, the electric field in the three sharp corners is much higher than other regions. The higher gate leakage current also been observed in GAA-MNC TFTs because higher electric field in the three sharp corners as shown in Fig. 3-14.

3.3.2 NH_3 Plasma Passivation

Unlike single-crystalline silicon (c-Si), poly-Si is rich in grain boundary defects and intra-grain defects, and the electrical activity of these charge-trapping centers profoundly affects the electrical characteristics of poly-Si TFTs. The turn-on characteristics, including threshold voltage, subthreshold swing, and mobility, of poly-Si TFTs are much inferior to those of c-Si devices due to the fullness of defect states in the device channel region. Moreover, the density of defects in poly-Si film fabricated by low-temperature solid phase crystallization is much high. If there are more defects in channel, larger gate voltage is required to fill the greater number of traps to turn on. Carrier mobility is degraded by scattering with charge-trapping centers and surmounting the potential barrier height which is built by charged traps. It has been reported the NH_3 plasma treatment can improve the characteristics of poly-Si TFTs [3.24]. The hydrogen and nitrogen can passivate the dangling bonds in grain boundary and pile up at the SiO_2/poly-Si interface.

Fig. 3-15 exhibits the comparison of transfer characteristics between the GAA-MNC TFTs with and without 1-hour NH_3 plasma treatment, while the comparison of output characteristics is exhibited in Fig. 3-16. For comparison, the characteristics of conventional TFTs also demonstrate in Figs. 3-17 and 3-18. The major parameters are listed in Table 3-1. After NH_3 plasma treatment, the GAA-MNC and conventional TFTs reveal higher on current, higher mobility, steeper subthreshold swing and lower threshold voltage. The defects are passivated after NH_3 plasma treatment, so the performances of GAA-MNC and conventional TFTs are improved. The GIDL currents of GAA-MNC and conventional TFTs decrease more than one order and the kink effect happens later at higher drain voltage. The kink effect and GIDL current are both related to the density of traps in active region and high electric field at the drain junction. The non-ideal increased current is suppressed when the dangling bonds are tied to the hydrogen and nitrogen. It is observed that the improvement of mobility in the GAA-MNC TFTs is higher than in conventional ones. That is because NH_3 plasma passivation in multi-channel TFTs is more efficient than conventional single-channel TFTs as the exposed surface is increased [3.25].

3.4 Dimensional Scalability

Recently, poly-Si TFTs are attractive for their applications on active-matrix displays, such as pixel switches, drivers, and peripheral control circuit [3.26], [3.27]. For these applications, scaled-down LTPS TFTs with high performance are much required. The scaled-down devices enable higher circuit density in SRAMs and EEPROMs, and increase the driving current and operation speed of peripheral driving circuit in active-matrix applications. The short-channel and narrow-width effects of scaled-down devices are studied in this section.

3.4.1 Short Channel Effects

As the channel length shrank, there are several short-channel effects resulted in device characteristics. First, because the lateral electric field from drain bias becomes larger in short channel, the kink effect and drain-induced barrier lowering (DIBL) become more pronounced. Second, the threshold voltage becomes smaller and this phenomenon is well-known as threshold voltage roll-off. Moreover, the floating-body architecture and charge trapping by defect states result in serious avalanche induced effects in poly-Si TFTs [3.30]. The avalanche-induced effects become more severe as the TFT dimension is reduced due to the enhancement of impact ionization caused by the increasing electric field. Therefore, lot severe short-channel effects are shown in poly-Si TFTs as compared to the single-crystalline Si transistors.

Figs. 3-19 and 3-20 show the normalized transfer characteristics of the GAA-MNC TFTs and conventional top gate TFTs, respectively. Those devices have the fixed channel width (W) of 3 μm and various channel length (L) from 1 to 5 μm. Obviously, the conventional TFTs show serious threshold voltage roll-off. The threshold voltage is extracted from normalized transfer characteristics and compared in Fig. 3-21. In conventional TFTs, the threshold voltage shifts from 2.88 V to 2 V as decreasing the channel length from 1 to 5 μm. There is negligible threshold voltage roll-off in the GAA-MNC TFTs. The improvement of short-channel effects is attributed to the stronger gate controllability from the GAA structure with multiple nanowire channels.

3.4.2 Narrow Width Effect

As the channel width scaled down, the poly-Si TFTs are reported to show lower threshold voltage [3.31]. In this section, the shifts of threshold voltages between the GAA-MNC and conventional TFTs are compared.

Figs. 3-22 and 3-23 show the normalized transfer characteristics of the GAA-MNC TFTs and conventional top-gate TFTs with various channel widths, respectively. It demonstrates that the threshold voltage decreases with the channel width decreasing in conventional TFTs. As compared to conventional TFTs, the threshold voltage of the GAA-MNC TFTs with various channel width is approaching constant. The threshold voltage is extracted from normalized transfer characteristics and compared in Fig. 3-24. The figure displays that the threshold voltage of conventional TFTs drops significantly as the channel width scaled down to 1μm or less, while there is negligible threshold voltage shift in the GAA-MNC TFTs. The reason is discussed below.

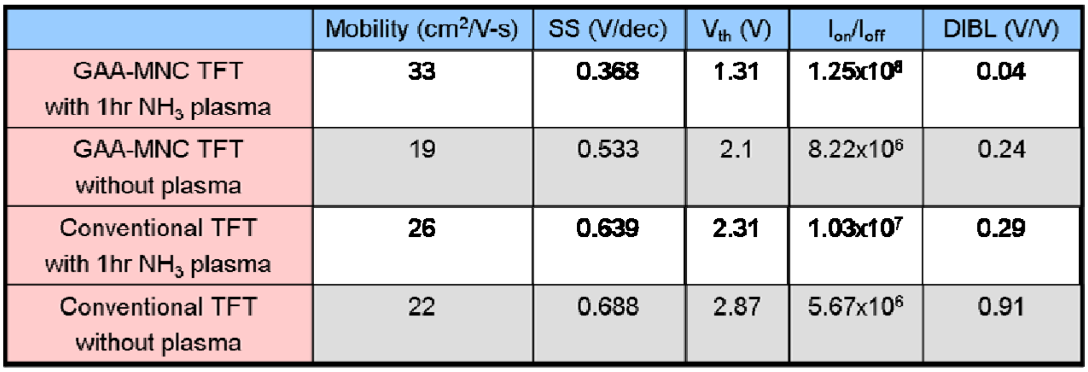
Due to the narrow-dimensional active island, the gate electrode is deposited not only on the surface channel width defined by the designed layout but also the two-side edges of this island. The two-side edges provide additional channel width which is two times of the thickness of the active layer. The edge channels show negligible influence as the channel width is large enough. But, as decreasing the channel width, the edge channels become comparable to the main (surface) channel. In narrow width devices, the edge channels provide additional current and lower the threshold voltage.

3.5 Summary

In this chapter, the gate-all-around poly-Si TFTs with multiple nanowire channels (GAA-MNC TFTs) were fabricated by a simple method. The spacer technique was used to form the multiple nanowire channels without any advanced lithography. The spacer technique was used to form the multiple nanowire channels without any advanced lithography. The GAA-MNC TFTs exhibited excellent electrical characteristics as compared to conventional ones. The mobility increased from 26 to 33 cm^2/V-s, the threshold voltage V_{th} decreased from 2.31 to 1.31 V, the subthreshold swing SS decreased from 0.64 to 0.37 V/decade, minimum I_{OFF} decreased from 3.69×10^{-12} to 3.33×10^{-13} A, maximum I_{on} increased from 3.81×10^{-5} to 4.17×10^{-5} A, I_{on}/I_{off} increased from 1.03×10^{7} to 1.25×10^{8}, and DIBL decreased from 0.29 to 0.04 V/V. Those improvements of the gate controllability of GAA structures could be ascribed to three sharp corners, and less defects in nanowire channels as compared with conventional TFTs. The GAA-MNC TFTs showed lower minimum leakage current at low gate voltage than conventional ones owing to fewer defects. The GAA-MNC TFTs showed higher leakage current at high electric field because the higher gate electric field resulted from surrounding gate and three sharp corners. On the plasma-passivation aspect, the GAA-MNC TFTs exhibited better defect plasma passivation efficiency than conventional TFTs. It can be attributed to multiple nanowire channels increase the exposed surface to NH_3 plasma. The improvement of short-channel effects was attributed to the better gate controllability from the GAA structure and three sharp corners of the nanowire channels. The threshold voltage of GAA-MNC TFTs was consistent with various channel width; while the threshold voltage of conventional TFTs was deceased with narrow channel. It is because the edge channels of conventional TFTs provide additional current and lower the threshold voltage. The superior gate controllability of GAA-MNC TFTs can suppress the high drain electric field at the drain junction which enhances the device reliability. Since the GAA-MNC TFTs exhibited excellent performance, including good electrical characteristics, better NH_3 plasma passivation efficiency and superior scalability, they are very promising for the applications in future SOP and 3-D ICs.

Tables

Table 3-1 Electrical characteristics of gate-all-around TFTs with multiple nanowire and conventional TFTs before and after 1-hour NH_3 plasma passivation.



	Mobility (cm^2/V-s)	SS (V/dec)	V_{th} (V)	I_{on}/I_{off}	DIBL (V/V)
GAA-MNC TFT with 1hr NH_3 plasma	**33**	**0.368**	**1.31**	**$1.25\text{x}10^8$**	**0.04**
GAA-MNC TFT without plasma	19	0.533	2.1	$8.22\text{x}10^6$	0.24
Conventional TFT with 1hr NH_3 plasma	**26**	**0.639**	**2.31**	**$1.03\text{x}10^7$**	**0.29**
Conventional TFT without plasma	22	0.688	2.87	$5.67\text{x}10^6$	0.91

Figures

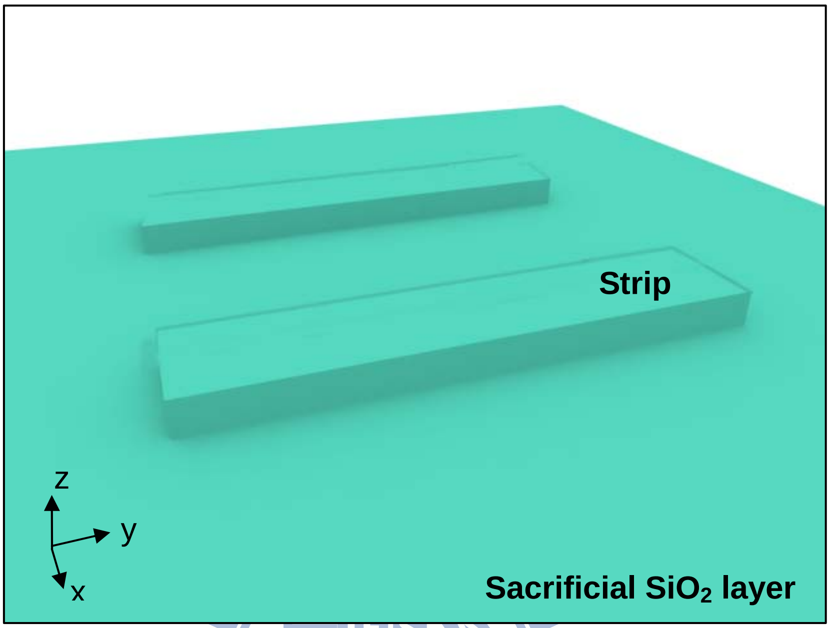


Fig. 3-1(a) The tilted view process step of the strip formation.

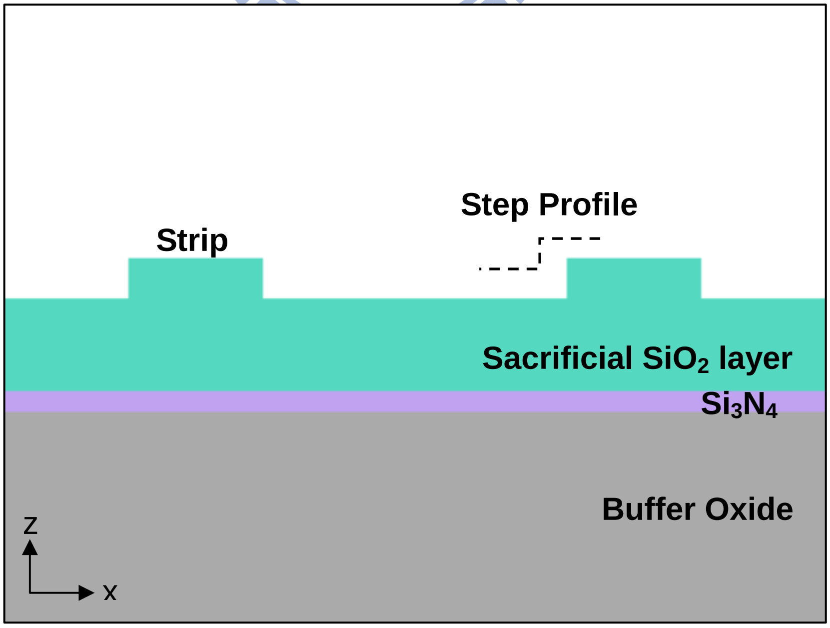


Fig. 3-1(b) The cross-section view step of the strip formation.

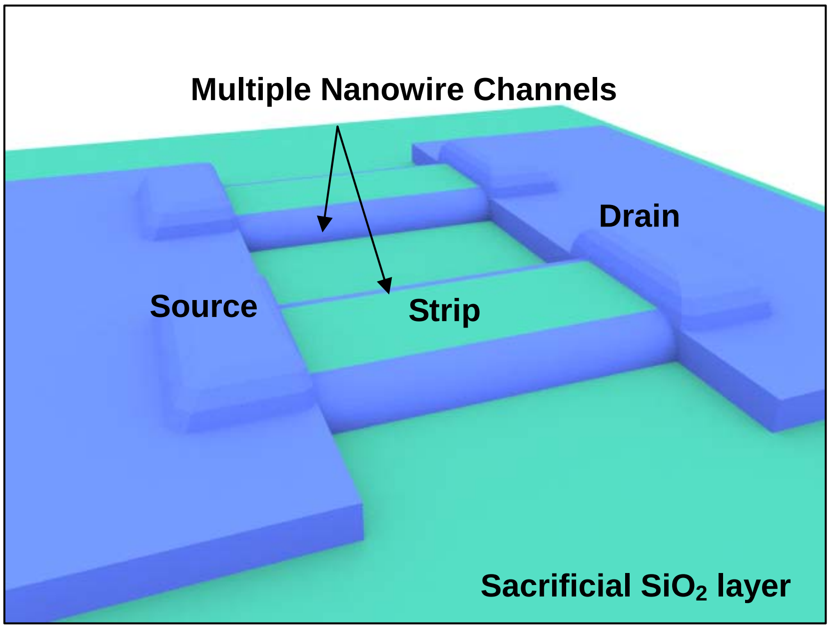


Fig. 3-1(c) The tilted view step of the nanowire-channel formation.

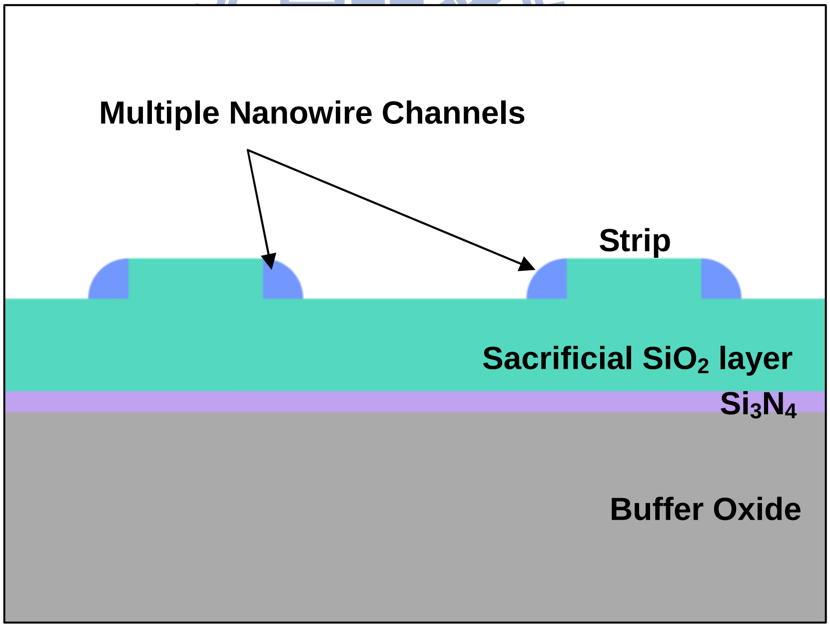


Fig. 3-1(d) The cross-section view step of the nanowire-channel formation.

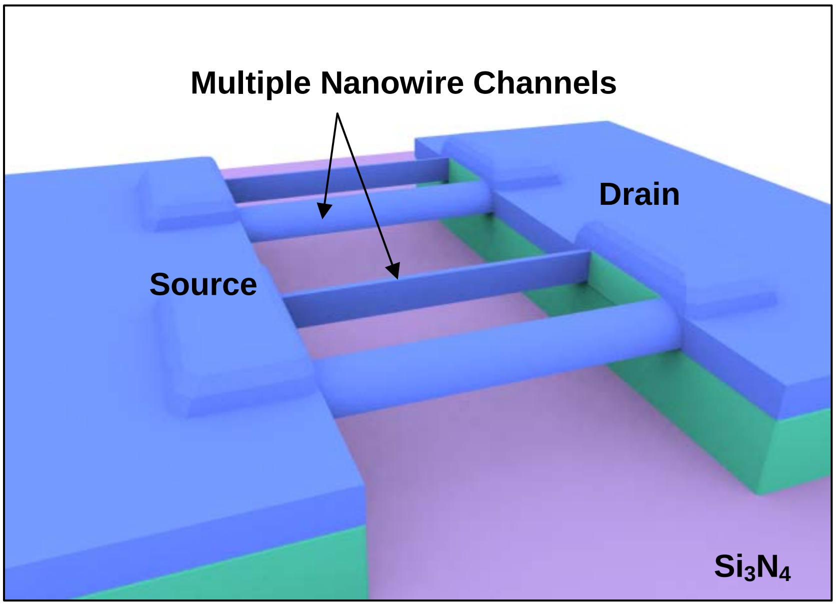


Fig. 3-1(e) The tilted view step of the suspending nanowire-channel formation.

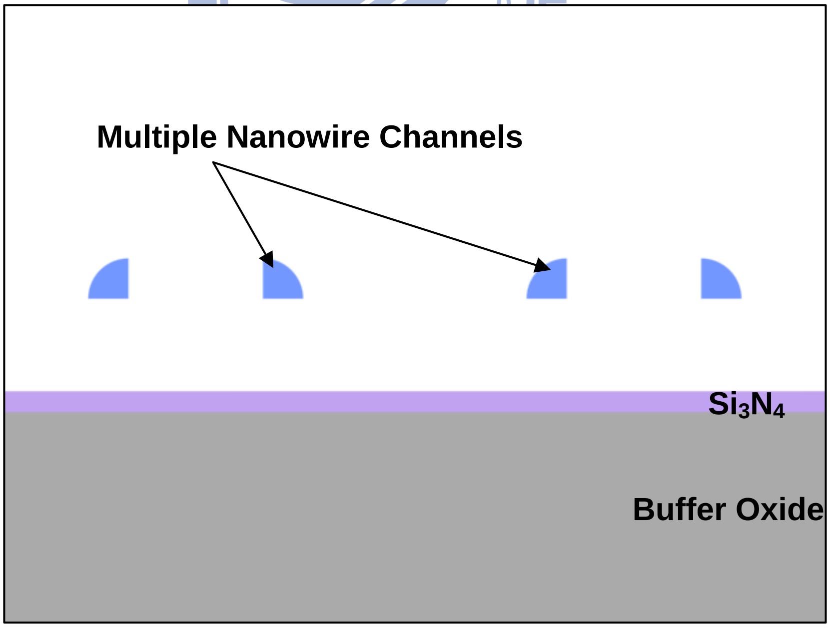


Fig. 3-1(f) The cross-section view step of the suspending nanowire-channel formation.

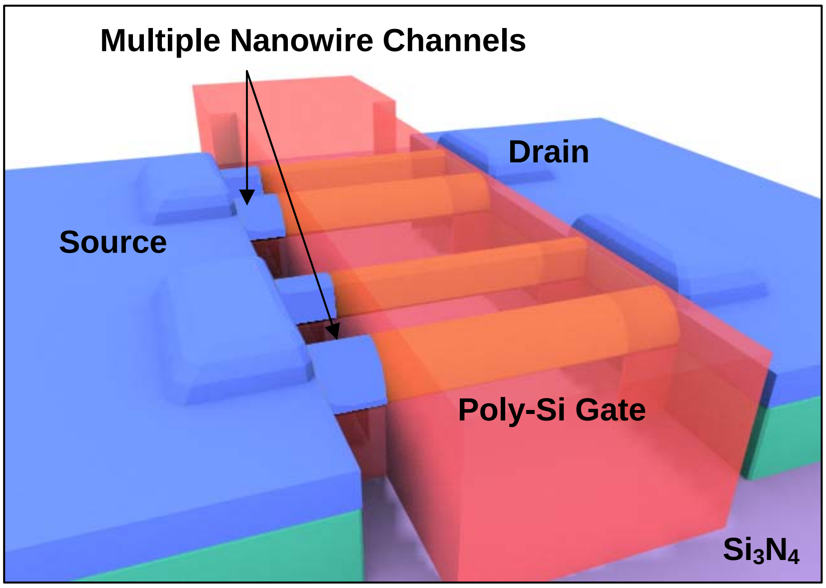


Fig. 3-1(g) The tilted view step of the gate formation.

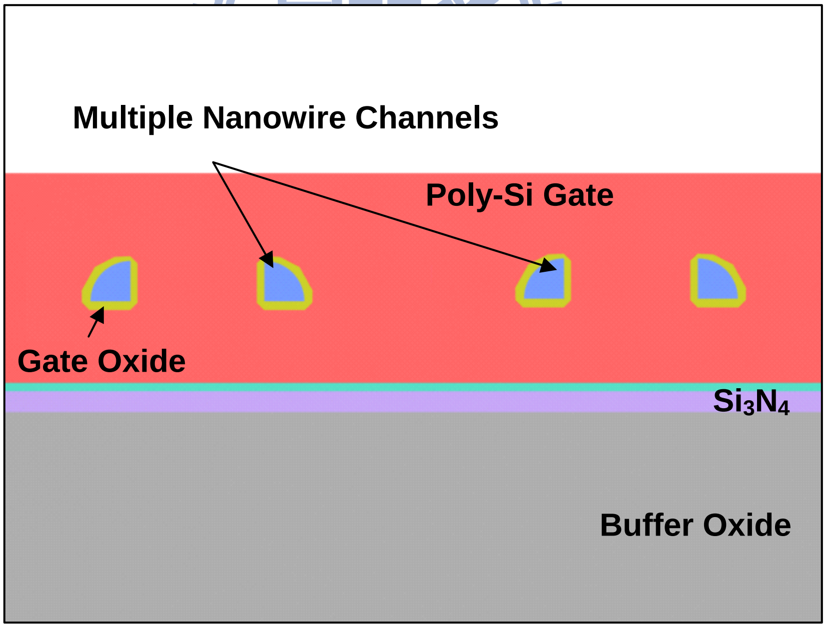


Fig. 3-1(h) The cross-section view step of the gate formation.

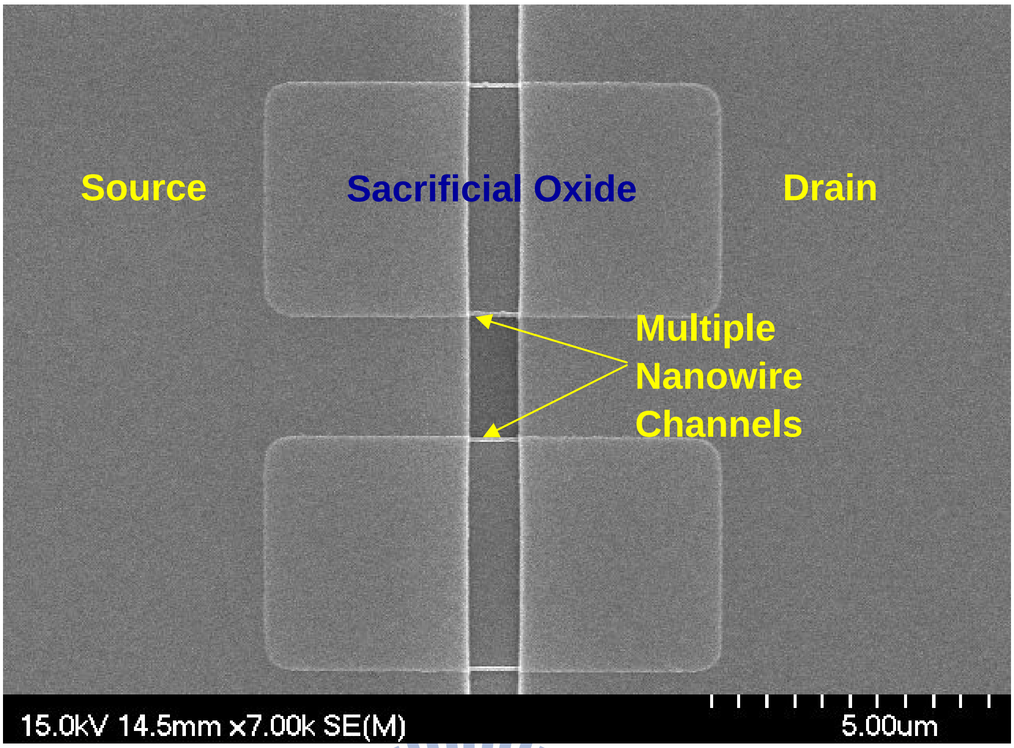


Fig. 3-2(a) The top view SEM image of one sacrificial strip with twin spacer nanowire before HF etching.

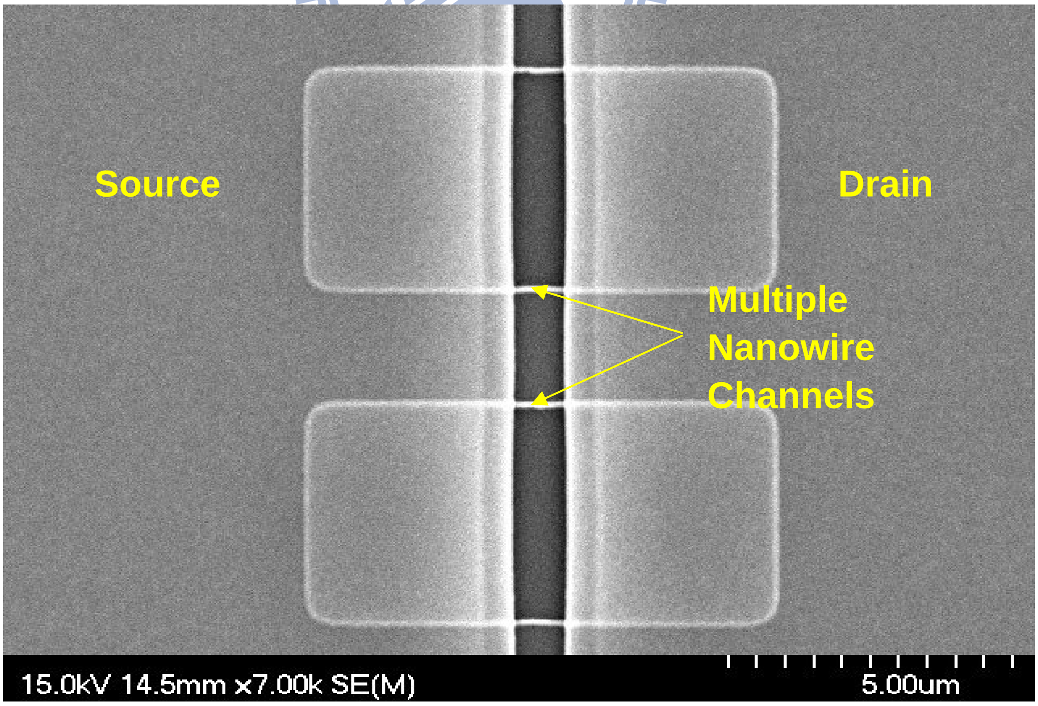


Fig. 3-2(b) The top view SEM image of one sacrificial strip with twin spacer nanowire after HF etching.

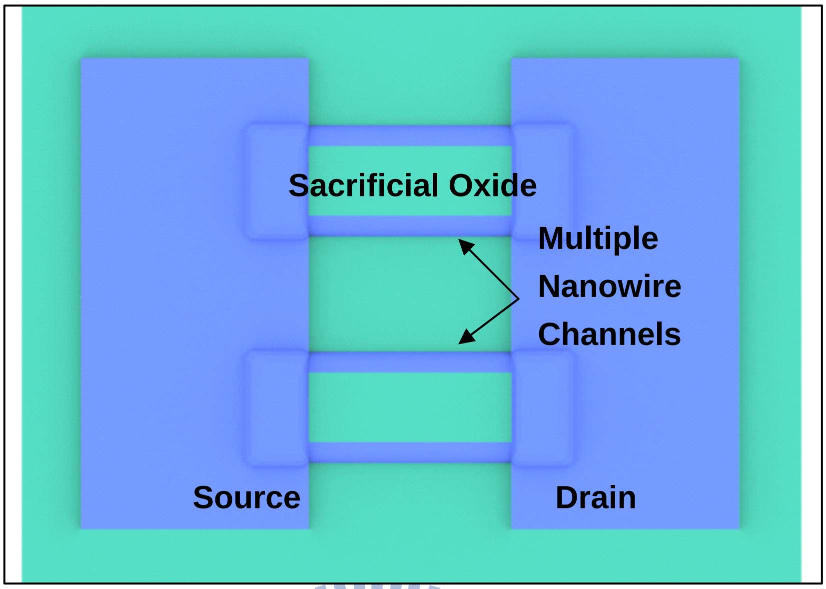


Fig. 3-2(c) The corresponding process step of one sacrificial strip with twin spacer nanowire before HF etching in top view.

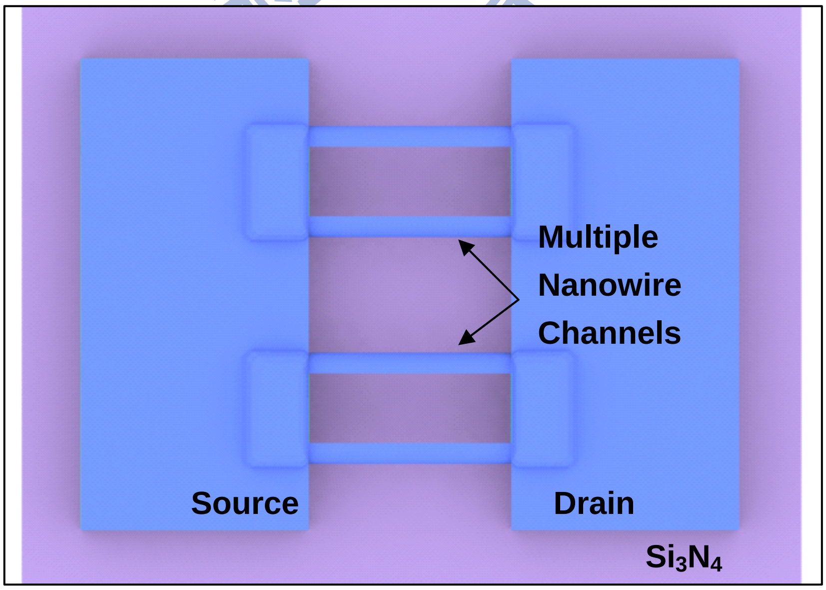


Fig. 3-2(d) The corresponding process step of one sacrificial strip with twin spacer nanowire after HF etching in top view.

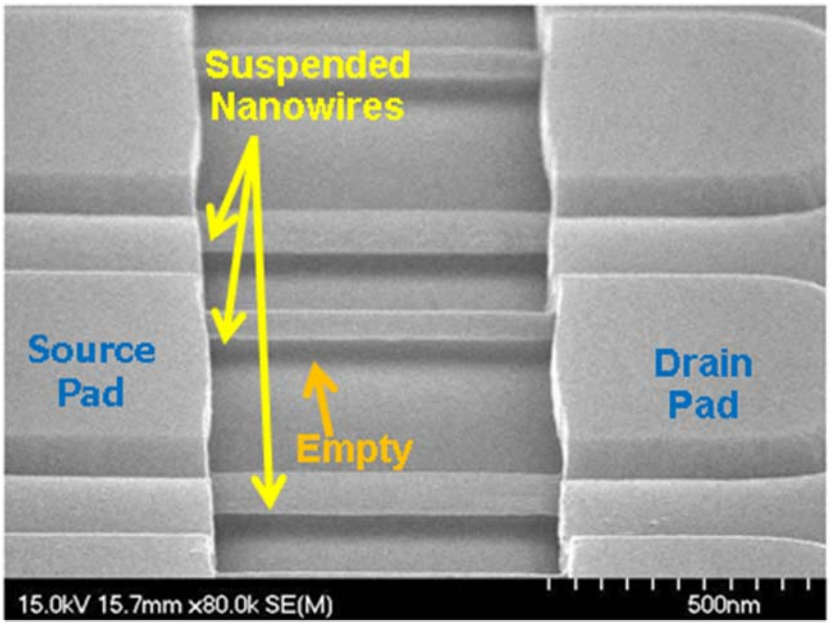


Fig. 3-3(a) The tiled view SEM image of multiple nanowire channels after HF etching.

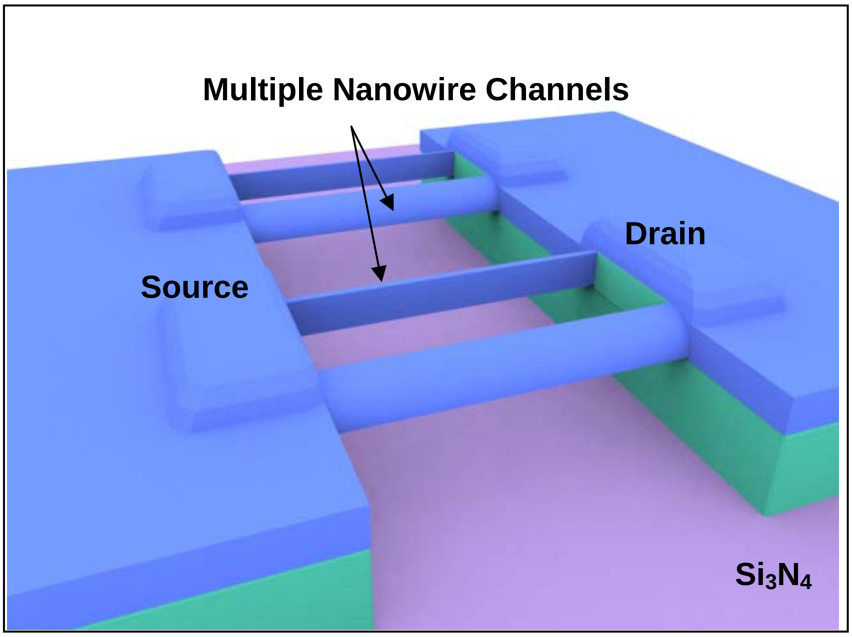


Fig. 3-3(b) The corresponding process step of multiple nanowire channels after HF etching in tiled view.

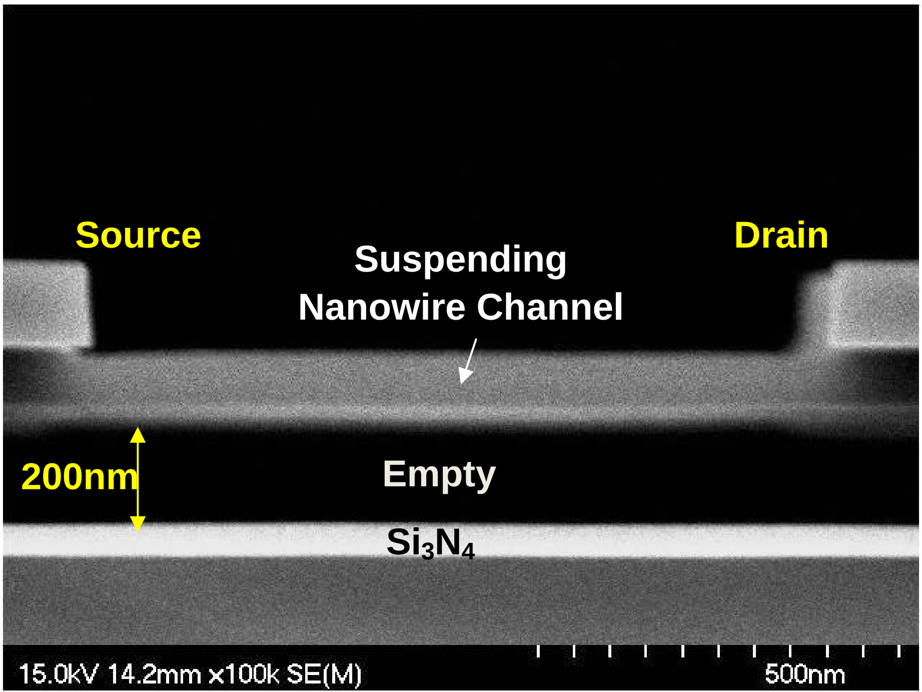


Fig.3-4(a) The cross-section SEM image of suspending channels.

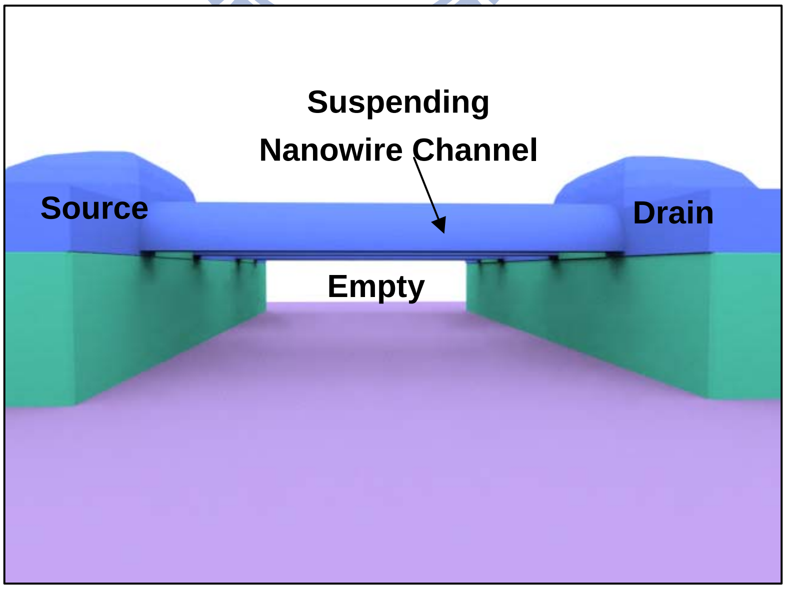


Fig. 3-4(b) The corresponding process flow of multiple nanowire channels after HF etching in cross-section view.

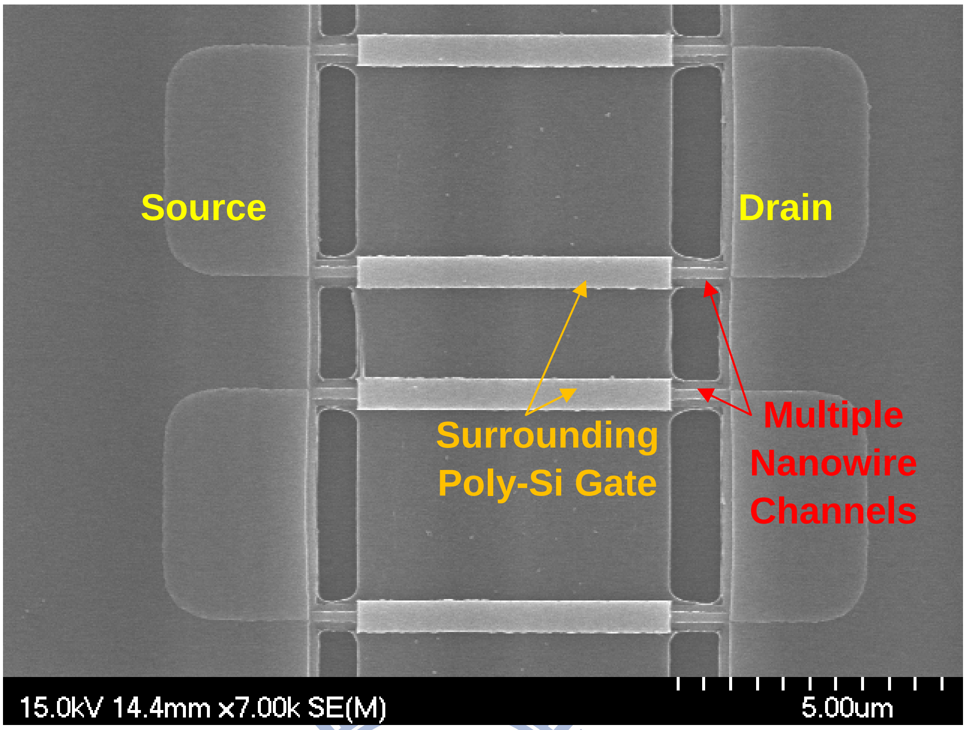


Fig. 3-5(a) The top view SEM image after patterning gate.

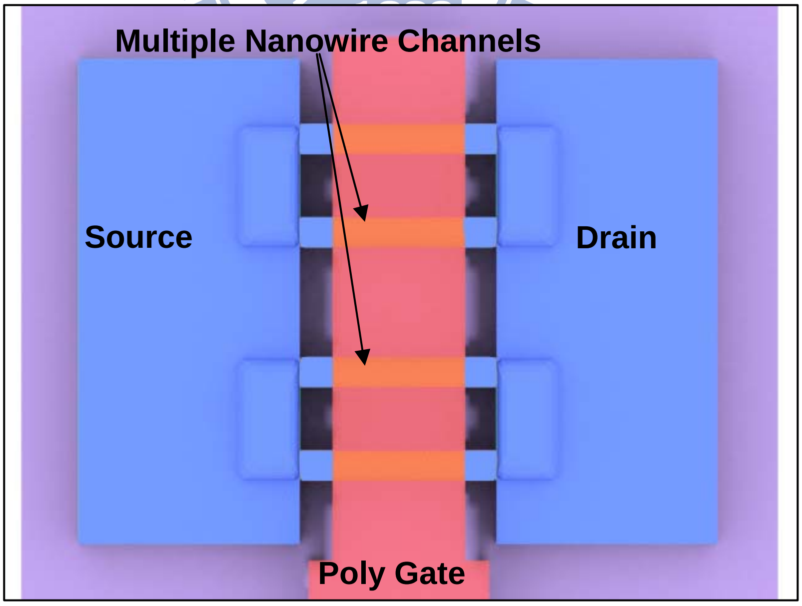


Fig. 3-5(b) The corresponding process step after patterning gate in top view.

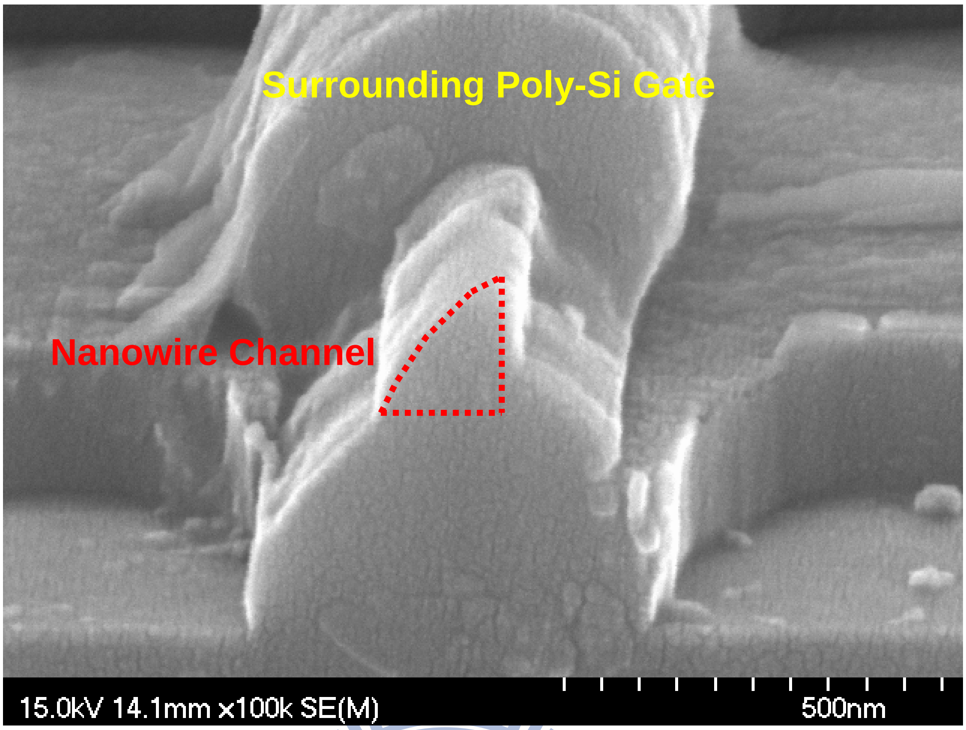


Fig. 3-6 The cross-section SEM image of the nanowire channel wrapped around by the patterned gate stacks near drain pad.

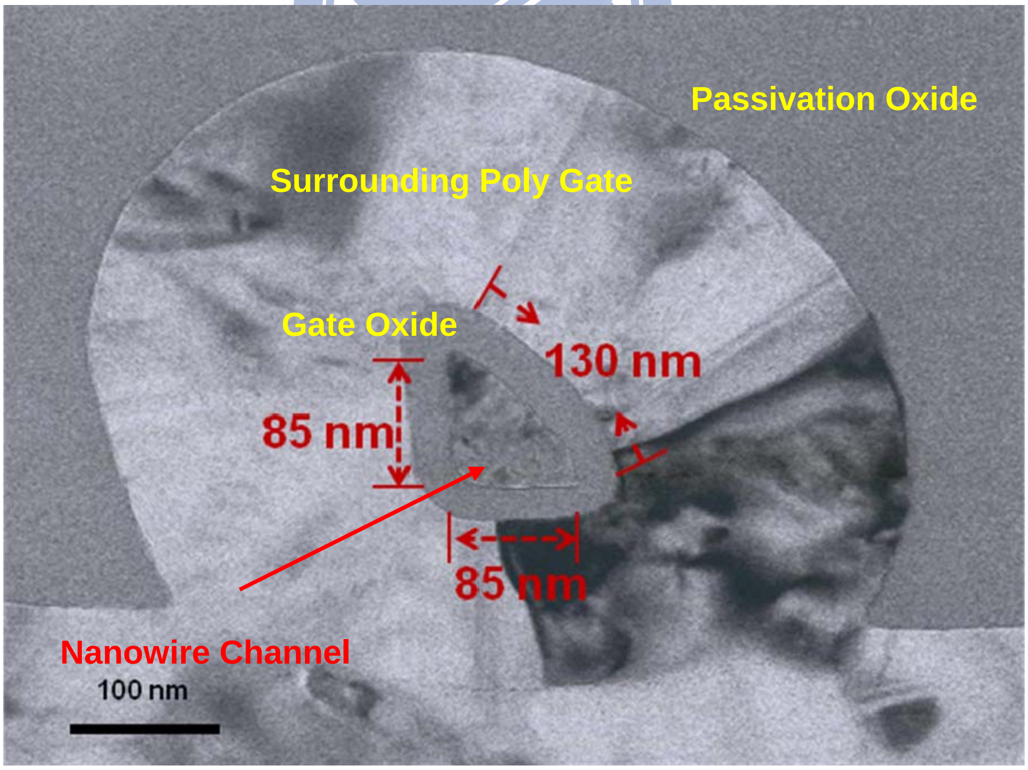


Fig. 3-7 The cross-section TEM image of nanowire channel wrapped around by the gate stacks.

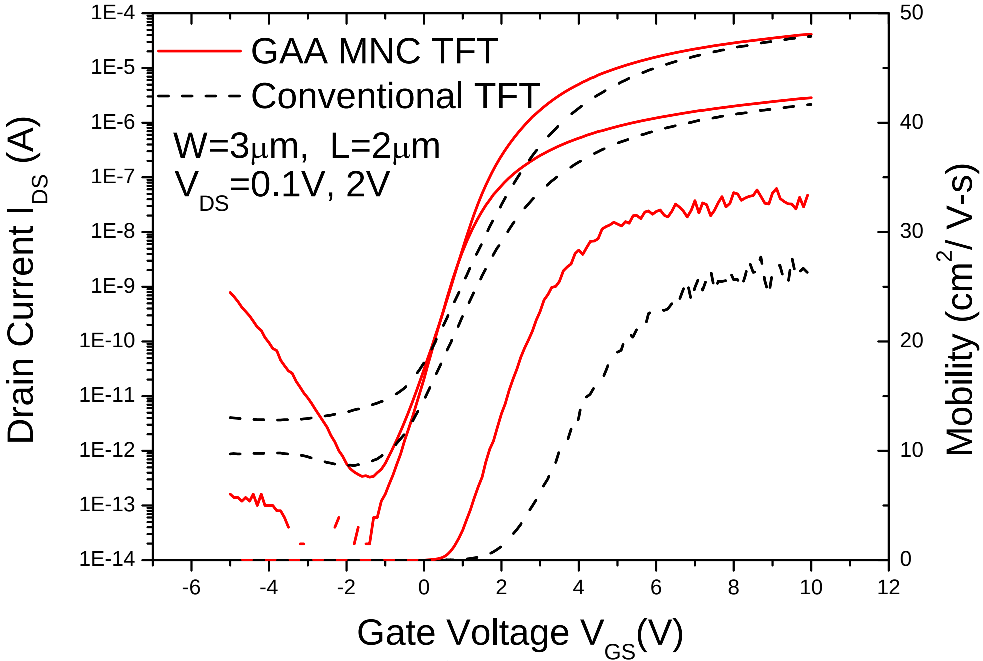


Fig. 3-8 Transfer characteristics of gate-all-around poly-Si TFTs with multiple nanowire channels and conventional TFTs.

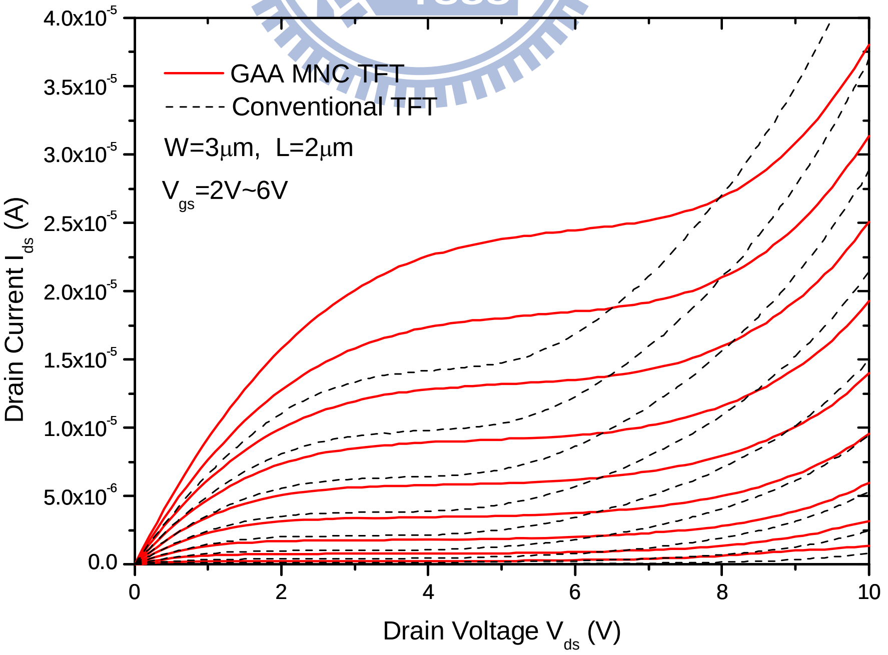


Fig. 3-9 Output characteristics of gate-all-around poly-Si TFTs with multiple nanowire channels and conventional TFTs.

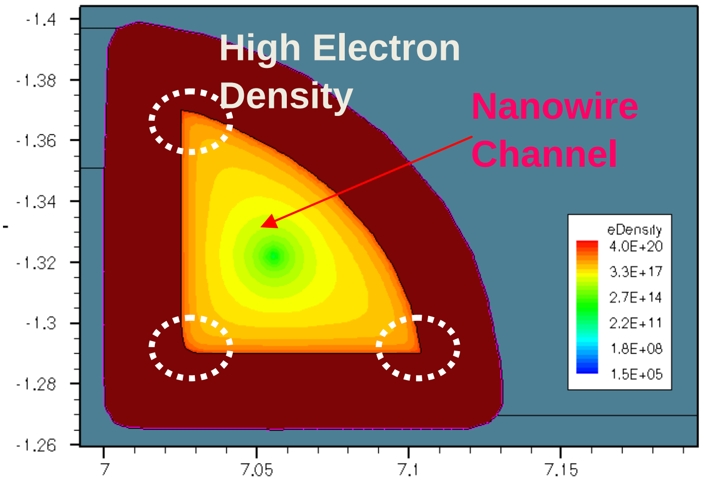


Fig. 3-10 The electron density simulation of gate-all-around poly-Si TFTs with multiple nanowire channels by ISE-DESSIS.

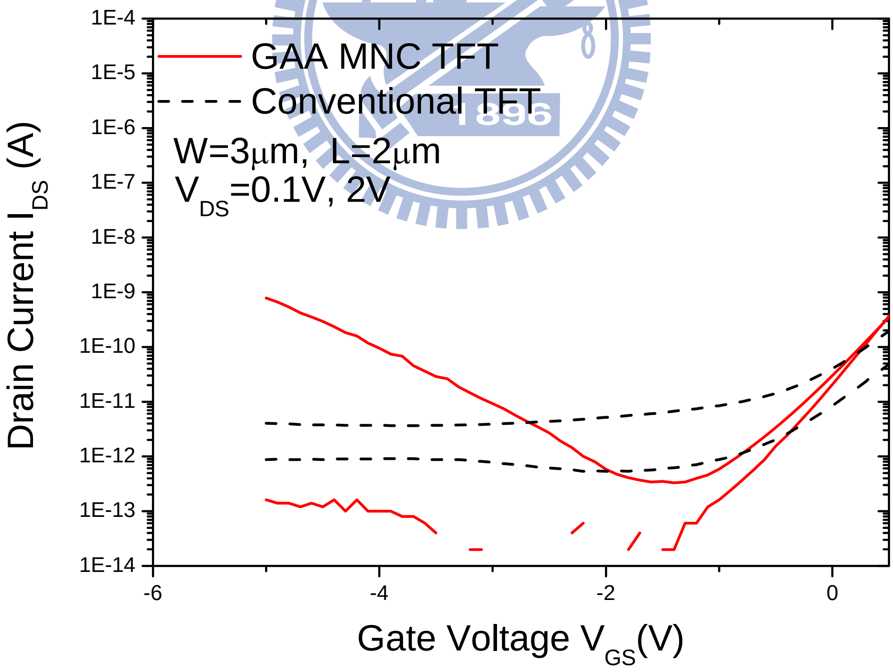


Fig. 3-11 Comparison of leakage current between GAA-MNC and conventional TFTs.

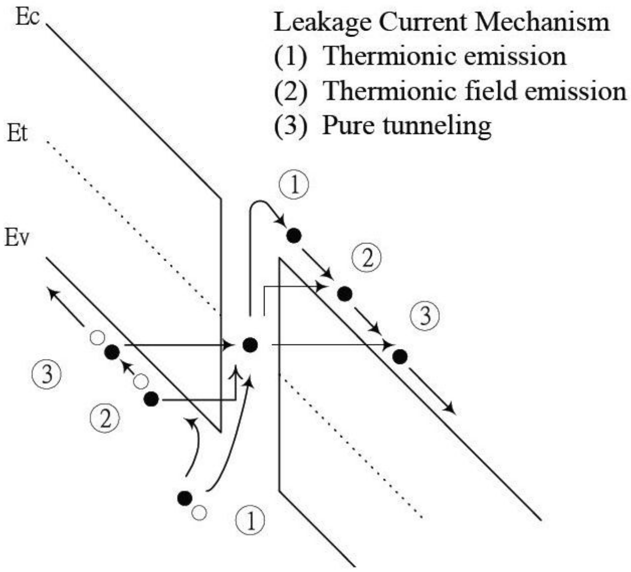


Fig. 3-12 Leakage current mechanisms.
(1) Thermionic emission
(2) Thermionic filed emission
(3) Pure tunneling (ban-to-band tunneling)

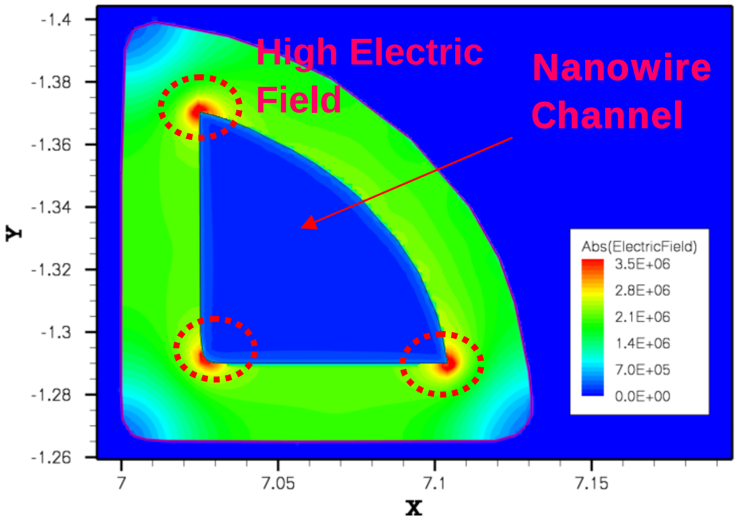


Fig. 3-13 The electric field simulation of GAA-MNC TFTs by ISE-DESSIS.

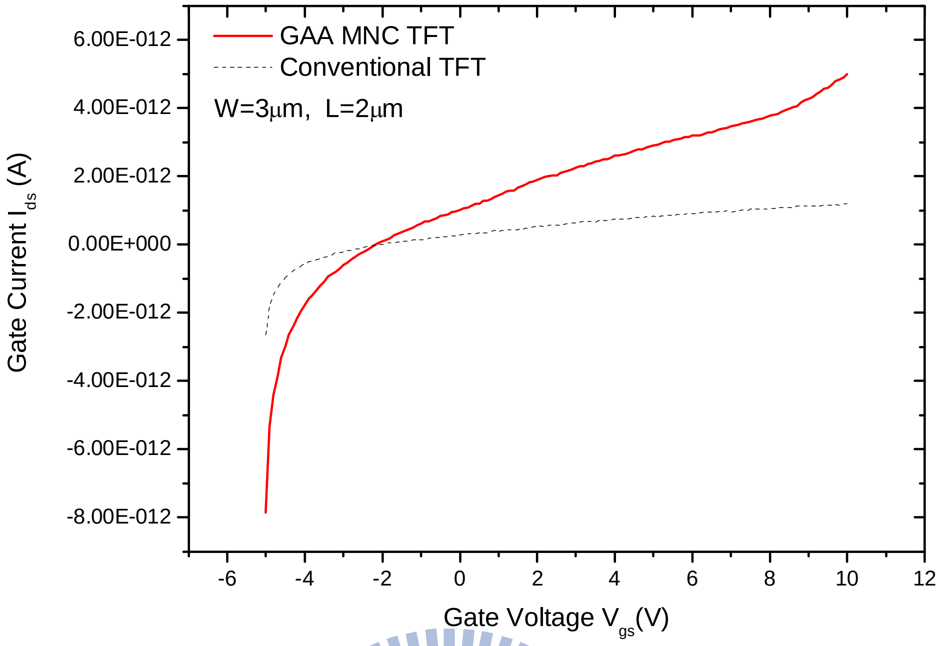


Fig. 3-14 Comparison of gate current between GAA-MNC and conventional TFTs.

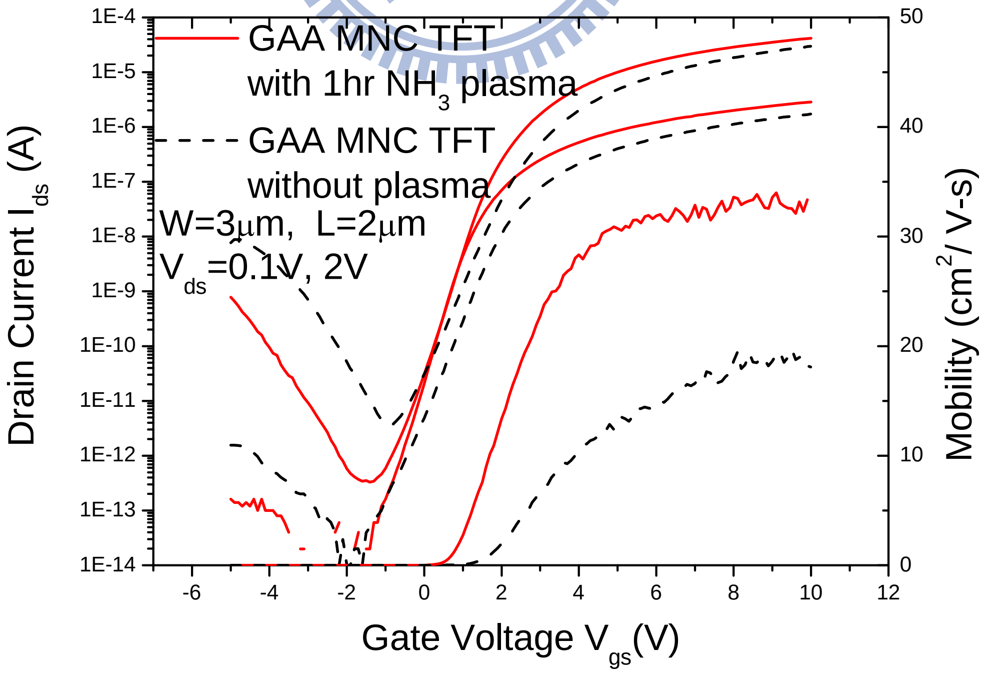


Fig. 3-15 Transfer characteristics of gate-all-around poly-Si TFTs with multiple nanowire channels before and after 1-hour NH_3 plasma passivation.

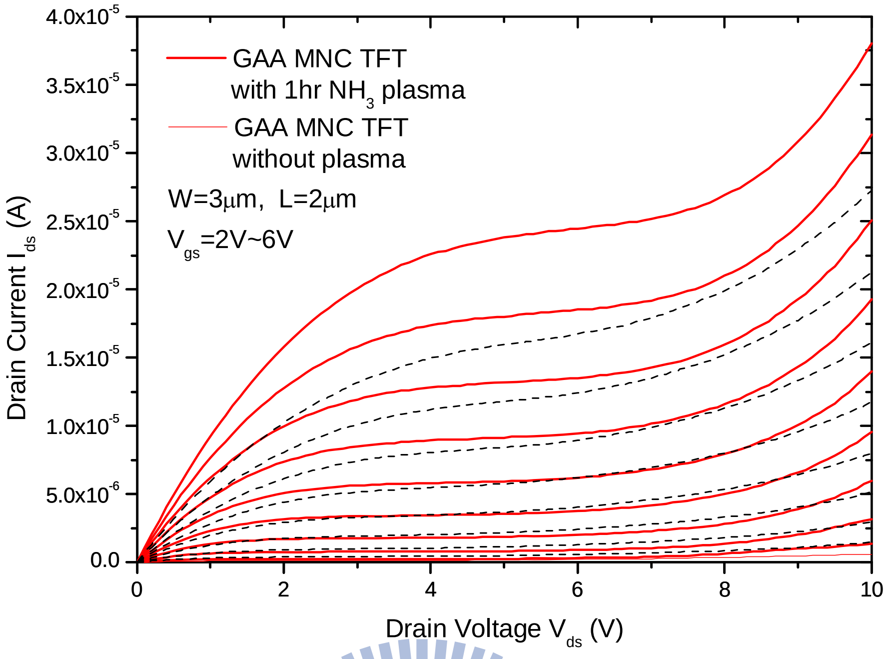


Fig. 3-16 Output characteristics of gate-all-around poly-Si TFTs with multiple nanowire channels before and after 1-hour NH_3 plasma passivation.

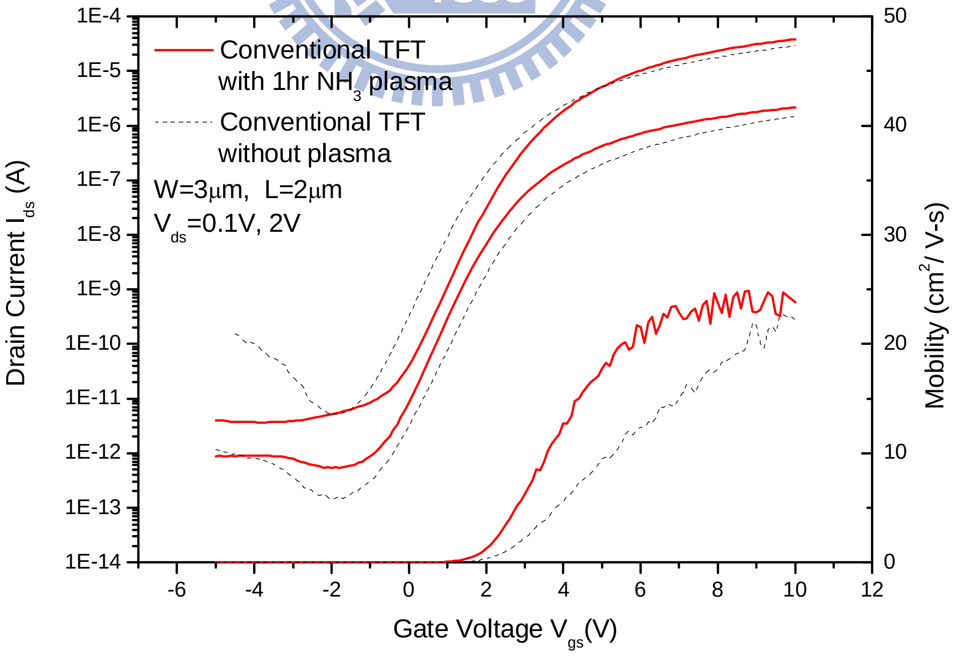


Fig. 3-17 Transfer characteristics of conventional TFTs before and after 1-hour NH_3 plasma passivation.

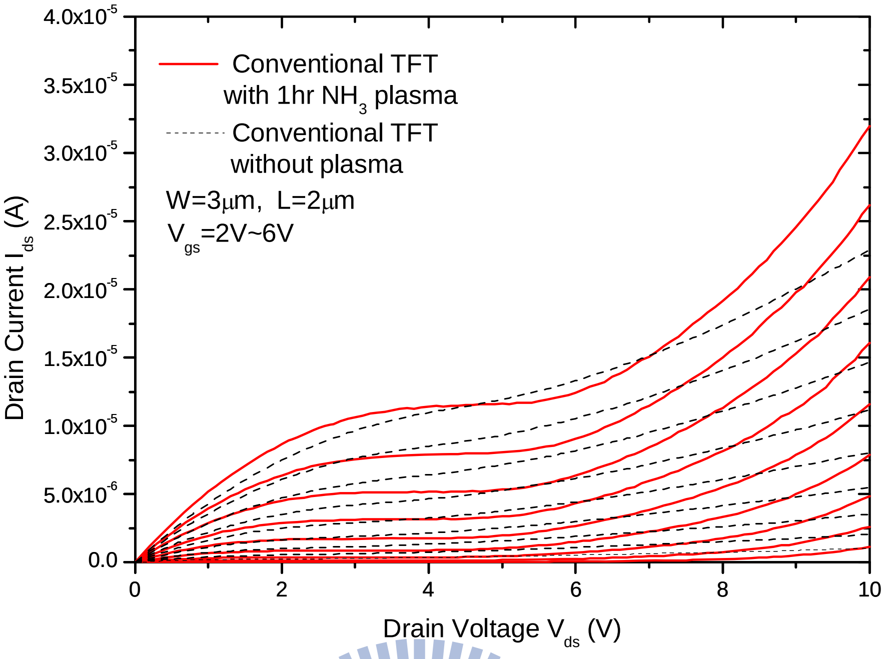


Fig. 3-18 Output characteristics of conventional TFTs before and after 1-hour NH_3 plasma passivation.

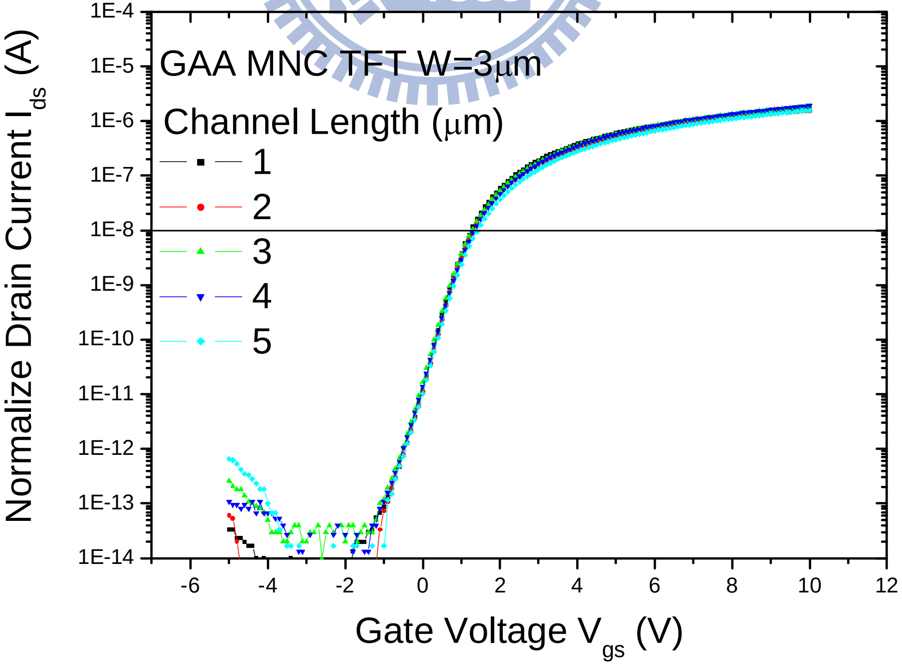


Fig. 3-19 Normalized transfer characteristics of gate-all-around poly-Si TFTs with multiple nanowire channels.

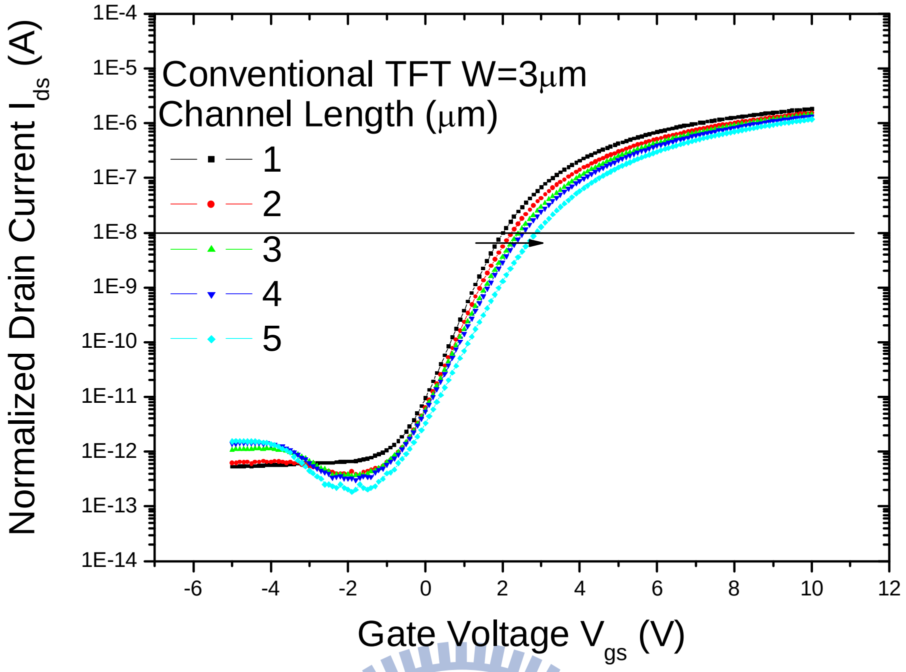


Fig. 3-20 Normalized transfer characteristics of conventional TFTs.

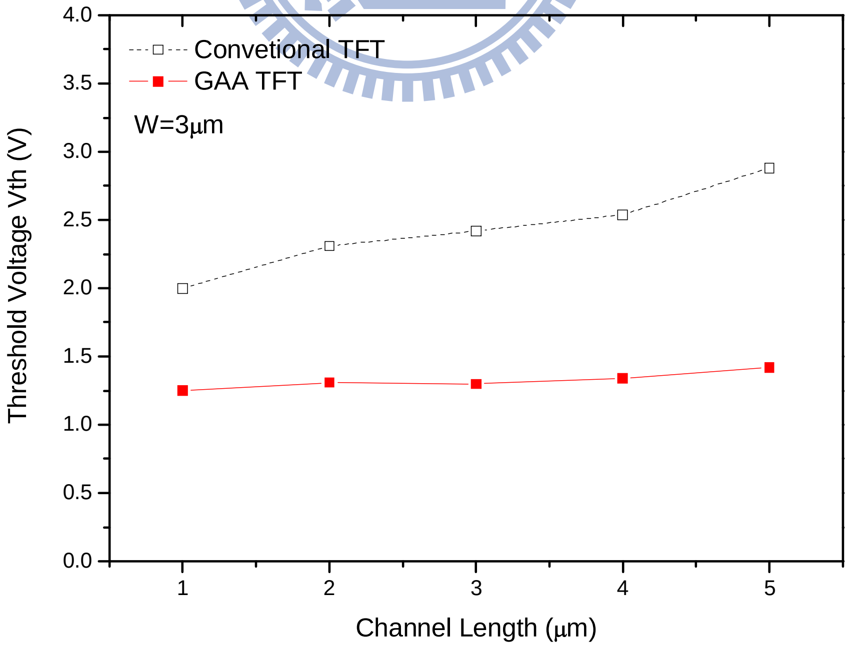


Fig. 3-21 The threshold voltage of poly-Si TFTs with multiple nanowire channels and conventional TFTs with various channel length.

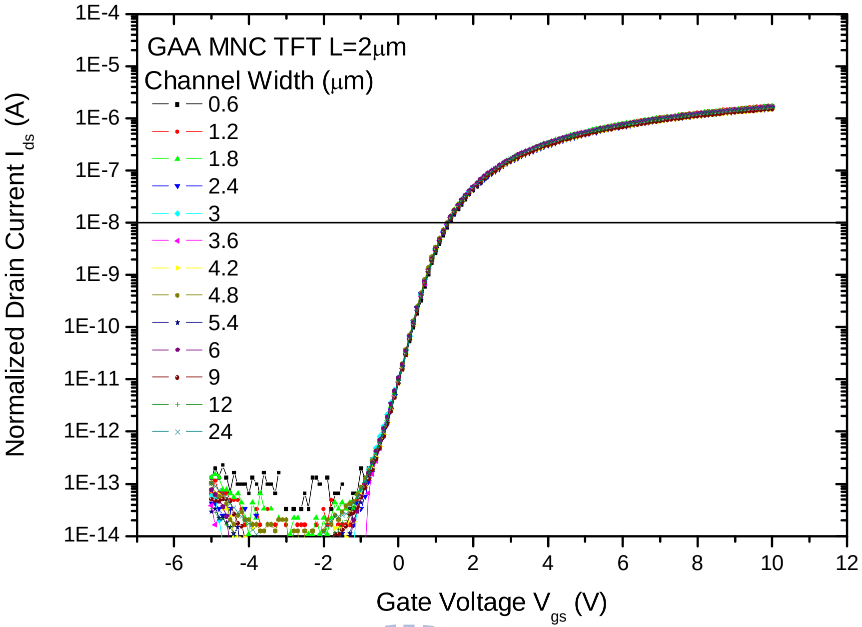


Fig. 3-22 Normalized transfer characteristics of gate-all-around poly-Si TFTs with multiple nanowire channels.

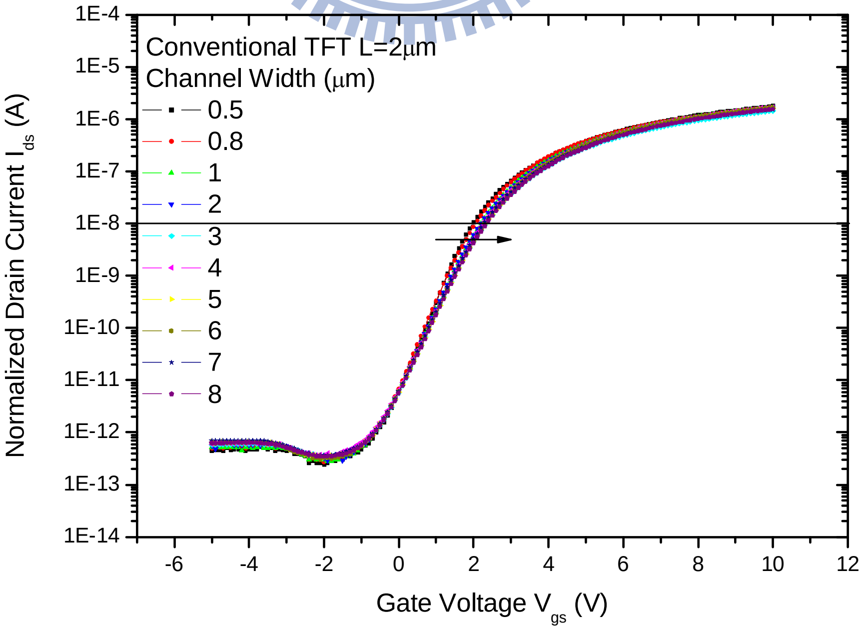


Fig. 3-23 Normalized transfer characteristics of conventional TFTs.

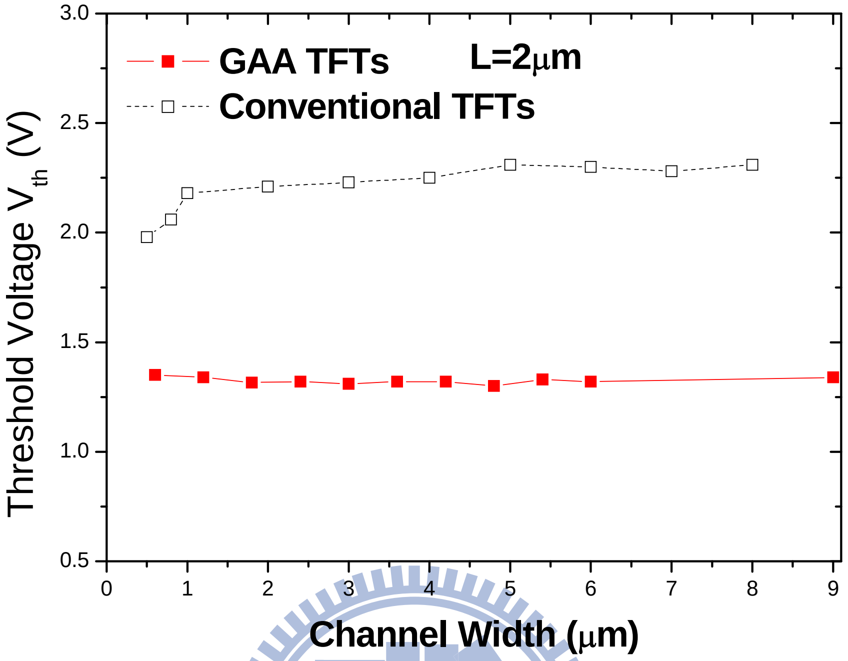


Fig. 3-24 The threshold voltage of poly-Si TFTs with multiple nanowire channels and conventional TFTs with various channel width.

Chapter 4

High-Crystallinity Silicon Nanowire Thin-Film Transistors with Gate-All-Around Structures

4.1 Introduction

In chapter 3, gate-all-around structure has been demonstrated to be the good alternative device structure for the ultimate scaling of LTPS TFTs, however, due to the poor crystallinity of solid phase crystallization, its mobility performance is still not good for high-speed SOP applications.

For device application, the structural properties of the poly-Si thin films are of major interest. The primary concerns are the grain size, quality of the grains, and the grain size distribution in channel, and these properties will strongly inference the electrical characteristics of poly-Si. Laser crystallization of a-Si thin film can be performed using a variety of lasers and different techniques [4.1]-[4.6]. However, excimer laser crystallization (ELC) is the most promising method for its great potential in mass production and high-quality silicon grains without damage to glass substrates [4.7]-[4.9]. The principle advantage of excimer lasers is the strong adsorption of UV light in silicon. Consequently, most of laser energy is deposited close to the surface of the silicon thin film and the thermal strain on the substrate is much lower than in the case of lasers with longer wavelength. The basic transformation processes for excimer laser crystallization can be divided into three crystallization regimes depending on the applied laser fluences and are relatively well understood [4.10], [4.11]. Large-grain poly-Si thin films always result in high-performance poly-Si thin-film devices due to the reduction of defect traps of the grain boundaries. Hence, enlarging grain size is the most effective manner for improving the performance of poly-Si devices. Although conventional ELC method can result in large-grain poly-Si thin films, the grain size of ELC poly-Si thin films depends on applied laser energy density, film thickness, substrate temperature and so on. Besides, lots laser crystallization methods have been proposed to produce large grains with uniform grain-size distribution, including sequential lateral solidification [4.12], the grain-filter method [4.13], additional reflective or antireflective capping layer [4.14], phase-modulated ELC [4.15], dual-beam excimer laser annealing (ELA) [4.16], double-pulsed laser annealing [4.17], selectively floating a-Si active layer [4.18], continuous-wave laser lateral crystallization [4.19], selectively enlarging laser crystallization [4.20], and so on. However, some of them are still complex and not easy to control, and difficult to simultaneously achieve large grain and uniform distribution of grain size.

In this chapter, two kinds of novel processes with nano-scale channel dimension were demonstrated for fabricating high-crystallinity Si nanowire LTPS TFTs with gate-all-around structures. Due to the gate-all-around operation and high-crystallinity formed in the nanowire channel, the both proposed devices have a high driving current, steeper subthreshold slope, superior SCE immunity, and suppression of the kink effect.

4.2 Experiments

In this chapter, two types of novel processes were demonstrated for fabricating multiple-gate TFTs with high-crystallinity Si nanowire (NW) channels. The one is the excimer-laser-crystallized (ELC) nanowire TFT, in which the nanowire structure features only-one grain boundary. The other is the spacer-patterned nanowire TFT based on large-grain poly-Si thin film prepared with sequential-lateral-solidification (SLS) crystallization [4.12], in which the nanowire can be controlled to be approximated single-crystalline.

4.2.1 Fabrication Sequence of Excimer-Laser-Crystallized Nanowire Thin Film Transistors

The fabrication of the excimer-laser-crystallized (ELC) nanowire TFTs is similar as GAA-MNC poly-Si TFTs mentioned in chapter 3 except for the crystallization method. The key steps are schematically illustrated in Fig. 4-1. At first, a 50-nm-thick SiN and a 300-nm-thick tetra-ethyl-ortho-silicate (TEOS) SiO_2 were sequentially deposited at 780 and 700 ˚C by low pressure chemical vapor deposition (LPCVD) system on oxidized silicon wafer as a selectively etching-stop and a sacrificial layers, respectively. The sacrificial SiO_2 layer, then, was patterned with several dummy strips and anisotropically etched only 100 nm in-depth to form the step profiles. After a 100-nm-thick a-Si conformal deposition by LPCVD at 550˚C, only the photo-resists (PRs) for the source/drain (S/D) pads were patterned to overlap on the two edges of those dummy strips by standard optical lithography. Subsequently, a reactive ion etch (RIE) was used to remove the a-Si; meanwhile, a couple of spacer nanowire channels were *in-situ* resided with a self-aligned manner against the sidewall of each designed strip and naturally connected to the source/drain (S/D) pads. It should be noted that the nano-scale dimension of the nanowire channels can be defined simply by controlling the RIE time without any advanced lithography, each strip produces twin nanowire channels, as well as the multiple nanowire channels can be designed with those designed strips (n strips × 2 wires/strip = 2n wires). After 100-nm-thick SiO_2 capping, a-Si nanowires were transferred into poly-Si type by KrF excimer laser crystallization with 320 mJ/cm^2 at room temperature as shown in Fig. 4-1(a). Then, the unique suspending MNCs were constructed after the SiO_2-strips were etched away (down to the SiN etch-stop layer) by a HF etchant. Then, the 25-nm-thick TEOS SiO_2 and the 200-nm-thick phosphorous *in-situ* doped poly-Si were conformally deposited by LPCVD system at 700 and 550 °C as gate insulator and gate electrode, respectively. After gate patterning, self-aligned phosphorous S/D implantation was performed at 30 keV to a dose of 5×10^{15} cm^{-2} [Fig. 4-1(b)] and a 300-nm-thick passivation oxide layer was deposited, followed by a S/D activation. Contact opening formation and metallization were carried out. For structure comparison, the conventional planar (CP) poly-Si TFTs were fabricated with the same process run. Besides, for crystallization comparison, both corresponding CP and GAA-MNC structured poly-Si TFTs with SPC crystallization were fabricated as well.

4.2.2 Fabrication Sequence of Gate-All-Around Thin Film Transistors with Single-Crystalline-Like Nanowire Channels

At first, a 40-nm a-Si layer was deposited on oxidized wafer by the low-pressure chemical vapor deposition furnace (LPCVD, 550°C). Sequential-lateral -solidification (SLS) crystallization with 900 mJ/cm^2 was performed to transfer a-Si into poly-Si with large grain size of 3 × 0.8 μm^2. After a 100-nm-thick TEOS oxide deposition by LPCVD at 700 °C, oxide was patterned as several strips by standard optical lithography and etched anisotropically with 100-nm in-depth by the reactive ion etching (RIE) to form the step profile as shown in Fig. 4-2 (a). After that, a 100-nm SiN_x film was deposited by LPCVD at 680 °C; Subsequent reactive ion etching (RIE) formed the sidewall spacers that served as a hard mask in the following SLS poly-Si etching process as shown in Fig. 4-2 (b). By controlling the RIE conditions and the thickness of the SiN_x film, the feature size of the SiN_x units could be scaled down to the nanoscale without using any advanced photolithography techniques. Next, the TEOS dummy block was stripped off by DHF as shown in Fig. 4-2 (c). Then, anisotropic RIE of poly-Si layer led to the formation of the twin poly-Si NW in which the wire width was transferred by the size of the SiN_x features [Fig. 4-2 (d)]. SiN_x was then removed by hot H_3PO_4 at 165 °C, as shown in Fig. 4-2 (e). The poly-Si NW was then released from the buffer oxide through diluted HF solution by removing 200-nm of thermal SiO_2, Followed by sequential conformal deposition of 25-nm-thick TEOS and 200-nm *in situ* N^+ poly-Si using LPCVD at 550°C. The channel was surrounded by TEOS and N^+ poly-Si, as shown in Fig. 4-2 (f). After gate patterning, self-aligned phosphorous S/D implantation was performed at 30 keV to a dose of 5×10^{15} cm^{-2} and a 300-nm-thick passivation oxide layer was deposited by LPCVD at 700 °C . Standard contact opening formation and metallization were carried out. For structure comparison, the conventional planar (CP), tri-gate (without buffer-oxide etching) poly-Si TFTs were fabricated with the same process run. Besides, for crystallization comparison, corresponding CP, tri-gate and GAA-MNC structured poly-Si TFTs with SPC crystallization were fabricated as well.

4. 3 Results and Discussion

4.3.1 Material Analyses of Excimer-Laser-Crystallized Nanowire

As the principle of excimer laser crystallization, a lateral temperature gradient can be created between the adjacent areas and there must be un-melting solid Si to act as the seeds for lateral crystallization. In the proposed structure, as shown in Fig. 4-1(a), the a-Si region in the nanowire channel is much thinner than that of oxide strip sidewall of S/D pad adjacent to nanowire, which is similar as recessed structure. Thus, by completely melting in the a-Si nanowire region and partially melting in the a-Si at S/D pads overlapped oxide strip sidewall, a lateral temperature gradient will exist between the complete melting liquid-phase region and un-melting solid-phase seeds, and grains will grow laterally towards the complete melting region from the un-melting solid seeds. However, Fig. 4-3 shows the nanowire directly crystallized by excimer laser with 200 mJ/cm^2 without capping any oxide, it is observed that the nanowire has been ablated with only some residual of Si nano dots. The better heat-sinking property of nanowire with high surface-to-volume ratio resulted in serious supercooling phenomenon. To overcome this issue, a capped oxide has been performed with the optimum laser energy of 320 mJ/cm^2 to prevent such supercooling phenomenon. Evidently, the existence of only-one grain-boundary could be found in the middle nanowire channel after Secco-etch, as shown in Fig. 4-4 (a). Fig. 4-4 (b) shows the corresponding SEM image of crystallized nanowire which is intact after oxide de-capping and before Secco-etch, proving the only-one grain-boundary exists in Fig. 4-4 (a).

Fig. 4-5 (a) shows the SEM image of the fabricated excimer-laser-crystallized nanowire GAA TFT. Its corresponding cross-section TEM image is shown in Fig. 4-5 (b). The good step-coverage is observed on GAA structure both for TEOS gate oxide and phosphorous *in-situ* doped poly gate, and the vertical sidewall thickness (T_{Fin}), the horizontal width (W_{Fin}) and the bevel length of each nanowire channel are about 80, 70, and 130 nm, respectively. Thus the total surrounding width of each nanowire channel is 280 nm. The aspect ratio T_{Fin}/W_{Fin} of each nanowire channel in GAA-MNC TFT (approximately equals to one) is much larger than that in CP TFT and thus features like a fin structure. Fig. 4-6 demonstrates the comparison of transfer characteristics between GAA-ELA and GAA-SPC MNC TFTs, while the comparison of output characteristics are demonstrated in Fig. 4-7.

4.3.2 Electrical Characteristics of Excimer-Laser-Crystallized Nanowire Thin Film Transistors

The GAA-ELA MNC TFTs exhibit excellent electrical performance as compared to GAA-SPC MNC TFTs. The mobility increases from 30 to 273 cm^2/V-s, the threshold voltage V_{th} decreases from 1.65 to -0.94 V, the SS decreases from 450 to 142 mV/decade, I_{on}/I_{on} increases from 1.24×10^6 to 1.37×10^7, and DIBL decreases from 0.268 to 0.157 V/V. Fig. 4-8 demonstrates the comparison of transfer characteristics between GAA-ELA MNC TFTs and CP-ELA TFTs as well. The mobility increases from 121 to 273 cm^2/V-s, the threshold voltage V_{th} decreases from 0.4 to -0.94 V, the SS decreases from 374 to 142 mV/decade, I_{on}/I_{off} increases from 5.6×10^6 to 1.37×10^7, and DIBL decreases from 0.365 to 0.157 V/V. The excellent mobility and I_{on}/I_{off} are attributed that only one grain boundary exist in middle of channel for GAA-ELA MNC TFTs. CP-ELA TFTs and GAA-SPC MNC have bad mobility characteristics due to poor crystallinity. The excellent SS and DIBL in

GAA-ELA MNC TFTs are attributed that increasing gate controllability and crystallinity improvement [4.21]. While CP-ELA TFTs have larger DIBL due to short channel effect occurred. Table 4-1 illustrates the comparison of characteristics for GAA-ELA, GAA-SPC and CP-ELA.

The leakage current mechanisms are displayed in Fig. 4-9 [4.22]. In low electric field region, the electrons are thermally excited from the valence band into the trap states and then jumping into the conduction band. The phenomenon is called thermionic emission which contributes the low electric field off-state leakage current. A number of excited electrons in thermionic emission strongly depend on the quantity of the defects and traps in channel. In medium electric field region, the electrons are thermally excited from the valence band into the trap states and then tunneling into the conduction band by the gate-drain electric field. This mechanism is known as thermionic-filed emission and depends on both the trap states and electric field. In high electric field region, the band diagram is bent strongly under high gate-drain electric field in the gate/drain overlapped region. The electrons tunnel directly from the valence band to the conduction band. This is called as the band-to-band tunneling and cause high leakage current in gate-drain junction which is also known as gate-induced drain leakage (GIDL). The GIDL current highly depends on the gate-to-drain electric field and becomes more serious with the assistance of traps.

The GAA-ELA MNC TFTs shows lower leakage current at the low gate electric field region as compared to CP TFTs in Fig. 4-10. It is because there is less volume defects in GAA-MNC TFTs' channel resulting in the reduction of thermionic emission. However, at the high gate electric field region in Fig. 4-11, the GIDL current is more significant in the GAA-ELA MNC TFTs. The higher GIDL current comes from the higher gate electric field. Also, the three sharp corners enhance the electric field resulting in the high GIDL current. The related simulation results are shown in Fig.

4-12, the electric field in the three sharp corners is much higher than other regions.

4.3.3 Material Analyses of Single-Crystalline-Like Silicon Nanowire with Spacer Patterned Method

Fig. 4-13 shows the uniformly-distributed poly-Si grain with size of 3 × 0.8 μm^2 in average prepared by SLS crystallization. The nitride spacer (8 nm) is much smaller than the grain width (0.8 μm), which make the nitride spacer locate within a single-grain simply in term of probability, thus the resulting nanowire can be performed with approximated single crystalline easily. Fig. 4-14 shows the SEM image of the fabricated spacer-patterned-nanowire tri-gate TFT. Fig. 4-15 shows it correspondingly cross-section TEM image of the spacer-patterned nanowire TFT.

4.3.4 Electrical Characteristics of Single-Crystalline-Like Silicon Nanowire Thin Film Transistors with Spacer Patterned Method

Fig. 4-16 and 4-17 compare the transfer and output characteristics of GAA-SLS MNCs with tri-gate-SLS MNC TFTs. The electrical characteristics of those TFTs are listed in Table 4-2. GAA-SLS MNC TFTs with field effect mobility of 596 cm^2/V-s and $I_{on}/_{off}$ current ratio of 8.65 × 10^7 can be achieved. The excellent mobility and $I_{on}/_{off}$ current ratio are attributed that nanowire channels locate within single grain and exhibit single-grain-like performance. Both of the multi-gate structures (GAA and tri-gate structures) show less DIBL effect (from 0.11 to 0.06 V/V) and steeper SS (from 227 to 109 mV/dec). Gate-all-around (GAA) structure were proposed to demonstrate the best immunity for DIBL effect and steeper SS because the gate controls the channel region on all sides, while tri-gate structure only controls the channel region on three sides. Fig. 4-18 displays the comparison of electrical performance between GAA-SLS MNC TFTs and CP-SLS TFTs. The GAA-SLS MNCs TFTs in all electrical parameters show excellent results as compared to CP-SLS TFTs. The electrical characteristics of those TFTs are listed in Table 4-3. Fig. 4-19 shows the comparison of GAA-SLS MNC TFTs and CP-SLS TFTs with fixed channel length of 0.5 μm and various channel widths from 0.15 to 4 μm for 20 samples extracted. Due to multiple-nanowire channels effect, the standard deviation of mobility is less while nanowire channels more than 20 nanowires. This result indicates that the GAA-SLS MNC TFTs have better uniformity of mobility while nanowire channels more than 20 NWs.

Fig. 4-20 shows the output characteristics of GAA-SLS MNC TFTs. Under $V_{GS} > V_{DS}$ (typically called self-heating mode), the drain current is decreased as temperature rising, indicating that the lattice-vibration mechanism is dominant. On the others word, nearly single-crystalline-like nanowire has been achieved [4.23]. Fig. 4-21 shows the output characteristics of GAA-SPC MNC TFTs, kink effect is dominant in saturation region due to serious avalanche effects enhanced by the plentiful defects in SPC-crystallized poly-Si channel.

4.4 Summary

In this chapter, two-type laser crystallized methods for gate-all-around poly-Si

TFTs with multiple nanowire channels (GAA-MNC TFTs) are fabricated by using a simple process sequence. Unlike E-beam patterned nanowires, the proposed nanowires are only performed with standard optical lithography and spacer formation methods. The fabricated GAA-ELA MNC TFTs exhibit excellent electrical performance as compared to those SPC counterparts. Under the on-state operation, the GAA-MNC TFTs demonstrate lower V_{th} (from 1.65 to -0.94 V), smaller DIBL (from 0.268 to 0.157 V/V), stepper subthreshold swing (SS) (from 450 to 142 mV/decade), less kink current, higher on current (from 1.24×10^{6} to 1.37×10^{7} A), and higher mobility (from 30 to 273 cm^2/V-s). The drawback of such ELC-nanowires are still one grain boundary exist in the middle of nanowire channel and only suitable for short channel devices.

On the other hand, gate-all-around (GAA) poly-Si TFTs with single-crystalline-like nanowires were proposed as well. The fabricated GAA-SLS MNC TFTs exhibit excellent electrical performance as compared to CP-SLS MNC TFTs ones. The GAA-SLS MNC TFTs demonstrate lower V_{th} (from -0.25 to -0.75 V), smaller DIBL (from 0.41 to 0.06 V/V), stepper subthreshold swing (SS) (from 327 to 109 mV/decade), less kink current, higher on current (from 6.43×10^{6} to 8.65×10^{7} A), and higher mobility (from 208 to 596 cm^2/V-s).

For Channel Engineering：

Due to nano-dimensional channel within one grain, the single-crystalline-like naowire TFT with excellent higher field-effect mobility of 596 cm^2/V-s is achieved.

For Gate Engineering：

Due to the gate-controllability enhancement, the negligible DIBL and better SS characteristics of GAA devices with short channel (0.35 μm) has been demonstrated.

Tables

Table 4-1 The comparison of characteristics for GAA-ELA, GAA-SPC and CP-ELA TFTs.

	Mobility ($cm^2/V\text{-}s$)	**SS (mV/dec)**	**Vth (V)**	**Ion/Ioff @ Vds = 2 V**	**DIBL (V/V)**
GAA ELA	273	142	-0.94	1.37×10^7	0.157
GAA SPC	30	450	1.65	1.24×10^6	0.268
CP ELA	121	374	0.40	5.60×10^6	0.365

Table 4-2 The electrical characteristics of GAA-SLS MNC and TRI-Gate SLS MNC TFTs.

	Mobility ($cm^2/V\text{-}s$)	**SS (mV/dec)**	**Vth (V)**	**Ion/Ioff @ Vds = 2 V**	**DIBL (V/V)**
GAA SLS	596	109	-0.75	8.65×10^7	0.06
TRI-Gate SLS	502	227	0.04	6.58×10^7	0.11

Table 4-3 The electrical characteristics of GAA-SLS MNC and CP-SLS MNC TFTs.

	Mobility ($cm^2/V\text{-}s$)	**SS (mV/dec)**	**Vth (V)**	**Ion/Ioff @ Vds = 2 V**	**DIBL (V/V)**
GAA SLS	596	109	-0.75	8.65×10^7	0.06
TRI-Gate SLS	502	227	0.04	6.58×10^7	0.11
CP SLS	208	327	-0.25	6.43×10^6	0.41

Figures

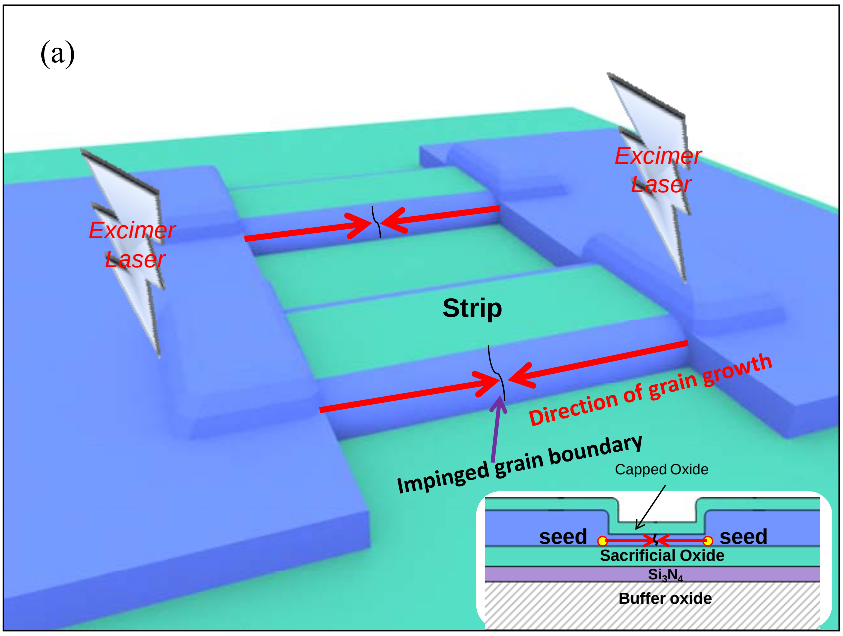


Fig. 4-1(a) The schematic diagram for the nanowire-channel formation and the grain growth during excimer laser irradiation.

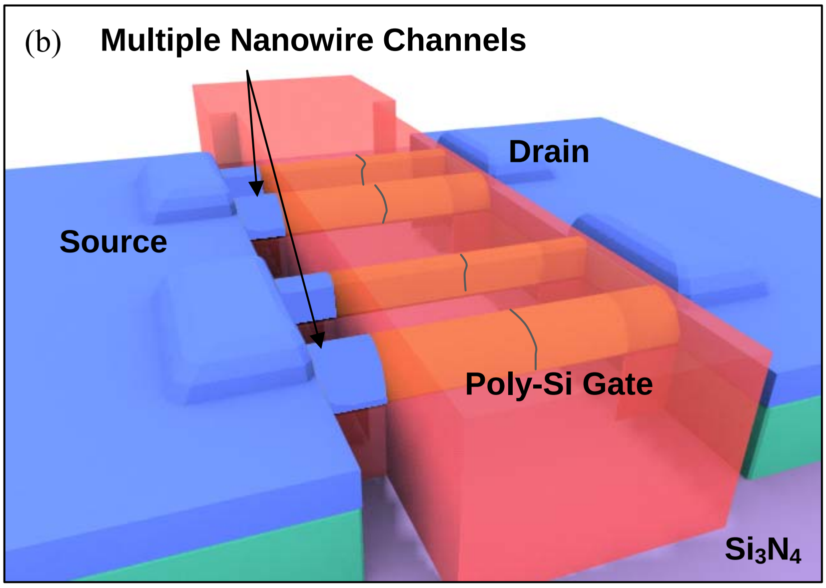


Fig. 4-1(b) The schematic diagram of gate formation.

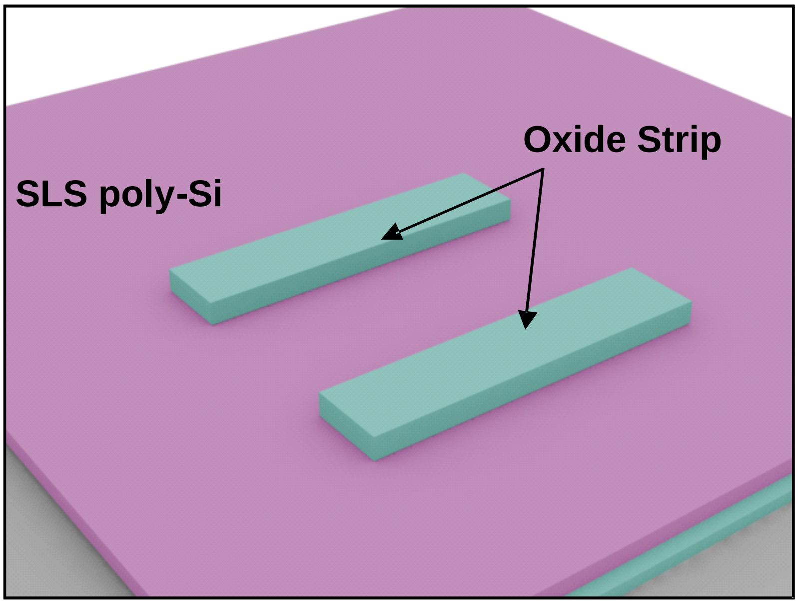


Fig. 4-2(a) The oxide strip formation.

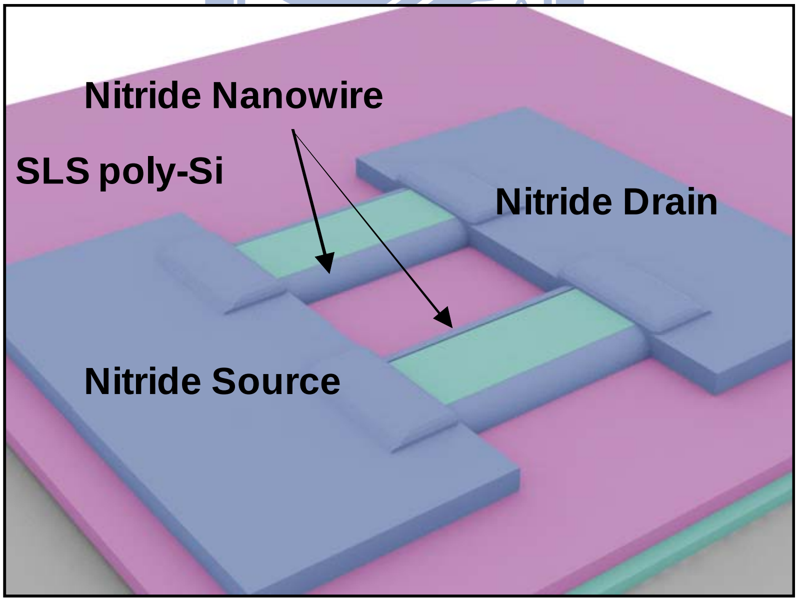


Fig. 4-2(b) The nitride spacer nanowire formation.

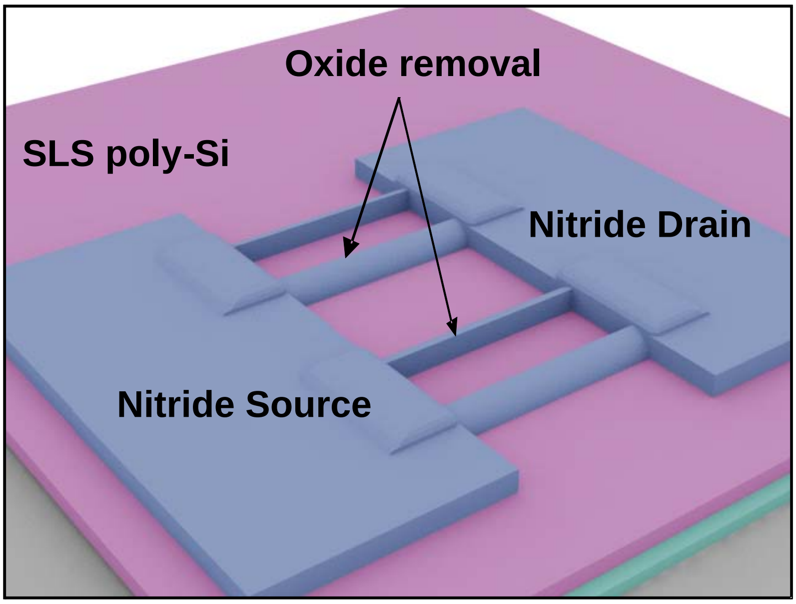


Fig. 4-2(c) Oxide removal by DHF.

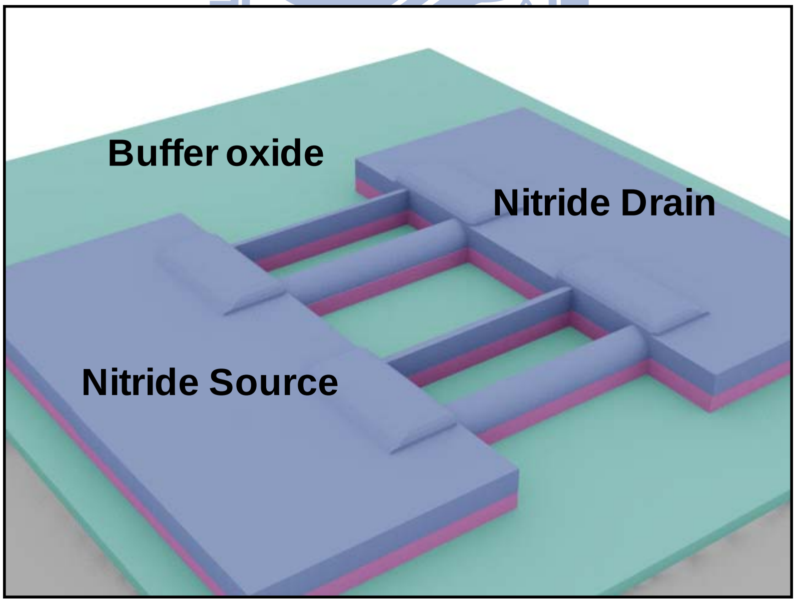


Fig. 4-2(d) A dry etching was performed to pattern the nanowire from the nano-scale nitride hard mask.

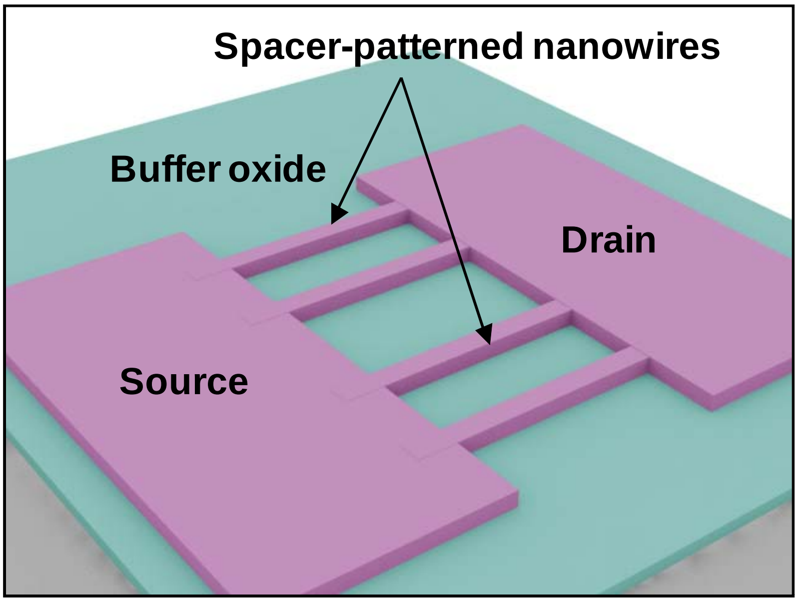


Fig. 4-2(e) Nitride removal by H_3PO_4 acid.

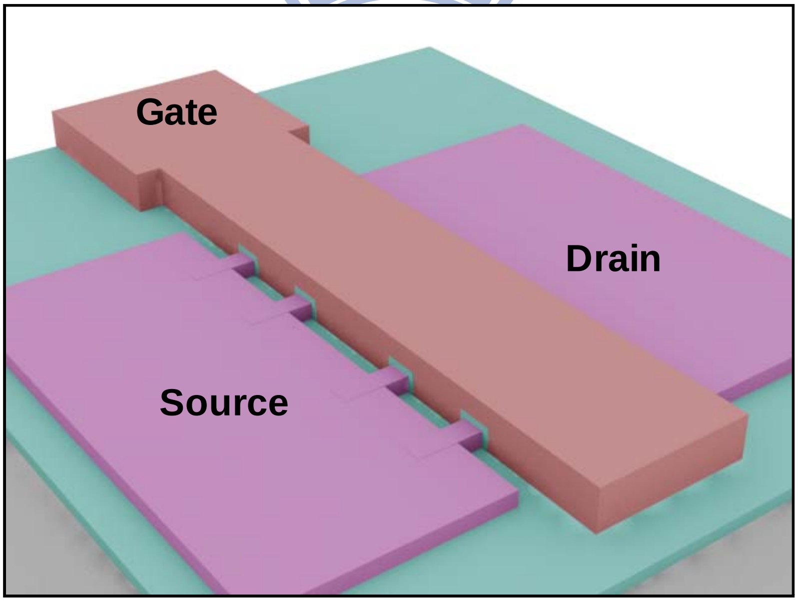


Fig. 4-2(f) the gate formation.

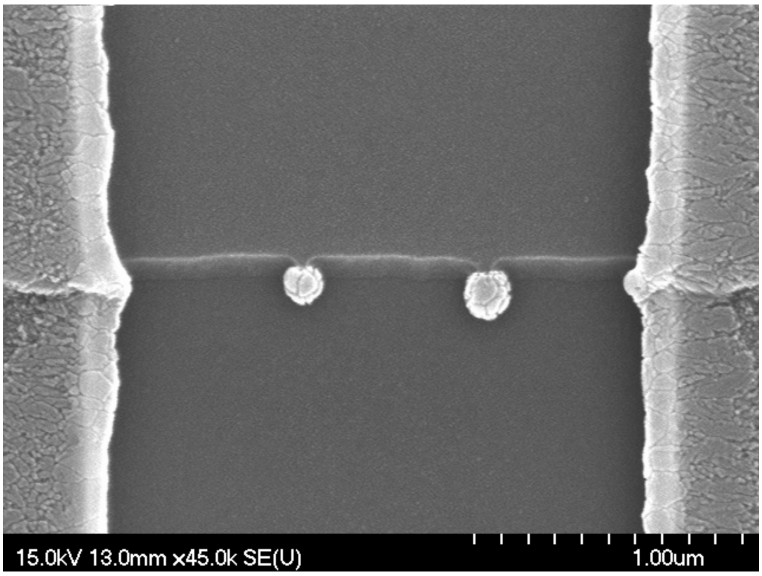


Fig. 4-3 Si nano-dots formation after excimer laser irradiation with 200 mJ/cm^2 and without capping oxide.

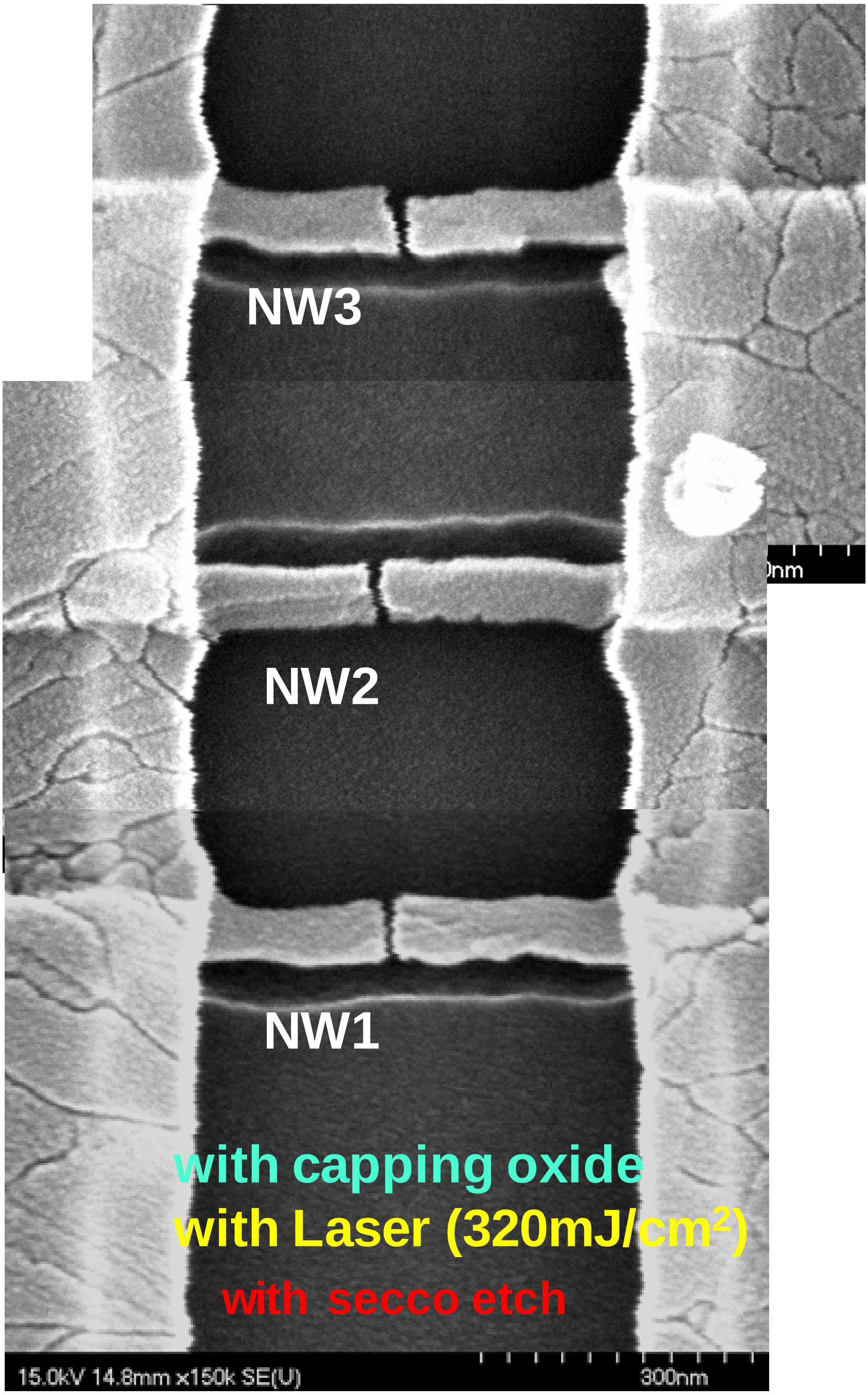


Fig. 4-4 (a) SEM graphs of laser-crystallized poly-Si nanowire after the Secco-etch treatment.

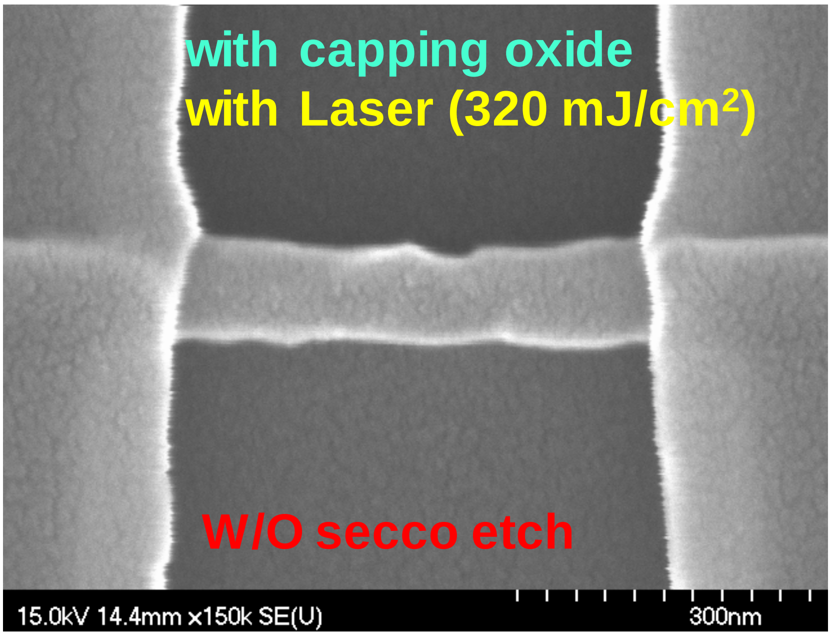


Fig. 4-4 (b) SEM graphs of laser-crystallized poly-Si nanowire before the Secco-etch treatment.

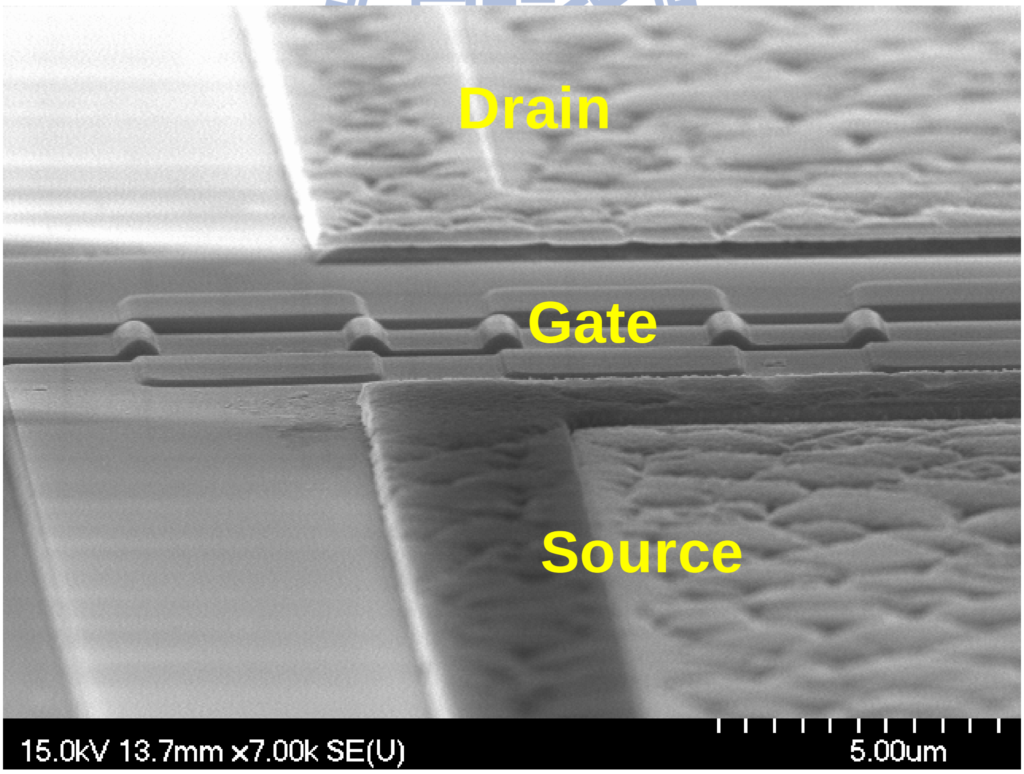


Fig. 4-5 (a) SEM observation of the fabricated excimer-laser-crystallized nanowire GAA TFT

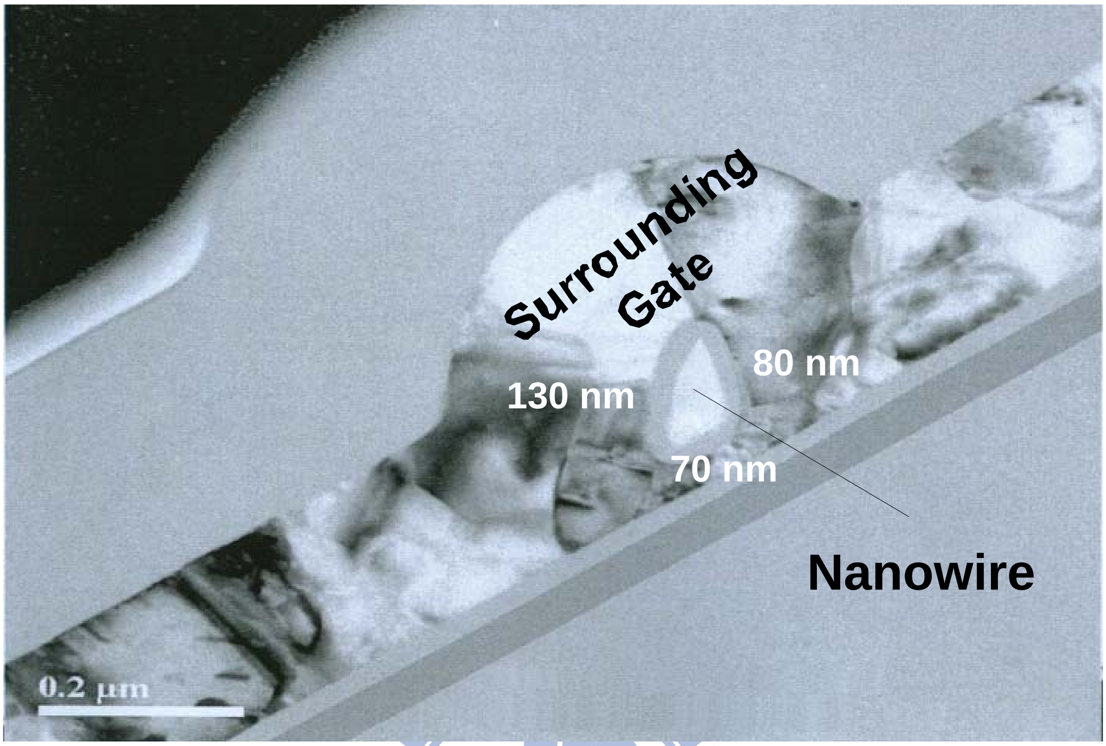


Fig. 4-5 (b) X-TEM observation of excimer-laser-crystallized nanowire GAA TFT

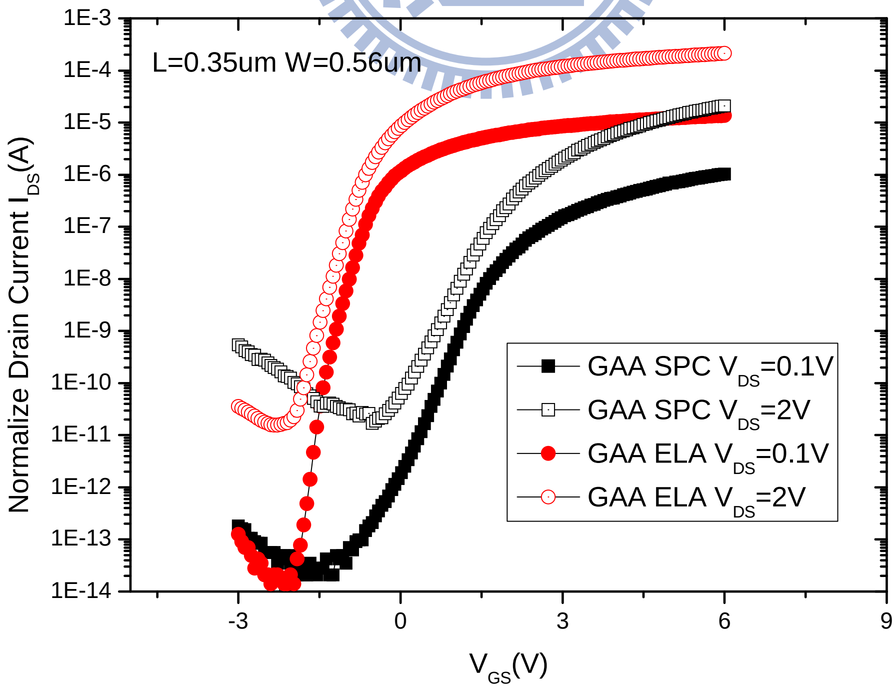


Fig. 4-6 The comparison of normalized transfer characteristics between GAA-ELA MNC TFTs and GAA-SPC MNC TFTs.

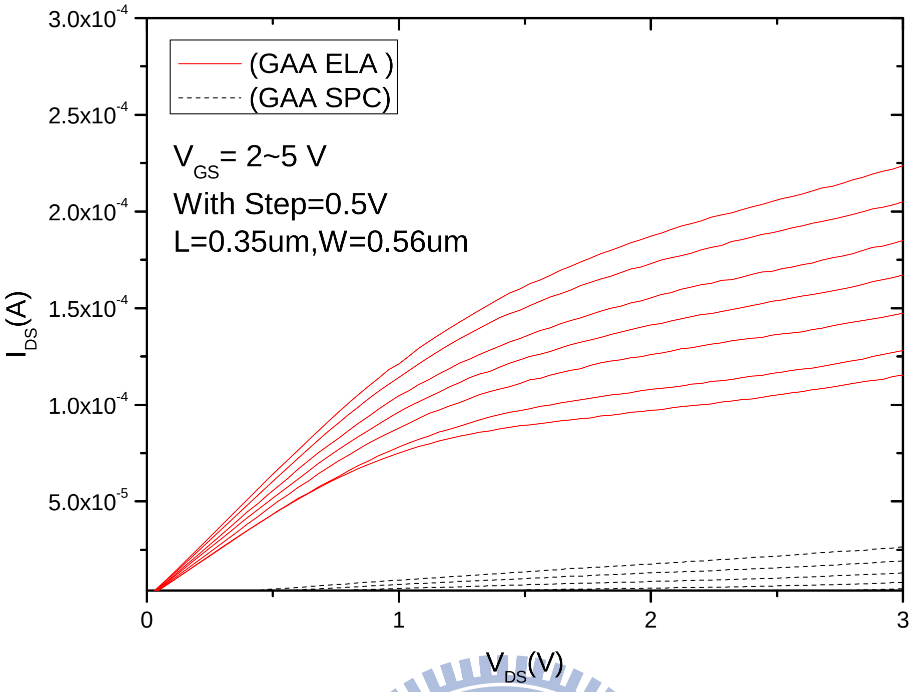


Fig. 4-7 The output characteristics of GAA-ELA MNC TFTs as compared to CP-ELA TFTs.

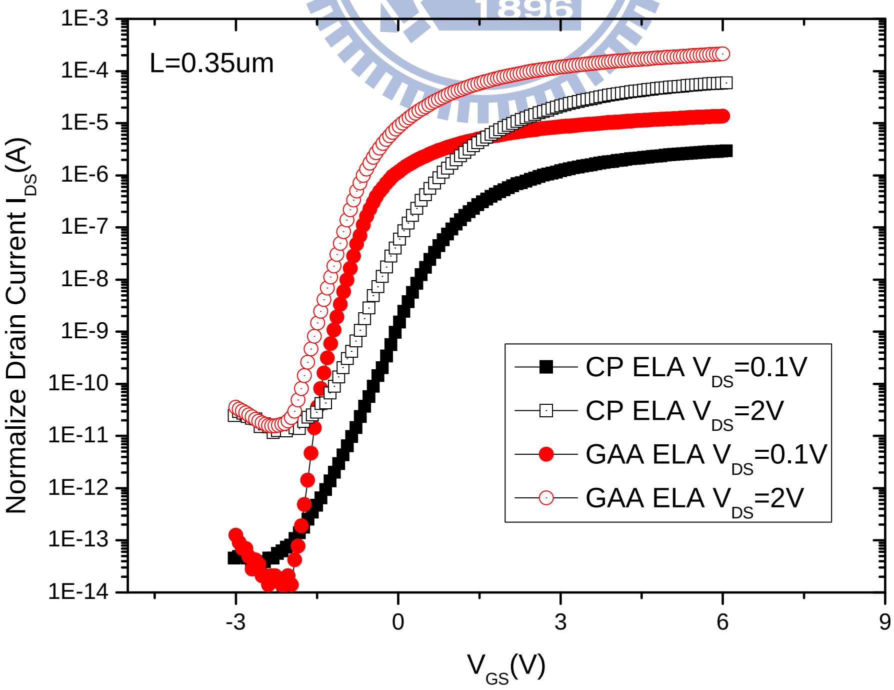


Fig. 4-8 The comparison of normalized transfer characteristics between GAA-ELA MNC TFTs and CP-ELA TFTs.

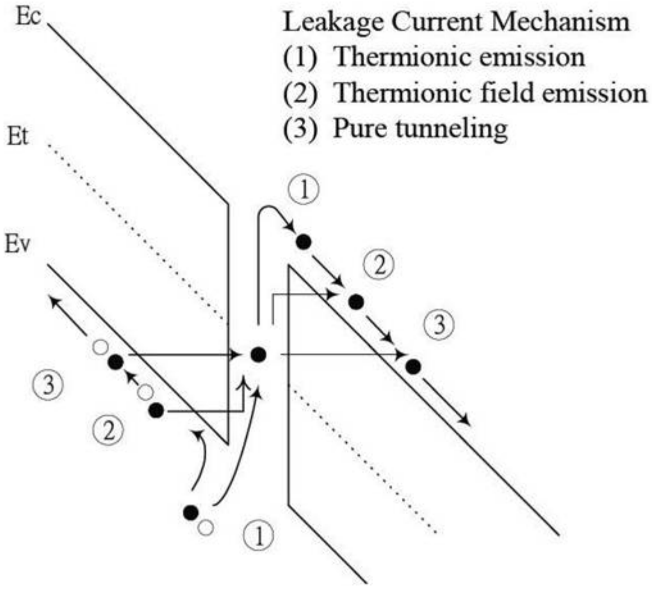


Fig. 4-9 Leakage current mechanisms.
(1) Thermionic emission
(2) Thermionic filed emission
(3) Pure tunneling (ban-to-band tunneling)

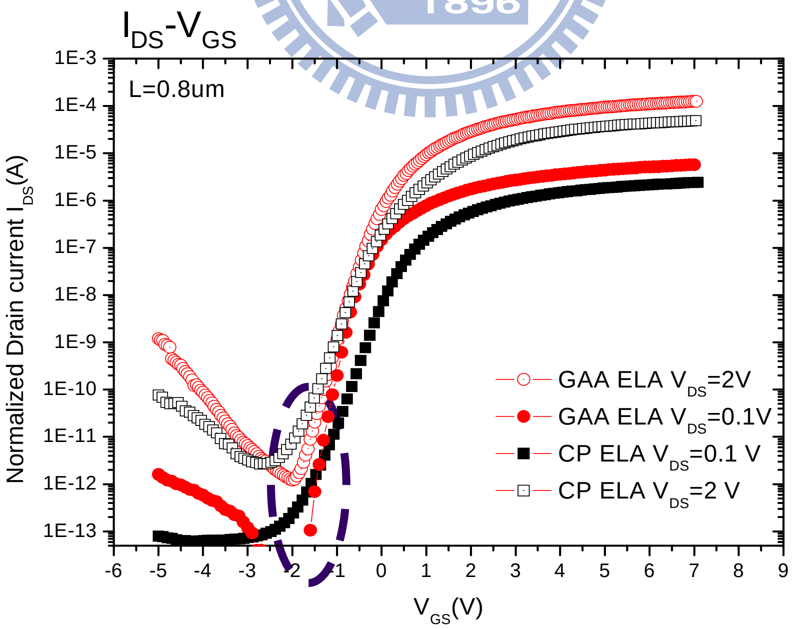


Fig. 4-10 The low leakage current at the low gate electric field region of GAA-ELA MNC TFTs as compared to CP TFTs.

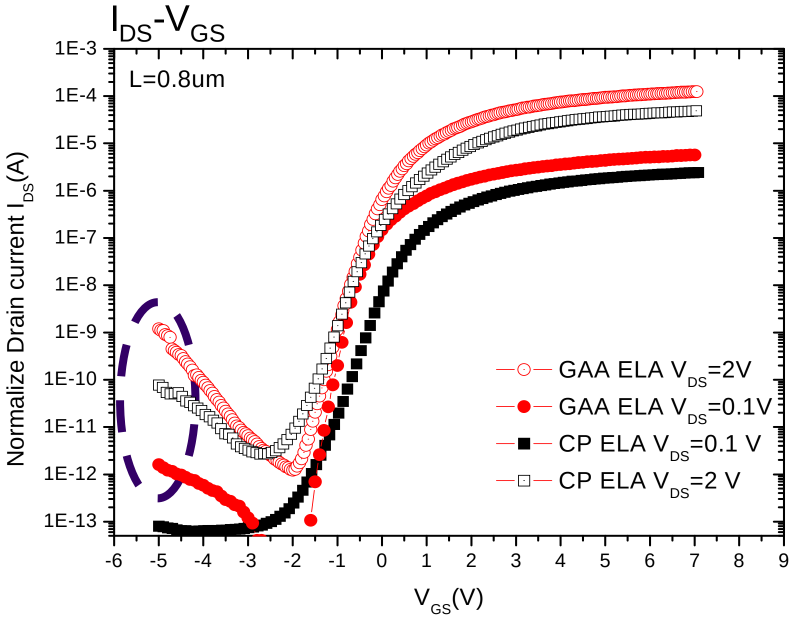


Fig. 4-11 The high leakage current at the high gate electric field region of GAA-ELA MNC TFTs as compared to CP TFTs.

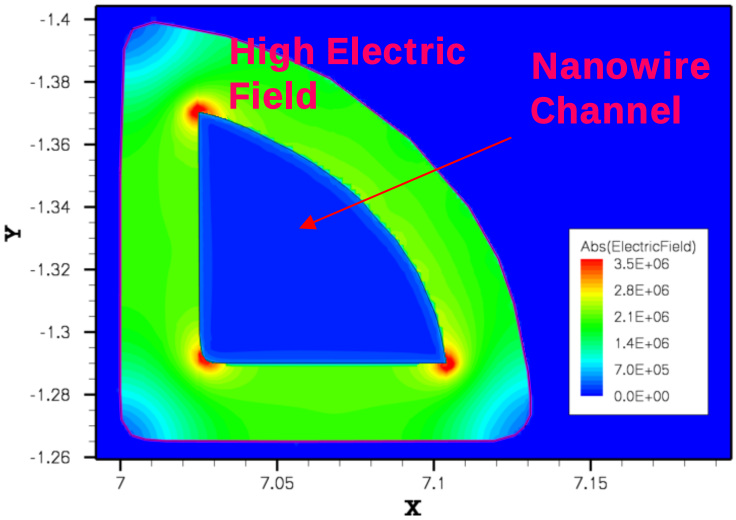


Fig. 4-12 The electric field simulation of GAA-ELA with multiple nanowire channels TFTs by ISE-DESSIS.

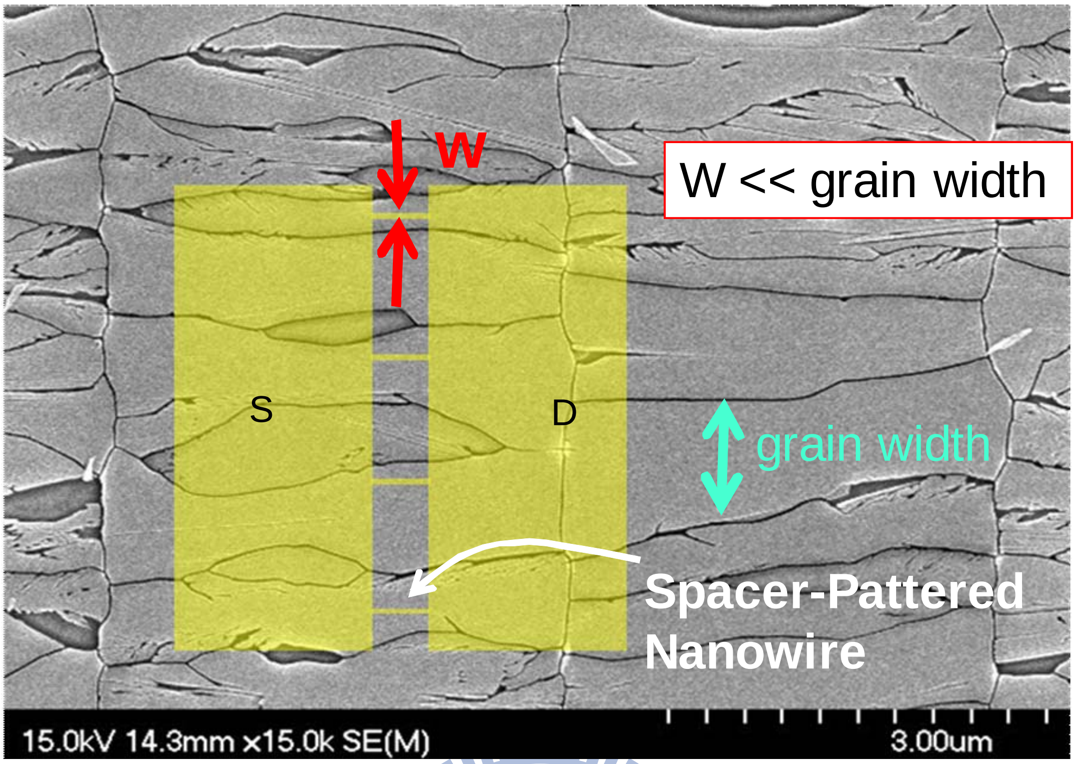


Fig. 4-13 The uniformly-distributed poly-Si grain with size of 3 × 0.8 μm^2 in average prepared by SLS crystallization.

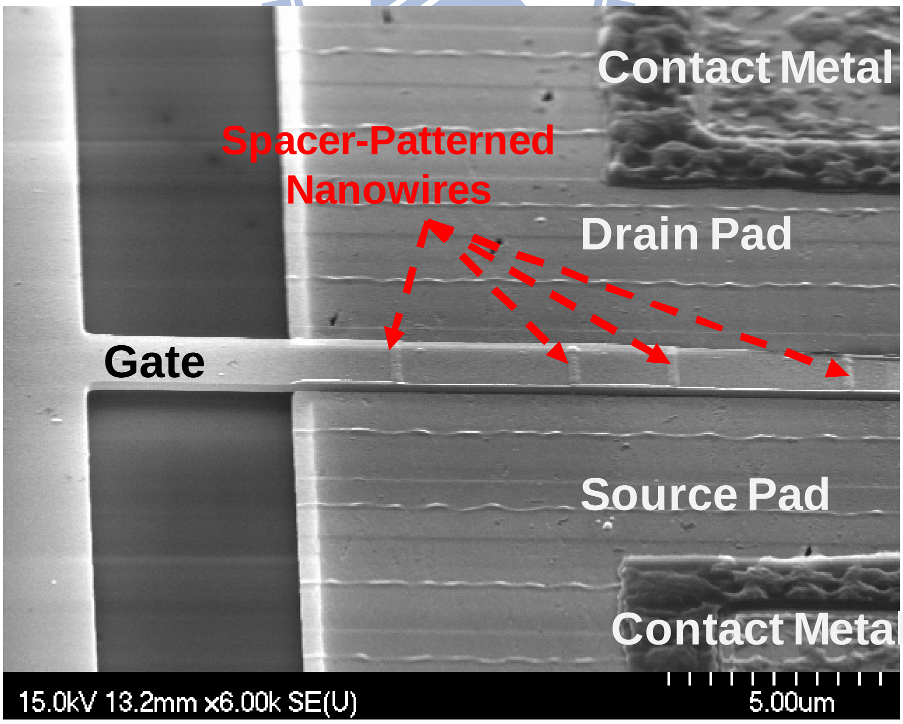


Fig. 4-14 SEM observation of the fabricated spacer-patterned-nanowire Tri-Gate TFT

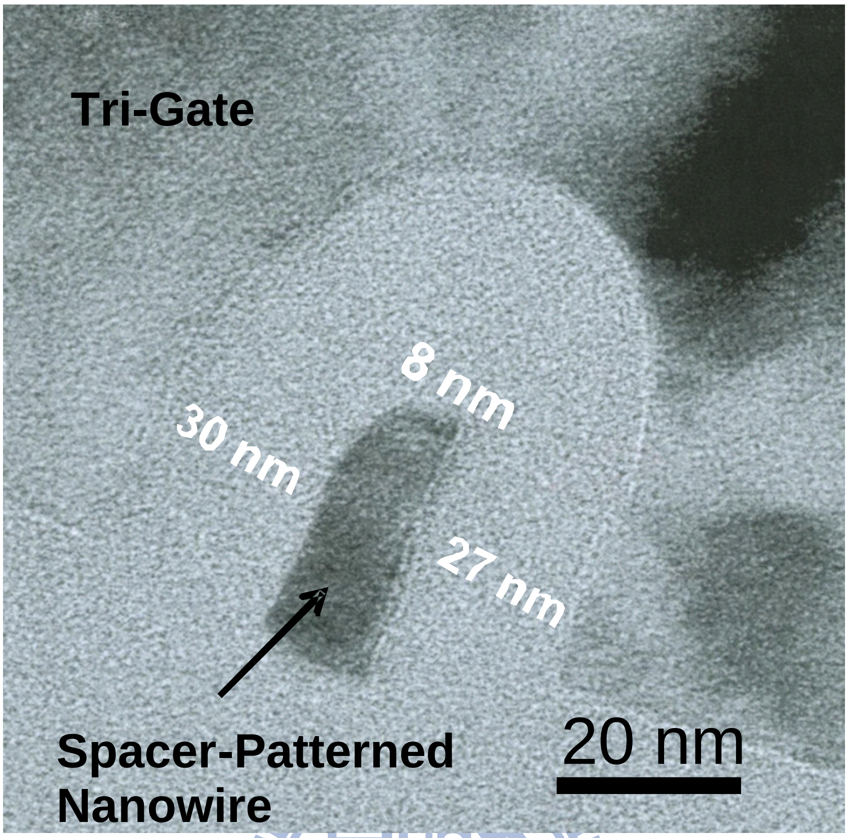


Fig. 4-15 The correspondingly cross-section TEM image of the spacer-patterned-nanowire tri-gate TFT.

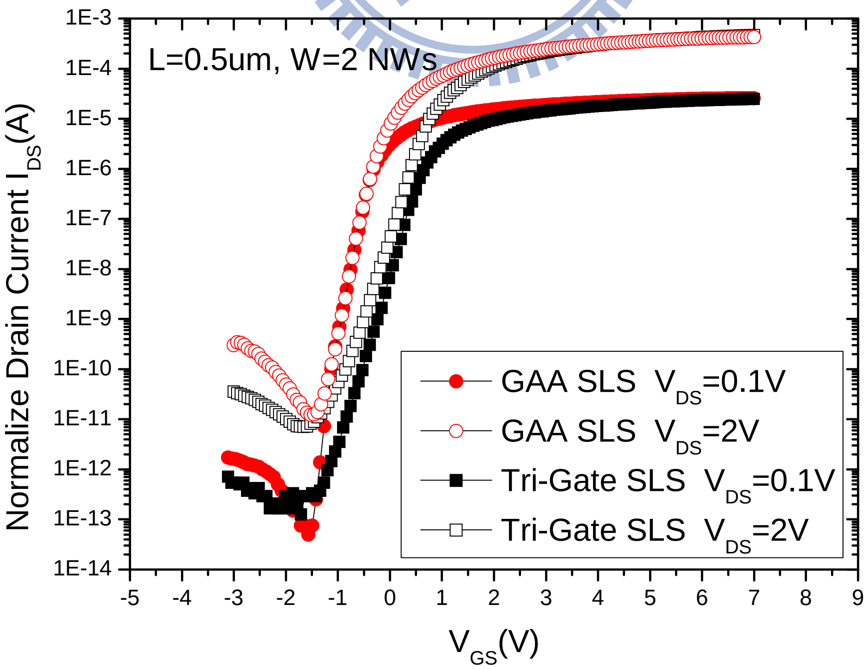


Fig. 4-16 The normalized transfer characteristics of GAA-SLS MNCs with Tri-Gate-SLS MNCs TFTs.

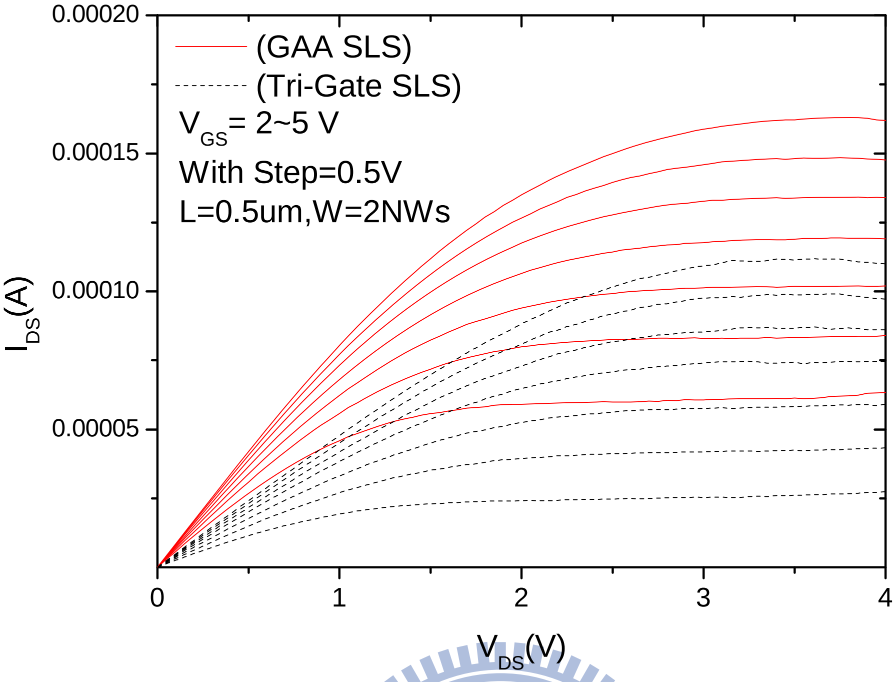


Fig. 4-17 The output characteristics of GAA-SLS MNCs with Tri-Gate-SLS MNCs TFTs.

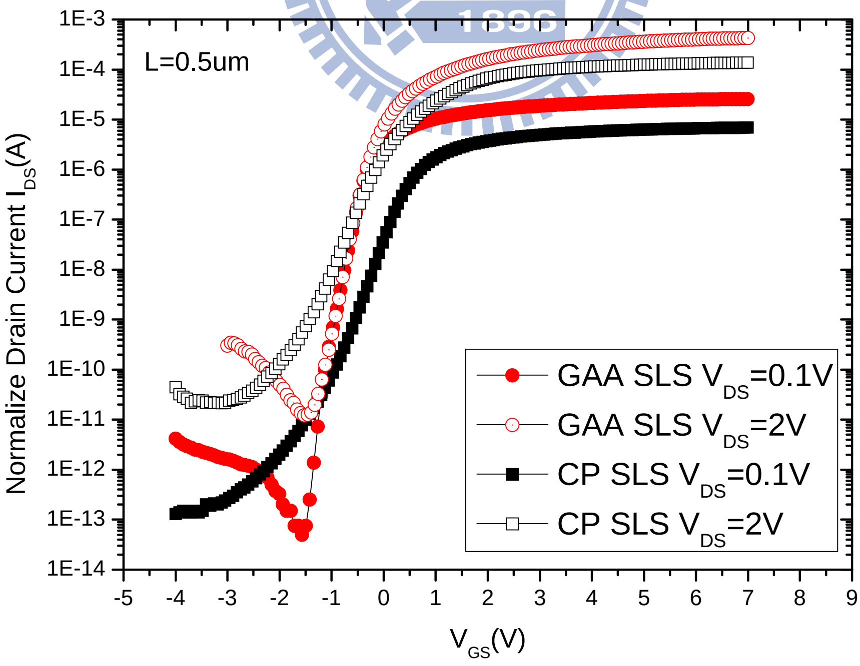


Fig. 4-18 The normalized transfer characteristics of GAA-SLS MNCs with CP-SLS TFTs.

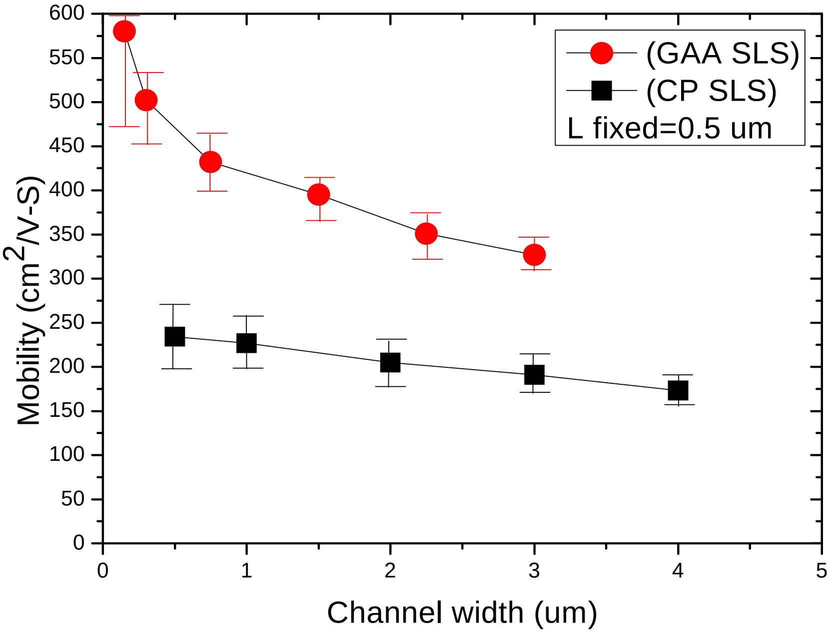


Fig. 4-19 The comparison of GAA-SLS MNC TFTs and CP-SLS TFTs with fixed channel in 0.5 μm and various channel width from 0.15 to 4 μm.

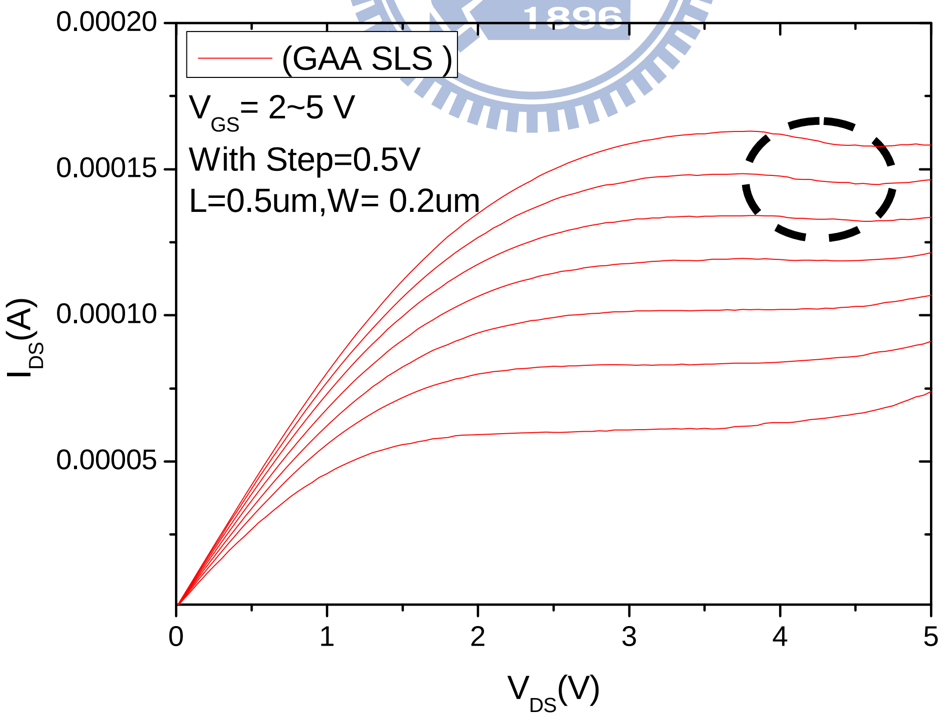


Fig. 4-20 The output characteristics of GAA-SLS MNC TFTs.

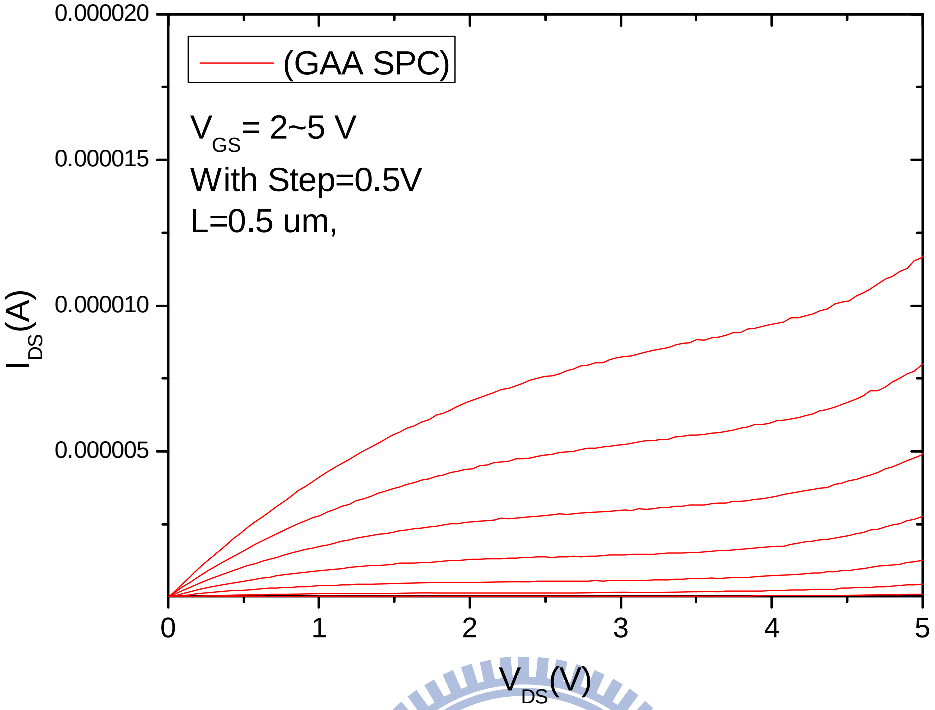


Fig. 4-21 The output characteristics of GAA-SPC MNC TFTs

Chapter 5

Novel Field-Enhanced-Nanowire Poly-Si TFT Nonvolatile Memories with Gate-All-Around Structures

5.1 Introduction

Poly-Si thin film transistors (TFTs) have been widely used as pixel switching elements in active-matrix displays. For further achieving system-on-panel (SOP) applications, other functional elements based on poly-Si TFT technology, such as memories, sensors, drivers, and controllers, are also needed to develop to fully integrate on the same display panel [5.1]-[5.6]. It is well-known that the nonvolatile memory (NVM) is a critical element for data storage, signal processing, and power saving in portable electronic systems [5.7]. And, due to the process compatibility with poly-Si TFT, silicon–oxide–nitride–oxide–silicon (SONOS)-type devices, instead of traditional floating-gate ones, have been considered as a promising NVM candidate for SOP applications [5.6], [5.8], [5.9]. However, unlike floating-gate NVM, conventional planar (CP) SONOS memories do not have gate-coupling design, thus suffering from the insufficient programming/erasing (P/E) efficiency [5.10]. To improve this issue for TFT SONOS, field-enhanced corner tips, produced by sequential lateral solidified (SLS) crystallization or E-beam lithography, has been reported to improve the P/E speed [5.6]. However, the location control of SLS tips and low-throughput of E-beam arise the process complexity and cost issue [5.11]. In this chapter, based on previous proposed gate-all-around structure, two kinds of trapping-charge memory devices with field-enhanced nanowire and/or silicon-oxide-vacuum-oxide-silicon (SONVAS) structures were proposed to improve the memory performance and reliability with a simple process sequence.

5.2 Experiments

5.2.1 Fabrication Sequence of Field-Enhanced-Nanowire Poly-Si TFT SONOS Memory with a Gate-All-Around Structure

The proposed FEN poly-Si TFT SONOS device was schematically shown in Fig. 5-1 [5.12]. At first, a 50-nm-thick Si_3N_4 (as etch-stop layer) and a 300-nm-thick tetra-ethyl-ortho-silicate (TEOS) SiO_2 (as sacrificial layer) films were sequentially deposited in low pressure chemical vapor deposition (LPCVD) system on oxidized silicon wafer. Several strips with step height of 100 nm were patterned on surface of the sacrificial SiO_2 layer by reactive ion etch (RIE), and followed by a conformal deposition of 100-nm-thick a-Si layer. After source/drain (S/D)-pad lithography and its RIE process, couples of spacer nanowires were *in-situ* resided against the sidewall of those designed strips and naturally connected to the S/D pads, which were formed to be the device active region. It should be noted that each spacer nanowire inherently features three sharp corners, and its nano-dimension is simply controlled with RIE time without any advanced lithography [5.12]-[5.14]. Subsequently, a solid phase crystallization at 600 ˚C in N_2 ambient for 24 hours was performed to transform the a-Si into poly-Si. After the SiO_2 strip removing by diluted hydro-fluoric acid (DHF), the tunneling oxide, nitride storage, blocking oxide (ONO: 5 nm/10 nm/10 nm), and 200-nm-thick phosphorous *in-situ* doped poly-Si were sequentially deposited to wrap around those suspending spacer nanowires by LPCVD system, as shown in Figs. 5-2 and 5-3. Fig. 5-4 shows the corresponding cross-sectional transmission electron microscopy (XTEM) image of the ONO dielectrics and poly-Si gate which were conformally deposited on the top sharp corner. After gate patterning and self-aligned phosphorous implantation, the passivation oxide deposition and S/D activation were sequentially performed. Finally, standard contact opening and metallization were carried out to complete the fabrication. For comparison, the conventional planar (CP) poly-Si TFTs were also fabricated with the same process sequence.

5.2.2 Fabrication Sequence of Field-Enhanced-Nanowire Poly-Si TFT SONVAS Memory with a Gate-All-Around Structure

The fabrication sequence of proposed FEN Poly-Si TFT SONOS memory has been described in the previous section. A 5-nm-thick tunneling oxide, a 10-nm-thick nitride trap layer, a 10-nm-thick blocking oxide, and a 200-nm-thick phosphorous in-situ doped poly-Si were sequentially deposited conformally to wrap around those suspending spacer nanowires by LPCVD systems after sacrificial oxide was removed by diluted HF. After patterning gate, the *in-situ* doped poly-Si gate, blocking oxide and Si_3N_4 trap layer were etched out by RIE, while the tunneling oxide was kept remaining, as shown in cross-section schematic image in Fig. 5-5. A phosphorous ion implantation was performed with a dosage of 5×10^{15} cm^{-2} and a energy of 35 keV. A 200-nm-thick Si_3N_4 was deposited and then etched back to form two Si_3N_4 spacers resided against the poly-Si gate as shown in cross-section schematic image in Fig. 5-6. The tunneling oxide was then side-etched for 350 nm in length by 1:10 diluted BOE immersion as shown in Fig. 5-7. A 300-nm-thick passivation oxide was deposited by SiH_4-based PECVD system and the following processes were same as the previous FEN TFT SONOS device. The FEN TFT SONVAS structure is shown in cross-section schematic image in Fig. 5-8.

5. 3 Results and Discussion

5.3.1 Electrical Characteristics of Field-Enhanced-Nanowire Poly-Si TFT SONOS Memory with a Gate-All-Around Structure

Both FEN- and CP-TFT SONOS devices were characterized for transistor and memory performances. Those devices have a gate length (L) of 1 μm and a channel width (W) of 3 μm, where the W of FEN-TFT SONOS is defined by 10 nanowires with 5-strip structure [5.12]. The threshold voltage (V_{th}) is defined by the criterion $I_{DS} = (W/L) \times 10^{-8}$ A at $V_{DS} = 0.1$ V. For memory operations, in this work, the TFT SONOS memory is programmed and erased by Fowler-Nordheim (FN) tunneling mechanism. Figs. 5-9 (a) and 5-9 (b) show the transfer characteristics of the CP and the proposed FEN TFT SONOS devices after DC stress at V_{GS}= 7 V condition. The results, clearly, indicate the transfer characteristics are the same even the stress time is 1000 seconds. Thus, the read disturb can be neglected under the normal transistor operation. Figs. 5-10 and 5-11 show the transfer characteristics of the CP and FEN TFT SONOS devices with various programming times at a gate voltage of 15 V, respectively. For erasing operations, the transfer characteristics of the CP and FEN TFT SONOS devices with various erasing times at gate voltage of -15 V are shown in Figs. 5-12 and 5-13, respectively. It is obviously found that the program/erase (P/E) efficiency of the FEN TFT SONOS device is significantly better than the CP one. In the programming characteristics, the FEN TFT SONOS exhibit a large V_{th} shift of 2.71 V in 1×10^{-3} seconds at a gate pulse of +15 V, while there is only 0.49 V shift in CP device. The erase characteristics also show that the FEN TFT SONOS devices are much faster (a V_{th} shift of 2.11 V in 1×10^{-3} seconds at a gate pulse of -15 V) than the CP counterparts. The improvement on P/E speed and window can be attributed to the field enhancement from the three sharp corners to promote carrier injection through the tunneling oxide into the nitride storage layer. The V_{th} shifts after programming and erasing operation for the CP and FEN TFT SONOS devices with various voltages are plotted in Figs. 5-14 (a) and 5-14 (b).

For further clarifying this P/E efficiency enhancement, the simulations of electrical fields for the CP and FEN TFT SONOS structures were performed by ISE-TCAD simulator. The distribution of electrical field and band diagrams across the stacked ONO dielectrics was numerically simulated at a gate bias of 15 V for the CP and FEN TFT SONOS devices as shown in Figs. 5-15 and 5-16, respectively. The sharp geometry of these three corners enhances the electric field at the Si/tunneling oxide interface and depresses the electric field in the blocking oxide. The large field at the Si/tunneling oxide interface enhances the carrier-injection probability and thus increases both the P/E speeds of FEN TFT SONOS device. In addition, the reduction of the electric field in the blocking oxide prevents charges tunneling from the nitride to the poly-gate and from the poly-gate to the nitride. The P/E activity is thus facilitated between the channel and tunneling oxide rather than between the blocking oxide and the gate. In contrast, for CP SONOS structures, as shown in Fig. 5-15, the electric field in the tunneling oxide is equal to that in the blocking oxide, leading to lower P/E efficiency. In addition, Fig. 5-16 exhibits the FEN TFT SONOS device has shorter tunneling distance than the CP SONOS device. Fig. 5-17 shows the retention characteristic after 10^4 P/E cycles for FEN TFT SONOS device, where the memory window is maintained up to the tested time of 10^4 seconds. It shows the memory window will be 1.1 V after extrapolating to retention time of 10 years. The program-state V_{th} drops negligibly; however, there is some charge loss (V_{th} loss from 2.05 to 2.4 V) in erase state from 1 to 100 seconds. This is because some holes are trapped insecurely at the trap states in the tunneling oxide instead of nitride storage layer during erasing, and then those trapped hole are detrapped easily from tunneling oxide to channel during the early retention test. In addition, the endurance reliability of FEN TFT SONOS device is shown in Fig. 5-18, the memory window is kept 1.68 V but V_{th} rises about 1 V after 10^4 P/E cycles. The rising of memory window results from that the charges trapped in Si_3N_4 deep level traps are hard to be erased and the subthreshold swing is degraded due to the tunneling oxide is damaged during P/E cycles.

5.3.2 Electrical Characteristics of Field-Enhanced-Nanowire Poly-Si TFT SONVAS Memory with a Gate-All-Around Structure

Fig. 5-19 exhibits the tiled-view SEM image of the FEN TFT SONVAS device. It shows the nitride spacers resided against the sidewall of the gate and S/D extentions and the empty gap was existed between the gate and the nanowire channel. The cross-section schematic image of nanowire channel with vacuum tunneling layer is shown in Fig. 5-20.

In this work, the FEN TFT SONVAS memory is also programmed and erased by Fowler-Nordheim (FN) tunneling mechanism. Fig. 5-21 show the transfer characteristics of the FEN TFT SONVAS devices with various programming times at a gate voltage of 15 V. For erasing operations, the transfer characteristics of the FEN TFT SONVAS devices with various erasing times at gate voltage of -15 V are shown in Figs. 5-22. The V_{th} shifts after programming and erasing operation with various times at a gate voltage of 15 and -15 V, respectively, for the CP, FEN TFT SONOS and FEN TFT SONVAS devices are listed in Table 5-1 and compared in Figs. 5-23 and 5-24. It is obvious that the program/erase (P/E) efficiency of the FEN TFT SONVAS device is much improved as compared to that of the FEN TFT SONOS especially from initial to 1 μsec, which is ascribed to the further field enhancement of the lowest k property of vacuum. Since carriers are only facilitated to trap in the local states near the three sharp corners of such FEN structure, the improvement of FEN SONVAS compared to FEN SONOS become approximated constant with longer operation time, which may be attributed to the dominance of the trap-state volume rather than the field enhancement.

For further clarifying this P/E efficiency enhancement, the simulations of electrical field for the FEN TFT SONOS and FEN TFT SONVAS structures were performed by ISE-TCAD simulator. The distribution of electrical field across the stacked ONO dielectrics was numerically simulated at a gate bias of 15 V for the FEN TFT SONOS and FEN TFT SONVAS devices as shown in Figs. 5-25 and 5-26, respectively. Figs. 5-25 and 5-26 indicate that the FEN TFT SONVAS device has larger electric field in the tunneling layer and lower electric field in the blocking oxide. Due to the low-k property of vacuum, there is higher percentage of voltage dropped in the vacuum layer, resulting in larger electric field in the vacuum layer. The large field in the vacuum layer enhances the carrier-injection probability and thus increases both the P/E speeds in FEN TFT SONVAS device. In addition, the reduction of the electric field in the blocking oxide prevents charges tunneling from the nitride to the poly-gate and from the poly-gate to the nitride. The P/E activity is thus facilitated between the channel and vacuum layer rather than between the blocking oxide and the gate. The band diagram was numerically simulated at a gate bias of 15 V for the FEN TFT SONVAS device as shown in Fig. 5-27. It shows the FEN TFT SONVAS device also has short tunneling distance. Fig. 5-28 shows the retention characteristics of FEN TFT SONOS and FEN TFT SONVAS devices after 10^4 cycles, where the memory window of FEN TFT SONVAS device is maintained with little degradation up to the tested time of 10^4 sec. It shows the memory window will be larger than 1.4 V after extrapolating to retention time of 10 years. The larger memory window after extrapolating to retention time of 10 years for FEN TFT SONVAS device results from its higher P/E speed. The endurance characteristic of FEN TFT SONVAS device is shown in Fig. 5-29. The 2.4 V memory window was kept and the window rises only 0.5 V after 10^4 P/E cycles. The less memory window shift after 10^4 P/E cycles for FEN TFT SONVAS device results from less dangling bonds and interface traps produced during P/E cycles. The subthreshold swing of FEN TFT SONOS and FEN TFT

SONVAS devices after P/E cycles is shown in Fig. 5-30 and Table 5-2, respectively. The subthreshold swing of FEN TFT SONOS device degraded from 390 to 523 mV/decade and that of FEN TFT SONVAS device only degraded from 345 to 384 mV/decade after 10^4 P/E cycles.

5.4 Summary

In this chapter, novel FEN TFT SONOS and FEN TFT SONVAS memory devices with gate-all-around structures have been demonstrated.

First, a simple and cost-effective method was performed to fabricate the FEN TFT SONOS device. The simple spacer technique was used to form the nanowire channels without any advanced lithography. The FEN TFT SONOS devices have superior performance than CP SONOS devices with higher on current, smaller V_{th}, steeper subthreshold swing (SS), higher on/off ratio, and higher mobility, which are contributed to the enhanced gate controllability by the three sharp corners and GAA structure together with the reduced number of grain-boundary defects in the nanowire channel. In addition, the proposed FEN TFT SONOS device exhibits higher P/E speed due to much enhanced electric field in the tunneling layer and lower electric field in the blocking oxide as compared to the CP SONOS devices. The FEN TFT SONOS device exhibited a V_{th} shift of 2.71 V and 2.11 V at V_{GS} = +15/-15 V in 1×10^{-3} seconds for FN programming and erasing operations, respectively; while the reference CP SONOS devices only showed the negligible change. And, the FEN TFT SONOS devices also showed stable retention and reasonable endurance characteristics. For retention, the FEN TFT SONOS device maintained 1.1-V memory window after ten years. For endurance, the FEN TFT SONOS device kept 1.68 V memory window after 10^4 P/E cycles.

Second, a novel FEN TFT SONVAS device which the original tunneling oxide was replaced with vacuum is demonstrated as well. The proposed FEN TFT SONVAS device exhibits higher P/E speed than FEN TFT SONOS device especially in 1 μs due to larger electric field in the vacuum tunneling layer and lower electric field in the blocking oxide. It exhibited a V_{th} shift of 3.17 V and 2.68 V at V_{GS} = +15/-15 V in 1×10^{-3} seconds for programming and erasing operations, respectively. And, the FEN TFT SONVAS device also showed better retention and endurance characteristics. For retention, the FEN TFT SONVAS maintained 1.4-V memory window after ten years. For endurance, the FEN TFT SONVAS kept 2.4-V memory window with only 0.5-V shift.

Since the FEN TFT SONOS and FEN TFT SONVAS devices exhibited excellent performance, such as good electrical characteristics, high P/E efficiency, and stable reliability, they are very promising for the future applications in SOP and 3-D ICs.

Tables

Table 5-1 The V_{th} shifts after programming and erasing operation at a gate voltage 15 V and -15 V, respectively, for the CP, FEN TFT SONOS and FEN TFT SONVAS devices

	CP SONOS	FEN TFT SONOS	FEN TFT SONVAS			CP SONOS	FEN TFT SONOS	FEN TFT SONVAS
Time (sec)	V_{th} - shift (V)				Time (sec)	V_{th} - shift (V)		
1.E-06	*0.35*	*1.48*	*1.8*		1.E-06	*-0.15*	*-0.27*	*-0.51*
1.E-05	0.42	1.99	2.29		1.E-05	-0.20	-0.57	-0.98
1.E-04	0.44	2.4	2.77		1.E-04	-0.27	-1.67	-2.02
1.E-03	0.49	2.71	3.17		1.E-03	-0.32	-2.11	-2.68
0.01	0.56	3.24	3.78		0.01	-0.48	-2.68	-2.92
0.1	0.78	3.9	4.21		0.1	-0.50	-2.83	-3.13
1	0.95	4.41	4.74		1	-0.54	-3.01	-3.34

Table 5-2 The subthreshold swing of FEN TFT SONOS and FEN TFT SONVAS devices after P/E cycles

	cycles (times)	**initial**	**10**	**100**	**1000**	**10K**
FEN TFT SONVAS	S.S. (mV/decade)	345	347	351	360	**384**
FEN TFT SONOS	S.S. (mV/decade)	390	400	412	457	523

Figures

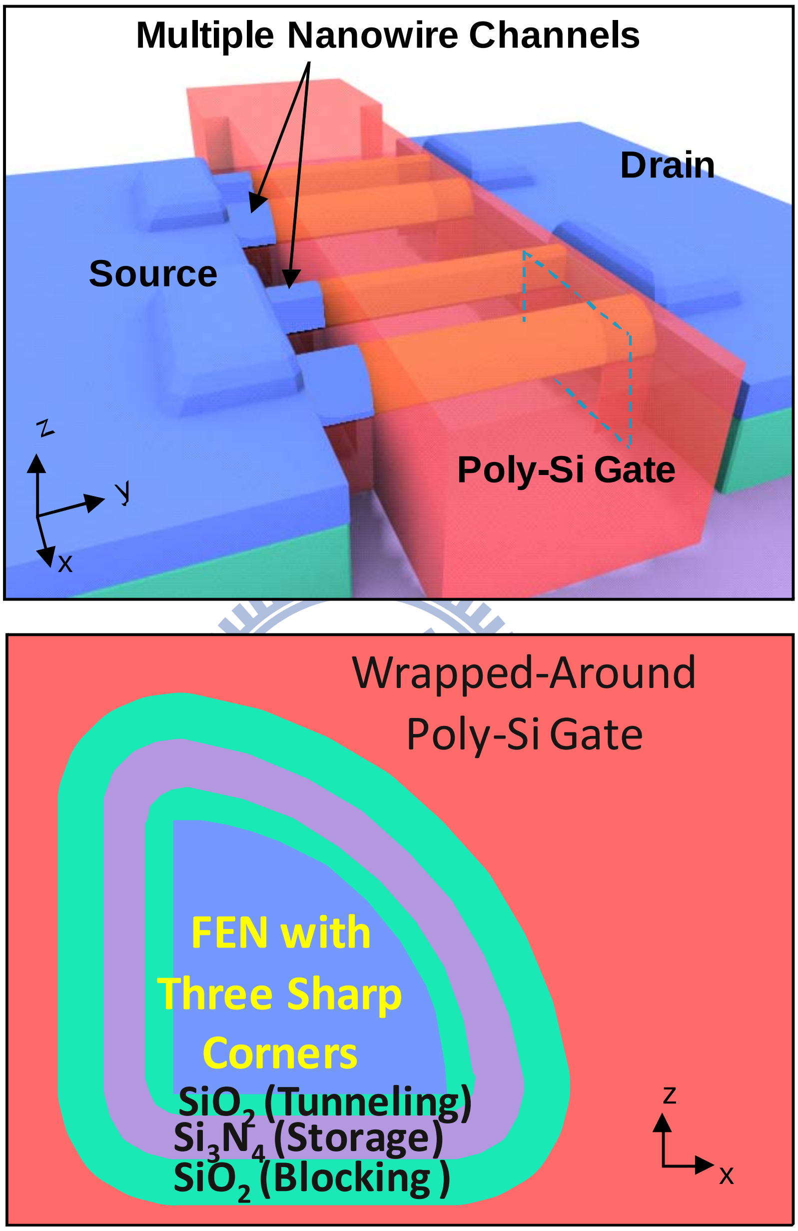


Fig. 5-1. (a) Tilted view of schematic device structure of the proposed FEN-TFT SONOS. (b) Schematic cross-sectional image of each field-enhanced (spacer) nanowire channel with three sharp corners.

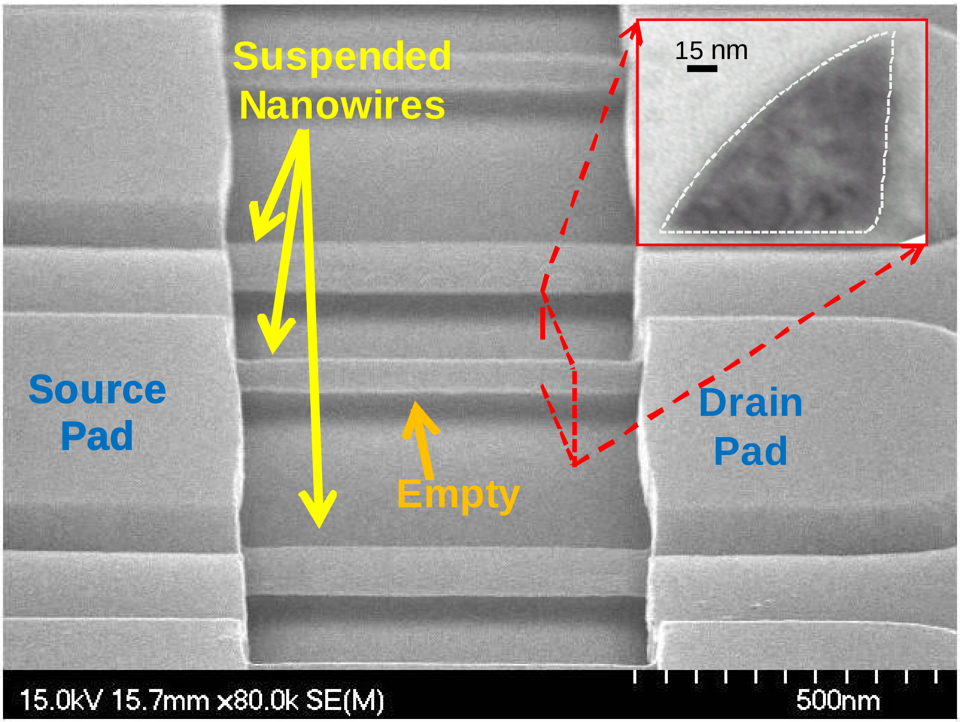


Fig. 5-2. Tilted view of schematic device structure of the proposed FEN-TFT SONOS.

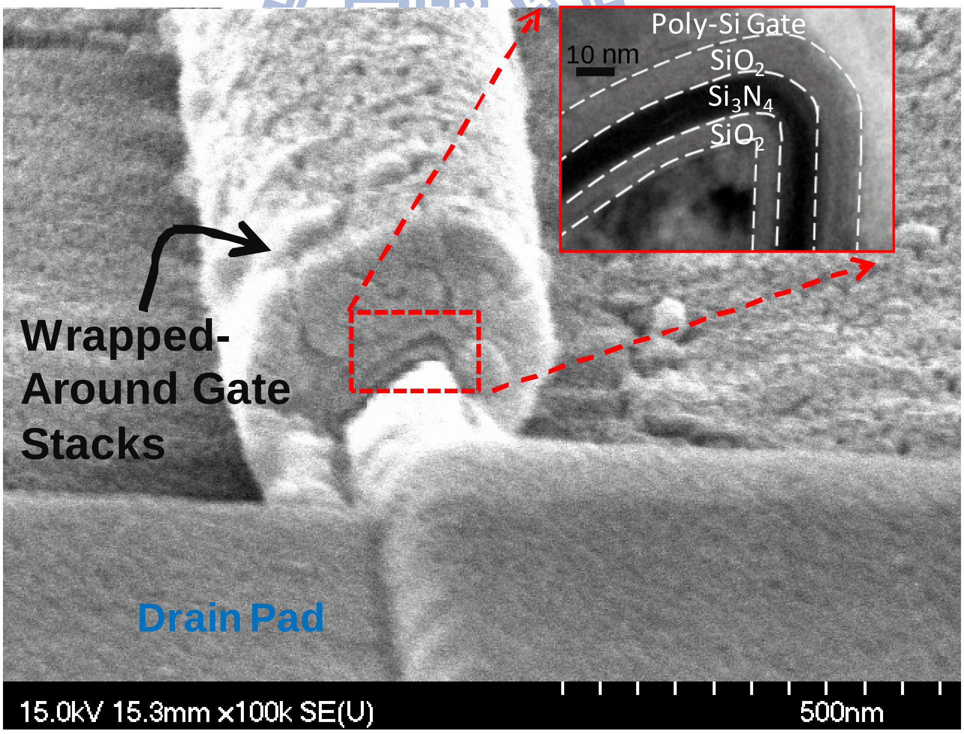


Fig. 5-3. Schematic cross-sectional image of each each field-enhanced (spacer) nanowire channel with three sharp corners. The inset shows its corresponding TEM image of the conformal ONO dielectric deposition on the top sharp corner.

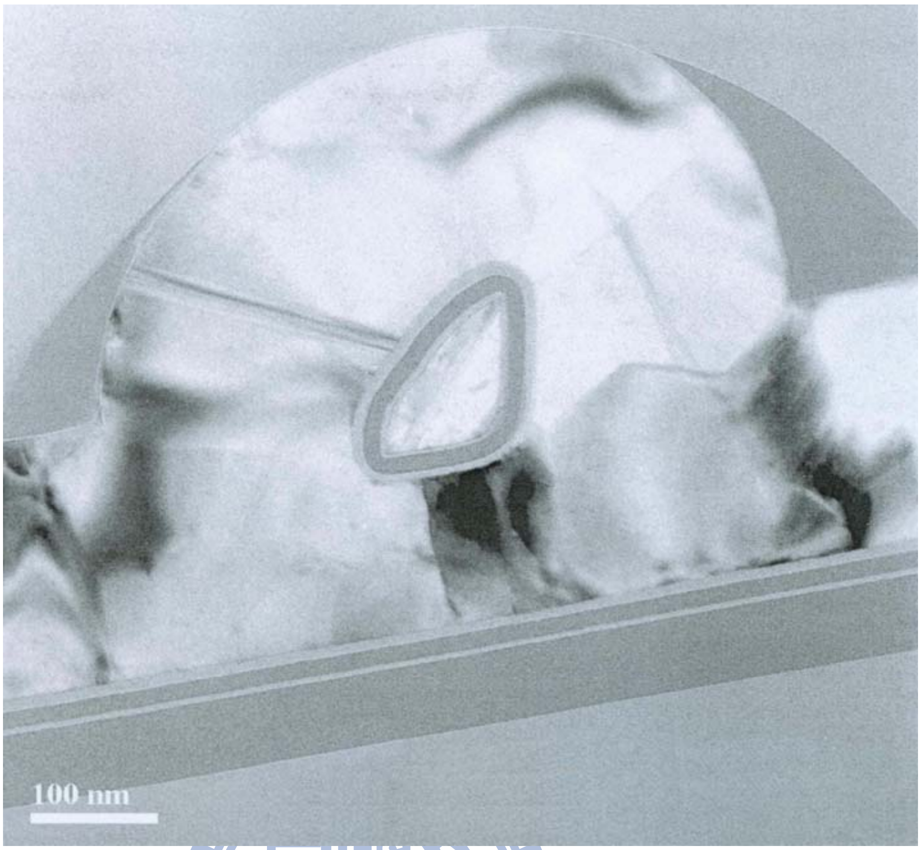


Fig. 5-4 the XTEM image of the conformal ONO dielectric deposition on the three sharp corners of the fabricated FEN TFT SONOS.

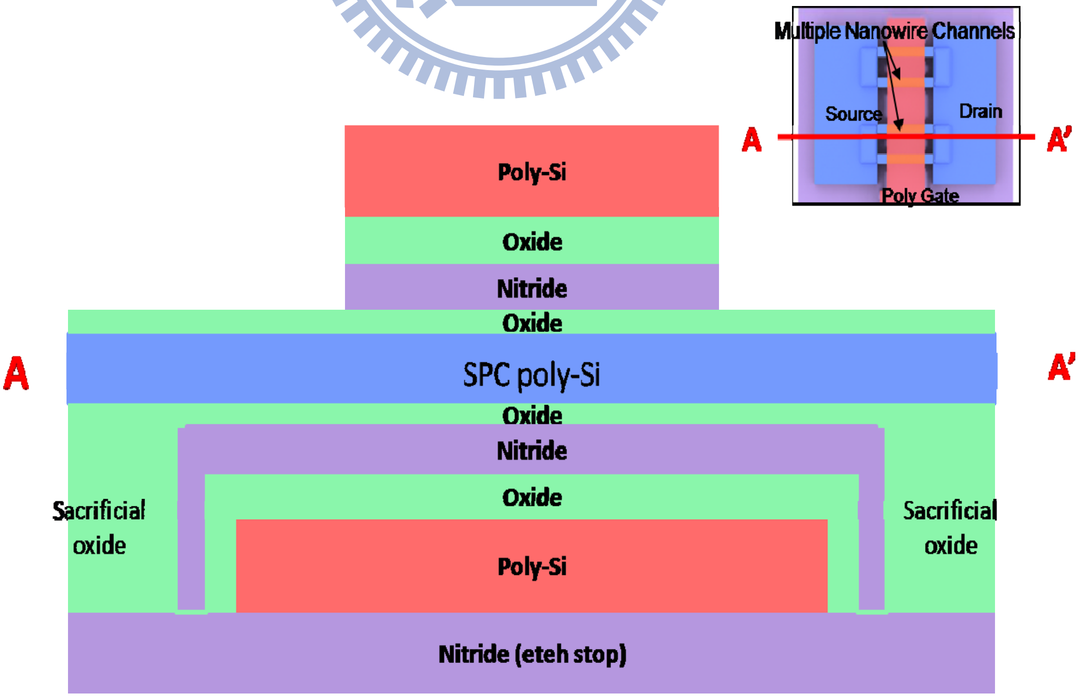


Fig.5-5 The cross-section schematic image after patterning the in-situ doped poly-Si gate

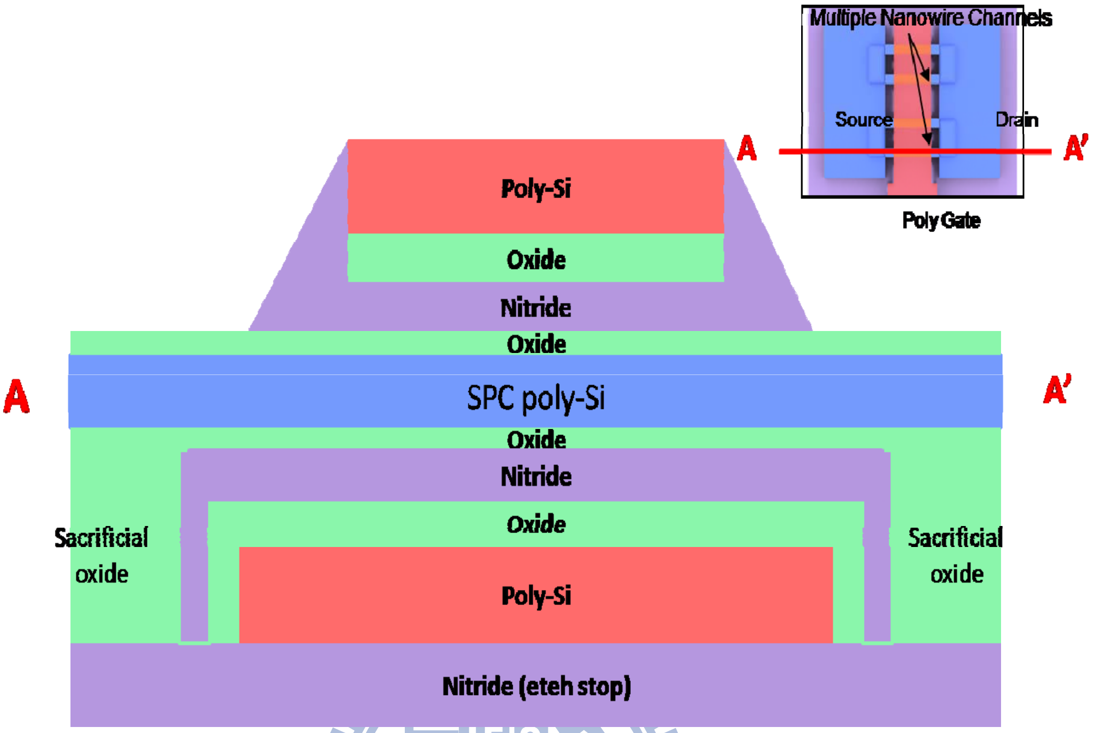


Fig.5-6 The cross-section schematic image after nitride spacers formed.

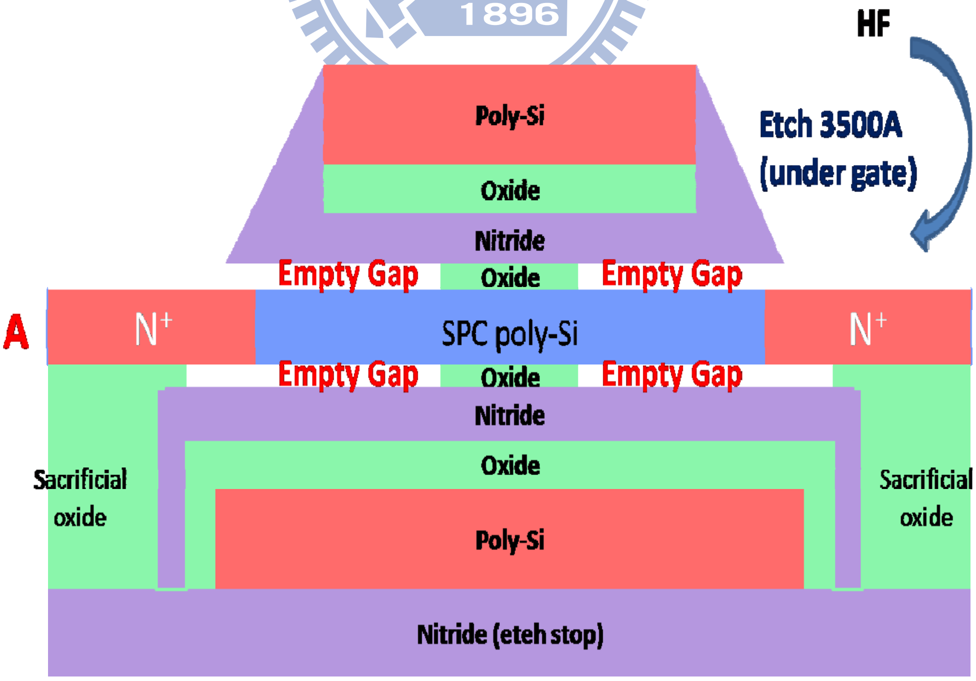


Fig. 5-7 The cross-section schematic image after tunneling oxide etched with 1:10 diluted BOE

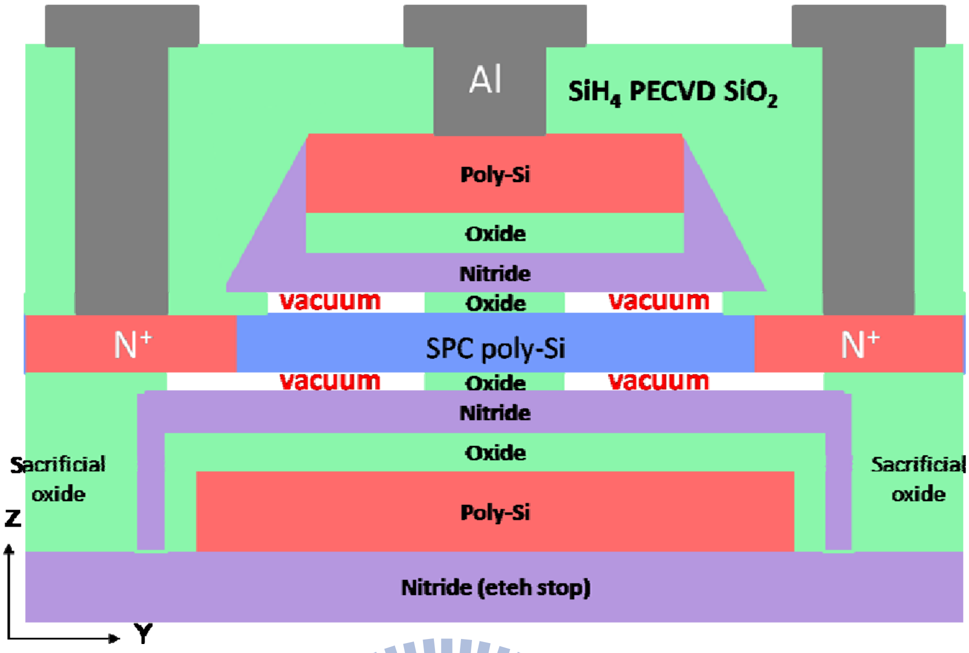


Fig. 5-8 The cross-section schematic image after passivation and metallization.

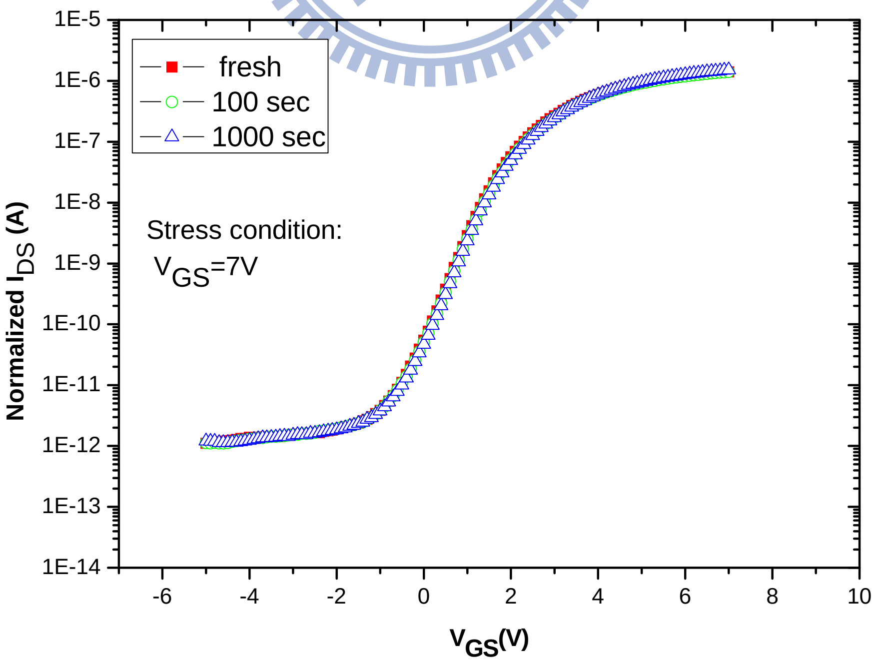


Fig. 5-9 (a) Transfer characteristics of the CP SONOS device after DC stress at V_{GS} = 7 V condition.

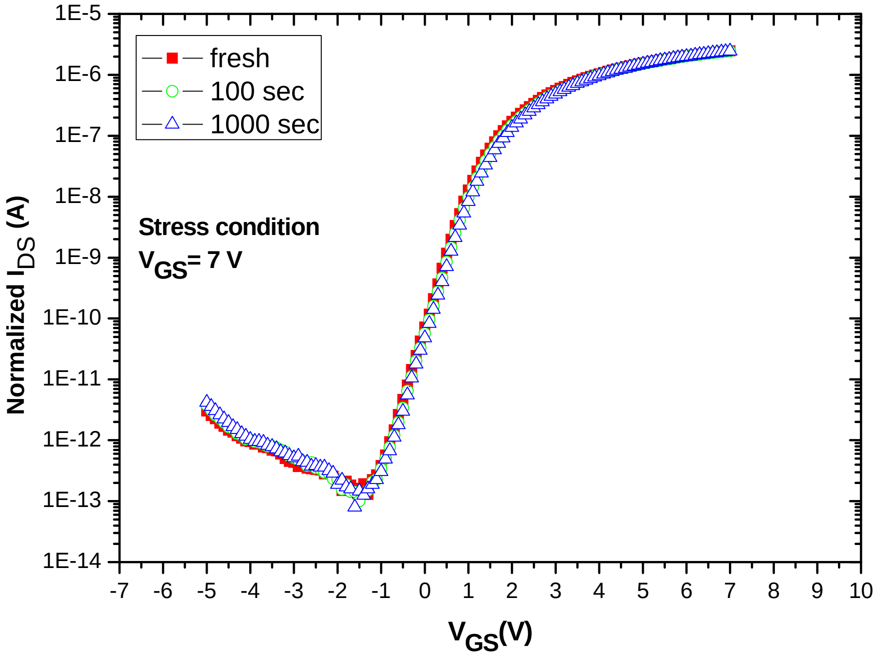


Fig. 5-9 (b) Transfer characteristics of the FEN TFT SONOS device after DC stress at V_{GS} = 7 V condition.

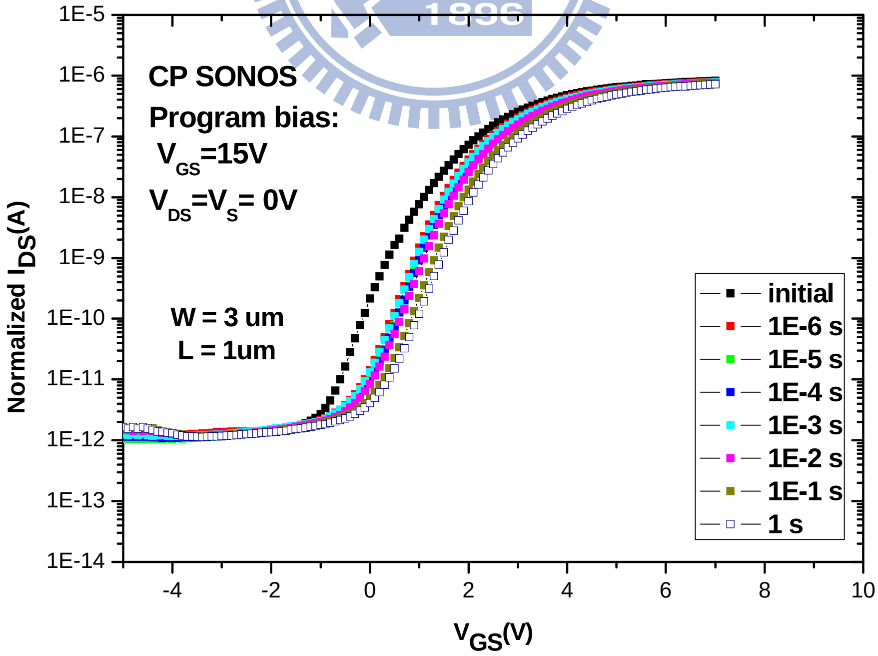


Fig. 5-10 Transfer characteristics of the CP SONOS device with various programming times at V_{GS} = 15 V.

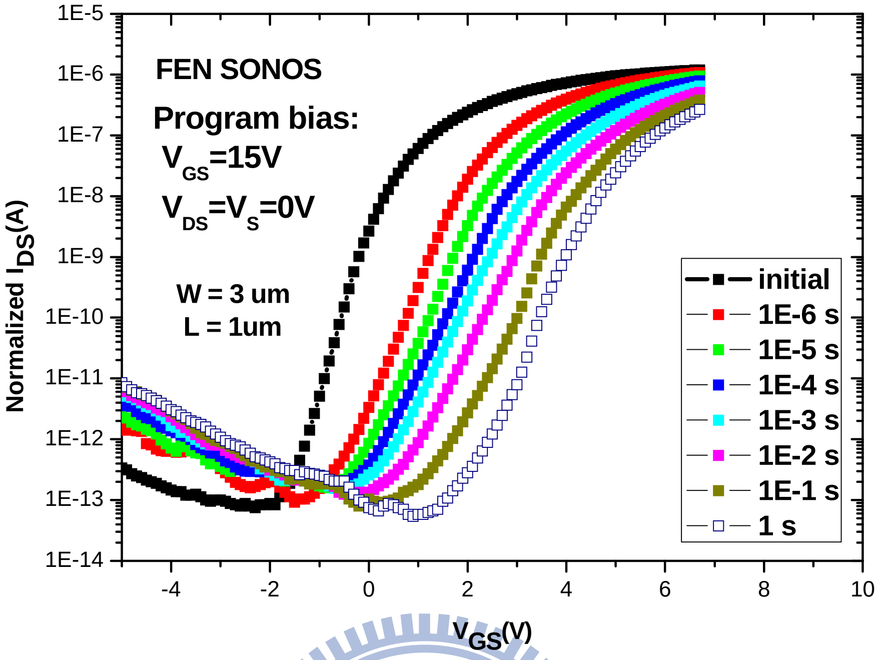


Fig. 5-11 Transfer characteristics of the FEN TFT SONOS device with the various programming times at V_{GS} = 15 V.

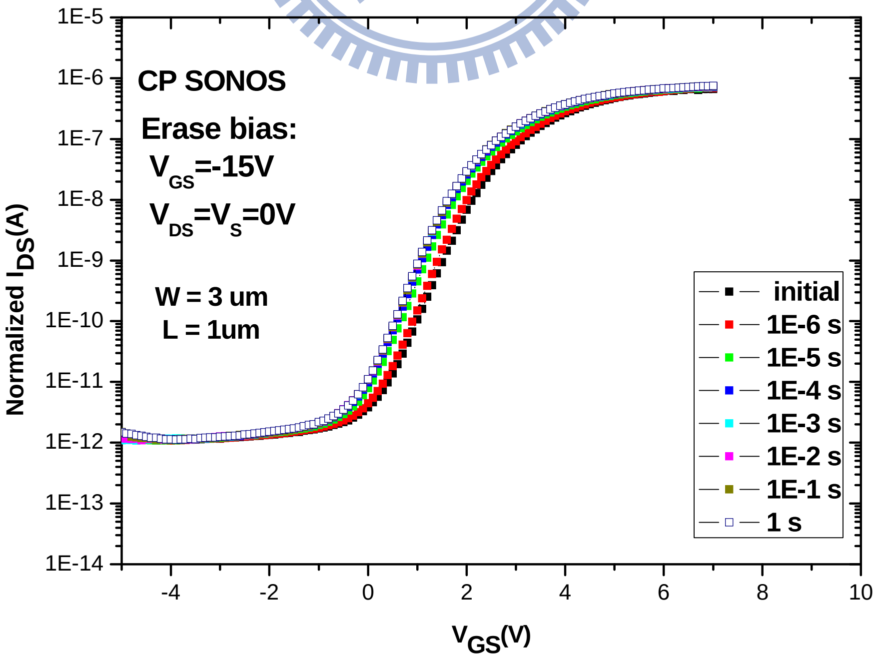


Fig. 5-12 Transfer characteristics of the CP SONOS device with the various erasing times at V_{GS} = -15 V.

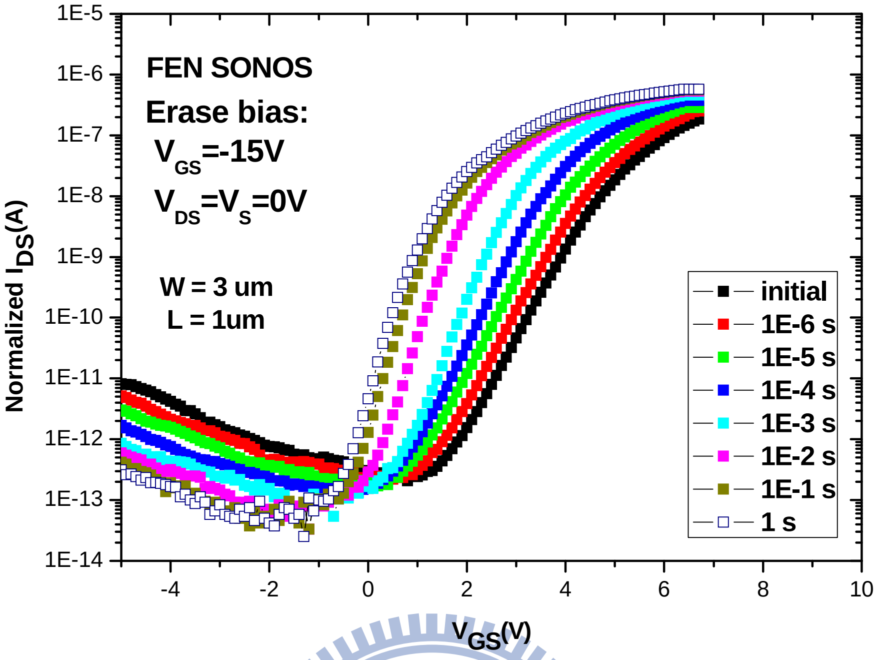


Fig. 5-13 Transfer characteristics of the FEN TFT SONOS device with the various erasing times at V_{GS} = -15 V.

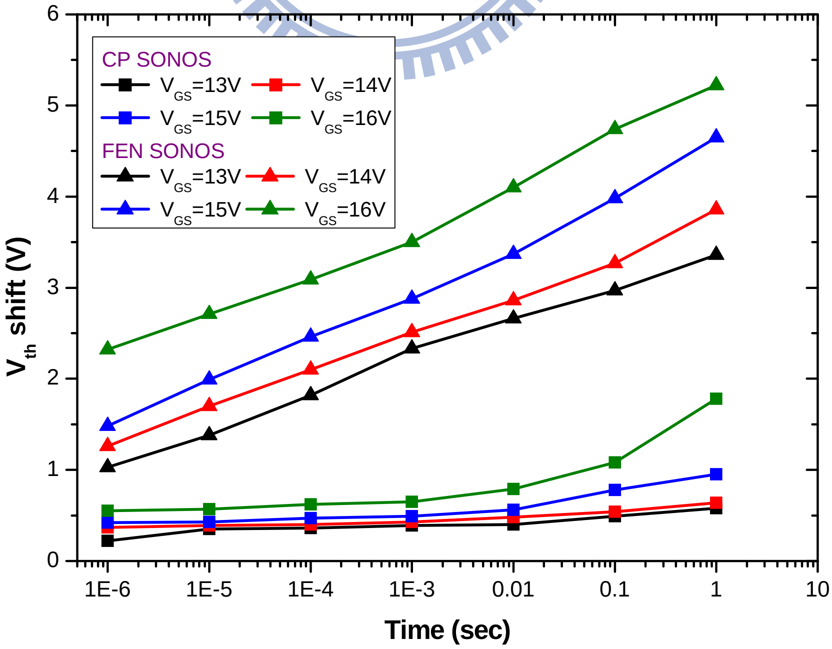


Fig. 5-14 (a) V_{th} shifts after programming for the CP SONOS and FEN TFT SONOS devices with various gate voltages

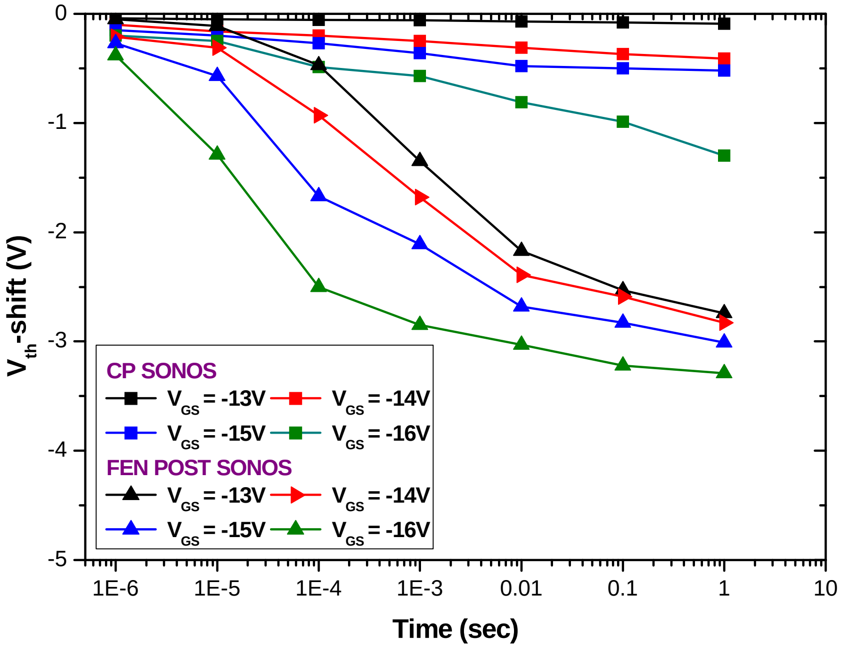


Fig. 5-14 (b) V_{th} shifts after erasing operation for the CP SONOS and FEN TFT SONOS devices with various gate voltages.

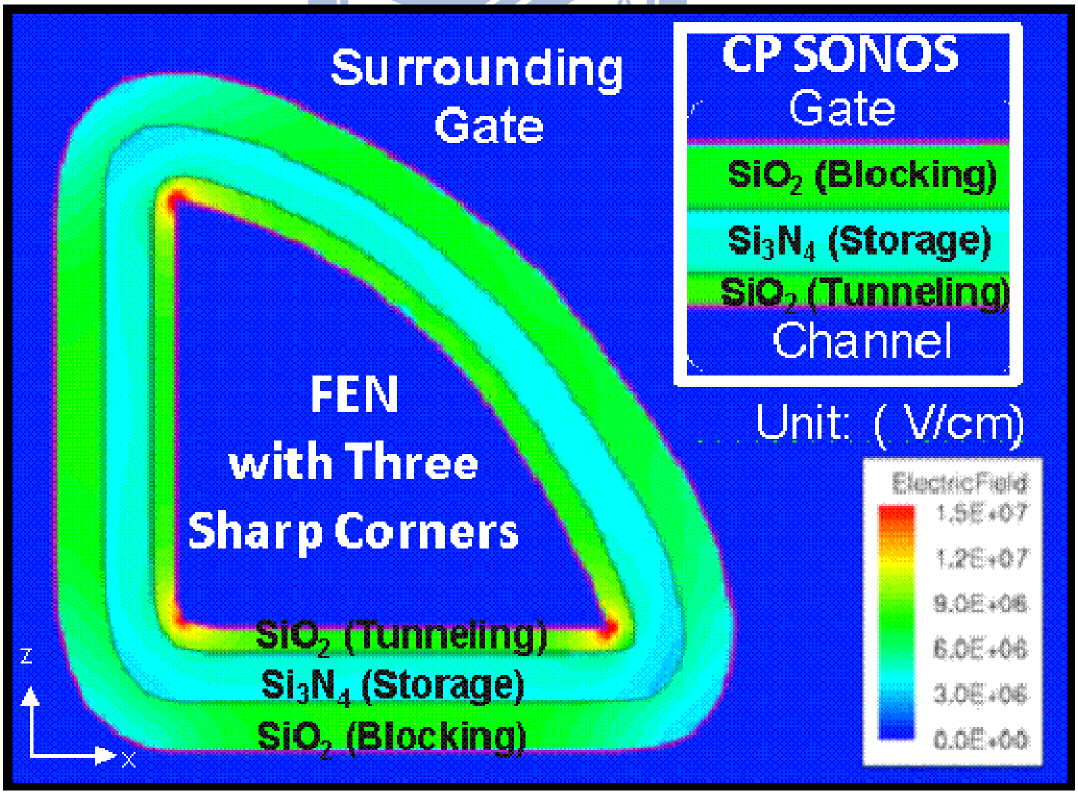


Fig. 5-15 The distribution of electrical field across the stacked ONO dielectrics for the CP and FEN TFT SONOS devices at V_{GS} = 15 V.

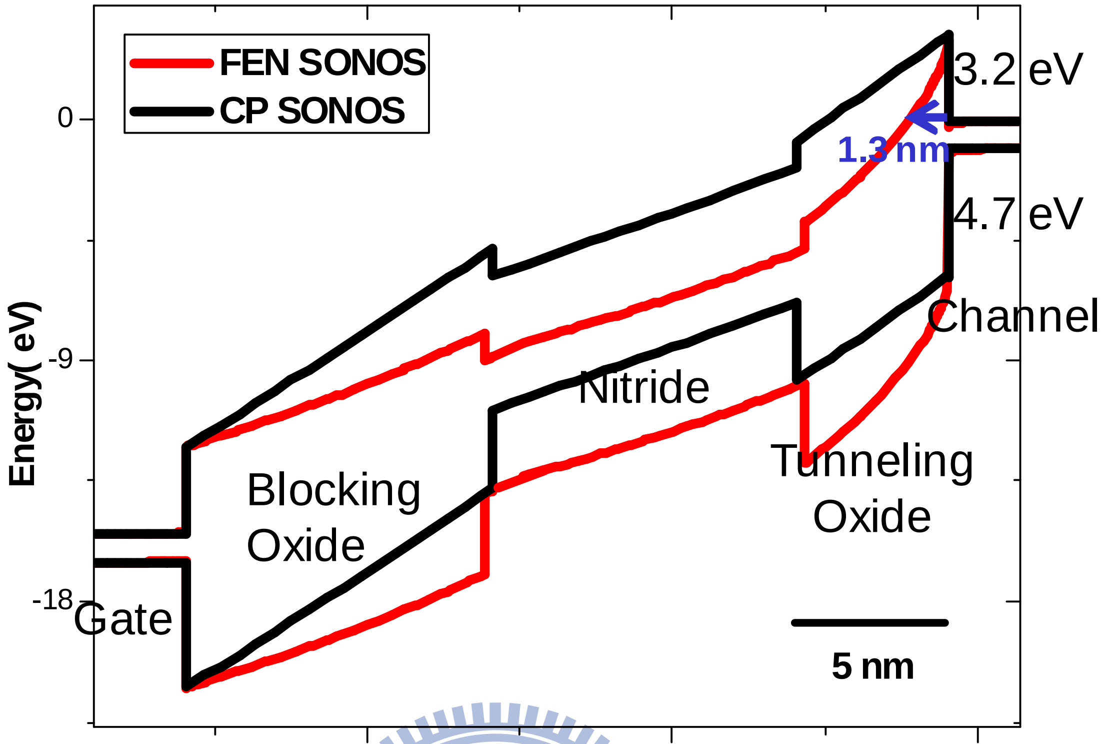


Fig. 5-16 The band diagrams of the CP and FEN TFT SONOS devices at V_{GS} = 15 V.

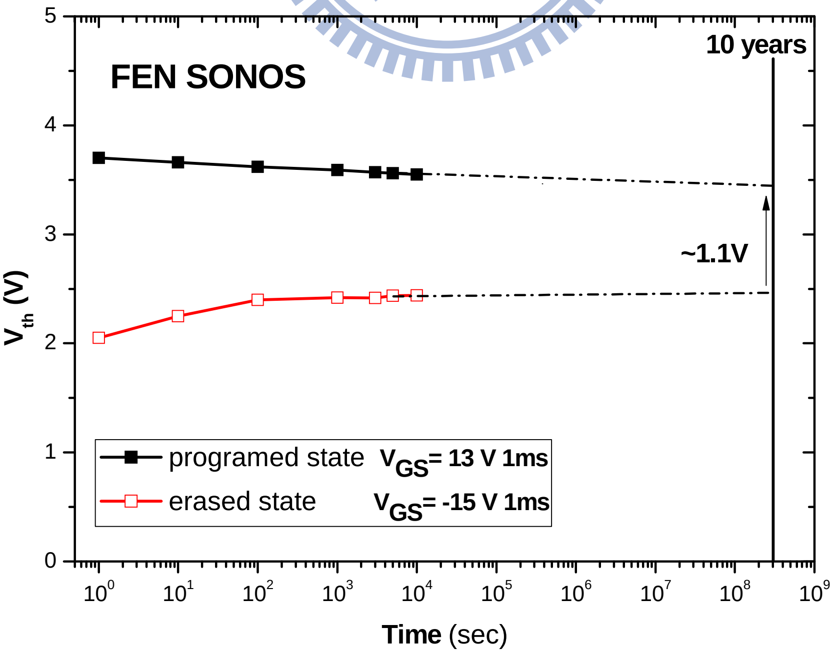


Fig. 5-17 Retention characteristic of the FEN TFT SONOS device after 10^4 P/E cycles.

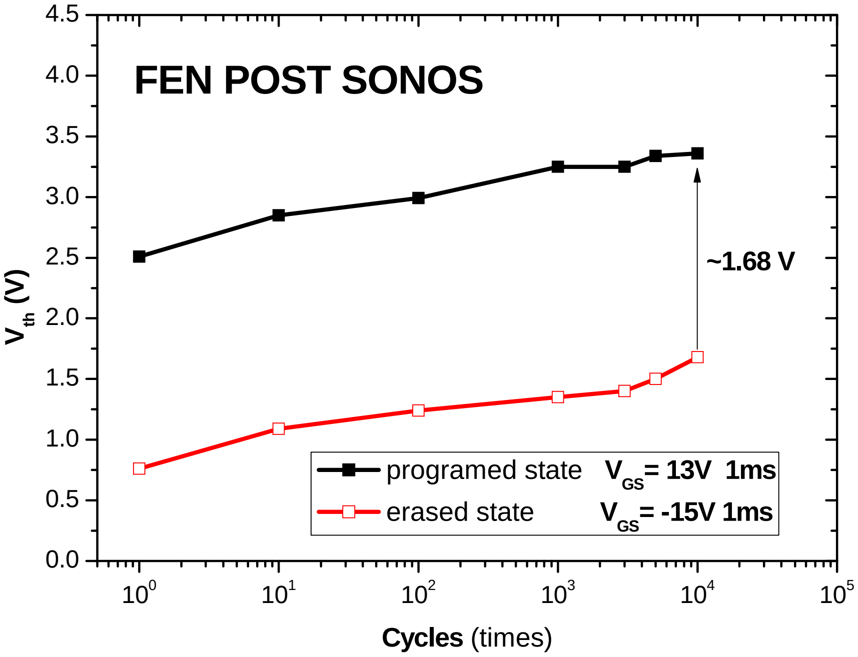


Fig. 5-18 Endurance characteristic of the FEN TFT SONOS device.

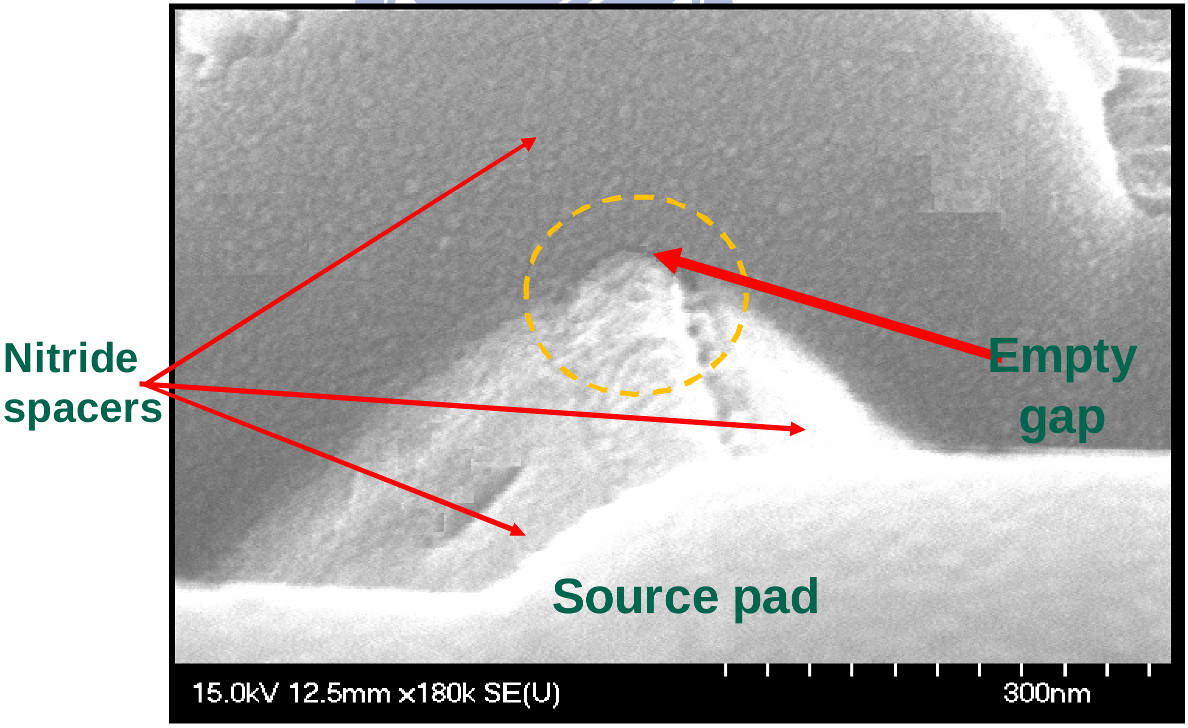


Fig. 5-19 The tiled-view SEM image of the FEN TFT SONVAS device

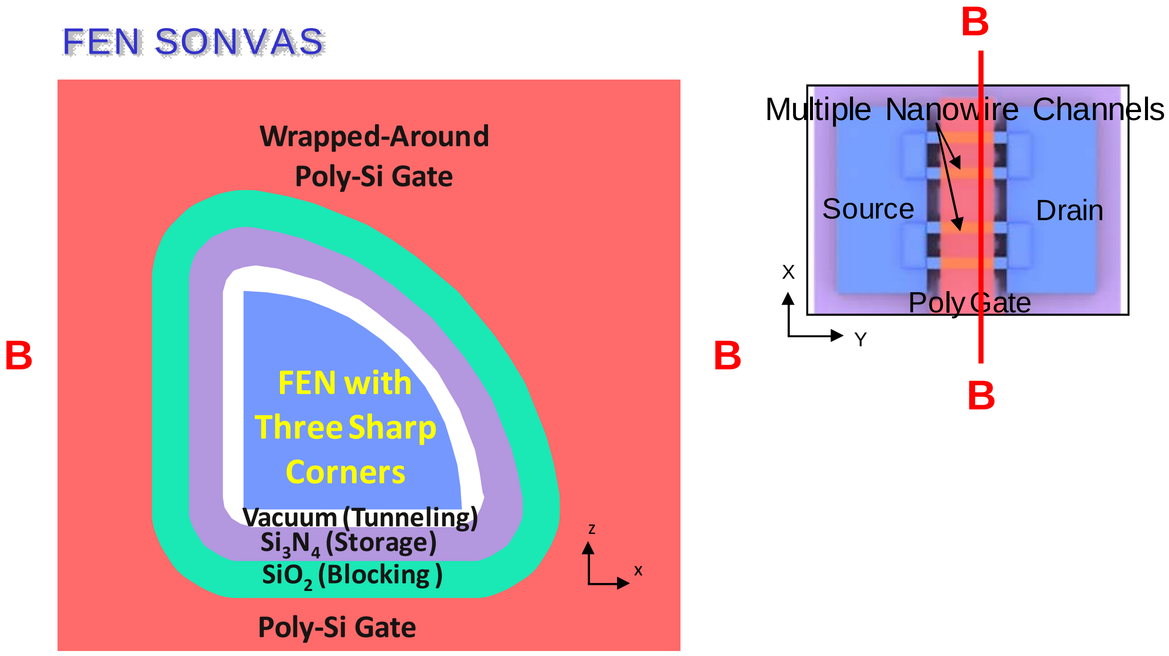


Fig. 5-20 The cross-section schematic image of nanowire channel with vacuum tunneling layer.

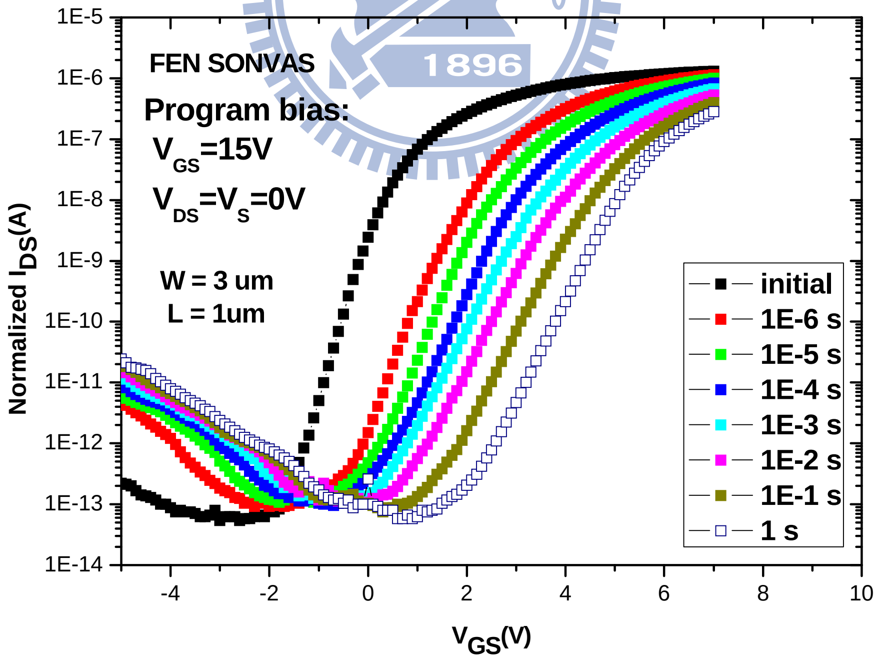


Fig. 5-21 Transfer characteristics of the FEN TFT SONOS device with various programming times at V_{GS} = 15 V.

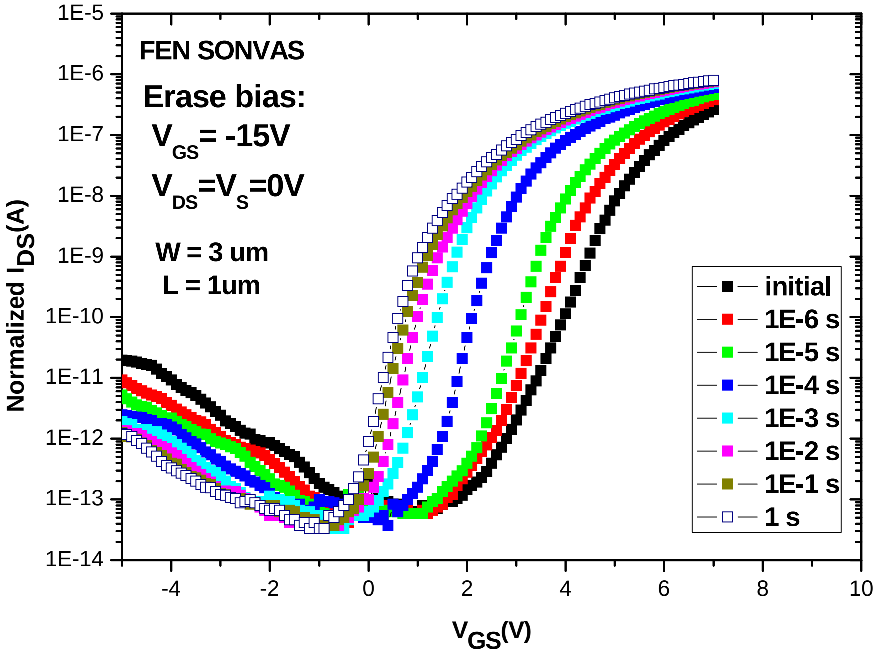


Fig. 5-22 Transfer characteristics of the FEN TFT SONOS device with various erasing times at V_{GS} = 15 V.

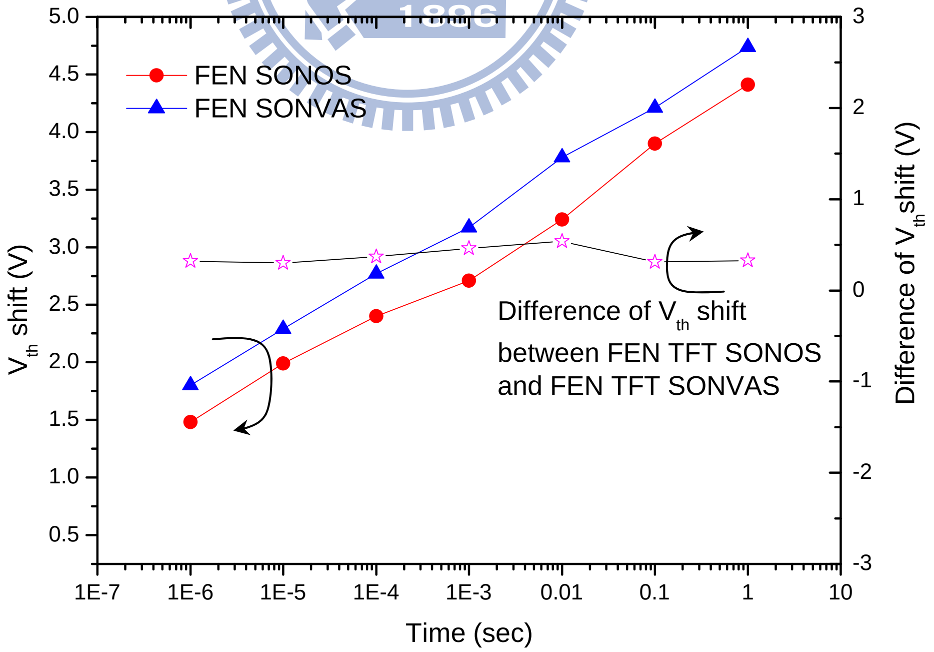


Fig. 5-23 The comparison of V_{th} shift between the FEN TFT SONOS and FEN TFT SONVAS devices with various programming times at V_{GS} = 15 V.

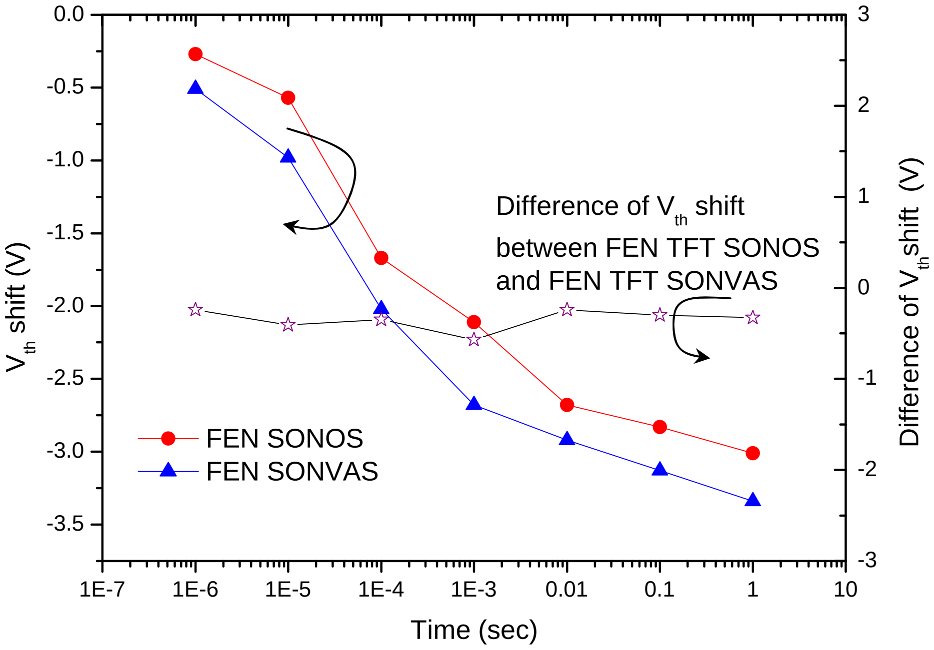


Fig. 5-24 The comparison of V_{th} shift between the FEN TFT SONOS and FEN TFT SONVAS devices with various erasing times at V_{GS} = -15 V.

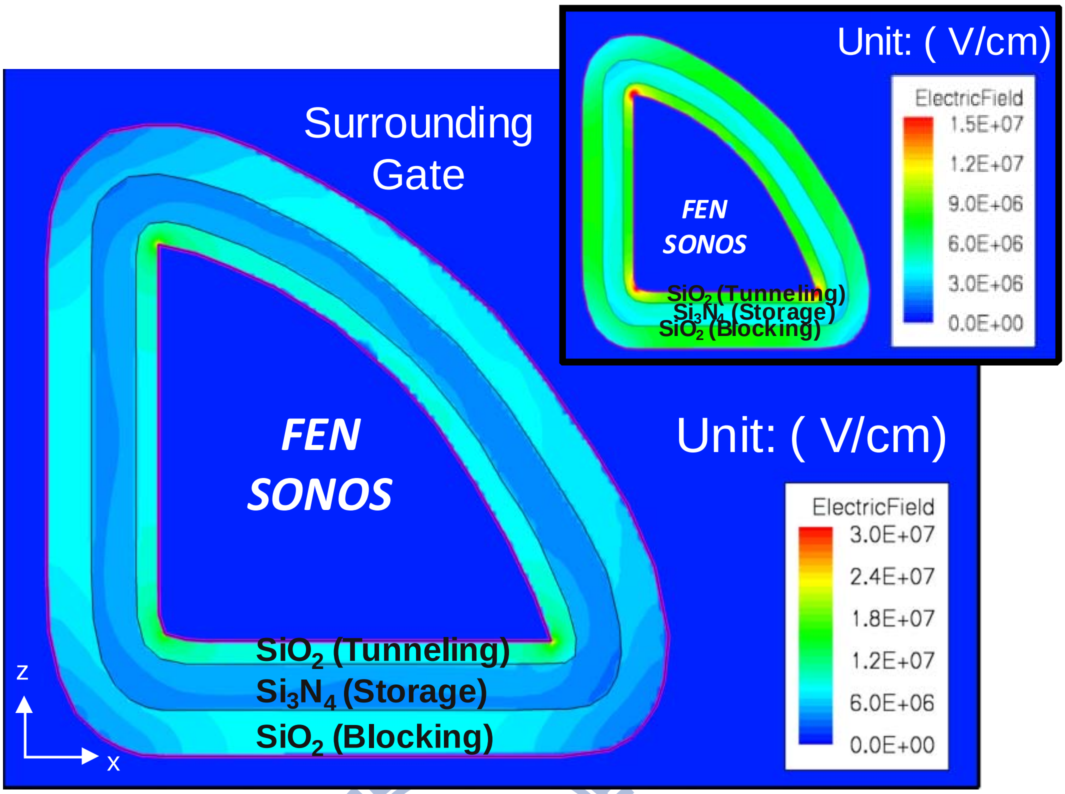


Fig. 5-25 The distribution of electrical field across the stacked ONO dielectrics for the FEN TFT SONOS devices at V_{GS} = 15 V.

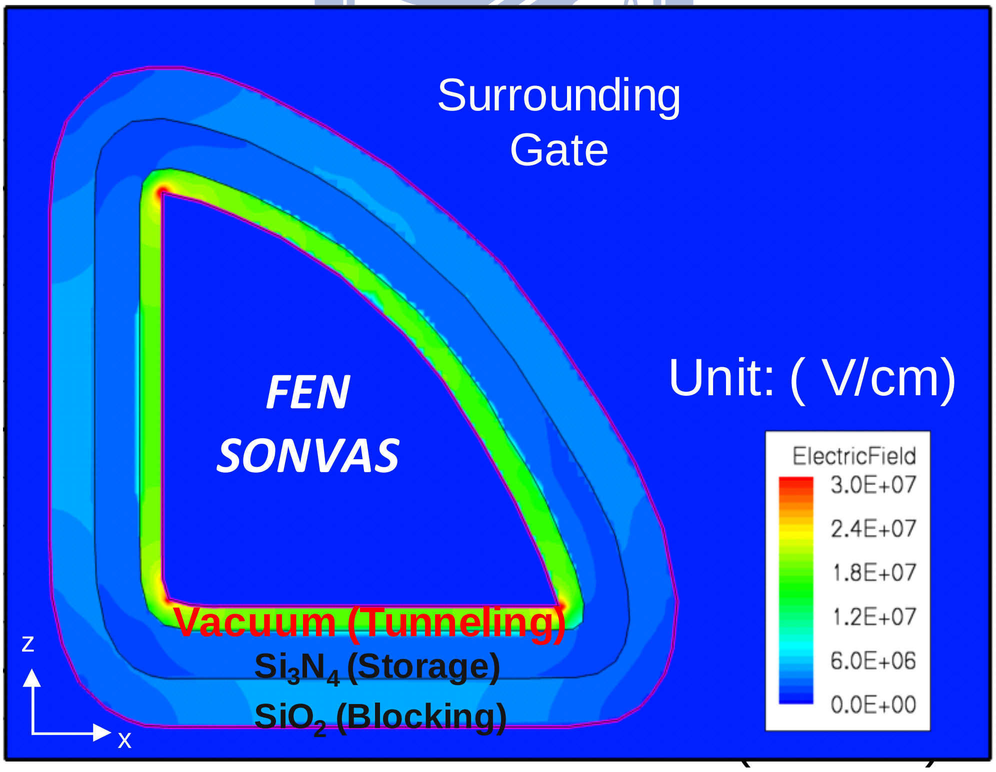


Fig. 5-26 The distribution of electrical field across the stacked ONO dielectrics for the FEN TFT SONVAS devices at V_{GS} = 15 V.

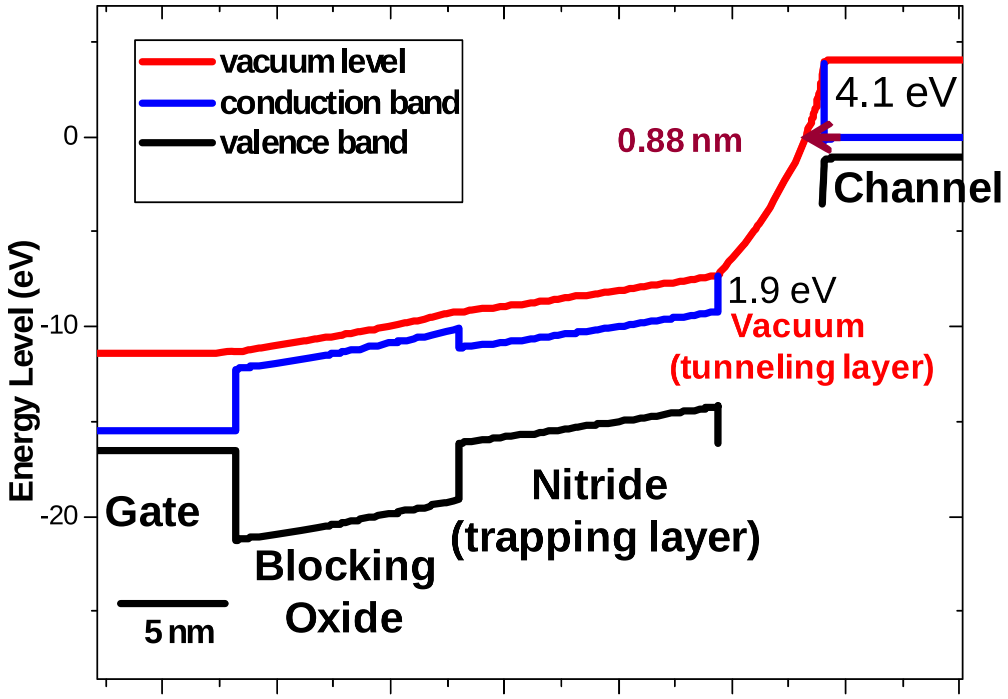


Fig. 5-27 The band diagrams of the CP and FEN TFT SONOS devices at V_{GS} = 15 V.

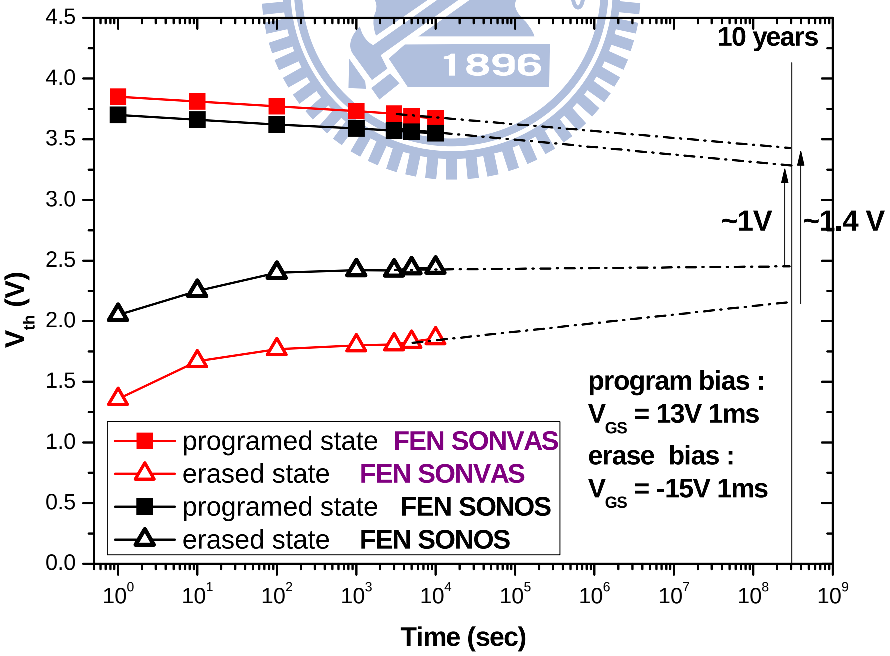


Fig. 5-28 Retention characteristics of FEN TFT SONVAS device after 10^4 P/E cycles.

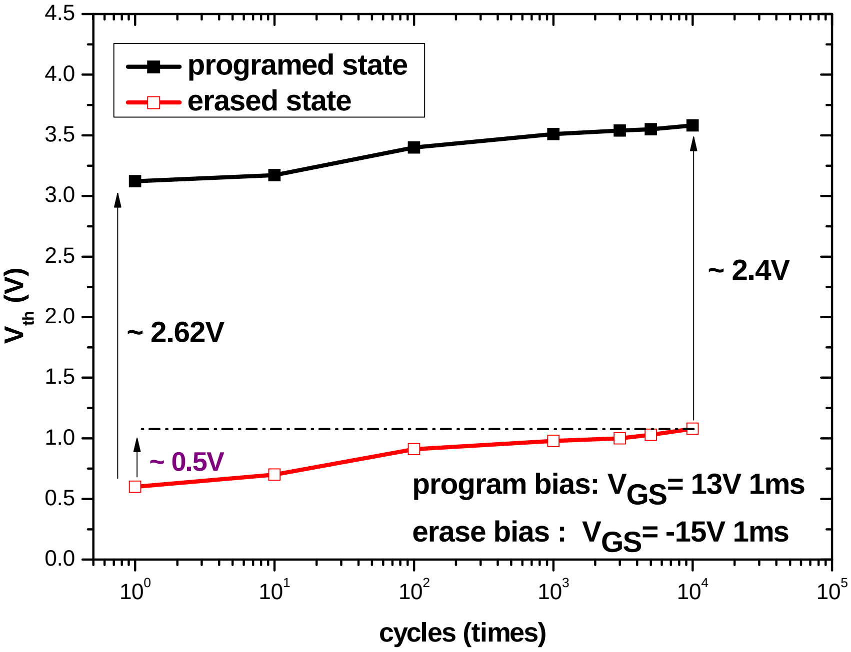


Fig. 5-29 Endurance characteristic of the FEN TFT SONOS device.

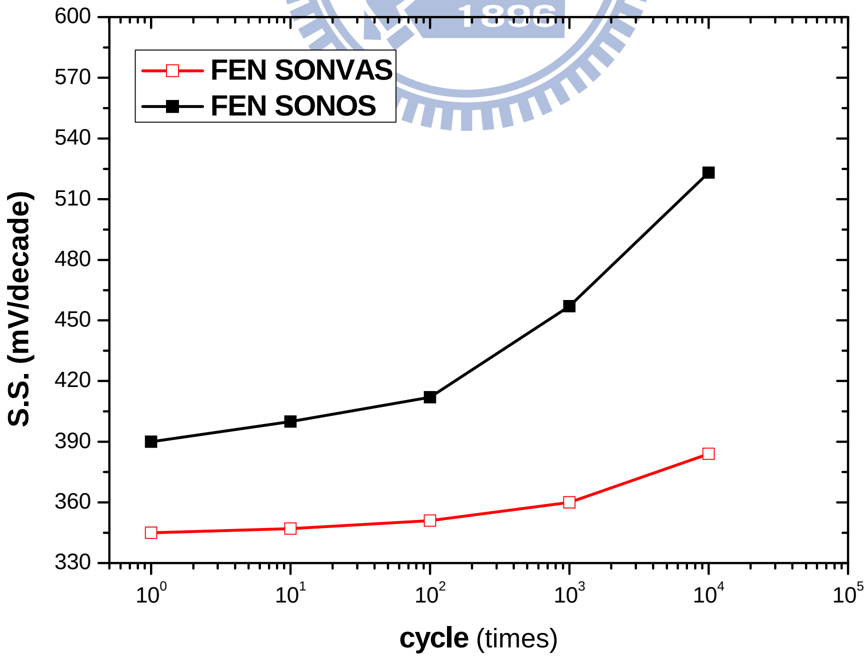


Fig. 5-30 The subthreshold swing of the FEN TFT SONOS and FEN TFT SONVAS devices after P/E cycles.

Chapter 6

Novel Polycrystalline Silicon Nanowire Field Emitters

6.1 Introduction

Field emission displays (FEDs) have been considered as the most promising candidates for the next-generation flat panel displays (FPDs) due to their image excellences in high contrast ratio, high brightness, and very quick response [6.1]-[6.3]. For further requirements on stable emission current and low operation voltage, field emitters have to be controlled by and integrated with active transistors [6.4]-[6.9]. It is well-known that poly-Si thin film transistors (TFTs) not only have been widely used as pixel switching elements on glass for active-matrix liquid-crystal display (AMLCD) and active-matrix organic light emitting diode (AMOLED), but also can be combined and integrated as functioned circuits (driving circuitry) for realization of system on panel (SOP). Therefore, for active-matrix field emission display (AMFED) applications, it is worthwhile to develop a field emitter device whose manufacturing is compatible to poly-Si TFT technology. Although there is non-Si based materials created for field emitters, it is too complex for process integration and aligned arrays. Spacer formation is a simple and matured technique in semiconductor industry [6.10], and in previous chapters, we have utilized this technique to promote transistor and memory performance on poly-Si TFTs and SONOS NVM for SOP applications. In this chapter, we further applied this technique on two types of field emitters for the possibilities of replacement of LCD display elements in terms of system integration and image performance.

6.2 Experiments

6.2.1 Fabrication Sequence of Double-Corner-Nanowire Field Emitters

The key fabrication steps of the proposed field emission emitter are schematically illustrated in Fig. 6-1. At first, a 300-nm-thick tetra-ethyl-ortho-silicate (TEOS) SiO_2 were deposited by low pressure chemical vapor deposition (LPCVD) system on oxidized silicon wafer. (Oxidized silicon wafer was simulated as a glass substrate). Numerous strips with step height of 100-nm were patterned on surface of the sacrificial SiO_2 layer by reactive ion etch (RIE), and followed by a conformal deposition of 100-nm-thick a-Si layer. After grid-pad lithography (patterned to overlap on the two edges of those strips) and its RIE process, numerous couples of spacer nanowires were *in-situ* resided against the sidewall of those designed strips and naturally connected with their neighboring two grid pads, as shown in Figs. 6-1(a) and (b) in the tilted and cross-section views, respectively. It should be noted that each spacer nanowires, inherently featuring three sharp corners, are simply constructed with RIE process without any advanced lithography or complex technique. After that, a solid phase crystallization at 600 °C in N_2 ambient for 24 hours was performed to transform the a-Si into poly-Si. Subsequently, phosphorous dopants were implanted into all the poly-Si grids and nanowires with a dose of 5×10^{15} cm^{-2} at 30 keV and were activated at 600 °C for 10 hours. After an isotropic etching of the SiO_2 strip for 50 nm by diluted hydro-fluoric acid (DHF), the outer two sharp corners of each nanowire were released to serve as field emitters and the other (inner) one was still tied with the residual SiO_2 strip to brace the whole nanowire body, as shown in Fig. 6-1(c).

6.2.2 Fabrication Sequence of Triple-Corner Nanowire Emitter *in-situ* Vacuum Encapsulated with Surrounding Anode

The fabrication steps of the triple-corner-nanowire emitter *in-situ* vacuum encapsulated with surrounding anode electrode are schematically illustrated in Fig. 6-2, which are similar as that of GAA-MNC in chapter 3. At first, a 50 nm Si_3N_4 and a 300 nm SiO_2 served as the etch-stop layer and the sacrificial layer were deposited on the oxidized wafer by the low-pressure chemical vapor deposition furnace (LPCVD) at 580 and 700 °C, respectively. The sacrificial SiO_2 layer was patterned as several strips by standard optical lithography and then etched anisotropically with 100 nm in-depth by the reactive ion etching (RIE) to form the steps. Next, a 100-nm-thick a-Si layer was conformally deposited on sacrificed layer for active layer by LPCVD at 550 °C. After that, the active region was patterned only on the source, drain and the end of strips by transformer-coupled plasma reactive ion etching (TCP-RIE). HBr and O_2 are used as etching gas sources in TCP-RIE. The recipe is selected here because it has higher selectivity to SiO_2 sacrificial strips (50:1) and can precisely control the dimension with slower etching rate (2 nm/sec). Due to the step profile of strips, the spacer nanowires were remained along the sidewalls of the strips after etching. It should be noted that the nano-scale dimension of the nanowire channels can be defined only by controlling the RIE time without any advanced lithography, each dummy strip produces twin nanowire channels, as well as the multiple channels can be designed with patterning several dummy strips (n strips × 2 wires/strip = 2n wires). Then, the solid phase crystallization (SPC) was performed at 600 ˚C for 24 hours to transform the a-Si into poly-Si. Subsequently, phosphorous dopants were implanted into all the poly-Si pads and nanowires with a dose of 5×10^{15} cm^{-2} at 30 keV and were activated at 600 ˚C for 10 hours. After that, the suspending channels were formed by etching the sacrificial SiO_2 layer with diluted HF, and the etching-stopper layer would stop etching process down to the buried oxide. Then a 25-nm-thick SiO_2 and a 200-nm-thick phosphorous *in-situ* doped poly-Si were deposited conformally around the suspending channels as the gate insulator and gate electrode, respectively. After gate definition, a SiO_2 side-etching by diluted HF immersion was performed to split the anode and cathode. Then, a 300-nm-thick SiO_x passivation layer was deposition by e-gun and while vacuum was *in-situ* encapsulated between anode and cathode. The contact hole opening and metallization were carried out to finish device fabrication.

6. 3 Results and Discussion

6.3.1 Emission Characteristics of Double-Corner-Nanowire Field Emitters

Figs. 6-3 and 6-4 show the SEM and TEM images of the fabricated arrayal double-corner spacer nanowire emitter, respectively. It can be observed that those resulting spacer nanowire are arrayal against those designed oxide strip as well as the outer two sharp corners of each nanowire are released to serve as field emission sites and the other (inner) one was tied with the residual SiO_2 strip to brace the whole nanowire body.

The electron field emission characteristics of the proposed arrayal double-corner spacer nanowire emitters were measured in a high-vacuum environment under a pressure of 5 × 10^{-6} torr. A glass substrate coated with indium tin oxide (ITO) and P22 phosphor (ZnS: Cu, Al) was used as the anode plate, and the gap between the cathode and the anode plate was set to be 160 μm as shown in Fig. 6-5. Fig. 6-6(a) also shows that exponential dependence relationship between the emission current and the applied voltage. The $\ln(I/V^2)$-1/V plot shown in Fig. 6-6(b) gives a straight line, indicating that the field emission from double-corner nanowires follows the Fowler–Nordheim (F-N) behavior. The calculation was carried out by using the simplified F-N equation [6.11]-[6.12].

$$I = \frac{A\beta^2 V^2}{\phi}\exp[-B\frac{\phi^{\frac{3}{2}}}{\beta V}] \text{......} (1)$$

where I is the emission current, V is the applied voltage, Φ is the work function. A and B are constants, corresponding to 1.563×10^{-10} ($AV^{-2}eV$) and 6.833×10^{3} ($VeV^{-3/2}$ μm^{-1}), respectively, The β is the field enhancement factor, which is used to indicate the degree of the field emission enhancement of any tip shape on a planar surface. The β is a parameter dependent on the geometry of nanowire, crystal structure, and density of emitting points. The β can be determined, based on the slope of the $\ln(I/V^2)$-1/V plot. In the case, the value of β has been calculated to be 72050 using the Si work function value (i.e., 3.6 eV). The F-N tunneling began at 330 V, and its corresponding electron field and turn-on current are 2.06 V/μm and 1.362 × 10^{-9} A, respectively. And, the maximum current at 1000 V is 9.741 × 10^{-6} A. Its corresponding luminescent image is very uniform, demonstrated in Fig. 6-7.

Although the emission performance of the proposed double-corner-nanowire field emitters is still poor than carbon nanotube (CNT) counterparts, the fabrication of the proposed double-corner-nanowire field emitters are only required a simple spacer-formation step and easily compatible to low temperature poly-Si (LTPS) TFT process. Unlike the simplicity of spacer formation, CNT material is often produced difficulty in macroscopic quantities by using graphite evaporation in the course of arc discharge or laser ablation or by using thermal decomposition of hydrocarbons. [6.13]. Usually, CNT are dispersed and misaligned in the material, which restrict their applications on FED. Thus, such LTPS-based double-corner-nanowire field emitters have great potential for replacement of LCD display elements in terms of system integration and image performance.

6.3.2 Emission Characteristics of Triple-Corner-Nanowire Emitters *in-situ* Vacuum Encapsulated with Surrounding Anode

Figs. 6-8, 6-9, and 6-10 show the top-view SEM, cross-session SEM, and cross-session TEM images of the triple-corner nanowire emitter *in-situ* vacuum encapsulated by surrounding anode, respectively. The proposed emitter was *in situ* encapsulated at ultra low pressure of 1×10^{-6} torr, thus the measurement can be performed directly under atmosphere instead of vacuum-environment system. Fig. 6-11(a) demonstrates the I-V curve of the proposed vacuum microelectronic devices. The field emission turns on at as low as 0.14 V due to the controlled, small distance of 30 nm between anode and cathode, and its corresponding electron field and turn-on current are 4.67 V/μm and 6.384×10^{-11} A, respectively. And, the maximum current at 2 V is 6.360×10^{-8} A. The F-N plot is shown in Fig. 6-11(b), in which the negative slope verifies the F-N tunneling occurrence.

6.4 Summary

In this chapter, we applied this spacer technique on two types of field emitters for the possibilities of replacement of LCD display elements in terms of system integration and image performance. For spacer nanowire field emitter, the F-N characteristic with turn-on field of 2.06 V/um has been performed. For triple-corner nanowire emitter *in-situ* vacuum encapsulated by surrounding anode electrode, the F-N characteristic has been performed with turn-on voltage of 0.14 V, which is lowest one in record to date.

Figures

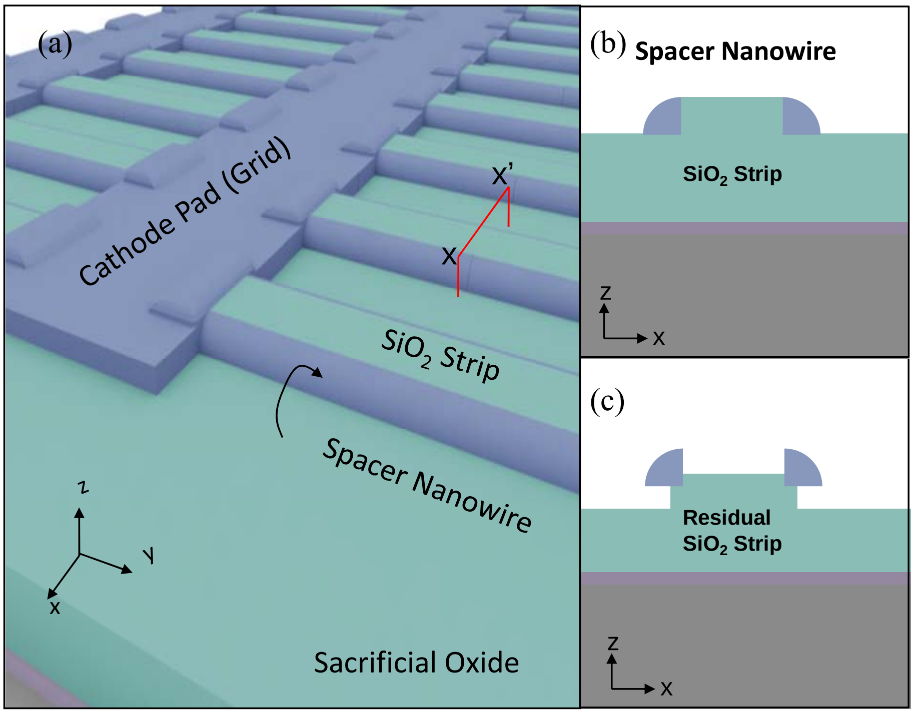


Fig. 6-1 The key fabrication steps of the proposed spacer field emission emitter.

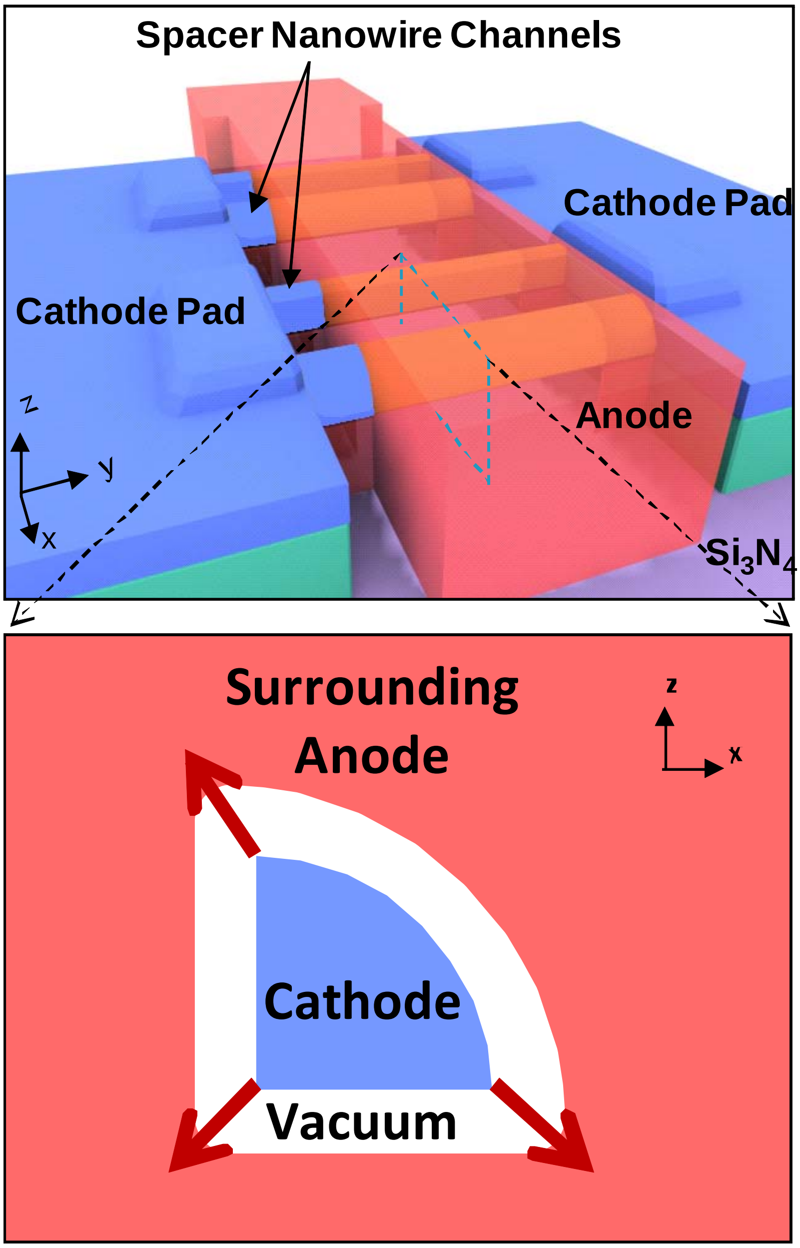


Fig. 6-2 The key fabrication steps of the triple-corner nanowire emitter *in-situ* vacuum encapsulated by surrounding Anode Electrode.

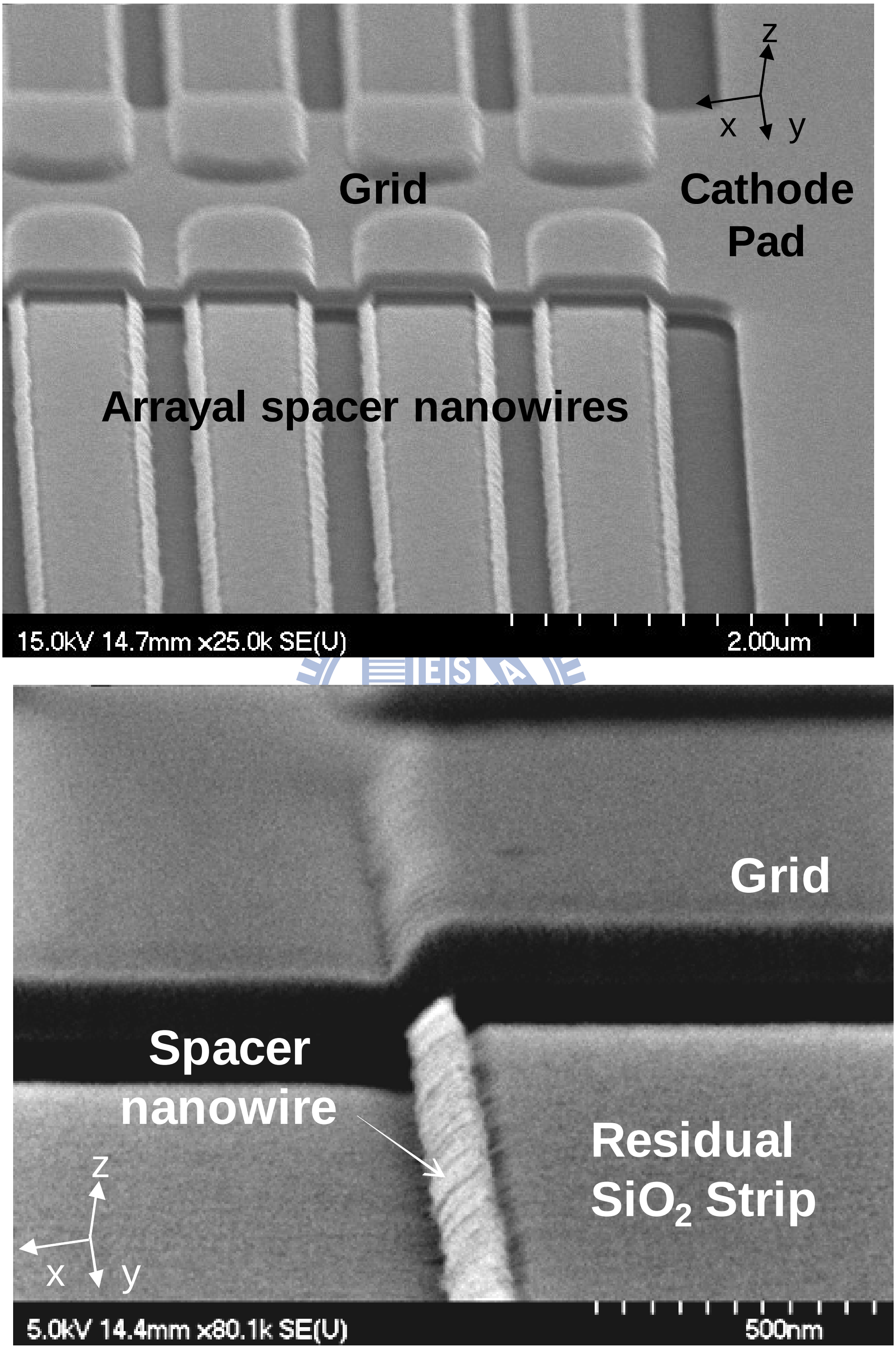


Fig. 6-3 SEM image of the arrayal double-corner spacer nanowire emitter

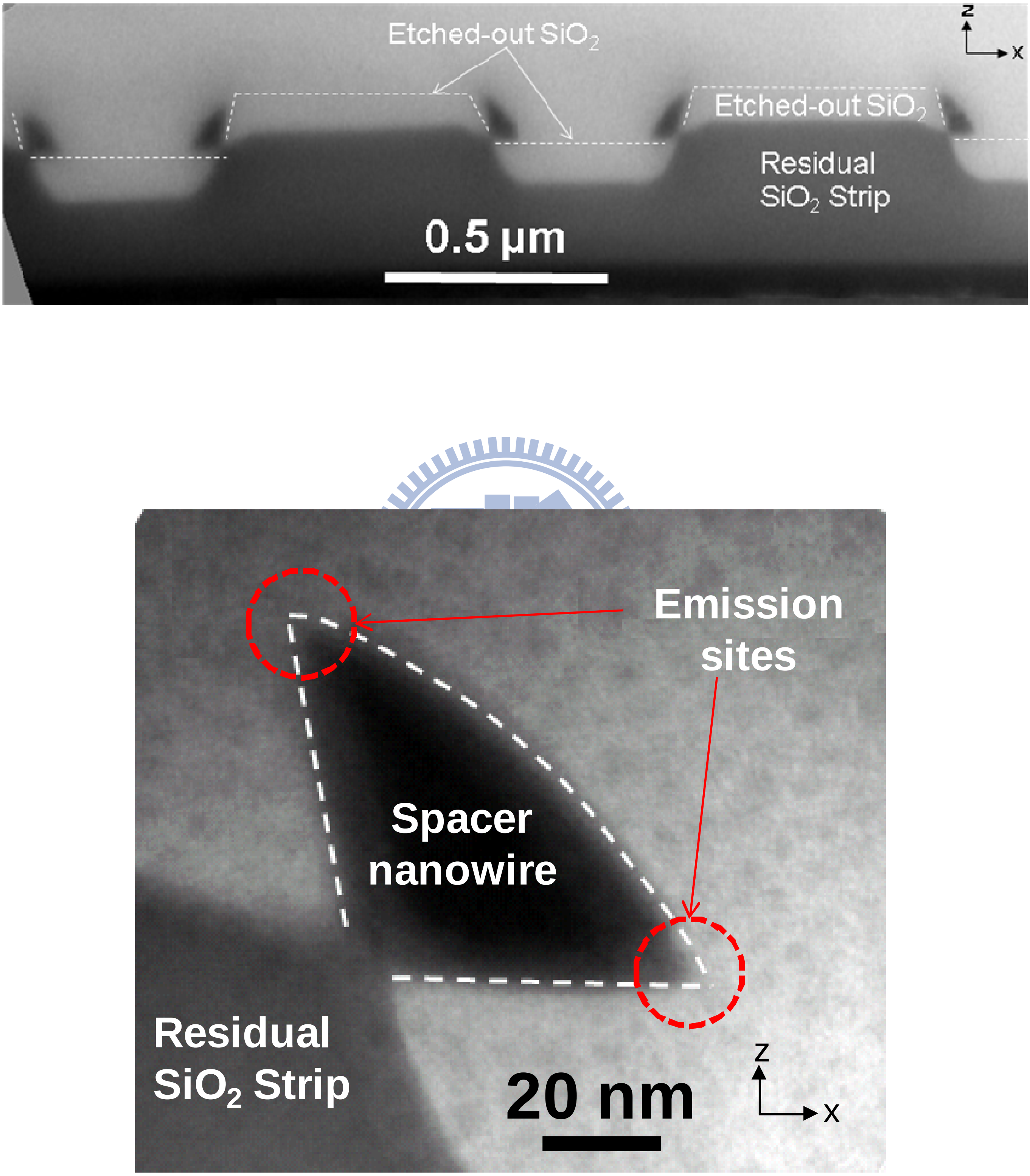


Fig. 6-4 TEM image of the arrayal double-corner spacer nanowire emitter

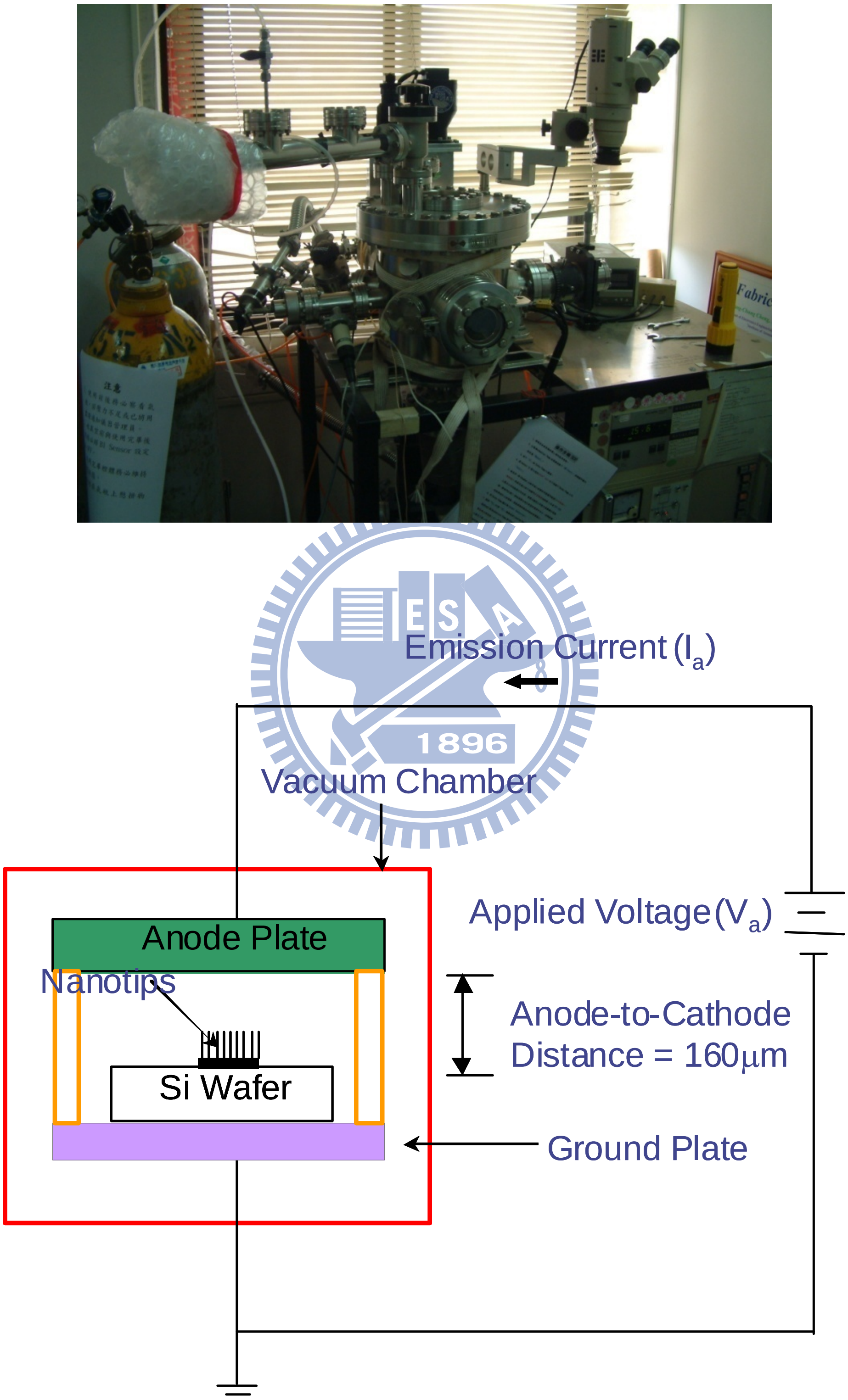


Fig. 6-5 The apparatus and schema of the vacuum measure unit.

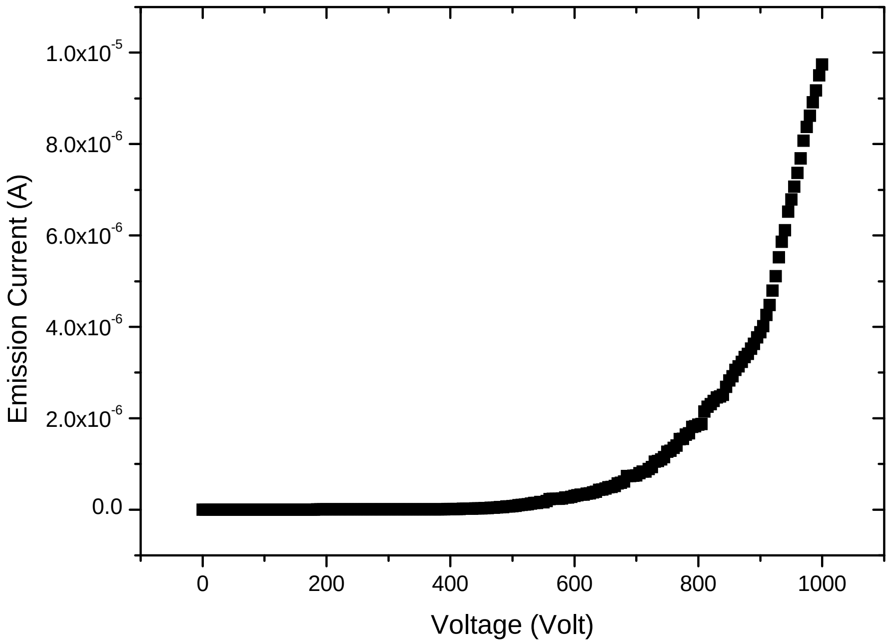


Fig. 6-6 (a) The I-V curve of the proposed double-corner spacer nanowire emitter

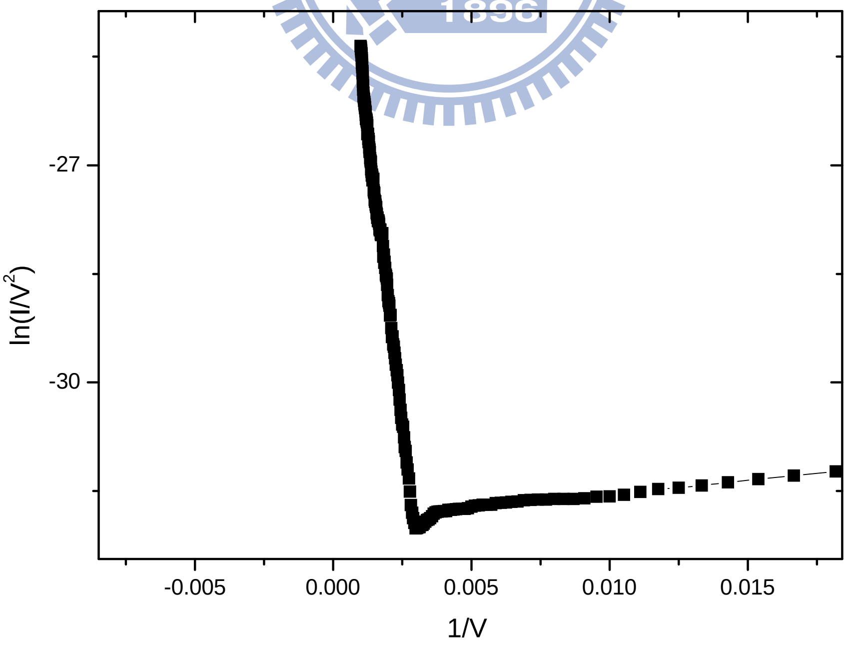


Fig. 6-6 (b) The F-N plot of the proposed double-corner spacer nanowire emitter.

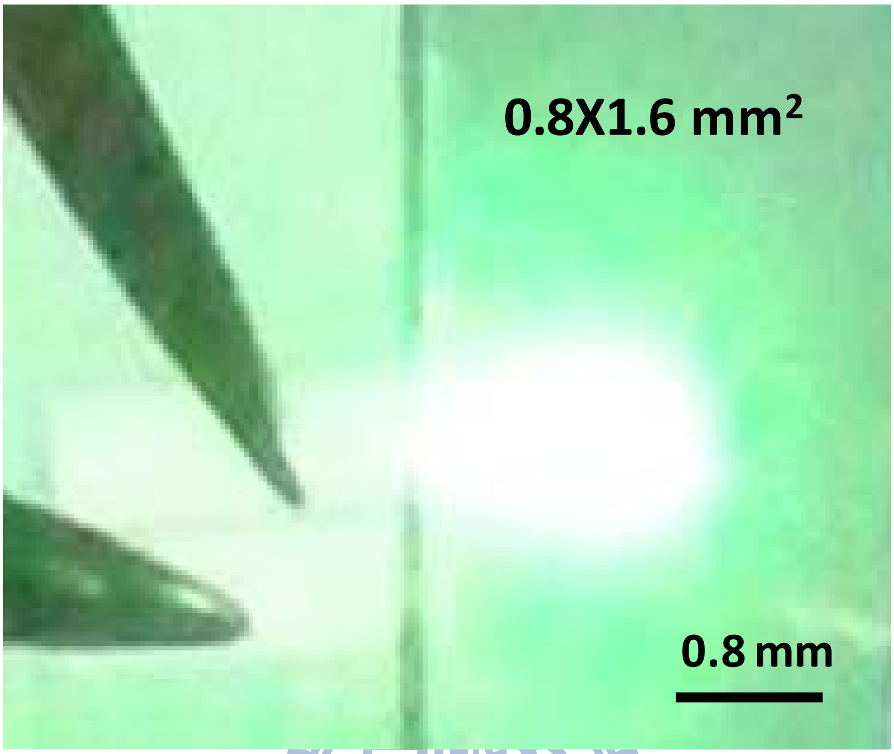


Fig. 6-7 The luminescent image of the double-corner spacer nanowire emitter

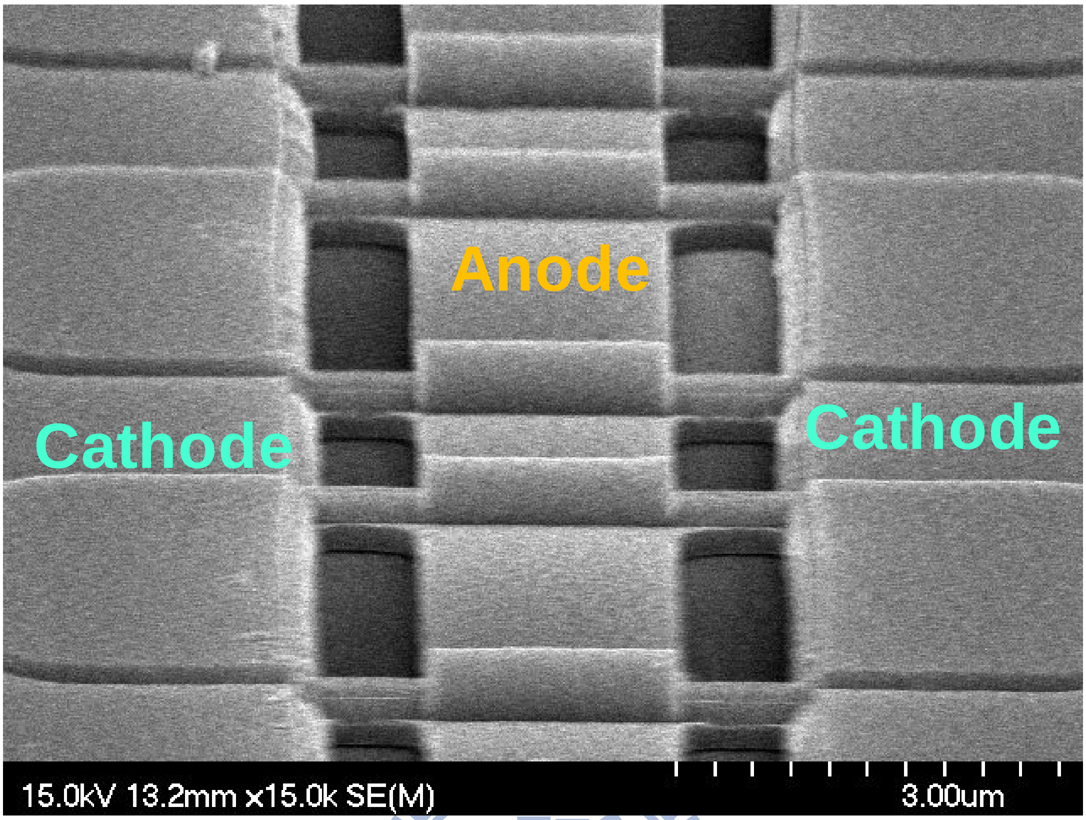


Fig. 6-8 Top-view SEM image of the fabricated triple-corner-nanowire emitter with surrounding anode.

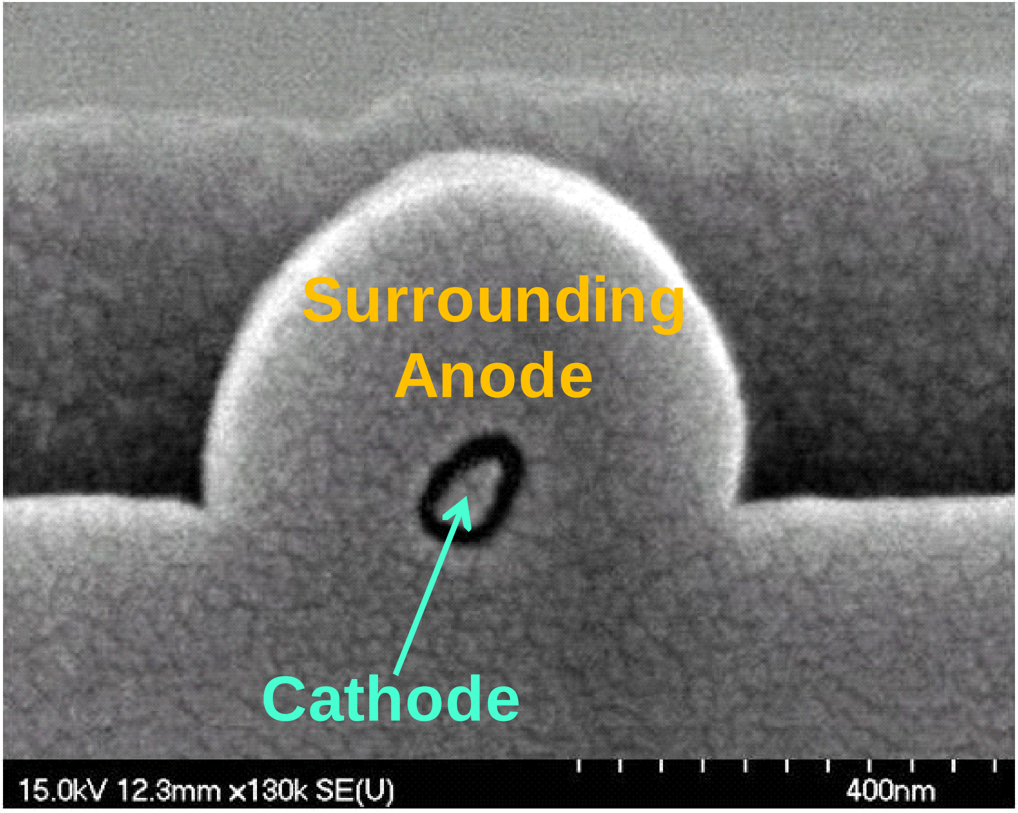


Fig. 6-9 Cross-session-view SEM image of the fabricated triple-corner-nanowire emitter with surrounding anode

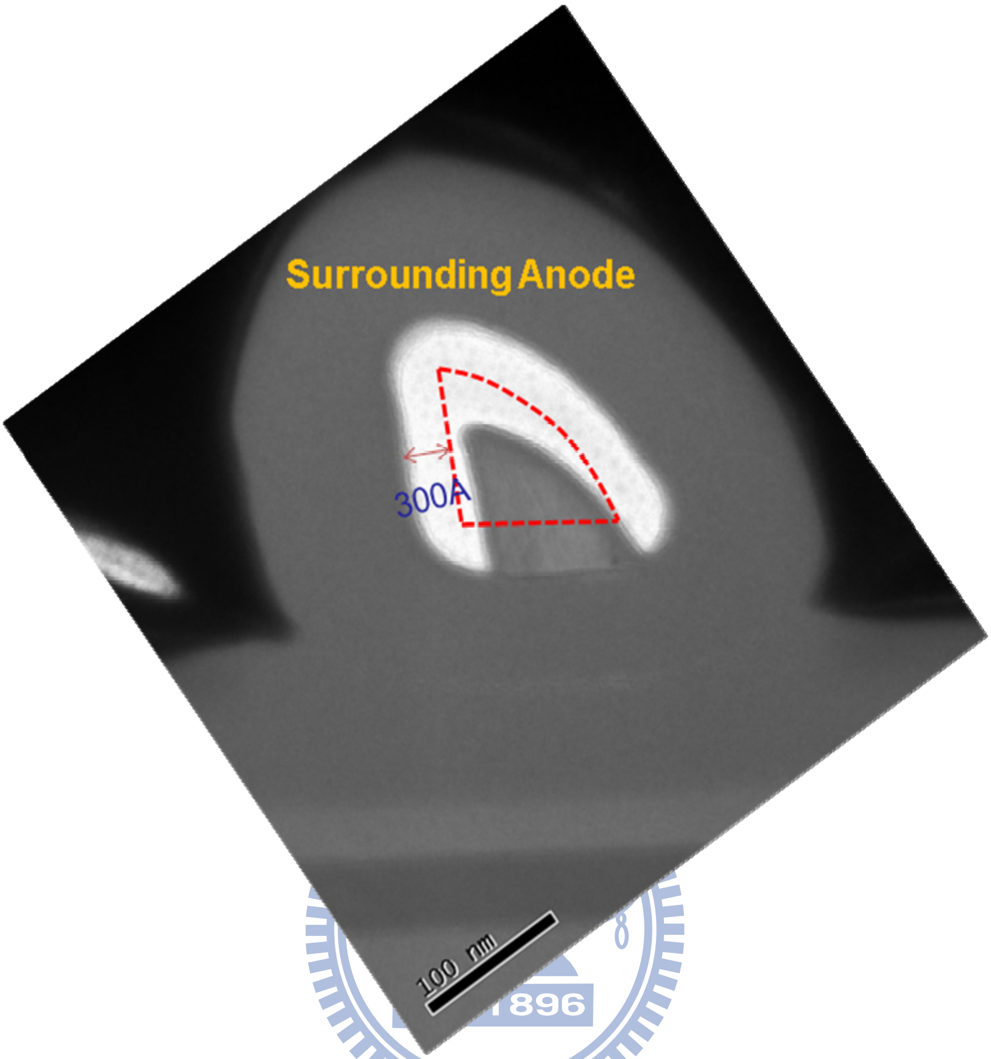


Fig. 6-10 FIB-prepared TEM image of the triple-corner nanowire emitter *in-situ* vacuum encapsulated with surrounding anode, in which the dash line indicates the original position of the triple-corner nanowire before FIB cutting.

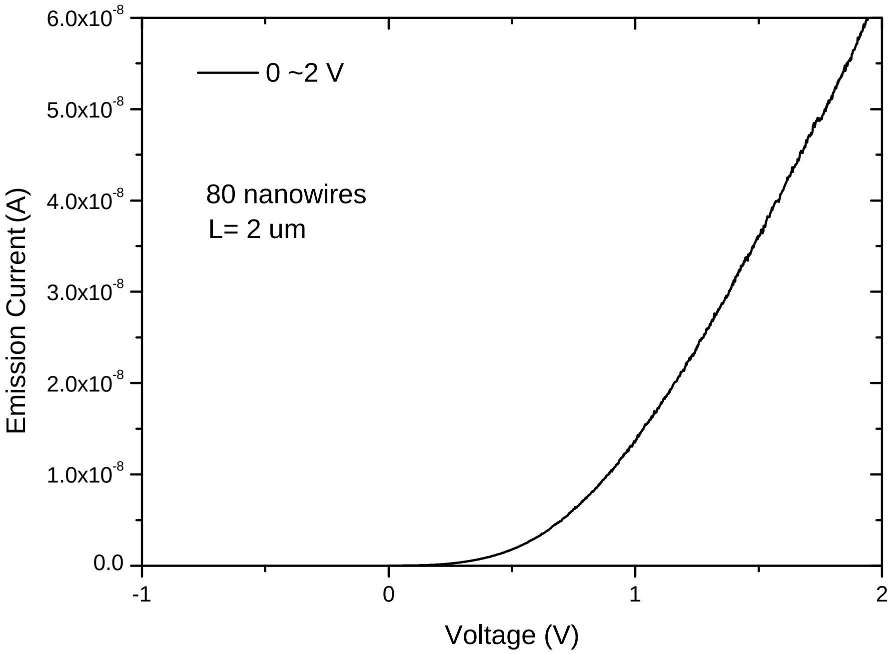


Fig. 6-11 (a) The I-V curve of the triple-corner nanowire emitter *in-situ* vacuum encapsulated with surrounding anode.

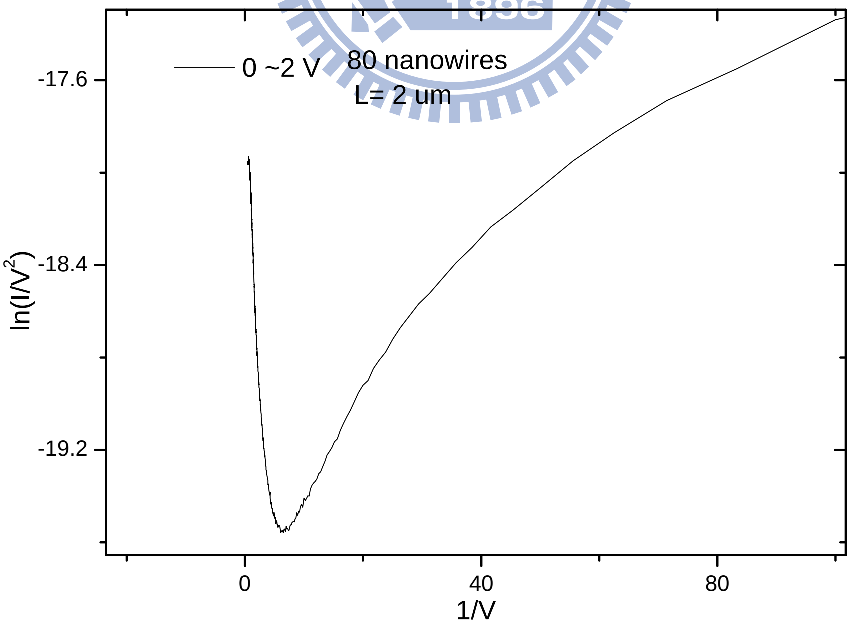


Fig. 6-11 (b) The F-N plot of the triple-corner nanowire emitter *in-situ* vacuum encapsulated with surrounding anode.

Chapter 7

Summary and Conclusions

In this work, various techniques are studied for the fabrication of high-performance low-temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) in terms of drain, gate, and channel engineering, accompanying with the versatile SOP development for SONOS memories, field emitters and flexible electronics.

A novel T-Gate poly-Si TFT with *in-situ* vacuum gaps has been proposed and fabricated only with a simple procedure. The T-Gate structure is formed only by a selective-etching technology of the Mo/ITO bi-layers. Then, vacuum gaps are *in-situ* embedded in this T-Gate structure subsequent to capping the SiH_4-based passivation oxide under a vacuum process chamber. The proposed T-Gate poly-Si TFTs have excellent performance and superior reliability. The off-state leakage current at V_{GS} = -15V and V_{DS} = 3V is greatly suppressed about 10^4 times less than the conventional one and the hot-carrier reliability also can be much improved as well. Those are due to the remarkable reduction of the E_{ML} and E_{MV} near the drain depletion region.

The novel GAA-MNC TFTs have been also demonstrated by using a simple process sequence. The MNCs were performed only with a sidewall-spacer formation. And, the unique suspending MNCs are also achieved to build the GAA structure. Owing to the overall effects of the nano-scale dimension, the three sharp corners of the spacer NW, the 3D GAA structure, together with the more effective plasma passivation of such MNC scheme, the GAA-MNC TFTs reveal high-performance characteristics and excellent SCE immunity.

Two types of novel processes are demonstrated for fabricating high-crystallinely Si nanowire LTPS TFTs with multi-gate structures for channel engineering development. Due to the multi-gate operation and high-crystallinity formed in the nanowire channel, the both devices have a high driving current, steeper subthreshold slope, superior SCE immunity, and suppression of the floating-body effect. Therefore, such high-crystallinity TFTs are therefore ideally suitable for future active-matrix organic light-emitting diode and system-on-panel applications.

A field-enhanced nanowire (FEN) LTPS-TFT silicon-oxide-nitride-oxide-silicon (SONOS) memory with a gate-all-around (GAA) structure has been proposed to improve the program and erase (P/E) performance. Each nanowire inherently has three sharp corners fabricated simply by sidewall spacer formation to obtain high local electric fields. The field-enhanced carrier tunneling via such a structure leads to faster P/E speed and wider memory window for the FEN SONOS as compared to the conventional planar (CP) counterpart. The FEN POST SONOS device exhibits a V_{th} shift of 2.71 V and 2.11 V at V_{GS} = +15/-15 V in 1 ms for FN programming and erasing (P/E) operations, respectively. Other than FEN structure, vacuum, lowest k, was further as a substitute for tunneling oxide to perform the novel silicon-oxide-nitride-vacuum-silicon (SONVAS) structure, for the first time. Due to the further electric field enhancement from vacuum introduction in tunneling layer, the FEN SONVAS exhibited larger V_{th} shifts of 3.17V and 2.68V at V_{GS} = +15/-15V in 1 ms for FN P/E operations, respectively. Besides, due to the empty property of vacuum, there are less dangling bonds and tunneling-oxide traps produced during P/E cycles, so that FEN SONVAS exhibits much improved endurance reliability as well.

In additions to the results as mentioned above, we applied this spacer technique on two types of field emitters for the possibilities of the replacement of LCD display elements in terms of system integration and image performance. For spacer nanowire field emitter, the F-N characteristic with turn-on field of 2.06 V/um has been performed. For triple-corner nanowire emitter in-situ vacuum encapsulated by surrounding anode electrode, the F-N characteristic has been performed with turn-on voltage of 0.14 V, which is lowest one in the record to date.

Chapter 8

Future Prospects

There are some interesting and important topics that are valuable for the future further research about the low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs):

(1) To further improve the performance of LTPS TFT devices and circuits composed by LTPS TFTs, scaling down the physical dimension of TFT is an effective approach. As the thickness of gate oxide is scaled down with device dimension, the quality of deposited oxide can hardly meet the requirements for the gate insulator. Hence, some novel approaches for the formation of high-quality thin gate dielectric may be adopted to replace the deposition of gate dielectric. Plasma oxidation using a high-density plasma (HDP) source has been shown to be the most promising approach to form high-quality thin gate dielectrics at low temperature.

(2) Although excimer lasers have been shown to be the most promising candidates for crystallization of a-Si thin films in the mass production of LTPS TFT systems on LCD panels, however, the instability and short pulse duration of excimer lasers make the formation of uniform and large grained poly-Si thin films hard. Solid-state lasers, which include pulsed and continuous-wave (CW) lasers, may be the other alternatives for crystallizing a-Si thin films due to the advantages of good stability of laser fluence and long melting duration during laser irradiation.

(3) Self-heating effect has been shown to be an important issue for LTPS TFT systems on thermal insulating glass substrates from the viewpoint of device performance and reliability. As a result, some novel approaches are required to dissipate the heat generating during the device operation.

(4) Although LTPS-based field emitter has been proposed, it is further worthwhile to

develop the integration process for both devices of LTPS TFTs and LTPS-based field emitters to realize the active-matrix field emission displays (AMFEDs).

(5) For multi-bit operation, high-mobility LTPS-TFT SONOS for channel hot electron (CHE) P/E scheme should be developed as well.

(6) Although device structures with gate, drain, and channel engineering are proposed to improve the performance individually, it is further worthwhile to combine all to improve the device performance. As described in chapters 3 and 4, the field enhancement in the gate-all-around LTPS TFTs results in undesired high off-state leakage current, the T-Gate structure proposed in chapter 2 can be further applied to reduce the leakage current.

(7) In chapter 4, two types of novel processes were demonstrated for fabricating multiple-gate TFTs with high-crystallinity Si nanowire (NW) channels. The one is the excimer-laser-crystallized (ELC) nanowire TFT, in which the nanowire structure features only-one grain boundary. The other is the spacer-patterned nanowire TFT based on large-grain poly-Si thin film prepared with sequential-lateral-solidification (SLS) crystallization [4.12], in which the nanowire can be controlled to be approximated single-crystalline. From these two devices, the grain-boundary effect can be further discussed to fully understand the physical mechanism of the influence of grain boundary on carrier transport in channel.

(8) Although the three sharp corners of spacer nanowire have been proposed to enhance the program/erase (P/E) efficiency in chapter 5, the different curvature of these three sharp corners would result in different volume of carrier emission and thus the variation of subthreshold swing (S.S.) with different P/E operation time. Thus, it is further worthwhile to round off the sharp corners of spacer nanowire to make the curvatures around the nanowire the same.

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(92 年 9 月～94 年 6 月)

國立交通大學電子工程研究所博士班

（94 年 9 月～98 年 8 月）

論文題目：應用於系統面板之各種薄膜電晶體元件結構之研究

Study on the Thin Film Transistors with Various Device Structures for System-on-Panel Applications