國立交通大學

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博士論文

奈米點應用於先進非揮發性記憶體之製作與特性研究

Fabrication and Electrical Characterization of Advanced Nonvolatile Memories Based on Nanocrystals

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中 文 摘 要

近年來，以傳統浮閘(Floating gate)記憶體為基本元件之非揮發性固態半導體記憶體已被廣泛的應用於各種電子產品。為獲得更高密度、低功率損耗與快速讀寫的操作驅使目前非揮發性記憶體在元件尺寸上持續的微縮。然而傳統浮閘記憶體在寫入與抹除的持續操作後，會在穿遂氧化層產生漏電路徑使得原本儲存的電荷全部流失回到矽基版，而且這個情形隨著尺寸的微縮而更加的嚴重。因此，在資料保存時間(Retention)和耐操度(Endurance)的考量下，微縮穿遂氧化層的厚度是非常困難的。具非揮發性的奈米點記憶體被提出並存有希望可取代傳統浮閘記憶體。由於以空間上與電性上分離的奈米點作為儲存中心，所以可以有效改善尺寸微縮時，記憶體元件在多次讀寫操作後的資料儲存能力。除了奈米點記憶體外，電阻式非揮發性記憶體(RRAM)近年來也成為學者與工業界的焦點。主要是由於其製程簡單且與動態隨機存取記憶體(DRAM)製程相似，可以被整合到半導體的後段製程。電阻式記憶體擁有高速、非揮發性與低電壓操作的特性等優點。

在本論文中，我們將研究鉬(Mo)與鉬化矽作為奈米點材料來克服傳統非揮發性記憶體在微縮過程中會遭遇到的困難。相較於其他金屬材料，鉬具有低價格，高溫熱穩定性，與高功函數等優點。我們首先提出對鉬化矽退火以形成鉬金屬奈米點，並應用在奈米點非揮發性記憶體上。在室溫環境中，利用雙電子槍(dual electron-gun)同時以一比三的比例蒸鍍矽與鉬(Si and Mo)的方式來形成奈米點自

我形成層，再以退火的方式使奈米點形成。在我們的實驗中，我們發現奈米點的大小與組成的成分會因退火的氣氛(ambience)不同而有所差異。在氮氣熱退火下，可以發現所形成的奈米點大約 5-nm 且所組成的成分主要為矽化鉬($MoSi_2$)，而在氧氣退火下，會使得所形成的奈米點大小約 20-nm 且組成成分以氧化鉬為主(Mo oxide)。除此之外，我們發現在氧氣退火前先疊一層氧化矽可阻擋氧化鉬揮發。此為形成氧化鉬奈米點的一個關鍵步驟。

近年來已經發展了許多方法來形成金屬奈米點記憶體，一般而言，大多數的方法都需要長時間的熱退火製程在氧氣的環境下，這個步驟會影響現階段半導體製程中的熱預算和產能且同時造成金屬奈米點過氧化的現像。因此在本論文中，我們使用一個簡單且快速的製程方法來形成金屬鉬奈米點，並將其應用於非揮發性記憶體元件上。我們在氬氣和氧氣(Ar/O_2)的環境中濺鍍鉬與矽的混合層，藉由熱退火於氮氣環境下來形成奈米點。利用形成氧化物時不同形成能(formation energy)的差異，可以在氮氣快速退火的過程中形成金屬奈米點。同樣的我們也利用此方法濺鍍鉬與矽的混合層在(Ar/N_2)的環境中，我們發現，高密度(6×10^{12} cm^{-2})的鉬金屬奈米點可以被形成於氮化矽(SiN_x)中，這將有助於解決奈米點記憶體在元件尺寸微縮時可能造成記憶體元件參數變化的問題。最後我們製作雙層鉬奈米點記憶體結構並探討其特性。相較於單層奈米點，我們發現發現多層奈米點不僅在室溫下且在高溫下都擁有較好的電荷儲存能力和保存能力。

由於許多製作奈米點的方法，諸如離子佈植法(ion implantation)、氧化方法(oxidation)與濺鍍法(sputtering)等都可能在形成奈米點的過程中造成奈米點周遭的介電質受到損害而影響記憶體的特性。因此，我們提出氨(NH_3)電漿處理技術來改善奈米點周遭介電質的品質，以應用於非揮發性奈米點記憶體。氨電漿技術被廣泛的應用於半導體工業，由於它的低溫特性，可以降低製程的熱預算。我們在鉬奈米點嵌入氧化矽與氮化矽的記憶體元件上進行氨電漿的處理，研究中發現藉由氨電漿的處理可以引入氮鍵結於奈米點周遭的介電質。這些氮鍵結可以有效的鈍化介電質中的缺陷，並改善金屬奈米點的記憶體特性。

相較於浮閘金屬奈米點非揮發性記憶體，電阻式記憶體被廣泛的研究以期能整合於後段製程。在論文中，我們研究氧化鋁的電阻式記體特性在不同退火溫度下的影響。研究中發現，傳統金屬/絕緣層/金屬 (MIM)結構之電阻式記憶體元件

的特性會有很大的變化與不穩定性，這增加了元件在設計與操作上的複雜度。因此，我們提出金屬/絕緣層/奈米點/絕緣層/金屬的結構來改善電阻式記憶體的特性。實驗的結果發現，電阻式記憶體的電流不管在開啟(ON-state)或者關閉的狀態(OFF-state)會因為金屬奈米點的嵌入而穩定下來。除此之外，由關閉狀態至開啟狀態的起始電壓變化的範圍也會縮小。最後，我們將對我們的研究主題作一總結。

Fabrication and Electrical Characterization of Advanced Nonvolatile Memories Based on Nanocrystals

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Abstract

Floating gate composed nonvolatile memories (NVMs) have been widely application in electronic devices in recent years. Requirements of high density, low power consumption and high speed operation drive the memory device scaling down. However, all of the charges stored in the floating gate will leak into the substrate if the tunnel oxide has a leakage path in the conventional NVM during endurance test. Therefore, the tunnel oxide thickness is difficult to scale down without influence of retention and endurance characteristics. Nanocrystals (NCs) NVMs are one of promising candidates to substitute for conventional floating gate memory because the discrete NCs as charge storage centers instead of continuous floating gate can effectively improve data retention for the device scaling down. On the other hand,

resistive switching random access memories (RRAM) have recently received academic and industry's attention for its benefit of high density, high operation speed and simple structure. Furthermore, the fabrication process of RRAM is similar to that of DRAM, and therefore can be easily integrated into back-end process of memory device.

In this thesis, we propose Mo and Mo silicide as material for fabrication of nanocrystal to overcome the limitation in conventional NVMs during the scaling down process. Compared with other materials, Mo-based material has advantages of low cost, high thermal stability and high work function. Furthermore, Mo has been proposed for the metal gate, and is compatible with the MOSFET fabrication process. Besides, for back-end memory process, we embedded nanocrystal in RRAM to reduce variation of memory characteristics of RRAM.

First, we proposed a Mo silicide serving as NCs self-assembling layer for application in NCs NVMs. Mo silicide layer was deposited by dual electron-gun evaporation of Mo and Si pellets at room temperature, and a post annealing was performed to form NCs. In our results, we found that annealing ambience can influence the size, density and composition of NCs. When Mo silicide layer annealing in N_2 ambience, the size of NCs is about 5-nm, and the composition of NCs is dominated by $MoSi_2$. However, when annealing in O_2 ambience, Mo oxide NCs was formed and its size is about 20-nm. In addition, we found that a pre-annealing-capping oxide layer is a key process to form Mo oxide NCs.

There are many methods have been develop to form nanocrystals for nonvolatile memory application. Most of the methods need long-term annealing in oxygen ambience. This procedure will influence thermal budget and throughput for the current manufacture technology of semiconductor industries. Hence, a simple and fast fabrication technique of Mo NCs was demonstrated for NVM application in this thesis.

The NVM structure of Mo NCs embedded in the SiO_x layer was fabricated by annealing Mo silicate, which was deposited by sputtering Mo and Si target in Ar and O_2 ambience. In the formation process, the oxygen plays a critical role for the NCs formation during sputter process. A high density (~10^{12} cm^{-2}) NCs also can be simply and uniformly fabricated in our study. We also proposed a formation of Mo NCs embedded in SiN_x by replacing O_2 by N_2 ambience during the sputtering process. A high density Mo NCs was embedded in the silicon nitride (SiN_x) which presented larger memory effect. Therefore, by using internal competition mechanism in charge trapping layer for these elements (Mo, Si, and O or N), we can obtain a metallic NCs NVM with low thermal budget process. Besides, double-layer NCs NVM structure was fabricated in this work. We found that double-layer NCs structure has better charge storage and retention over than single-layer one under high temperature test because of Coulomb blockade effect can be reduce by sharing the stored carriers into both the first layer and second NCs layer. Furthermore, carriers stored in the first layer can build-up Coulomb expulsion force to reduce the tunneling probability of carriers stored in the secondary NCs layer.

Many proposed methods for fabrication of NCs such as ion implantation, oxidation and sputtering are expect to induce defect in the dielectric around nanocrystals, and influence charge storage ability of memory device. Therefore, we used a post treatment of ammonia (NH_3) plasma to improve the quality of the surrounding dielectric. Ammonia plasma treatment has been widely application in semiconductor industry for its low thermal budget. In this work, ammonia plasma treatment was performed on Mo NCs embedded in oxide or nitride. The results indicate that nitrogen bonding can be introduced into surrounding dielectric to passivate defects, and therefore improve the nonvolatile memory characteristics of the memory device.

In addition to floating gate device, we study the resistive switching random access memories (RRAM) for application in back-end nonvolatile memories. Aluminum oxide was employed as resistive switching layer in this work. We found that the variation of resistive switching characteristics in conventional structure, metal/insulator/metal structure, is large. This increases the complexity of designing and operation of the device. Therefore, we proposed metal/ insulator/nanocrystals/ insulator/metal to reduce variation of memory characteristics in RRAM device. In the final part of this dissertation, the conclusion is presented.

Key words: Nanocrystal, Nonvolatile memory, Mo, double layer, RRAM, resistive switching.

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歲月如梭，遙想當年進交大時，我仍是個少不經事的研究生，一路以來，碩士班畢業、念博士班、考資格考、做研究、寫論文與實驗室同仁一起生活的日子仍歷歷在眼前，如今六年來的研究生活已經告一段落了。回首這些日子來的點點滴滴，因為有許多人、事、物的幫助與影響下，才得以完成我的博士生涯。

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昭正 夏

2009 年 7 月於新竹交大

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Chapter 1

Introduction

1.1 Overview of Flash Memory

In recently years, flash memory has been widely used in the portable productions, such as MP3 player, PDA, Notebook, flash driver and so on. Flash memory is nonvolatile, which is that no power is needed to maintain the data storage in the chip. The flash memory can be classified into two types, NOR and NAND flash memories, according to their functions and advantages [1.1]. NOR Flash offers faster read speed and random access capabilities, making it suitable for code storage in devices such as PDA and cell phone. In contrast to NOR flash, the NAND memory, which offers faster write/erase capability and higher density is typically used for storing large quantities of data. Flash memory has several advantages such as fast read access time and better kinetic shock resistance than hard disk. The fabrication process of flash memory is compatible with the current complementary-metal-oxide-semiconductor (CMOS) process and is a suitable solution for embedded memory application. It has become the mainstream nonvolatile memory device in last few decades.

The flash memory is based on the floating gate device, which was invited by Kahng and Sze at Bell Labs in 1967 [1.2]. The floating device, as shown in figure 1-1, is constructed by the MOSFET device with a modified gate stack (tunnel oxide/floating gate/blocking oxide/gate electrode). In the floating device, charges are injected from the silicon substrate across the tunneling oxide and stored in the floating gate. The stored charges can cause a threshold-voltage shift, and the device is at a high-threshold state (programmed). For a well-designed memory device, the stored

charge can maintain in floating gate over 100 years without external power [1.2]. After a suitable erase voltage is applied, the stored charges can be extracted from floating gate, and the device returns to a neutral state (no charges in the floating gate).

To achieve the high density array, low power consumption, high speed operation, and enough reliability on commercial applications, the cell size of floating gate device must be scaling down. However, conventional poly-silicon floating device has a limitation on scaling down of the tunnel oxide. According to the 2007 International Technology Roadmap for Semiconductors (ITRS) flash memory [1.3], tunnel oxide thickness must be more than 6-nm to assure enough retention time, as shown in Fig. 1-2. This basic limitation on tunnel oxide leads to a high programming/erasing voltage and low operation speed for the device. If tunnel oxide were scaling to below 2-nm, the programming/erasing voltage could be reduced to smaller than 4V. Although the thin tunnel oxide can effectively enhance the programming/erasing speed and reduce operation voltage, the thick oxide is required to guarantee the ten years retention time. Furthermore, after endurance test, traps can generate in tunnel oxide, which might induce a leak path in the tunnel oxide and results in the stored charge loss. These difficult trade-off problems hinder the scaling.

To overcome the trade-off problems, discrete trapping center instead of electrically continuous poly-silicon floating gate have been received much attention in recent years [1.4-1.6]. Unlike to the poly-silicon gate, charges stored in the distributed centers can suppress their lateral migration. Therefore, even if an intrinsic defect or extrinsic defect chain exists in the tunnel oxide, they can only influence a few trapping centers allowing aggressive scaling of tunnel oxide. The main realize of discrete trapping center is poly-silicon/oxide/nitride/oxide/Si (SONOS) memory and nanocrystal memory. Both structures have been proposed to reduce the tunnel oxide without sacrificing the retention time.

1.1.1 SONOS Nonvolatile Memory Devices

Since the first nitride based device was proposed by Wegener et al. in 1967s, the device structure has been evolution to SONOS structure. The evolution is shown in Fig. 1-3. Early nitride based device was constituted by metal/nitride/oxide/silicon (MNOS) device in 1967s. It is well known that silicon nitride film have a large number of trapping centers. Therefore, employing the silicon nitride as the charge trapping layer can cause an enough threshold voltage shift for circuit to identify logic "0" and "1". The silicon nitride trap-based devices are widely studied for charge storage device in early 1970s. Initial device structure, MNOS, was constructed by aluminum gate electrode, 45nm-thick silicon nitride layer, silicon oxide and p-channel device. Write/erase voltage of device is as high as 25-30 V. In the late 1970s and early 1980s, the nitride based device move to the n-channel SNOS device with improved write/erase voltages of 14-18 V. In the late 1980s and early 1990s, n- and p-channel SONOS device emerged with low write/erase voltages of 5-12 V. Compared with SNOS device, the SONOS device has some advantages: (a) the device reduces write voltage because the blocking action of the top oxide removes any limitation on the reduction of the nitride thickness; (2) charge transport between gate electrode and nitride trap layer is minimized for both gate polarities, particularly for hole injection; (3) retention is improved because there is a minimal loss of charge for the gate electrode.

In recent years, there has been a dramatic proliferation of research concerned with SONOS memory because its advantages over the conventional floating gate device. These include reduction of operation voltage, increase of operation speed, enhancement of reliability and elimination of drain-induced turn-on [1.7, 1.8]. Unlike to the conventional floating device, charges are stored in distributed trap in nitride layer of SONOS device. Typical traps density is in the order of 10^{18}-10^{19} cm^{-3}

according to the Yang et al.'s calculation [1.9]. The charges stored in the distributed traps can prevent charges from being moving in nitride floating gate layer, and therefore the SONOS device has better endurance than the conventional floating gate memory.

Even though the SONOS memory device has a lot of advantages over the conventional floating gate memory, the SONOS is still face the challenge on the future nonvolatile memory application, which demand for low operation voltage (<5 V), low power consumption, long-term retention, and excellent endurance. Various approaches have been proposed for improving the SONOS performance and reliability, such as nitride bandgap engineering, device structure engineering and high-k material as the charge storage layer [1.10]. Chen et al. proposed a Si_3N_4 bandgap engineering method to improve the endurance and retention characteristics. A nitride layer with different Si/N ratio throughout the layer can significantly increased the charge trapping efficiency [1.11].

T. Sugizaki et al. proposed HfO_2 and Al_2O_3 as the charge trapping layer to replace the silicon nitride. They found that employing HfO_2 or Al_2O_3 as the charge trapping layer can improve the program/erase speed. The Al_2O_3 with high valence band shift to Si substrate can prevent the memory from being over-erase. Tan et al. showed that over-erase phenomenon in SONOS memory can also be minimized by replacing silicon nitride with mixed HfO_2 and Al_2O_3 as the charge storage layer. The charge retention and endurance performance was improved by the addition of 10% Al_2O_3 in HfO_2 to form HfAlO thin film as the charge trapping layer [1.12]. M. She et al. demonstrated that high quality nitride instead of SiO_2 as the tunnel dielectric for SONOS structure memory can improve the programming speed and retention time under a low programming voltage [1.13]. C. H. Lee et al. proposed a nitride based device structure of SiO_2/SiN/Al_2O_3/TaN metal gate (SANOS) [1.14]. The charges in

the SiN layer can be erased efficiently by Fowler-Nordheim tunneling mechanism of holes even at thicker tunnel oxide where the holes direct tunneling is suppressed. The effect of TaN gate with higher work function than poly-silicon gate can improve the program/erase characteristics of the SANOS devices. The use of TaN metal gate can block electron current through the Al_2O_3 more efficiently than a conventional poly-silicon gate, which results in faster program/erase speed, and significant decrease of the saturation level of the erase V_{TH}.

S. C. Chen et al. studied a polycrystalline silicon thin film transistor with oxide/nitride/oxide stack gate structure and multiple nanowire channels for nonvolatile SONOS memory application [1.15]. The proposed structure can improve electrical characteristics including increase of drain current, a steep subthreshold slop and excellent program/erase efficiency due to the tri-gate structure and channel corner effect. Such structure is thereby highly promising to application on future system-on-panel display application.

Novel device structures are also indispensable to make the floating gate nonvolatile memory more scalable. SONOS memory device can make tunnel oxide decreased, and a FinFET structure has the better controlling capability on short channel effect than the conventional MOSFET structure. FinFET embedded with nitride layer as the floating gate (FinFET SONOS memory) has been demonstrated with a small cell size to provide excellent performance and reliability. Hence, FinFET SONOS memory is also a potential candidate for next generation floating gate nonvolatile memory [1.16, 1.17].

1.1.2 Nanocrystal Nonvolatile Memory Devices

The nanocrystal memory is a direct descendant of conventional floating gate memory [1.4]. The biggest difference between nanocrystal and conventional floating

gate memory is the manner of charge storage. In conventional floating gate memory, charges are stored in electrically continuous polycrystalline silicon floating gate. However, charges are stored in the separated nanocrystals for the nanocrystal memory. Fig. 1-4 illustrates a typical nanocrystal memory device. As shown in the Fig., the nanocrystals are separated by their surrounding dielectric. When programming voltage is applied on gate electrode, carriers can inject from conduction channel to the nanocrystals. The injected carriers can store in the lateral isolated nanocrystals. Each nanocrystal will typically store only a handful of electrons and the charges stored in these nanocrystals collectively control the channel conductivity. The first nanocrystal memory device was proposed in 1995 by S. Tiwari et al, who demonstrated the nonvolatile memory device with a Si nanocrystals floating gate [1.18]. They showed that a large bistability with a significant threshold voltage shift can be obtained at low bias voltages with built-in Coulomb blockade of additional carrier injection.

Using the nanocrystals as charge storage media instead of poly-Si floating gate has several advantages. First, memory with discrete charge storage elements allow more aggressive scaling of the tunnel oxide and exhibit superior characteristics compared to Flash memories in terms of operation voltage and write/erase speed. The main reason for the improvement is because charges stored in electrically isolated nanocrystals are more immunity to local defect chain. Due to the absence of drain with floating gate coupling, nanocrystal memory suffers from less drain-induced-barrier-lowering (DIBL) effect than conventional floating gate device. This advantage allows the use of a high drain bias in read operation mode, and therefore improves the memory access time. Furthermore, Nanocrystal memories are characterized by excellent immunity to stress induced leakage current (SILC) and oxide defect due to the distributed nature of charge storage. Research in the nanocrystal memories have focused on the development of fabrication processes,

nanocrystal materials and integration of nanocrystal based storage layer in real memory devices.

The process for fabrication nanocrystal memory requires well control on four important parameters: (1) Tunnel oxide thickness. The oxide thickness must be well controlled and uniformity must be good enough to prevent the variation from cell to cell. (2) The quality of blocking oxide. The quality of the oxide must ensure that the carrier cannot tunnel from gate electrode to nanocrystal layer. (3) The density of nanocrystal and (4) the size of nanocrystal. Considering the nanocrystal size, larger nanocrystal size provides high program/erase efficiency because the larger size of nanocrystal suffers from smaller quantum confinement and coulomb blockade effects. However, it is desirable to reduce the nanocrystal size to achieve a high density of nanocrystal on the channel for a uniform devices array. Therefore, there is a trade-off in the nanocrystal size. A typical target is a density of 10^{12} cm^{-2}, and this require nanocrystal size of about 5-nm.

The ideal goal in optimizing the nanocrystals memory device is to achieve both the fast write/erase of DRAM and the long retention time of Flash memories. For this purpose it is needed to produce an asymmetry in charge transport through the gate dielectric to maximize the ratio of $I_{G,write/erase}$ / $I_{G,retention}$.

So far, there are many materials have been proposed for nanocrystal nonvolatile memory application such as Si, Ge, HfO_2, CeO_2, Co, Ni, Pt and Mo. These materials can be classified into three categories: semiconductor, high-k dielectric and metallic nanocrystals. Fig. 1-5 shows the band diagram for the (a) Ge, (b) HfO_2 and (c) Mo.

A. Semiconductor Nanocrystal Memories

Since S. Tiwari et al. proposed the first Si nanocrystal memory device, there is much research on improving the retention and endurance characteristics of the device.

R. Ohba et al. proposed that self-aligned doubly stacked Si nanocrystals as the floating gate to enhance the memory characteristics [1.18]. Their structure is shown in Fig. 1-6(a). The mechanism for improving the memory characteristics is originated from the quantization effect on the lower nanocrystal. As indicated in Fig. 1-6(b), the smaller nanocrystal at the bottom has larger quantum confinement effect over than that for the larger nanocrystal. Therefore, after the charge inject into the upper nanocrystal, the charge is blocked by lower nanocrystal, which improves the retention of the memory. However, this method needs a well control on size of nanocrystal and the oxide layer between the upper and lower nanocrystals.

King and Hu demonstrated that the superior properties of Ge nanocrystal memory over those based on Si in terms of writing/erasing and retention time because smaller band gap of Ge. Recently, the simulation results indicated that the Ge/ Si heteronanocrystal improves the retention characteristics dramatically without influencing the writing/erasing speed. J. Lu et al. demonstrated the Charge storage characteristics in the metal-oxide-semiconductor memory structure based on gradual $Ge_{1-x}Si_x$/Si heteronanocrystals. Their results show that the retention of hole was improved. The main reason for improved retention of hole is due to additional Si barrier to block the hole, as shown in Fig. 1-7.

Although various methods has been proposed to improve the reliability of semiconductor nanocrystal memories, the nanocrystal suffer from a severe quantum confinement effect. The quantum confinement effect can widen the band gap as the decrease of the nanocrystal size. Theoretical calculation shows that Ge nanocrystal will experience a serious conduction band shift when its size is smaller than 5-nm. This effect limits the ultimate size of nanocrystal and impedes the device scaling down.

B. High-k dielectrical Nanocrystal Memories

Two bits operation through charge storage in nitride layer upon drain or source side have been widely investigated. The crucial issue for two bits operation is migration of the stored charge, which degrades the threshold voltage shift (or memory window). To alleviate the issue, Chen et al. proposed the high-k dielectric nanocrystal nonvolatile memories in 2004 [1.19, 1.20]. They fabrication the nanocrystal by using co-sputtering Hf and Si in oxygen followed with high-temperature annealing to form the high-k dielectric nanocrystal for SONOS-type memory devices. These devices are not only like SONOS-type nonvolatile memory but also can restrain the stored charge lateral migration effect. Therefore, the performance of high-k dielectric nanocrystal for 2-bits operation is better than SONOS-type memory device.

C. Metallic Nanocrystal Memories

In optimizing nonvolatile memory device, the ideal goal is to achieve the fast write/erase of DRAM and long retention time of Flash memories simultaneously. For this purpose we need to create an asymmetry in charge transport through the gate dielectric to maximize the $I_{G,\ Write/Erase}/I_{G,\ Retention}$ ratio. One approach to achieve this goal is to engineer the depth of the potential well at the storage nodes, thus creating an asymmetrical barrier between the substrate and the storage nodes, i.e., a small barrier for writing and a large barrier for retention. This can be achieved if the storage nodes are made of metal nanocrystals. Then by engineering the metal work function, the barrier height can be adjusted by about 2 eV, giving much freedom for device optimization.

Compared with semiconductor or high-k dielectric nanocrystal memories, the metal nanocrystals memories have several advantages include higher density of states around the Fermi level, stronger coupling with the conduction channel, a wide range

of available work functions, and smaller energy perturbation due to carrier confinement [1.21]. Furthermore, electrostatic modeling from both analytical formulation and numerical simulation is demonstrated that the metal nanocrystals can significantly enhance the electric field between the nanocrystal and the conduction channel, and hence can achieve much higher efficiency in low-voltage operation [1.22].

In the future, the driving force behind the development of nanocrystal memory is its potential on scaling device structure without sacrificing reliability and improving operation speed. Nevertheless, there are still challenges await nanocrystal memories in the long road to commercialization.

1.1.3 Conclusion

Nanocrystal memories have been presented in the mid-nineties as a possible alternative to conventional floating-gate nonvolatile memory, by allowing a further decrease in the thickness of tunnel oxide. Research in this area has focused on the development of nanocrystal materials and fabrication processes, and on the integration of nanocrystal-based storage layers in actual memory devices. Although, various methods have been investigated to improve nanocrystal memory characteristics, it is also a rigorous challenge on nanocrystal memory for next generation nonvolatile memory in term of uniformity of nanocrystal size and its reliability.

1.2 Motivation

According to the Semiconductor Industry Association (SIA) International Technology Roadmap for Semiconductors (ITRS) report, it can be realize that the severe challenges of floating gate flash are to achieve reliable, low-power, and high

program/erase speed [1.3]. The challenges are originated from: (1) the limitation on the thickness of tunnel oxide, and (2) reliability of the memory device. For the tunnel oxide thickness, the ITRS report indicated that the oxide thickness of floating gate device is restricted to 6-nm to guarantee enough retention time for memory applications. However, high speed and low power operation require the thinner tunnel oxide. In order to get balance between program/erase speed and retention time, there is a trade-off between the speed and the retention to get the optimal tunnel oxide thickness. On the other hand, the limitation on reliability is due to the stress induced formation of leakage path in tunnel oxide. As the memory device suffer from a large number of program/erase cycles, the carrier transport through tunnel oxide can generate the leakage path, which results in total stored charge leak out of the floating gate through the generated leakage path. Therefore, the conceptual of discrete charge storage media instead of continuous poly-Si floating gate was proposed to surmount the limitations and realized through charge trapping layer (such as nitride layer with traps) and discrete nanocrystals. Unlike to the floating gate, the charge stored in discrete centers can alleviate the trade-off between the high speed operation and long term retention, allowing further scaling down of the memory devices.

1.3 Organization of This Thesis

In this thesis, we investigated the molybdenum-based nanocrystal memory to overcome the limitation of conventional floating gate memory. Furthermore, we introduce nanocrystal into resistance switching memory RAM (RRAM) to enhance the memory characteristics.

Chapter 1 introduces the function and characteristic of NOR and NAND flash memory. Furthermore, discrete charge storage type memories including SONOS-type and nanocrystal-type are organized and discussed. The evolvement of the

SONOS-type memory and the research of current status on the nanocrystal memory are reviewed.

In chapter 2, we briefly describe the programming/erase operations of the majority of Flash memories described in the literature. Some important mechanisms such as Programming/Erasing mechanisms, basic Physical characteristic, and reliability of nonvolatile memory and Gibbs free energy are reviewed. The programming/Erasing can be performed by different tunneling mechanism.

In chapter 3, we investigate the nonvolatile memory characteristics of Mo silicide nanocrystal memory through annealed electron-gun evaporated Mo silicide layer in different ambience. Mo nanocrystal can be formed after annealed in N_2 ambience. However, the retention of the Mo nanocrystal is not ideal. The retention can be improved by introduce oxygen during annealing process due to reduce the Si dangling bonds in surrounding dielectric.

In chapter 4, Mo nanocrystal embedded in silicon oxide (SiO_x) and nitride (SiN_x) as charge storage layer is studied. Mo nanocrystal can form in the SiO_x after annealing oxygen-incorporated Mo silicide layer at a critical temperature without degrading the tunnel oxide. It is found that the memory window and retention are influenced by various annealing temperature. Furthermore, the density of nanocrystal can be increased by annealing nitrogen-incorporated Mo silicide layer. The Mo nanaocrystal in SiN_x have larger memory window than Mo nanocrystal in SiO_x because the high density of nanocrystal and high permittivity of nitride can enhance the coupling to the conduction channel.

In chapter 5, we investigate the ammonia plasma treatment influence on Mo nanocrystal memory. It is found that the treatment can improve the quality of surrounding dielectric by nitrogen passivation. After the passivation, the memory characteristic of Mo nanocrystal in dielectric can be improved. In addition, we

compare the memory characteristics between Mo in SiO_x and Mo in SiN_x as charge storage layer. The different characteristics are explained through charging effect.

Resistance switching memory emerges as a new candidate for future nonvolatile memory. The resistance switching memory has a capacitor-like structure composed of insulating or semiconducting materials sandwiched between two metal electrodes. Because of its simple structure, highly scalable cross-point and multilevel stacking memory structures have been proposed. In chapter 6, the reproducible and stable resistance switching phenomenon in Al_2O_3 is demonstrated. The Ni silicide nanocrystal is introduced into Al_2O_3 to enhance the memory characteristics.

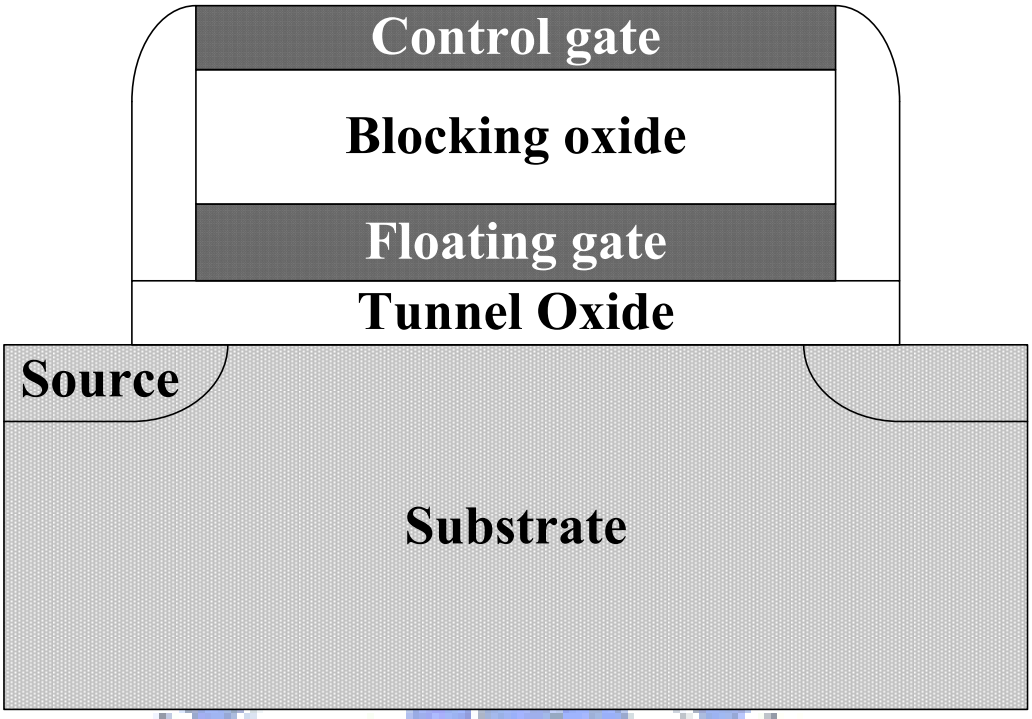


Figure 1-1 Structure of the conventional floating-gate nonvolatile memory device. Electronically continuous poly-silicon floating gate is employed as the charge storage media.

Year of production	2004	2007	2010	2013	2016
Technology node (nm)	90	65	50	35	25
Flash NOR Lg(um)	0.2-0.22	0.19-0.21	0.17-0.19	0.14-0.16	0.12-0.14
Flash NOR highest W/E voltage (V)	7-9	7-9	7-9	7-9	7-9
Flash NAND highest Voltage (V)	17-19	15-17	15-17	15-17	15-17
NOR tunnel oxide(nm)	8.5-9.5	8-9	8-9	8	8
NAND tunnel oxide(nm)	7-8	6-7	6-7	6-7	6-7

Solution exist | Solution known | Solution NOT known

Figure 1-2 Tunnel oxide and operation voltage scaling predicted by the 2007 International Technology Roadmap for Semiconductors.

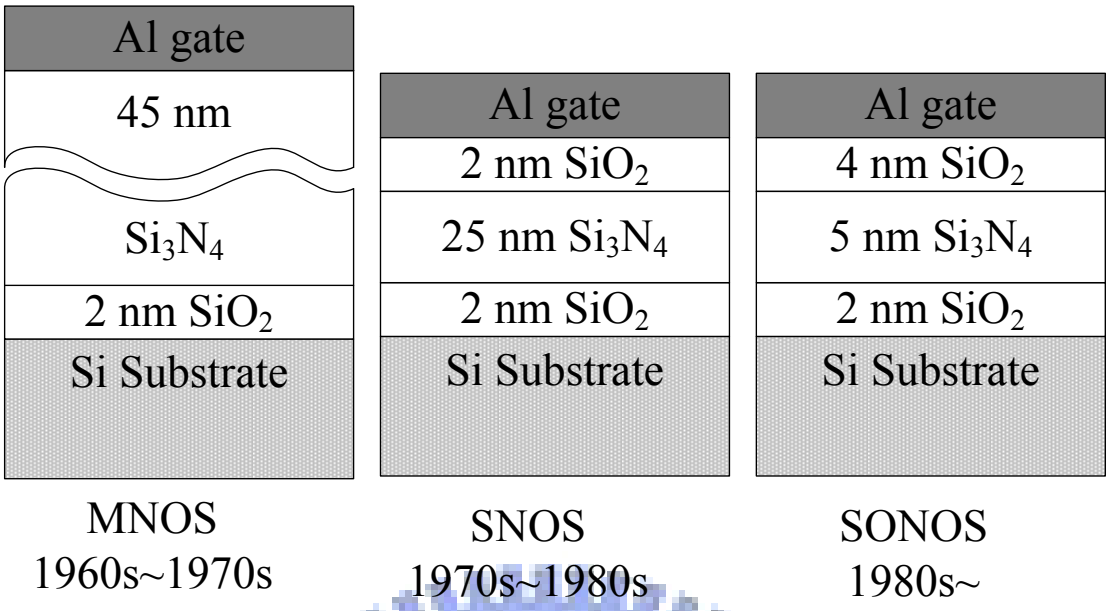


Figure 1-3 Development of the gate stack of SONOS EEPROM memory devices. The optimization of nitride and oxide films has been the main focus in recent years.

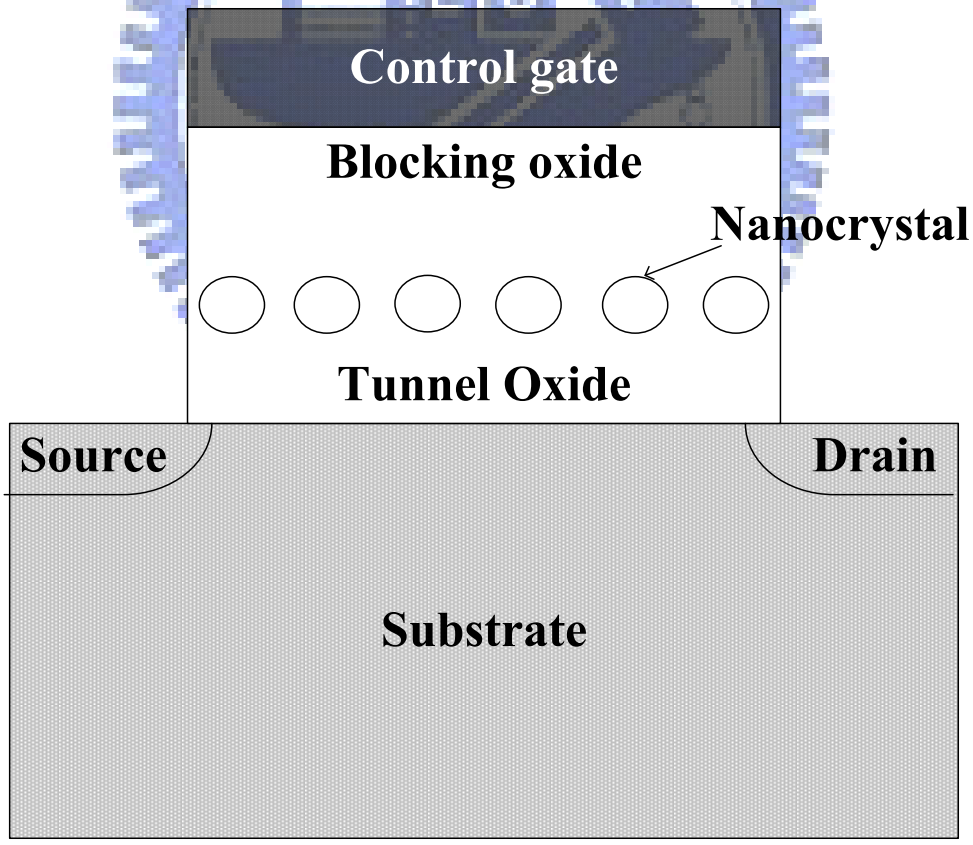


Figure 1-4 structure of the nanocrystal nonvolatile memory device. The nanocrystals are used as the charge storage element instead of the continuous poly-Si floating gate.

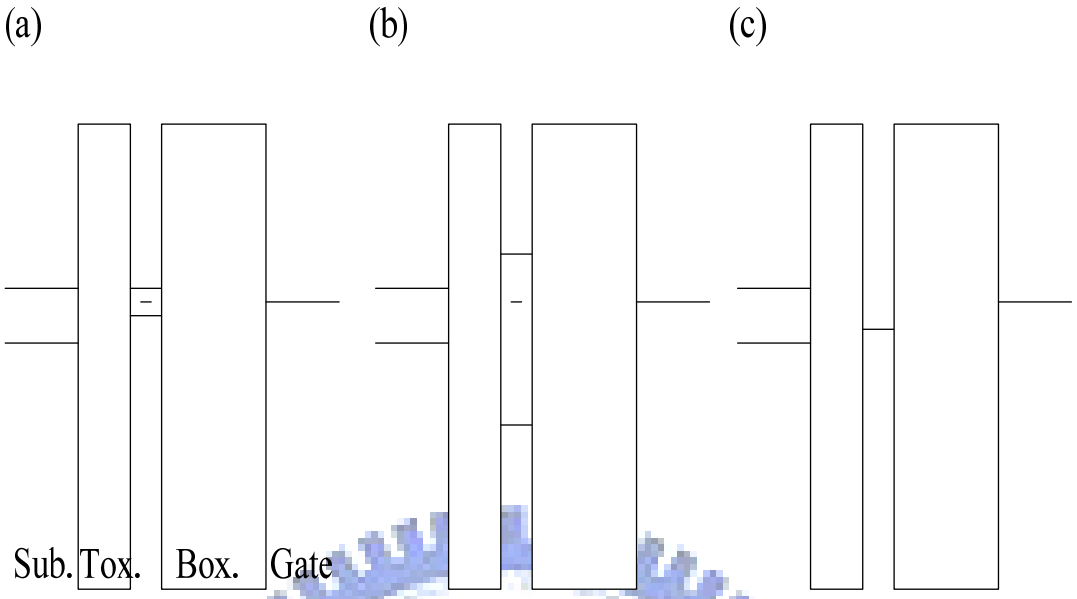


Figure 1-5 The band diagram for the (a) Ge, (b) HfO_2, (c) Mo nanocrystals. Sub.: substrate, Tox.: tunnel oxide, Box.: blocking oxide.

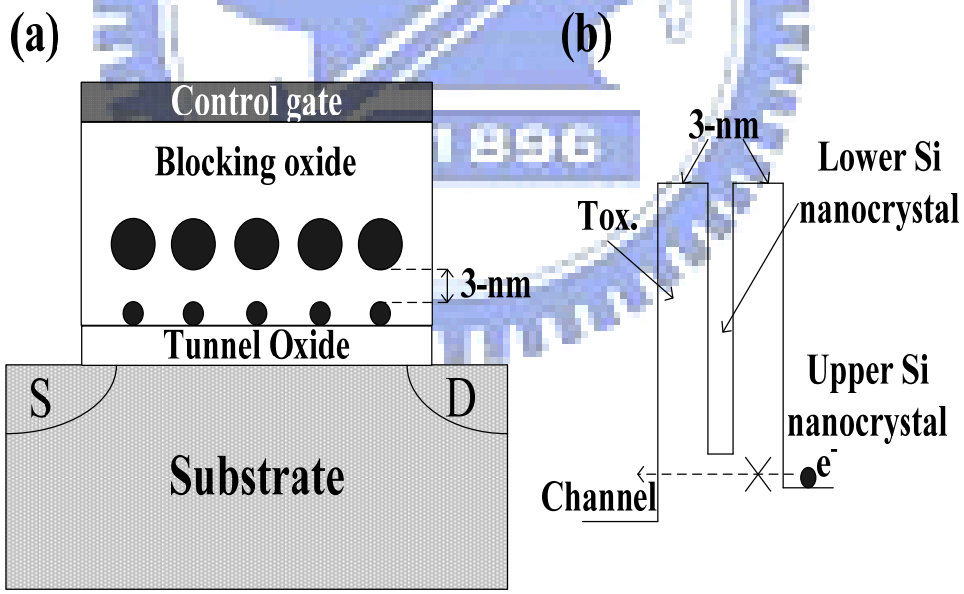


Figure 1-6 (a) self-aligned doubly stacked Si nanocrystals device and (b) energy band diagram of the structure

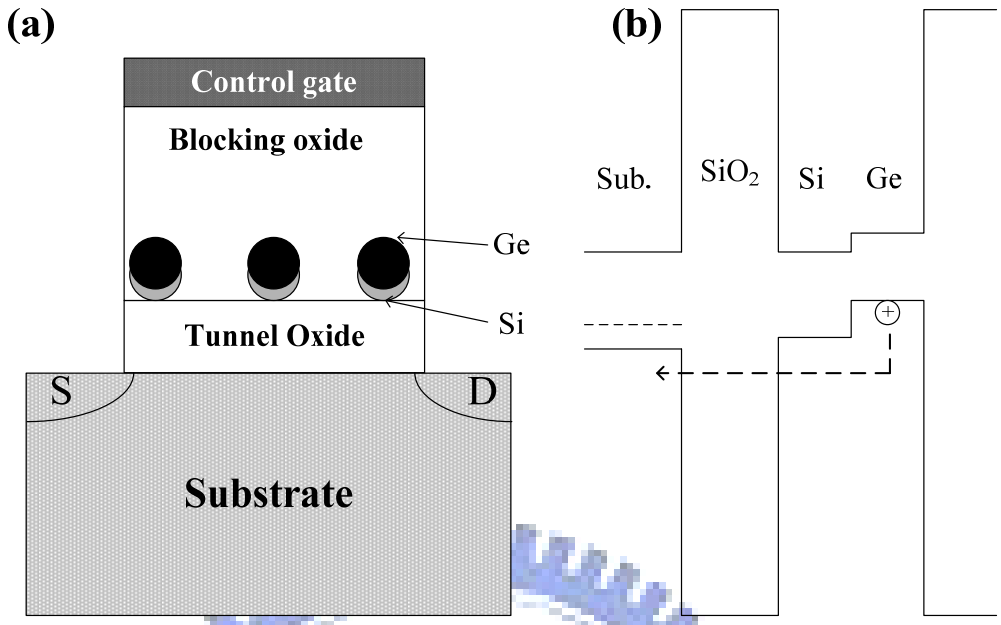


Figure 1-7 (a) Schematic diagram of the p-channel memory device using Ge–Si as floating gates. (b) Energy-band structure of the memory.

Chapter 2

Basic Principles of Nonvolatile Memory

2.1 Programming/Erasing mechanisms of nonvolatile memory

Charge storage based nonvolatile memories (NVMs), such as nanocrystal memory and polycrystalline silicon/silicon oxide/nitride/silicon oxide/silicon substrate (SONOS) structure memory, are based on the conceptual of floating gate device. Using various programming mechanism, after charging, the total stored charge Q is equal to integrated injection current. This results in a shift of the threshold voltage by the amount

$$\Delta V_T = -\frac{d_2 Q}{\varepsilon_2} \tag{2-1}$$

where Q is the total charge stored in the floating gate, and C_{FG} is the capacitances between the floating-gate (FG) and control gate [2.1-2.3].

Two methods are used to measure the threshold-voltage shift: (1) change in the channel conductance g_D of the MOSFET which is measured at small drain voltages. The channel conductance of an n-channel MOSFET is given by

$$g_D = \frac{I_D}{V_D} = \frac{Z}{L}\mu C_{ox}(V_G - V_T), \qquad V_G > V_T, \tag{2-2}$$

and (2) I_D-V_G plot as shown in Fig. 2-1. After the programming, the floating-gate of the memory are charged with a number of negative charges and results in threshold-voltage shift to a higher level (Curve B), which is defined as a state of "1" in binary. On the other hand, the stored charge can be removed after erasing and the threshold-voltage changes from the higher value to a lower one, which is defined as a state of "0" (curve A).

There are many mechanisms can be used to programming and erasing the memory cell. In general, the mechanisms can be divided into two categorizes, hot carrier injection and tunnel effect including direct tunneling, Fowler-Nordheim tunneling and band to band tunneling. These mechanisms for programming/erasing of memory cell can result in difference characteristics and we will briefly introduce them at the following.

Models for programming/erasing

2.1.1 Tunneling effect

Tunneling mechanisms is a quantum mechanical phenomenon. Unlike to classical mechanics, an electron can be represented by its wave function. The function does not terminate on the side wall of a finite potential barrier but can penetrate into the barrier as shown in Fig. 2-2. The tunneling probability can be calculated from the Schrodinger equation. For complicated barrier shapes, simplification of the equation is made by the WKB (Wentzel-Kramers-Brillouin) approximation if the potential $U(x)$ is a slow function of x. The tunneling probability can then be calculated by

$$T_t = \frac{|\psi_B|^2}{|\psi_A|^2} \approx \exp\{-2\int_{x_1}^{x_2}\sqrt{\frac{2m^*}{\hbar 2}[U(x)-E]}dx\}. \quad (2\text{-}3)$$

With tunnel probability eqn. (2-3), the tunneling current J_t can be calculated from the production of the number of available carriers in the Region-A, and the number of empty states in the region-B,

$$J_t = \frac{qm^*}{2\pi^2\hbar^3}\int F_A N_A T_t (1-F_B) N_B dE \quad (2\text{-}4)$$

where F_A, F_B, N_A, and N_B are the Fermi-Dirac distributions and densities of states and the subscript represents the corresponding regions.

For the different profile of potential barrier, the tunneling effect can be classified

into four different tunneling mechanisms, direct tunneling (DT), Fowler-Nordheim tunneling (FN), modified Fowler-Nordheim tunneling (MFN) and trap assistant tunneling (TAT). These mechanisms are the main carrier transport mechanisms employed in the floating gate NVM. Fig. 2-3 shows these four tunnel effects.

A. Direct Tunneling effect (DT)

For nanocrystal memories, the control-gate coupling ratio of nanocrystal memory devices is inherently small [2.4]. As a result, FN tunneling cannot serve as an efficient write/erase mechanism when a relatively thin tunnel oxide is used because the strong electric field cannot be confined in one oxide layer. When the thickness of tunnel oxide is below 5 nm, the direct tunneling is employed in nanocrystal memories instead. Furthermore, the direct tunneling is more sensitive to the barrier width than barrier height. However, two to four orders of magnitude reduction in leakage current can still be achieved if the metals with a large work function, such as Au or Pt, which corresponding to high barrier height , [2.5].

B. Fowler–Nordheim Tunneling effect (FN)

One of most important injection mechanism employed in floating gate devices is the Fowler—Nordheim tunneling, which is a field—assisted electron tunneling mechanism. Electrons in the silicon conduction band see a triangular energy barrier with a width dependent on the applied field. The height of the potential barrier is determined by the electrode material and band structure of SiO_2. At sufficiently high field, the energy band diagram of the SiO_2 is very steep and thin enough to allow that the electrons can tunnel into the conduction band of SiO_2. Using a free-electron gas model for the metal and the WKB approximation for the tunneling probability [2.6], one obtains the following expression for current density [2.7]:

$$J = \frac{q^3 F^2}{16\pi^2 h^2 \Phi_B} \exp\left[\frac{-4(2m_{OX}^*)^{1/2}\Phi_B^{3/2}}{3\hbar qF}\right] \quad (2\text{-}3)$$

where Φ_B is the barrier height, m^* is the effective mass of the electron in the forbidden gap of the dielectric, h and $\hbar$ is the Planck's constant and the constant divided by 2π, q is the electronic charge, and F is the electric field through the oxide. However, the exponential dependence of tunnel current on the oxide-electrical field causes some critical problems on device process control because, for example, a very small variation of oxide thickness among the cells in a memory array produces a great difference in programming or erasing currents, thus spreading the threshold voltage distribution in both logical states.

C. Modified Fowler-Nordheim tunneling (MFN)

Modified Fowler–Nordheim tunneling (MFN) is frequently observed in SONOS-type memories where the operation is designated to low-voltage (<10V, depending on the Equivalent oxide thickness). A relatively small electric field on tunnel oxide cannot drive charges to inject into the charging trapping layer by DT or FN mechanism. Therefore, the electrons in conduction of the gate should tunnel through the oxide barrier and a triangular nitride barrier, which is MFN tunneling.

D. Trap assistant tunneling effect (TAT)

The charge storage mediums with many traps may cause another tunneling mechanism. For example, the charges tunnel through a thin oxide and arrive to the traps of nitride layer at very low electric field in SONOS systems. During trap assisted injection, the traps are emptied with a smaller time constant and then they are filled. The charge carriers are thus injected at the same distance into the nitride as for MFN injection. Because of the sufficient injection current, trap assistant tunneling

may influence in retention [2.8].

2.1.2. Channel Hot-Electron Injection

The physical mechanism of Channel Hot-Electron Injection (CHEI) can be simply understood qualitatively. An electron traveling from the source to the drain gains energy from the lateral electric field and loses energy to the lattice vibrations (acoustic and optical phonons). At low fields, this is a dynamic equilibrium condition, which holds until the field strength reaches approximately 100kV/cm [2.9]. For fields exceeding this value, electrons are no longer in equilibrium with the lattice, and their energy relative to the conduction band edge begins to increase. Electrons are "heated" by the high lateral electric field, and a small fraction of them have enough energy to surmount the barrier between oxide and silicon conduction band edges. Figure 2-4 shows schematic representation of CHEI in n-MOSFET. On the other hand, the effective mass of hole is heavier than one of electron. It is too hard to obtain enough energy to surmount oxide barrier. Therefore, hot-hole injection is rarely employed in nonvolatile memory operation. For an electron to overcome this potential barrier, three conditions must be held [2.10].

1) Its kinetic energy must be higher than the potential barrier.

2) It must be directed toward the barrier.

3) The field in the oxide should be collecting it.

Nevertheless, a description of the injection conditions can be accomplished with two different approaches. The CHEI current is often explained and simulated following the "lucky electron" model [2.11]. This model is based on the probability of an electron's being lucky enough to travel ballistically in the field for a distance several times the mean free path without scattering, eventually acquiring enough energy to cross the potential barrier if a collision pushes it toward the Si/SiO_2 interface.

Consequently, the probability of injection is the lumped probability of the following events, which are depicted in Figure 2-5 [2.12].

1) The carrier has to be "lucky" enough to acquire enough energy from the lateral electric field to overcome the oxide barrier and to retain its energy after the collision that redirects the electron toward the interface ($P_{\Phi b}$).

2) The carrier follows a collision-free path from the redirection point to the interface (P_{ED}).

3) The carrier can surmount the repulsive oxide field at the injection point, due to the Schottky barrier lowering effect, without suffering an energy-robbing collision in the oxide (P_{oc}).

The current density of CHEI is expressed as

$$I_{inj} = A_d I_{ds} (\frac{\lambda E_m}{\varphi_b})^2 \exp(-\varphi_b / \lambda E_m) \quad (2\text{-}4)$$

Here I_{ds} is the channel current and A_d is a constant. φ_b is the injection barrier and λ is the mean free path associated with the phonon scattering. E_m is the lateral electric field at drain.

2.1.3. Band to Band Tunneling (BTBT)

Band to band tunneling application to nonvolatile memory was first proposed in 1989. Chen et al. demonstrated a high injection efficiency (~1%) method to programming EPROM devices [2.13]. Band-to-band Tunneling (BTBT) process occurs in the deeply depleted doped surface region under the gate to drain / gate to source overlap region. In this condition, the band-to-band tunneling current density is expressed as

$$I_{inj} = A_d I_{ds} (\frac{\lambda E_m}{\varphi_b})^2 \exp(-\varphi_b / \lambda E_m) \quad (2\text{-}5)$$

(a) Band to Band Hot Electron Tunneling Injection

This injection mechanism is used to nonvolatile memory of PMOS structure. When band-bending is higher than the energy gap of the semiconductor, the tunneling electron from the valence band to the conduction band becomes significant. The mechanism is at the condition for positive gate voltage and negative drain voltage. Hence, the hot electrons are injected through the tunnel oxide and then recombine the stored electrons as shown in Fig. 2-6.

(b) Band to Band Hot Hole Tunneling Injection

The injection is applied for NMOS nonvolatile memory device. The mechanism is at the condition for negative gate voltage and positive drain voltage. Hence, the hot holes are injected through the tunnel oxide and then recombine the stored electrons as shown in Fig. 2-7.

The electrons (n-type) / holes (p-type) are accelerated by a lateral electric field toward the channel region and some of the electrons with sufficient energy can surmount the potential barrier of SiO_2 [2.14-2.16]. Due to the small oxide field, the electron/hole influence through the oxide can easily reach hundreds of coulombs per square centimeter without failure, it means to the improvement reliability of memory cells.

2.1.4. Channel Initiated Secondary Electron Injection (CHISEI)

The main difference between CHE and CHISEI is that the CHISEI is operation as CHE with a negative bias on body (V_B). The CHISEI is highly sensitive to the lateral electrical field and vertical electrical filed. The procedure and the band diagram for the application of CHISEI are as shown in Fig. 2-8. The superior injection of CHISEI operation mode leads to a better program efficiency. The improved program efficiency results from the substrate enhanced gate current component. Under

optimized substrate condition, the substrate hot carriers and subsequent injection are expected for the application of low power and high speed.

2.2 Basic Physical Characteristic of Nanocrystal Memory

In the nanocrystal memory, due to the small size of the nanocrystal (3~5 nm), the quantum effect will be obviously. Furthermore, storage carriers in nanocrystal can raise the potential energy due to Coulomb effect. Both quantum effect and Coulomb effect can influence the memory characteristics of the nonvolatile memory.

2.2.1 Quantum Confinement Effect

The quantum dot is a quasi-zero-dimensional nano-scale object and is also composed by small amount of atoms. The quantum confinement energy depended on nanocrystal size has been studied both experimentally and theoretically with the tight-binding model [2.17]. The quantum confinement effect becomes significant when the nanocrystal size shrinks to the nanometer range, which causes the ground state of nanocrystal to shift to higher energy compared with bulk material [2.18]. This result will reduce the barrier high, the difference between work function of the nanocrystal and tunnel oxide. The reduction of the barrier will degrade charge storage ability and programming efficiency for the semiconductor nanocrystals. The theoretical shift of ground state for semiconductor and metal nanocrystals has been proposed by W. Guan et al. at 2007 [2.19]. The ground state shift (ΔE) of Ge and Mo nanocrystals are expressed as

$$\Delta E_{Si} = E(\infty) + \frac{1.39}{d_{Si}^2 + 1.788 d_{Si} + 0.688} \quad \text{and} \quad \Delta E_{Mo} = \frac{0.231}{d_{Mo}^3} \tag{2-6}$$

Where E (∞) is the conduction band minimum for bulk Si and d is the diameter of nanocrystal. For example, a 3 nm Si nanocrystal can have a conduction band shift of 0.1 eV as compared with bulk Si, which is significant enough to affect the electrical

performance of the nanocrystal memory cell. Figure 2-9 shows the conduction band minimum up-shift of Si and Ge nanocrystal, and Fermi level up-shift of metal NC as a function of nanocrystal size by W. Guan's model.

2.2.2 Coulomb Blockade Effect

When an electron is stored in nanocrystal, the potential energy of nanocrystal raised with electrostatic charging energy $e^2/2C_{nc}$, where C_{nc} is the nanocrystal capacitance. The C_{nc} is dependent on nanocrystal size, permittivity and thickness of surrounding dielectric, the tunnel oxide and the blocking oxide. The capacitance is self-consistently calculated using an electrodynamics method [2.20]. The electron charge will raise the nanocrystal potential energy and reduce the electric field across the tunnel oxide, resulting in reduction of the tunneling current density during the write process. It is more dominant at low programming voltages (< 3V). In a flash memory array, device cells often encounter disturbances with low gate voltage soft-programming. The Coulomb blockade effect can effectively inhibit the electron tunneling at low gate voltage and improve the flash memory array immunity to disturbance. However, the Coulomb blockade effect should be reduced by employing large nanocrystal if large tunneling current and fast programming speed were desired. The Coulomb blockade effect has a detrimental effect on the retention time because the electrons in the nanocrystal are inclined to back into the channel by tunneling if the nanocrystal potential energy is high in retention mode.

2.3 Reliability of Nonvolatile Memory

Unlike to logic IC, nonvolatile memory is more concerned with reliability than performance. The reliability includes two parts, retention and endurance. Both reliability tests are very importance for nonvolatile memory application to the

portable electronic productions market and they are norm to define the charge loss ratio in the long-term use. In general, nonvolatile memory must be able to bear 100K-1M program/erase cycles (endurance), and has 10-year retention. Therefore, in this section, the authors will present the operation mechanisms and related non-ideal factors of retention and endurance tests.

A. Retention

For nonvolatile memory, the data information must be conserved over than ten years. This means that the charge loss rate of the stored carriers in the floating gate or discrete trapping centers have to be as low as possible. For example, in modern Flash cells, floating gate capacitance is approximately 1 fF. A loss of only 1 fC can cause a 1V threshold voltage shift. If we consider the constraints on data retention in ten years, the charge loss rate has to less than five electrons per day [2.21].

The possible origins of charge loss are through: 1) tunneling or thermionic emission mechanisms; 2) defects in the tunnel oxide; and 3) de-trapping of charge from insulating layers around the storage medium. Several discharge mechanisms may be responsible for time and temperature dependent on retention behavior of nonvolatile memory devices. Figure 2-11 shows an energy band diagram of SONOS device in the excess electron state [2.22], illustrating trap-to-band tunneling, trap-to-trap tunneling, and band-to-trap tunneling, thermal excitation and Poole-Frenkel emission retention loss mechanisms.

These mechanisms can be classified into two categories. The first category contains tunneling processes that are not temperature sensitive (trap-to-band tunneling, trap-to-trap tunneling and band-to-trap tunneling). The second category contains those mechanisms that are temperature dependent. Trapped electrons may redistribute vertically inside the nitride by Poole–Frenkel emission, which will give rise to a shift

in the threshold voltage. Moreover, at elevated temperatures, trapped electrons can also be thermally excited out of the nitride traps and into the conduction band of the nitride (thermal excitation), and drift toward the tunnel oxide, followed by a subsequent tunneling to the silicon substrate.

Besides, the defects generated in the tunnel oxide can bring about decline in retention because the trap can assist carrier tunneling out of storage centers. The defects can be divided into an extrinsic and an intrinsic one. The former is stem from defects in the device structure; the latter originate from the physical mechanisms that are employed to program and erase the cell. Moreover, charges can be trapped in the insulating layers around the storage medium during wafer processing, as a result of the plasma damage, or during the UV exposure which is normally used to bring the cell into a well-defined state at the end of the process. The charges can subsequently de-trapping with time, especially at high temperature. The charge variation results in a variation of the storage medium potential and thus in channel length decrease [2.23]. The retention capability of Flash memories have to be checked by using accelerated tests that usually adopt screening electric fields and hostile environments at high temperature.

B. Endurance

Endurance is a number of erase/write operations. Generally speaking, Flash products are specified for 10^6 erase/program cycles. Nevertheless, the endurance requirement may be relaxed with the increase of memory density for the other applications. The endurance requirement is relaxed to 100K cycles for 256 MB memory. In the higher density, a certain cell in a block has less possibility to be written and erased since the memory operation on the cell is repeated after using up the whole memory blocks. The endurance requirement is sufficient for the user to take

700 photos with a 1MB size every day for 10 years. A typical result of an endurance test on a single cell is shown in Fig. 2-12. As the experiment is performed by applying constant pulses, the variations of threshold voltage for program and erase state are described as “program/erase threshold voltage window closure” and give a measure of the tunnel oxide degradation [2.25, 2.26]. The reduction of programmed threshold voltage with cycling is due to trap generation in the oxide and to interface state generation at the drain side of the channel. The evolution of the erase threshold voltage reflects the dynamics of net fixed charge in the tunnel oxide as a function of the injected charge. The initial lowering of the erase is due to a pile-up of positive charge which enhances tunneling efficiency, while the long-term increase of the erase is due to a generation of negative traps.

Moreover, a high field stress on thin oxide is known to increase the current density at low electric field. The excess current component, which causes a significant deviation from the current–voltage curves from the theoretical FN characteristics at low field, is known as stress-induced leakage current (SILC). SILC is clearly attributed by stress-induced oxide defects, which leads to a trap assisted tunneling, as shown in Fig. 2-13. The main parameters controlling SILC are the stress field, the amount of charge injected during the stress, and the oxide thickness. For fixed stress conditions, the leakage current increases strongly with decreasing oxide thickness [2.27-2.28].

2.4 Gibbs free energy

In thermodynamics, the Gibbs free energy is a thermodynamic potential which measures the "useful" or process-initiating work obtainable from an isothermal, isobaric thermodynamic system. When a system changes from a well-defined initial state to a well-defined final state, the Gibbs free energy (ΔG) equals the work

exchanged by the system with its surroundings, less the work of the pressure forces, during a reversible transformation of the system from the same initial state to the same final state. The change (ΔG) in Gibbs free energy is a parameter to measure a spontaneous tendency of the reaction. The ΔG is usefully defined by

$$\Delta G = \Delta H - T\Delta S \quad (2\text{-}7)$$

Where H is the enthalpy, T is temperature, and S is the entropy. If ΔG is negative, the reaction is a spontaneous. If ΔG is positive, the reverse reaction is a spontaneous. The larger ΔG value indicates that the reaction is easier to take place with higher reaction rate. After reaction, the ΔG value represents the energy which is released as heat to the environment. At chemical equilibrium, the rate of forward reaction is equal to the rate of reverse reaction, ΔG = 0. In generally, the ΔG value is nearly dominated by the enthalpy (ΔH) because the TΔS value is much less than ΔH.

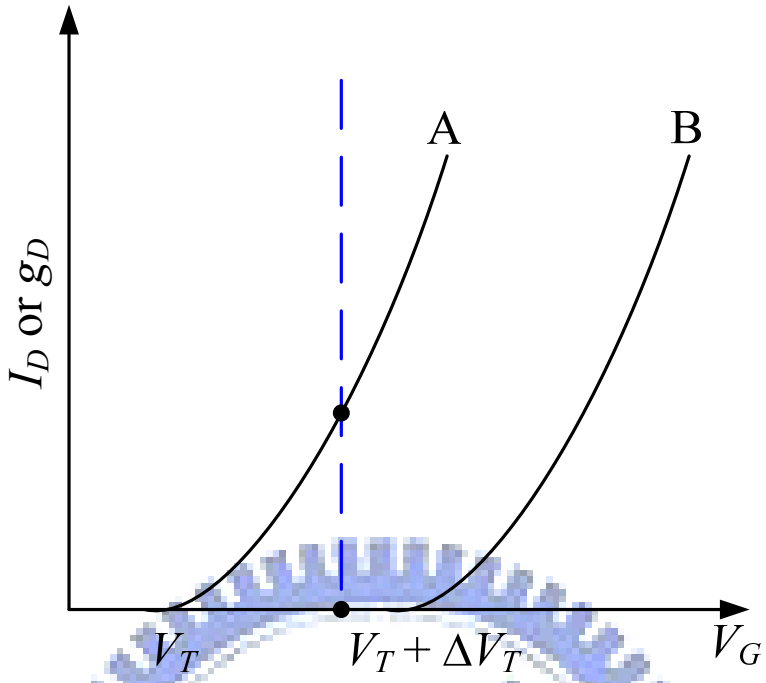


Fig. 2-1 I_D– or g_D–V curves of an FG device when there is no charge stored in the FG (curve A) and when negative charges are stored in the FG (curve B).

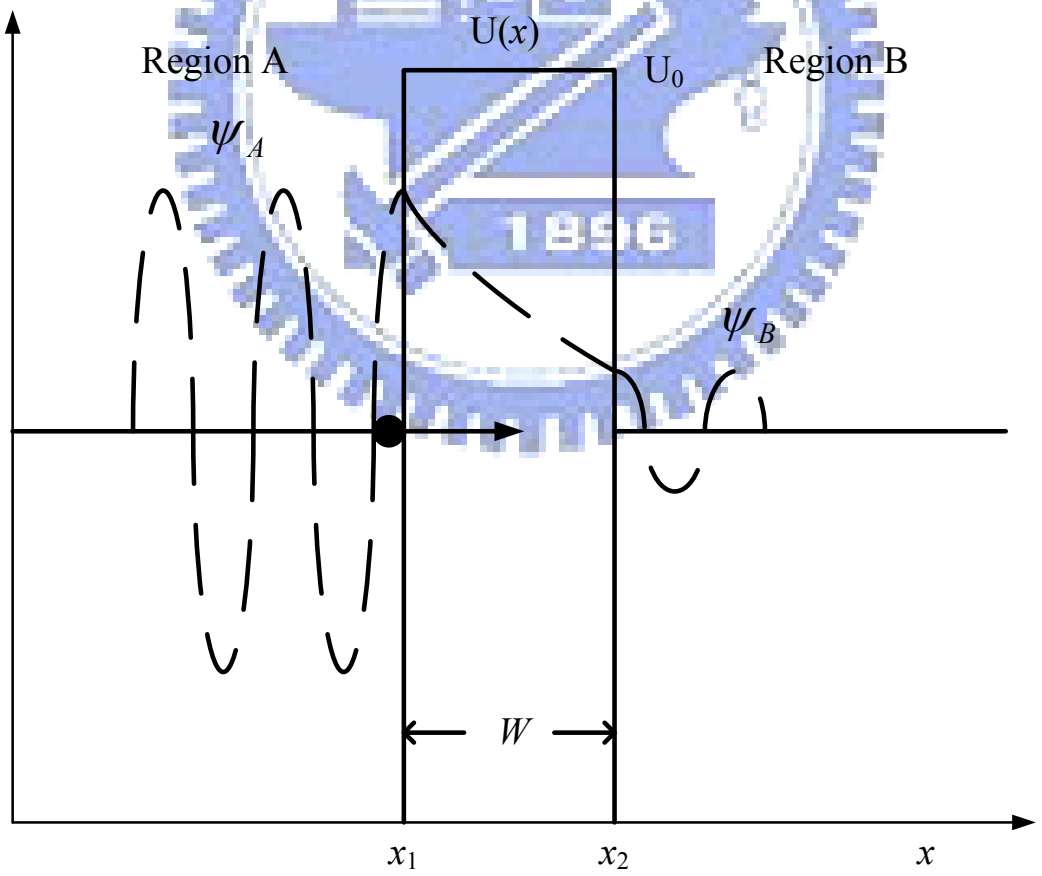
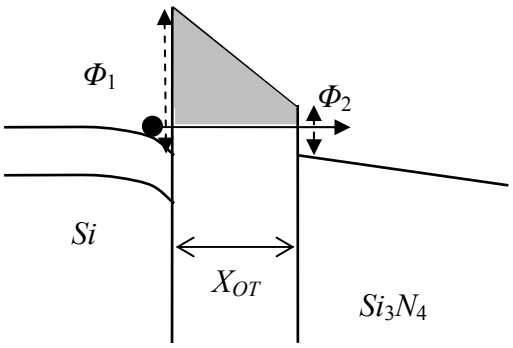
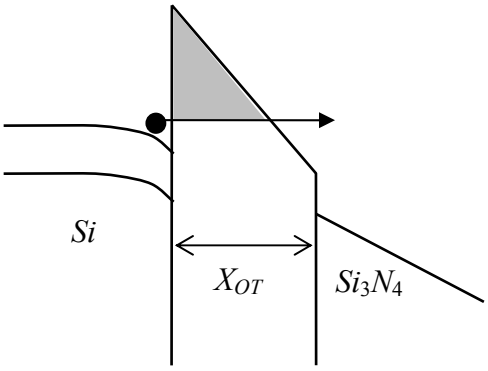


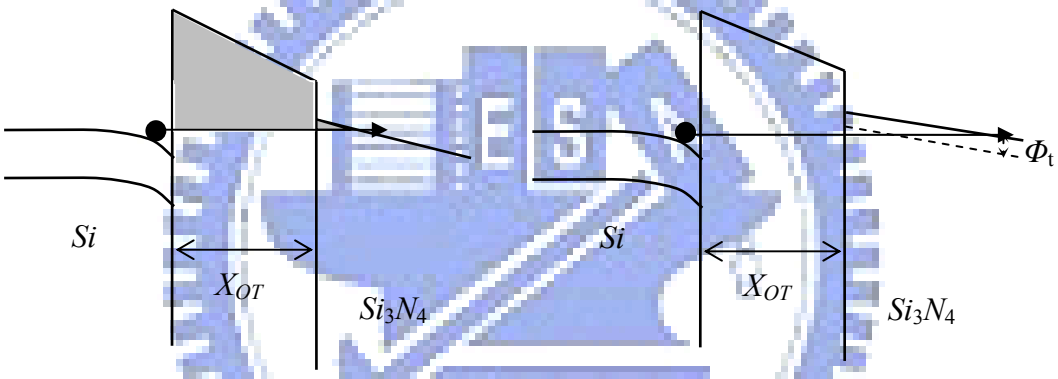
Fig. 2-2 Wavefunctions exhibiting electron tunneling through a rectangular barrier.





DT occur when $\frac{\Phi_1}{X_{OT}} > |E_{OT}| > \frac{\Phi_1 - \Phi_2}{X_{OT}}$

FN occur when $|E_{OT}| > \frac{\Phi_1}{X_{OT}}$



MFN occur when

$$\frac{\Phi_1 - \Phi_2}{X_{OT}} > |E_{OT}| > \frac{\Phi_1 - \Phi_2}{X_{OT} + \left(\varepsilon_{ox} / \varepsilon_N\right) X_N}$$

TAT occur when

$$\frac{\Phi_3}{X_{OT}} > |E_{OT}| > \frac{\Phi_3}{X_{OT} + \left(\varepsilon_{ox} / \varepsilon_N\right) X_N}$$

$$\Phi_3 = \Phi_1 - \Phi_2 - \Phi_t$$

Fig. 2-3 Four tunnel mechanisms in the nonvolatile memory described by Hu and White et al.

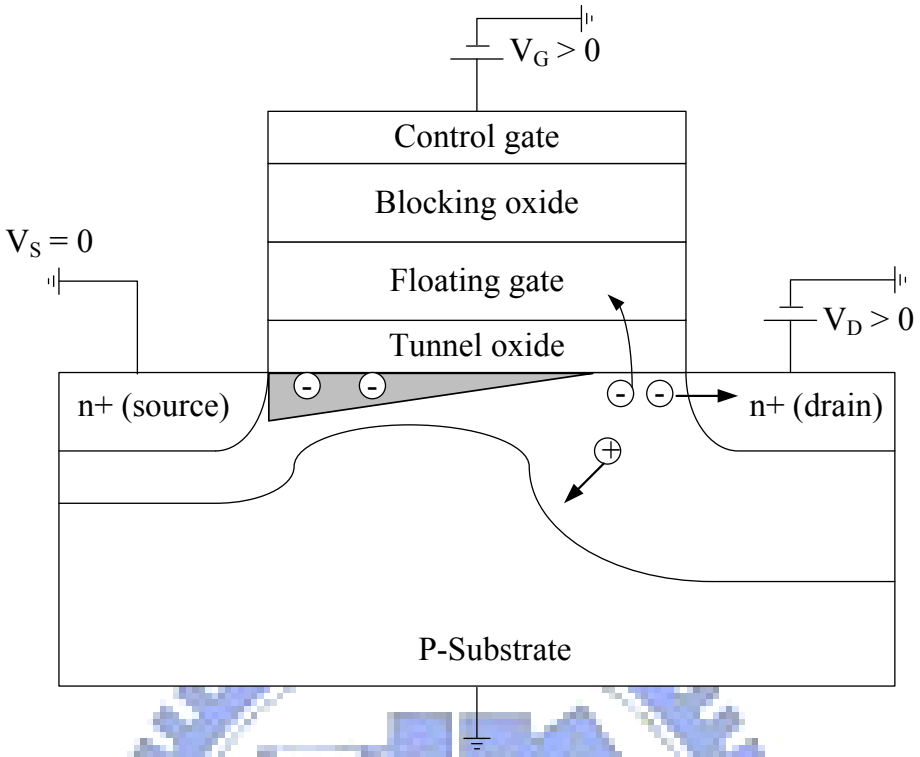


Fig. 2-4 Schematic cross section of MOSFET.

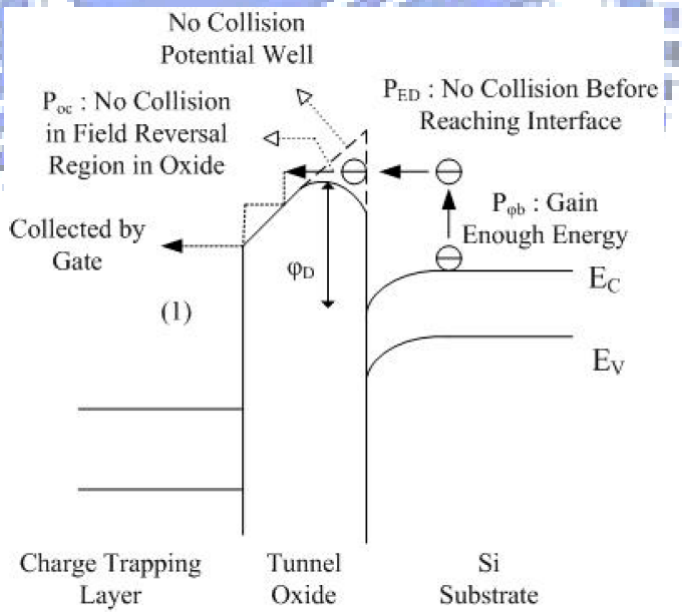


Fig. 2-5 Schematic energy band diagram describing the three processes involved in electron injection.

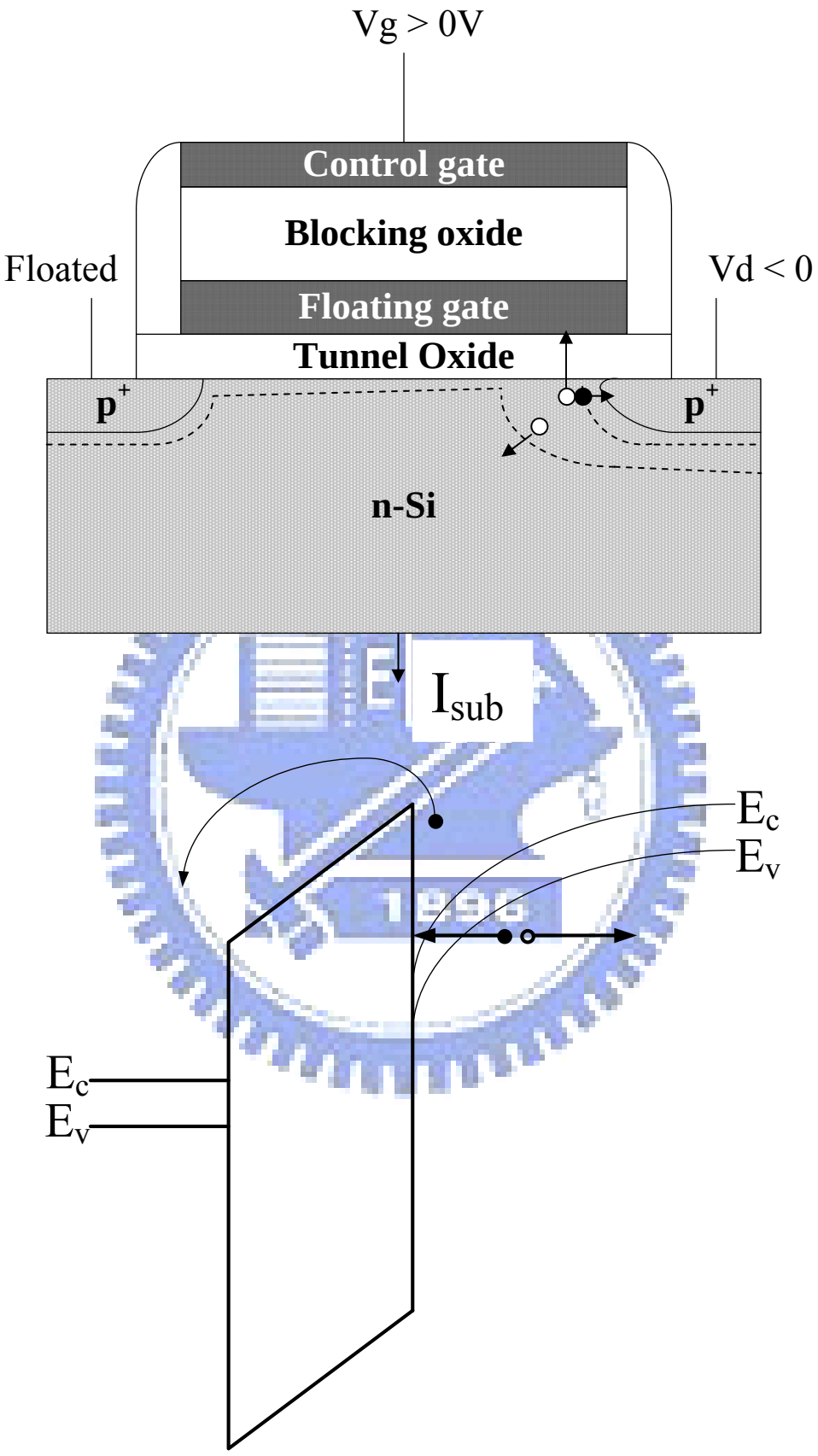


Figure 2-6 Schematic sketch and energy band diagram of Band to Band Hot hole Injection.

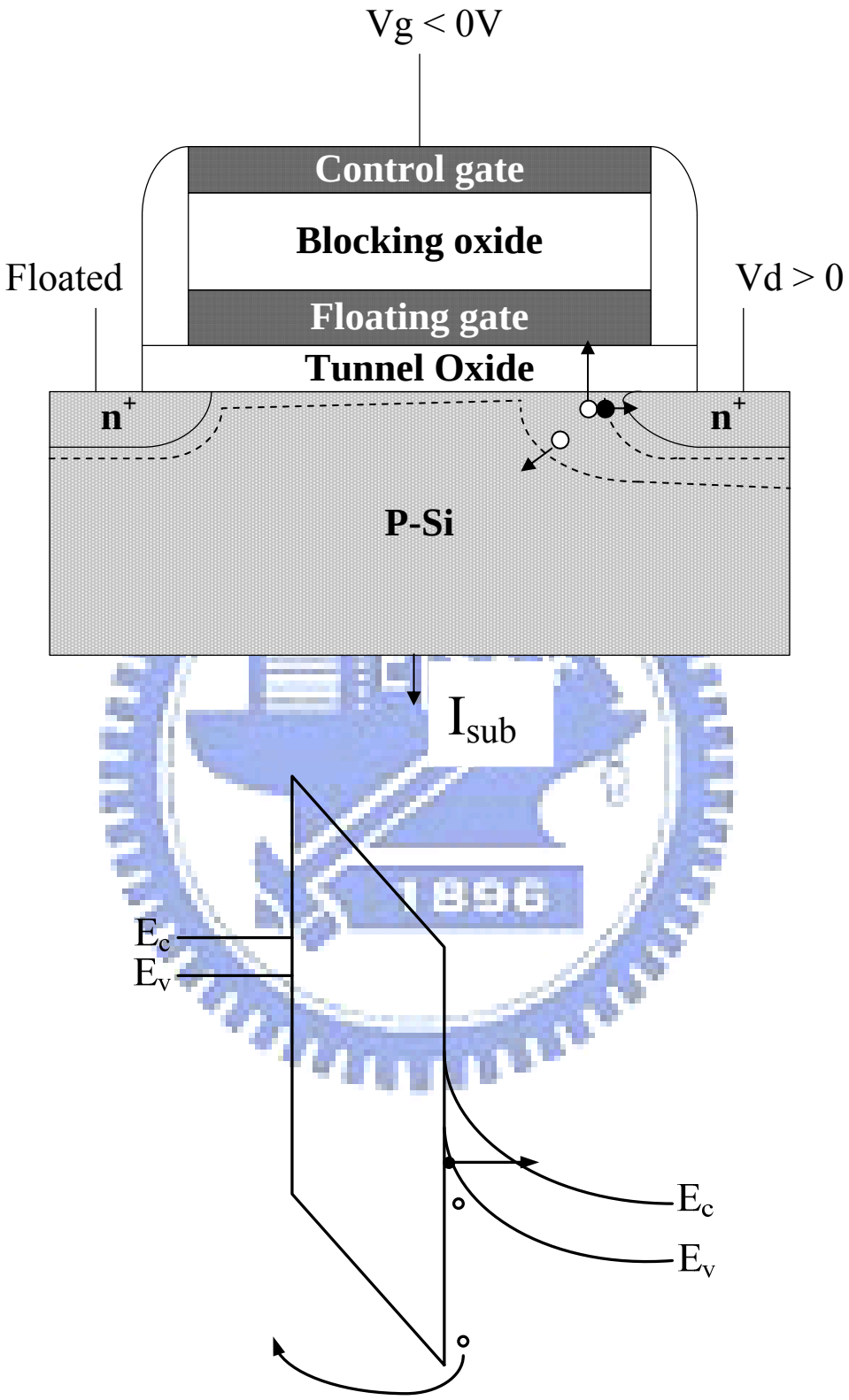


Figure 2-7 Schematic sketch and energy band diagram of Band to Band Hot hole Injection.

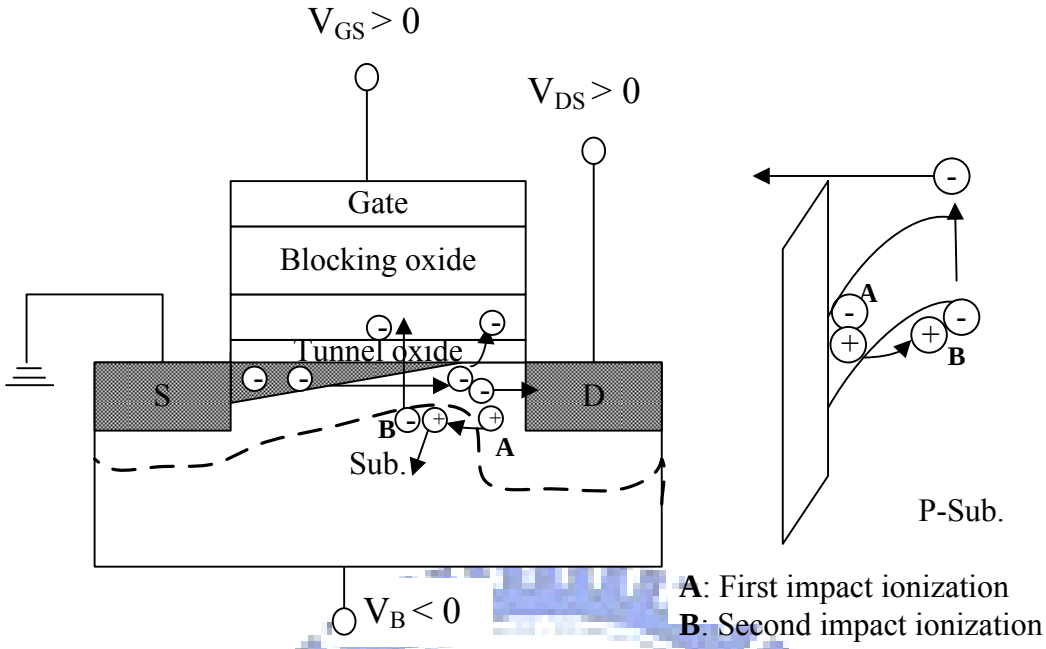


Figure 2-8 Schematic sketch and energy band diagram of Channel Initiated Secondary Electron Injection.

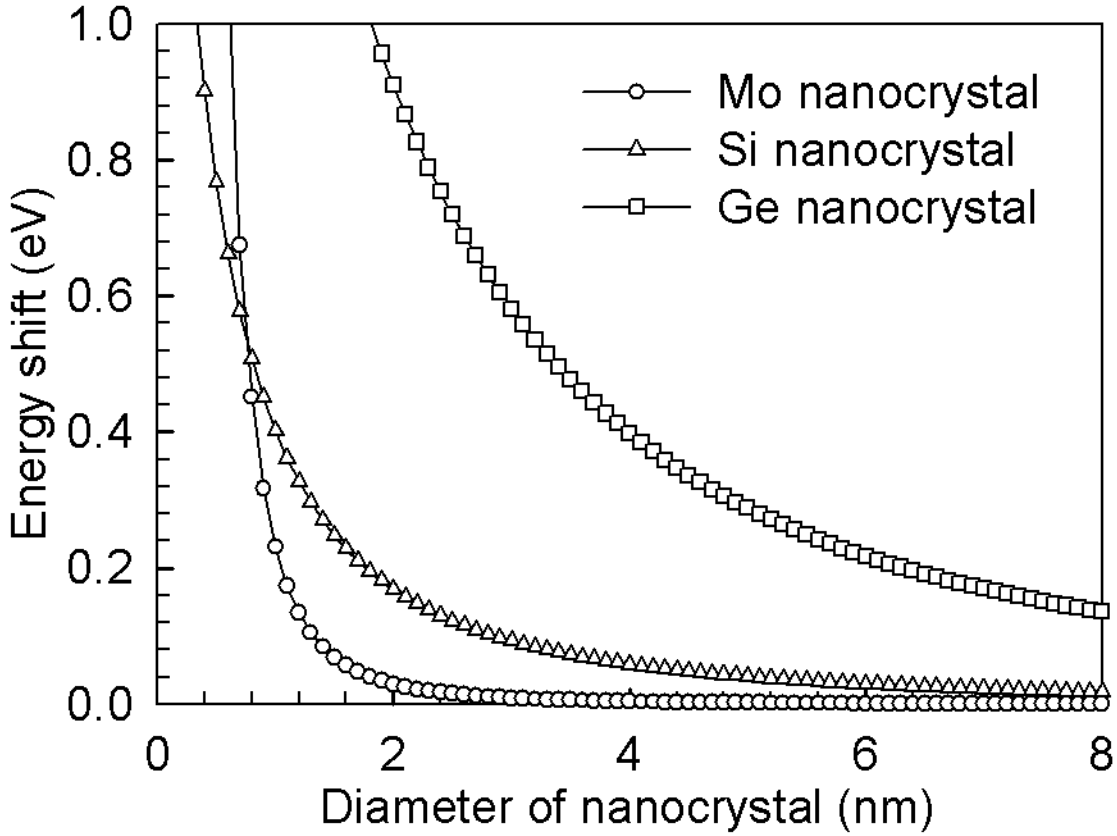


Figure 2-9 Conduction band minimum up-shift of silicon nanocrystal and Fermi level up-shift of metal NC as a function of nanocrystal size by W. Guan's model [2.19].

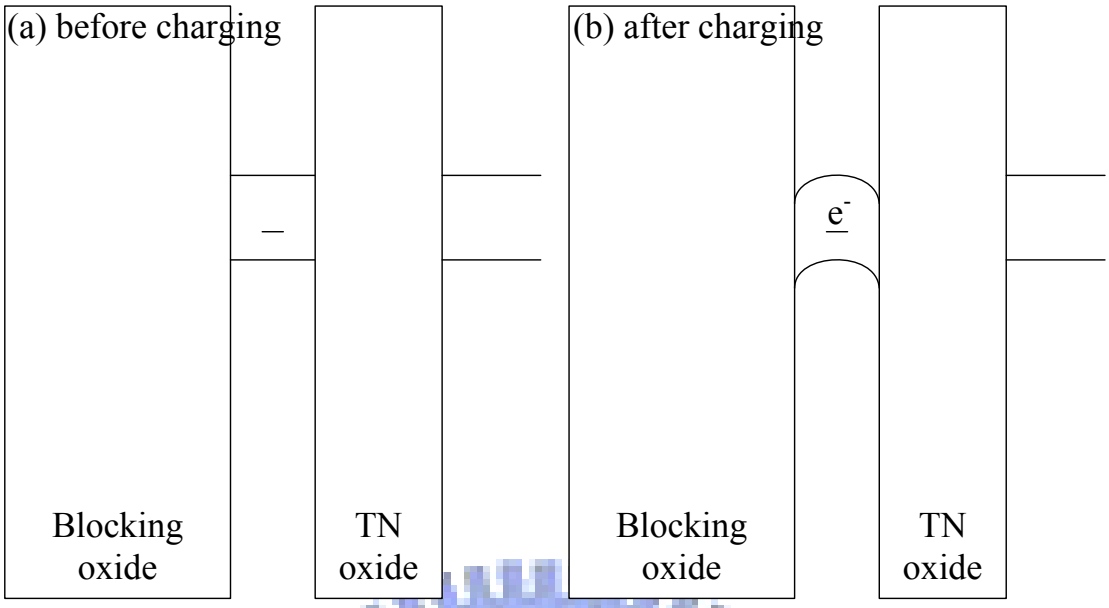


Figure 2-10 Conduction band minimum up-shift of silicon nanocrystal and Fermi level up-shift of metal NC as a function of nanocrystal size by W. Guan's model [2.19].

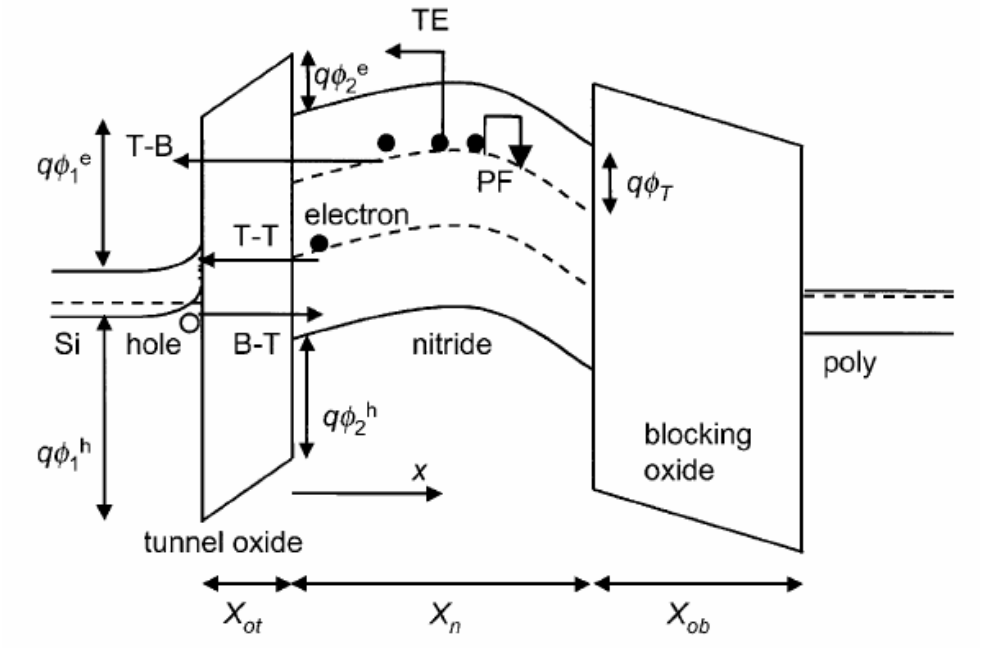


Figure 2-11 Energy band diagram of a SONOS device in the excess electron state, showing retention loss mechanisms: trap-to-band tunneling (TB), trap-to-trap tunneling (T-T), band-to-trap tunneling (B-T), and thermal excitation (TE) and Poole–Frenkel emission (PF) [2.22].

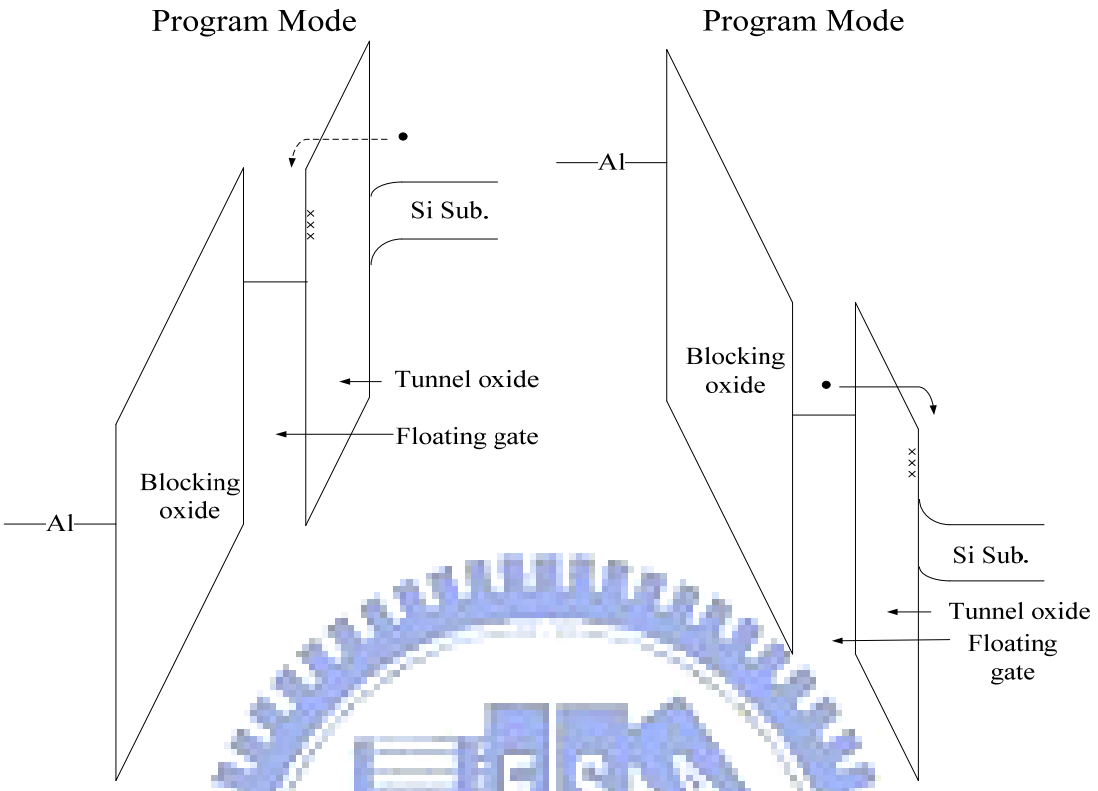


Figure 2-12 Threshold voltage window closure as a function of program/erase cycles on a single cell owing to the degradation of tunnel oxide.

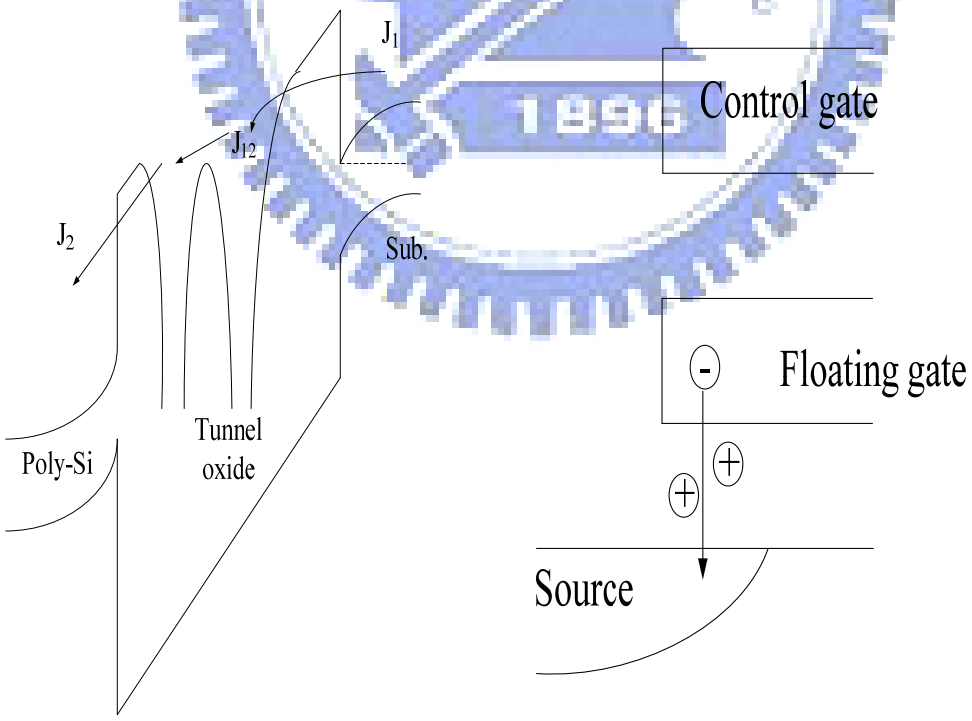


Figure 2-13 Anomalous SILC model. The leakage is caused by a cluster of positive charge generated in the oxide during erase.

Chapter 3

Molybednum-silicide-based nanocrystal nonvolatile memories

3.1 Formation and memory characteristics of molybednum silicide nanocrystal embedded in oxide

3.1.1 Introduction

Floating gate (FG) device composed of nonvolatile memory (NVM) is widely application to portable productions. The device is made up of the metal-oxide-semiconductor field-effect transistor (MOSFET) embedded with a continuous conductive poly-Si layer in the gate oxide for charge storage [3.1]. To enable high-speed and low power consumption operations of the device, the oxide layer has to be scaled down, especially the oxide layer between the FG and Si substrate (tunnel oxide). However, the long retention time demands a thick tunnel oxide to prevent the stored charges from leaking out of the FG [3.2]. One way to satisfy the conflicting requirements on tunnel oxide is to employ the distributed nanocrystal (NCs) as the discrete charge trapping centers [3.3]. Recently, much attention has been directed toward metallic NCs for their several advantages, such as a stronger coupling with the conduction channel and a wide range of available work functions [3.4]. Metal silicide has been studied for the fabrication of NC memory for their extensive applications on the semiconductor fabrication process [3.5-3.8] Furthermore, a conventional MOSFET required a high-temperature process for dopant activation (900°C) [3.9]. Therefore, the thermal stability of NCs should also be considered. Mo silicide has been proposed for the metal gate, and is compatible with the MOSFET fabrication process due to its high thermal stability [3.10]. Mo silicide is

thus an attractive candidate for NC memory application. However, little research has been done on Mo silicide for NC memory application. In this article, the mixed Mo–Si layer was investigated as an NC self-assembling layer [3.6].

3.1.2 Experiment

Figure 3-1 exhibits the device structure and process flow in this work. A 6 in. p-type silicon wafer with (100) orientation was cleaned by a standard RCA cleaning process, followed by a dry oxidation process at 950°C in an atmospheric pressure chemical vapor deposition furnace to form a 5 nm thick tunnel oxide. Subsequently, a 10 nm thick mixed Mo–Si layer was deposited onto the tunnel oxide by dual electron-gun (E-gun) evaporation. A 30 nm thick oxide layer was then deposited on the mixed Mo–Si layer as the blocking oxide layer, which was utilized to prevent the carriers of the gate electrode from injecting into the charge trapping layer by Fowler–Nordheim tunneling. The blocking oxide was deposited by a plasma-enhanced chemical vapor deposition (PECVD) system at 300°C with precursor gases N_2O (120 sccm) and SiH_4 (75 sccm). The radio-frequency power and chamber pressure of the PECVD system were 50 W and 67 Pa, respectively. Afterward, the formation of Mo silicide NDs was employed by an RTA process. The RTA process was performed at 900°C for 60 s in N_2 ambient at an atmospheric pressure. Finally, an Al gate electrode patterned by a shadow mask was evaporated by a thermal coater to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. A rapid thermal annealing (RTA) system was used to nucleate the Mo silicide NDs. The electrical measurement, including capacitance–voltage (*C*-*V*), was executed to define the memory effect and leakage current properties. In addition, the microstructure analyses and the chemical condition were performed by transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS), respectively.

3.1.3 Result and discussion

Figure 3-2 shows the *C-V* hysteresis of the MOIOS structure. The *C-V* was performed by bidirectional voltage sweeping. The voltage sweeping conditions were separated into two sets: (*i*) sweeping from 6 to −6 V and the reverse, and (*ii*) from 9 to −9 V and the reverse. The memory windows for the MOIOS structure were 1.5 and 5.1 V under the operation conditions (*i*) and (*ii*), respectiv]ely. The Mo silicide NCs of the MOIOS structure captured the injected carriers from the channel, leading to a flatband voltage shift of the memory device. In addition, the hysteresis was counterclockwise. The counterclockwise hysteresis *C-V* curve stems from the injection of electrons from the deep inversion layer and discharge of electrons from the deep accumulation layer of p-type Si substrate [3.11].

Figure 3-3 is the cross-section transmission electron microscopy (TEM) image for the stacked structure with the mixed Mo–Si layer after RTA treatment. The spherical NCs between the tunnel oxide layer and blocking oxide layer were observed clearly. The aerial density and mean size of the Mo silicide NCs estimated from the TEM analysis in Fig. 3 are 1.1×10^{12} cm^{-2} and 4–7 nm, respectively. The XPS analysis was also performed with monochromatic Al Kα (1486.71ev) X-ray radiation to estimate the chemical composition of the mixed Mo–Si films as shown in Fig. 3-4. The blocking oxide was removed by dilute HF acid before the XPS analyses. The charging energy effect of the XPS spectrum is calibrated with the binding energy shift of the C 1s peak which is due to the surface contamination. Comparing the Mo 3d spectra of the annealed film with that of the as-deposited film, the binding energy of the as-deposited film can be decomposed into a stronger peak at 228.2 eV and a weak peak at 228.0 eV as shown in Fig. 3-4 (a). In contrast, the Mo 3p spectral of the annealed sample exhibits one XPS peak at position of 228.0 eV as shown in Fig. 3-4

(b). The main peak in as-deposited film was shift from 228.2 ev to 228.0 ev. This binding energy shift corresponds closely to the previously reported values −0.2 eV [3-11, 3-12]. Moreover, Mo silicide is formed after thermal treatment at 900°C in N_2 ambient according to the previous literature [3.13]. Hence, we speculate that the Mo silicide NCs aggregated in the mixed Mo–Si layer driven by thermal energy during the annealing. In addition, the significant memory window of the MOIOS structure is contributed from the Mo silicide NCs. Fig. 3-5(a) and (b) show the XPS Si 2p spectral for the as-deposited and annealed Mo–Si film. In Fig. 3(a), there are two peaks at binding energy of 99.1 and 102.3 ev. The peak position of 99.1 ev and 102.3 ev are correspondence to Si–Si and Si–O bonds. The binding energy of Si–O bond is less than stoichiometry silicon dioxide (103.3 ev). Furthermore, we can note that the peak intensity of Si-Si bond is stronger than Si–O bond. However, after the annealing, the Si-Si peak shifts to 99.4 ev as shown in Fig 2(b). This shift can be attributed to Si-Mo bond due to formation of Mo silicide after annealing. Moreover, the Si–O bond shift from 102.3 ev to 102.6 and the peak intensity is stronger than Mo–Si bond. The results indicate that more silicon was oxidized leading to the stronger Si–O intensity. This oxidation may be due to the oxygen radical bombardment on the surface of Mo–Si layer generated from PECVD process. However, the binding energy of 102.6 ev is still smaller than that of stoichiometry silicon dioxide indicating that the formed surrounding oxide is poor and deficiency with oxygen.

In order to investigate the retention properties, the MOIOS structure was programmed by stress voltage of 10 V on the aluminum gate electrode for 10 sec. After programming, the flatband voltage departs from the original value as shown in Fig. 3-6 because of the charge storage in the nanocrystals. The flatband voltage shift is difference in flatband voltages between programming state and qusi-neutral state. The change in flatband voltage shift over time was used to observe the retention

behavior of the memory structure. It can be found that the flatband voltage shift is 2.5 V at the beginning of measurement time. The stored charges inside the nanocrystals can built repulsive electrical field and raise Fermi energy of the nanocrystals, which increases the tunnel probability (tunneling from nanocrystals to substrate) of the stored charges. The stored charges will therefore tunnel out from the nanocrystals and the flat-band voltage shift decreases as the time past. After 10^2 sec retention time, the flatband shift back to original value (the value before programming). This retention time seem to be too short for nanocrystal memory with a 5-nm tunneling oxide. According to XPS results, the poor quality of surrounding oxide may be the reason for this short retention time. When the charges stored in the nanocrystals, if the isolation between nanocrystals cannot prevent the stored charges from lateral migration, the stored charges will leak out of nanocrystals by one defect chain in tunnel oxide as the situation in electrically continuous poly-Si floating gate. To improve the retention of Mo silicide nanocrystal, we will proceed to improvement of surrounding oxide quality.

3.1.4 Conclusion

This section we investigated the formation of Mo silicide nanocrystal by annealing a mixed Mo–Si layer which was deposited by a dual E-gun evaporation system. The TEM results indicated the formation of nanocrystals in the annealed Mo–Si layer, and XPS results indicated the main phase of the nanocrystal is the Mo silicide and the surrounding oxide is deficiency. Furthermore, we investigated the memory characteristics of the Mo silicide nanocrystal. The memory windows are 1.5 and 5.1 V under the bidirectional sweeping voltage of 6 and 9 V, respectively. The significant memory window resulted from the formation of Mo silicide NCs using the RTA system. The Mo silicide NC memory device with low operation voltage is

suitable for the demand for the current NVM. However, for the retention, it is required to improve the surrounding oxide.

3.2 Influence of post-annealing ambient on the memory characteristics of molybdenum-based nanocrystal memory

3.2.1 Introduction

In the previous section, the main issue for the Mo silicide nanocrystal is the retention, and the XPS results provide a clue. It can be observed that that even the nanocrystals is formed if the surrounding oxide is not good enough to prevent the carriers from lateral migration, the stored charges can still leak out of nanocrystals immediately. In the section 3.1, the XPS results indicate the surrounding oxide is deficiency of enough oxygen bonds. Therefore, we try to oxidize unsaturated Si—O bonds of the surrounding oxide by introducing oxygen during annealing process. We found that the annealing in oxygen ambience can influence the charge storage ability of the nanocrystal memory. Furthermore, we found that capping oxide before the annealing process is important process for fabrication of Molybdenum nanocrystal.

3.2.2 Experiment

Figure 3-7 exhibits the device structure and process flow in this work. A 6 in. p-type silicon wafer with (100) orientation was cleaned by a standard RCA cleaning process, followed by a dry oxidation process at 1000°C in an atmospheric pressure chemical vapor deposition furnace to form a 5 nm thick tunnel oxide. Subsequently, a 10 nm thick mixed Mo–Si layer was deposited onto the tunnel oxide by dual electron-gun (E-gun) evaporation. Afterward, two samples were annealed in oxygen ambience at 900°C before and after deposition of blocking oxide. The blocking oxide was deposited with 30-nm-thick used to prevent the carriers of the gate electrode from injecting into the charge trapping layer by Fowler–Nordheim tunneling. The blocking

oxide was deposited by a plasma-enhanced chemical vapor deposition (PECVD) system at 300°C with precursor gases N_2O (120 sccm) and SiH_4 (75 sccm). The radio-frequency power and chamber pressure of the PECVD system were 50 W and 67 Pa, respectively. Afterward, the formation of NCs was employed by an RTA process. Finally, an Al gate electrode patterned by a shadow mask was evaporated by a thermal coater to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. A rapid thermal annealing (RTA) system was used to nucleate the Mo silicide NCs. The main difference with the study in the previous section is that the annealing ambience is oxygen instead of nitrogen. The electrical measurement, including capacitance–voltage (*C*-*V*), was executed to define the memory effect and leakage current properties. In addition, the microstructure analyses and the chemical condition were performed by transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS) Secondary ion mass spectra (SIMS) , respectively.

3.2.3 Results and discussion

Fig. 3-8 is the comparison of SIMS for the samples before annealing, and annealing with and without pre-capping blocking oxide. The pre-capping oxide means deposition of blocking oxide before annealing process. In the Fig., the intensity of Mo signal for the annealed sample is lower than that for the sample without annealing. Furthermore, the intensity of Mo signal for the sample annealing with pre-capping oxide is stronger than that for the sample without pre-capping oxide. The result indicated that the Mo concentration decreased after annealing in O_2 ambience and the capping oxide process before annealing can restrain the Mo concentration from diminishing. It has been proposed that Mo oxide is volatility at temperature larger than 750°C [3.14]. The reduction of Mo concentration can be attributed to the evaporation of Mo oxide. During the oxidation process without pre-capping oxide

layer, there is no diffusion barrier for oxygen and the oxygen can directly in contact with Mo-Si layer. The oxidation and evaporation rate for the sample without the pre-capping oxide sample should be higher than that for the sample with pre-capping oxide layer. If there is a pre-capping oxide layer before annealing process in oxygen ambience, the oxygen need to diffuse through the pre-capping oxide layer to contact the surface of the Mo-Si layer before the oxidation occurs. This implies a slower oxidation rate for the pre-capping oxide sample compared with the sample without pre-capping oxide. Furthermore, the pre-capping oxide layer can suppress the evaporation of the formed Mo oxide, resulting in a larger amount of Mo concentration remained in the structure when comparing with the sample without the pre-capping oxide layer.

Fig. 3-9(a) and (b) show the C-V curve of the samples without and with pre-capping oxide layer, respectively. For both samples, the C-V hysteresis curve is counterclockwise due to substrate injection. Obviously, the memory window of the sample without pre-capping oxide layer is smaller than that with pre-capping oxide which indicated that the less charges can be stored in sample without pre-capping oxide. The difference in memory window between two samples can be attributed to the reduction of Mo concentration.

Comparing the C-V curve of the oxygen-annealed sample with N_2-annealed sample in Fig. 3-2, the memory window of the O_2-annealed sample is smaller than that of N_2-annealed sample, which indicated that less charges can be stored in the nanocrystals for O_2-annealed sample. Fig. 3-10 is the XPS analyses for the sample after annealing with pre-capping oxide layer. In Fig 3-10(a), the Mo 3d spectra show a broad hump. The hump can be decomposed into the several peaks which are originated from the metallic Mo, MoO_3 and Mo sub-oxide. Note that the area of signal for Mo oxide is larger than that for metallic Mo. The area ratio percentage between

two signals is about 69:31. This result implies that most of Mo was oxidized during the oxygen-annealing process. Fig 3-10(b) is the Si 2p spectra for the Mo-Si layer. It can be found that the peak position in the spectra is about 103.3 ev. The position is corresponding to the stoichiometry silicon oxide (SiO_2). Obviously, the introduction of oxygen ambience during annealing process can oxidize the unsaturation bonds in Mo-Si layer.

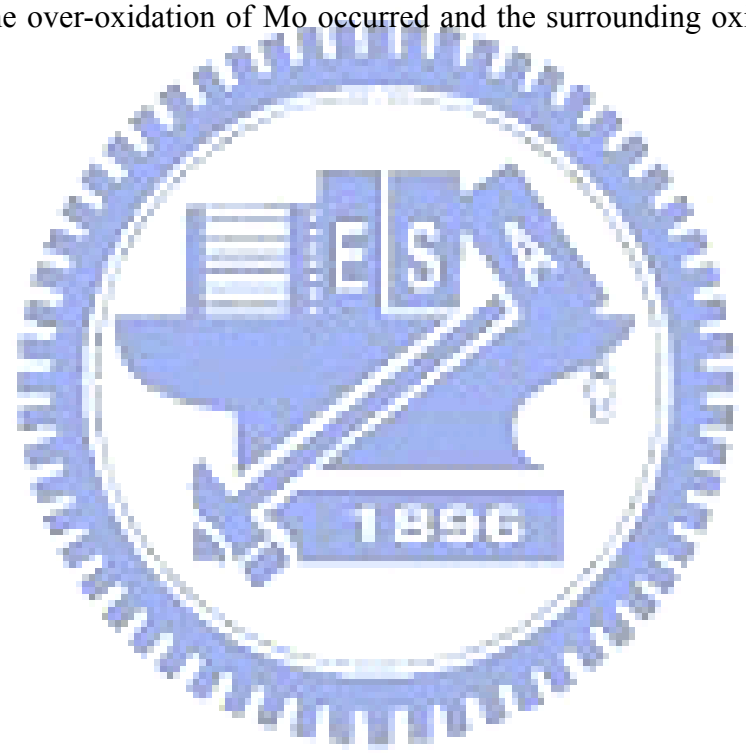
According to the XPS results, the difference in memory window between two samples can be attributed to the over-oxidation of the metallic Mo. We speculate that the smaller memory window for N_2-annealed sample was due to the formation of Mo oxide that is a semiconductor-like metal oxide with a band gap of 3.2ev. Therefore, Mo oxide has lower density of state for the charge storage and smaller coupling with substrate when compared with metallic Mo resulting in the smaller memory window.

To investigate the difference in nanostructures of the Mo-Si layer annealed in nitrogen and oxygen ambience, TEM analyses for both samples are shown in Fig. 3-11. We note that after annealing in oxygen ambience, the size of nanocrystal is about 20-nm which is larger than the 7-nm for the sample annealed in N_2 ambience. Furthermore, the tunnel oxide for the oxygen-annealed sample seems to be encroached by nanocrystals. According to XPS, it is possible that nanocrystal size increase is due to formation of Mo oxide.

Fig. 3-12 is the comparison of retention behavior between O_2-annealed sample and N_2-annealed sample. After external bias was applied on gate electrode with amplitude of 10 V for 5 sec, the retention behavior was monitored by flatband voltage shift. It can be found that the O_2-annealed sample has a slower flatband voltage shift than N_2-annealed sample. This result indicates that the O_2-annealed sample has a better retention than N_2-annealed sample, which can be attributed to the improvement of surrounding oxide quality.

3.2.4 Conclusion

In this section, we investigated the influence of difference annealing ambience on formation of Mo silicide nanocrystal and its memory characteristics. We found that a pre-capping oxide layer before the oxidation process is very important. This pre-capping oxide layer can reduce oxidation rate of Mo silicide layer and preventing the Mo oxide from being evaporation. Furthermore, the pre-capping oxide layer can enhance the memory window of the memory device. From the XPS analyses, we found that the over-oxidation of Mo occurred and the surrounding oxide quality was improved.



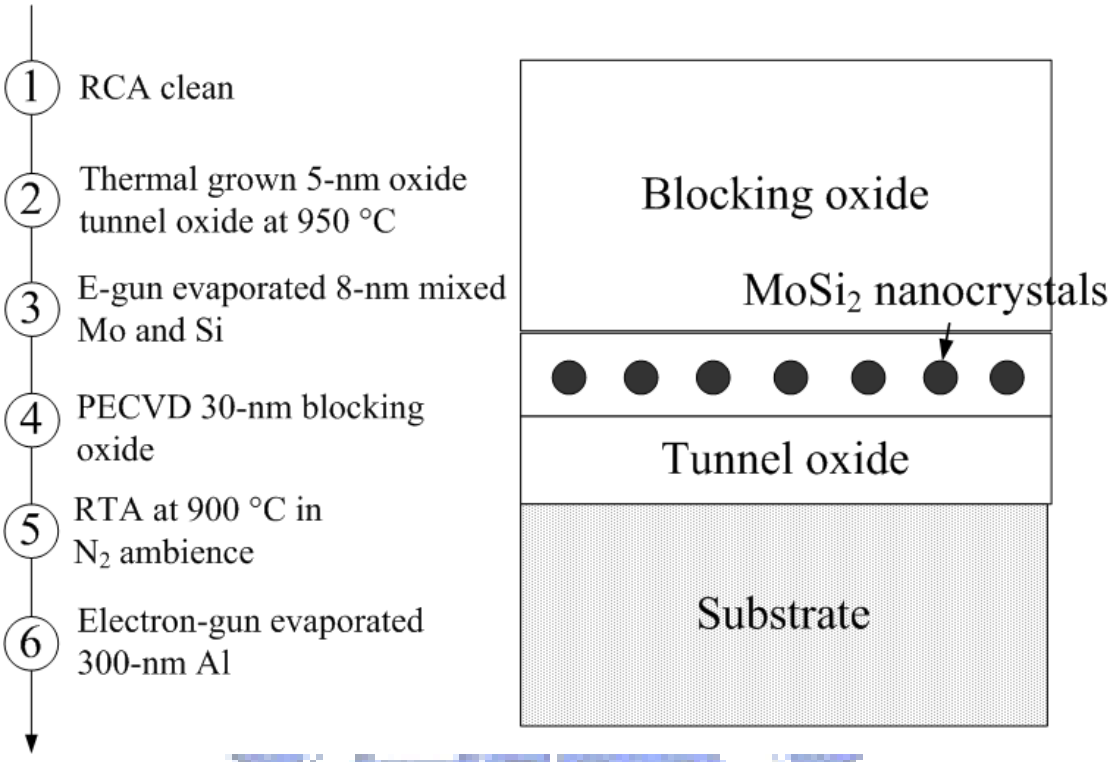


Figure 3-1 Process of flow and device structure of this study. The annealing process at step 5 is in nitrogen ambience.

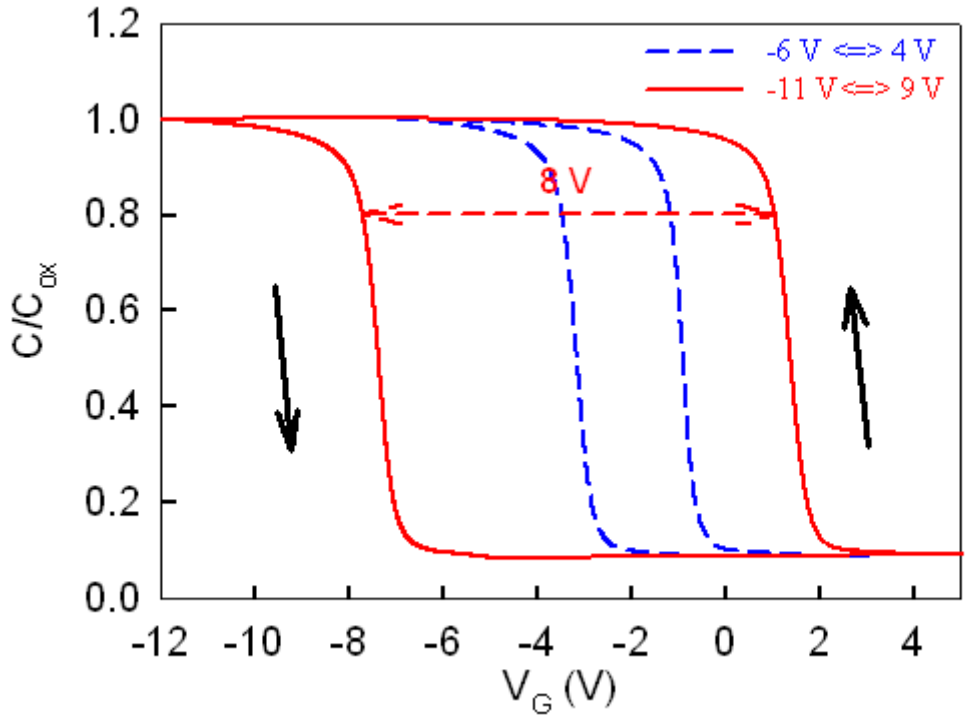


Figure 3-2 The capacitance-voltage (C-V) hysteresis of the MOIOS structure. A counterclockwise memory window is about 5.1 V at the sweeping voltage of 9 V.

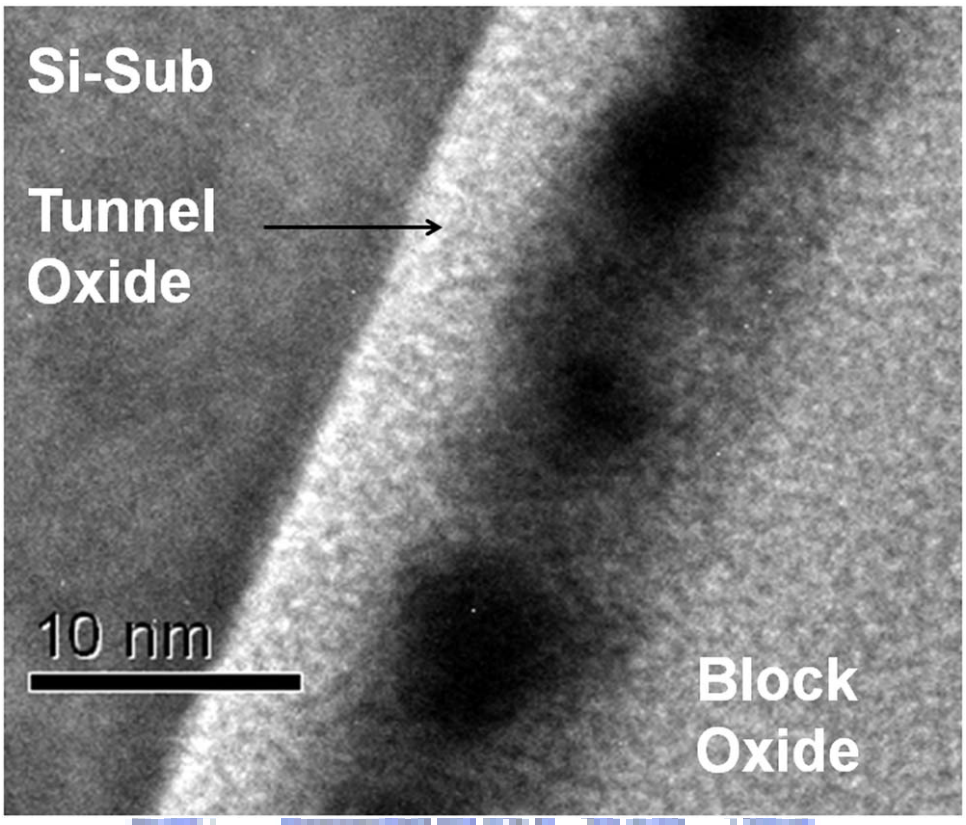


Figure 3-3 The transmission electron microscopy (TEM) analysis of Mo silicide nanodots layer.

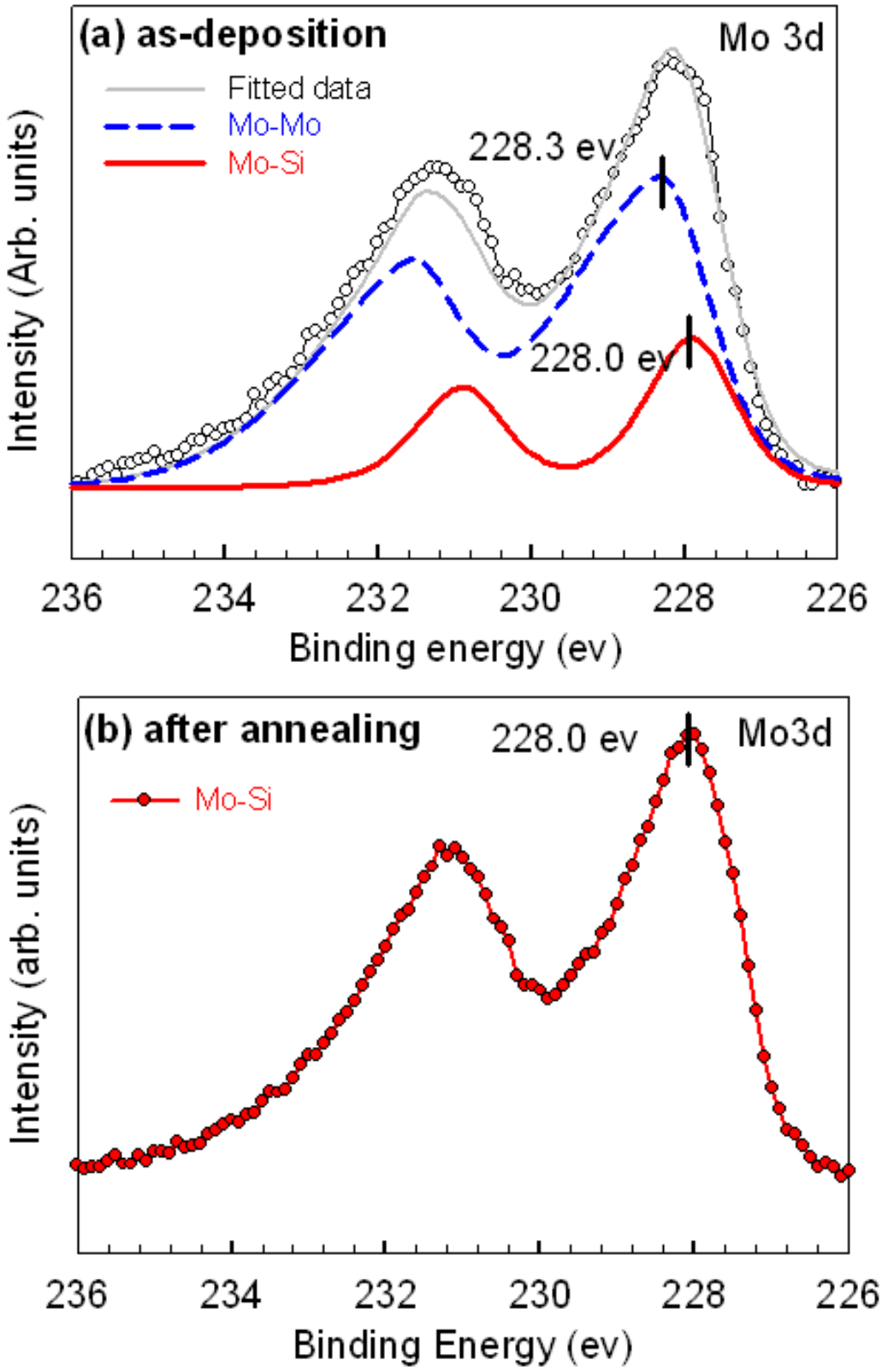


Figure 3-4 XPS of Mo 3d spectrum of the Mo silicide layer with and without annealing.

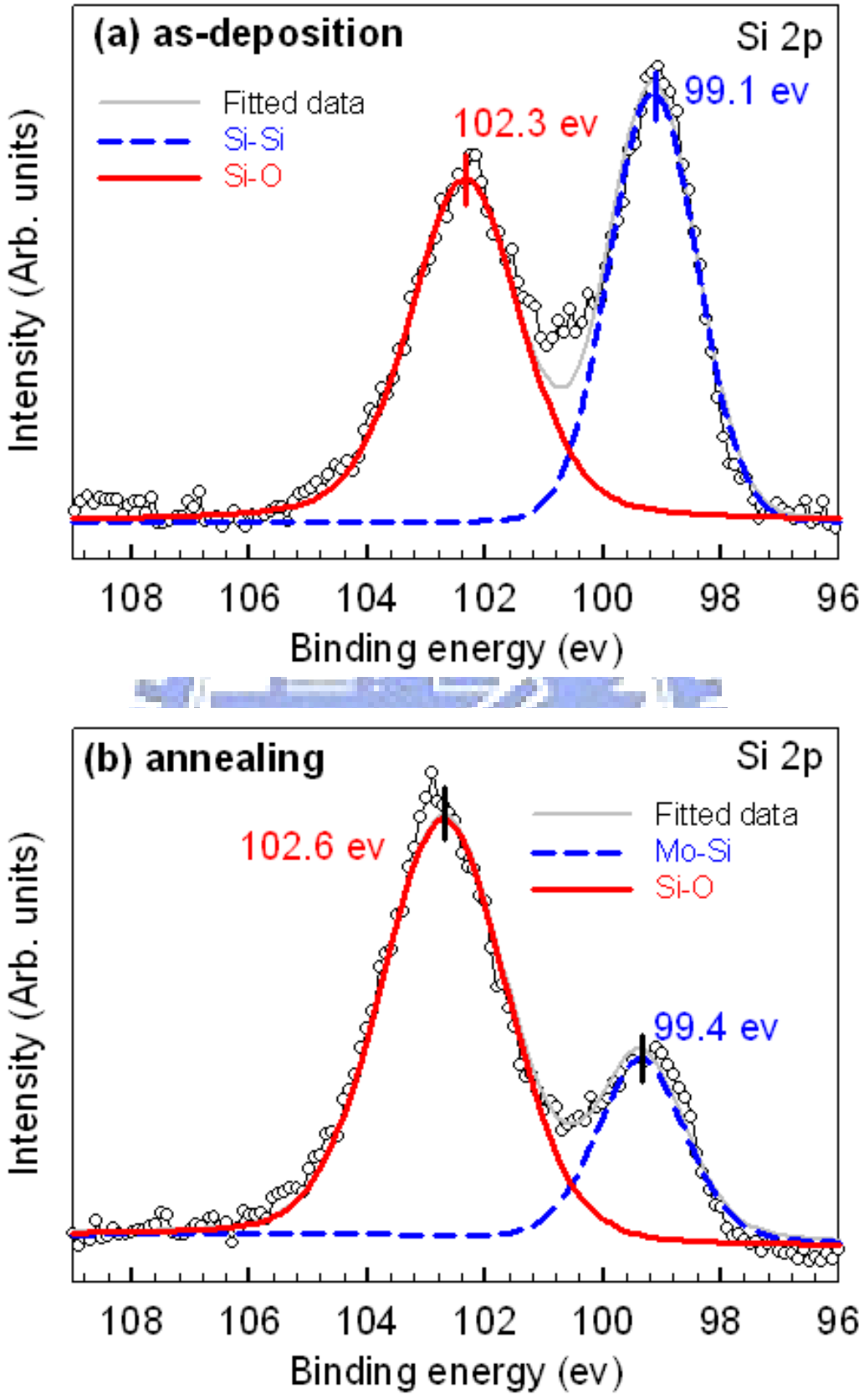


Figure 3-5 XPS of Si 2p spectrum of the Mo silicide layer with and without annealing.

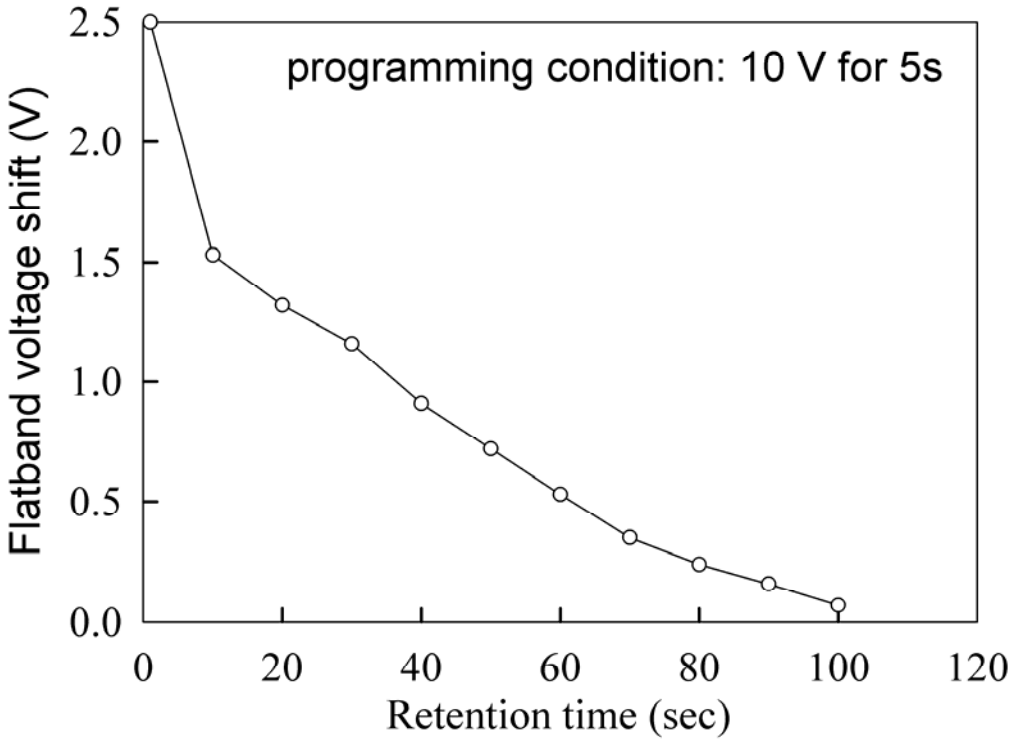


Figure 3-6 Retention behavior of Mo silicide nanocrystal.

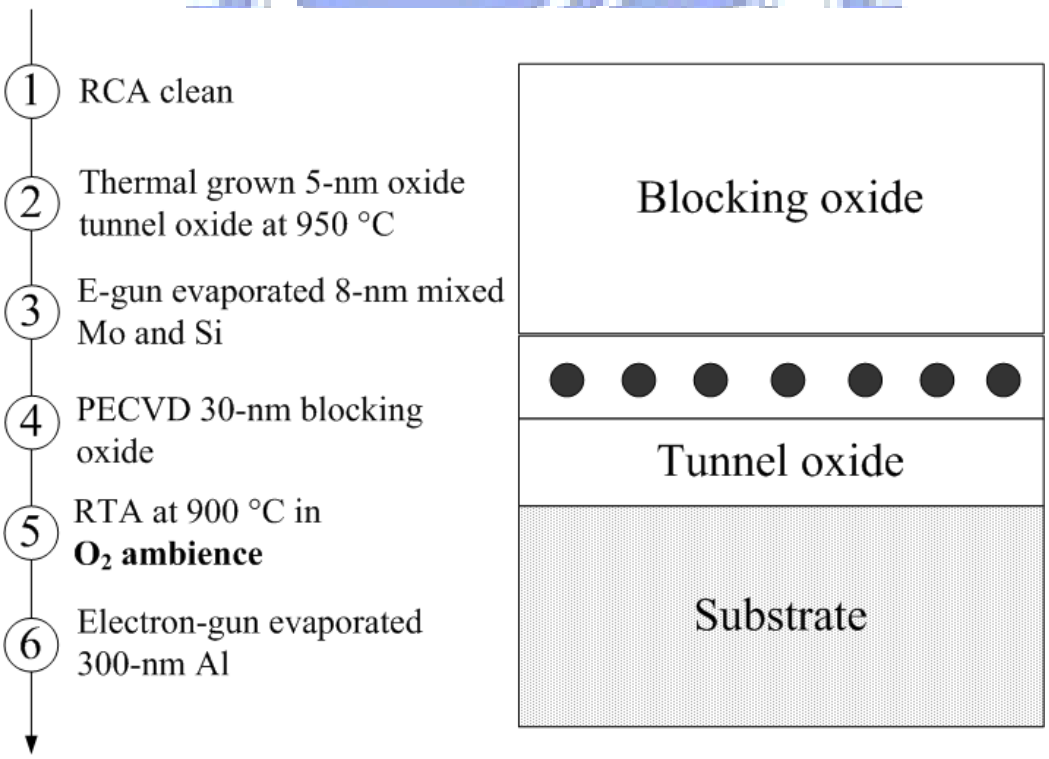


Figure 3-7 Process flow and device structure of this study. The annealing was performed in oxygen ambience.

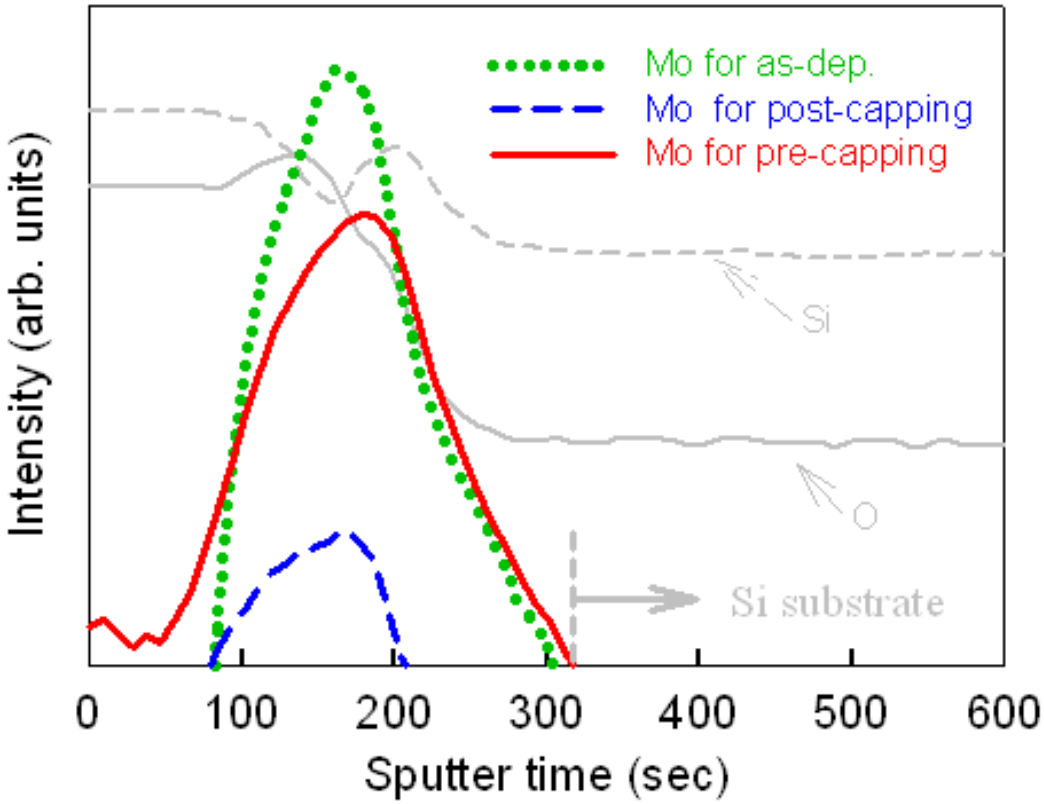


Figure 3-8 Secondary ion mass spectra (SIMS) of the oxide/Mo silicide/oxide/substrate structure.

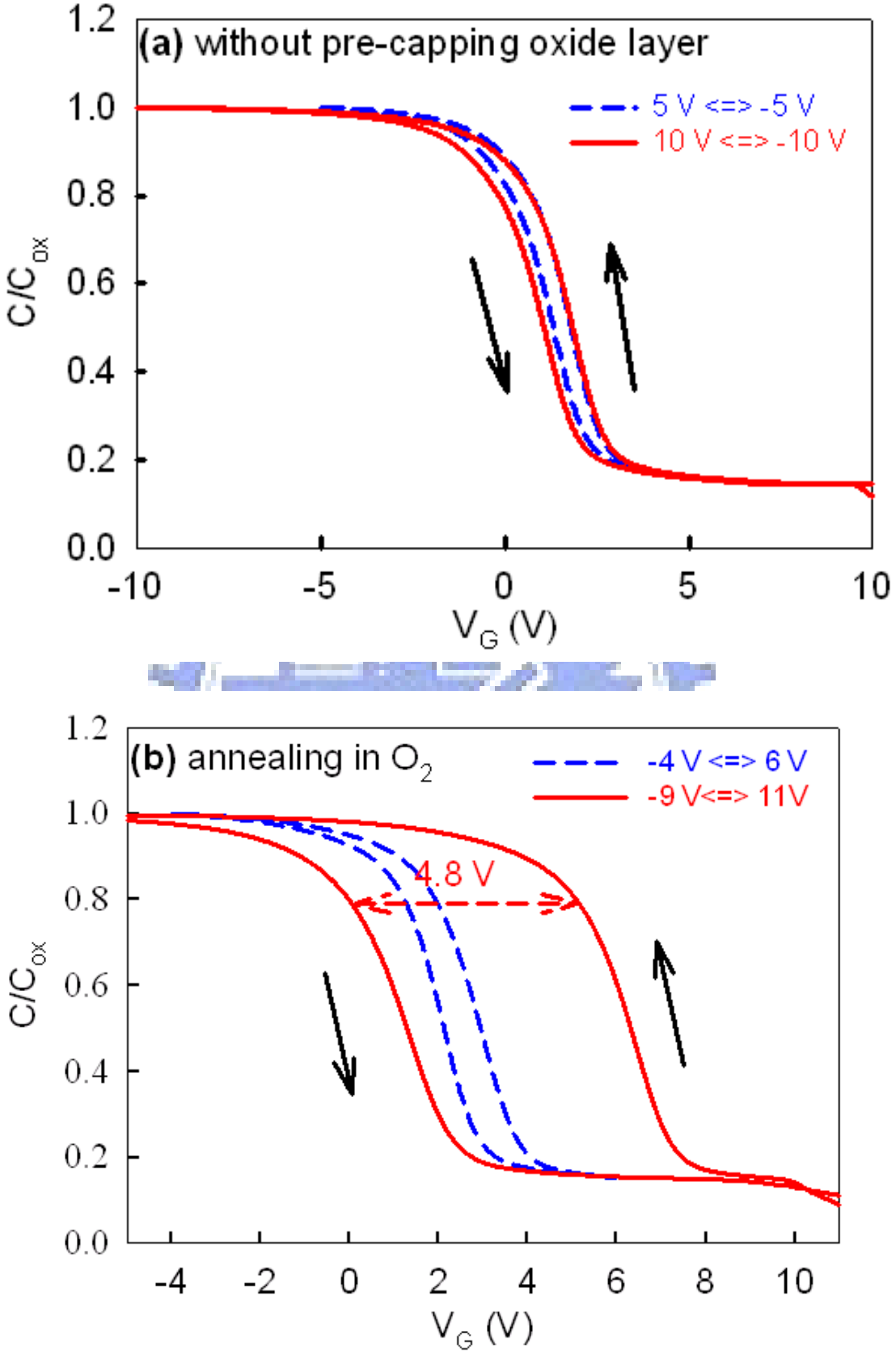


Figure 3-9 The C-V curve of the sample (a) without and (b) with pre-capping oxide layer.

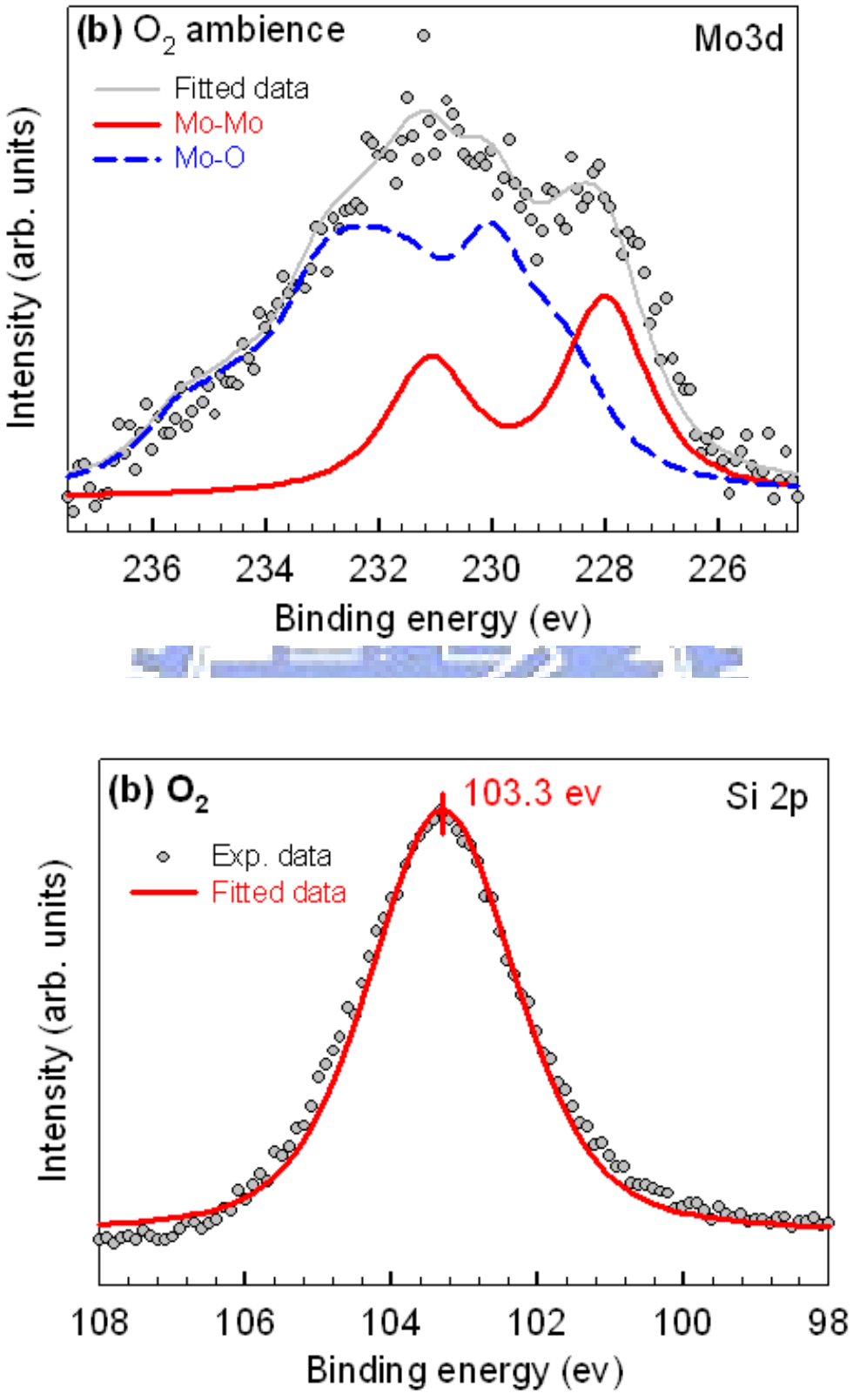


Figure 3-10 XPS Mo 3d and Si 2p spectra for the Mo silicide layer after annealing in oxygen ambience.

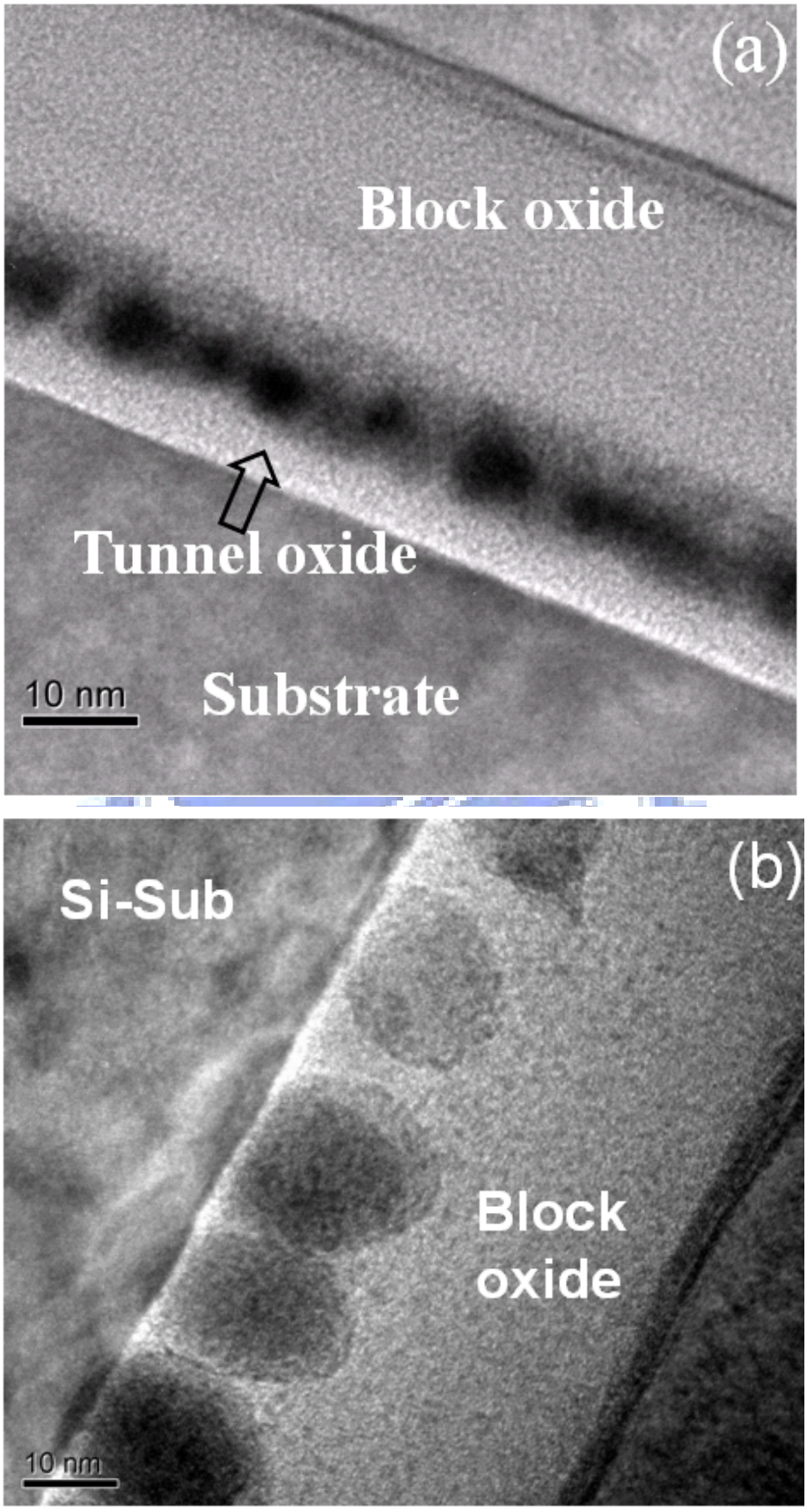


Figure 3-11 TEM results of Mo silicide annealing in (a) nitrogen ambience and (b) oxygen ambience.

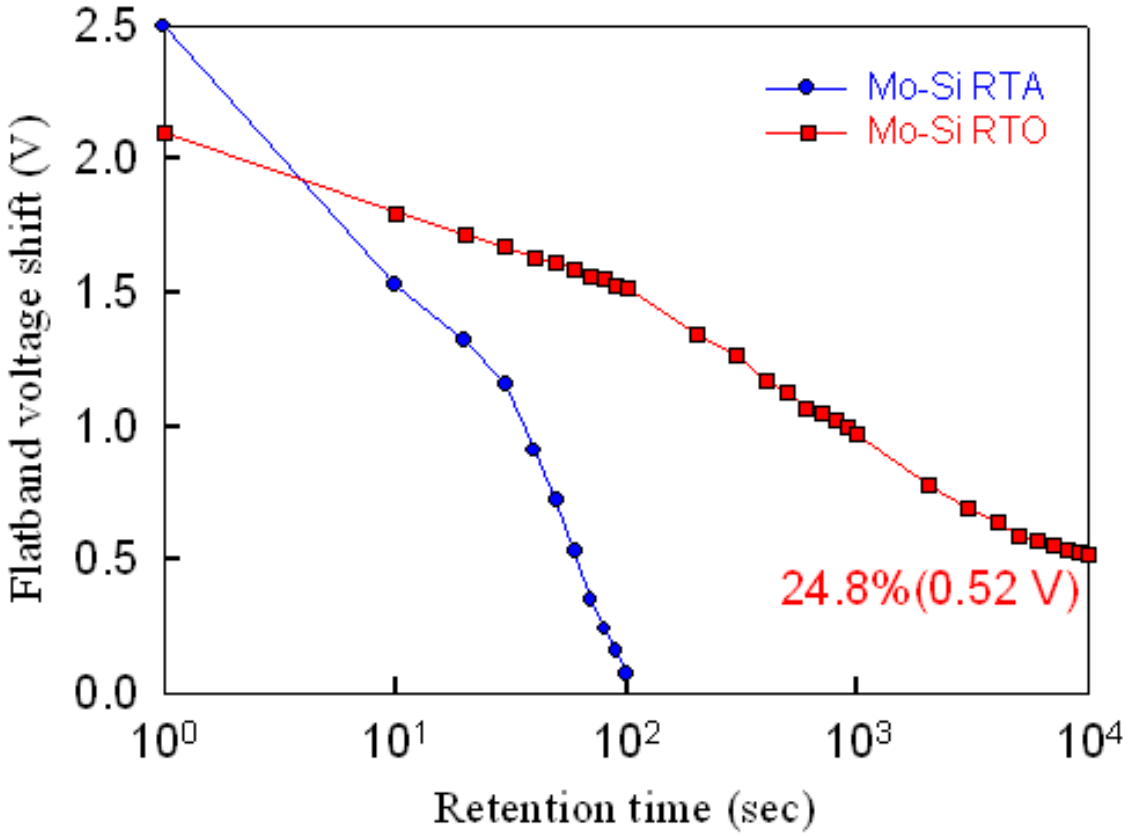


Figure 3-12 Retention behavior of Mo silicide annealing in nitrogen and oxygen ambience.

Chapter 4

Memory characteristics of Mo nanocrystal embedded in silicon oxide and silicon nitride

4.1 Formation and memory characteristics of Mo nanocrystal embedded in silicon oxide

4.1.1 Introduction

In recently years, discrete nanocrystals composed floating gate nonvolatile memory structure has been widely investigated as a candidate for next generation nonvolatile memory because charges stored in lateral isolated nanocrystals instead of continuous conducting polycrystalline silicon layer are more immunity to the local defect chain in the tunnel oxide [4.1-4.4]. Many materials, such as Si, Ge, Ni, and Co have been proposed to fabricate nanocrystal memory [4.2-4.6]. Because of benefits on strong coupling, deep quantum well and large density of state, metal nanocrystals have recently received much attention for research [4.5-4.7]. However, the use of metal must take thermal stability issue into account because the metal diffusion into or chemical reaction with tunnel oxide during the memory fabrication process will compromise performance of the memory structure [4.6]. Mo is an attractive candidate because of its high work function, compatible with complementary metal-oxide-semiconductor (CMOS) process and high thermal stability [4.8].

In this section, nonvolatile memory characteristics of Mo nanocrystals embedded in SiO_x were investigated by thermal annealing oxygen incorporated Mo silicide layer. Our experiment results show that the Mo oxide was formed in the as-deposited layer,

and nanocrystal can be formed after annealing at a critical temperature. Lee et al. proposed that the formation of metal oxide during nanocrystals fabrication process reduces charge storage ability [4.9]. To reduce the metal oxide, they need to perform a long-term thermal treatment in hydrogen ambience. In our investigation, we found that the Mo oxide was reduced after a critical annealing temperature, and this result improved the charge storage ability of Mo nanocrystal memory cell.

4.1.2 Experiment

Fig. 4-1 is the process flow and memory structure in this experiment. The memory structure was fabricated on a 6 inch *p*-type Si substrate. A 5-nm-thick dry oxide (tunnel oxide) was thermally grown at 950 °C on the substrate in a horizontal furnace after the substrate was cleaned by Radio Corporation of America (RCA) process. An 8-nm-thick oxygen incorporated Mo silicide layer was deposited on the tunnel oxide by co-sputtering Mo and Si targets in Ar (24 sccm)/O_2 (2 sccm) ambience. Subsequently, a 30-nm-thick silicon dioxide (blocking oxide) was deposited on the layer by plasma enhanced chemical vapor deposition at 300°C. Thermal annealing process at 700, 800 and 900°C was performed in N_2 60s to investigate the temperatures influence on the memory characteristics of oxygen incorporated silicide layer. Finally, a 500-nm-thick Al gate patterned with shadow mask was evaporated by thermal coater to form the memory structures. Secondary ion mass spectrometry (SIMS) was employed to analysis the element distribution in the sample. Transmission electron microscope (TEM) and x-ray photoelectron spectroscopy (XPS) were used to analysis the microstructure and chemical composition of nanocrystals and their surrounding oxide. Electrical characteristics of the capacitance-voltage *C-V* hysteresis were measured by HP4284 Precision *LCR* Meter with frequency of 1 MHz.

4.1.3 Result and discussion

Fig. 4-2 is the secondary ion mass spectrometry (SIMS) depth profile of the blocking oxide/O-Mo-Si/tunnel oxide/Si-substrate structure. The O_2^+ was adopted as primary incident ion. The structure was sputtering with O_2^+ from the surface to the substrate. It can be found that the Mo element profile for as-deposited sample is similar to that for 900°C-annealed sample, which indicate that there is no obvious Mo diffusion into the tunnel after annealing. This result is important because the diffusion of metal element into tunnel oxide can degrade the reliability of the memory including retention and endurance characteristics.

To investigate the change of chemical composition of oxygen incorporated Mo silicide thin film after annealing at various temperatures, the XPS analyses were performed by using an Al Kα (1486.6 eV) X-ray. Figure 4-3 shows the XPS Mo 3d core level spectra for as-deposited sample and 700, 800 and 900°C annealed samples. It can be found that Mo oxide formed in the as-deposited thin film, and the intensity of Mo oxide decreased as annealing temperature increased. After 900°C annealing, there is only metallic Mo in the thin film, as shown in Fig. 4-3(d). Fig. 4-4 shows the XPS O 1s core level spectra for as-deposited sample and 700, 800 and 900°C annealed samples. It can be found in the Fig. 4-4(a) that the peak position of Si-O bond is at 532.4 ev for the as-deposited sample. The binding energy of as-deposited thin film is smaller than that of stoichiometry silicon oxide (533.4 ev), which indicate that the oxide formed in as-deposited sample is deficiency. As the annealing temperature increased, the binding energy shifted toward higher binding energy. According to literature, the increment of O 1s binding energy is attributed to the oxygen bonding with deficient silicon oxide [4.9]. From XPS Mo 3d and O 1s results,

we considered that a redox between MoOx and SiO_x occurred during the thermal annealing process. For the redox behavior in the oxygen incorporated Mo silicide layer, the formation energy of Si oxide (−750 kJ/mole) is larger than that of Mo oxide (−450 kJ/mole). Therefore, the oxygen of Mo oxides prefers to bond with Si than Mo during the thermal annealing at 900 °C, which results in the reduction in Mo oxide and improves the quality of SiOx.

Figure 4-5 shows the cross-section TEM image of 700 and 800 °C annealed samples to observe the microstructure transformation. It can be found in the figure 4-5(a) that the oxygen incorporated Mo silicide thin film after 700 °C annealing was continuous. However, after annealing at 800 °C [Fig. 4-5(b)], spherical nanocrystals were formed in the thin film. This result indicate that the temperature as high as 800 °C is required to form the Mo nanocrystal.

Figure 4-6 shows C-V curve of the 700°C-annealed sample. The curve was obtained after the gate voltage swept from inversion to accumulation region of the substrate and the reverse. In Fig., the memory window (width of the loop) of 700 °C annealed sample is approximation to 0 V. The results indicate that the injected charges cannot be stored in 700°C-annealed sample. For the C-V result of 700 °C annealed sample, the floating-gate-like charge storage layer was considered. As indicated in the cross-section TEM result for 700°C-annealed sample [Fig. 4-5(a)], the oxygen incorporated Mo silicide film is continuous. Therefore, the injected charges can lateral migrate and leak out of the thin film through one defect chain in the tunnel oxide.

Figure 4-7(a) and (b) show the C-V curves of 800 and 900 °C annealed samples. It can be found in Fig. that there are obvious hysteresis loop at the sweeping voltage of -11 to 9 and the reverse, which indicates that the injected charges can be stored in the annealed thin film because the formation of discrete Mo nanocrystals as charge

storage centers can preventing the all stored charges from leaking out of the nanocrystals through one defect chain. The loop is counterclockwise due to substrate injection through the tunnel oxide. We note that the memory window of 900 °C annealed sample is twice larger than that of 800 °C one. For difference in the memory windows between 800 and 900 °C annealed samples, the density, size and composition of nanocrystal was considered. Fig. 4-8 shows the plan-view TEM of the 800 and 900 °C annealed samples. It can be found in the Fig. 4-8(a) and (b) that the average size is about 4-nm, and the density of nanocrystal is about 10^{12} cm^{-2} for both samples. From the plan-view TEM results, the density and size of 900 °C annealed sample is close to that of 800 °C one. Therefore, we exclude the possibility of the size and density effect on the significant difference of memory window in the both samples. According to XPS results, we speculate that the larger memory window for 900 °C annealed sample was due to the reduction in Mo oxide that was proposed as a semiconductor like metal oxide. Therefore, the Mo oxide has lower density of state than metallic Mo for charge storage.

Figure 4-9 shows the retention behavior of 800 and 900 °C samples. The retention was measured by stress voltage of 10 V on gate electrode for 5s. The memory window is obtained by comparing the C-V curves of a charged state to a quasineutral state. It can be found that the memory window of 800 °C annealed sample decreased significant and remained ~11% after 10^4 sec. In contrast, the retention of 900 °C annealed sample remained ~74%. From the XPS results (Fig. 4-3), the different retention behavior was considered to the quality of the surrounding oxide. When charges are storage in the nanocrystals, the stored charges can escape laterally

through the traps in the surrounding oxide. If the tunnel oxide has a leakage path, the lateral escaped charges will leak into the substrate. Because the surrounding oxide quality of 900 °C annealed sample was improved by the redox reaction between Mo oxide and SiO_x, the more charges can be remained in the Mo nanocrystals.

4.1.4 Conclusion

Mo nanocrystal was fabricated for nonvolatile memory application through thermal annealing oxygen incorporated Mo silicide thin film. Nanocrystal can form after annealing temperature larger than 800°C. The XPS results indicate the existence of Mo oxide and SiO_x in as-deposited oxygen-incorporated Mo silicide layer. As the annealing temperature increased, the amount of Mo oxide decreased. After the 900°C annealing, the Mo oxide was reduced. The average size and density of Mo nanocrystals were estimated to be about 4 nm and 10^{12} cm^{-2} for the 800 and 900°C annealed samples. The memory window of 900°C (3.6 V) is larger than that of 800°C one (1.3 V) due to reduction of Mo oxide in the thin film. The high density of 10^{12} cm^{-2} and large memory window of oxygen incorporated Mo silicide thin film after annealing at 900 °C can be application on nanocrystal nonvolatile memory.

4.2Formation and memory characteristics of Mo nanocrystal embedded in silicon nitride

4.2.1 Introduction

Recently, metal nanocrystal memories attracted much attention as a promising candidate for next generation nonvolatile memory (NVM). Comparing with

semiconductor nanocrystal, metal nanocrystal has some advantages, such as higher density of states around the Fermi level and a wide range of available work functions. However, when integrating the nanocrystal into the memory device structure, there are still some challenges for scaling. One of the main critical issue that limits the scaling is the variation of the electrical characteristics between cells because the smaller size of device is, the lower numbers of nanocrystals are. Therefore, the formation of high density nanocrystal which can alleviate the electrical fluctuation between memory cells is important.

In this study, we investigate the formation of Mo nanocrystal by annealing the nitrogen incorporated Mo and Si layer for nonvolatile memory application. Molybdenum is widely application in VLSI technology due to its high thermal stability. Furthermore, the Mo nanocrystal can be as smaller than 2-nm without suffering from serious quantum confinement effect as shown in Fig. 4-10 [4-16]. In our experimental results, we found that introducing the nitrogen during the nanocrystal fabrication process can influence the density of Mo nanocrystal. Furthermore, we study the memory characteristics of Mo nanocrystal embedded in silicon oxide (Mo in SiO_x) and nitride layer (Mo-NC in SiN_x) and explain the difference in reliability between Mo-NC in SiO_x and Mo-NC in SiN_x through device simulation.

4.2.2 Experiment

The memory structure was fabricated on a 6 inch *p*-type Si substrate. A 5-nm-thick dry oxide (tunnel oxide) was thermally grown at 950 °C on the substrate in a horizontal furnace after the substrate was cleaned by Radio Corporation of America (RCA) process. An 8-nm-thick oxygen or nitrogen incorporated Mo silicide layer was deposited on the tunnel oxide by co-sputtering Mo and Si targets in Ar/O_2

or in Ar/N_2 mixed ambience. Subsequently, a 30-nm-thick silicon dioxide (blocking oxide) was deposited on the layer by plasma enhanced chemical vapor deposition at 300°C. Thermal annealing process at 900°C was performed in N_2 60s to form Mo nanocrystal. Finally, a 500-nm-thick Al gate patterned with shadow mask was evaporated by thermal coater to form the memory structures. Transmission electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) were used to analysis the microstructure and chemical composition of nanocrystals and their surrounding oxide. Electrical characteristics of the capacitance-voltage *C-V* hysteresis were measured by HP4284 Precision *LCR* Meter with frequency of 1 MHz.

4.2.3 Results and discussion

Figure 4-11(a) and (b) are Si 2p and N 1s XPS spectra, respectively. As shown in Fig. 4-11(a), the peak of Si 2p spectrum is smaller than the binding energy (102.3 ev) of stichiometry silicon nitride (Si_3N_4). Furthermore, there are two peaks at 394.0 ev and 398.0 ev, which are corresponding to the Mo-Mo and Si-N bonds, respectively. The XPS result indicates that the formed Mo nanocrystal is embedded in SiN_x where x is smaller than 1.33.

Figure 4-12(a) and (b) are the plane-view TEM analysis for 900°C-annealed oxygen- and nitrogen-incorporated Mo silicide layer after 900°C annealing. From the TEM analysis, the average size and density of formed Mo nanocrystal in oxygen-incorporated layer is about 4~5nm and 1×10^{12} cm^{-2}, respectively. In contrast, the size of Mo nanocrystal in nitrogen-incorporated layer is about 2-3nm, and the density is as high as 6×10^{12} cm^{-2}. The high density, which can prevent variation between cells, is benefit on scaling down the memory structure. The higher density of Mo nanocrystal in SiN_x can be attributed to the larger number of dangling bonds in the SiN_x according to XPS results. The dangling bonds can act as a nucleation site for

agglomeration of nanaocrystals.

Figure 4-13(a) and (b) are the C-V curves of Mo nanocrystal in SiO_x and SiN_x, respectively. The hysteresis for both samples is counterclockwise due to carrier injection and ejection from substrate and nanocrystals. For the Mo in SiO_x, the memory is 3.6 V under sweeping voltage of -11 to 9 V and vice verse. However, the memory window for the Mo in SiN_x under the same sweeping condition is 9.5 V. Figure 4-14 is a comparison of memory window shift between Mo in SiO_x and Mo in SiN_x. It can be seen that the memory window of Mo in SiN_x at various sweeping voltages is larger than that of Mo in SiO_x. This suggests that the Mo nanocrystal in SiN_x can store more number of carriers per unit cell than Mo nanocrystal in SiO_x due to its higher density of nanocrystal.

Fig. 4-15(a) and (b) are the retention of Mo nanocrystal in SiO_x and in SiN_x, respectively. It can be seen that the retention of Mo in SiO_x after 10^4 retention time has remaining charges of 74%. However, the ΔV_{FB} shift decreases significantly and arrive at 0 after 10^3 retention time. The poor retention behavior of Mo in SiN_x may result from the poor surrounding dielectric of Mo nanocrystal (SiN_x) according to XPS results.

4.2.4 Conclusion

We have investigated memory characteristics of Mo nanocrystal embedded in SiN_x. The density of Mo nanocrystal in SiN_x is as high as 6×10^{12} cm^{-2}. This high density can reduce the fluctuation of the memory characteristics while the nonvolatile memory device scaling down. The Mo nanocrystal in SiN_x, which has large memory window under low operation voltage, is suitable for next generation nonvolatile memory application.

4.3Enhancement of Charge Storage Ability of Double layer nanocrystal memory structure of Mo embedded in oxide

4.3.1 Introduction

Nonvolatile memory based on the floating gate structure plays an important role in portable electronic productions for its advantages of nonvolatility and low power consumption. However, scaling of the floating gate structure is limited by thin tunneling oxide in terms of reliability [4.17]. To address this, discrete nanocrystals as a charge storage layer have recently been investigated to replace the electrical continuous poly-Si layer in the floating gate structure [4.18-20]. Using discrete nanocrystals as charge-storage centers instead of a poly-Si layer can prevent the total stored charges from being lost through a leakage path in the tunnel oxide and therefore allows further scaling of the memory structure. Among nanocrystals, such as semiconductors, high-permittivity insulators and metal nanocrystals, the metal nanocrystals have received much attention than the others because the metal nanocrystals have the advantages of a higher density of states around the Fermi level, stronger coupling with the conduction channel, a wide range of available work functions, and smaller energy perturbation due to carrier confinement [4-19]. Ng et al. proposed a densely stacked silicon nanocrystal layers to keep the better retention time because the charges stored in the nanocrystals near the blocking oxide have low tunnel probability to leak into substrate. However, there are very few researches to investigate the formation and nonvolatile memory effect of multi-layer metal nanocrystals.

In this section, the formation and charge storage effect of nonvolatile multi-layer Mo nanocrystals memory were revealed. The nanocrystals were formed by annealing a stacked oxygen-incorporated Mo silicide thin film. The memory characteristics were

compared with single-layer nanocrystals including memory window and retention.

4.3.2 Experiment

The process flow and memory structure are shown in Fig. 4-16. The memory structures were fabricated on a 6 in. p-type Si substrate. A 5-nm-thick dry oxide (tunnel oxide) was grown at 950°C on the substrate in a horizontal furnace after a standard RCA cleaning process. An 8-nm-thick oxygen-incorporated Mo silicide (OMoSi) layer was deposited on the tunnel oxide by cosputtering Mo and Si targets in Ar (24 sccm)/O_2 (2 sccm) ambience. The 5-nm-thick middle oxide was deposited by a plasma-enhanced chemical vapor deposition system at 300°C with precursor gases N_2O (120 sccm) and SiH_4 (75 sccm). A thermal annealing process at 900°C was performed in N_2 for 60s. To form double layer of nanocrystal, 8-nm-thick OMoSi layer was deposited on the middle oxide and capped with 30-nm-thick blocking oxide. The sample was then annealed at 900°C for 60sec to form the second nanocrystals layer. Finally, a 500 nm thick Al gate electrode patterned with a shadow mask was evaporated by a thermal coater to form the memory structures. Transmission electron microscopy (TEM) was used to analyze the nanostructure of the nanocrystals and their surrounding oxide. Electrical characteristics of the capacitance–voltage (C-V) hysteresis were measured by an HP4284 Precision LCR Meter with frequency of 1 MHz.

4.3.3 Results and discussion

Figure 4-17(a) is a cross-sectional TEM image of a double-layer nanocrystal sample. From the cross-sectional TEM, it can be seen that the double-layer nanocrystals were formed after the 900°C annealing. Figure 4-18(a) is the C-V curve of a double-layer sample after the gate voltage is swept from the inversion to the

accumulation region of the substrate (4 to − 6 V) and (9 to − 11 V) and the reverse (−6 to 4 and −11 to 9 V). The C-V curve is also a counterclockwise hysteresis. It is seen that the memory window at the larger sweeping voltage of −11 to 9 V is about 6.6 V, which is larger than that of the single layer (3.6 V).

Figure 4-19 shows a comparison of the memory window between the single- and double-layer structures at various amplitudes of sweeping voltage. It can be found that as the sweeping voltage increases, the memory window increases in both structures. We note that the memory windows of the double-layer structure are larger than those of the single layer. For the difference in the memory window between the single- and double-layer memory structures, we consider that the injected carriers can be stored in the nanocrystals at the upper and lower layer of the double-layer structure, leading to the larger memory window than the window of a single-layer structure. Furthermore, the increment of the memory window becomes less and saturates in the single-layer structure at sweeping amplitudes higher than 8 V. This phenomenon can be attributed to the charging energy effect [4.18]. As the sweeping voltage increases, the increment of memory window indicates the increase of stored charge in the nanocrystals. The stored charges in the single-layer nanocrystals can lead to a large charging energy, which reduces the electric field on the tunnel oxide and blockades the injected carriers into nanocrystals. However, there was no observed memory window saturation phenomenon in the double-layer structure. It was considered that the charges stored in the lower layer of the double-layer structure can be released to the upper layer, which reduces the charge energy in the lower layer. Therefore, the memory saturation phenomenon is not serious in the double-layer structure. The double-layer memory structure can increase the memory window and is preferred for applications in nonvolatile memory.

Figure 4-20(a) and (b) show the comparison of the retention between the single-

and double-layer structure at room temperature and at 85°C, respectively. It can be seen that the retention characteristics of both structures at room temperature are similar. However, the retention characteristics at 85°C in Fig. 3b show that the double-layer structure has better retention (charge remaining at 61%) after 10^4 retention times than the single-layer structure (charge remaining at 16%). The good retention of the double-layer structure is due to the coulomb blockade effects on the upper-layer nanocrystals from the bottom layer nanocrystals. As shown in Fig. 4-21(b), after the charge is stored in the nanocrystals of both layers, the stored charges in lower layer nanocrystals can raise the electronic energy in the middle oxide to blockade the stored charges in the upper-layer nanocrystals. So the memory effects of the nonvolatile memory device can be improved by using the double-layer nanocrystal structure.

4.3.4 Conclusion

The double-layer nanocrystal memory was fabricated through annealing the stacked oxygen-incorporated Mo silicide layer at 900°C. The results showed that the double-layer structure has a larger memory window (6.6 V) and better retention (61%) than the single-layer structure (16%) at 85°C. Therefore, the double-layer structure, which can enhance memory characteristics, is promising for applications in nonvolatile memory.

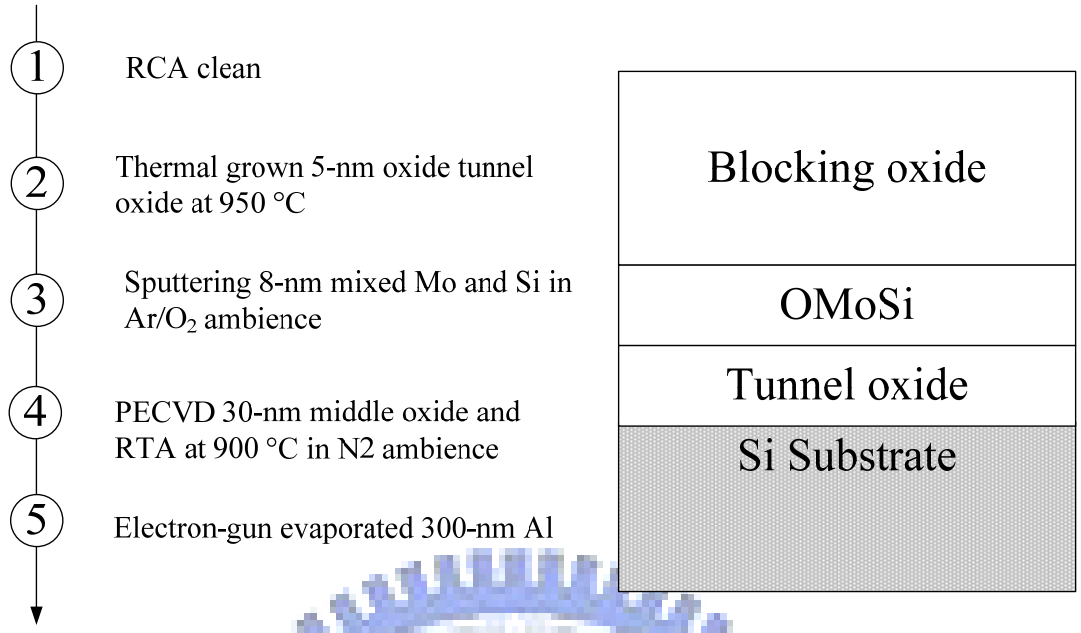


Figure 4-1 Process flow and device structure of Mo nanocrystal embedded in silicon oxide.

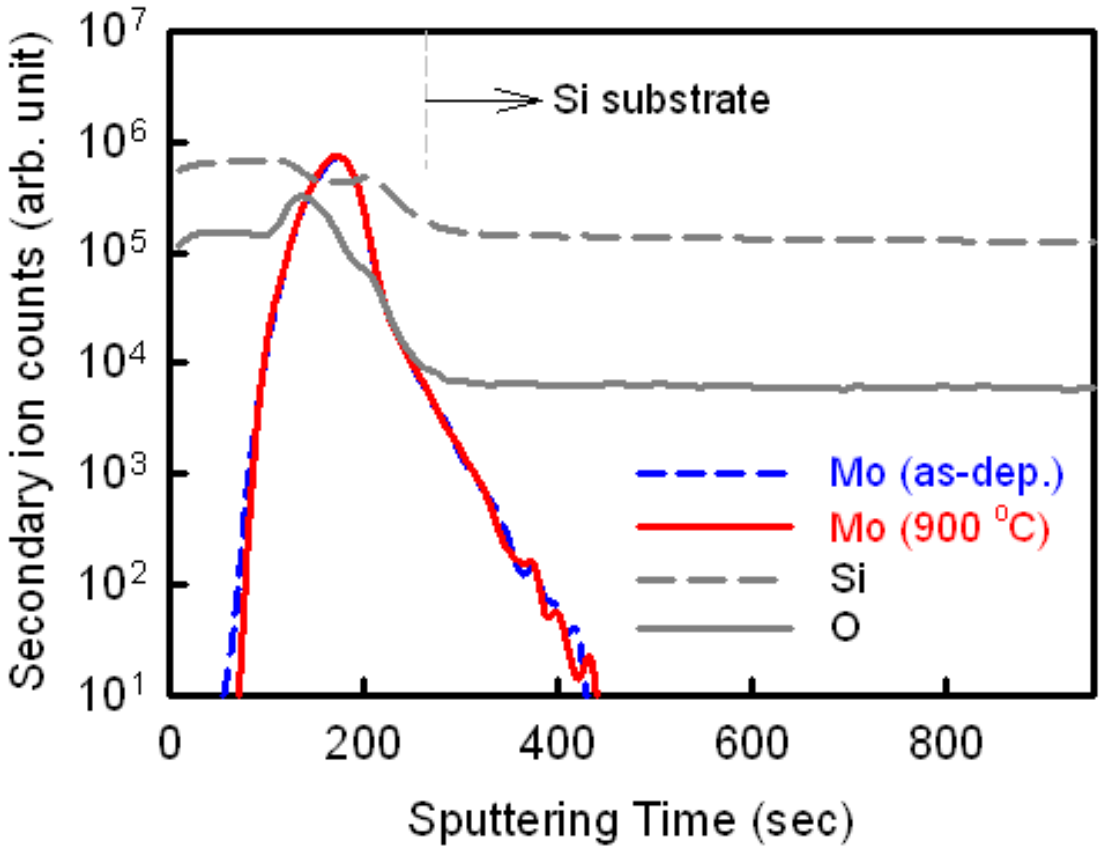


Figure 4-2 Secondary ion mass spectra in SiO_2/OMoSi/SiO_2/Si substrate of as-deposited and 900°C-annealed samples.

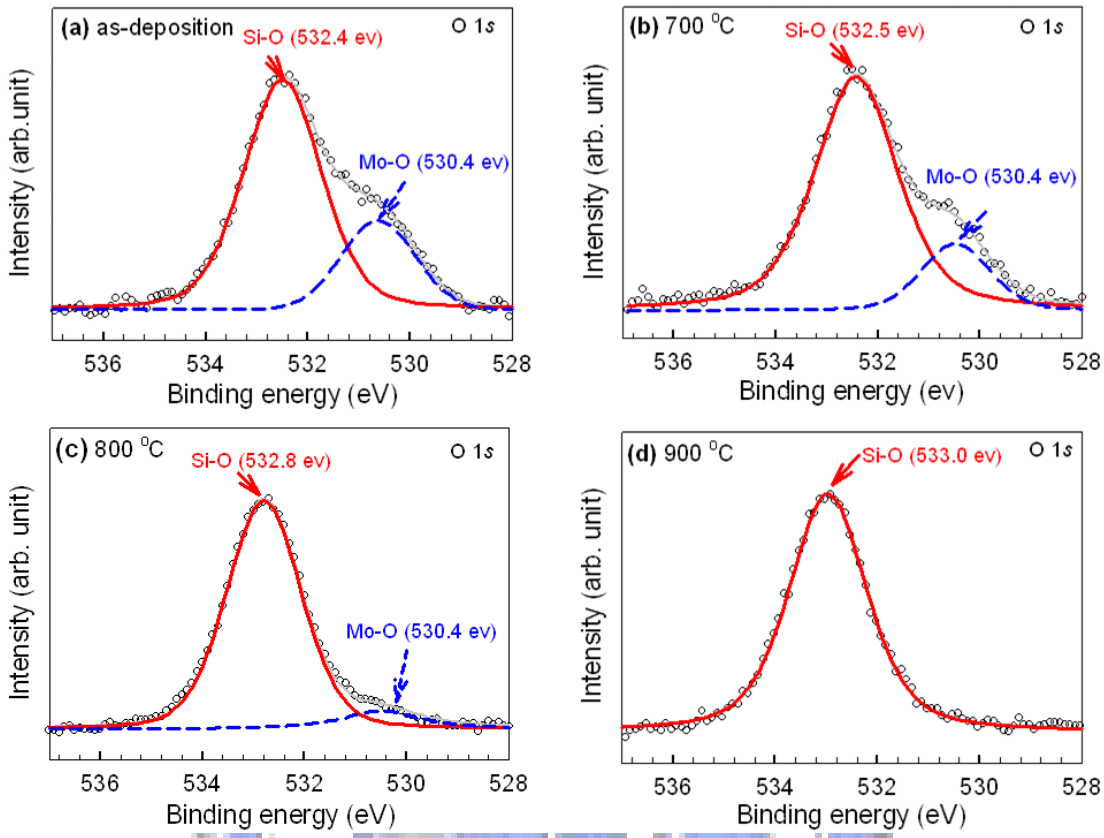


Figure 4-3 XPS O 1s spectra of OMoSi layer at various annealing temperatures.

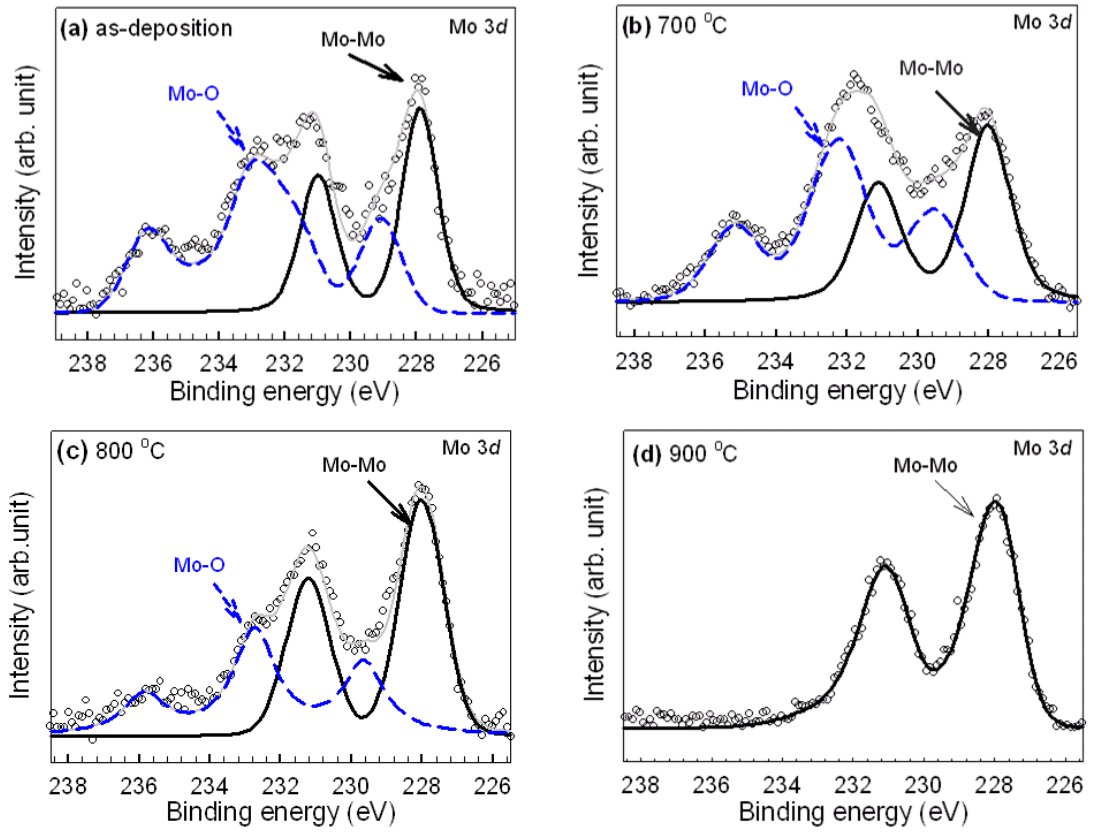


Figure 4-4 XPS Mo 3d spectra of OMoSi layer at various annealing temperatures.

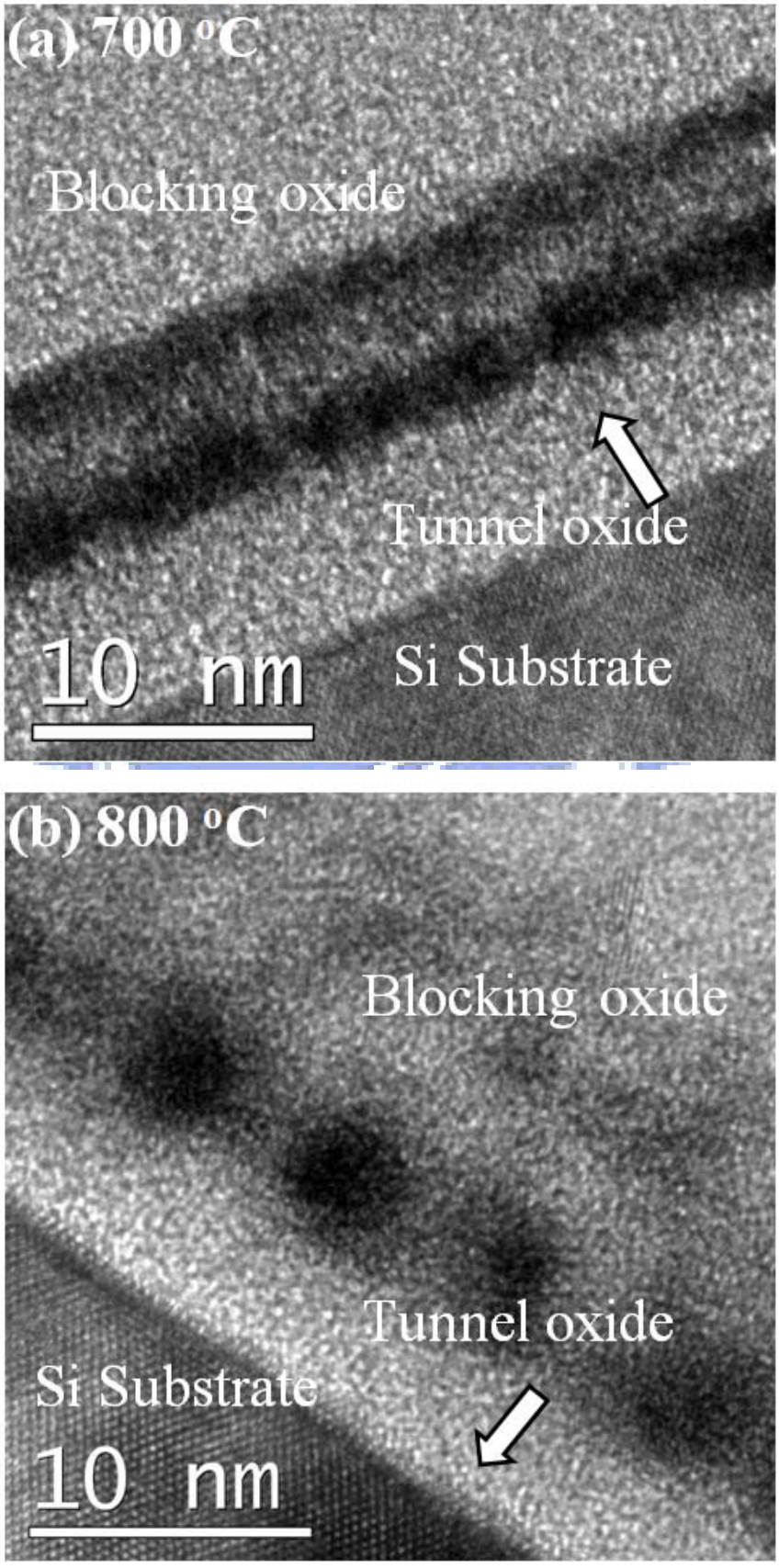


Figure 4-5 Cross-section TEM of OMoSi layer after annealing at (a) 700°C and (b)

800°C.

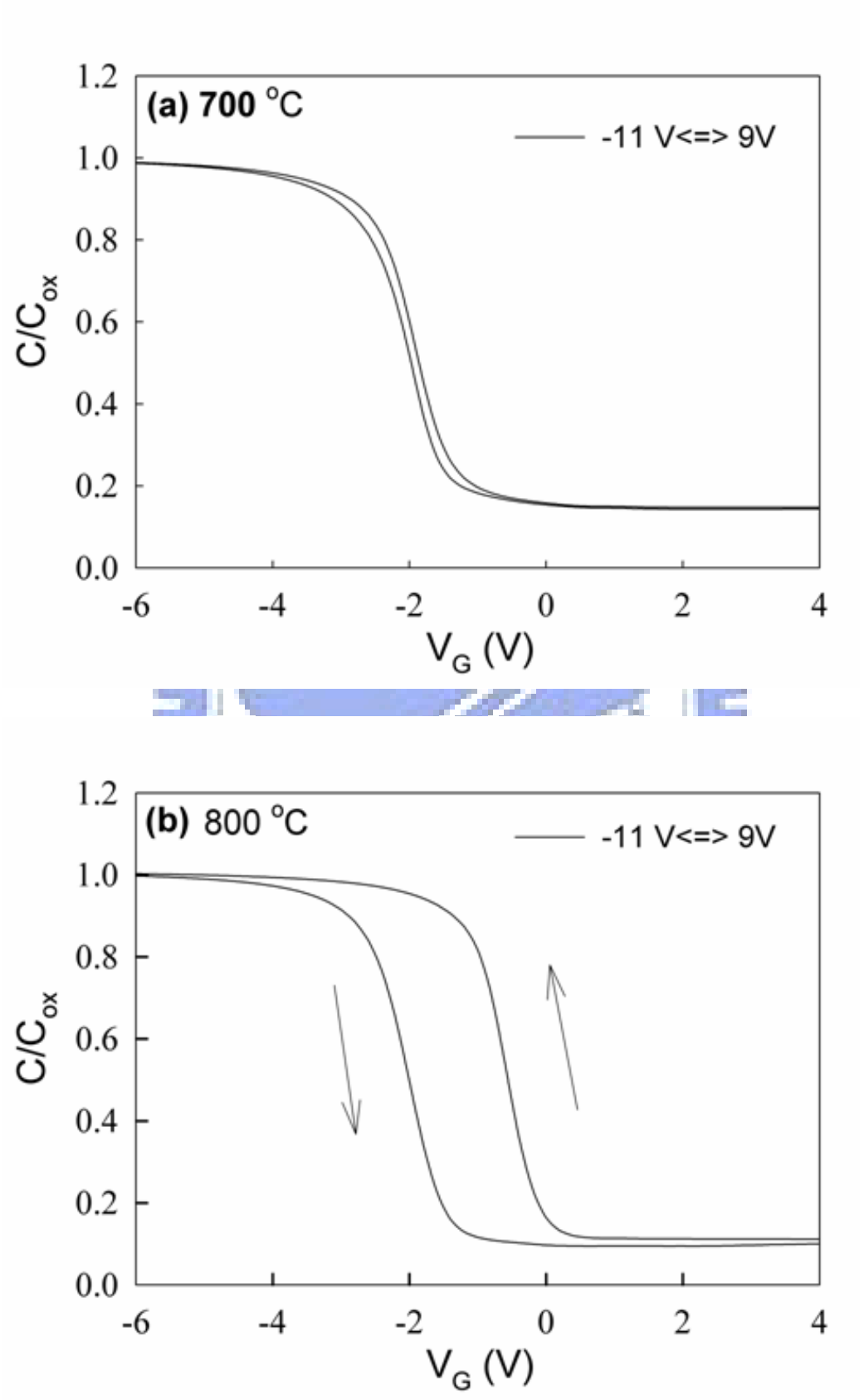


Figure 4-6 C-V curve of (a) 700°C- and (b) 800°C-annealed samples.

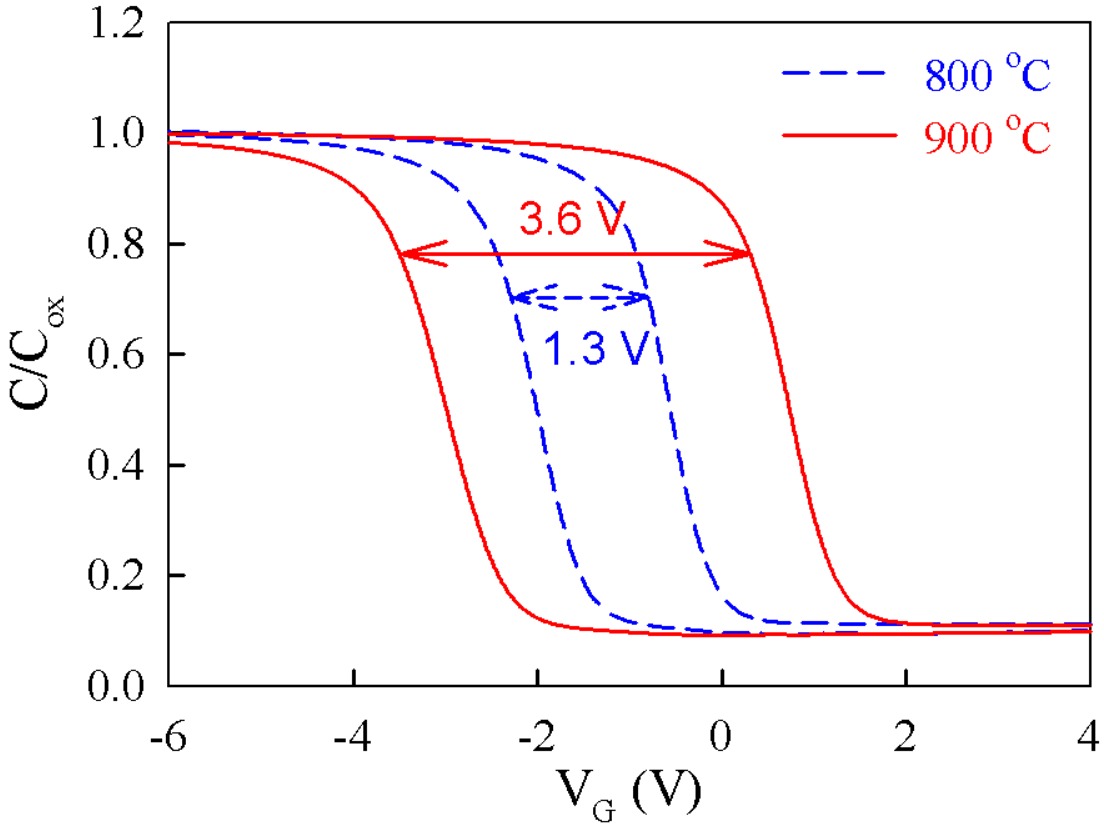


Figure 4-7 A comparison of memory window between 800°C and 900°C -annealed samples.

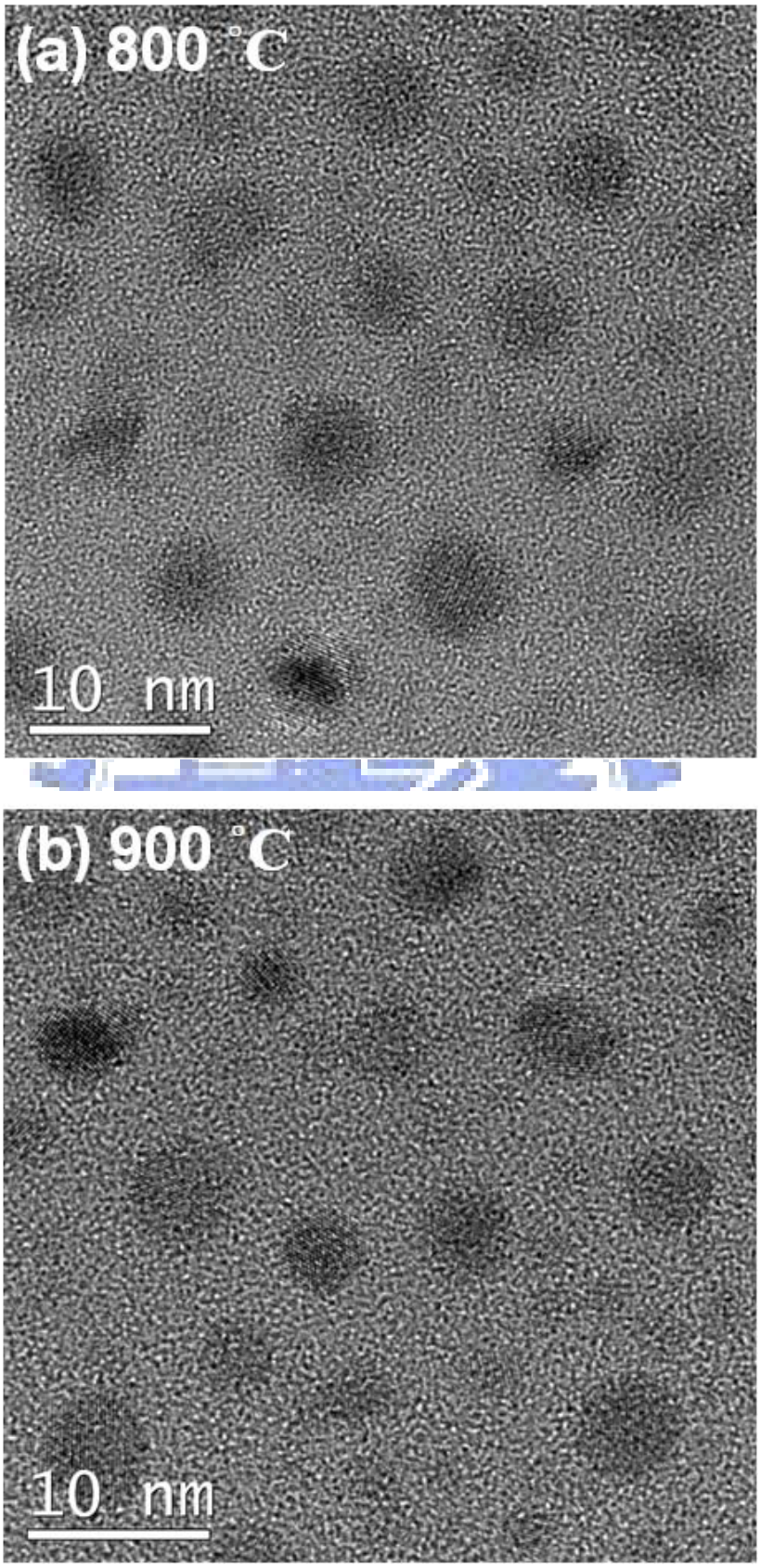


Figure 4-8 TEM plane-view of OMoSi layer after annealing at (a) 800°C and (b) 900°C.

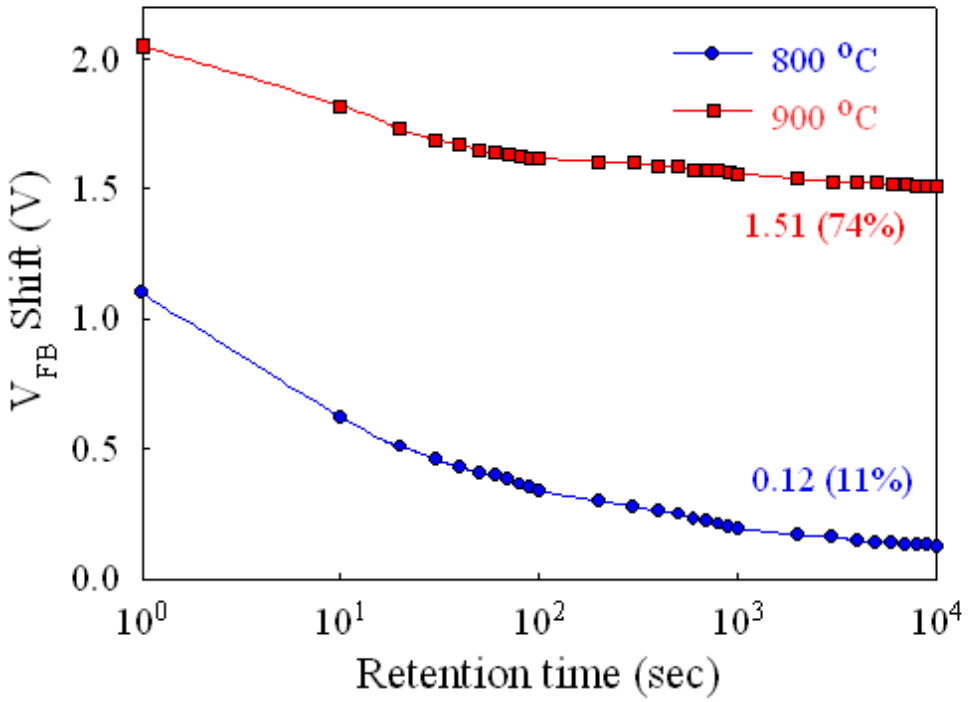


Figure 4-9 Comparison of retention between 800 and 900 °C annealed samples.

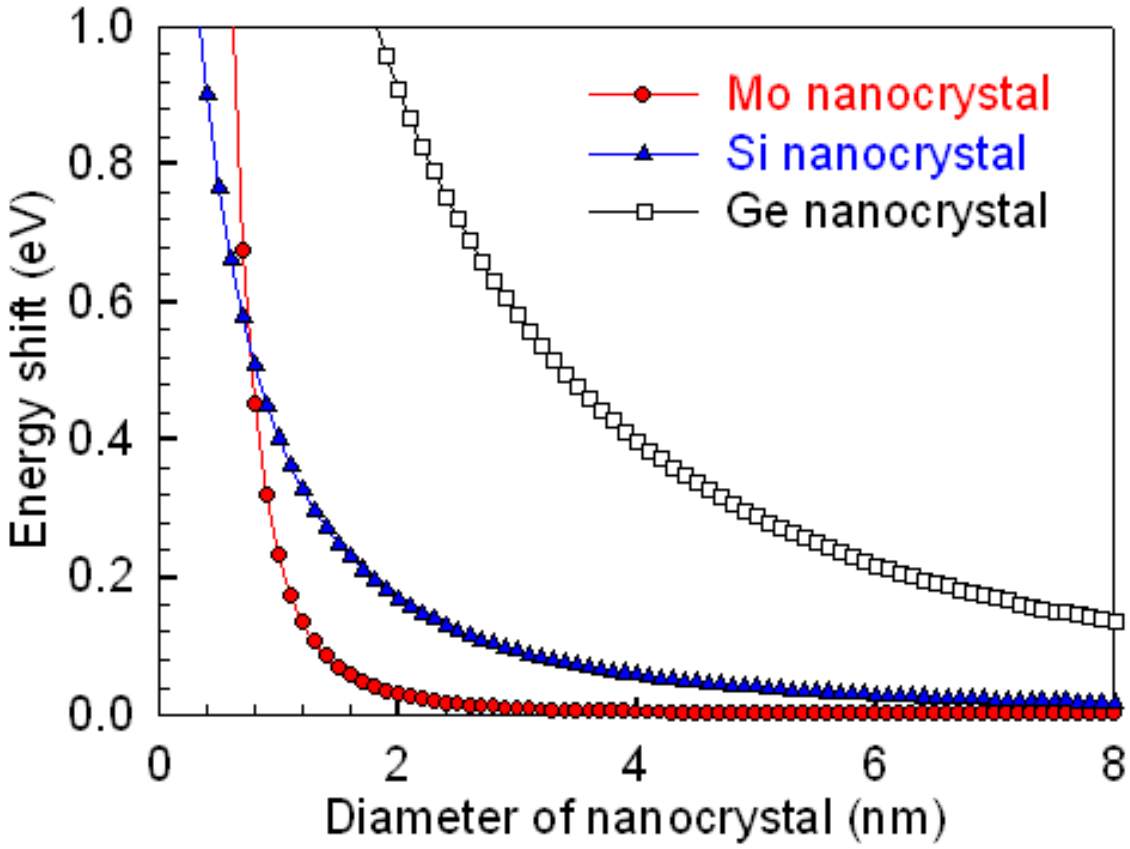


Figure 4-10 Quantization effect on Si, Ge and Mo nanocrystal [4-16].

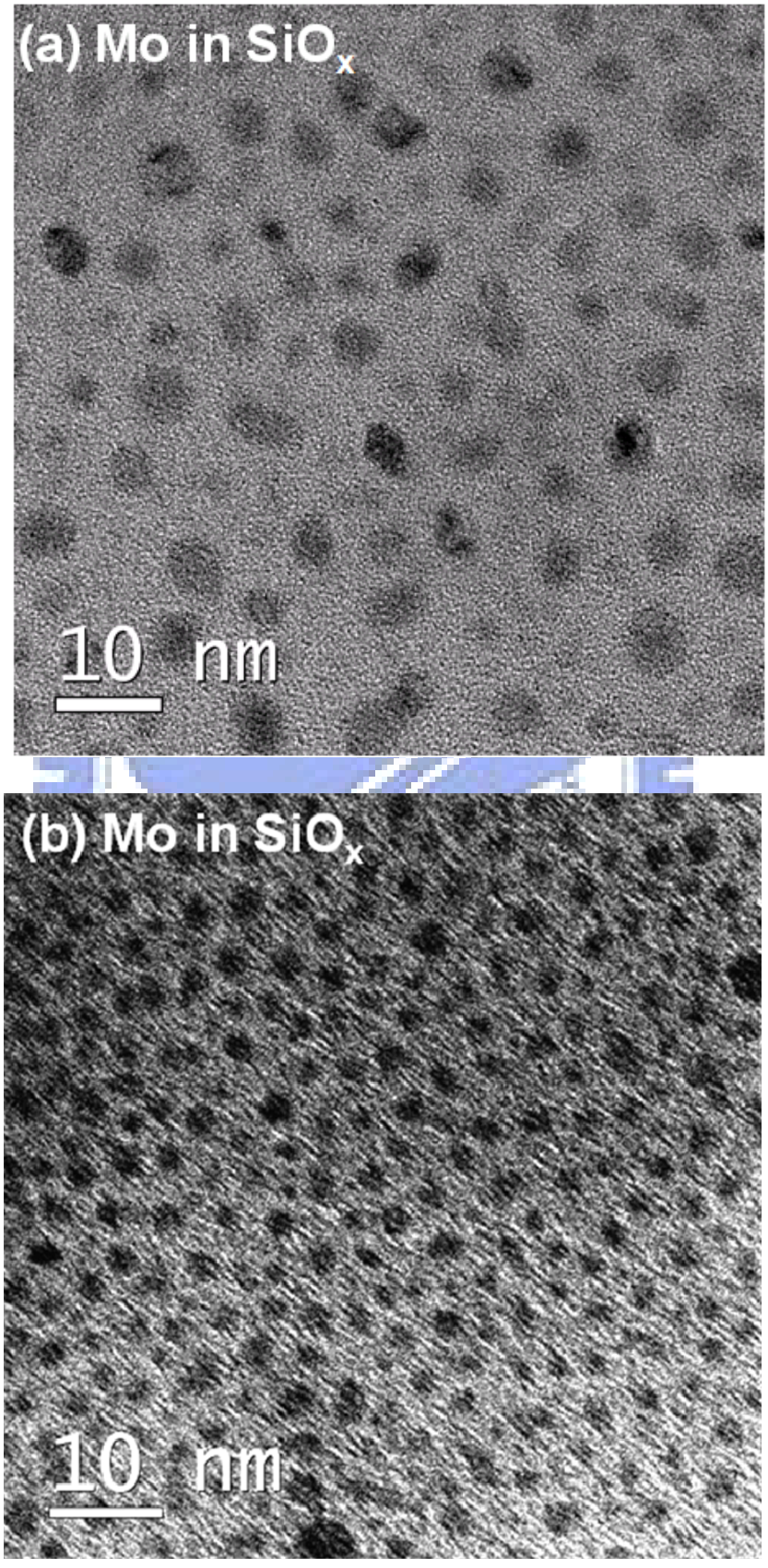
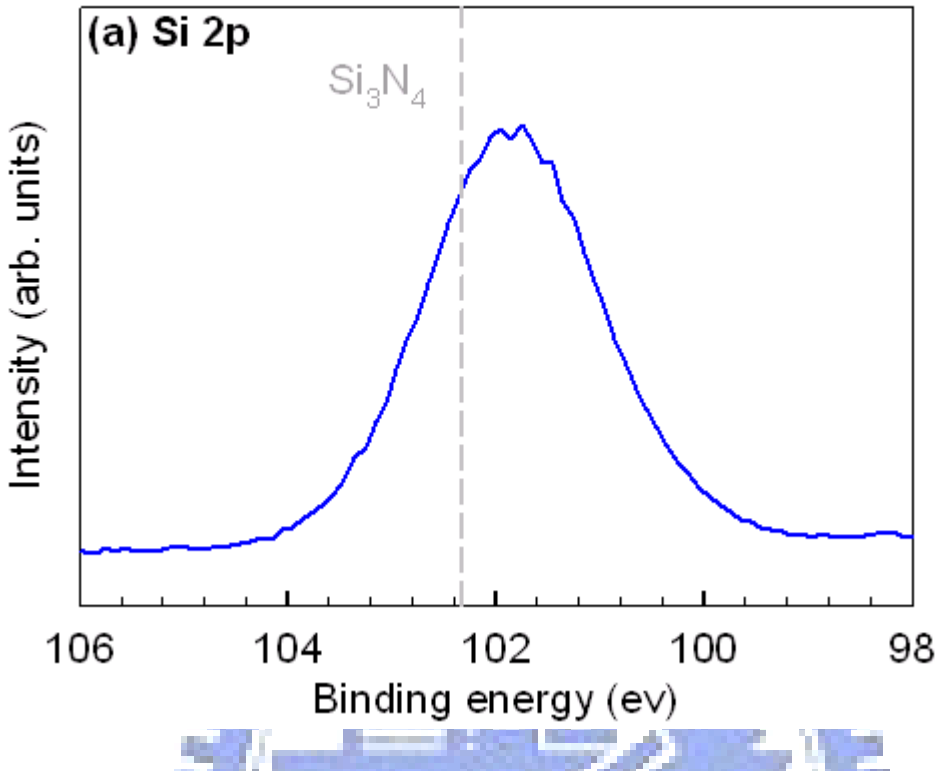


Figure 4-11 Plane-view TEM of Mo nanocrystal embedded in SiO_x and SiN_x.



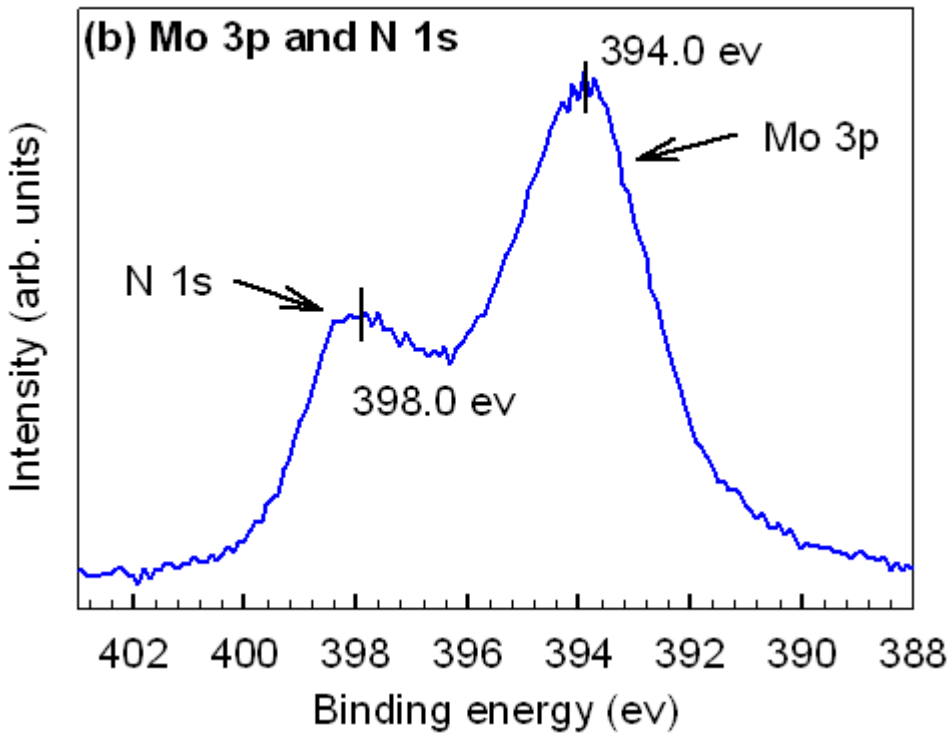


Figure 4-12 XPS Si 2p (a), and N 1s and Mo 3p (b) of nitrogen incorporated Mo silicide layer after annealing at 900 °C

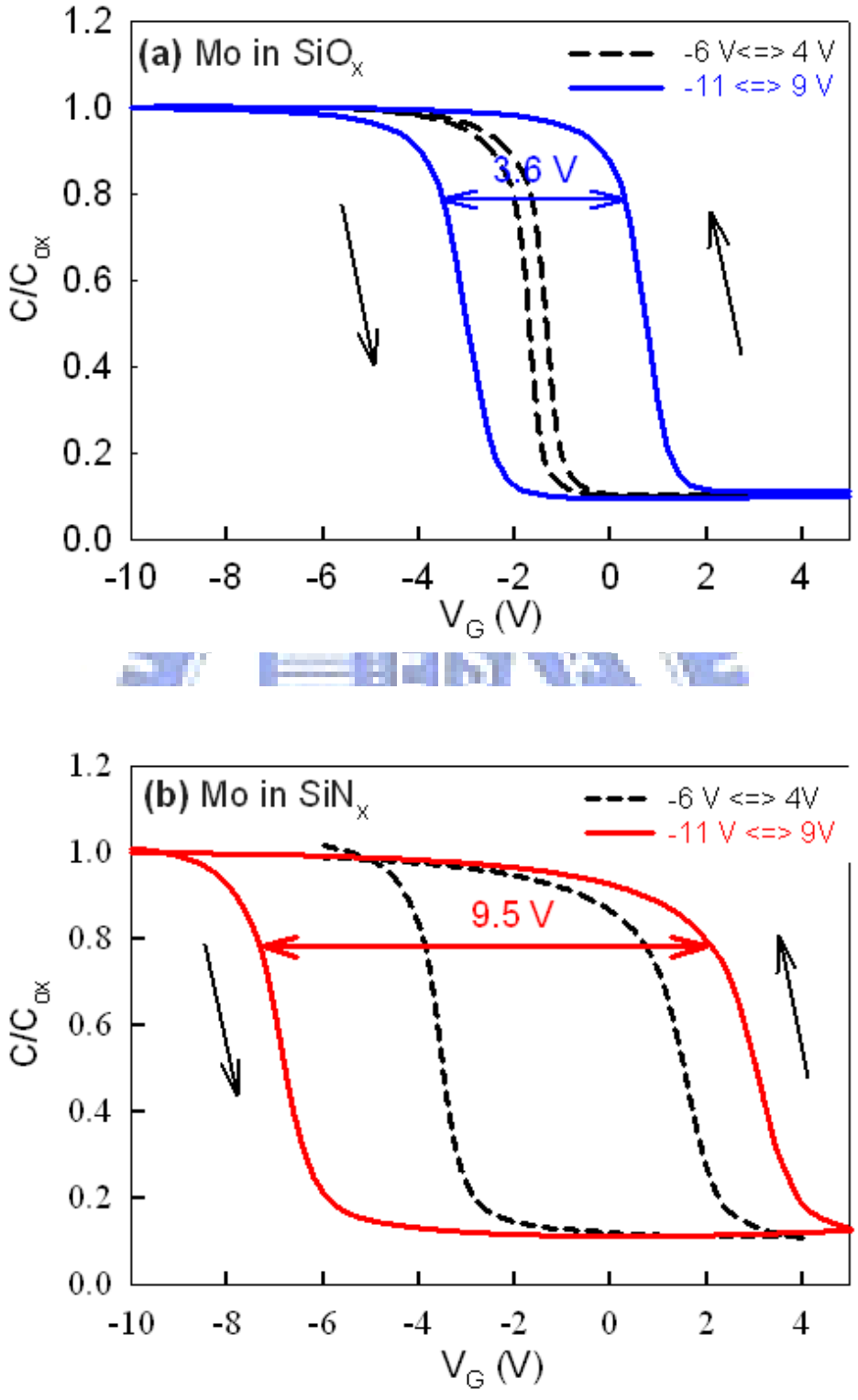


Figure 4-13 C-V curve of Mo nanocrystal embedded in SiO_x and SiN_x.

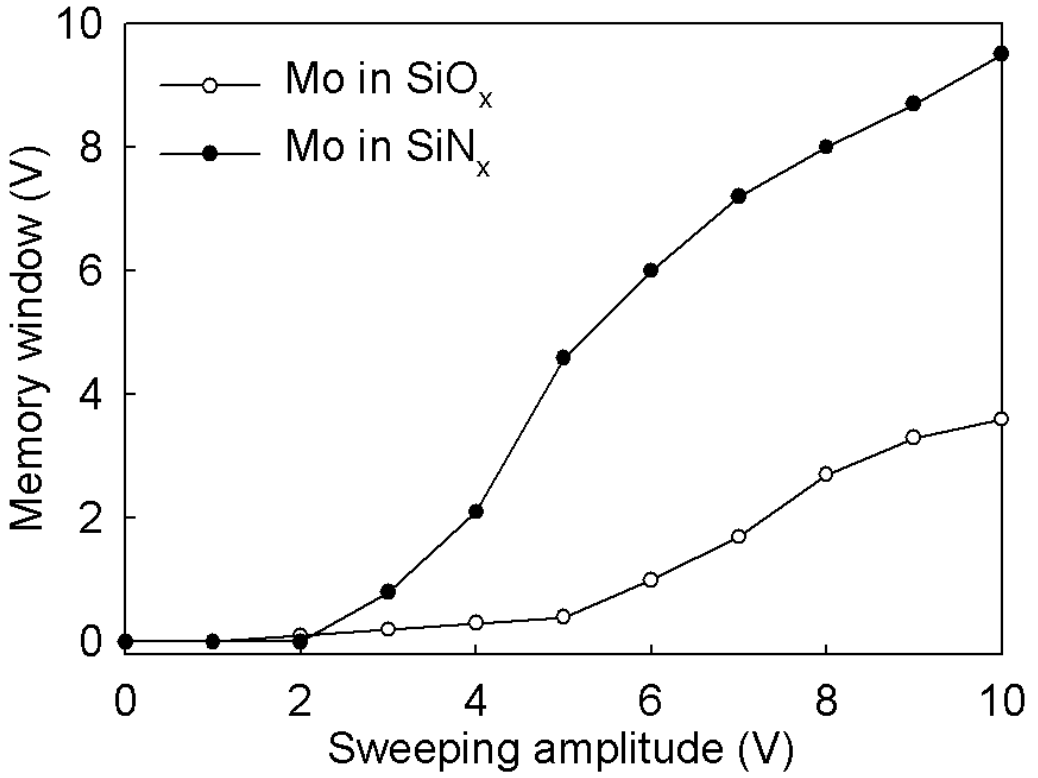


Figure 4-14 Memory window of Mo in SiO_x and SiN_x at various sweeping voltages.

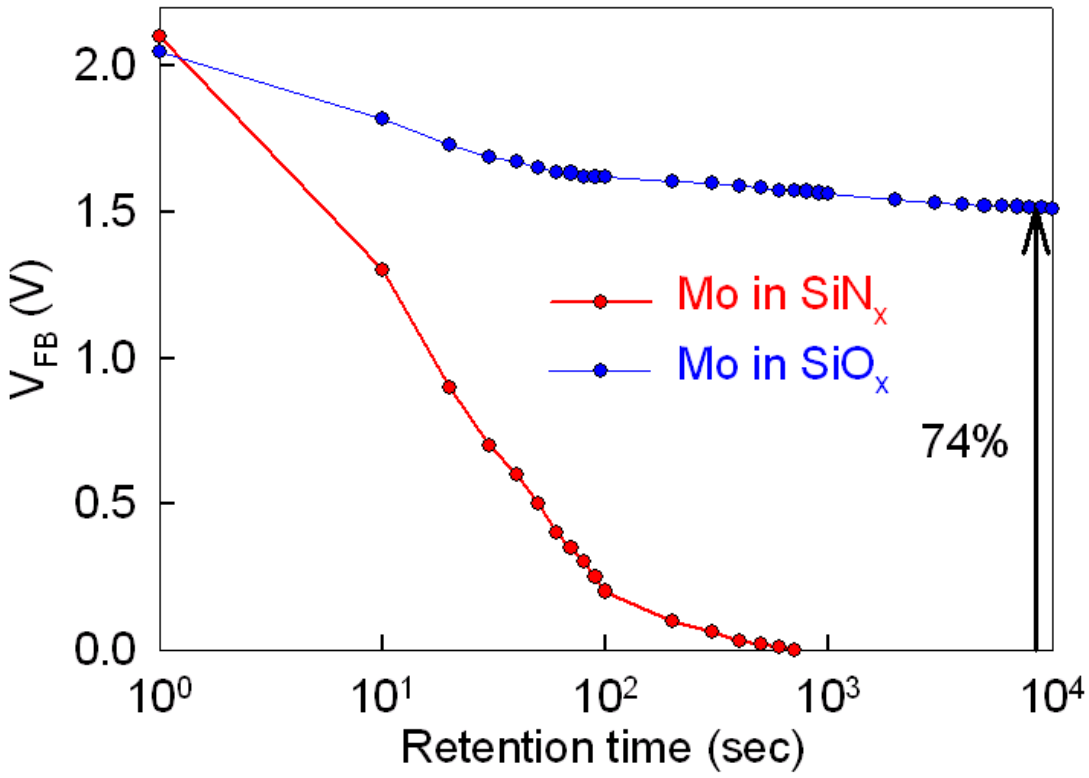


Figure 4-15 A comparison of retention behavior for Mo in SiN_x and Mo in SiO_x.

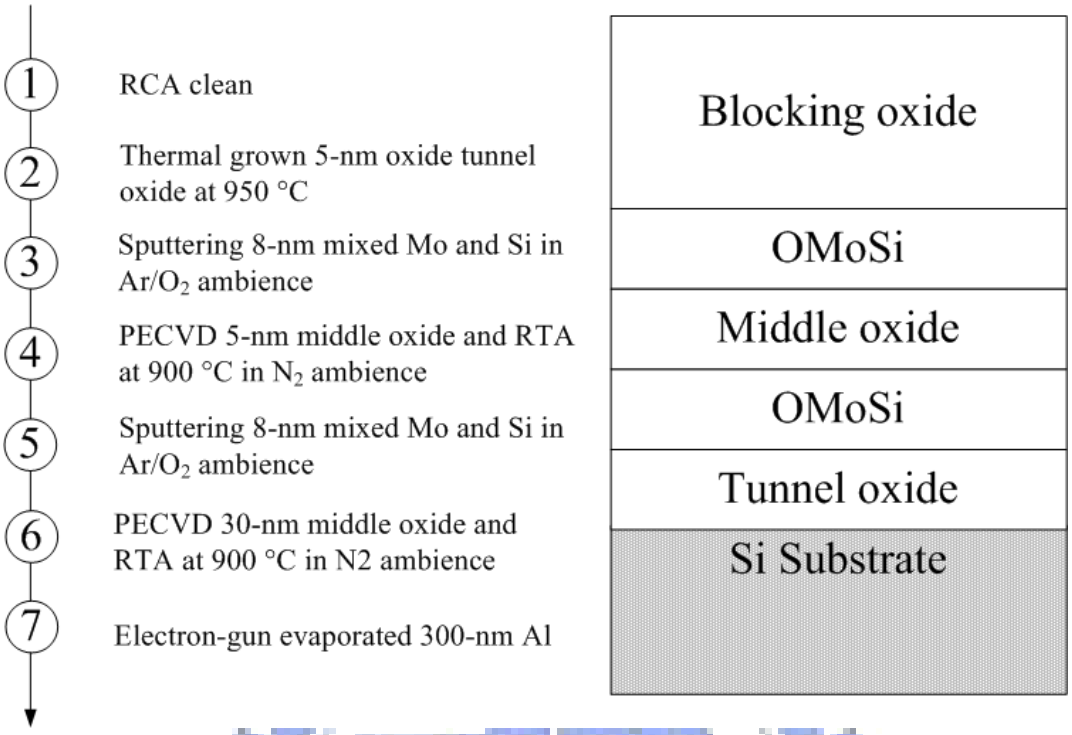


Figure 4-16 Process flow and memory structure of double layer Mo nanocrystal.

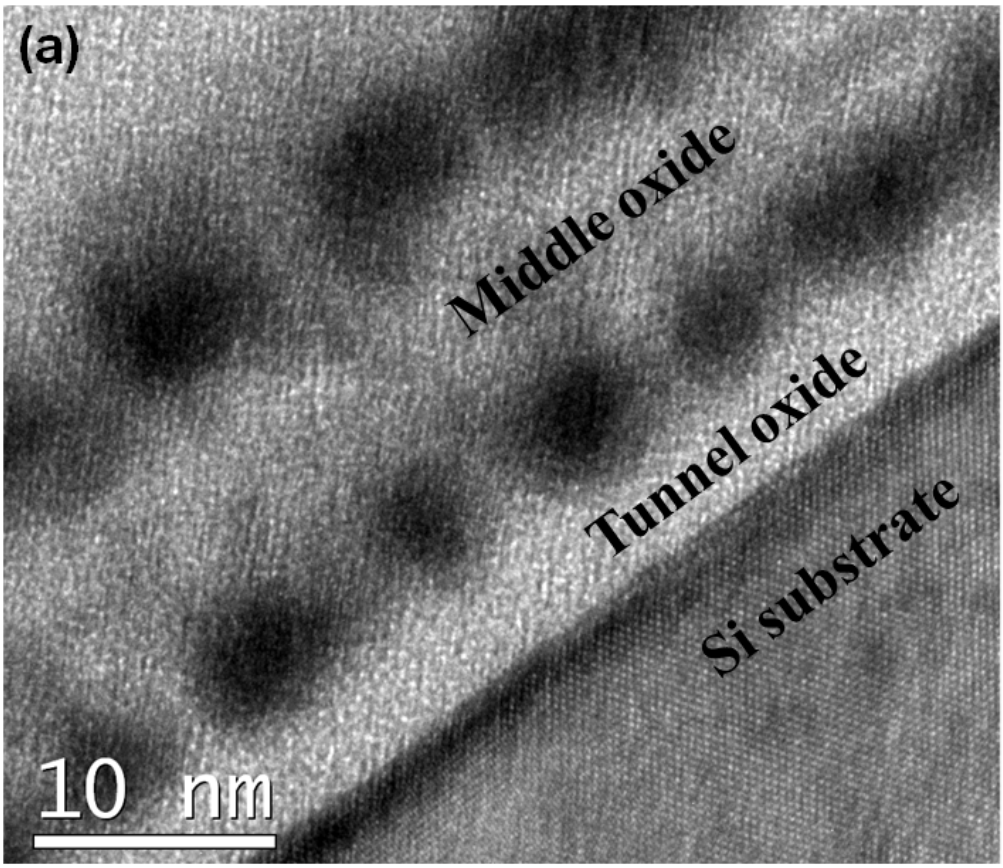


Figure 4-17 Cross-section TEM of double layer Mo nanocrystal embedded in silicon oxide.

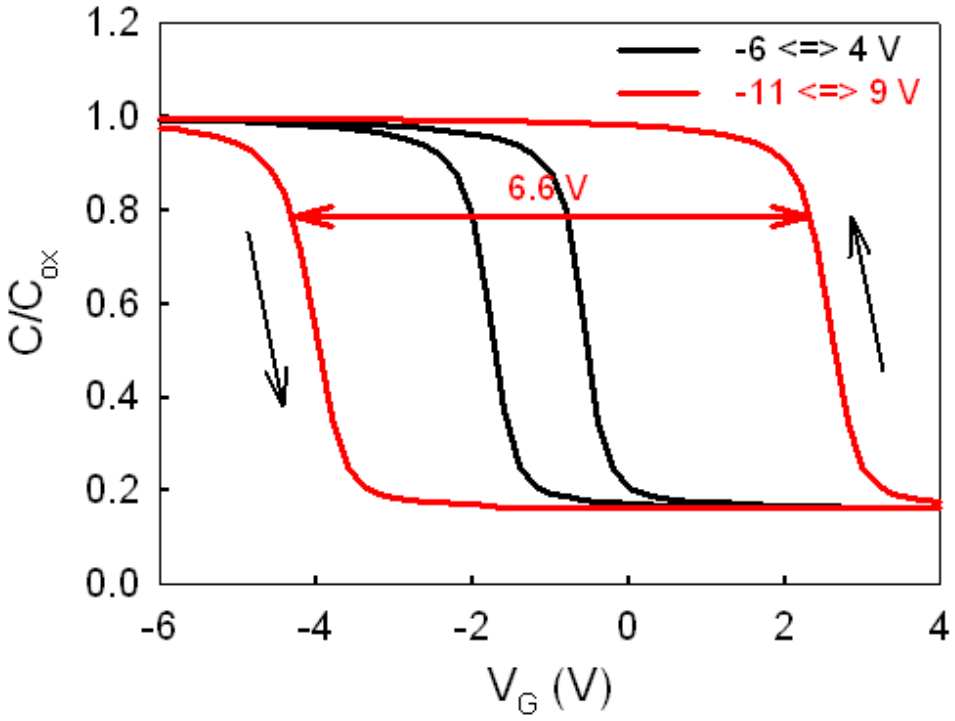


Figure 4-18 C-V curve of double layer structure for Mo nanocrystal in SiO_X.

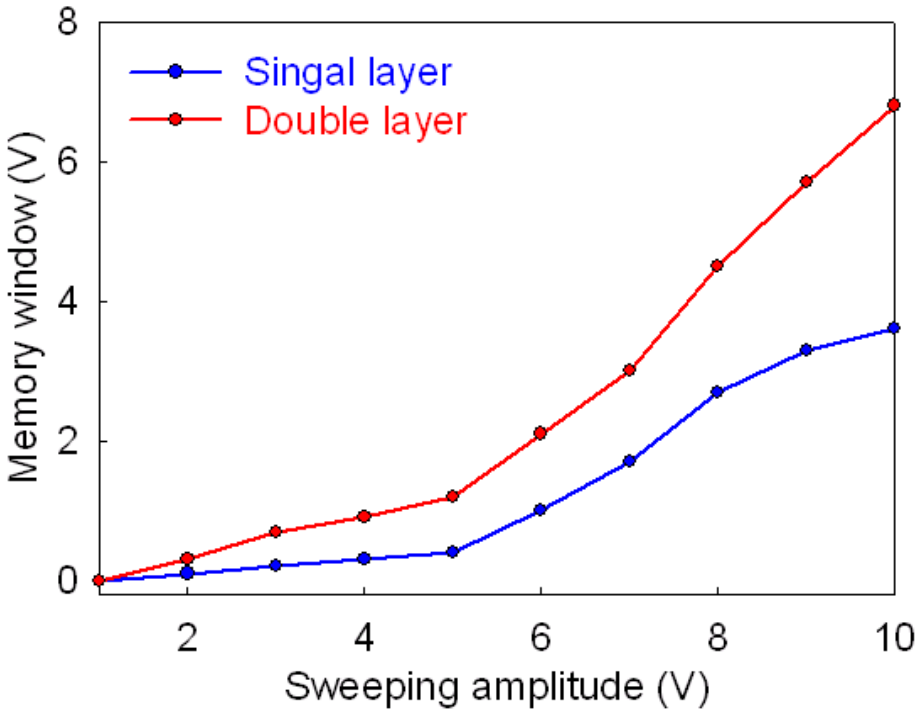


Figure 4-19 Memory window of single and double layer at various sweeping amplitudes.

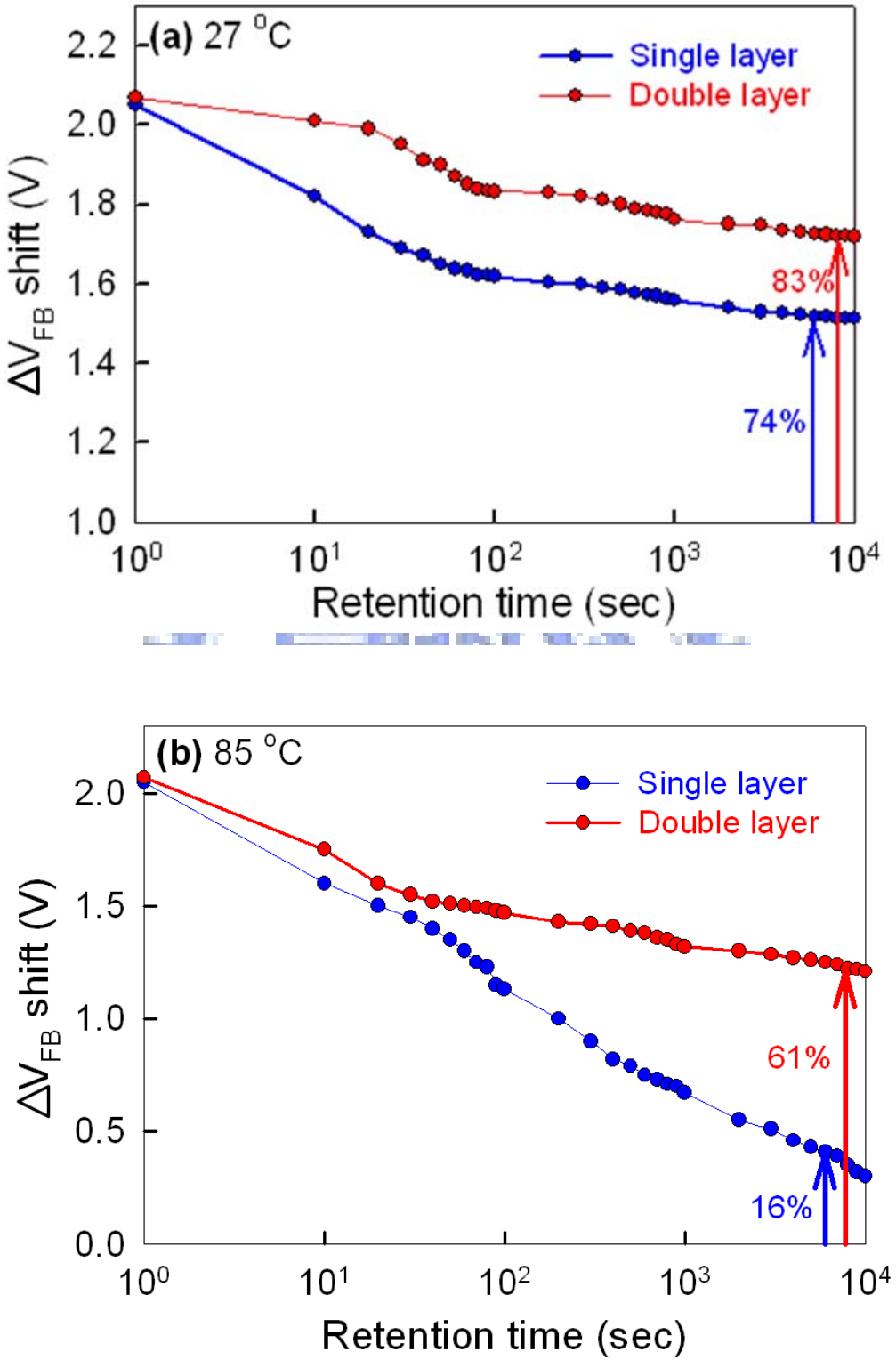


Figure 4-20 Comparison of retention characteristics for single- and double- layer structures at (a) room temperature (27°C) and (b) 85°C.

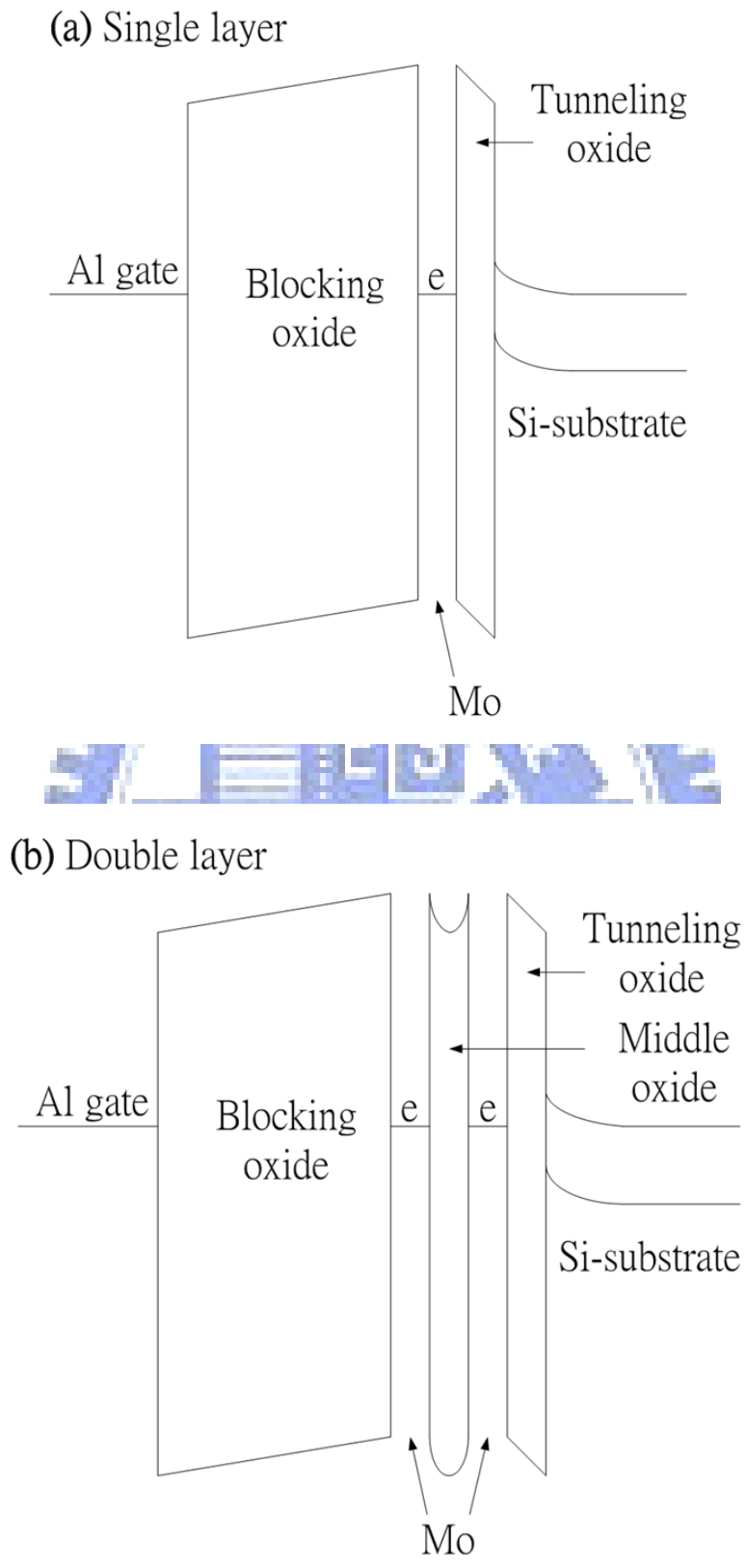


Figure 4-21 Band diagrams of (a) single- and (b) double-layer structures in retention.

Chapter 5

Memory characteristics of Mo nanocrystal influenced by ammonia plasma treatment

5.1 Charge storage characteristics of Mo nanocrystal memory influenced by ammonia plasma treatment

5.1.1 Introduction

Nonvolatile memory composed of floating structure plays an important role in portable devices such as cell-phones, notebook computers and digital cameras. However, conventional floating structure confronts a bottleneck on reduction of tunnel oxide in the memory structure because carriers stored in an electrical continuously conducting polycrystalline silicon (poly-Si) floating gate will totally lose if one defect chain exists in the tunnel oxide [5.1,5.2]. The nanocrystals embedded in dielectric as charge storage centers in the floating gate structure has attracted much attention for next generation nonvolatile memory because carriers stored in electrically isolated nanocrystals can suppress carrier loss [5.2]. Several methods have been investigated to fabricate nanocrystals such as ion implantation [5.3,5.4], sputtering [5.5,5.6] and oxidation [5.7,5.8]. It is expected that those processes can induce defects or traps in the dielectric around nanocrystals during the fabrication process. The induced deficiency in the surrounding dielectric can lead to stored charges leaking out of the nanocrystals through trap assisted tunneling [5.9]. Therefore, the quality of the surrounding oxide which electrically isolates the nanocrystals is an important issue in research on nanocrystal memory. Two possible

ways to gain good reliability are improving the surrounding oxide of nanocrystal by using hydrogen treatment with a high pressure at high temperature (> 900°C) and nitrogen annealing at high temperature (> 1000°C). However, it is well known that the Si—H bond is weak and easily to be broken during endurance tests. For the nitrogen annealing, a high temperature process (> 1000°C) is required to dissociate the nitrogen to strengthen the surrounding oxide layer [5.10,5.11] Therefore, the process is not appropriate for application in semiconductor industry and for nanocrystal memory in terms of thermal budget.

In this study, Mo nanocrystal memory was fabricated through annealing the oxygen incorporated Mo silicide layer [5.12]. We investigated effect of ammonia (NH_3) plasma treatment on memory characteristics of Mo nanocrystal embedded in SiO_x as the charge storage layer. The plasma enhanced process is widely used in the semiconductor industry for its benefit with regard to small thermal budget, which is important for IC technology because the thermal budget may lead the redistribution of source/drain dopant or density and size of nanocrystal. Furthermore, the NH_3 plasma treatment technique has been investigated to improve the quality of gate dielectric [5.13,5.14]. Our experimental results show that the memory characteristics including memory window, retention and endurance were influenced by incorporation of nitrogen into the surrounding oxide.

5.1.2 Experiment

The experimental process flow and memory structure is shown in Figure 5-1. The memory-cells were fabricated on 6 inch *p*-type Si substrate. After the substrate was cleaned by a standard RCA process, a 5-nm-thick dry oxide layer was grown at 950°C on the substrate in a horizontal furnace. An 8-nm-thick Mo silicate layer was then deposited on the oxide layer using co-sputtering Mo and Si in Ar (24 sccm)/O

(2sccm) ambience. 30-nm-thick Si oxide was deposited on the Mo silicate layer as the blocking oxide by plasma enhanced chemical vapor deposition at 300°C. The thermal annealing process was performed in N_2 ambience at 900°C for 60s to form Mo nanocrystals embedded in SiO_x. Cells were subsequently treated with NH_3 plasma in a PECVD chamber for 30 min with a NH_3 gas flow rate of 20 sccm and chamber pressure of 67 torr at 50W. For the electric characteristic measurement, 500-nm-thick Al was thermally evaporated with a shadow mask on the blocking oxide to form the metal-oxide-semiconductor structure. The microstructure of Mo nanocrystals was analyzed through a transmission electron microscope (TEM). The chemical bonding and composition of the charge storage layer was analyzed with X-ray photoemission spectroscopy (XPS). Electrical characteristics were measured using a Keithley4200 and HP4284 Precision *LCR* meter with a frequency of 1 MHz.

5.1.3 Result and discussion

Figure 5-2(a) and (b) show the TEM for the charge storage layer with and without the plasma treatment. The average size and density of both samples are estimated at about 4-5 nm and 10^{12} cm^{-2}. Density as high as 10^{12} cm^{-2} is a basic requirement for nanocrystal memory to prevent the variation of memory characteristics between cells during reduction of the nonvolatile memory structure. In this case, however, the high density results in the thickness of the surrounding oxide, which electrically isolates nanocrystals, being only 4-5 nm, as shown in the Fig 5-2. Therefore, if traps exist in the oxide, this can result in a serious tunnel process of the stored carriers between nanocrystals (trap assisted tunnel mode) [5-9].

In our previous study, we found that the oxide surrounding the Mo nanocrystal is deficient (oxygen deficiency) [5-12]. Figure 5-3 shows XPS Mo 3*p* and N 1*s* spectra of the charge storage layer (a) without and (b) with the plasma treatment, both

performed by using a monochromatic Al *Kα* (1486.6 ev) X-ray. It can be seen that an additional XPS peak (397.8 ev) appears in Mo 3*p* and N 1*s* spectra of the charge storage layer after the plasma treatment due to formation of O-Si-N bonds. This suggests that the incomplete bonds in SiO_x bonded with nitrogen after the plasma treatment, as shown in Fig. 5-3 [5.15].

Figure 5-4(a) and (b) show the *C-V* curves of the MOS structure embedded with the Mo nanocrystal for the sample with and without the plasma treatment, respectively. At the smaller sweeping voltage of 2 V, there is a negligible memory window in Fig 5-4(a) and (b) corresponding to the quasi-neutral state (i.e. no charge is stored in the charge storage layer under this sweeping range). At the larger sweeping voltages (-11 V to 9 V and vice versa), there are counterclockwise memory hysteresis, as evident in Fig. 5-4(a) and (b). The counterclockwise hystereses are due to carrier transport through tunnel oxide between the charge storage layer and the Si substrate. We note that the memory windows were reduced (0.6 V reduction) for the sample with the plasma treatment. The reduction of the memory window after the treatment was related to the nitrogen passivation in the charge storage layer. It has been suggested that the traps in the oxide around nanocrystals can capture carriers and contribute to the memory window [5.12]. According to XPS results, the nitrogen was incorporated into the oxide around the Mo nanocrystals after the treatment. The incorporated nitrogen can passivate the traps in the oxide, which reduce the charge storage centers in the surrounding oxide, leading to the smaller memory window.

Figure 5-5 is a comparison of retention behavior for the samples with and without the plasma treatment, respectively. Retention was measured at stress voltage of 10 V on Al gate electrode for 5s. The memory window was obtained by comparing the *C-V* curves between the charged state and the quasi-neutral state. When carriers are stored in the nanocrystals, the stored carriers will raise the potential energy of the

nanocrystals and increase escape probability of the stored carriers. Furthermore, carriers trapped in the shallow traps are unstable, and can easily leak back to the silicon substrate. In the Fig. 5-5, for retention time before 10^2 sec, the charge loss rate is significant, becoming stable over a longer retention time. This result is in consistent with partial carriers trapping in the shallow trap states of the SiO_x matrix around the nanocrystals. Because the decline rate of flatband voltage after 10^2 sec retention time is stable, the reduction rate of flatband voltage has an exponential dependence on retention time according to the one-dimensional direct tunneling model [5.16]. Therefore we can extrapolate the retention characteristics to 10 years with a slope of the stable range

$$m = \frac{V_{FB2} - V_{FB1}}{\log t_2 - \log t_1},$$

where V_{FB1} and V_{FB2} are the flatband voltage shift at the retention time of 10^2 sec (t_1) and 10^4 sec (t_2), respectively. A 1.4 V memory window (charge remaining at 68%) can be obtained after 10 years by analyzing the extrapolation value of retention data. In contrast, the charge loss rate of the sample after the treatment is slower than that without the treatment, with the memory window remaining at 86%. The superior retention of the sample with the treatment can be explained by the nitrogen passivation of the traps in the oxide around Mo nanocrystals, schematically expressed in Fig. 5-6. When carriers are stored in nanocrystals after programming, if there is a defect chain in the tunnel oxide, the nanocrystal which aligns with the defect chain will be discharged immediately. As shown in Fig. 5-6(a) for the sample without the plasma treatment, the carriers stored in the neighbor nanocrystals can escape to the discharged nanocrystal by traps assisted tunneling, which results in a faster loss rate of the stored carriers. For the sample with the plasma treatment, the traps in the surrounding oxide were reduced by nitrogen passivation. The trap assisted lateral

migration of the stored carriers was suppressed, which improves the retention of the memory structure, as shown in Fig. 5-6(b).

Figure 5-7(a) is a comparison of the endurance characteristics of the samples with and without the plasma treatment under pulse conditions of V_G = ±15 V for 1ms, respectively. For the sample without the plasma treatment, the ΔV_{FB} (the difference between programming and erase states) was reduced significantly, remaining 51% after 10^6 program/erase cycles. However, the plasma-treated sample exhibits robust endurance characteristic (ΔV_{FB} of 89% after 10^6 program/erase cycles). It has been previous shown that the ΔV_{FB} reduction during such an endurance test is due to the degradation of the gate oxide [5-13]. Carriers tunneling from the substrate into the charge storage layer during the endurance test can release energy to destroy the surrounding dielectric [Fig. 5-7(b)], which results in the reduction of the ΔV_{FB}. For the sample without the plasma treatment, there are a large number of weak or dangling bonds in the surrounding oxide induced during the formation of nanocrystals. The bonds can easily break during the programming/erase cycles, leading to a faster degradation rate of the surrounding oxide. After the plasma treatment, because the traps were reduced, and the surrounding oxide was strengthened by the nitrogen incorporation, the generation rate of traps reduced, resulting in the better endurance characteristic.

Table 5-1 compares the memory characteristics of Mo nanocrystal before and after NH_3 plasma treatment. It can be seen that the NH_3 plasma treated Mo nanocrystal memory with good reliability characteristic is suitable for nonvolatile memory application [5.17-5.19].

5.1.4 Conclusion

In conclusion, the nonvolatile memory characteristics of the Mo nanocrystals

were influenced by the ammonia plasma treatment. The *C-V* hysteresis reduced from 3.6 to 3.0 V due to reduction of trapping centers in the surrounding oxide. The retention characteristic improved from 68% to 86% remained charges after the plasma treatment because the carriers' lateral migration between nanocrystals was suppressed through the nitrogen passivation of the traps in the surrounding oxide. The incorporation of nitrogen into the charge storage layer through the NH_3 plasma treatment can strengthen the endurance characteristic of Mo nanocrystals memory. It is promising to use the NH_3 plasma treatment to passivate the surrounding oxide of nanocrystals for the next generation floating gate flash memory devices.

5.2Influence of ammonia plasma treatment on the memory characteristics of Mo nanocrystal embedded in silicon nitride

5.2.1 Introduction

In the chapter 5, we try to increase the density of Mo nanocrystal by annealing nitrogen-incorporated Mo silicide layer. The density as high as 6×10^{12} cm^{-2} can be attained. It is know that the high density can prevent the memory characteristics from being variation between memory cells. Furthermore, Mo embedded in SiN_x has a large memory window at the relative low sweeping voltage. It seems that Mo nanocrystals embedded SiN_x as the charge storage layer can be application in nonvolatile memory with the advantages of high density and low voltage operation. However, retention behavior of Mo nanocrystals embedded in SiN_x is too poor to be used in nonvolatile memory. In this section, we try to improve the memory characteristics of the Mo nanocrystal embedded in SiN_x by post ammonia plasma treatment.

5.2.2 Experiment

The memory-cells were fabricated on 6 inch p-type Si substrate. After the substrate was cleaned by standard RCA process, a 5-nm-thick dry oxide was grown at 950°C on the substrate in a horizontal furnace. An 8-nm-thick Mo silicate layer was then deposited on the oxide layer using co-sputtering Mo and Si in Ar (24 sccm)/N_2 (20sccm) ambience. 30-nm-thick Si oxide was deposited on the Mo silicate layer as the blocking oxide by plasma enhanced chemical vapor deposition at 300°C. Thermal annealing process was performed in N_2 ambience at 900°C 60s to form Mo nanocrystals embedded in SiN_x. Cells were subsequently treated with NH_3 plasma in PECVD chamber for 30 min with a NH_3 gas flow rate of 20 sccm and the chamber pressure of 67 torr at power of 50W. For electric characteristic measurement, 500-nm-thick Al was thermally evaporated with a shadow mask on the blocking oxide to form the metal-oxide-semiconductor structure. The microstructure of Mo nanocrystals was analysis through Transmission electron microscope (TEM). The chemical bonding and composition of the charge storage layer was analysis with X-ray photoemission spectroscopy (XPS). Electrical characteristics were measured using Keithley4200 and HP4284 Precision LCR meter with frequency of 1 MHz.

5.2.3 Result and discussion

In our previous study, we found that the surrounding nitride of Mo nanocrystal is deficiency (nitrogen deficiency). Figure 5-8(a) and (b) show XPS Mo 3*p* and N 1*s*, and Si 2*p* spectra of the charge storage layer without and with the plasma treatment, performed by a monochromatic Al *K*α (1486.6 ev) X-ray. In Fig. 6-8(a), the XPS peak at 394.0 ev and 397.8 ev are due to Mo—Mo bonds and Si—N bonds, respectively. Comparison of the intensity of Si—N bonds between samples with and without the plasma treatment, the intensity of Si—N bond for sample with the treatment is

stronger than that of sample without the treatment. The stronger intensity can be attributed to nitrogen incorporated into to the charge storage layer by NH_3 plasma. In Fig. 6-8(b), the peak position for the charge storage layer without plasma treatment at 100.1 ev is due to Si—N bond. The peak position moves toward the higher binding energy for the sample with the plasma treatment. According to the previous literature, the increase of the binding energy is due to more nitrogen binding with Si dangling bond which improve the quality of surrounding nitride [5.20].

Figure 6-9(a) and (b) show the *C-V* curves of MOS structure embedded with Mo nanocrystal for the sample with and without the plasma treatment, respectively. At the sweeping voltages of -6 to 4 V and -11 to 9 V, there are counterclockwise memory hystereses in Fig. 6-9(a) and 6-9(b). The counterclockwise hystereses are due to carrier transport through tunnel oxide between the charge storage layer and the Si substrate. We note that there is a 1.7 V reduction of the memory window for the sample with the plasma treatment. The reduction of the memory window after the treatment was related to the nitrogen passivation in charge storage layer. The deficient silicon nitride layer is widely used in SONOS memory. The traps in the nitride around nanocrystals can capture carriers contributing to the memory window. According XPS results, the nitrogen was incorporated into the nitride after the treatment. The incorporated nitrogen can passivate the traps in the silicon nitride, which reduce the charge storage centers in the surrounding dielectric, leading to the reduction of the memory window.

Figure 5-10 is a comparison of retention behavior for the samples with and without the plasma treatment, respectively. After programming, the memory window was obtained by comparing the *C-V* curves between the charged state and the quasi-neutral state. When carriers are stored in the nanocrystals, the stored carriers will raise the potential energy of the nanocrystals and increase the escaping

probability of stored carriers, which results in reduction of V_{FB} shift. For the sample without the plasma treatment, the flatband voltage shift decreases significant and return to quasi-neutral state at 10^3 sec, which indicates that the stored carriers was totally discharged from nanocrystals. In contrast, the charge loss rate of the sample after the treatment is slower than that without the treatment, and the stored carriers remain ~88.9%. For the stored carriers, there are three main discharging paths: discharging from nanocrystals to the control gate, discharging from one nanocrystal to the adjacent nanocrystal, and discharging from nanocrystals to the substrate. Because the control oxide is thicker than the tunneling oxide, discharging via the control oxide can be neglected. Furthermore, the tunnel oxide of the both samples is thermal growth in furnace at the same time, so the carriers discharging from nanocrystals to the substrate should have the same rate. However, the experimental results show the different lose rate of stored carriers between two samples. We considered that the obvious difference in the loss rate between both samples is due to the quality of surrounding nitride according to the XPS results. When carriers are storage in nanocrystals after programming, if there is an intrinsic defect chain in the tunnel oxide, the nanocrystal which aligns with the defect chain will be discharged immediately. Because the surrounding nitride is as thin as 3-nm, the carriers stored in the neighbor nanocrystals can easily escape to the discharged nanocrystal by trap assisted tunneling in the surrounding nitride, which results in a faster loss rate of the stored carriers. Since the quality of surrounding nitride in the sample without plasma treatment has much deficiency, the stored carriers can leak out of nanocrystal by lateral migration. For the sample with the plasma treatment, the traps in the surrounding nitride were reduced by nitrogen passivation. The trap assisted lateral migration of the stored carriers was suppressed, which improves the retention of the memory structure.

5.2.4 Conclusion

In conclusion, the nonvolatile memory characteristics of the Mo nanocrystals were influenced by the ammonia plasma treatment. The *C-V* hysteresis reduced from 9.5 to 7.8 V due to reduction of trapping centers in the surrounding nitride. The retention characteristic improved from 0% to 89.9% remaining charges after the plasma treatment because the carriers' lateral migration between nanocrystals was suppressed through the nitrogen passivation of the traps in the surrounding nitride. The plasma-treated Mo nanocrystal embedded in nitride layer with high density (6×10^{12} cm^{-2}) and good retention can be application in nanocrystal nonvolatile memory.

5.3 Comparison of memory characteristics of Mo nanocrystal embedded in SiO_x and SiN_x

5.3.1 Introduction

In the chapter 4, we investigated the nonvolatile memory characteristics of the Mo nanocrystal embedded in SiO_x and SiN_x. The results indicated the Mo nanocrystal embedded in SiN_x has larger memory window than Mo in SiO_x. However, poor retention behavior of Mo nanocrystal in SiN_x made us proceed to enhance the charge storage ability by ammonia plasma treatment. The results show a significant improvement on retention behavior although the Mo nanocrystal in SiN_x sacrifices 1.7 V memory window.

In this section, we will compare the memory characteristics between ammonia plasma treated Mo nanocrystal in SiO_x and SiN_x. The results will be explained through electrical simulation on both memory structures.

5.3.2 Results and discussion

Fig. 5-11 show the memory window of the Mo nanocrystal embedded in SiO_x and SiN_x. The memory window for the Mo nanocrystal in SiO_x is around 3.0 V under -11 to 9 V sweeping voltage. In contrast, the memory window of the Mo nanocrystal in SiN_x is around 7.8 V. The larger memory window can be attributed to the high density of nanocrystal. During the voltage sweeping, carriers can inject from substrate to the nanocrystal and then capture by nanocrystals. The memory window can be calculated from the total stored charges divided by capacitance of control oxide. If one nanocrystal can capture one electron during the sweeping voltage, the total of the stored carriers per unit cell for the higher density of nanocrystal are larger than that for the lower one. This results in larger memory window for Mo nanocrystal in SiN_x than that for Mo nanocrystal in SiO_x.

Figure 5-12 is the retention characteristics before and after 10^6 program/erase (P/E) cycles for both samples. The program/erase voltage is 15/-15 V for 10ms. In Fig. 5-12(a), the remaining charges of Mo nanocrystal embedded in SiO_x is 87.9% before the P/E cycles, which is approximation to the 88.9% remaining charges for Mo nanocrystal in SiN_x. After the P/E cycles, the remaining charges is 71.9% for the Mo in SiO_x. The retention characteristic of Mo in SiO_x has 16% degradation. In contrast, the retention of Mo in silicon nitride has only 8% degradation. These results indicated that Mo nanocrystal embedded in SiN_x layer as the charge storage layer has better reliability than Mo nanocrystal in SiO_x. The better retention characteristic of Mo in SiN_x can be explained by electric field simulation for both structures. Figure 6-13(a) shows electrical field distribution in the memory structure. Figure 6-13(b) is the electrical field characteristics along the Y-axis at the center of nanocrystal. It can be found that the maximum electrical field for the Mo embedded in oxide is 3.76 MV/cm. However, the electrical field for the Mo embedded in nitride is 2.96 MV/cm. During P/E cycles, the larger electrical field indicates that higher number of carriers transport

between nanocrystal and substrate resulting in a significant degradation on tunnel oxide. Therefore, the retention of Mo in oxide is poor than Mo in SiN_x.

5.3.3 Conclusion

Memory characteristics of Mo nanocrystal embedded in SiO_x and SiN_x was investigated in this section. Table 5-3 concludes the Memory characteristics of Mo nanocrystal embedded in SiO_x and SiN_x. The memory window can be enhanced by Mo nanocrystal embedded in SiN_x. The larger memory for the Mo nanocrystal in SiN_x can be attributed to the higher density of nanocrystal. The retention after 10^6 P/E cycles has 16% and 8% degradation for the Mo nanocrystal in SiO_x and SiN_x, respectively. The larger memory window and better reliability of high density Mo nanocrystal embedded in SiN_x can be application in next generation nonvolatile memory.

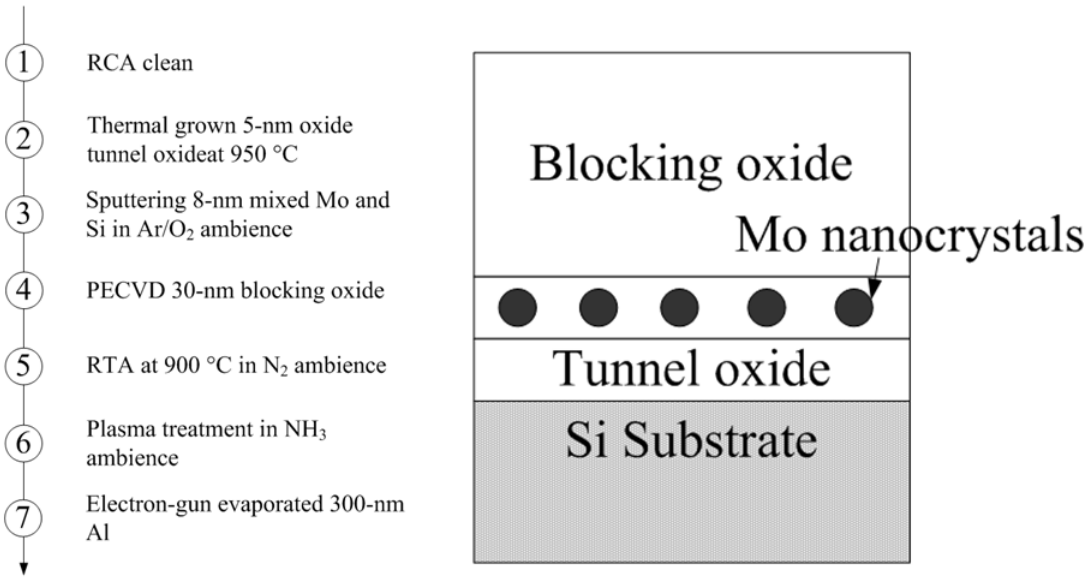


Figure 5-1 Process flow and structure of plasma treated Mo nanocrystal memory.

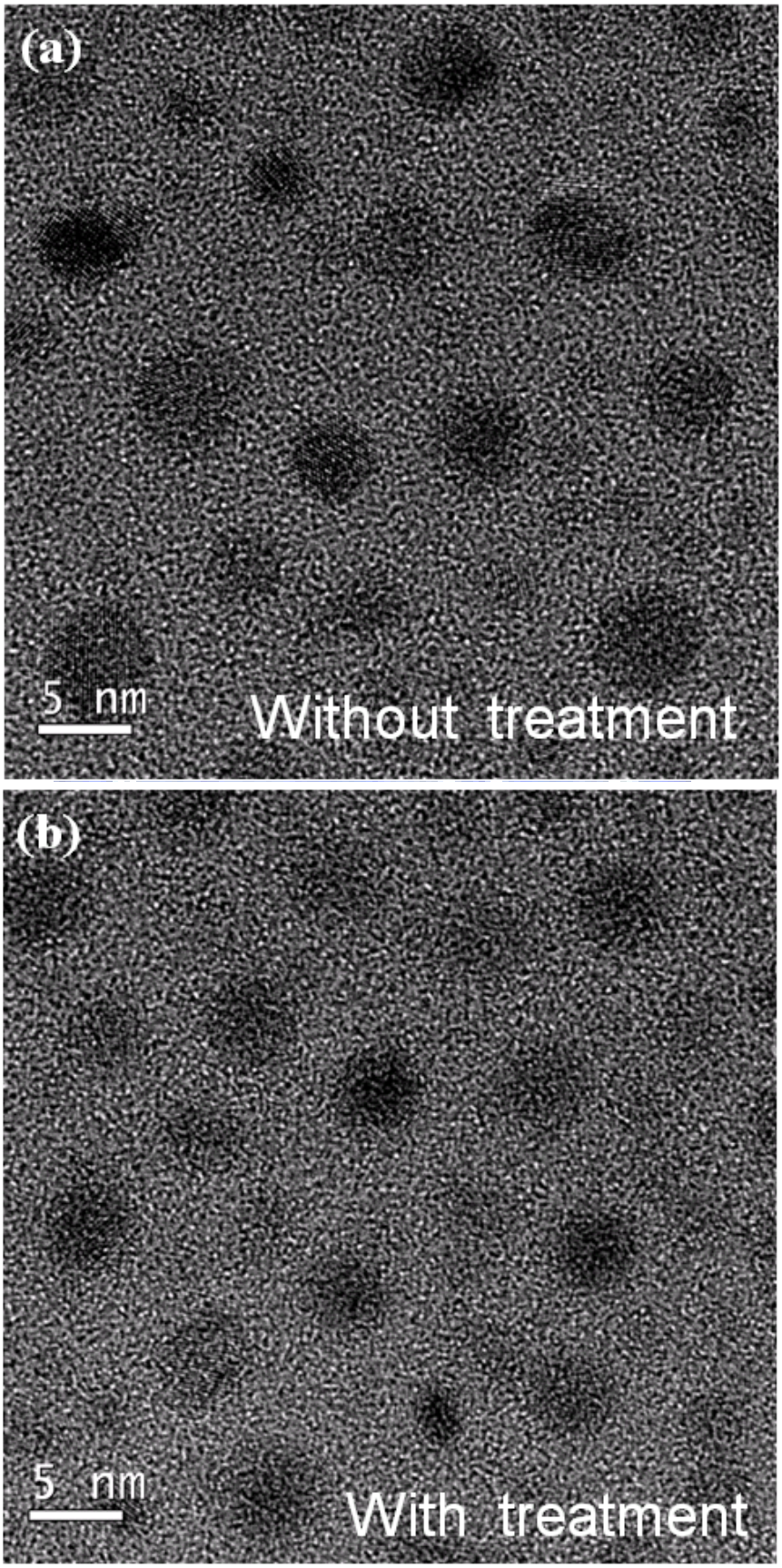


Figure 5-2 Plane-view TEM of Mo nanocrystal memory (a) without and (b) with NH_3 plasma treatment.

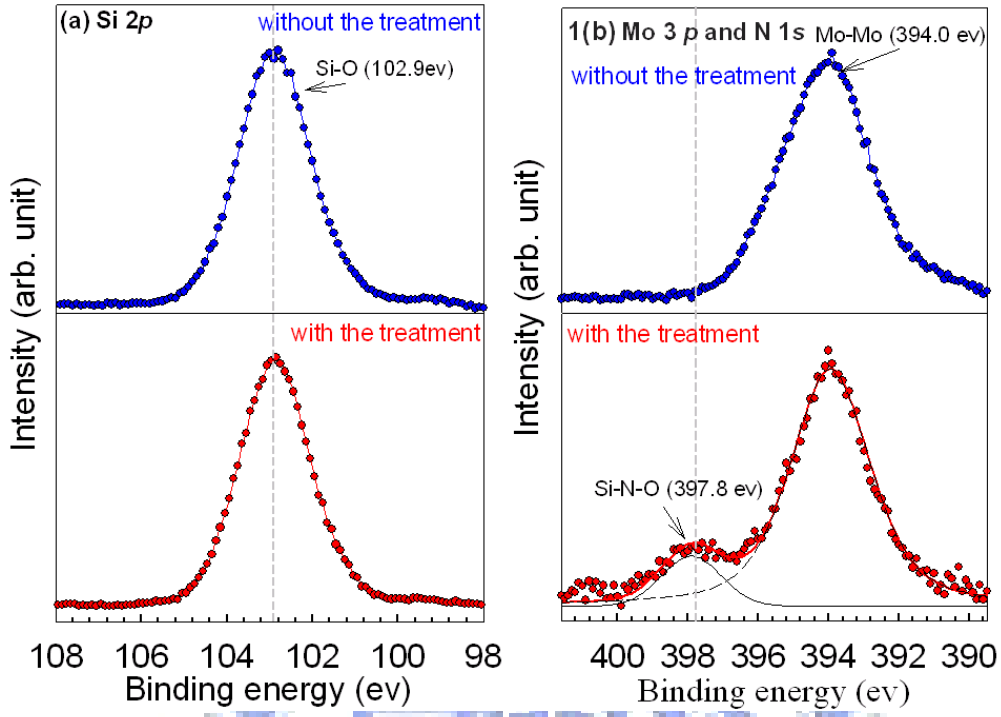


Figure 5-3 XPS (a) Si 2p, and (b) Mo 3p and N 1s spectra of oxygen-incorporated Mo silicide layer with and without plasma treatment.

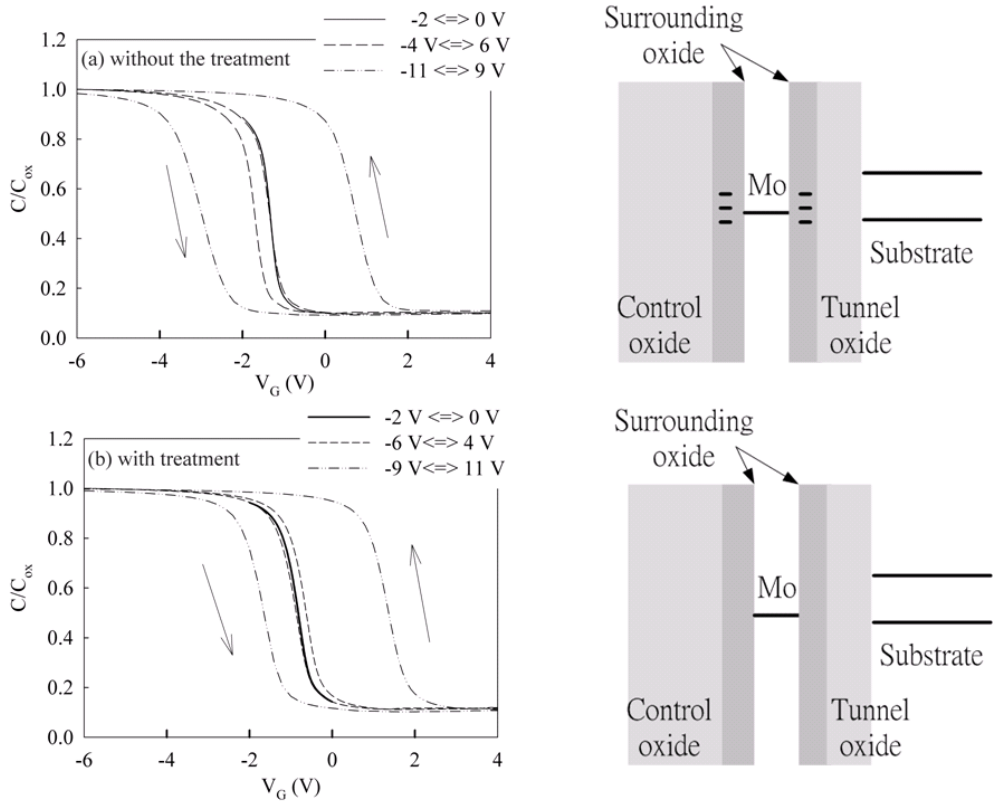


Figure 5-4 C-V characteristics and band diagram of Mo nanocrystal memory (a) without and (b) with NH_3 plasma treatment.

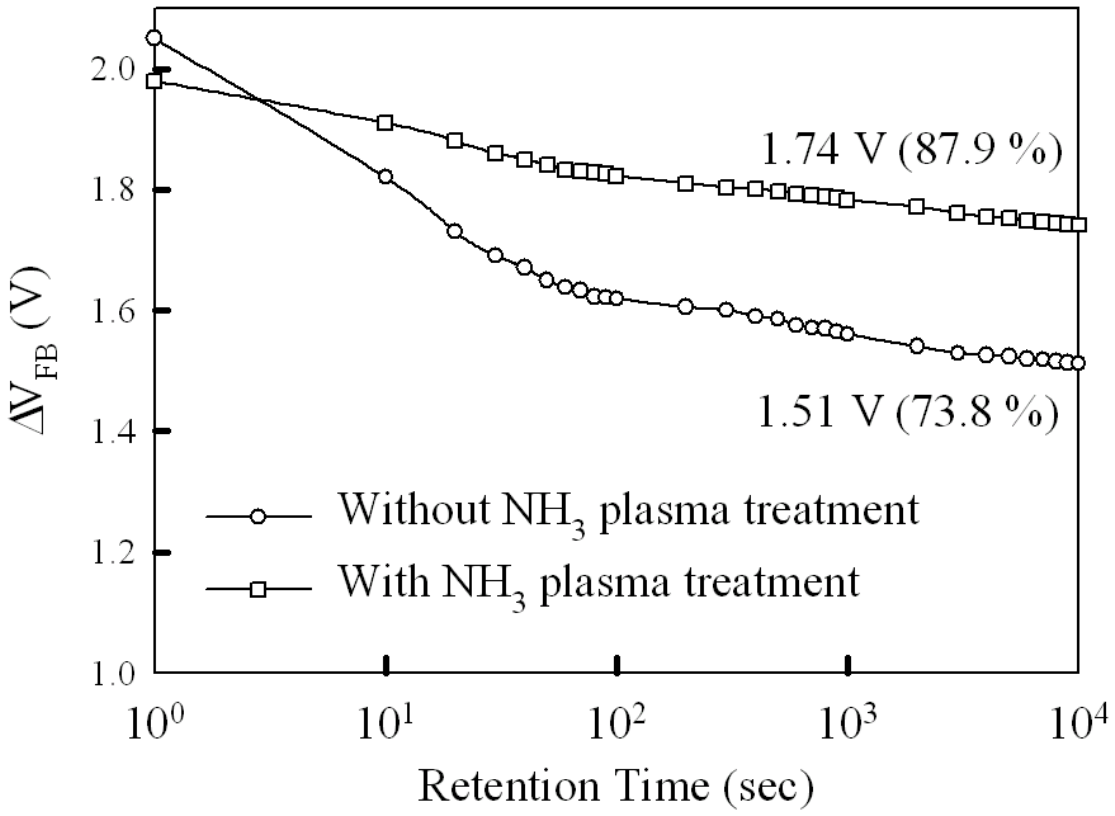


Figure 5-5 Comparison of retention behavior of Mo nanocrystal memory with and without plasma treatment.

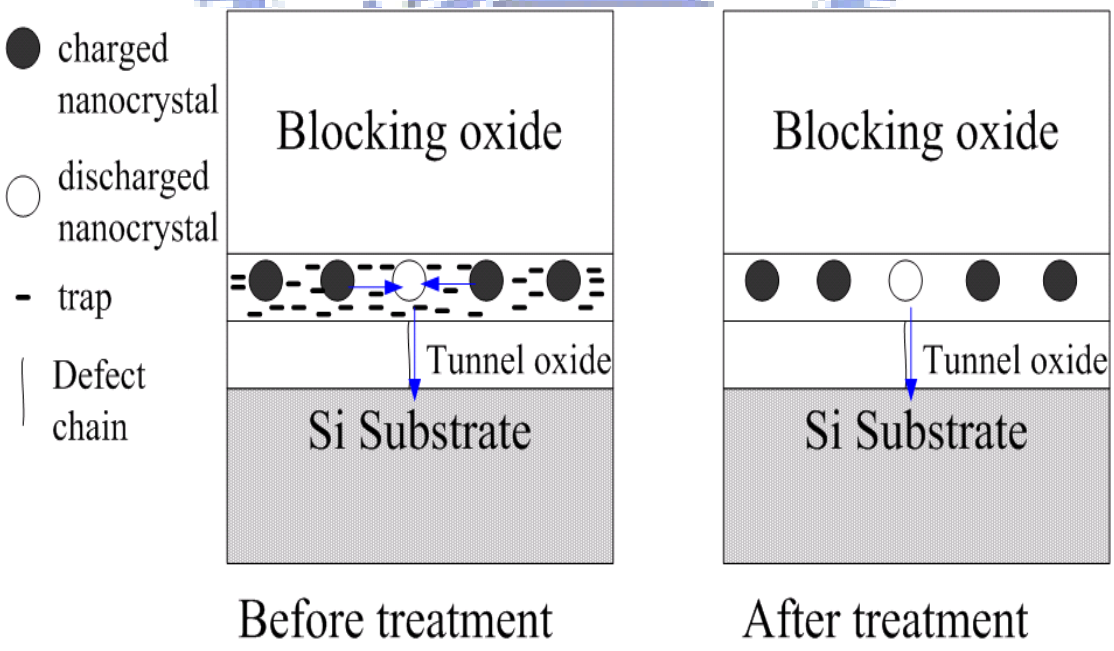


Figure 5-6 Schematically explanation of difference in retention behavior between nanocrystal memory (a) without and (b) with plasma treatment.

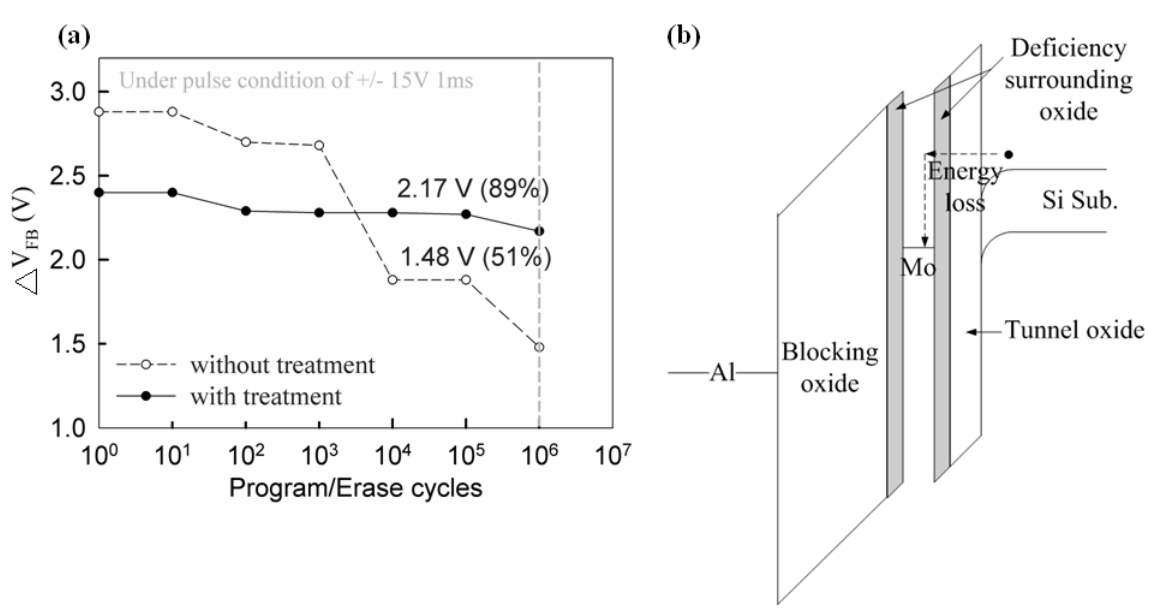
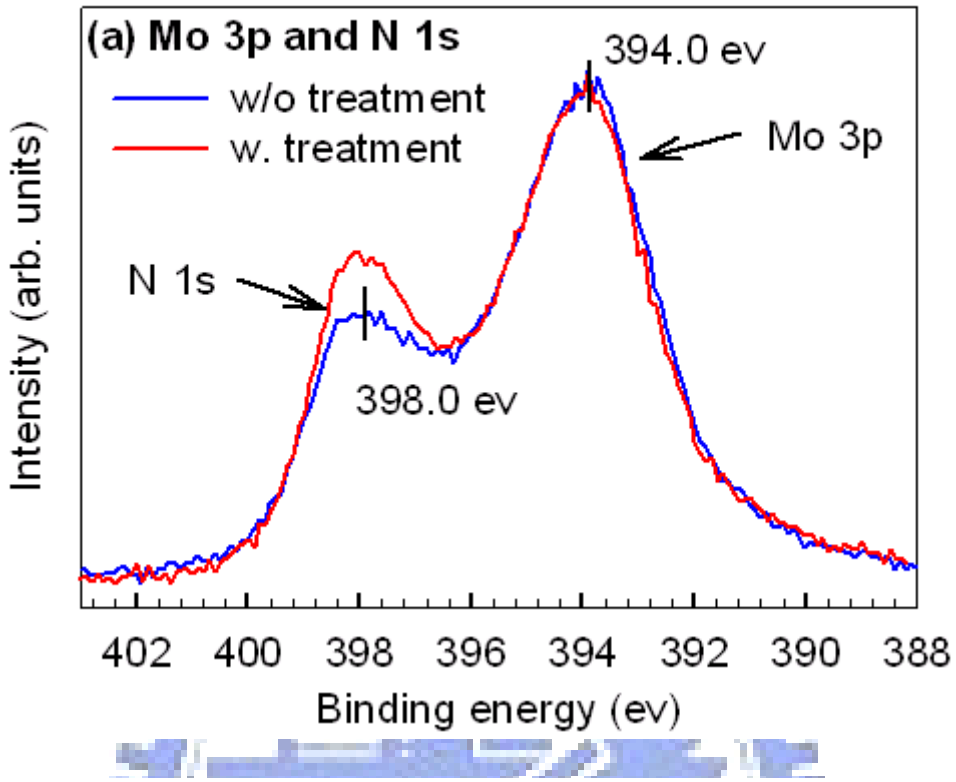


Figure 5-7 (a) Comparison of endurance characteristics of Mo nanocrystal memory with and without plasma treatment. (b) Band diagram of Mo nanocrystal memory during programming.

	Mo in SiOx (STD)	Mo in SiOx (NH_3)
Memory window	3.6 V	3 V
Retention	73.8%	87.9%

Table 5-1 Comparison of memory characteristics for Mo nanocrystal in SiO_x without and with plasma treatment



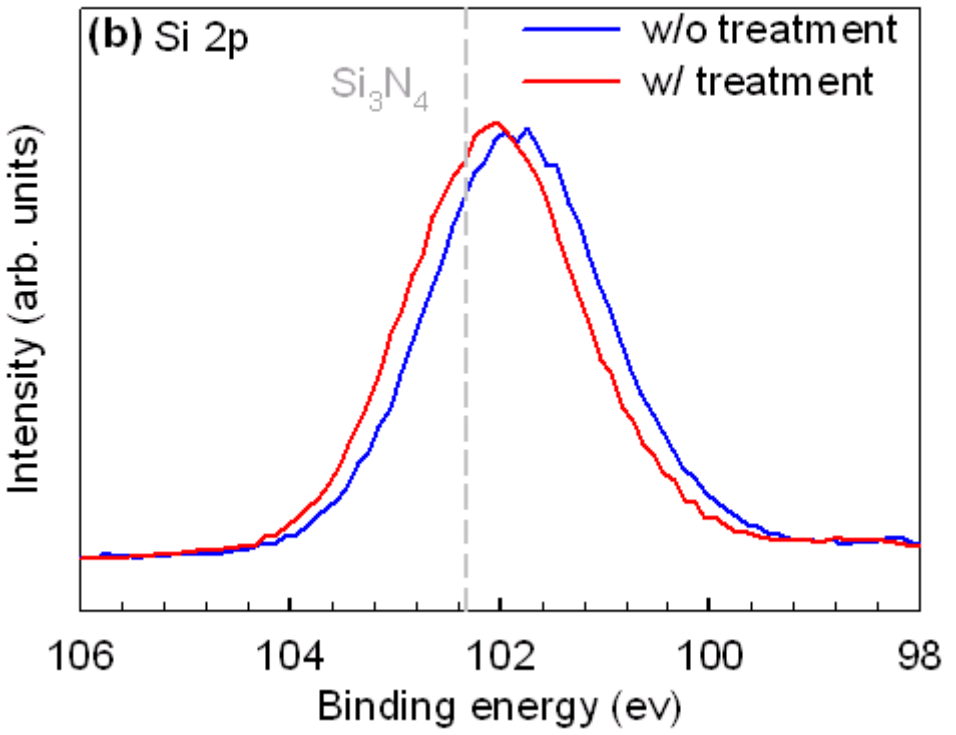


Figure 5-8 XPS (a) Mo 3p and N 1s, and (b) Si 2p spectra of nitrogen incorporated Mo silicide layer.

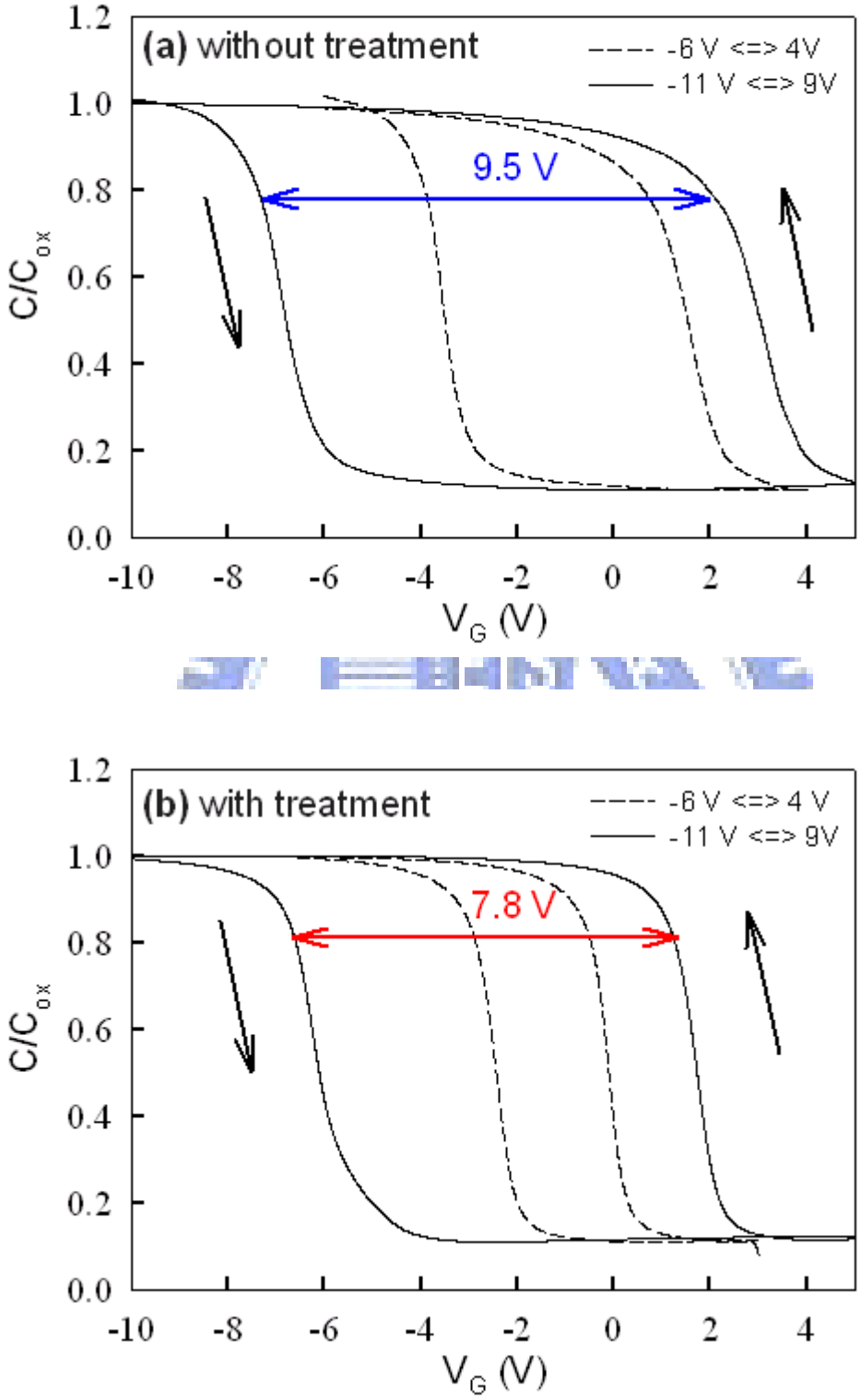


Figure 5-9 C-V characteristics at various sweeping voltage for Mo nanocrystal memory (a) without and (b) with plasma treatment.

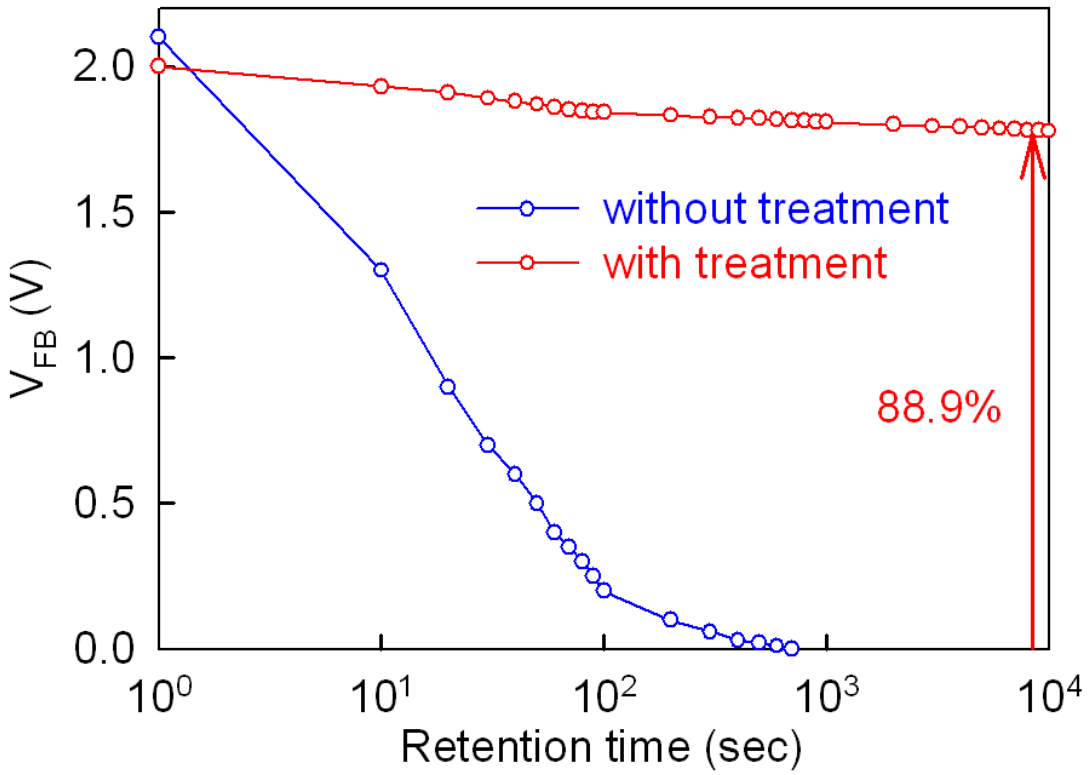


Figure 5-10 Comparison of retention behavior between the Mo nanocrystal memory without and with plasma treatment.

	Mo in SiNx (STD)	Mo in SiNx (NH3)
Memory window	9.5 V	7.8 V
Retention	0%	88.9%

Table 5-2 Comparison of memory characteristics for Mo nanocrystal in SiN_x without and with plasma treatment

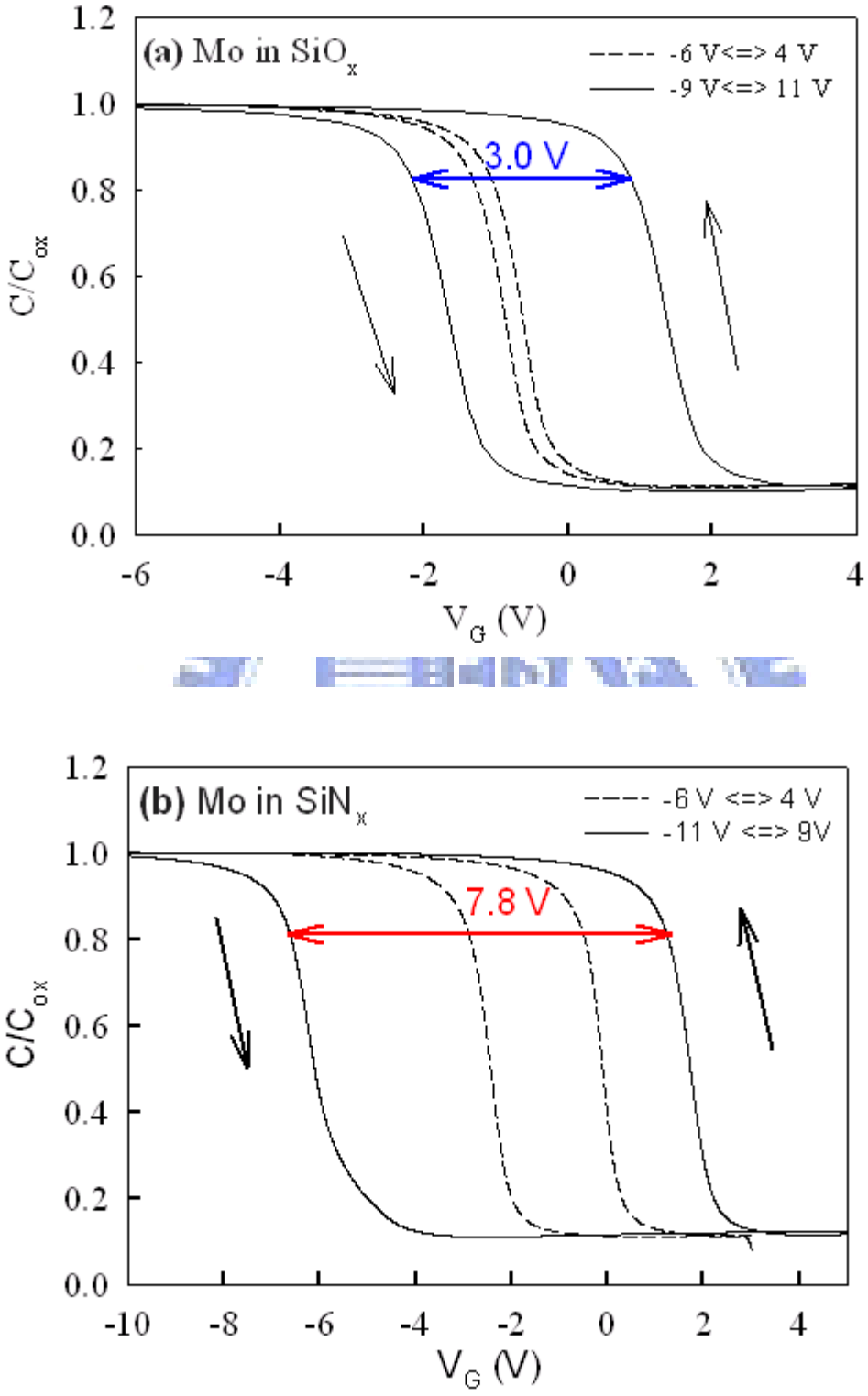


Figure 5-11 C-V hysteresis characteristic of (a) Mo in SiO_x and (b) Mo in SiN_x after NH_3 plasma treatment.

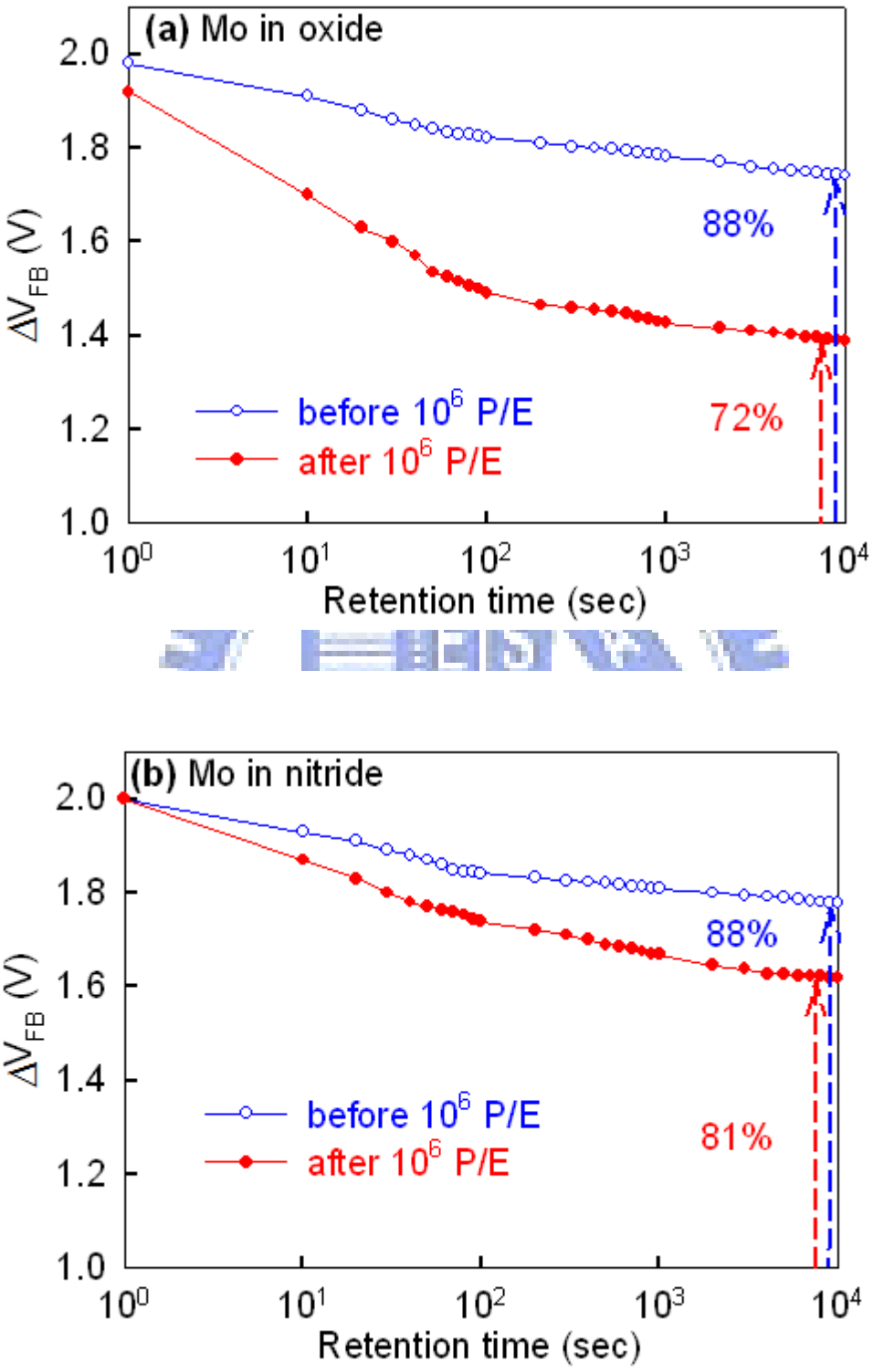


Figure 5-12 Retention behavior of Mo nanocrystal in (a) SiO_x and (b) SiN_x before and after 10^6 program/erase (P/E) cycles.

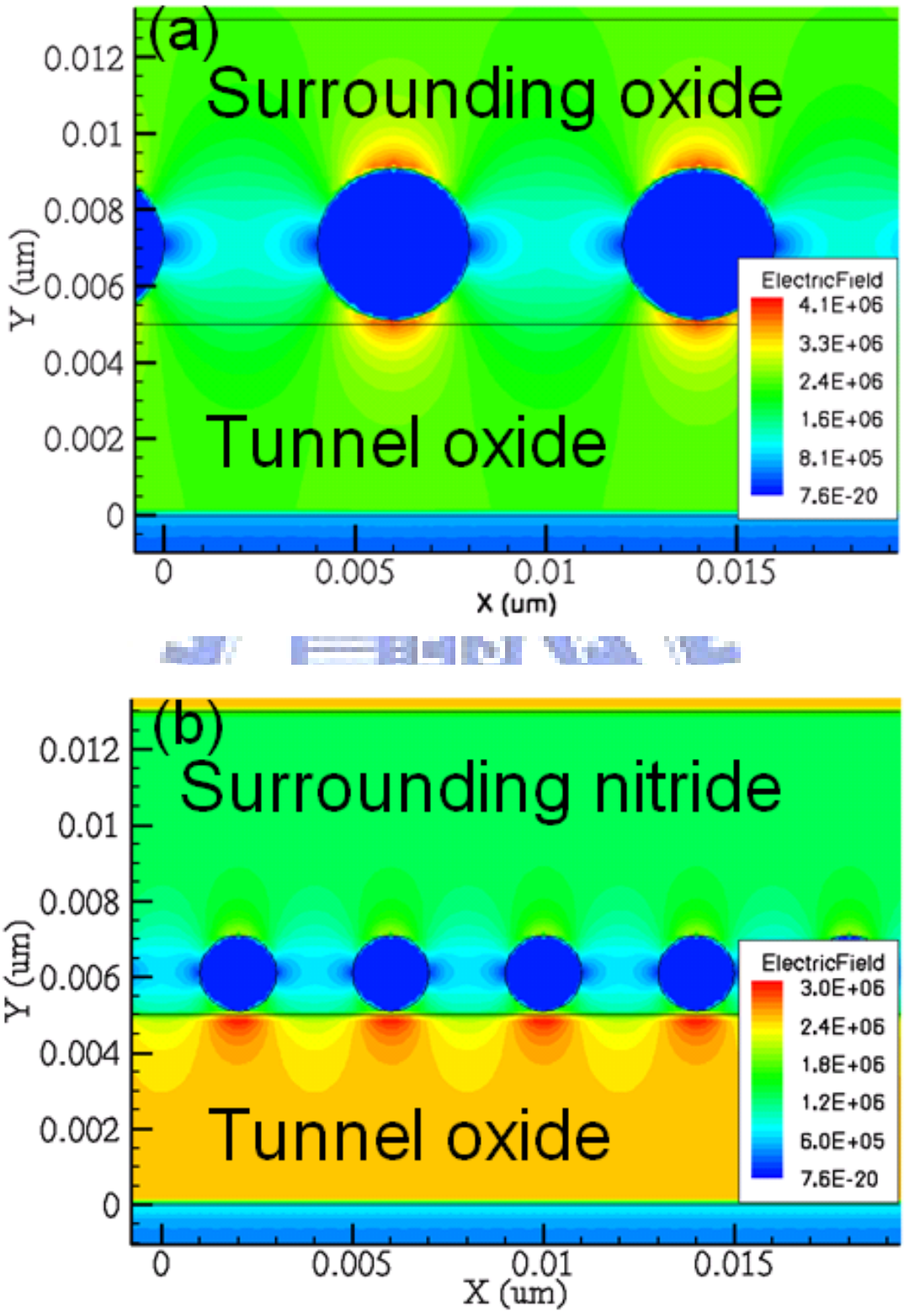


Figure 5-13 Simulation structure and electrical field distribution of Mo nanocrystal embedded in (a) SiO_x and (b) SiN_x.

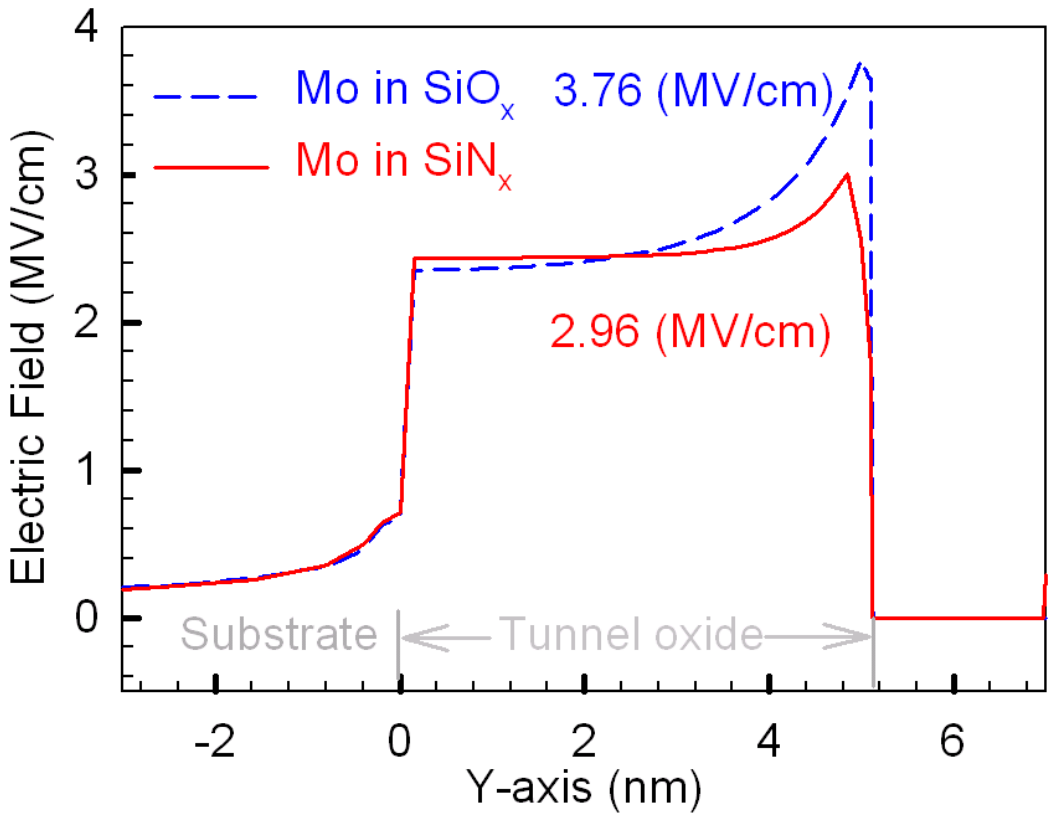


Figure 5-14 Electrical field distribution along Y-axis crossing the Mo nanocrystal in SiO_x and in SiN_x.

	Mo in SiO_x (NH_3)	Mo in SiN_x (NH_3)
Memory window	3.0 V	7.8 V
Retention	88%	89%
Retention after 10^6 P/E cycles	72%	81%

Table 5-3 Comparison of memory characteristics for Mo nanocrystal in SiO_x and SiN_x after NH_3 plasma treatment.

Chapter 6

Nanocrystal technique application in Resistive Switching Memory

6.1 Introduction

In recent years, the RRAM using transition metal oxide is paid much attention for the academia and industry. Because the RRAM combined with the speed of static random access memory (SRAM), density of dynamic random access memory (DRAM), and nonvolatile characteristic of flash memory, it has potential to be the next-generation nonvolatile memory. The basic RRAM is the Metal/Insulator/Metal (MIM) structure and its memory effect is operated by using an extra electric field to change the resistance of transition metal oxide (resistance switching layer). This result will appear reversible transformation between high and low resistance to define the data information for memory operation. Because the RRAM is a back-end process, it can be easily integrated into the current memory process to realize the System on Chip (SoC) or System in Package (SiP) applications [16, 28-29]. However, resistance switching memory still faces an issue about variation of device parameter such as switching voltage, on-state and off-state current.

In this section, we try to stabilize the device parameter of resistance switching memory by embedding nanocrystal. We fabricated the Ni nanocrystal embedding in aluminum oxide. The aluminum oxide was used as resistance switching layer. We found that Ni nanocrystals can influence characteristics of resistance switching in aluminum oxide.

6.2 Experiment

The experimental process flow and memory structure is shown in Figure 6-1. The memory-cells were fabricated on 6 inch *p*-type Si substrate with 300-nm buffer oxide, which was used to electrically isolate the substrate and bottom electrode. After the substrate was cleaned with standard RCA process, 300-nm-thick wet oxide was grown at 980°C on the substrate in a horizontal furnace. An 20-nm-thick Ti layer was deposited on the oxide layer using sputtering Ti target as a adhesion layer. Afterward, 80-nm-thick Pt layer were deposited on $Ti/SiO_2/Si$ substrate as bottom electrode. 35-nm-thick Aluminum oxide as resistance switching layer embedded with or without 6-nm-thcik oxygen incorporated Ni silicide layer was deposited on the Pt layer by electron-gun evaporation. The Ni silicide layer was deposited by sputtering mixed Ni and Si target in Ar/O_2 ambience. The thermal annealing process was performed in N_2 ambience at 300, 500, and 700°C for 150s to form Ni nanocrystals embedded in SiO_x. For electric characteristic measurement, 200-nm-thick Ti was thermally evaporated with a shadow mask on the aluminum oxide to form the metal-insulator-metal (MIM) structure. Nanostructure of Ni nanocrystals was analyzed through transmission electron microscopy (TEM). Chemical bonding and composition of the resistance switching layer was analyzed with X-ray photoemission spectroscopy (XPS). Electrical characteristics were measured using Keithley4200 meter.

6.3 Result and discussion

Figure 6-2 shows the TEM analyses for the MIM structure embedded with oxygen-incorporated Ni silicide layer annealing at various temperatures. In Figure 6-2(a), the thicknesses of aluminum oxide and oxygen-incorporated Ni silicide layer are about 35-nm and 6-nm, respectively. It can be seen that oxygen-incorporated Ni silicide layer was agglomerated into spheres after annealing at temperature up to 500°C [Fig. 6-2(c)]. The high resolution image in the inset of Fig. 6-2(c) shows lattice

image of a sphere indicating that Ni was crystallization after the annealing. The aluminum oxide was crystallization after annealing at 700°C [Fig. 6-2(d)]. To calculate the average size and density of nanocrystals, plane-view TEM analyses were performed. The average size and density of nanocrystals are about 4-nm and 10^{12} cm^{-2}, as shown in Fig. 6-3.

Figure 6-4 shows XPS Al 2*p* spectra of the aluminum oxide layer annealing at various temperatures, which was performed by using a monochromatic Al *K*α (1486.6 ev) X-ray. It can be seen in Fig. 6-4(a) that the position of XPS peak for as-deposited aluminum oxide is about 73.78 ev deviating from the peak position of Al_2O_3 (74.5 ev). After annealing, the peak position is shift toward to higher binding energy as shown in Fig. 6-4(b). The XPS results indicate that as-deposited aluminum oxide is more deficient with oxygen vacancy than the aluminum oxide after annealing process because it was deposited at low temperature environment.

Figure 6-5 depicts the current-sweeping voltage (I-V) characteristics for twenty cycles in aluminum oxide annealing at 500°C, and in aluminum oxide embedded with oxygen-incorporated Ni silicide layer annealing at various temperatures. I-V characteristics were measured by dual sweeping with a sequence of sweeping voltage from 0 V to -2 V, -2 V to 0 V, 0 V to 2 V and 2 V to 0 V as indicated by a sequence of numbers on arrow in Fig. 6-5. During the switching from low to high conducting current, a compliance on current (5 mA) of the device is need to prevent sample from being broken by electrical damage (arrowhead 4 to 6). The resistive switching phenomenon is that the conductivity of the memory device can be altered by sweeping voltage over than a specific voltage, which is reproducible. It can be seen that the I-V of as-deposited sample shows a high-conducting current and cannot be switched to low conducting current by sweeping voltage. However, for the 300°C-annealed sample with the oxygen-incorporated silicide layer, and the

500°C-annealed sample with and without Ni nanocrystal, their initial state are in the high conducting current (ON-state) and switched to low conducting current (OFF-state) after sweeping voltage from 0 to -2 V (arrowhead 1 to 3 indicated in Fig. 6-5), and the state is recovery to ON-state after sweeping voltage from 0 to 2 V (arrowhead 4 to 6). It can be seen that the variation of the high- and low-conducting current, and V_T (the voltage at current switching from low to high, arrowhead 5) are large in the 300°C-annealed sample with the oxygen-incorporated silicide layer, and the 500°C-annealed sample without the oxygen-incorporated silicide layer. In contrast, I-V characteristic of the sample with Ni nanocrystals have a stable switching characteristics; that is the conducting states and set voltage of sample with Ni nanocrystal shows a smaller variation.

Figure 6-6 is the I-V characteristics of sample with NCs after I-V of negative sweeping is folded to positive one. It can be seen that the I-V characteristics is symmetry at a large range of sweeping voltage indicating that the carrier transport in the sample is independent on electrode. This indicates that carrier transport in the sample should be dominated by bulk conduction. The double-logarithmic scale plots of the I-V curves for both positive and negative sweeping region in the Ti/Al_2O_3/Ni NCs/Al2O3/Pt device are indicated in Fig. 6-7. In negative sweeping region of ON-state, the high conducting current in the device indicates the existence of the high conducting path in the device, and Ohmic conduction is observed. Then, a sequence of decreases is observed in conducting current, causing by rupturing the conducting path, and SCLC appears in bias decreasing sweeping. In the smaller bias region for negative sweeping of OFF-state, Ohmic conduction is observed due to thermal free carriers exceeding the injected ones. For process of resistive switching from OFF- to ON-state in positive sweeping region, the conduction mechanism obeys Ohmic in low bias region followed by SCLC in high bias region. At bias larger than V_T, the device

switching to ON-state due to formation of high-conducting paths. The conducting mechanism, again, obeys Ohmic in positive bias region of ON-state.

For the stabilization of I-V characteristics of the device embedded with Ni nanocrystals, Fig. 6-8 depicts a simple band diagram at ON-state of negative bias. According to XPS results and above discussion, the high conducting current in Al_2O_3 is possible due to formation of a defect band for current conduction. During the carrier conduction in the memory device, the carriers can be more easily transport through nanocrystals which act as short path [Fig. 6-8(a)] than through 6-nm thick surrounding oxide [Fig.6-9 (b)]. Furthermore, as shown in Fig. 6-9, the electrical field simulation indicates that the max electrical field across nanocrystal is twice larger than across surrounding oxide between nanocrystals. We consider that the stabilization of memory device embedded with nanocrystals is that nanocrystals can fix high-conducting paths across nanocrystals, as shown in Fig. 6-9. However, for the memory device without embedded with nanocrystals, the formation of high-conducting paths should be randomly, resulting in large variation of memory switching parameter.

Figure 6-10 show the retention behavior of the memory device embedded with nanocrystals. It can be seen that the conducting current between ON- and OFF-state is larger than 2 orders, and is stable even after 10^5 retention time. This indicates the memory device is possible to be application in non-volatile memory.

6.4 Conclusion

Nonvolatile memory characteristics of Ti/Al oxide/Pt embedded with Ni nanocrystals were investigated in this section. The cross-section TEM results indicates that the formation of Ni nanocrystal after annealing oxygen-incorporated Ni silicide layer at 500°C. The plane-view TEM indicates the average size and density of the

nanocrystals are about 4-nm and 10^{12} cm^{-2}. The The XPS results indicate the Al oxide layer is deficiency. The conducting mechanism of ON-state in the device is dominated by Ohmic and the conducting mechanism of OFF-state in the device is Ohmic in low bias region and SCLC in high bias region. The memory characteristics including ON- and OFF-states current, and switching voltage can be stabilize by embedding nanocrystals in to the device because conducting-path can be fixed across nanocrystals instead of random formation in device without nanocrystals. The ON- and OFF-state is stable during retention test. The proposed device structure can be application in next generation nonvolatile memory.

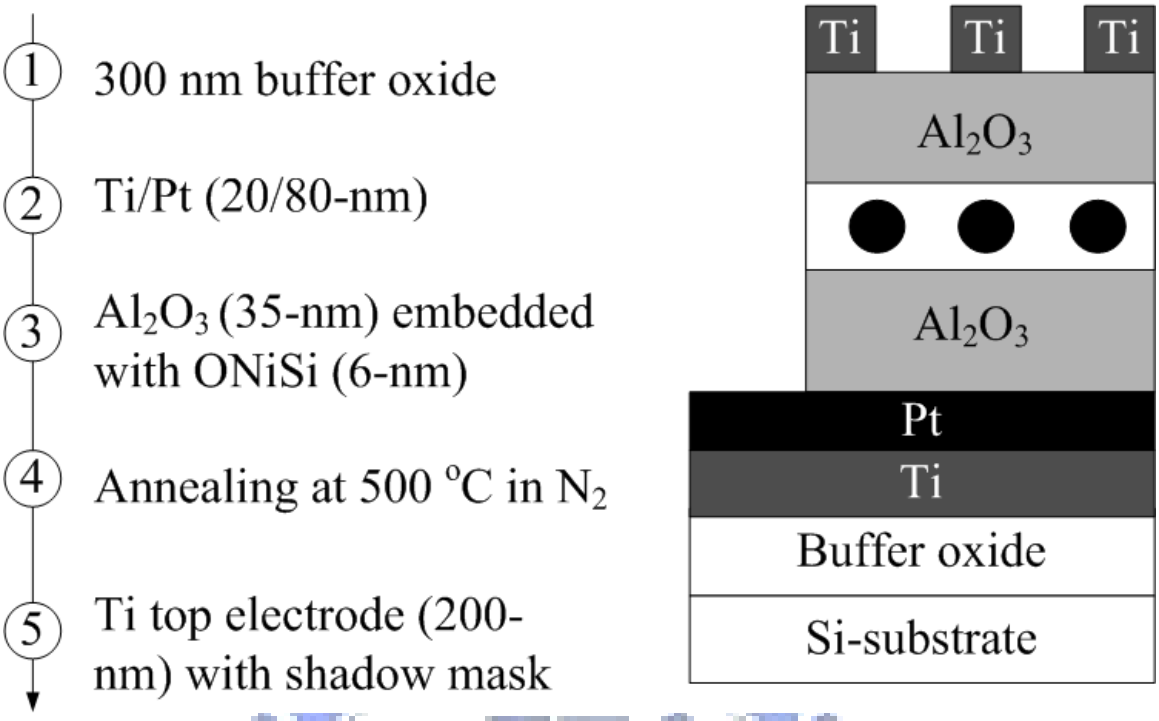
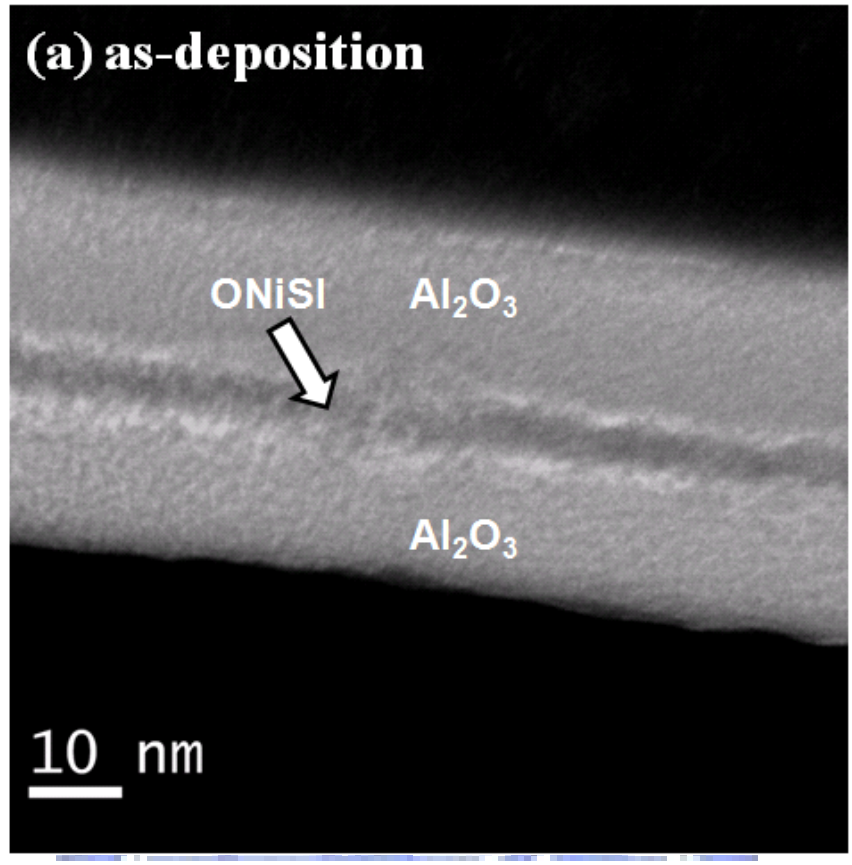
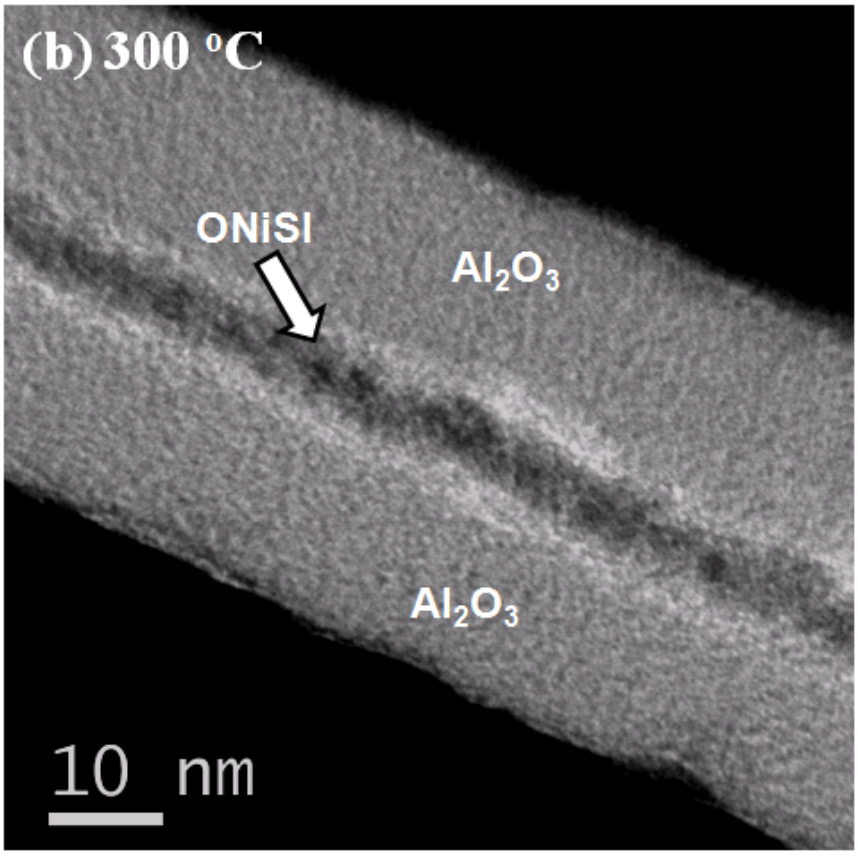


Figure 6-1 Process flow and structure of RRAM embedded with Ni nanocrystals


(a) as-deposition
ONiSI
Al_2O_3
Al_2O_3
10 nm


(b) 300 °C
ONiSI
Al_2O_3
Al_2O_3
10 nm

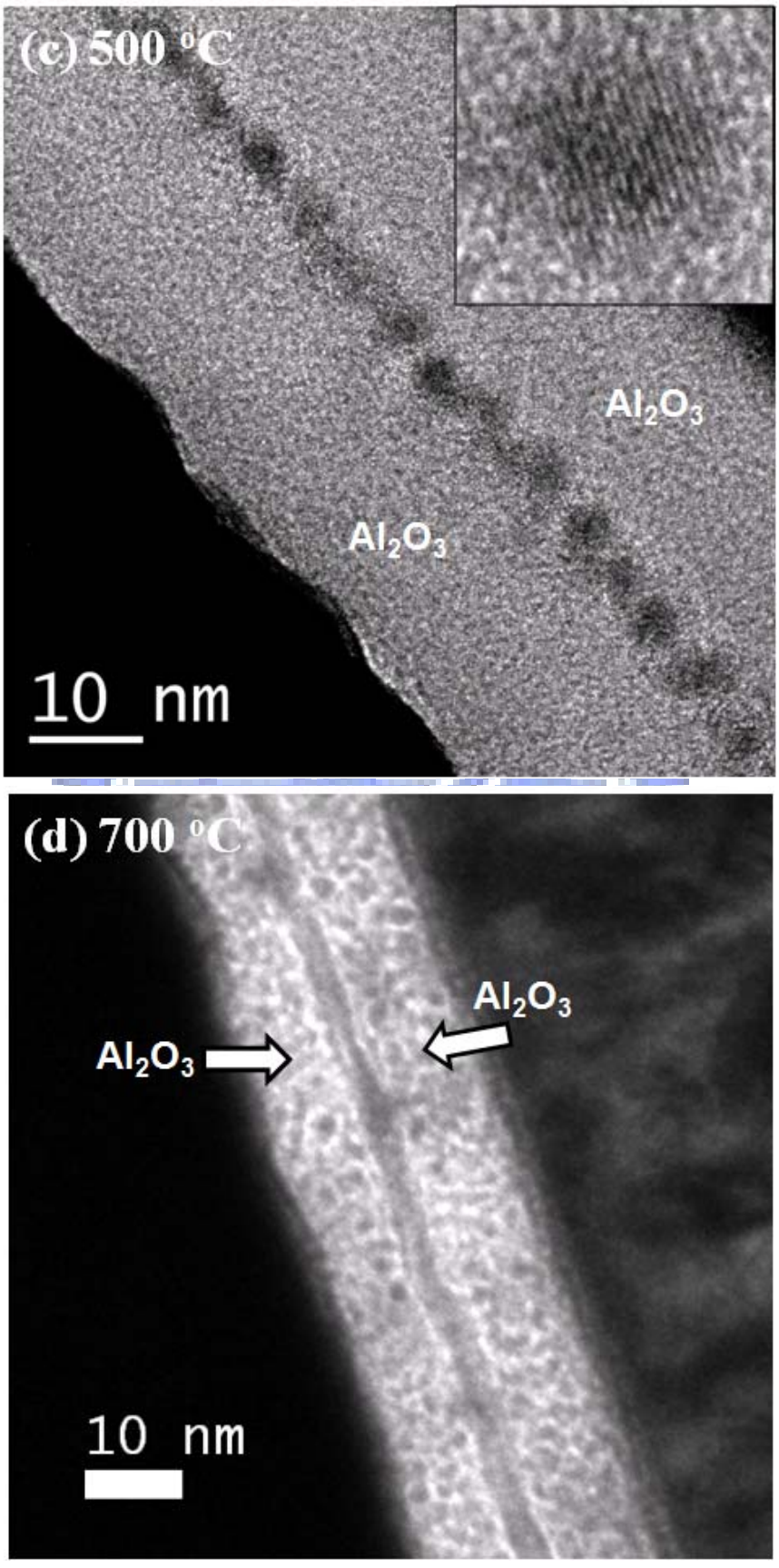


Figure 6-2 Cross-section TEM analyses of Ti/ Al_2O_3/Ni silicide/ Al_2O_3/Pt structure for (a) as-deposited, and after annealing at (b) 300°C, (c) 550°C and (d) 700°C

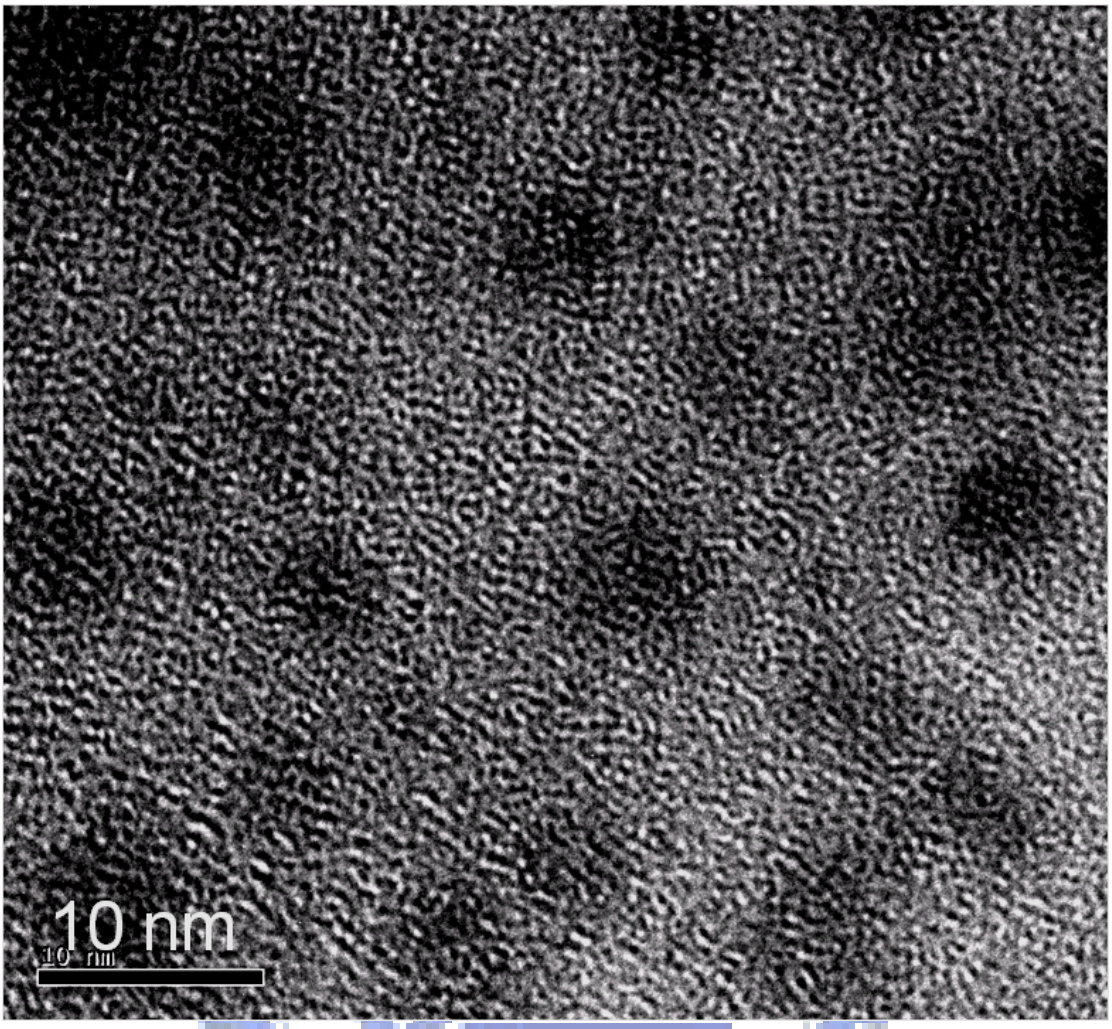


Figure 6-3 plane-view TEM analyses for Al_2O_3/Ni silicide/Al_2O_3 structure after annealing at 500°C

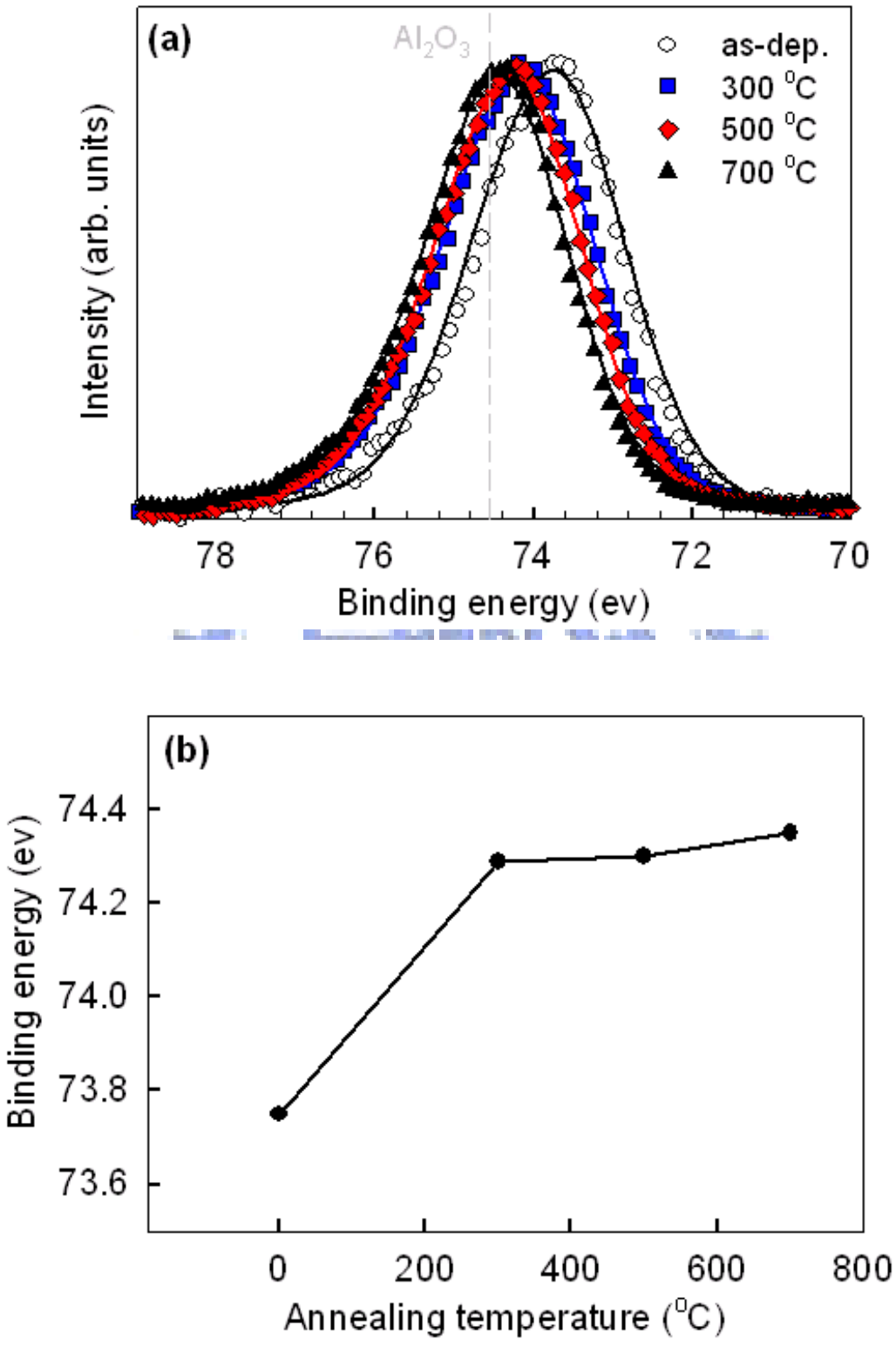
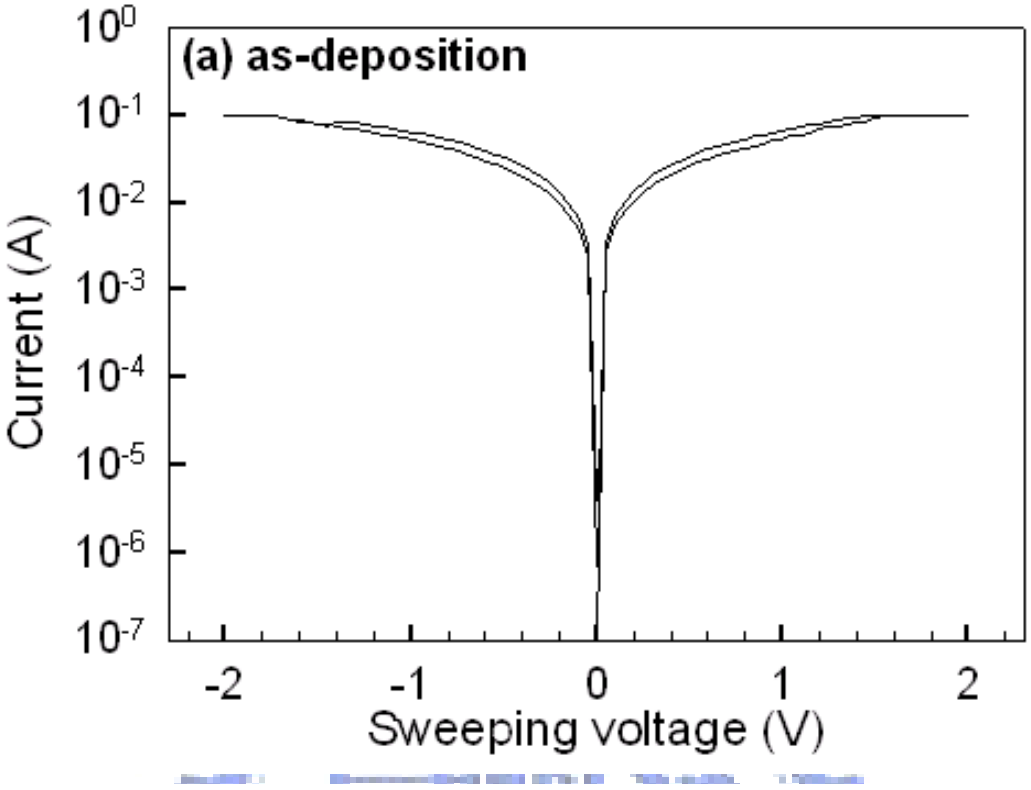
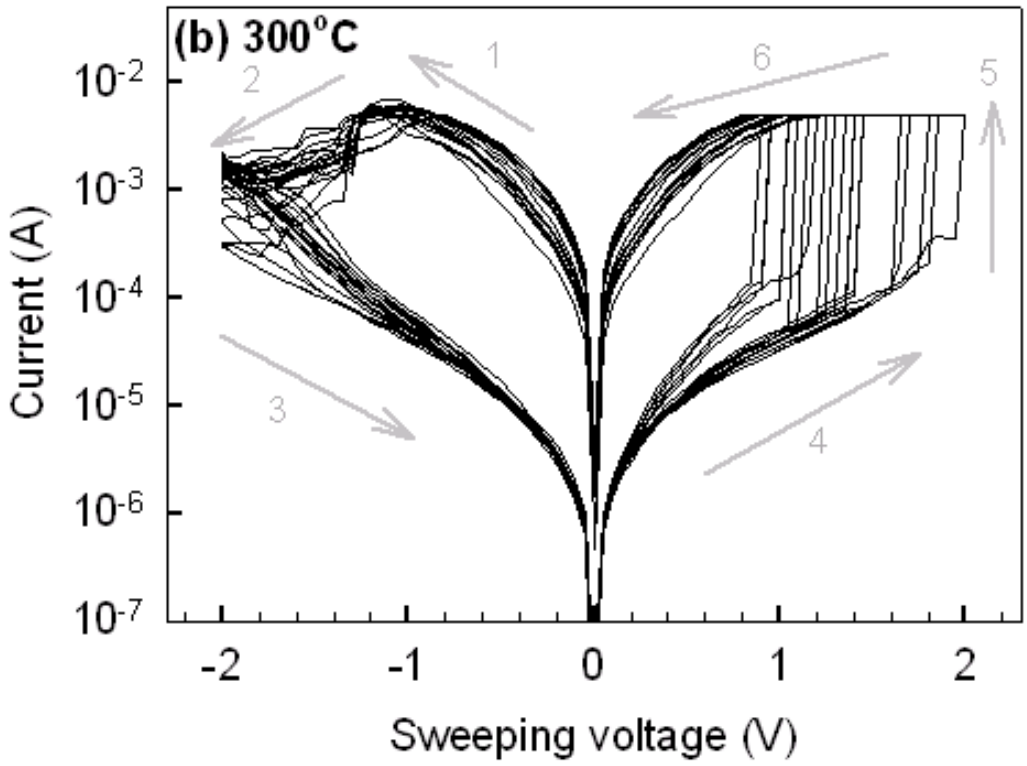


Figure 6-4 XPS Al 2p spectra at various annealing temperature (a) and binding energy shift (b).


(a) as-deposition
Current (A)
Sweeping voltage (V)


(b) 300°C
1
2
3
4
5
6
Current (A)
Sweeping voltage (V)

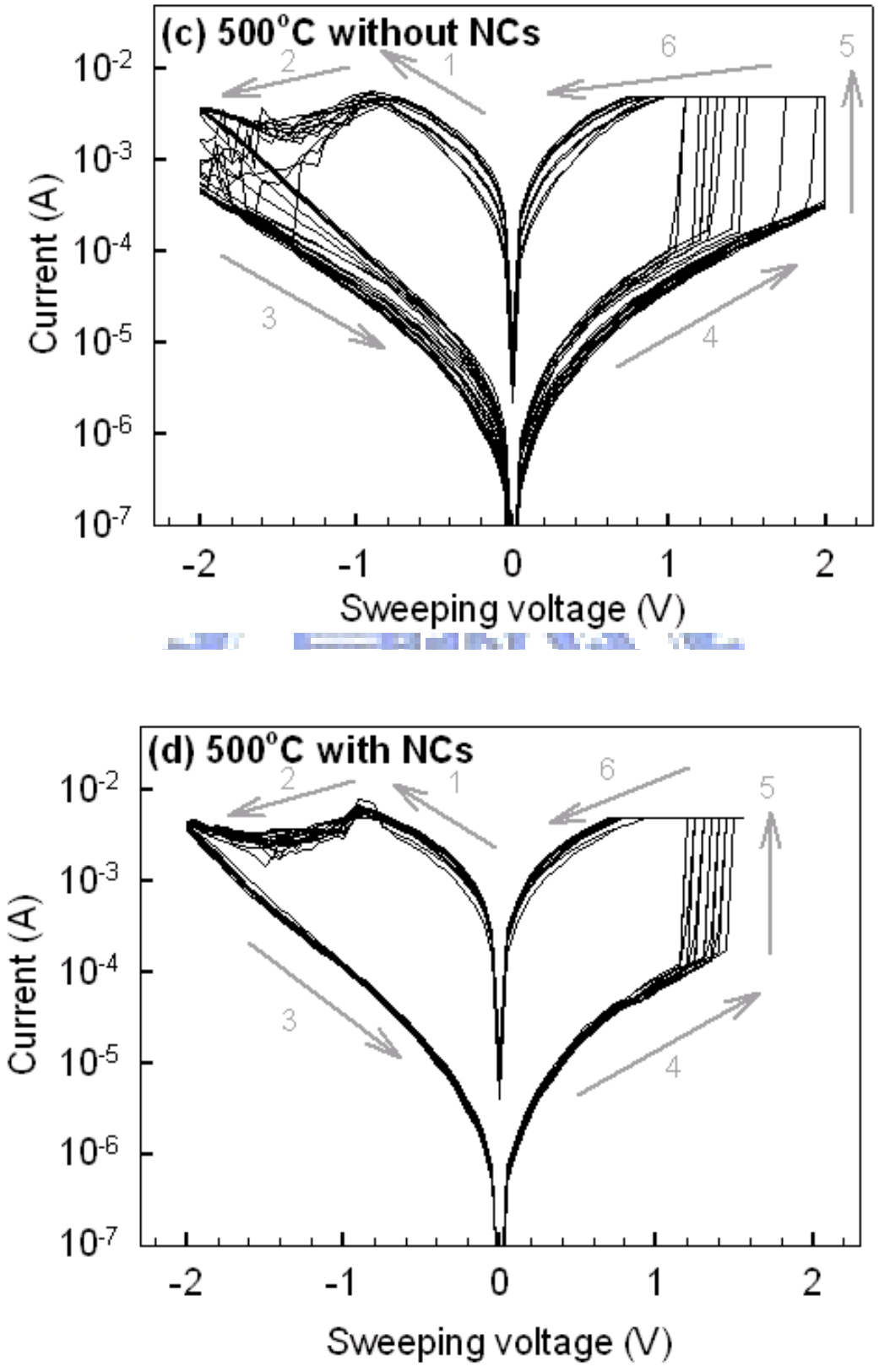


Figure 6-5 conducting current-sweeping voltage characteristics of (a) as-deposited sample with Ni-O-Si layer, (b) annealing at 300°C, and annealing at 500°C (c) without and (d) with Ni-O-Si layer

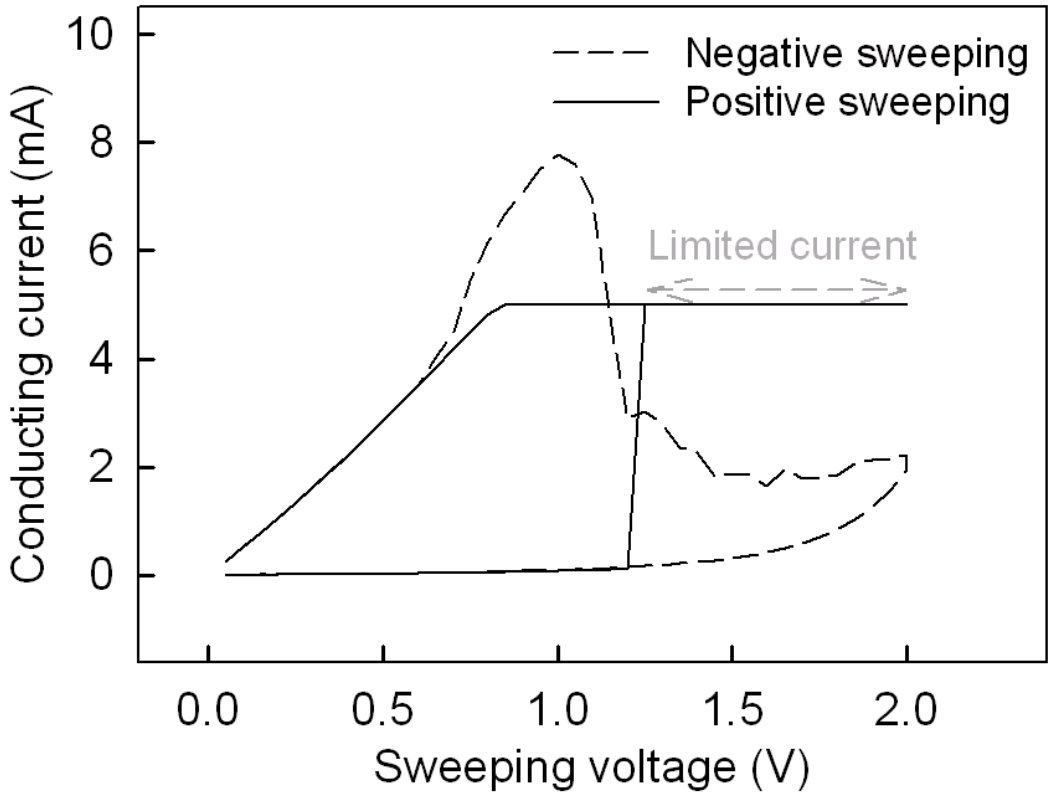
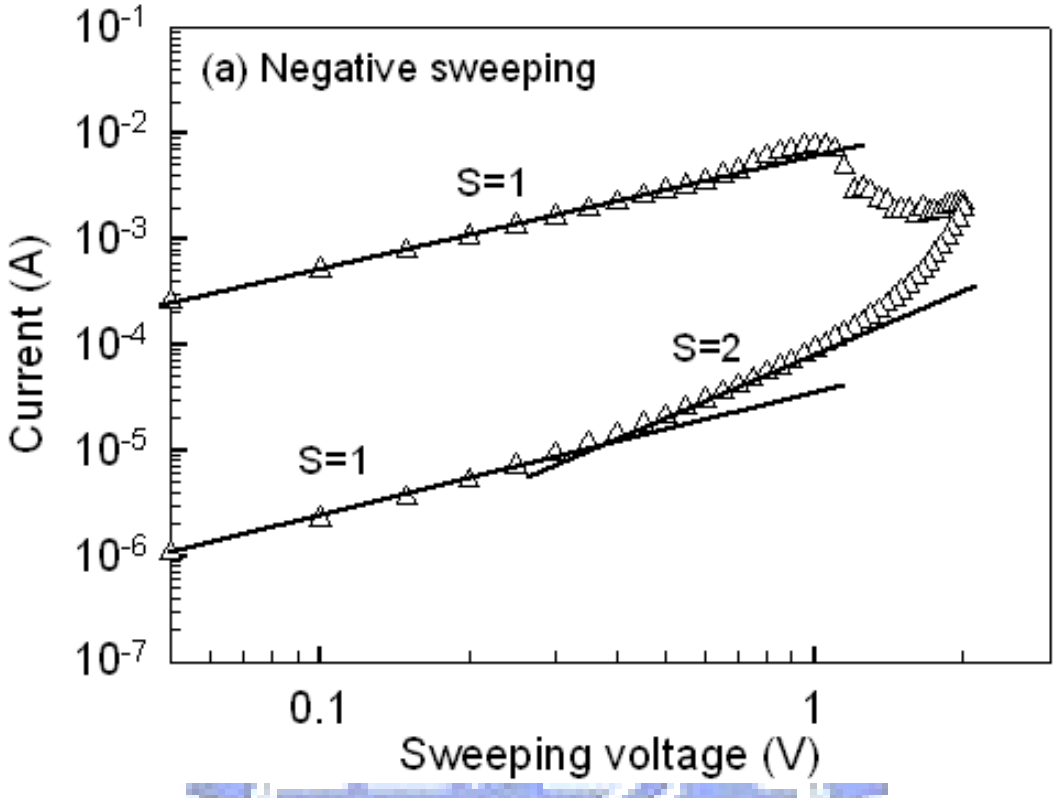


Figure 6-6 linear-linear plot of I-V characteristic for the memory device embedded with Ni nanocrystals.



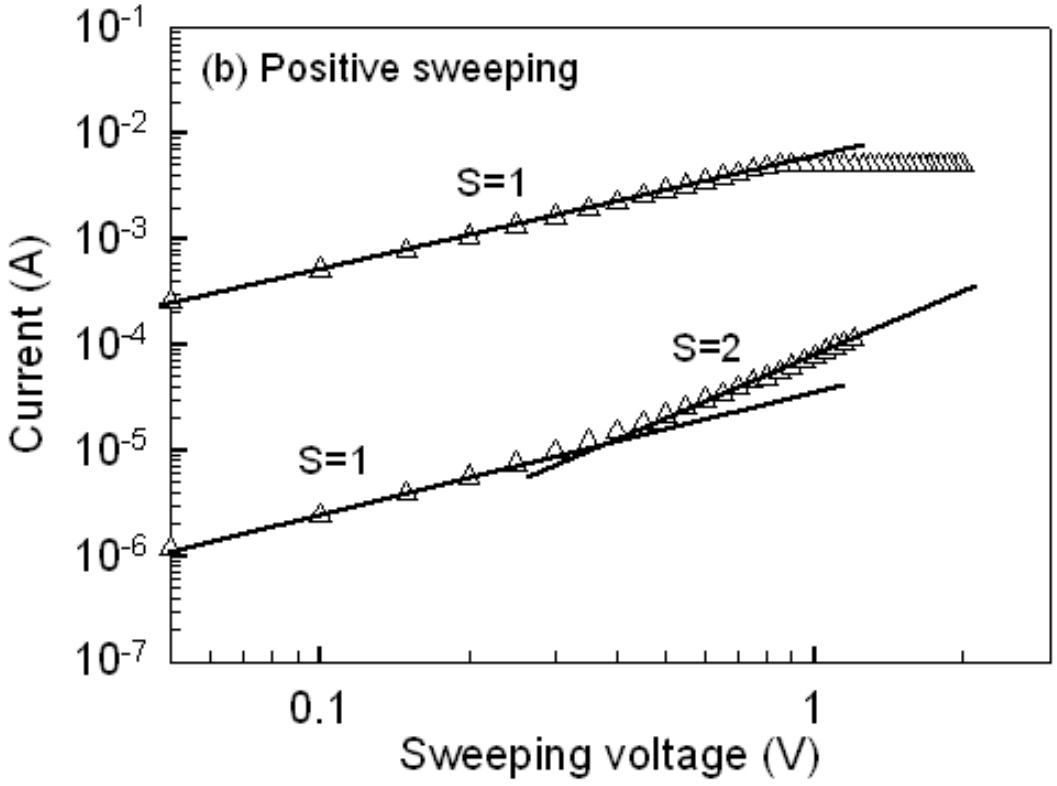


Figure 6-7 Double-logarithmic scale plots of the I-V curves for both positive and negative sweeping region in the Ti/Al_2O_3/Ni NCs/Al2O3/Pt device

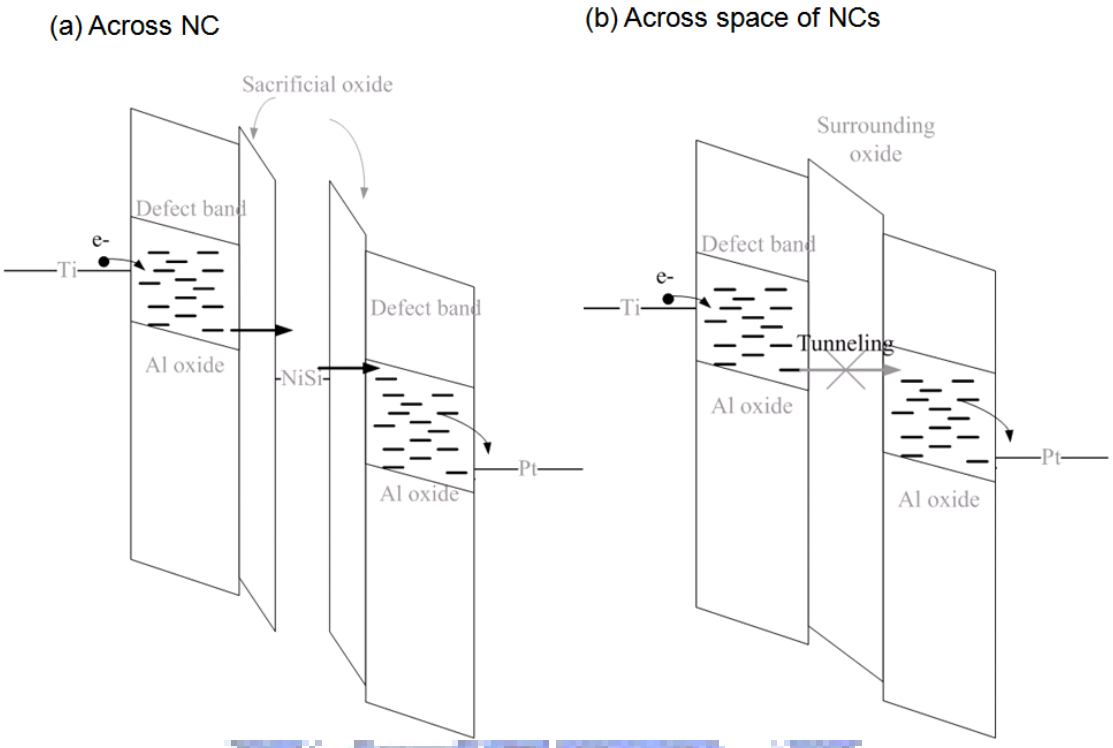


Figure 6-8 Simple band diagram at ON-state of negative bias in the Ti/Al_2O_3/Ni NCs/Al2O3/Pt device.

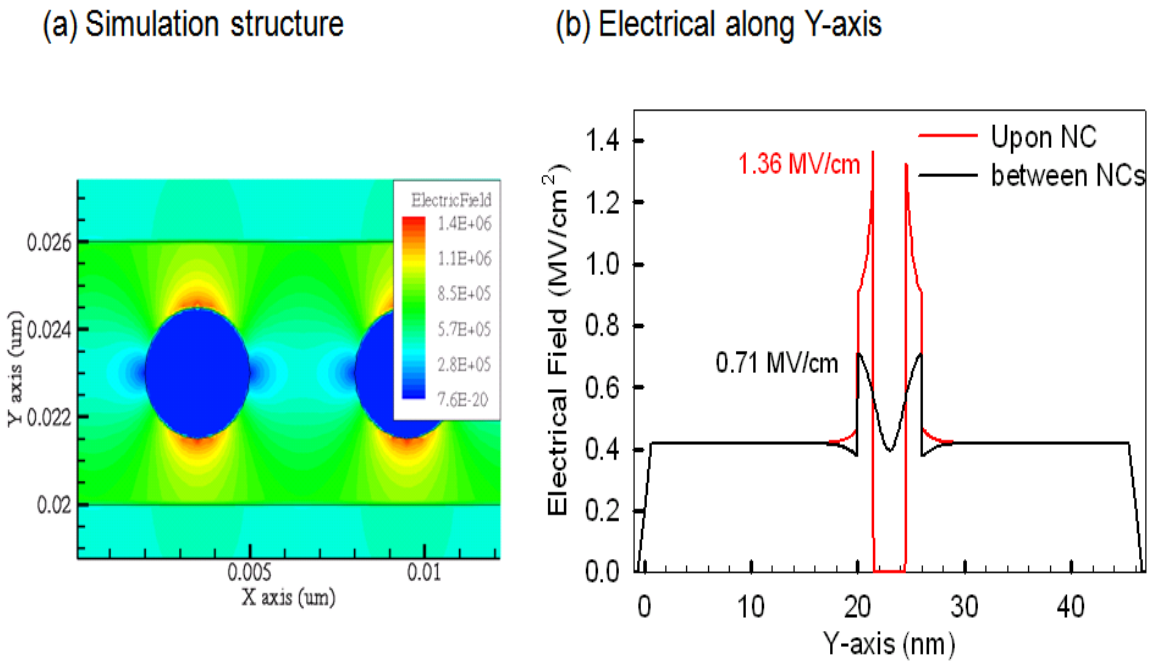


Figure 6-9 Electrical field simulation in the Ti/Al_2O_3/Ni NCs/Al2O3/Pt device.

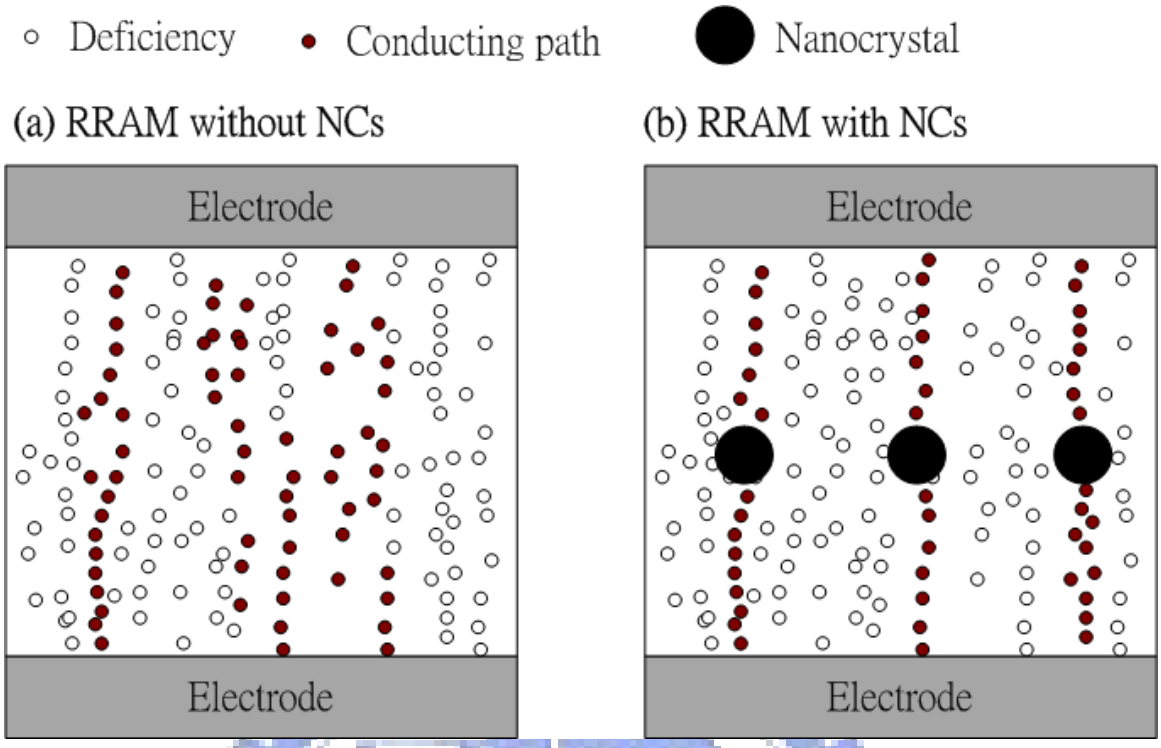


Figure 6-10 Formation of high-conducting path in the memory device (a) without and (b) with nanocrystal.

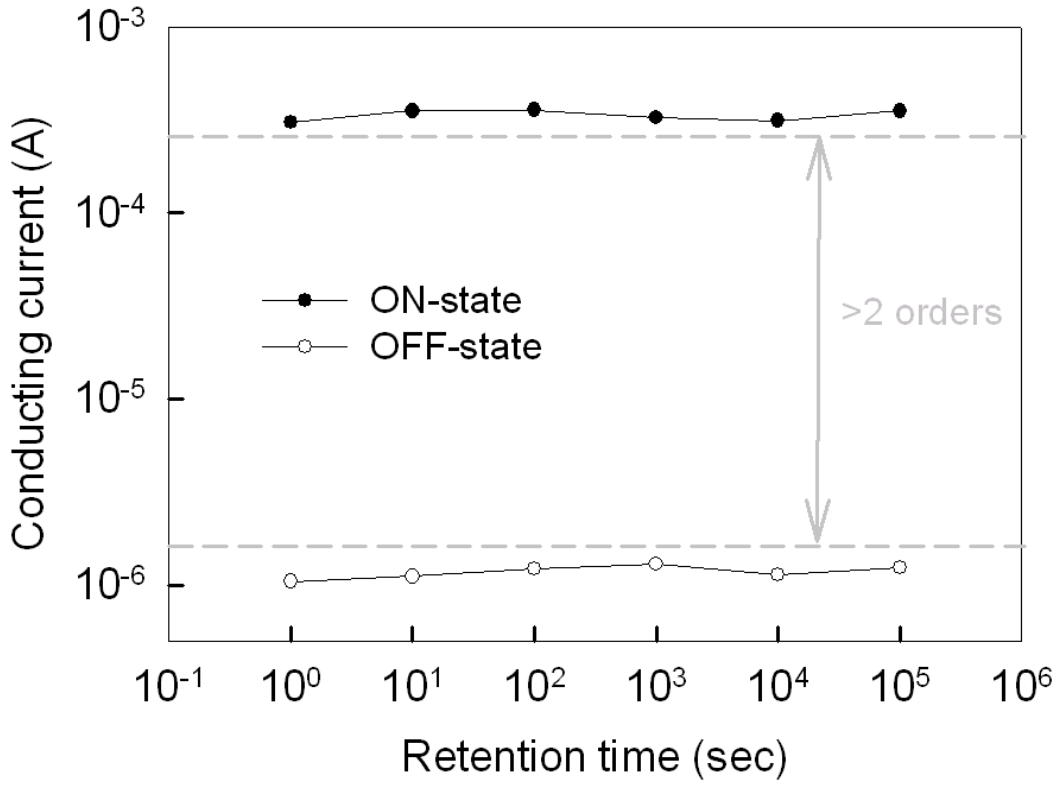


Figure 6-11 Retention characteristics of Ti/Al_2O_3/Ni NCs/Al2O3/Pt device.

Chapter 7

Conclusion

We investigated the annealing ambience influence on mixed Mo and Si layer for nanocrystal memory application. The N_2–annealed mixed Mo and Si layer form an average size of 5-nm $MoSi_2$ nanocrystals, and O_2–annealing on the mixed layer results in a formation of Mo oxide nanocrystals with an average size of 20-nm. Annealing the mixed layer in O_2 ambience can improve the surrounding oxide of nanocrystals and retention behavior. However, the memory window is reduced due to over-oxidation of Mo, interaction of Mo oxide with tunnel oxide occurred.

To prevent over-oxidation of Mo and degradation of tunneling oxide, we proposed an oxygen- and oxygen-incorporated Mo silicide (Si-O-Mo and Si-N-Mo) as nanocrystal self-assembling layers. The results show that as the annealing temperature up to 800°C, continuous (Si-O-Mo) layer agglomerates into nanocrystals. Further increasing annealing temperature to 900°C can result in a reduction of Mo oxide into metallic Mo. The redox reaction is because the difference in formation energy between Mo oxide and Si oxide induces an internal completion between Si, O and Mo. The average size and density of nanocrystals formed by annealing Si-O-Mo layer at 800 and 900°C are the same (5-nm and 10^{12} cm^{-2}). However, memory window of 900°C-annealed Si-O-Mo layer is larger than that of 800°C due to the metal oxide composition in 800°C-annealed Si-O-Mo layer. Furthermore, the 900°C-annealed layer have better retention characteristic than 800°C one which is attributed to the improvement of dielectric around nanocrystals, suppressing lateral migration of stored carriers. On the other hand, smaller size and high density of Mo nanocrystals can be formed in Si-N-Mo layer. The size and density are about 2-nm and 6×10^{12} cm^{-2}. This high density can effectively reduce the variation of memory characteristics between

memory cells when device scaling down.

Furthermore, we fabricated double-layer nanocrystal memory by stacking two Si-O-Mo layers separated with a middle oxide layer. The results indicate that the double-layer nanocrystal memory structure can increase memory window because of higher density of nanocrystal than single-layer structure. Besides, the retention characteristics of double-layer structure is better than single-layer one due to reduction of charging energy and Coulomb blockade effect from first layer of double layer structure.

To improve the quality of dielectric around nanocrystals, a post NH_3 plasma treatment was performed on memory devices of Mo nanocrystal embedded in oxide (Mo-SiO_x) and in nitride (Mo-SiN_x). The nitrogen was incorporated into the surrounding dielectric. The memory window was found to be reduced because shallow traps in surrounding dielectric were passivated by nitrogen incorporation. Furthermore, the retention behavior of both memory devices was improved due to curing surrounding dielectric. The plasma treatment method with small thermal budget has potential to be application in nanocrystal memory device.

The memory characteristics of plasma-treated Mo-SiO_x and Mo-SiN_x devices including memory window, retention and endurance characteristics were compared. The Mo-SiN_x has larger memory window than Mo-SiO_x device due to its higher density. Furthermore, retention of Mo-SiN_x device after endurance test is better than that of Mo-SiO_x device. Electrical simulation results for both Devices under programming were employed to investigate difference in retention behavior after endurance test. It was found that electrical field in tunnel oxide of Mo-SiO_x device is larger than that of Mo-SiN_x device. This explains the poor retention behavior in Mo-SiO_x device.

Resistive switching characteristics of Al_2O_3 were studied to integrate in back-end

process of nonvolatile memory. As-deposited Al_2O_3 layer shows an initial high-conducting state, and low device yield due to larger amount of oxygen deficiency in the as-deposited film. After annealing at 300 and 500°C, the quality of Al_2O_3 layer was improved increasing the device yield. However, ON- and OFF-states current, and turn-on voltage (V_T) show a large variation between cycles. The large variation in devices can be attributed the random formation and rupture of high conducting paths. We stabilize the memory characteristics by embedding Ni nanocrystals into Al_2O_3 layer. The results indicated that variation of conducting current of ON- and OFF-state was reduced. The current fitting show that the conducting mechanism of the memory device is Ohmic in the ON-state. However, the conducting current of OFF-state obeys Ohmic conduction in low bias region and space-charge-limited-conduction in high bias region. Electrical simulation results show that the max electrical field across nanocrystal is twice larger than that across the space between nanocrystals. We construct a band diagram to explain why nanocrystal embedded in Al_2O_3 can stabilize the memory characteristics of resistive switching memory. The higher electrical field and conductivity across nanocrystal than space between nanocrystals can fix formation and rupture of high conducting paths which improve the stability.

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