國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

互補式金氧半積體電路靜電放電防護之設計最佳化與故障分析

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摘要

隨著奈米尺度互補式金氧半製程時代的來臨與系統單晶片應用的持續發展，靜電放電(Electrostatic Discharge, ESD)防護已成為積體電路產品可靠度中相當艱鉅的挑戰。為避免積體電路遭受靜電放電的威脅與破壞，所有積體電路與外界接觸的輸入輸出銲墊(Pad)或是電源銲墊，皆須搭配靜電放電防護設計。然而，輸入輸出銲墊上的靜電放電防護電路會在訊號路徑上產生寄生效應。若訊號路徑上的寄生效應過大，將導致電路性能的嚴重衰減。尤其於類比輸入輸出界面電路與跨電源組之內部傳輸界面電路應用中，靜電放電防護電路在訊號路徑上引起的寄生效應必須達到最小化的設計。寄生效應嚴格限制的情況下，電源箝制靜電放電防護電路(Power-Rail ESD Clamp Circuit)是達成積體電路產品全晶片靜電放電防護極為有效的設計。它不僅可以提升電源線至接地線的靜電放電防護能力，亦能顯著強化輸入輸出銲墊至電源線(VDD)與接地線(VSS)或是接點對接點(Pin-to-Pin)的靜電放電防護能力。搭配電源箝制靜電放電防護電路與類比輸入輸出銲墊的靜電放電防護電路，將可共構出適用於類比輸入輸出界面電路的低寄生效應靜電放電防護電路。此外，跨電源組內部傳輸界面電路的靜電放電防護問題，亦可利用電源箝制靜電放電防護電路與主動式跨電源組靜電放電防護電路(Active Cross-Power-Domain ESD Protection Circuit)成功獲得解決。具備有效且可靠的靜電放電防護設計，能夠提供奈米尺度積體電路產品足夠的耐用年限，並能讓產品使用者更加安心。

為獲得良好的靜電放電防護能力，擁有閘極驅動機制的 N 型金氧半電晶體電源箝

制靜電放電防護電路，已經廣泛使用於奈米尺度互補式金氧半製程技術的積體電路產品。這些電源箝制靜電放電防護電路具有一特定電路架構，即是以多級反相器(Multi-Stage Inverters)實現控制電路，驅動主靜電放電箝制 N 型金氧半電晶體(Main ESD Clamp NMOS Transistor)。本論文的第二章分析兩種控制電路架構，分別為三級反相器與一級反相器，對於靜電放電防護與應用所造成的影響，藉以驗證適用於電源箝制靜電放電防護電路的最佳化設計。研究中發現不良的電路設計架構，會導致 N 型金氧半電晶體的電源箝制靜電放電防護電路，在電性高速暫態(Electrical Fast Transient, EFT)測試與高速電源啟動(Fast Power-On)測試下，發生異常的閂鎖導通現象(Latch-On Event)。本章後段利用高敏度微光顯微鏡(Emission Microscope, EMMI)，清楚解釋電源箝制靜電放電防護電路的異常閂鎖導通故障機制。

除了控制電路以外，N 型金氧半電晶體電源箝制靜電放電防護電路的靜電放電暫態偵測電路(ESD-Transient Detection Circuit)亦是決定電源箝制靜電放電防護電路性能與應用的關鍵因素。本論文第三章提出了一個嶄新的靜電放電暫態偵測電路，其特點為極小的靜電放電暫態偵測電容設計下，成功延長主靜電放電箝制 N 型金氧半電晶體導通時間，進而提升電源箝制靜電放電防護電路的導通效率與靜電放電耐受度。此外，這個靜電放電暫態偵測電路擁有優異抵抗誤觸發(Mis-Trigger)與閂鎖導通的能力，可以安全使用於高速電源啟動的特殊電路系統。

在電源箝制靜電放電防護電路的設計中，主靜電放電箝制元件(Main ESD Clamp Device)將是直接影響靜電放電防護能力的最主要因素。一直以來，矽控整流器元件(Silicon Controlled Rectifier, SCR)即是以極高的單位面積靜電放電耐受度而備受矚目。然而過高的觸發電壓與較差的導通速度，使得矽控整流器元件在先進製程的靜電放電防護應用上受到很大的限制。本論文的第四章提出具有低觸發電壓與高導通效率的常開型效能矽控整流器設計(Initial-On SCR Design)。未使用特殊的常開型元件與未進行製程調整的情況下，以矽控整流器元件搭配內嵌 P 型金氧半電晶體做為觸發控制電路完成常開型效能矽控整流器設計，適用於一般的互補式金氧半製程技術，大大增加矽控整流器元件於深次微米與奈米尺度積體電路的靜電放電防護應用。此外，這個常開型效能的矽控整流器於 2.5 伏特的操作電壓下擁有足夠高的導通電壓(Holding Voltage, Vh)，可避免電性閂鎖(Latchup)的問題。經由實驗晶片量測結果，以 P 型金氧半電晶體觸發的常開型效能矽控整流器，已成功驗證於 0.25 微米互補式金氧半製程技術。

本論文第五章針對前一章所提出的金氧半電晶體觸發矽控整流器(MOS-Triggered

SCR)元件進行設計最佳化的分析與研究。金氧半電晶體觸發矽控整流器元件的觸發機制與靜電放電電流分佈會受到內嵌金氧半電晶體的通道長度的改變而有所不同，通道長度將對於矽控整流器元件的觸發電壓(Trigger Voltage, Vt1)、導通電壓、導通電阻(On Resistance, Ron)、二次崩潰電流(Second Breakdown Current, It2)與靜電放電耐受度有相當大的影響。為使金氧半電晶體觸發矽控整流器於深次微米與奈米尺度的積體電路之靜電放電防護應用中達到最佳效能，內嵌金氧半電晶體的通道長度與電路佈局設計最佳化已透過各項參數的分析比較呈現於第五章。

於類比輸入輸出界面電路的應用中，本論文第六章以兩種類比輸入輸出銲墊的靜電放電防護電路，搭配不同的電源箝制靜電放電防護電路進行設計最佳化研究。本章使用 0.18 微米 1.8 伏特與 3.3 伏特互補式金氧半製程技術，分別設計了四種可應用於類比輸入輸出界面電路的靜電放電防護電路。其中，分析三種電源箝制靜電放電箝制元件分別為閘極驅動 N 型金氧半電晶體(Gate-Driven NMOS)、基體觸發的場氧化層元件(Substrate-Triggered Field-Oxide Device, STFOD)與基體觸發 N 型金氧半電晶體(Substrate-Triggered NMOS, STNMOS)，在類比輸入輸出界面電路的電源箝制靜電放電防護電路中的防護效能，藉以找出適當的電源箝制靜電放電箝制元件。經由實驗晶片量測結果，在 0.18 微米的互補式金氧半製程技術中，適用於類比輸入輸出界面電路的靜電放電防護設計，是以雙二極體(Double Diode)作為類比輸入輸出銲墊上的靜電放電防護電路，這兩個二極體分別放置於類比輸入輸出銲墊至電源線與接地線間，搭配閘極驅動 N 型金氧半電晶體電源箝制靜電放電防護電路。經由掃瞄式電子顯微鏡的觀察，四種類比輸入輸出電放電防護設計的故障機制，獲得更完整的分析與討論。施加負靜電放電電壓於類比輸入輸出銲墊且電源線接地的測試條件(Negative-to-VDD Mode, ND-Mode)下，以雙二極體與基體觸發場氧化層元件所建構的類比輸入輸出靜電放電防護設計，產生了異常的故障點。這個故障機制是由於寄生於靜電放電防護二極體與 N 型防護環(Guard Ring)間的 npn 雙極性接面電晶體(Bipolar Junction Transistor, BJT)意外觸發導致大量靜電放電電流，經這個寄生 npn 雙極性接面電晶體釋放造成防護環的燒熔破壞。本章的最後針對此故障機制提出相對應的解決方案。

由於積體電路設計的複雜化，越來越多的電路功能整合入同一個單晶片上，而這些電路區塊因為操作電壓的不同與電源雜訊耦合的考量，各自擁有獨立的電源組，然而這樣的獨立電源組架構相當不利於跨電源組靜電放電防護，使得跨電源組靜電放電防護設計成為極需被解決的問題。本論文第七章首先探討了一件積體電路產品的跨電源組界面

電路故障案例。於此案例中，產品的人體放電模式靜電放電耐受度可以達到 2000 伏特，但其機械放電模式靜電放電耐受度則無法達到 150 伏特。施加負靜電放電電壓於輸入輸出銲墊且電源線接地的機械放電模式的測試條件下，靜電放電電流經由跨電源組界面電路釋放，造成界面電路的閘極氧化層、接面與接觸(Contact)的嚴重燒熔破壞。藉由故障分析技術，清楚分析跨電源組靜電放電電流釋放路徑與故障機制。本章的第二部分，針對目前已發表的跨電源組界面電路靜電放電防護設計進行分析，藉以更進一步了解跨電源組間靜電放電防護設計策略。在本章的最後一部份，提出了適用於跨電源組界面電路的主動式跨電源組靜電放電防護設計，並且於 130 奈米互補式金氧半製程技術中獲得成功的驗證。於跨電源組人體放電模式與機械放電模式靜電放電測試中，其靜電放電耐受度分別達到 4000 伏特與 400 伏特。

第八章總結本論文的研究成果，並提出數個接續本論文研究方向的研究題目。本論文所提出的各項新型設計，均搭配實驗晶片量測結果以驗證設計之理論，且有相對應的國際期刊與國際研討會論文發表。本論文中數個創新設計已提出專利申請。

DESIGN OPTIMIZATION AND FAILURE ANALYSIS OF ON-CHIP ESD PROTECTION IN CMSO INTEGRATED CIRCUITS

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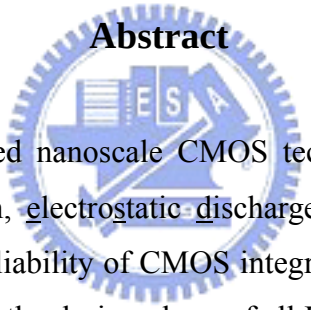

Abstract

With the era of the advanced nanoscale CMOS technology and the development of system-on-chip (SoC) application, electrostatic discharge (ESD) protection has become a tough challenge on the product reliability of CMOS integrated circuits. ESD protection must be taken into consideration during the design phase of all IC products. In order to prevent the ESD failures and damages in IC products, all pads which connect the IC and the external world need to be provided with ESD protection circuits, including the input/output (I/O) pads, VDD pads, and VSS pads. However, the ESD protection devices at the I/O pads inevitably cause parasitic effects on the signal path. If the parasitic effects on the signal path are too large, the circuit performance will be seriously degraded. In other words, the parasitic effects which are induced by ESD protection on the signal paths need to be minimized, especially in analog I/O interface circuits and internal transmission interface circuit between separated power domains. The power-rail ESD clamp circuit is an efficient design to achieve whole-chip ESD protection in IC products. It not only can enhance ESD robustness of VDD-to-VSS ESD stress, but also can significantly improve ESD robustness of the ESD stresses between input/output and VDD/VSS or pin-to-pin combinations. A turn-on efficient power-rail ESD clamp circuit between VDD and VSS is co-constructed into the analog ESD protection circuit to improve the overall ESD level of the analog I/O interface circuits.

Moreover, the ESD issues of interface circuits between separated power domains also can be solved by turn-on efficient power-rail ESD clamp circuit cooperated with active cross-power-domain ESD protection designs. With efficient on-chip ESD protection designs, the integrated circuits with nanoscale CMOS technology can be safely used and provide moderate life time.

NMOS-based power-rail ESD clamp circuits with gate-driven mechanism have been widely used to obtain the desired ESD protection capability. All of them are usually based on a similar circuit scheme with multiple-stage inverters to drive the main ESD clamp NMOS transistor with large device dimension. In Chapter 2, the designs with 3-stage-inverter and 1-stage-inverter controlling circuits have been studied to verify the optimal circuit schemes in the NMOS-based power-rail ESD clamp circuits. Besides, the circuit performances among the main ESD clamp NMOS transistors drawn in different layout styles cooperated with the controlling circuit of 3-stage inverters or 1-stage inverter are compared. Among the NMOS-based power-rail ESD clamp circuits, an abnormal latch-on event has been observed under the EFT test and fast power-on condition. The root cause of this latch-on failure mechanism has been clearly explained by the emission microscope with InGaAs FPA detector.

Besides controlling circuit in NMOS-based power-rail ESD clamp circuit, a power-rail ESD clamp circuit with a new proposed ESD-transient detection circuit of ultra small capacitor has been presented and verified to possess a long turn-on duration and high turn-on efficiency in chapter 3. In addition, the power-rail ESD clamp circuit with the proposed ESD-transient detection circuit also showed an excellent immunity against the mis-trigger and the latch-on event under the fast power-on condition.

In chapter 4, a novel SCR design with "*initial-on*" function is proposed to achieve the lowest trigger voltage and the highest turn-on efficiency of SCR device for effective on-chip ESD protection. Without using the special native device (NMOS with almost zero or even negative threshold voltage) or any process modification, this initial-on SCR design is implemented by PMOS-triggered SCR device, which can be realized in general CMOS processes to enhance the applications of SCR devices for deep-submicron or nanoscale CMOS technology. This initial-on SCR design has a high enough holding voltage to avoid latchup issues in a VDD operation voltage of 2.5 V. The new proposed initial-on ESD protection design with PMOS-triggered SCR device has been successfully verified in a fully-silicided 0.25-μm CMOS process.

In chapter 5, the channel length of the embedded MOS transistor in the MOS-triggered

SCR device has been demonstrated to dominate the trigger mechanism and current distribution to govern the trigger voltage, holding voltage, on resistance, second breakdown current, and ESD robustness of the MOS-triggered SCR device. MOS-triggered SCR devices have been reported to achieve efficient on-chip ESD protection in deep-submicron or nanoscale CMOS technology. The embedded MOS transistor in the MOS-triggered SCR device should be optimized to achieve the most efficient ESD protection in advanced CMOS technology. In addition, the layout style of the embedded MOS transistor can be adjusted to improve the MOS-triggered SCR device for ESD protection.

In chapter 6, different ESD protection schemes have been investigated to find the optimal ESD protection design for analog I/O buffer in a 0.18-μm 1.8-V and 3.3-V CMOS technology. Three power-rail ESD clamp devices, which are gate-driven NMOS, substrate-triggered field-oxide device (STFOD), and substrate-triggered NMOS (STNMOS) with dummy gate, are used for power-rail ESD clamp circuits to compare the protection efficiency in analog I/O applications. From the experimental results, the pure-diode ESD protection devices and the power-rail ESD clamp circuit with gate-driven NMOS are the suitable design for analog I/O buffer in the 0.18-μm CMOS process. Each ESD failure mechanism was inspected by SEM photograph in all analog I/O pins. An unexpected failure mechanism was found in the analog I/O pins with pure-diode ESD protection design under ND-mode ESD stress. The parasitic npn bipolar transistor between ESD clamp device and guard ring structure was triggered to discharge the ESD current and cause damage under ND-mode ESD stress.

Chapter 7 presents several complex ESD failure mechanisms in the interface circuits of an IC product with multiple separated power domains. In this case, the MM ESD robustness can not achieve 150 V in this IC product with separated power domains, although it can pass the 2-kV HBM ESD test. The ND-mode MM ESD currents were discharged by circuitous current paths through interface circuits to cause the gate oxide damage, junction filament, and contact destroy of the internal transistors. The detailed discharging paths of ND-mode ESD failures were analyzed in this paper. In addition, some ESD protection designs have been illustrated and reviewed to further comprehend the protection strategies for cross-power-domain ESD events in chapter 7. Moreover, one new active ESD protection design for the interface circuits between separated power domains has been proposed and successfully verified in a 0.13-μm CMOS technology. The HBM and MM ESD robustness of the separated-power-domain interface circuits with the proposed active ESD protection

design can achieve over 4 kV and 400 V, respectively.

Chapter 8 concludes the achievement in this dissertation, and suggests several future works in this research field. In this dissertation, several novel designs have been proposed in the aforementioned research topics. Measured results of fabricated test chips have demonstrated the performance improvement. The achievement of this dissertation has been published in several international journal and conference papers. Several innovative designs have been applied for patents.

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陳 世 宏
誌於竹塹交大
九十八年 一月

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Chapter 1

Introduction

In this chapter, the background and the organization of this dissertation are discussed. First, the main concerns of electrostatic discharge (ESD) protection design for integrated circuits in deep-submicron and nanoscale complementary metal-oxide-semiconductor (CMOS) processes are introduced. Secondly, the ESD protection design for analog input/output (I/O) interface circuits and the cross-power-domain ESD issues of CMOS integrated circuit (IC) products with multiple separated power domains are discussed. Finally, the organization of this dissertation is described.

1.1. Background of ESD Protection Design for Integrated Circuits in Advanced CMOS Technologies

With the continuous evolution of CMOS technology, electrostatic discharge (ESD) protection has become a tough task on the product reliability of CMOS integrated circuits. The scaled down device dimension with thinner gate oxide and shallower junction depth in nanoscale CMOS technology is easily damaged by ESD stress. The ESD specification of commercial IC products are generally required to be higher than 2 kV in human-body-model (HBM) [1] and 200 V in machine-model (MM) [2] ESD stresses. The ESD-test pin combinations are shown in Fig. 1.1. ESD stresses may have positive or negative voltages on an I/O pin with respect to the grounded VDD or VSS pin. For comprehensive ESD verification, the VDD-to-VSS ESD stresses and pin-to-pin ESD stresses had also been specified to verify the whole-chip ESD robustness, which are shown in Fig. 1.2 and 1.3, respectively. Therefore, on-chip ESD protection circuits must be added into CMOS ICs to achieve the required ESD robustness [3]-[5]. A typical design of on-chip ESD protection circuits is illustrated in Fig. 1.4. The power-rail ESD clamp circuit is an efficient design to achieve whole-chip ESD protection in IC products [6], [7]. It not only can enhance ESD robustness of VDD-to-VSS ESD stress, but also can significantly improve ESD robustness of the ESD stresses between input/output and VDD/VSS [7].

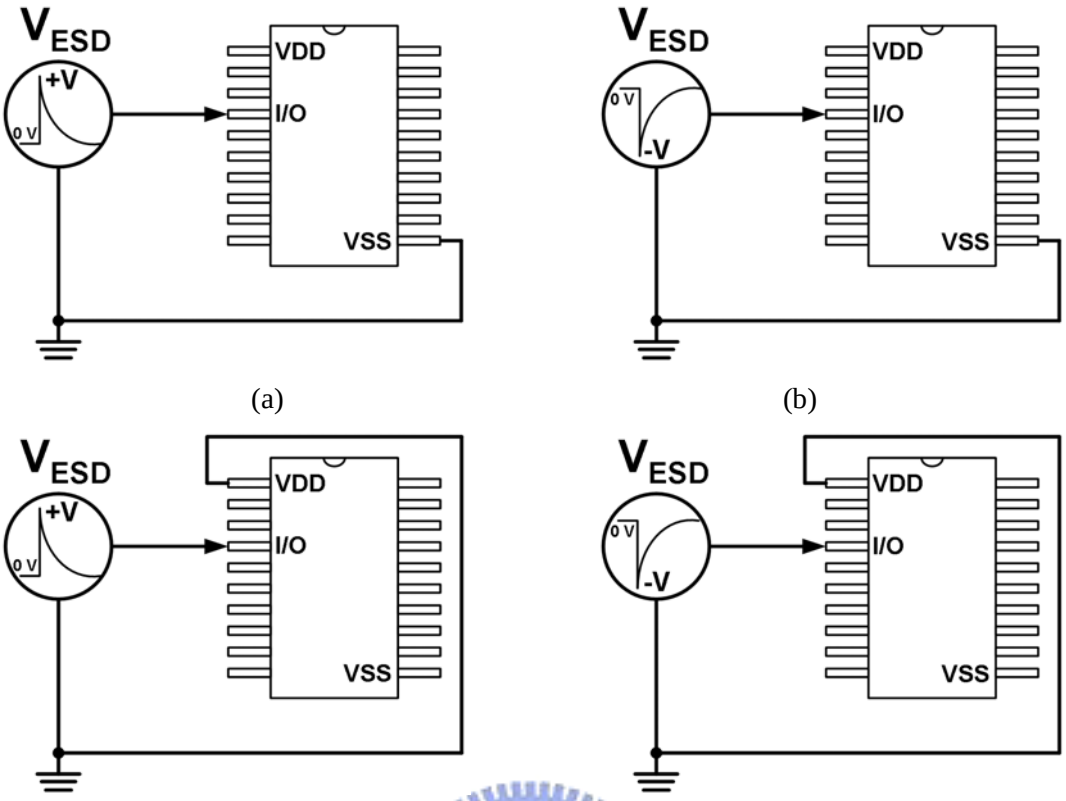


Fig. 1.1. Four ESD-test pin combinations for the IC products: (a) positive-to-VSS mode (PS-mode), (b) negative-to-VSS mode (NS-mode), (c) positive-to-VDD (PD-mode), and (d) negative-to-VDD (ND-mode).

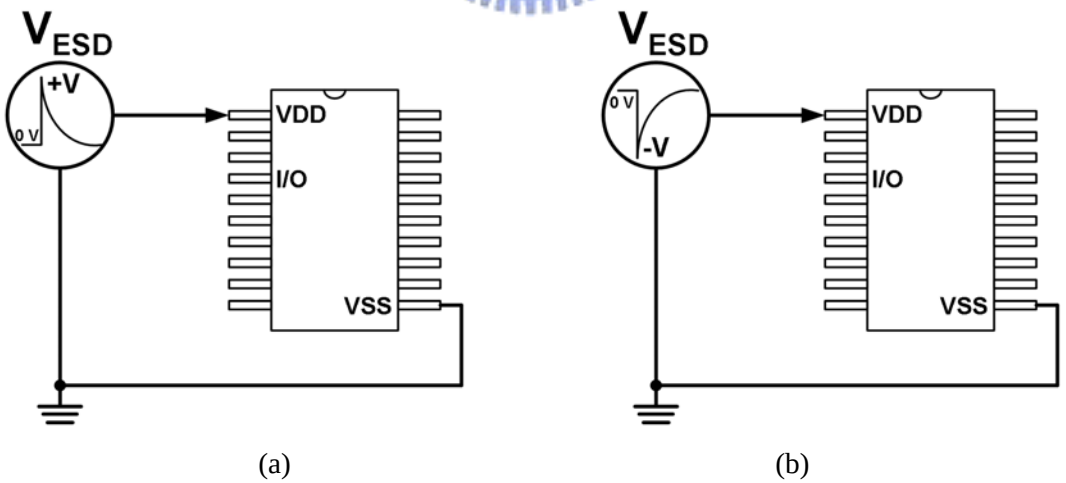
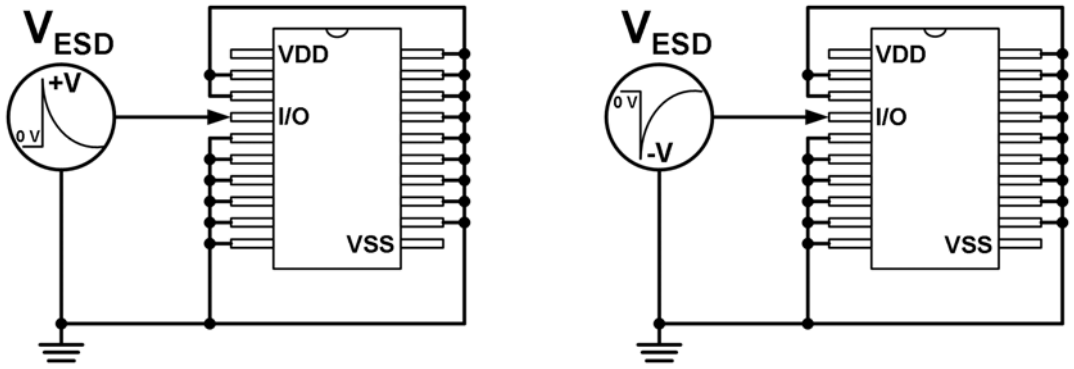


Fig. 1.2. Pin combinations in VDD-to-VSS ESD tests: (a) positive mode, and (b) negative mode.



(a) (b)

Fig. 1.3. Pin combinations in pin-to-pin ESD tests: (a) positive mode, and (b) negative mode.

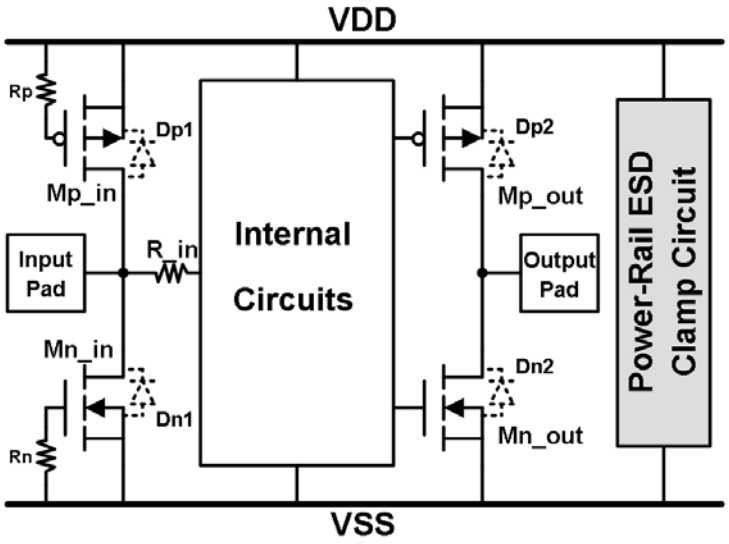


Fig. 1.4. Typical on-chip ESD protection circuits for CMOS ICs.

In general, the power-rail ESD clamp circuit consists of an ESD-transient detection circuit, a controlling circuit, and a main ESD clamp devices, as shown in Fig. 1.5. The ESD-transient detection circuit, which is usually implemented by resistor-capacitor (RC) network, is used to distinguish ESD-stress conditions from normal circuit operation conditions due to the difference in the rise time between these two conditions [6], [7]. Then, the controlling circuit implemented by single- or multi-stage inverters cooperates with the RC-based ESD-transient detection circuit to command the main ESD clamp device into the on state or the off state under the ESD-stress conditions and normal circuit operation conditions. The main ESD clamp device is always required to provide a low impedance discharging path under ESD-stress conditions, while it must be kept off under normal circuit operation conditions. NMOS transistors have been widely used as the main ESD clamp device to obtain the desired ESD protection capability.

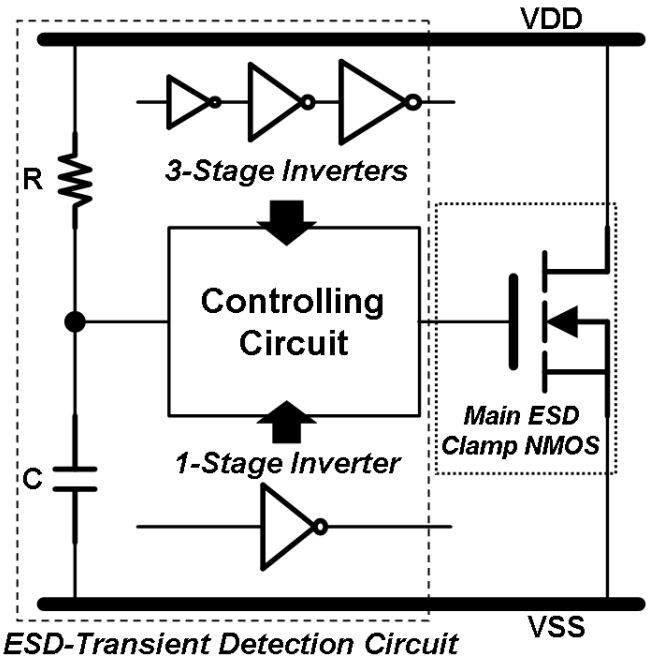


Fig. 1.5. Typical design scheme for NMOS-based power-rail ESD clamp circuit with RC-based ESD-transient detection circuit.

During the positive-to-VDD (PD) mode and negative-to-VSS (NS) mode ESD stresses, ESD current is discharged through the forward-biased Dp1 and Dn1, which are parasitic diodes in gate-VDD PMOS (GD-PMOS) transistor, Mp_in, and gate-grounded NMOS (GG-NMOS) transistor, Mn_in, respectively. To avoid the GD-PMOS and GG-NMOS from being operated under breakdown condition during the positive-to-VSS (PS) mode and negative-to-VDD (ND) mode ESD stresses, which results in a substantially lower ESD robustness, the power-rail ESD clamp circuit is used between VDD and VSS to provide ESD current paths between the power rails [7]. Thus, ESD current is discharged from the I/O pad through the parasitic forward-biased Dp1 in Mp_in to VDD, and discharged to the grounded VSS pin through the turned-on power-rail ESD clamp circuit during PS-mode ESD stresses, as shown in Fig. 1.6(a). Similarly, ESD current is discharged from the VDD pin through the turned-on power-rail ESD clamp circuit and the parasitic forward-biased Dn1 in Mn_in to the I/O pad during ND-mode ESD stresses, as shown in Fig. 1.6(b). Under VDD-to-VSS ESD tests, ESD current flows through the power-rail ESD clamp circuit between VDD and VSS. During pin-to-pin ESD stresses, ESD current flows from the zapped I/O pad through the parasitic forward-biased Dp1 in Mp_in, the turned-on power-rail ESD clamp circuit, and the parasitic forward-biased Dn2 in Mn_out to the grounded I/O pad, as shown in Fig. 1.6(c). With the turn-on efficient power-rail ESD clamp circuit, ESD current can be discharged by

the parasitic forward-biased diodes in GD-PMOS and GG-NMOS transistor to obtain the higher ESD robustness under all ESD test modes.

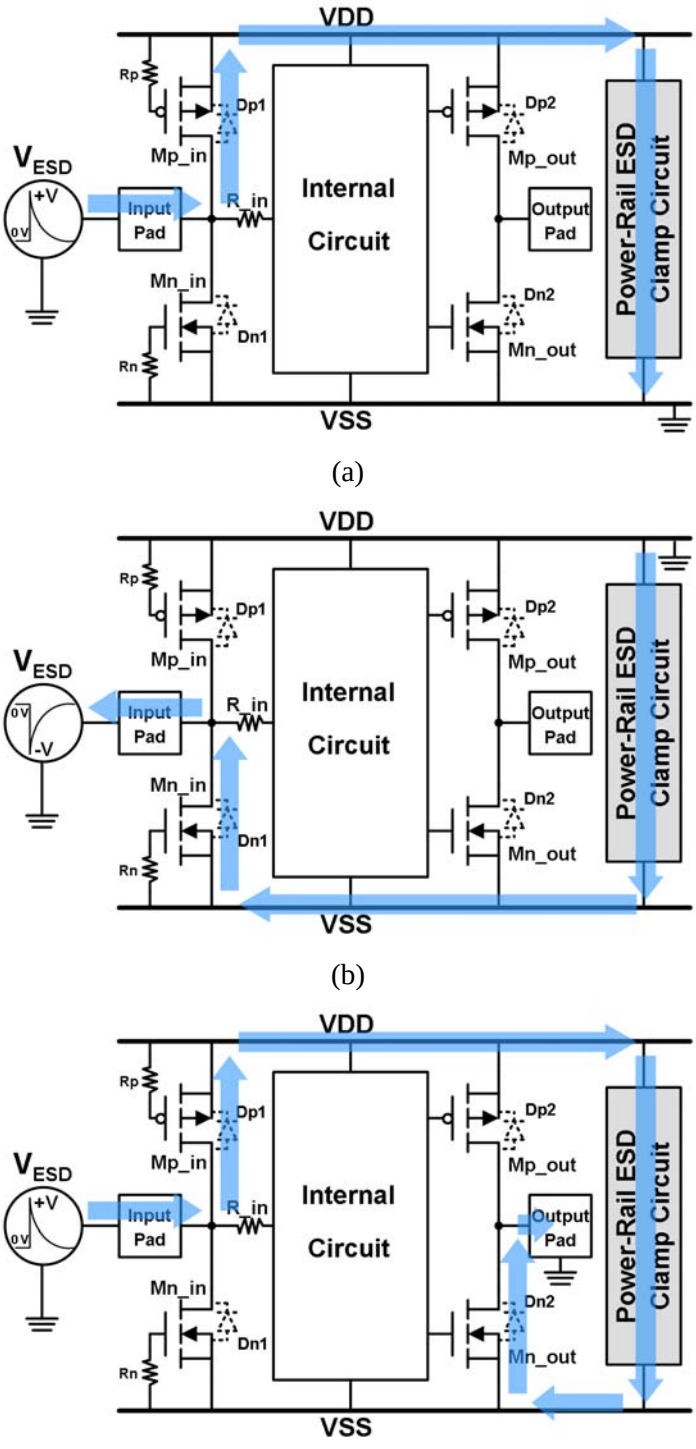


Fig. 1.6. ESD current paths in the typical double-diode ESD protection scheme under (a) PS-mode ESD stresses, (b) ND-mode ESD stresses, and (c) pin-to-pin ESD stresses.

1.1.1. Issues of ESD-Transient Detection Circuit and Controlling Circuit

To efficiently protect the core circuits realized with much thinner gate oxide in nanoscale CMOS technology, some studies had reported the efficient power-rail ESD clamp circuits with modified circuit designs [8]-[11]. All of them were based on the power-rail ESD clamp circuits with gate-driven mechanism which was basically implemented by the RC-based ESD-transient detection circuit with a controlling circuit [6]-[11], as illustrated in Fig. 1.5. Besides, those previous works also adopted the power-rail ESD clamp NMOS transistor with no snapback operations to obtain excellent turn-on efficiency. The snapback phenomenon usually occurs in NMOS transistors, npn bipolar transistors, or silicon controlled rectifiers (SCRs) under higher voltage and current stress conditions. No snapback means that the huge ESD current was discharged by the channel current of NMOS transistors. Therefore, those NMOS transistors in the power-rail ESD clamp circuits were traditionally drawn with huge channel width of several-thousand micrometer to achieve the required ESD robustness under no snapback operation. They were often called as Big FET (BFET) in some previous literatures [8]-[11]. 3-stage inverters, which were adopted as a function of tapered buffer [12]-[16], usually performed the controlling circuit to efficiently turn-on or turn-off the BFET, which has large capacitive load from the NMOS transistor with a huge channel width in power-rail ESD clamp circuit. The tapered buffers, which are the multiple inverter stages with cascaded arrangement, are constantly applied to drive the large loading capacitance under a desirable propagation delay and power consumption [12]-[14]. However, such design concerns are not always appropriate to the function of the controlling circuits in the power-rail ESD clamp circuits because of two main reasons. First, the controlling circuits are only required to propagate a unity signal, such as logical high or logical low, in order to turn on the main ESD clamp devices under ESD-stress conditions, but they are not required to propagate a dynamic signal or alternating logic under normal circuit operation conditions. Second, the controlling circuits are always biased at the static off state under the normal circuit operation conditions in the power-rail ESD clamp circuits. Some basic circuit performances, such as short-circuit dissipation and propagation delay, would not be improved by the controlling circuits with the tapered buffer arrangement. Therefore, the controlling circuits with tapered buffer concepts should be unnecessary and even be unsuitable for power-rail ESD clamp circuits.

In addition, based on the traditional RC-based ESD-transient detection circuit [6], [7], the RC-time constant which is the product of the resistance (R) and capacitance (C) essentially dominated the turn-on duration of the main ESD clamp NMOS transistor. Therefore, the RC-time constant of the RC-based ESD-transient detection circuit should be

designed to sufficiently achieve a desirable turned-on duration of the main ESD clamp NMOS transistor. In general, the turn-on duration was adjusted to meet the period of human-body-model (HBM) ESD event, which is about several hundred nano-seconds (ns) [1]. The extended RC-time constant not only accompanies with the larger layout sizes of the resistance and capacitance, but also is subject to mis-trigger the main ESD clamp NMOS transistor under fast power-on applications [10]. Several previous works proposed special circuit schemes with feedback circuit techniques to extend the turn-on duration under a small RC-time constant [9], [10], [17]-[19]. However, those feedback circuit designs always suffered from the latch-on threats under the fast power-on events or the electrical fast transient noise [20], [21]. Besides, other circuit schemes without feedback circuit techniques, such as on-time control circuit [9] and multi-RC-triggered [11], also had been presented to achieve the desirable turn-on duration and to avoid the latch-on threat. But, extra resistors and capacitors have to be implanted into these designs, which occupying a quite silicon area. In summary, the circuit scheme of controlling circuit and ESD-transient detection circuit should be optimized to obtain more efficient and reliable power-rail ESD clamp circuit in nanoscale CMOS technology.

1.1.2. Issue of SCR Device as Main ESD Clamp Device

In IC products, the on-chip ESD protection designs are required to provide higher ESD robustness with smaller layout area to save the chip area. Silicon controlled rectifiers (SCRs) have been used as on-chip ESD protection devices, because of their superior area-efficient ESD robustness [22]. However, SCR has some drawbacks, such as higher trigger voltage (Vt1), lower turn-on efficiency, and even latchup danger. The traditional I-V characteristic of the SCR device is shown in Fig. 1.7. The higher trigger voltage and lower turn-on efficiency would not efficiently protect the internal circuits in deep-submicron or deep-submicron CMOS technology. Therefore, the low-voltage-triggered SCR (LVTSCR) was invented to reduce the trigger voltage of SCR device [23]. Moreover, some advanced circuit techniques (the gate-coupled [24], substrate-triggered [25], and GGNMOS-triggered [26] techniques) were also reported to enhance the turn-on efficiency of SCR devices. However, those modified SCR designs [23]-[26] still function as the initial-off ESD devices. Recently, in order to further enhance the turn-on speed, the native-NMOS-triggered SCR (NANSCR) has been reported to achieve more efficient ESD protection for CMOS ICs in a 0.13-μm CMOS technology [27]. In this NANSCR, it uses the special native device to achieve the "*initial-on*"

function. The native device is the NMOS transistor with the almost zero threshold voltage (about 0.1 V). It is directly built in a lightly-doped p-substrate, whereas the normal NMOS is in a heavily-doped p-well in p-substrate CMOS technology. Besides, to keep such NANSCR in off state when the IC is in normal operation, it needs the on-chip negative-bias generator [28]. Such extra efforts to realize the NANSCR with negative gate bias for on-chip ESD protection design would cause some limitation in practical applications of general CMOS ICs. On the other hand, the lower holding voltages (lower than VDD operation voltage) could cause latchup triggering by external noise pulses during normal circuit operation conditions. Several previous studies had been presented to increase the holding voltage during normal circuit operation conditions, such as dynamic holding voltage SCR (DHVSCR) [29], SCR devices with stacked diode string [25], and stacked SCR devices [30]. In addition, the high-current-triggered SCR devices had been proposed to safely protect the internal circuits without being accidentally triggered on by the electrical noisy pulse during normal circuit operation conditions [31]. SCR device is susceptible to latchup danger, especially in the application of power-rail ESD clamp circuit. However, with the scale-down device dimension in nanoscale CMOS technology, the VDD operation voltage is also scaled down in order to meet the circuit requirement and gate-oxide reliability. If the holding voltage of the SCR device is greater than the VDD operation voltage, latchup issue will not occur in such IC products with nanoscale CMOS technology. Therefore, the SCR device can be more safely and widely to use as power-rail ESD clamp circuit in nanoscale CMOS technology.

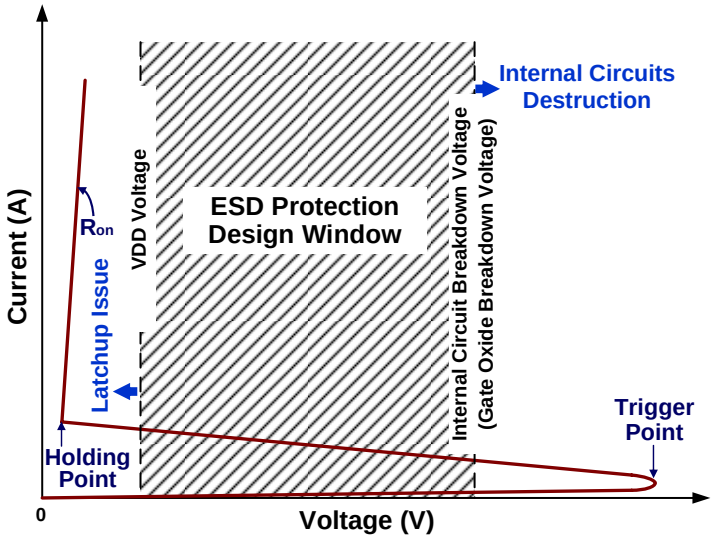


Fig. 1.7. The design window for ESD protection. The traditional I-V characteristic of SCR device can not meet to this ESD protection design window.

1.2. ESD Issues in Analog I/O and Multiple Separated Power Domains Interface Circuits

A conventional ESD protection design for the digital input pin is also shown in Fig. 1.4. The gate-grounded NMOS (GGNMOS) and gate-VDD PMOS (GDPMOS) are often designed with a large device dimension and a wider drain-contact-to-poly-gate layout spacing to sustain the desired ESD level, typically 2 kV in HBM and 200 V in MM ESD stresses. The resistor R in the digital input ESD protection circuit is usually included to effectively protect the gate oxide of input stage. However, the series resistance between the input pad and input stage is forbidden for current-mode input signals or high-frequency applications. Furthermore, the series resistance and the large junction capacitance of the ESD clamp devices cause a long RC delay to the input signals; therefore, such ESD protection circuit is not suitable for analog I/O interface circuits [32]. A typical ESD protection design for analog I/O interface circuit has been reported, as shown in Fig. 1.8. In order to reduce the input capacitance of the analog I/O interface circuits, the N-cell and P-cell are both designed with smaller device dimensions. However, such small devices can't sustain high enough ESD level, while the analog pin is zapped in the positive-to-VSS (PS-mode) or the negative-to-VDD (ND-mode) ESD stress (the devices operated in the breakdown condition). Therefore, a turn-on efficient power-rail ESD clamp circuit between VDD and VSS was co-constructed into the analog ESD protection circuit to improve the overall ESD level of the analog I/O interface circuits.

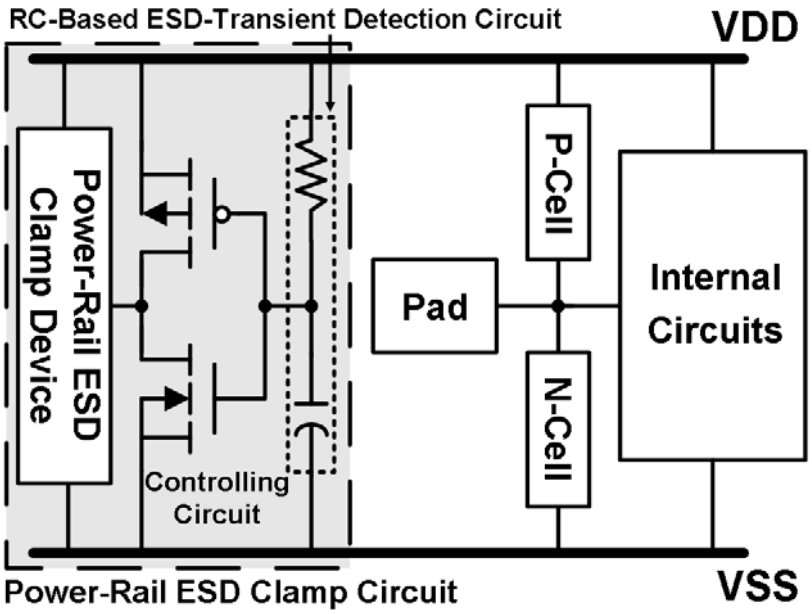


Fig. 1.8. The ESD protection circuit for analog I/O pin. The protection circuit includes the P-cell, N-cell, and power rail ESD clamp circuit.

In addition, as the ultra-large-scale-integrated (ULSI) circuits being continually developed toward system-on-chip (SoC) applications, more and more multiple separated power domains are used in a SoC IC for specified circuit functions, such as digital/analog circuit blocks, mixed-voltage circuit blocks, and power management considerations, as shown in Fig. 1.9. However, the IC products with multiple separated power domains often have more unexpected current paths during ESD stresses and easily cause damages across interface circuits between different power domains beyond the ESD protection circuits of I/O cells [33]-[37], as presented in Fig. 1.10. Such ESD failures across interface circuits between different power domains are often difficult to be clearly examined and revised, even with a lot of failure analysis procedures. Several cross-power-domain ESD protection designs had been studied and proposed to avoid ESD damages on the interface circuits between two separated power domains [33]-[38]. The bi-directional diode connection had been generally used to connect the separated power or ground pins in different power domains, as shown in Fig. 1.11. The bi-directional diode connection can construct the completely whole-chip ESD current discharging paths under cross-power-domain ESD stresses [39], [40]. According to the previous studies [40]-[42], the overstress voltages across the interface circuits between separated power domains easily caused the ESD damages, such as gate oxide damage, junction filament, and contact destroy under cross-power-domain ESD stresses.

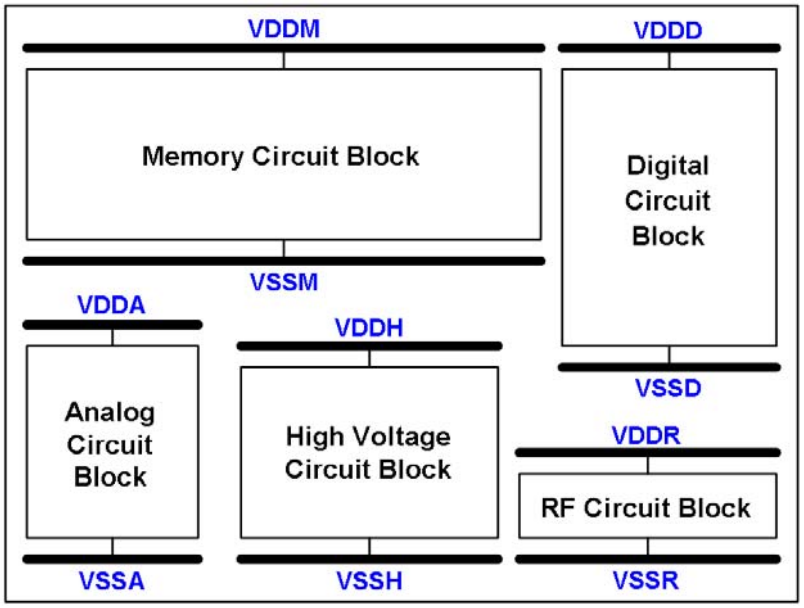


Fig. 1.9. The integrated circuits are continually developed toward system-on-chip (SoC) applications. Multiple separated power domains are used in a SoC IC for specified circuit functions.

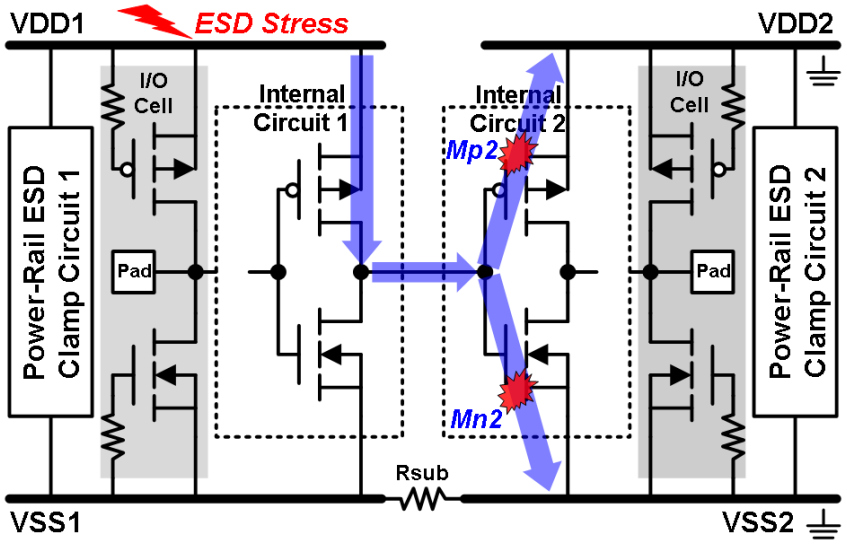


Fig. 1.10. Interface circuits across separated power domains are easily damaged under cross-power-domain ESD stresses.

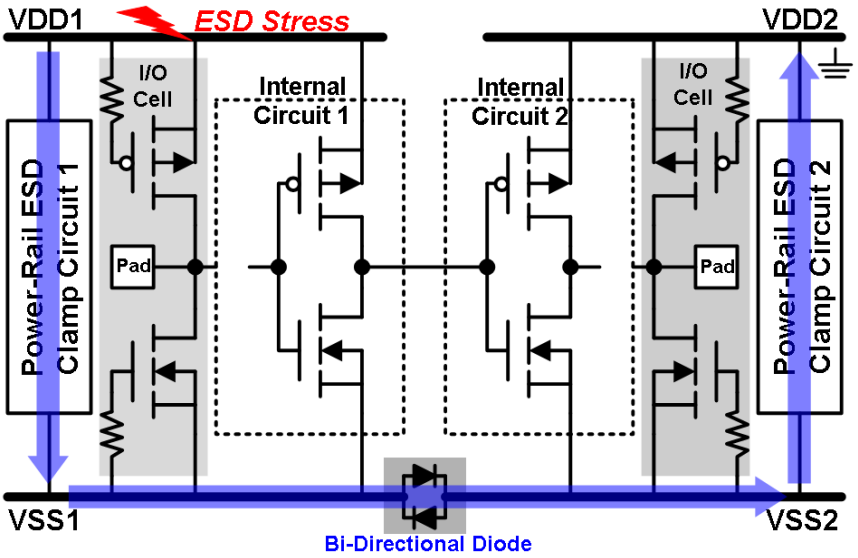
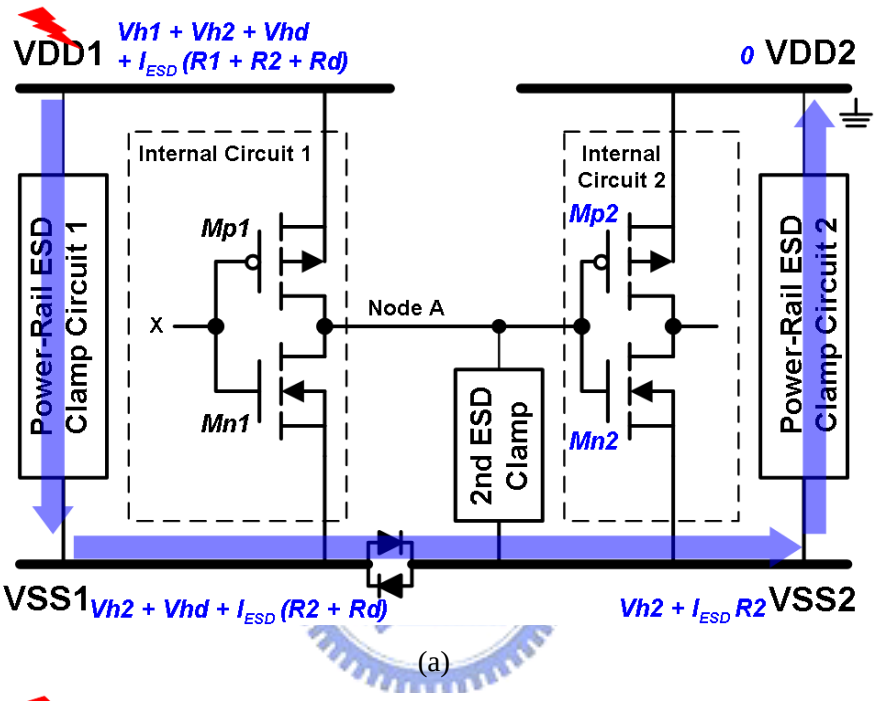


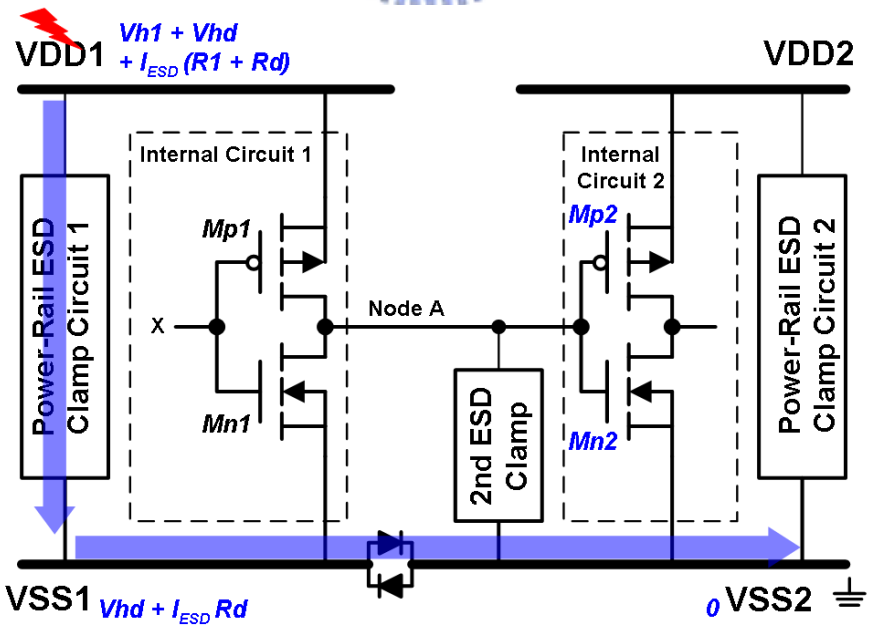
Fig. 1.11. Bi-directional diode connection had been generally used to connect the separated power or ground pins in different power domains.

When the ESD voltage was applied on the VDD1 and grounded VDD2 under the cross-power-domain ESD stresses, the ESD current can be discharged from the VDD1 to the VSS1 by the power-rail ESD clamp circuit 1 in the power domain one, from the VSS1 to the VSS2 through the inserted bi-directional diode connection, and then from the VSS2 to the grounded VDD2 through the other power-rail ESD clamp circuit 2 in the power domain two, as the discharged path shown by dashed line in Fig. 1.12(a). The Vh1 and Vh2 are the holding voltage of the power-rail ESD clamp circuits 1 and 2, respectively. Then, the Vhd is the holding voltage of the bi-directional diode connection between the separated power domains.

Among the parameters, the R1, R2, and Rd are the turn-on resistances of the power-rail ESD clamp circuits 1, 2, and the bi-directional diode connection, respectively. When the ESD current was conducted by this long discharging path, it would induce the overstress voltage across the each MOS transistor in interface circuits between separated power domains [40]-[42]. The induced voltage drops with discharging ESD currents from VDD1 to VDD2 on each node of the interface circuit had been estimated, as shown in Fig. 1.12(a).



(a)



(b)

Fig. 1.12. The estimations of the induced voltage potential under the cross-power-domain (a) VDD1-to-VDD2, and (b) VDD1-to-VSS2, ESD stresses.

The voltage potential at node A could be raised up to the VDD1 because the driver's PMOS transistor (Mp1) had an initially floating gate situation. The highest voltage drop was applied across the gate oxide of the receiver's PMOS transistor (Mp2) in interface circuits under the VDD1 to VDD2 ESD stresses. On the other hand, the highest voltage drop was also generated across the gate oxide of the receiver's NMOS transistor (Mn2) in interface circuits under the VDD1 to VSS2 ESD stresses. The similar estimation on voltage drops during ESD stress was presented in Fig. 1.12(b). As the CMOS technologies being continually shrunk toward nanometer scales, the breakdown voltages of ultra-thin gate oxide in the MOS transistors were sharply reduced to impact the ESD protection designs. It was important to avoid the gate oxide damages of the MOS transistors in the interface circuits by ESD-current induced overstress voltages. Therefore, the second ESD clamp (2^{nd} ESD clamp) designs had been applied to reduce the overstress voltages across the interface circuits, as shown in Figs. 1.12(a) and 1.12(b). Furthermore, the 2^{nd} ESD clamp with desired trigger mechanism [38], [40]-[42] also had been proposed to rapidly and efficiently clamp the overstress voltages across the interface circuits between separated power domains, especially in the integrated circuits with nanoscale CMOS technology.

1.3. Organization of This Dissertation

To overcome the challenges in ESD protection design for power-rail ESD clamp circuits, analog I/O interface circuits, and cross-power-domain interface circuits in deep-submicron and nanoscale CMOS integrated circuits, several new designs are developed and verified in this dissertation. This dissertation comprises eight chapters. In Chapter 2, the comparison of the controlling circuit implemented with 1-stage or 3-stage inverters has been presented [43]. Then, the drain-contact-to-poly-gate spacing (D) of the main ESD clamp NMOS transistor has been also split in order to investigate the influence of this spacing on the ESD protection capability. In Chapter 3, an efficient ESD-transient detection circuit with capacitance coupling mechanism has been proposed to accomplish the desirable function on commanding the main ESD clamp NMOS transistor. A novel initial-on SCR design is proposed to achieve the lowest trigger voltage and the highest turn-on efficiency of SCR device in Chapter 4. Chapter 5 further discusses optimizations on the initial-on SCR devices are presented [44]-[46]. The modified initial-on SCR device with merged layout style is also proposed to enhance its ESD protection capability. Besides ESD protection design for power-rail ESD clamp circuit, the comparison among different ESD protection designs for analog I/O

interface circuits is presented [47] in Chapter 6. A new active ESD protection design for the interface circuits between separated power domains is proposed [48] in Chapter 7. Chapter 8 gives the conclusions and future works of this dissertation. The outlines of each chapter are summarized below.

Chapter 2 presents the comparison between 1-stage and 3-stage inverters in the controlling circuits. The circuit performances of both controlling circuits in power-rail ESD clamp circuits are measured and compared under ESD-stress conditions and normal circuit operation conditions. On the other hand, the drain-contact-to-poly-gate spacing (D) of the main ESD clamp NMOS transistor has been also split from 0.25 μm to 2.0 μm in order to investigate the influence of this spacing on the ESD protection capability. Through the arranged combinations of different controlling circuits and main ESD clamp NMOS transistors in different layout styles, the influence can be thoroughly investigated from the characteristic and performance of each power-rail ESD clamp circuit in silicon. The optimized circuit scheme for controlling circuits and layout style for the main ESD clamp NMOS transistors can be suggested for using in the power-rail ESD clamp circuits.

In Chapter 3, an efficient ESD-transient detection circuit has been proposed and verified in 130-nm 1.2-V CMOS technology. This design abandons the feedback circuit techniques and adopts capacitance coupling mechanism to accomplish the desirable function on commanding the main ESD clamp NMOS transistor. Through experimental measurements, such as turn-on verification, transmission line pulse (TLP) stress, ESD stress, and fast power-on test, this power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit presents an excellent performance to meet the specified requirements. According to the measured results, the new proposed ESD-transient detection circuit possesses the sufficient turn-on duration under the ESD-stress conditions and high mis-trigger and latch-on immunities under the fast power-on conditions.

In Chapter 4, a novel initial-on SCR design is proposed to achieve the lowest trigger voltage and the highest turn-on efficiency of SCR device for effective on-chip ESD protection. Without using the special native device or any process modification, this initial-on SCR design is realized by circuit skill with the PMOS transistor and RC-based ESD-transient detection circuit in general CMOS processes. This initial-on SCR design, which is implemented by PMOS-triggered SCR device cooperated with RC-based ESD-transient detection circuit, also presents a high enough holding voltage in a fully-silicided 0.25-μm CMOS process to avoid latchup issues in normal circuit operation conditions. Such initial-on

SCR devices can achieve the whole-chip ESD protection scheme for input, output, power-rail ESD clamp circuit, and the ESD clamp cells between the separated power domains.

Chapter 5 presents further optimizations on the PMOS-triggered SCR devices. The modified PMOS-triggered SCR device with merged layout style is proposed to further enhance its ESD protection capability. In addition, NMOS transistors are also embedded into the SCR structures to implement NMOS-triggered SCR devices. The device characteristics of these two different MOS-triggered SCR devices are compared to optimize the on-chip ESD protection design in CMOS ICs. Moreover, the obvious differences on the Vh of NMOS-triggered SCR devices under DC and TLP measurements have been attributed to the current distributions through the parasitic npn bipolar transistor in the SCR device.

In Chapter 6, different ESD protection designs for the analog I/O pin are compared to find the optimal ESD protection circuit for the analog I/O interface circuit in 0.18-μm 1.8-V/3.3-V CMOS technology. In addition, the failure analyses on both 1.8-V and 3.3-V analog I/O pins are presented after ND-mode and PS-mode ESD stresses. In the ESD protection designs with MOS devices, ESD robustness is dominated by the ESD levels of GGNMOS or GDPMOS under the PS-mode or ND-mode ESD stresses. However, the failure mechanism is different from the ESD protection design with pure diodes under PS-mode or ND-mode ESD stresses. Besides, an unexpected failure mechanism has been found in the analog I/O pin with the pure-diode ESD protection circuit. The parasitic npn bipolar transistor formed by the N+ diode and the N-well guard ring structure provides the ESD current path during the ND-mode ESD stress, which causes a low ESD level to the analog I/O pin.

The cross-power-domain ESD issues are investigated in Chapter 7. First, a failure study in a 0.35-μm 3.3 V/5 V mixed-mode CMOS IC product with two separated power domains is presented. The ESD failure spots were specially observed at the interface circuits between the separated power domains after ND-mode MM ESD stress of 100 V. However, this IC product has 2-kV HBM ESD robustness in each ESD test combination of I/O pin to power/ground pins. Therefore, the efficient ESD protection designs should be applied on the interface circuits between the separated power domains against such cross-power-domain ESD stresses. Secondly, several active cross-power-domain ESD protection designs were reviewed to compare their ESD protection strategies for interface circuits between separated power domains. Besides, one new active ESD protection design for the interface circuits between separated power domains has been also proposed to solve the interface circuit damages under cross-power-domain ESD stresses. This ESD protection design has been implemented by

PMOS and NMOS transistors with the ESD-transient detection function in a 0.13-μm 1.2-V CMOS technology. It can be rapidly triggered on and efficiently reduced the overstress voltages across the gate oxides of the MOS transistors of the receivers in interface circuits between separated power domains under the cross-power-domain ESD stresses. The proposed ESD protection design for the interface circuits between separated power domains has been successfully verified with 4-kV HBM and 400-V MM ESD robustness against cross-power-domain ESD stresses.

Chapter 8 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in this chapter.

Chapter 2

Evaluation on NMOS-Based Power-Rail ESD Clamp Circuits with Gate-Driven Mechanism

In this chapter, two different circuit schemes for the controlling circuit in power-rail ESD clamp circuit are compared. The circuit performances of two controlling circuits, which are respective implemented by 1-stage inverter and 3-stage inverters, in power-rail ESD clamp circuits are measured and compared under ESD-stress conditions and normal circuit operation conditions. In addition, the layout style of the main ESD clamp NMOS transistor has been also studied in order to investigate the influence of this spacing on the ESD protection capability. Through the eight arranged combinations of two different controlling circuits and main ESD clamp NMOS transistors in four different layout styles, the influence can be thoroughly investigated from the characteristic and performance of each power-rail ESD clamp circuit in silicon. Moreover, the impact of the fast power-on application [10], [11] or the transient noise on power/ground lines [20], [21] on the power-rail ESD clamp circuits has been also discussed in this chapter. According to these experimentally measured results, the optimal circuit scheme for controlling circuit and layout style for the main ESD clamp NMOS transistor can be suggested for using in the power-rail ESD clamp circuit.

2.1. Power-Rail ESD Clamp Circuits with Different Controlling Circuits and Layout Styles for Main ESD Clamp NMOS

2.1.1. Influence of the RC-Time Constants

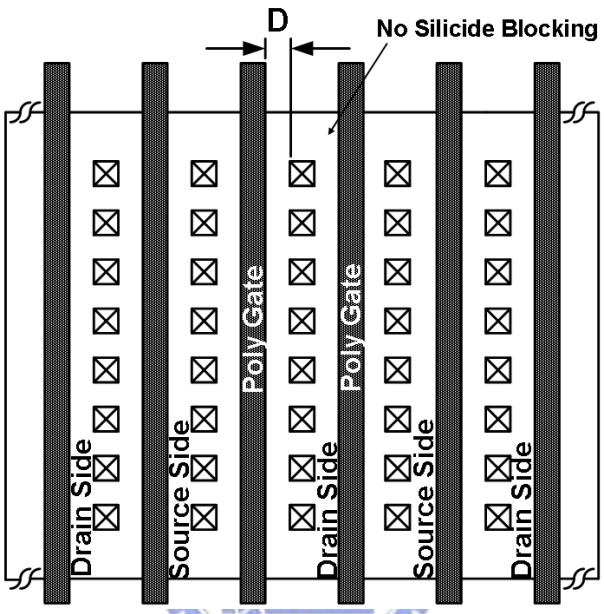
It has been studied and reported that the RC-time constants of the RC-based ESD-transient detection circuits made an impact on the ESD robustness of the power-rail ESD clamp circuits. In a previous work [49], all main ESD clamp NMOS transistors were drawn as the BFETs with the drain-contact-to-poly-gate spacings from 0.22 μm to 0.44 μm and no silicide blocking on the diffusions. The total channel widths of those BFETs were

identically 2000 μm. However, they occupied different silicon areas. According to the measured results in that previous work, the ESD robustness were not significantly improved or enhanced by increasing the RC-time constant from 0.1 μs to 1.0 μs. Furthermore, the longest RC-time constant of 1.0 μs could slightly induce some degradation on ESD robustness of the power-rail ESD clamp circuit. But, the drain-contact-to-poly-gate spacings have strong impact to ESD robustness of the NMOS-based power-rail ESD clamp circuits under the same RC-time constant. The ESD robustness can be efficiently increased by increasing the drain-contact-to-poly-gate spacings among all RC-time constants. However, the large drain-contact-to-poly-gate spacings will enlarge the total occupied silicon areas of the main ESD clamp NMOS transistors. Based on the practical applications of the standard I/O cell libraries, each I/O cell (such as input pin, output pin, VDD pin, and VSS pin) was usually required to possess a rigid cell space in order to easily and automatically arrange these pins in chip layout. In general, the VDD pin (or VSS pin) was included the power-rail ESD clamp circuit to provide the ESD protection between VDD and VSS. Therefore, the power-rail ESD clamp circuit which consists of the RC-based ESD-transient detection circuit, the controlling circuit, and the main ESD clamp NMOS transistor must be restrained into an established silicon area to match the rigid cell space. According to the measured results in that previous study [49], because the influences of the RC-time constant from 0.1 μs to 0.5 μs on ESD robustness were not significant, the RC-time constant has been fixed at 0.2 μs in this work to reduce the occupied silicon area of the resistor and capacitor in this testchip.

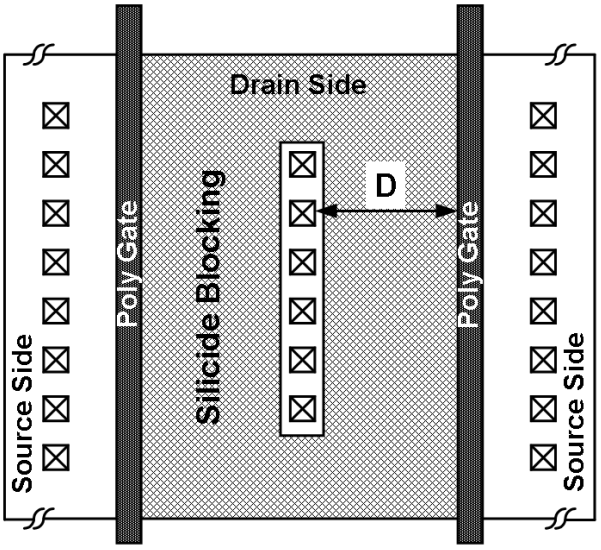
2.1.2. Controlling Circuits and Layout Styles

Both controlling circuits, which are the 1-stage inverter and the 3-stage inverters, are respectively arranged to command the main ESD clamp NMOS transistors with different drain-contact-to-poly-gate spacings. One of the main ESD clamp NMOS transistors has the layout style with minimized drain-contact-to-poly-gate spacing (D) and no silicide blocking (SB) on its diffusion, as shown in Fig. 2.1(a). This NMOS transistor, which is the Big FET (BFET), will be expected to have no snapback operation. However, another one has a totally different layout style with extended drain-contact-to-poly-gate spacing (D) and silicide blocking (SB) on its diffusion, as shown in Fig. 2.1(b). It is a traditional ESD clamp NMOS transistor with snapback operation. It has been proven that the parasitic npn bipolar transistor was turned on to induce the snapback operation in such ESD clamp NMOS transistor [4], [5]. The drain-contact-to-poly-gate spacings of the BFET and traditional ESD clamp NMOS

transistors are 0.25 μm and 2.0 μm, respectively. Besides, different layouts on the main ESD clamp NMOS transistor, called the modification design in this work, with a drain-contact-to-poly-gate spacing of 0.75 μm has been also implemented in the testchip with or without silicide blocking on its drain-side diffusion. Through such splits in layout, the influences of the drain-side equivalent resistance on circuit performance and ESD robustness can be used to judge the optimal layout style for the main ESD clamp NMOS transistor.



(a)



(b)

Fig. 2.1. The main ESD clamp NMOS transistor has (a) the BFET layout style with the drain-contact-to-poly-gate spacing (D) of 0.25 μm and no silicide blocking (SB) on its diffusions, and (b) the traditional layout style with the D of 2.0 μm and SB on its drain-side diffusions.

The eight designs of power-rail ESD clamp circuits from the combinations of the main ESD clamp NMOS transistor in different layout styles and the controlling circuit with different inverter stages have been drawn in the testchip for comparison, as shown in Table 2.1. For comparison purpose, the layout areas of the main ESD clamp NMOS transistors among those eight designs are kept the same in layout. Therefore, the total channel width of the traditional ESD clamp NMOS transistor is 624 μm, whereas that of the BFET is about 2600 μm. The total channel width of main ESD clamp NMOS transistor with the drain-contact-to-poly-gate spacing of 0.75 μm is 1144 μm. In addition, the RC time constant in those eight designs are all kept at 200 ns. This testchip has been fabricated in a 0.13-μm 1.2-V CMOS process.

Table 2.1

Eight Designs of the Power-Rail ESD Clamp Circuits Verified in this Work

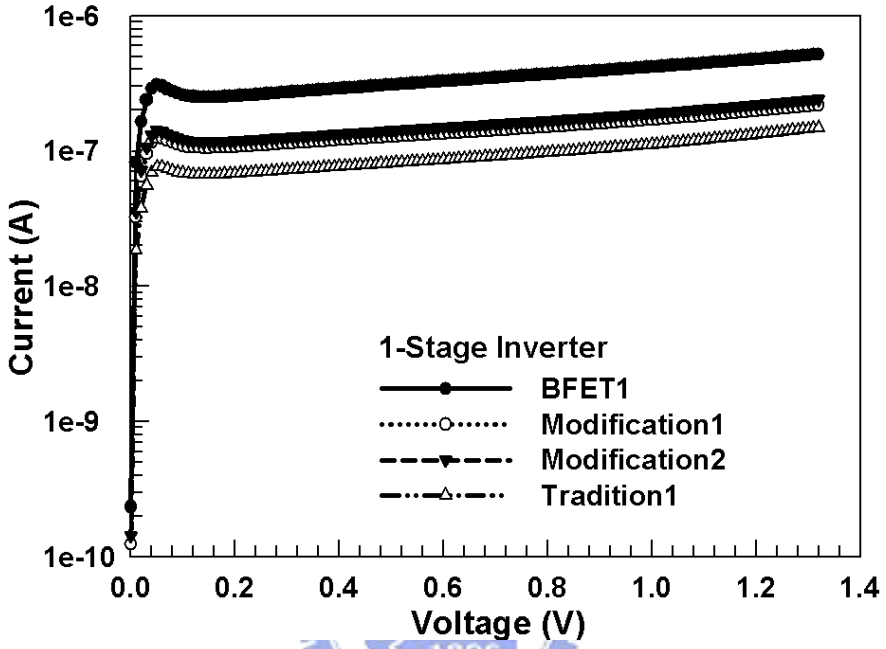
<table>
<tr><th rowspan="2">Design</th><th rowspan="2">Controlling Circuit</th><th colspan="2">Main ESD Clamp NMOS</th></tr>
<tr><th>Drain-Contact-to -Poly-Gate Spacing (D)</th><th>Silicide Blocking (SB)</th></tr>
<tr><td>Tradition1</td><td>1-Stage Inverters</td><td rowspan="2">2.0 μm</td><td rowspan="2">Yes</td></tr>
<tr><td>Tradition2</td><td>3-Stage Inverter</td></tr>
<tr><td>Modification1</td><td rowspan="2">1-Stage Inverters</td><td rowspan="4">0.75 μm</td><td>No</td></tr>
<tr><td>Modification2</td><td>Yes</td></tr>
<tr><td>Modification3</td><td rowspan="2">3-Stage Inverter</td><td>No</td></tr>
<tr><td>Modification4</td><td>Yes</td></tr>
<tr><td>BFET1</td><td>1-Stage Inverters</td><td rowspan="2">0.25 μm</td><td rowspan="2">No</td></tr>
<tr><td>BFET2</td><td>3-Stage Inverter</td></tr>
</table>

2.2. Experimental Results in Component-Level Tests

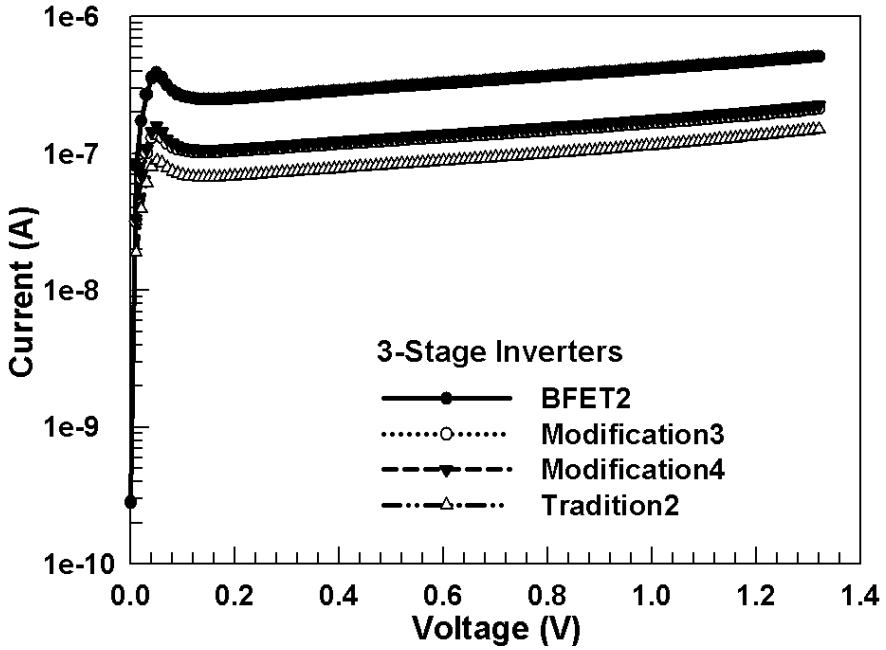
2.2.1. DC Leakage Current

Power-rail ESD clamp circuits must be kept off to avoid unnecessary VDD-to-VSS leakage current under normal circuit operation conditions. However, the main ESD clamp

NMOS transistors always have huge device dimension to achieve the required ESD robustness. Thus, they will be some concern on leakage, especially in the nanoscale CMOS technology. The leakage currents of the power-rail ESD clamp circuits with controlling circuits of 1-stage inverter and 3-stage inverters in are shown in Figs. 2.2(a) and 2.2(b), respectively.



(a)



(b)

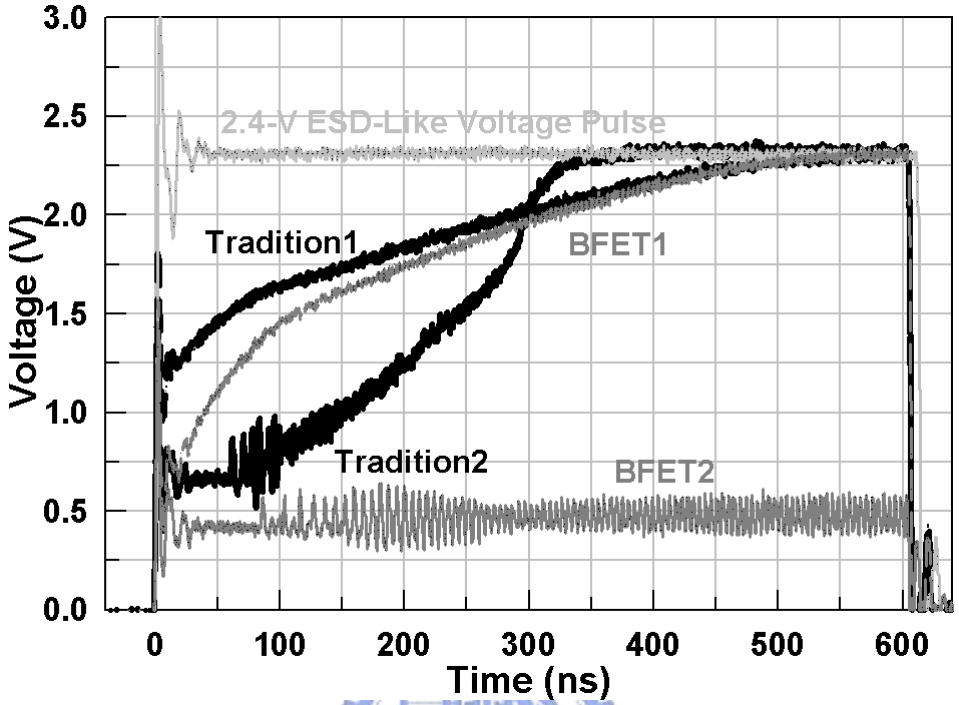
Fig. 2.2. DC leakage currents among the power-rail ESD clamp circuits of different designs with controlling circuit of (a) with 1-stage inverter and (b) 3-stage inverters.

There is no obvious difference on the leakage currents between the power-rail ESD clamp circuits with different controlling circuits under the identical main ESD clamp NMOS transistor. The leakage currents of BFET1 (or BFET2) are 0.5 μA under the VDD bias of 1.2 V, whereas those of Tradition1 (or Tradition2) are below 0.15 μA at the same VDD bias. In addition, no significant difference of the leakage currents is observed between the main ESD clamp NMOS transistor with or without silicide blocking (SB) on its diffusion, as illustrated in the measured results of Modification1 and Modification2 (or Modification3 and Modification4). According to the measured results, the leakage currents of Tradition1 and Trdition2 are 3-times less than those of BFET1 and BFET2 due to the large channel widths in BFET1 and BFET2. Therefore, the leakage current of the power-rail ESD clamp circuit is strongly dependent on the channel width of the main ESD clamp NMOS transistor.

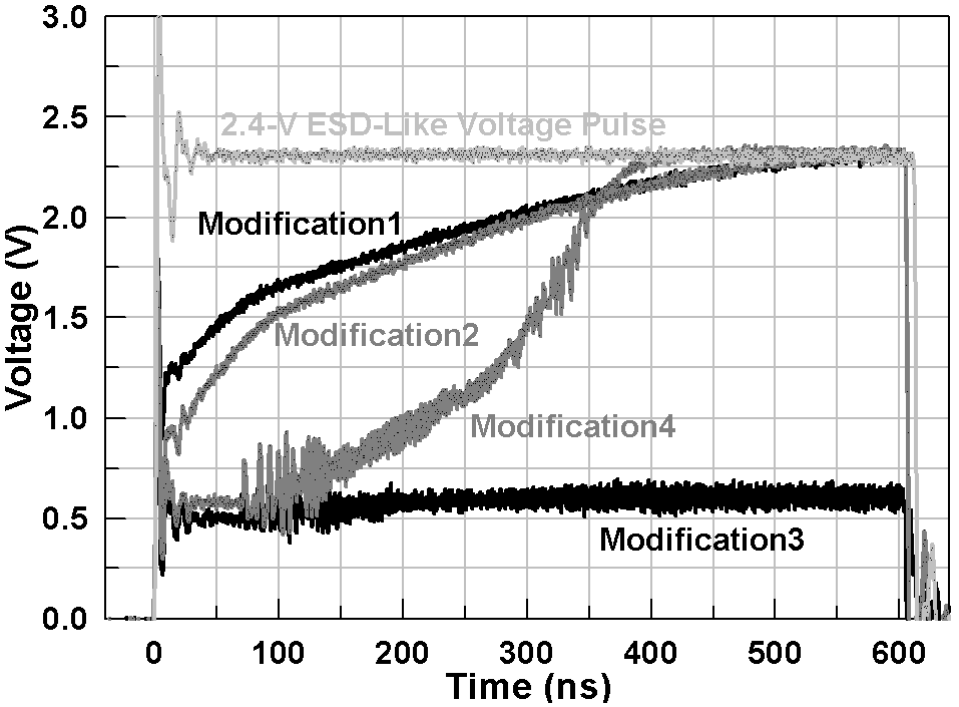
2.2.2. Turn-On Verification under ESD-Like Stress Condition

To observe the turn-on efficiency among the different power-rail ESD clamp circuits, a 2.4-V ESD-like voltage pulse with 2-nano-seconds (ns) rise time is applied on the VDD terminal with VSS terminal grounded in each circuit. The voltage pulse with a rise time of 2 ns and duration of 600 ns generated from a pulse generator is used to simulate the fast rising edge of HBM ESD event [1]. The sharp-rising edge of the ESD-like voltage pulse will be detected by the RC-based ESD-transient detection circuit and then to turn on the main ESD clamp NMOS transistor. When the main ESD clamp NMOS is turned on, the voltage waveform on VDD node will be clamped as the measured results shown in Figs. 2.3(a) and 2.3(b). Tradition1 and BFET1, both of which have 1-stage inverter in the controlling circuits, presented similar voltage waveforms under 2.4-V ESD-like voltage pulses. Besides, Tradition2 clamped the overshoot voltage pulses to a lower voltage level during the first 300 ns of the ESD-like voltage pulses. However, the BFET2 performs an excellent ability to clamp the overshoot voltage pulse to a much lower voltage level, as shown in Fig. 2.3(a). On the other hand, the influences of drain-side silicide blacking on turn-on behaviors of the power-rail ESD clamp circuits have been measured in Fig. 2.3(b). Under the same drain-contact-to-poly-gate spacings of 0.75 μm, Modification3 exhibits the best turn-on efficiency among other designs. Besides, the turn-on efficiency of Modification4 is higher than that of Modification1 and Modification2 during the first 350-ns pulse duration. According to the measured results, the controlling circuit with 3-stage inverters seems to be an optimal candidate to implement the main ESD clamp NMOS transistor with BFET layout

style in the power-rail ESD clamp circuit. The controlling circuit would hold a dominant factor on the turn-on behaviors of the power-rail ESD clamp circuit.



(a)

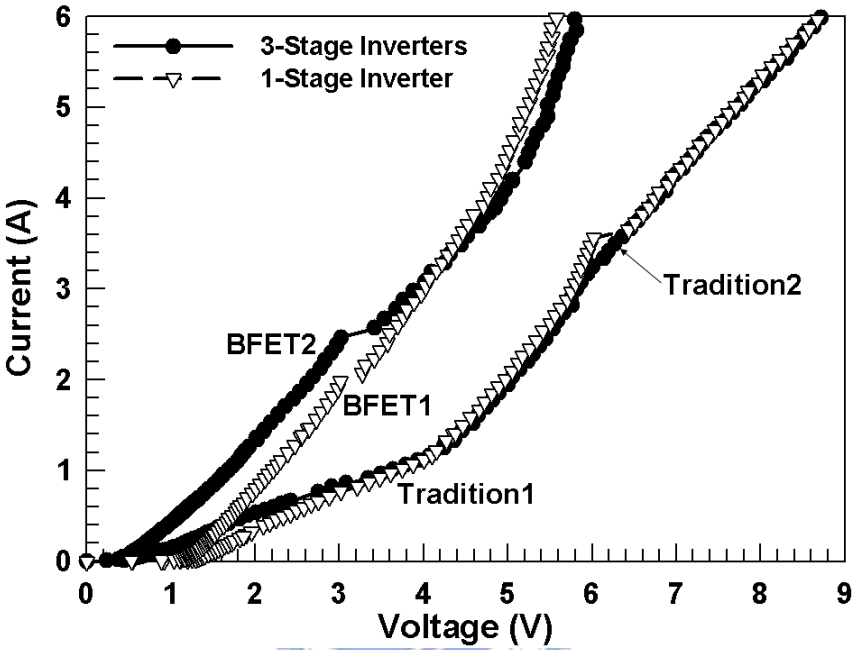


(b)

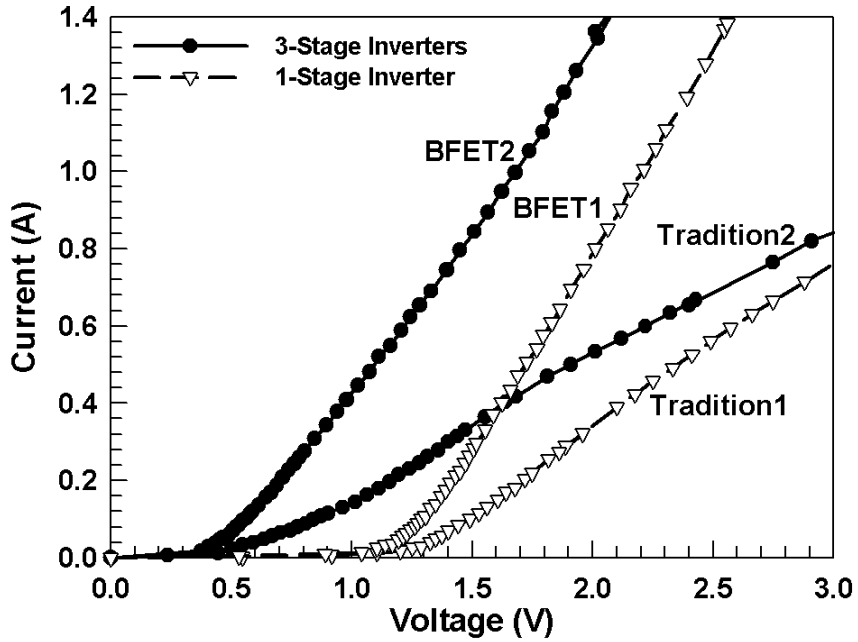
Fig. 2.3. The measured voltage waveforms of (a) Tradition1, Tradition2, BFET1, and BFET4, and of (b) Modification1, Modification2, Modification3, and Modification4, under 2.4-V ESD-like voltage pulses with 2-ns rise time.

2.2.3. TLP I-V Characteristics and HBM ESD Robustness

The Transmission Line Pulse (TLP) [50] measured I-V characteristics of the power-rail ESD clamp circuits are shown in Figs. 2.4(a), 2.4(b), 2.5(a), and 2.5(b). This TLP system has a 100-ns pulse width and 10-ns rise time.

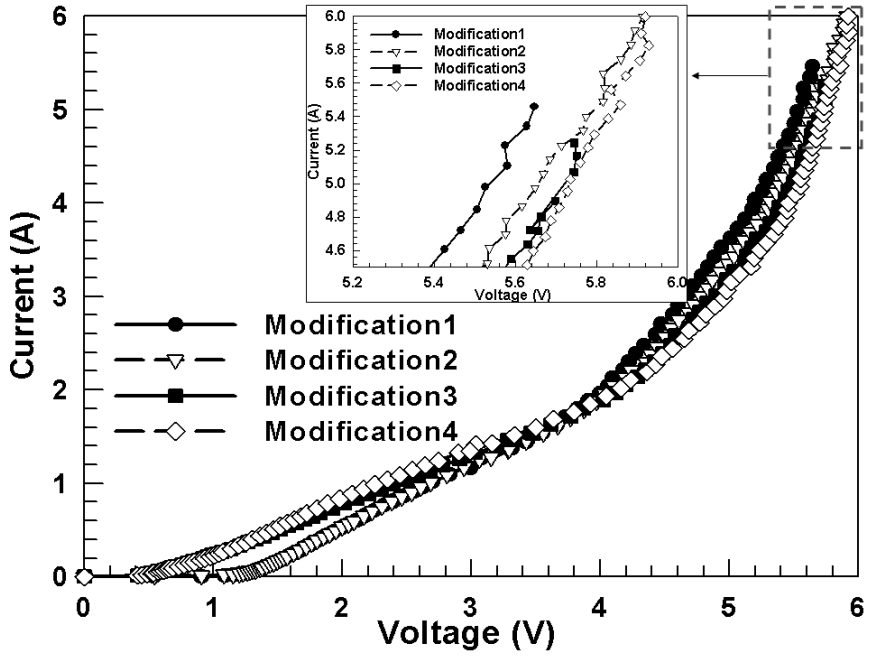


(a)

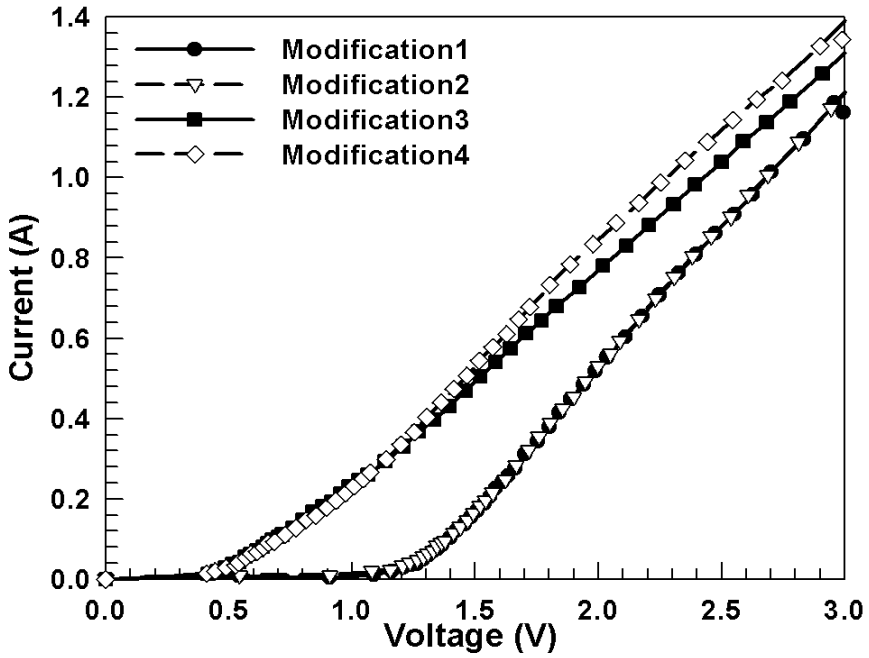


(b)

Fig. 2.4. (a) The TLP I-V curves of Tradition1, Tradition2, BFET1, and BFET2. (b) The zoomed-in view of (a) around the low-current region.



(a)



(b)

Fig. 2.5. (a) The TLP I-V curves of Modification1, Modification2, Modification3, and Modification4. (b) The zoomed-in view of (a) around the low-current region.

In Fig. 2.4(a), the TLP I-V curves can be simply discriminated between the main ESD clamp NMOS transistors with traditional or BFET layout styles. Although the second breakdown currents (It2) of these four designs can achieve over 6 A, the difference of on resistance (Ron) clearly distinguished the designs with traditional main ESD clamp NMOS transistor from those with BFET. Due to smaller total channel widths in Tradition1 and

Tradition2, their clamp voltage (Vclamp) and Ron are signification higher than those of BFET1 and BFET2. Higher Vclamp and Ron in Tradition1 and Tradition2 easily induced some damages to the internal circuits. In addition, the TLP I-V curves of Tradition1 and Tradition2 presented obvious two-stage Ron in Fig. 2.4(a). The phenomenon of two-stage Ron can be attributed to the changes of the discharging paths. The currents were conducted through the channel of the main ESD clamp NMOS transistor under the low current region, and they would be discharged by the parasitic npn bipolar transistor of the main ESD clamp NMOS transistor [18]. Moreover, the controlling circuits with 3-stage inverters can enhance the turn-on efficiency, such as lower trigger voltage (Vt1) and smaller on resistance, especially under the low current region in both traditional and BFET designs, as shown in Fig. 2.4(b). It was ever reported that the higher Vt1 and insufficient turn-on duration in the ESD devices will induce some damages to interface circuits [51]. The enhancement of the turn-on efficiency is more emphasized on the design with the controlling circuit of 3-stage inverter cooperated with BFET. However, the influence of the different controlling circuits with 3-stage inverters and 1-stage inverter on the turn-on efficiency is gradually indistinct under the high current region. When the measured current is over ~ 2.5 A, no obvious difference of Vclamp between BFET1 and BFET2, both of which have the total channel widths of 2600 μm, is observed in Fig. 2.4(a). The phenomenon can be also attributed to the changes of the discharging paths. Under such high current region, the huge current can not be totally discharged by the channel of the main ESD clamp NMOS transistor. The parasitic npn bipolar transistor would be triggered on to discharge huge current. Therefore, the gate-driven enhancement by the 3-stage inverters will disappear under the high current region.

The similar measured results also can be observed in Modification1, Modification2, Modification3, and Modification4. Figs. 2.5(a) and 2.5(b) present the TLP I-V curves of the power-rail ESD clamp circuits with silicide blocking or without silicide blocking diffusions in the main ESD clamp NMOS transistor under the drain-contact-to-poly-gate spacing of 0.75 μm. These four TLP I-V curves have the similar trends, especially in the high current range. The trigger voltages of Modification3 and Modification4 are lower than those of Modification1 and Modification2. The second breakdown currents (It2) of the designs with silicide blocking (Modification2 and Modification4) are higher than those without silicide blocking (Modification1 and Modification3), as shown in the insert of Fig. 2.5(a). The influence of the drain-side silicide blocking on the Ron and Vclamp is not obvious, as illustrated in Figs. 2.5(a) and 2.5(b). According to the TLP measured results, the design

scheme of controlling circuit would affect the trigger voltage of the power-rail ESD clamp circuit. However, the on resistance and Vclamp would be dominated by the drain-side layout style in the main ESD clamp NMOS transistor.

The HBM ESD robustness of the eight different power-rail ESD clamp circuits are listed in Table 2.2. The power-rail ESD clamp circuit with design of BFET2 sustains the highest HBM ESD stress of 7 kV. However, the ESD robustness of Tradition2 is below 6 kV. The four designs with the drain-contact-to-poly-gate spacing of 0.75 μm have the similar ESD robustness from 5.5 kV to 6.0 kV. The ESD robustness of these four designs do not have significant enhancement by depositing silicide blocking oxide layer on their drain-side diffusions of the main ESD clamp NMOS transistors or by adopting 3-stage inverters in the controlling circuit.

Table 2.2

HBM ESD Robustness of the Eight Power-Rail ESD Clamp Circuits

Designs	HBM	
	Positive	Negative
Tradition1	6.5 kV	> 8.0 kV
Tradition2	5.5 kV	> 8.0 kV
Modification1	5.5 kV	> 8.0 kV
Modification2	6.0 kV	> 8.0 kV
Modification3	6.0 kV	> 8.0 kV
Modification4	5.5 kV	> 8.0 kV
BFET1	6.5 kV	> 8.0 kV
BFET2	7.0 kV	> 8.0 kV

A faint relation between the ESD robustness and the controlling circuits (or the layout style of the main ESD clamp NMOS transistor) is summarized in Table 2.2. The 3-stage inverters in controlling circuit could be suitable for the main ESD clamp NMOS transistor

without silicide blocking on its diffusion. Such an NMOS transistor has a lower parasitic resistance on its surface channel. However, the controlling circuit with 3-stage inverters would induce some degradation on ESD robustness of the designs with drain-side silicide blocking in the main ESD clamp NMOS transistor. Therefore, based on the measured results of the TLP I-V characteristics and HBM ESD robustness, the 3-stage inverters in controlling circuit did not have improvement for the power-rail ESD clamp circuits in nanoscale CMOS technology.

2.2.4. Power-On Condition and Normal Circuit Operation Condition

In general, the normal VDD power-on voltage waveform of CMOS ICs has a rise time in the order of milli-second (ms). Due to such a slow rise time in normal power-on conditions, the ESD-transient detection circuit with a RC time constant of ~μs can distinguish the power-on signal to keep the main ESD clamp NMOS transistor off. All of the power-rail ESD clamp circuits studied in this work can successfully achieve this desired task under normal power-on conditions. However, the power-rail ESD clamp circuits with RC-based ESD transient detection circuits were easily mis-triggered to cause themselves into a “latch-on” state, which the potential on VDD node will be continuously clamped at a lower voltage, under some abnormal fast power-on conditions [10], [11] or transient noise on VDD power lines [20], [21]. In this work, the eight different power-rail ESD clamp circuits were verified by a 1.2-V voltage pulse with 100-ns rise time, which is used to simulate the abnormal fast power-on condition, to investigate their immunities from the mis-trigger and latch-on state. The measured results are respectively shown in Figs. 2.6 and 2.7. Unfortunately, the power-rail ESD clamp circuits with 3-stage inverters in controlling circuit present the worse immunity for mis-trigger under the 1.2-V fast power-on test conditions. BFET2 will be mis-triggered on to enter latch-on state under the 1.2-V fast power-on test condition. The voltage waveform is clamped at a very low voltage level around 0.3 V to 0.6 V, as illustrated in Fig. 2.6. Such phenomenon is much harmful for the applications of the power-rail ESD clamp circuits in real IC products. Besides, Modification3 also presents a similar measured result to that of BFET2. Tradition2 and Modification4, both of which have the silicide blocking on their drain sides, will be mis-triggered at the first 250 ns and first 420 ns, respectively, under the 1.2-V fast power-on test condition with 100-ns rise time. However, all of designs with 1-stage inverter in the controlling circuit, such as Tradition1, BFET1, Modification1, and Modification2, exhibit the higher mis-trigger immunity under this 1.2-V

fast power-on test condition. Their voltage waveforms can follow up with the fast power-on voltage waveforms, as presented in Figs. 2.6 and 2.7.

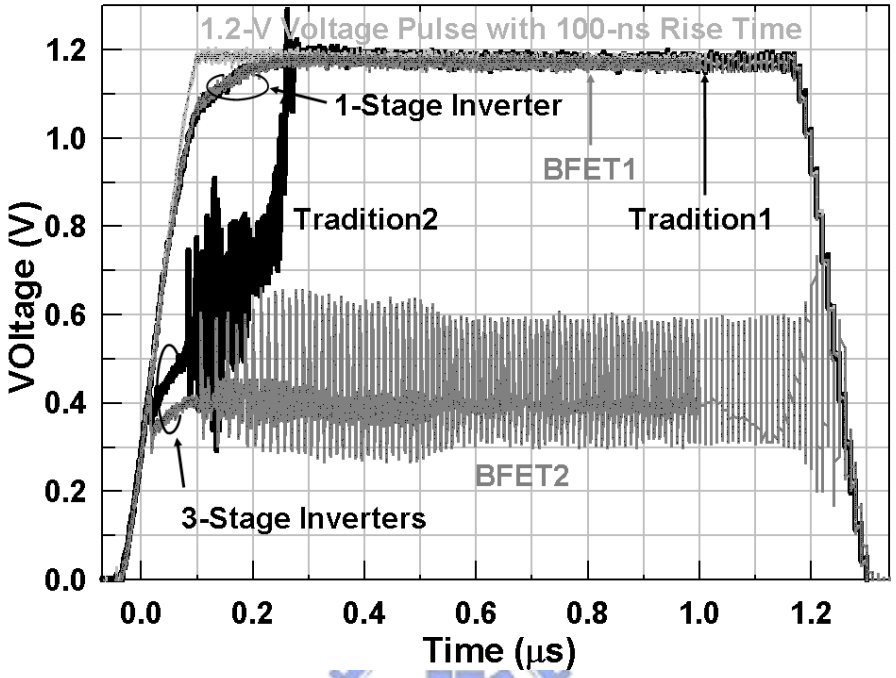


Fig. 2.6. The measured voltage waveforms of Tradition1, Tradition2, BFET1, and BFET2 under the 1.2-V fast power-on condition with 100-ns rise time.

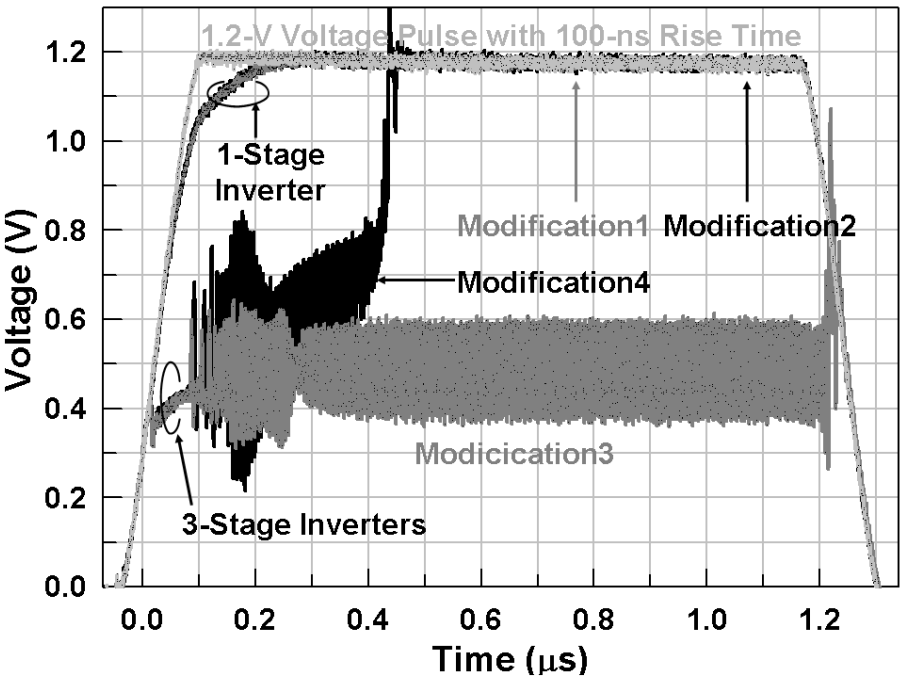


Fig. 2.7. The measured voltage waveforms of Modification1, Modification2, Modification3, and Modification4 under the 1.2-V fast power-on condition with 100-ns rise time.

Although the 3-stage inverters for controlling circuit would enhance the gate-driven ability to slightly increase the ESD robustness and decrease Vclamp (and Ron), they will dramatically degrade the immunity against mis-trigger and latch-on issues under the fast power-on condition. Based on the aforementioned results, the controlling circuits with 1-stage inverter should be the optimal choice among the power-rail ESD clamp circuits with RC-based ESD-transient detection circuit.

2.3. Experimental Results in System-Level Test

2.3.1. Electrical Fast Transient (EFT) Test

The reliability of microelectronic products has been put more emphasis on the electromagnetic compatibility (EMC). In order to avoid the occurrence of the malfunction and mis-trigger during normal system operation conditions, the on-chip ESD protection circuits also has been required to meet the EMC regulation. For power-rail ESD clamp circuits, the impact of the transient noise coupled from microelectronic system on the power (or ground) line has attracted more attentions. The transient noise could induce some power-rail ESD clamp circuits into serious latch-on failure according to the previous studies [20], [21]. In this work, the electrical fast transient (EFT) test [52] has been applied on the eight different power-rail ESD clamp circuits to judge their immunities against fast transient noise on their power lines. The EFT voltage waveforms consist of many bursts with 15-ms duration and these bursts are repeated every 300 ms, as shown in Fig. 2.8(a). Besides, each voltage pulse in the burst has a rise time of 5 ns and a pulse width of 50 ns, as illustrated in Fig. 2.8(b). Moreover, because the minimum EFT voltage waveforms of 200 V provided by EFT generator would easily destroy the on-chip devices in nanoscale CMOS technology, the EFT voltage waveforms were decayed by a 100-time attenuator before they were directly applied to the VDD terminals of the power-rail ESD clamp circuits. The measurement setup for the EFT test was demonstrated in Fig. 2.9. Fig. 2.10(a) shows the measured results of BFET1 and BFET2 under the 4-V EFT test on the VDD terminals, both of which have the BFET (D= 0.25 μm without SB) layout styles for the main ESD clamp NMOS transistors. The overshooting voltages on the VDD nodes can be effectively clamped by these two power-rail ESD clamp circuits. BFET1 exhibits a smooth waveform, only decaying the voltage amplitude on the VDD terminal, whereas BFET2 presents a rough waveform during the period of the EFT execution. Besides, the measured results of Tradition1 and Tradition2

have been illustrated in Fig. 2.10(b). The overshooting voltage on the VDD nodes also can be clamped by the designs with the traditional ESD clamp NMOS transistor (D= 2.0 μm with SB). Nevertheless, Tradition1 shows a smoother waveform during the period of the EFT execution. Based on the measured results in Figs. 2.10(a) and 2.10(b), the power-rail ESD clamp circuits with 1-stage inverter in controlling circuit possess better capability for clamping transient noise on VDD terminals.

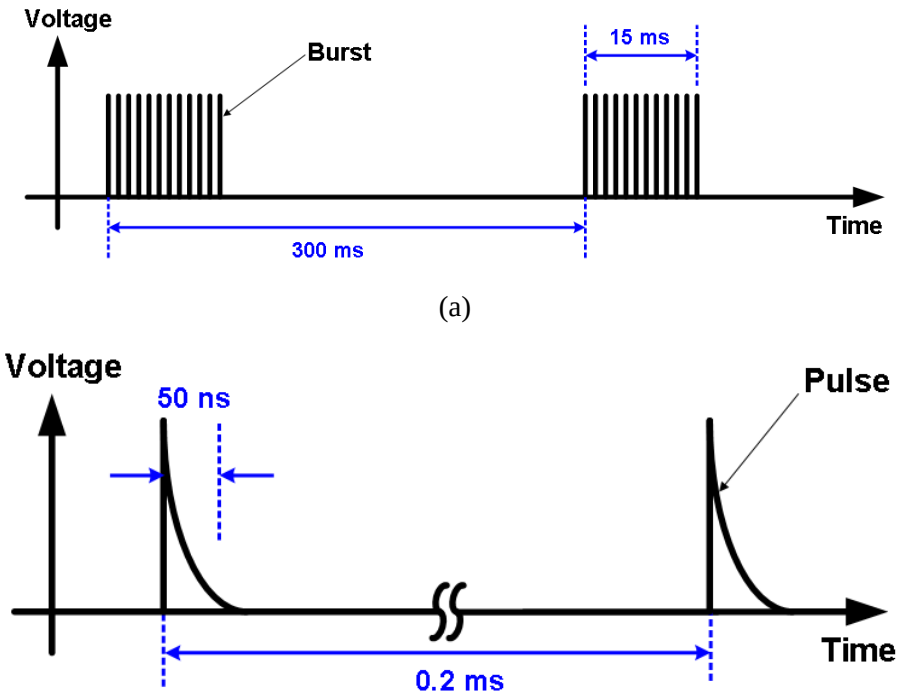


Fig. 2.8. Specified electrical fast transient (EFT) waveforms of (a) burst, and (b) single pulse, with a repetition frequency of 5 kHz.

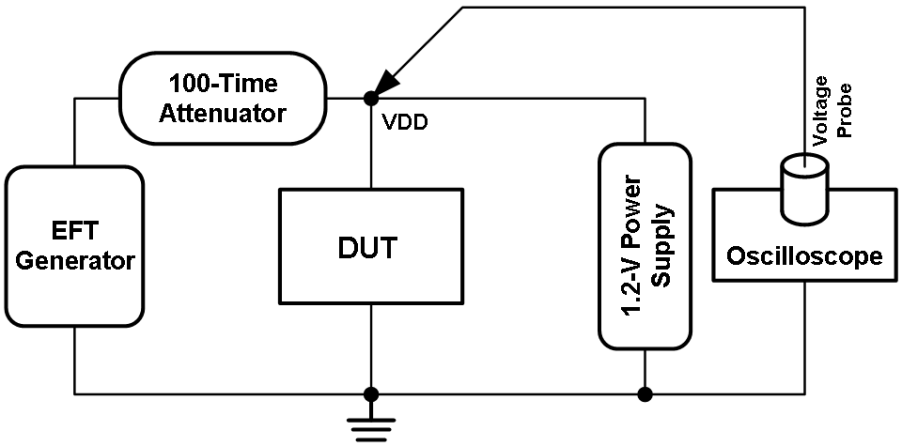
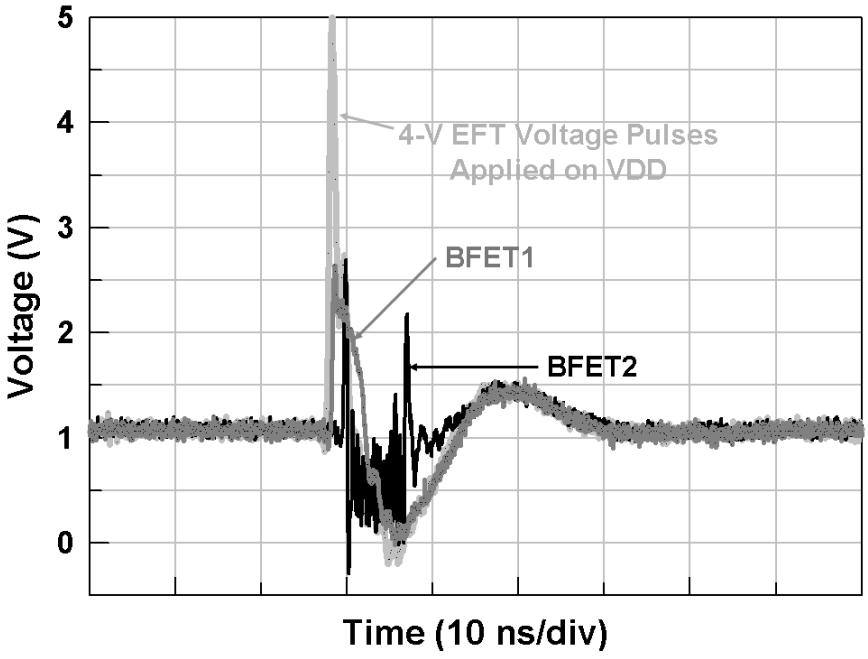
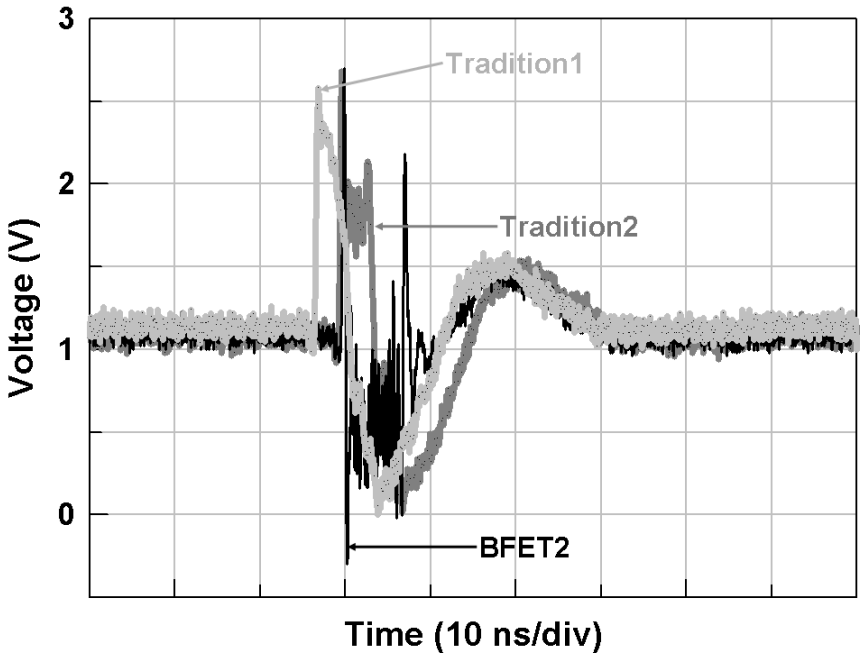


Fig. 2.9. Measurement setup for electrical fast transient (EFT) test on the DUT with the VDD bias of 1.2 V.



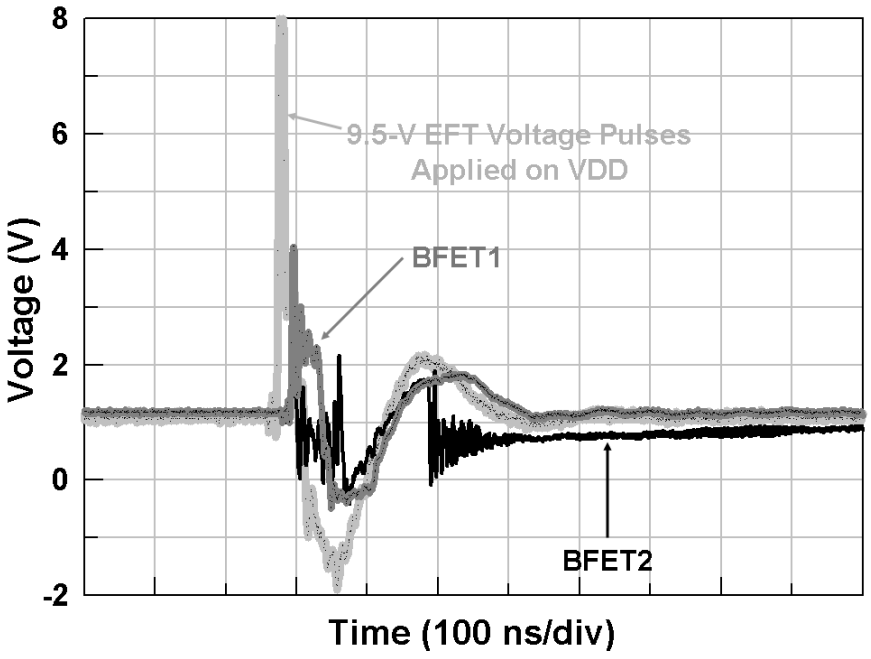
(a)



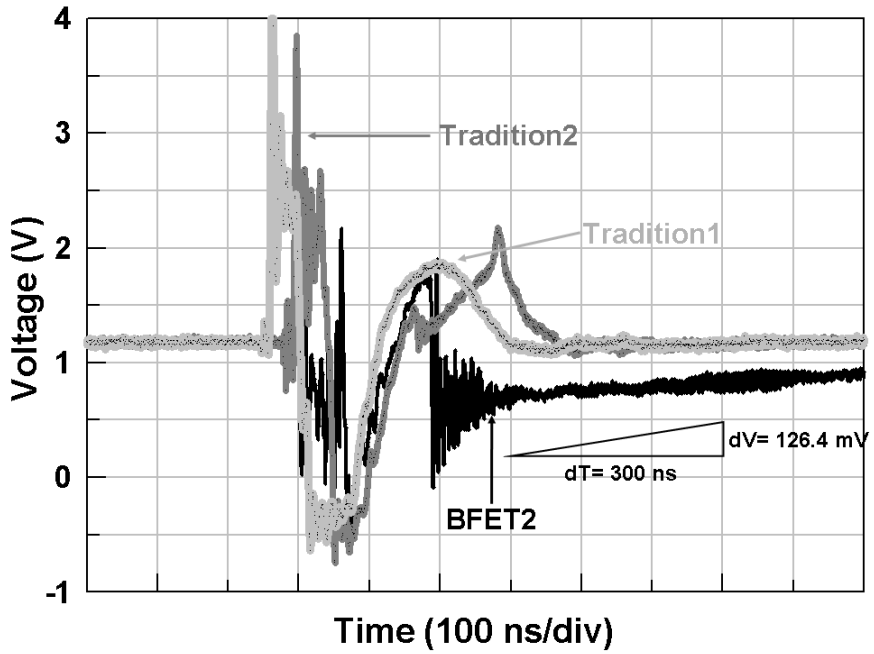
(b)

Fig. 2.10. Under the 4-V EFT voltage pulse, the measured voltage waveforms of (a) BFET1 and BFET2, and (b) Tradition1 and Tradition2.

With the 9.5-V EFT voltage stress on the VDD terminals, the measured results are presented in Figs. 2.11(a) and 2.11(b). All of the designs can efficiently clamp the overshooting voltage pulses on the VDD nodes during the EFT stresses. However, after the duration of the EFT voltage pulse, the voltage potential on VDD terminal is not successfully recovered to the normal operation voltage of 1.2 V in BFET2, as shown in Fig. 2.11(b).



(a)



(b)

Fig. 2.11. Under the 9.5-V EFT voltage pulse, the measured voltage waveforms of (a) BFET1 and BFET2, and (b) Tradition1 and Tradition2.

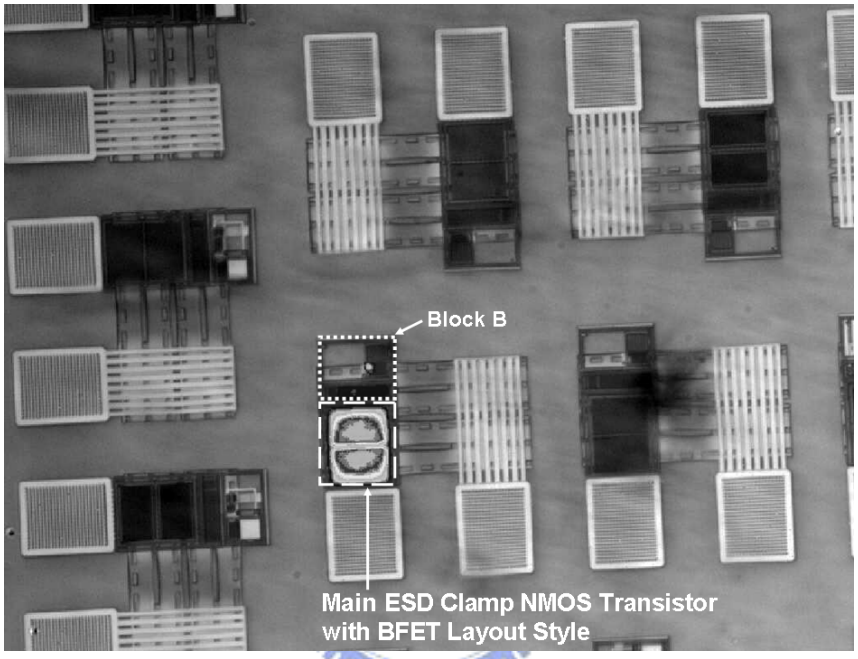
Although the voltage potential on VDD node would be slowly elevated toward 1.2 V, the huge conducting current from VDD to VSS does not vanish under the VDD node recovery to 1.2 V. The main ESD clamp NMOS transistor is still kept at on state after 9.5-V EFT stress, which is the occurrence of latch-on event. In contrast, the voltage waveforms of other designs can be quickly recovered to 1.2 V after the duration of the EFT voltage pulse and no

conducting current from VDD to VSS is observed after 9.5-V EFT stress. Moreover, according to the measured results in Fig. 2.11(b), the recovery period of Tradition2 is larger than that of Tradition1. Tradition2 would induce an irregular overshooting voltage pulse at the end of the duration of the EFT voltage pulse. In a nutshell, the RC-based ESD-transient detection circuit with the controlling circuit of 3-stage inverters and the main ESD clamp NMOS transistor with BFET (D= 0.25 μm without SB) layout style are very dangerous to be used as the power-rail ESD clamp circuit due to the mis-trigger and latch-on concern.

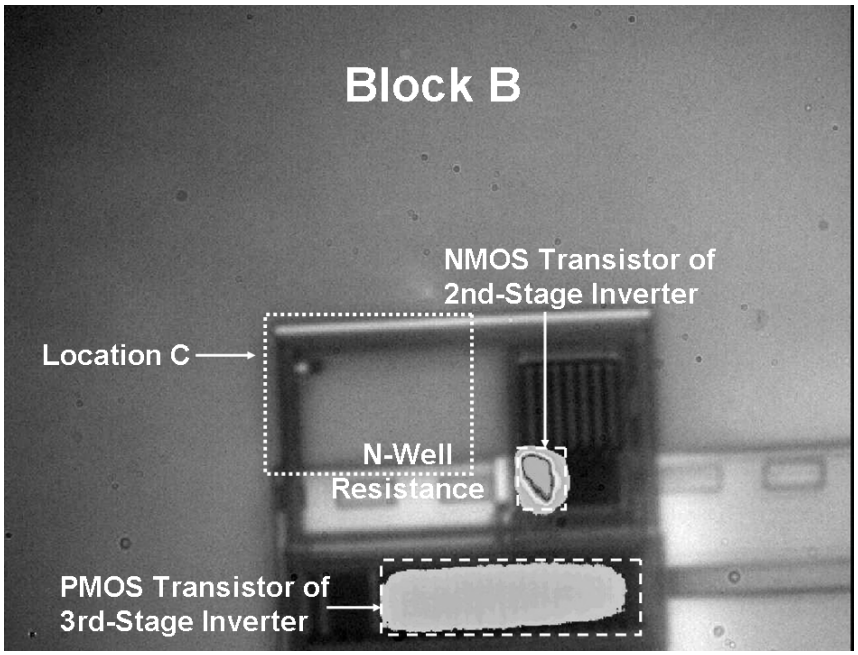
2.3.2. Latch-On Mechanism

According to the measured results of the EFT test and fast power-on condition, BFET2 would induce the latch-on phenomenon if the fast transient noises applied on the VDD terminal. The potential on the VDD node will be clamped into a lower voltage level or the huge conducting current from VDD to VSS will be observed, as shown in Figs. 2.6, 2.11(a), and 2.11(b). However, such power-rail ESD clamp circuit with RC-based ESD-transient detection circuit should maintain in a high impedance state from VDD to VSS after the turn-on duration of main ESD clamp NMOS transistor. Tradition2 clearly presents this characteristic, as shown in Fig. 2.6. But, the voltage waveforms of BFET2 are always clamped to a lower voltage potential under the fast power-on condition. There is an abnormal mechanism to contribute a positive feedback path that in turn triggers the occurrence of the latch-on event. In order to observe the root cause of this latch-on mechanism, the failure analysis has been executed by the emission microscope with InGaAs focal plane arrays (FPA) detector [53], which has an excellent capability to capture the photon emission of wavelength range from 800 nm to 1700 nm. This failure analysis equipment is suitable for the abnormal location with very slight photon emissions [53]-[55] because of the higher quantum efficiency. Figs. 2.12(a), 2.12(b), and 2.12(c) illustrated the results of the failure analysis after the EFT test. According to the images in Figs. 2.12(a) and 2.12(b), the main ESD clamp NMOS transistor with BFET layout style is turned on into the latch-on status after the 9.5-V EFT voltage stress because the PMOS transistor in the third-stage inverter and the NMOS transistor in the second-stage inverter are also in the on state. The PMOS transistor in the third-stage inverter and the NMOS transistor in the second-stage inverter kept in the on state could be attributed to voltage drop across the n-well resistance of the RC-based ESD-transient detection circuit. Generally, the n-well resistance is usually regarded as a common choice in such RC-based ESD-transient detection circuit to obtain an adequate

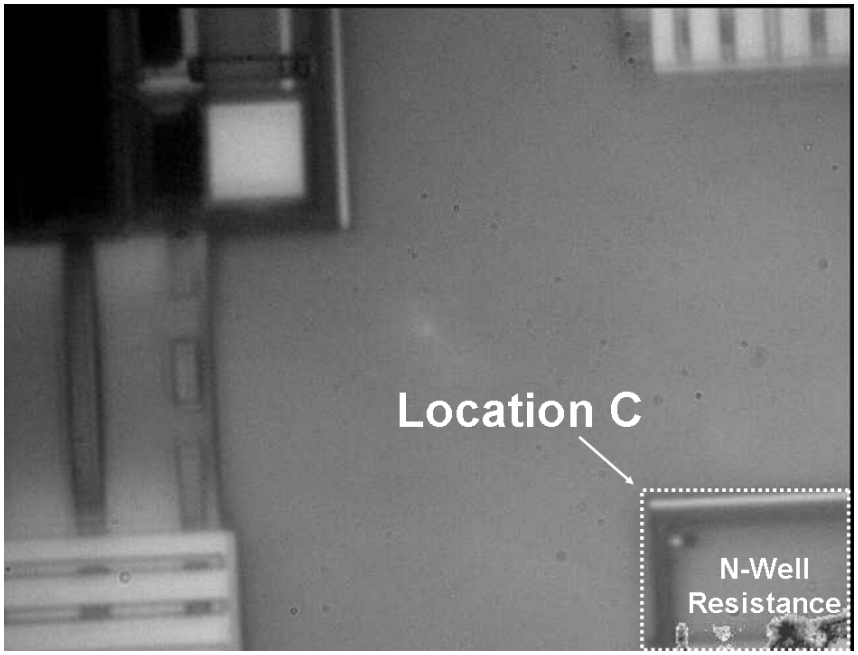
resistance and a sufficient RC-time delay. However, based on the previous studies [56], [57], a few electrons would be captured by this n-well resistance since this n-well resistance could be performed as the guard ring of the minority to capture the minority carriers (electrons) in the p-substrate. The slight hot spots on the n-well resistance have been observed in Fig. 2.12(c). It induces some voltage drop across the n-well resistance because the electrons were captured and conducted by this n-well resistance.



(a)



(b)



(c)

Fig. 2.12. Through the emission microscope with InGaAs FPA detector, (a) the abnormal emission spots after the EFT test are located at the NMOS transistor of the second-stage inverter, the PMOS transistor of the third-stage inverter, and main ESD clamp NMOS transistor. (b) The zoomed-in view around the controlling circuit and the RC-based ESD-transient detection circuit. (c) The emission image is only located at the n-well resistance of the RC-based ESD-transient detection circuit.

Due to the slight voltage drop across the n-well resistance, the PMOS transistor in first-stage inverter can be slightly turned on. Then, through the amplification of the first-stage inverter, the NMOS transistor in the second-stage inverter and the PMOS transistor in the third-stage inverter are thoroughly in the on state, as shown in Fig. 2.12(b) with bright hot spots. In the layout, although the n-well resistance has been surrounded by the N+/n-well minority guard rings connected to VDD, some escaped electrons still were captured by the n-well resistance. Therefore, the voltage drop across the n-well resistance is slight, which can not induce the latch-on phenomenon in BFET1. On the other hand, because the design with the traditional ESD clamp NMOS transistor (D= 2.0 μm with SB) has a smaller channel width to generate less channel conduction current and substrate injection current, the latch-on phenomenon would not occur in such designs. The latch-on event can be also observed in Modification3. But, the latch-on event was not observed in Modification1, Modification2, and Modifictaion4. Consequently in layout, the width of N+/n-well minority guard rings connected to VDD and the distance between the n-well resistance and the main ESD clamp NMOS transistor should be enlarged to prevent the threat of latch-on event under the EFT test

and fast power-on condition. However, such adjustments would extend some layout areas of the power-rail ESD clamp circuit in the standard I/O cell library.

2.4. Summary

The designs with controlling circuits of 3-stage inverters and 1-stage inverter have been studied to verify the optimal circuit schemes in NMOS-based power-rail ESD clamp circuits. In addition, the circuit performance among the four different main ESD clamp NMOS transistors drawn with different drain-contact-to-poly-gate spacings and co-designed with different inverter stages in the controlling circuits are compared. According to the experiments and analyses, the 3-stage inverters for controlling circuit and BFET layout style for the main ESD clamp NMOS transistor can slightly increase the ESD robustness, but they will dramatically degrade the immunity against mis-trigger and latch-on issues under the EFT test and fast power-on condition. The 1-stage inverter should be an appropriate and reliable candidate for the controlling circuit in the power-rail ESD clamp circuits. Finally, the latch-on phenomenon has been successfully observed by the emission microscope with InGaAs FPA detector. The root cause to induce such failure can be attributed to the abnormal mechanism of the voltage drop across the n-well resistance after the EFT test.

Chapter 3

Area-Efficient ESD-Transient Detection Circuit with Ultra Small Capacitance for On-Chip Power-Rail ESD Protection in CMOS ICs

In this chapter, an efficient ESD-transient detection circuit has been proposed and verified in 130-nm 1.2-V CMOS technology. This design abandons the feedback circuit techniques and adopts capacitance coupling mechanism to accomplish the desirable function on commanding the main ESD clamp NMOS transistor. Through experimental measurements, such as turn-on verification, transmission line pulse (TLP) stress [50], ESD stress, and fast power-on test, this power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit presents an excellent performance to meet the specified requirements. According to the measured results, the new proposed ESD-transient detection circuit possesses the sufficient turn-on duration under the ESD-stress conditions and high mis-trigger and latch-on immunities under the fast power-on conditions.

3.1. Background

In order to efficiently protect the core circuits realized with much thinner gate oxide in nanoscale CMOS technology, some previous studies had reported the efficient NMOS-based power-rail ESD clamp circuits without snapback operation [8]-[11], [17]-[19], [58], [59]. All of them adopted the gate-driven mechanism, which was basically implemented by an ESD-transient detection circuit and a controlling circuit, to respectively command the main ESD clamp NMOS transistor into the on state or the off state under the ESD-stress conditions and normal circuit operation conditions, as illustrated in Fig. 3.1. Two major different circuit schemes, which are RC-time delay technique [6]-[11] and capacitance coupling mechanism [18], [19], were usually used as the ESD-transient detection circuit in the power-rail ESD clamp circuit. Then, the controlling circuit was always implemented by single- or multi-stage inverters. In such power-rail ESD clamp circuit, main ESD clamp NMOS transistor can

thoroughly discharge huge ESD current by its channel current to exhibit excellent turn-on efficiency, such as lower trigger voltage (Vt1) and lower clamped voltage (Vclamp).

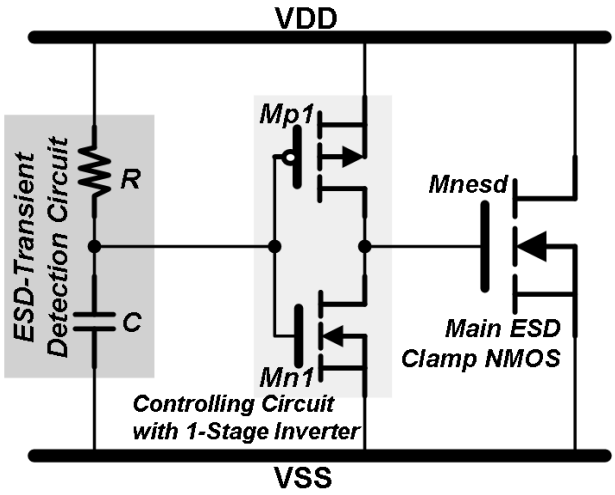


Fig. 3.1. Typical design scheme for NMOS-based power-rail ESD clamp circuit with an ESD-transient detection stage and controlling stage.

The main ESD clamp NMOS transistor without snapback operation has to be kept at the on state under the whole duration of ESD events in order to ensure that the ESD current can be discharged by its channel current. Based on the traditional RC-based ESD-transient detection circuit [6], [7], the RC-time constant which is the product of the resistance (R) and capacitance (C) essentially dominated the turn-on duration of the main ESD clamp NMOS transistor. Therefore, the RC-time constant of the RC-based ESD-transient detection circuit should be designed to sufficiently achieve a desirable turned-on duration of the main ESD clamp NMOS transistor. In general, the turn-on duration was adjusted to meet the period of human-body-model (HBM) ESD event, which is about several hundred nano-seconds (ns) [1]. The extended RC-time constant not only accompanies with the larger layout sizes of the resistance and capacitance, but also is subject to mis-trigger the main ESD clamp NMOS transistor under fast power-on applications [10]. Several previous works proposed special circuit schemes with feedback circuit techniques to extend the turn-on duration under a small RC-time constant [9], [10], [17]-[19]. However, those feedback circuit designs always suffered from the latch-on threats under the fast power-on events or the electrical fast transient noise [20], [21]. Besides, other circuit schemes without feedback circuit techniques, such as on-time control circuit [9] and multi-RC-triggered [11], also had been presented to achieve the desirable turn-on duration and to avoid the latch-on threat. However, extra resistors and capacitors have to be implanted into these designs, which occupying a quite

silicon area. In this chapter, an efficient ESD-transient detection circuit adopted capacitance coupling mechanism is proposed to accomplish the desirable function with ultra-small capacitance for using in power-rail ESD clamp circuit.

3.2. Realization of Power-Rail ESD Clamp Circuit

3.2.1. New Proposed ESD-transient Detection Circuit

Area-efficient ESD-transient detection circuit with ultra small capacitor has been presented in Fig. 3.2, which adopts capacitance coupling mechanism to achieve the required functions on the power-rail ESD clamp circuit. This area-efficient ESD-transient detection circuit consists of an ultra small capacitor (C1), cascode NMOS transistors (Mnc1 and Mnc2), a resistor (R1), and a switch NMOS transistor (Mns), commanding the main ESD clamp NMOS transistor through a controlling circuit with single-stage inverter. The ultra small capacitor is implemented by metal-oxide-metal (MOM) parasitic capacitance. The cascode NMOS transistors are used as a large resistor and cooperated with the ultra small capacitor to construct a capacitance coupling network [60], [61]. The node A between the ultra small capacitor and the cascode NMOS transistors is connected to gate terminal of the switch NMOS transistor. Then, its drain terminal is tied to the VDD through the resistor and also connected to the input of the controlling circuit.

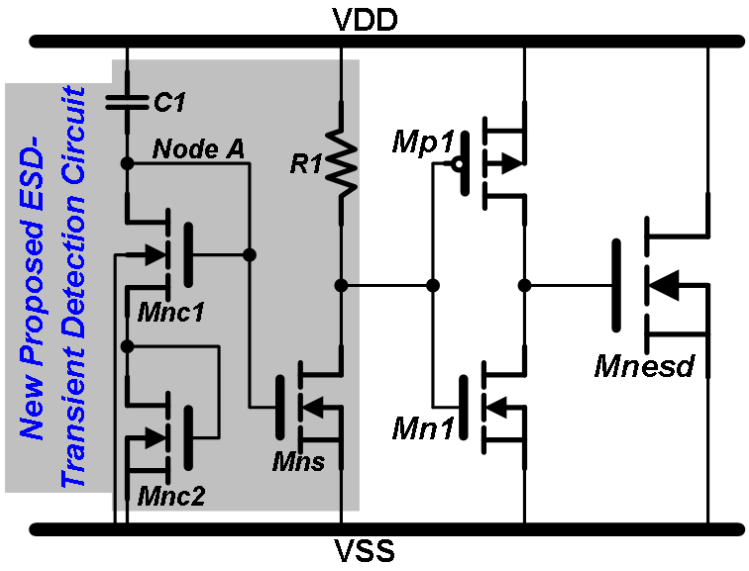


Fig. 3.2. Novel power-rail ESD clamp circuit with an new proposed ESD-transient detection circuit. This new proposed ESD-transient detection circuit is composed of an ultra small capacitor (C1), cascode NMOS transistors (Mnc1 and Mnc2), a resistor (R1), and a switch NMOS transistor (Mns).

Through the controlling circuit, the switch NMOS transistor can rule the main ESD clamp NMOS transistor to keep at “on” or “off” state. Finally, the main ESD clamp NMOS transistor has been drawn with the BigFET layout style, which has the minimum drain-contact-to-poly -gate spacing of 0.25 μm and without silicide blocking on its diffusion. This testchip is fabricated in a 130-nm 1.2-V CMOS process. Compared with the layout area of the power-rail ESD clamp circuit with traditional RC-based ESD-transient detection circuit, this work with the new proposed ESD-transient detection circuit is far smaller in the power-rail ESD clamp circuit, as shown in Figs. 3.3(a) and 3.3(b). The cell height of the novel power-rail ESD clamp circuit is reduced about 15 % and the layout area of the ESD-transient detection circuit is more reduced about 50 %.

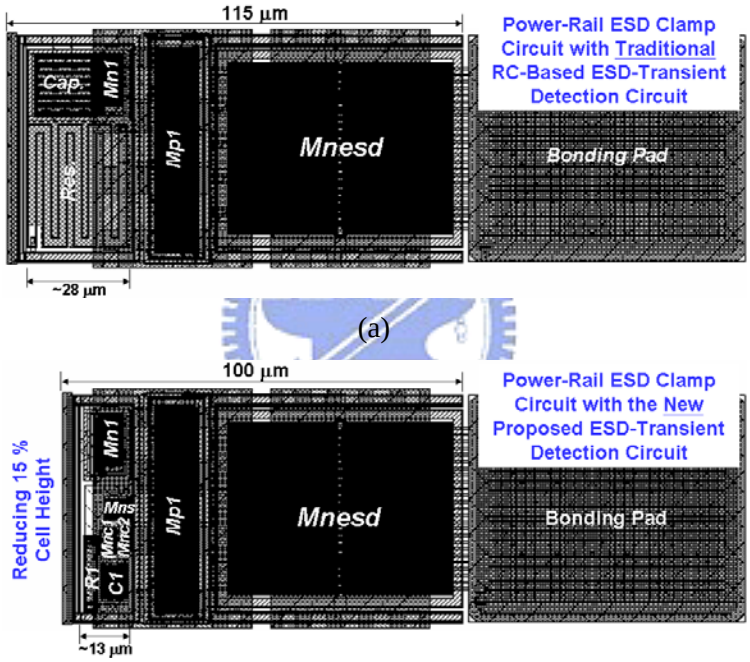


Fig. 3.3. The comparison of the layout areas between the power-rail ESD clamp circuits with (a) the traditional, and (b) the new proposed, ESD-transient detection circuits.

3.2.2. Operation Principles

During the positive VDD-to-VSS ESD stress condition, the potential of the node A will be synchronously evaluated toward a positive voltage potential by the capacitance coupling of the ultra small capacitor to trigger on the switch NMOS transistor. Then, through the switch NMOS transistor and the controlling circuit, the gate terminal of the main ESD clamp NMOS transistor will be promptly charged toward the positive voltage potential. The main ESD clamp NMOS transistor is turned on to clamp and discharge the huge ESD voltage and

ESD current. The turn-on duration of the main ESD clamp NMOS transistor is dominated by the potential of node A. This potential is synchronously kept at the positive voltage potential by the capacitance coupling; however, it will be slowly pulled down due to the turned-on cascode NMOS transistors. Because the gate terminals of these two cascode NMOS transistors with small device dimensions have been connected to their drain terminals, they are operated at saturation region to provide a huge resistance under the positive VDD-to-VSS ESD event. Finally, when the potential of node A is lower than the threshold voltage of NMOS transistor, the switch NMOS transistor will be turned off to force the main ESD clamp NMOS transistor off. Based on the simulation result, the turn-on duration of the main ESD clamp NMOS transistor can achieve over 600 ns in the power-rail ESD clamp circuit with the ultra small capacitor of only ~10 femto-Farad (fF), as presented in Fig. 3.4.

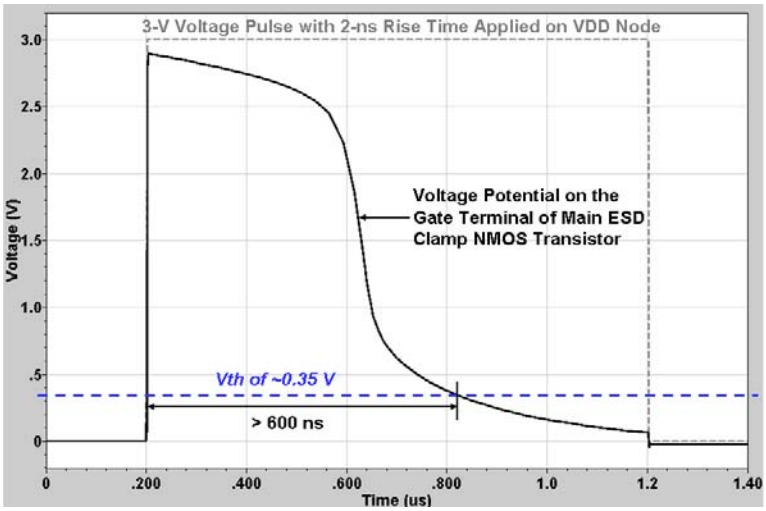


Fig. 3.4. The simulation result of the voltage potential on the gate terminal of main ESD clamp NMOS transistor in power-rail ESD clamp circuit.

The 3-V voltage pulse with rise time of 2 ns was applied on VDD node with VSS node grounded. The voltage potential on the gate terminal of main ESD clamp NMOS transistor is higher than the threshold voltage of ~0.35 V during the period of ~620 ns. The detailed design parameters, such as device sizes of cascode NMOS transistors and switch NMOS transistor, have been listed in Table 3.1. On the other hand, the parasitic drain-bulk diode of the main ESD clamp NMOS transistor can provide low impedance path under negative VDD-to-VSS ESD stress. Under the normal power-on condition, the normal VDD power-on voltage waveform has a rise time in the order of milli-second (ms). Such power-on voltage waveform will not produce enough coupling potential on the node A to trigger on the switch NMOS transistor. The potential of node A will be actually kept at ground through the high

resistance path of the cascode NMOS transistors. Therefore, the main ESD clamp NMOS transistor will be kept at “off” state under the normal circuit operation condition. Besides, the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit also presents a high immunity against mis-trigger and latch-on event.

Table 3.1

Design Parameters in the Power-Rail ESD Clamp Circuit with the New Proposed ESD-Transient Detection Circuit

Design Parameters	
Ultra Small Capacitor	10 fF
Device Size of Cascode NMOS	4 μm/2 μm (W/L)
Resistor	1.5 kΩ
Device Size of Switch NMOS	60 μm
Device Size of Main ESD Clamp NMOS	2600 μm

3.3. Experimental Results

3.3.1. Turn-On Verification under ESD-Like Stress Condition

In order to observe the turn-on efficiency of the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit, 2.4-V and 5-V ESD-like voltage pulses with 2-nano-seconds (ns) rise time are applied on the VDD terminal with VSS terminal grounded. The voltage pulses with a rise time of 2 ns and duration of 1 μs generated from a pulse generator are used to simulate the fast rising edge of HBM ESD event [12]. The sharp-rising edge of the ESD-like voltage pulse will be detected by the ESD-transient detection circuit and then to turn on the switch NMOS transistor. The main ESD clamp NMOS transistor is therefore triggered on by the controlling circuit. When the main ESD clamp NMOS transistor is turned on, the voltage waveform on VDD terminal will be clamped as the measured results shown in Fig. 3.5. According to the measured results in Fig. 3.5, the new proposed design exhibits an excellent turn-on efficiency to clamp the overshooting voltage to a much lower voltage level. The voltage waveform of the new proposed design can be constantly clamped by the turned-on main ESD clamp NMOS transistor during the whole 1-μs pulse width. On the contrary, the voltage waveform of the traditional design will quickly raise and its clamped voltage is much higher than that of the new proposed design after the duration of 200 ns. The

new proposed ESD-transient detection circuit can efficiently extend the turn-on duration of the main ESD clamp NMOS transistor in the power-rail ESD clamp circuit. The longer turn-on duration of the main ESD clamp NMOS transistor would assure that the low impedance path was entirely provided from VDD to VSS under the whole HBM ESD event, and would also enhance the ESD robustness of the power-rail ESD clamp circuit.

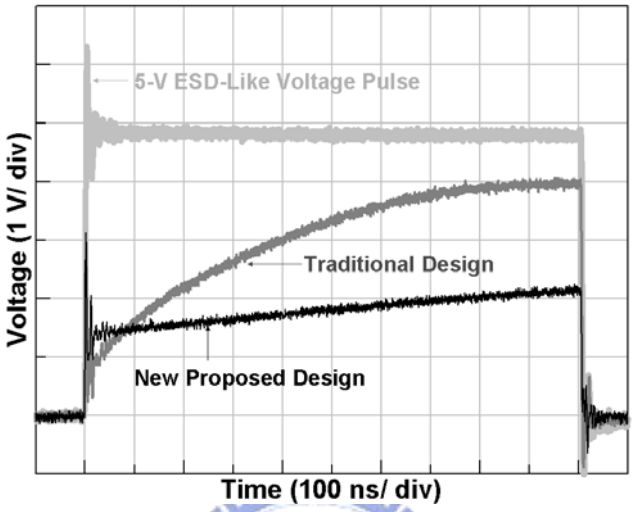


Fig. 3.5. The measured voltage waveforms of power-rail ESD clamp circuits with the traditional and new proposed ESD-transient detection circuits under 5-V ESD-like voltage pulses with 2-ns rise time.

3.3.2. TLP I-V Characteristics and ESD Robustness

The Transmission Line Pulse (TLP) [17] measured I-V characteristics of the power-rail ESD clamp circuits with the traditional and new proposed ESD-transient detection circuits are shown in Fig. 3.6. This TLP system has a 100-ns pulse width and 2-ns rise time. These two power-rail ESD clamp circuits present the desired TLP I-V characteristics. No obvious difference among the TLP measured results was observed between these two designs. The second breakdown currents (It2) of these two power-rail ESD clamp circuits can achieve over 7 A. Their clamped voltages (Vclamp) and on resistances (Ron) are similar. Table 3.2 shows the HBM and MM ESD robustness of these two power-rail ESD clamp circuits. The HBM and MM ESD robustness of the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit are 8.0 kV and 400 V, respectively, which are obviously higher than those of the power-rail ESD clamp circuit with the traditional ESD-transient detection circuit. According to the failure analysis by SEM observation, the failure spot of the traditional design is located on the unexpected junction melting damages between the n+/n-well minority guard ring and the p+ majority guard ring after 6.0-kV HBM ESD stress, as shown in Figs. 3.7(a) and 3.7(b). Because the power-rail ESD clamp circuit with

traditional ESD-transient detection circuit has insufficient turn-on duration, the huge ESD current could not efficiently discharge during the whole HBM ESD event to induce the unexpected failure spot after 6.0-kV HBM ESD stress.

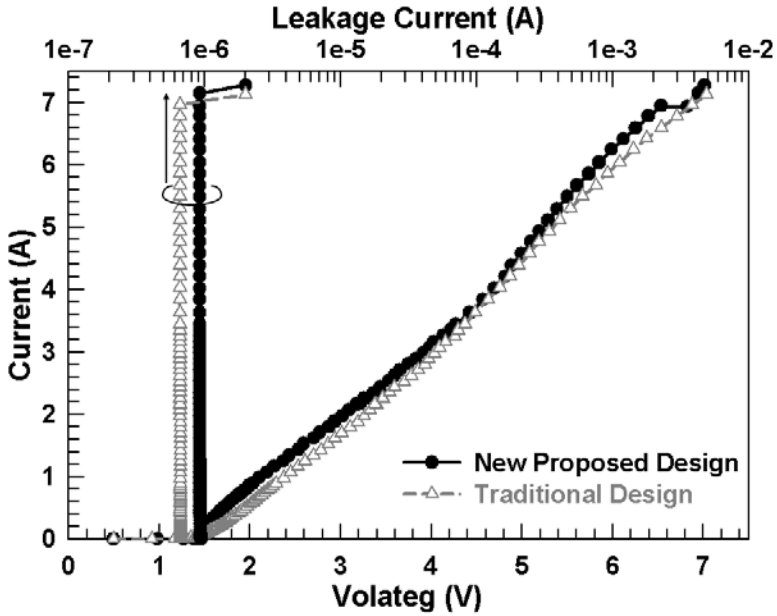
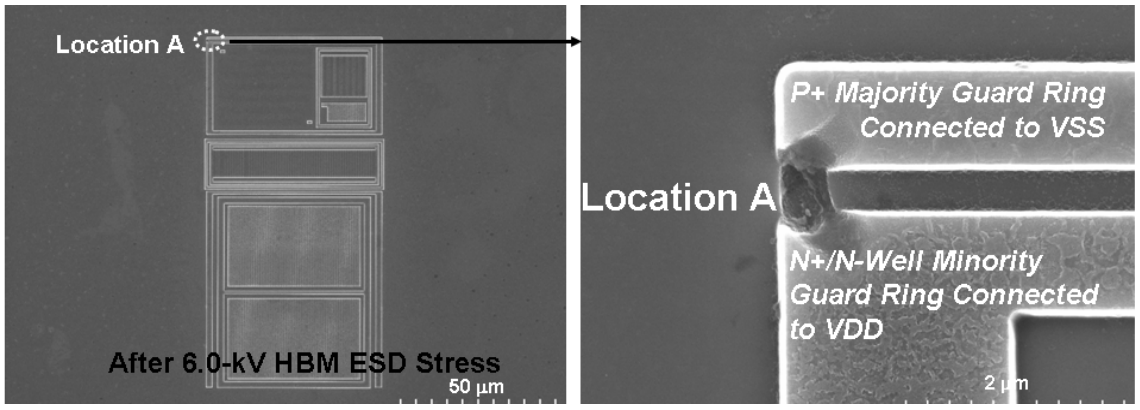


Fig. 3.6. The TLP I-V curves of the power-rail ESD clamp circuits with the traditional and the new proposed ESD-transient detection circuits.

Table 3.2

HBM and MM ESD Robustness of the Power-Rail ESD Clamp Circuits with the Traditional and the New Proposed ESD-Transient Detection Circuits

Design	HBM	MM
Traditional	5.5 kV	200 V
New Proposed	8.0 kV	400 V



(a) (b)

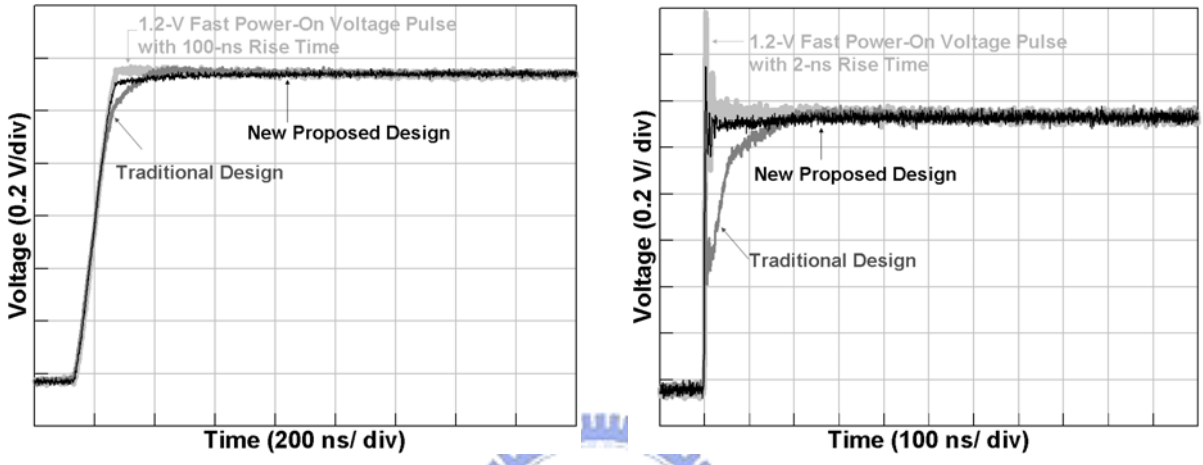
Fig. 3.7. (a) The failure spot of the power-rail ESD clamp circuit with the traditional ESD-transient detection circuit after 6.0-kV HBM ESD stresses. (b) Zoomed-in view of failure spot at Location A.

3.3.3. Fast Power-On Condition and Discussion

In general, the normal VDD power-on voltage waveform has a rise time in the order of milli-second (ms) and amplitude of VDD operation voltage. Due to such a slow rise time and small amplitude in normal power-on conditions, the coupling potential on the node A is too weak to turn on the switch NMOS transistor. Therefore, the main ESD clamp NMOS transistor will be well kept at off state. In this work, both power-rail ESD clamp circuits with the traditional and the new proposed ESD-transient detection circuits can successfully achieve this desirable task under normal power-on conditions. However, some previous studies [9]-[11], [20], [21] have illustrated that several power-rail ESD clamp circuits with RC-based ESD-transient detection circuits and feedback circuit schemes were easily mis-triggered and into the latch-on state under the fast power-on conditions with the rise time in the order of nano-second (ns). The design with the new proposed ESD-transient detection circuit has been applied with 1.2-V voltage pulses with 100-ns or 2-ns rise time, both of which are used to simulate the fast power-on condition, to investigate its immunities against the mis-trigger and latch-on event. The measured results are respectively shown in Figs. 3.8(a) and 3.8(b). Its measured voltage waveforms do not show any obvious degradation under the fast power-on condition with voltage pulse of 1.2 V and rise time of 100 ns or 2 ns. On the contrary, the power-rail ESD clamp circuit with the traditional ESD-transient detection circuit suffered from the mis-trigger under the fast power-on conditions. Its voltage waveforms will be slightly degraded under the 1.2-V fast power-on pulse with 100-ns rise time, and be dramatically degraded under that with 2-ns rise time. Since the feedback circuit schemes were not used in this work, the latch-on event was not observed in these two power-rail ESD clamp circuits. Compared with the results in the previous studies [9]-[11], [18], [19], the power-rail ESD clamp circuit with new proposed ESD-transient detection circuit possesses an excellent immunity against mis-trigger and latch-on event. Because the new proposed ESD-transient detection circuit adopts the capacitance coupling mechanism, this new proposed design not only distinguishes the abnormal overshooting voltage pulse by its rise time, but also discriminates this voltage pulse by its voltage amplitude. The new proposed ESD-transient detection circuit can easily distinguish the ESD event from the fast power-on condition with the voltage amplitude of 1.2 V and the rise time of 2 ns.

In addition, the electrical fast transient (EFT) test [52] is applied on the power-rail ESD clamp circuit with new proposed ESD-transient detection circuit to judge its immunity against fast transient noise on the power line. With 10-V EFT voltage stress on the VDD node,

the measured result is shown in Fig. 3.9. The new proposed design can efficiently clamp the overshooting voltage pulse on VDD node during EFT stress. After the duration of 10-V EFT voltage pulse, the voltage potential on VDD node is well remained at 1.2 V and no conducting current from VDD to VSS is observed. According to the EFT measured result, the new proposed ESD-transient detection circuit also possesses an excellent immunity against mis-trigger and latch-on event under electrical fast transient noise applied on VDD terminal.



(a) (b)

Fig. 3.8. The measured voltage waveforms of the power-rail ESD clamp circuits with the traditional and the new proposed ESD-transient detection circuits under the 1.2-V fast power-on conditions with (a) 100-ns rise time and (b) 2-ns rise time.

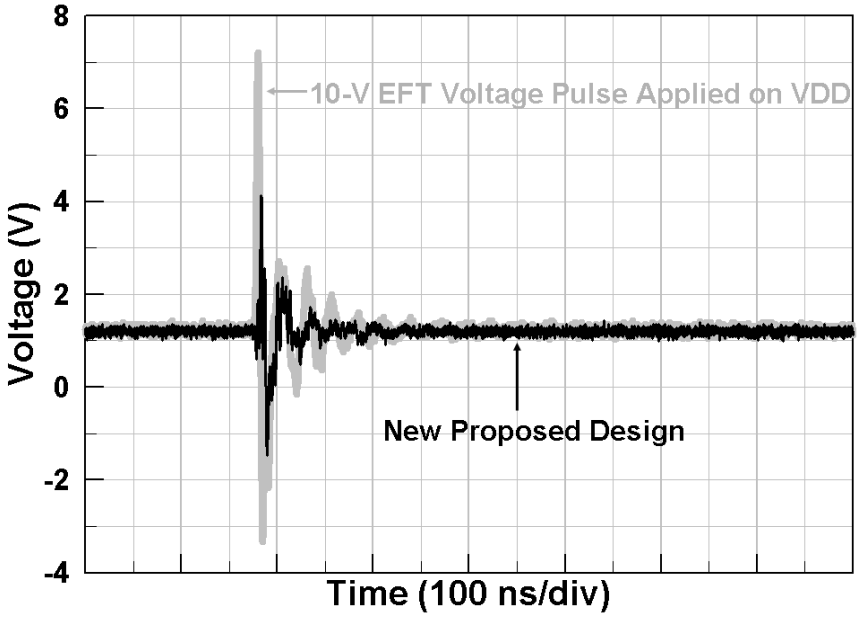


Fig. 3.9. Under the 10-V EFT voltage pulse, the measured voltage waveform of the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit.

3.4. Summary

A new proposed ESD-transient detection circuit cooperated with NMOS-based power-rail ESD clamp circuit has been presented and successfully verified in a 130-nm CMOS technology. The new proposed ESD-transient detection circuit adopts the capacitance coupling mechanism and a switch NMOS transistor to command the main ESD clamp NMOS transistor by the general controlling circuit with single-stage inverter. According to the measured results, the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit exhibits the superior ESD robustness of 8.0 kV and 400 V in HBM and MM ESD stresses, respectively. Moreover, it also possesses an excellent immunity against the mis-trigger and latch-on event under the 1.2-V fast power-on condition with the rise time of 2 ns.

Chapter 4

Implementation of *Initial-On* ESD Protection Concept with PMOS-Triggered SCR Devices in Deep-Submicron CMOS Technology

In this chapter, a novel initial-on SCR design is proposed to achieve the lowest trigger voltage and the highest turn-on efficiency of SCR device for effective on-chip ESD protection. Without using the special native device or any process modification, this initial-on SCR design is realized by circuit skill with the PMOS transistor in general CMOS processes [45]. This initial-on SCR design also presents a high enough holding voltage in a fully-silicided 0.25-μm CMOS process to avoid latchup issues in normal circuit operation conditions.

4.1. Background

In the past, the traditional ESD protection devices are initially kept off in CMOS ICs, as illustrated in Fig. 4.1. When the pad is zapped with ESD pulse, the ESD clamp device is triggered on by the ESD stress voltage to conduct ESD current from the pad to ground. However, when the core circuits are realized with a much thinner gate oxide in a deep-submicron CMOS technology, the traditional ESD protection design cannot be able to effectively protect the core circuits with thinner gate oxide. To effectively protect the core circuits with much thinner gate oxide in the deep-submicron CMOS technology, a new on-chip ESD protection concept with the initial-on ESD protection device is shown in Fig. 4.2. The ESD clamp device is kept off, when the IC is in the normal circuit operation conditions. But, the ESD clamp device is initially on, when the IC is floating without any power bias. When the pad is zapped by ESD, the ESD clamp device standing in the already-on status can quickly discharge ESD current from the pad to ground. Therefore, this new ESD protection concept can effectively protect the internal circuits in a deep-submicron CMOS technology [62]. The optimum ESD protection design window is restricted within the

range between VDD operation voltage and the gate oxide breakdown voltage. The ESD protection circuits should be triggered on to discharge the ESD currents, and to protect the internal circuits without gate oxide damage. Therefore, the trigger voltage of the ESD protection circuit must be lower than the breakdown voltage of the internal circuits. In addition, the holding voltage and on resistance (R_{on}) of ESD protection circuit will significantly influence the ESD robustness of CMOS IC product. The lower holding voltage and smaller on resistance (R_{on}) can provide more efficient ESD protection. However, the holding voltage of ESD protection devices must be higher than the VDD operation voltage to prevent the latchup under normal circuit operation condition [63]. In IC products, the on-chip ESD protection designs are required to provide higher ESD robustness with smaller layout area to save the chip area. Silicon controlled rectifiers (SCRs) have been used as on-chip ESD protection devices, because of their superior area-efficient ESD robustness [22]. However, SCR has some drawbacks, such as higher trigger voltage (Vt1), lower turn-on efficiency, and even latchup danger.

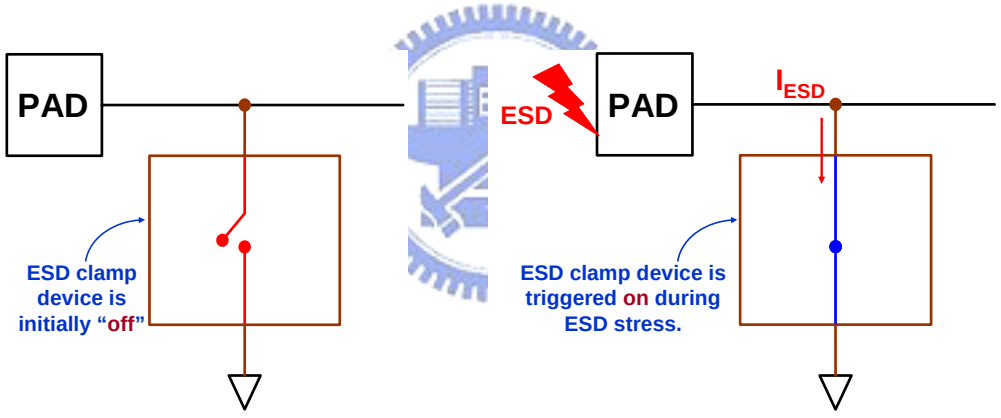


Fig. 4.1. The traditional ESD protection design with the initial-off ESD protection device. (a) The ESD clamp device was kept off in normal circuit operation conditions. (b) During ESD stress, the ESD clamp device was triggered on to discharge ESD current.

The related previous studies [22]-[31] on solving the disadvantages have been reported in Chapter 1. In this chapter, a novel initial-on SCR design implemented by PMOS-triggered SCR device is proposed to achieve the lowest trigger voltage and the highest turn-on efficiency of SCR device for effective on-chip ESD protection. Without using the special native device or any process modification, this initial-on SCR design is realized by circuit skill with the embedded PMOS transistor cooperated with RC-based ESD-transient detection circuit in general CMOS processes [45]. This initial-on SCR design has a high enough

holding voltage to avoid latchup issues in a VDD operation voltage of 2.5 V. The new proposed initial-on ESD protection design with PMOS-triggered SCR device has been successfully verified in a fully-silicided 0.25-μm CMOS process.

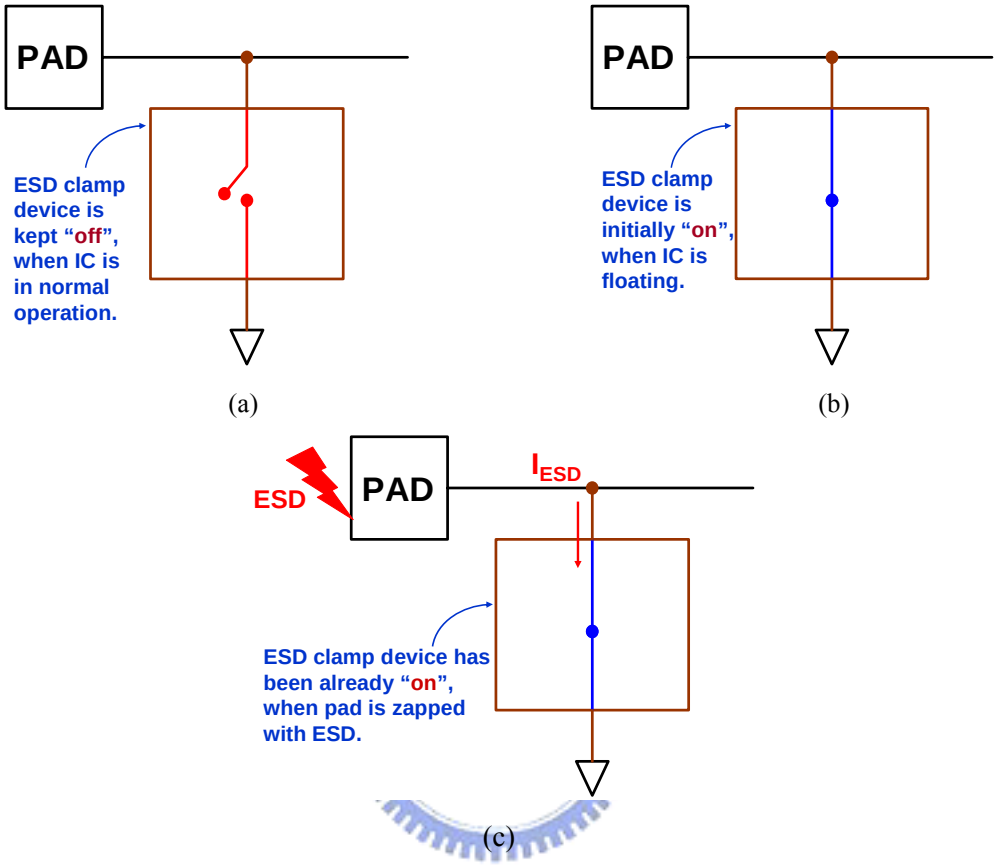


Fig. 4.2. The new ESD protection concept with the initial-on ESD protection device. (a) The ESD clamp device was kept off in normal circuit operation conditions. (b) The ESD clamp device was initially on when IC was floating. (c) The already-on ESD clamp device can rapidly discharge ESD current during ESD stress.

4.2. Realization of the Initial-On SCR Design

4.2.1. Implementation of the Initial-On ESD Protection Circuit

The new proposed initial-on ESD protection design, which consists of the SCR device with PMOS-triggered technique and the RC-based ESD transient detection circuit, is shown in Fig. 4.3. A PMOS transistor is directly embedded into the SCR structure to achieve the initial-on function for ESD protection. The source and drain terminals of the PMOS transistor are connected to the additional n+ diffusion and p+ diffusion of the SCR structure, respectively, as illustrated in Fig. 4.3. These additional p+ diffusion and n+ diffusion are the

p-triggered and n-triggered nodes in p-substrate and n-well of this SCR structure, respectively, to enhance the turn-on efficiency of SCR during ESD stress. The gate terminal of the embedded PMOS is controlled by a RC-based ESD transient detection circuit, which is used to distinguish the ESD-stress conditions from the normal circuit operation conditions.

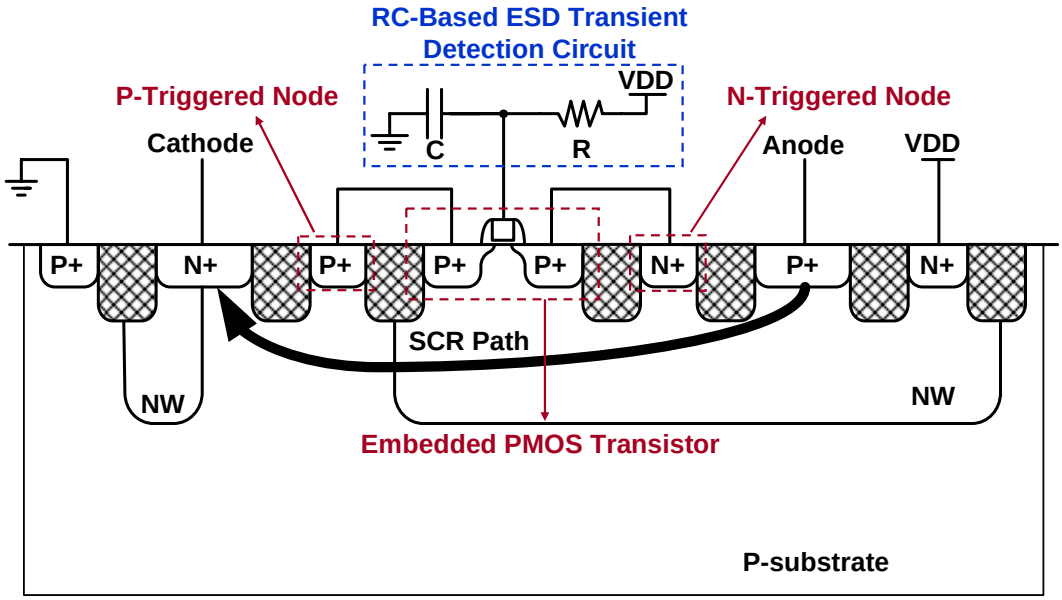
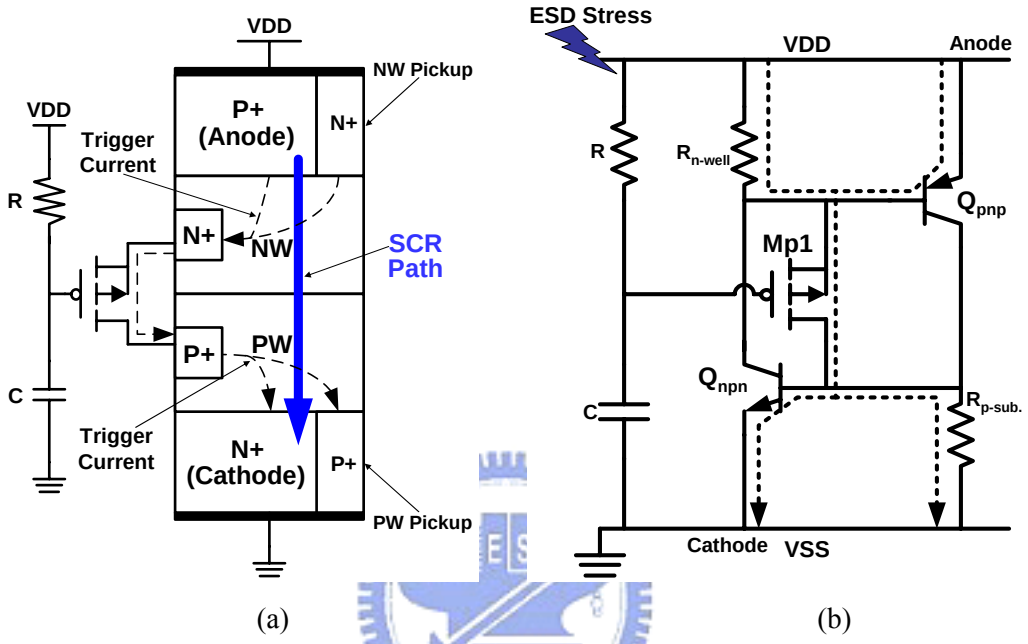


Fig. 4.3. The cross-sectional view of the initial-on SCR design with PMOS-triggered technique.

4.2.2. Operation Principles

Under positive VDD-to-VSS ESD-stress condition, the gate voltage of embedded PMOS is initially kept at zero in the power-rail ESD clamp circuit, as shown in Fig. 4.4(a). With an initial gate voltage of 0 V, the PMOS transistor is initially on to conduct the ESD current from the anode (P+) of SCR or pickup (N+) of n-well, and then inject into the p-well/p-substrate of SCR device, as the dashed lines illustrated in Fig. 4.4(a). With the both trigger currents in the n-well and p-well/p-substrate synchronously, the SCR can be fired on quickly. Finally, the ESD current is mainly discharged from the anode to the cathode of SCR device. The equivalent circuit of the initial-on SCR design is shown in Fig. 4.4(b). The initial-on PMOS transistor provides the conduction paths to generate the voltage bias between emitters and bases, which in turns induce base currents of the parasitic vertical pnp bipolar transistor (Qpnp) and lateral npn bipolar transistor (Qnpn) to trigger on the SCR device to discharge ESD current. Due to the difference in the rise time between the ESD pulse and the VDD power-on voltage, the RC time constant of the ESD-transient detection circuit is designed about 0.1~1 micro-second to distinguish the ESD-stress condition from the normal

circuit operation condition [6], [7]. To achieve the desired operation, the RC time constant of the ESD-transient detection circuit in Figs. 4.4(a) and 4.4(b) is designed around 1 μs in this work. During normal circuit operation condition with the normal VDD and VSS power supplies, the gate of embedded PMOS is biased at VDD to keep itself off. Therefore, the PMOS-triggered SCR device is always kept off during the normal circuit operation condition.

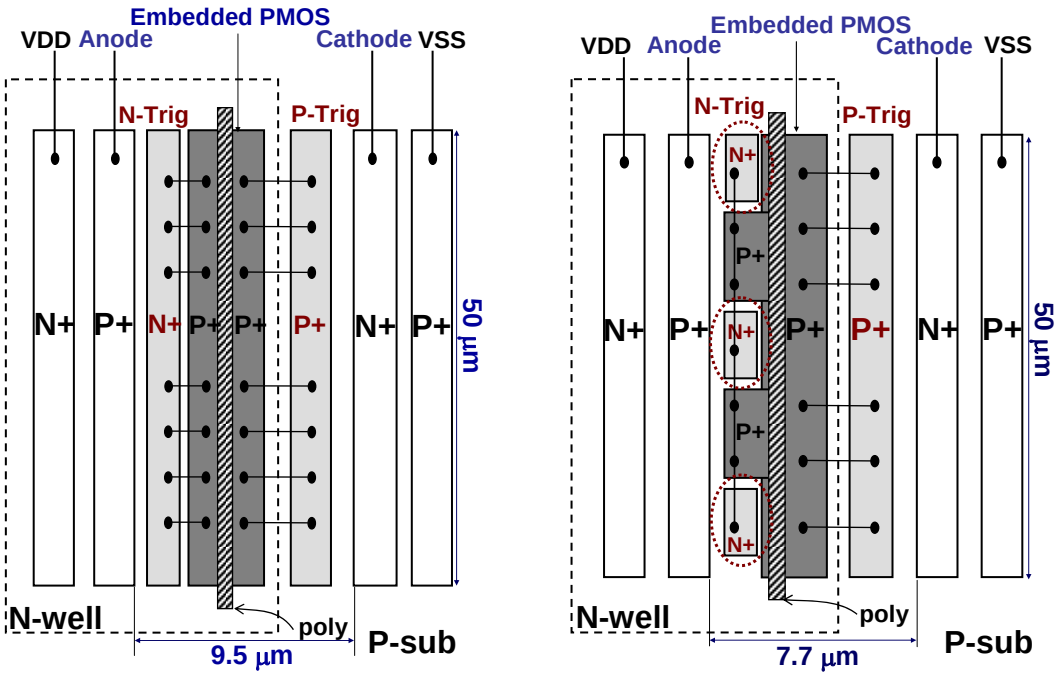


(a) (b)

Fig. 4.4. (a) The operation of the initial-on SCR design for power-rail ESD clamp circuit. (b) The equivalent circuit of the initial-on SCR design. The embedded PMOS transistor generates the trigger current to initiate the turn-on of SCR during ESD stress.

4.2.3. Layout Structure for Initial-On SCR Device

To investigate the turn-on phenomena and circuit characteristics, two types of layout implementations (structure-1 and structure-2) for the proposed initial-on SCR device are verified in this work, as shown in Figs. 4.5(a) and 4.5(b). The SCR structure is consisted of P+ diffusion of anode, the n-well, the p-substrate (p-well), and the N+ diffusion of cathode in each test structure. The embedded PMOS transistors of structure-1 and structure-2 are different in the layout of the n-triggered node and the anode-to-cathode spacing. Because the n-triggered node has been merged into the source terminal of PMOS transistor, the anode-to-cathode spacing of structure-2 is reduced to 7.7 μm, whereas the anode-to-cathode spacing of structure-1 is 9.5 μm in a 0.25-μm CMOS process. The device characteristics, such as holding voltage, on resistance (R_{on}), and ESD robustness, of the PMOS-triggered SCR device can be adjusted by its anode-to-cathode spacing.



(a) (b)

Fig. 4.5. The top views of initial-on SCR devices with (a) structure-1 and (b) structure-2 layout styles realized in a 0.25-μm CMOS process.

4.3. Experimental Results

The initial-on SCR devices, in Figs. 4.5(a) and 4.5(b), have been fabricated in a 0.25-μm salicided CMOS process without using the silicide-blocking mask. The active width of each SCR device is drawn with 50 μm in the test chip.

4.3.1. DC Characteristics for the Initial-On SCR Devices

According to the measured device DC characteristics, the breakdown voltages of the P+ drain diffusion/n-well junction in PMOS and N+ drain diffusion/p-well junction in NMOS are respectively 7 V and 6.5 V in the 0.25-μm CMOS process. The n-well/p-well junction breakdown voltage is higher than 15 V in the same CMOS process. If the ESD protection devices are triggered on by junction-breakdown mechanisms, such as gate-grounded NMOS (GGNMOS), gate-VDD PMOS (GDPMOS), and LVTSCR, the junction-breakdown mechanisms often have higher trigger voltages which could not efficiently protect the internal circuits with thinner gate oxide in the deep-submicron or nanoscale CMOS technologies. Therefore, the initial-on ESD protection concept realized with PMOS-triggered SCR device is proposed in this work to achieve the lower trigger voltage and the higher turn-on efficiency. In order to observe the influence of embedded PMOS gate bias on the trigger voltage of SCR

devices, the gate-biased voltages (V_G) of 0, 1, 2, and 3 V were applied to the gate terminal of the embedded PMOS transistor. The measurement setup is shown in Fig. 4.6(a). The measured DC I-V curves of the initial-on SCR devices with structure-1 and structure-2 layout styles under different gate-biased voltages are shown in Figs. 4.6(b) and 4.6(c), respectively.

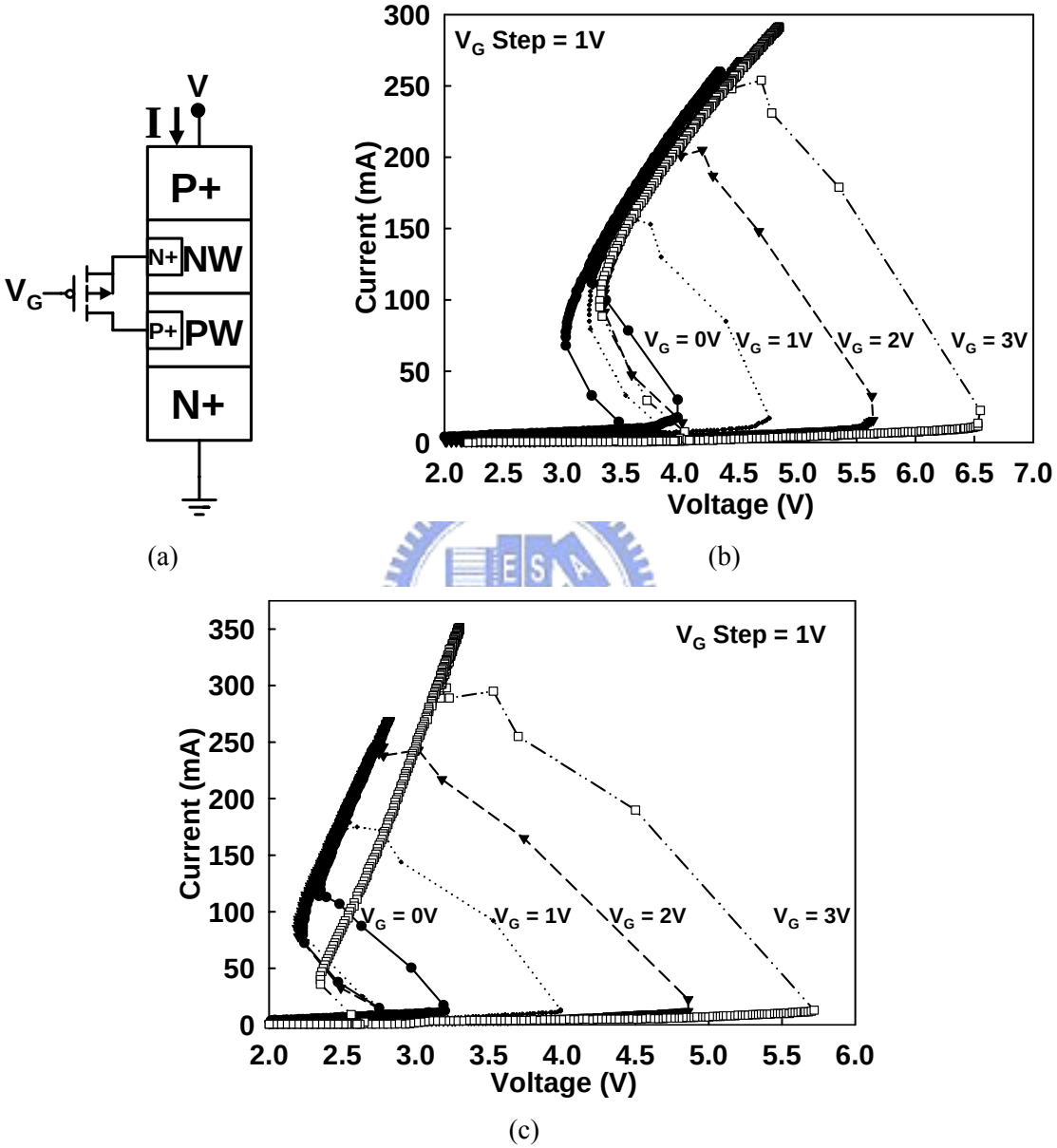
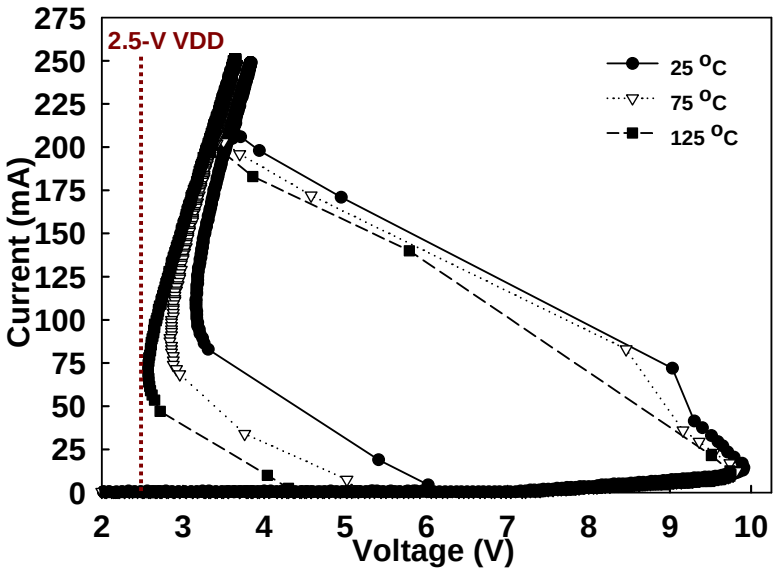


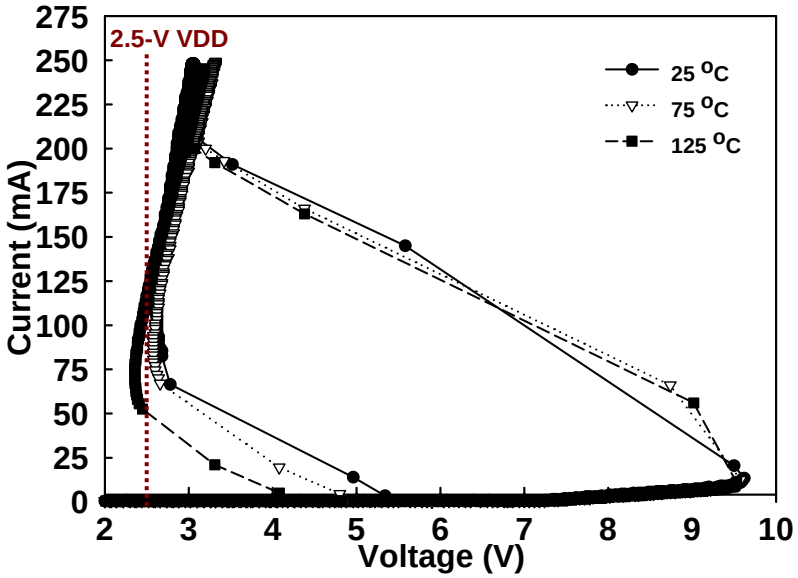
Fig. 4.6. (a) The different gate-biased voltages were applied to the gate terminal of the embedded PMOS transistor in the SCR structure. The measured DC I-V curves of the initial-on SCR devices with the layout styles of (b) structure-1, and (c) structure-2, under different gate-biased voltages.

The trigger voltage (Vt1) of PMOS-triggered SCR device is reduced with the decrease of the gate-biased voltage. When the gate voltage of the embedded PMOS is decreased from 3 V to 0 V, the Vt1 of PMOS-triggered SCR device is decreased from ~6.6 V to ~4 V and from

~5.75 V to ~3.3 V in structure-1 and stricture-2, respectively. These results have proven that the Vt1 of SCR device can be significantly reduced by the proposed PMOS-triggered technique. The holding voltage of the PMOS-triggered SCR device is slightly increased when the gate voltage of embedded PMOS is increased, as shown in Figs. 4.6(b) and 4.6(c). With an initial gate voltage of 0 V, the SCR device has the lowest holding voltage to effectively clamp the over-stress ESD pulse. In addition, another issue of using SCR device as the ESD protection device is the latchup concern under normal circuit operation condition. The gate terminal of the embedded PMOS transistor was biased at VDD through the resistor in the ESD-transient detection circuit during normal circuit operation conditions. To avoid latchup issue, the holding voltage of SCR devices must be designed greater than the maximum voltage of VDD. Under the temperatures of 25, 75, and 125 ^{o}C, the holding voltages of PMOS-triggered SCR devices in the layout styles of structure-1 and structure-2 with gate bias at VDD were shown in Figs. 4.7(a) and 4.7(b), respectively. The dependence of SCR holding voltages in structure-1 and structure-2 layout styles on the operating temperature is shown in Fig. 4.7(c). The holding voltages of the PMOS-triggered SCR device in structure-1 layout style are about ~3.15 V to ~2.65, which is higher than the 2.5-V VDD voltage, under operating temperatures of 25 to 125 ^{o}C. The holding voltages of the PMOS-triggered SCR device in structure-2 layout style are about ~2.78 V to ~2.45 under operating temperatures of 25 to 125 ^{o}C. A diode can be added in series with the PMOS-triggered SCR device of structure-2 to further increase the total holding voltage for latchup-free applications in the CMOS ICs with VDD of 2.5 V.



(a)



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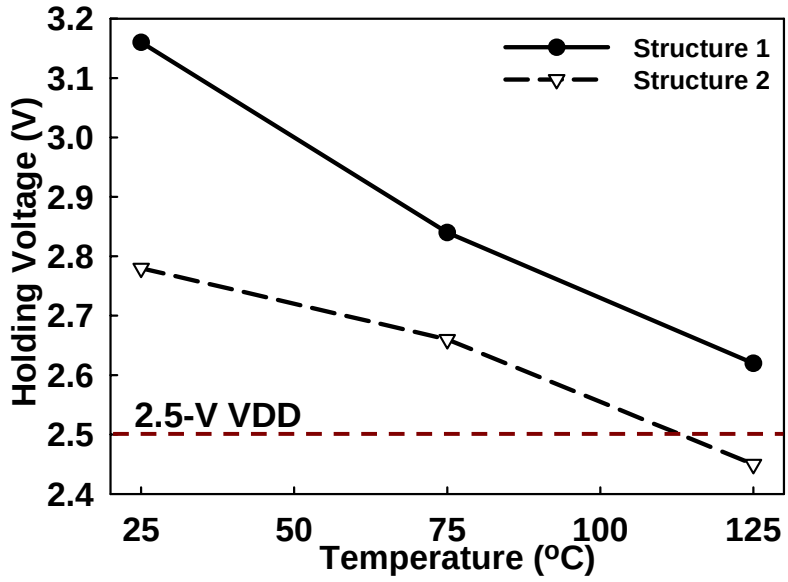


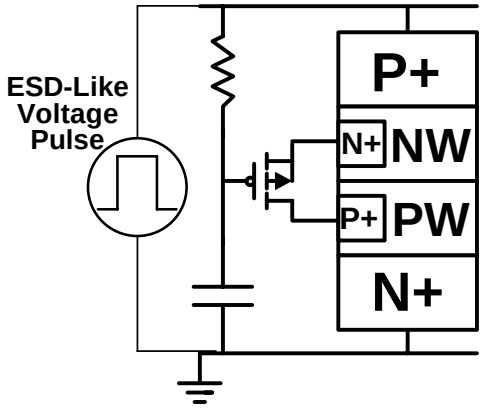
(c)

Fig. 4.7. The DC I-V curves of the initial-on SCR devices with the layout styles of (a) structure-1, and (b) structure-2, under different temperatures. (c) The dependence of SCR holding voltage on the temperature.

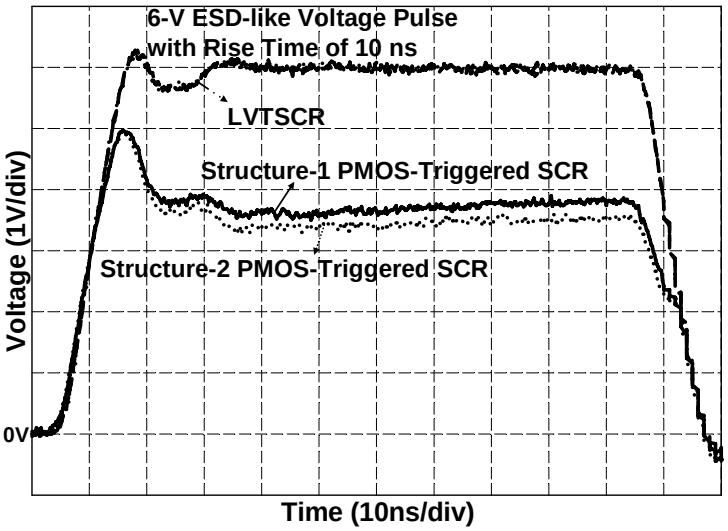
4.3.2. Turn-on Verification

To observe the turn-on efficiency of the initial-on SCR device, 6-V ESD-like voltage pulses with different rise times were applied on the anodes of PMOS-triggered SCR with structure-1, structure-2, and the traditional LVTSCR [23]. The measurement setup for investigating the turn-on efficiency of the initial-on SCR device is illustrated in Fig. 4.8(a). The rise time of Human Body Model (HBM) ESD event is about 2 ns to 10 ns [1]. The

clamped voltage waveforms by different SCR devices are compared in Figs. 4.8(b) and 4.8(c) under the rise times of 10 ns and 1.8 ns, respectively.



(a)



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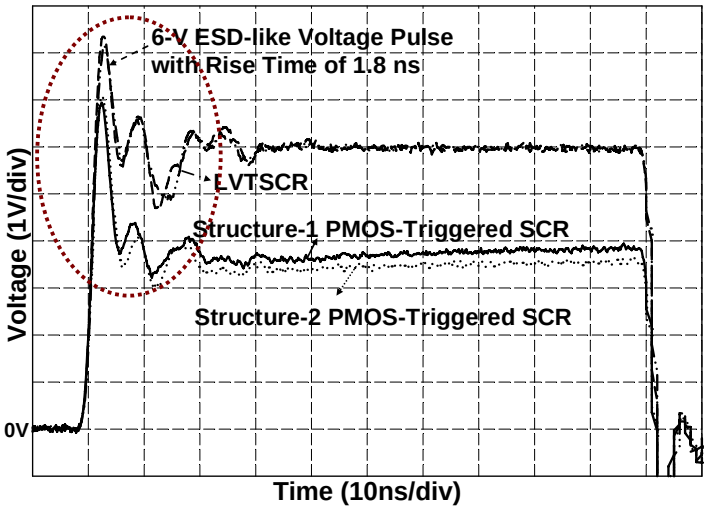

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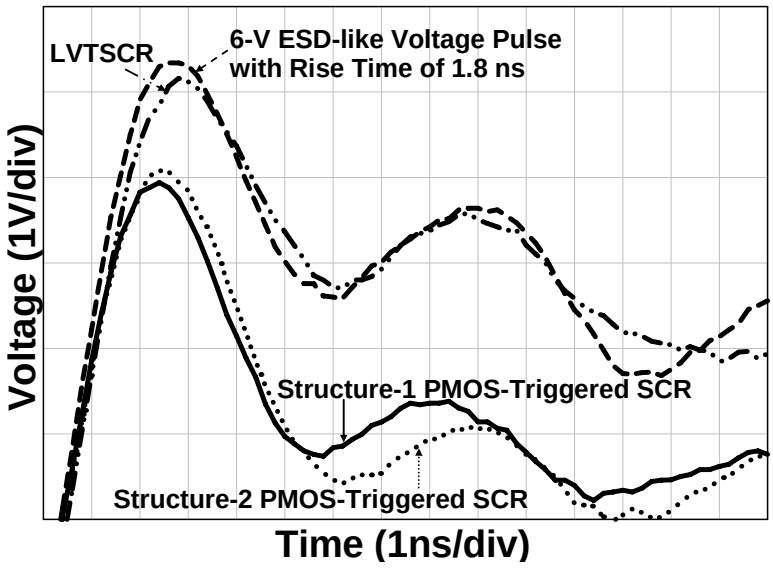


(d)

Fig. 4.8. (a) The measurement setup with ESD-like voltage pulse to investigate the turn-on efficiency of the LVTSCR and the PMOS-triggered SCR in structure-1 and structure-2 layout styles. The 6-V ESD-like voltage pulses were applied to the anodes of SCR devices with the rise time of (b) 10 ns and (c) 1.8 ns. (d) The zoomed-in view on the clamped voltage waveform of (c) around the rising edge.

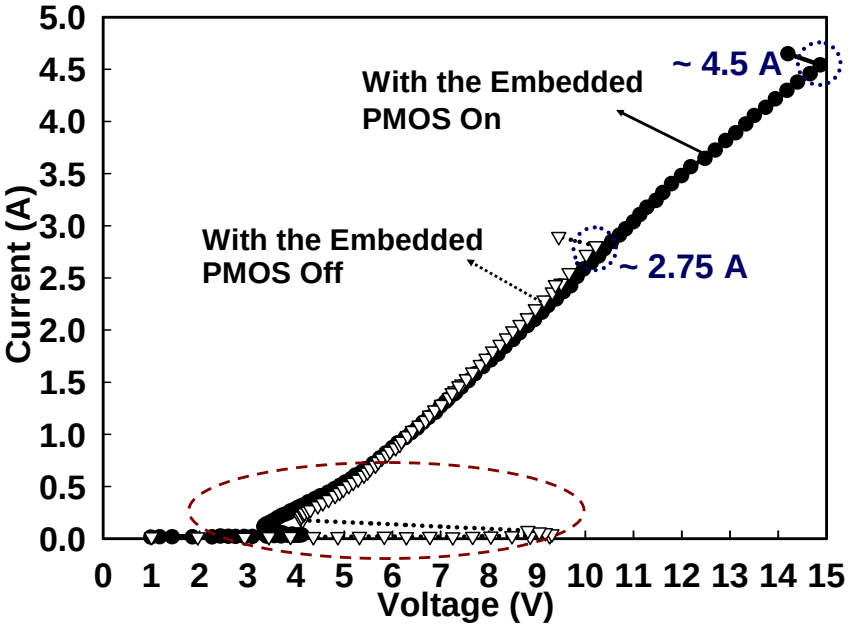
In Fig. 4.8(b), the applied 6-V ESD-like voltage pulse with a rise time of 10 ns is clamped by the PMOS-triggered SCR devices to a lower voltage level (below 4 V). In Fig. 4.8(c) with a rise time of as short as 1.8 ns which is faster than the typical rise time of HBM ESD event, the PMOS-triggered SCR devices performed a lower trigger voltage and higher turn-on efficiency than LVTSCR did. Because the LVTSCR device was triggered by junction breakdown occurring between p-well and the N+ drain diffusion of the embedded GGNMOS transistor, the trigger voltage of LVTSCR was much higher than that of the proposed PMOS-triggered SCR device. When the 6-V ESD-like voltage pulses with the rise time of 10 ns or 1.8 ns were applied on the PMOS-triggered SCR devices, the main SCR structures were rapidly turned on by the PMOS-generated trigger current. However, the LVTSCR device can not be turned on to clamp the overshooting ESD voltage pulses when the 6-V ESD-like voltage pulses were applied. According to the measurement results in Figs. 4.8(b) and 4.8(c), the PMOS-triggered SCR devices can be firstly turned on at a lower applied voltage pulse to efficiently clamp the overshooting ESD voltage pulse to a lower voltage level (below 4 V) at the short period. The rising edges of the voltage waveforms clearly prove the higher turn-on efficiency of the new proposed initial-on SCR devices under both structure-1 and structure-2

layout styles, as the zoomed-in waveforms shown in Fig. 4.8(d). With lower trigger voltage and higher turn-on efficiency, the PMOS-triggered SCR devices can rapidly clamp the overshooting ESD voltage pulse to a lower voltage level. With duration of less than 10 ns, the overshooting ESD voltage pulse can be rapidly clamped to avoid the damage occurrence in internal circuits. Thus, the internal circuits with thinner gate oxide can be well protected by the new proposed initial-on SCR devices.

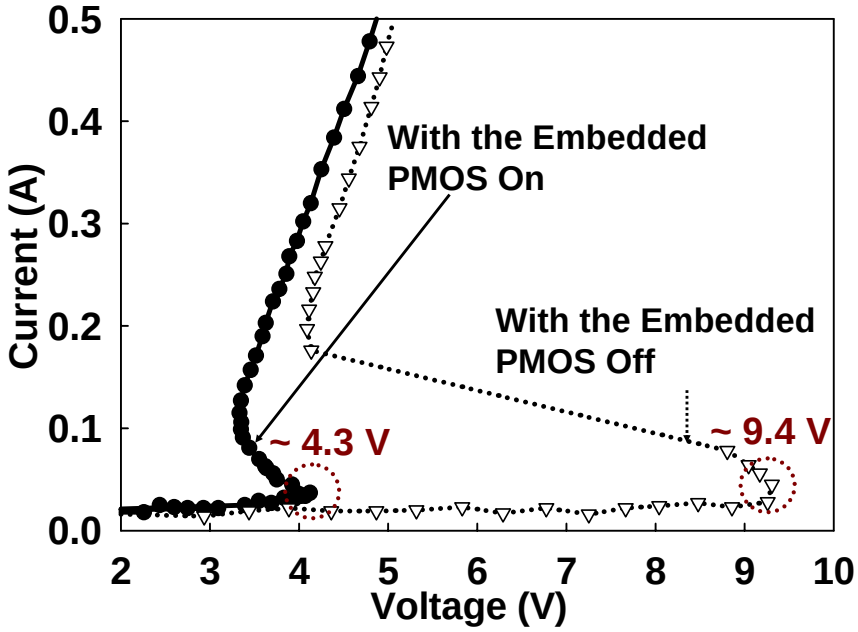
4.3.3. TLP Characteristics

The Transmission Line Pulse (TLP) measured I-V characteristics of the new proposed initial-on SCR devices with the structure-1 and structure-2 layout styles are shown in Figs. 4.9(a), 4.9(b), 4.10(a), and 4.10(b), respectively. The PMOS-triggered SCR devices were measured by the TLP system with a 100-ns pulse width and a 2-ns to 10-ns rise time. The trigger voltages of the PMOS-triggered SCR devices in structure-1 and structure-2 can be significantly reduced from ~9.4 V to ~4.3 V and from ~9.3 V to ~4.2 V, respectively, as shown in Figs. 4.9(b) and 4.10(b). If the gate of embedded PMOS transistor is connected to the anode of SCR (to keep the PMOS off), the SCR devices have trigger voltages of ~9.4 V and ~9.3 V in structure-1 and structure-2, respectively. The second breakdown currents (It2) of the PMOS-triggered SCR devices are also obviously improved, when the embedded PMOS transistor is turned on, as shown in Figs. 4.9(a) and 4.10(a). The PMOS-triggered SCR devices with the embedded PMOS off were triggered by the junction breakdown between the n-well and the P+ drain diffusion of the embedded PMOS transistor. The trigger voltages of the PMOS-triggered SCR devices with the embedded PMOS off are much higher than that with the embedded PMOS on. In addition, because the junction breakdown occurred between the n-well and the P+ drain diffusion of the embedded PMOS transistor, the breakdown mechanism caused the local joule heats at this junction. When the higher TLP energy pulses were applied to the PMOS-triggered SCR devices with the embedded PMOS off, some junction location was produced with high enough joule heats to destroy the contacts. However, the PMOS-triggered SCR devices with the embedded PMOS on were triggered on by the trigger current generated from the PMOS transistor. The higher TLP energy pulses can be effectively discharged by the SCR structures without junction breakdown to avoid the local joule heat occurrence. Therefore, the It2 values of PMOS-triggered SCR devices with the embedded PMOS on are much higher than that with the embedded PMOS off, as shown in Figs. 4.9(a) and 4.10(a). The It2 of the proposed PMOS-triggered SCR device is about 4.5

A (4.6 A) with the layout style of structure-1 (structure-2), whereas the widths of SCR devices are only 50 μm. Moreover, for the PMOS-triggered SCR devices, a It2 of 3.5 A can be achieved before the gate-oxide breakdown of 12 V in the given 0.25-μm CMOS technology with a 5-nm gate-oxide thickness.

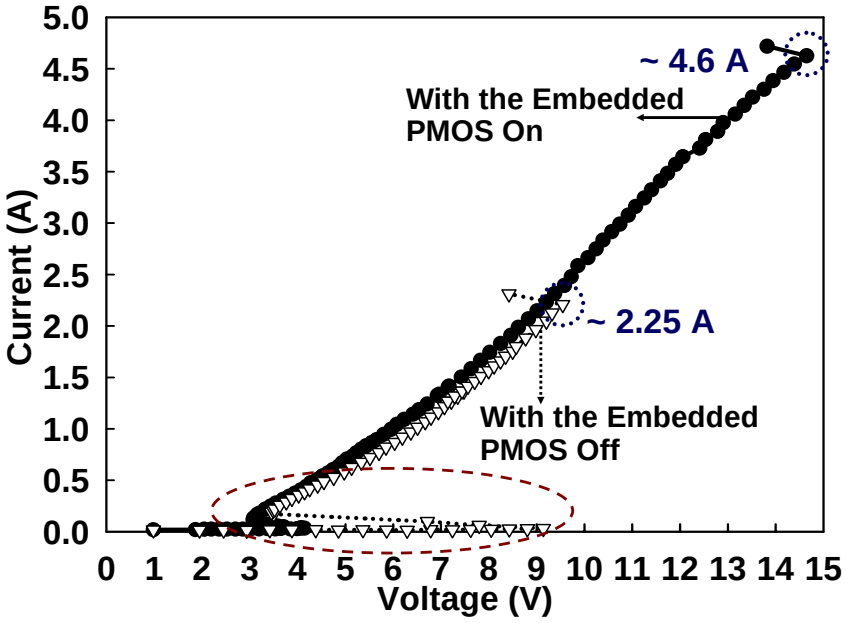


(a)

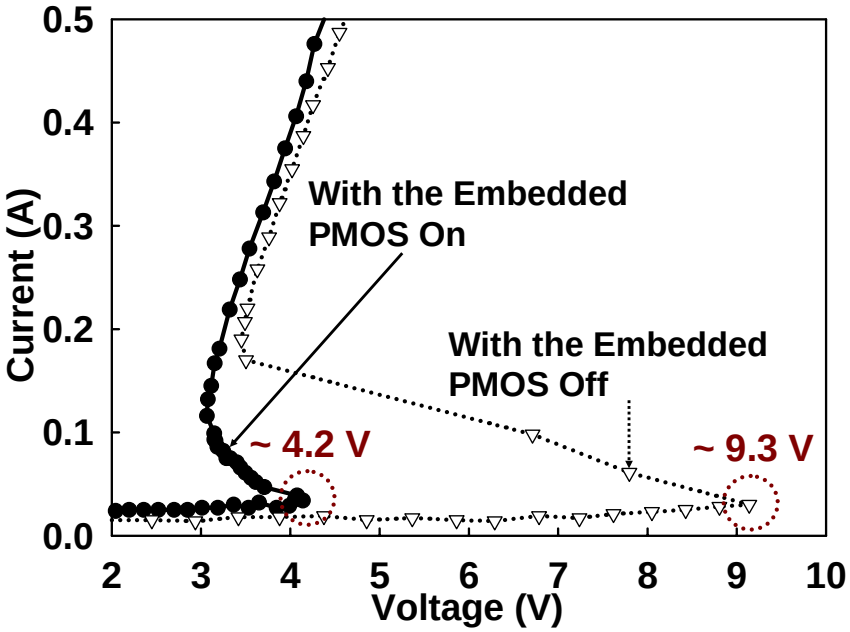


(b)

Fig. 4.9. (a) The TLP-measured I-V curves of the PMOS-triggered SCR device with structure-1 layout style under the embedded PMOS on or off. (b) The zoomed-in view of (a) around the low-current region.



(a)



(b)

Fig. 4.10. (a) The TLP-measured I-V curves of the PMOS-triggered SCR device with structure-2 layout style under the embedded PMOS on or off. (b) The zoomed-in view of (a) in the low-current region.

4.3.4. ESD Robustness

The HBM ESD robustness of the initial-on SCR devices was measured by the *ZapMaster* ESD simulator. The failure criterion is defined as 30% voltage shifting from its original I-V curve at 1-μA bias. With a device width of 50 μm in the given 0.25-μm

fully-silicided CMOS process, the HBM ESD levels of the initial-on SCR devices with structure-1 and structure-2 layout styles are 5.5 kV and 6.0 kV, respectively. Due to the smaller distance between anode and cathode of the SCR device with the structure-2 layout style which has a lower holding voltage, the ESD robustness of PMOS-triggered SCR in structure-2 is higher than that in structure-1.

4.4. Applications for On-Chip ESD Protection

4.4.1. Whole-Chip ESD Protection Scheme

The on-chip ESD protection designs for input, output, and power-rail ESD clamp circuits with the proposed PMOS-triggered SCR devices and the corresponding ESD-transient detection circuits are shown in Fig. 4.11(a). The initial-on SCR device with the lowest Vt1 and the highest turn-on efficiency, as compared to the other SCR devices [22], can effectively protect the internal circuits against ESD damage. Application for power-rail ESD clamp circuit, the initial-on SCR device with the gate bias of VDD on the embedded PMOS has a high enough holding voltage to prevent the latchup issue under the normal circuit operation condition. In addition, the RC-based ESD transient detection circuits among the I/O cells can share the same R and C to save chip area, as that (R1 and C1) shown in Fig. 4.11(a). The initial-on SCR device can provide bi-direction low-impedance discharging paths, which include the turn-on path of the SCR structure and the parasitic diode between n-well and p-well (p-substrate), as shown in Fig. 4.11(b). The initial-on SCR device is placed from each pad to VSS to provide ESD protection for the input or output circuits. The ESD current discharging paths under different ESD-stress conditions, which are positive-to-VSS (PS) mode, negative-to-VSS (NS) mode, positive-to-VDD (PD) mode, and negative-to-VDD (ND) mode, are shown in Figs. 4.12(a), 4.12(b), 4.12(c), and 4.12(d), respectively. In Figs. 4.12(a) and 4.12(b) during PS-mode and NS-mode ESD stresses, the ESD currents are discharged by the initially turned-on PMOS-triggered SCR device and the parasitic diode in the SCR structure, respectively. In Fig. 4.12(c) during PD-mode ESD stress, the ESD current is discharged by the initially turned-on PMOS-triggered SCR device from the pad to the VSS metal line, and then from VSS to the grounded VDD through the parasitic diode of another PMOS-triggered SCR device in the power-rail ESD clamp circuit. In Fig. 4.12(d) during ND-mode ESD stress, the negative ESD current is discharged by the parasitic diode of the SCR device from the pad to the VSS metal line, and then through the initially turned-on

PMOS-triggered SCR device in the power-rail ESD clamp circuit to the grounded VDD pin.

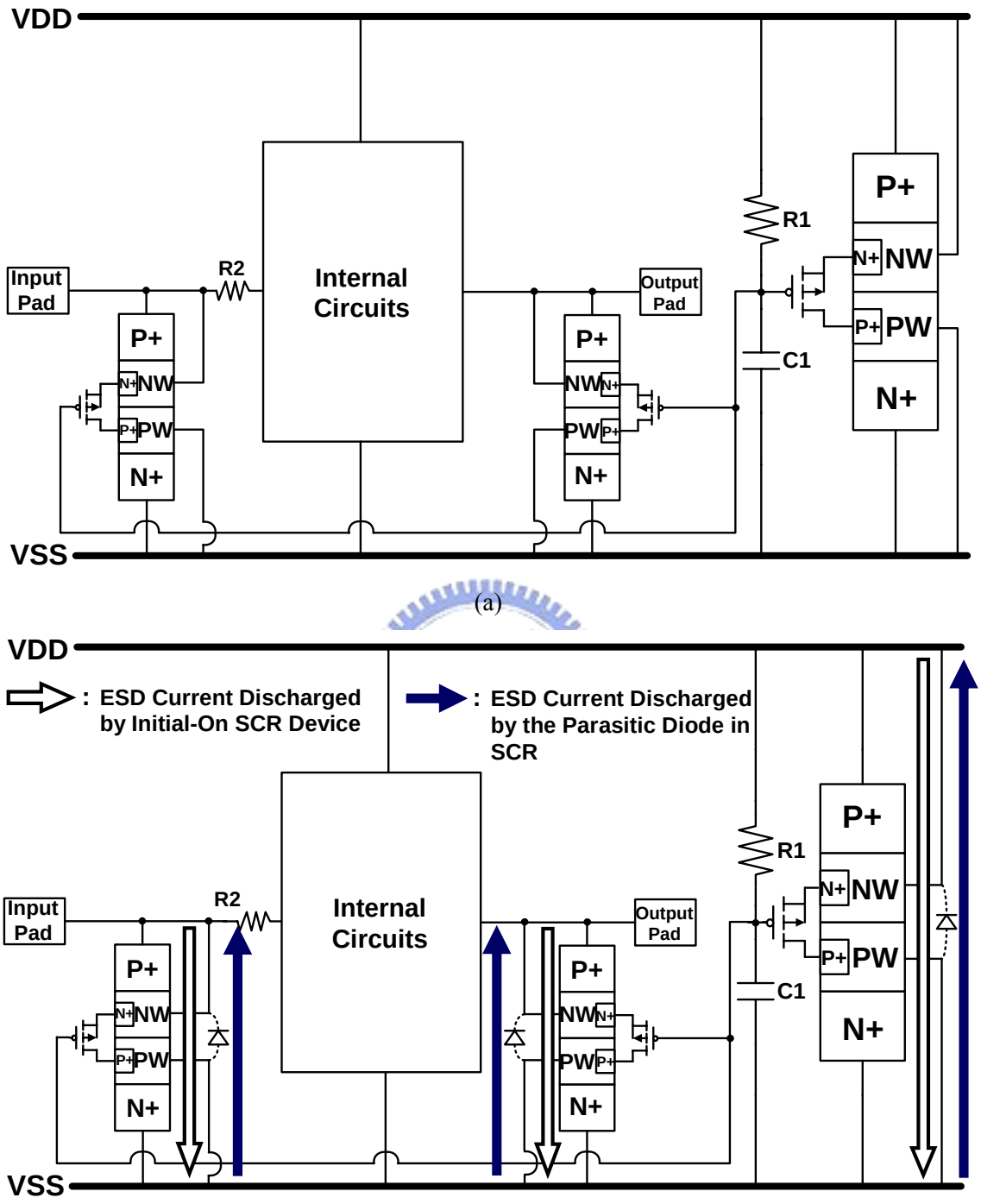


Fig. 4.11. (a) The on-chip ESD protection design for input, output, and power-rail ESD clamp circuits with the initial-on SCR devices. (b) The initial-on SCR device can provide the low-impedance bi-direction discharging paths to discharge ESD currents during different ESD stress conditions.

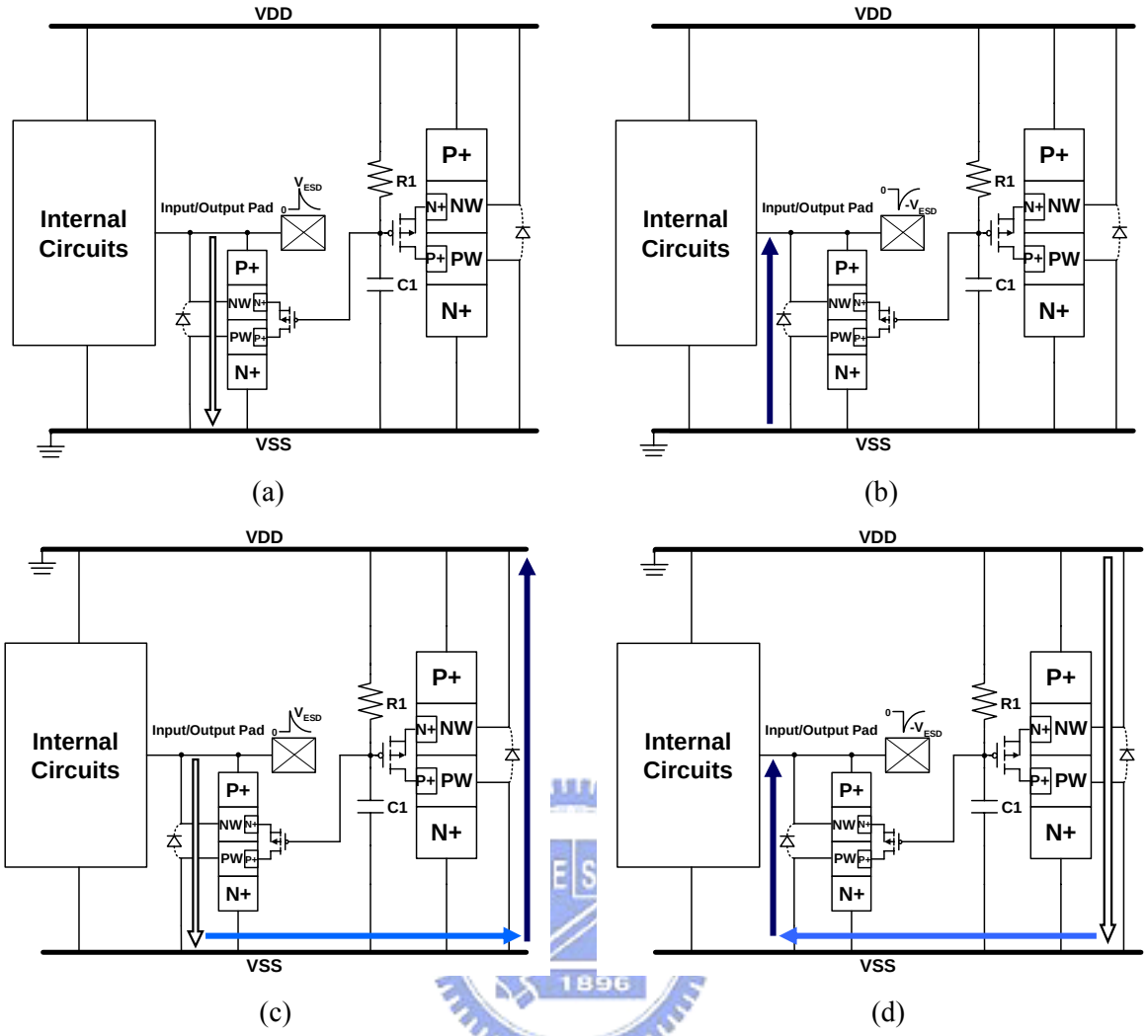


Fig. 4.12. The ESD current discharging paths during the ESD stresses of (a) positive-to-VSS (PS) mode, (b) negative-to-VSS (NS) mode, (c) positive-to-VDD (PD) mode, and (d) negative-to-VDD (ND) mode.

4.4.2. ESD Protection for IC with Multi-Power Domains

The interface circuits in CMOS ICs with separated power domains are often damaged by ESD stress, especially during the I/O pin to I/O pin ESD test. For the chip with separated power domains, the whole-chip ESD protection scheme realized with the proposed initial-on SCR devices and ESD buses is shown in Fig. 4.13. In the same power domain, the anodes of the PMOS-triggered SCR devices are connected to the pads (including I/O, VDD, and VSS pads), and their cathodes are connected to the common ESD bus. The ESD bus can be realized by the wide metal line in the chip to efficiently conduct ESD current of several amperes during ESD stresses. To further save layout area, such ESD bus can be co-designed with the seal ring of the chip [37]. Between the ESD buses, the initial-on SCR devices are also used to connect the separated ESD buses to avoid ESD damage on the interface circuits

between the separated power domains. During ESD stresses, the PMOS-triggered SCR devices with the initial-on function in the whole-chip ESD protection scheme can be quickly triggered on to efficiently protect the internal circuits. The proposed initial-on SCR devices can achieve the same turn-on efficiency of the already-on (native) device for ESD protection, but neither the extra on-chip negative voltage generator nor the native device is needed to realize with this initial-on ESD protection concept with the PMOS-triggered SCR device.

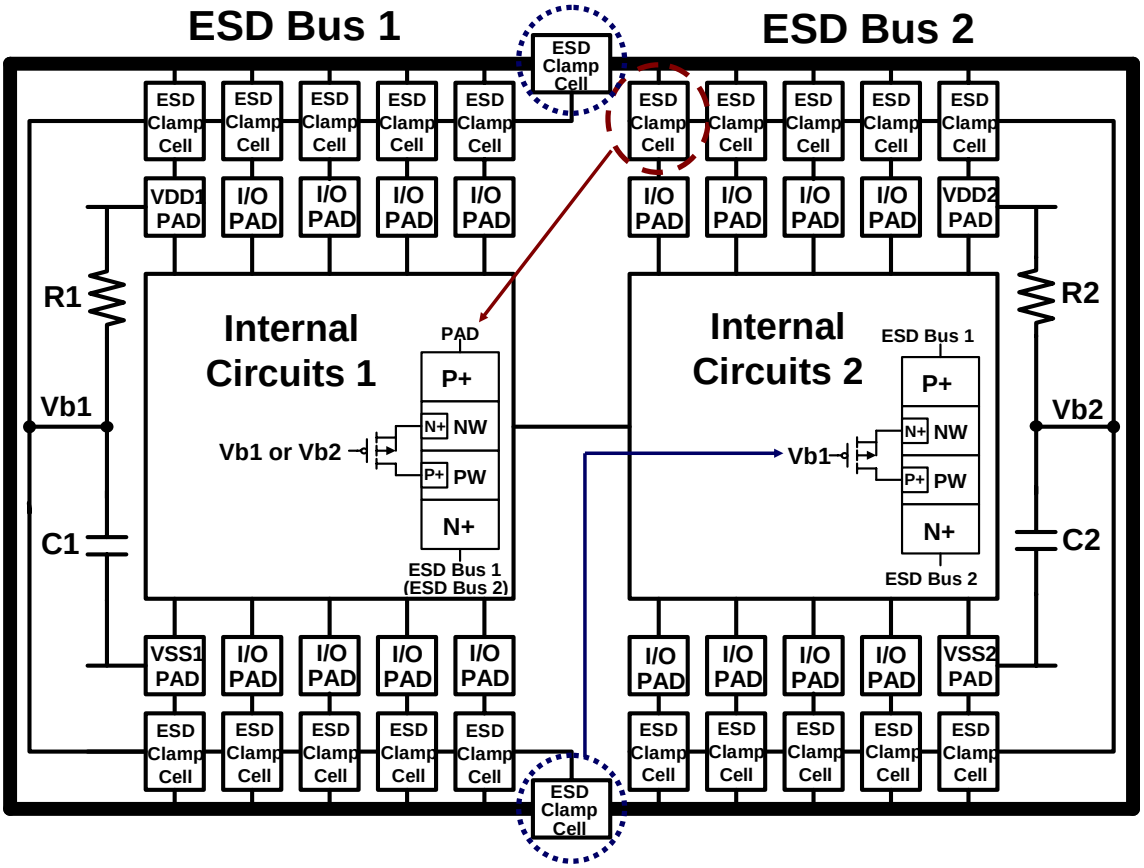


Fig. 4.13. The ESD protection scheme realized with the initial-on SCR devices and ESD buses for the chip with separated power domains.

4.4.3. Discussion

The PMOS-triggered SCR devices have also been implemented in advanced CMOS technologies, such as 0.18-μm CMOS technology and 90-nm CMOS technology. According to the measured results of PMOS-triggered SCR devices in 0.18-μm CMOS technology, the PMOS-triggered SCR devices have the lower trigger voltage (below 3.6 V) and higher second breakdown current (over 4 A) to efficiently protect the internal circuits in deep-submicron CMOS technologies. In addition, the lower holding voltage and smaller

layout area of the SCR devices always are the advantageous to others devices, such as GGNMOS and parasitic lateral NPN bipolar transistor. According to the TLP I-V characteristics of the PMOS-triggered SCR devices, the holding voltages of the PMOS-triggered SCR devices are about 3 V (2.8 V) in 0.25-μm (0.18-μm) CMOS technology. The holding voltages of parasitic diodes in SCR structures are about 0.85 V in 0.25-μm and 0.18-μm CMOS technologies. Due to these excellent ESD protection characteristics, which are lower trigger voltage and lower holding voltage, and higher ESD robustness with smaller layout area, the proposed initial-on ESD protection design with PMOS-triggered SCR device is suitable to apply in nanoscale CMOS technology. To decrease the voltage across the ultra-thin gate oxide of the internal circuits is the main challenge of ESD protection designs. The overstress voltages across the ultra-thin gate oxide will induce the oxide breakdown to cause internal circuit damages. During the ESD stresses, the huge ESD voltages must be firstly clamp to avoid the damages of internal circuits. However, when the ESD currents discharged through the arranged ESD protection circuits, such as pad-to-VDD ESD clamp devices, pad-to-VSS ESD clamp devices, power-rail ESD clamp devices, VDD metal lines, or VSS metal lines, the voltage across the gate oxide were still raised by the holding voltages and IR drops of the ESD clamp devices, and IR drops of the VDD or VSS metal lines. The raised voltages across the gate oxide could cause the damages on the gate oxide of the internal circuits.

For the whole-chip ESD protection design scheme with PMOS-triggered SCR devices, the ESD currents can be discharged by the initially turned-on PMOS-triggered SCR device or parasitic diode in the SCR structure from the pad to the VSS, and then from VSS to VDD through the parasitic diode of another PMOS-triggered SCR device or the other initially turned-on PMOS-triggered SCR device in the power-rail ESD clamp circuit under different ESD-stress conditions. The detail ESD-current discharging paths were illustrated in Figs. 4.12(a), 4.12(b), 4.12(c), and 4.12(d). The discharging paths of PD-mode and ND-mode are longer than that of PS-mode and NS-mode. Therefore, when the ESD stress applied on an input pin, the raised voltage across the gate oxide of the PMOS transistor under PD-mode and ND-mode ESD stresses are higher than that of the NMOS transistor under PS-mode and NS-mode ESD stresses. Under PD-mode or ND-mode ESD stress, raised voltage (V_{oxide}) across the gate oxide of the PMOS transistor can be simply evaluated by the holding voltages (V_h) of a PMOS-triggered SCR device and a parasitic diode, the IR drops of the ESD current (I_{ESD}) discharging through the on resistances (R_{on}) of a PMOS-triggered SCR device and a

parasitic diode, and the IR drops of the ESD current (I_{ESD}) discharging through the resistance (R_M) of VSS metal line. The related equation of the raised voltage is shown as following. The raised voltages across the gate oxide of the PMOS transistor under PD-mode and ND-mode ESD stresses are shown in equation (4.1). The equations (4.2) and (4.3) are shown the raised voltages across the gate oxide of the NMOS transistor under PS-mode and NS-mode ESD stresses, respectively.

$$V_{oxide} = V_{h,\ SCR} + V_{h,\ diode} + I_{ESD} \times (R_{on,\ SCR} + R_{on,\ diode} + R_M) \quad (4.1)$$

$$V_{oxide} = V_{h,\ SCR} + I_{ESD} \times R_{on,\ SCR} \quad (4.2)$$

$$V_{oxide} = V_{h,\ diode} + I_{ESD} \times R_{on,\ diode} \quad (4.3)$$

The holding voltages of the PMOS-triggered SCR devices are about 3 V in 0.25-μm CMOS technology. The holding voltages of parasitic diodes in SCR structures are about 0.85 V in 0.25-μm CMOS technologies. The on resistances (R_{on}) of a PMOS-triggered SCR device and a parasitic diode in the SCR structure with the 50-μm device sizes are respectively about 2.5 Ω and 1.25 Ω. Generally, the resistances of the VSS metal lines or VDD metal lines are about several tens mini- Ω in deep-submicron CMOS technology. Before the gate-oxide breakdown of 12 V in the given 0.25-μm CMOS technology, the I_{ESD} can achieve over 2 A (about HBM ESD robustness of 3 kV) under the PD-mode or ND-mode ESD stress in the whole PMOS-triggered SCR devices with the device sizes of 50 μm. On the other hand, the I_{ESD} of the NS-mode or PS-mode ESD stress was higher than that of the PD-mode or ND-mode, because the whole-chip ESD protection design scheme with PMOS-triggered SCR devices had the shorter ESD discharging paths in NS-mode or PS-mode ESD stress.

For more advanced CMOS technology applications with the ultra thin gate oxide, the holding voltage and the on resistance (R_{on}) of the PMOS-triggered SCR devices needs to be further decreased to reduce the raised voltage across the ultra thin gate oxide of the internal circuits. However, the holding voltages of the SCR devices are dependent on the anode-to-cathode spacing of the SCR structures. The anode-to-cathode spacing of the PMOS-triggered SCR devices can be adjusted by the layout modifications of the embedded PMOS transistor, n-triggered node, and p-triggered node, such as the PMOS-triggered SCR devices with different layout styles of structure-1 and structure-2. The holding voltages of the PMOS-triggered SCR devices can be adjusted by different layout styles with different

anode-to-cathode distances to reduce for more advanced CMOS technology applications. The holding voltages would be reduced below 2 V in the SCR devices with the shortest anode-to-cathode spacing. In addition, the on resistances (R_{on}) of the PMOS-triggered SCR devices can be significantly reduced by increasing the device widths. The on resistances (R_{on}) of the PMOS-triggered SCR devices are directly proportional to the device widths. The ESD robustness also can be obviously improved in the increments of the device widths. Therefore, the PMOS-triggered SCR devices with the shorter anode-to-cathode spacing and large device width can efficiently reduce the raised voltage across the ultra thin gate oxide of the internal circuits for ESD protection applications in nanoscale CMOS technology.

4.5. Summary

The "*initial-on*" ESD protection concept realized by the PMOS-triggered SCR device with RC-based ESD-transient detection circuit has been successfully designed and verified in a 0.25-μm salicided CMOS process. Compared to the LVTSCR, the lowest trigger voltage and the highest turn-on efficiency of SCR device can be achieved by the proposed PMOS-triggered technique for effective on-chip ESD protection. Such a PMOS-triggered SCR also presents a high enough holding voltage to overcome the latchup issue under the normal circuit operation condition. The ESD robustness of the PMOS-triggered SCR can be higher than 5.5 kV with a device width of as small as 50 μm. Therefore, such initial-on SCR devices can achieve the whole-chip ESD protection scheme for input, output, power-rail ESD clamp circuit, and the ESD clamp cells between the separated power domains.

Chapter 5

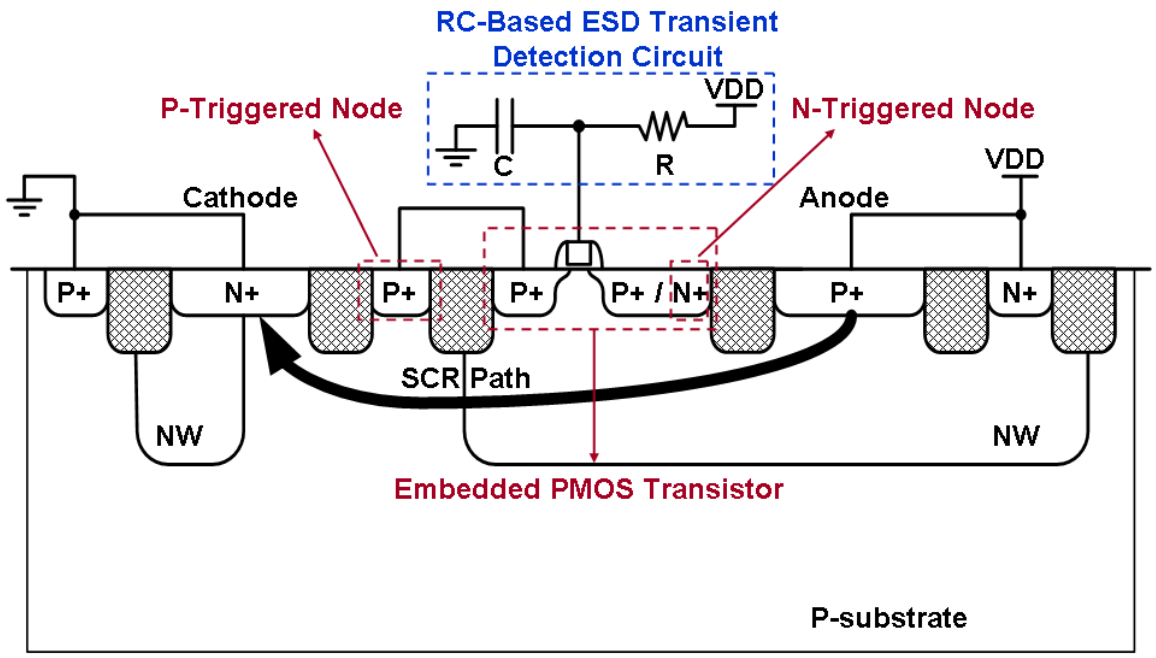
Optimization on MOS-Triggered SCR Structures for On-Chip ESD Protection

As discussed in Chapter 4, the performance of initial-on SCR design implemented by PMOS-triggered SCR device has been proposed to achieve the lowest trigger voltage and the highest turn-on efficiency of SCR device for effective on-chip ESD protection. In this chapter, further optimizations on the PMOS-triggered SCR devices are presented. The modified PMOS-triggered SCR device with merged layout style is proposed to enhance its ESD protection capability. In addition, NMOS transistor is also embedded into the SCR structures to implement NMOS-triggered SCR devices. The device characteristics of these two different MOS-triggered SCR devices are compared to optimize the on-chip ESD protection design in CMOS ICs.

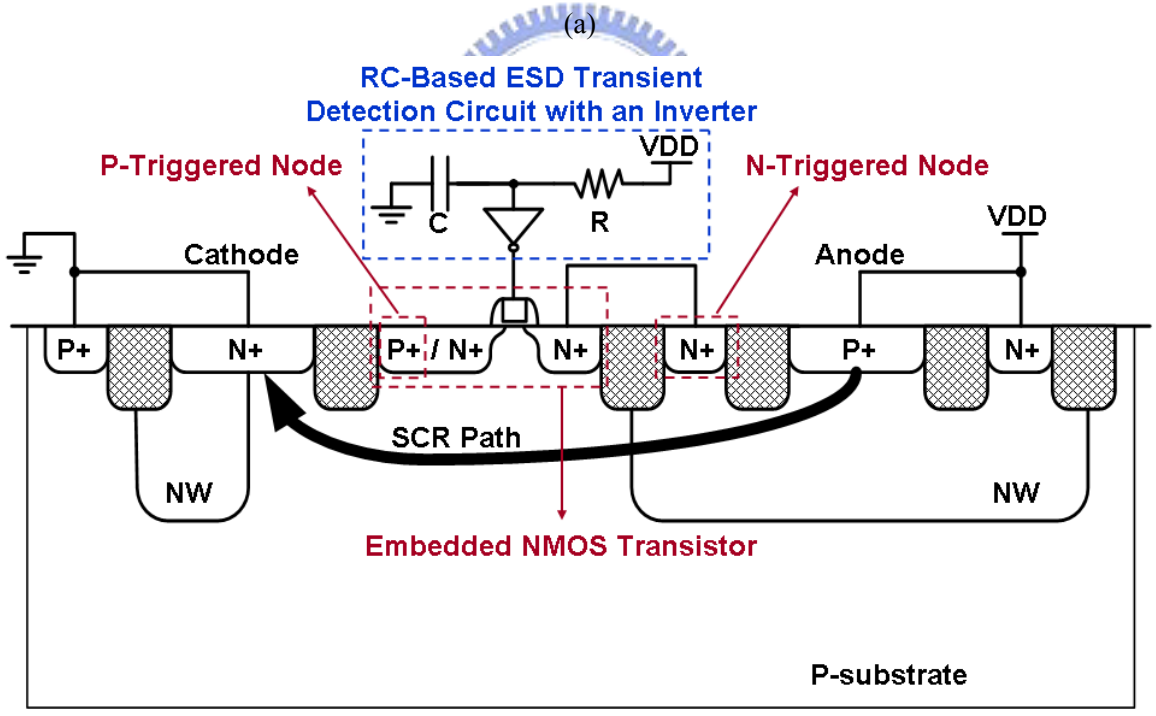
5.1. SCR Devices with Embedded MOS Transistors

The PMOS-triggered SCR device with embedded PMOS transistor and RC-based ESD transient detection circuit is shown in Fig. 5.1(a) [45]. The source and drain terminals of embedded PMOS transistors are respectively connected to the n-triggered and p-triggered nodes to synchronously generate double trigger currents into n-well and p-well of the SCR structure. The gate terminal of embedded PMOS transistor is tied to a RC-based ESD transient detection circuit. Compared to the PMOS-triggered SCR device, the NMOS-triggered SCR device is implemented with an embedded NMOS transistor, as shown in Fig. 5.1(b). The source and drain terminals of the embedded NMOS transistor are respectively connected to the p-triggered and n-triggered nodes. The gate terminal of embedded NMOS transistor is tied to a RC-based ESD transient detection circuit with an inverter. Due to the difference in the rise times between the ESD pulse and the VDD power-on voltage, the RC time constant in the ESD transient detection circuit is traditionally designed about 0.1~1 micro-second to distinguish the ESD stress condition from the normal circuit operation condition [6], [7]. To achieve the desirable operation, the RC time constant

of ESD transient detection circuit is designed as 0.4 μs in this work.



(a)

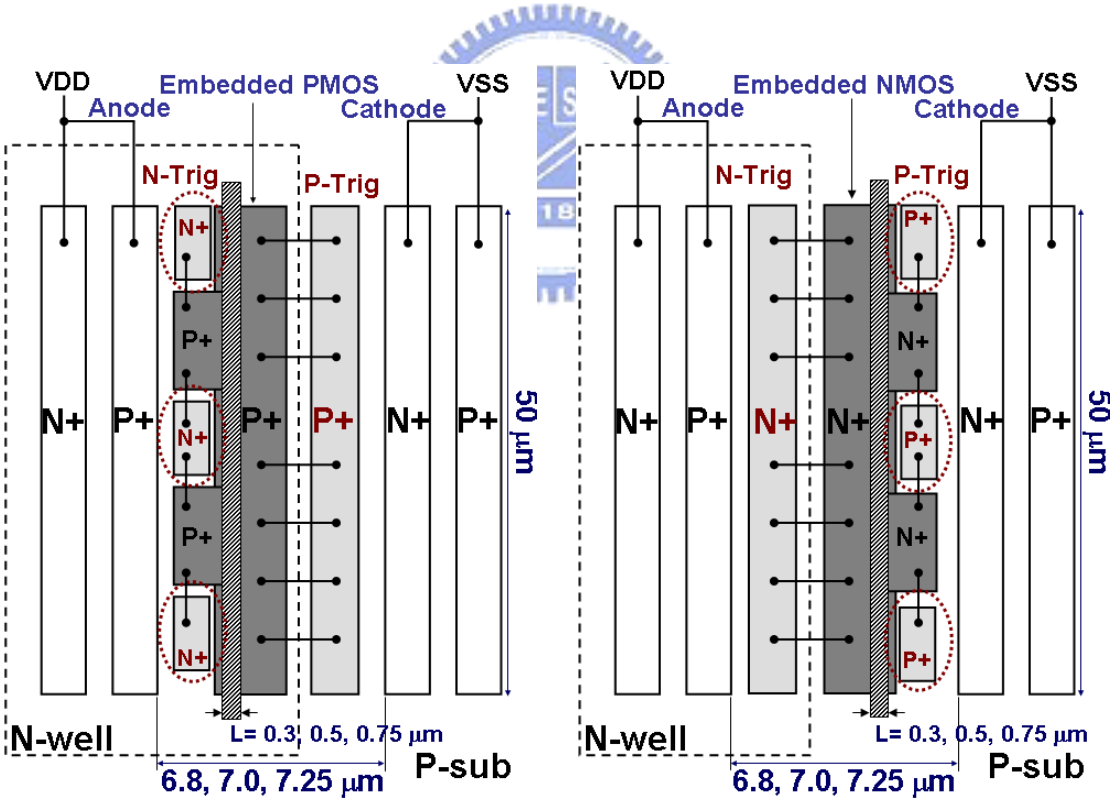


(b)

Fig. 5.1. Cross-sectional views of (a) the PMOS-triggered SCR device with RC-based ESD transient detection circuit, and (b) the NMOS-triggered SCR device with RC-based ESD transient detection circuit and an inverter.

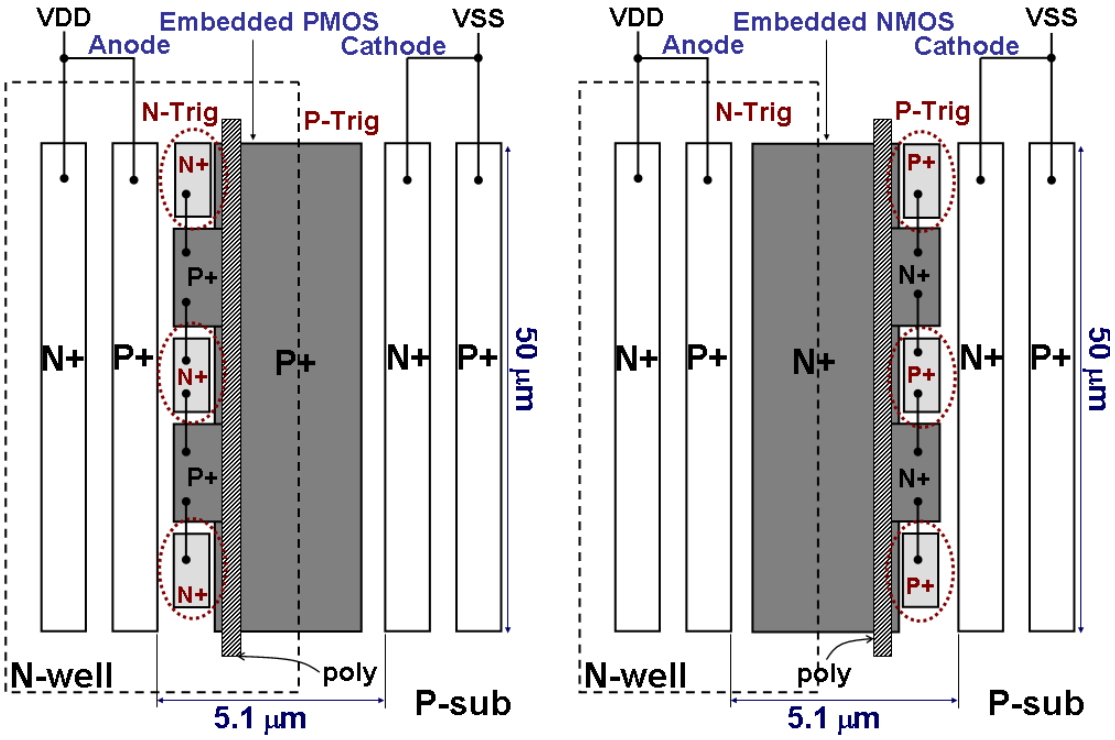
Three different channel lengths (L), which are 0.3 μm, 0.5 μm, and 0.75 μm, of the embedded MOS transistors in the MOS-triggered SCR devices are investigated in this work.

The layout top views of the MOS-triggered SCR device are illustrated in Figs. 5.2(a) and 5.2(b). With the three different channel lengths in the embedded MOS transistors, the anode-to-cathode spacings are therefore different in the MOS-triggered SCR devices. They are 6.8 μm, 7.0 μm, and 7.25 μm in the MOS-triggered SCR devices with channel lengths of 0.3 μm, 0.5 μm, and 0.75 μm in the embedded MOS transistors, respectively. The MOS-triggered SCR device with merged layout style is also proposed and implemented in this work. The p-triggered node (or the n-triggered node) was directly merged into the drain side of the embedded PMOS transistor (or the embedded NMOS transistor), and located across the junction between n-well and p-well. The layout top views of the MOS-triggered SCR devices with shorter anode-to-cathode spacing are illustrated in Figs. 5.3(a) and 5.3(b). This shorter anode-to-cathode spacing is only 5.1 μm with the channel length of 0.3 μm in the embedded MOS transistor. The device widths of all MOS-triggered SCR devices in this work are kept the same of 50 μm, which have been fabricated in a 0.18-μm fully-silicide CMOS process.



(a) (b)

Fig. 5.2. Top views of (a) the PMOS-triggered, and (b) the NMOS-triggered, SCR devices with three different channel lengths of 0.3 μm, 0.5 μm, and 0.75 μm in the embedded MOS transistor (original layout style).



(a) (b)

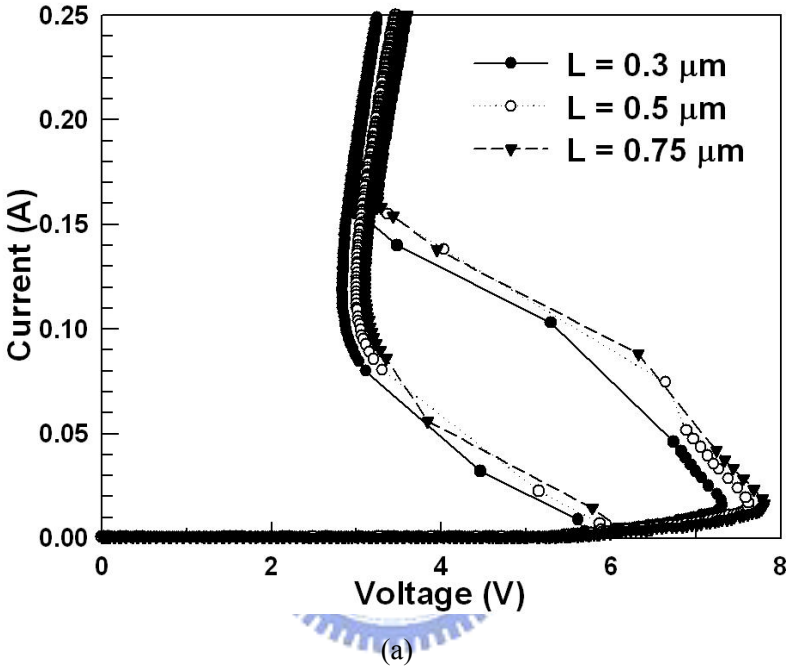
Fig. 5.3. Top views of (a) the PMOS-triggered SCR device, and (b) NMOS-triggered SCR device, with merged layout style. Both anode-to-cathode spacings of PMOS-triggered and NMOS-triggered SCR devices are only 5.1 μm.

5.2. Experimental Results

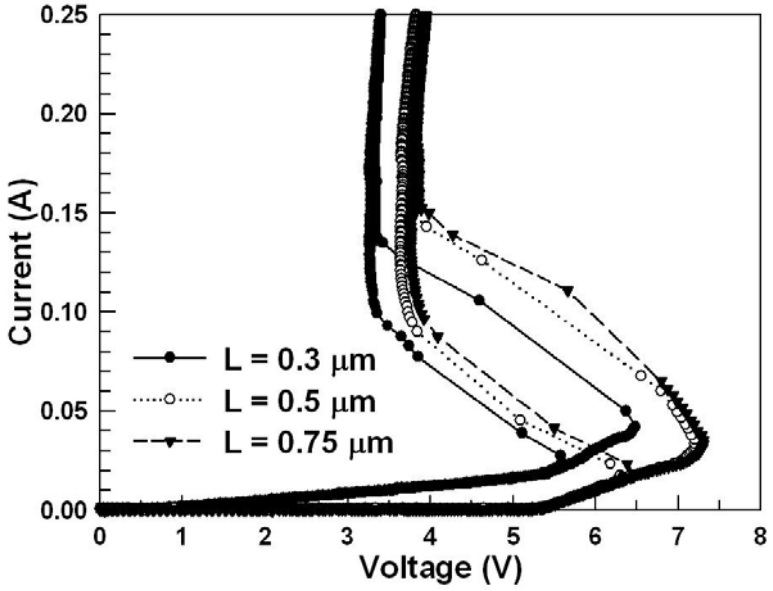
5.2.1. Device Characteristics of the MOS-Triggered SCR Devices

During the normal circuit operation condition with VDD and VSS biases, the gate terminals of embedded PMOS and NMOS transistors were biased at VDD and VSS respectively to keep themselves off. The measured DC I-V curves of the MOS-triggered SCR devices with different channel lengths in the embedded MOS transistors (original layout style) are shown in Figs. 5.4(a) and 5.4(b). The DC trigger voltage (Vt1) and holding voltage (Vh) of PMOS-triggered SCR device with 0.3-μm channel length are 7.30 V and 2.82 V, respectively. On the other hand, the NMOS-triggered SCR devices with 0.3-μm, 0.5-μm, and 0.75-μm channel lengths have the Vh of 3.28 V, 3.63 V, and 3.75 V, respectively. Their corresponding Vt1 are 6.50 V, 7.17 V, and 7.19 V. The Vt1 and Vh are increased by increasing the channel length of the embedded MOS transistor. Besides, according to the measured results in Figs. 5.5(a) and 5.5(b), the Vt1 of the MOS-triggered SCR device with merged layout style is similar to that with original layout style. However, the merged layout

style can slightly reduce the Vh of MOS-triggered SCR devices due to the shorter anode-to-cathode spacing in the layout. All Vh of MOS-triggered SCR devices with different channel lengths and different layout styles are still greater than VDD of 1.8 V in this work. The DC Vt1 and Vh of PMOS-triggered and NMOS-triggered SCR devices were listed in Table 5.1, respectively. The difference in Vt1 between the NMOS-triggered and PMOS-triggered SCR devices can be attributed to the different drain breakdown voltages of NMOS and PMOS transistors.

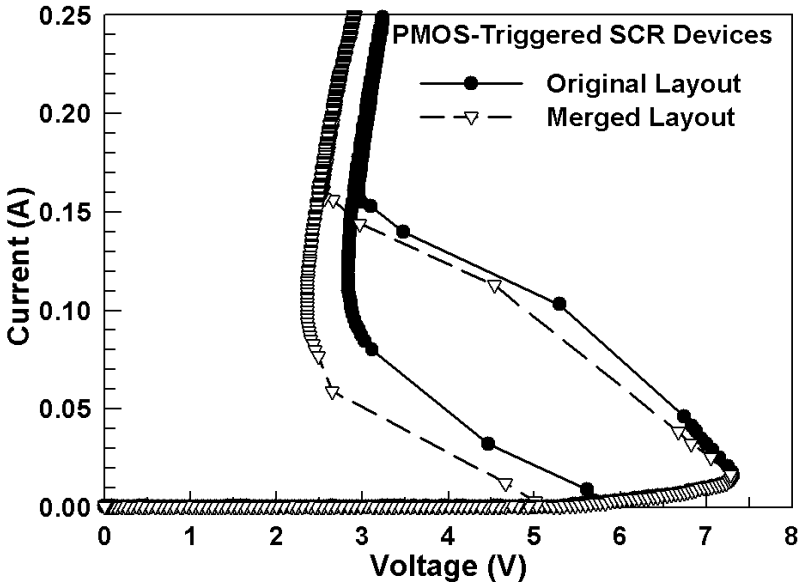


(a)

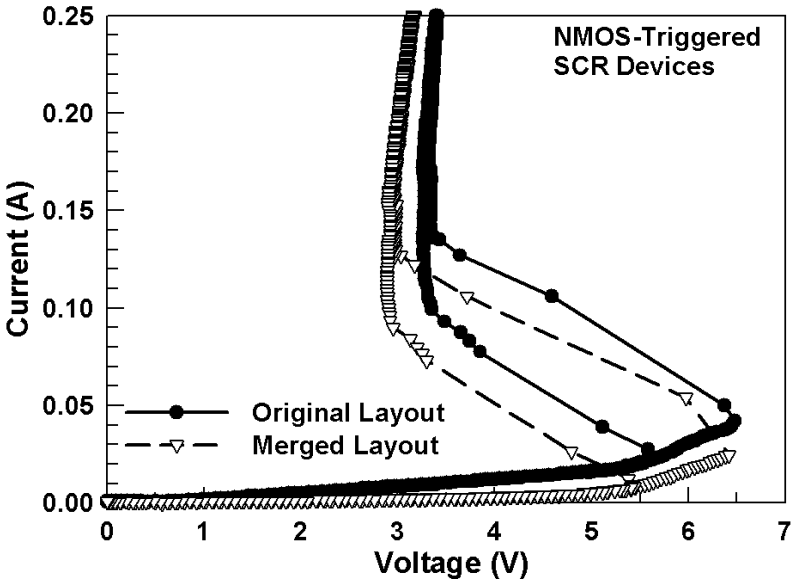


(b)

Fig. 5.4. The DC I-V curves of (a) the PMOS-triggered, and (b) the NMOS-triggered, SCR devices with three different channel lengths in the embedded MOS transistors (original layout style).



(a)



(b)

Fig. 5.5. The DC I-V curves of (a) the PMOS-triggered, and (b) the NMOS-triggered, SCR devices under two different layout styles.

5.2.2. Turn-on Verifications of the MOS-Triggered SCR Devices

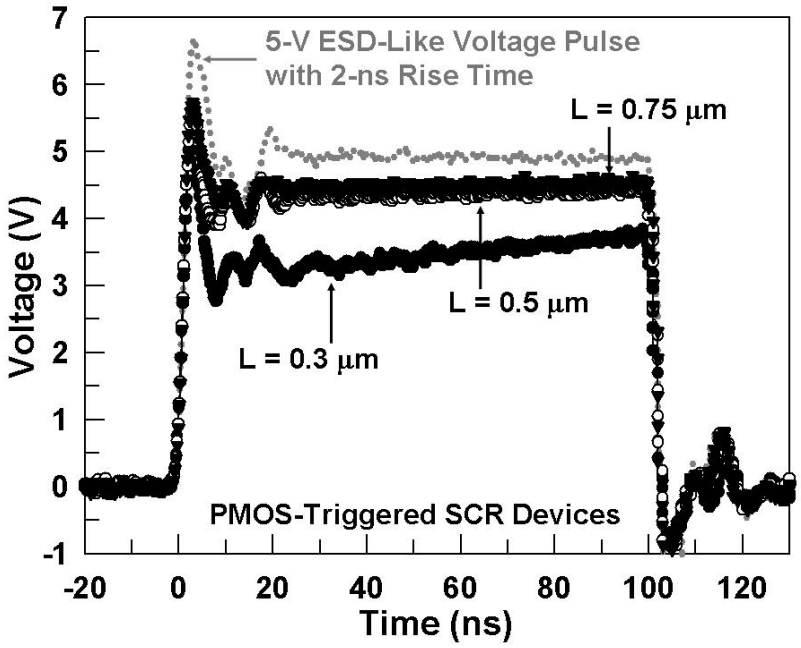
In order to observe the turn-on efficiency of the MOS-triggered SCR devices with different channel lengths in the embedded PMOS and NMOS transistors, a 5-V ESD-like voltage pulse with fast rise time of 2 ns was applied on each VDD terminal (anode) of the MOS-triggered SCR device with its VSS terminal (cathode) grounded. The rise time of Human-Body-Model (HBM) ESD event is about 2 ns to 10 ns [1]. The voltage pulse with a rise time of 2 ns generated from a pulse generator is used to simulate the fast rising edge of

HBM ESD event. The sharp-rising edge of the ESD-like voltage pulse will be detected by the RC-based ESD transient detection circuit and then to trigger on the MOS-triggered SCR devices. When the MOS-triggered SCR device is turned on, the voltage waveform on VDD node will be clamped down as the measured results shown in Figs. 5.6(a) and 5.6(b). The PMOS-triggered SCR device (original layout style) with 0.3-μm channel length in the embedded PMOS transistor can efficiently clamp the overshooting ESD voltage pulse to a lower voltage level, as shown in Fig. 5.6(a). However, all of NMOS-triggered SCR devices (original layout style) with 0.3-μm, 0.5-μm, and 0.75-μm channel lengths present high turn-on efficiency to clamp the voltage potentials at a much lower level. Due to the larger driving current capability in the embedded NMOS transistor, the NMOS-triggered SCR devices exhibit excellent turn-on efficiency, as illustrated in Fig. 5.6(b).

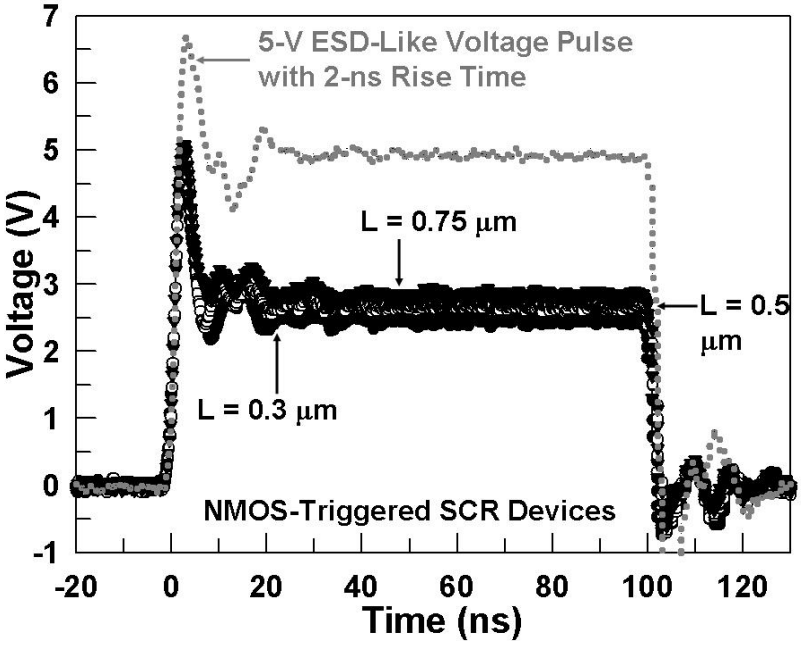
Table 5.1

Device Characteristics of PMOS-Triggered and NMOS-Triggered SCR Devices with Three Different Channel Lengths in Embedded MOS Transistors and Two Different Layout Styles

Device Characteristics		Original Layout Style						Merged Layout Style	
		L= 0.3 μm		L= 0.5 μm		L= 0.75 μm		L= 0.3 μm	
		PMOS-Triggered	NMOS-Triggered	PMOS-Triggered	NMOS-Triggered	PMOS-Triggered	NMOS-Triggered	PMOS-Triggered	NMOS-Triggered
DC	Vt1	7.30 V	6.50 V	7.61 V	7.17 V	7.83 V	7.19 V	7.30 V	6.48 V
	Vh	2.82 V	3.28 V	3.00 V	3.63 V	3.12 V	3.75 V	2.35 V	2.88 V
TLP	Vt1	3.50 V	2.47 V	4.41 V	2.72 V	5.12 V	2.98 V	3.40 V	2.44 V
	Vh	2.81 V	2.36 V	3.10 V	2.56 V	3.38 V	2.68 V	2.40 V	2.28 V
	Ron	2.71 Ω	2.60 Ω	3.28 Ω	2.81 Ω	3.31 Ω	2.78 Ω	2.40 Ω	2.13 Ω
	It2	3.05 A	2.67 A	3.51 A	2.71 A	3.92 A	2.78 A	4.17 A	4.22 A
ESD Level	HBM	5.0 kV	4.0 kV	6.5 kV	4.5 kV	6.5 kV	4.5 kV	7.0 kV	7.0 kV
	MM	200 V	150 V	250 V	200 V	300 V	200 V	350 V	350 V



(a)



(b)

Fig. 5.6. Under 5-V ESD-like voltage pulses with 2-ns rise time, the clamped voltage waveforms by (a) the PMOS-triggered SCR devices, and (b) the NMOS-triggered SCR devices, under three different channel lengths in the embedded MOS transistors (original layout style).

5.2.3. TLP I-V Characteristics and ESD Robustness

The TLP [50] I-V curves of the MOS-triggered SCR devices with different channel lengths and layout styles in the embedded PMOS or NMOS transistors were shown in Figs. 5.7(a), 5.7(b), 5.8(a), and 5.8(b), respectively.

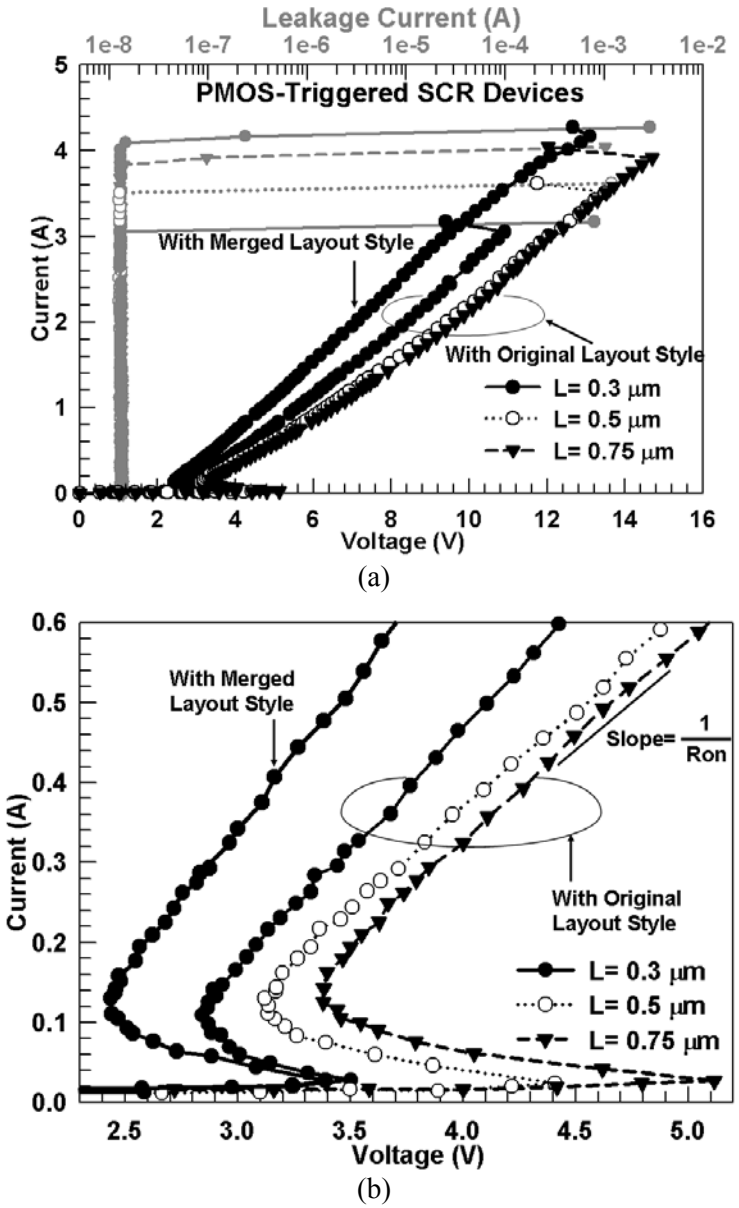


Fig. 5.7. (a) The TLP-measured I-V curves of the PMOS-triggered SCR devices with different channel lengths and different layout styles in the embedded PMOS transistors. (b) The zoomed-in view of (a) around the low-current range.

The trigger voltages (Vt1) of the PMOS-triggered SCR devices are decreased from ~5.12 V to ~3.50 V in the embedded PMOS transistors with 0.75-μm to 0.3-μm channel lengths, whereas those of the NMOS-triggered SCR devices are also decreased from ~2.98 V to ~2.47 V by decreasing the channel lengths from 0.75 μm to 0.3 μm. The shorter channel lengths in the embedded MOS transistors can generate the higher trigger currents to reduce the Vt1 of MOS-triggered SCR devices. The holding voltages (Vh) are decreased from ~3.38 V to ~2.81 V by decreasing the channel lengths from 0.75 μm to 0.3 μm in the embedded PMOS transistors, and those are similarly decreased from ~2.68 V to ~2.36 V by decreasing

the channel lengths in the embedded NMOS transistors. The on resistances (Ron), which are extracted from TLP-measured I-V curves, of the PMOS-triggered (or NMOS-triggered) SCR devices with 0.3-μm, 0.5-μm, and 0.75-μm channel lengths in the embedded PMOS transistors (or NMOS transistors) are 2.71 Ω, 3.28 Ω, and 3.31 Ω (or 2.60 Ω, 2.81 Ω, and 2.78 Ω), respectively, as listed in Table 5.1. The second breakdown currents (It2s) are increased from ~3.05 A to ~3.92 A (from ~2.67 A to ~2.78 A) by increasing the channel lengths from 0.3 μm to 0.75 μm in the PMOS-triggered (NMOS-triggered) SCR devices.

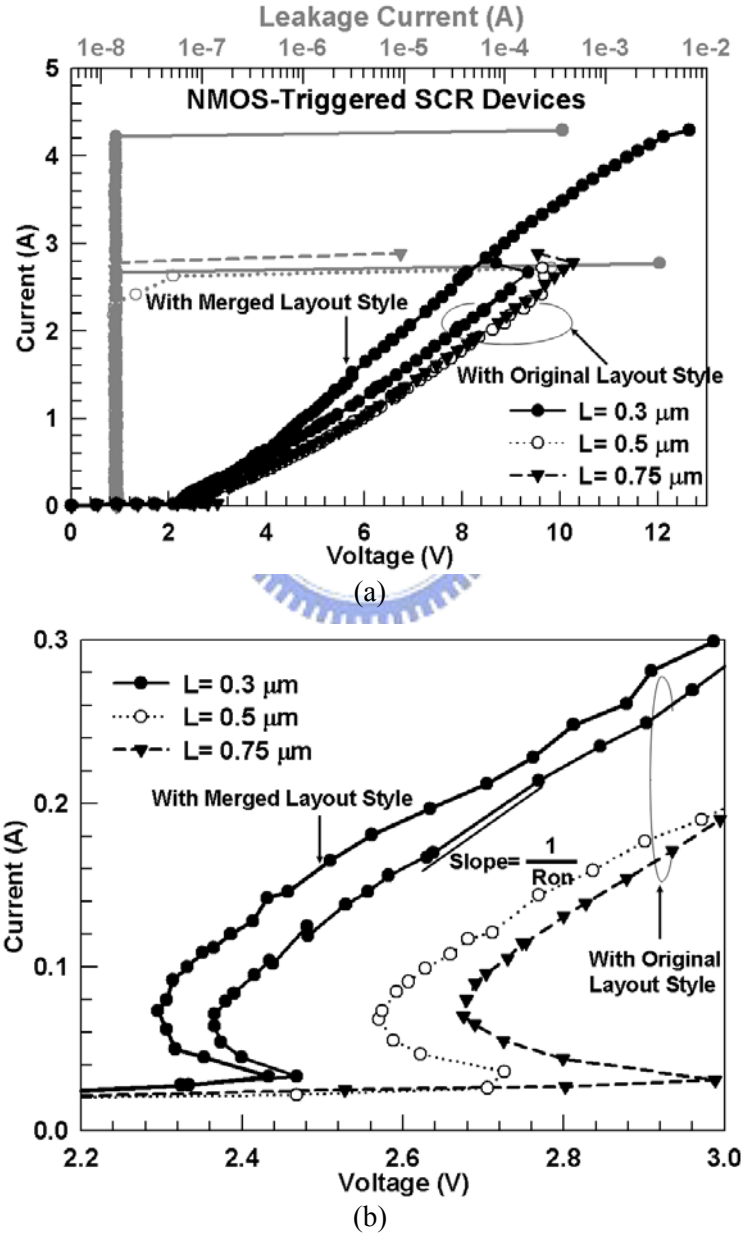


Fig. 5.8. (a) The TLP-measured I-V curves of the NMOS-triggered SCR devices with different channel lengths and different layout styles in the embedded NMOS transistors. (b) The zoomed-in view of (a) around the low-current range.

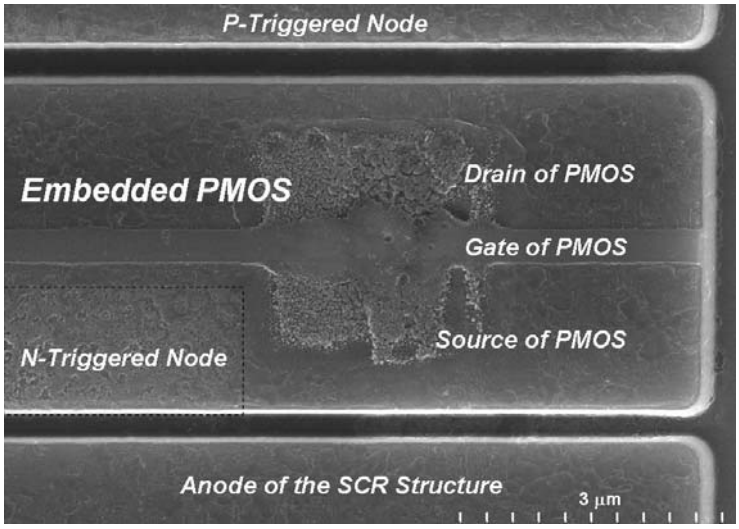
In addition, the HBM (MM) ESD robustness of the PMOS-triggered SCR devices with 0.3-μm, 0.5-μm, and 0.75-μm channel lengths are 5.0 kV (200 V), 6.5 kV (250 V), and 6.5 kV (300 V). They are 4.0 kV (150 V), 4.5 kV (200 V), and 4.5 kV (200 V) in NMOS-triggered SCR devices, as listed in Table I. Although the NMOS-triggered SCR devices have lower Vh and Ron, all of the PMOS-triggered SCR devices have the higher ESD robustness and It2. The reasons will be attributed to the different failure mechanisms in PMOS-triggered and NMOS-triggered SCR devices. Moreover, the MOS-triggered SCR device with merged layout style has a lower Vh, a smaller Ron, and a higher It2 due to a shorter anode-to-cathode spacing and higher turn-on efficiency. The It2 of the PMOS-triggered (NMOS-triggered) SCR device with merged layout style achieves 4.17 A (4.22 A), which is over 1-A higher than that with original layout style, as compared in Figs. 5.7(a) and 5.8(a). The HBM (MM) ESD robustness of the PMOS-triggered and NMOS-triggered SCR devices with merged layout styles are 7.0 kV (350 V) and 7.0 kV (350 V), respectively, in Table 5.1.

5.3. Failure Analysis and Discussion

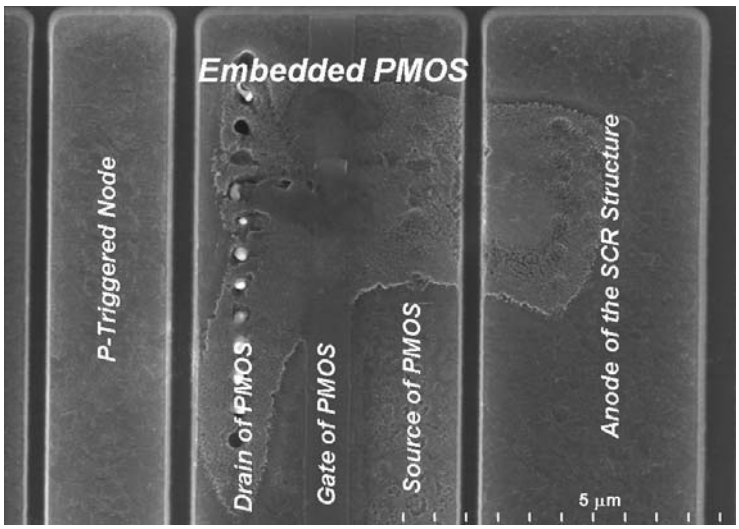
5.3.1. Failure Analysis

The failure spot investigated by SEM image is located at the embedded PMOS transistor in the PMOS-triggered SCR device with 0.3-μm channel length, as shown in Fig. 5.9(a). However, the failure spots are located at the anode diffusions of the PMOS-triggered SCR devices with 0.5-μm and 0.75-μm channel lengths, as shown in Figs. 5.9(b) and 5.9(c). The shorter channel length of 0.3 μm in the embedded PMOS transistor causes the crowding ESD currents nearby the embedded PMOS transistor, and generates the huge local joule heats to destroy the embedded PMOS transistor. In addition, the shorter channel length in the embedded PMOS transistors has the lower channel resistance to conduct the huge ESD current through the surface channel of PMOS transistor to cause ESD damages. On the other hand, since the driving capability of the NMOS transistor is higher than that of the PMOS transistor, the failure spots on all NMOS-triggered SCR devices are located in the embedded NMOS transistors after 4.5-kV or 5-kV HBM ESD stresses, as shown in Fig. 5.9(d). The embedded NMOS transistors conduct huge ESD currents, and the local joule heats are produced to damage the embedded NMOS transistor from drain to source. This failure mechanism can explain that the ESD robustness of NMOS-triggered SCR devices was not

increased by increasing the channel lengths of embedded NMOS transistors.



(a)



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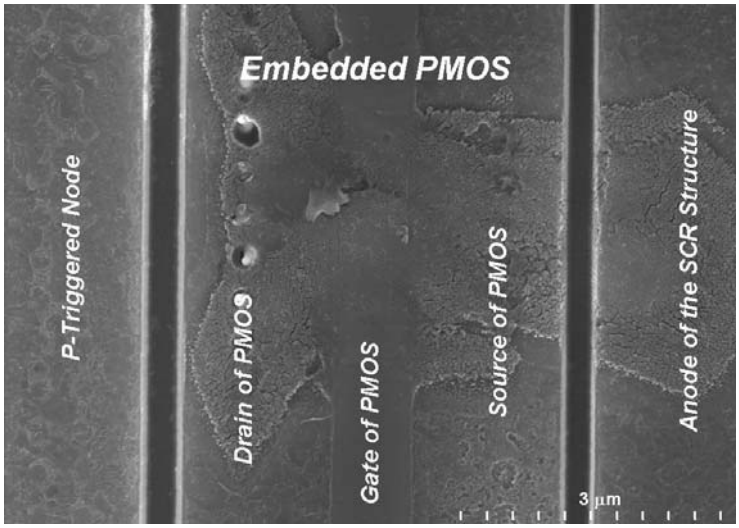

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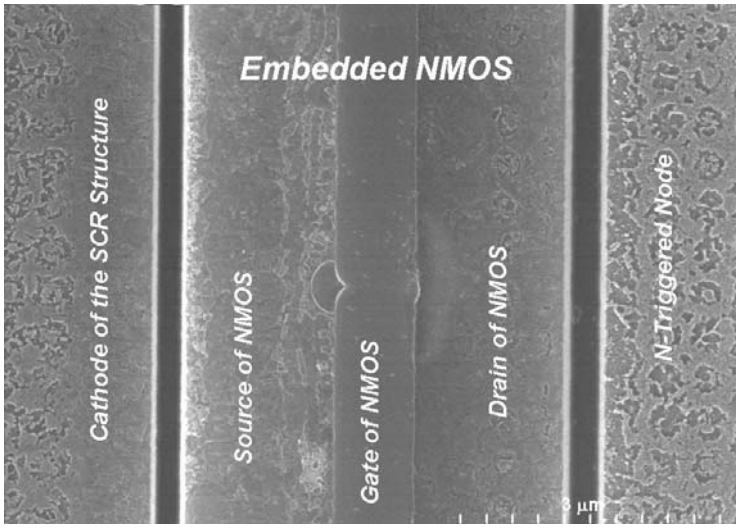


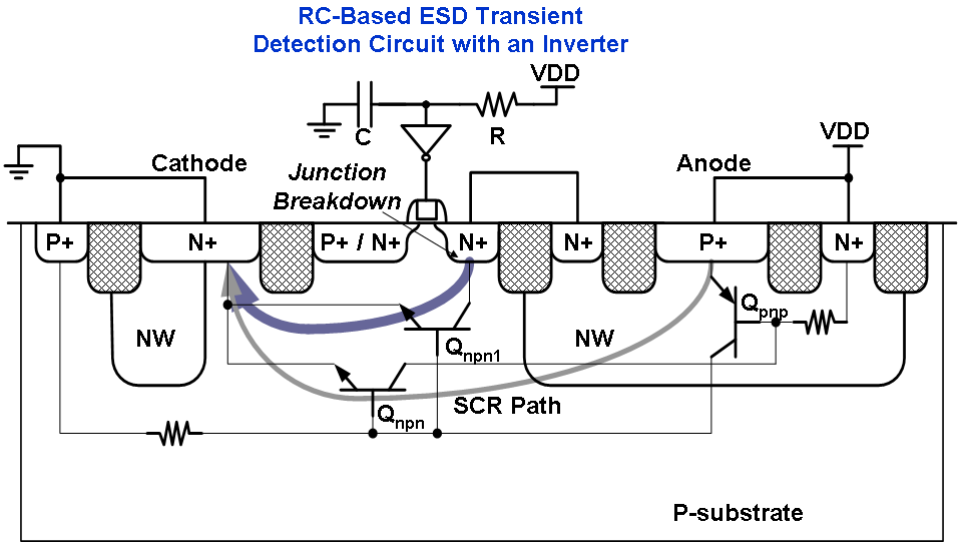
(d)

Fig. 5.9. (a) The failure spot is located at the embedded PMOS transistor in the PMOS-triggered SCR device with 0.3-μm channel length. (b) and (c) The failure spots are located at the anode to embedded PMOS transistors in the PMOS-triggered SCR devices with 0.5-μm and 0.75-μm channel lengths. (d) The failure spot is located at the embedded NMOS transistor in the NMOS-triggered SCR device with 0.75-μm channel length.

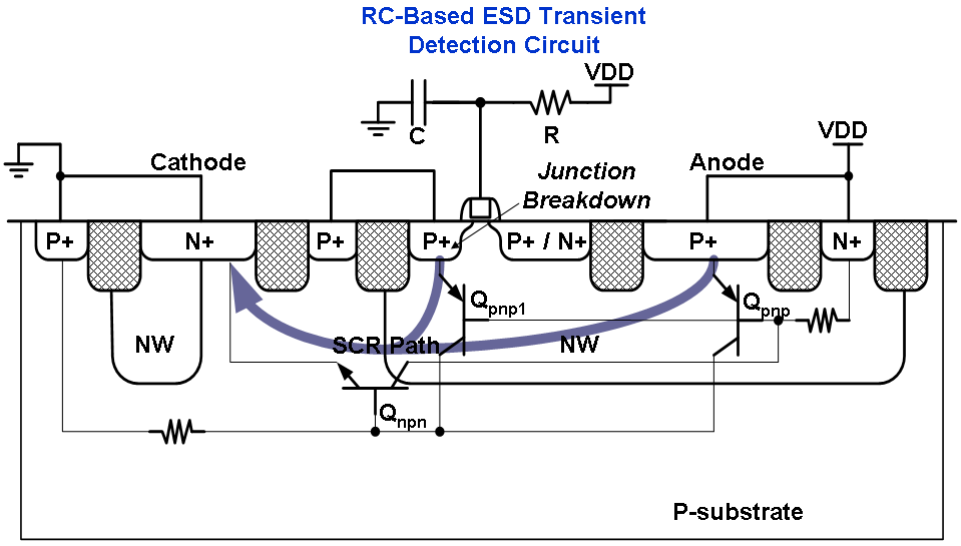
5.3.2. Discussion

According to the previous work [64], the holding voltage (Vh) of SCR device under DC measurement was much lower than that of the same SCR device under TLP measurement. However, a different measured result has been observed in the NMOS-triggered SCR devices in this work. The Vh of NMOS-triggered SCR device under DC measurement is obviously higher than that under TLP measurement. But, the Vh of the PMOS-triggered SCR device under DC measurement is slightly lower than that under TLP measurement. The major mechanism of this abnormal phenomenon can be attributed to the different parasitic structures in these two MOS-triggered SCR devices, as shown in Figs. 5.10(a) and 5.10(b). The current distributions would be affected by the parasitic structures to cause the differences in the device I-V characteristics under DC and TLP measurements. When the gate terminal of embedded NMOS transistor was biased at VSS, the drain-bulk junction breakdown of the embedded NMOS transistor in NMOS-triggered SCR device would be induced under DC measurements with overstress voltage. The parasitic npn bipolar transistor (Qnpn1), which is formed by the drain-side N+ diffusion, p-substrate, and the cathode of NMOS-triggered SCR device, will be triggered on to conduct main currents under DC measurement, as shown in Fig. 5.10(a). The Vh of the NMOS-triggered SCR devices was dominated by the parasitic npn

bipolar transistor under DC measurement. However, such parasitic npn bipolar transistor does not exist in the PMOS-triggered SCR devices. The drain-side P+ diffusion, the n-well, and the p-substrate also construct a parasitic pnp bipolar transistor (Qpnp1) in the SCR device, as shown in Fig. 5.10(b). The Vh of the PMOS-triggered SCR devices were determined by the SCR path. On the other hand, no junction breakdown occurs in the MOS-triggered SCR devices under TLP measurements. The embedded MOS transistors can be turned on by the RC-based ESD transient detection circuit to produce the trigger currents in n-well and p-substrate, therefore the SCR devices will be rapidly triggered on during TLP measurement. The Vh of MOS-triggered SCR devices are ruled by the SCR paths under TLP measurement.



(a)



(b)

Fig. 5.10. The turn-on mechanisms of (a) NMOS-triggered SCR device, and (b) PMOS-triggered SCR device, under DC measurement with the embedded MOS transistors in off state.

5.4. Summary

In this chapter, the device characteristics of SCR devices with different embedded MOS transistors have been compared and investigated. The turn-on efficiency, such as Vt1, Vh, and Ron, of the MOS-triggered SCR devices is decreased by decreasing the channel lengths in the embedded MOS transistors. But, the It2 and ESD robustness of the MOS-triggered SCR devices are increased by increasing the channel lengths, especially in the PMOS-triggered SCR devices. In addition, the merged layout style of the embedded MOS transistor can obviously improve It2 and ESD robustness of the MOS-triggered SCR devices. Moreover, the obvious differences on the Vh of NMOS-triggered SCR devices under DC and TLP measurements have been attributed to the current distributions through the parasitic npn bipolar transistor in the SCR device.

Chapter 6

ESD Failure Mechanisms of Analog I/O Cells in a 0.18-μm CMOS Technology

In this chapter, different ESD protection designs for the analog I/O pin were compared to find the optimal ESD protection circuit for the analog I/O pin in 0.18-μm 1.8-V/3.3-V CMOS technology. In addition, the failure analyses on both 1.8-V and 3.3-V analog I/O pins are presented after ND-mode and PS-mode ESD stresses. In the ESD protection designs with MOS transistors, ESD robustness is dominated by the ESD levels of GGNMOS or GDPMOS under the PS-mode or ND-mode ESD stresses. However, the failure mechanism is different from the ESD protection design with pure diodes under PS-mode or ND-mode ESD stresses. Besides, an unexpected failure mechanism has been found in the analog I/O pin with the pure-diode ESD protection circuit. The parasitic npn bipolar transistor formed by the N+ diode and the N-well guard ring structure provides the ESD current path during the ND-mode ESD stress, which causes a low ESD level to the analog I/O pin.

6.1. ESD Protection Schemes for Analog I/O Interface Circuits

6.1.1. ESD Protection Circuit

Four ESD protection designs for analog I/O pins with 1.8-V and 3.3-V devices in a 0.18-μm CMOS process are compared in this work, as listed in Table I. The GGNMOS and GDPMOS with a channel width of 50 μm are used for pad-to-VSS (N-cell) and pad-to-VDD (P-cell) ESD protection, respectively. The silicide-blocking widths on drain side are 1.5 μm (1.91 μm) in all 1.8-V (3.3-V) MOS protection devices. The source sides of all 1.8-V (3.3-V) MOS protection devices were formed with silicidation. The HBM ESD robustness of the standalone GGNMOS or GDPMOS with such small dimension (50 μm) is less than 500V in the given 0.18-μm CMOS process when the GGNMOS or GDPMOS is zapped in the PS-mode or ND-mode ESD stresses (the devices in the drain-breakdown condition). However,

the 50-μm wide GGNMOS or GDPMOS can sustain an HBM ESD level of 6000 V in the same 0.18-μm CMOS process when the GGNMOS or GDPMOS is zapped in the negative-to-VSS (NS-mode) or positive-to-VDD (PD-mode) ESD stresses (the devices operated in the drain diode forward-biased condition). To avoid GGNMOS and GDPMOS into the drain breakdown condition, an efficient power-rail ESD clamp circuit is constructed in the analog I/O ESD protection circuits. In Fig. 6.1, the RC-based ESD-transient detection circuit [6], [7] is applied to trigger on the ESD clamp device to provide a low impedance path between the VDD and VSS, while the pad is zapped in the PS-mode or ND-mode ESD stresses. Because the power-rail ESD clamp device can be turned on under PS-mode or ND-mode ESD stresses, the ESD current is discharged through the forward-biased drain diode and the turned-on power-rail ESD clamp device, as illustrated in Fig. 6.1. The power-rail ESD clamp device is usually designed with a large device dimension to provide the higher ESD robustness and lower impedance path between VDD and VSS to effectively discharge ESD current under PS-mode or ND-mode ESD stresses. Because the ESD clamp device is added between VDD and VSS, the large parasitic junction capacitance of the ESD clamp device does not contribute to the analog pin. Therefore, this ESD protection design for analog pin can sustain a high ESD robustness but only with a low parasitic input capacitance.

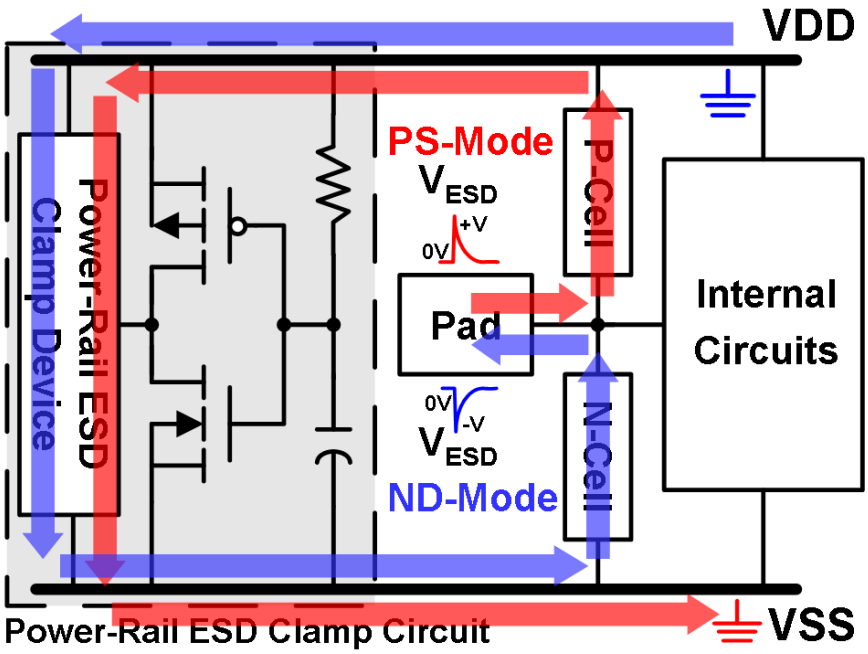


Fig. 6.1. The power-rail ESD clamp circuit can provide a low-impedance path between VDD and VSS to discharge the ESD current under the PS-mode and ND-mode ESD stresses. ESD current is discharged through the P-cell (N-cell) and power-rail ESD clamp device during PS-mode (ND-mode) ESD stress.

In high-frequency analog circuit applications, the parasitic effects of ESD protection devices often play a critical factor to influence the circuit performance. Due to the smaller parasitic effect in the pure diode structure, the ESD protection design with pure diodes for input stage is more suitable than the ESD protection design with MOS devices in high-frequency circuit applications [65], [66]. In Table 6.1, the pure-diode ESD protection design between pad and VDD (VSS) is also designed to compare with the MOS protection circuit. The pure N+ diode and the pure P+ diode are constructed by the N+/P-well junction diode and the P+/N-well junction diode, respectively. The pure-diode ESD protection designs are drawn with the same equivalent perimeters as the channel width of the MOS devices in the test chip. In Table 6.1, the "P/D" terms mean the perimeters of the diode structures and the distances between N+ (P+) diffusions and the P+ (N+) diffusions in N+ diodes (P+ diodes), respectively, in pure-diode structures.

Table 6.1

Different ESD Protection Designs for 1.8-V and 3.3-V Analog I/O Pins

Designs		N-cell & P-cell	Power-Rail ESD Clamp Device
AIO_1	1.8-V	GGNMOS: W/L= 50/0.25 μm GDPMOS: W/L= 50/0.25 μm	Gate-Driven NMOS [7] W/L= 290/0.25 μm
	3.3-V	GGNMOS: W/L= 50/0.44 μm GDPMOS: W/L= 50/0.44 μm	Gate-Driven NMOS [7] W/L= 290/0.44 μm
AIO_2	1.8-V	GGNMOS: W/L= 50/0.25 μm GDPMOS: W/L= 50/0.25 μm	STFOD [68] W/L= 180/0.28 μm
	3.3-V	GGNMOS: W/L= 50/0.44 μm GDPMOS: W/L= 50/0.44 μm	STFOD [68] W/L= 180/0.28 μm
AIO_3	1.8-V	GGNMOS: W/L= 50/0.25 μm GDPMOS: W/L= 50/0.25 μm	STNMOS with Dummy Gate [69] W/L= 180/0.28 μm
	3.3-V	GGNMOS: W/L= 50/0.44 μm GDPMOS: W/L= 50/0.44 μm	STNMOS with Dummy Gate [69] W/L= 180/0.34 μm
AIO_4	1.8-V	Pure N+ Diode: P/D= 50/0.44 μm Pure P+ Diode: P/D= 50/0.44 μm	STFOD [68] W/L= 180/0.28 μm
	3.3-V	Pure N+ Diode: P/D= 50/0.44 μm Pure P+ Diode: P/D= 50/0.44 μm	STFOD [68] W/L= 180/0.28 μm

* P/D = Perimeter of the diode / Distance between anode and cathode of the diode.

The turn-on efficiency of the ESD clamp devices with gate-driven and substrate-triggered designs had been studied in a 0.35-μm CMOS technology [67]. In this work, the gate-driven NMOS [7], substrate-triggered field oxide device (STFOD) [68], and

the substrate-triggered NMOS (STNMOS) with dummy gate [69] are used as the power-rail ESD clamp devices to verify the utility for the analog I/O pins in 0.18-μm CMOS technology, as shown in Table 6.1. The "W/L" terms in STFOD mean the perimeters (W) of the parasitic npn bipolar transistors in STFOD, and the distances (L) between the collector and the emitter of the parasitic npn bipolar transistors in STFOD. The STNMOS with dummy gate is a new proposed power-rail ESD clamp device, which has been drawn in the test chip and compared with gate-driven NMOS and STFOD. The device structures of gate-driven NMOS, STFOD, and STNMOS with dummy gate are shown in Figs. 6.2(a), 6.2(b), and 6.2(c), respectively.

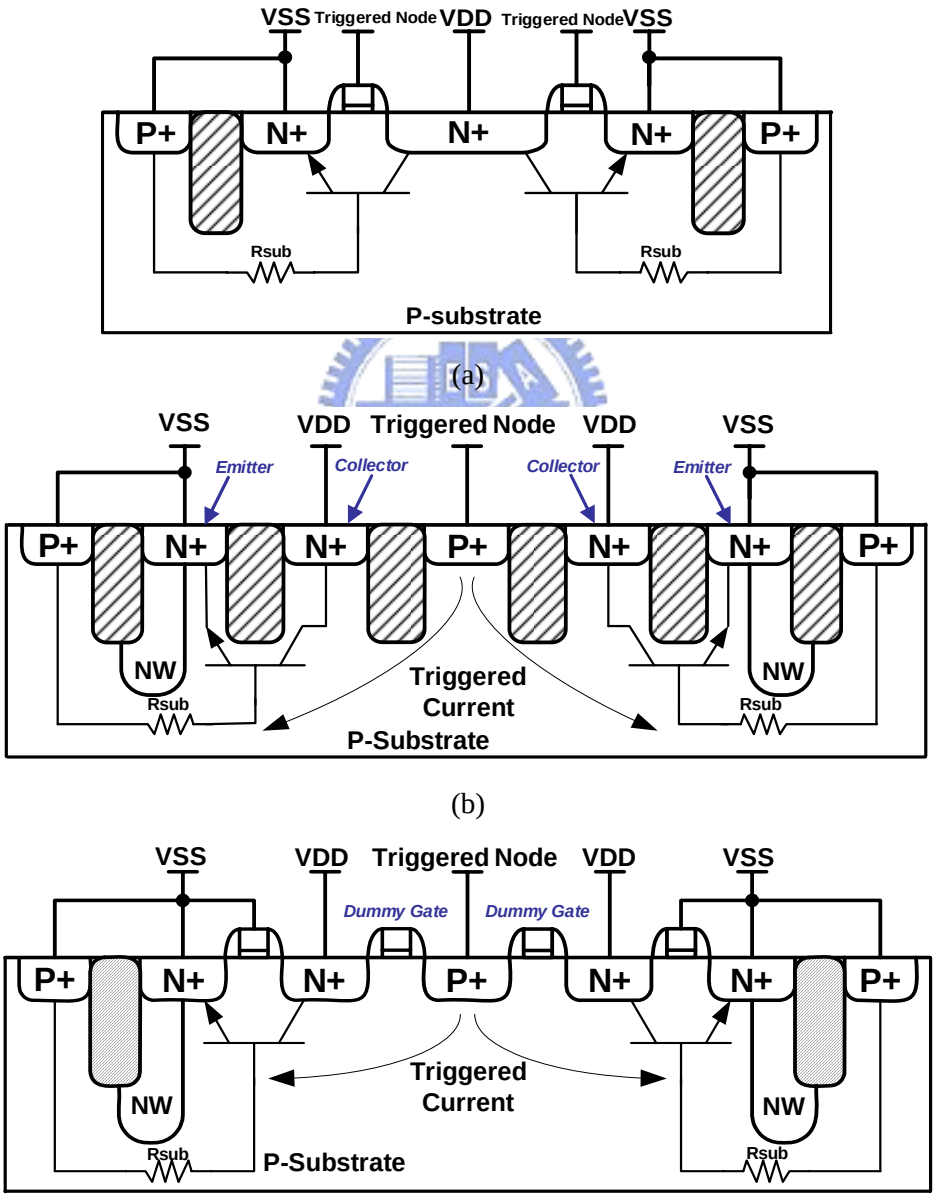


Fig. 6.2. The cross-section views of (a) gate-driven NMOS, (b) substrate-triggered FOD (STFOD), and (c) substrate-triggered NMOS (STNMOS) with dummy gate.

In Fig. 6.2(c), the dummy gate is used to reduce the distance between the triggered note and the base of parasitic npn bipolar transistor in NMOS structure. It can improve the turn-on efficiency of STNMOS by enhancing the triggered current to achieve the base region of the npn bipolar transistor, as illustrated in Fig. 6.2(c). The silicide-blocking widths on collector side are 1.5 μm (1.5 μm) in 1.8-V (3.3-V) STFOD and STNMOS. Each analog I/O cell has been drawn in the same silicon area of an I/O cell with power-rail ESD clamp device and ESD-transient detection circuit. Therefore, all analog I/O cells have the same cell height of 89 μm (excluding the bonding pad) and cell pitch of 65 μm. In addition, each analog I/O pin was connected to the input stage of an inverter in the silicon chip to evaluate the core-circuit protection efficiency in each ESD test condition. Due to the transient gate oxide breakdown voltages as a function of the physical gate oxide thickness, the Transmission Line Pulse (TLP) measurement results of transient gate oxide breakdown voltages are 10-12 volts and 16-18 volts in 1.8-V and 3.3-V processes, respectively.

6.1.2. Turn-On Efficiency of Power-Rail ESD Clamp Circuit

Due to the difference in the rise time between the ESD voltage and the VDD power-on voltage, the power-rail ESD clamp circuit provides a low-impedance path between VDD and VSS power lines during the ESD-stress condition, but it becomes an open circuit between the power lines in VDD power-on condition. To meet these requirements, the RC time constant of the ESD-transient detection circuit is designed about 0.1~1 micro-second to achieve the desired operations. To verify the aforementioned ESD-transient detection function, an experimental setup is shown in Fig. 6.3(a) [7]. A voltage pulse with a rise time about 5 nano-seconds to simulate the HBM ESD pulse is generated from a pulse generator (HP8110A) and applied to VDD power line with the VSS grounded. The sharp-rising edge of the ESD-like voltage pulse will trigger on the ESD clamp device to degrade the voltage waveform on VDD power line. The measured voltage waveforms, which are clamped by the gate-driven NMOS, the substrate-triggered FOD, and the substrate-triggered NMOS with dummy gate, under ESD-like voltage stress of the 3.3-V (1.8-V) analog I/O pins on the VDD power line are shown in Figs. 6.3(b), 6.3(c), and 6.3(d) (Figs. 6.4(a), 6.4(b), and 6.4(c)), respectively. The maximum voltage degradations of the gate-driven NMOS, the substrate-triggered FOD, and the substrate-triggered NMOS with dummy gate are 2 V, 0.8 V, and 1 V, respectively, in the 1.8-V analog I/O pins. Then, they are 3.5 V, 1.5 V, and 2 V in the gate-driven NMOS, the substrate-triggered FOD, and the substrate-triggered NMOS with

dummy gate, respectively, in the 3.3-V analog I/O pins.

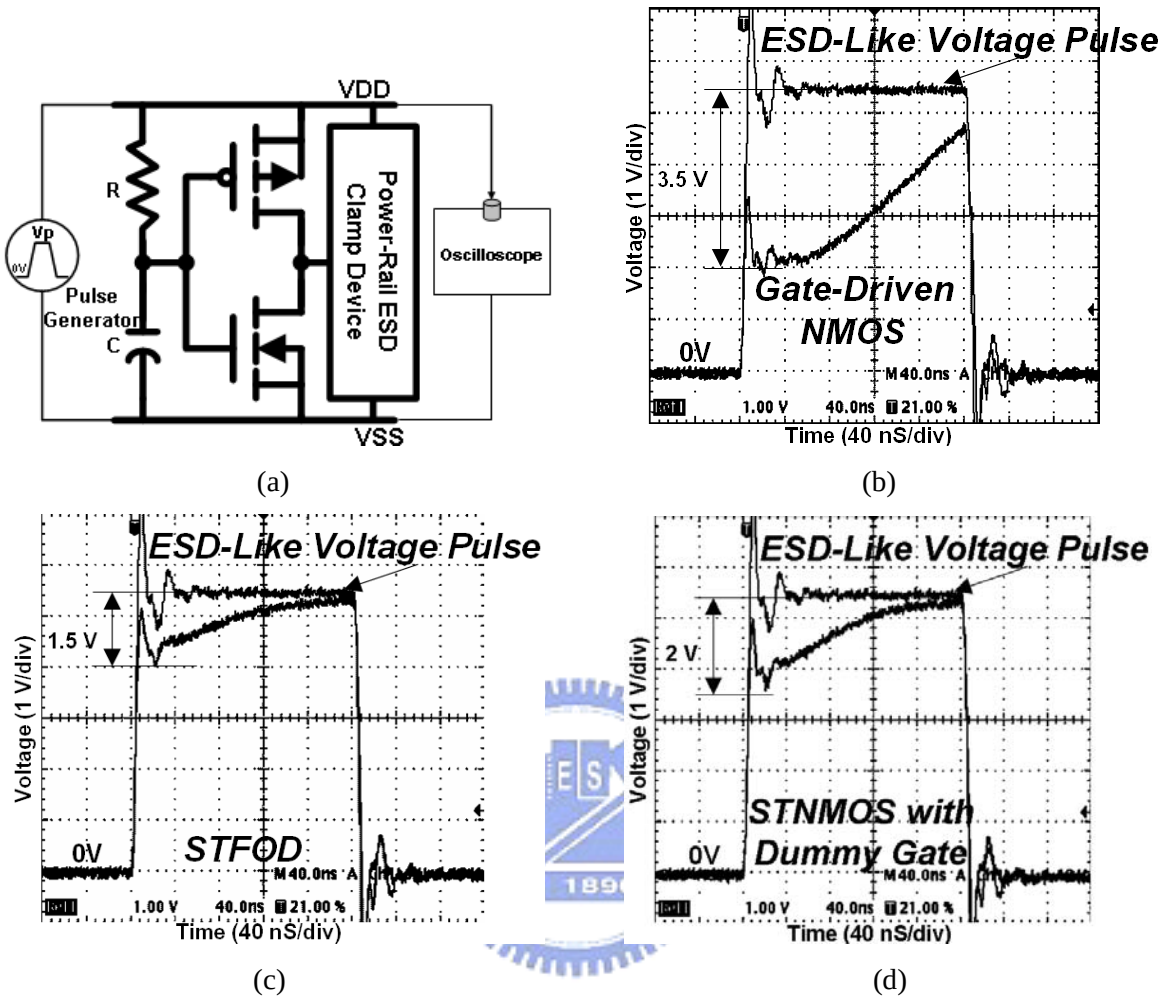


Fig. 6.3. (a) The experimental setup to measure the turn-on efficiency of the power-rail ESD clamp circuits. The measured voltage waveforms of the 3.3-V analog I/O pins on VDD node, which are clamped by (b) gate-driven NMOS, (c) substrate-triggered FOD, and (d) substrate-triggered NMOS with dummy gate, under ESD-like stress condition.

According to the measured results, the gate-driven NMOS has signification voltage degradation to effectively clamp ESD-like voltage pulse in both 3.3-V and 1.8-V analog I/O pins in the given 0.18-μm CMOS process. Therefore, the gate-driven NMOS could be a more suitable as power-rail ESD clamp design for 1.8-V and 3.3-V analog I/O pins in the sub-quarter-micron CMOS technology which has STI (shallow trench isolation) structure. On the other hand, the difference of the maximum voltage drops in the substrate-triggered FOD and the substrate-triggered NMOS with dummy gate is caused by the difference of the base width of the parasitic lateral npn bipolar transistors in the ESD clamp device. The current gain (β) of the STNMOS with dummy gate can be increased by reducing the distance from

the two separated N+ regions. The ESD robustness of the power-rail ESD clamp circuits with the gate-driven NMOS, the substrate-triggered FOD, and the substrate-triggered NMOS with dummy gate are 5.5 kV, 3.0 kV, and 3.0 kV, respectively, in 1.8-V process (which are 2.5 kV, 1.5 kV, and 2.0 kV, respectively, in 3.3-V process). The transient characteristics of the power-rail ESD clamp circuits, such as trigger voltage and turn-on resistance, are also shown in Table 6.2. According to the whole measured results, the power-rail ESD clamp circuits with the gate-driven NMOS have the lowest turn-on resistance and fastest turn-on speed; therefore it can provide the best turn-on efficiency and ESD robustness in the sub-quarter-micron CMOS technology which has STI (shallow trench isolation) structure.

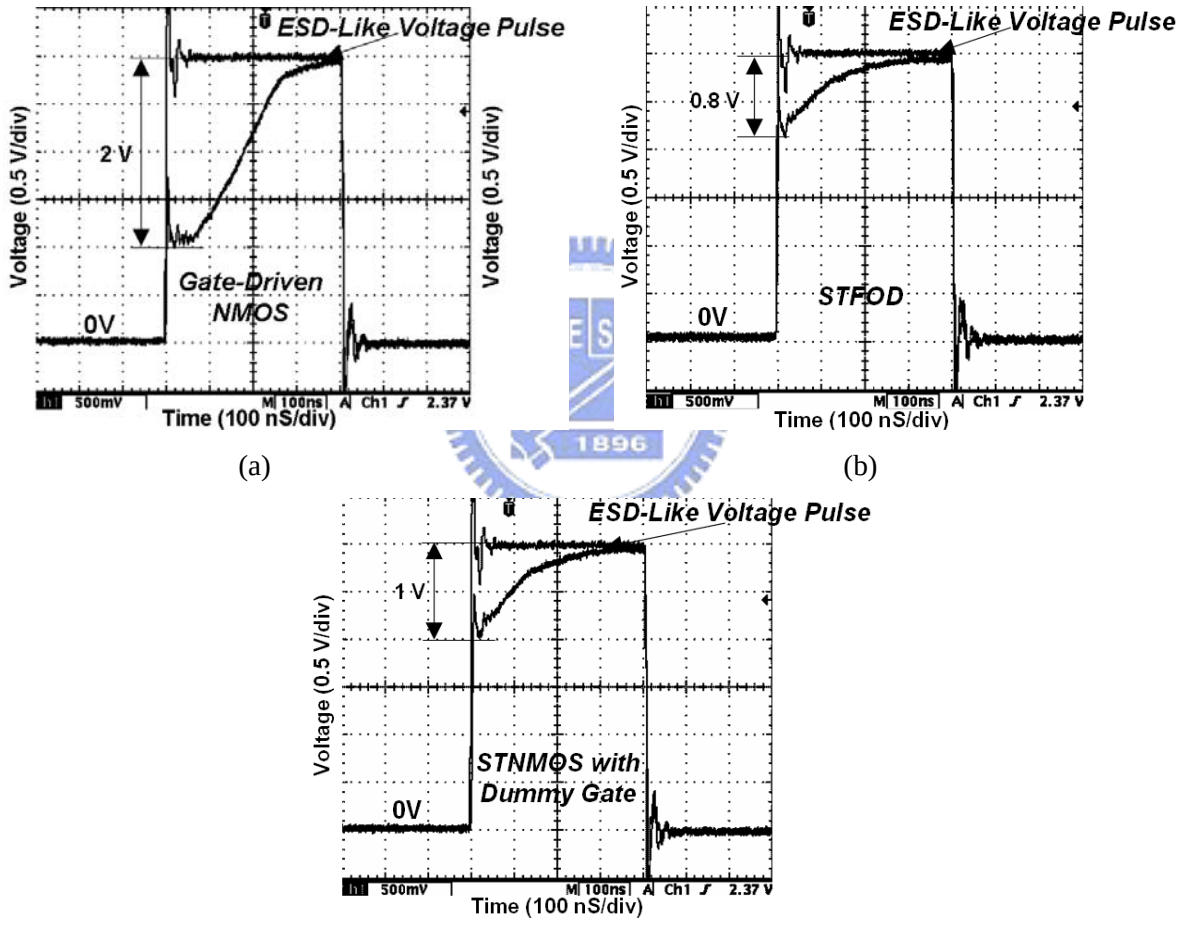


Fig. 6.4. The measured voltage waveforms of the 1.8-V analog I/O pins on VDD node, which are clamped by (a) gate-driven NMOS, (b) substrate-triggered FOD, and (c) substrate-triggered NMOS with dummy gate, under ESD-like stress condition.

6.2. Experimental Results and Discussion

The device characteristics, such as junction breakdown voltages (reverse-biased

condition) and turn-on resistances (forward-biased condition) of the GGNOMS and GDPMOS in 1.8-V and 3.3-V devices, are shown in Table 6.2. In 1.8-V and 3.3-V devices, the junction breakdown voltages of pure-diode structures are higher than those of the MOS transistors. The turn-on resistances of the pure-diode structures and MOS transistors in N-cells and P-cells were measured during the ESD currents discharged by the forward-biased pure-diode structures or forward-biased drain diodes. However, the slightly lower turn-on resistances of the pure-diode structures can be attributed to the fully silicided process in N+ (P+) diffusions and the P+ (N+) diffusions in the pure N+ diodes (P+ diodes).

Table 6.2

The Transient Characteristics of Different ESD Protection Devices

N-cell and P-cell		MOS Transistors		Diode Devices	
		GGNMOS	GDPMOS	N+ Diode	P+ Diode
Junction Breakdown (Reverse-Biased Condition)	1.8-V	5~6 V	6 V	11 V	10 V
	3.3-V	7.5 V	7.5 V	16 V	16 V
Turn-On Resistance (Forward-Biased Condition)	1.8-V	~ 2.67 Ω		~ 2.24 Ω	
	3.3-V	~ 2.7 Ω		~ 2.19 Ω	
Power-Rail ESD Clamp Circuits		Gate-Driven NMOS	STFOD	STNMOS	
Trigger Voltage	1.8-V	5 V	6 V	4 V	
	3.3-V	7.5 V	7.3 V	5 V	
Holding Voltage	1.8-V	5 V	6 V	4 V	
	3.3-V	6 V	7.3 V	5 V	
VDD-to-VSS Turn-On Resistance	1.8-V	~ 1.78 Ω	~ 1.85 Ω	~ 2.52 Ω	
	3.3-V	~ 1.65 Ω	~ 2.47 Ω	~ 2.25 Ω	

6.2.1. HBM ESD Robustness

The HBM ESD robustness of the 1.8-V and 3.3-V analog I/O pins are shown in Table 6.3 and Table 6.4, respectively. In 1.8-V analog I/O pins, the ESD levels of the AIO_1, AIO_2, AIO_3, and AIO_4 are 0.5 kV, smaller than 0.5 kV, 0.5 kV, and 3.0 kV, respectively, in PS-mode ESD stress. Then, the PS-mode ESD levels of the AIO_1, AIO_2, AIO_3, and AIO_4 in 3.3-V analog I/O pins are 1.5 kV, smaller than 0.5 kV, 1.5 kV, and 2.0 kV, respectively. The analog I/O pins with the pure-diode protection have the higher ESD level

among all ESD test modes. In 1.8-V I/O designs, the ESD levels of the analog I/O pins with the MOS devices are much weaker than that with the diode devices during a PS-mode ESD stress. On the other hand, the ND-mode ESD levels don't achieve the general specification (2 kV) in AIO_2 of 1.8-V analog I/O pins, and AIO_2 and AIO_4 of 3.3-V analog I/O pins. The ESD robustness of the 1.8-V and 3.3-V I/O analog pins with MOS protection circuits are dominated by PS-mode ESD levels, but the analog pins with pure-diode protection circuits are dominated by ND-mode ESD levels. The difference in ESD robustness among analog I/O pins was inspected by failure analysis after PS-mode and ND-mode ESD stresses.

Table 6.3

The HBM ESD Robustness of 1.8-V Analog I/O Pins

Designs	PS-mode	NS-mode	PD-mode	ND-mode
AIO_1	0.5 kV	-3.5 kV	7.5 kV	-2.5 kV
AIO_2	< 0.5 kV	-3.5 kV	7.5 kV	-1.0 kV
AIO_3	0.5 kV	-3.5 kV	7.5 kV	-2.5 kV
AIO_4	3.0 kV	-5.5 kV	6.0 kV	-2.0 kV

Table 6.4

The HBM ESD Robustness of 3.3-V Analog I/O Pins

Designs	PS-mode	NS-mode	PD-mode	ND-mode
AIO_1	1.5 kV	-3.5 kV	7.5 kV	-2.0 kV
AIO_2	< 0.5 kV	-3.5 kV	7.5 kV	-0.5 kV
AIO_3	1.5 kV	-3.5 kV	7.5 kV	-2.0 kV
AIO_4	2.0 kV	-5.5 kV	6.5 kV	-1.5 kV

6.2.2. Failure Analysis

The I-V curves of 3.3-V and 1.8-V analog I/O pins were measured to identify which device or junction was damaged after PS-mode and ND-mode ESD stresses. The results are

listed in Table 6.5 and 6.6, respectively. The analog pins with GGNMOS and GDPMOS shorted to ground after PS-mode ESD stress. The 1.8-V and 3.3-V GGNMOS devices of the AIO_1, AIO_2, and AIO_3 were damaged to cause the short circuit between the analog pin and VSS.

Table 6.5

The Failures on the 1.8-V and 3.3-V Analog I/O Pins after PS-Mode ESD Stress

1.8-V Designs	Shorting Path	3.3-V Designs	Shorting Path
AIO_1	Pad-to-VSS	AIO_1	Pad-to-VSS
AIO_2	Pad-to-VSS	AIO_2	Pad-to-VSS
AIO_3	Pad-to-VSS	AIO_3	Pad-to-VSS
AIO_4	VDD-to-VSS	AIO_4	VDD-to-VSS

Table 6.6

The Failures on the 1.8-V and 3.3-V Analog I/O Pins after ND-Mode ESD Stress

1.8-V Designs	Shorting Path	3.3-V Designs	Shorting Path
AIO_1	Pad-to-VDD	AIO_1	Pad-to-VDD
AIO_2	Pad-to-VDD	AIO_2	Pad-to-VDD
AIO_3	Pad-to-VDD	AIO_3	Pad-to-VDD
AIO_4	VDD-to-VSS	AIO_4	VDD-to-VSS

The failure spot of 1.8-V analog I/O pins is shown in Figs. 6.5(a) and 6.5(b) after PS-mode ESD stress. After 0.5-kV or 1-kV ESD stresses, the AIO_1, AIO_2, and AIO_3 show local damage in GGNMOS. The ESD damage is located under poly gate oxide to cause the short circuit between analog pin to VSS, as shown in Fig. 7. On the other hand, the failure spots of the 3.3-V analog I/O pins are shown in Figs. 6.6(a) and 6.6(b) after PS-mode ESD stresses. In Fig. 6.6(a), the huge ESD current discharged through the parasitic npn bipolar transistor of the GGNMOS of AIO_3 to violently destroy the silicon substrate after 2-kV PS-mode ESD stress. The GGNMOS of AIO_2 shows only slight damage after 0.5-kV

PS-mode ESD stress, as shown in Fig. 6.6(b).

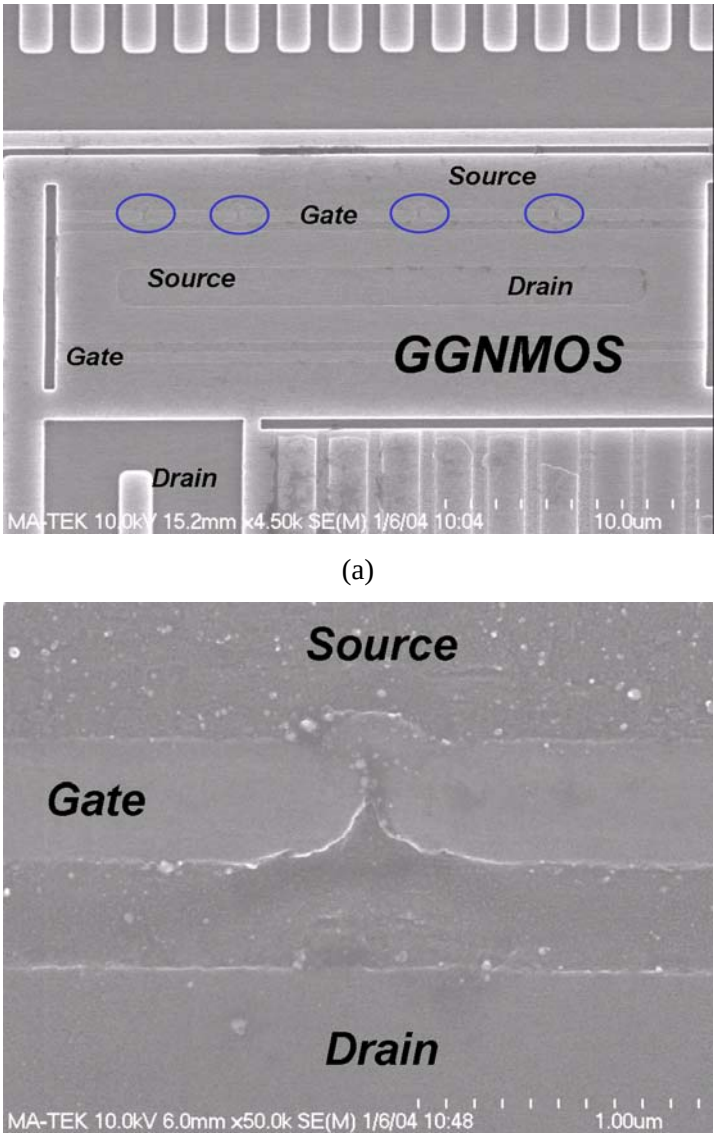
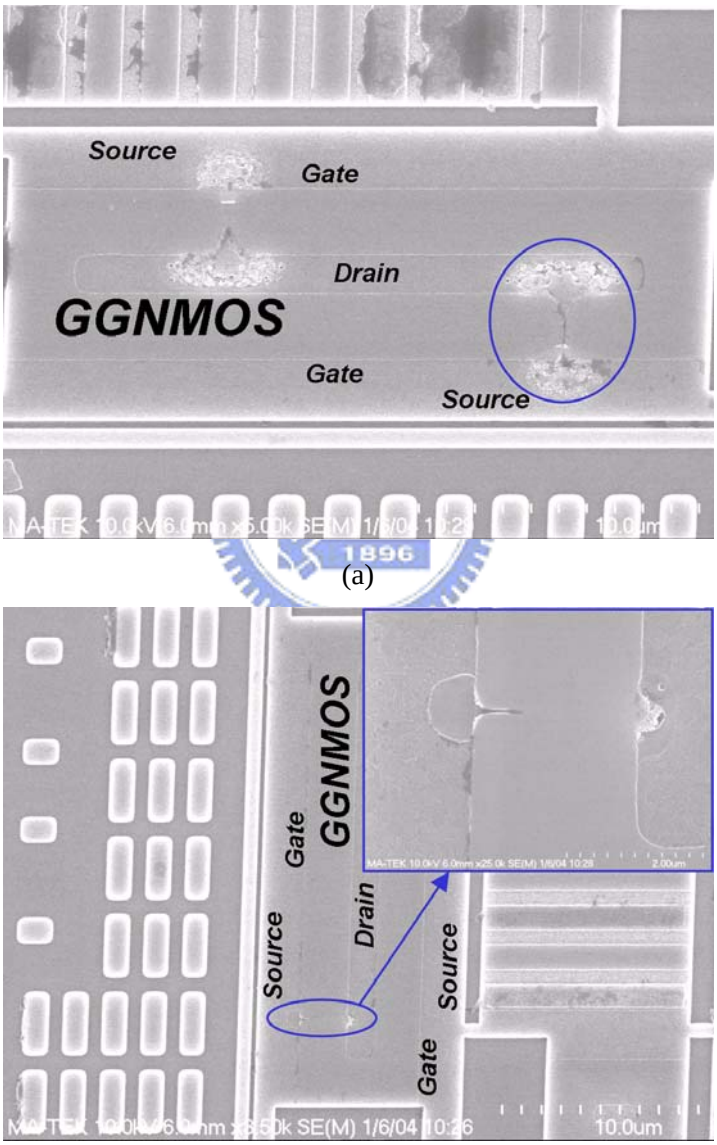


Fig. 6.5. (a) The failure spot is located at the GGNMOS in 1.8-V analog I/O pins with the MOS ESD protection design of AIO_2 after 0.5-kV PS-mode ESD stress. (b) The zoomed-in view of the failure spot.

Due to the difference in the turned-on efficiency of power-rail ESD clamp circuit of the AIO_1, AIO_2, and AIO_3, the distributions of the ESD current are also different in AIO_1, AIO_2, and AIO_3 of the 3.3-V analog I/O pins. In AIO_1 and AIO_3, the ESD current majority discharged through the drain-diode of the P-cell and the turned-on power-rail ESD clamp circuit to grounded VSS under PS-mode ESD stress. The parasitic npn bipolar transistor of the small GGNMOS would be turned on by the increasing voltage drop between

analog pin and VSS, and be destroyed to cause serious damages under higher ESD stresses. But, the small GGNMOS of AIO_2 was unexpectedly turned on to discharge the ESD current and cause slight damage under lower ESD level, because the ineffective power-rail ESD clamp circuit didn't provide the low-impedance discharging path. In addition, due to the lower drain-breakdown voltage and thinner gate oxide in the 1.8-V analog pins, the GGNMOS would be damage to cause regional failure spot under about 0.5-kV to 1-kV PS-mode ESD stress, as presented in Figs. 6.5(a) and 6.5(b).

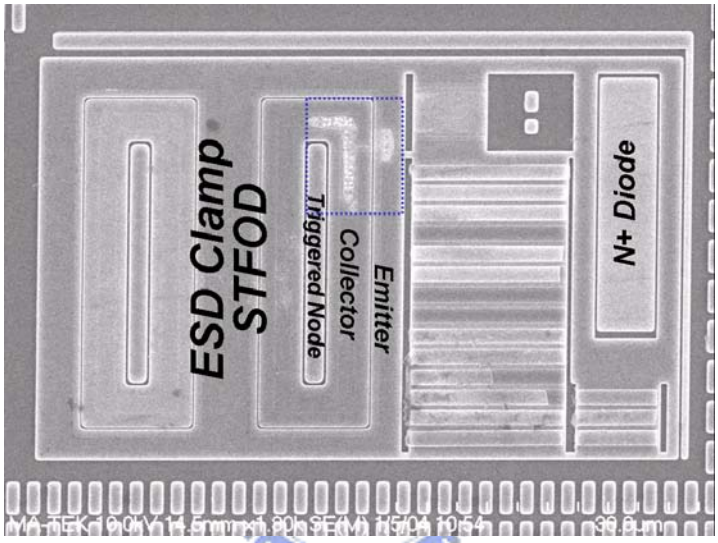


(a)

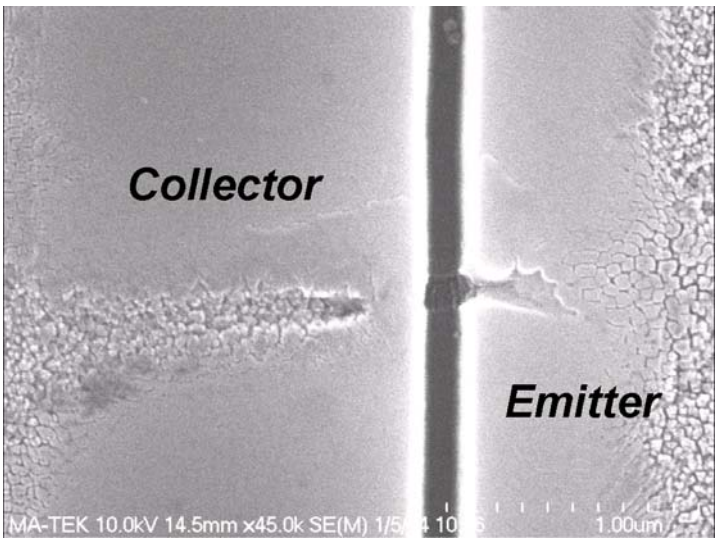
(b)

Fig. 6.6. (a) The failure spot is located at the GGNMOS in 3.3-V analog I/O pin with the MOS ESD protection design of AIO_3 after 2.0-kV PS-mode ESD stress. (b) The failure spot is located at the GGNMOS in 3.3-V analog I/O pin with the MOS ESD protection design of AIO_2 after 0.5-kV PS-mode ESD stress.

However, the measured results of the analog pins with pure diodes to implement N-cell and P-cell are obviously different. The I-V curves show that the VDD shorting to ground after PS-mode ESD stress. The power-rail ESD clamp devices are damaged to cause the short circuit between VDD and VSS in the 1.8-V and 3.3-V analog I/O pins, as shown in Figs. 6.7(a), 6.7(b), 6.8(a), and 6.8(b). In these SEM photographs, the failure spots are located at the parasitic npn transistors of the STFODs. The clearly destroyed path is occurred between the collector to the emitter of the parasitic npn bipolar transistor in the STFOD, as shown in Figs. 6.7(b) and 6.8(b).

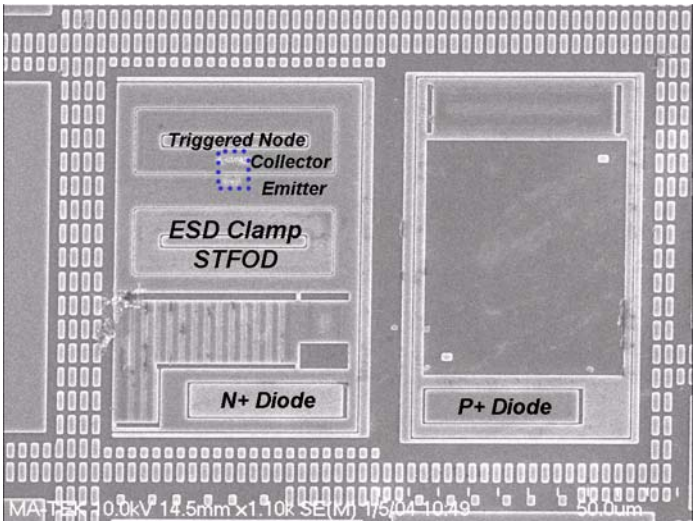


(a)

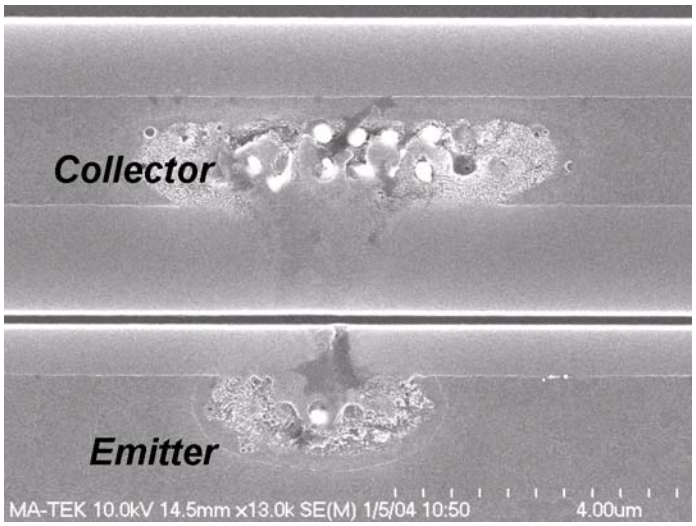


(b)

Fig. 6.7. (a) The failure spot is located at the ESD clamp FOD in 1.8-V analog I/O pins with the pure-diode ESD protection design of AIO_4 after 3.5-kV PS-mode ESD stress. (b) The zoomed-in view of the failure spot.



(a)

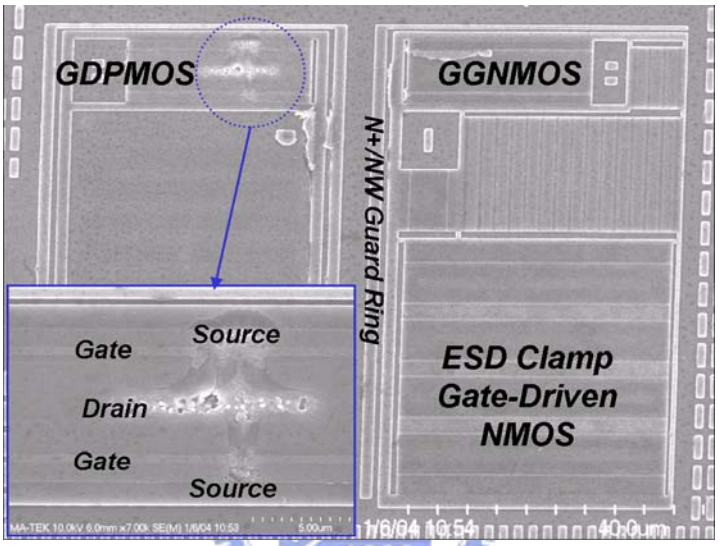


(b)

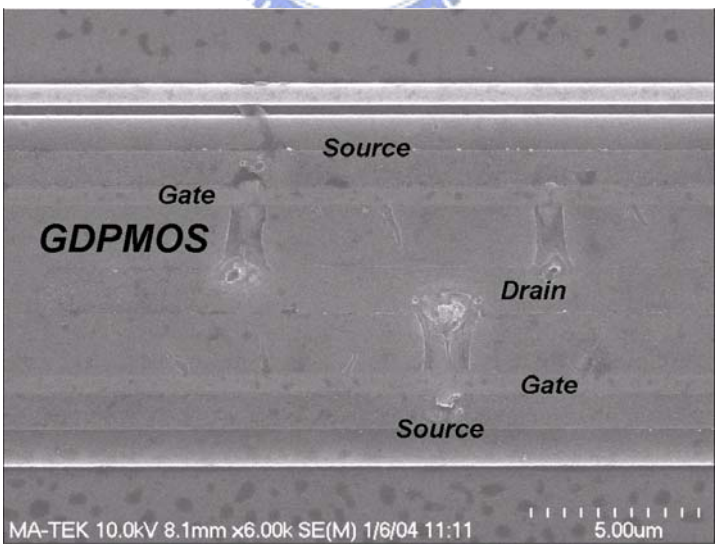
Fig. 6.8. (a) The failure spot is located at the ESD clamp FOD in 3.3-V analog I/O pins with the pure-diode ESD protection design of AIO_4 after 2.5-kV PS-mode ESD stress. (b) The zoomed-in view of the failure spot.

The power-rail ESD clamp device will dominate the ESD levels of these analog I/O pins with the pure-diode under PS-mode ESD stress. The failures on the analog I/O pins after PS-mode ESD stress are summarized in Table 6.5. On the other hand, the failures on the analog I/O pins after ND-mode ESD stress are listed in Table 6.6. After the ND-mode ESD stress, the GDPMOS is damaged in those analog pins of AIO_1, AIO_2, or AIO_3 in 1.8-V and 3.3-V applications, as illustrated in Figs. 6.9(a) and 6.9(b). The parasitic pnp bipolar transistor of the GDPMOS was also turned on by the increased voltage drop between VDD and analog pin to seriously destroy under higher ND-mode ESD stress in AIO_1 and AIO_3 of the 1.8-V and 3.3-V analog I/O pins. Both the AIO_2 with a lower ESD level should be

also attributed to the ineffective power-rail ESD clamp circuit. According to the turn-on verification on the power-rail ESD clamp circuit, the STFOD could not rapidly discharge the ESD current to result in the GDPMOS conducting the huge current through the drain breakdown condition under lower ESD stresses, as shown in Fig. 6.9(b). The ESD levels of the analog I/O pins with the MOS ESD protection design are dominated by the ESD robustness of the GGNMOS and GDPOMS under PS-mode and ND-mode ESD stresses, respectively.



(a)

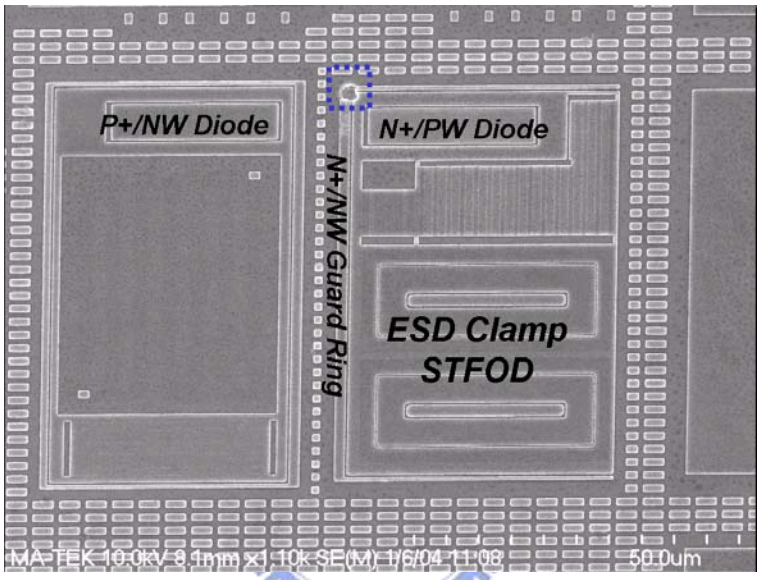


(b)

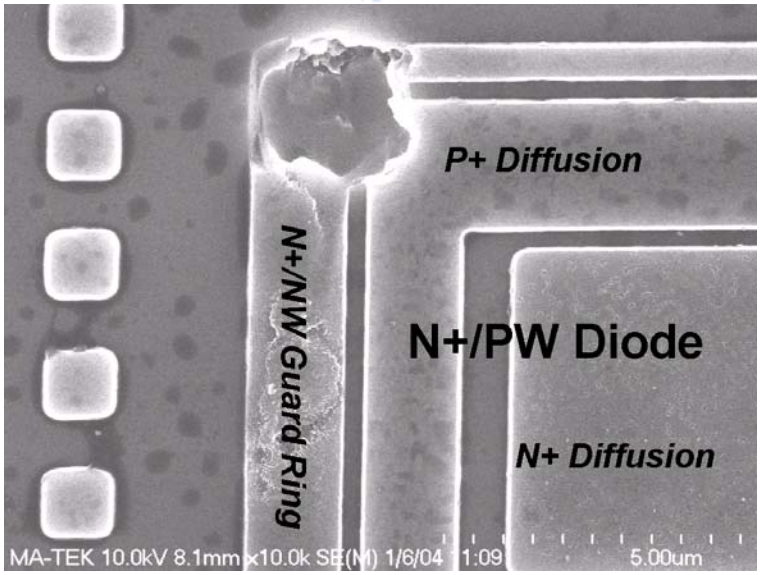
Fig. 6.9. (a) The failure spot is located at the GDPMOS in 1.8-V analog I/O pin with the MOS ESD protection design of AIO_1 after 3.0-kV ND-mode ESD stress. (b) The failure spot is located at the GDPMOS in 1.8-V analog I/O pin with the MOS ESD protection design of AIO_2 after 1.5-kV ND-mode ESD stress.

6.2.3. Unexpected Failure Spot in ND-mode ESD Stress

In Table 6.3 and Table 6.4, the lowest ESD robustness in the both AIO_4 designs is dominated by the ND-mode ESD stress. To identify the failure location for further improving its ESD level, the sample of AIO_4 after ND-mode ESD failure was de-layered. The unexpected ESD failure was located at the guard ring structure of the analog I/O pin with the pure-diode ESD protection design after ND-mode ESD stress, as shown in Figs. 6.10(a) and 6.10(b).



(a)



(b)

Fig. 6.10. (a) After 2.5-kV ND-mode ESD stress, the failure spot is located at the guard ring in AIO_4 of 1.8-V process. (b) The zoomed-in view of the failure spot at guard ring corner.

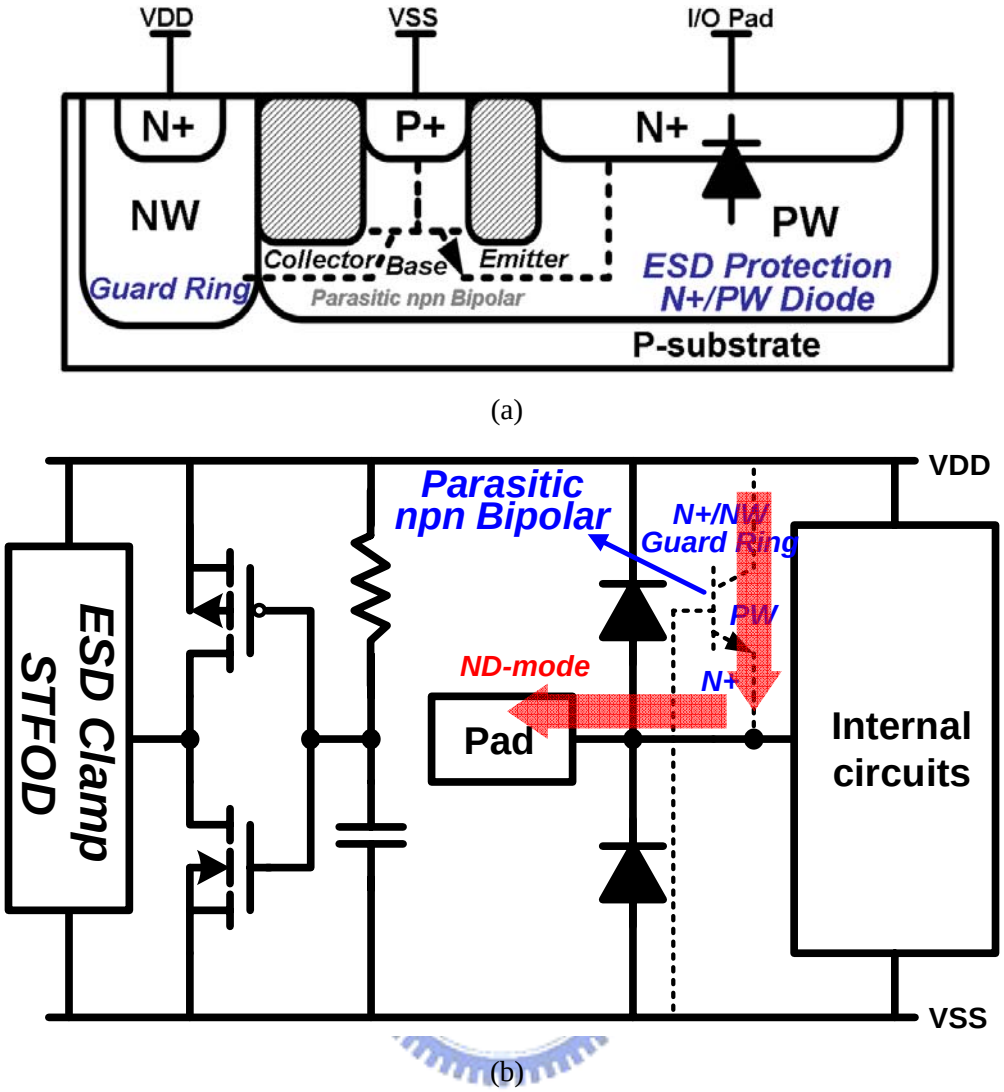


Fig. 6.11. (a) The parasitic npn bipolar transistor was constructed between the N+/PW diode and N+/NW guard ring. (b) The ESD current discharged through the parasitic npn bipolar transistor to grounded VDD during the ND-mode ESD stress causes the unexpected ESD failure.

Interaction between the N+/PW diode and the N+/NW guard ring was determined to be the cause of the failure under ND-mode ESD stress, in Fig. 6.10(b). In order to overcome latchup issues, the ESD protection devices are often surrounded by the guard rings, which are commonly connected to VDD or VSS. These guard rings could interact with the ESD protection devices to degrade the ESD robustness of the protection circuits [70]. As shown Fig. 3, the ND-mode ESD current should be discharged through the forward-biased diode between the I/O pad to VSS and the power-rail ESD clamp device to the grounded VDD. However, the parasitic npn bipolar transistor which was formed between the N+/PW diode and the N+/NW guard ring was triggered on to form a direct discharging path between the I/O pad and the grounded VDD during the ND-mode ESD stress, as the dashed lines

illustrated in Fig. 6.11(a). In Fig. 6.11(b), it explains that the ND-mode ESD current is discharged through this parasitic bipolar transistor to cause damage at the corner of the guard ring due to the localized heat. In addition, the current gain (β) and the avalanche multiplication factor of the parasitic bipolar transistor are important parameters contributing to this failure mechanism. To overcome this failure, the spacing between N+/NW guard ring to N+/PW diode should be increased to eliminate the parasitic npn BJT effect. On the other hand, replacing the power-rail ESD clamp circuit with higher turn-on efficiency can avoid the turn-on of parasitic npn BJT to degrade the ESD robustness under ND-mode ESD stress. In addition, the power-rail ESD clamp circuit with high turn-on efficiency also can improve the ESD robustness of PS-mode ESD stress by providing the efficient and low-impedance discharging path between VDD and VSS. A successful modification with optimal power-rail ESD clamp circuit has been practically verified in a 0.13-μm CMOS process to achieve HBM ESD level of 7.0 kV for analog I/O cell.

6.3. Summary

Different ESD protection schemes for the analog input/output cells have been investigated to find the optimal analog ESD protection design for deep-submicron CMOS technology. According to the experimental results, the GGNMOS was not a suitable ESD protection device for analog I/O cells in deep-submicron CMOS process, such as 0.18-μm and below. The pure-diode ESD protection device between the pad to VDD (VSS) would be an optimal design for the analog I/O pins. In addition, the gate-driven NMOS for power-rail ESD clamp circuit also performs a higher ESD robustness for analog I/O pins in deep-submicron CMOS technology with STI structure. Finally, layout optimization with a wider spacing between N+/PW diode and N+/NW guard ring, as well as improvement on the power-rail ESD clamp circuit with higher turn-on efficiency, should be used to avoid the unexpected ESD failure under ND-mode ESD stress in such analog I/O cells.

Chapter 7

Active ESD Protection Design for Interface Circuits between Separated Power Domains against Cross-Power-Domain ESD Stresses

In this chapter, a failure study of the internal ESD damage on the interface circuits of a 0.35-μm 3.3 V/5 V mixed-mode CMOS IC product with two separated power domains is presented [48]. The ESD failure spots were specially observed at the interface circuits of the separated power domains after negative-to-VDD mode (ND-mode) machine-model (MM) ESD stress [2] of 100 V. However, this IC product has a 2-kV human-body-model (HBM) ESD robustness [1] in each ESD test combination of I/O pin to power/ground pins. Therefore, the efficient ESD protection designs should be applied on the interface circuits between the separated power domains against such cross-power-domain ESD stresses. Secondly, several active cross-power-domain ESD protection designs were reviewed to compare their ESD protection strategies for interface circuits between separated power domains. Besides, one new active ESD protection design for the interface circuits between separated power domains has been also proposed to solve the interface circuit damages under cross-power-domain ESD stresses. This ESD protection design has been implemented by PMOS and NMOS transistors with the ESD-transient detection function in a 0.13-μm 1.2-V CMOS technology.

7.1. Failure Study under Cross-Power-Domain ESD Stresses

7.1.1. ESD Protection Cell Designs for the Commercial IC Product with Separated Power Pins

The ESD protection scheme for input, output, and power-rail ESD clamp circuits in this IC product is shown in Fig. 7.1. The internal circuit 1 is a digital circuit block, and the internal circuit 2 is an analog circuit block. Each circuit block has an individual power-rail ESD clamp circuit. The gate-grounded NMOS (GGNMOS) and gate-VDD PMOS

(GDPMOS) with a channel length/width of 0.8 μm/300 μm are used for pad-to-VSS and pad-to-VDD ESD protection at each I/O pad, respectively.

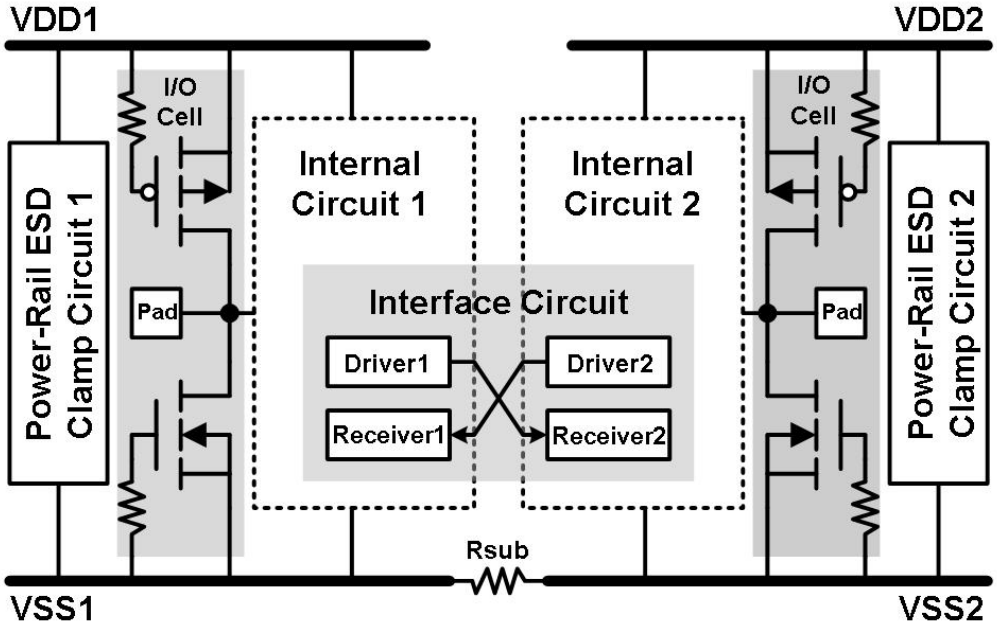


Fig. 7.1. ESD protection scheme in an IC product with separated power domains. The ESD protection circuits included input, output, and power-rail ESD clamp circuits.

The power-rail ESD clamp circuit, which is implemented with the substrate-triggered field-oxide-device (STFOD) [68], [71] with RC-based ESD transient detection circuit [6], [7] is individually installed in each power domain, as illustrated in Fig. 7.1. The perimeter of the STFOD is equivalent to 216 μm. The STFOD as a power-rail ESD clamp circuit of a VDD (or VSS) cell had been successfully verified with over 4-kV HBM and 400-V MM ESD robustness in this 0.35-μm 3.3 V/5 V CMOS process. In addition, each I/O cell with GGNMOS and GDPMOS of 300-μm channel width also had been verified to achieve over 4-kV HBM and 400-V MM ESD robustness in the same process. Due to noise consideration between power domains, the VDD1 was separated from the VDD2. Then, the VSS1 and VSS2 only connected by the parasitic p-substrate resistance (Rsub) without bi-directional diode connection in this chip.

7.1.2. Internal ESD Damages on the Interface Circuits between Separated Power Domains

After HBM ESD tests of all I/O pins to each power/ground pin and power-to-ground

ESD test, the HBM ESD robustness achieved 2 kV, which is the basic specification for commercial IC products. However, the MM ESD robustness can not achieve 200 V in positive-to-VSS mode (PS-mode), positive-to-VDD mode (PD-mode), negative-to-VSS mode (NS-mode), and ND-mode MM ESD stresses. Even the ND-mode MM ESD robustness of Pin-A and Pin-B can not achieve 200 V by VDD1 and VDD2 shorting together in the test board under ND-mode ESD stress. The ESD test results for this IC product are shown in Table 7.1. After ESD tests are finished, a monitor on leakage current is used to judge whether the I/O pin under ESD test is passed or failed. The traced I-V characteristics of the investigated IC before and after ESD stress are shown in Fig. 7.2.

Table 7.1

HBM and MM ESD Robustness of the Pin-A and Pin-B I/O Pins in this IC Product

ESD Test	I/O Pins	PS-Mode	NS-Mode	PD-Mode	ND-Mode
HBM	Pin-A	> 2.0 kV	> 2.0 kV	> 2.0 kV	> 2.0 kV
	Pin-B	> 2.0 kV	> 2.0 kV	> 2.0 kV	> 2.0 kV
MM	Pin-A	150 V	150 V	150 V	150 V
	Pin-B	150 V	150 V	150 V	100 V

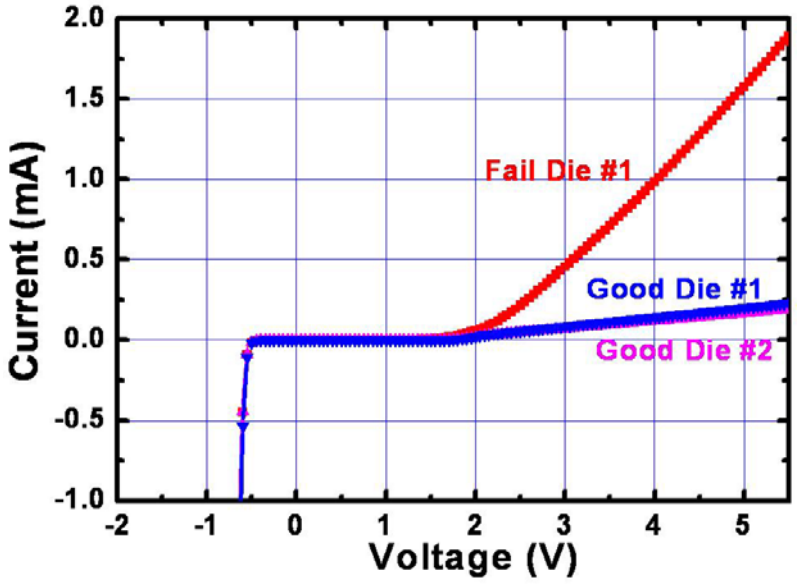


Fig. 7.2. After ND-mode MM ESD stress on I/O pins, the I-V characteristics of VDD2-to-VSS2 showed higher leakage currents than that before ESD stress.

Obviously, after the 200-V MM ESD stress, the leakage current at 3.3 V between VDD2 and VSS2 showed leakage current about 10 times higher, as compared with that of good dies. From the measured I-V characteristics, there are some ESD damages in the internal circuits between VDD2 and VSS2 after ESD stress. These internal ESD damages have also been clearly observed by the physical failure analysis, such as emission microscope (EMMI) and scanning electron microscope (SEM).

7.1.3. Failure Mechanism under Cross-Power-Domain ESD Stresses

In order to indicate the failure locations caused by ND-mode MM ESD stresses, the EMMI was used to find abnormal ESD failure spots in this IC. The measured EMMI photos are shown in Figs. 7.3(a) and 7.3(b) with the corresponding IC layout patterns of the ND-mode MM ESD failure sample. All the circled areas in Fig. 7.3(c) are the ESD damage locations indicated by EMMI around the interface circuits after ND-mode MM ESD stress.

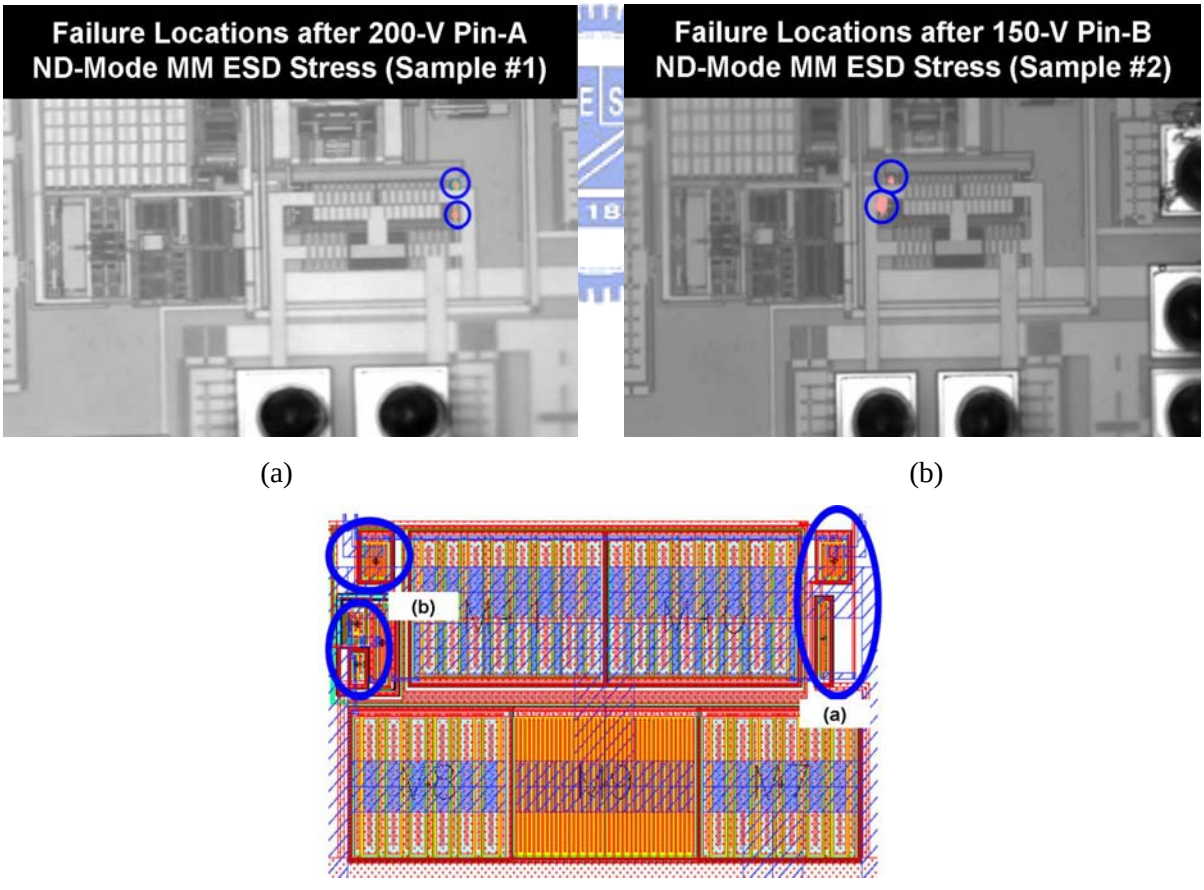
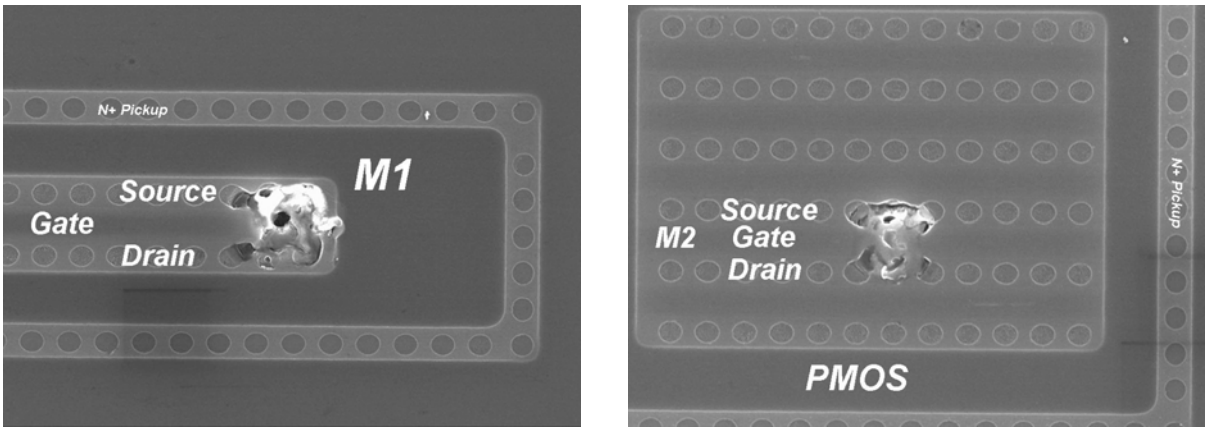


Fig. 7.3. According to EMMI failure analysis, abnormal hot spots were found at the interface circuits (see the circled areas) after ND-mode MM ESD stress on (a) Pin-A, and (b) Pin-B. (c) The corresponding layout locations of the interface circuits were indicated the failure spots in (a) and (b).

The ESD damages are recognized at the interface circuits by comparison with circuits and layout patterns to the SEM photos of ESD damaged failure spots. After Pin-A ND-mode MM ESD stress, the SEM photos of failure spots are shown in Figs. 7.4(a) and 7.4(b). The clear failure spots were found in two PMOS transistors (M1 and M2) of the interface circuits.



(a) (b)

Fig. 7.4. After ND-mode MM ESD stress on Pin-A, the failure spots were located at (a) PMOS transistor (M1), and (b) the other PMOS transistor (M2).

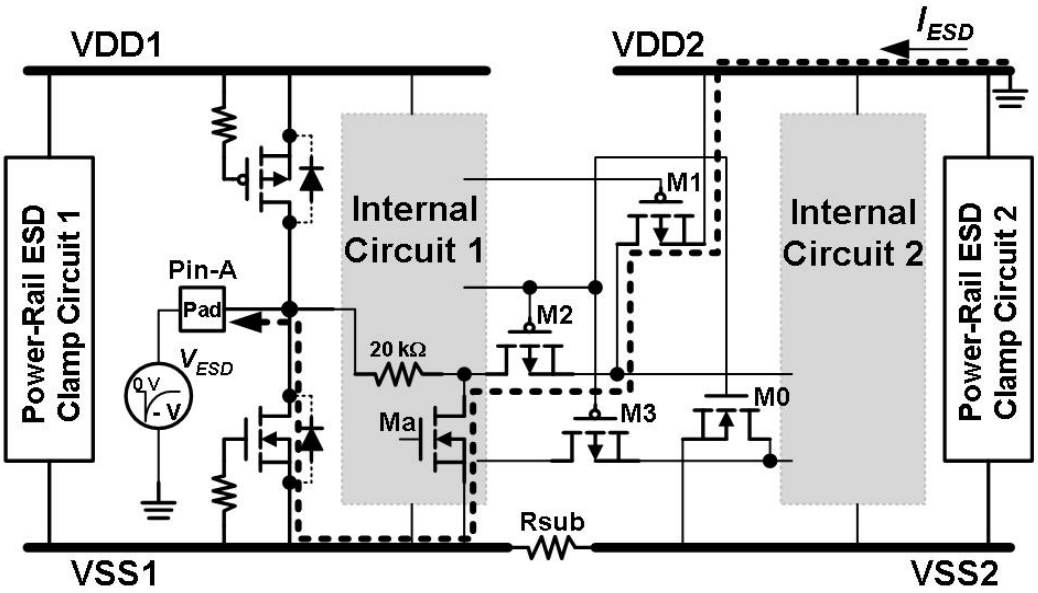
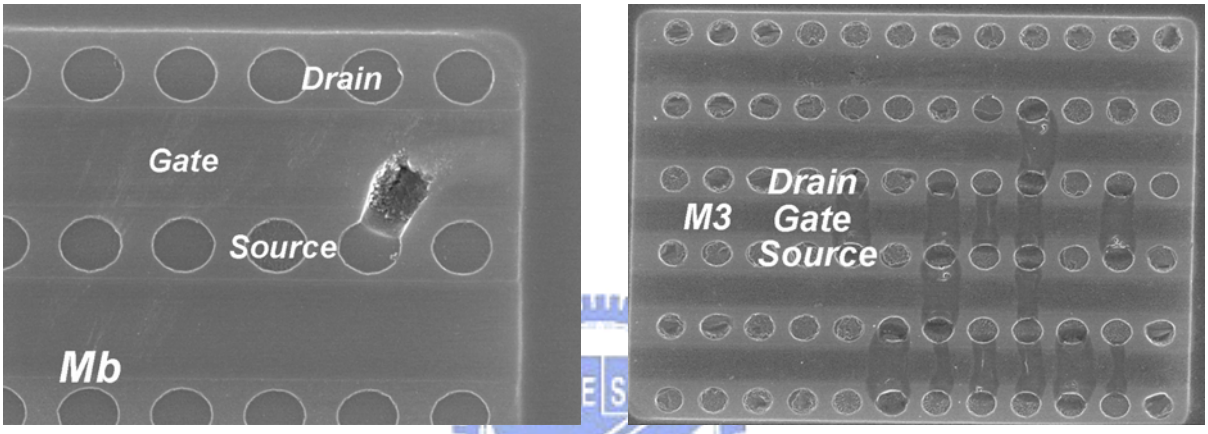


Fig. 7.5. The ESD current could be discharged through the circuitous path to cause ESD damages to M1 and M2 during ND-mode MM ESD stress on Pin-A.

However, the Pin-A are connected to the internal circuit 1 through a 20-kΩ poly-resistor, which can effectively block the ESD currents to damage internal circuits nearby the I/O cell. Therefore, the ESD current could be discharged by the circuitous path to cause damages on

the M1 and M2 after Pin-A ND-mode MM ESD stress, as shown in Fig. 7.5. Due to the larger device size of the Ma in Fig. 7.5, the ESD current didn't destroy it during ND-mode MM ESD stress. On the other hand, the failure spots were also found in two transistors of interface circuits after Pin-B ND-mode MM ESD stress, as shown in Figs. 7.6(a) and 7.6(b). ND-mode MM ESD currents were discharged by two mainly current paths, as the dashed lines shown in Fig. 7.7. These two paths provided the current paths to distributive discharge ESD current. The corresponding failure photos on the interface devices Mb and M3 are shown in Figs. 7.6(a) and 7.6(b), respectively.



(a) (b)

Fig. 7.6. (a) NMOS transistor (Mb), and (b) PMOS transistor (M3) of the interface circuits were destroyed after ND-mode MM ESD stress on Pin-B.

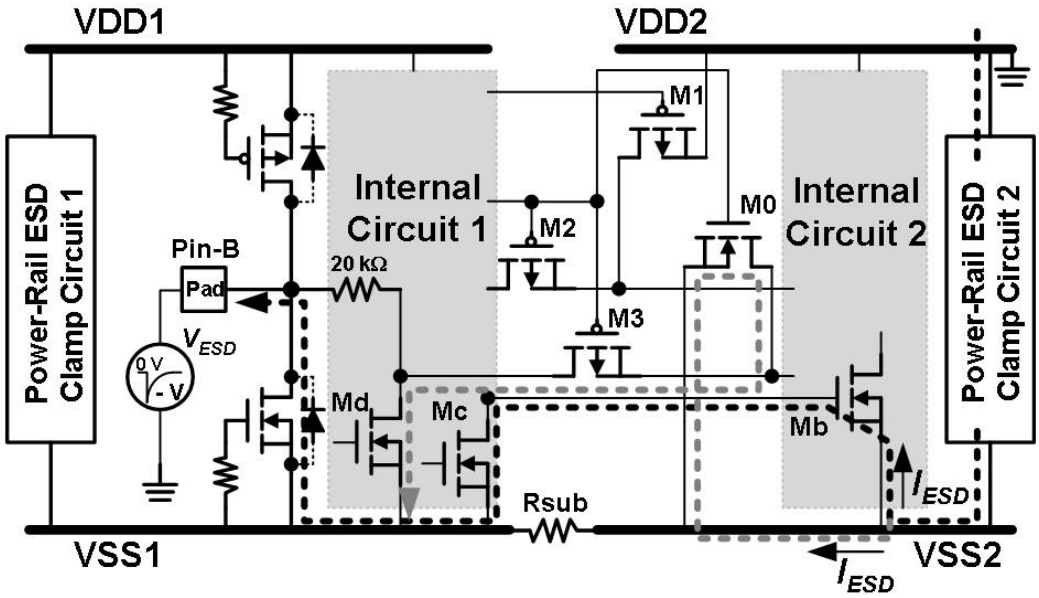


Fig. 7.7. ESD discharging paths during ND-mode MM ESD stress on Pin-B. The Mb and M3 were damaged after such ESD stress.

7.1.4. Proposed Solutions to Rescue such ESD Failures

To overcome such ESD failures at the interface circuits between separated power domains, adding the suitable blocking resistors (Rblock) to the interface devices and installing the bi-directional diode connection in original ESD protection scheme were proposed in Fig. 7.8. Two extra blocking resistors are added at the source terminal of the M1 and the gate terminal of the Mb, respectively. The bi-directional diode connection was used to connect the separated ground lines (VSS1 and VSS2). The diode numbers of the bi-directional diode connection were optimized to prevent different ground-line noise coupling issue between the separated ground lines of analog and digital circuit blocks. To further provide higher ground-line noise coupling isolation, the bi-directional silicon-controlled rectifier (SCR) [72] with ESD-detection circuit can be used to replace the bi-directional diode connection between the separated power lines (VDD1 and VDD2). By using the proposed ESD protection solutions, the ESD current will be effectively discharged along the desired connection of ground lines under ND-mode MM ESD stress. In addition, the blocking resistors also can avoid the ESD currents discharging through the undesirable paths. Therefore, the abnormal internal ESD damages can be overcome in this IC product with separated power lines.

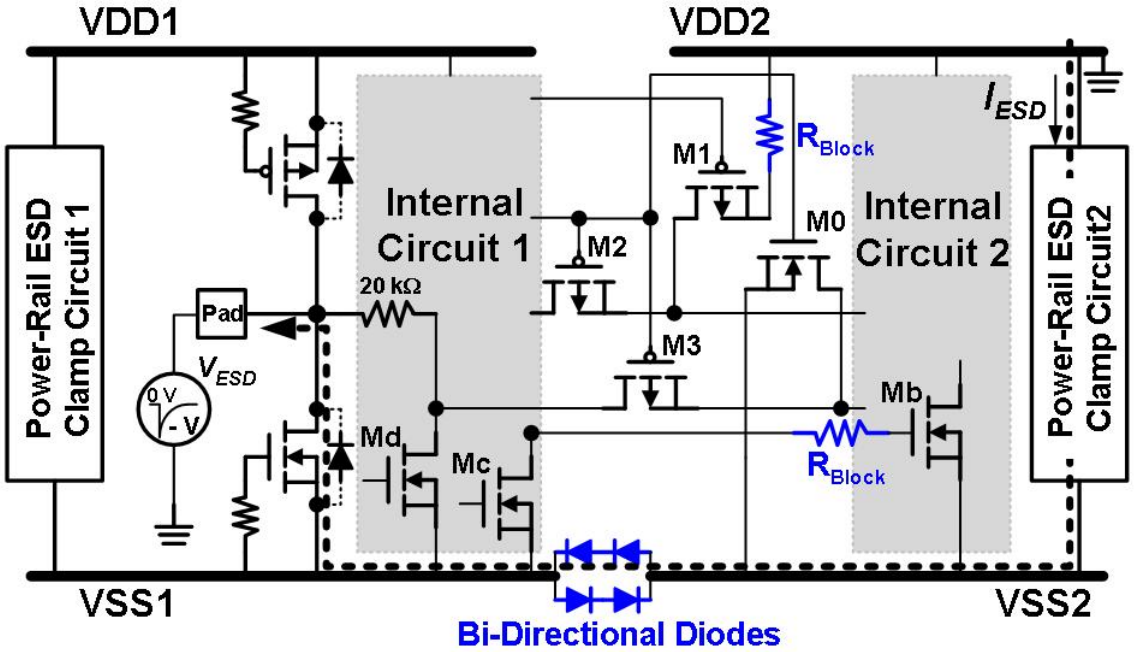


Fig. 7.8. The proposed ESD protection solution to rescue ESD failures at the interface circuits of this IC product with separated power domains.

7.2. Active ESD Protection Designs for Interface Circuits between Separated Power Domains

7.2.1. ESD Threats and Damages of Interface Circuits between Separated Power Domains

With more circuit blocks integrated into an IC product to meet different applications, such circuit blocks usually have separated power domains to supply the power and ground signals in each individual circuit block. In addition, the interface circuits were also adopted to communicate with different circuit blocks inside the chip. However, the interface circuits between separated power domains are often damaged under cross-power-domain ESD stresses [33]-[38]. The bi-directional diode connections between the separated power domains are usually applied to construct a completely whole-chip ESD protection design [39], [40], as shown in Fig. 7.8. In general, the bi-directional diode connections are only used to connect the separated VSS pins due to different VDD1 and VDD2 voltage levels and noise-coupling considerations [39], [40]. When the ESD voltage was applied on the VDD1 and grounded VDD2 under the cross-power-domain ESD stresses, the ESD current can be discharged from the VDD1 to the VSS1 by the power-rail ESD clamp circuit 1 in the power domain one, from the VSS1 to the VSS2 through the inserted bi-directional diode connection, and then from the VSS2 to the grounded VDD2 through the other power-rail ESD clamp circuit 2 in the power domain two, as the discharged path shown by dashed line in Fig. 7.9(a). The Vh1 and Vh2 are the holding voltage of the power-rail ESD clamp circuits 1 and 2, respectively. Then, the Vhd is the holding voltage of the bi-directional diode connection between the separated power domains. Among the parameters, the R1, R2, and Rd are the turn-on resistances of the power-rail ESD clamp circuits 1, 2, and the bi-directional diode connection, respectively. When the ESD current was conducted by this long discharging path, it would induce the overstress voltage across the each MOS transistor in interface circuits between separated power domains [40]-[42]. The induced voltage drops with discharging ESD currents from VDD1 to VDD2 on each node of the interface circuit had been estimated, as shown in Fig. 7.9(a). The voltage potential at node A could be raised up to the VDD1 because the driver's PMOS transistor (Mp1) had an initially floating gate situation. The highest voltage drop was applied across the gate oxide of the receiver's PMOS transistor (Mp2) in interface circuits under the VDD1 to VDD2 ESD stresses. On the other hand, the highest voltage drop was also generated across the gate oxide of the receiver's NMOS transistor (Mn2) in interface circuits

under the VDD1 to VSS2 ESD stresses. The similar estimation on voltage drops during ESD stress was presented in Fig. 7.9(b).

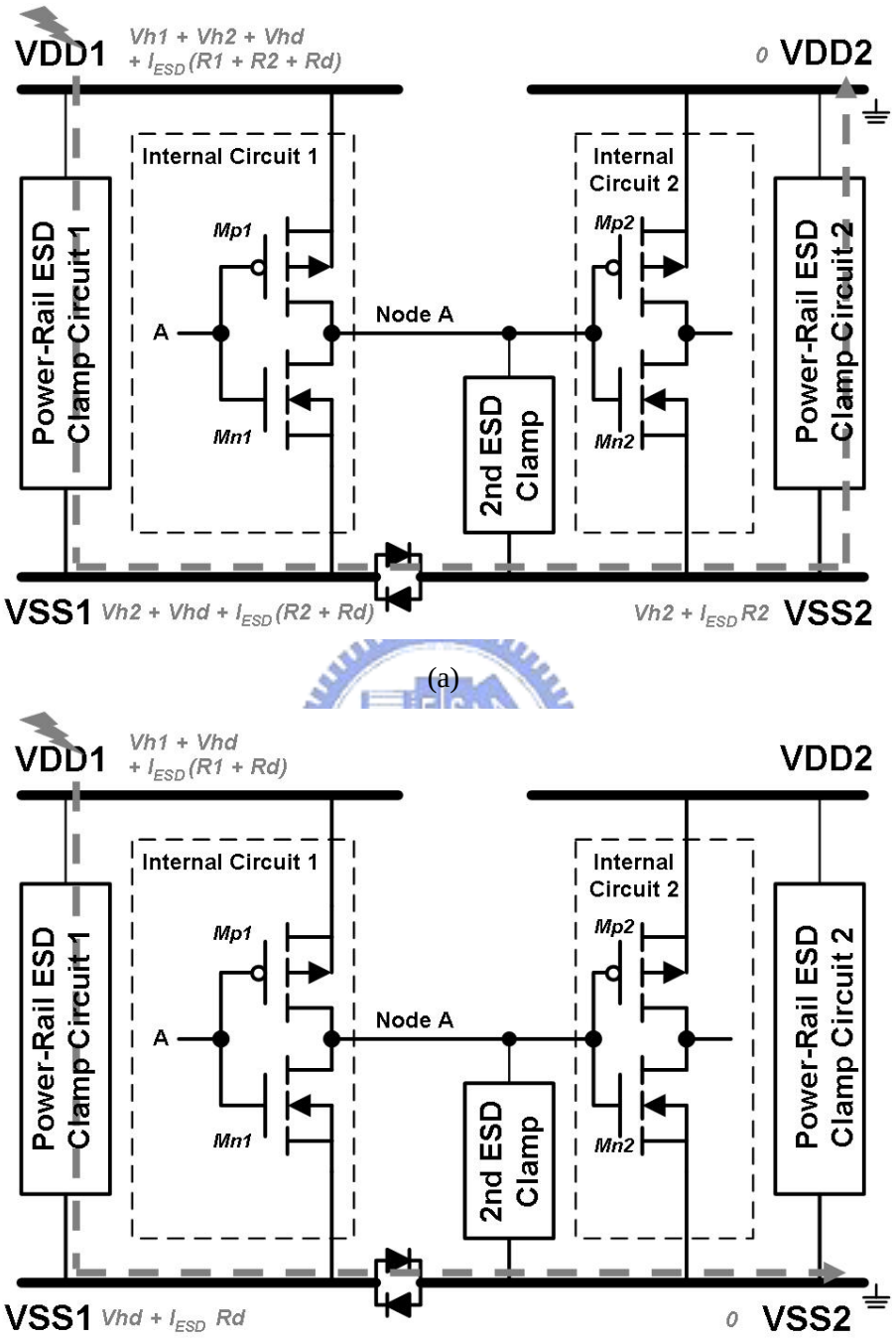


Fig. 7.9. The estimations of the induced voltage potential under the cross-power-domain (a) VDD1-to-VDD2, and (b) VDD1-to-VSS2, ESD stresses.

Therefore, the 2nd ESD clamp designs were usually installed nearby the MOS transistors of receiver to reduce the overstress voltage under the cross-power-domain ESD stresses

[40]-[42], as shown in Figs. 7.9(a) and 7.9(b). As the CMOS technologies being continually shrunk toward nanometer scales, the breakdown voltages of ultra-thin gate oxide in the MOS transistors were sharply reduced to impact the ESD protection designs. It was important to avoid the gate oxide damages of the MOS transistors in the interface circuits by ESD-current induced overstress voltages. The overview on some 2nd ESD clamp designs will be presented and compared in the following sub-section.

7.2.2. Review on ESD Protection Designs for Interface Circuits between Separated Power Domains

The resistor-diode clamp design [40], which consists of a resistor (R1) and two diodes, was allocated in the interface circuits between separated power domains in order to restrict the ESD current distribution and to clamp the overstress voltage across the gate oxide of the receiver's MOS transistors, as shown in Fig. 7.10.

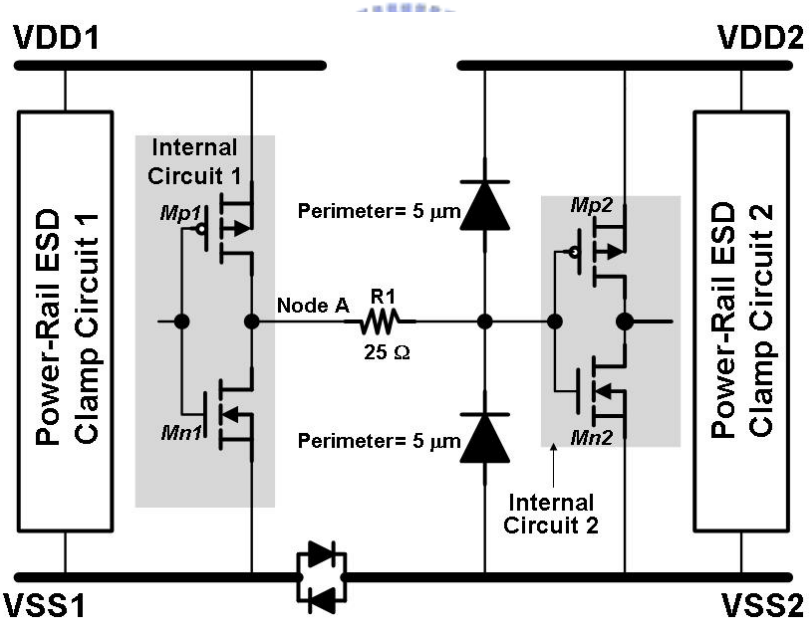


Fig. 7.10. The ESD protection design with resistor-diode clamp had been proposed to protect the interface circuits between separated power domains [40].

These two clamped diodes can be respectively replaced by the gate-grounded NMOS (GGNMOS) transistor and gate-VDD PMOS (GDPMOS) transistor to further enhance the clamping efficiency. However, such traditional junction-breakdown clamp designs with diodes, GGNMOS, or GDPMOS could not be suitable for interface circuits with ultra-thin oxide against cross-power-domain ESD stresses. Therefore, some second ESD protection

designs with special trigger mechanisms, such as the modified interface circuits with special drivers and receivers [41] as well as the ground-current-trigger (GCT) NMOS transistor [42], had been proposed to efficiently reduce the overstress voltages across the ultra-thin gate oxides of the MOS transistors in interface circuits between separated power domains.

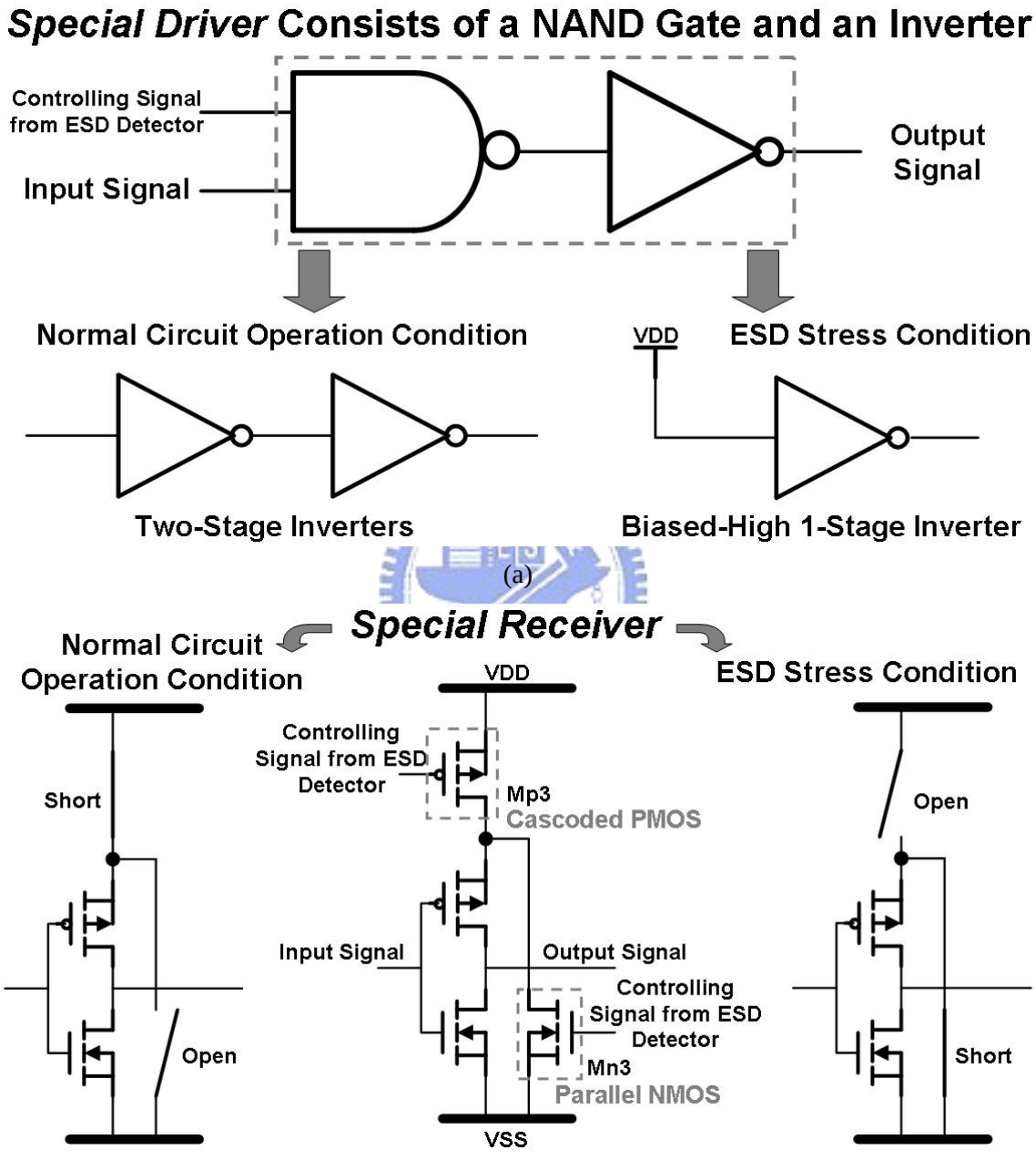


Fig. 7.11. The ESD protection design with (a) a special driver and (b) a special receiver for interface circuits between separated power domains [41].

The special driver and receiver had been implemented for interface circuits between separated power domains, which were collaborated with an ESD detector to accomplish

differently desired functions under the cross-power-domain ESD stress condition and the normal circuit operation condition, as presented in Figs. 7.11(a) and 7.11(b) [41]. The special driver was composed of a 1-stage NAND gate and a 1-stage inverter. Through different signals from the ESD detector, the driver can be respectively performed as cascaded 2-stage inverters and a biased-high 1-stage inverter under normal circuit operation condition and VDD1-to-VDD-2 cross-power-domain ESD stress, as illustrated in Fig. 7.11(a). In addition, the special receiver consisted of a 1-stage inverter, a PMOS transistor (Mp3) cascoded on the inverter, and a NMOS transistor (Mn3) in parallel to the inverter. The cascoded PMOS and the parallel NMOS transistors, both of which were controlled by the ESD detector, will be respectively turned on and off under normal circuit operation condition, whereas the Mp3 and the Mn3 will be respectively turned off and on under cross-power-domain ESD stress, as shown in Fig. 7.11(b). Although such special designs in the driver and receiver [41] can reduce and restrain the overstress voltage across the gate oxide of receiver's PMOS and NMOS transistors, the complicated connection could be an obstacle to practical applications.

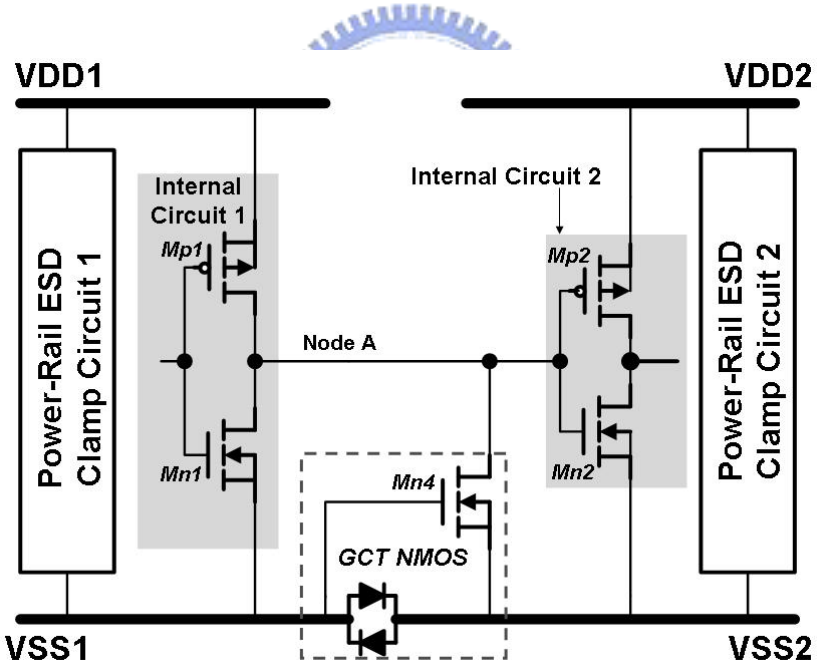


Fig. 7.12. The ESD protection design with grounded-current-trigger (GCT) NMOS transistor for interface circuits between separated power domains [42].

On the other hand, the grounded-current-trigger (GCT) NMOS transistor [42] had been also proposed to act as a 2nd ESD clamp for interface circuits between separated power domains, as shown in Fig. 7.12. The GCT NMOS transistor can be turned on to clamp the overstress voltage across the gate oxide of receiver's PMOS and NMOS transistors by the

induced voltage drop between VSS1 and VSS2 under cross-power-domain ESD stress. But, it will be kept off due to the same voltage potential on VSS1 and VSS2 under normal circuit operation condition. This active 2nd ESD clamp design can achieve high ESD robustness under cross-power-domain ESD stress [42]. In this work, one new active ESD protection design for interface circuits between separated power domains was proposed to solve this problem.

7.3. New Cross-Power-Domain ESD Protection Design

7.3.1. Implementation of the New Proposed Design for Cross-Power-Domain ESD Protection

An ESD protection design was implemented by gate-controlled PMOS (GC-PMOS) and gate-controlled NMOS (GC-NMOS) transistors with the ESD-transition detection function for interface circuits between separated power domains, as shown in Fig. 7.13. The GC-PMOS (Mp3) and GC-NMOS (Mn3) were placed nearby the receiver in the interface circuits to clamp overstress voltages across the gate oxides of the receiver's NMOS and PMOS transistors (Mn2 and Mp2), respectively. The gate terminals of GC-PMOS and GC-NMOS transistors were respectively connected to the VDD2 and VSS2 through the 1-kΩ resistance. The 1-kΩ resistances are adopted to avoid the gate-oxide damages to GC-PMOS and GC-NMOS transistors during the ESD stresses. During the VDD1-to-VSS2 cross-power-domain ESD stress, the positive ESD voltage was applied at the VDD1 with the grounded VSS2. The gate-to-source voltage (Vgs) of the GC-PMOS transistor (Mp3) was high enough to turn this Mp3 on under VDD2 floating. The voltage potential of node A can be clamped by the turn-on Mp3 to restrict the overstress voltage across the receiver's NMOS transistor (Mn2). When the negative ESD voltage was applied at VDD1 with the grounded VSS2, the forward-biased parasitic diode, which was consisted of N-well and P+ drain diffusion in Mp3, will provide excellent ability to clamp the voltage across Mn2. In addition, the GC-NMOS transistor (Mn3) was useful to prevent ESD damage under the VDD1-to-VDD2 ESD stresses. When the positive ESD voltage was applied at the VDD1 with the grounded VDD2, the ESD current initially discharged by the desired path, which was the dashed line in Fig. 7.9(a). This ESD discharging current will induce the voltage levels on VDD1, VDD2, VSS1, and VSS2. The induced voltage level of VSS2 was higher than that of VDD2 under the positive VDD1-to-VDD2 ESD stresses. The GC-NMOS

transistor (Mn3) can be turned on by the induced voltage levels of VSS2 and VDD2. Then, the voltage level at node A can be restricted to avoid damages to the gate oxide in the interface circuits. The GC-NMOS transistor can also be turned on in the negative ESD stresses since the voltage level at node A would be lower than that of VSS2. On the other hand, the parasitic npn bipolar transistor in Mn3 can be triggered on to restrict the voltages across the gate oxides of Mn2 and Mp2 under VDD1-to-VDD2 ESD stresses.

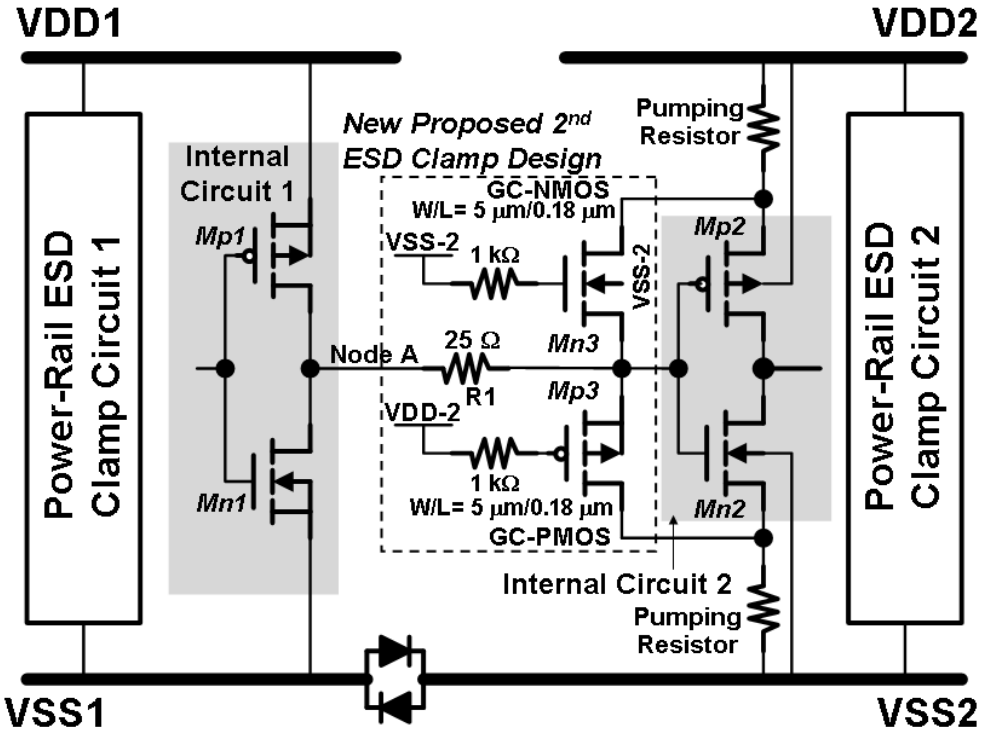


Fig. 7.13. A proposed cross-power-domain ESD protection design with gate-controlled PMOS and NMOS (GC-PMOS and GC-NMOS) transistors and source pumping mechanism.

According to previous studies, gate oxide breakdown voltages of gate-to-source terminals and gate-to-bulk terminals are quite different in NMOS transistors [73]. The gate oxide breakdown voltage of gate-to-source terminal is remarkably lower than that of gate-to-bulk terminal. In order to enhance the ESD robustness of the input stage with thin gate oxide in nanoscale CMOS process and extend the design windows of ESD protection circuits, the source pumping design had been used to reduce the ESD voltage across the gate-to-source terminal in the NMOS transistor of input stage under HBM and CDM ESD stresses [73], [74]. In Fig. 7.13, a resistor had also been inserted between VDD2 (or VSS2) and source terminal of Mp2 (or Mn2) to comprise source pumping mechanism. The partial ESD currents could be conducted by turned-on Mp3 and Mn3, also raised the source-terminal potentials of Mn2 and

Mp2 to reduce the voltage across the gate-to-source terminals of Mn2 and Mp2. The source pumping mechanisms can be expected to further enhance the ESD robustness of the receivers in interface circuits under the cross-power-domain ESD stresses.

7.3.2. Experimental Results

The cross-power-domain ESD protection design with the GC-PMOS and GC-NMOS transistors had been implemented in 0.13-μm 1.2-V CMOS process. Two other different cross-power-domain ESD protection designs, which were diodes [40] and ground-current-triggered (GCT) NMOS transistor [42], were also compared with the design with GC-PMOS and GC-NMOS transistors under the same process. The cross-power-domain ESD protection design with diodes was identical with the aforementioned scheme, as shown in Fig. 7.10. However, the GCT NMOS transistor was only substituted for the GC-PMOS transistor to construct a complete cross-power-domain ESD protection in this work, as shown in Fig 7.14.

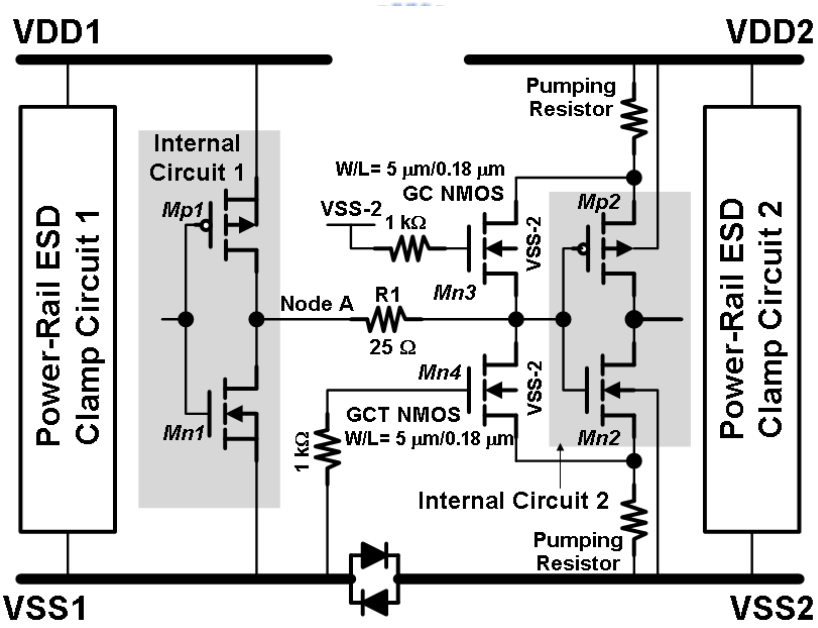


Fig. 7.14. The cross-power-domain ESD protection design with GCT NMOS and GC-NMOS transistors and source pumping mechanism.

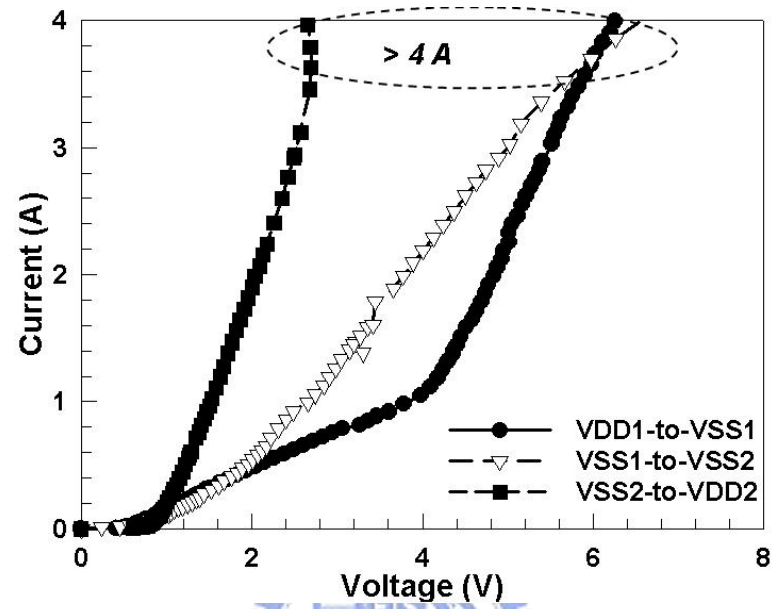
Both device sizes (W/L) of the gate-controlled PMOS (Mp3) and NMOS (Mn3) transistors are 5 μm / 0.18 μm. Then, the value of R1 is 25 Ω. Because the ESD currents were not mainly discharged by the Mn3 and Mp3, these transistors did not need to occupy huge device dimensions. The equivalent perimeters of the diodes are 5 μm, and the device size (W/L) of the GCT NMOS transistor is also 5 μm / 0.18 μm in this work. These

cross-power-domain ESD protection designs had the identical ESD protection elements of the power-rail ESD clamp circuit in each power domain and the bi-directional diode connection between separated power domains. The I-V characteristics of these three designs were measured by transmission-line-pulse (TLP) system, which generated the current pulses with 100-ns duration time and 10-ns rise time to be able to obtain the device characteristics under high-current stresses [50].

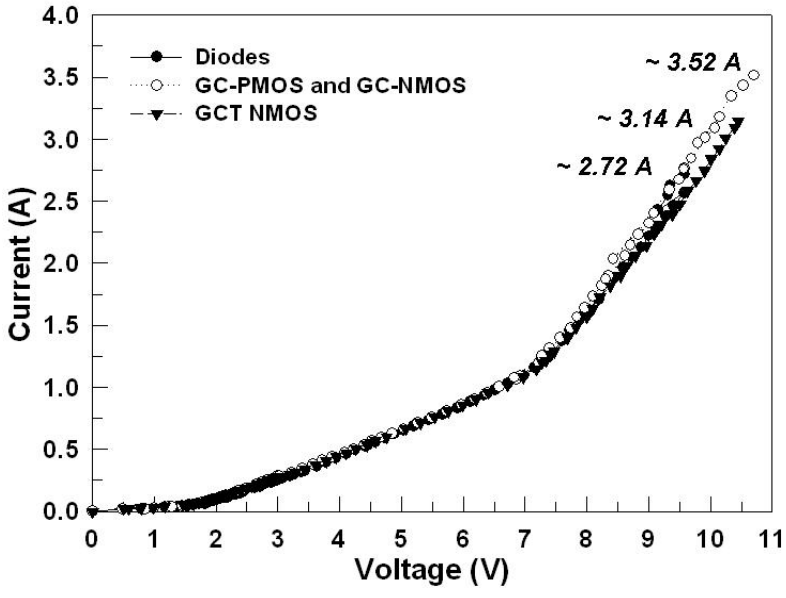
The TLP I-V characteristics of the cross-power-domain ESD protection design with the GC-PMOS and GC-NMOS transistors under VDD1-to-VSS1, VSS1-to-VSS2, and VSS2-to-VDD2 three different stress combinations had been measured and illustrated in Fig. 7.15(a). The symbol of VDD1-to-VSS1 (VSS1-to-VSS2 or VSS2-to-VDD2) means that the TLP current pulse was applied at the VDD1 (VSS1 or VSS2) under the grounded VSS1 (VSS2 or VDD2). Therefore, the VDD1-to-VSS1 curve presents the TLP I-V characteristic of a power-rail ESD clamp circuit which consists of RC-based ESD-transient detection circuit and main power-rail ESD clamp NMOS transistor between VDD1 and VSS1. Then, the VSS1-to-VSS2 is the TLP I-V characteristic of the bi-directional diode connection between VSS1 and VSS2, while the VSS2-to-VDD2 is the TLP I-V characteristic of the parasitic drain-bulk diode in the power-rail ESD clamp NMOS transistor between VSS2 and VDD2. Moreover, the TLP measured results of all three different cross-power-domain ESD protection designs were shown in Fig. 7.15(b). Under the VDD1-to-VSS2 stresses, these three different cross-power-domain ESD protection designs presented high second breakdown currents (It2). The cross-power-domain ESD protection design with GC-PMOS and GC-NMOS transistors had the highest It2 value about 3.52 A. The HBM and MM ESD robustness of these three designs were presented in Table 7.2, under VDD1-to-VSS2 and VDD1-to-VDD2 ESD stresses. The new proposed ESD design had the highest ESD robustness among all ESD stresses. However, the cross-power-domain ESD protection design with diodes presented an unexpected ESD robustness under VDD1-to-VDD2 ESD stresses. The related attributions of the low ESD robustness in the design with diodes would be discussed and explained by failure analyzing in following section.

In addition, the influence of source pumping mechanism was investigated in cross-power-domain ESD protection designs with GCT NMOS transistor. The comparisons between the cross-power-domain ESD protection designs with and without source pumping resistance were shown in Fig. 7.16(a). The It2 value of the design with source pumping resistance was significantly higher than that without source pumping resistance. The It2 values of the designs with and without source pumping resistance are about 3.14 A and 2.26 A

under VDD1-to-VSS2 TLP stresses, respectively. On the other hand, the other TLP measured results, which the cross-power-domain ESD protection designs were adopted as GC-PMOS and GC-NMOS transistors, with the different source pumping resistances of 5 Ω and 15 Ω were also shown in Fig. 7.16(b).



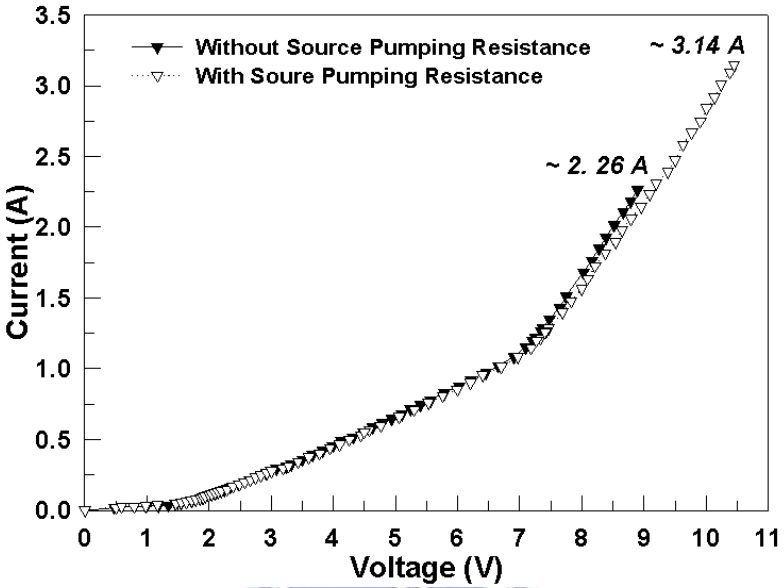
(a)



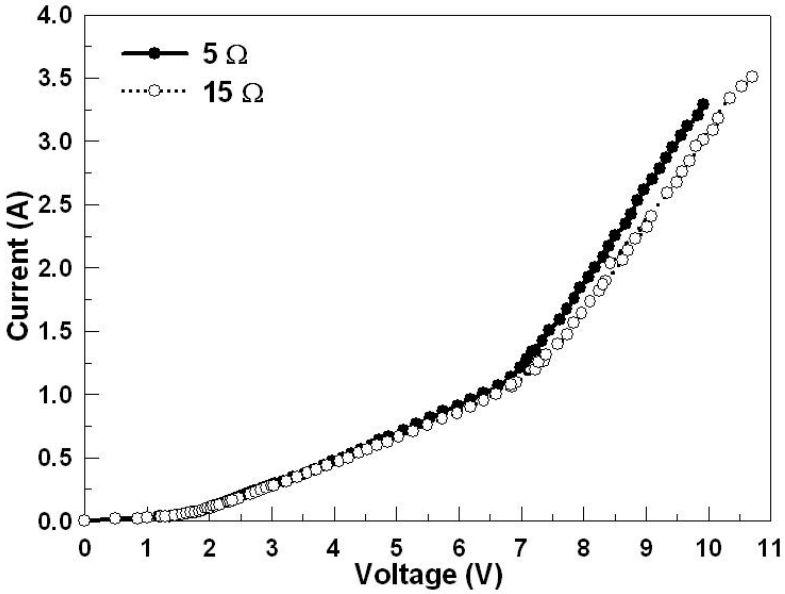
(b)

Fig. 7.15. (a) The 100-ns TLP measured I-V characteristics of the cross-power-domain ESD protection design with GC-PMOS and GC-NMOS transistors under VDD1-to-VSS1, VSS1-to-VSS2, and VSS2-to-VDD2 three different stress combinations. (b) The 100-ns TLP measured I-V characteristics of the three different cross-power-domain ESD protection designs under VDD1-to-VSS2 stresses.

The It2 values were increased by increasing the resistance of the source pumping resistors. According to the measured results, the source pumping resistance can be expected to enhance the ESD robustness for the cross-power-domain ESD protection designs. However, this source pumping resistances would also cause the body effect and affect the circuit performance on the receiver.



(a)



(b)

Fig. 7.16. The influence of source pumping mechanism on the TLP measured I-V characteristics of the cross-power-domain ESD protection designs under VDD1-to-VSS2 stresses. (a) With or without source pumping resistance in the design with GCT NMOS transistor. (b) With source pumping resistance of 5 Ω or 15 Ω in the design with GC-PMOS and GC-NMOS transistors.

Table 7.2

HBM and MM ESD Robustness of the Different Cross-Power-Domain ESD Protection Designs under VDD1-to-VSS2 and VDD1-to-VDD2 ESD Testing Conditions

VDD1 to VSS2

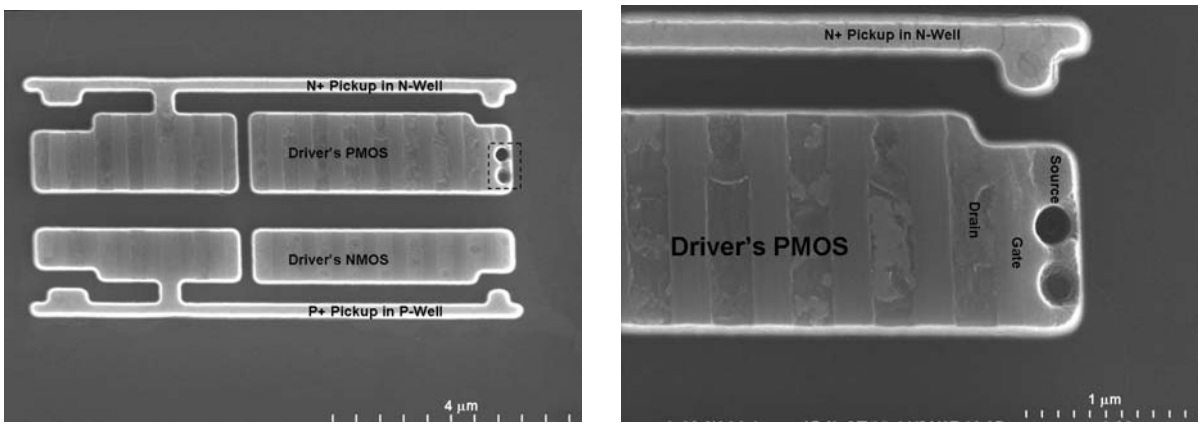
Designs / ESD	Resistor-Diode	Modified GCT NMOS	GC-PMOS & GC-NMOS (New Proposed)
HBM	3.5 kV	4.5 kV	4.5 kV
MM	450 V	450 V	550 V

VDD1 to VDD2

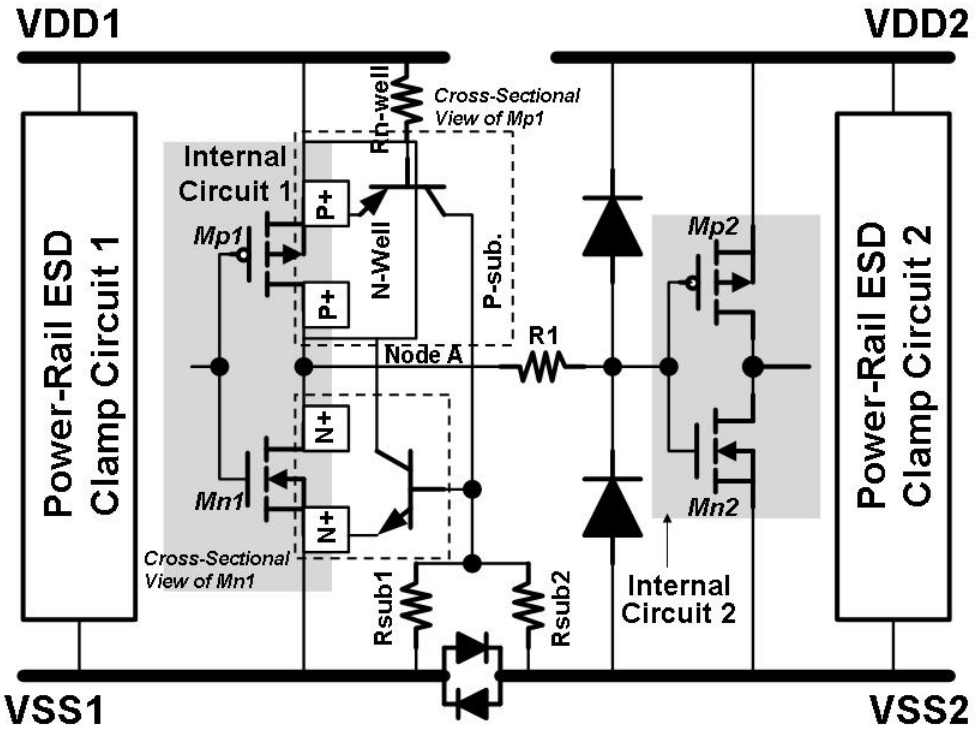
Designs / ESD	Resistor-Diode	Modified GCT NMOS	GC-PMOS & GC-NMOS (New Proposed)
HBM	2 kV	3.5 kV	4.5 kV
MM	300 V	350 V	400 V

7.3.3. Failure Analysis and Discussion

The cross-power-domain ESD protection design with diodes presented lower ESD robustness among all ESD testing conditions, shown in Table 7.2. However, the lower ESD robustness of the ESD protection design with diodes can be attributed to two completely different failure mechanisms under VDD1-toVSS2 and VDD1-to-VDD2 ESD stresses, respectively. First, the failure spot of the design with diodes was located at the source side of the driver's PMOS transistor under VDD1-to-VSS2 ESD stresses, as shown in Figs. 7.17(a) and 7.17(b). This failure spot only occurred on the source side of the driver's PMOS transistor. The gate area and drain side of the driver's PMOS transistor did not be destroyed after VDD1-to-VSS2 ESD stresses, as illustrated in Fig. 7.17(b). The failure mechanism could be explained that the vertical pnp bipolar transistor was turned on to cause the serious contact spike on the source side, as shown in Figs. 7.17(b) and 7.17(c). This vertical pnp bipolar transistor consisted of the P+ source diffusion of the driver's PMOS, the N-well, and the mutual P-substrate, as shown in Fig. 7.17(c). Furthermore, this vertical pnp bipolar transistor would easily incorporate with a lateral npn bipolar transistor, which consists of the n-well, the p-substrate, and the N+ source diffusion of the driver's NMOS to construct a parasitic SCR path between VDD1 and VSS1, as also illustrated in Fig. 7.17(c).



(a) (b)

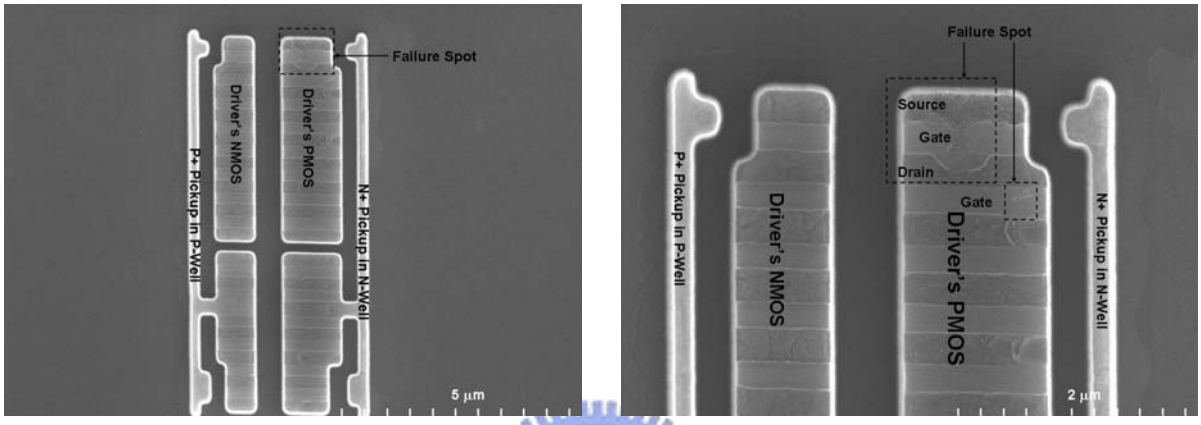


(c)

Fig. 7.17. (a) After VDD1-to-VSS2 HBM ESD stress, the failure spots of the cross-power-domain ESD protection design with diodes were located at the source side of the driver's PMOS transistor (Mp1). (b) The zoomed-in view of the failure spot. (c) The failure mechanism of the cross-power-domain ESD protection design with diodes under VDD1-toVSS2 HBM ESD stress.

Because the protecting diode between node A and VSS2 was under the reverse biasing condition, the partial ESD current could not conduct from the driver's PMOS transistor to grounded VSS2. The partial ESD current could be discharged through this SCR path between VDD1 and VSS1 and the diode between VSS1 and VSS2 since no guard ring and pick up were installed between the driver's PMOS and NMOS transistors under such situation. In

contrast, the failure mechanisms of the cross-power-domain ESD protection designs with GCT NMOS, GC-PMOS, and GC-NMOS transistors were caused by the drain-to-source filaments that were clearly proved in Figs. 7.18(a) and 7.18(b). The partial ESD current conducted from the source side to drain side in the driver's PMOS transistor to cause the damage to the surface layer on this PMOS transistor under VDD1-to-VSS2 ESD stresses [42].



(a) (b)

Fig. 7.18. (a) After VDD1-to-VSS2 HBM ESD stress, the failure spots of cross-power-domain ESD protection design with GC-PMOS and GC-NMOS transistors were located at the driver's PMOS transistor (Mp1). (b) The zoomed-in view of the failure spot.

Secondly, the failure spot of the ESD protection design with diodes was located at the source and drain sides of the driver's PMOS transistor under VDD1-to-VDD2 ESD stresses, as shown in Fig. 7.19(a). This failure spot was similar to those of the cross-power-domain ESD protection designs with GCT NMOS, GC-PMOS, and GC-NMOS transistors under VDD1-to-VSS2 and VDD1-to-VDD2 ESD stresses, as shown in Figs. 7.18(b) and 7.19(b). Since the protecting diode between node A and VDD2 was under the forward biasing condition, the ESD currents could easily conduct from the driver's PMOS transistor to grounded VDD2. This discharging path sustained huge ESD current to cause the source-to-drain filament on the driver's PMOS transistor, as presented in Fig 7.19(a). Besides, the failure spot was also found in the receiver's PMOS transistor after VDD1-to-VDD2 ESD stresses, especially in MM ESD event, as shown in Fig. 7.19(c). This failure spot did not occur on the cross-power-domain ESD protection designs with GCT NMOS, GC-PMOS, and GC-NMOS transistors. The ESD protection design with diodes conducted huge ESD current cause the damage to the receiver's PMOS transistor under VDD1-to-VDD2 MM ESD

stresses. Therefore, the unsuitable current distributions of the cross-power-domain ESD protection design with diodes were caused the lower ESD robustness under VDD1-to-VSS2 and VDD1-to-VDD2 ESD stresses. Because these ESD protection designs were mainly focused on the receiver's gate oxide threat, the failure spots did not be located on the receiver except that of the ESD protection design with diodes. However, according to the above measured results and failure analyses, the ESD robustness of the cross-power-domain ESD protection designs with GCT NMOS, GC-PMOS, and GC-NMOS transistors seemed to be restricted and dominated by the failure mechanism of the driver's PMOS transistors. The blocking resistance, which is shown in Fig. 7.8, should be appropriately inserted between driver's source terminal and VDD1 in order that the ESD robustness of the interface circuits between separated power domains could be further enhanced.

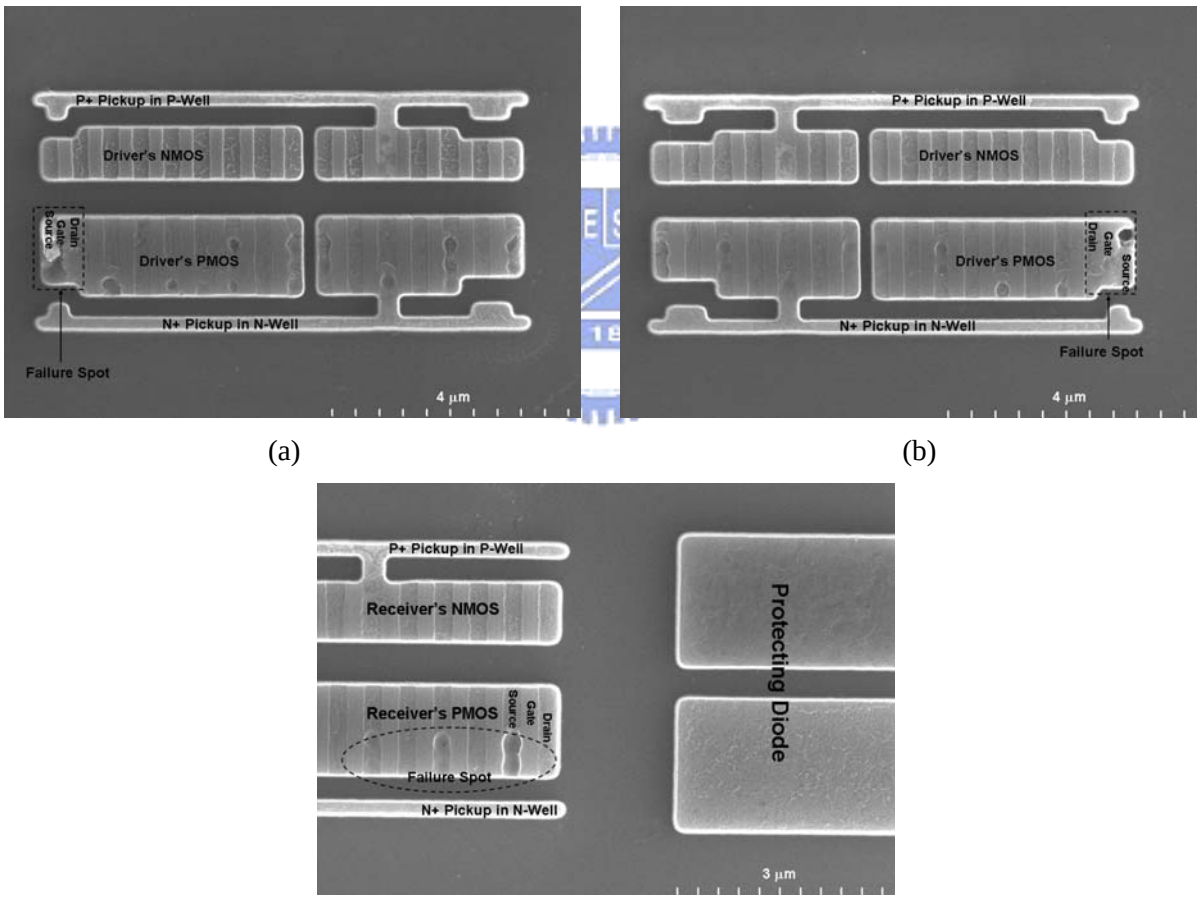


Fig. 7.19. (a) and (b), both cross-power-domain ESD protection designs with diodes and GC-PMOS and GC-NMOS transistors have the failure spots at the driver's PMOS transistor (Mp1) after VDD1-to-VDD2 ESD stresses. (c) The other failure spots of cross-power-domain ESD protection designs with diodes were found at the receiver's PMOS transistor (Mp2) after VDD1-to-VDD2 MM ESD stress.

7.4. Summary

Due to the circuit performance considerations, the IC product has two separated power domains to cause ESD failures in interface circuits between different power domains. MM ESD currents are discharged through some unexpected paths in the interface circuits during ND-mode ESD stress. Each failure mechanism of Pin-A and Pin-B has been clearly analyzed and illustrated by the failure spot images and ESD current discharge paths. The effective solutions have been proposed to overcome abnormal internal ESD damage by means of adding the blocking resistors to the interface devices and installing the suitable bi-directional diode connection cells between the separated power lines. The optimum modifications have been proven in the new version IC product to sustain MM ESD level of greater than 200V. Besides, the cross-power-domain ESD protection designs with resistor-diode clamp, the special driver and receiver, or the GCT NMOS transistor have been reviewed to compare the ESD protection schemes for interface circuits between separated power domains. Moreover, one new active ESD protection design with gate-controlled PMOS and NMOS transistors has been proposed and successfully verified to sustain 4-kV HBM and 400-V MM ESD stresses in a 0.13-μm 1.2-V CMOS technology. The source pumping mechanism was also proven to significantly enhance the ESD robustness under the cross-power-domain ESD stresses. Finally, the failure mechanisms of three different cross-power-domain ESD protection designs, which were diodes, GCT NMOS, GC-PMOS, and GC-NMOS transistors, have been distinctly illustrated according to the related ESD failure locations and discharge paths.

Chapter 8

Conclusions and Future Works

This chapter summarizes the main results of this dissertation. Suggestions for future research in power-rail ESD clamp circuits, analog I/O interface circuits, and cross-power-domain ESD protection circuits for on-chip ESD protection design with advanced nanoscale CMOS technology are also provided in this chapter.

8.1. Main Results of This Dissertation

With the evolution of CMOS technology, the electrostatic discharge (ESD) threat has become a major reliability concern for CMOS IC products fabricated in the advanced nanoscale CMOS process. The power-rail ESD clamp circuit is an efficient design to achieve whole-chip ESD protection in IC products. It not only can improve ESD robustness of VDD-to-VSS ESD stress, but also can significantly enhance ESD robustness of input/output-to-VDD/VSS and pin-to-pin ESD stresses. Furthermore, to efficiently protect the core circuits realized with much thinner gate oxide and shallower junction in nanoscale CMOS technology, the efficient power-rail ESD clamp circuits must be added into CMOS chips to avoid the damages to the fragile gate oxide and the junction. Thus, the optimization of circuit schemes, such as controlling circuit and ESD-transient detection circuit, is an essential challenge for ESD protection in nanoscale CMOS technology. In this dissertation, the circuit schemes, which are implemented by single-stage and multi-stage inverters, for controlling circuit has been compared and verified. In addition, the ESD-transient detection circuit also needs to be optimized to further reduce the occupied chip area and prevent mis-trigger and latch-on concerns under fast power-on operation. In this dissertation, an efficient ESD-transient detection circuit adopted capacitance coupling mechanism has been has been proposed and verified. With the proposed circuit scheme for ESD-transient detection circuit, the controlling circuit of 1-stage inverter can be accomplished the desirable function on commanding the main ESD clamp NMOS transistor in power-rail ESD clamp circuit.

On-chip ESD protection devices are often required to provide higher ESD robustness

with smaller layout area to reduce the occupied chip area, especially in the high-pin-count IC products. Silicon controlled rectifiers (SCRs) have been used as on-chip ESD protection devices, because of their superior area-efficient ESD robustness. SCR device as power-rail ESD clamp device has also been presented in this dissertation. A novel initial-on SCR design has been proposed and verified to achieve the lowest trigger voltage and the highest turn-on efficiency of SCR device. Besides the enhancement of the power-rail ESD clamp circuit, the ESD protection designs for analog I/O interface circuits and cross-power-domain interface circuit are proposed and verified in this dissertation. In order to reduce the input capacitance of the analog I/O interface circuit, the ESD clamp devices between input pad and VDD (or VSS) are designed with smaller device dimensions. However, such small devices can't sustain high enough ESD level, while the analog pin is stressed in the positive-to-VSS (PS-mode) or the negative-to-VDD (ND-mode) ESD stress (the devices operated in the breakdown condition). Therefore, an efficient power-rail ESD clamp circuit between VDD and VSS was co-constructed into the analog ESD protection circuit to improve the overall ESD level of the analog I/O interface circuit. Finally, as the ultra-large-scale-integrated (ULSI) circuits being continually developed toward system-on-chip (SoC) applications, more and more multiple separated power domains are used in a SoC IC for specified circuit functions, such as digital/analog circuit blocks, mixed-voltage circuit blocks, and power management considerations. A new active ESD protection design for the interface circuits between separated power domains has been also proposed to solve the interface circuit damages under cross-power-domain ESD stresses.

Chapter 2 compares the designs with controlling circuits of 3-stage inverters and 1-stage inverter to verify the optimal circuit schemes in NMOS-based power-rail ESD clamp circuits. In addition, the circuit performance among the four different main ESD clamp NMOS transistors drawn with different drain-contact-to-poly-gate spacings and co-designed with different inverter stages in the controlling circuits are compared. According to the experiments and analyses, the 3-stage inverters for controlling circuit and BFET layout style for the main ESD clamp NMOS transistor can slightly increase the ESD robustness, but they will dramatically degrade the immunity against mis-trigger and latch-on issues under the EFT test and fast power-on condition. The 1-stage inverter should be an appropriate and reliable candidate for the controlling circuit in the power-rail ESD clamp circuits. Finally, the latch-on phenomenon has been successfully observed by the emission microscope with InGaAs FPA detector. The root cause to induce such failure can be attributed to the abnormal mechanism of the voltage drop across the n-well resistance after the EFT test.

In Chapter 3, a new proposed ESD-transient detection circuit cooperated with NMOS-based power-rail ESD clamp circuit has been presented and successfully verified in a 130-nm CMOS technology. The new proposed ESD-transient detection circuit adopts the capacitance coupling mechanism and a switch NMOS transistor to command the main ESD clamp NMOS transistor by the general controlling circuit with single-stage inverter. According to the measured results, the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit exhibits the superior ESD robustness of 8.0 kV and 400 V in HBM and MM ESD stresses, respectively. Moreover, it also possesses an excellent immunity against the mis-trigger and latch-on event under the 1.2-V fast power-on condition with the rise time of 2 ns.

In Chapter 4, the "*initial-on*" ESD protection concept realized by the PMOS-triggered SCR device with RC-based ESD-transient detection circuit has been successfully designed and verified in a 0.25-μm salicided CMOS process. Compared to the LVTSCR, the lowest trigger voltage and the highest turn-on efficiency of SCR device can be achieved by the proposed PMOS-triggered technique for effective on-chip ESD protection. Such PMOS-triggered SCR also presents a high enough holding voltage to overcome the latchup issue under the normal circuit operation condition. The ESD robustness of the PMOS-triggered SCR can be higher than 5.5 kV with a device width of as small as 50 μm. Therefore, such initial-on SCR devices can achieve the whole-chip ESD protection scheme for input, output, power-rail ESD clamp circuit, and the ESD clamp cells between the separated power domains.

In Chapter 5, the device characteristics of SCR devices with different embedded MOS transistors have been compared and investigated. The turn-on efficiency, such as Vt1, Vh, and Ron, of the MOS-triggered SCR devices is decreased by decreasing the channel lengths in the embedded MOS transistors. But, the It2 and ESD robustness of the MOS-triggered SCR devices are increased by increasing the channel lengths, especially in the PMOS-triggered SCR devices. In addition, the merged layout style of the embedded MOS transistor can obviously improve It2 and ESD robustness of the MOS-triggered SCR devices. Moreover, the obvious differences on the Vh of NMOS-triggered SCR devices under DC and TLP measurements have been attributed to the current distributions through the parasitic npn bipolar transistor in the SCR device.

Chapter 6 investigates different ESD protection schemes for the analog input/output cells to find the optimal analog ESD protection design for deep-submicron CMOS technology. According to the experimental results, the GGNMOS was not a suitable ESD protection

device for analog I/O cells in deep-submicron CMOS process, such as 0.18-μm and below. The pure-diode ESD protection device between the pad to VDD (VSS) would be an optimal design for the analog I/O pins. In addition, the gate-driven NMOS for power-rail ESD clamp circuit also performs a higher ESD robustness for analog I/O pins in deep-submicron CMOS technology with STI structure. Finally, layout optimization with a wider spacing between N+/PW diode and N+/NW guard ring, as well as improvement on the power-rail ESD clamp circuit with higher turn-on efficiency, should be used to avoid the unexpected ESD failure under ND-mode ESD stress in such analog I/O cells.

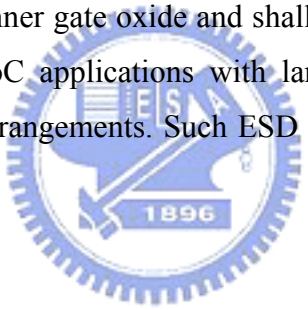
The cross-power-domain ESD issues in IC products are presented in Chapter 7. Due to the circuit performance considerations, the IC product has two separated power domains to cause ESD failures in interface circuits between different power domains. MM ESD currents are discharged through some unexpected paths in the interface circuits during ND-mode ESD stress. Each failure mechanism of Pin-A and Pin-B has been clearly analyzed and illustrated by the failure spot images and ESD current discharge paths. The effective solutions have been proposed to overcome abnormal internal ESD damage by means of adding the blocking resistors to the interface devices and installing the suitable bi-directional diode connection cells between the separated power lines. The optimum modifications have been proven in the new version IC product to sustain MM ESD level of greater than 200V. Besides, the cross-power-domain ESD protection designs with resistor-diode clamp, the special driver and receiver, or the GCT NMOS transistor have been reviewed to compare the ESD protection schemes for interface circuits between separated power domains. Moreover, one new active ESD protection design with gate-controlled PMOS and NMOS transistors has been proposed and successfully verified to sustain 4-kV HBM and 400-V MM ESD stresses in a 0.13-μm 1.2-V CMOS technology. The source pumping mechanism was also proven to significantly enhance the ESD robustness under the cross-power-domain ESD stresses. Finally, the failure mechanisms of three different cross-power-domain ESD protection designs, which were diodes, GCT NMOS, GC-PMOS, and GC-NMOS transistors, have been distinctly illustrated according to the related ESD failure locations and discharge paths.

8.2. Future Works

In advanced nanoscale CMOS technology, the efficient design for power-rail ESD clamp circuit has been proposed and verified in this dissertation. However, leakage issues of power-rail ESD clamp circuit become much severe for the low-power and portable

applications. As mentioned in Chapter 3, utilizing metal-oxide-metal (MOM) capacitor to replace the conventional MOS capacitor is a feasible method. Furthermore, the SCR devices can also prevent the extra leakage current induced by the main ESD clamp NMOS transistor with huge device dimension. To achieve successful ESD protection design for low power application, power-rail ESD clamp circuit with low leakage design methodology is necessary in the future.

With the evolution of CMOS technology, the operation frequency and transmission rate is significantly increased in specific integrated circuits. For analog I/O interface circuit, the parasitic capacitance of ESD clamp devices is a limitation, especially in high-speed I/O interface circuit. On the other hand, the parasitic capacitance of cross-power-domain ESD clamp devices also degrades the data transmission between separated power domains. Thus, developing ESD protection designs with low capacitance for high-speed analog I/O and cross-power-domain interface circuits are promising in the future. Moreover, the on-chip ESD protection designs for charged-device model (CDM) events [75], [76] will be another strict task to protect the much thinner gate oxide and shallower junction in nanoscale CMOS technology, especially for the SoC applications with larger chip area and more complex consideration of power domain arrangements. Such ESD related topics will be the continual future works for research.



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Design Optimization and Failure Analysis of On-Chip ESD Protection in CMOS Integrated Circuits

Publication List

(A) Referred Journal Papers:

[1] **Shih-Hung Chen** and M.-D. Ker, "Investigation on seal-ring rules for IC product reliability in 0.25-μm CMOS technology," *Journal of Microelectronics Reliability*, vol. 45, no. 9-11, pp. 1311–1316, Sep.-Nov. 2005.

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