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電子工程學系 電子研究所

博士論文

具備新穎自我對準升高式源/汲極結構之低溫複晶矽薄膜電晶體元件之開發與寬通道效應之研究

Development of Novel Self-Aligned Raised Source/Drain Structure for Low-Temperature Polysilicon Thin-Film Transistor and the Study of the Channel Width Widening Effect

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中華民國九十七年二月

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中文摘要

在這篇論文中我們專注於新的低溫複晶矽薄膜電晶體結構開發，並針對當通道寬度大於源汲極寬度時，寬通道效應所造成的電流增加做研究與討論。

首先，我們利用傳統熟知之金屬鑲嵌與化學機械研磨技術，用以開發出新穎之具備自我對準之閘極與增高式源汲極結構之低溫複晶矽薄膜電晶體元件，在此一結構中，鄰近源/汲極區之通道厚度將增厚，此一特徵將可有效降低元件關閉時汲極區附近之側向電場，可使此一結構之漏電流相較於傳統共平面結構至少降低十倍以上。我們更利用 2-D 模擬軟體進一步討論與研究側向電場在不同之通道深度處之數值變化。

接著，我們利用一次蝕刻或過蝕刻方式製作另一具有自我對準之增高式源汲極結構的低溫複晶矽薄膜電晶體元件。，此一結構相較於傳統增高式源汲極結構製作流程而言，可減少一次微影製程，並且製作更簡單。此外，由於利用閘極區域定義之光阻層作為下層通道區域定義之蝕刻阻擋層，因而此結構之通道寬度將與閘極區域寬度等寬，並大於源汲極區域之寬度。該特徵將可使此一新穎結構除了具有與先前開發之增高式源汲極結構相同低的漏電流外，更可提升薄膜電晶體之驅動電流與增加開關電流比。

最後，我們特別針對在通道寬度大於源汲極寬度之條件下薄膜電晶體驅動電流進行研究。由於現有之金氧半場效電晶體或複晶矽薄膜電晶體之驅動電流物理模型乃是建立在通道寬度與源汲極寬度等寬之前提條件，因而利用現行之驅動電流模型，我們並無法解釋薄膜電晶體之驅動電流在通道寬度大於源汲極寬度時的導通行為並進行預估驅動電流數值。因此，我們利用一具有通道寬度大於源汲極寬度特性之測試結構，進行薄膜電晶體之驅動電流的研究，並提出一簡單的關係式，解釋驅動電流與通道長度、通道寬度與源汲極寬度間之關聯性。

Development of Novel Self-Aligned Raised Source/Drain Structure for Low-Temperature Polysilicon Thin-Film Transistor and the Study of the Channel Width Widening Effect

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Abstract

In this thesis, we concentrate our efforts on new Low-temperature Poly-Si TFT structure development, and discuss the effect of channel width widening on a Poly-Si TFT which will occur when the channel width is larger than the source/drain width.

First, we apply the damascene process and Chemical Mechanical Polish (CMP) Technology to develop a novel TFT structure with a self-aligned gate and raised source/drain (SAGRSD). In this structure, thick channel regions will be formed near the source/drain regions, this feature will suppress the lateral electric field near the drain region to reduce the OFF-state leakage current of the Poly-Si TFT at least one order of magnitude as comparing to the conventional co-planar Poly-Si TFT. We also used 2-D simulation tool, MEDICI, to verify that the lateral electric field near the

drain region will be reduced by using this novel TFT structure, and discussed the lateral electric field in different channel depth in thick channel region near the source/drain regions.

Secondly, we also develop another new low-temperature Poly-Si TFT structure with self-aligned raised source/drain (SARSD) by one-step etching or over-etching method. For this new structure, thick source/drain regions and a thin channel region could be achieved with only four mask steps, which are less than that in conventional raised SD TFT’s. Moreover, the channel width of the proposed structure would be larger than its source/drain width. Wide channel width will improve the ON-state current due to carrier will flow from the source to the drain via new current flow paths occurred in the side channel region. Therefore, this structure will have the ON-state current and the ON/OFF current ratio of the Poly-Si TFT, and maintain low OFF-state leakage current as same as SAGRSD TFT.

Finally, we also find that current physical models for MOS or Poly-Si drain current are not suitable to explain the behavior of the drain current flow in the channel region of the SARSD TFT in which the channel width is wider than the source/drain width. Therefore, we use a test structure to clarify and define the relationship of the drain current among the channel length, the source/drain width and the channel width when the channel width is wider than the source/drain width.

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Chapter 1

INTRODUCTION

1.1 BACKGROUND AND MOTIVATION

In recent years, the broad band networks have been expanding, and mobile information and communication tools have been widely used. The flat panel display (FPD) which acts as a critical interface to connect with people is assembled into those mobile tools, such as cellular phones, personal digital assistants (PDA), digital cameras, notebook PCs, and so on [1.1]. Therefore, the FPD plays an important role in human life. Up to now, the FPD has been replacing the cathode ray tube (CRT) based traditional display. Meanwhile, the current FPD market has been dominated by amorphous silicon thin-film transistors (α-Si TFTs) based active matrix liquid crystal display (AMLCD) [1.2]. However, α-Si TFTs have a low carrier mobility to limit the signal response time, and are with a large and dark area on a panel to limit the resolution. They inherently limit the performance of active matrix displays. In order to overcome these disadvantages, many techniques on low-temperature polycrystalline silicon thin file transistors (LTPS-TFTs) have been proposed to replace α-Si TFTs. LTPS TFTs integrated peripheral driver circuits with AMLCDs have been widely used [1.3], [1.4]. And an average of their carrier mobility is more than one hundred times the mobility of α-Si TFTs. This technology is being considered as the candidate to achieve a system on panel (SOP) and ultimately sheet computer in the future [1.5], [1.6].

Many technologies for fabricating the high-performance LTPS-TFTs have been extensively investigated, such as methods of α-Si crystallization, defect reduction, and novel TFT structure fabrication.

α-Si crystallization means that an amorphous silicon layer is crystallized into a polycrystalline silicon layer by annealing. The α-Si crystallization is the most important step in the fabrication of LTPS-TFTs. This step is the key process of limiting the thermal budget on large area glass substrates. The performance of LTPS-TFTs is strong dependent on the quality of an active layer. The solid phase crystallization (SPC) [1.7] ~[1.9], metal induced crystallization (MIC) [1.10] ~[1.12], and excimer-laser crystallization (ELC) [1.13] ~[1.15] are the main methods in the fabrication of LTPS-TFTs.

However, whether α-Si films are crystallized by solid phase crystallization (SPC) or by excimer-laser crystallization (ELC), it is hard to avoid existences of grain boundaries in the channel regions for large dimension device. Moreover, existences of grain boundaries and high drain electric field will cause an increase in the leakage current, a variation in the threshold voltage with the drain bias, a kink effect in the output characteristics, and a poor hot-carrier stress endurance [1.16]. These effects can be eliminated by reducing the electric field near the drain region. Therefore, many novel structures are developed to reduce the electric field. For example, the field-induced drain [1.17] ~[1.20], sub-gate coupling structure [1.21] ~[1.24], dual gate structure

[1.25], double-gate structure [1.26] ~[1.28] and lightly-doped drain structure [1.29] ~[1.35]. Unfortunately, most of these structures usually need complicated processes, causing a barrier for being fabricated on a large area glass structure. Therefore, how to simplify the fabrication of high-performance poly-Si TFTs is the most important issue in LTPS TFT-based active matrix displays [1.36].

The well-know El-Mansy/Ko model [1.37] and [1.38] describes the maximum channel electric field for the bulk MOSFET's as

$$E_{\max}=(V_{DS}-V_{Dsat})/l \tag{1.1}$$

Where the characteristic length l is given as

$$l=\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}x_{j}} \tag{1.2}$$

and ε_{si} and ε_{ox} are the permittivity for Si and SiO$_2$, respectively; t_{ox} is the gate oxide thickness, and x_j is the drain junction depth. Hence, it can be concluded that for a given oxide thickness, the $E_{\max}$ can be reduced by increasing the junction depth.

Therefore, increasing the drain junction depth is one way of reducing electric field near the drain side. For the conventional co-planar TFT, increasing the channel thickness could increase drain junction depth at the same time. However, it has been reported that increasing channel thickness will not only increase grain-boundary traps, but also reduce the ON-state current and increase OFF-state leakage current, as shown in Fig. 1-1 and 1-2. Therefore, we hope to develop a novel TFT structure, as shown in Fig. 1-3, to suppress the maximum channel electric field by increasing the junction depth.

1.2 THESIS ORGANIZATION

In this thesis, we concentrate our efforts on new TFT structure development, and discuss the effect of channel wide widening on a Poly-Si TFT which will occur when the channel width is larger than the source/drain width.

Chapter 1 describes the background and motivation. In chapter 2, we apply the damascene process to develop a novel TFT structure with a self-aligned gate and raised source/drain. 2-D simulation tool, MEDICI, is also used to verify that the electric field near the drain region will be reduced by using this novel TFT structure. In chapter 3, another new TFT structure is proposed. For this new structure, thick source/drain regions and a thin channel region could be achieved with only four mask steps, which are less than that in conventional raised SD TFT's. Moreover, the channel width of the proposed structure would be larger than its source/drain width. Wide channel width will improve the ON-state current due to carrier will flow from the source to the drain via new current flow paths occurred in the side channel region. Therefore, in chapter 4, the effect of channel width widening on a Poly-Si TFT in the linear region are thus studied carefully.

Finally, in chapter 5, a conclusion is given for this thesis, and some future works about this thesis are proposed.

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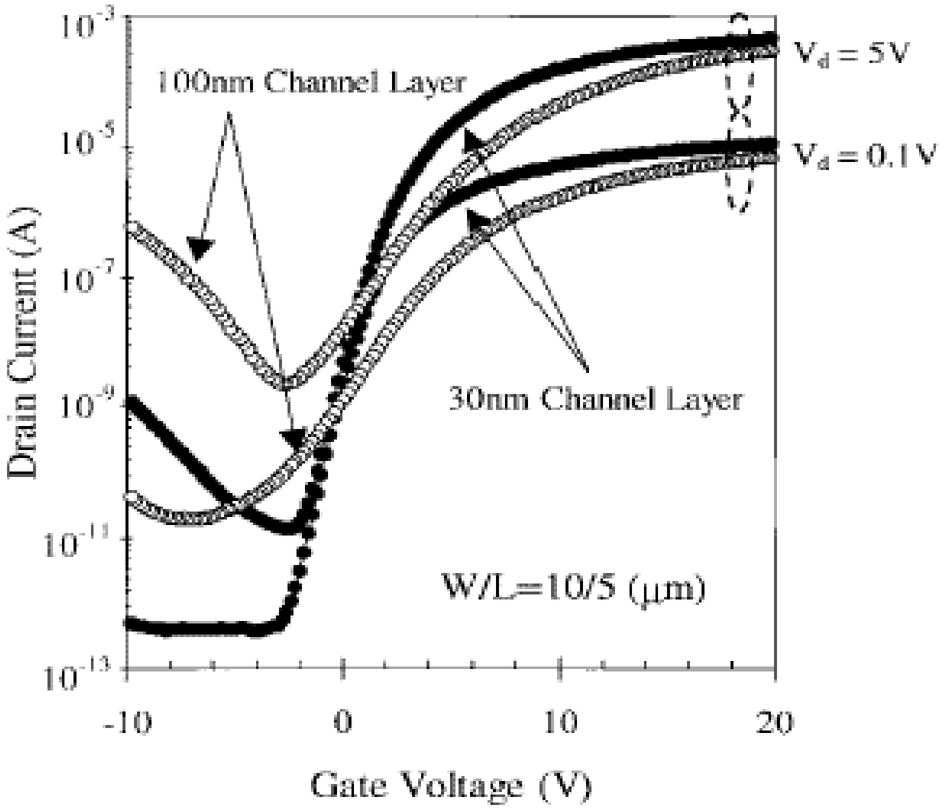

Fig. 1-1 I_{ds} – V_{gs} transfer characteristics of the conventional co-planar TFT with thicker (100nm) and thinner (30nm) channel thicknesses.

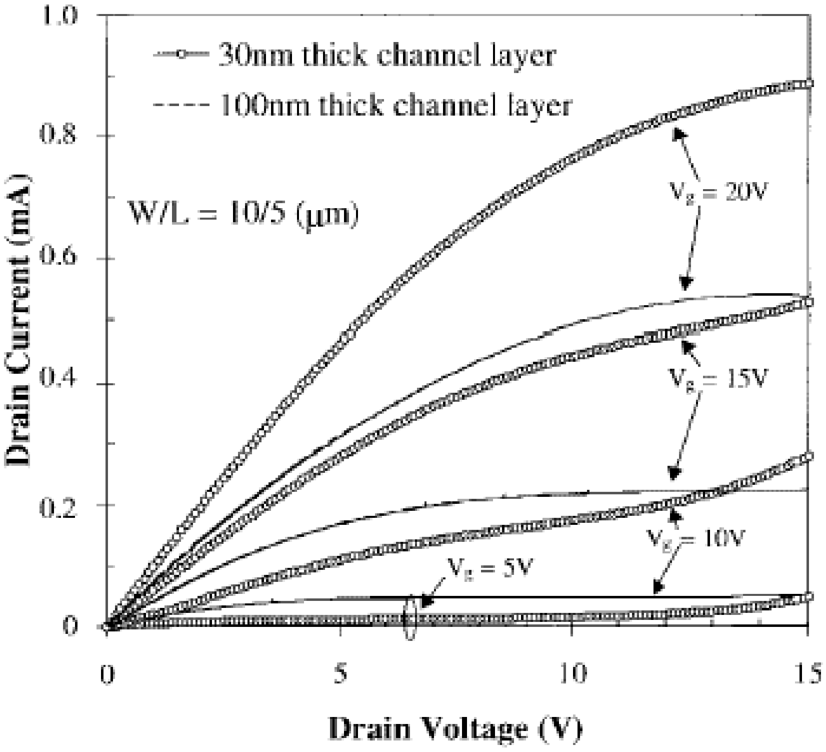

Fig. 1-2 I_{ds} – V_{ds} output characteristics of the conventional co-planar TFT with thicker (100nm) and thinner (30nm) channel thicknesses.

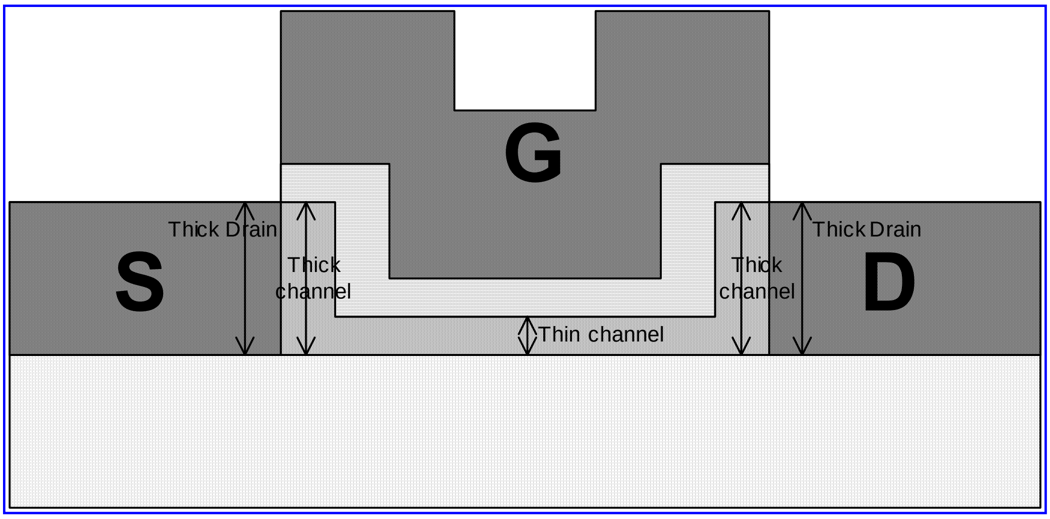

Fig. 1-3 Proposed new RSD TFT structure.

Chapter 2

A Novel Low-Temperature Polysilicon Thin-Film Transistors with a Self-Aligned Gate and Raised Source/Drain Formed by Damascene Process

2.1 INTRODUCTION

Low-temperature polycrystalline silicon (LTPS) TFT's have been widely investigated for several years [2.1]. However, the undesired OFF-state leakage current for a poly-Si TFT is much higher than that of an amorphous TFT. It is well known that the OFF-state leakage current mechanism is the field emission via grain boundary traps due to high electric field in the drain depletion region [2.2]. Thus, suppressing the off-state leakage current by reducing the drain electric field is required. Several methods have been proposed to achieve this purpose, such as offset gated structure [2.3], lightly doped drain structure [2.4] and field induced drain structure [2.5], [2.6]. In the lightly doped offset drain structure, the On-state current is significantly suppressed at the same time [2.7]. In the field induced drain structure, an additional photo masking step is required and unavoidable photo masking misalignment error will occur [2.5], [2.6]. It also has been previously reported that the thick source/drain region not only serves to reduce the lateral electric field, thus maintaining the breakdown voltage [2.8],[2.9], but also to reduce the source/drain series resistance.

Pervious methods used to fabricate such structures with thin active channel and thick source/drain regions, however, are not self-aligned in nature, and require additional masks [2.8],[2.9], when compared to the conventional co-planar TFTs.

In this chapter, a novel four mask steps self-aligned gate RSD Poly-Si TFT structure formed by the damascene process (D-SAGRSD TFT) is proposed. The new device features a thin active channel region and a thick source/drain region. The Gate and RSD regions are self-aligned and no additional mask is needed. Moreover, we use the 2-D numerical simulator MEDICI for device analysis to study the variation of the lateral electric field influenced by device structure in both ON-state and OFF-state. For the sake of simplicity, the single crystalline silicon model already available in MEDICI is used to just estimate the electric field effects of these two Poly-Si TFT structures.

2.2 DEVICE FABRICATION

Fig. 2-1 shows the process flow of the D-SAGRSD TFT structure. First, a 300-nm α-Si layer for active region was deposited by low pressure chemical vapor deposition (LPCVD) system using SiH_4 at 550°C on 500-nm thermal oxidized silicon wafers. After patterning, the active region was formed using reactive ion etching (RIE) at this mask step. Then, the first (650-nm) plasma enhanced chemical vapor deposition (PECVD) tetraethoxysilane (TEOS) oxide layer was deposited at 350 °C.

Chemical-mechanical polishing (CMP) process was employed to planarize the first TEOS oxide surface, as shown in Fig. 2-1(a). The thickness of the first TEOS oxide above the active region after polishing is about 300-nm. After patterning, the RIE process was used to etch the α-Si layer and then selective BOE etching was used to form a T-sharp gutter, as shown in Fig. 2-1(b). Because the α-Si layer had no stopper layer, the α-Si thin channel region thickness was controlled by etching rate (8.33 Å/sec). Additionally, the α-Si film thickness was determined by Ellipsometer, and the thickness of the thin channel region was accurately controlled, with an error of within ±3% (50 ± 1.5 nm). After etching, the thickness of the active region became 50-nm. After the photoresist was removed, the α-Si film was annealed in nitrogen ambient at 600°C for 24 h to become the poly-Si film. After recrystallization, the etching damages of the channel surface were recovered and the surface roughness is approximately 3 nm. A 50-nm plasma enhanced chemical vapor deposition (PECVD) TEOS gate oxide layer was deposited at 350 °C, and then a 300-nm LPCVD Poly-Si film was deposited. After CMP process was employed to planarize the Poly-Si film surface to form the T-sharp gate as shown in Fig. 2-1(c), the 50-nm TEOS gate oxide and the first TEOS oxide were removed by BOE solution. Then, Gate, Source and Drain regions were formed by ion implantation of Phosphorous (Dose = 5×10^{15} cm^{-2} at 50 keV) and then activated in nitrogen ambient at 600 °C for 24 h, as shown in Fig. 2-1(d). After the source, drain and gate activation, the second (500-nm) passivation TEOS oxide was deposited by PECVD. Contact holes were opened using wet etching of the passivation oxide layer. A layer of aluminum was then deposited by thermal coater system with a thickness of 600 nm. After metal patterning, a forming gas anneal is performed at 400°C for 30 min. The total masks of our fabrication processes are four masks, which are less than those of conventional processes in a RSD poly-Si TFT [2.8],[2.9]. For comparison, the conventional co-planar poly-Si TFTs with 50-nm channel thickness were also fabricated in the same run. The total channel length of the proposed TFT is shown in Fig. 2-2.

2.3 RESULTS AND DISCUSSION

The I_{ds}-V_{gs} transfer characteristics of the proposed D-SAGRSD TFT structure compared with the conventional co-planar TFT were shown in Fig. 2-3. It can be observed that, even though the D-SAGRSD TFT has a slightly lower ON-state current and a slightly higher minimum OFF-state current, much lower OFF-state leakage current (V_{gs} = -10 V and V_{ds} = 5 V) can be also obtained. The proposed TFT has two symmetrical thick channel regions near source and drain sides. These thick channel regions have much more grain boundary traps than the thin channel region, and these grain boundary traps would cause the ON-state current decreasing and minimum OFF-state current increasing. Besides, as shown in Fig. 2-4(a), the current flow lines of the conventional co-planar TFT in the ON-state are uniform distribution in the inversion layer near the oxide/channel interface. However, for the proposed D-SARSD TFT, even most of the carriers can transport in the inversion layer near the oxide/ Poly-Si interface, some carriers still can directly transport to the drain region in the thick channel region, as shown in Fig. 2-4(b). This phenomenon may be due to the variation of the lateral electric field in the thick channel region near the drain side. Figs. 2-5 and 2-6 show the simulation positions of the lateral electric field of the conventional co-planar TFT and the proposed D-SAGRSD TFT simulated by MEDICI, respectively. The simulation results of the conventional co-planar TFT and the proposed D-SAGRSD TFT are shown in Table 2-1. It can be observed that the maximum lateral electric field of the proposed D-SAGRSD TFT in the point C of Fig. 2-6 is remarkable larger than that of the conventional co-planar TFT in ON-state. Therefore, we can conclude that, for the proposed D-SAGRSD TFT, carriers in the thick channel region can transport to the drain region via the inversion layer near the oxide/ Poly-Si interface, and directly transport to the drain region due to high lateral electric field near the drain side. Moreover, the proposed TFT would have a higher threshold voltage and a larger sub-threshold swing than those of the conventional TFT due to bad channel control in the corners of the channel and bad oxide/Poly-Si interface of the vertical channel region.

For the OFF-state current measured at higher drain and reverse gate bias (V_{ds} = 5 V, V_{gs} = -10 V), the main reason of much lower OFF-state current of the proposed D-SAGRSD TFT is that the leakage current is determined by the electron-hole pair generation rate in the depletion region at the drain edge. The pair generation rate is strongly dependent on the number of trap-states in the forbidden gap, lateral electric field and a generation volume of the depletion region [2.10]-[2.12]. Although a thick drain region causes the generation volume of the D-SAGRSD TFT to increase, the maximum lateral electric field near the drain region of the D-SAGRSD TFT, as shown in Fig. 2-7, is also largely dropped (see Table 2-2) due to thick source/drain regions [2.13]. At higher drain and reverse gate bias (V_{ds} = 5 V, V_{gs} = -15 V), the leakage current would be due to the thermionic field emission via grain boundary defects [2.14]. Even though the generation volume would be increased, the D-SAGRSD TFT, therefore, would have a lower OFF-state leakage current than that of the conventional TFT because the maximum lateral electric field near the drain region is notably reduced. Fig. 2-8 shows the I_{ds} - V_{ds} curves of the proposed TFT compared with the conventional TFT. In the insert plots, it can be observed that the proposed TFT has a lower source/drain parasitic resistance due to steeper slopes of I_{ds} - V_{ds} of the proposed TFT in the linear region. However, in the saturation region, the ON-state current of the proposed TFT is lower than that of the conventional TFT; it is because the maximum lateral electric field of the proposed TFT is also dropped due to thick source/drain regions (see Table 2-1).

2.4 SUMMARY

In this chapter, a novel four mask steps n-channel self-aligned gate raised source/drain Poly-Si TFT formed by damascene process was proposed and investigated. Remarkable OFF-state current can be obtained and good ON/OFF current ratio can be maintained for the proposed D-SAGRSD TFT. The self-aligned gate and raised source/drain regions can be formed without the additional mask step and therefore reduce the lateral electric field near the drain side to suppress the OFF-state current. This new TFT structure may be an attractive device structure for future high-performance large-area device applications.

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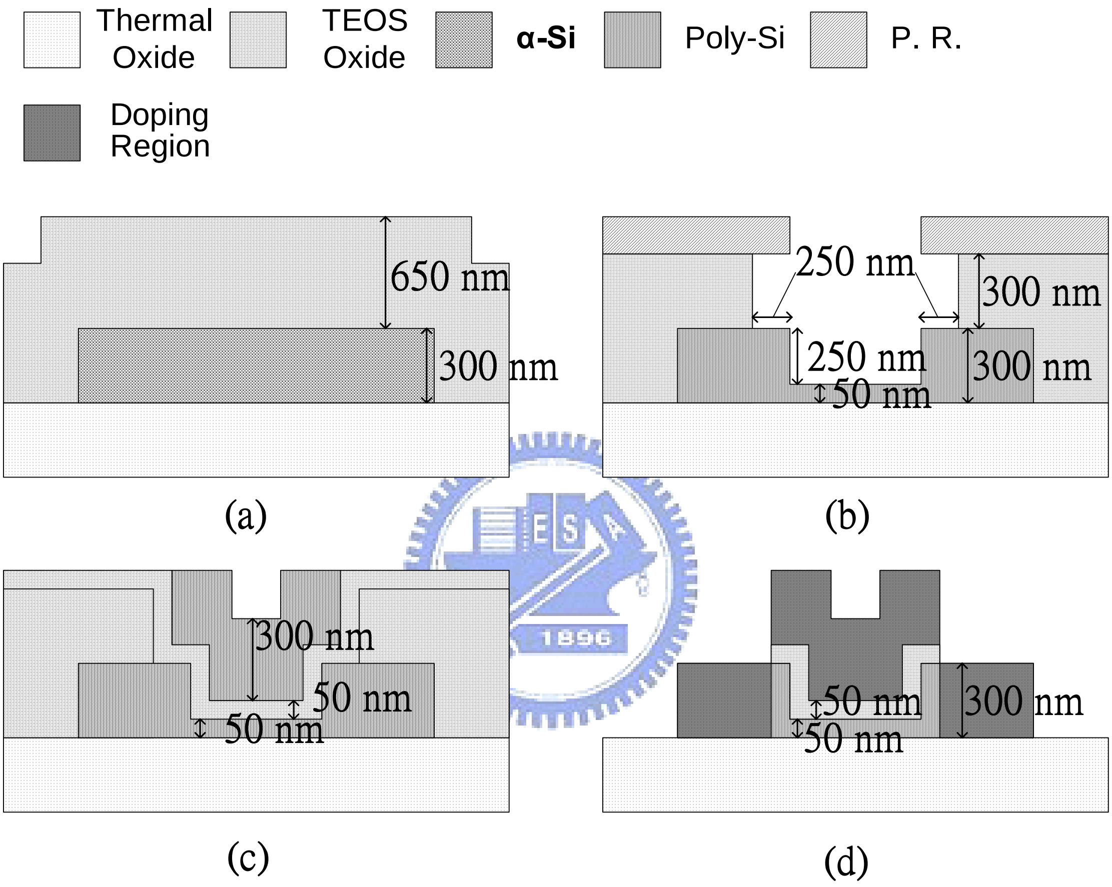


(a) (b) (c) (d)

Fig. 2-1 (a)-(d) Schematic cross sections of the major fabrication steps of the proposed n-channel D-SAGRSD TFT.

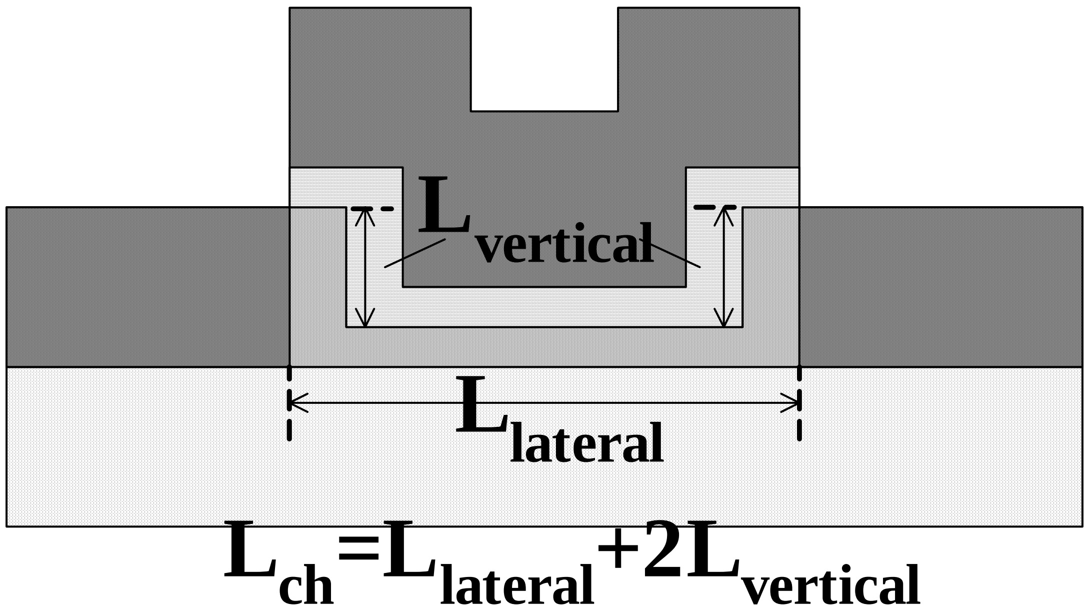


Fig. 2-2 Cross-section view of the proposed D-SAGRSD TFT structure.

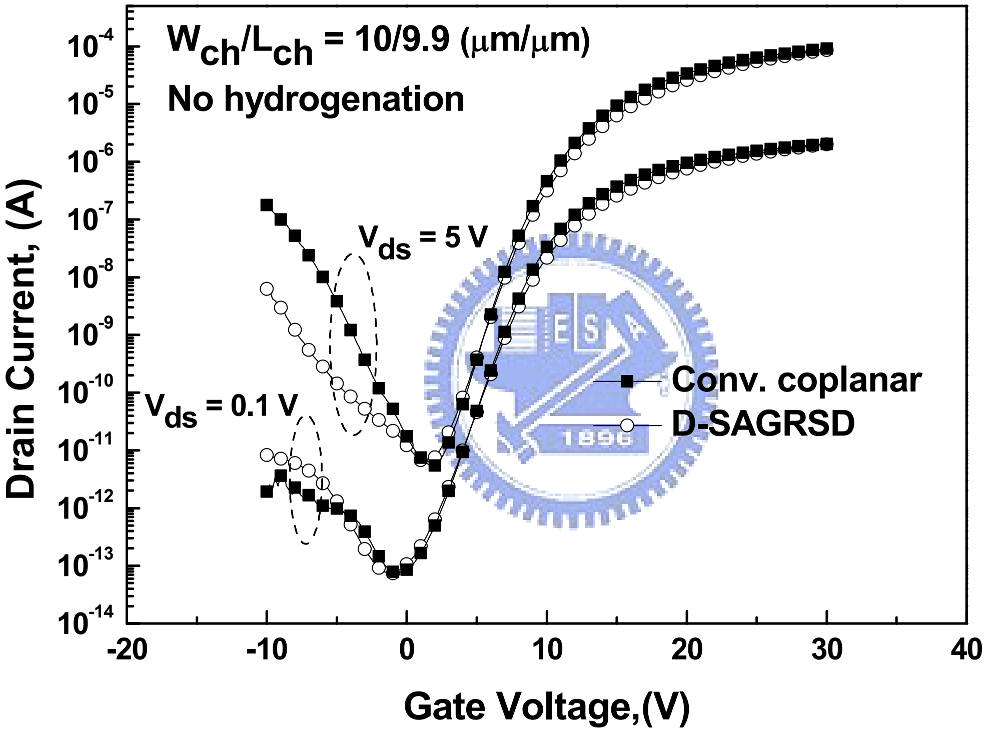
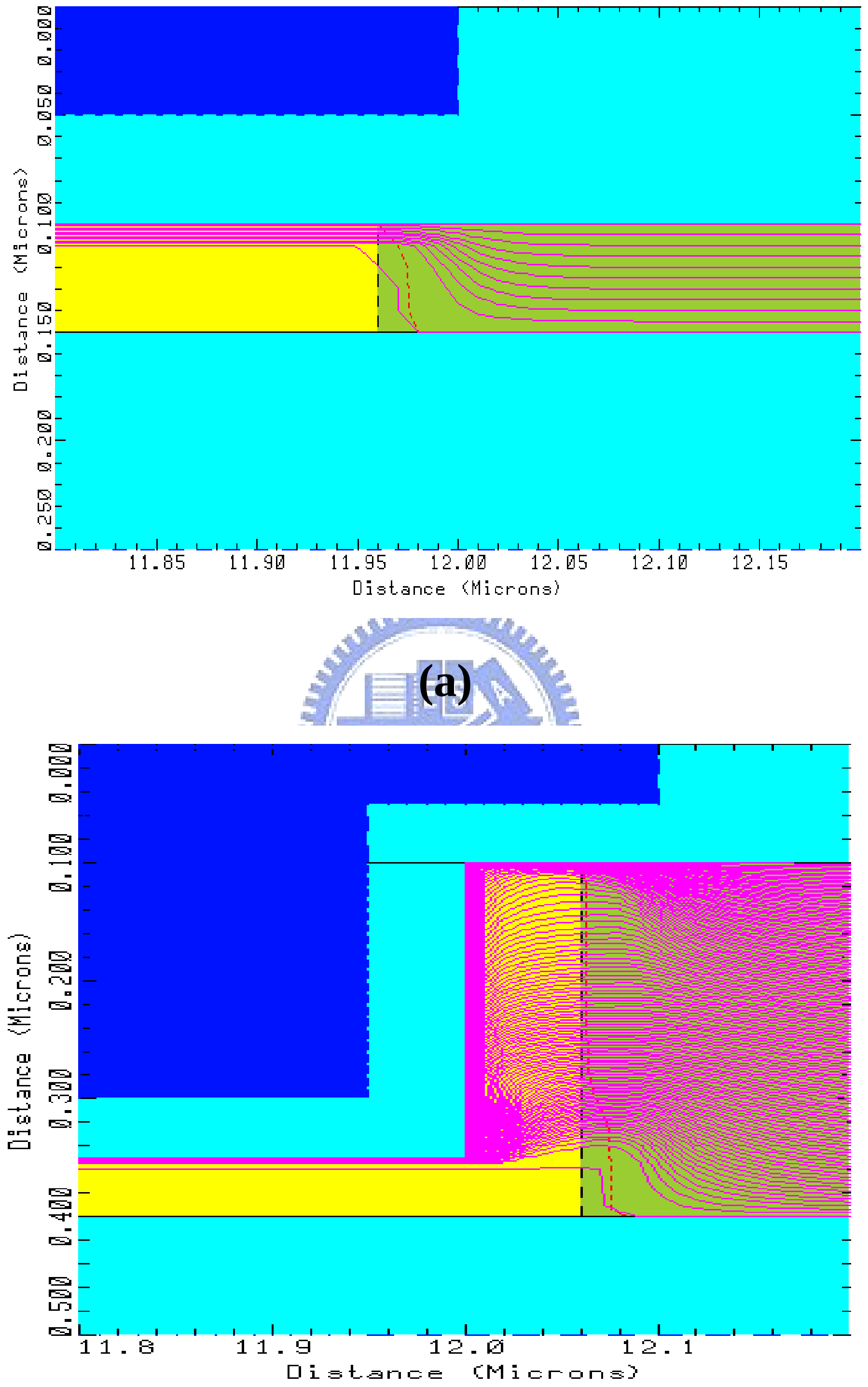


Fig. 2-3 $I_{ds} - V_{gs}$ transfer characteristics of the proposed D-SAGRSD TFT and the conventional co-planar TFT.



(a)

(b)

Fig. 2-4 Simulation current flow lines of (a) the conventional co-planar TFT; (b) the proposed D-SAGRSD TFT.

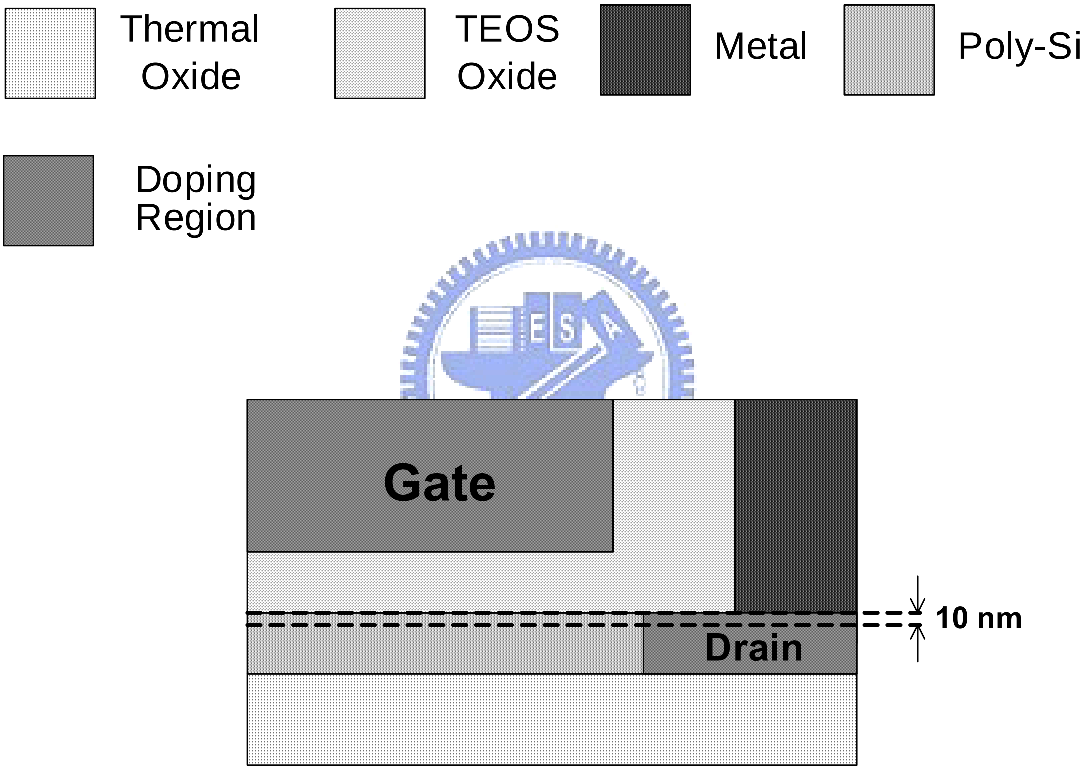


Fig. 2-5 Simulation position of the lateral electric field of the conventional co-planar TFT.

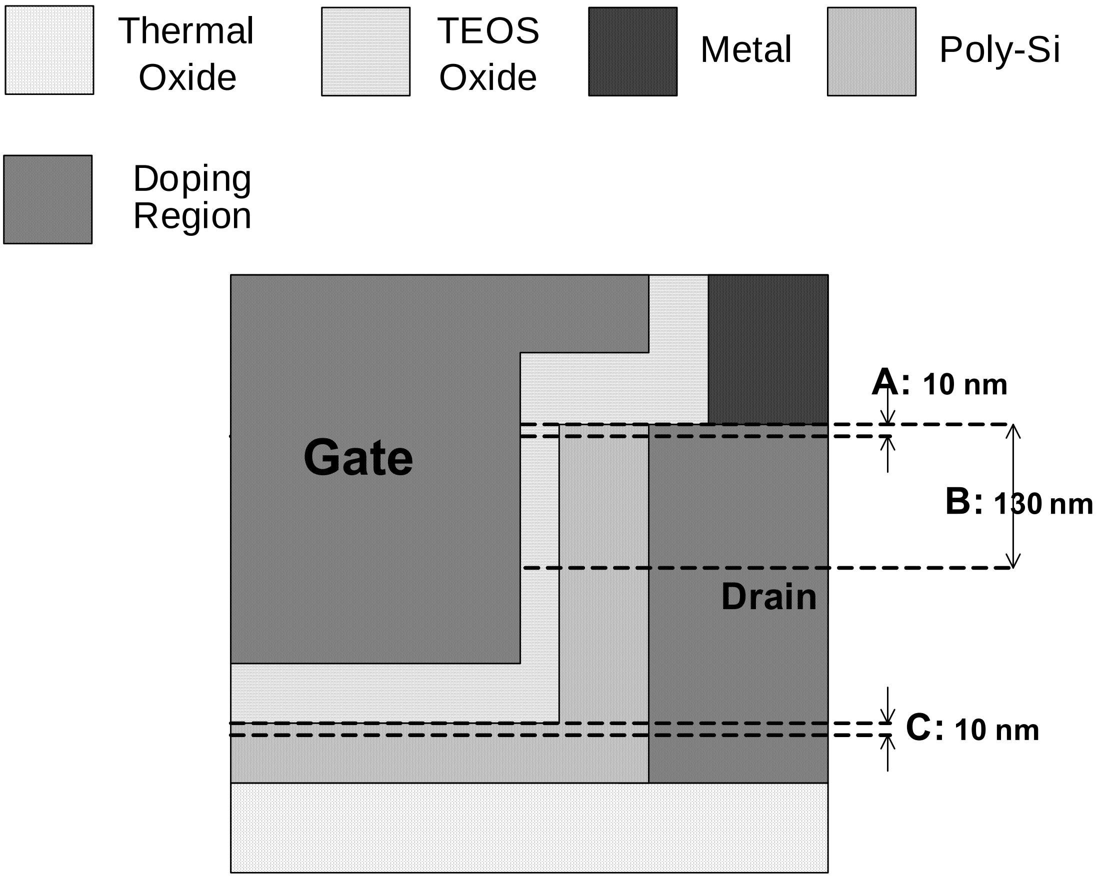


Fig. 2-6 Simulation positions of the lateral electric field of the proposed D-SAGRSD TFT.

Table 2-1 Maximum lateral electric field of the conventional and proposed TFT structures in the ON-state.

ON-state **@V_{gs} = 30 V; V_{ds} = 20 V**	**Conventional co-planar**	**D-SAGRSD A**	**D-SAGRSD B**	**D-SAGRSD C**
Max. Lateral Electric Field (MV/cm)	**0.110**	**0.082**	**0.108**	**0.421**

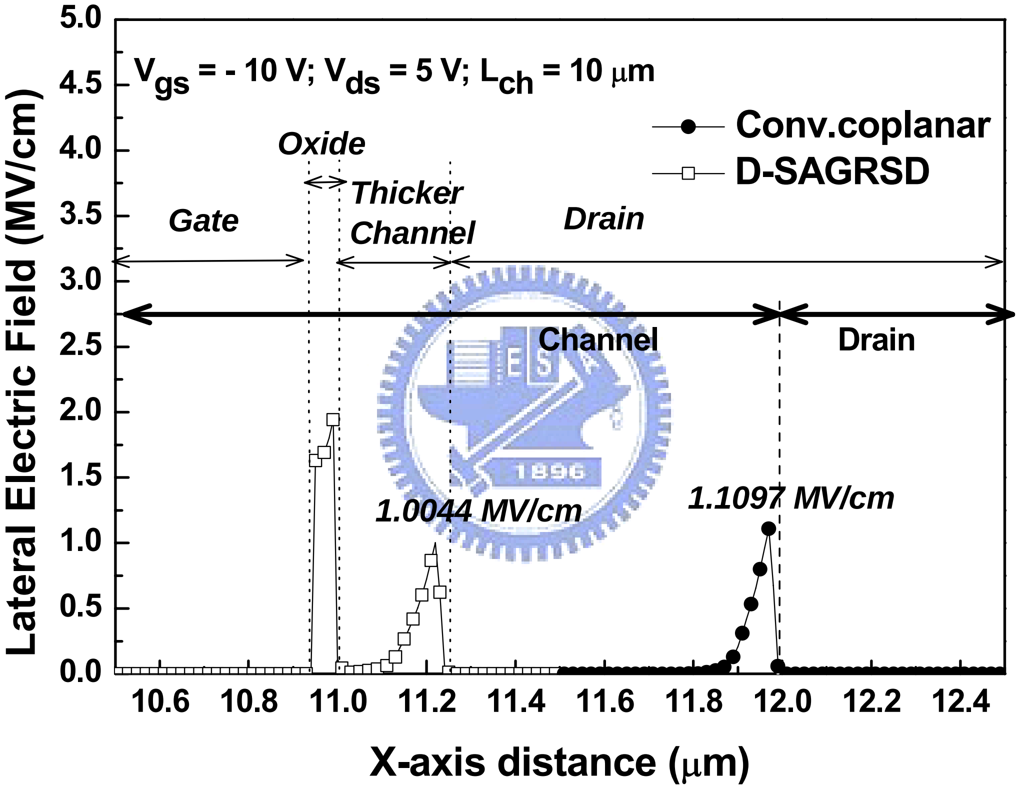


Fig. 2-7 Simulated lateral electric field distribution of the proposed D-SAGRSD TFT and the conventional co-planar TFT in the OFF-state.

Table2-2 Maximum lateral electric field of the conventional and proposed TFT structures in the OFF-state.

OFF-state @V_{gs} = -10 V; V_{ds} = 5 V	**Conventional co-planar**	**D-SAGRSD A**	**D-SAGRSD B**	**D-SAGRSD C**
Max. Lateral Electric Field (MV/cm)	**1.11**	**1.00**	**0.366**	**0.338**

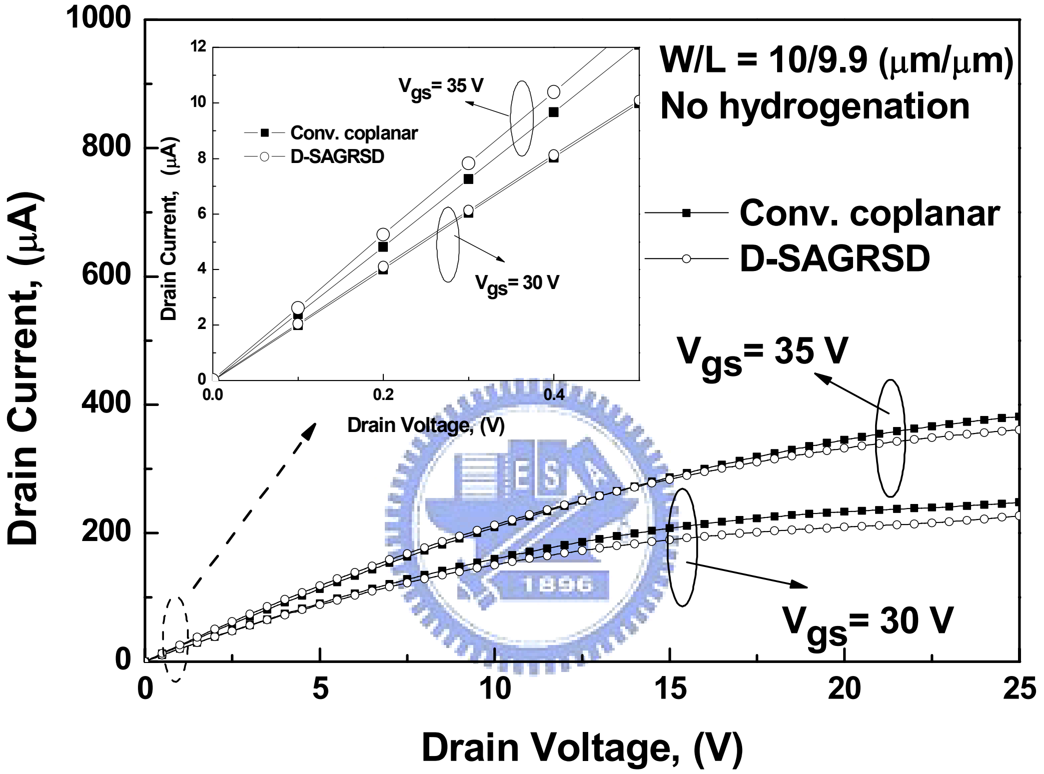


Fig. 2-8 I_{ds} – V_{ds} output characteristics of the proposed D-SAGRSD TFT and the conventional co-planar TFT. The insert plots are the I_{ds} – V_{ds} output characteristics of the proposed D-SAGRSD TFT and the conventional co-planar TFT in the linear region.

Chapter 3

A Novel Four-Mask Step Low-Temperature Polysilicon Thin-Film Transistors with Self-Aligned Raised Source/Drain (SARSD)

3.1. INTRODUCTION

Low-temperature polycrystalline silicon (LTPS) TFTs appear to be one of the most promising technologies for the ultimate goal of building large area electronic systems on glass substrate [3.1]. In flat panel liquid crystal, electroluminescent, and plasma displays, as well as other applications such as high-speed printers and page width optical scanners, poly-Si TFTs can be used to integrate peripheral driver circuits on glass for system integration [3.2]. In order to integrate peripheral driving circuits on the same glass substrate, both a large current drive and a high drain breakdown voltage are necessary for poly-Si TFT device characteristics. It has been previously reported that the use of a thinner active channel film is beneficial for obtaining a higher current drive [3.3],[3.4].The use of thin active channel layer, however, inevitably results in poor source/drain contact and large parasitic series resistance. An ideal TFT device structure, therefore, should consist of a thin active channel region, while maintaining a thick source/drain region. The thick source/drain region serves on not only to reduce the lateral electric field, thus maintaining the breakdown voltage [3.5],[3.6], but to reduce the source/drain series resistance. Pervious methods used to fabricate such ideal structures with thin active channel and thick source/drain region, however, are not self-aligned in nature, and require additional masks [3.5],[3.6], when compared to the conventional co-planar TFTs.

In chapter 2, the D-SAGRSD TFT has been proposed. However, this structure has a slightly low ON-state drain current and a low ON/OFF current ratio, even the OFF-state leakage current can be suppressed. In this chapter, a novel TFT with self-aligned raised source/drain (SARSD) structure is proposed. The new device features a thin, wider active channel region and a thick source/drain region. This new device also has a higher ON-state drain current and a higher ON/OFF current ratio than those of the D-SAGRSD TFT. Moreover, the OFF-state leakage current of the SARSD TFT is as low as that of the D-SAGRSD TFT. The RSD regions of this new device are self-aligned and no additional mask is needed.

3.2. DEVICE FABRICATION

The fabrication processes of the novel n-channel poly-Si SARSD TFT were as follows: A 350-nm thick α-Si layer for active region was deposited by low pressure chemical vapor deposition (LPCVD) system using SiH_4 at 550°C on 500-nm thermal oxidized silicon wafers. After patterning, the thin α-Si (50 nm) regions and the thick α-Si (350 nm) regions were formed using reactive ion etching (RIE) at this mask step, as shown in Fig. 3-1(a). The widths of the thick α-Si (350 nm) regions were 5 μm. Then the deposited α-Si film was annealed in nitrogen ambient at 600°C for 24 h to become the poly-Si film. After recrystallization, the etching damages of the channel surface were recovered and the surface roughness is approximately 3 nm. A 50-nm plasma enhanced chemical vapor deposition (PECVD) gate oxide layer was deposited at 350 °C, and then a 300-nm LPCVD poly-Si gate was deposited. After defined the undoped gate region (gate mask area = L_{ch} x W_{ch}, as shown in Fig. 3-2), the remnant 50-nm oxide film and 50-nm poly-Si film would be further removed using the RIE system to form an isolated active region, as shown in Figs. 3-1(b) and 3-1(c). After the photoresist was removed, Gate, Source and Drain regions were formed by ion implantation of Phosphorous (Dose = 5 x 10^{15} cm^{-2} at 50 keV) and then activated in nitrogen ambient at 600 °C for 24 h, as shown in Fig. 3-1(c). It is worth pointing out that the gate region width (W_{ch}) is larger than that of the source/drain region (W_{sd}). Therefore, a thin and wider active region would be formed below the whole of gate region, as shown in Fig. 3-2. After the source, drain and gate activation, the 500-nm passivation oxide was deposited by PECVD. Contact holes were opened using wet etching of the passivation oxide layer. A layer of aluminum was then deposited by thermal coater system with a thickness of 600 nm. After metal patterning, a forming gas anneal is performed at 400°C for 30 min. The total masks of our fabrication processes are four masks, which are less than those of conventional processes in a RSD poly-Si TFT [3.5],[3.6]. For comparison, the conventional co-planar poly-Si TFTs with 50-nm channel thickness were also fabricated in the same run.

3.3 RESULTS AND DISCUSSION

Fig. 3-3 shows SEM photograph of the proposed SARSD TFT structure. To ensure that current flow of the proposed SARSD structure would be as shown in Fig. 3-2, the 2-D numerical simulator MEDICI was used. Fig. 3-4 shows the simulated current flow lines of the conventional co-planar and proposed SARSD poly-Si TFT structures in ON-state. The channel length and width of the simulated conventional co-planar structure are 15 μm and 5 μm, respectively. From the simulation results in Fig. 3-4(a), the simulated current flow lines of the conventional structure are uniform distribution in the channel region and source/drain regions. However, for the proposed SARSD structure as shown in Fig. 3-4(b), the current flow paths are different from the conventional sample in ON-state. It is because that the channel width is wider than source/drain width, and wide channel width would obtain a high drain current. Therefore, it can be convinced that the proposed RSD structure would obtain a higher drain current than that of conventional co-planar one.

As shown in Fig. 3-5, the proposed SARSD TFT has a higher ON-state current (V_{gs} = 30V) and a lower OFF-state leakage current (V_{gs} = -15V) than those of the conventional TFT. In ON-state, the main reasons of high ON-state current are due to wide channel width (W_{ch} = 33 μm) and small source/drain parasitic resistances [3.6]. On the contrary, in OFF-state, the minimum

OFF-state leakage current of the proposed SARSD TFT is only slightly larger than that of the conventional TFT. It is because that the leakage current is determined by the electron-hole pair generation rate in the depletion region at the drain edge. The pair generation rate is strongly dependent on the number of trap-states in the forbidden gap, lateral electric field and a generation volume of the depletion region [3.7]-[3.9]. Although a thick drain region causes the generation volume of the SARSD TFT (must be approximately W_{sd} x thickness of the depletion region) to increase, the maximum lateral electric field near the drain region of the proposed SARSD TFT is largely dropped from 2.13 MV/cm to 1.57 MV/cm due to thick source/drain region [3.10]. At high drain and reverse gate bias (V_{ds} = 5 V, V_{gs} = -15 V), the leakage current would be due to the thermionic field emission via grain boundary defects [3.11]. Therefore, the proposed SARSD TFT has a lower OFF-state leakage current than that of the conventional TFT because the maximum lateral electric field near the drain region is largely dropped, even though the generation volume would be increased. As shown in Fig. 3-6, the proposed SARSD TFT has a higher saturation current and a lower parasitic resistance than those of the conventional one for different gate bias.

Fig. 3-7 shows the I_{ds} - V_{gs} transfer characteristics of the proposed SARSD TFT with different channel width. Fig. 3-8 shows maximum ON-state current and minimum OFF-state leakage current of the proposed SARSD TFT with various the side channel width, and the conventional co-planar TFT. It is obvious that the ON-state current is increased with increasing the channel width. However, as shown in Fig. 3-8, the minimum OFF-state leakage current is also increased with increasing the channel width. Fig. 3-9 shows the OFF-state leakage current of the proposed SARSD TFT with various the side channel width, and the conventional co-planar TFT measured at V_{gs} = -15 V and V_{ds} = 5 V. In Fig. 3-9, it is obvious that the OFF-state leakage current of the proposed SARSD TFT is significant lower than that of the conventional co-planar TFT for different channel width. Moreover, as shown in Fig. 3-10, the optimum condition of the SARSD TFT for the case of L_{ch} /W_{sd} = 15 μm/ 5 μm is W_{sc} = 2 μm.

3.4. SUMMARY

In this chapter, a novel four mask steps n-channel low-temperature poly-Si TFT with a self-aligned raised source/drain region and a thin channel was proposed and investigated. The gate mask was used to form a large area thin-channel region below the gate region, and the self-aligned raised source/drain region can be formed without the additional mask step. A lower off-sate leakage current and a higher ON/OFF current ratio can be obtained for the proposed SARSD TFT. The TFT fabrication processes are fully compatible with the conventional four-mask ones. This new TFT structure may be an attractive device structure for future high-performance large-area device applications.

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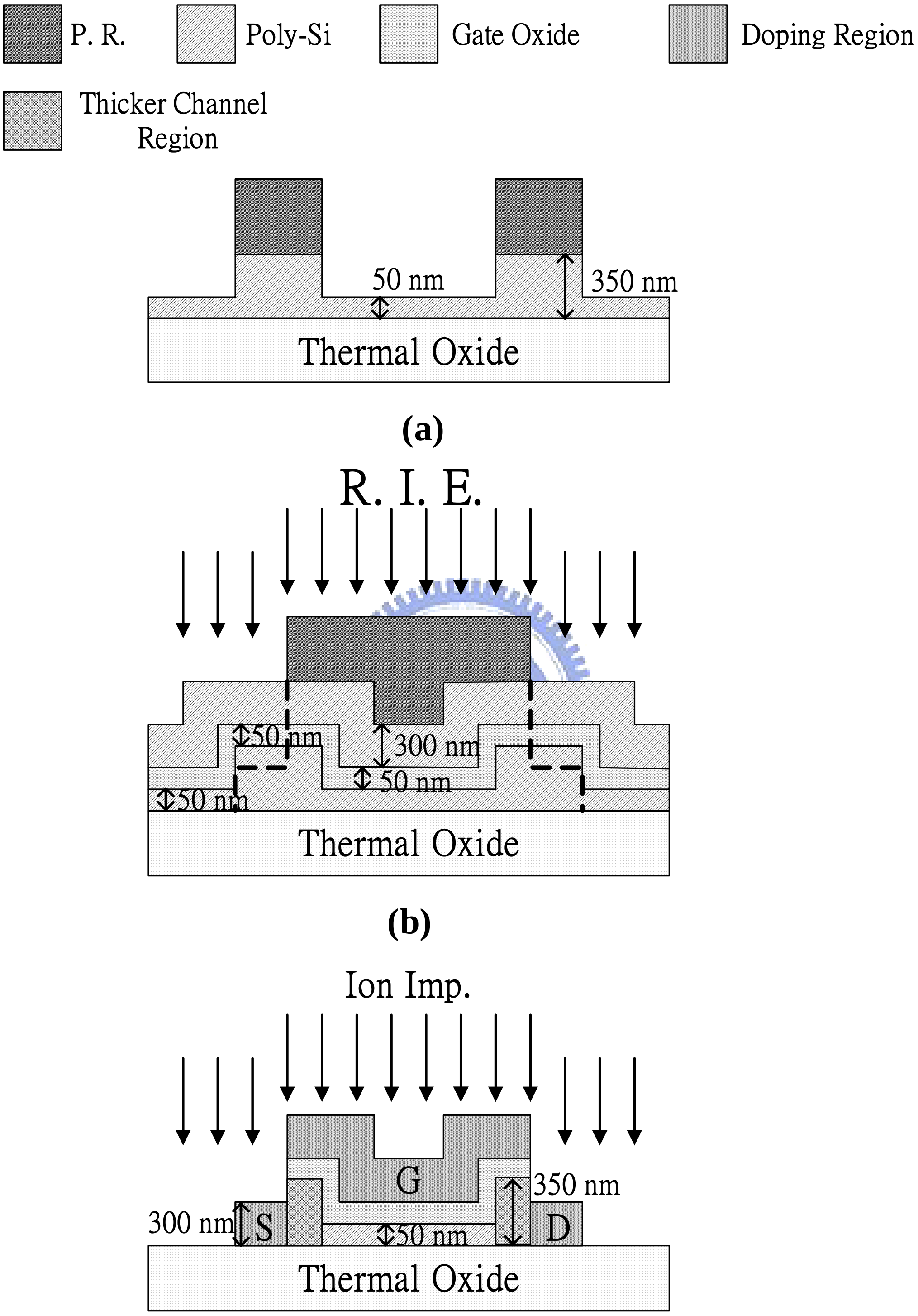

(a)

(b)

(c)

Fig. 3-1 (a)-(c) Schematic cross section of the major fabrication steps of the proposed n-channel SARSD TFT.

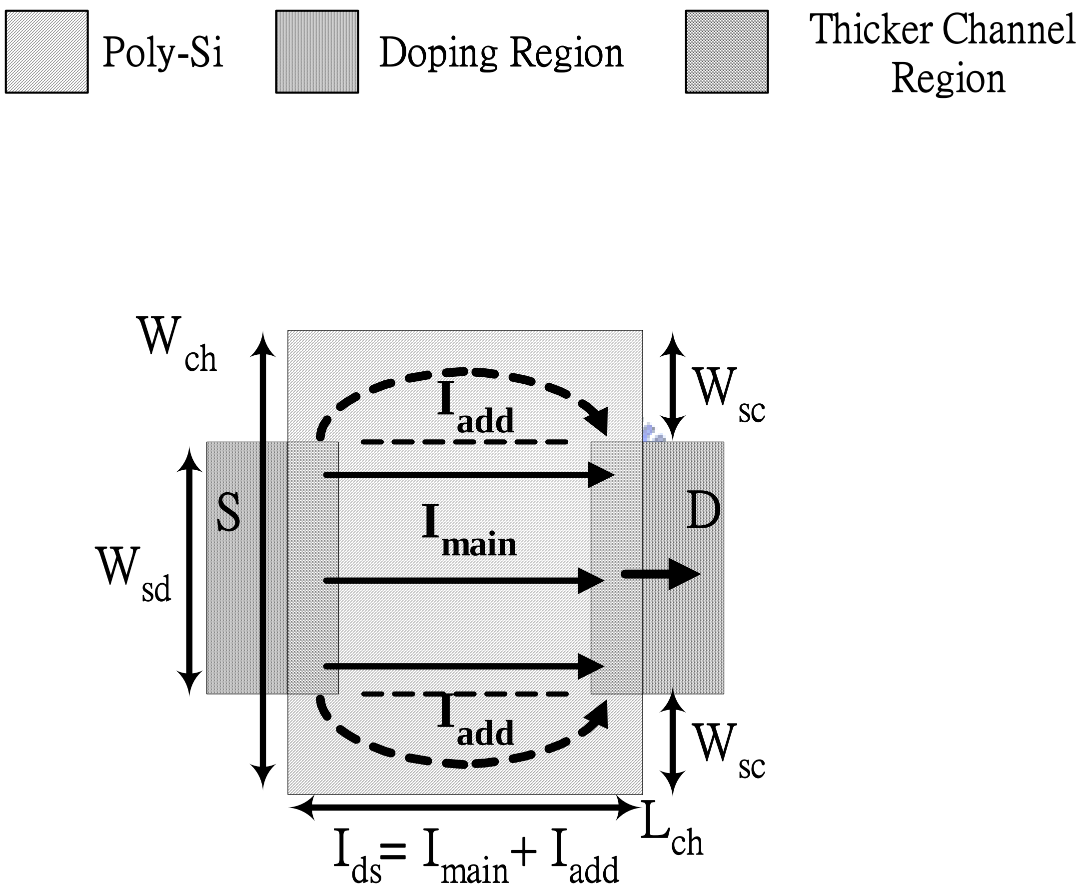

Fig. 3-2 Schematic diagram of the current flow lines of the proposed SARSD structure.

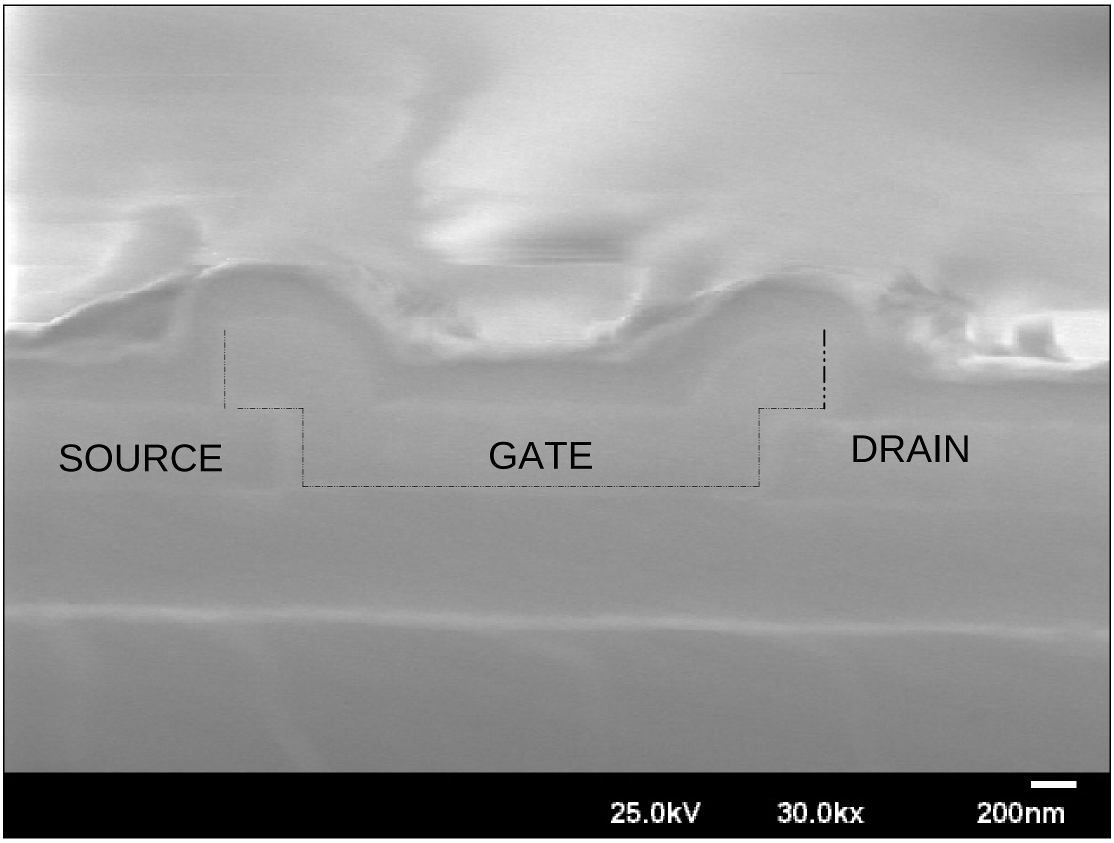

Fig. 3-3 SEM photograph of the proposed SARSD TFT structure.

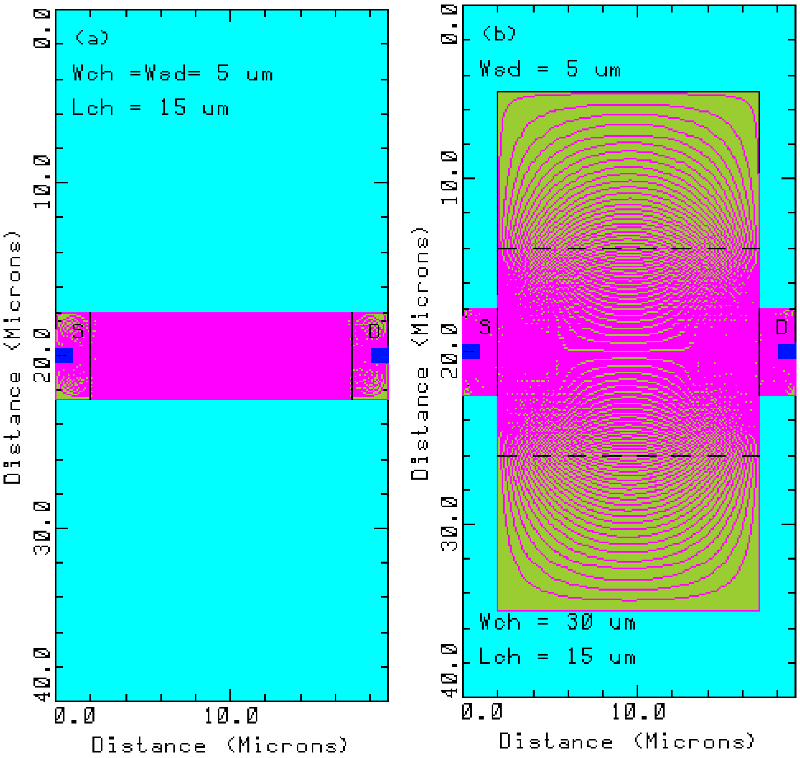

Fig. 3-4 Current flow lines simulated by MEDICI in (a) the conventional co-planar structure with L_{ch} = 15 μm and W_{ch} = W_{sd} = 5 μm; (b) the SARSD structure with L_{ch} = 15 μm, W_{sd} = 5 μm and W_{ch} = 30 μm.

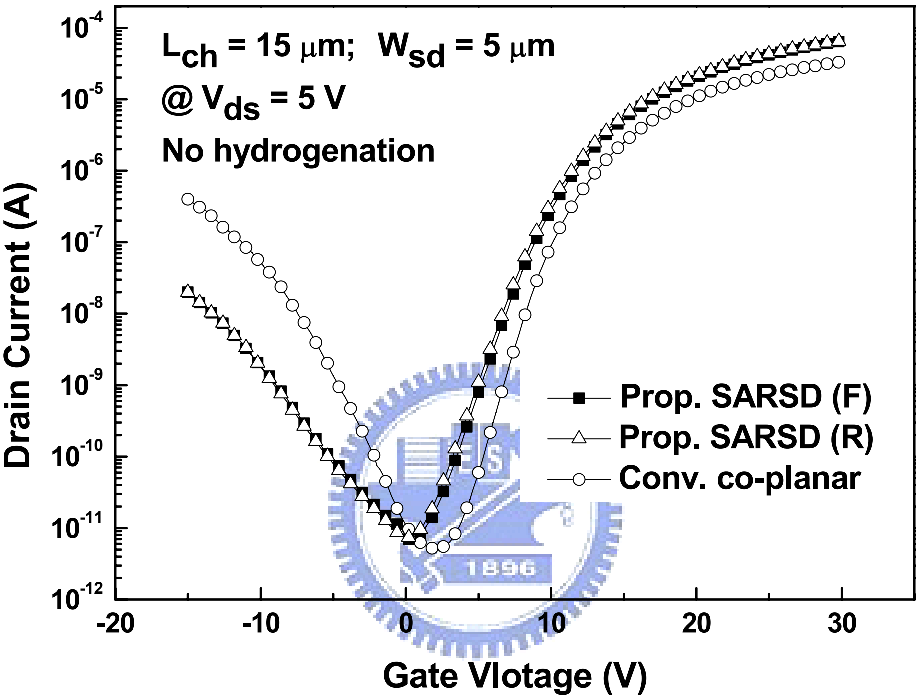

Fig. 3-5 I_{ds}-V_{gs} transfer characteristics of the proposed SARSD TFT in both forward mode (F) and reverse mode (R) and the conventional co-planar TFT, in which the reverse mode is source and drain electrodes exchanged.

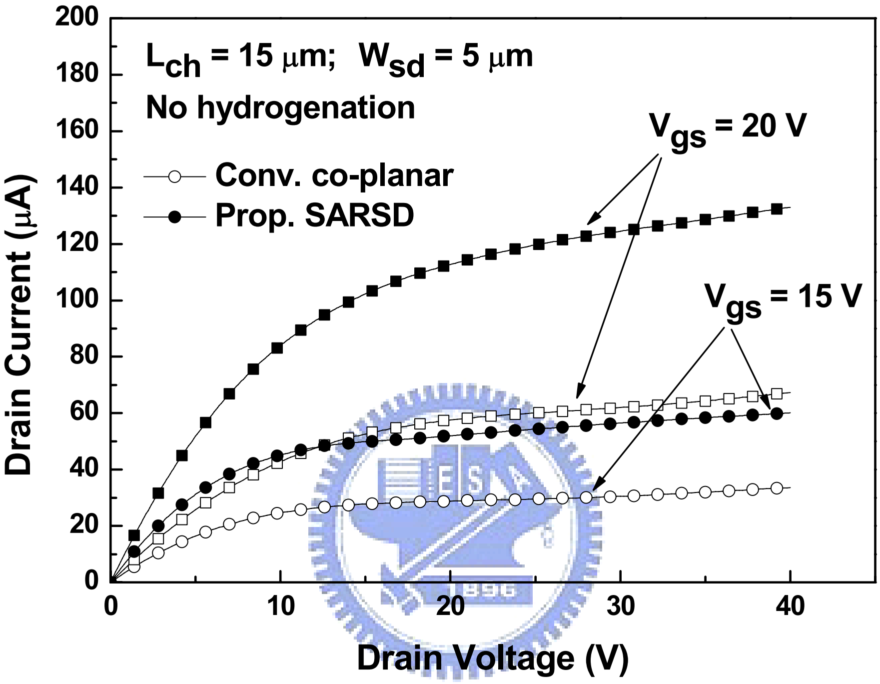

Fig. 3-6 I_{ds}-V_{ds} output characteristics of the proposed SARSD TFT and the conventional co-planar TFT.

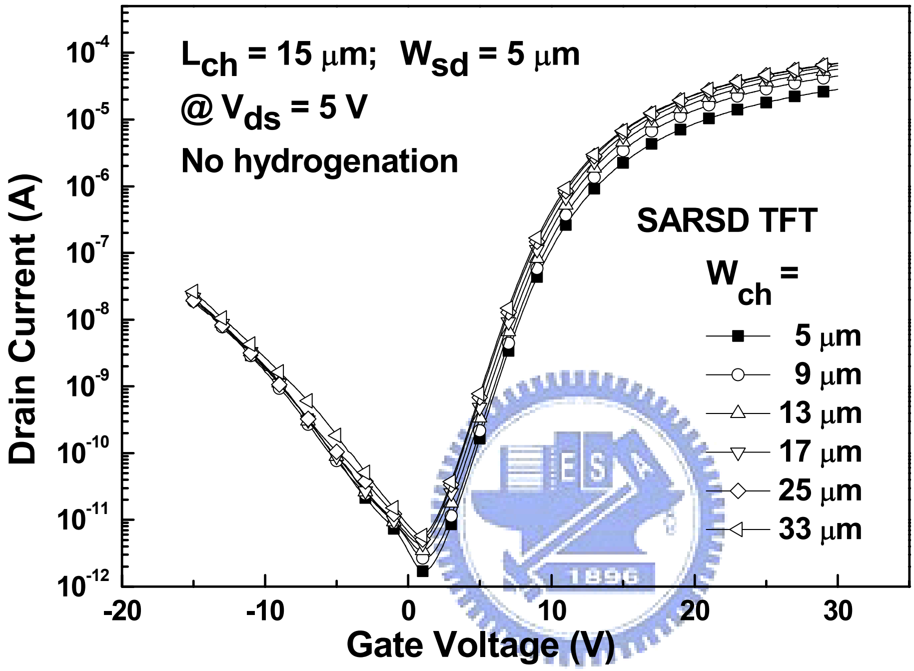

Fig. 3-7 I_{ds}-V_{gs} transfer characteristics of the proposed SARSD TFT with different channel width.

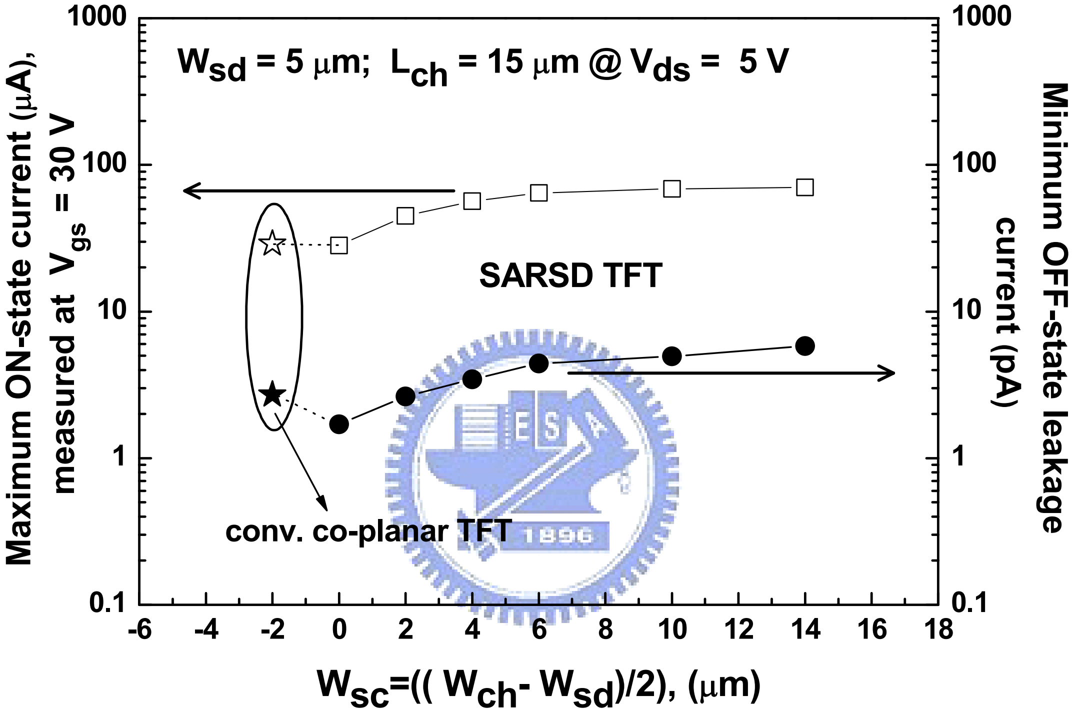

Fig. 3-8 Maximum ON-state current and minimum OFF-state leakage current of the proposed SARSD TFT with various the side channel width, and the conventional co-planar TFT.

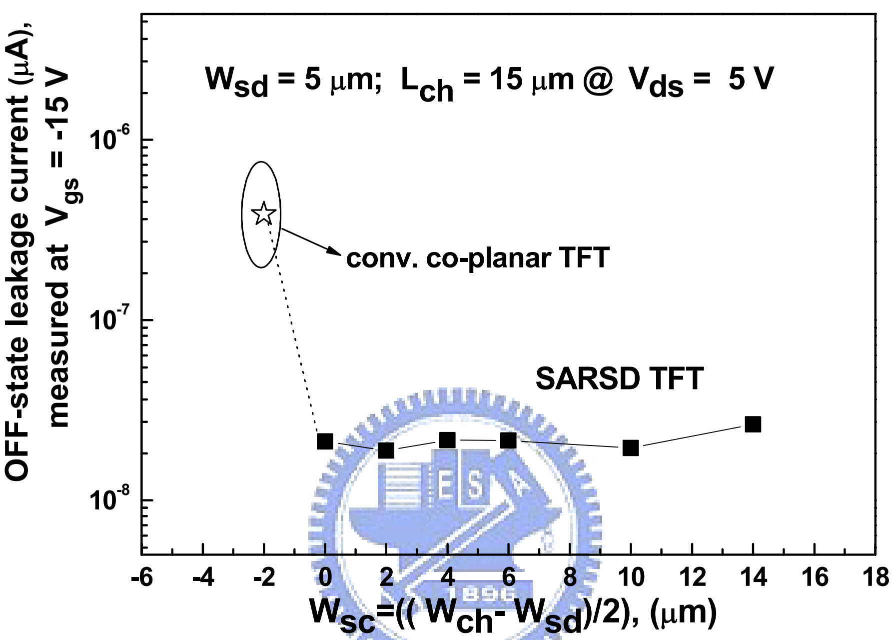

Fig. 3-9 OFF-state leakage current of the proposed SARSD TFT with various the side channel width, and the conventional co-planar TFT measured at V_{gs}=-15V and V_{ds}=5V.

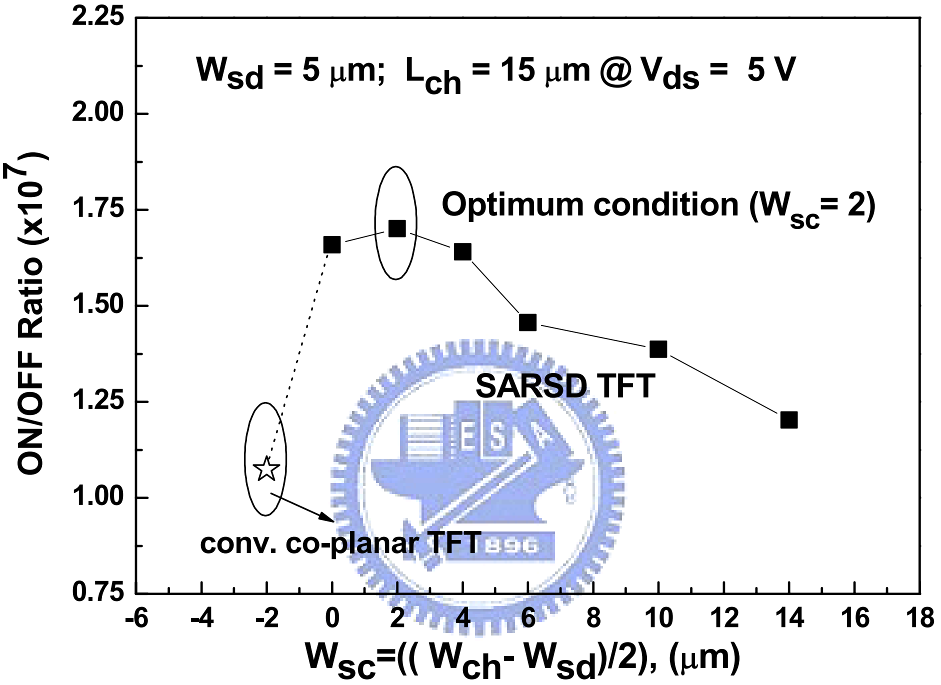

Fig. 3-10 ON/OFF current ratio of the proposed SARSD TFT with various the side-channel width, and the conventional co-planar TFT.

Chapter 4

Effect of Channel Width Widening on a Poly-Si Thin-Film Transistor Structure in the Linear Region

4.1 INTRODUCTION

Low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) are one of the most promising technologies for the ultimate goal of building large area electronic systems on glass substrates [4.1]. In flat panel liquid crystal, electroluminescence, and plasma displays, as well as other applications such as high-speed printers and page-width optical scanners, Poly-Si TFTs can be utilized to integrate peripheral driver circuits on glass for system integration [4.2]. To integrate peripheral driving circuits on the same glass substrate, a large current drive and a high drain breakdown voltage are necessary for poly-Si TFT devices. Previous studies reported that use of a thin active channel film is beneficial for obtaining a high current drive [4.3],[4.4]. However, use of a thin active channel layer typically results in poor source/drain contact and large parasitic series resistance. A thick source/drain region not only reduces the lateral electric field, thus maintaining the breakdown voltage [4.5],[4.6], it also reduces the source/drain series resistance [4.6]. Therefore, an ideal TFT device structure should consist of a thin active channel region while maintaining a thick source/drain region.

To achieve this ideal TFT structure, we have proposed a novel four-mask step TFT structure with self-aligned raised source/drain (SARSD) [4.7]. In the SARSD TFT structure, a special structure was formed that had a wide channel width and a narrow source/drain width. A high ON-state drain current was obtained due to low channel resistance and additional current flow paths existing in the side-channel regions [4.7]. Several models have been proposed to explain the behavior of the ON-state drain currents of Poly-Si TFT’s and to simulate these ON-state drain current values [4.8]–[4.11]. However, drain currents of these models were all derived from the assumption that the channel width is identical to the source/drain width. Simulating the ON-state drain current of a SARSD TFT structure using these models is unreasonable [4.8]–[4.11]. Some studies have discussed the case of a narrow channel width [4.12]–[4.14]; however, no study has discussed the variations in the ON-state drain current when the channel width is larger than the source/drain width. Therefore, before new physical models are proposed to elucidate and simulate the ON-state drain current of a structure with a wide channel width and narrow source/drain width, such as a SARSD TFT, the relationship among the ON-state drain current of a structure with a wide channel width and narrow source/drain width, the channel width, the channel length and the source/drain width must be defined clearly. This task is the aim of this study examining the wide channel width effect in Poly-Si TFTs. This study will help those to further understand the behavior of the carrier transport in the channel region when the channel width is larger than the source/drain width, and explain the increase of the ON-state current of a wide channel width TFT structure, such as the SARSD TFT structure.

This study uses a test structure with a wide channel width and a narrow source/drain width to analyze the influences of the channel width, the channel length and the source/drain width on ON-state drain current. Because the kink effect causes an anomalous current increase in the saturation region, this study only focus on the ON-state drain current in the linear region.

4.2 DEVICE FABRICATION

The fabrication processes for a tested n-channel poly-Si TFT with a wide channel width and narrow source/drain width were as follows. A 50-nm thick α-Si layer for the active region was deposited by a low pressure chemical vapor deposition (LPCVD) system using SiH_4 at 550°C on 500-nm thermal oxidized silicon wafers. The active region was patterned by a G-line stepper and formed using reactive ion etching (RIE) (Fig. 4-1(a)). The deposited α-Si film was then annealed at 600°C for 24 h to become a poly-Si film. A 50-nm plasma-enhanced chemical vapor deposition (PECVD) gate oxide layer was deposited at 350 °C. A 300-nm LPCVD poly-Si gate was then deposited. Because the G-line stepper system has a layer-to-layer misalignment of less than 0.15 μm, the gate region (Fig. 4-1(b)) has two overlapping regions 0.15 μm long that ensure that the source/drain width is narrower than the channel width. After the gate region formation, gate, source and drain regions were formed by ion implantation of phosphorous (dose = 5×10^{15} cm^{-2} at 50 keV) and then activated at 600 °C for 24 h (Fig. 4-1(c)). Following source, drain and gate activation, the 500-nm passivation oxide was deposited by PECVD. Contact holes were opened using wet etching of the passivation oxide layer. A layer 600 nm thick of aluminum was then deposited by a thermal coater system. After metal patterning, Al sintering was carried out at 400°C for 30 min.

The channel region (Fig. 4-1(c)) is divided into one main-channel region (region I) and two side-channel regions (region II). The channel length and width are represented as L_{ch} and W_{ch}, respectively. The channel width (W_{ch}) is wider than the source/drain width (W_{sd}); the channel width can be written as

$$W_{ch}=W_{mc}+2W_{sc}=W_{sd}+2W_{sc} \tag{4.1}$$

where W_{sc} is the width of the side-channel region (region II in Fig.1(c)) in the test structure, and W_{mc} is the main-channel width that is equal to the source/drain width (W_{sd}).

For comparison, the conventional poly-Si TFT’s structure, in which the channel width is identical to the source/drain width, is also fabricated. The physical device parameters of the conventional structure are identical to those of the test structure.

4.3 RESULTS AND DISCUSSION

4.3.1 Simulation Results of the Test Structure ($W_{ch} > W_{sd}$) and the Conventional Structure ($W_{ch} = W_{sd}$)

To simulate the current flows of the test and the conventional structures, the two-dimensional (2-D) numerical simulator MEDICI was used [4.15]. Fig. 4-2(a) shows the simulated current flow lines of the conventional structure in the ON-state. The channel length and the channel width of the simulated conventional structure are 10 μm and 5 μm, respectively. Based on the simulation results (Fig. 4-2(a)), the simulated current flow lines of the conventional structure are uniformly distributed in the channel region (region I in Fig. 4-1(c)) and the source/drain region. However, for the test structures with a wide channel width (Figs. 2(b), 2(c) and 2(d)), there are additional current flow paths that differ from those of the conventional sample existing in the side-channel regions (region II in Fig. 4-1(c)) of the test structure in the ON-state. Furthermore, comparing the simulation results of Fig. 4-2(b) with those of Fig. 4-2(c), the additional current flow is generated in the side-channel regions (region II) and the distribution width of the current flow lines in the side-channel regions increases as the channel length increases (L_{ch} = 3 μm to L_{ch} = 10 μm). This finding implies that the current flow distribution in the side-channel regions depends on the channel length. Comparing the simulation results of Fig. 4-2(c) with those of Fig. 4-2(d), the distribution and the effective distribution width of current flow lines of W_{sd} = 10 μm in region II are almost identical to those of W_{sd} = 5 μm, even when the source /drain width (W_{sd} = 5 μm to W_{sd} = 10 μm) is increased. This finding indicates that an increase in the source/drain width (or main-channel width) does not significantly alter the distribution of current flow lines in region II.

4.3.2 Equivalent Circuit of the Channel Region of the Test Structure ($W_{ch} > W_{sd}$) in the Linear Region

This study uses an equivalent circuit in Fig. 4-3 to further elucidate the additional current flow paths of the test structure in the side-channel regions. In the side-channel regions (Fig. 4-3), the resistance of the path 2 (R_{sc2}) is larger than that of the path 1 (R_{sc1}) because the path 2 is longer than the path 1. Consequently, the current flow via the path 2 must be less than the current flow via the path 1. According to this equivalent circuit, the total channel resistance (R_{tot}) of the test structure can be written as:

$$R_{tot} = \frac{1}{\frac{1}{R_{mc}} + \frac{2}{R_{sc1}} + \frac{2}{R_{sc2}} + \ldots\ldots\ldots\ldots} < R_{mc} \tag{4.2}$$

and

$$R_{mc} = \frac{L_{ch}}{W_{sd}\mu_{eff}C_{ox}(V_{gs}-V_{th})} \tag{4.3}$$

where R_{mc} is the resistance of the main-channel region in the linear region, and R_{mc} is the channel resistance of the conventional structure in the linear region [4.16], and C_{ox}, μ_{eff} and V_{th} are gate dielectric capacitance per unit area, effect mobility and threshold voltage, respectively. According to Eq. 4.2, the total channel resistance (R_{tot}) of the test structure is smaller than that of the main-channel region (R_{mc}). In other words, R_{tot} of the test structure is smaller than that of the conventional structure. Therefore, in the linear region, the ON-state drain current of the test structure is higher than that of the conventional structure. As discussed, when the distance of current path is sufficiently long, the resistance of current path would be too large for current flow. Thus, we suggest that, in the linear region, the distribution of most current flow paths should be restricted within a certain effective width in the side-channel region ($W_{sc,eff}$) and the ON-state drain current will become gradually independent of W_{sc} as W_{sc} increases. In other words, the ON-state drain current of the test structure is saturated at a certain value when W_{sc} is sufficiently large.

4.3.3 Electrical Characteristics of the Test Structure ($W_{ch} > W_{sd}$) and the Conventional Structure ($W_{ch} = W_{sd}$) in the Linear Region

Figs. 4-4 ~ 4-6 present the experimental data for the test structure. In Fig. 4-4(a), the I_{ds}-V_{gs} transfer characteristics of the test structure with different side-channel widths are compared with those of the conventional sample. The ON-state drain currents of the test structures are all higher than those of the conventional structure for different side-channel widths. Additionally, the ON-state drain current of the test structure initially increases as the side-channel width (W_{sc}) increases, and then becomes gradually independent of W_{sc} after reaching a certain W_{sc} value, even when the W_{sd}/L_{ch} ratio of the test structure decreases from 10 μm /5 μm to 5 μm /15 μm (Fig. 4-5(a)). These experimental results are consistent with observations and suggestions in Section 4.3.2. Figs. 4-4(b) and 4-5(b) show the output characteristics of the test structure with different side-channel widths. The ON-state drain currents of the test structure are larger than those of the conventional structure in both linear and saturation regions. Additionally, according to the output characteristics (Figs. 4-4(b) and 4-5(b)) in the linear region, the channel resistance reduces as W_{SC} increases. Therefore, according to the experimental results (Figs. 4-4 and 4-5) and Eq. 4.2, we conclude that the main reason for a high ON-state drain current of the test structure is low channel resistance.

Fig. 4-6 shows the ON-state drain current distributions of the test structure varied with the side-channel width for different channel lengths and the source/drain widths. Twenty test TFTs were measured for each condition. Based on the experimental results (Figs. 4-6(a) and 4-6(b)), the ON-state drain current of the test structure initially increases as W_{SC} increases, and then gradually becomes saturated when W_{SC} exceeds a threshold value. This special side-channel width is called the effective side-channel width ($W_{SC,eff}$), and most current flow lines are included within its corresponding effective channel width ($W_{ch,eff}$) obtained from Eq. 4.1. The effect in that a high ON-state drain current is obtained when the channel width is larger than that of the source/drain is called the side-channel current effect (SCCE). Moreover, the value of the effective side-channel width ($W_{SC,eff}$) decreases as the channel length increases, even when the source/drain width increases from 5 μm to 10 μm. This experimental finding is consistent with the simulation results (Fig. 4-2).

To analyze the increased ratio of the ON-state drain current caused by the SCCE, the average values of the ON-state drain current gain (A_i) versus the side-channel width are plotted (Figs. 4-7(a) and 4-7(b). The ON-state drain current gain (A_i) is defined as

$$A_i \equiv \frac{I_{ds,t} - I_{ds,c}}{I_{ds,c}} \qquad (4.4)$$

where $I_{ds,c}$ is the ON-state drain current of the conventional structure, $I_{ds,t}$ is the ON-state drain current of the test structure with different side-channel widths, and ($I_{ds,t}$ - $I_{ds,c}$) is the net value of the ON-state drain current flow through region II.

Based on the experimental results (Figs. 4-7(a) and 4-7(b)), the average ON-state drain current gain (A_i) of the test structure increases as the channel length increases. Additionally, for the same channel length (such as L_{ch} = 15 μm), the effective side-channel widths ($W_{sc,eff}$) of W_{sd} = 5 μm and W_{sd} = 10 μm are approximately the same. These experimental results are consistent with the simulation results (Figs. 4-2(b) ~ 4-2(d)); in other words, the increase in the source/drain width (or main-channel width) does not significantly increase the distributions of current flow lines in region II. However, the reduction of the W_{sd} from 10 μm to 5 μm increases the average value of A_i. Therefore, we conclude that the effective side-channel width ($W_{sc,eff}$) is dependent on the channel length (L_{ch}) and independent of the source/drain width (W_{sd}), and the SCCE is dependent on the side-channel width, the channel length and the source/drain width.

4.3.4 Relationship among the ON-state Drain Current or the ON-state Drain Current Gain and the Channel Length, the Side-Channel Width and the Source/Drain Width in the Linear Region

To investigate the relationship among the ON-state drain current gain (A_i), the channel length, the side-channel width and the source/drain width, this study analyzes the distributions of the ON-state drain current gain (A_i) against L_{ch} and the L_{ch}/W_{sd} ratio with different channel widths and the side-channel widths (Fig. 4-8 and Fig. 4-9), respectively. The ON state current gains A_i is directly proportional to L_{ch} for both W_{sd} = 5 μm and 10 μm (Figs. 4-8(a) and 4-8(b)). Moreover, the ON state current gains A_i is directly proportional to the L_{ch}/W_{sd} ratio for both W_{sd} = 5 μm and 10 μm (Figs. 4-9(a) and 4-9(b)). Therefore, we conclude that the ON state current gain is directly proportional to L_{ch} and the L_{ch}/W_{sd} ratio, and depends on W_{sc}.

According to the experimental results (Figs. 4-8 and 4-9), the simple relationship among the ON-state drain current gain (A_i), the channel length L_{ch} and the source/drain width W_{sd} can be written as:

$$A_i \cong B\frac{L_{ch}+C}{W_{sd}} \tag{4.5}$$

where B and C are constants.

In the cases of $W_{sc} \geq W_{sc.eff}$, B is approximately 0.48 based on the slopes of the auxiliary straight lines (Figs. 4-9(a) and 4-9(b)), and C is roughly -1.55 according to the intercepts of the auxiliary straight lines (Figs. 4-8(a) and 4-8(b)).

By combining Eqs. 4.4 and 4.5, the maximum ON-state drain current gain ($A_{i,max}$) caused by the SCCE is obtained:

$$A_{i,max} \equiv \frac{I_{ds,t,max} - I_{ds,c}}{I_{ds,c}} \cong 0.48(\frac{L_{ch}^{-1.55}}{W_{sd}}) \tag{4.6}$$

In the case of $W_{sc} \geq W_{sc.eff}$, if the channel length and the source/drain width are determined, the saturated or maximum ON-state drain current of the test structure ($I_{ds,t,max}$) can be written as:

$$I_{ds,t,max} \cong [1 + 0.48(\frac{L_{ch}^{-1.55}}{W_{sd}})]I_{ds,c} \tag{4.7}$$

Fig. 4-10 presents the experimental data and the calculated data. The calculated data roughly agrees with the experimental data for different source/drain widths and different applied drain biases (V_{ds} = 5 V or 10 V) (Fig. 4-10).

However, for L_{ch} = 15 μm (Figs. 4-8(a) and 4-9(a)), the experimental data diverge from the auxiliary straight line because the side-channel width (W_{sc}) of the test structure of L_{ch} = 15 μm, which is 6 μm, is smaller than the effective side-channel width ($W_{sc,eff}$) of the test structure of L_{ch} = 15 μm, which is approximately 10 μm (Fig. 4-7). Therefore, the ON-state drain current gain (A_i) is limited by the side-channel width (W_{sc}) and the experimental data of L_{ch} = 15 μm cannot be fitted to the auxiliary straight line. However, for the case of L_{ch}/W_{sd} = 15 μm/5 μm (Figs. 4-8(b) and 4-9(b)), the experimental data are not fitted to the auxiliary straight line, even though W_{sc}(= 14 μm) is larger than $W_{sc,eff}$ (~ 10 μm). It has been reported that the channel resistance is directly proportional to the L_{ch}/W_{sd} ratio [4.16]. A large L_{ch}/W_{sd} ratio indicates substantial channel resistance. Therefore, the main reason for why the experimental data of L_{ch}/W_{sd} = 15 μm/ 5 μm are not fitted to the auxiliary straight line (Figs 4-8(b) and 4-9(b)) is that a large channel resistance dominates.

Therefore, when the channel width is wider than the source/drain width, the side-channel current effect (SCCE) is generated, and this effect will cause an increase in the ON-state drain current due to the additional current flow paths existing in the side-channel regions and low channel resistance. As the side-channel width increases, the ON-state drain current initially increases and then gradually becomes independent of the side-channel width when the side-channel width is larger than the effective side-channel width, which depends on the channel width and is independent of the source/drain width. This study also demonstrates that the ON-state drain current gain (A_i) is directly proportional to the channel length (L_{ch}) and the ratio of the channel length to the source/drain width (L_{ch}/W_{sd}), and dependent on the side-channel width. Moreover, when the ratio of the channel length to the source/drain width is excessively large, high channel resistance caused by large ratio of the channel length to the source/drain width will suppress the SCCE and limit the increase in the ON-state drain current gain.

4.4 SUMMARY

In this chapter, it is the first study to discuss the ON-state drain current of a special thin film transistor structure with a wide channel width and a narrow source/drain width in the linear region.

The experimental results indicate that when the channel width is wider than the source/drain width, the side-channel current effect (SCCE) is generated; this effect increases the ON-state drain current due to the additional current flow paths existing in the side-channel regions and low channel resistance. As the side-channel width increases, the ON-state drain current initially increases and then gradually becomes independent of the side-channel width when the side channel width is larger than the effective side channel width, which depends on the channel width and is largely independent of the source/drain width. This study also demonstrates that the ON-state drain current gain is directly proportional to the channel length and the ratio of the channel length to the source/drain width, and dependent on the side-channel width. Moreover, a simple relationship among the ON-state drain current, the source/drain width and the channel length is identified. These experimental results will prove helpful to further understand the carrier transport mechanisms in the ON-state when the channel width is larger than the source/drain width. These experimental results will also prove useful in the development of complete ON-state current modeling.

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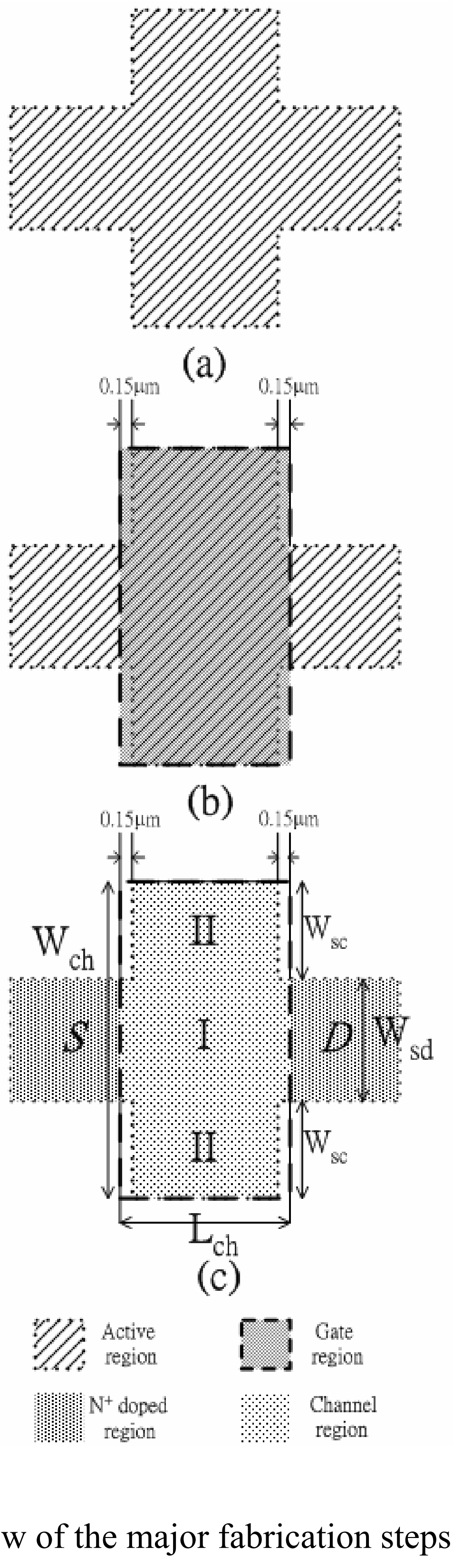


Fig. 4-1 Schematic top view of the major fabrication steps for the test TFT's.

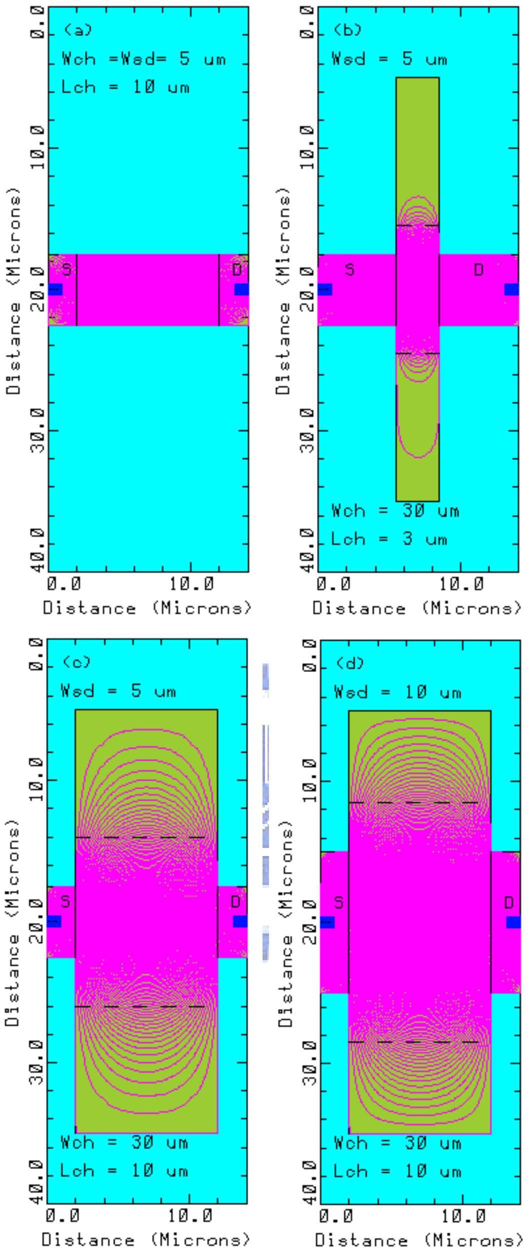


Fig. 4-2 Current flow lines simulated by MEDICI in (a) the conventional structure with L_{ch} = 1 0 μm and W_{ch} = W_{sd} = 5 μm; (b) the test structure with L_{ch} = 3 μm, W_{sd} = 5 μm and W_{ch} = 30 μm; (c) the test structure with L_{ch} = 10 μm, W_{sd} = 5 μm and W_{ch} = 30 μm; (d) the test structure with L_{ch} = 10 μm, W_{sd} = 10 μm and W_{ch} = 30 μm.

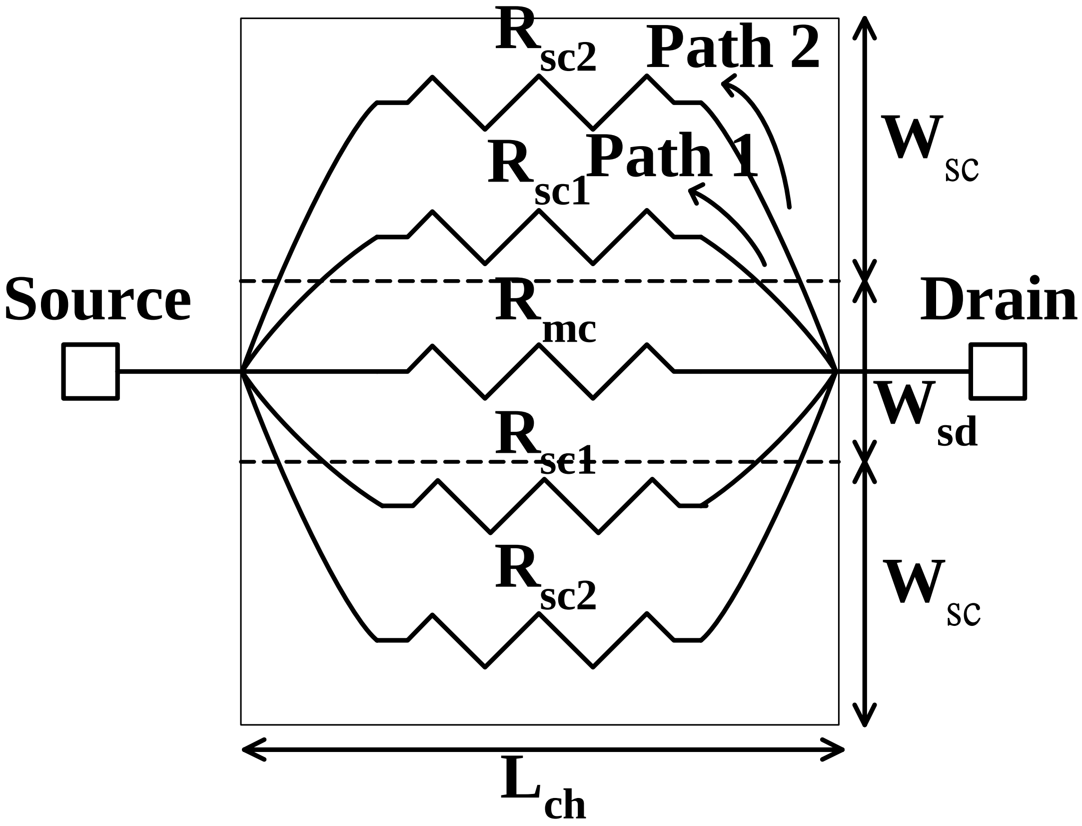
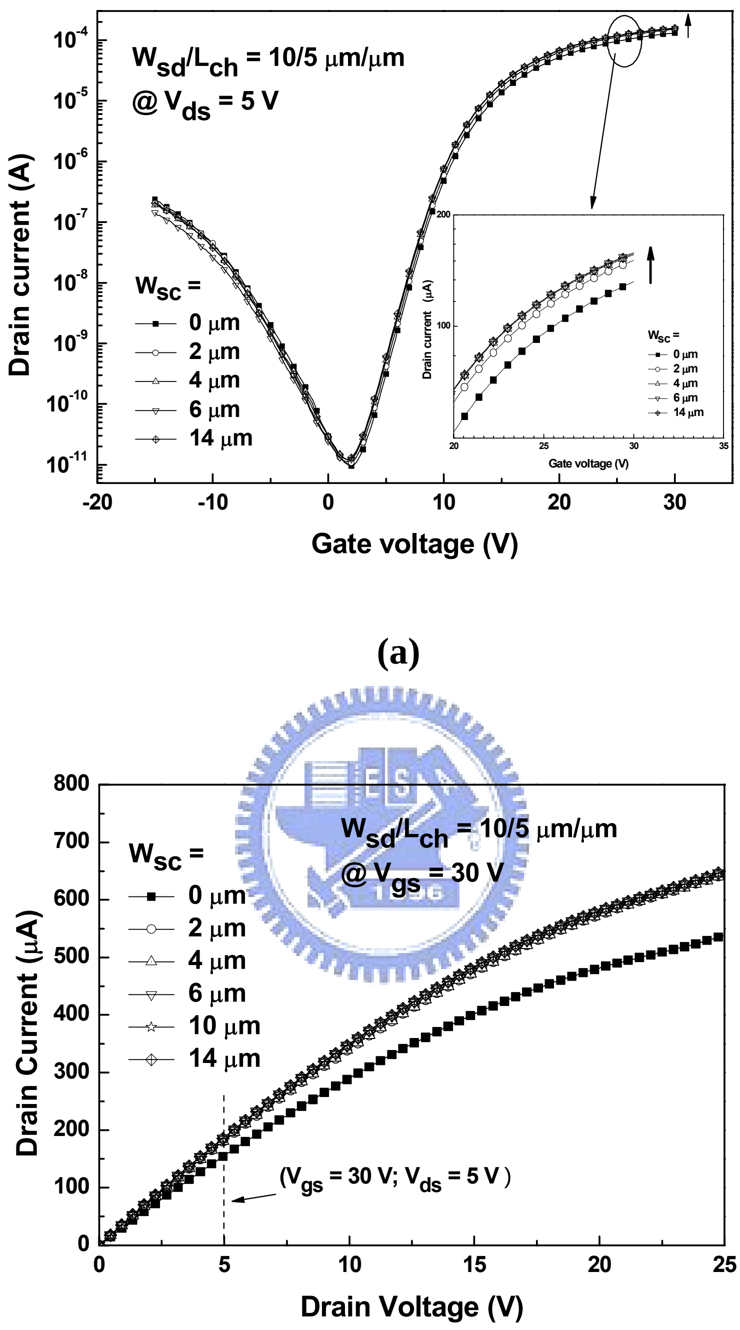


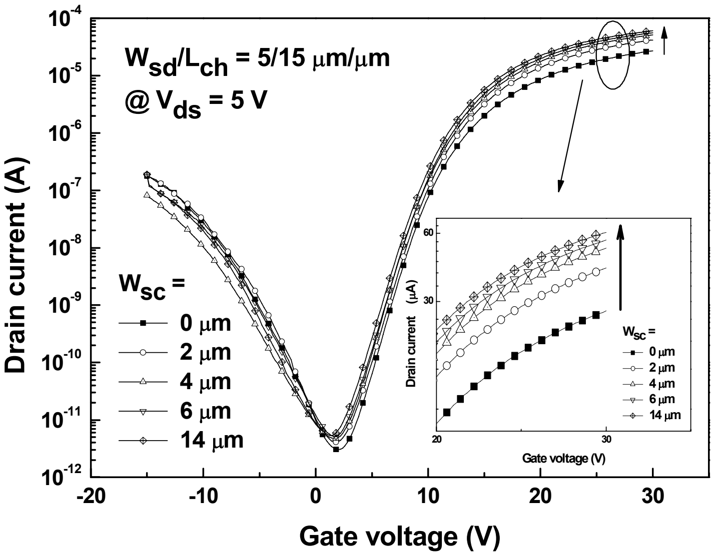
Fig. 4-3 Equivalent circuit of the channel region of the test structure ($R_{m,c}$ is the main-channel resistance; $R_{s,c}$ is the side-channel resistance).



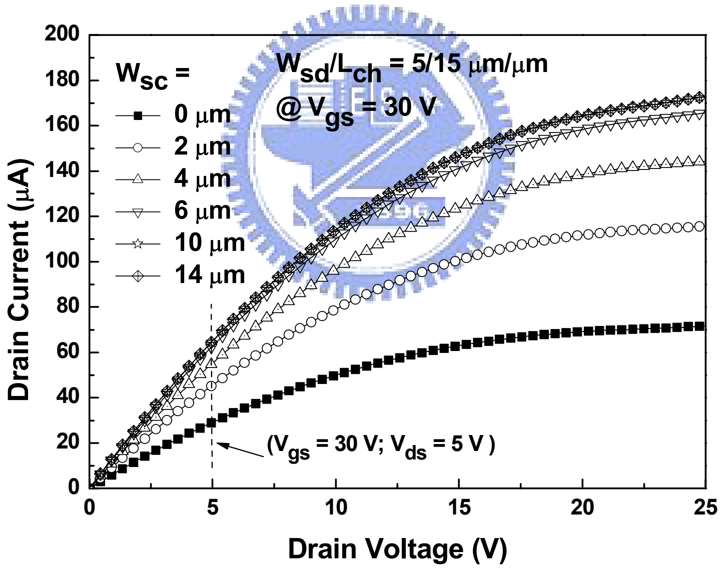
(a)

(b)

Fig. 4-4 I_{ds}-V_{gs} transfer characteristics; (b) I_{ds}-V_{ds} output characteristics of the test structure with L_{ch} /W_{sd} = 1 0 μm /5 μm with different side-channel widths (W_{sc}) compared with the conventional structure.

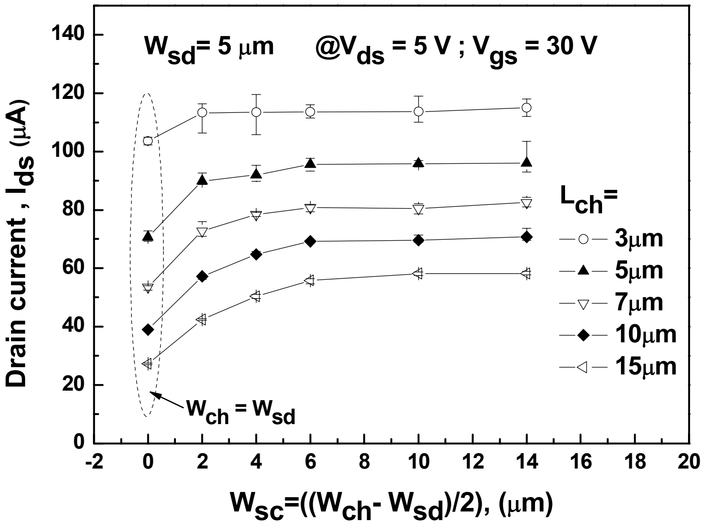


(a)

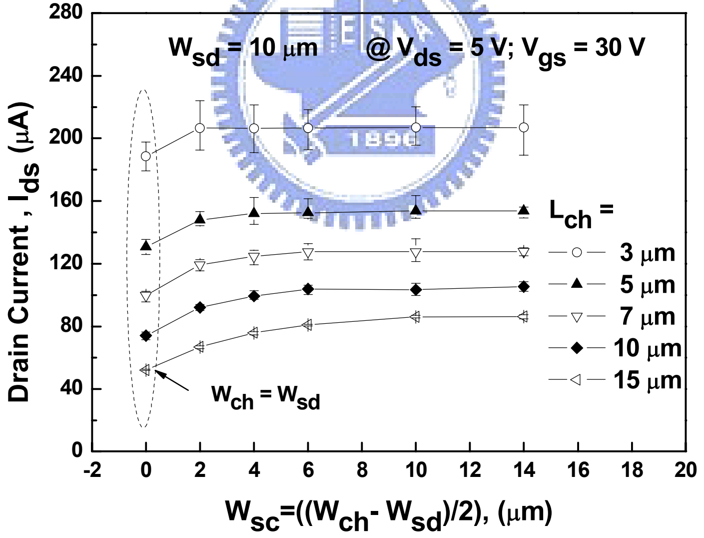


(b)

Fig. 4-5 I_{ds}-V_{gs} transfer characteristics; (b) I_{ds}-V_{ds} output characteristics of the test structure of L_{ch} /W_{sd} = 5 μm / 15 μm with different side channel widths (W_{sc}) compared with the conventional structure.



(a)



(b)

Fig. 4-6 Distributions of the ON-state drain currents of the test structure with (a) W_{sd} = 5μm; (b) W_{sd} = 1 0 μm as a function of the side-channel width W_{sc}.

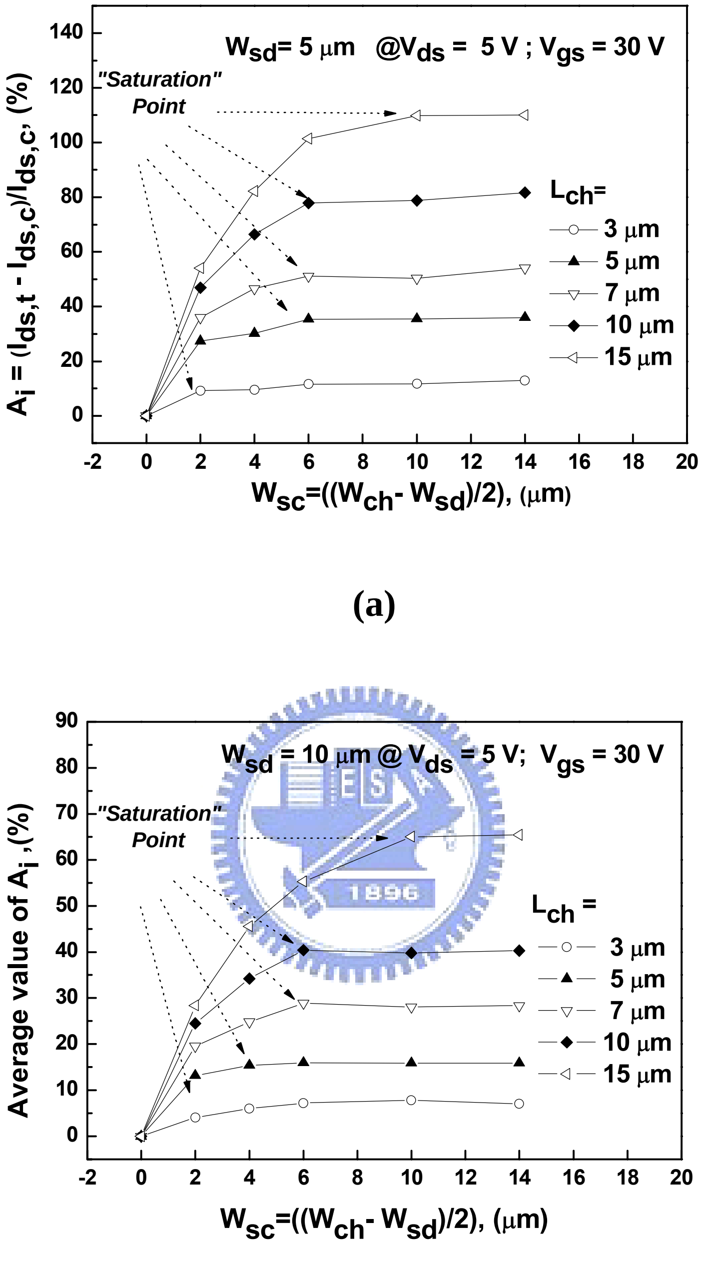
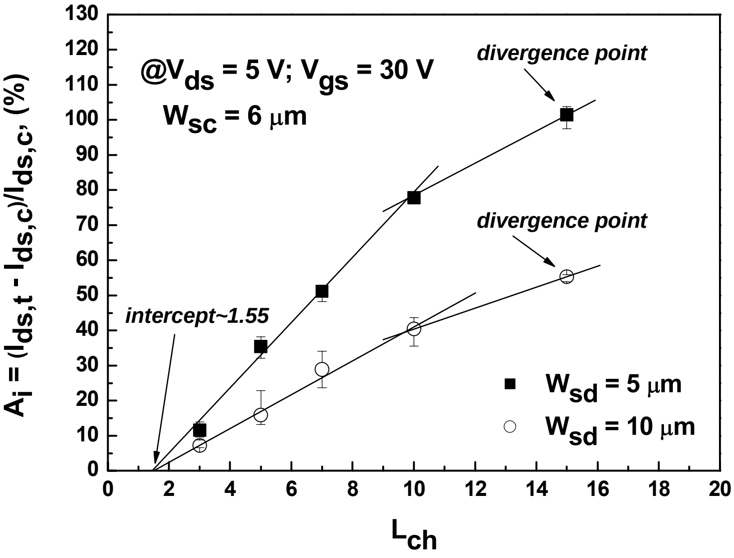
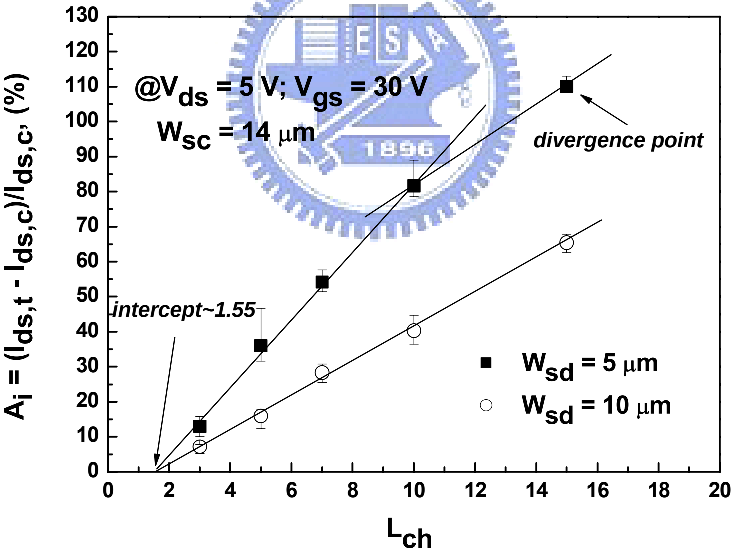


Fig. 4-7 Average values for the ON-state drain current gain A_i of the test structure with (a) W_{sd} = 5μm and (b) W_{sd} = 1 0 μm as a function of the side-channel width W_{sc}.

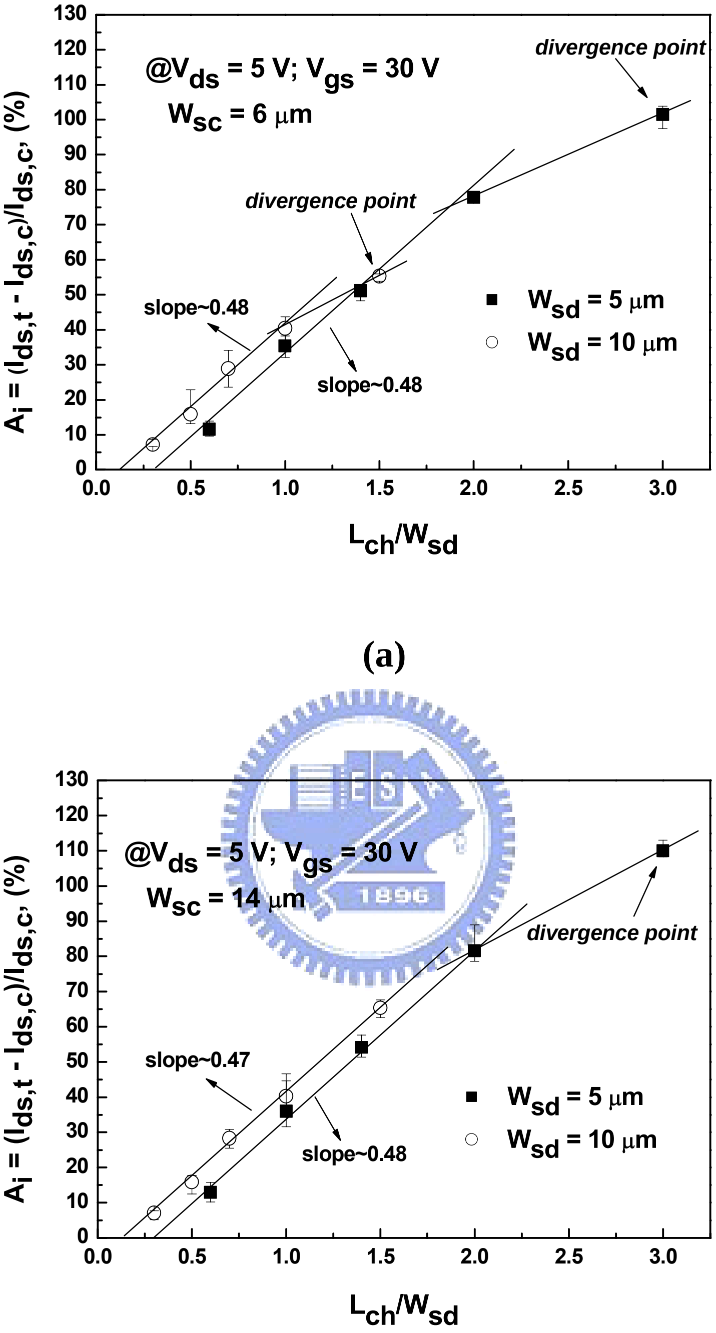


(a)



(b)

Fig. 4-8 Distributions of the ON-state drain current gain A_i of the test structure with (a) W_{sc} = 6 μm and (b) W_{sc} = 1 4 μm compared with channel length L_{ch}.



(a)

(b)

Fig. 4-9 Distributions of the ON-state drain current gain A_i of the test structure with (a) W_{sc} = 6 μm; (b) W_{sc} = 1 4 μm compared with the ratio of the channel length to the source/drain width L_{ch}/W_{sd}.

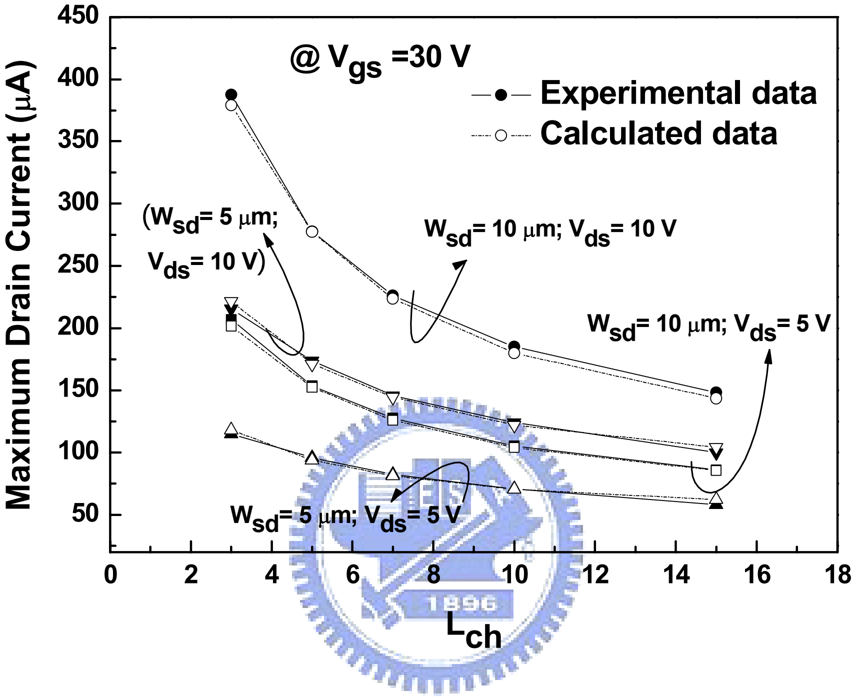


Fig. 4-10 Experimental and calculated maximum ON-state drain current for the test structure with different source/drain widths and different applied drain biases compared with the channel length L_{ch}, in which solid symbols represent the experimental data and empty symbols represent the calculated data obtained from Eq. 4.7.

Chapter 5

CONCLUSION AND FUTURE WORKS

5.1 CONCLUSION

In this thesis, we have developed two novel RSD TFT structures to improve the OFF-state leakage current of the TFT devices by reducing the electric field near the drain region. We also study the effect of channel width widening on a Poly-Si TFT when the channel width is larger than the source/drain width, such as SARSD TFT structure.

For the D-SAGRSD structure in chapter 2, we utilized the damascene process and Chemical Mechanical Polishing (CMP) technology to form a RSD TFT which the gate region can be self-aligned. This structure can significantly improve the OFF-state leakage current by increasing the junction depth to reduce the electric field near the drain region, but slightly decrease the ON-state current. The new TFT does not require any additional lithography steps to form raised source and drain regions and self-aligned gate.

For the SARSD structure in chapter 3, we utilized gate mask to form an isolated active region after defining the gate region. This structure features a self-aligned raised source/drain region and a thin, wide channel region below the whole of the gate region. Comparing with the conventional co-planar TFT, the leakage current of the SARSD TFT can be reduced due to reduction of the lateral electric field near the drain region, and the ON-state current of the SARSD TFT would be increased due to wide channel width. Therefore, SARSD TFT has a higher ON/OFF current ratio and a lower ON-state leakage current than those of the conventional co-planar TFT

. Additionally, current device models are not suitable to explain the behavior of the ON-state drain currents of Poly-Si TFT's and to simulate these ON-state drain current values because the drain currents of these models were all derived from the assumption that the channel width is identical to the source/drain width. No study has discussed the variations in the ON-state drain current when the channel width is larger than the source/drain width. Therefore, in chapter 4, a simple relationship among the ON-state drain current of a structure with a wide channel width and narrow source/drain width, the channel width, the channel length and the source/drain width is identified. These experimental results will prove helpful to further understand the carrier transport mechanisms in the ON-state when the channel width is larger than the source/drain width. These experimental results will also prove useful in the development of complete ON-state current modeling.

5.2 FUTURE WORKS

Although, we have proposed two novel Poly-Si TFT's structures to improve the leakage current of the Poly-Si TFT's, and study the effect of channel width widening on a Poly-Si TFT when the channel width is larger than the source/drain width. However, there are still some problems should be solved. We introduce these issues and future works in several parts:

(1) For the proposed TFT structures (SARSD and D-SAGRSD TFTs), though increasing channel region thickness near the drain region will reduce the lateral electric field, but unfortunately, it will also induce large amount of the grain boundary traps near the drain region. These grain boundary traps will cause proposed TFT structures to have higher threshold voltage and worse stability under stress than the conventional co-planar TFTs. Hydrogenation by using PECVD is a well-known technology to passivate these grain boundary traps. However, different channel thicknesses have different optimum hydrogenation times. It is difficult to passivate defects of the thin channel region and thick source/drain regions at the same time.

Therefore, how to effective reduce or passivate these grain boundary traps is a very important issue for using SARSD and D-SAGRSD TFTs.

(2) Although a simple relationship among the ON-state current, the channel length, the channel width and the source/drain width is proposed to explain the behavior of the ON-state current of the TFT when the channel width is larger than the source/drain width, this simple relationship is only focus in the linear region. Therefore, more experiments and further analysis are necessary to establish a more complete device model in both linear region and saturation region.

(3) In this thesis, we used Solid Phase Crystallization (SPC) technology to re-crystallize the Poly-Si film. However, it is necessary to use Laser-crystallization to enlarge Poly-Si grains for obtaining high mobility and high drive current.

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中文：具備新穎自我對準升高式源/汲極結構之低溫複晶矽薄膜電晶體元件之開發與寬通道效應之研究

英文：Development of Novel Self-Aligned Raised Source/Drain Structure for Polysilicon Thin-Film Transistor and the Study of the Channel Width Widening Effect

學術著作目錄

A. 國際性期刊 (Letter) :

[1]（新，3 點）Kow Ming Chang, Gin Min Lin, and Guo Liang Yang, “A Novel Low-Temperature Polysilicon Thin-Film Transistors With a Self-Aligned Gate and Raised Source/Drain Formed by the Damascene Process,” *IEEE Electron Device Letters*, vol. 28, no. 9, pp. 806-808, Sep. 2007.

[2]（新，3 點）Kow Ming Chang, Gin Min Lin, Cheng Guo Chen and Mon Fan Hsieh, “A Novel Four-Mask Step Low-Temperature Polysilicon Thin-Film Transistors with Self-Aligned Raised Source/Drain (SARSD),” *IEEE Electron Device Letters*, vol. 28, no. 1, pp. 39-41, Jan. 2007.

B. 國際性期刊 (Journal) :

[1]（新，3 點）Kow Ming Chang, and Gin Ming Lin, “Effect of Channel Width Widening on a Poly-Si Thin-Film Transistor Structure in the Linear Region,” *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2418-2425, Sep. 2007.

C. 專利:

[1] 張國明，林俊銘:“新穎堆疊式源/汲極與薄通道複晶矽薄膜電晶體結構及其製作方法”

著作總點數: 9 點