國立交通大學

電 機 與 控 制 工 程 學 系

碩 士 論 文

連續時間和差類比數位轉換器之迴圈延遲補償器設計之研究

On Loop Delay Compensation Design for Continuous-Time ΣΔ ADC

研 究 生：何峻徹

指導教授：董蘭榮 博士

中 華 民 國 九 十 六 年 九 月

連續時間和差類比數位轉換器之迴圈延遲補償器設計之研究

On Loop Delay Compensation Design for Continuous-Time ΣΔ ADC

研 究 生：何峻徹　　Student：Jyun-Chen Ho

指導教授：董蘭榮 博士　　Advisor：Lan-Rong Dung

國 立 交 通 大 學

電 機 與 控 制 工 程 學 系

碩 士 論 文

A Thesis

Submitted to Department of Electrical and Control Engineering

College of Electrical Engineering and Computer Science

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of

Master of Science

In

Electrical and Control Engineering

September 2007

Hsinchu, Taiwan, Republic of China

中 華 民 國 九 十 六 年 九 月

On Loop Delay Compensation Design for Continuous-Time ΣΔ ADC

Student：Jyun-Che Ho　　Advisor：Lan-Rong Dung

Institute of Electrical and Control Engineering National Chiao-Tung University

Abstract

A ΔΣ modulator is well-known as a very efficient technique for the implementation of high resolution A/D converters in low to medium bandwidth applications. Comparing with switched-capacitor (discrete-time) technique in the past, the continuous time circuitry is more suitable for today's growing bandwidth applications. The thesis presents the implementation of a ΔΣ modulator with continuous-time techniques. Different numbers of digital delay in the ΔΣ feedback loop have been analyzed based on mathematic theorems in detail. The chip is designed with 1.8V power supply by using 0.18μm TSMC CMOS process, with power consumption 6.5mW and the core area 0.05mm^2. The simulation result shows that the ADC achieves a 62dB peak signal-to-noise pulse distortion ratio (Peak-SNDR) within a 2MHz bandwidth with a sampling rate of 100MHz.

連續時間和差類比數位轉換器之迴圈延遲補償器設計之研究

研 究 生：何峻徹　　指導教授：董蘭榮 博士

國立交通大學電機與控制工程學系

摘要

和差調變器以往是非常廣泛的應用於低中頻寬、高解析度的一項技術。然而相較於過去傳統所常用的交換型電容(離散時間)的技術，隨著對於頻寬需求的增加，連續型的電路設計方式將會更適合於現今高頻寬的應用。本論文就實現連續型和差調變器來做一些探討。在於和差調變器回授路徑上，不同的延遲時間將會依據一些數學理論來做詳細地分析。此晶片使用台積電 0.18μm CMOS 製程，供應電壓為 1.8 V，消耗功率為 6.5-mW，晶片核心面積為 0.05mm^2。模擬結果在100MHz的取樣頻率、2MHz 的頻寬內得到峰值SNDR為 62dB。

Acknowledgments

I would like to appreciate many people who help me in graduate studies in National Chiao-Tung University. First, I would like to thank my advisor, Professor Lan-Rong Dung, for his useful guidance and support. Without his inspiring discussions and strongly urge, this thesis is impossible to be done.

I would like to thanks all SoCLAB members for accompanying me in my graduate life. I relax my mind by sharing pleasure and pains with them. We not only research together but also play together. I also thank that they even give me some girls' msn. I would like to thank Teng-Hung Chang for his useful suggests and comments in the meeting.

Finally, I would like to gratefully acknowledge my parents and my brother and sister. My family gives me a fine environment so that I could focus on research with my level best. Their love, care and patience are main motive power in the past two years.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Continuous-Time ΣΔ Modulators

Data converter is one of the key components in electronic systems. Since the real world is inherently analog and the trend in voice, video, telecommunication, computer and many other applications is to get a digital form. The analog digital interfaces become critical paths. Data converters are composed of many analog building blocks such as operational amplifiers (opamps), track-and-holds and comparators, which make their design very challenging in high speed and low voltage design. Unlike Nyquist A/D converters, which need high-precision analog components, a sigma-delta (ΣΔ converter shows less sensitivity to analog circuit non-idealities. The most popular oversampling ADC architecture is based on a ΣΔ modulator. The ΣΔ A/D converter usually consists of an analog part called a ΣΔ modulator producing a bit stream followed by a digital part implementing decimation and digital filtering to complete the A/D conversion [1].

As decreasing supply voltage in recent CMOS technologies, it causes design on switched-capacitor (SC) circuit difficulty. Some problems will be found in SC circuit design such as high switch resistances limit the signal swing rang and also limit the sampling frequency. Some circuit techniques, like bootstrapping switch and switched–opamp, have been developed to overcome these problems. These techniques increase complexity in circuit design. However continuous-time (CT) ΣΔ modulators do not suffer these problems because they do not require precision track-and-hold

circuits. They take advantage of modern technologies with high speed but low precision capabilities [7, 8]. In SC circuit, input-signal sampling errors, like charge injection, settling-time errors and some other discrete time problems that do not exit in CT techniques. The gain bandwidth product (GBW) and slew rate requirements of the used opamps are much lower compared to their DT counterparts [2, 3, 4, 5]. Moreover, CT implementations of ADCs extend the input frequency range from a few 100 kHz up to a few 10 MHz [6]. Giving some examples, a CT complex sigma-delta multi-bit modulator, implemented in standard 0.25-μm CMOS technology and meeting all major requirements for application in IEEE 802.11a/b/g wireless LAN receivers was presented in [10]. The clock frequency is 320 MHz, producing an oversampling ratio of 16 for 20 MHz channel bandwidths and dissipates only 32 mW of power. Another wide bandwidth continuous-time ΣΔ ADC, operating between 20 and 40 MS/s output data rate, is implemented in 130-nm CMOS [11]. The ΣΔ ADC achieves 76-dB SNR 12 ENOB over a 20-MHz signal band at an OSR of 16. The power consumption of the CT ΣΔ modulator itself is 20 mW.

Furthermore, the sampling operation takes place inside the modulator. So sampling errors and out of band signals are greatly suppressed by the high gain loop filter. This thesis demonstrates a third order ΣΔ modulator with different compensation delays. It shows some practical advantages and drawbacks of a continuous time ΣΔ implementation, which have been proved by analysis and simulations.

1.2 Organization of the Thesis

This section gives a brief overview of the following chapters. Chapter 2 reviews some fundamentals of a ΣΔ modulator and introduces concepts of a CT ΣΔ modulator. Stability criteria in a ΣΔ modulator are also critically reviewed and perform equivalence between DT and CT modulator based on *modified z* transform. The method is general and systematic. Several low-pass design examples are given to illustrate the effectiveness of the transformation method.

Chapter 3 involves effects of circuit non-idealities and describes available error cancellation and compensation techniques. Some non-idealities models are also built for system level simulation.

Chapter 4 describes some methods to compensate for excess loop delay. Based on some stability theorems, different compensation delays and loop filter gain error relation have been discussed. It discusses the sensitivity of continuous-time modulators to the compensation loop delays.

Chapter 5 presents a circuit implementation of a CT ΣΔ modulator with quarter delay compensation. It concludes with simulation results of the entire ΣΔ modulator circuit with the active-RC amplifier.

Chapter 6 concludes the thesis and the main contributions could be summarized in this section.

Chapter 2

Fundamentals of ΣΔ modulators

2.1 Sampling and Quantization

The conversion of analog signal to digital domain can distribute into two basic operations: sampling in time and quantization in amplitude. In order to reconstruct the original signal without aliasing, an analog filter, called anti-aliasing filter, enforces the Nyquist condition. The Nyquist theorem is $fs \geq 2f_B = f_N$, there f_s is the sampling frequency, f_B is the signal bandwidth and f_N is the Nyquist frequency.

The process of quantization in amplitude encodes a continuous range of analog values into a set of discrete levels. The key distinguish characteristic of a quantizer is its number of bits B, which correlates with the number of different output levels. If the analog input is mapped into 2^B discrete levels, the quantizer is said to have B-bits resolution. The quantizer step width is defined as $\Delta = \frac{A}{2^B - 1}$, showed in Fig. 2.1, where A is the input signal full-scale. Because the quantizer is a nonlinear component in the A/D converter, in order to analyze the quantization noise, the non-ideality must to be linearized. There is a basic of the additive white noise model for the quantizer [1]. Then, the quantizer is reduced to an unknown gain k and a quantization error or noise $e(n)$. For analysis convenience, the quantizer gain has been set to one, as indicated in Fig. 2.1. With this model, the quantization noise power and its noise power spectral density is derived to [1, 12]:

$$\sigma_e^2 = \int_{-\infty}^{\infty} e^2 \, pdf_e de = \frac{\Delta^2}{12}, \quad S_e^2 = \frac{\Delta^2}{12}\frac{1}{fs} \tag{2.1}$$

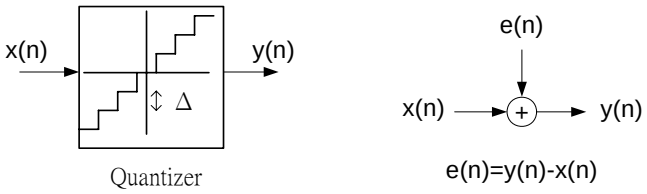


Figure 2.1 Linear quantizer model

2.2 Nyquist-Rate, Oversampling and Noise-Shaping Converters

The Nyquist ADC signal-to-noise-ratio (SNR) can be expressed as the following form:

$$SNR_p|_{Nyquist} = B6.022dB + 1.76dB \tag{2.2}$$

From (2.1) it is obvious that an increase of the sampling frequency lowers the quantization noise power spectral density. By sampling higher than the Nyquist frequency and filtering the out-of-band noise. The quantization noise in the signal band can be reduced. This is main ideal of oversampling ADC. A ΣΔ modulator not only over-samples, but also shapes the quantization noise to out-of-band. Thus, the following filter called the decimator filters the out-of-band quantization noise. A typical block diagram of a ΣΔ ADC is given in Fig. 2.2. A ΣΔ modulator is the different transfer behavior for the quantization error signal, the noise transfer function (NTF) and the input signal, the signal transfer function (STF). Both equations are derived as:

$$STF(z) = \frac{Y(z)}{U(z)} = \frac{1}{\frac{1}{H(z)} + 1},\ NTF(z) = \frac{1}{1 + H(z)} \tag{2.3}$$

By assuming the filter function in Fig. 2.2 to be a DT integrator $\frac{z^{-1}}{1 - z^{-1}}$, the 1st order modulator is obtained and the NTF in (2.3) becomes a first order high-pass filter. The

in-band noise (IBN) yields:

$$INB \approx \int_{-f_B}^{f_B} 4\pi^2 \frac{\Delta^2}{12 f_S} (\frac{f}{f_S})^2 df = \frac{\Delta^2}{12} \frac{\pi^2}{3} \frac{1}{OSR^3} \tag{2.4}$$

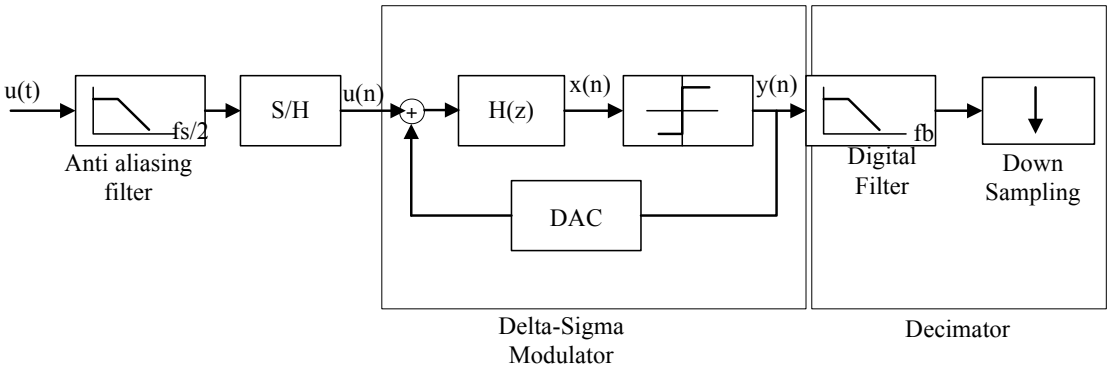


Figure 2.2 Block diagram of ΣΔ ADC

Considering the extended general form to the N-order case, the equation (2.4) also could be derived as generally form:

$$INB \approx \frac{\Delta^2}{12} \frac{\pi^2}{3} \frac{1}{OSR^{2N+1}} \tag{2.5}$$

2.3 ΣΔ Modulator Design Issues

In this section, several design issues in design a ΣΔ modulator are presented. The order, oversampling ratio, and numbers of quantizer bits influence a ΣΔ modulator. Their stability constraints will also be described.

2.3.1 Performance Increase in ΣΔ Modulators

From (2.5) and the consideration above, there are several approaches to increase the performance of ΣΔ modulator. First, increasing the loop filter order, the operating principle of ΣΔ modulators is based on shaping the quantization noise from the in-band to higher frequency. It is obvious to use a more aggressive and higher order (N) filter function as in (2.5). By doing this, the decrease of the INB with the OSR in (2.5) becomes better $INB \propto OSR^{-2N-1}$. With the higher order, it results in instability

through overloading the quantizer. Thus, in order to increase the stability, the loop filter coefficient should be scaling suitable [17].

From (2.5), it is obvious that using higher OSR will reduce the quantization noise. For higher OSR, the higher sampling frequency increases. From this consideration, analog components, like comparators, opamps and track-and-holds should be able to operate in the high frequency. The circuit realization is more difficult and the power consumption will increase.

Finally, reducing the quantization step width, that is to increase the quantizer number of bits. By doing this, the intrinsic resolution is increased proportionally to $(2^B - 1)^2$. According to (2.5) the quantizer step width, as a symbol Δ indicated in (2.5), the quantizer noise power decreases proportionally. Furthermore, the incorporation of multi-bit internal quantizer tends to make higher order modulators more stable. Because the feedback DAC fed the modulator input, its errors are directly seen at the modulator input. For a single-bit internal quantize this problem does not arise, because a two level DAC is intrinsically linear. For a 1.5-bit tri-level quantizer, the DAC linearity also does not degrade the modulator performance seriously [15].

2.3.2 Stability Constraints and Scaling

The drawback of single-loop single-bit ΣΔ modulators with order higher than 2nd is their tendency to instability. The stability is defined as a modulator normal operating condition. All integrator outputs remain bounded over time with bounded input [1, 16]. In order to ensure the ΣΔ modulator operates stably, having chosen an optimized noise transfer function (NTF) to meet the specification. The analysis of stability is also important. Therefore, several methods can be used, among others simulation or calculation. The method of root-locus plots has been

commonly adopted to analyze the stability. For the unknown quantizer gain k, which has no definition in the case of a single-bit ΣΔ modulator, has been assumed as a variable gain when performing the root-locus analysis. Avoiding overloading the integrator output could sustain system stability [16].

2.4 CT Loop Filter Synthesis

In fact, CT ΣΔ modulators are mixed CT-DT systems. While the input signal is continuous and the loop filter is composed of CT integrators, the output signal is sampled. The feedback DAC signal can either have a constant output during each clock cycle (NRZ case), or have its output decay exponential (SCR case). Different feedback DAC waveforms make the calculation of the CT ΣΔ modulator loop filter coefficients difficult. The NTF is usually designed in such a way that the in-band quantization noise is sufficiently low to be neglected compared to the circuit transistors noise. After calculations of the proper CT coefficients required to obtain the desired NTF, these coefficients should be scaled for maximum output swing of the integrators.

In order to overcome problems associated with the design and analysis of mixed CT-DT systems, CT ΣΔ modulators can be designed entirely in the DT domain. A DT-to-CT transformation method can then be applied in order to obtain the equivalent CT ΣΔ modulator.

2.4.1 Equivalence between DT and CT

A general DT ΣΔ modulator is showed in Fig. 2.3, where $H_d(z)$ is the DT loop filter. A general CT ΣΔ modulator is also showed in Fig. 2.4, where $H_c(s)$ is the CT loop filter and $H_{DAC}(s)$ is the CT feedback transfer function. The objective is to

design the CT loop filter $H_c(s)$ for given a feedback DAC $H_{DAC}(s)$ and makes the CT loop gain $G_c(z)$ equals to DT loop gain $G_d(z)$. This can be expressed as below.

$$\begin{aligned} G_d(z) &= G_c(z) \\ \frac{X_d(z)}{Y_d(z)} &= \frac{X_c(z)}{Y_c(z)} \\ G_d(z) &= z[H_c(s)H_{DAC}(s)] \end{aligned} \tag{2.6}$$

where $G_d(z) = H_d(z)$

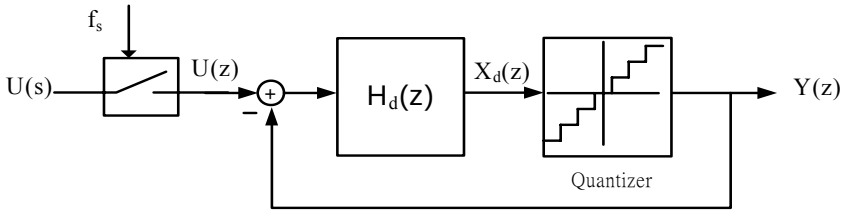


Figure 2.3 DT ΣΔ modulator

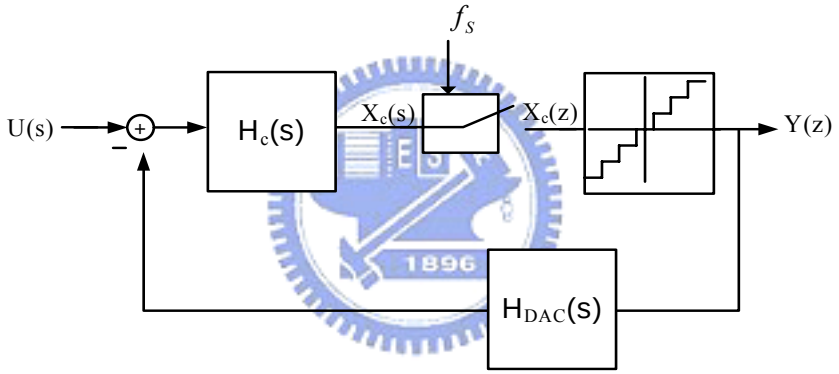


Figure 2.4 CT ΣΔ modulator

Previous work on ΣΔ DT-CT equivalence has usually solved (2.6) in the time domain using the following relationship:

$$Z^{-1}[G_d(z)] = [H_c(s)H_{DAC}(s)] \tag{2.7}$$

This transformation between DT and CT domain is called impulse invariant transformation, because it makes the open-loop impulse responses equal at the sampling times. Both modulators will produce the same output bit streams if we ensure that the inputs to their quantizers are the same, each quantizer would then make the same decision. Therefore two modulators are equivalent, if for the same input waveform, their quantizer input voltages at sampling instant are equal.

The complicated mathematics involved in the computation of time-domain convolution make this method not adapted to design systematically and has usually been used for specific cases [18, 19].

A more general transformation method, using state-space has been presented in [20]. Heavy use of matrix notation, singularity problems and the use of special control and optimization Matlab functions [21] make the use this transformation technique rather difficult.

Beside the DT-CT conversion, directly design a CT loop filter from its desired NTF is also published [6, 22]. This will probably be the upcoming method since it allows the optimization of the CT loop filter until it shows sufficient robustness against process variations, excess loop delay and clock jitter [6].

In this work we perform the DT-CT equivalence directly in the z-domain using *modified -z-transform* technique. While avoiding the complex mathematics necessary to perform time-domain convolution, this technique enables us to get the z-transform of signals having variations between two sampling instants. By using this method, the feedback DAC can be RZ or NRZ and the shape of the feedback signal can either be rectangular or non-rectangular.

2.4.2 Rectangular Feedback Signal

During a period T, the rectangular feedback signal, show in Fig. 2.5, can be describe in time-domain by following relationship:

$$h_{dac}(t) = u(t - t_d) - u(t - t_d - \tau) \tag{2.8}$$

where $u(t)$ is unit step function. The following equation is derived by applying the *Laplace* transform.

$$H_{DAC}(s) = \frac{e^{-t_d s} - e^{-(t_d + \tau)s}}{s} \tag{2.9}$$

The z-transformation of the CT ΣΔ loop gain can be expressed by

$$Z[G_d(z)] = Z[H_c(s)H_{DAC}(s)] \tag{2.10}$$

Substituting (2.9) into (2.10) results in

$$G_c(z) = Z[\frac{H_c(s)e^{-t_d s}}{s}] - Z[\frac{H_c(s)e^{-(t_d+\tau)s}}{s}] \tag{2.11}$$

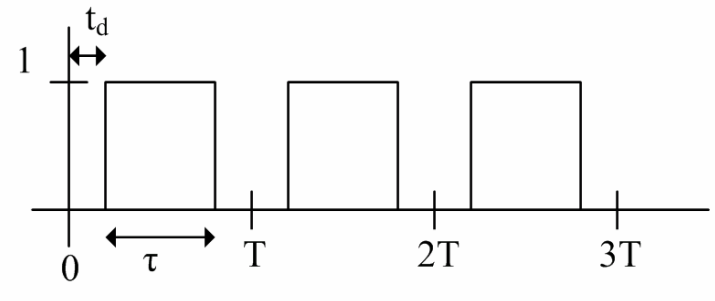


Figure 2.5 CT rectangular feedback signal

Equation (2.11) is rewritten in following form:

$$G_c(z) = Z_{m1}[\frac{H_c(s)}{s}] - Z_{m2}[\frac{H_c(s)}{s}] \tag{2.12}$$

where $m_1 = 1 - \frac{t_d}{T}$ and $m_2 = 1 - \frac{(t_d + \tau)}{T}$. In order to design a CT ΣΔ modulator which is equivalent to a DT ΣΔ modulator, we use equation (2.12) and (2.6) to get the general expression for DT-CT equivalence.

The method to calculate the *modified-z-transform* starting from the *Laplace* representation is the *Residue* theorem. This method is systematic and more convenient for design automatic. Equation (2.12) can be written in the following form:

$$\begin{aligned} G_c(z) = & \sum_{\text{pi=pole of } \frac{H_c(s)}{s}} \text{Residues of } \frac{H_c(s)e^{-m_1 Ts}}{s} \frac{e^{m_1 Ts}}{z - e^{Ts}}\Big|_{\text{at pi}} \\ & - \sum_{\text{pi=pole of } \frac{H_c(s)}{s}} \text{Residues of } \frac{H_c(s)e^{-m_2 Ts}}{s} \frac{e^{m_2 Ts}}{z - e^{Ts}}\Big|_{\text{at pi}} \end{aligned} \tag{2.13}$$

Using (2.13) the loop gain of the CT ΣΔ $G_c(z)$ can be expressed in DT z domain. Comparing coefficients of the numerator and the denominator of $G_c(z)$ with those of the DT loop gain $G_d(z)$, the coefficients of CT loop filter $H_c(s)$ could be obtained. In a special case of a NRZ feedback signal, with $t_d = 0$ and $\tau = T$, and by

substitution in (2.9), we have a well-known zero-order-hold relation:

$$H_{DAC}(s) = \frac{1 - e^{-Ts}}{s} \tag{2.14}$$

2.4.3 Decaying RC Feedback Signal

In fact, the rectangular feedback signal is commonly used in CT modulators. It is useful to design feedback with non-rectangular signals. First, it can be used to model non-idealities in the rectangular feedback, such as non-zero rise and fall time. The second is that the non-rectangular feedback shape is possible to reduce the modulator sensitivity to clock jitter noise (in this thesis section 3.2.2).

In this section we show the DT-CT transformation can be used for CT ΣΔ modulators with decaying RC feedback signals. A decaying RC signal is shown in Fig. 2.6.

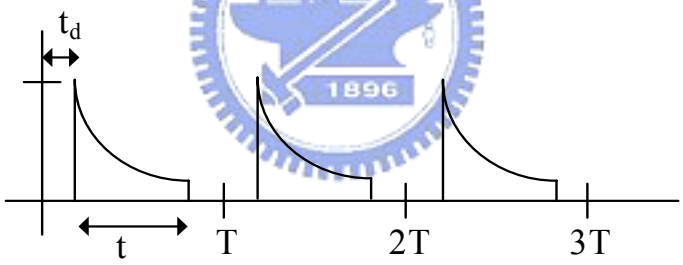


Figure 2.6 CT decaying RC feedback signal

Using the same method as described in section 2.4.2, the decaying RC feedback signal can be written in the time-domain by the following relationship:

$$h_{dac}(t) = e^{\frac{-1}{RC}(t-t_d)}[u(t-t_d) - u(t-t_d-\tau)] \tag{2.15}$$

The following equation is derived by applying the *Laplace* transform.

$$H_{DAC_{RC}}(s) = \frac{e^{-t_d s} - e^{-(t_d+\tau)s} e^{\frac{-\tau}{RC}}}{s + \frac{1}{RC}} \tag{2.16}$$

Substituting (2.16) into (2.10) results in

$$Z[G_c(s)] = Z[\frac{H_c(s)e^{-t_d s}}{s+\frac{1}{RC}}] - Z[\frac{H_c(s)e^{-(t_d+\tau)s}}{s+\frac{1}{RC}}]e^{\frac{-\tau}{RC}} \tag{2.17}$$

Using the *Residue* theorem, (2.17) could be derived in the following form:

$$G_c(z) = Z_{m1}[\frac{H_c(s)}{s+\frac{1}{RC}}] - e^{\frac{-\tau}{RC}} Z_{m2}[\frac{H_c(s)}{s+\frac{1}{RC}}] \tag{2.18}$$

where $m_1 = 1 - \frac{t_d}{T}$ and $m_2 = 1 - \frac{(t_d+\tau)}{T}$. The modified z transform can be calculated using *Residue* theorem method as describe in (2.13).

2.4.4 With an Additional Feedback Path

Loop delay is one of the major sources of instability and performance degradation in CT ΣΔ modulators. Loop delay is mainly due to the comparator response time and the latch propagation delay in the quantizer. It is also due to the propagation delay in the digital circuitry required to perform Dynamic Element Matching (DEM) of the feedback DAC elements in the case of multi-bit ΣΔ modulators. A loop-delay compensation is suggested to add an additional feedback signal into the quantize input, as indicated in Fig. 2.7 [2, 23].

In this section, we put an explicit delay of one period $\frac{t_d}{T} = 1$, or half a period, $\frac{t_d}{T} = 0.5$ in the feedback loop. This delay should be sufficiently large to include comparator and digital circuitry delay with enough margins to include additional delay due to signal dependency, process or temperature variations. The fixed half period delay or unit period delay in the feedback path can be introduced by a synchronization latch. The compensation coefficient kb is calculated by comparing loop gain transfer function $G_d(z)$ and $G_c(z)$, as written below:

$$\begin{aligned} G_d(z) &= G_c(z) \\ H_d(z) &= z[H_{DAC}(s)(k_b + H_c(s))] \end{aligned} \tag{2.19}$$

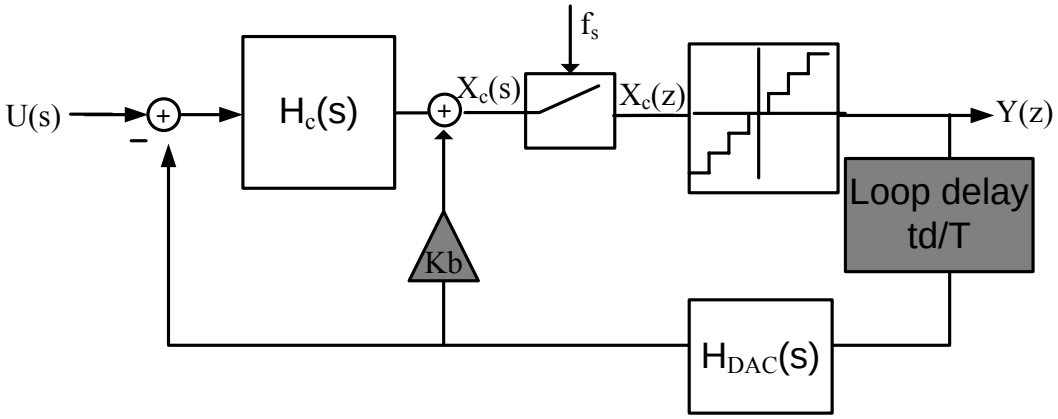


Figure 2.7 CT ΣΔ modulator with loop delay and compensation path Kb

The loop gain transfer function with loop-delay compensation could be written in the following form:

$$G_c(z) = z[\frac{1-e^{-Ts}}{s} e^{-\frac{t_d}{T}s}(k_b + H_c(s))] \tag{2.20}$$

Using the modified-z-transform and *Residue* theorem, we get:

$$G_c(z) = (1-z^{-1}) \sum_{\text{pi=pole of } \frac{k_b+H_c(s)}{s}} \text{Residues of } \frac{k_b + H_c(s)}{s} \frac{e^{mTs}}{z-e^{Ts}}\Big|_{\text{at pi}} \tag{2.21}$$

Comparing the coefficient of the numerator and the denominator of above $G_c(z)$ with those of the DT loop gain $G_d(z)$, the coefficients of the CT loop filter $H_c(s)$ and compensate kb coefficient could be obtained.

2.4.5 Design Examples

In this section we show a systematic design approach to calculate CT ΣΔ from well-known DT toolbox. Without loss of generality, two main topologies:

- CRFF: Cascade of Resonators Feed-forward Form, Fig. 2.8 and Fig. 2.9
- CRFB: Cascade of Resonators Feedback Form, Fig. 2.11 and Fig. 2.12

The DT ΣΔ coefficients have been obtained using Richard Schreier's ΣΔ Toolbox [21]. Using the design procedure written in above section, the CT ΣΔ coefficients were

obtain for NRZ and decaying RC signals.

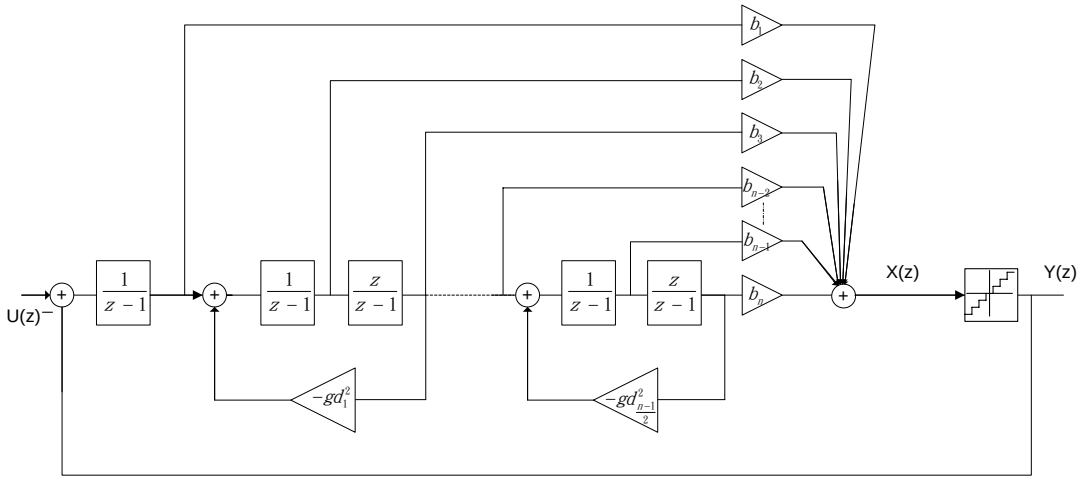


Figure 2.8 DT CRFF

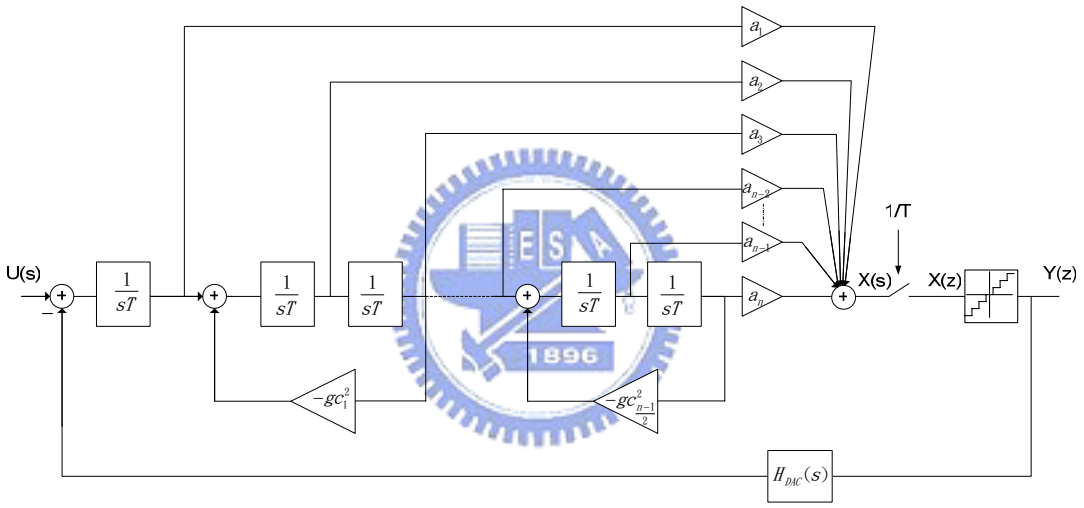


Figure 2.9 CT CRFF

We take CRFF third order, OSR=25 as an example. From the DT ΣΔ Toolbox, we could get the DT ΣΔ coefficients. Comparing (2.13), (2.21) with DT ΣΔ coefficients, the CT ΣΔ coefficients could be obtained. This design procedure has been implemented using the symbolic mathematical tool *MAPLE*. We could get the different CT ΣΔ coefficients with different feedback DAC waveforms. The CRFF third order modulator coefficients are listed in following Table 2.1. In order to prevent too large signal swing in the integrators, we let all integrator coefficients equal to 0.5 in the CTΣΔ modulators.

Table 2.1 CRFF third order modulator DT and CT coefficients

DT		CT NRZ (with t_d=0)		CT NRZ (with t_d=0.5)	
b1	0.752	a1	2.0247	a1	2.606
b2	0.574	a2	2.294	a2	2.605
b3	0.156	a3	1.246	a3	1.246
g_d^2	0.01	g_c^2	0.038	g_c^2	0.038
		kb	0	kb	0.581

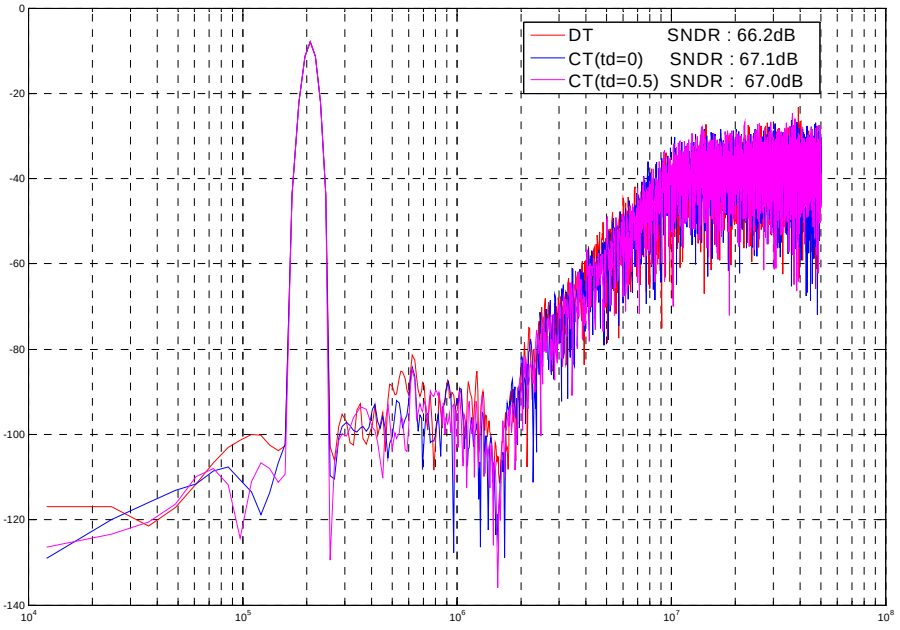


Figure 2.10 CRFF third order DT and CT Simulink PSD (OSR=25)

In order to study the behavior of the resulting CT ΣΔ modulators, the Matlab/Simulink simulations have been performed to compare them with DT ΣΔ. Fig. 2.10 shows the power spectral density (PSD) of the DT and calculated CT modulators. It is obvious from Fig. 2.10 the CTΣΔ modulators using the coefficient calculated using DT-to-CT transformation method are equivalent to the original DT ΣΔ

modulator.

Using the same method, we can also get the coefficients in the CRFB topologies with different feedback shapes those are rectangular or decaying RC waveforms. The CRFB topologies are shown as Fig. 2.11 and Fig. 2.12.

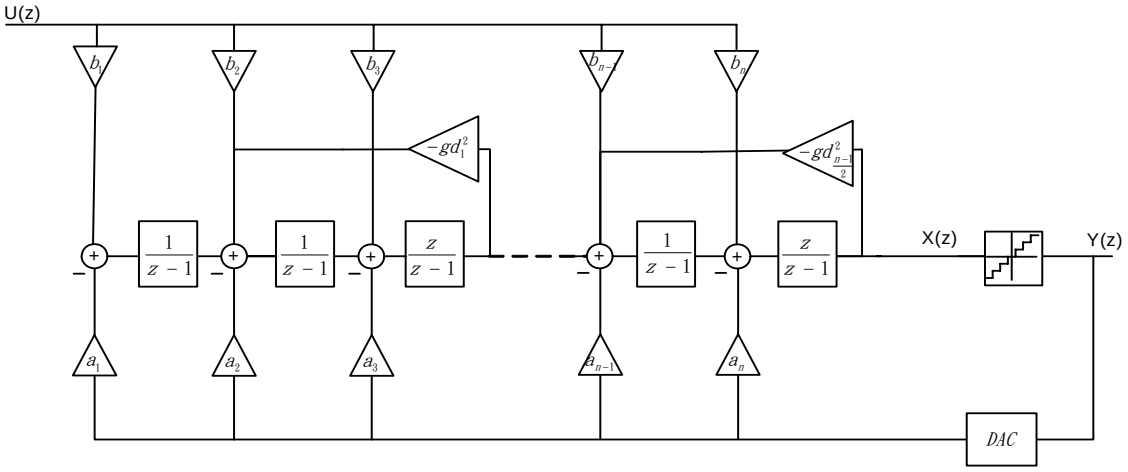


Figure 2.11 DT CRFB

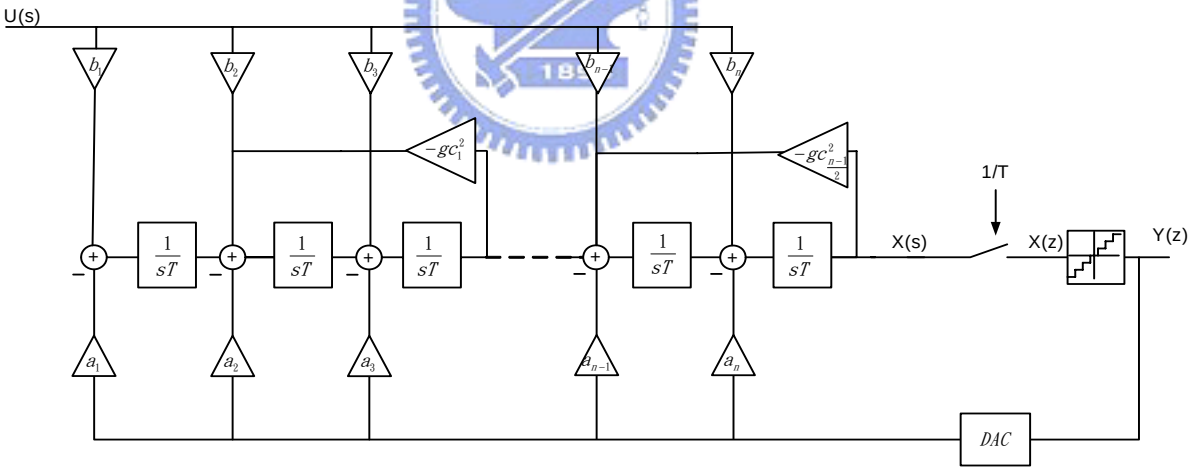


Figure 2.12 CT CRFB

Comparing (2.13), (2.18) with DT ΣΔ coefficients, the CT ΣΔ coefficients could also be obtained. The CRFB CT ΣΔ modulator coefficients with different feedback shapes are listed in Table 2.2

Table 2.2 CRFB third order modulator coefficients

DT		CT NRZ		CT (decaying RC with RC=0.1T_s)	
a1	0.0446	a1	0.3568	a1	3.5934
a2	0.2371	a2	0.9484	a2	9.7215
a3	0.5577	a3	1.3376	a3	13.9662
b1	0.0446	b1	0.3568	b1	0.3568
b2	0.2371	b2	0.9484	b2	0.9484
b3	0.5577	b3	1.3376	b3	1.3376
g_d^2	0.0095	g_c^2	0.038	g_c^2	0.038

In order to verify the coefficients in Table 2.2, we must build the decaying RC waveform in Matlab/Simulink for behavior simulations. The s-domain of decaying RC could be derived in the following form:

$$h_{DAC}(t) = e^{-\frac{1}{RC}(t-t_d)}[u(t-t_d) - u(t-t_d-\tau)]$$
$$\text{for RC decaying feedback } t_d = 0.5T_s \quad \tau = 0.5T_s \tag{2.22}$$
$$H_{DAC}(s) = \frac{e^{-0.5s} - e^{-s}e^{-0.5/RC}}{s + \frac{1}{RC}}$$

Because quantizer outputs must pass through a track-and-hold, the decaying RC derived from the combination of s-domain and z-domain could be shown as:

$$H_{T\&H}(s)RC(s,z) = H_{DAC}(s)$$
$$RC(s,z) = \frac{z^{-0.5} - z^{-1}e^{-0.5Ts/RC}}{1 - z^{-1}} \frac{s}{s + \frac{1}{RC}} \tag{2.23}$$

From above (2.23), we can easily build the decaying RC model in Matlab/Simulink,

as indicated in Fig. 2.13.

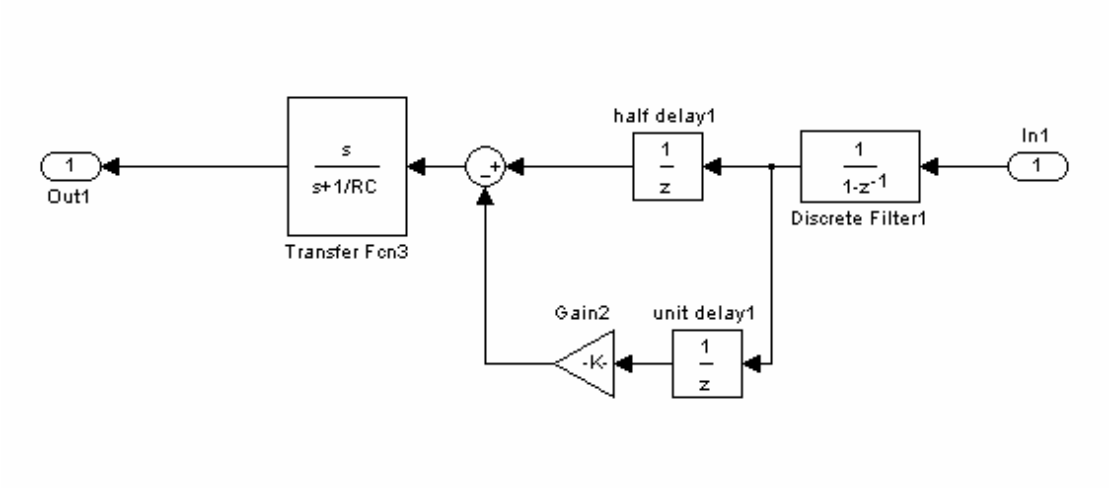


Figure 2.13 The RC decaying model in Matlab/Simulik

The simulation result of the decaying RC waveform is shown in Fig. 2.14, where the value of RC in this condition is $RC=0.1T_s$.

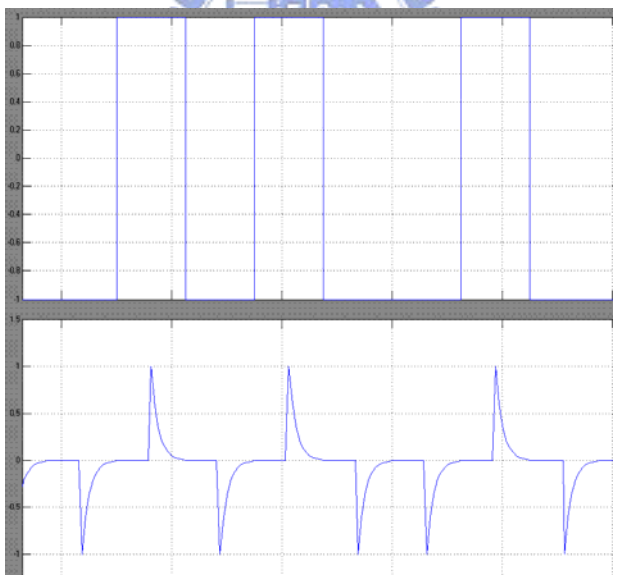


Figure 2.14 RC decaying Waveform simulations in Simulink

Fig. 2.15 shows the PSD of the CRFB third order ΣΔ of the DT and calculated CT modulators. It is obvious from Fig. 2.15, the CT ΣΔ modulators with rectangular and non-rectangular (decaying RC) feedback signals using the coefficient calculated using DT-to-CT transformation method is equivalent to the original DT ΣΔ modulator.

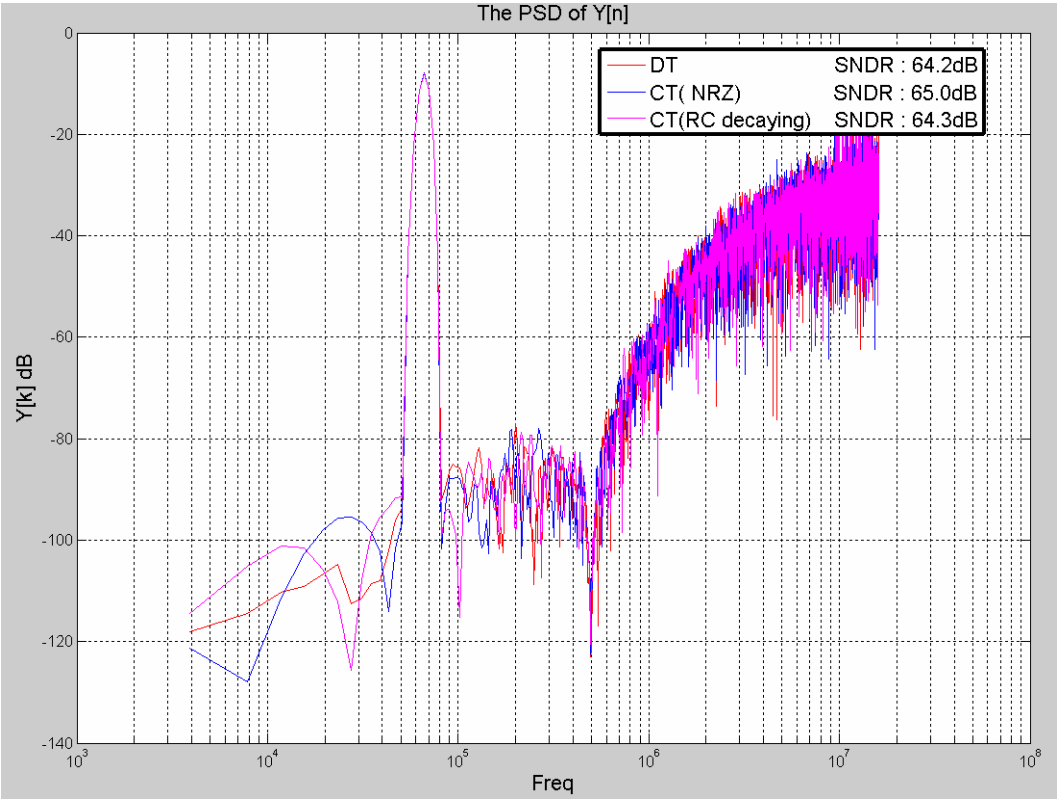


Figure 2.15 CRFB third order DT and CT Simulink PSD (OSR=25)

2.5 Architectures and Implicit Anti-Aliasing Feature

In this section, the differences of the most typical architectures (CRFF in Fig. 2.9, CRFB in Fig. 2.12) for the implementation CT ΣΔ modulator are present. Note that the CRFF has been derived from the CRFB by applying the flow graph reversal procedure [24].

2.5.1 Feed-Forward (FF) and Feedback (FB) Architectures

For a feed-forward architecture, the signal and noise transfer functions are identical, being high-pass filters with less attenuation in the signal band going from the first stage to the last one. Therefore, the first stage variable will contain only a very small component of the input signal and a large amount of filtered quantization noise. The non-linearity of the second integrator will not introduce in-band

components, but only out-of-band distortions. The last integrator will introduce the large amount of in-band distortions, but these will be shaped by the loop filter. For this topology, only the linearity of the input integrating stage is critical, all others are not detrimental to SNDR. However the feed-forward architecture shows reduced anti-aliasing behavior and in addition a strong STF peaking around the cutoff frequency.

In the case of CRFB topology, each state variable will contain some filtered quantization noise plus a filtered version of the input signal. Since the output of an integrator represents the input of the subsequent integrating stage, it follows that the linearity of the first integrating stage is more critical than the linearity of the final one. For the CRFB topology, the linearity of integrators is important for all stages. The second integrator requires almost the same linearity as the first one, and the specifications for the subsequent stages can be eased as one approaches the quantizer.

In the CRFF topology, the influence of the input integrator non-linearity is the same as in the case of CRFB topology, but the linearity of all other stages is not affecting SNDR to suck great extent. The STF of the feedback-compensated modulator has a flat response providing filtering to interferers.

Thus, in order to get a power efficient ΣΔ modulator while maintaining a good filtering characteristic, a combination of FF and FB has become popular [11]. In [11] the feedback path to the output of the first integrator has been replaced by a feed-forward path. As a consequence, the feed-forward approach adds a zero to the STF and resulted in reducing the filtering by one order and introducing a small peak near the cutoff frequency.

2.5.2 Implicit Anti-Aliasing Feature

In a DT system, Nyquist taught us that when the sampling rate is f_s, any two

tones which differ in frequency by a multiple of f_s are indistinguishable from one another and so overlap in a spectral plot. This problem is usually referred to as signal aliasing. DT ΣΔ modulators usually require an extra filter to be placed prior to their input to bandlimit the input signal and hence reduce the problem of aliasing. An implicit feature of CT ΣΔ modulators is that they have some built-in anti-aliasing protection.

It is easy to understand this intuitively by taking a first order low pass CT modulator as an example. In Fig. 2.16 the quantizer input in the z domain obeys the following relation:

$$x(n+1) = x(n) - y(n) + \frac{1}{T_s}\int_{nT_s}^{(n+1)T_s} u(t)dt \tag{2.24}$$

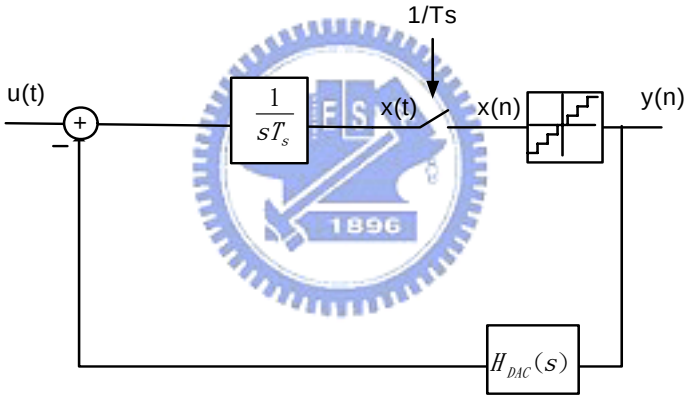


Figure 2.16 First order CT ΣΔ modulator

Notice that the input signal is integrated over one clock period prior to being sampled. The input is multiplied by a rectangular pulse. We may also write that input integral as a convolution of the input with a rectangular pulse:

$$\begin{aligned}\int_{nT_s}^{(n+1)T_s} u(t)dt &= u(t) * rect(nT_s, (n+1)T_s) \\ &= U(s)\cdot \sin c(\frac{f}{f_s})\end{aligned} \tag{2.25}$$

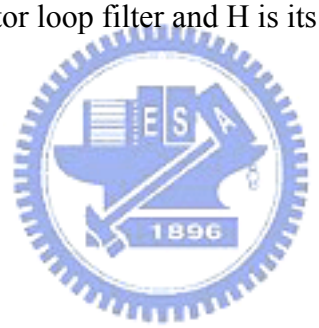
The convolution in the time domain is the same as multiplication in the frequency domain. Equation (2.25) tells us that the input spectrum is multiplied by the spectrum of a rectangular pulse, namely, a sinc function. This latter function has spectral nulls

at frequencies $\pm af_s$, $a \geq 1$. We are concerned about signals near multiples of the sampling frequency, which would alias to near dc, and that signals are attenuated by the sinc. In a CT modulator, the anti-aliasing property arises because the sampling happens after the integrator.

We would expect higher order modulators to have more antialias protection because they have more integrators before the sampler. In the general case, it has been shown that the implicit antialias filter for a CT ΣΔ can be plotted against frequency w by evaluating [19].

$$\frac{\hat{H}(jw)}{H(\exp(jwT_s))}, \tag{2.26}$$

where $\hat{H}$ is the CT modulator loop filter and H is its DT equivalent.



Chapter 3

Non-idealities in CT ΣΔ Modulators

In this chapter, we consider some non-idealities in CT ΣΔ circuit implements. We survey the literature on the performance effect of non-idealities in CT ΣΔ modulators and summarize the results that are germane to the design of CT ΣΔ modulators.

3.1 Errors of the Filters

The loop filter transfer function is the major performance determining part of a ΣΔ modulator, because it defines the NTF and therewith the quantization noise-shaping behavior. Without loss of generality, in the following active-RC integrators are considered, as showed in Fig. 3.1, shows a typical schematic with n_A inputs and with an amplifier transfer function A(s). With ki being the integrator scaling coefficients, the integrator transfer function (ITF) is the following form.

$$ITF(s) = \frac{k_i f_S}{s(1+\frac{1}{A(s)}) + \frac{1}{A(s)}\sum_{l=1}^{N} k_1 f_s} \approx \frac{k_i f_S}{s} \text{ (when } A(s) \to \infty) \qquad (3.1)$$

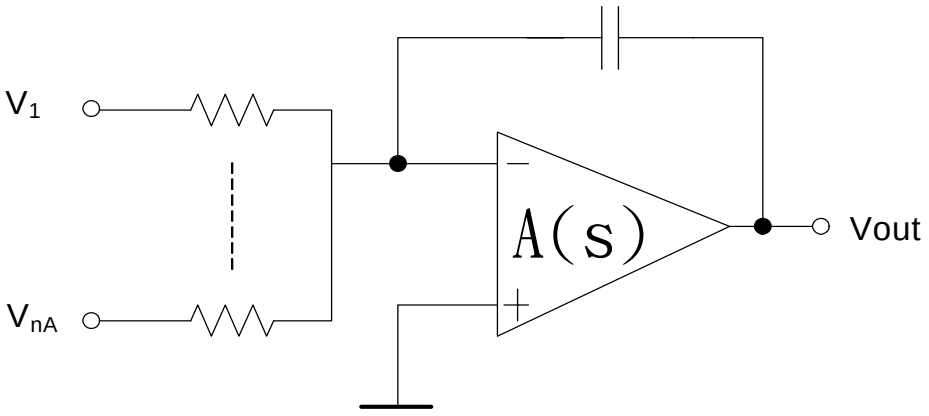


Figure 3.1 An active RC integrator with an amplifier

3.1.1 Gain Errors

Gain errors in CT modulators are more serious than an order of magnitude larger than in SC implements, because the integrator gains are mapped into capacitor relative ratios. These are intrinsically precise and variations are lower than 0.1% typically. In CT ΣΔ modulators integrator gains are mapped into resistor-capacitor product, which largely vary over process and temperature by values of ±30%.

It has been frequently reported that integrator gain variations have serious influence on single-loop ΣΔ modulators. A negative shift of the integrator gain yields less aggressive noise-shaping behavior and thus slightly higher IBN. In contrast, a positive shift of the integrator gain yields more aggressive noise-shaping, but this effect could lead to instability of the modulators. The time constant of the active-RC integrator is determined by the absolute product of the resistor and capacitor. It is possible to avoid this sensitivity by moving the poles of the signal transfer function of the modulator to cover a greater range of the RC-variation with a stable modulator [26]. The influence on the in-band quantization noise can be calculated from Equation (3.2), where ΔRC is the RC-variation value and a_1 is the first integrator coefficient.

$$IBN \approx \frac{\pi^6 \Delta^2}{84} \frac{(1+\Delta RC)^6}{a_1^2 OSR^7} \tag{3.2}$$

In Fig. 3.2 it is shown that RC variations influence on the CT ΣΔ modulators, which using NRZ half delay feedback, the coefficients as list in Table 2.1. Consequently, time constant tuning may become necessary [6, 11, 26]. Assume a reference clock is well defined, stable and low jitter, a simpler trimming of integrator time constants can be accomplished by digitally programming binary weighted capacitor arrays with switches [11]. In [26] a capacitive tuning is proposed to achieve a time constant accuracy less than ±10%.

For cascaded modulators, the behavior is even worse. Since these architectures depend on matching between analog and digital transfer functions. Nonetheless, a digital correction is possible and recent implementations prove the approach [27].

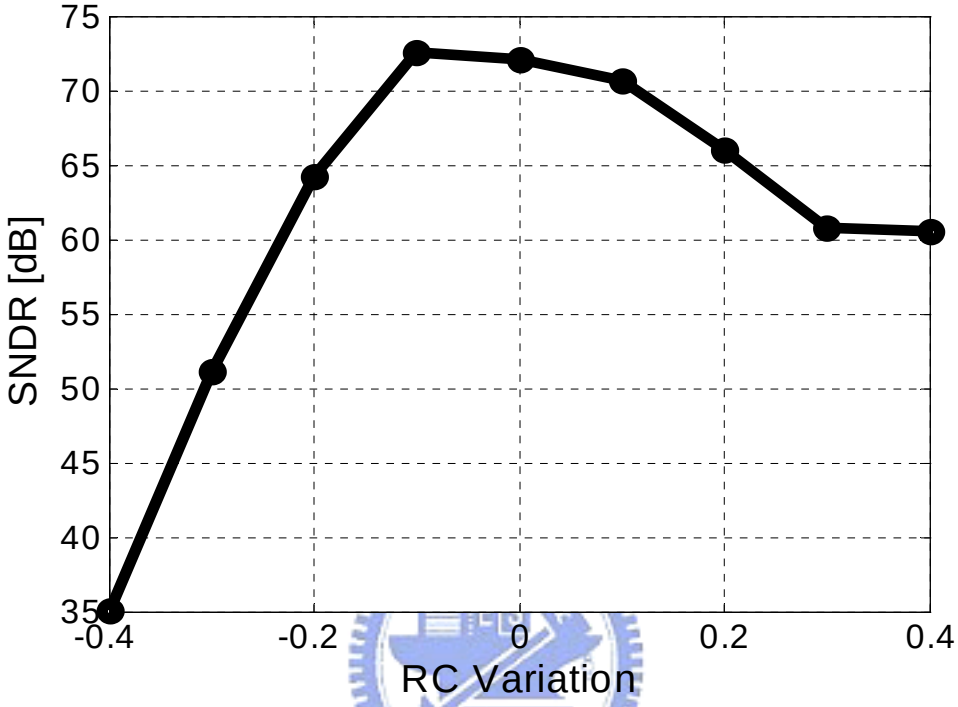


Figure 3.2 RC-variations influence of a CT modulator

3.1.2 Finite DC-Gain

Finite dc-gain shows the same effect as in DT implementations. Finite dc-gain causes the NTF zeros are moved away from dc to higher frequency as do the poles of the filters. In presence of a finite opamp gain can express in the following form [28]:

$$IBN \approx \frac{\Delta^2}{12}\frac{\pi^6}{7a_1^2}\left[\frac{1}{OSR^7}+\frac{21}{5OSRA_v^2}\right] \tag{3.3}$$

The critical gain of a 3rd order ΣΔ modulator is equal to

$$A_{v,3dB} \approx \sqrt{\frac{21}{5}}\frac{OSR}{\pi} \tag{3.4}$$

3.1.3 Finite Gain Bandwidth

CT implementations are claimed to work with lower GBW of the opamps. This has been attributed to the lack of the high current peaks of SC implemented DT circuits. Nevertheless, in [29] for a 3rd order modulator a margin of around 1.5fs was found; [30] claimed an integrator non-dominant pole of 2-3 times the sampling frequency. Recently, [31] a finite amplifier model was introduced. With $GBW = A_{dc} w_A$ and $A(s) = \frac{A_{dc}}{\frac{s}{w_A} + 1}$ from (3.1), the ITF can be derived as:

$$ITF_{GBW}(s)\Big|_i = \frac{k_j f_s}{s} \cdot \frac{\frac{GBW}{GBW + \sum |k_j f_s|}}{\frac{s}{GBW + \sum |k_j f_s|} + 1} \tag{3.5}$$

Consequently, the non-ideal influence of finite GBW is in first order approximation a gain error and a non-dominant pole. For rectangular feedback the non-dominant pole can be modeled as feedback delay. Thus, compensation is possible as correction of gain errors and excess loop delay [32]. In Fig. 3.3 the integrator with finite GBW is simulated for NRZ feedback pulse form.

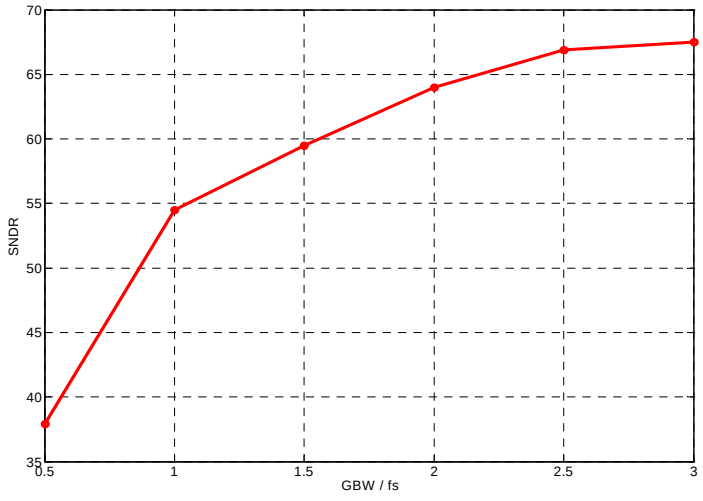


Figure 3.3 SNDR of the 3rd order modulator with finite GBW opamps

3.1.4 Further Filter Non-Idealities

Beside finite dc-gain and bandwidth in opamps, many other filter non-idealities exist, while a short overview is given here:

Finite slew rate is a nonlinear effect and causes distortion as well as an increase of the noise floor: in DT implementations signal transitions are very fast SC-pulses and finite slew rate yields incomplete signal settling. By using CT circuitry, the slew rate specifications can be relaxed. This is because in CT modulators the signals changed much more slowly than DT ones.

Circuit noise is generally designed as the dominant noise source in a ΣΔ modulator. The main contributor is the first integrator. There exists no sampling capacitor in CT ΣΔ modulators. For the low noise consideration, this requires larger transconductances and consequently higher bias current. The circuit noise and power relation was written in following form:

$$\overline{v_n}^2 \propto \frac{1}{g_m} \propto \frac{1}{\sqrt{I_{DS}}} \tag{3.6}$$

The input referred noise power density is approximately in the following relationship:

$$S_i^2 = 8kT(R_{in} + R_{DAC} + \frac{2n_{e,th}}{3gm_{,in}}) + \frac{K_f n_{e,f}}{C^2{}_{ox} WLf} \tag{3.7}$$

Note that since the noise is not sampled until it has been filtered. The aliased noise components are attenuated by noise-shaping. Therefore, the input referred noise power that appears in the signal band is equal to:

$$\overline{v}^2{}_{in,therm} = \frac{8kTa_i}{OSR \cdot R_{in} C_1}(R_{in} + R_{DAC} + \frac{2n_f}{3gm_2}) \tag{3.8}$$

We require smaller resistances (R_{in} and R_{dac} respectively) and a larger transconductance and consequently higher bias current in low circuit noise design.

Non-linearities of the first filter stage are similarly important as the linearity of

the feedback DAC. The voltage dependency of the amplifier dc-gain, the output impedance and the integrator resistors may introduce substantial distortion especially at larger input amplitudes. To reduce non-linearities, the input resistors should be as large as possible [33], limited by thermal noise. Also, increasing the bias current in the differential pair improves the linearity of the input stage. The limited output swing, also know as clipping, is a signal-dependent variation of the system states from their ideal values and results in severely increased the signal band noise as well as distortion.

3.2 Errors of the Feedback DAC

3.2.1 Excess Loop Delay

In [2, 7] timing non-ideality known as excess loop delay was considered. The excess loop delay can arise from two different effects：first, due to a finite respond time of the DAC output to the clock edges and its input [7]；Second, due to a designed delay between the quantizer sampling edge and the subsequent latch feeding the DAC, The delay shifts the DAC pulse into the next sampling instant. This is the case for NRZ DAC with any delay, shown in Fig. 3.4.

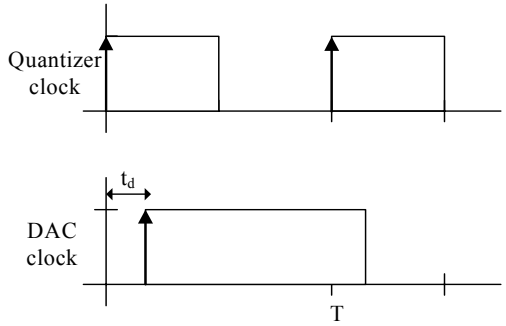


Figure 3.4 Illustrate of NRZ DAC pulse with loop delay

Excess loop delay is a serious non-ideality because it alters the equivalence between the CT and DT representations of the loop filter and causes the numerator

order of transfer function increases by one. Its effect on performance is severe if the sampling clock speed is an appreciable fraction (10% or more) of the maximum transistor switching speed. This is becoming more likely nowadays as desired conversion bandwidths increase and a ΣΔ modulation with an aggressively high clock rate relative to the transistor switching speed is considered for the converter architecture [34].

3.2.2 Clock Jitter

Clock jitter, that is statistical variations of the sampling frequency, depends on the purity of the clock source. In the past, ΣΔ modulators were found to be tolerant to timing jitter. Nonetheless, this advantage only holds in DT implementations. In contrast, CT modulators are affected much more severely by clock jitter, which is seen as the major disadvantage of CT ΣΔ implementations. The clock jitter influence on CT ΣΔ modulators can be illustrated in Fig. 3.5.

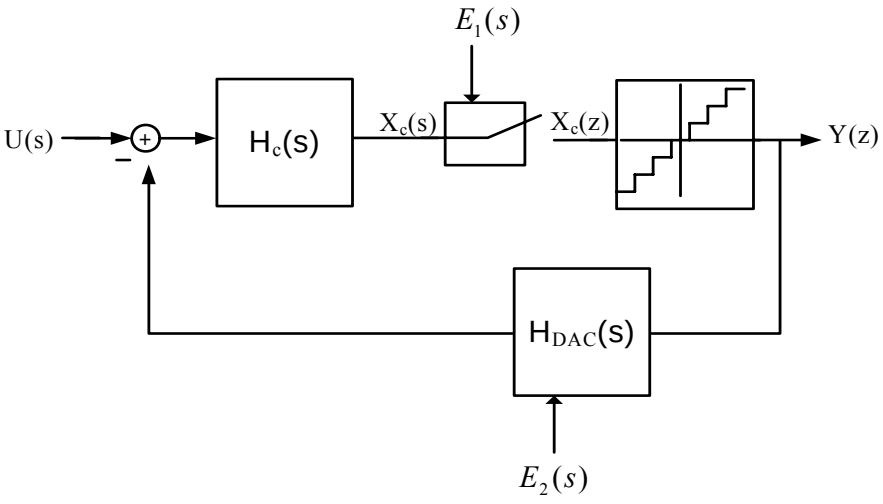


Figure 3.5 Jitter error sources in CT ΣΔ modulators

There are two different sources of clock jitter errors (E_1 and E_2) in the modulator loop. The sampled internal quantizer is prone to jitter, but this error E_1 is maximally

suppressed by the modulator loop. The dominant jitter error in CT implementations appears through the feedback DAC error E_2. A CT ΣΔ modulator integrates the feedback waveform and a statistical variation of the feedback results in a statistical integration error and in increased noise.

The random variation in the delay time t_d is called pulse-delay jitter and the random variation in pulse-width τ is called pulse-width jitter. These two types of jitter are illustrated in Fig. 3.6.

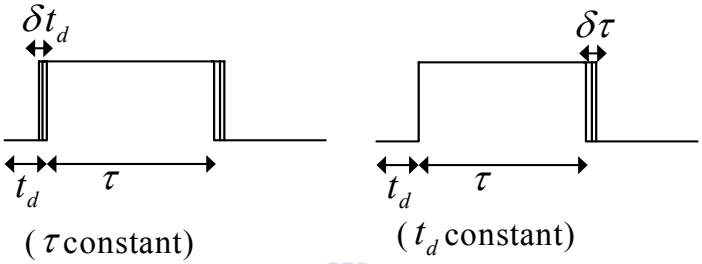
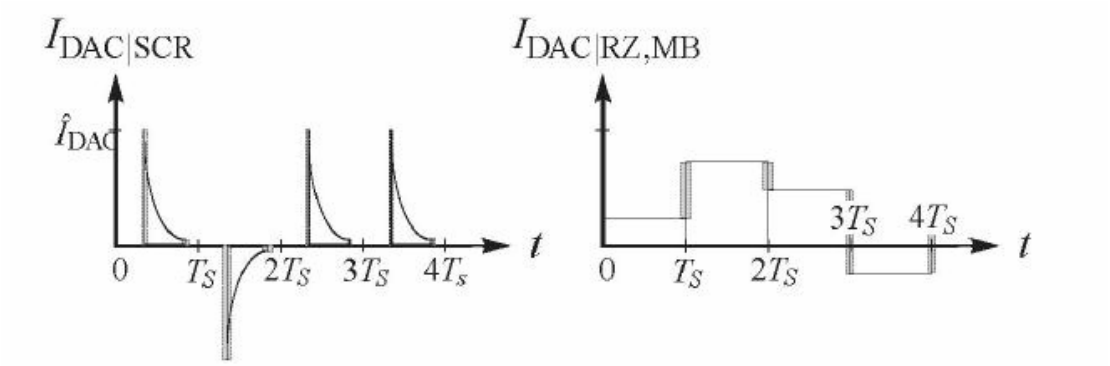
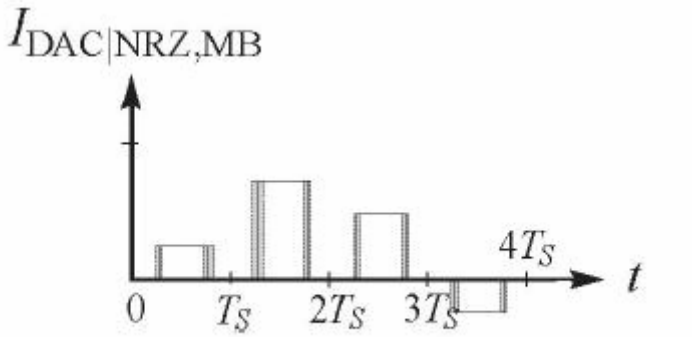


Figure 3.6 (a) Pulse-delay jitter (b) Pulse-width clock jitter

It has been shown that pulse-delay jitter is much less critical than pulse-width jitter [35]. Thus, several methods to reduce the clock jitter sensitivity will be introduced. In [36] a technique with exponentially decaying, switched-capacitor-resistor (SCR) feedback in CT ΣΔ modulators have been employed, as shown in Fig. 3.7a .In the following, different feedback waveforms like sinusoid [37], linear or quadratically decaying were proposed [38]. Beside this, multi-bit DAC implementations also reduce the jitter sensitivity. This is because that the smaller step size reduced the charge error. But it must be noted that only NRZ multi-bit feedback effectively reduces clock jitter noise, but not the often employ RZ multi-bit feedback, as illustrated in Fig. 3.7b, 3.7c.



(a) Exponential DAC pulse (b) Multi-bit NRZ DAC pulse



(c) Multi-bit RZ DAC pulse

Figure 3.7 Exponentially decaying and multi-bit NRZ and RZ pulse sequence under clock jitter influence.

In order to reduce the large sensitivity to jitter, [48] also proposed to use SC pulse in a CT modulator. SC feedback is usually adopted in DT charge integrators. In the CT domain, the integration is done over one clock period. Thus, the pure charge feedback is not directly applicable. To be able to define the feedback pulse over time, an SC is combined with an additional series resistor. The resulting architecture is shown exemplarily in Fig. 3.8, where the DAC circuit is named SCR feedback. Due to its influence on the feedback pulse shape, the additional resistor also allows the definition of the jitter sensitivity over the feedback time constant and reduces the speed requirements of the active parts of the modulator.

$$\tau_{RC} = R_R C_R = bT_S \tag{3.9}$$

Note that, the τ_{RC} lowest limit is the switch turn on resistor r_{on}. If $r_{on} > R_R$, then the τ_{RC} time constant will be dominant by switch turn on resistor r_{on} [36].

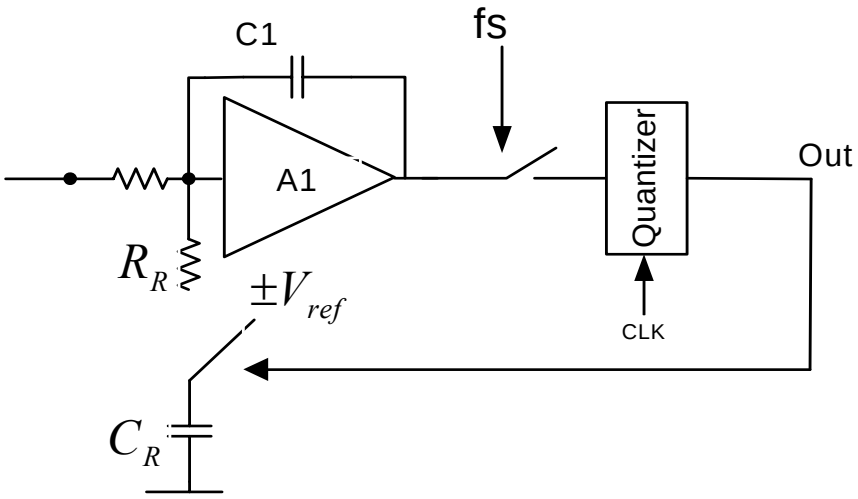


Figure 3.8 A ΣΔ modulator with SCR feedback

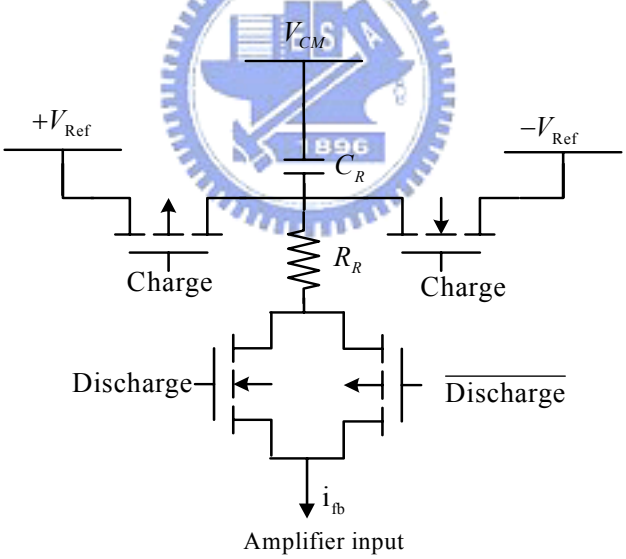


Figure 3.9 Implementation of the SCR feedback circuit

A unit of SCR feedback DAC cell as in Fig. 3.9. Principally the SCR feedback DAC has two modes of operation: first charging the capacitors C_R to either the positive or negative reference voltage, depending on the quantizer digital output signal V_{out}, and then discharging the capacitors over the resistors R_R to the input of

the integrators. To simplify the system design, these phases were chosen equal to the system clock phases. We take the first half of the clock cycle to charge the feedback capacitors, depending on the comparators output, and discharge it in the second half, translating into a feedback pulse position. Here the capacitor C_R is charged on either positive or negative reference voltage when $\text{Charge} = Clk \cdot V_{out}$ is high. It is discharge over R_R to the integrator input when $\text{Discharge} = \overline{Clk}$ is high.

In order to have the jitter relaxation benefits of multilevel DAC while maintaining high linearity, Finite Impulse Response (FIR) DAC can be used in as reported in [39,49]. The quantizer is one bit and the DAC response pulse is widened over n clock cycles and the jitter contribution is approximately averaged over n periods. In [39] it is reported that using 9-level instead of 2-level DAC reduces the jitter noise contribution by 18dB. By using this FIR DAC method, it also increased loop delay and lead to stability problem.

3.2.3 Jitter Noise Power Analysis

The pulse-width jitter has a much more degrading effect on the SNR than the pulse-delay jitter. In the following analysis, we will neglect the pulse-delay jitter and only the pulse-width jitter will be taken into account.

In order to calculate the noise power generated by the pulse-width clock jitter, let us look at the output of the first integrator of the modulator in the ideal case.

$$\frac{1}{T_s}\int_{t_d}^{t_d+\tau}\frac{T_s}{\tau}dt = 1 \tag{3.10}$$

If the pulse-width has an error of $\delta\tau$, the output of the first integrator will be

$$\frac{1}{T_s}\int_{t_d}^{t_d+\tau}\frac{T_s}{\tau}dt = 1+\frac{\delta\tau}{\tau} \tag{3.11}$$

The error in the output of integration is then equal to $\frac{\delta\tau}{\tau}$. Assuming that the clock jitter causes timing errors $\delta\tau$ with variance σ_j^2, we can say that the jitter noise power in the signal band is equal to

$$\text{Jitter Noise Power}|_{\text{NRZ}} = \frac{\sigma_j^2}{\tau^2}\frac{f_s}{2OSR} \tag{3.12}$$

The signal-to-jitter noise ratio (SNR_j) can then be described by the following relation:

$$SNR_j = \frac{\alpha^2\tau^2}{\sigma_j^2}\frac{OSR}{f_s}, \tag{3.13}$$

where α^2 is the amplitude of the sinusoidal input signal. From equation (3.13), we can see that SNR_j is directly proportional to τ. Since in the NRZ case $\tau = T_s$ and in the RZ case, $\tau < T_s$, it is clear that CT ΣΔ modulators with a RZ feedback signal are more sensitive to clock jitter than modulators with a NRZ feedback signal. Using the same method, we can also derive jitter noise powering the SCR feedback in the following form:

$$\text{Jitter Noise Power}|_{\text{SCR}} = N_j|_{NRZ}\left(\frac{T_s}{2\tau_{RC}}\right)^2 e^{-\frac{T_s}{\tau_{RC}}} \quad ; \tag{3.14}$$

where $N_j|_{NRZ}$ is NRZ jitter noise power

It is obvious that the improvement is only dependent on the exponential decaying multiplication of τ_{RC}.

Another interesting solution to reduce CT ΣΔ modulators sensitivity to clock jitter is to use a multi-bit quantizer [45, 46]. The feedback DAC step size in a multi-bit modulator is significantly lower than in the 1-bit case. Thus, the jitter sensitivity is reduced proportionally. In fact we can say that:

$$\text{Multibit Jitter Noise Power} = \frac{\text{Single bit Noise Power}}{(\text{Number of Quantization Steps})^2} \tag{3.15}$$

Pulse waveform asymmetry is also reduced by the same amount as clock jitter noise. Equation (3.15) is valid only for NRZ feedback signals. In a RZ feedback signal, large transitions occur at each clock cycle. This results in higher jitter and pulse waveform asymmetry similar to monobit modulators. If nonlinearity due feedback pulse asymmetry needs to be reduced, a RZ feedback signal could be used [45, 46].

3.2.4 Jitter Noise Model

In order to model the jitter noise in system level simulation, the following method is often used. Fig. 3.10 shows the block diagram of a generic single-loop CT ΣΔ. In such a system, there are two points that require a precise clock signal, the sampler S before the quantizer and the DAC that generates the feedback pulse p(t). The clock timing error in DAC ΔT_{DAC} may not have the same timing error in the sampling clock ΔT_Q

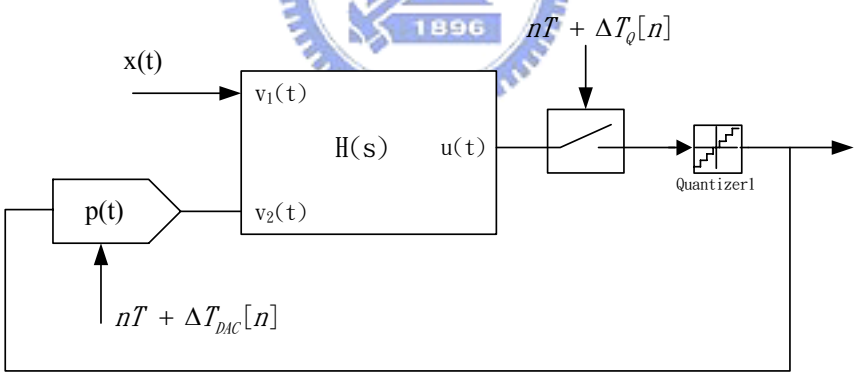


Figure 3.10 Block diagram of a CT ΣΔ modulator including timing uncertainties

We will not consider ΔT_Q in our model because it does not contribute significantly to increase the precision of the predictions and simulations. In general, DAC timing uncertainties $T_{DAC}[n]$ result in a wrong position of the feedback pulses and also in an error in its duration, as shown in Fig. 3.11.

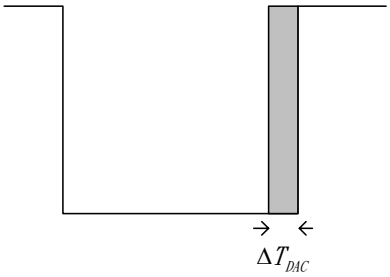


Figure 3.11 Feedback DACs timing error

For a NRZ feedback pulse, the expression of this error area is:

$$\Delta A[n] = \left(y[n] - y[n-1]\right) \cdot \Delta T_{DAC}[n] \tag{3.16}$$

We may find the equivalent additive error sequence that produces the same area error in a feedback pulse train with the ideal temporization:

$$e_j[n]\frac{\Delta A[n]}{T} = \left(y[n] - y[n-1]\right) \cdot \frac{\Delta T_{DAC}[n]}{T} \tag{3.17}$$

This simple equation (3.17) leads to the model of Fig. 3.12,

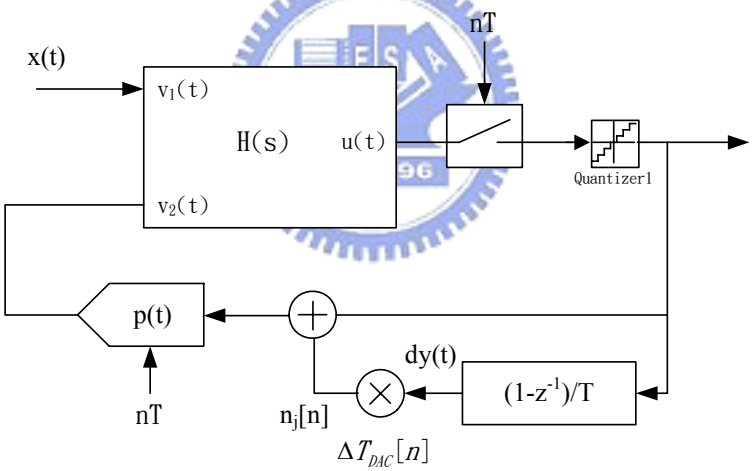


Figure 3.12 The Block diagram of a CT ΣΔ modulator including an additive jitter model.

By adding this jitter noise model in Matlab/Simulink, we can success to simulate the jitter noise effect the CT ΣΔ modulators. The following Fig. 3.13 is the simulation result. In here, the amount of jitter is normalize to clock period and represented in percentages of clock period. For an example, the jitter equals to 1% of clock period at 100MHz sample frequency that also indicates clock jitter equals to 100p.

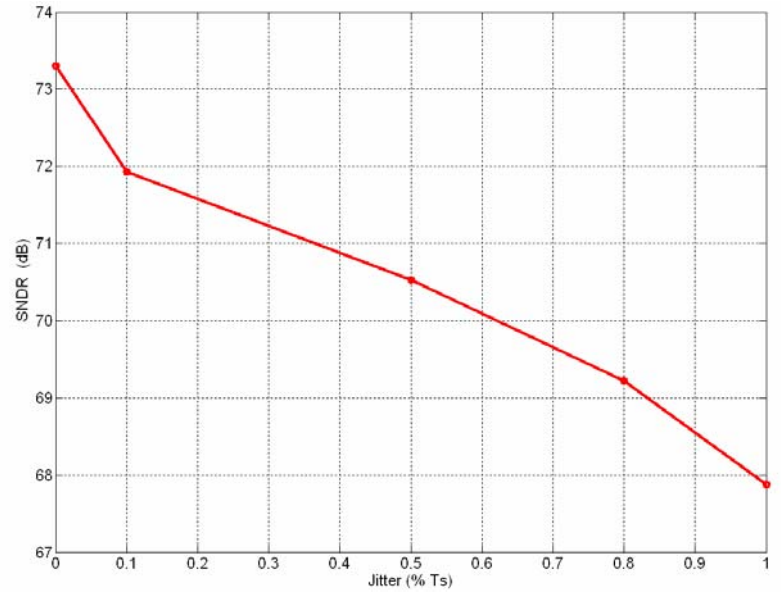


Figure 3.13 SNDR of the 3rd order modulator with the jitter noise model

3.2.5 Further DAC Non-Idealities

Beside the timing non-idealities, there are some other DAC non-idealities, which be mentioned here. The finite DAC response time and consequently non-equal rise and fall times of the feedback pulse cause a charge mismatch for RZ or even inter symbol interference (ISI) for NRZ pulses. When DAC output current pulses, having unequal rise and fall times, are integrated, the result of the integration depends on the data sequence. This data dependency produces harmonic distortion. As shown in Fig. 3.14, the effect of this feedback waveform asymmetry can be highly attenuated by using a RZ feedback signal.

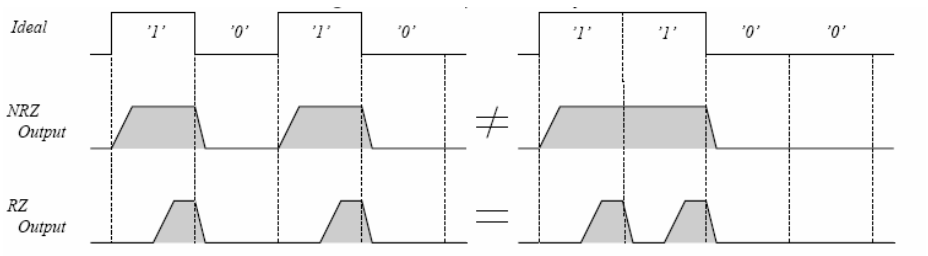


Figure 3.14 Rise and fall time asymmetry

DAC non-linearity is similarly important in CT as in DT modulators, since the low resolution feedback DAC needs linearity as good as the overall modulator. This is due to that DAC errors are directly fed into the input of the modulator. Therefore the feedback DAC requires linearity better than the overall modulator. Many techniques have been published to improve the DAC linearity, such as dynamic element matching (DEM) [3, 13] or current calibration [5, 14].

Finite output impedance of the feedback current sources becomes especially important in Gm-C filters realizations. Here, the feedback current steering DAC sees the full filter output swing and thus DAC finite output impedance reduces the linearity.

3.3 Errors of the Internal Quantizer

The quantizer is located at the most insensitivity. This is why ΣΔ modulators are mostly insensitivity to errors of the internal quantizer, which are usually offset, hysteresis [42]. Nonetheless, in CT modulators have to be paid for quantizer timing issues. This is caused by timing induced errors like propagation and signal dependent delay：An excess loop delay can be caused by the internal quantizer. More severely, the delay of the decision is dependent on the signal amplitude. A statistically variant quantizer delay causes equivalent performance degradation as clock jitter [43]. This signal dependent delay is easily circumvented by inserting a latch between the quantizer and the feedback DAC. Thus, the quantizer has a constant time to settle.

Chapter 4

Analysis on Different Loop Delay Compensation

The excess loop delay degrades the CT ΣΔ modulators performance in section 3.2.1. There exist some methods to compensate for the excess loop delay. We explore some past proposals and suggest some methods for practical implementations.

4.1 Excess Loop Delay Compensation

In general, in a CT modulator with enough excess loop delay to push the falling DAC pulse edge past a sampling period, the order of the equivalent DT loop is one higher than the order of the CT loop filter. Thus, we use an RZ DAC instead of an NRZ DAC, the loop gain in CT modulators $G_c(z)$ would remain the same order as the loop gain in DT modulators $G_d(z)$ for t_d<0.5. If we knew exactly what t_d is, we could select suitable loop filter coefficients to get exactly the equivalent DT-CT transformation. Thus, for a given t_d<0.5 and RZ DAC pulses, we can make our CT loop gain $G_c(z)$ matched exactly the desired DT loop gain $G_d(z)$. It has long been recognized that it is sensible to use RZ DAC pulses in CT modulators for excess loop delay consideration.

If there exists enough excess delay to push the falling edge of a DAC pulse past a sampling period, it will increase the modulator order by one. Therefore, there will be (n+1) coefficients in the numerator of the equivalent $G_c(z)$; with only n feedback coefficients, the system is not fully controllable. By adopting a tuning approach where

each coefficient is tuned iteratively until the DR is maximized, it is possible to improve the DR. The tuned performance is still not as good as the no excess delay, but it is an important performance improvement compared to the untuned coefficients performance. It is a strong encouragement to design tunable coefficients, possibly even for on-line calibration against process and temperature variations. How to design a tuning algorithms to get maximize SNDR that works on a chip, perhaps even while the modulator is operating, is an interesting topic for future research [7].

An additional feedback path should restore full controllability to the system. This has been suggested in [2]. In the block diagram of Fig. 2.7, a second NRZ feedback path was added whose output goes directly to a summing node after the final integrator (that is immediately prior to the quantizer).

As mentioned above, the excess loop can be compensated by several methods. A commonly useful method is an additional NRZ feedback path that added whose output goes directly to a summing node after the final integrator. While the excess loop delay is not over a quantizer sampling clock period ($0 \le t_d \le T_s$), a CT ΣΔ modulator with the feedback delay can be compensated to get the performance as good as no delay.

In the following sections, we analyze a CT ΣΔ modulator with different loop delay compensation based on some mathematic theorems. We take third order as an example. First, we get different ΣΔ modulators coefficients by using the *modified Z* transform in section 2.4, we can get the following CRFF third order modulators coefficients with different loop delay compensation, listed in following Table 4.1.

We found that the longer delay compensation modulators need larger a1, a2, a3 and additional feedback kb coefficients. From coefficients listed in Table 4.1 above, CT ΣΔ modulators performances were verified by using Matlab/Simulink. The power spectral density is shown in Fig. 4.1 respectively. With different loop delay

compensation, they get almost same performances.

Table 4.1 Coefficients of CRFF third order modulators with different delay

CT NRZ	a1	a2	a3	g_c^2	kb
t_d=0	2.0247	2.294	1.246	0.038	0
t_d=0.125	2.1706	2.372	1.2464	0.038	0.131
t_d=0.25	2.3213	2.45	1.2464	0.03786	0.2714
t_d=0.5	2.606	2.605	1.246	0.038	0.581
t_d=1	3.328,	2.917	1.2464	0.03786	1.3251

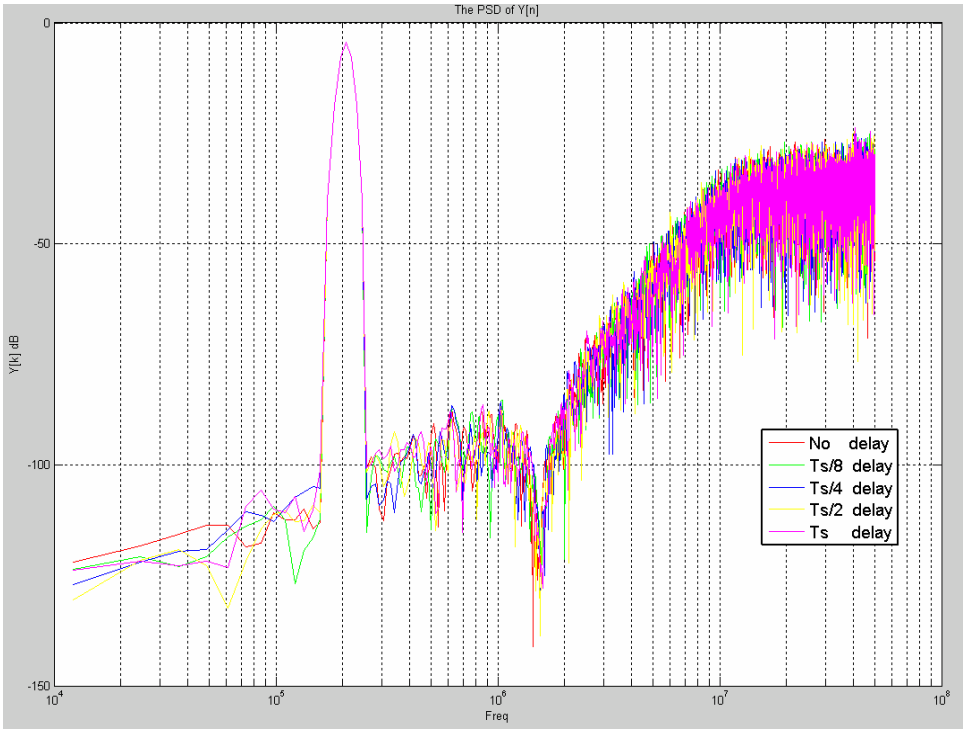


Figure 4.1 CT CRFF third order modulators with different loop delay compensation PSD in system level (OSR=25)

4.2 Noise Power Gain (NPG)

Component variations lead to changes of the designed NTF such that ΣΔ

modulators performances may be degraded. The ΣΔ modulators may even become unstable. Some stability constraints must be used to examine the NTF's stability. Noise power gain (NPG) limitation described in [17] can be used to examine the stability of a ΣΔ modulator. The NPG is defined as following form.

$$NPG = \frac{1}{\pi}\int_0^{\pi} \left(\left|NTF(e^{jw})\right|\right)^2 dw \qquad (4.1)$$

The NPG is the amplification factor of the quantization noise. Large NPG will increase high-frequency noise, which may result in destabilization of the modulator loop. The NPG_{max} defined as that a ΣΔ modulator has stable operation in the region below the corresponding instability edge, which is the boundary between stable and unstable regions. It is the maximum allowable NPG.

4.2.1 Boundary of Noise Power Gain

By aggressively selecting an NTF close to the instability edge, a large PSNDR can be obtained. However, the NPG of an aggressive NTF may be easily changed from a stable region to an unstable region due to a ΣΔ modulator coefficient variations resulting from large RC absolute variations in recent CMOS process. The NPG value may be larger than NPG_{max}, result in destabilization a ΣΔ modulator.

While it is well-known that low order ΣΔ modulators are subject to in-band tone problems, it should be remembered that high-order ΣΔ modulators could also have large in-band tones. These tones cannot be efficiently reduced even when a ΣΔ modulator is implemented with fully differential circuits because the odd harmonics may be larger than the even ones. To overcome this problem, we should maintain NPG large enough to reduce in-band tones. We should let NPG larger than NPG_{min} such that the SNR is dominated primarily by the in-band noise floor. In contrast, if the NPG is below NPG_{min}, the SNR is dominated primarily by the in-band tones.

4.2.2 NPG Values of Different Delay Compensation

Since the stability of a ΣΔ modulator is examined in terms of NPG limitations, variations of NPG due to modulator RC product variations with different delay compensation have to be investigated. We use the loop filter coefficients listed in Table 4.1. The NPG values of different delay compensation are shown in Fig. 4.2. When RC variations equal zero, which means no process variations, the NPG value in different delay compensation is the same. That is because their NTF is mapped into the same DT ΣΔ transfer function. Now, process variations alter the NTF, which alter NPG and lower the effective SNR. In Fig. 4.2, in a negative shift of time constant, the NPG of the modulator with longer delay compensation increases rapidly. When the NPG is increased over NPG_{max}, it results in destabilization of the modulator.

In contrast, in a positive shift of time constant, the NPG alters smoothly. Those do not affect stability issue, so there is no larger different performance. Considering negative shift and positive of time constant together, we found that a ΣΔ with less delay compensation produces a low-process variations sensitivity design.

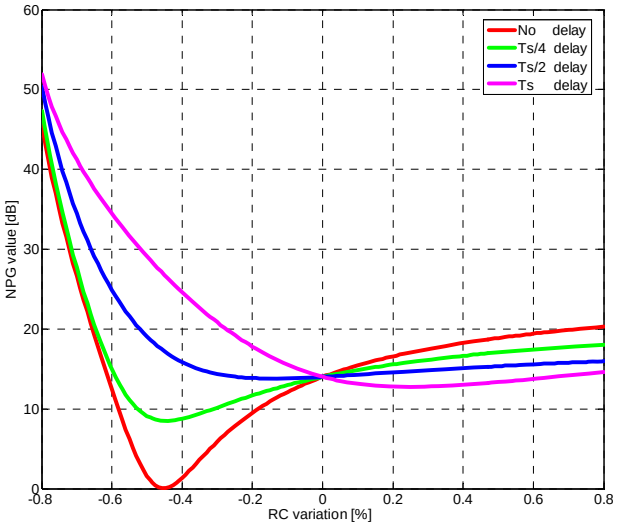


Figure 4.2 Third order NPG of different delay compensation in RC variations

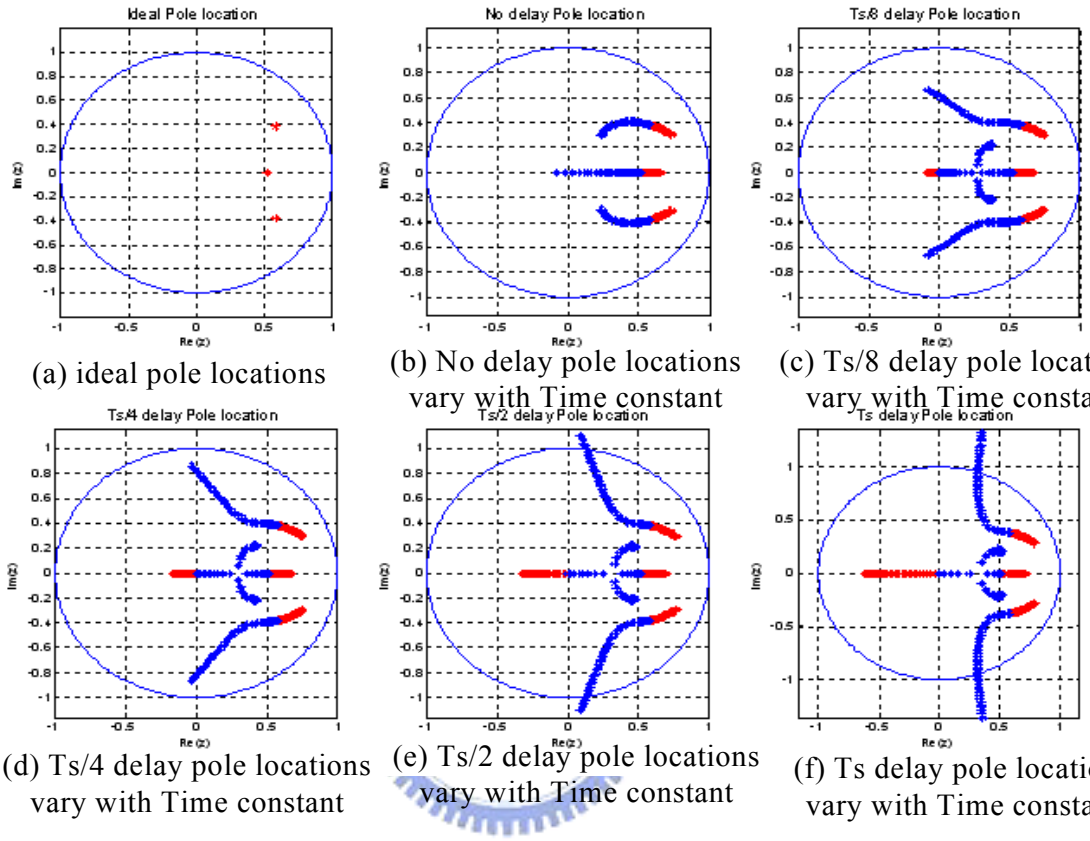
4.3 Pole Locations of Noise Transfer Function

Now, we analyzed delay difference in other method, based on root locus theorem. A nonzero delay t_d augments the order of the modulator from n to (n+1). Thus, a third order modulator with timing delay, the number of poles is increased from three to four. We take this delay as a part of influence on the stability. Next, we also assume this delay to be constant in time and known. The latter can be very well approximated by the introduction of a synchronization latch.

In the CT implementation, the integrator gain is realized by the product of a resistor (or the inverse of a transconductance) and a capacitor value. In a typical technology, the variation of this product can be up to ±30%. The modulator open-loop gain can be described as a discrete transfer function $G_c(z)$. Now, we can investigate the robust stability of the modulator by plotting pole locations with RC product variations. The third order modulator pole locations are shown in Fig. 4.3(a). There are only three poles in the non-delay architecture, as showed in Fig. 4.3(b). For timing delay topology, it will add an extra pole at $z = 0$, as showed in Fig. 4.3(c)-4.3(f). Without RC product variations ($\Delta RC = 0$), the pole locations in delay topologies are the same as the non-delay topology. An extra pole at (0,0) in Fig. 4.3(c)-4.3(f), will be cancelled by a zero at (0,0), which is well-known as pole-zero cancellation.

With a negative shift of time constant (ΔRC from 0% to -40%), it results in a positive shift of the integrator gain. It causes two poles moving toward unit circle rapidly, as shown in Fig. 4.3 blue lines expressed. It leads to instability of the modulators. In contrast, a positive shift of time constant (ΔRC from 0% to 40%), it results in a negative shift of the integrator gain yields less aggressive noise shaping, as shown in Fig. 4.3 red line expressed. In contrast to blue lines, there is no serious difference in red lines. Whether RC variations decrease or increase, we can find a

following property. The longer delay compensation, the more rapidly poles move from original pole locations to unit circle. We can also conclude that CT ΣΔ modulators with longer delay compensation topologies are more unstable systems.



(a) ideal pole locations

(b) No delay pole locations vary with Time constant

(c) Ts/8 delay pole locations vary with Time constant

(d) Ts/4 delay pole locations vary with Time constant

(e) Ts/2 delay pole locations vary with Time constant

(f) Ts delay pole locations vary with Time constant

Figure 4.3 The 3rd order pole locations of different delay compensation in RC variations (Blue lines represent RC product variations from 0% to -40%. In contrast, red lines represent RC product variations from 0% to 40%).

The distances of four poles from zero point (0,0) are shown in Fig. 4.4. The two complex poles (pole1 、pole2) move toward outside the unit circle quickly, shown in Fig. 4.4. They may be at outside the unit circle in large RC variations, which are the pole distances from (0,0) over 1. Thus, the two complex poles are dominant poles in the ΣΔ modulator. Comparing to the complex poles (pole1 、pole2), the pole3 and pole4 are less significant. Even in large RC variations, their locations are always in unit circle. We can also calculate averages of all poles distances from (0,0). The pole average distance in less delay architecture is always farther from unit circle. In this

way, we also prove that the less delay architecture is a more robust system.

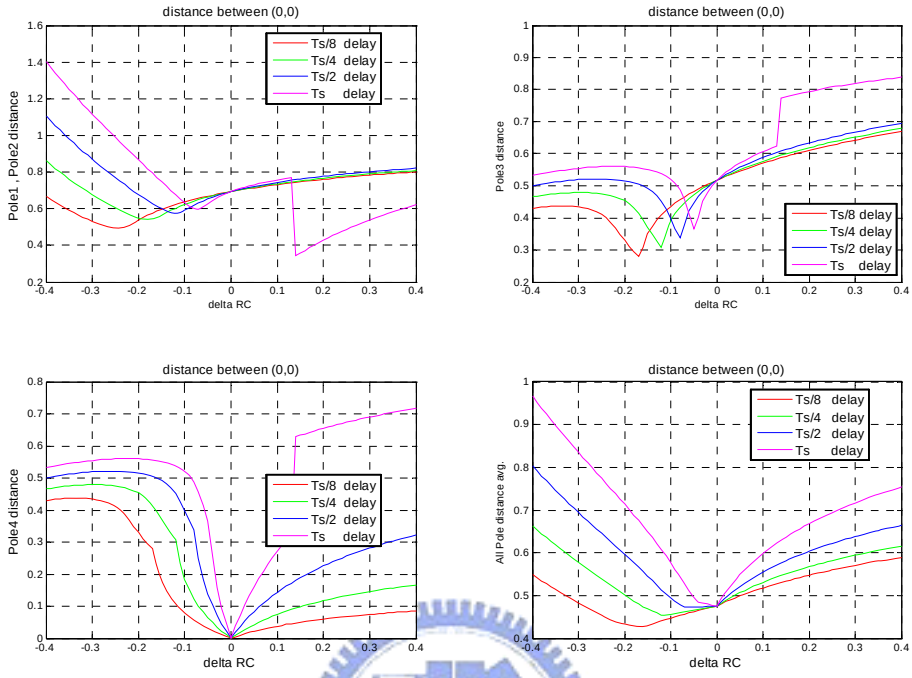


Figure 4.4 Third order ΣΔ pole distances from (0,0) with different delay compensation

4.4 Third Order Simulation Results

As described in section 4.2 and section 4.3, the same characteristic is proved in noise power gain (NPG) or pole locations. A ΣΔ modulator with less delay compensation is more robust and stable in the process variations.

For stability issue, a negative shift of time constant is more serious than a positive shift. In a negative shift of time constant, it leads to instability of the modulators and degrades the SNR performance. In the longer delay compensation architecture, the SNR is degraded quickly. In contrast, in a positive shift of time constant, it also degrades the ΣΔ modulator, but is does degrade seriously as negative shift. Their SNR performances are no seriously different with different delay compensation. The simulation results are shown in Fig. 4.5, the simulation result is

the same as theorem analysis in above sections. Considering worst performance case, the 3rd order simulation result is shown in Fig. 4.6.

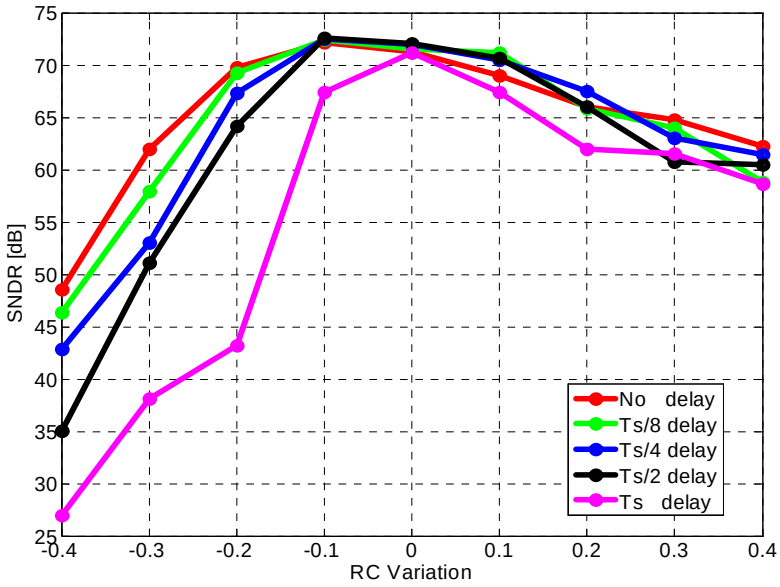


Figure 4.5 RC-variations influence on third order ΣΔ with different delay

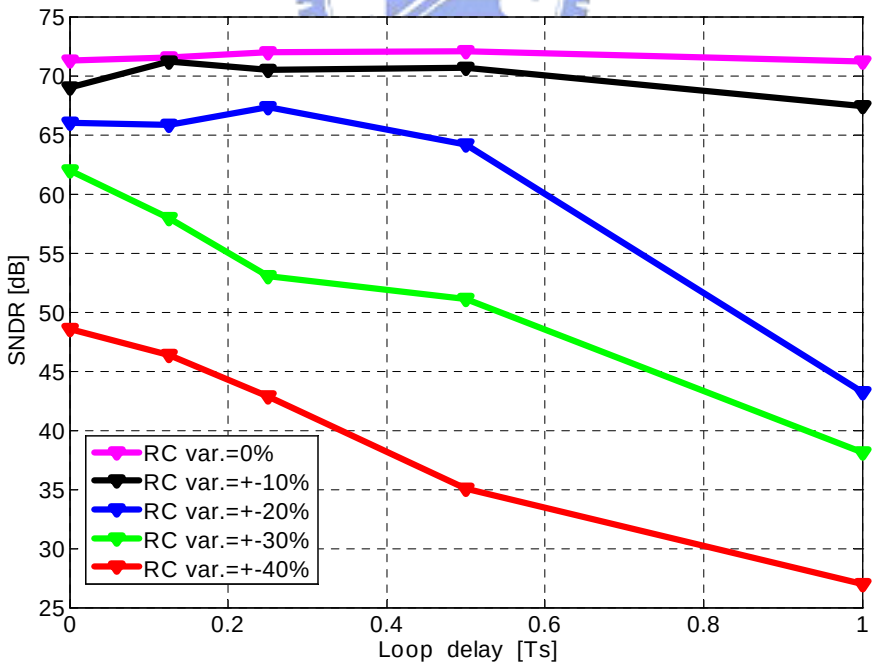


Figure 4.6 Worst case of RC-variations influence on 3rd order ΣΔ with different delay compensation in system level simulation

The histograms of SNDR deviations for ΣΔ modulators with different delay

compensation in a maximum coefficient variation of ±30% are shown in Fig. 4.7. The less delay compensation architecture has smaller deviation. Their standard deviations are 2.94, 4.44, 6.92, 10.52dB respectively.

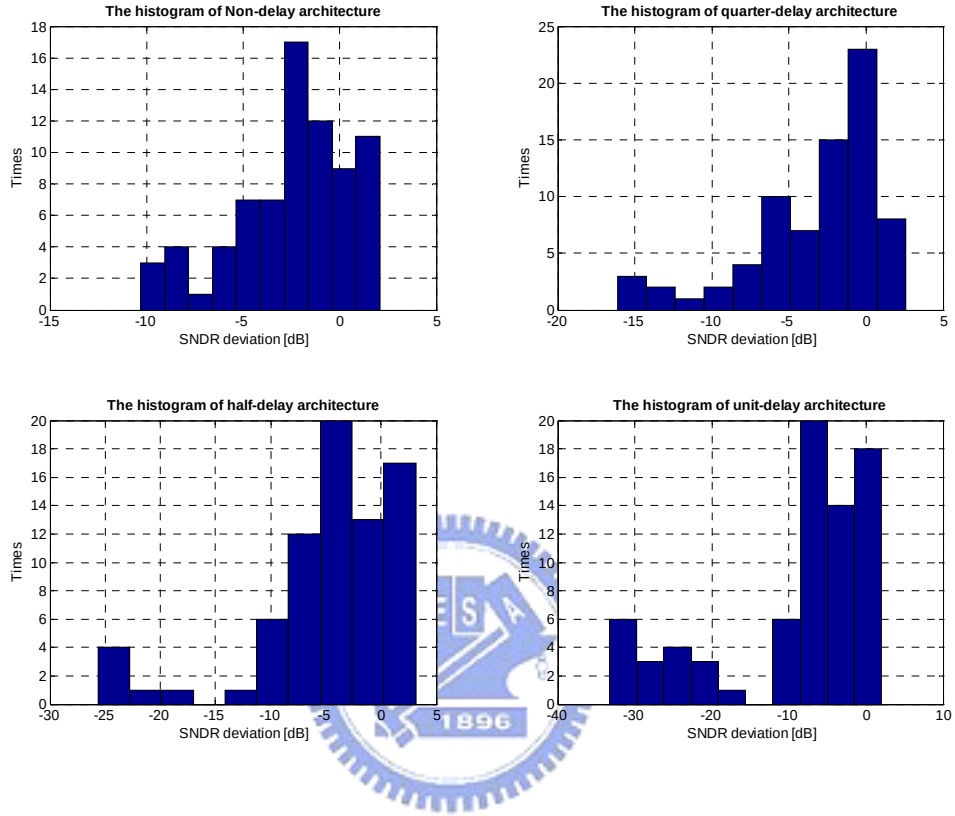


Figure 4.7 3rd order histograms of SNDR deviations with ±30% process variations

4.5 Analysis and Simulation Result of Other Higher Order ΣΔ Modulator

Now, we check other higher order CT ΣΔ modulators to get the general form. Using the same method, the fourth order is proved. The same as above section, we first get the fourth order coefficients. Using the same method in section 2.4, we get the coefficients listed in Table 4.2 and the PSD simulation result is shown in Figure 4.8.

Table 4.2 Coefficients of CRFF fourth order modulator with different delay

CT NRZ	a1	a2	a3	a4	g_{c1}^2	g_{c2}^2	kb
t_d=0	2.0328	2.371	1.6259	0.4624	0.0114	0.0731	0
t_d=0.125	2.1842	2.4744	1.6549	0.4624	0.0114	0.0731	0.132
t_d=0.25	2.3422	2.5788	1.6837	0.4624	0.0114	0.0731	0.2732
t_d=0.5	2.6778	2.7929	1.7416	0.4624	0.0114	0.0731	0.5866
t_d=1	3.4317	3.2427	1.857	0.462	0.0114	0.0731	1.3480

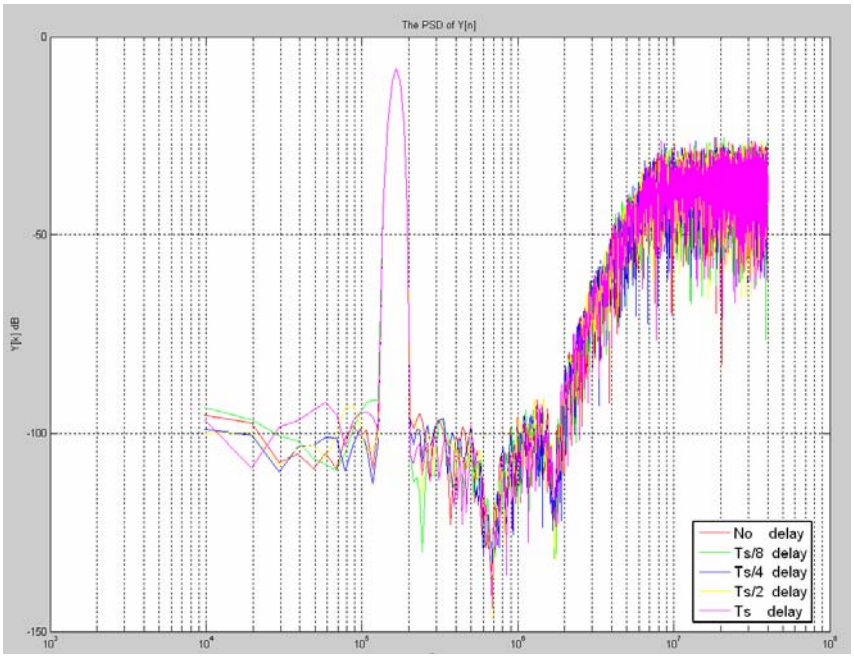


Figure 4.8 CT CRFF fourth order with different delay compensation PSD (OSR=20)

The following analysis is the same as section 4.2 and 4.3. We do not describe in detail again. The NPG values are shown in Fig. 4.9. The pole locations and distances are plotted in Fig. 4.10 and 4.11 respectively.

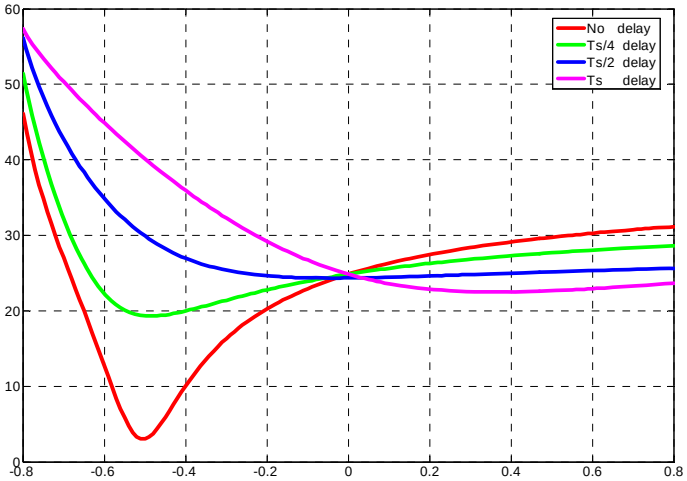


Figure 4.9 Fourth order NPG of different delay in RC variations

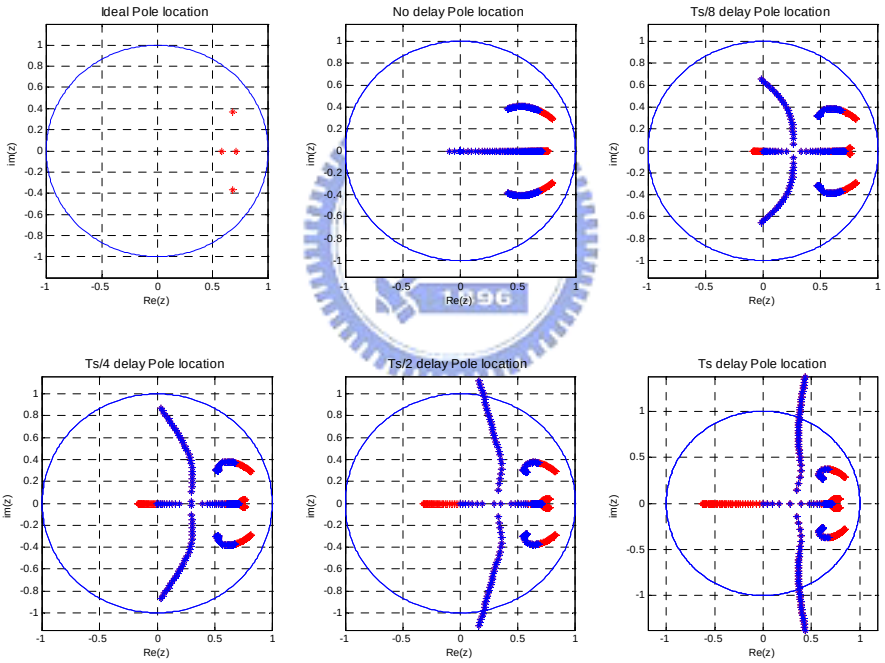


Figure 4.10 The 4th order pole locations of different delay in RC variations (Blue lines represent RC product variations from 0% to -40%. In contrast, red lines represent RC product variations from 0% to 40%).

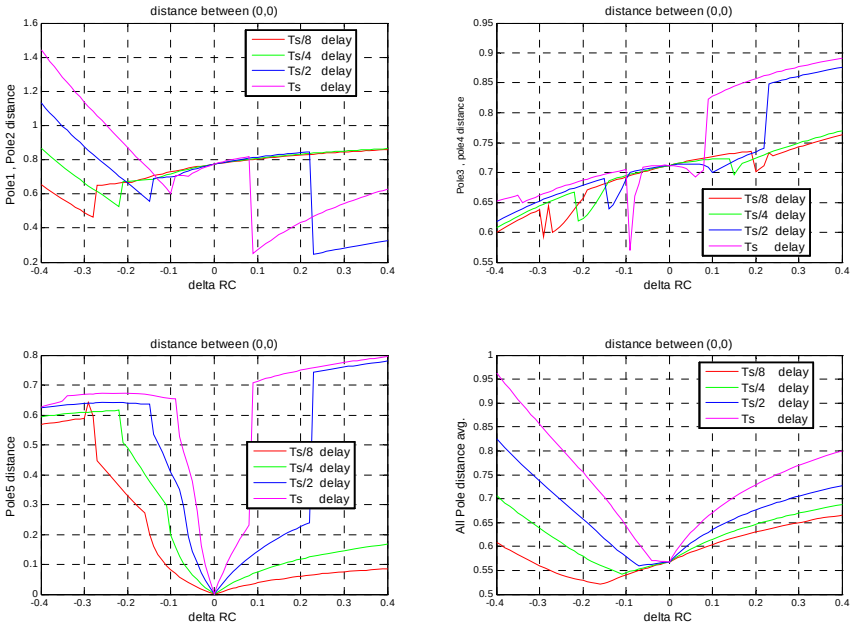


Figure 4.11 4th order ΣΔ pole distances from (0,0) with different delay compensation

Finally, the Matlab/Simulink simulation results are also shown in Figure 4.12. Considering worst performance case, we plot the 4th order simulation result in Figure 4.13. Thus fourth order design examples have been examined as well. The results hold the same property. For a fifth order ΣΔ modulator, we can also find the same property as 3rd and 4th. Thus, we do not show again in detail. From analysis of third order and fourth order, it reveals that higher order ΣΔ modulator have larger NPG and pole locations variations than lower order ones.

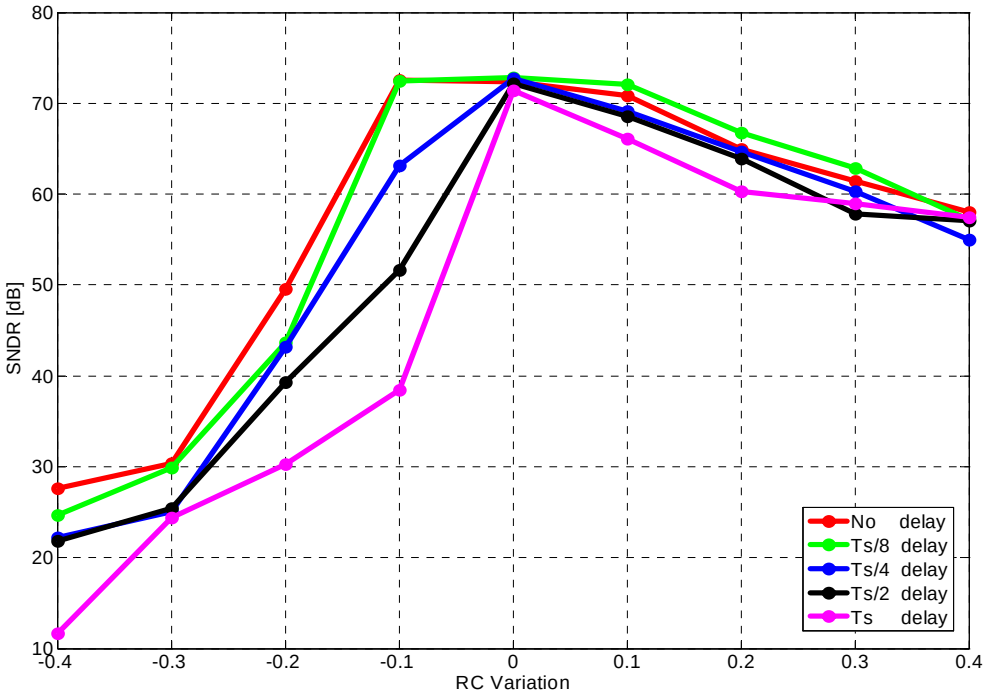


Figure 4.12 RC-variations influence on fourth order ΣΔ modulator with different delay compensation

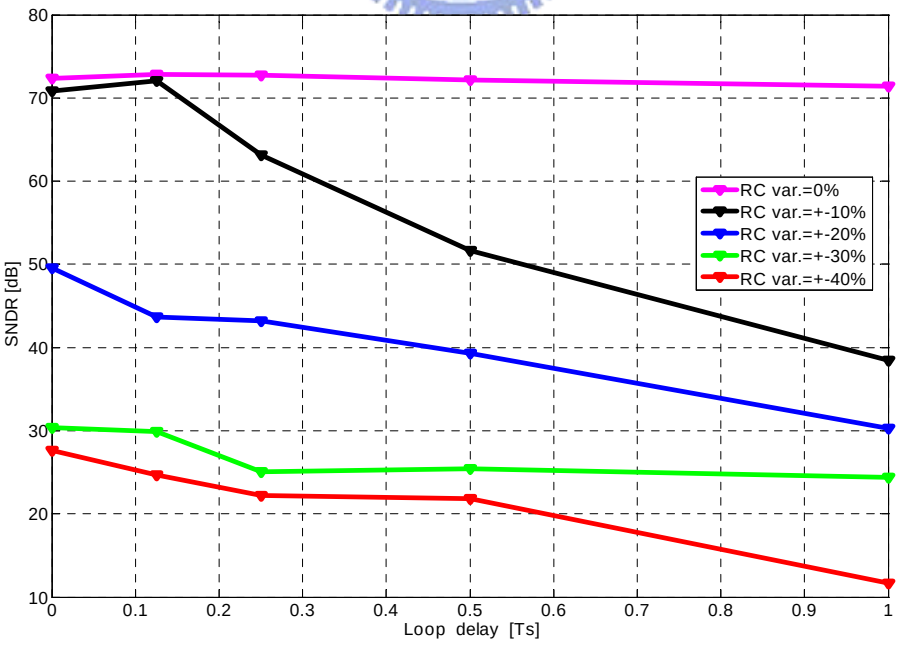


Figure 4.13 Worst performance case of RC variations influence on fourth order ΣΔ with different delay compensation in system level simulation

The 4th order and 2nd order histograms of SNDR deviations for ΣΔ modulators with different delay compensation in a maximum coefficient variation of ±30% are shown in Fig. 4.14 and Fig. 4.15.

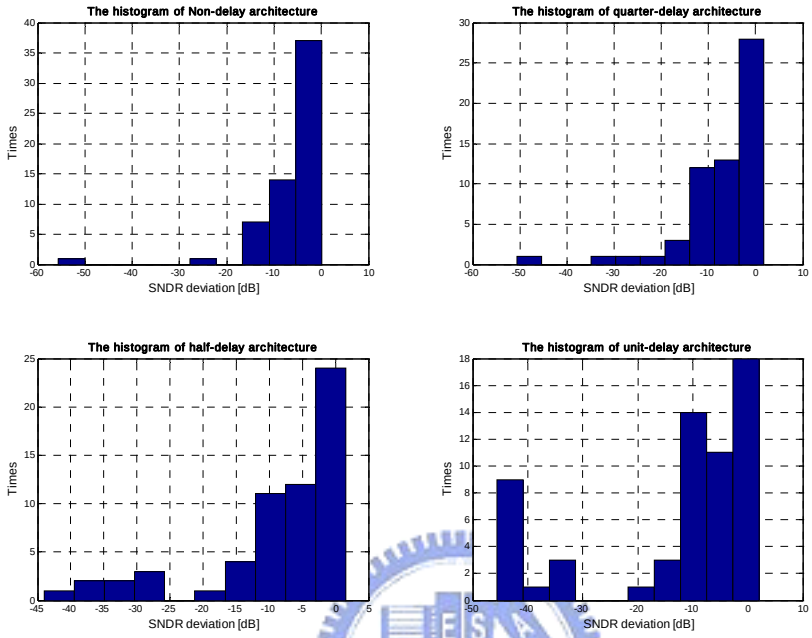


Figure 4.14 4th order histograms of SNDR deviations with ±30% process variations

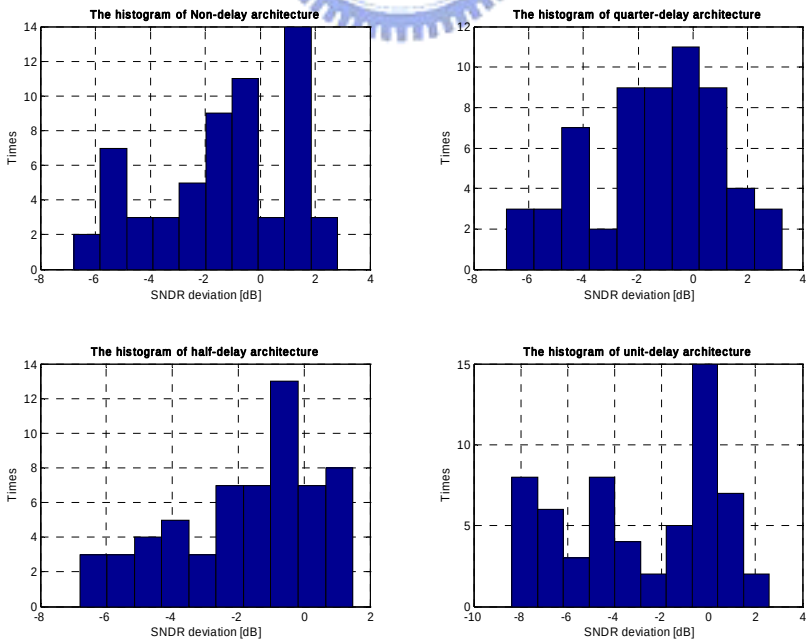


Figure 4.15 2nd order histograms of SNDR deviations with ±30% process variations

We could find that there is no large difference in a $\Sigma\Delta$ modulator with different loop delay compensation in 2nd order $\Sigma\Delta$ modulator. Process variations don't degrade performance seriously.

Now, we try to find a critical ΔRC value, which is defined as the poles lying on the unit circle. In discrete time signal processing theorem, a discrete system is unstable, if its poles are outside the unit circle. Thus, if a system tolerates larger ΔRC range, it will be a more robust and stable system. The critical ΔRC value is shown in Fig. 4.16. It also proves that a less delay compensation is more stable.

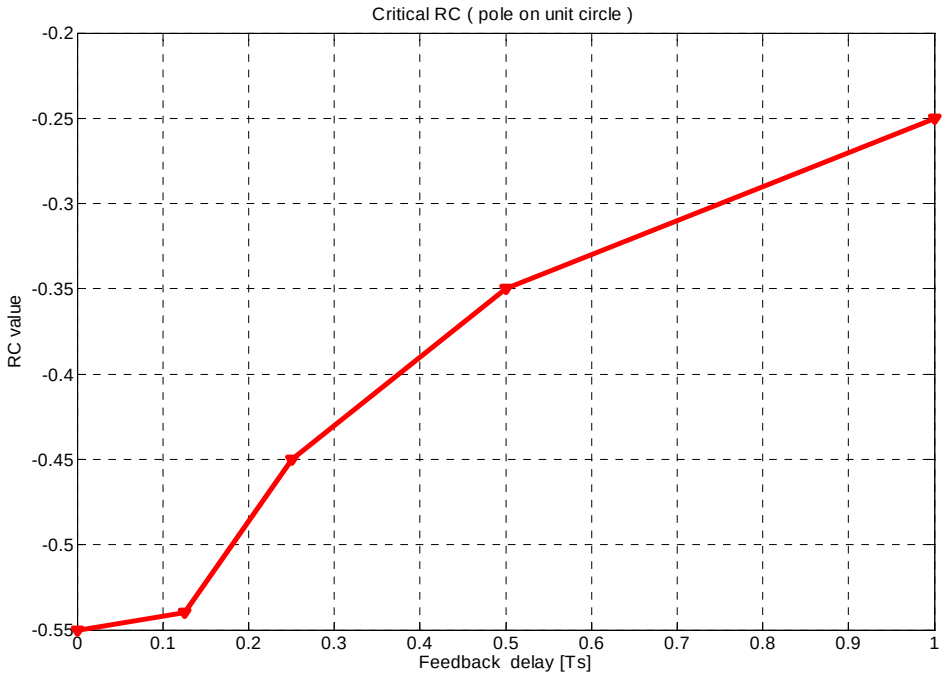


Figure 4.16 The critical ΔRC values of different delay compensation

Chapter 5

A Practical Circuit Implementation

The following chapter is devoted to the practical design a 3rd order continuous time ΣΔ modulator for W-CDMA receiver. Moreover, continuous-time filter implementations and circuit design solutions are presented.

5.1 Loop Filter Implementation

In the following, commonly used continuous time integrator implementations are discussed. A continuous-time ΣΔ modulator is composed of active or passive filters. A continuous time ΣΔ modulator with passive filters was first proposed in [47]. Its loop filter consists of only resistors and capacitors. The only active component is the quantizer. The passive networks consume no power, introduce no distortions; but they cannot provide any gain either. In [47], the quantization noise is suppressed by the gain provided by the quantizer. A combination of active and passive integrator was proposed in [48], as shown in Fig. 5.1. The passive networks can save power, and the active integrators can provide high gain to suppress the quantization noise.

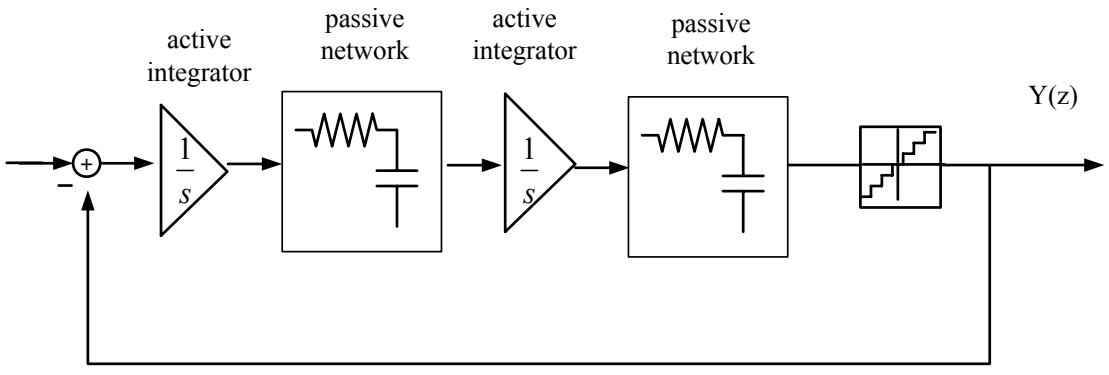


Figure 5.1 A continuous time ΣΔ modulator with active-passive loop filter

Generally, CT ΣΔ modulators are composed of gm-C [10,50,51] or active-RC active integrators [3,6,11,13,22,29,53] or a combination of both [5,15,52,54]. Gm-C integrators are based on a transconductance amplifier and a capacitor as shown in Fig. 5.2. The input voltage is fed through a transconductor gm and generates a current $i = g_m v_{in}$, which is integrated on the capacitor C. Thus, the ideal transfer-function of a gm-C integrator yields:

$$ITF(s) = a_i \frac{f_S}{s} = \frac{g_m}{sC} \tag{5.1}$$

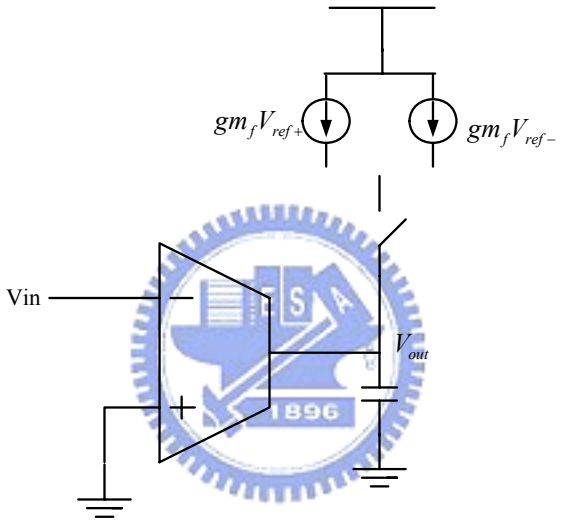


Figure 5.2 Simplifier schematic of a gm-C integrator

This kind of integrator exhibits some considerable advantages over other techniques: they are easily tunable [49], require low current consumption for high-speed application, present only a capacitive load for previous integrators and generate only small excess phase shift. On the other hand, transconductance amplifiers are required to have full signal swing to maintain the dynamic range. This requires a large linearity input range. Source degeneration is often employed to improve the linearity but at the expense of an increased input referred noise floor and reduced power efficiency [26].

5.1.1 Active-RC Filter

Another commonly used integrator structure in CT modulators is active-RC integrators, as shown in Fig. 5.3. This is due to their simplicity, linearity, and parasitic insensitivity. The ideal integrator transfer function of the active RC integrator is given

$$ITF(s) = a_i \frac{f_S}{s} = \frac{1}{sRC} \tag{5.2}$$

Assuming the amplifier is high, the input nodes closely meet virtual ground conditions and the input resistor R performs a linear V/I conversion. Linearity limitations mainly result from the amplifier. In order to show good performance, the amplifier has to provide high open loop gain, low noise contribution and large output signal swing. The input signal is converted into a current by which flows into the virtual ground node of the first integrator. The data-dependent DAC output voltage is also converted into a current by resistors and subtracted from the input current.

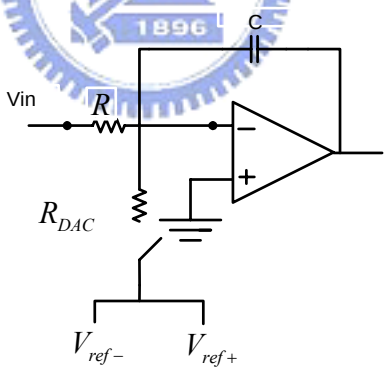


Figure 5.3 Simplifier schematic of an active-RC integrator

The choice of an active-RC integrator was made for several reasons. The virtual ground of the amplifier is ideal as a current feedback point for the current steering DAC employed in the topology. Since the amplifier will keep its output to keep its virtual ground swing small, the DAC non-linearity due to finite output resistance is minimized. The active-RC integrator is suited for low-voltage operation in that large signals are seen only at the input resistor and the output of the amplifier where careful

design can allow nearly rail-rail operation.

In order to meet all of these requirements over the entire bandwidth a large GBW, multi-stage feed-forward compensated amplifiers with class-AB output stage are commonly used. Additionally, the feed-forward path through the integrating capacitor generates a right half plane (RHP) zero, which introduces an excess phase shift. A frequently enhancement of the simple active-RC integrator is the insertion of a resistor R_z in series to the integration capacitor [29].

In conventional ΣΔ with feed-forward topology, the coefficients are implemented using transconductance amplifiers. Nowadays, these are realized with capacitors, which are defined by the capacitor C_{fi} and C_3 ratio, shown in Fig. 5.4. In contrast to a feed- forward architecture using transconductance amplifiers (gm cells) [6, 50], the implemented solution consumes no power in the feed-forward branches. Additionally, the feed-forward coefficients are inherently linear, even for large input signal swings. The main advantage of this structure is the elimination of the feed forward summing amplifier at the output of the filter. Using feed-forward capacitances, the summing node can be shifted from the output to the input of the last integrator stage [13].

The integrator gains are determined by the resistors R_i and capacitors C_i. The resistor is chosen to be 25k in order to fit the input noise requirement. The smaller integrator resistors R_i will decrease input resistor noise, but it will lead to larger integrator capacitors C_i. This will take more power consumption in opamps design. The values of the resistors R_1 and R_{DAC} of the first integrator are determined by the low power requirement, so that these are maximized in terms of the maximum tolerable in-band noise limit.

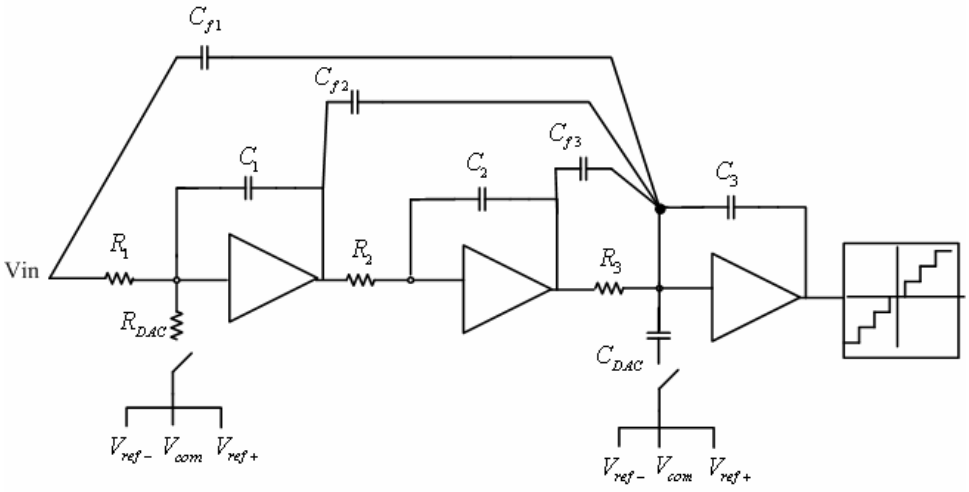


Figure 5.4 Capacitive feed-forward filter implementation in active-RC filter

Thus, a trade off between resistor noise and power consumption must be considered. In our design, sampling rate at 100MH and using the coefficients with t_d=0.25, as listed in Table 4.1, we get the values of capacitors and resistors, shown in Table 5.1. In order to meet the linearity specifications at the low supply voltage, all the analog modules are fully differential.

Table 5.1 The values of capacitors and resistors in 3rd CT ΣΔ with 0.25Ts feedback

R_1	25kΩ	C_{f1}	0.4pF
R_2	25kΩ	C_{f2}	0.93pF
R_3	40kΩ	C_{f3}	0.98pF
C_1	0.8pF	R_{DAC}	25kΩ
C_2	0.8pF	C_{DAC}	0.10pF
C_3	0.4pF		

5.1.2 Bias Circuit

This is a wide swing current mirror into the constant transconductance bias circuit as shown in Fig. 5.5. This modification greatly minimizes most of the

detrimental second order imperfections caused by the finite output impedance of the transistor, without greatly restricting signal swings. It is also including wide swing current mirror and a start up circuit.

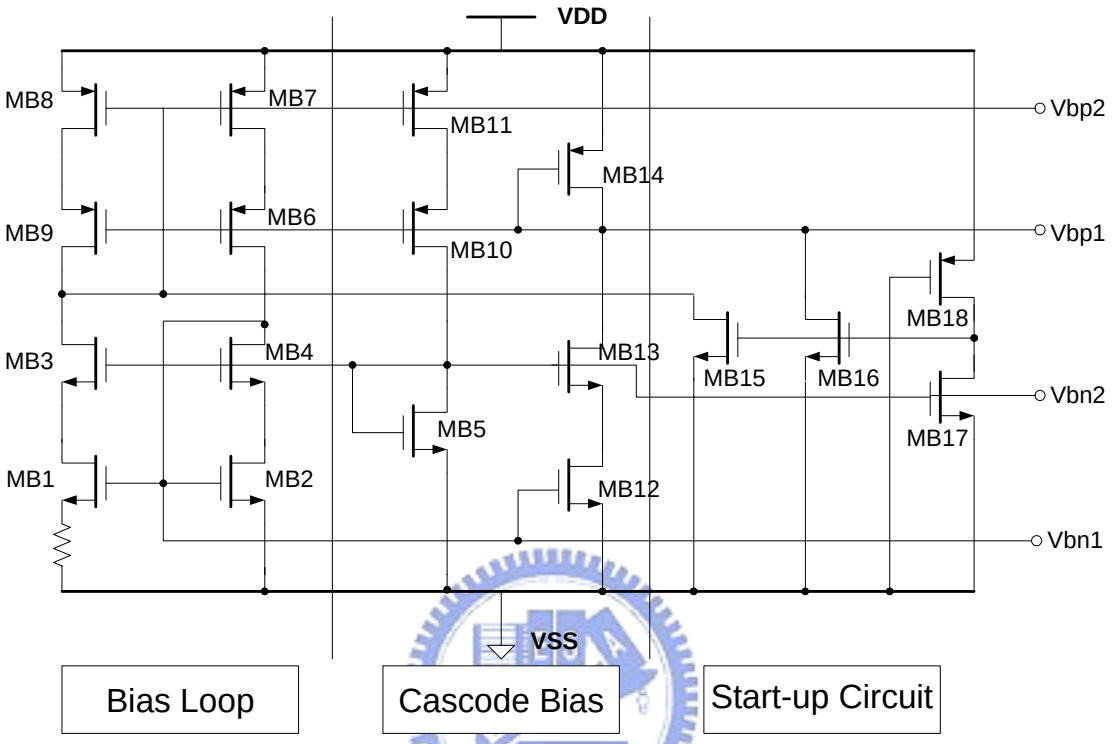


Figure 5.5 Bias circuit schematic

5.1.3 Two-Stage Operation Amplifier

For system simulations the operational amplifiers were described using a two-pole model (GBW, Adc) [31], [32]. Sampling rate at 100MHz, the opamps require a bandwidth higher than 200MHz and dc gain higher than 55dB. A single amplifier cell and its common mode feedback (CMFB), shown in Fig. 5.6, 5.7, satisfy the requirement of integrators.

The amplifier used is a conventional two-stage design employing miller compensation. This topology is suitable for driving resistors with minimal power consumption. As the linearity of the first integrator is most significant, its GBW was set higher than two times of sampling rate (200MHz). The second and third

integrator's noises and distortions are shaped by the first integrator such that there is no serious effect on the overall modulator performance. So the second and third stage opamps can be scaled down to reduce power consumption.

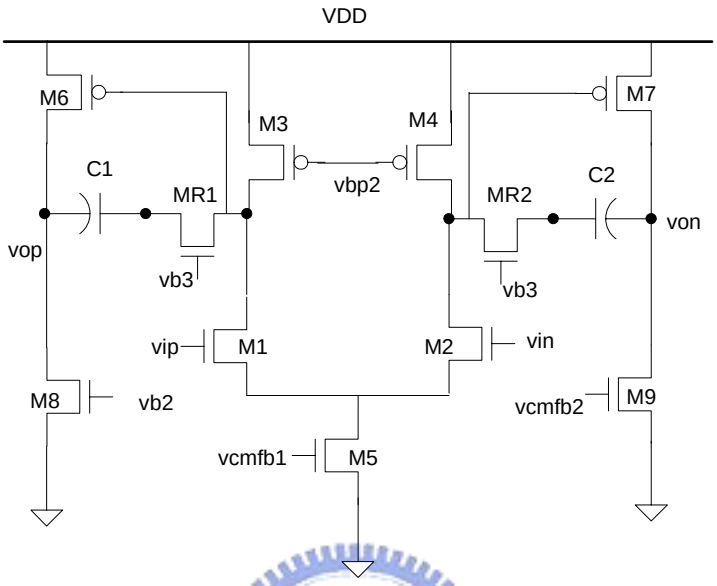


Figure 5.6 two-stage opamp schematic

Due to an unintentional feed-forward path through the miller capacitor, a right-half-plane (RHP) zero is also created and the phase margin is degraded. If a proper nullifying resistor(transistor MR1、MR2 in Fig. 5.6 as resistors) is inserted in series with the miller capacitor [55], such a zero can be removed.

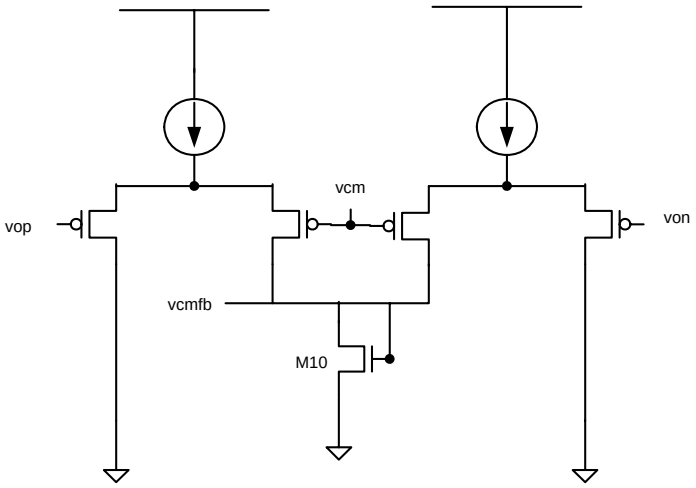


Figure 5.7 CMFB schematic

The simple CT CMFB circuit is realized only with a few additional devices. Using two differential pairs to implement the common-mode input stage, they detect the common-mode output voltage. This output voltage is compared to a common-mode reference voltage V_{cm} with the common-mode input stage. If these voltages are not equal, the common-mode output stage (M10) will drive the MOS transistors (M5 in Fig. 5.6) to balance the common-mode output voltage with the reference voltage. The first stage opamp simulation results are summarized in Table 5.2.

Table 5.2 Simulation performance of first stage opamp

DC gain		58dB
ICMR		-27dB
Unit-gain Freq.		225MHz@CL=2pf,RL=25KΩ
Output swing		0.2V~1.5V
Input Noise		28.5nV /rt hz
Slew Rate	Rising	168V/μs@ CL=2pf
	Falling	176 V/μs @ CL=2pf

5.2 Tri-Level Quantizer and DAC Realization

A high speed and high accuracy comparator is used from [56], as shown in Fig. 5.8. The dynamic operation of this circuit is divided into a reset time interval and a regeneration time interval. During ck2 is logic high**,** the comparator is in the reset mode. Current flows through the closed resetting switch M12, which forces the previous two voltages to be equalized.

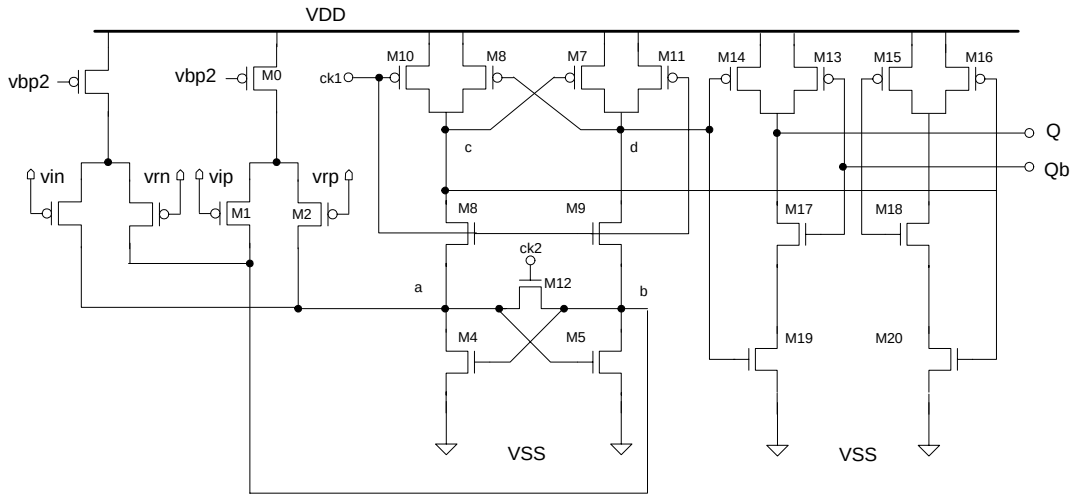


Figure 5.8 comparator schematic

The regeneration is initialized by the opening of switch M12. The first step of regeneration is within the short time slot between ck2 getting low and ck1 getting high. The n-channel flip-flop, together with the p-channel flip-flop, regenerates the voltage differences between nodes “a” and “b” and between nodes “c” and “d”. The voltage difference between node “c” and node “d” is soon amplified to a voltage swing nearly equal to the power supply voltages.

Two differential-differential type comparators are used to implement a tri-level 1.5-bit quantizer, as shown in Fig. 5.9. The input signal from $-V_{ref}$ to $+V_{ref}$ and the quantizer has the thresholds at $-\frac{V_{ref}}{2}$ and $\frac{V_{ref}}{2}$. The Vrefp and Vrefn equal to 1.35V and 0.45V respectively in this design.

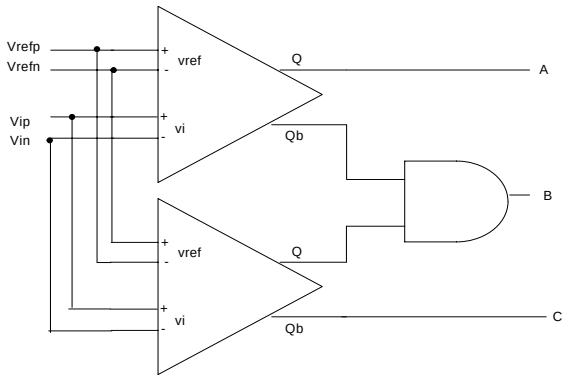


Figure 5.9 Tri-level quantizer schematic

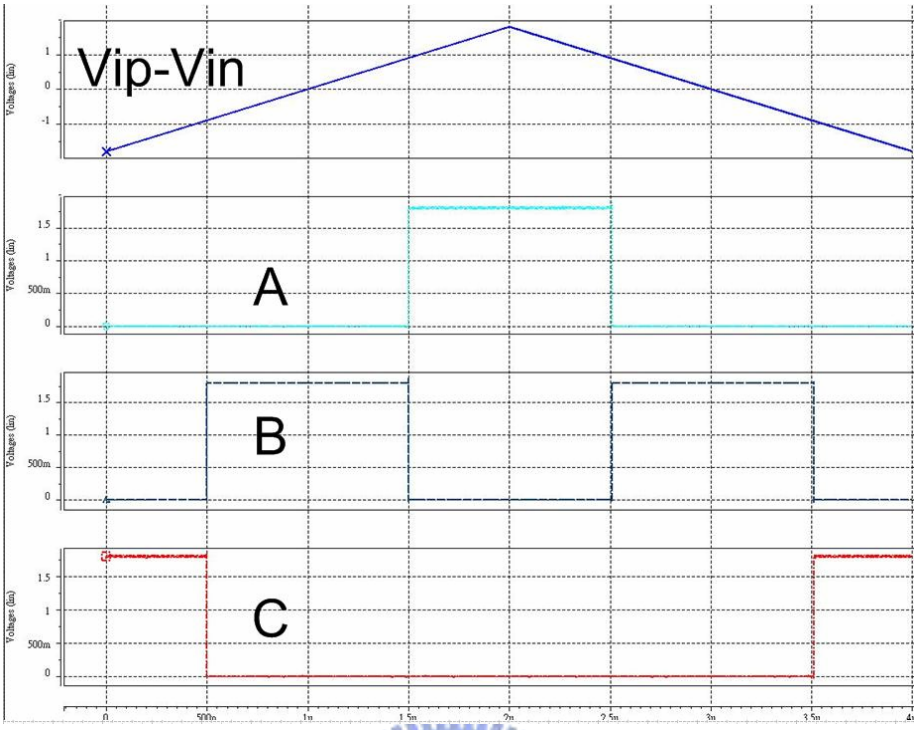


Figure 5.10 The 1.5-bit quantizer simulation result

If the differential signal is higher than $\frac{V_{ref}}{2}$ (0.45V), then the "A" signal will be logic high and others "B" and "C" will be logic low. If the differential signal is between $-\frac{V_{ref}}{2}$ (-0.45V) and $\frac{V_{ref}}{2}$ (0.45V), then the "B" signal will be logic high and others "A" and "C" will be logic low. Finally, if the differential signal is lower than $-\frac{V_{ref}}{2}$ (-0.45V), then the "C" signal will be logic high and others "A" and "B" will be logic low. The tri-level 1.5-bit quantizer simulation result is shown in Fig. 5.10.

From section 3.2.1, we know that the feedback excess loop delay is a serious non-ideality. One of the excess loop delay sources is quantizer signal dependent delay. In section 4.1, a fixed delay implemented by a synchronization latch can compensate to the original non-delay architecture.

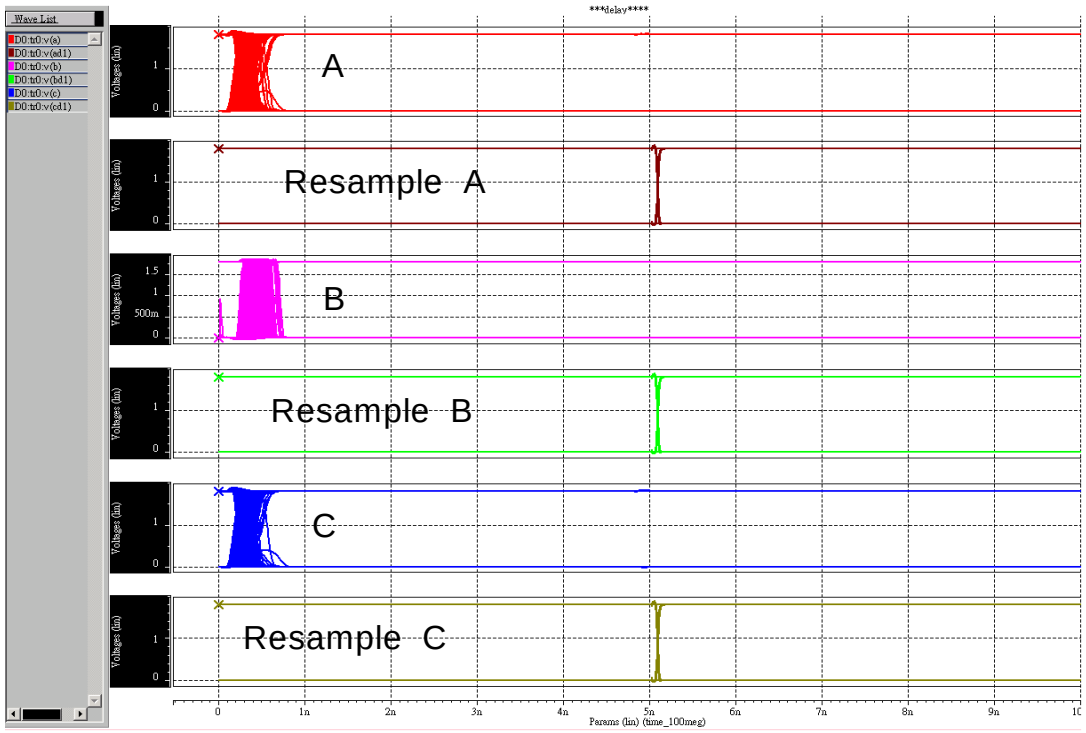


Figure 5.11 The eye diagram of the 1.5-bit quantizer

We plotted the eye diagram in Fig. 5.11 to observe the quantizer signal dependent delay. We found all output signals (A、B、C) have an uncertain rise time and fall time. This signal dependent delay is easily circumvented by inserting a latch after the quantizer. After inserting a latch, the signal dependent delay will be fixed to a latch delay time, shown in Fig. 5.11.

The implemented 1.5-bit NRZ global feedback (DAC1) consists of a feedback resistor (R_{DAC}), $\pm V_{ref}$ (1.8V,0V) V_{com}(0.9V) and a switch. Another local feedback (DAC2) consists only of a feedback capacitor (C_{DAC}), $\pm V_{ref}$ (1.8V,0V) V_{com}(0.9V) and a switch.

In order to observe the quantizer signal-dependent delay degraded the ΣΔ modulator, the PSD simulation result with different number of digital delay compensation are shown in Fig. 5.12. Because of the signal-dependent delay, the non-delay architecture has higher noise floor than other fixed delay architectures.

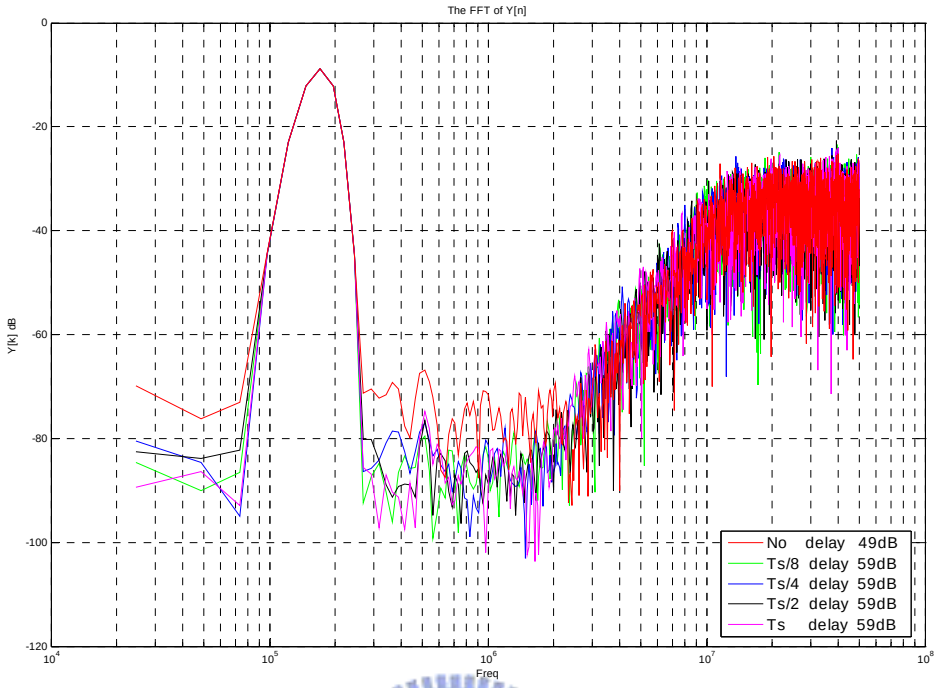


Figure 5.12 CT CRFF third order with different delay PSD in circuit level (OSR=25)

The modulator operates at sampling rate 100 MHz; the ADC consumes 6.5mW of power from a 1.8V supply. Over half of the power is consumed by the opamps, listed in Table 5.3.

Table 5.3 Power consumption table

Power consumption	power@1.8V[mW]
Bias	0.57
1st opamp	2.08
2nd and 3rd opamp	1.28x2
1.5b Quantizer	0.28
DAC and others	1.03
Total	6.5

5.3 Circuit Level Simulation Result

The worst simulation result of different delay compensation is shown in Fig. 5.13. Comparing with system level simulation, the main difference is that the non-delay architecture in circuit implementation has a signal dependent delay to degrade the SNR performance.

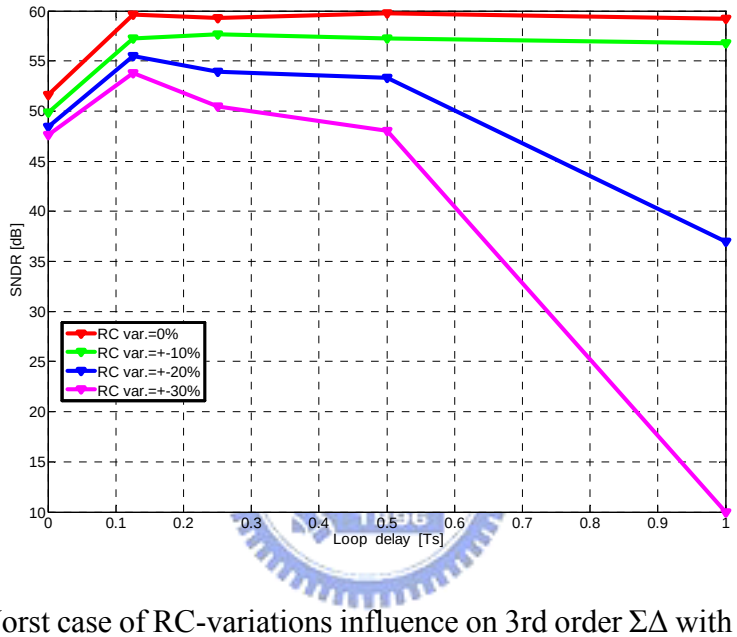


Figure 5.13 Worst case of RC-variations influence on 3rd order ΣΔ with different delay in circuit level simulation

The circuit simulation with different corner and temperature are shown in Fig. 5.14 and Fig. 5.15. The less delay architecture is found that has better system performance with lower design requirements of amplifiers. We could note that a ΣΔ modulator with less delay compensation is more robust and stable in process and temperature variations.

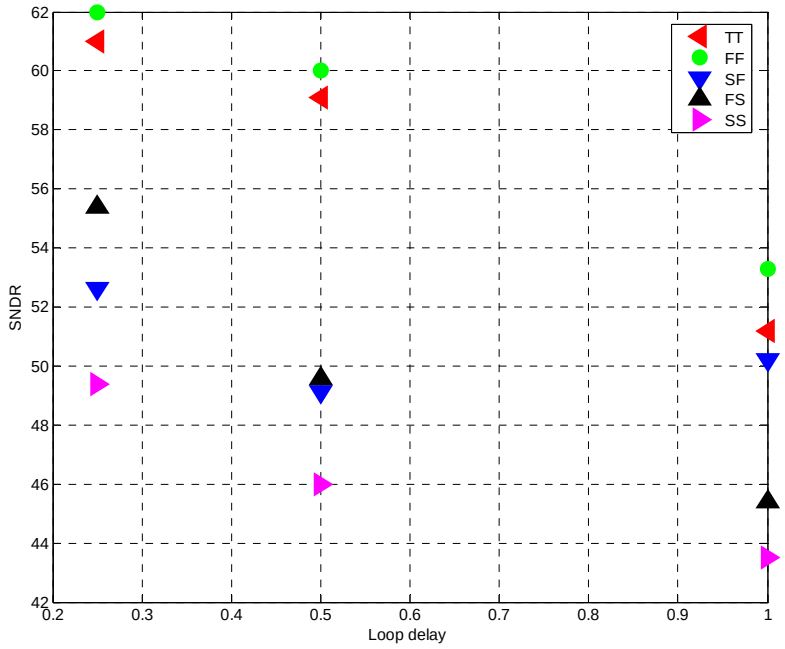


Figure 5.14 SPICE corner simulation

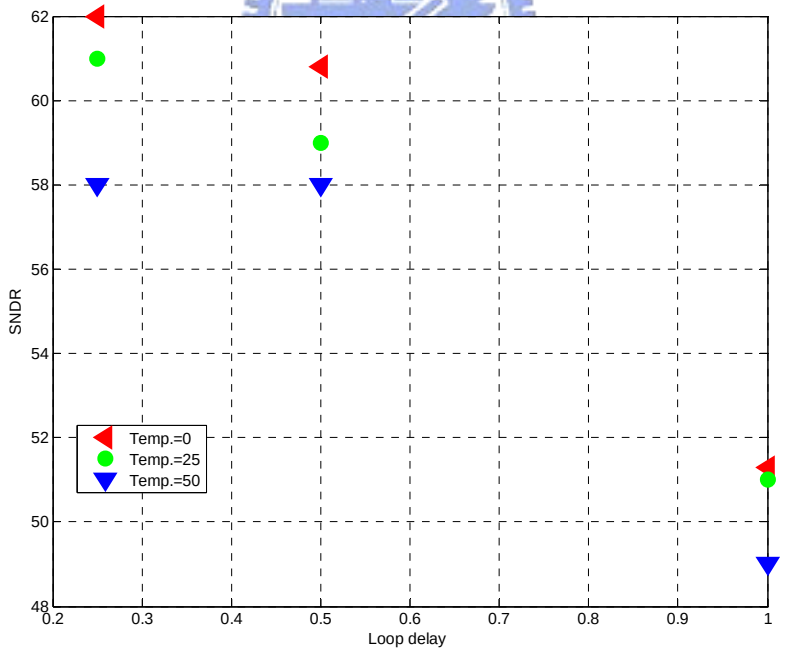


Figure 5.15 Temperature simulation

The third order ΣΔ modulator with quarter delay feedback was designed in TSMC 0.18um 1P6M MIM standard process. The core chip layout is shown in Fig.

5.16. To prevent the substrate noise from coupling each other, the analog and digital parts are separated and surrounded by the clean guard rings. The layout of the integrators and comparators is symmetry for balancing the differential signal paths. The core area of the chip is 220×200μm^2.

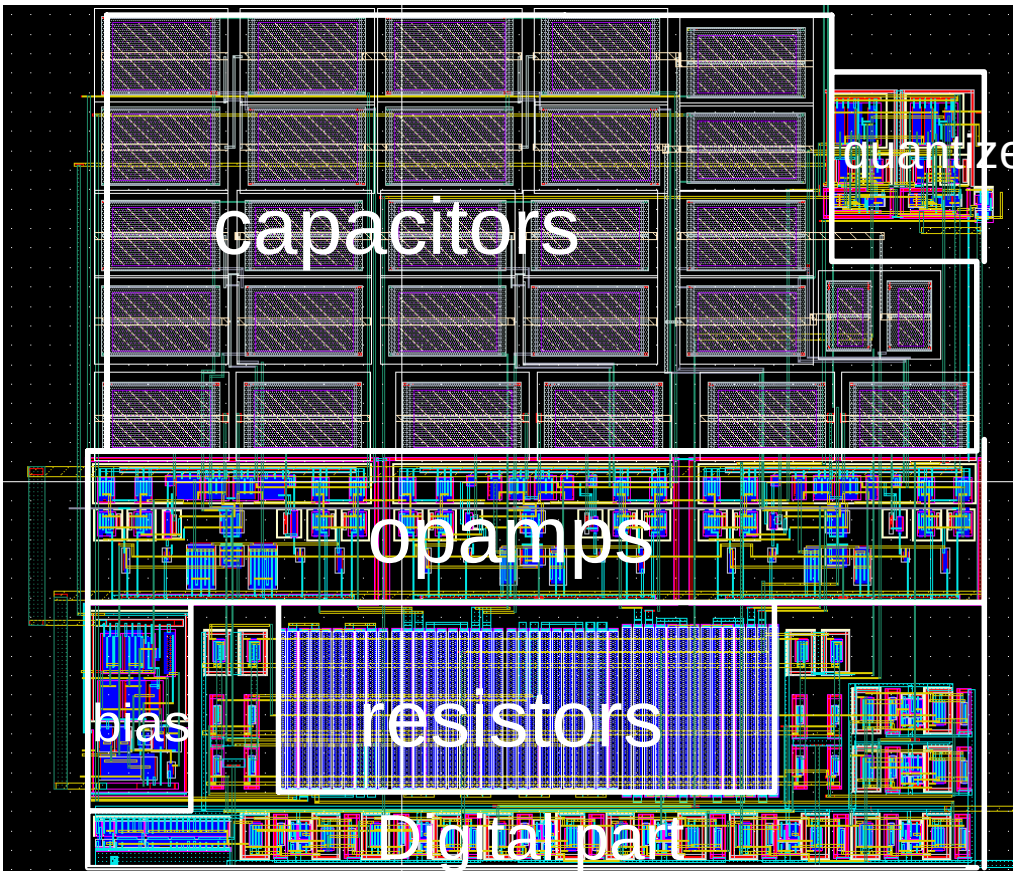


Figure 5.16 Chip layout of a third order ΣΔ modulator

Fig. 5.17 depicts the simulation output PSD for low and high signal frequencies (42-KHz and 1.2-MHz) at input level of -7dB respectively. The full-scale signal 0 dB refers to a sine wave at the input with 1.8pp. The behavior is almost the same for low and high input frequencies (both SNDR equal about 60dB). For large input amplitudes, the distortion due to the integrators increases rapidly. When the input signal exceeds the reference voltage, the ADC is overloaded and the performance is degraded. Fig. 5.18 shows SNDR versus the normalized input levels as a function of

input signal amplitude. Table 5.4 shows a summary of the performance.

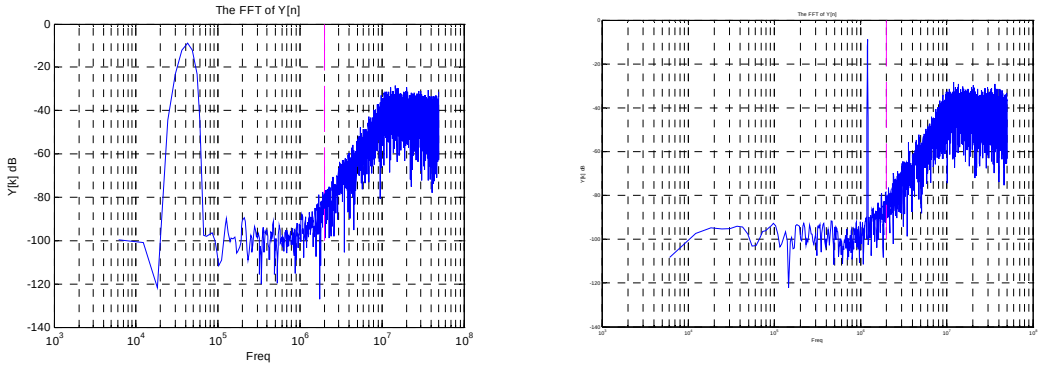


Figure 5.17 (a) PSD at fi=42.72-KHz (b) PSD at fi=1.2-MHz

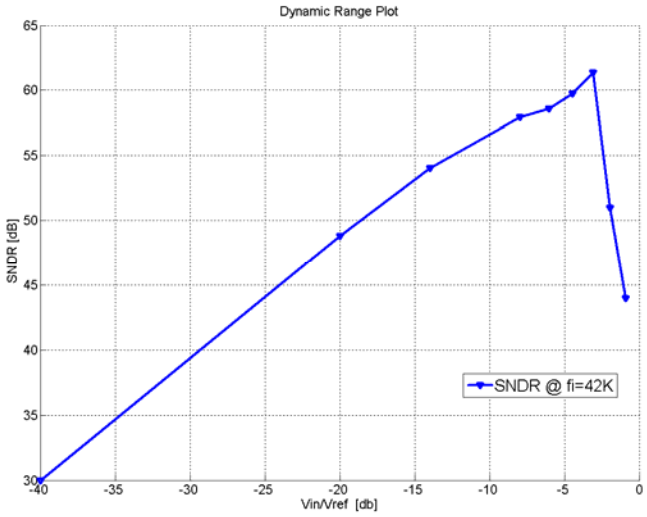


Figure 5.18 SNDRs versus input signal

Table 5.4 Performance Summary

Technology	1.8V / 0.18um
Signal Bandwidth	2MHz
OSR	25
Peak SNDR	62dB
Dynamic Range	64dB
Power consumption	6.5mW@VDD=1.8v

Chapter 6

Conclusion

With the rapid growth in portable electronic market, integrating the digital and analog circuits on a single chip at low supply voltage will be an indispensable trend in the future. The CT ΣΔ modulators are popularly used in modern communication system. Due to their low sensitivity to the analog components, they are suitable for being utilized to implement the high speed and medium resolution.

In this thesis, different loop delay compensation effect on a CT ΣΔ modulator was explained. It's worth mentioning that using higher quantizer sampling rate at feedback latches could produce different numbers of digital feedback delay. In this design, we used feedback latches with two times of quantizer sampling rate to produce quarter delay timing.

Different classes of CT ΣΔ modulators with different delay compensation were discussed in this thesis. Process variations alter the NTF, which alter NPG and lower the effective SNR. The longer loop delay compensation, the more rapidly poles move toward the unit circle from original pole locations. The characteristic is proved in NPG or pole locations, this thesis proves that a ΣΔ modulator with less delay compensation is more robust and stable in process variations.

This thesis proves the property not only on mathematic theorems, but also proves it on practical circuit implements. A third order CT ΣΔ modulator with active-RC integrators has been accomplished in 0.18μm TSMC CMOS process. The coefficients of the modulator were calculated by using the *modified-z*-transform technique.

References

[1] S. R. Rorsworthy, R. Schreier, and G. Temes, *Delta-sigma Data Converters*, Piscataway, NJ:IEEE Press, 1997.

[2] P..Benabes, M.Keramat and R. Kielbasa, "A Methodology for designing continuous-time sigma-delta modulators" *European Design and Test Conference (ED&TC 97)*, pp. 46-50, Paris, 1997.

[3] M.S. Kappes, "A 2.2-mW CMOS Bandpass Continuous-Time Multibit Δ-Σ ADC with 68 dB of Dynamic Range and 1-MHz Bandwidth for Wireless Applications," *IEEE J. Solid-State Circuits*, Vol. 38, pp. 1098-1104, July 2003.

[4] M. Moyal, M. Groepl, H.Werker, G.Mitteregger, and J. Schambacher, "A 700/900 mW/channel CMOS dual analog front-end IC for VDSL with integrated 11.5/14.5 dBm line drivers," in *IEEE ISSCC Dig. Tech.Papers*, 2003, pp. 416–504.

[5] S. Yan and E. Sánchez-Sinencio, "A continuous-time ΣΔ modulator with 88 dB dynamic range and 1.1 MHz signal bandwidth," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2003, vol. 46, pp. 62–63

[6] S. Paton, A. Di Giandomenico, L. Hernández, A. Wiesbauer,Potscher, and M. Clara, "A70-mW 300-MHz CMOS continuous-time sigma-delta ADC with 15-MHz bandwidth and 11-bits of resolution," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1062, Jul. 2004.

[7] J.A. Cherry and W.M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion*, 2000.

[8] L . Breems and J.H. Huising, *Continuous-Time Sigma-Delta Modulation for A/D Conversion in Radio Receivers*, 2001.

[9] Buhmann, A.; Keller, M.; Ortmanns, M.; Gerfers, F.; Manoli, Y.;“ Time-Continuous Delta-Sigma A/D Converters: From Theory to Practical Implementation” *Advanced Signal Processing, Circuits, and System Design Techniques forCommunications*, Page(3):169-216, May 2006

[10] J. Arias and etc, “A 32-mW 320-MHz Continuous-Time Complex Delta-Sigma ADC for Multi-Mode Wireless-LAN Receivers,” *IEEE J. Solid-State Circuits*, Vol. 41, No. 2, pp. 339-351, Feb. 2006.

[11] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, B. Romani, A. Melodia, and V. Melini, "A 14b 20mW 640MHz CMOS CT ΣΔ ADC with 20MHz Signal Bandwidth and 12b ENOB," in Proc. *IEEE Int. Solid-State Circuits Conf*, 2006, pp. 62-63.

[12] M.Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion*, Springer, Berlin, Heidelberg, New York, 2006

[13] Lukas Dörrer, Franz Kuttner, Patrizia Greco, Patrick Torta, and Thomas Hartig, “A 3-mW 74-dB SNR 2-MHz Continuous-Time Delta-Sigma ADC With a Tracking ADC Quantizer in 0.13-µm CMOS” *IEEE J. Solid-State Circuits* VOL. 40, NO. 12, DECEMBER 2005

[14] Paton, S.; Poscher, T.; Di Giandomenico, A.; Kolhaupt, K.; Hernandez, L.;Wiesbauer, A.; Clara, M.; Frutos, R.; **“**Linearity Enhancement Techniques in Low OSR, High Clock Rate Multi-bit Continuous-Time Sigma-Delta Modulators**”** *Custom Integrated Circuits Conferences*, Page(s):527 – 530,Oct. 2004

[15] Robert H. M. van Veldhoven, Brian J. Minnis, Hans A. Hegt, and Arthur H. M. van Roermund, “A 3.3-mW ΣΔ Modulator for UMTS in 0.18-µm CMOS With 70-dB Dynamic Range in 2-MHz Bandwidth” *IEEE J. Solid-State Circuits* VOL. 37, NO.12, DECEMBER 2002

[16] L. Risbo, *ΣΔ Modulators - Stability Analysis and Optimization*, Ph.D. thesis, Technical University of Denmark, 1994.

[17] Tai-Haur Kuo; Kuan-Dar Chen; Jhy-Rong Chen; "Automatic coefficients design for high-order sigma-delta modulators" *IEEE Transactions on Circuits and Systems -I*, Volume 46, Issue 1, Jan. 1999 Page(s):6 – 15

[18] J.C. Candy. .A Use of Double Integration in Sigma Delta Modulation *IEEE Transactions on Communication*, vol. com-33(No. 3):189.199, March 1985.

[19] O. Shoaei. .*Continuous-Time Delta-Sigma A/D Converters for High Speed Applications* PhD thesis, Carleton University, Ottawa, Canada, 1995.

[20] R. Schreier and B. Zhang. .Delta-Sigma Modulators Employing Continuous-Time Circuitry.. *IEEE Transactions on Circuits and Systems -I*, vol. 43(No. 4):324.332, April 1996.

[21] R. Schreier. *The Delta-Sigma toolbox for MATLAB*. Oregon State University, http://www.mathworks.com, November 1999.

[22] L. Doerrer, A. Di Giandomenico, and A. Wiesbauer, "A 10-Bit, 4mW Continuous-Time Sigma-Delta ADC for UMTS in a 0.12um CMOS process," in Proc. *European Solid-State Circuits Conf*, 2003, pp. 245-248.

[23] Aboushady, H.; Louerat, M.-M. "Loop delay compensation in bandpass continuous-time ΣΔ modulators without additional feedback coefficients" *International Symposium on Circuits and Systems*, volume 1, 23-26 Page(s):I - 1124-7 Vol.1 May 2004

[24] A. Oppenheim and R. Schafer, *Discrete-Time Signal Processing*,Prentice-Hall, 1989

[25] Beilleau, N.; Aboushady, H.; Louerat, M.M.;" Filtering adjacent channel blockers using signal-transfer-function of continuous-time ΣΔ modulators" *Midwest Symposium on Circuits and Systems* Volume 1, 25-28 July 2004

Page(s):I - 329-32 vol.1

[26] S. Yan and E. Sanchez-Sinencio, “A Continuous-Time ΣΔ with 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth,” *IEEE J. Solid-State Circuits*, Vol. 39, No. 1, Jan. 2004

[27] L.J. Breems, R. Rutten and G. Wetzker, “A Cascaded Continuous-Time ΣΔ Modulator With 67-dB Dynamic Range in 10-MHz Bandwidth,” *IEEE J. Solid-State Circuits*, Vol. 39, No. 12, pp. 2152-2160, Dec. 2004.

[28] F. Gerfers. A Design Strategy for Low-Voltage “Low-Power Continuous-Time ΣΔ A/D Converters” In *Design, Automation and Test Conference, DATE***,** pages 361-368, 2001.

[29] F. Gerfers, M. Ortmanns, and Y. Manoli, “A 1.5V, 12-Bit Power Efficient Continuous Time Third-Order ΣΔ Modulator,”*IEEE J. Solid-State Circuits*,Vol. 38, No. 8, pp. 1343-1352, Aug. 2003.

[30] N. Wongkomet and B. E. Boser, “An Analysis of Continuous Time Sigma Delta Modulators,” *Electrical Engineering Conference* No.21,1998

[31] M. Ortmanns, F. Gerfers, and Y. Manoli, “Influence of finite integrator gain bandwidth on CT sigma delta modulators,” in *Proc. IEEE Int. Symp. Circuits Systems*, vol. 1, May 2003, pp. 925–928.

[32] M. Ortmanns, F. Gerfers and Y. Manoli, “Compensation of Finite Gain-Bandwidth Induced Errors in Continuous-Time Sigma-Delta Modulators,” *IEEE Transaction on Circuits and System-I*, Vol. 51, No.6, pp. 1088-1099, June 2004.

[33] L. J. Breems, E. J. van der Zwan, and J. H. Huijsing, “Design for Optimum Performance to Power Ration of a Continuous Time ΣΔ Modulator,” in *Proc. European Solid-State Circuits Conf.*, 1999, pp 318-321.

[34] J.A. Cherry and W.M. Snelgrove, “ Excess Loop Delay in Continuous-Time

Delta-Sigma Modulators," *IEEE Transactions on Circuit and System I*, Vol. 46, No.4, pp. 376-389, April 1999.

[35] O. Oliaei, " Jitter Effects in Continuous Time ΣΔ Modulators with delayed Return-To-Zero Feedback," in *Proc. IEEE Int. Conf. On Electronics, Circuits and Syst.*, 1998, p. 351354.

[36] M. Ortmanns, F. Gerfers, and Y. Manoli, "A Continuous-Time Sigma –Delta Modulator with reduced Jitter Sensitivity," in *Proc. European Solid-State Circuits Conf.* 2002, pp. 287-290

[37] Susan Luschas, and Hae-Seung Lee," High-Speed ΣΔ Modulators With Reduced Timing Jitter Sensitivity," *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II*: ANALOG AND DIGITAL SIGNAL PROCESSING, VOL. 49, NO. 11, NOVEMBER 2002

[38] F. Gerfers, M. Ortmanns, Philipp Schmitz "A Transistor-based Clock Jitter Insensitive DAC Architecture, *IEEE ISCAS*, pp. 21-24, May 2006.

[39] B. M. Putter, " ΣΔ ADC with finite impulse response feedback DAC," *IEEE Int. Solid-State Circuits Conf*. pp.76-77, Feb. 2004.

[40] O. Oliaei, "Continuous-time sigma-delta modulator incorporating semi-digital FIR filters, "*IEEE Int. Symp. On Circuits and Systems*, pp. 957-960, May2003.

[41] L. Hernandez, A. Wiesbauer, S. Paton and A. Di Giandomenico," Modelling and Optimization of Low Pass Continuous-Time Sigma-Delta Modulators for Clock Jitter noise Reduction," *IEEE ISCAS*, Vol. 1, pp. I- 1072-5, May 2004.

[42] F. Medeiro, B. Perez-Verdu, and A. Rodriguez-Vazquez, *Top-Down Design of High Performance Sigma-Delta Modulators*, Kluwer Academic Pub, 1999.

[43] J. A. Cherry, W. M. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta–sigma modulators," *IEEE Trans. on Circuit and System II*, vol. 46, pp. 661-676, June 1999.

[44] E.J. van der Zwan. “A 2.3mW CMOS ΣΔ Modulator for Audio Applications” *ISSCC Digest of Technical Papers*, pages 220-221, February 1997.

[45] H. Aboushady, J.R. Westra, and E.C. Dijkmans. “*A 120 dB Dynamic Range ΣΔ DAC for Super Audio Compact Disc”* Philips Research Report, December 1999

[46] R. Adams, K.Q. Nguyen, and K. Sweetland. “A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling”.*IEEE Journal of Solid-State Circuits*,vol. 33(No. 12):1871.1878, December 1998

[47] F. Chen and B. Leung, "A 0.25 mW low-pass passive sigma-delta modulator with build-in mixer for a 10-MHz IF input," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 6, Jun. 1997.

[48] Song, T. Yan, S. Dept. of Electr. & Comput. Eng., Texas Univ., Austin, TX, USA;“ A low power 1.1 MHz CMOS continuous-time delta-sigma modulator with active-passive loop filters” *IEEE ISCAS*, pp.21-24, May 2006.

[49] Shoaei, O. Snelgrove, W.M. Bell Labs, Lucent Technol., Allentown, PA; “Design and implementation of a tunable 40 MHz-70 MHz Gm-C bandpass ΣΔ modulator” *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II*: ANALOG AND DIGITAL SIGNAL PROCESSING, VOL. 44, NO. 7, JULY 1997.

[50] EJ, and DTJKMANS, EC: “A 0.2 mW CMOS modulator for speech coding with 80dB dynamic range” *IEEE Journal of Solid-State Circuits*,vol. 32, no. 6, Jun. 1997.

[51] Sansen, W.M.C.; Schoofs, R.; Steyaert, M.S.J.;” A Design-Optimized Continuous Time Delta–Sigma ADC for WLAN Applications**”** *IEEE Transactions on Circuits and Systems -I*, Volume 54, Jan. 2006 Page(s):209 – 217

[52] Robert H. M. van Veldhoven “A Triple-Mode Continuous-Time ΣΔ Modulator WithSwitched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS

Receiver"*IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 38, NO. 12, DECEMBER 2003

[53] Friedel Gerfers, Maurits Ortmanns, Yiannos Manoli ,"A 1 V, 12-Bit Wideband Continuous-Time Modulator ΣΔ for UMTS Applications" in Proc. *IEEE ISCAS*,2003,pp. 921-924

[54] Toshiaki Nagai, Hiroyuki Satou, Hiroshi Yamazaki, Yuu Watanabe Fujitsu, Kawasaki, Japan,"A 1.2V 3.5mW ΣΔ Modulator with a Passive Current Summing Network and a Variable Gain Function" in *Proc. IEEE ISSCC* ,2005,pp. 494-495.

[55] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. New York: Oxford Univ. Press, 2002.

[56] G. M. Yin, F.Op't Eynde, and W.Sansen "A High-Speed CMOS Comparator with 8-b Resolut