High-Frequency Characteristic Fluctuations of Nano-MOSFET Circuit Induced by Random Dopants

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***Abstract*—As the dimension of semiconductor device shrunk into nanometer scale (nanoscale), characteristic fluctuation is more pronounced, and become crucial for circuit design. In this paper, discrete-dopant-induced characteristic fluctuation of 16-nm-gate metal–oxide–semiconductor field effect transistors (MOSFET) circuit under high-frequency regime is quantitatively studied. The circuit gain, the 3 dB bandwidth and the unity-gain bandwidth of the tested nanoscale transistor circuit are calculated concurrently capturing the discrete-dopant-number- and discrete-dopant-position-induced fluctuations in the large-scale statistically sound "atomistic" device/circuit coupled simulation. For the 16-nm-gate MOSFET circuit, the number of discrete dopants, varying from zero to 14, may result in 5.7% variation of the circuit gain, 14.1% variation of the 3 dB bandwidth, and 10.4% variation of the unity-gain bandwidth. To suppress the high-frequency characteristic fluctuations, an improved doping distribution along the longitudinal diffusion direction from the MOSFET's surface to substrate is further performed to examine the associated fluctuation. The improved vertical doping profile with less dopants locating near surface of channel effectively reduces the fluctuations of the circuit gain, the 3 dB bandwidth and the unity-gain bandwidth dramatically. Compared with the original doping profile, the reduction is 32.3%, 19.4% and 51.8%, respectively. This study provides an insight into random-dopant-induced intrinsic high-frequency characteristic fluctuations and verifies the potential fluctuation suppression technique on high-frequency characteristic fluctuations of nanoscale transistor circuit.**

***Index Terms*—Characteristic fluctuation, fluctuation suppression technique, high frequency, modeling and simulation, nanometer scale metal–oxide–semiconductor field effect transistors (MOSFET) device and circuit, random dopant effect.**

I. Introduction

SILICON-BASED devices are scaled down continually in order to increase density and speed. The gate lengths of scaled metal–oxide–semiconductor field effect transistors (MOSFETs) have been the sub-30 nm for 45 nm node high-performance circuit design [1]. Moreover, the devices with sub-10-nm-gate lengths have been currently investigated [2]–[5]. For the RF/mixed-signal applications, a cutoff frequency higher than 200 GHz have been also reported [6], [7]. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, variations in the process parameters, etc., are known as indispensable components of the circuit design methodology [8]–[12]. However, attention is seldom drawn to the existence of high-frequency characteristic fluctuations of active device due to random dopant placement. With device scaling, various randomness effects resulting from the random nature of manufacturing process, such as ion implantation, diffusion, and thermal annealing [13], have induced significant fluctuations of electrical characteristics in nanometer scale (nanoscale) MOSFETs. The number of dopants is of the order of tens in the depletion region of a nanoscale MOSFET, whose influence on device characteristic is large enough to be distinct [14].

Various random dopant effects have been recently studied in both experimental and theoretical approaches [14]–[35]. Fluctuations of characteristics are caused not only by a variation in an average doping density, which is associated with a fluctuation in the number of impurities, but also with a particular random distribution of impurities in the channel region. Diverse approaches have recently been reported to study fluctuation-related issues in semiconductor devices [19]–[31] and circuit [32]–[35]. Unfortunately, the effect of the discrete dopants induced high-frequency characteristic fluctuations on nanoscale MOSFET circuit has not been well investigated yet. In this work, a statistically sound "atomistic" device/circuit mixed-mode simulation approach is thus employed to analyze the discrete-dopant-induced high-frequency characteristic fluctuations in nanoscale MOSFET circuit, concurrently capturing "dopant concentration variation" and "dopant position fluctuation". The statistically generated large-scale doping profiles are similar to the physical process of ion implantation and thermal annealing [36]. Based on the statistically (totally randomly) generated large-scale doping profiles, device simulation is performed by solving a set of 3-D drift-diffusion equations with quantum corrections by the density gradient method [37]–[40], which is conducted using a parallel computing system [41]–[43]. In estimation of the high-frequency characteristic fluctuation, for obtaining more physical insight device and pursuing higher accuracy [44], a device/circuit coupled simulation [45]–[47] with discrete dopant distribution is conducted to examine the associated high frequency characteristic fluctuations of circuit, which concurrently considers the discrete-dopant-number- and discrete-dopant-position-induced fluctuations. We notice that the accuracy of developed analyzing technique has been quantitatively verified in the experimentally measured characteristics of sub-20 nm devices [21]–[25].

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Channel engineering technique has been known to be an effective way to suppress the random-dopant-induced characteristic fluctuation [18], [24], [27]. However, these studies are focus on the effectiveness of the suppression of dc characteristic fluctuations. Suppression techniques for high-frequency characteristic fluctuation are still lack for nanoscale MOSFET circuit. Therefore, to examine the fluctuation suppression on the high-frequency characteristic fluctuations of the explored nanoscale MOSFET circuit, an improved vertical doping profile along the longitudinal diffusion direction from the device's surface to substrate is implemented. We thus calculate the fluctuations of the circuit gain, the 3 dB bandwidth, and the unity-gain bandwidth [48] of the tested circuit, and compare with the results before the improvement. Our comprehensive results show that the number of discrete dopants, varying from zero to 14, in the 16 nm MOSFET circuit, may result in 5.7% variation of the circuit gain, 14.1% variation of the 3 dB bandwidth, and 10.4% variation of the unity-gain bandwidth. For the aforementioned doping profile with less dopants locating near surface of channel, the fluctuations of the threshold voltage, the circuit gain, the 3 dB bandwidth, and the unity-gain bandwidth are simultaneously reduced 14.2%, 32.3%, 19.4%, and 51.8%. Intrinsic high-frequency characteristic fluctuations of the nanoscale transistor circuit induced by random dopants and the effectiveness of fluctuation suppression technique are thus intensively explored.

This paper is organized as follows. In Section II, we introduce the analyzing technique for studying the random dopants effect in nanoscale device and circuit. In Section III, we examine the discrete-dopant-induced characteristic fluctuations of the 16 nm device and circuit. Both dc and high-frequency characteristics are discussed, where the suppression technique for high-frequency characteristic fluctuations is also performed. Finally, we draw conclusions and suggestion future work.

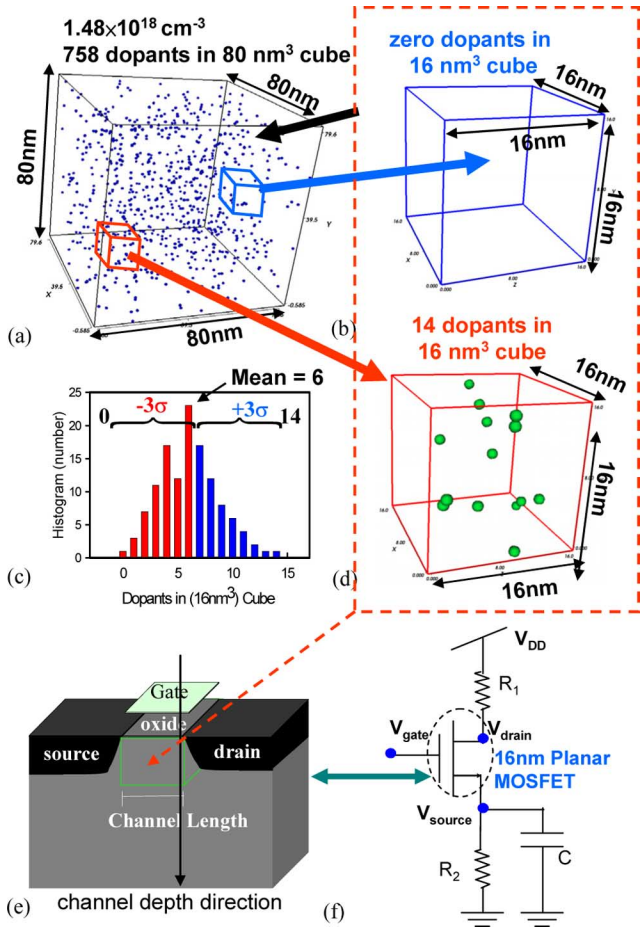

Fig. 1. (a) Discrete dopants randomly distributed in the 80 nm^3 cube with the average concentration of 1.48 × 1018 cm^{-3}. There will be 758 dopants within the cube, but dopants may vary from zero to 14 (the average number is six) within its 125 sub cubes of 16 nm^3 [(b), (c), and (d)]. The 125 sub cubes are equivalently mapped into channel region for dopant position/number- sensitive device simulation and device/circuit coupled simulation as shown in (e) and (f).

II. Nano-MOSFET Circuit and Simulation Technique

The nominal channel doping concentration of these devices is 1.48 × 10^{18} cm^{-3}. They have a 16 nm gate, a gate oxide thickness of 1.2 nm, and a workfunction of 4.4 eV. Outside the channel, the doping concentrations in the source/drain and background are 1.1 × 10^{20} cm^{-3} and 1 × 10^{15} cm^{-3}, respectively.

For the channel region, to consider the effect of random fluctuation of the number and location of discrete channel dopants, 758 dopants are firstly randomly generated in an 80 nm^3 cube, in which the equivalent doping concentration is 1.48 × 10^{18} cm^{-3}, as shown in Fig. 1(a). The 80 nm^3 cube is then partitioned into 125 sub cubes of 16 nm^3. The number of dopants may vary from zero to 14, and the average number is six, as shown in Fig. 1(b), (c), and (d), respectively. These 125 sub cubes are then equivalently mapped into the channel region of the device for the 3-D device simulation with discrete dopants, as shown in Fig. 1(e). The common-source circuit with sinusoid input wave (offset is equal to 0.5 V), shown in Fig. 1(f), is used as a tested circuit to explore the fluctuation of high-frequency characteristics. All statistically generated discrete dopants, shown in Fig. 1, are incorporated into the large-scale 3-D device/circuit mixed-mode simulation which is conducted in our parallel computing system [19], [40]. The device simulation is performed by solving a set of 3-D density-gradient equation coupling with Poisson equation as well as electron-hole current continuity equations [37]–[40]. There is no well-established device compact model for such ultrasmall nanoscale devices and to include the nonquasi static behavior of charge particle, so a 3-D quantum mechanical simulation of the device coupling with circuit equation is employed [19], [45]. The circuit nodal equations of the tested circuit are formulated and directly coupled with aforementioned device equations for device/circuit mixed-mode simulation. The time-domain simulation results are simultaneously used for the calculation of the property of the frequency response, where the frequency is sweep from 1 × 10^8 Hz to 1 × 10^{13} Hz. We notice that the device mobility and characteristic fluctuation has been validated with the experimentally measured dc baseband data [21]–[25].

To examine the effectiveness of the channel engineering technique in both nanoscale device and circuit, along the longitudinal diffusion direction from surface to substrate, an improved vertical doping profile with less dopants locating near surface

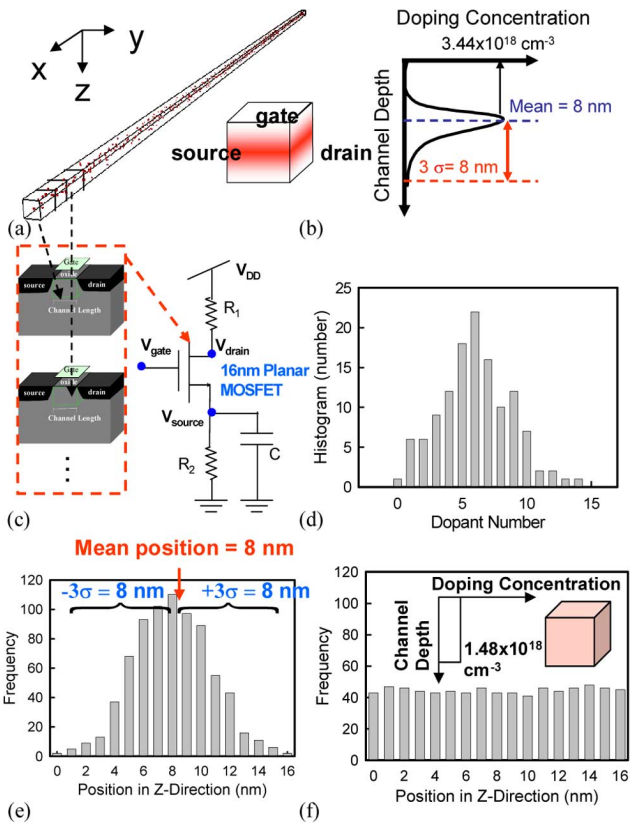

Fig. 2. There will be 758 dopants within a large rectangular solid, in which the equivalent doping concentration is 1.48×1018 cm^{-3}. The dopant distribution in the direction of channel depth, the arrow line in Fig. 1(e), follows the normal distribution (b). Partitioned cubes are equivalently mapped into channel region for dopant position/number-sensitive device simulation and device/circuit coupled simulation, as shown in (c). Similarly, dopants within the 16 nm^3 cubes may vary from zero to 14 (the average number is six) (d). The vertical dopant distribution of the improved and the original doping profile, which is generated from Fig. 1, are shown in (e) and (f).

of channel [18], [24], [27]–[29] is further implemented. 758 dopants are firstly randomly generated in a large rectangular solid (x, y, z: $16 \times 2000 \times 16$ nm), in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}, as shown in Fig. 2(a). The distribution of the generated dopants' position in the z-direction follows the normal distribution, as shown in Fig. 2(b). Both the mean position and the three sigma of this distribution are eight nanometers, which can be controlled by the manufacturing processes of ion implementation and thermal annealing [36]. The inset of Fig. 2(b) shows the nominal case of the improved vertical doping profile, where the darker region indicates the higher doping concentration. The large rectangular solid is then partitioned into 125 sub cubes of 16 nm^3 cube and mapped into device channel for discrete dopant and device/circuit coupled mixed-mode simulation, as shown in Fig. 2(c). The number of dopants may vary from zero to 14, and the average number is six, as shown in Fig. 2(d). The longitudinal dopant distribution of the improved and the original doping profile, which is generated from Fig. 1, are studied in Fig. 2(e) and (f), respectively. The inset of Fig. 2(f) shows the distribution of doping concentration for the original doping profile. Since the position of discrete dopants generated in Fig. 1 is random in each direction,

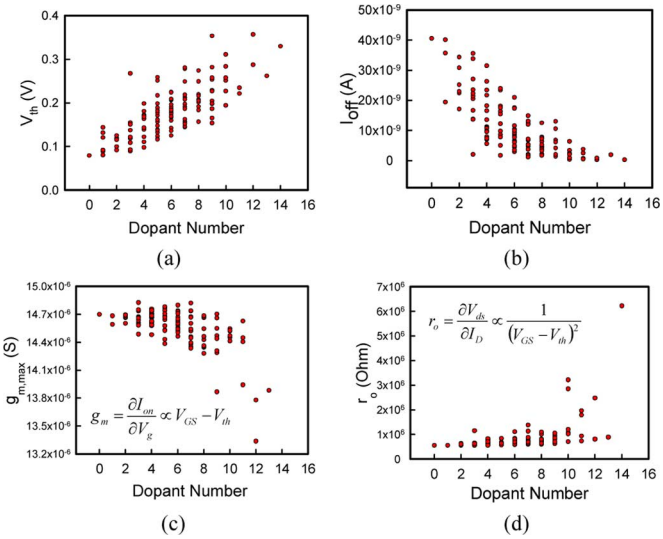

Fig. 3. DC characteristic fluctuations of: (a) $V_{\rm th}$, (b) $I_{\rm off}$, (c) $g_{m,\max}$, and (d) r_o of the 125 discrete dopant fluctuated 16-nm-gate planar MOSFET.

the distribution of dopant number in channel depth is uniform. We notice that the threshold voltages of the nominal devices for both the improved and original doping profiles, whose channel doping profile is continuously doped with 1.48×10^{18} cm^{-3}, are adjusted to be the same value 140 mV. Result shows that numbers of dopant appearing near the channel surface for the improved doping profile is significant less than that of the original doping profile, and thus may induce less surface potential fluctuation than the other.

III. Results and Discussion

In this section we first discuss the high-frequency characteristic fluctuations induced by discrete dopant through the characteristic fluctuation of device viewpoint. Then the improved doping profile technique is quantitatively calculated to examine the associated fluctuation suppression in both dc and high-frequency characteristic fluctuations.

Fig. 3 shows the dc characteristic fluctuations of the 125 discrete dopant fluctuated 16 nm planar MOSFETs. From the random-dopant-number point of view, the equivalent channel doping concentration is increased when the dopant number increases, which substantially alters the threshold voltage $(V_{\rm th})$, off-state currents $(I_{\rm off})$, maximum transconductance $(g_{m,\max})$, and output resistance of transistor (r_o), shown in Fig. 3(a)–(d), respectively. The threshold voltage is determined from a current criterion that the drain current larger than 10^{-7} (W/L) ampere. An expression of $g_{m,\max}$ and the output resistance of transistor (r_o) are shown in insets of Fig. 3(c) and (d). As the number of dopants in channel is increased, the device's $V_{\rm th}$ is increased and thus decreases the off-state current. Since the threshold voltage is increased with increasing channel doping concentration, according to the definition in insets of Fig. 3(c) and (d), $g_{m,\max}$ is decreased and r_o is increased as the number of dopants is increased. The position of random dopants induced different fluctuation of characteristics in spite of the same number of dopants. Furthermore, the magnitude of the spread characteristics increases as the number of dopants increases.

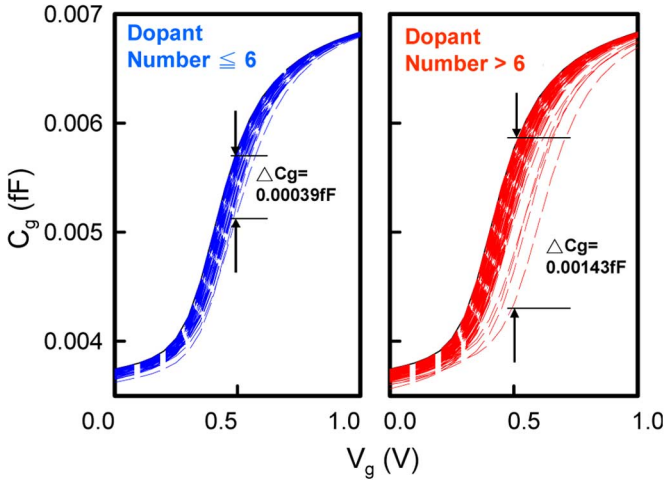

Fig. 4. Fluctuations of $C_{\rm g}$ for the 125 discrete dopant fluctuated 16-nm-gate planar MOSFET. The left plot is for the cases of the number of dopants equal or less than six, the average number whose equivalent channel doping concentration is 1.48 × 1018 cm^{-3}, and the right one is for the cases of the number of dopants larger than six.

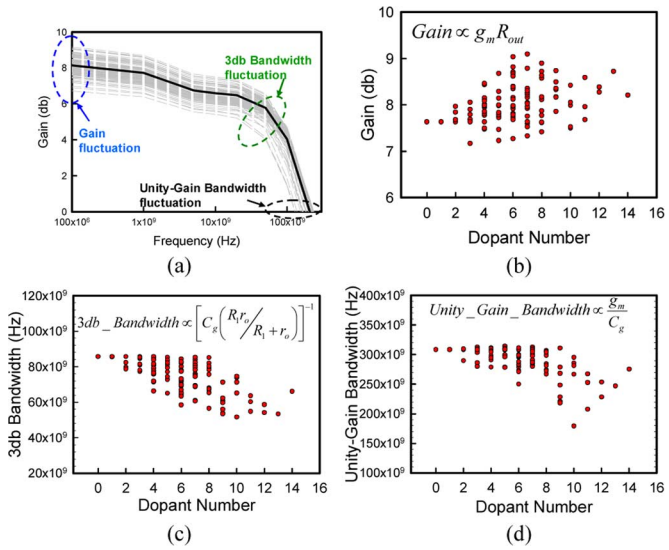

Fig. 5. (a) High frequency response of the 125 discrete dopant fluctuated 16-nm-gate planar MOSFET, where the black line indicates the nominal case and dashed lines are the discrete dopant fluctuated cases. (b) Gain, (c) 3 dB bandwidth, and (d) unity-gain bandwidth fluctuations of the 125 discrete dopant fluctuated 16-nm-gate planar MOSFET circuit.

The detailed physical mechanism is described somewhere else [21]–[25].

The fluctuation of gate capacitance $(C_{\rm g})$, as shown in Fig. 4, indicates that the maximum variation of gate capacitance $(\Delta C_{\rm g})$ is dominated by the number of discrete dopants. For cases with number of dopants in device channel larger than six, the average number whose equivalent channel doping concentration is 1.48 × 10^{18} cm^{-3}, the maximum variation of $C_{\rm g}$ under 0.5 V gate voltage is about 0.00143 fF, which is about 3.5 times larger than other cases with number of dopants in channel equal or less than six. The magnitude of fluctuation is increased as number of dopants is increased. Therefore, as expected, the device characteristic is much more scattered as the number of dopants is increased, as shown in Fig. 3. Therefore, we can infer a larger high-frequency characteristic fluctuation induced by larger numbers of dopant in the nano-MOSFET circuit.

Fig. 5(a) shows the circuit gain versus operation frequency for all fluctuated cases, where the solid line shows the nominal case, whose channel doping profile is continuously doped with 1.48 × 10^{18} cm^{-3}. The circuit gain, 3 dB bandwidth, and unity-gain bandwidth of the nominal case are 8.14 dB, 68 GHz, and 281 GHz, respectively. The corresponding high-frequency characteristic fluctuations for the explore circuit are explored, as shown in Fig. 5(b)–(d), where the insets show the trend of circuit gain, 3 dB bandwidth, and unity-gain bandwidth as a function of device characteristic and circuit element. The gain of the studied circuit is proportional to transconductance multiplied by output resistance of circuit. The circuit output resistance $R_{\rm out}$ is given by

$$R_{\rm out} = \left(\frac{I_{\rm out}}{V_{\rm out}} + \frac{1}{r_o}\right)^{-1} \tag{1}$$

where $I_{\rm out}$ and $V_{\rm out}$ are the output current and voltage of the studied circuit. As the number of dopants in device channel is increased, the on-state current of transistor, which associated with the output current of the test circuit, is decreased and thus increases the output voltage of the circuit. Additionally, the output resistance of transistor, r_o, is increased with increasing threshold voltage. Therefore, the circuit output resistance, $R_{\rm out}$, is increased as threshold voltage is increased. We notice that although the dependence of $R_{\rm out}$ and g_m on threshold voltage is opposed, the trend of circuit gain fluctuation is dominated the output resistance due to the square dependence of r_o on $V_{\rm GS} - V_{\rm th}$. Therefore, the trend of circuit gain fluctuation is dominated by the output resistance and increased as number of dopant is increased, as shown in Fig. 5(b). Fig. 5(c) and (d) show the fluctuation of 3 dB bandwidth and the unity-gain bandwidth of the nano-MOSFET circuit, which indicate the variations of switching speed nano-MOSFET circuit resulted from random discrete dopants. The insets of Fig. 5(c) and (d) show the main sources of variations contributed from device characteristics fluctuations, g_m, r_o, and $C_{\rm g}$, as shown in Figs. 3(c) and (d) and 4. As the number of dopant in device channel is increased, the depletion width is decreased, and then increases the gate capacitance. The fluctuation of $C_{\rm g}$ accompanied with increasing r_o and decreasing g_m result in a decrement of 3 dB bandwidth and the unity-gain bandwidth on increasing dopant number. Similar to the dc characteristic of device, the high-frequency characteristic fluctuation of the nanoscale MOSFET circuit is much more scattered as number of dopants is increased. The standard deviations of the gain, 3 dB bandwidth, unity-gain bandwidth, and gain-bandwidth product are 0.46 dB, 9.63 GHz, 29.3 GHz, and 64.4 GHz, respectively. The high-frequency characteristic fluctuations of the tested circuit are summarized in Table I.

To evaluate the fluctuation suppression technique [18], [24], [27] on high-frequency characteristic fluctuations of the nanoscale MOSFET circuit, an improved vertical doping profile is implemented, where both the mean position and the three sigma of the vertical doping profile are eight nanometers. The

TABLE I
SUMMARIZED HIGH-FREQUENCY CHARACTERISTIC FLUCTUATIONS OF THE NANO-MOSFET CIRCUIT

	Gain (db)	3dB bandwidth (Hz)	Unity-gain bandwidth (Hz)
Nominal	8.138	$6.84\text{x}10^{10}$	$2.81\text{x}10^{11}$
Standard deviation	0.465	$9.63\ \text{x}10^{9}$	$2.93\text{x}10^{10}$
Variation	0.057	0.141	0.104

discrete dopants locating near the channel surface may substantially alter the surface potential and then disturb the distribution of electric field and current conducting path. The characteristic of device is significantly perturbed by both number and position of discrete impurities [21]–[25]. The mechanism of channel engineering is to reduce the probability of dopants appearing at channel region by introducing a lightly channel doping near the surface. Moreover, the holes in the heavily doped region, the mean position of the vertical doping profile, start to screen the charge of the discrete random acceptors in the depletion layer, reducing their effect on the threshold voltage fluctuation. Any further increase of doping concentration in the heavily doped region reduces further the width of the depletion layer and enhances the screening [27]. Fig. 6(a) shows the $I_{\rm D} - V_{\rm G}$ characteristics of the discrete dopant fluctuated device generated from the improved (dashed lines) and the original (solid lines) doping profiles. The spreading range of the improved doping profile is reduced and indicates a suppression of fluctuation on dc characteristic of device. The fluctuation of the threshold voltage is shown in Fig. 6(b), where the square symbol indicates the cases of the improved doping profile and the "×" symbols symbol shows the cases of original doping profile. The scattering range of the threshold voltage is significantly suppressed, and the fluctuation of threshold voltage is reduced from 58.5 mV to 50.2 mV. Fig. 6(c)–(e) show the fluctuations of the on-state current $(I_{\rm on})$, and maximum transconductance $(g_{m,\max})$, respectively. As expected, the fluctuation of on-state current and maximum transconductance is effectively suppressed due to the less dopant locating near the channel surface. However, the fluctuation of off-state current can not be further suppressed due to the similar numbers of dopant locating near the path of leakage current (about 4 nm below the gate oxide). This result implies the importance of the vertical doping profile optimization.

Fig. 7(a) shows the gate capacitance fluctuation of the studied doping profiles, where the dashed and solid lines show the improved and the original doping profile, respectively. The fluctuation of gate capacitance is suppressed by 16.4%. The screening effect in the heavily doped region screens the charge of the discrete random acceptors in the thin depletion layer, and reduces their effect on the gate capacitance fluctuation. The suppressed fluctuation of gate capacitance and dc characteristic of device implies the effectiveness of the fluctuation suppression technique on the high-frequency characteristics. The high-frequency response of the nanoscale MOSFET circuit is shown in Fig. 7(b). As expected, the spreading range of the improved doping profile is reduced through the improvement of doping profile. The fluctuation of the high-frequency characteristics, the circuit gain, the

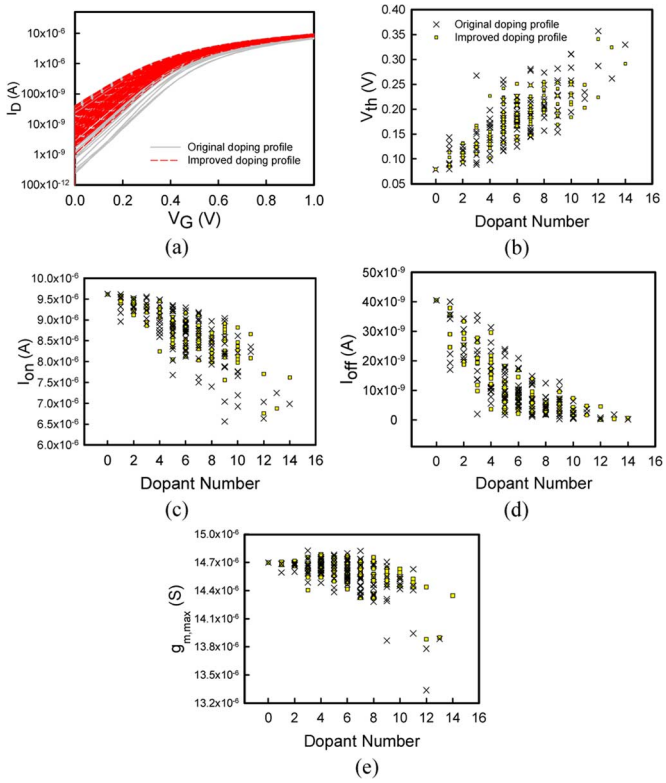

Fig. 6. Fluctuations of: (a) $I_{\rm D} - V_{\rm G}$, (b) $V_{\rm th}$, (c) $I_{\rm on}$, (d) $I_{\rm off}$, and (e) $(g_{m,\max})$ of the 125 discrete dopant fluctuated 16-nm-gate planar MOSFETs, where the square and "×" indicate the cases of the improved and original doping distributions, respectively.

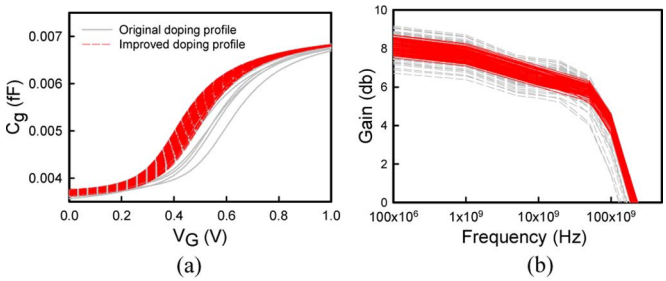

Fig. 7. Comparison of gate capacitance and frequency response fluctuations of the discrete dopant fluctuated 16-nm-gate cases generated from the improved (dashed line) and original (solid line) doping distributions.

3 dB bandwidth and the unity-gain bandwidth of the nanoscale MOSFET circuit are calculated; as shown in Fig. 8(a)–(c), the square and "×" symbols indicate the cases of the improved and original doping distributions. The effectiveness of fluctuation suppression technique in nanoscale device and circuit is summarized in Fig. 9. The fluctuation suppressions of the characteristics of the nanoscale device circuit are more pronounced than that of device due to the second-order nonlinear effect of circuit characteristics. The fluctuation suppression of the high frequency characteristics is resulted from less dc characteristic and gate capacitance fluctuation of device by introducing a doping profile of Gaussian distribution along the longitudinal direction from surface to substrate. The result confirms the fluctuation suppression technique on high-frequency characteristic fluctuation of nanoscale device circuit and show the effectiveness of

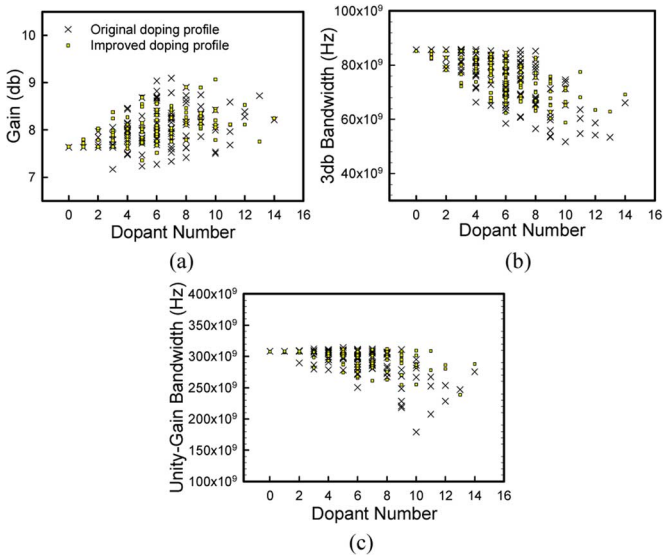

Fig. 8. Comparison of: (a) gain, (b) 3 dB bandwidth, and (c) unity-gain bandwidth fluctuations of the 125 discrete dopant fluctuated 16-nm-gate planar MOSFET circuit with the improved (squares) and original ("×") doping profiles.

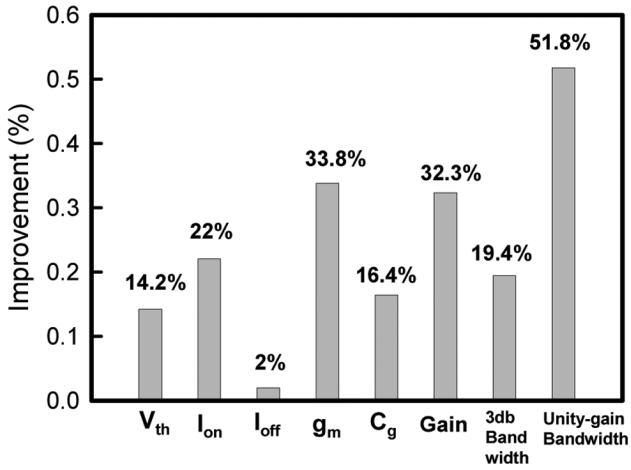

Fig. 9. Effectiveness of fluctuation suppression technique in both the nanoscale device and circuit.

TABLE II
COMPARISON OF HIGH-FREQUENCY CHARACTERISTIC FLUCTUATIONS FOR DEVICES WITH ORIGINAL AND IMPROVED DOPING PROFILE

	V_{th} (mV)	I_{on} (A)	I_{off} (A)	$g_{m,max}$(S)	C_g ($\times 10^{-3}$fF)
Original	58.5	6.7×10^{-7}	9.5×10^{-9}	2.1×10^{-7}	0.24
Improved	50.2	5.2×10^{-7}	9.3×10^{-9}	1.4×10^{-7}	0.20

	Gain (db)	3dB bandwidth (Hz)	Unity-gain bandwidth (Hz)
Original	0.465	9.63×10^{9}	2.93×10^{10}
Improved	0.314	7.76×10^{9}	1.14×10^{10}

fluctuation suppression technique. The comparison of characteristic fluctuations for devices without and with doping profile improvement is summarized in Table II.

IV. CONCLUSIONS

In this paper, both the discrete-dopant-induced dc and high-frequency characteristics fluctuations of 16-nm-gate MOSFET circuit have been studied using a 3-D "atomistic" simulation technique. Using the experimentally calibrated analyzing technique, the result have shown that the discrete-dopant fluctuated 16 nm MOSFET circuit exhibits 5.7% variation of the circuit gain, 14.1% variation of the 3 dB bandwidth and 10.4% variation of the unity-gain bandwidth. Without loss the device and circuit performance, by considering a doping profile with less dopants locating near surface of channel, the suppression technique on high-frequency characteristic fluctuations of the nanoscale transistor circuit have also shown its effectiveness. The improved doping profile significantly reduces the intrinsic characteristic fluctuation in the device level, and thus suppressed fluctuations of the tested circuit gain, the 3 dB bandwidth and the unity-gain bandwidth, and the reductions are 32.3%, 19.4%, and 51.8%, respectively. Experimental and theoretical verification will benefit the development of high-frequency 16-nm-gate MOSFET circuit; an experiment is thus currently under conducting to design, fabricate and measure the high-frequency characteristic fluctuations of the nanoscale device circuit.

We notice that the parasitic effects may play very important role in determining the overall high frequency performance in nanoscale transistor. Therefore, we have included the effects of the gate to source/drain overlap capacitance and the inner fringing capacitance in our modeling and simulation. According to the 2007 ITRS roadmap, the ideal gate capacitance per micron device width in inversion is about 0.671 fF/μm. The total gate capacitance per micron device width in inversion including the parasitic gate overlap/fringing capacitance per micron device width [including the Miller effect] is about 0.835 fF/μm. Therefore, the parasitic gate overlap/fringing capacitance is about 20% $((0.835-0.671/0.835)*100\% = 20\%)$ of the total gate capacitance. Besides the ITRS roadmap, according to [49], the effective fringing capacitance of state-of-art MOSFET is about 0.55 fF/μm and independent of the technology node, where the outer fringing capacitance is about 0.13 fF/μm. Compare it with the total gate capacitance of 0.68 fF/μm, the outer fringing capacitance is about 16% $((0.13/0.68)*100\% = 16\%)$ of the total gate capacitance. We believe that our simulation approach can reflect the dominating factor on RF performance. To include the parasitic effect in nanoscale transistors' circuit, a 3-D field simulation coupling with device and circuit simulation could be considered.

There are some practical and theoretical issues that worth to be addressed in our future work, such as the performance parameter fluctuations of high frequency characteristics, calibration of high-frequency measurement data, high-frequency circuit (e.g., LNA, mixer, etc) simulation, parasitic capacitance of nano-device, and modeling of device variability. This study is mainly based upon a large-scale statistically sound "atomistic" device and circuit coupled simulation methodology in time-domain for discrete-dopant-fluctuated nano-CMOS circuits. We are currently formulating the mathematical models and implementing this methodology in frequency domain together with harmonic balance technique, which will directly benefit the characteristic estimation using the frequency domain results, such as the calculation of S-parameters. For the design and optimization of high-frequency devices and circuits, the numerical simulation is the first step toward the modeling of

device variability and the development of compact modeling for capturing device variability is urgent.

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