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碩士論文

可適性調整相位邊限之電流回授補償技術
應用於無電容式低壓降線性穩壓器

Current Feedback Compensation Technique
for Adaptively Adjusting the Phase Margin
in Capacitor-Free LDO Regulators

研究生：楊奐箴
指導教授：陳科宏 博士

中華民國九十六年十二月

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研 究 生：楊奐箴　　Student：Huan-Chien Yang

指導教授：陳科宏　　Advisor：Ke-Horng Chen

國 立 交 通 大 學

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摘 要

隨著可攜式設備的蓬勃發展，為了有效使用分配有限的電池能量，電源管理系統是不可或缺的一環。低壓降線性穩壓器具有架構簡單、低雜訊、低成本的優點，對於電源管理晶片系統來說，低壓降線性穩壓器是一個非常重要而且廣泛應用的單元。

傳統低壓降線性穩壓器利用外部電容串聯寄生電阻補償，然而增益及極點位置隨負載變動，使得寄生電阻補償方式更顯得複雜。近年來，對於高效能(高精準度、高電源排斥比)之線性穩壓器需求越來越大，多級放大器之線性穩壓器恰可達到這個需求。同時，隨著系統單晶片的發展，無電容式之線性穩壓器逐漸受到重視。由於不需要外掛電容，電路板面積可大幅縮減，成本也大為降低。然而多級放大器之線性穩壓器的缺點是有最低負載的限制，導致無載時的功率耗費。

本論文將提出一可適性調整相位邊限之電流回授補償技術應用於無電容式低壓降線性穩壓器，此電流回授補償技術可可適性調整相位邊限在 60°左右以達到快速之暫態反應能力。同時，在不犧牲頻寬之情況下，最低負載限制大幅降低至 50μA。此外，電流回授補償技術使用與品質因素降低技術相當的補償電容，但電流回授補償技術可維持高的電源排斥能力頻寬。本論文使用 TSMC 0.35μm2P4M 製程，補償電容僅需 5pF 以及 1.5pF。實驗結果顯示，最低負載限制大幅降低至 50μA，而具可適性相位控制之低壓降線性穩壓器之暫態反應時間小於 4μs。

Current Feedback Compensation Technique for Adaptively Adjusting the Phase Margin in Capacitor-Free LDO Regulators

Student: Huan-Chien Yang Advisor: Dr. Ke-Horng Chen

Department of Electrical and Control Engineering
National Chiao-Tung University

Abstract

With the increasing demanding of portable devices, how to use the battery energy efficiently is the most concerned problem. Therefore, power management system is indispensable for modern consumer products. For power management system, low-dropout (LDO) liner regulator is the most common block due to the characteristics, such as simplicity, small board space, low noise and cost.

Conventional LDO regulator is compensated by the equivalent series resistor (ESR). However, this kind compensation is hardly to maintain because gain and poles locations are varied with load conditions. In recent years, the demanding for high performance liner regulator such as high load regulation and high power supply rejection is getting growing. The Multi-stage LDO can achieve this target. Meanwhile, with the development of SoC system, a capacitor-free LDO is preferred to reduce the board space and cost greatly. However, the most important disadvantage of multi-stage LDO is the minimum load restriction.

Therefore, a current feedback compensation (CFC) technique for capacitor-free LDO regulators with adaptively adjusting the phase margin is proposed in this thesis. CFC technique can adaptively adjust the phase margin for achieving better transient response than that with variant phase margin at different load current conditions. Not only fast transient response is attained due to suitable phase margin but also the minimum load current limitation can be greatly reduced to about 50μA without sacrificing bandwidth at light load current condition. Besides, CFC technique can have high PSRR bandwidth with compatible compensation capacitors compared to the Q-reduction technique. The capacitor-free LDO regulator with CFC technique is fabricated by TSMC 0.35μm 2P4M CMOS process with small compensation capacitors 5pF and 1.5pF. Experimental results demonstrate that the minimum load can be reduced to 50μA and transient response time with adaptively phase margin control is smaller than 4μs.

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Chapter 1

Introduction

Power management has become a more and more popular topic in recent years, especially for the battery-operated portable devices due to the longer using time. In other words, using the energy economically and power-saving techniques due to efficiency enhancement are two major solutions to achieve this target. In this chapter, we will show you why we need power management systems and what it is in Chapter 1.1 first. Second, we give a brief introduction about power management system common blocks, such as switching converters, liner regulators, and charge pump converters, and compare these different regulators in Chapter 1.2. In Chapter 1.3, we will show you why the linear regulators are the most common and important block in power management system. Finally, we will give our motivation in Chapter 1.4.

1.1 Power Management system

With the explosion development of integrated circuit, more and more functions are embedded in a device to meet the consumer requirement. As shown in Fig. 1, the growing of battery energy is not satisfied to chip requirement. But the running time of the portable devices, such as the lap tap, mobile phones and digital cameras, is a very important requirement for the consumers. Therefore, how to save the battery energy and use it more efficiently is the most important topic.

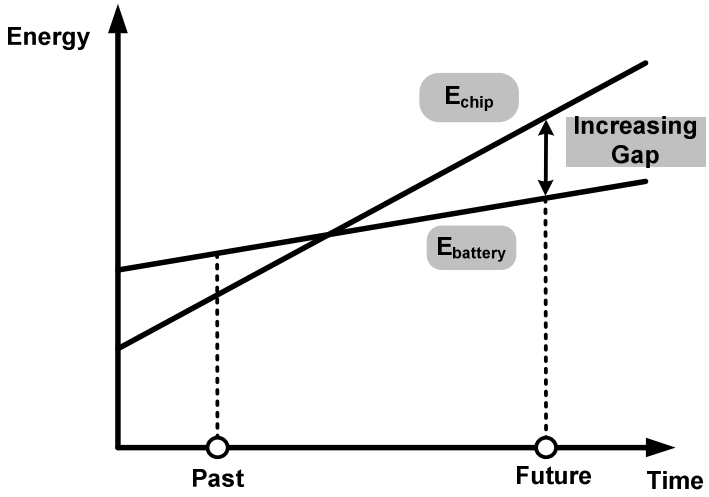


Fig. 1. Energy of chip requirement.

As mentioned before, the increase of battery content doesn't satisfy device requirement. In the other way, we must construct a power system using energy as economically as possible. As shown in Fig. 2, it may have many powered devices for a portable device. For example, a mobile phone may need at least five regulated voltages, one buck converter for core CPU, one boost converter for cooler LCD panel, one high PSRR LDO regulator for RF power amplifier, one LDO regulator for analog base-band, and one charge pump for white light LED driver. These blocks are only needed powered when the function are active. Therefore, the control unit of power management system has ability to shutdown, sleep, or active some power sources depended on the powered devices requirements. On the other hand, we can also enhance the efficiency of power sources, such as switching converter, linear regulator, and charge pumps. In this way, we can decrease the power dissipation to the minimum, and enhance the operating time to the longest. This is why the power management system becomes more and more important, especially for portable devices.

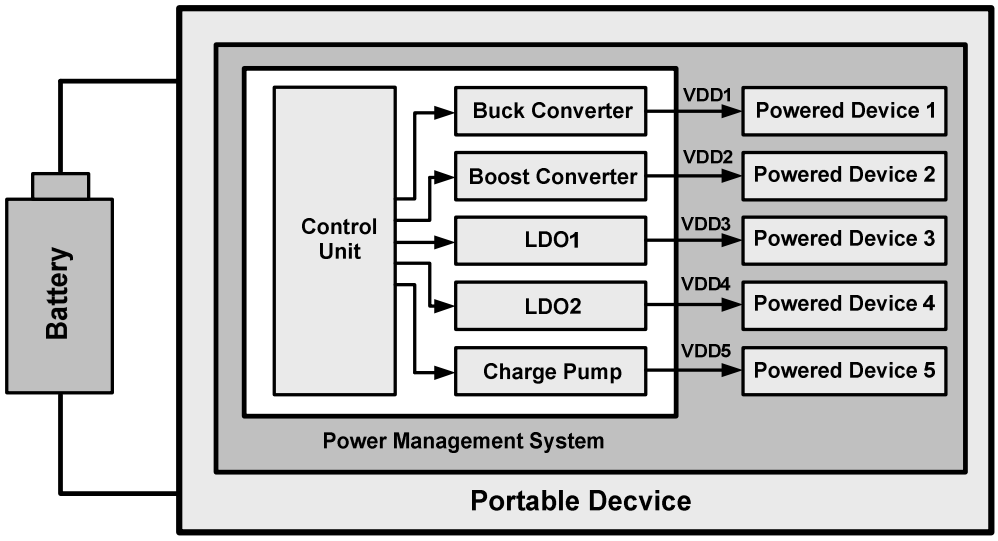


Fig. 2. Power management system.

1.2 Introduction to Different Regulators

In this section, we will give a brief introduction to three types of most common regulators, linear regulator, switching converter, and charge pump. Finally, we give a comparison about these three types of regulators.

1.2.1 Linear Regulator

As shown in Fig. 3, the linear regulator consist of a error amplifier to correct input and output difference, a pass device to supply load current, and a resistive feedback network. The structure is the most compact without complex control circuit, results in smaller chip size and cost. The linear regulator utilizes the feedback network to construct shut negative feedback effect to regulate the output voltage. In this way, this kind of regulator does not need switching clock, so the output noise can be minimized and the output voltage does not exist ripple. Without dual storage components, linear regulator only can be operated in buck operation. The efficiency of linear regulator is about the output voltage dividing input voltage. The highest

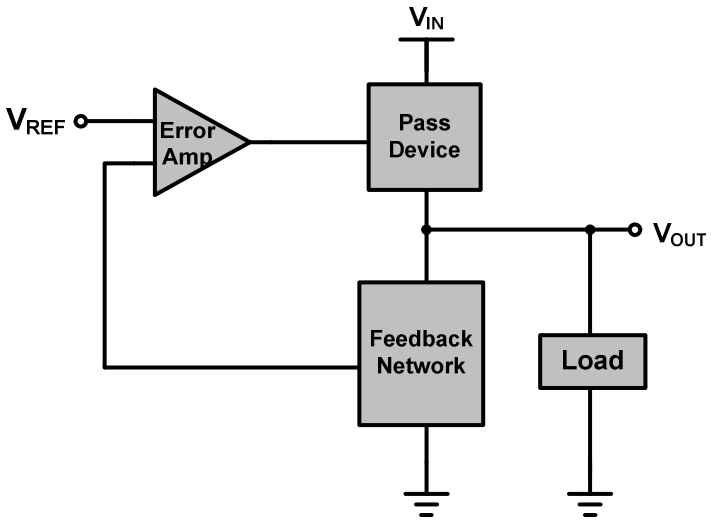


Fig. 3. Linear regulator.

efficiency occurs that output voltage is near input voltage, i.e. low dropout operation. The supply load ability depends on pass device's size.

1.2.2 Switching Converter

As shown in Fig. 4, this is a conventional voltage mode switching buck converter. It compares the output voltage with reference voltage to decide the duty cycle. When power PMOS conducts, the supply voltage will charge the inductor and capacitor. And in the next time, the power NMOS conducts, so the inductor will be discharged to the capacitor. Due to dual storage components, inductor and capacitor, the switching converter can be operated in buck or boost operation. Generally speaking, the efficiency can be achieved above 90% under heavy load condition. Meanwhile, with higher switching frequency in the range of hundreds of Kilo-Hertz to several Mega-Hertz, the storage components can be designed smaller to save the cost. But the EMI and noise problems become critical. Depended on efficiency requirement, the control circuit is much larger than the other two and the cost is the most. The supply

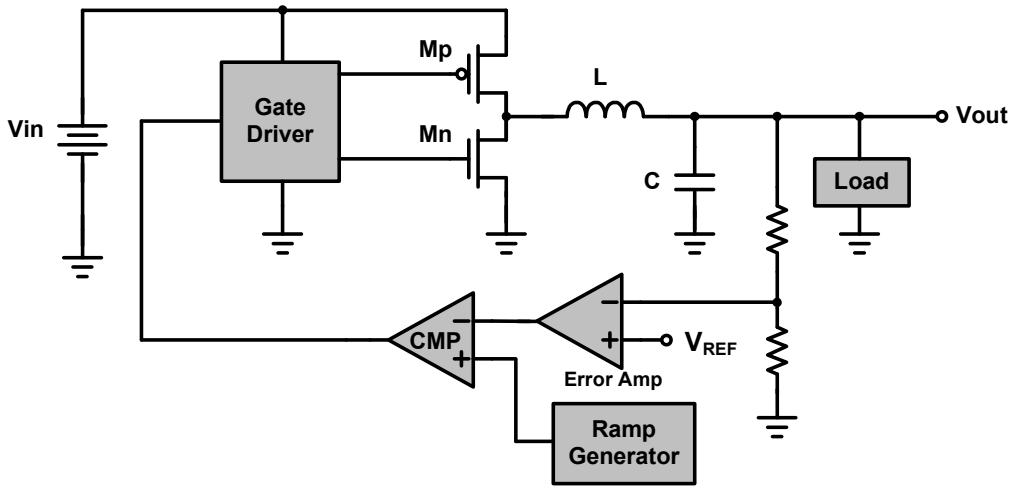


Fig. 4. Conventional voltage mode switching buck converter.

load ability is the largest always in the range about hundreds of milliamps to several amps.

1.2.3 Charge Pump

As shown in Fig. 5, this is a conventional charge pump converter. During ϕ_1 phase, the input voltage charges C_s to input voltage. During ϕ_2 phase, the output equals to input voltage adding voltage across C_s, and gets twice input voltage. With hysteric feedback control, the output is regulated at desired output voltage. The charge pump can also be operated in buck or boost mode, but the efficiency is higher in boost mode. The control circuit is more compact than switching converters, but more complex than linear regulators. Due to switching clock, charge pump also suffers from EMI and noise problems. But these problems are slighter than switching converters', results from smaller switching frequency in the range of hundreds of Kilo-Hertz. The supply load ability of charge pump is weak, because this depends on capacitor size and switching frequency.

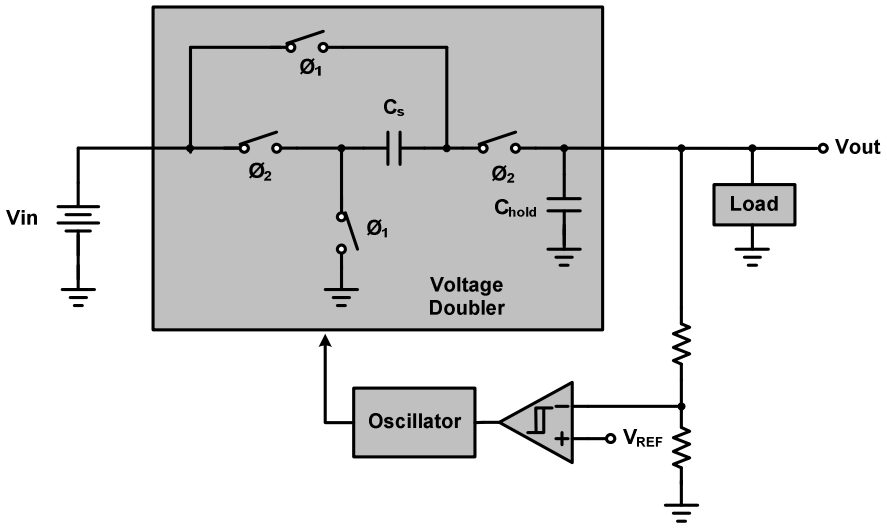


Fig. 5. Charge pump converter.

1.2.4 Comparison

In the above discussion, each type of regulator has its own advantages and disadvantages. Before deciding using which type of regulators as power source, you must take a good tradeoff between these characteristics.

TABLE I

COMPARISONS OF DIFFERENT TYPE REGULATORS.

Characteristic	*Linear Regulator*	*Switching Converter*	*Charge Pump*
Buck/Boost	Buck only	Buck/Boost	Buck/Boost
Efficiency	Minimum	Maximum	Medium
EMI/Noise	Minimum	Maximum	Medium
Supply Ability	Medium	Maximum	Minimum
Complex	Simplest	Most	Medium

1.3 Importance of Linear Regulator

The linear regulator is wildly used in power management system due to the compact structure results in low cost advantage. Meanwhile, without switching

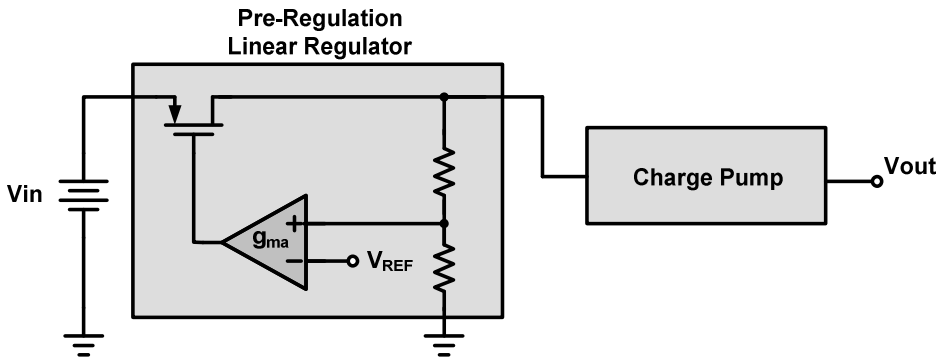


Fig. 6. Linear regulator served as pre-regulator.

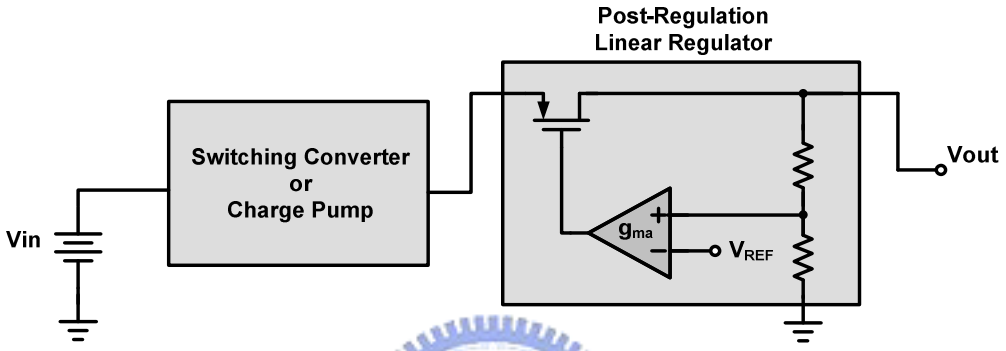


Fig. 7. Linear regulator served as post-regulator.

topology, the EMI and noise issues are minimized, especially for audio devices. On the other hand, the linear regulator can be cascaded before a charge pump as shown in Fig. 6. The linear regulator can supply a pre-regulated output voltage for charge pump, which input ripple and noise are minimized. This topology is widely used in white LED driver.

Meanwhile, the linear regulator can be cascaded after a switching converter or charge pump as shown in Fig. 7. The linear regulator is served as a post-regulator in order to minimize the output noise and ripple required by powered devices.

Via the above discussion, we know that linear regulators are the key and most common component in power management system. For modern power management system, designing a high performance linear regulator is essential. But there are still many difficulties in designing a high performance linear regulator.

1.4 Motivation

As well known, conventional low-dropout liner regulator is compensated by the equivalent series resistor (ESR). However, this kind compensation is hardly to maintain because gain and poles locations are varied with load conditions. In the recent years, the demanding for high performance liner regulator such as high resolution and high power supply rejection is getting growing. The Multi-stage LDO can achieve this target. Meanwhile, with the development of SoC system, a capacitor-free LDO is preferred to reduce the board space and cost greatly. However, the most important disadvantage of Multi-stage LDO is the limitation of minimum load.

Therefore, a current feedback compensation (CFC) technique for capacitor-free LDO regulators with adaptively adjusting the phase margin is proposed in this thesis. CFC technique can adaptively adjust the phase margin for achieving better transient response than that with variant phase margin at different load current conditions. Not only fast transient response is attained due to suitable phase margin but also the minimum load current limitation can be greatly reduced to about 50μA without sacrificing bandwidth at light load current condition. Besides, CFC technique can have high PSRR bandwidth with compatible compensation capacitors compared to the Q-reduction technique. The capacitor-free LDO regulator with CFC technique is fabricated by TSMC 0.35μm 2P4M CMOS process with small compensation capacitors 5pF and 1.5pF. Experimental results demonstrate that the minimum load can be reduced to 50μA and transient response time with adaptively phase margin control is smaller than 1μs.

Chapter 2

Convention al and Proposed LDO Regulators

From the previous discussion, the linear regulator is the most common component of power management system. With requirement of high performance LDO regulator, such as high load and line regulation, high power supply rejection ability, and fast transient response, the LDO regulator design becomes more and more difficult. In this Chapter, we will give you a complete introduction of low dropout voltage (LDO) regulator, and point out what problems they have. In the Chapter 2.1, we will give you an overall introduction to linear regulator performance definition first. Second, we will describe how a conventional LDO regulator works and what problems it has in the Chapter 2.2. Third, in order to solve the conventional structure problems, many structures have been proposed. But they inherently have lots of problems, we will show then in Chapter 2.3. Finally, to enhance LDO regulator performance dramatically, multi-stage LDO regulator design has been proposed. Inevitably, this kind of topology has many unsolved problems. Therefore, we will describe it in the Chapter 2.4.

2.1 Definitions of LDO Regulator

In this section, we will show you the LDO regulator's performance definitions, such as dropout voltage, quiescent current, efficiency, transient response, line and load regulation,

power supply rejection, and accuracy [1][2].

2.1.1 Dropout Voltage

The dropout voltage means that the difference between input voltage and output voltage when the shut feedback effect ceases to regulate the output voltage to a desired value under the maximum load condition. To more specified definition, the dropout voltage occurs at the output voltage drifted 2% of its value. When the dropout region occurs, the pass device is operated in linear region. Therefore, the dropout voltage can be expressed in equation (1).

$$V_{dropout} = I_o R_{on} \tag{1}$$

In modern LDO regulator design, efficiency is the most concerned performance. The dropout voltage is always designed about 200mV under maximum load current condition. In order to achieve low dropout voltage maintaining high efficiency, one way is to increase the power MOS size, but this will increase the chip size and results in more complex compensation. The other way is to increase the loop gain. The larger loop gain can maintain the regulation even if the power MOS operated in linear region.

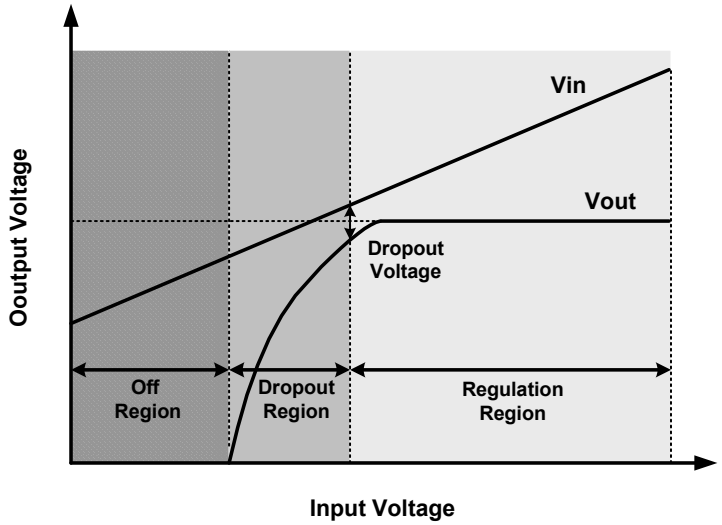


Fig. 8. Definition of dropout voltage.

2.1.2 Efficiency

The efficiency of linear regulator is defined as output power divide input power. The output power equals to output voltage multiply load current. The input power equals to input voltage multiply with load current and quiescent current. The quiescent current consists of bias current such as error amplifier bias current, band-gap reference current, feedback resistance network, and so on. In heavy load, the load current is far larger than the quiescent current, and the efficiency depends on the difference between input and output voltage, i.e. dropout voltage. In light load, the quiescent current may be near the load current, and the efficiency is further decreased. Therefore, we must minimized quiescent current at light load condition and the dropout voltage to achieve higher efficiency performance.

$$Efficiency = \frac{I_{Load} V_o}{(I_{Load} + I_q) V_i} \times 100\% \tag{2}$$

$$Efficiency_{current} = \frac{I_{Load}}{(I_{Load} + I_q)} \times 100\% \tag{3}$$

2.1.3 Transient Response

Transient response is the dynamic performance of linear regulator [3]. It can be separated into two parts, one is form load variation, named as load transient response, and the other is from line variation, named as line transient response.

As shown in Fig. 9, when the linear regulator suffers a load step current variation, the output voltage will be existed in a transition and variation period. During a load-transition from light load to heavy load, the pass device can't supply such large load current instantly. Therefore, the output voltage experiences a voltage drop. The drop period Δt_1 depends on the close-loop bandwidth BW_{cl}, and the slew rate at power MOS gate terminal. The response

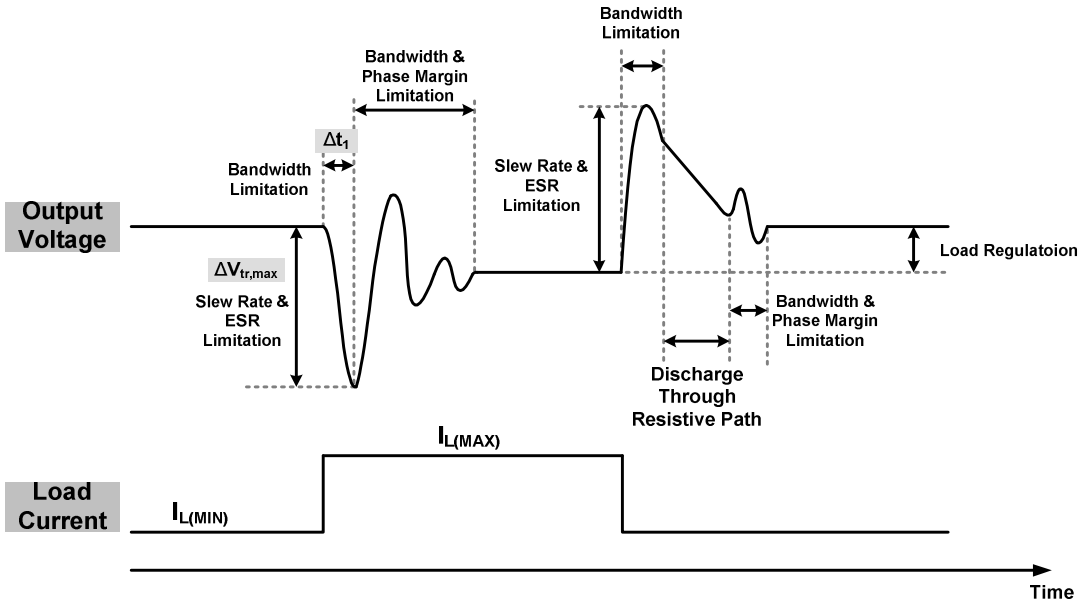


Fig. 9. Load transient response.

time can be approximate in the following equation:

$$\Delta t_1 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{par}\frac{\Delta V}{I_{sr}} \tag{4}$$

where BW_{cl} is the close-loop bandwidth of the linear regulator, C_{par} is the parasitic capacitor of the power MOS at gate terminal, I_{sr} is the bias current under slewing condition.

Due to this response time, the power MOS can't support load current requirement. The load will discharge the output capacitor and cause a voltage drop at this moment as shown in the Fig. 10.

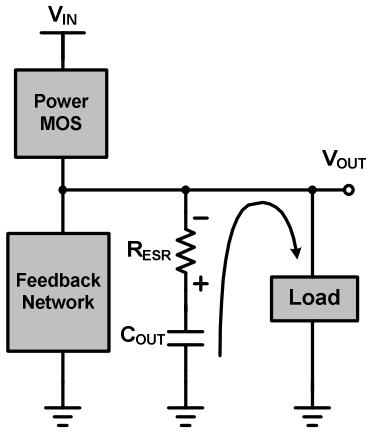


Fig. 10. Output drops during light to heavy load.

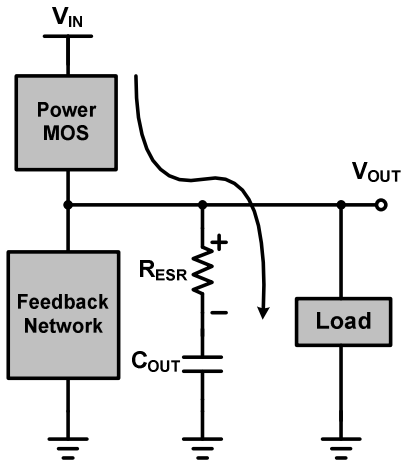


Fig. 11. Output drops during heavy to light load.

The output voltage drop depends on the output slew rate limitation $I_{o,max}/C_{OUT}$ and the system response time $\Delta V_{tr,max}$. The frequency compensation resistor R_{ESR} but also contributes an ESR drop ΔV_{ESR} during transient. The equation is shown in the following:

$$\Delta V_{tr,\max} = \frac{I_{o,\max}}{C_{OUT}} \Delta t_1 + \Delta V_{ESR} \tag{5}$$

Finally, the system will enter in small signal settling region. During this period, the system response is relative to the closed loop bandwidth and phase margin.

For the same reason, during a load-transition from heavy load to light load, the pass device can't shut the power MOS quickly. Therefore, the output voltage experiences a voltage peak. The response is the same as mentioned before, but the voltage peak response has some differences with voltage drop due to resistor R_{ESR}. Since the load step sharply, the power MOS can't shut rapidly. The redundant current will charge the output capacitor with additional ESR peak as shown in Fig. 11.

In the next time, the power MOS has been shunt off, and the unnecessary charge on the output capacitor will be discharge through the resistive network causing a voltage drop as show in Fig. 12. Finally, the output will settle to the desired voltage.

The other dynamic performance is line transient response as shown in Fig. 13, which

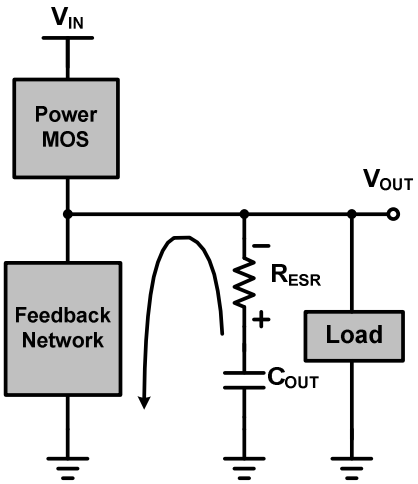


Fig. 12. Output discharge through resistive network.

means that the output variation under input voltage step. The line transient response is like load transient response. When the input step to a smaller value, power MOS will support less load current casing output drop. The response is like load current with light load to heavy load. When the input step to a larger value, power MOS will support more load current casing output peak. The response is like load transient with heavy load to light load.

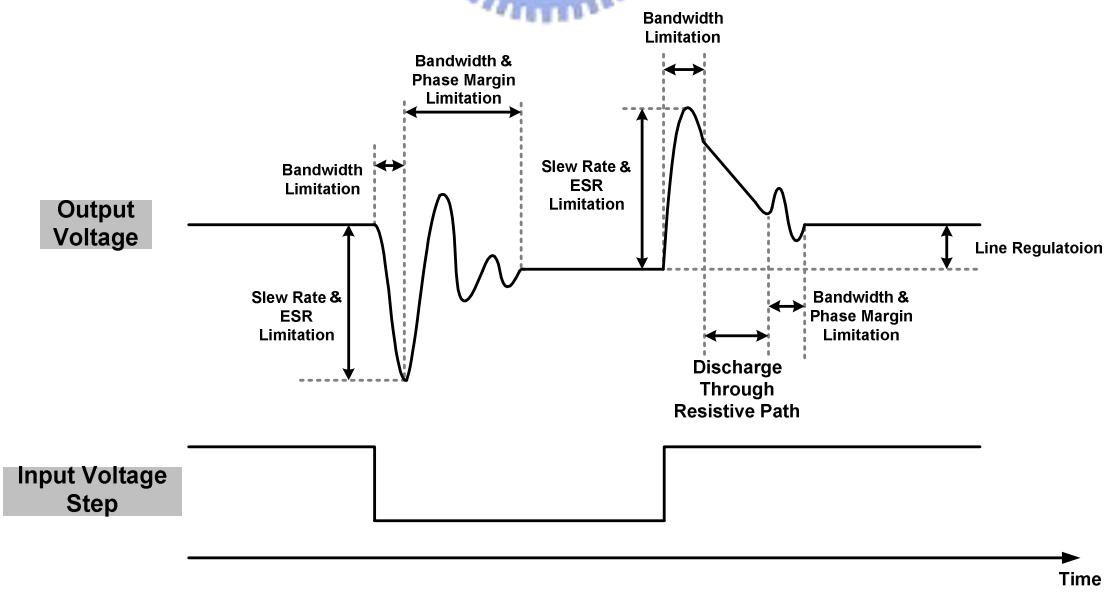


Fig. 13. Line transient response.

For the above discussion, to obtain better transient response, a higher bandwidth of linear regulator, faster slewing at power MOS gate terminal, larger output capacitor, and smaller ESR are recommended.

2.1.4 Line & Load Regulation

Line and load regulation are steady-state performances of linear regulator. These performances are two important specifications that related to output voltage accuracy. The line regulation means that the output voltage variation at different input conditions as shown in Fig. 14. To get better line regulation, a higher loop gain is required, but the stability is sacrificed. There is a tradeoff between precision and stability.

$$Line\ Regulation = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \approx \frac{g_m r_o}{L_o} + \frac{1}{\beta} \cdot \left(\frac{\Delta V_{REF}}{\Delta V_{IN}}\right) \tag{6}$$

where L_o is the loop gain of linear regulator, g_m and r_o are the transconductance and output resistance of power MOS, β is the feedback factor.

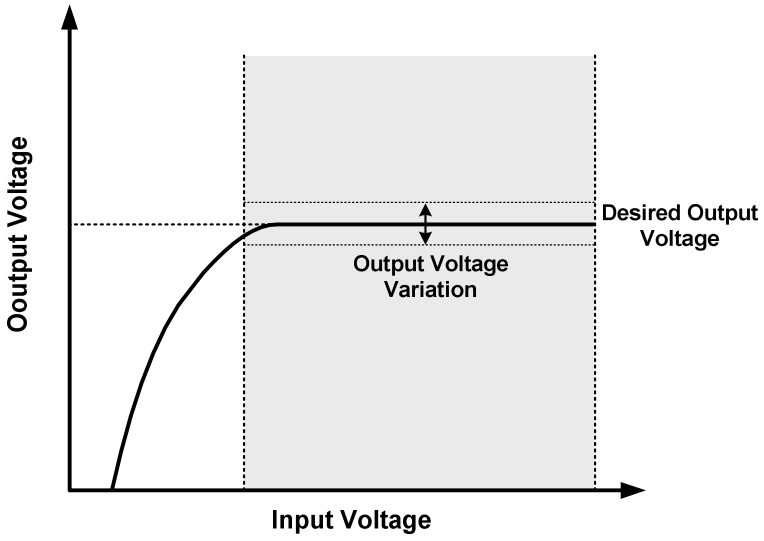


Fig. 14. Definition of line regulation.

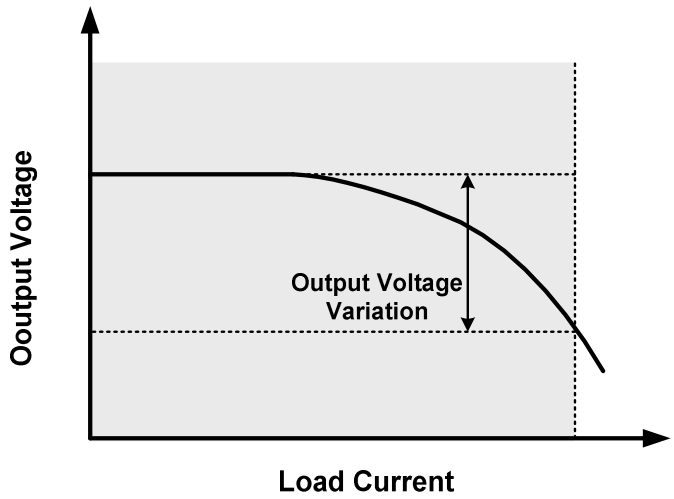


Fig. 15. Definition of load regulation.

The load regulation means that the precision of output voltage under different load conditions as shown in Fig. 15. In order to get better load regulation, a higher loop gain is still required, but the stability problem must be concerned.

$$Load\ \ Regulation = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = -\frac{r_o}{1+L_o} \tag{7}$$

where L_o is the loop gain of linear regulator, r_o is the output resistance of power MOS.

2.1.5 Power Supply Rejection (PSR)

Power supply rejection is a highly important performance of linear regulator. Since it does not using switching type to regulate output, it is widely cascaded before or after the switch type converter to be served as pre-regulator or post-regulator in order to minimize the input supply noise, especially for audio applications [4]-[6].

Due to the shut feedback of linear regulator, the output resistance is reduced a factor of loop gain, L_o. Z_o is the open loop output resistance to the ground, which shown in equation (8). $Z_{o\text{-}shunt}$ is modeling the output resistance of shunt feedback effect under low frequency

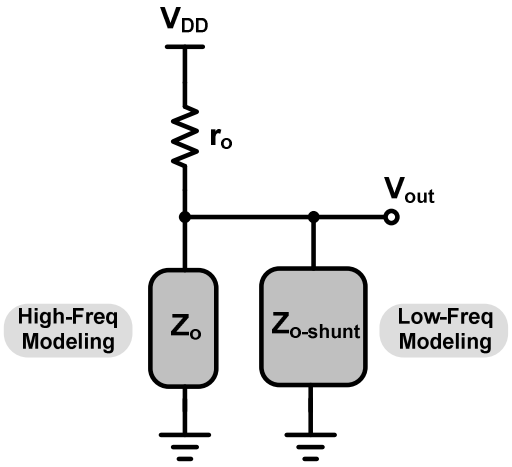


Fig. 16. Approximate modeling of PSR.

condition, which is given is equation (9).

$$Z_o = (Z_{OUT} + R_{ESR}) \| (R_1 + R_2) \tag{8}$$

$$Z_{o-shunt} = \frac{Z_o \| r_o}{L_o} \tag{9}$$

Therefore, the PSR performance of linear regulator can be approximate as simply voltage divider as shown in Fig. 16, which given in equation (10).

$$PSR = \frac{V_{OUT}}{V_{DD}} = \frac{(Z_o \| Z_{o-shunt})}{r_o + (Z_o \| Z_{o-shunt})} \tag{10}$$

At lower frequency, the shunt feedback is largest due to highest loop gain, so $Z_{o\text{-}shunt}$ is the dominant term. And PSR_{dc} can be approximate by voltage divider as following:

$$PSR_{dc} \approx \frac{R_{o-shunt}}{r_o + R_{o-shunt}} = \frac{\frac{r_o \| (R_1 + R_2)}{L_o}}{r_o + \frac{r_o \| (R_1 + R_2)}{L_o}} \approx \frac{1}{L_o} \tag{11}$$

As the frequency increased, the loop gain will be initially to decay at the bandwidth, BW_A, of the error amplifier, i.e. the shut feedback is deteriorated. This will cause a PSR zero at bandwidth of error amplifier. At the unit gain frequency, the shut feedback has no effect on

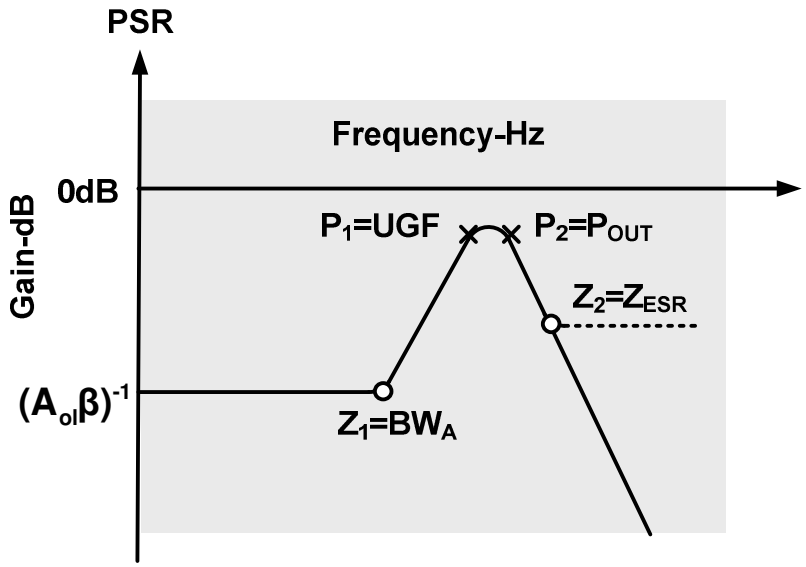


Fig. 17. PSR frequency response.

output resistance, since the loop gain has decayed under 0 dB. The PSR can be approximate as following:

$$PSR_{UGF} \approx \frac{Z_o}{r_o + Z_o} = \frac{(R_1 + R_2)}{r_o + (R_1 + R_2)} \approx 1 \tag{12}$$

At higher frequency, the output capacitor begins to shut the (R_1+R_2) to the ground. The PSR will be improved at output pole. Finally, if the system has ESR, the ESR will cause a PSR zero at high frequency as shown in equation (13).

$$PSR_{f>>UGF} \approx \frac{Z_o}{r_o + Z_o} = \frac{R_{ESR}}{r_o + R_{ESR}} \tag{13}$$

The PSR frequency response can be approximate in Fig. 17. The DC value of PSR is about the reciprocal of loop gain, L_o. With frequency increased to bandwidth of loop gain, the PSR will be deteriorated. The PSR will be decayed to 1 at unit gain frequency of loop gain. Finally, the output will shunt the resistive feedback network to the ground and improve the PSR performance.

2.1.6 Accuracy

The accuracy of linear regulator is considered all the effects, line regulation (ΔV_{LR}), load regulation (ΔV_{LDR}), reference voltage drift ($\Delta V_{o,ref}$), error amplifier drift ($\Delta V_{o,a}$), feedback resistor tolerance ($\Delta V_{o,r}$), and temperature coefficient (ΔV_{TC}), contributing to output voltage variation. The accuracy equation can be described in the equation (14).

$$Accuracy \approx \frac{|\Delta V_{LR}|+|\Delta V_{LDR}|+\sqrt{\Delta V^2_{o,ref}+\Delta V^2_{o,a}+\Delta V^2_{o,r}+\Delta V^2_{TC}}}{V_o}\times 100\% \quad (14)$$

The typical implementations achieve roughly 1% to 3% overall accuracy, results from all the disturbances described before.

2.2 Conventional LDO Regulators

There are many different types of pass device topology, such as NPN-Darlington type, bipolar types, and MOS types. We will show you what type is preferred with different applications. And then we will give a small signal analysis about low-dropout voltage linear regulator.

2.2.1 Types of Pass Device

The bipolar types of pass device shown in Fig. 18, NPN-Darlington, NPN, PNP can deliver the highest load current to output, which need larger biasing current. Due to biasing current, bipolar types of pass device are usually in high-speed operation. For the efficiency-concerned deign, low quiescent current and low dropout voltage are preferred. For low quiescent current purpose, MOS types are better than bipolar ones. For low dropout voltage, PMOS and PNP types are preferred, but PNP type needs large quiescent current due to smaller current gain. For the efficiency-priority LDO regulator, MOS types pass device are usually adopted. For PMOS type, the dropout voltage is the minimum, but the frequency

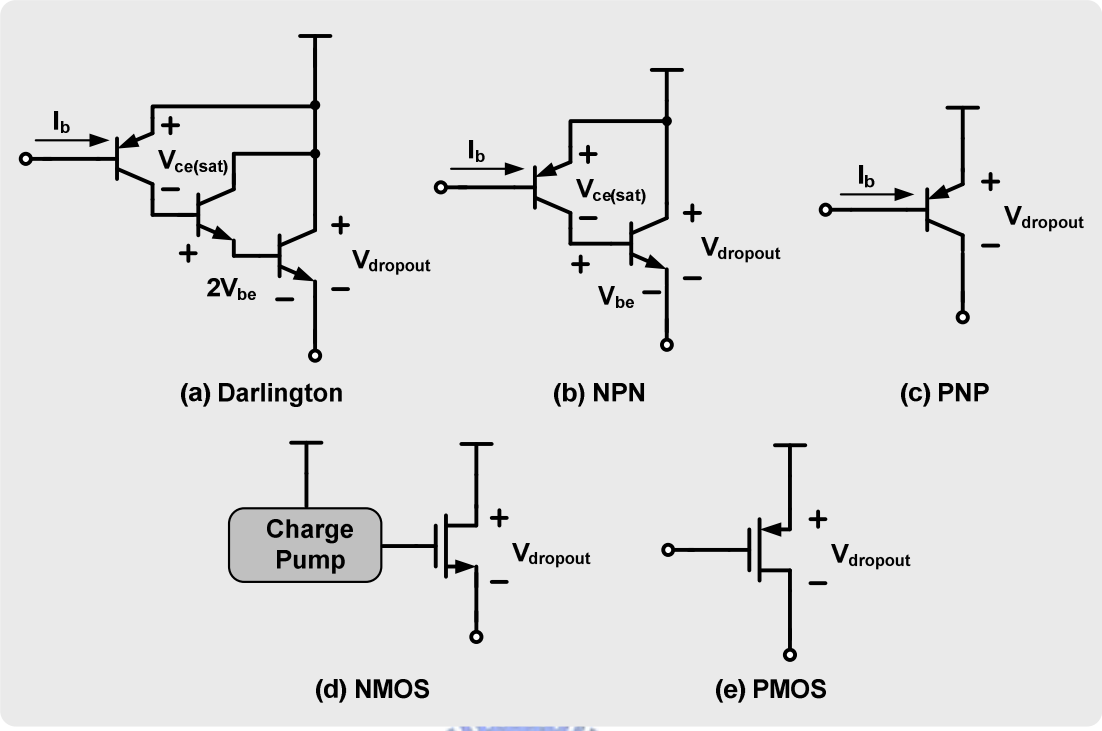


Fig. 18. Types of pass device.

response is more difficult results from large gate-to-drain capacitor C_{gd} with Miller effect. For NMOS type pass device, the most advantageous due to its low on resistance results in easier compensation and better PSR performance. If the NMOS type must be operated in low dropout, the charge pump is needed, which increases the circuit complexity. Generally speaking, we usually use PMOS type pass device to achieve LDO regulator design [7][8].

TABLE II

COMPARISONS OF DIFFERENT TYPE PASS DEVICES.

	Darlington	*NPN*	*PNP*	*NMOS*	*PMOS*
I_{out}	High	High	High	Medium	Medium
I_q	Medium	Medium	Large	Low	Low
$V_{dropout}$	$V_{ce(sat)}+2V_{be}$	$V_{ce(sat)}+V_{be}$	$V_{ce(sat)}$	$V_{gs}+V_{ds(sat)}$	$V_{ds(sat)}$
Speed	Fast	Fast	Slow	Medium	Medium
Compensation	Easy	Easy	Complex	Easy	Complex

2.2.2 Conventional LDO Regulators

As shown in Fig. 19, the conventional LDO regulator consists of a error amplifier with one dominant pole located at its output, one power PMOS pass device with gate capacitance C_{par}, and large gate-to-drain capacitor C_{gd}, a resistive feedback network R_1 and R_2, an output capacitor C_{OUT} with an equivalent serial resistor R_{ESR} for compensation, and a bypass capacitor C_b to reduce high frequency noise and help transient response [9]-[13].

Due to huge output capacitor with large output resistance of power PMOS and large gate capacitance C_{par} associated with huge output resistance of error amplifier R_{oa} to achieve high gain, the system has two low frequency poles. This system needs to be compensated. The most common compensation technique is adding an equivalent resistor to create a low frequency zero to compensate the first non-dominant pole located at power MOS gate terminal. There still exists in a higher frequency pole which associated with bypass capacitor and ESR. The overall poles and zero is shown in equation (15)-(18):

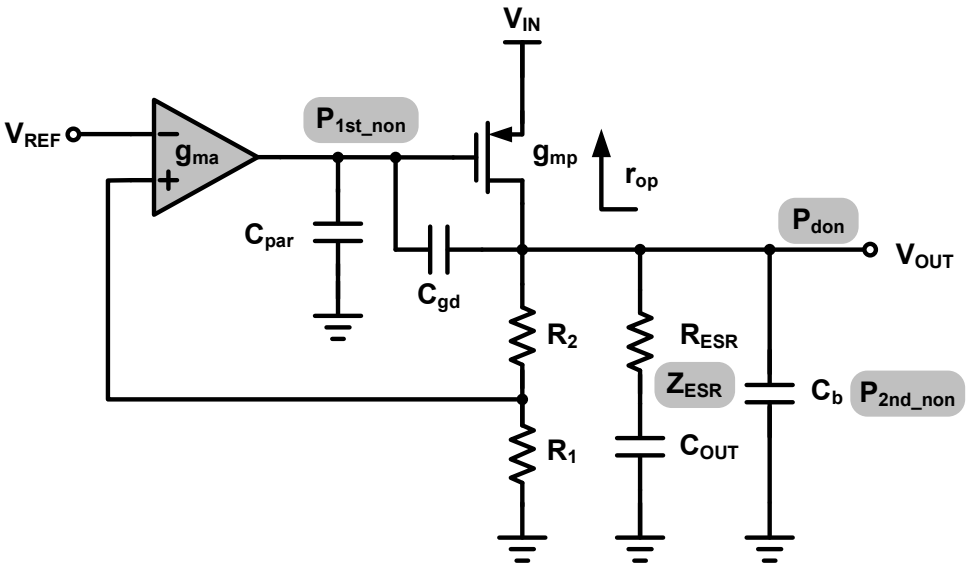


Fig. 19. Conventional LDO regulator.

$$P_{don} = \frac{1}{r_{op} C_{OUT}} \tag{15}$$

$$P_{1st\_non} = \frac{1}{R_{oa} C_{par}} \tag{16}$$

$$P_{2nd\_non} = \frac{1}{R_{ESR} C_b} \tag{17}$$

$$Z_{ESR} = \frac{1}{R_{ESR} C_{OUT}} \tag{18}$$

The ESR compensation technique exists in a stability problem resulting from non-constant unit gain frequency. As load increased, the dominant pole will move to higher frequency which is proportion to load current I_{laod} as shown in equation (19). Meanwhile, the loop gain will be decayed which is inverse proportion to radical of load current I_{laod} as shown in equation (20).

$$P_{don} = \frac{1}{r_{op} C_{OUT}} \propto \frac{1}{\frac{1}{\lambda I_{load}}} = I_{load} \tag{19}$$

$$L_o = \beta A_{oa} A_p = \beta A_{oa} g_{mp} r_{op} \propto \sqrt{I_{load}} \times \frac{1}{\lambda I_{load}} = \frac{1}{\sqrt{I_{load}}} \tag{20}$$

where r_{op} is the output resistance of power PMOS, C_{OUT} is output capacitor, is λ is the channel length modulation parameter, L_o is the open-loop gain, β is the feedback factor, A_{oa} is error amplifier gain, A_p is power PMOS gain, g_{mp} is transconductance of power PMOS.

As shown in Fig. 20, if the ESR zero was chosen to compensate the first non-dominant pole, it must be located before the magnitude decayed under 0 dB. As load current increased, the dominant pole moves to high frequency faster with loop gain decayed not in the same speed, the system may be unstable, which results from the magnitude is not decayed under 0 dB before second non-dominant occurs. With the same reason, if we compensate in heavy

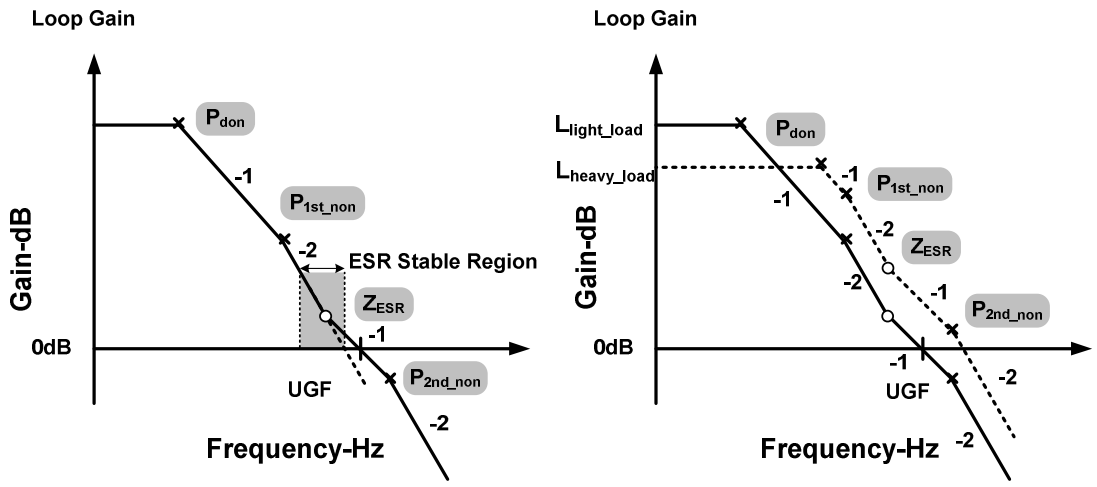


Fig. 20. Difficulty of ESR compensation.

load. The system still may be unstable in light load condition. Therefore, there is no simple rule to define ESR compensation due to variable unit gain frequency. Meanwhile, the compensation ESR will cause additional voltage drop under transient response.

2.3 Proposed LDO Regulators

Since the ESR compensation is hard to assure the stability under different load conditions and exists in unwilling voltage drop, there are many topologies have been proposed. In this section, we will show you some resolutions to ESR compensation technique.

2.3.1 Miller Compensation

In order to keep the unit gain frequency constant, Miller compensation technique is the intuitive method as show in Fig. 21. Utilizing the power PMOS gain, the Miller effect of compensation capacitor C_m will cause a dominant pole located at power PMOS gate terminal as shown in equation (21). The first non-dominant located at output can be approximate with C_m short as shown in equation (22). Due to large output capacitor, the compensation capacitor must be large resulting in the bandwidth reduction greatly and large

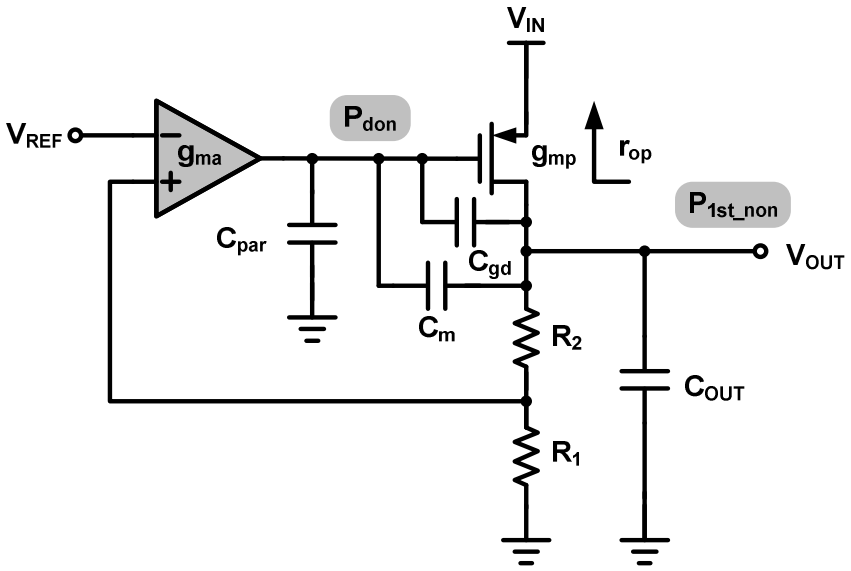


Fig. 21. Miller compensation technique for LDO regulators.

chip area. The Miller compensation capacitor connected across the power PMOS gate-to-drain will cause power supply noise directly couples to the output, and the power supply rejection will be sacrificed greatly. This kind compensation is not a good choice [14][15].

$$P_{don} = \frac{1}{g_{mp} R_{op} C_m R_{oa}} \tag{21}$$

$$P_{1st\_non} = \frac{g_{mp}}{C_{OUT}} \tag{22}$$

where g_{mp} is transconductance of power PMOS, R_{op} is the output resistance of power PMOS, C_m is compensation capacitor, C_{OUT} is output capacitor, R_{oa} is the output resistance of error amplifier.

2.3.2 Insert a Buffer Stage

The dominant pole compensation mentioned before has several drawback, such as bandwidth reduction, large compensation capacitor, and poor PSR performance. The buffer

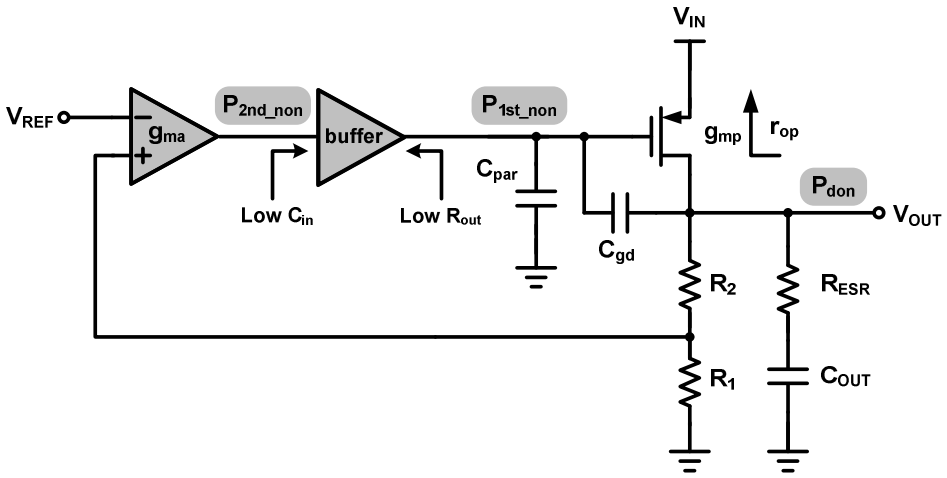


Fig. 22. Buffer stage for LDO regulator.

stage for linear regulator has been proposed. The buffer stage has characteristics of low input capacitor and low output resistance, splitting the pole at power MOS gate to two high frequency poles [16]. The overall system will be approximate a dominant pole system located at output. And the buffer stage can be a current-efficient stage which helps to enhance slewing ability at power PMOS gate. But the drawback is that the buffer stage is always formed a PMOS or NMOS common-drain stage, i.e. a level shifter, there will be at least a V_t drop to drive power MOS. Therefore, with a PMOS CD stage, the power PMOS can be fully turned on, results in a large power MOS is needed. On the other hand, with a NMOS CD stage, the power PMOS can be fully turned off, the quiescent current may be large. This is the main disadvantages of buffer stage for LDO regulator.

2.4 Multi-Stage LDO Regulators

The ESR compensation suffers from difficult compensation problem and ESR voltage drop. The dominant pole compensation sacrificed the bandwidth considerably with large compensation capacitor. The buffer stage confronts fully turn on and off problem, results in larger power MOS size or quiescent current. In recent days, the multi-stage LDO regulator

has been proposed to achieve high performance [17]-[23]. Due to multi-stage structure, the loop gain may be over one hundred decibel, causing the performance further improved such as line and load regulation, power supply rejection. Furthermore, the most attractive advantage of this kind LDO regulator is that it can be operated at capacitor-free condition with faster response resulting from a wider bandwidth. This reduced the PCB area greatly, especially for system on chip (SOC) application. But the multi-stage LDO regulator design has several unresolved problems. We will show you in this section.

2.4.1 Three-Stage LDO with Pole-Splitting

Compensation

The multi-stage LDO regulator usually consists of three-stage, one is the first high gain stage g_{m1}, g_{mcf}, and a second gain stage g_{m2}, and the power PMOS acting as third gain stage. The system at least has three poles, output of first stage, output of second stage, and output stage which C_3 modeling the parasitic capacitor of power PMOS. Under capacitor-free

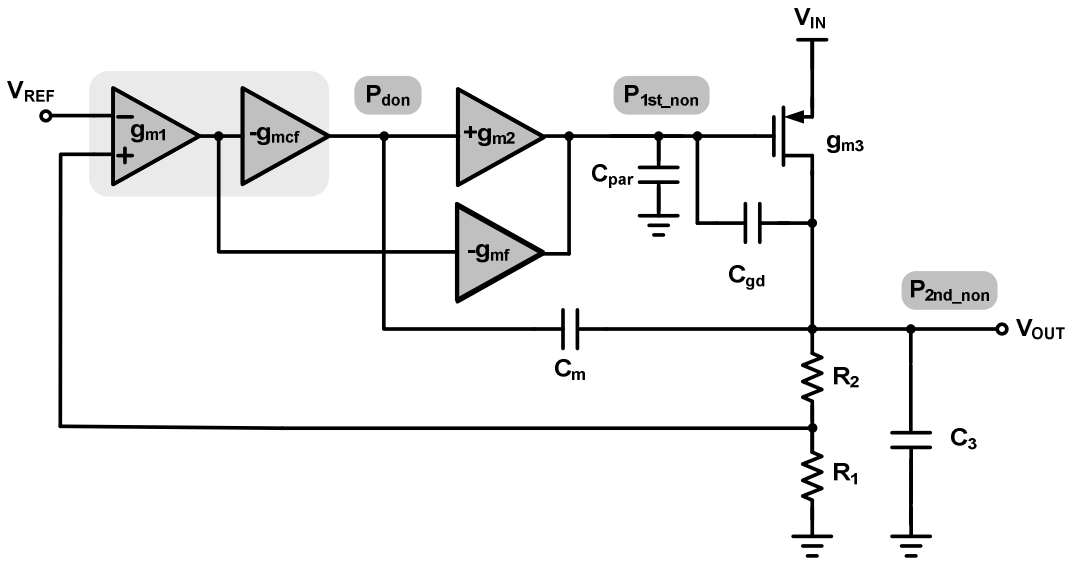


Fig. 23. Single Miller compensation for three-stage LDO regulator.

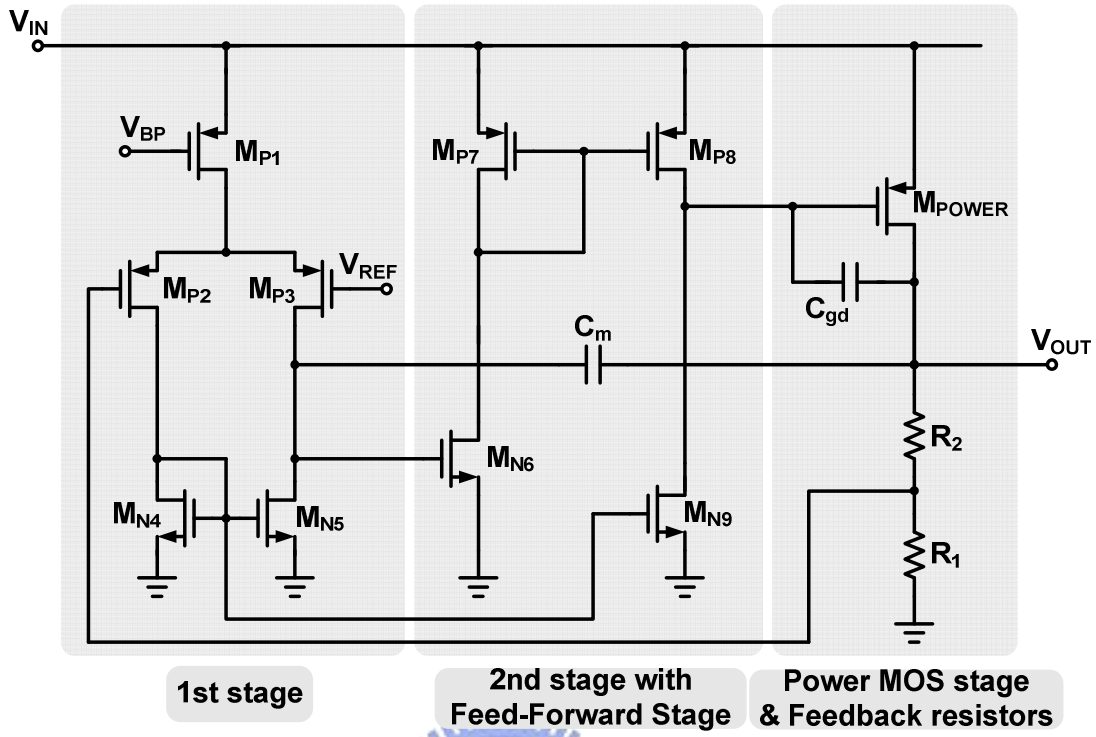


Fig. 24. Single Miller capacitor compensation for three-stage LDO regulator.

condition, the feedforward stage g_{mf} forms the push-pull stage to help the slewing at power MOS gate. And this stage will be adding a zero to help the system stability. There are many compensation techniques for three-stage amplifier design, such as nested Miller compensation, damping-factor-control compensation, and transconductance feedback compensation. But in LDO regulator design, due to large power PMOS associated with large gate-to-drain capacitor C_{gd}, about 7 pF in this paper, the various types of compensation technique may not be suited for LDO regulator design.

As shown in Fig. 23, this is the simplest three-stage LDO regulator with dominant compensation capacitor C_m. Associated with large gate-to-drain capacitor C_{gd}, this system is inherently a nested Miller compensation (NMC) structure [24][25].

The circuit level of SMC LDO regulator is shown in Fig. 24. The first stage consists of transistors M_{P1}~M_{N5}. Transistors M_{N6}~M_{P8} forms the second stage. Transistor M_{N9} is the feed-forward stage which forms push-pull stage associate with transistor M_{P8} to help transient

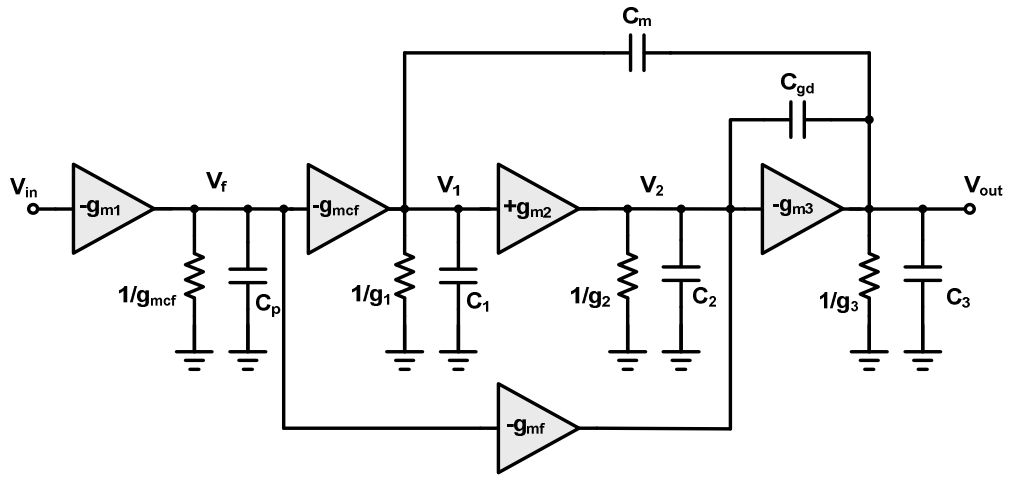


Fig. 25. Analysis structure of SMC LDO regulator.

response. The power MOS stage acts the third stage.

The analysis structure can be used Fig. 25. The g_{m1} is the transconductance of input differential pairs M_{P2} and M_{P3}, g_{mcf} is the transconductance of current mirror load M_{N5}, g_{m2} is the transconductance of M_{P8}, g_{mf} is the transconductance of M_{N9}, and g_{m3} is the transconductance of M_{POWER}. The $g_{1\text{-}2}$ and g_p are the output reactance of each stage and the C_p, $C_{1\text{-}2}$, and C_3 are the lumped parasitic capacitor of each stage. The huge gate-to-drain capacitor is represented as C_{gd}. The capacitor C_m is the compensation capacitor.

The small signal analysis is shown in Fig. 26. Using KVL and KCL theorems, the transfer function from input to output can be expressed in equation (23):

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}g_{m2}g_{m3}}{g_1g_2g_3}\frac{s^2\frac{C_mC_2}{g_{m2}g_{m3}} - s\frac{C_mg_{mf}}{g_{mcf}g_{m2}} - 1}{(1+\frac{s}{\frac{g_1g_2g_3}{C_mg_{m2}g_{m3}}})[s^2\frac{C_2C_3}{g_{m2}g_{m3}} + s\frac{(g_{m3}-g_{m2})C_mC_{gd}}{g_{m3}g_{m2}C_m} + 1]} \quad (23)$$

$$= -A_o\frac{s^2\frac{C_mC_2}{g_{m2}g_{m3}} - s\frac{C_mg_{mf}}{g_{mcf}g_{m2}} - 1}{(1+\frac{s}{p_{-3dB}})[s^2\frac{(C_{gd}+C_2)C_3}{g_{m2}g_{m3}} + s\frac{C_mC_{gd}(g_{m3}-g_{m2})}{g_{m2}g_{m3}C_m} + 1]}$$

where A_o is the DC loop gain, $P_{\text{-}3dB}$ is the dominant pole of this system.

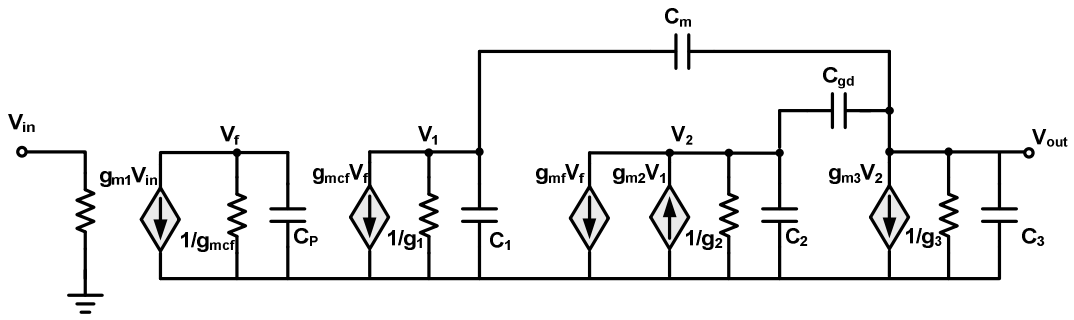


Fig. 26. Small signal analysis of SMC LDO regulator.

The system exists in three poles and one zero system can be shown in equation (24)-(27):

$$p_{-3dB} = \frac{g_1 g_2 g_3}{g_{m2} g_{m3} C_m} \tag{24}$$

$$z_1 = \frac{g_{mcf}}{C_m} \tag{25}$$

$$p_{1st-non} = \frac{g_{m2}}{C_{gd}}, \qquad p_{2nd-non} = \frac{g_{m3} C_{gd}}{C_2 C_3}, \quad heavy\ load\ condition \tag{26}$$

$$\omega_o = \sqrt{\frac{g_{m2} g_{m3}}{C_2 C_3}}, \quad Q = \sqrt{\frac{C_2 C_3}{g_{m2} g_{m3}}} \frac{g_{m2} g_{m3} C_m}{(g_{m3} - g_{m2}) C_m C_{gd}}, \quad light\ load\ condition \tag{27}$$

At heavy load, the system has one dominant pole, two separate non-dominant poles, and one zero. This zero is to compensate the first non-dominant pole under the heaviest load. As the load decreases, the first non-dominant will move to higher frequency slightly, and the second non-dominant pole will move to lower frequency, results the complex poles generation. When the load further decreases, the natural frequency will also decrease with the damping factor Q increased, which deteriorates the stability seriously. At ultra light load, the complex poles even move to right-half-plane, results in light load oscillation. The pole-zero location is show in Fig. 27.

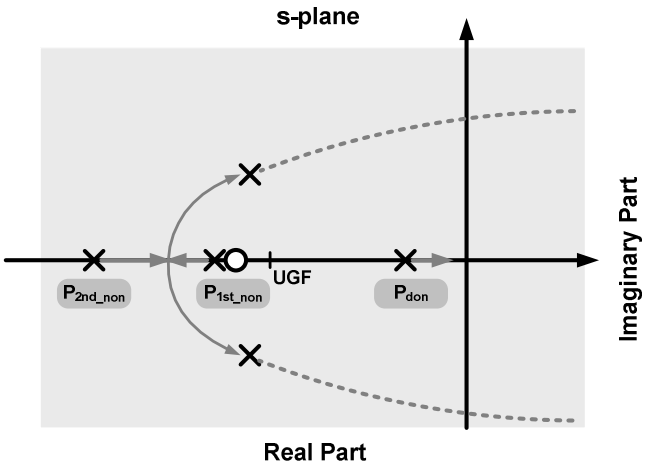


Fig. 27. Pole-zero location of SMC LDO regulator.

Just like nested Miller compensation, the single Miller compensation LDO regulator with embedded large gate-to-drain capacitor C_{gd} is a NMC structure inherently. Therefore, as the mentioned nested Miller compensation, the output transconductance g_{m3} must be much larger than the second stage's g_{m2}, which causes large power consumption. Meanwhile, for the capacitor application, the transconductance of second stage g_{m2} must be set large to improve transient response. Therefore, the minimum load current, i.e. current in the feedback resistor, must be large in the order of several mini-amps, causing low light load efficiency.

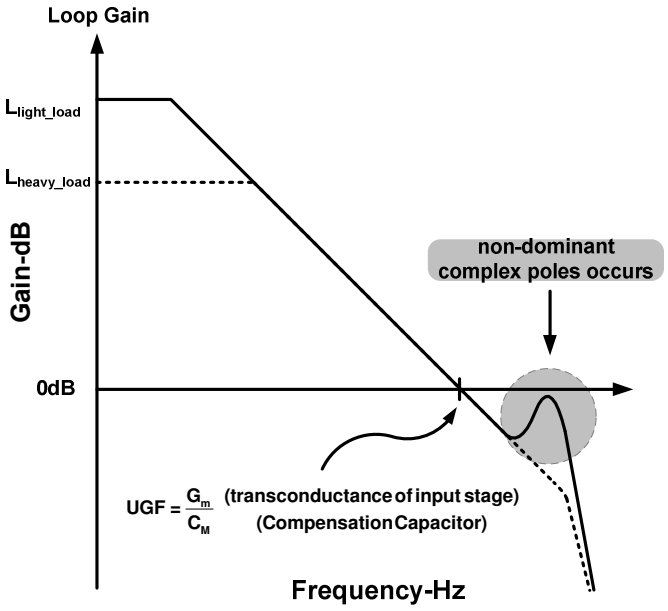


Fig. 28. Magnitude peaking at light load condition.

2.4.2 Three-stage LDO with Damping-Factor-Control Compensation

There are many compensation techniques for three-stage amplifier design [26]-[30] which have been proposed, such as active feedback compensation (AFFC), damping factor control compensation (DFC), transconductance feedback compensation (TCFC), and so on. The damping factor control is the first implement for multi-stage LDO design proposed in [17]. The damping factor block will cause a low resistance at high frequency, results in higher natural frequency and lower damping factor. The DFC block design proposed in [17], the compensation capacitor C_{m2} must be set equal to C_{m1} and the transconductance of damping factor stage g_{md} must be set four times of input transconductance g_{m1} to ensure stability, which cause large chip size and larger power consumption. The minimum load current is about 100 μA to 10 mA depending on design. This restriction comes from that the design [17] does not concerned the large gato-to-drain capacitor C_{gd} of power PMOSFET carefully.

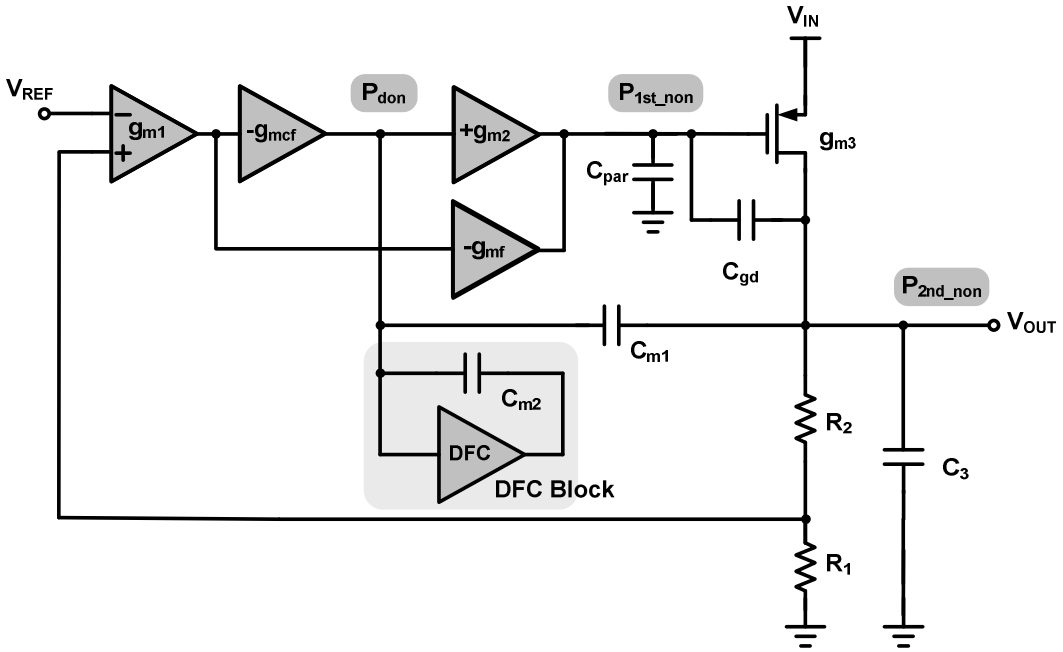


Fig. 29. LDO with Damping-Factor-Control compensation.

2.4.3 Three-stage LDO with Q-Reduction

Compensation

Although there are many compensation techniques for three-stage amplifier designs, there is no one suited for LDO regulator design, due to the NMC structure inherently. Therefore, the Q-reduction technique has been proposed in [18].

The circuit level of Q-reduction compensation LDO regulator is shown in Fig 31. The first stage consists of transistors M_{P1}~M_{N5}. Transistors M_{N6}~M_{P8} forms the second stage. Transistor M_{N9} is the feed-forward stage which forms push-pull stage associate with transistor M_{P8} to help transient response. The power MOS stage acts the third stage. The proposed Q-reduction compensation capacitor C_{cf} is connected from the g_{mcf} stage to the output of the second stage.

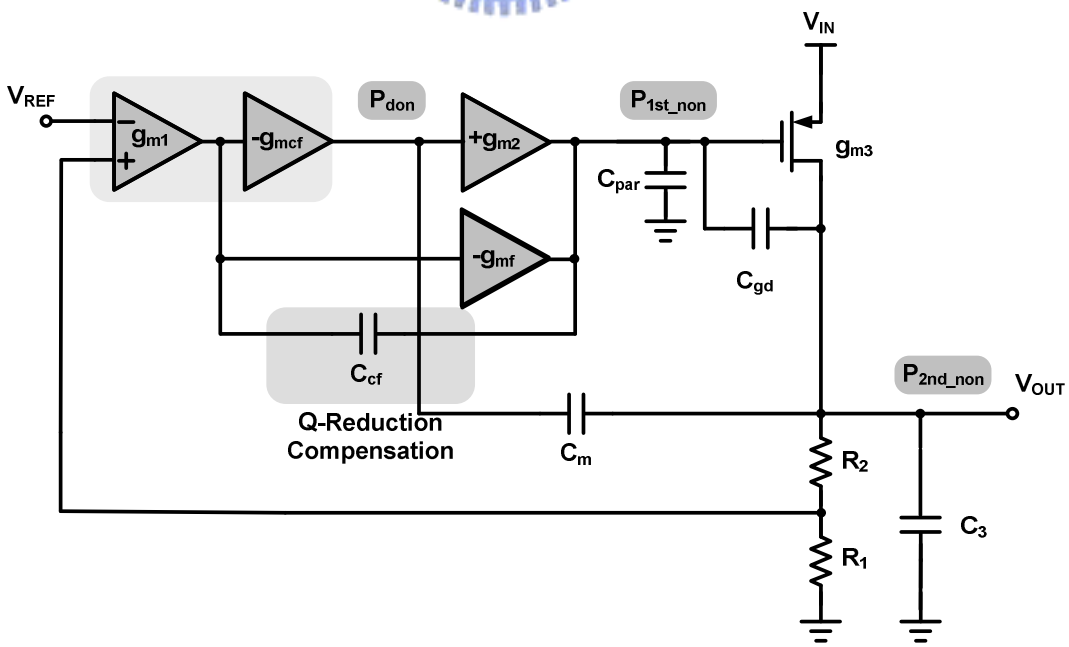


Fig. 30. LDO with of Q-reduction compensation.

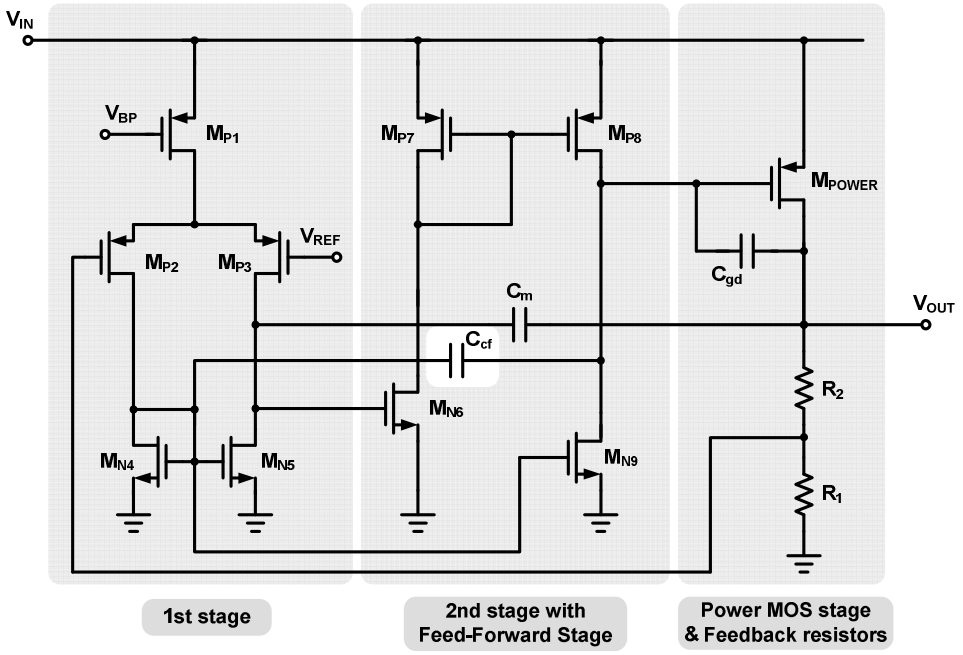


Fig. 31. Circuit level of LDO with Q-reduction compensation.

After small signal analysis, the input to output transfer function at light load can be expressed in equation (28). The natural frequency ω_o is slightly reduced by C_{cf} shown in equation (29) and the damping factor shown in equation (30) is reduce by the terms, $C_{cf}C_3g_{m2}+C_mC_{cf}g_{m2}g_{m3}/g_{mcf}$, compared to equation (27).

$$\frac{V_{out}}{V_{in}} = -A_o \frac{1+s(C_{cf}R_{cf}+\frac{g_{mf}C_m}{g_{m1}g_{m2}}-\frac{C_{gd}}{g_{m3}})-s^2[\frac{C_mC_2}{g_{m2}g_{m3}}+\frac{R_{cf}C_{gd}C_{cf}}{g_{m3}}]}{(1+s\frac{g_{m2}g_{m3}C_m}{g_1g_2g_3})\cdot[1+s\frac{(g_{m3}-g_{m2})C_mC_{gd}+g_{m2}C_{cf}C_3+g_{m2}g_{m3}R_{cf}C_mC_{cf}}{g_{m2}g_{m3}C_m}+s^2\frac{C_2C_3}{g_{m2}g_{m3}}]} \quad (28)$$

$$= -A_o \frac{1+s(C_{cf}R_{cf}+\frac{g_{mf}C_m}{g_{m1}g_{m2}}-\frac{C_{gd}}{g_{m3}})-s^2[\frac{C_mC_2}{g_{m2}g_{m3}}+\frac{R_{cf}C_{gd}C_{cf}}{g_{m3}}]}{(1+\frac{s}{p_{-3dB}})\cdot[1+s\frac{(g_{m3}-g_{m2})C_mC_{gd}+g_{m2}C_{cf}C_3+g_{m2}g_{m3}R_{cf}C_mC_{cf}}{g_{m2}g_{m3}C_m}+s^2\frac{C_2C_3}{g_{m2}g_{m3}}]}$$

$$\omega_o = \sqrt{\frac{g_{m2}g_{m3}}{C_2C_3}} \quad (29)$$

$$Q = \sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}}\frac{g_{m2}g_{m3}C_m}{(g_{m3}-g_{m2})C_mC_{gd}+g_{m2}C_{cf}C_3+\frac{1}{g_{mcf}}g_{m2}g_{m3}C_mC_{cf}} \quad (30)$$

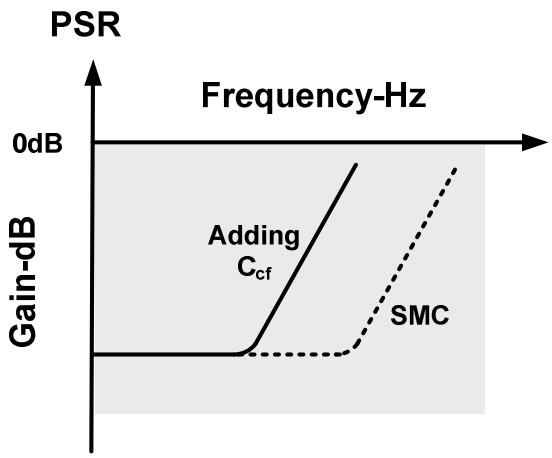


Fig. 32. PSR performance of Q-reduction compensation.

The most important drawback of Q-Reduction compensation is that the compensation capacitor connected form the power MOS gate to the ground reference, degenerates the auto-cancellation at the gate and source of power PMOS. This will result in the mid-frequency PSR deterioration as shown in Fig. 32.

2.4.4 Equivalent Two-Stage LDO Design

Unlike conventional dominant compensation of LDO regulator, the equivalent two-stage LDO regulator has been proposed in [31]. This structure consists of two stage M_{P6}~M_{P10} with high frequency poles, so the system can be approximate as a two poles system located at output of first stage and output as shown in equation (31)(32). The compensation capacitor C_m can be connected from ground reference to the output instead, and the power supply rejection performance will not be degenerated.

$$p_{-3dB} = \frac{1}{R_{o1} g_{m2}'' R_{op} C_m} \tag{31}$$

$$p_{1st-non} = \frac{g_{m2}''}{C_L} \tag{32}$$

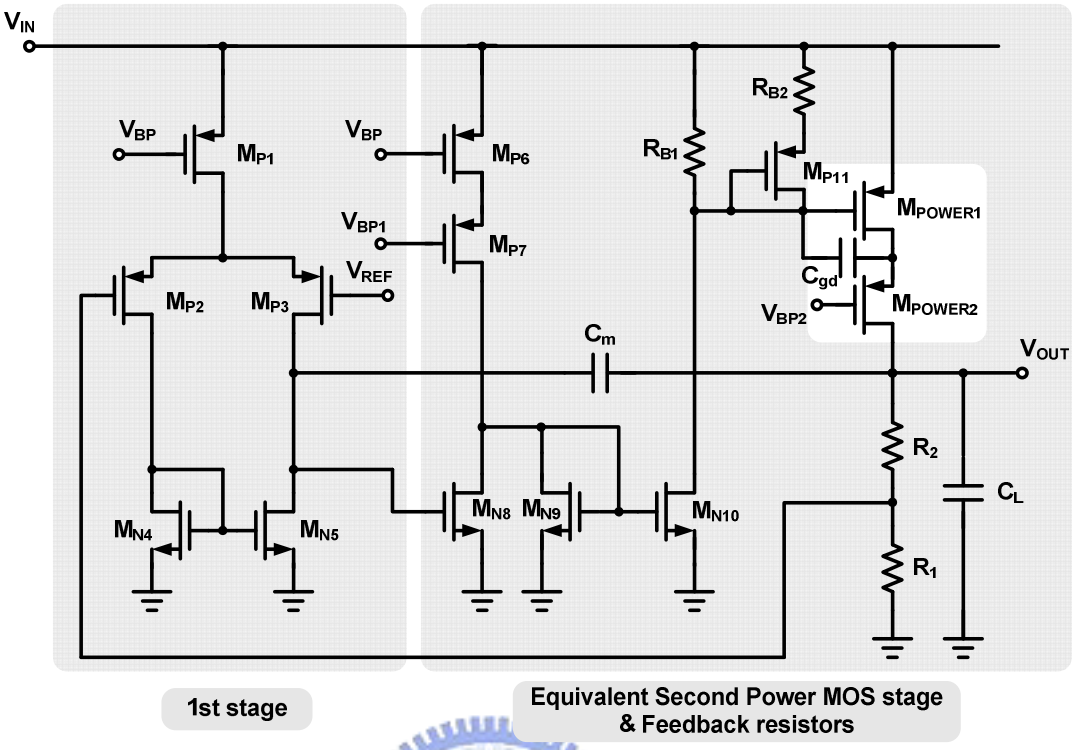


Fig. 33. Equivalent two-stage LDO regulator.

where R_{o1}, R_{op} are the output resistance of first and output stage, g_{m2}" is the equivalent transconductance of second stage, C_m, C_L are the compensation and load capacitor.

The above assumption is held under the second non-dominant pole at power MOS gate will not affect the system. This structure utilize resistive load R_{B1} to cause higher frequency second non-dominant, and the PSR performance is improved. When the load increases, the output pole will move to higher frequency. The switch M_{P11} will be turned on, the second non-dominant pole will also move to higher frequency preventing from complex poles generation to ensure the system stability. At the same time, the power MOS stage using cascade topology, M_{POWER1} and M_{POWER2}, minimize the Miller effect of gate-to-drain capacitor C_{gd} of M_{POWER1}, i.e. the gain of power MOS M_{POWER1} equals to one. This topology will increase twice chip size.

Chapter 3

Current Feedback Compensation for Capacitor-Free LDO Regulators

From the discussion in Chapter 2, the ESR compensation is hardly to ensure the stability under different load condition, which results from non-constant unit gain frequency. And the ESR will cause unwilling voltage dip during transient period. Then the compensation techniques without ESR are developed, such as Miller compensation and inserting a buffer stage. The Miller compensation technique needs large compensation capacitor and the bandwidth is reduced greatly. The buffer stage compensation has fully turned on and off problems. For now days, the high performance LDO regulator has be proposed, i.e. high load regulation and high power supply rejection. The multi-stage LDO design can achieve this target. But the three-stage LDO regulator with Miller compensation inherently forms a nested Miller compensation topology, causes a minimum load restriction. Therefore, the DFC compensation method proposed in [17]. But the NMC embedded structure degenerates the DFC block effects. And the Q-reduction method has been proposed in [18], the minimum load can be down to 100 μA. But this kind compensation deteriorates the PSR performance seriously. In this Chapter, we will propose a new frequency compensation technique, current feedback compensation for three-stage LDO regulator, which can be operated in ultra light load operation and with high power supply rejection and faster transient response.

3.1 Three-Stage LDO Regulator with Resistive Load at Second Stage

In the chapter 2.4.4, the equivalent two-stage LDO has been proposed. If there is no cascode power PMOS topology under capacitor-free condition, the system will be consist of one dominant pole and a pair of complex poles. The generation of complex poles will result in the minimum load restriction, but the smaller output resistance of the second stage by using resistive load will alleviate this effect and increase the power supply rejection performance by the same fluctuation at power PMOS gate and drain terminal.

The circuit level of three-stage LDO is shown in Fig. 34. The first stage consists of transistors M_{P1}~M_{N5}. The second stage consists of transistors M_{N6}~M_{P10} with resistive load R_B. The power PMOS stage acts the third stage.

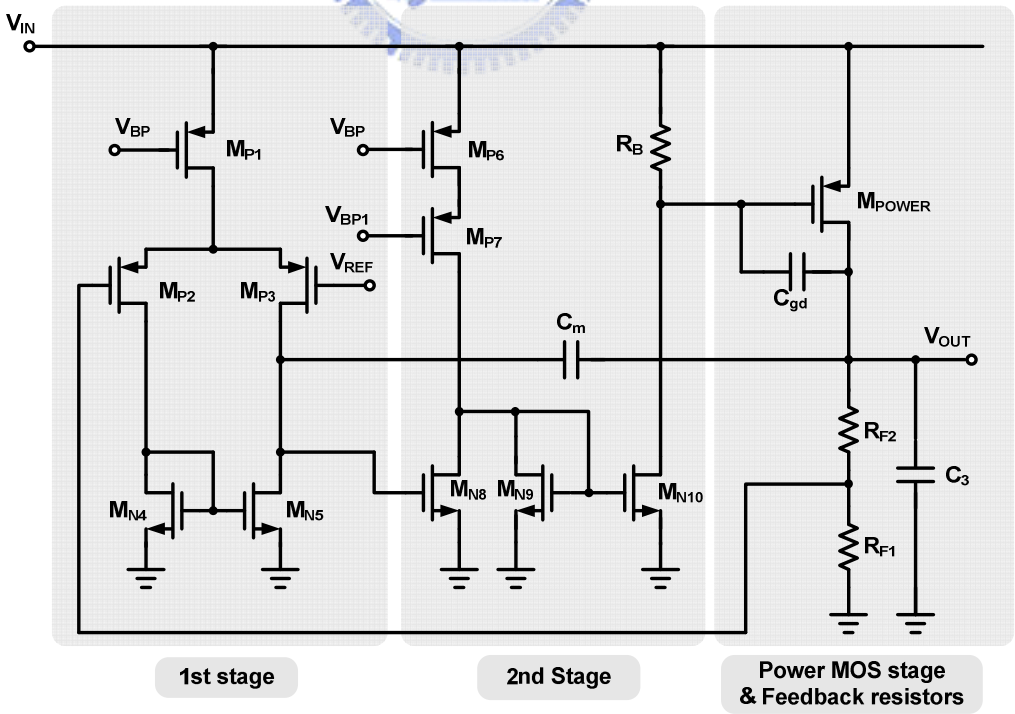


Fig. 34. Three-stage LDO with resistive load at second stage.

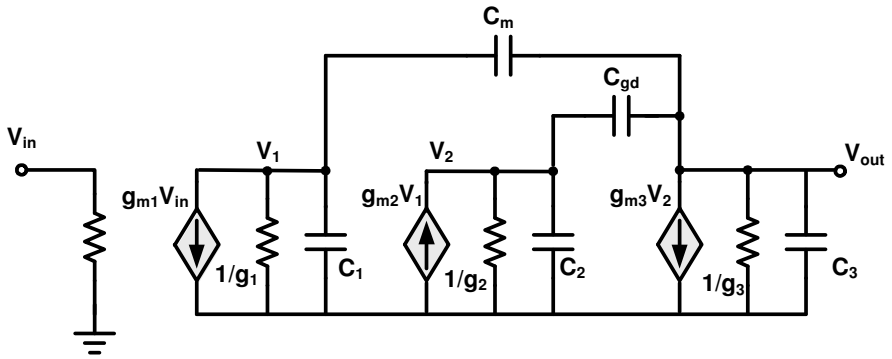


Fig. 35. Small signal of three-stage LDO with resistive load at second stage.

The analysis structure can be used Fig. 35. The g_{m1} is the transconductance of input differential pairs M_{P2} and M_{P3}, g_{m2} is the equivalent transconductance of M_{P8} ~M_{P10}, and g_{m3} is the transconductance of M_{POWER}. The $g_{1,}$ $g_{2,}$ g_3 are the output reactance of each stage and the $C_{1\text{-}3}$ are the lumped parasitic capacitor of each stage. The huge gate-to-drain capacitor is represented as C_{gd}. The capacitor C_m is the compensation capacitor.

Using KVL and KCL theorems, the transfer function from input to output can be expressed in equation (33):

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}g_{m2}g_{m3}}{g_1g_2g_3}\frac{s^2\frac{C_mC_2}{g_{m2}g_{m3}}+s\frac{C_{gd}}{g_{m3}}-1}{s^3\frac{C_mC_2C_3}{g_1g_2g_3}+s^2\frac{g_2C_mC_3+(g_{m3}-g_{m2})C_mC_{gd}}{g_1g_2g_3}+s\frac{g_{m2}g_{m3}C_m}{g_1g_2g_3}+1}$$
$$= -A_o\frac{s^2\frac{C_mC_2}{g_{m2}g_{m3}}+s\frac{C_{gd}}{g_{m3}}-1}{(1+\frac{s}{p_{-3db}})[s^2\frac{C_2C_3}{g_{m2}g_{m3}}+s\frac{g_2C_mC_3+(g_{m3}-g_{m2})C_mC_{gd}}{g_{m2}g_{m3}C_m}+1]} \quad (33)$$

where A_o is the DC loop gain, $P_{\text{-}3dB}$ is the dominant pole of this system.

The system is a three poles and two zeros system. One lower frequency zero is located in right-half-plane (RHP), and the other higher frequency zero is located in left-half-plane (LHP). But these two zeros are located at high frequency compared to unit gain frequency, so the zeros effects can be neglected. Pole locations under different load conditions can be shown in

equation (34)-(36):

$$p_{-3dB} = \frac{g_1 g_2 g_3}{g_{m2} g_{m3} C_m} \tag{34}$$

$$p_{1st-non} = \frac{g_{m2}}{C_{gd}}, \quad p_{2nd-non} = \frac{g_{m3} C_{gd}}{C_2 C_3} \qquad ,heavy\ load\ condition \tag{35}$$

$$\omega_o = \sqrt{\frac{g_{m2} g_{m3}}{C_2 C_3}} \ ,$$
$$Q = \sqrt{\frac{C_2 C_3}{g_{m2} g_{m3}}} \frac{g_{m2} g_{m3} C_m}{g_2 C_m C_3 + (g_{m3} - g_{m2}) C_m C_{gd}} \qquad ,light\ load\ condition \tag{36}$$

Compared the equation (36) with (27), the quality factor of three-stage LDO regulator with resistive load at second stage can be reduced by a factor of $g_2 C_m C_3$ compared with conventional SMC LDO design. But this reduction is not enough for low power design. In the next section, we propose a new technique to further reduce the quality factor.

3.2 Current Feedback Compensation (CFC) for Three-Stage LDO Regulator

For three-stage LDO design, there are two closed poles under light condition. One is located at the output of second stage which time constant is associated with the output resistance of second stage and large gate-to-drain capacitor multiplied by Miller effect. And the other is located at LDO output stage which time constant is associated with the larger output resistance of power MOS and large lump capacitor. So these nearby two poles will form the complex pair, and deteriorate the light load stability.

In order to reduce the Q-factor of complex poles, the most common method is to push the output pole or the output pole of second stage to a higher frequency. In three-stage LDO

using damping factor control [17], it puts the output pole to higher frequency. In that design, the minimum load is about 1mA by using a DFC compensation capacitor the same as miller capacitor about several pico-Farad. So this is not an effective method. Then in LDO with Q-reduction technique [18], it only uses a compensation capacitor 1pF to push the second stage output pole to higher frequency and the minimum load can be down to 100uA. But this capacitor is connected form a ground reference to a noisy reference, the PSR performance is great discounted.

So we proposed a new technique to break the minimum load restriction without sacrificing PSR performance. By push the output pole to higher frequency, the capacitor C_a connected between two ground reference V_f and V_1 as shown in Fig. 36. The resistor R_z is used to compensate first non-dominant pole under heavy load condition.

3.2.1 CFC Capacitor-Free LDO Regulators

For the proposed capacitor-free LDO regulator, the analysis structure is shown in Fig. 36. The g_{m1-3} is the equivalent transconductance of each stage. The g_1, g_2, g_3 are the equivalent output reactance of each stage and the C_{1-2}, and C_3 are the lumped parasitic capacitor of each stage. The huge gate-to-drain capacitor is represented as C_{gd}. The capacitors C_m and C_a are the compensation capacitors.

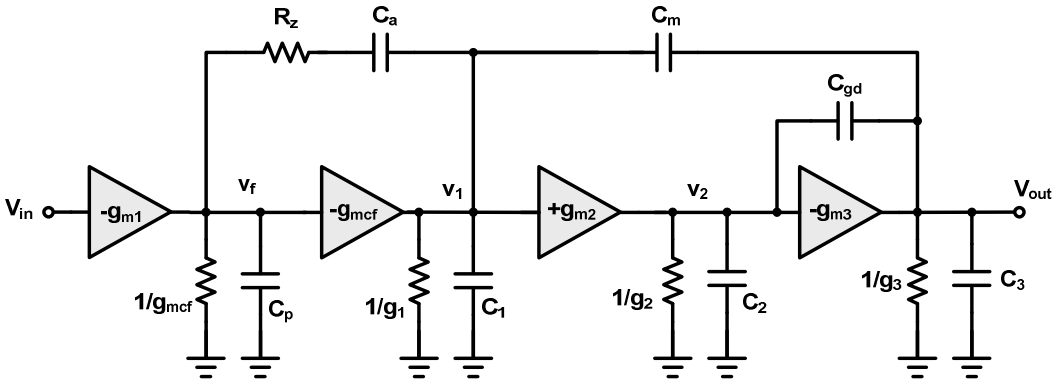


Fig. 36. Structure of CFC capacitor-free LDO regulator.

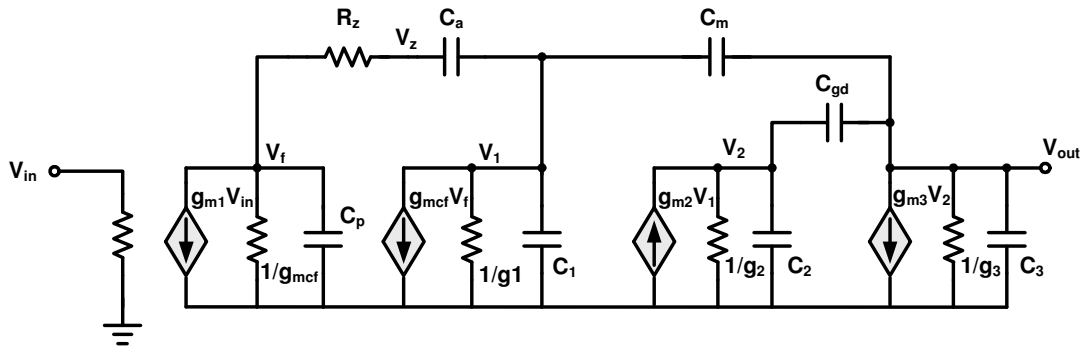


Fig. 37. Small signal analysis of CFC capacitor-free LDO regulator.

Using KVL and KCL theorems, the transfer function from input to output can be expressed in equation (37):

$$\frac{V_{out}}{V_{in}} = -A_o \frac{(sC_aR_z+1)(s^2\frac{C_mC_2}{g_{m2}g_{m3}} + s\frac{g_{m2}C_{gd}}{g_{m2}g_{m3}} - 1)}{(1+\frac{s}{\omega_{-3dB}})(1+\frac{s}{\omega_{1st-non}})} \cdot \frac{1}{(s^2\frac{C_2C_3}{g_{m2}g_{m3}} + s\frac{(\frac{1}{g_{mcf}}+R_z)(g_2C_3+g_3C_2+(g_{m3}-g_{m2})C_{gd})C_aC_m + (C_m+2C_a)C_2C_3}{(g_2C_3+g_3C_2+(g_{m3}-g_{m2})C_{gd})(C_m+2C_a)+2g_{m2}C_{gd}C_a+(\frac{1}{g_{mcf}}+R_z)g_{m2}g_{m3}C_aC_m} + 1)} \quad (37)$$

where A_o is the DC loop gain, P_{-3dB} is the dominant pole of this system.

The system is a four poles and three zeros system. Two zeros come from the second order polynomial which one lower frequency zero is located in right-half-plane (RHP), and the other higher frequency zero is located in left-half-plane (LHP). But these three zeros are located at high frequency compared to unit gain frequency, so the zeros effects can be neglected. The other zero comes from first order polynomial which is associated with capacitor C_a and resistor R_z. The dominant pole is decided by Miller compensation capacitor associated with the output resistance of first stage as shown in equation (38). The first non-dominant pole is located near the unit gain frequency not only to reduce the magnitude before the complex poles generation but also to maintain the system with proper phase margin about 60° for faster transient response. The two poles coming from the second order

polynomial in the denominator of equation (37) under different load conditions are shown in equation (41)(42) separately.

$$p_{-3dB} = \frac{g_1 g_2 g_3}{g_{m2} g_{m3} C_m} \propto \frac{1}{\sqrt{I_{Load}} \times \frac{1}{I_{Load}}} = \sqrt{I_{Load}} \tag{38}$$

$$p_{1st-non} = \frac{g_{m2} g_{m3} C_m}{(\frac{1}{g_{mcf}} + R_z) g_{m2} g_{m3} C_a C_m + (g_3 C_2 + g_{m3} C_{gd})(C_m + 2C_a)} \propto \frac{1}{k_1 + k_2 \sqrt{I_{Load}}} \tag{39}$$

where $k_1 = C_a(\frac{1}{g_{mcf}} + R_z)$, $k_2 = \frac{C_2(C_m + 2C_a)}{g_{m2} C_m}$

$$z_{LHP} = \frac{1}{C_a R_z} \tag{40}$$

$$p_{2nd-non} = \frac{g_{m2}}{C_{gd}}, \qquad p_{3rd-non} = \frac{g_{m3} C_{gd}}{C_2 C_3}, \text{heavy load condition} \tag{41}$$

$$\omega_o = \sqrt{\frac{g_{m2} g_{m3}}{C_2 C_3}} ,$$

$$Q = \sqrt{\frac{C_2 C_3}{g_{m2} g_{m3}}} \frac{(g_2 C_3 + g_3 C_2 + (g_{m3} - g_{m2}) C_{gd})(C_m + 2C_a) + 2 g_{m2} C_{gd} C_a + (\frac{1}{g_{mcf}} + R_z) g_{m2} g_{m3} C_a C_m}{(\frac{1}{g_{mcf}} + R_z)(g_2 C_3 + g_3 C_2 + (g_{m3} - g_{m2}) C_{gd}) C_a C_m + (C_m + 2C_a) C_2 C_3} \tag{42}$$

, *light load condition*

As load increases, the dominant pole will move to the higher frequency which is proportional to square of load as shown in equation (38). And the first non-dominant pole will move to lower frequency due to the equation (39). The slight lower frequency of the first non-dominant pole will decrease the stability at heavy load about ten degrees among one hundred mini-amp rated. The large resistor R_z will create a LHP zero associated with capacitor C_a to help the stability at heavy load. So the dynamic zero compensation is required. The complex poles will be separated into two poles as load increased. The poles and zero location as load increased are shown in Fig. 38.

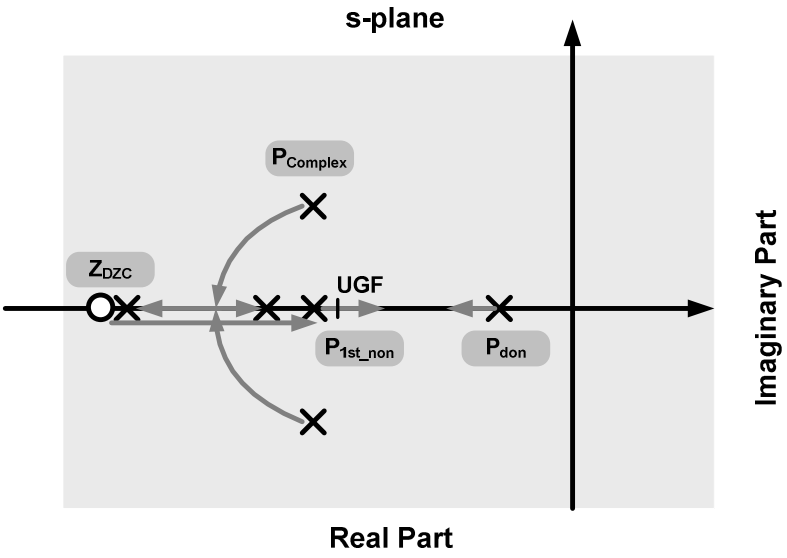


Fig. 38. Poles and zero locations of CFC LDO as load increased.

Compared with proposed compensation technique and without proposed compensation technique, the complex poles have been in right-half-plane (RHP) without proposed compensation technique causing the system unstable. With proposed compensation technique, the complex pole will be converted into left-half-plane (LHP) with low quality factor. Therefore, the system is still stable even with ultra light load.

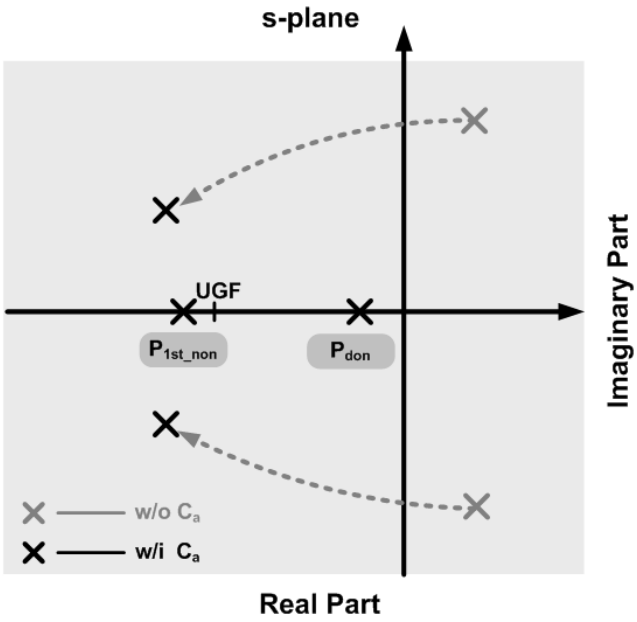


Fig. 39. Pole locations with CFC technique.

3.2.1.1 CFC Capacitor-Free LDO under Ultra Light Load

Condition with Smaller R_z

As well known, the complex poles will be generated under light load condition in three-stage LDO design which results from the inherently nested Miller compensation structure. These complex poles will degenerate the light load stability, so it will suffer the minimum load limitation which is not suitable for low power design. The proposed compensation technique pushes the output pole to higher frequency by reducing the equivalent resistance at higher frequency. As shown in equation (43), the quality factor is further reduced by a term, $C_2C_3(C_m+2C_a)/((1/g_{mcf})+R_z)$, compared to that without this technique as shown in equation (36).

$$Q = \sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}} \frac{g_{m2}g_{m3}C_aC_m}{g_2C_aC_mC_3 + (g_{m3}-g_{m2})C_aC_mC_{gd} + \frac{C_2C_3(C_m+2C_a)}{(\frac{1}{g_{mcf}}+R_z)}} \qquad (43)$$

The quality factor Q is reduced greatly because the term, $C_2C_3(C_m+2C_a)/((1/g_{mcf})+R_z)$, which is usually larger than the term , $g_2C_aC_mC_3$, one order more. The compensation resistor R_z must be small, since it will increase the equivalent resistance of output node at higher frequency, i.e. a resistor R_z in series with $1/g_{mcf}$. This will increase the quality factor, so the resistor R_z must be set to a small value under ultra light load condition. This compensation network decreases not only the quality factor but also the magnitude of loop gain behind the unit gain frequency by adding an additional pole located unit gain frequency nearby. So it can achieve further light load operation without using too large additional compensation capacitor. The frequency responses with and without proposed compensation network are shown in Fig. 40.

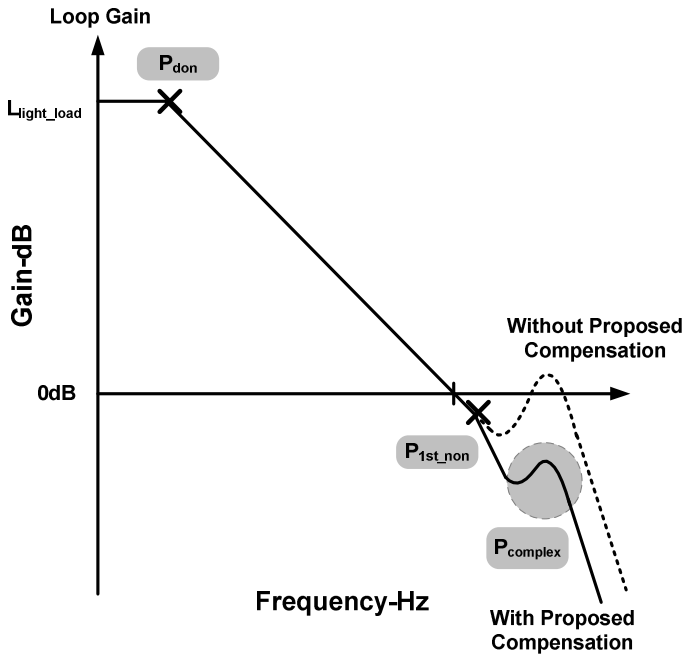


Fig. 40. CFC capacitor-free LDO under light load condition.

The pole locations with small resistor R_z are shown in equation (44)-(46):

$$p_{-3dB} = \frac{g_1 g_2 g_3}{C_m g_{m2} g_{m3}} \tag{44}$$

$$p_{1st-non} = \frac{g_{mcf}}{C_a} \tag{45}$$

$$\omega_o = \sqrt{\frac{g_{m2} g_{m3}}{C_2 C_3}} \quad ,$$

$$Q = \sqrt{\frac{C_2 C_3}{g_{m2} g_{m3}}} \frac{\frac{1}{g_{mcf}} g_{m2} g_{m3} C_a C_m}{(C_m + 2C_a) C_2 C_3} = \sqrt{\frac{C_2 C_3}{g_{m2} g_{m3}}} \frac{\frac{1}{g_{mcf}} g_{m2} g_{m3} C_m}{(\frac{C_m}{C_a} + 2) C_2 C_3} \tag{46}$$

The quality factor Q will be slightly increased as capacitor C_a is increased as shown in equation (46). But this effect is not important since the value of quality factor is relative low. The frequency response simulated by MATLAB as C_a increased is shown in Fig. 41.

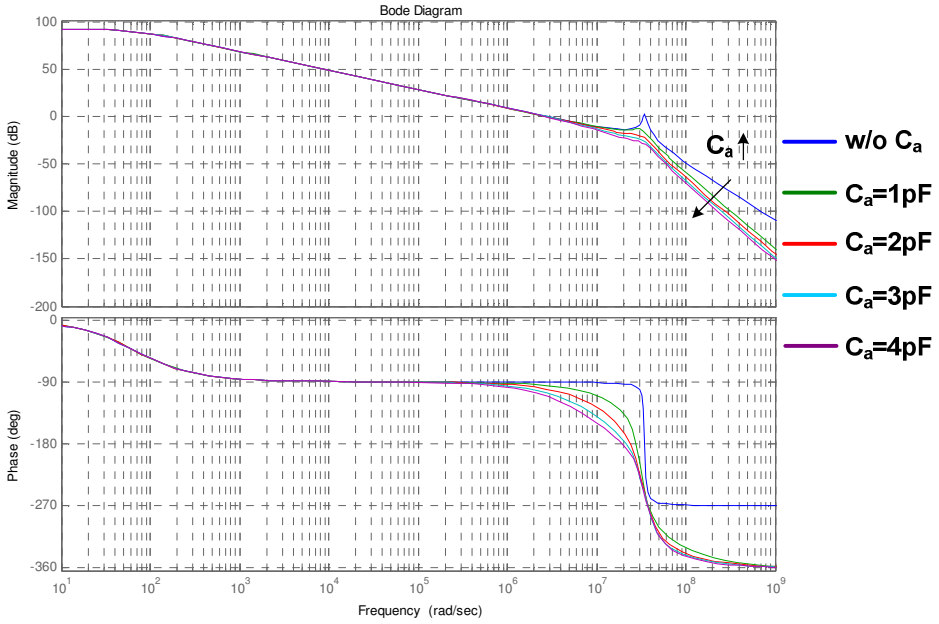


Fig. 41. Frequency response of CFC LDO simulated by MATLAB.

In order to maintain the phase margin about 60°, the first non-dominant pole must be placed above unit gain frequency by a factor of two by using separate poles approach under low Q approximation ~5 as shown in equation (47).

$$p_{1st-non} = 2 \cdot UGF = 2\frac{g_{m1}}{C_m} \tag{47}$$

In order to avoid the complex poles causing unstable, the first non-dominant pole must be set half of nature frequency at least as shown in equation (48). Since the magnitude rolls off with -20dB/dec after unit gain frequency and -40dB/dec after first non-dominant pole, there is at least 18dB margin for the complex poles with low Q approximation.

$$p_{1st-non} = \frac{1}{2}\omega_o \tag{48}$$

The zeros are located at relative high frequency compared to unit gain frequency. The overall system stability can be determined by equation (49):

$$PM = 180^\circ - \tan^{-1}(\frac{UGF}{p_{don}}) - \tan^{-1}(\frac{UGF}{p_{1st-non}}) - \tan^{-1}(\frac{\frac{UGF}{\omega_o}}{Q[1-(\frac{UGF}{\omega_o})^2]})$$

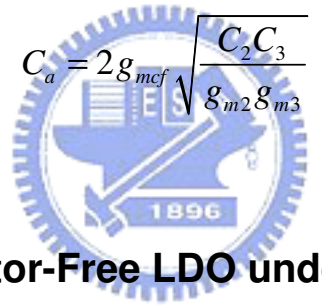
$$= 90^\circ - \tan^{-1}(\frac{UGF}{p_{1st-non}}) - \tan^{-1}(\frac{\frac{UGF}{\omega_o}}{Q[1-(\frac{UGF}{\omega_o})^2]}) \quad (49)$$

$$= 90^\circ - 26.56^\circ - 2^\circ \approx 60^\circ$$

By using equation (45)-(47) with separated pole approach, the compensation capacitors C_m and C_a can be obtained as shown in equation (50)(51).

$$C_m = 2\frac{g_{m1}}{g_{mcf}}C_a = 4g_{m1}\sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}} \quad (50)$$

$$C_a = 2g_{mcf}\sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}} \quad (51)$$



3.2.1.2 CFC Capacitor-Free LDO under Light to Medium

Load Condition

As load is increased in light to medium condition about 1mA to 10mA, the first non-dominant pole will slightly move to lower frequency due to R_z slightly increased by dynamic zero compensation. The complex poles will move to high frequency and contribute no phase shift to the system. The poles locations are shown in equation (52)(53).

$$p_{1st-non} = \frac{1}{(\frac{1}{g_{mcf}} + R_z)C_a} \quad (52)$$

$$\omega_o = \sqrt{\frac{g_{m2}g_{m3}}{C_2C_3}} \quad ,$$
$$Q = \sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}}\frac{g_{m2}}{C_{gd}} \tag{53}$$

The overall system stability can be determined by dominant pole and first non-dominant pole as shown in equation (54):

$$\begin{aligned} PM &= 180^\circ - \tan^{-1}(\frac{UGF}{p_{don}}) - \tan^{-1}(\frac{UGF}{p_{1st-non}}) \\ &= 90^\circ - \tan^{-1}(\frac{UGF}{p_{1st-non}}) \\ &\approx 60^\circ \end{aligned} \tag{54}$$

3.2.1.3 CFC Capacitor-Free LDO under Heavy Load

Condition with Larger R_z

As load is further increased about 10mA to 100mA, the first non-dominant pole as shown in equation (55) will move to lower frequency due to output reactance g_3 increased and R_z slightly increased. The low frequency zero z_{DZC} as shown in equation (56) will compensate this effect.

$$p_{1st-non} = \frac{g_{m2}g_{m3}C_m}{(\frac{1}{g_{mcf}} + R_z)g_{m2}g_{m3}C_aC_m + g_3C_2(C_m + 2C_a)} \tag{55}$$

$$z_{DZC} = \frac{1}{R_zC_a} \tag{56}$$

The second order polynomial in the equation (37) can be simplified to equation (57) at heavy load condition. As the discriminant of the second-order polynomial in (57) is smaller than zero, a pair of complex poles still exists in the system. But these complex poles located

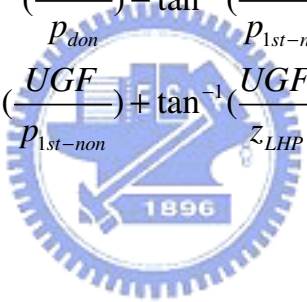
high frequency produces no effects to the system. As the discriminant of the second-order polynomial in (57) is large than zero, there are two separated poles in the system. Finally, if the second non-dominant pole exists, the poles locations are shown in equation (58). These two poles located at high frequency, so the effects can be neglected.

$$s^2 \frac{C_2 C_3}{g_{m2} g_{m3}} + s \frac{g_3 C_2 + g_{m3} C_{gd}}{g_{m2} g_{m3}} + 1 \tag{57}$$

$$p_{2nd-non} = \frac{g_{m2} g_{m3}}{g_3 C_2 + g_{m3} C_{gd}}, \qquad p_{3rd-non} = \frac{g_3 C_2 + g_{m3} C_{gd}}{C_2 C_3} \tag{58}$$

The overall system is a two lower poles and one lower zero system. The system stability can be decided by equation (59):

$$\begin{aligned} PM &= 180^\circ - \tan^{-1}\left(\frac{UGF}{p_{don}}\right) - \tan^{-1}\left(\frac{UGF}{p_{1st-non}}\right) + \tan^{-1}\left(\frac{UGF}{z_{LHP}}\right) \\ &= 90^\circ - \tan^{-1}\left(\frac{UGF}{p_{1st-non}}\right) + \tan^{-1}\left(\frac{UGF}{z_{LHP}}\right) \\ &\approx 60^\circ \end{aligned} \tag{59}$$



3.2.1.4 Summary of CFC Capacitor-Free LDO Regulators

The frequency response of CFC capacitor-free LDO under different load conditions is summarized in Fig. 42. In ultra light load condition, smaller than 1 mA, the dominant pole contributes ninety degree phase shift. The first non-dominant pole contributes near thirty degree phase shift, and the complex poles contributes smaller phase shift. So the overall system stability can be maintained about sixty degree. In light to medium load condition, about 1 mA to 10mA, the dominant pole contributes the same phase shift. The first non-dominant pole is moved to lower frequency and contributes thirty degree phase shift. The complex poles are located at higher frequency and contribute no phase shift. So the system stability is still maintained at sixty degree. Finally, in medium to heavy load condition, about

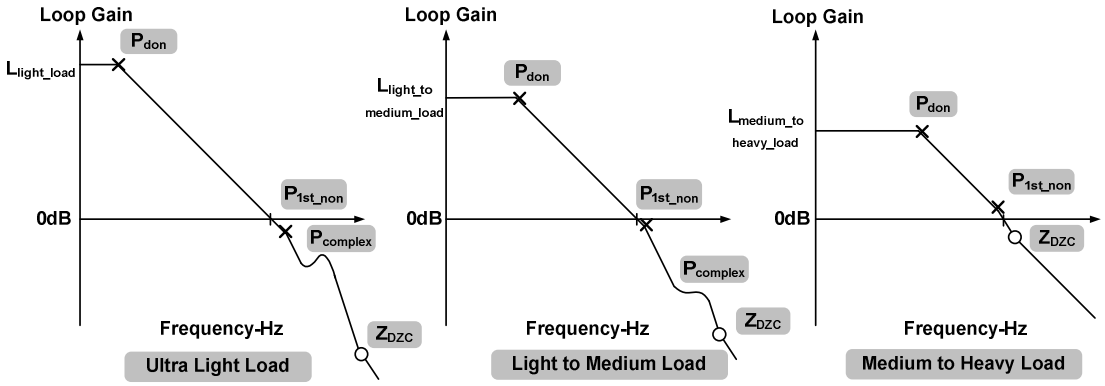


Fig. 42. Summarized poles and zero of CFC capacitor-Free LDO Regulators.

10 mA to 100mA, the dominant pole contributes the same phase shift. But the fist non-dominant pole is moved to further low frequency, the dynamic zero is moved to lower frequency to compensate it. Therefore, the phase margin of CFC capacitor-free LDO regulator can be maintained at sixty degree in the entire load range.

3.2.2 CFC LDO with an Off-Chip Capacitor

If the system needs an off-chip capacitor to have better transient response, the system will have two low frequency poles. One is the Miller compensation dominant pole, and the other is output pole. Therefore, the ESR must be needed to add a zero to help the overall stability.

The analysis structure can be used Fig. 43. The $g_{m1,2,p}$ is the equivalent transconductance of each stage. The g_{o1}, g_{o2}, g_{op} are the output reactance of each stage and the $C_{1\text{-}3}$ are the lumped parasitic capacitor of each stage. The huge gate-to-drain capacitor is represented as C_{gd}. The capacitor C_m is the compensation capacitor. C_{OUT} is the off-chip capacitor and R_{ESR} is the compensation ESR.

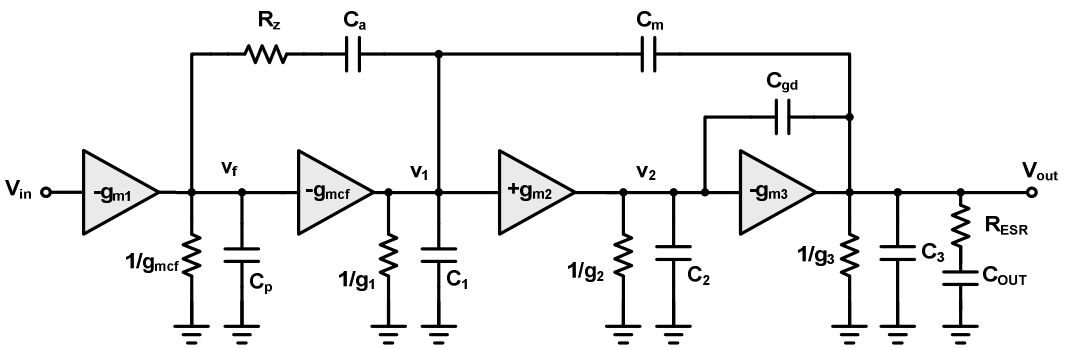


Fig. 43. Analysis structure of CFC LDO regulator with off-chip capacitor.

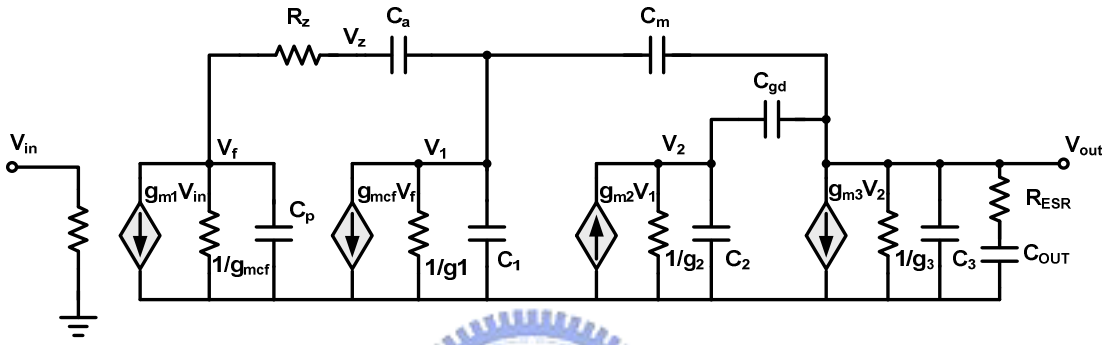


Fig. 44. Small signal analysis of CFC LDO regulator with off-chip capacitor.

The small signal analysis of proposed LDO regulator with off-chip capacitor is shown in Fig. 44.

Using KVL and KCL theorems, the transfer function from input to output can be expressed in equation (60):

$$\frac{V_{out}}{V_{in}} = -A_o \frac{(sR_{ESR}C_L+1)(sC_aR_z+1)(s^2\frac{C_2C_m}{g_{m2}g_{m3}}+s\frac{g_2C_m+g_{m2}C_{gd}}{g_{m2}g_{m3}}-1)}{(1+\frac{s}{\omega_{-3dB}})(1+\frac{s}{\omega_{1st-non}})(1+\frac{s}{\omega_{2nd-non}})} \quad (60)$$

where A_o is the DC loop gain, P_{-3dB} is the dominant pole of this system.

The system is a three poles and one zero system. The others zeros are located at high frequency compared to the unit gain frequency, so the effects can be neglected. The system has one dominant pole which is given by equation (61). The other low frequency pole, first non-dominant pole which given by equation (62), is compensated by the ESR zero which is given by equation (63). The second non-dominant as shown in equation (64) is located above

unit gain frequency.

$$p_{-3dB} = \frac{g_1 g_2 g_3}{g_{m2} g_{m3} C_m} \tag{61}$$

$$\omega_{1st-non} = \frac{g_{m2} g_{m3} C_m}{g_2 C_L (C_m + 2C_a) + g_{m2} g_{m3} R_{ESR} C_L C_m} \tag{62}$$

$$z_{ESR} = \frac{1}{R_{ESR} C_L} \tag{63}$$

$$\omega_{2nd-non} = \frac{g_2 (C_m + 2C_a) + g_{m2} g_{m3} R_{ESR} C_m}{(C_m + 2C_a) C_2} \tag{64}$$

3.2.2.1 Off-Chip Capacitor Design under No Load Condition

At no load condition, the poles and zero can be simplified to equation (65)-(68). If load is increased, the dominant will move to higher frequency proportional to squared root of load current with slope $g_1/C_m A_{v2}$. The first non-dominant pole is proportional to squared root of load current with slope $A_{v2} C_m/(C_m+2C_a)C_L$. Compared the slope between these two poles, the first non-dominant pole will move faster than dominant pole. Therefore, the worst case stability occurs at no load condition under light load condition.

$$p_{-3dB} = \frac{g_1 g_2 g_3}{C_m g_{m2} g_{m3}} \propto \frac{g_1}{C_m A_{v2}} \sqrt{I_{Load}} \tag{65}$$

$$p_{1st-non} = \frac{g_{m2} g_{m3} C_m}{g_2 C_L (C_m + 2C_a)} \propto A_{v2} \frac{C_m}{(C_m + 2C_a) C_L} \sqrt{I_{Load}} \tag{66}$$

$$z_{ESR} = \frac{1}{R_{ESR} C_L} \tag{67}$$

$$p_{2nd-non} = \frac{g_2}{C_2} \tag{68}$$

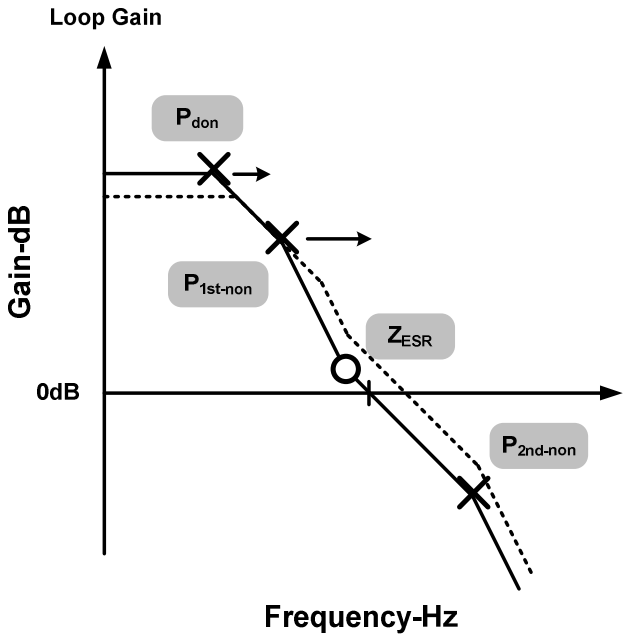


Fig. 45. Frequency response of off-chip capacitor design under light load condition.

Meanwhile, the second non-dominant pole located at power MOS gate terminal is near a constant value under light load condition which is usually in several hundreds kilo hertz. And the ESR zero is utilized to compensate the first non-dominant pole to maintain the system stability. The frequency response of overall system as load increased under light load condition is shown in Fig. 45.

The system has two low frequency poles and one low frequency zero. And the overall system stability can be obtained by equation (69):

$$\begin{aligned} PM &= 180^\circ - \tan^{-1}\left(\frac{UGF}{p_{don}}\right) - \tan^{-1}\left(\frac{UGF}{p_{1st-non}}\right) + \tan^{-1}\left(\frac{UGF}{z_{ESR}}\right) \\ &= 90^\circ - \tan^{-1}\left(\frac{UGF}{p_{1st-non}}\right) + \tan^{-1}\left(\frac{UGF}{z_{ESR}}\right) \\ &\approx 60^\circ \end{aligned} \tag{69}$$

3.2.2.3 Off-Chip Capacitor Design under Heavy Load

Condition

As load is increased under heavy load condition, the poles and zero locations can be reduced to equation (70)-(73).

$$p_{-3dB} = \frac{g_1 g_2 g_3}{C_m g_{m2} g_{m3}} \tag{70}$$

$$p_{1st-non} = \frac{1}{R_{ESR} C_L} \tag{71}$$

$$z_{ESR} = \frac{1}{R_{ESR} C_L} \tag{72}$$

$$p_{2nd-non} = \frac{g_{m2} g_{m3} R_{ESR} C_m}{(C_m + 2C_a) C_2} \tag{73}$$

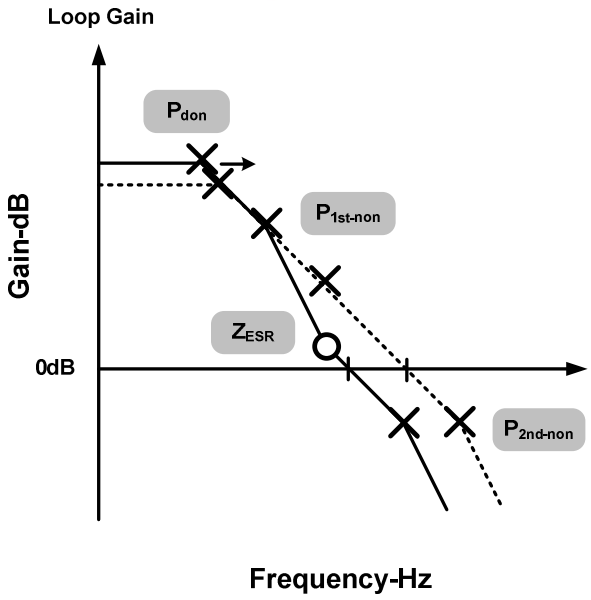


Fig. 46. Frequency response of off-chip capacitor design under heavy load condition.

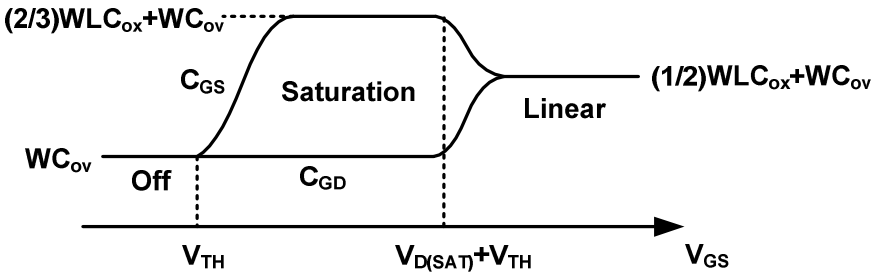


Fig. 47. Variation of gate-source and gate-drain capacitances versus V_{GS}.

The first non-dominant pole can be approximately cancelled by ESR zero, i.e. the output pole is equal to ESR zero. Therefore, the system stability is determined by the dominant pole and second non-dominant pole since the unit gain frequency increased greatly. The frequency response under heavy load condition is shown in Fig. 46.

However, if load is increased heavier with power MOS operated in linear region, the second non-dominant pole will be move to lower frequency to degenerate the stability. It is well know that the gate capacitance of power MOS is increased when operated form saturation region to linear region as shown in Fig. 47, so the second non-dominant pole will be move to lower frequency due to equation (73).

The phase margin of this system can be calculated by equation (74). Therefore, the ESR must be large enough to assure that the second non-dominant is larger enough than the unit gain frequency to maintain the stability.

$$\begin{aligned} PM &= 180^\circ - \tan^{-1}\left(\frac{UGF}{p_{don}}\right) - \tan^{-1}\left(\frac{UGF}{p_{1st-non}}\right) + \tan^{-1}\left(\frac{UGF}{z_{ESR}}\right) - \tan^{-1}\left(\frac{UGF}{p_{2nd-non}}\right) \\ &= 90^\circ - \tan^{-1}\left(\frac{UGF}{p_{1st-non}}\right) + \tan^{-1}\left(\frac{UGF}{z_{ESR}}\right) - \tan^{-1}\left(\frac{UGF}{p_{2nd-non}}\right) \\ &= 90^\circ - \tan^{-1}\left(\frac{UGF}{p_{2nd-non}}\right) \\ &\approx 60^\circ \end{aligned} \tag{74}$$

3.3 Bandgap Reference

For a linear regulator, an accurate and precise reference voltage which exhibits supply and temperature independent is required. The conventional bandgap reference is shown in Fig. 48.

The base-emitter voltage of bipolar transistors, the forward voltage of a pn-junction diode exhibits a negative temperature coefficient (TC). So we must generate a positive TC to compensate the negative TC. It was recognized that if two bipolar transistors operate at unequal current densities, then the difference between their base-emitter voltages is directly proportional to the absolute temperature. The V_{BE} difference exhibits a positive temperature coefficient:

$$\Delta V_{BE} = V_T \ln n \tag{75}$$

where $V_T = kT/q$ and n is the size ratio between two transistors.

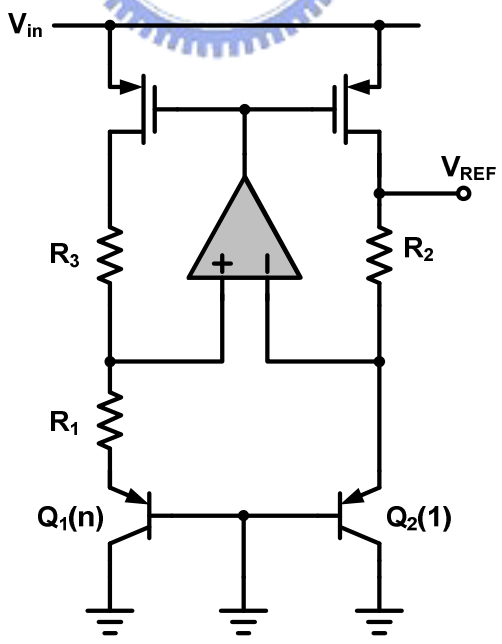


Fig. 48. Conventional bandgap reference.

So we have V_{BE1} - V_{BE2}=$V_T \ln n$, arriving at a proportional to absolute temperature (PTAT) current equal to $V_T \ln n$ /R_1. The reference voltage can be decided by the right branch as shown in equation (76):

$$V_{REF} = V_{BE} + \frac{R_2}{R_1} V_T \ln n \tag{76}$$

The resistor R_3 is added to minimize the channel length modulation effect between two PMOS transistors. Meanwhile, the circuit consists of two closed loop. One is positive feedback and the other is negative feedback. We must make sure that negative feedback is always larger than positive feedback.

The op amp of bandgap reference must provide a loop gain enough. Because PSR of the bandgap reference is important as fluctuations at the output of the reference at frequencies lower than the gain bandwidth of the regulator. There are two ways to improve PSR of bandgap reference. One is to enhance the loop gain of the op amp. The other way is to place a relatively large capacitor to shunt the output ripple to ground, but this increases start-up time and costs more [4].

Chapter 4

Circuit Implementations & Simulation Results

In this chapter, we will give a design procedure of our proposed LDO regulator according to previous theorems. In Chapter 4.1, the circuit implementation is introduced first, and then the design procedure is given step by step. The simulation results of each block are shown respectively. Then the system simulation results will be demonstrated in Chapter 4.2. Finally, the overall performance of proposed LDO is summarized in Chapter 4.3.

The specification of proposed LDO is shown in TABLE III. The proposed LDO is fabricated by TSMC 0.35μm 2P4M process. The input range is 3V to 4.5V, which is a conventional Li battery voltage range. The output voltage is 2.8V with typical operation. The load range is 50μA to 100mA under capacitor-free condition and 0 mA to 100 mA under off-chip capacitor condition.

TABLE III

SPECIFICATION OF CFC LDO REGULATOR.

	Capacitor-Free	*With Capacitor*	*Units*
Technology	TSMC 0.35μm 2P4M		
Supply voltage	3.0~4.5		*V*
Output voltage	2.8		*V*
Load current I_{Load}	50μ~100m	0m~100m	*A*

4.1 Circuit Implementation & Design

The system can be divided into three major blocks, main LDO structure, bandgap reference and biasing circuit. In this secession, the circuit implementation and design procedure will be described respectively.

4.1.1 CFC LDO Regulator Structure

In the schematic shown in Fig. 49, the basic structure of this LDO regulator consists of three gain stage. The first stage is a differential to single out high gain stage which consists of M_1~M_6. The second gain stage consists of M_7~M_{12} and R_B. The transistor M_7~M_{10} forms a wideband stage to create a ground reference form the compensation capacitor. And transistor M_{10}~M_{12} and R_B forms a common source stage with resistive load R_B to achieve high PSR performance. The third gain stage is common source power PMOS stage. The feedback resistors $R_{F1,2}$ form the shunt feedback effect to regulate the output voltage.

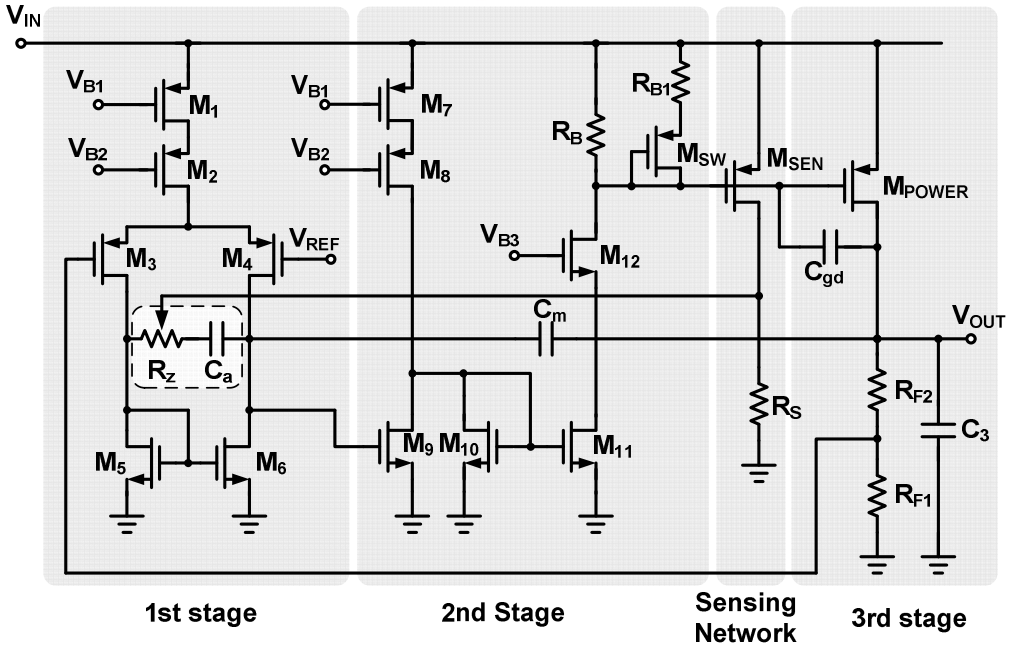


Fig. 49. Circuit schematic of CFC LDO regulator.

The dominant pole compensation capacitor is connected a ground reference, output of first stage, to the output to prevent noise directly pass to the output. The propose compensation network, C_a and R_z, is shown in dotted line in Fig. 49. The compensation capacitor C_a is connected to a ground reference to maintain high PSR performance. The dynamic resistor R_z acts dynamic zero compensation (DZC) is form by a PMOS operated in triode region controlled by the sensing network.

In order to achieve faster transient response, the unit gain bandwidth is set about near 1MHz. The compensation capacitor is usually in several pico-Farad. As shown in equation (77), the transconductance g_{m1} of input pair is set about 30 μS.

$$g_{m1} = UGF \cdot C_m \tag{77}$$

The output capacitor must still large enough about 50 pF. So the power MOS size is (35000/0.5) in this design. The minimum load current is about 50μA, and the transconductance g_{m3} is about 1.25 mS. The gate capacitance is about 30 pF, the transconductance g_{m2} is set about 1 mS to have faster slewing.

The DC gain is about 95dB according to equation (78).

$$A_{vo} = \frac{g_{m1} g_{m2} g_{m3}}{g_1 g_2 g_3} \tag{78}$$

The nature frequency ω_o according to equation (79) is about 4.5 MHz.

$$\omega_o = \sqrt{\frac{g_{m2} g_{m3}}{C_2 C_3}} \tag{79}$$

Under low Q assumption, the compensation C_a can be obtained according to equation (50)(51). The capacitor C_m and C_a are 5pF and 1.5 pF in this design respectively. The parameters of LDO under load current 50μA are listed in TABLE IV.

TABLE IV

PARAMETERS OF LDO UNDER LOAD CURRENT 50μA.

Transconductance of each stage					
g_{m1}	70 μS	g_{m2}	1.35 mS	g_{m3}	1.25 mS
g_{mcf}	34 μS				
Reactance of each stage					
g_1	0.264 μS	g_2	50 μS	g_3	34 μS
Parasitic capacitor of power PMOS					
C_2	28 pF	C_{gd}	6.4 pF	C_3	54 pF
C_m	5 pF	C_a	1.5 pF		

After the above design, the pole locations and AC parameters of proposed LDO under load current 50μA is shown in TABLE V. The DC gain and phase margin are 94.1 dB and 61.3° respectively. The dominant pole is located at low frequency 19Hz. The nature frequency ω_o is 4.5 MHz, and then the unit gain frequency is about 890 kHz. The first non-dominant pole is located at 1.8MHz to maintain the phase margin about 60°. The quality factor Q is 5.85 with nature frequency ω_o 4.5 MHz which has little effect on stability.

TABLE V

AC PARAMETERS OF CFC CAPACITOR-FREE LDO UNDER LOAD 50μA.

P_{-3dB}	$P_{1st\text{-}non}$	ω_o	Q	A_{vo}	UGF	PM
19 Hz	1.8 MHz	4.5 MHz	5.85	94.1dB	890kHz	61.3

The dynamic zero compensation (DZC) network is used to compensate the first non-dominant pole as load increased. The sensing ratio between power MOS M_{POWER} and sensing MOS M_{SEN} is set to 1000, i.e. the current consumption is 100 μA as load is 100 mA. The sensing resistor is designed to 2 kΩ to maintain the phase margin about 60° under the heaviest load 100 mA.

As mentioned before, the poles and zero locations are varied with load conditions. The poles and zero locations under different load condition are shown in TABLE VI. As load increased, the dominant pole is moved to higher frequency. However, the first non-dominant

pole is moved to lower frequency to degenerate the phase margin. But the dynamic zero compensation network generates a zero which is decreased as load increased. Therefore, the phase margin can be maintained near 60 degree. The nature frequency is increased as load increased, while the quality factor in decreased. And the complex poles will be become two separated poles under load current several mili-amp. The gain magnitude of proposed is decreased as load increased, and the unit gain frequency is near constant unless the heavy load condition with power MOS operated in linear region.

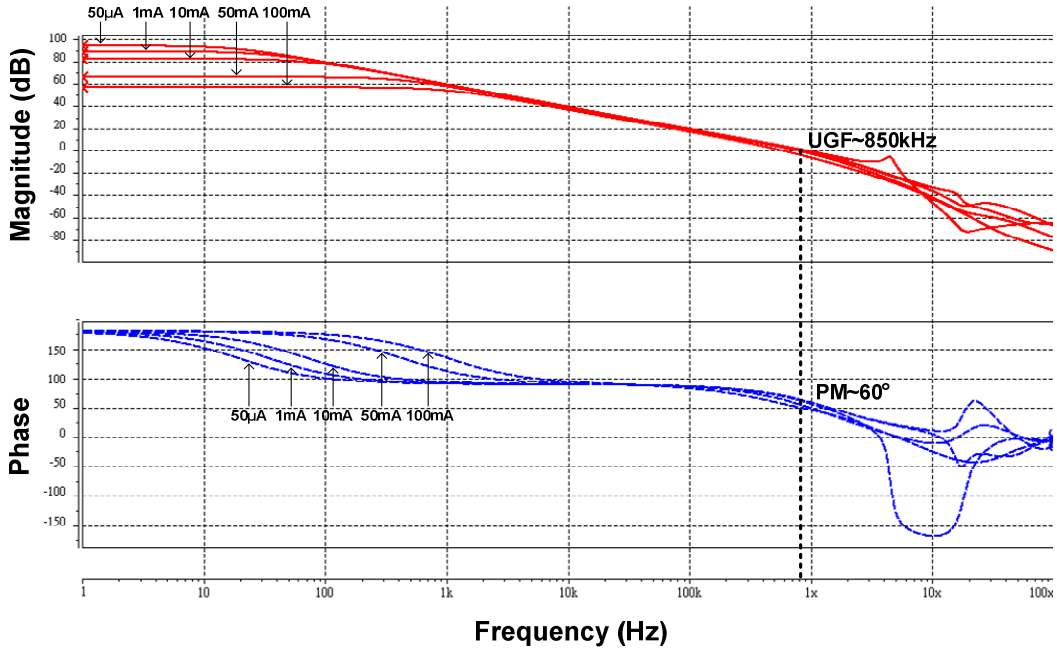


Fig. 50. Loop responses of CFC capacitor-free LDO under different load conditions.

TABLE VI

AC PARAMETERS OF CFC CAPACITOR-FREE LDO UNDER DIFFERENT LOAD.

Load	P_{-3dB}	$P_{1st\text{-}non}$	Z_{DZC}	ω_o	Q	A_{vo}	UGF	PM
50 µA	19 Hz	1.8 MHz	11.4 MHz	4.5 MHz	5.85	94.1dB	890kHz	61.3
500 µA	29 Hz	1.7 MHz	11.3 MHz	12.3MHz	5.00	90.4dB	855kHz	61.4
1 mA	34 Hz	1.7 MHz	11.3 MHz	16.0MHz	3.27	89.1dB	855kHz	63.7
10 mA	70 Hz	1.6 MHz	11.1 MHz	--	--	82.6dB	852kHz	63.6
50 mA	422 Hz	1.3 MHz	9.1 MHz	--	--	66.3dB	750kHz	58.6
100 mA	1 kHz	560 kHz	1.1 MHz	--	--	57.2dB	560kHz	58.5
	↗	↘	↘	↗	↘	↘	×	×

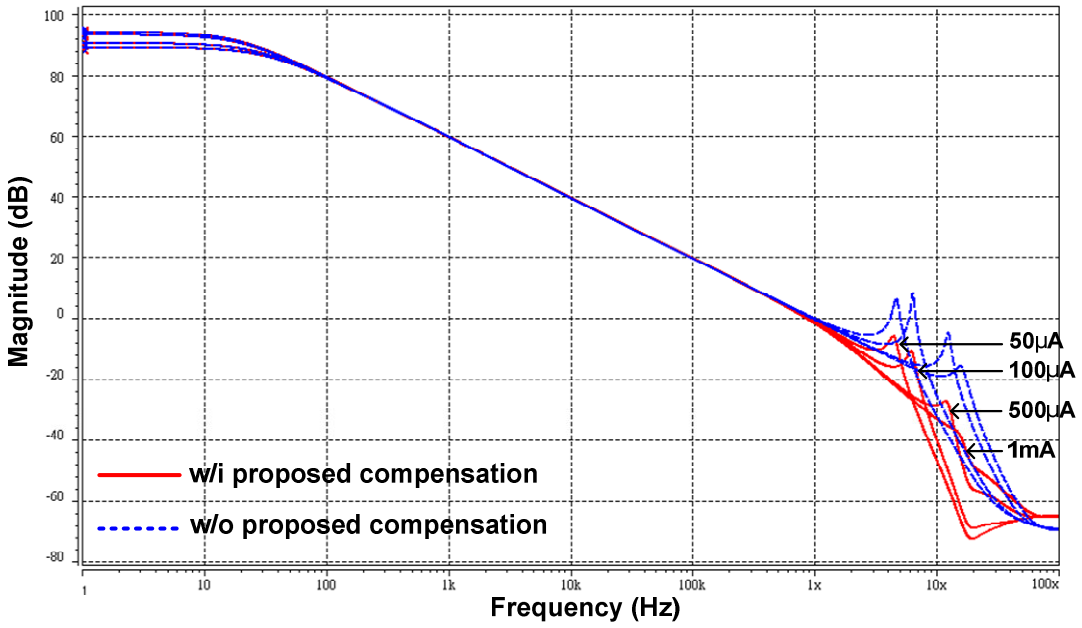


Fig. 51. Loop responses with and without CFC technique.

The frequency response under different load current is shown in Fig. 50. The magnitude rolls off with -20dB/dec after the dominant pole and with -40dB/dec above the first non-dominant pole. The unit gain frequency and phase margin always keeps in 850 kHz and 60 degree respectively.

Compared with proposed LDO with and without compensation, the quality factor Q has been decreased greatly and occurs at lower magnitude as shown in Fig. 51. The pole locations without proposed compensation are located right-half-plane under load current 50μA and 100μA. Although the poles are located left-half-plane under load current 500μA, the quality factor is too large to make the system unstable. With proposed compensation, right-half-plane poles are converted to left-half-plane poles with low quality factor Q. The system is remained stable even with ultra light load current.

The PSR performance of proposed LDO is shown in Fig. 52. The DC PSR is -92.5dB and -66.6dB under load current 1mA and 100mA respectively. The PSR at 1MHz is -28dB and -10dB under load current 1mA and 100mA respectively.

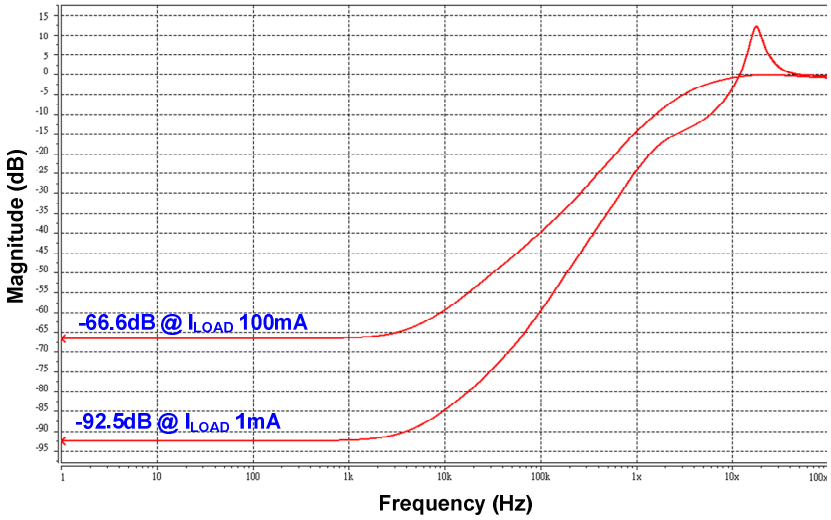


Fig. 52. PSR performance of CFC capacitor-free LDO regulator.

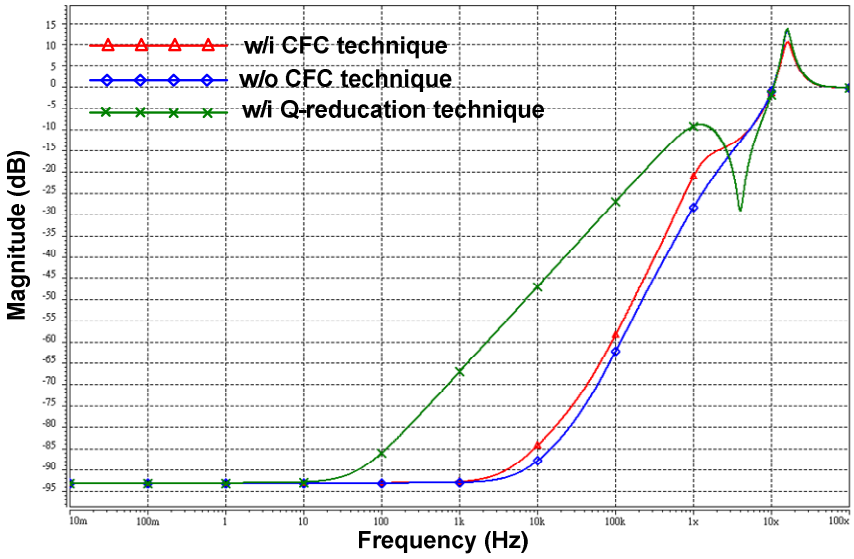


Fig. 53. PSR performance with different compensation technique.

The PSR performance with different compensation technique under load current 1mA is shown in Fig. 53. It shows that the high PSR characteristic is maintained even the CFC technique is used. If the Q-reduction technique is used, the PSR bandwidth is greatly reduced.

If the system needs an off-chip capacitor to have better transient response, the ESR is required to compensate the output low frequency pole. The frequency response with off-chip capacitor 10μF and ESR 1Ω under different load current is shown in Fig. 54.

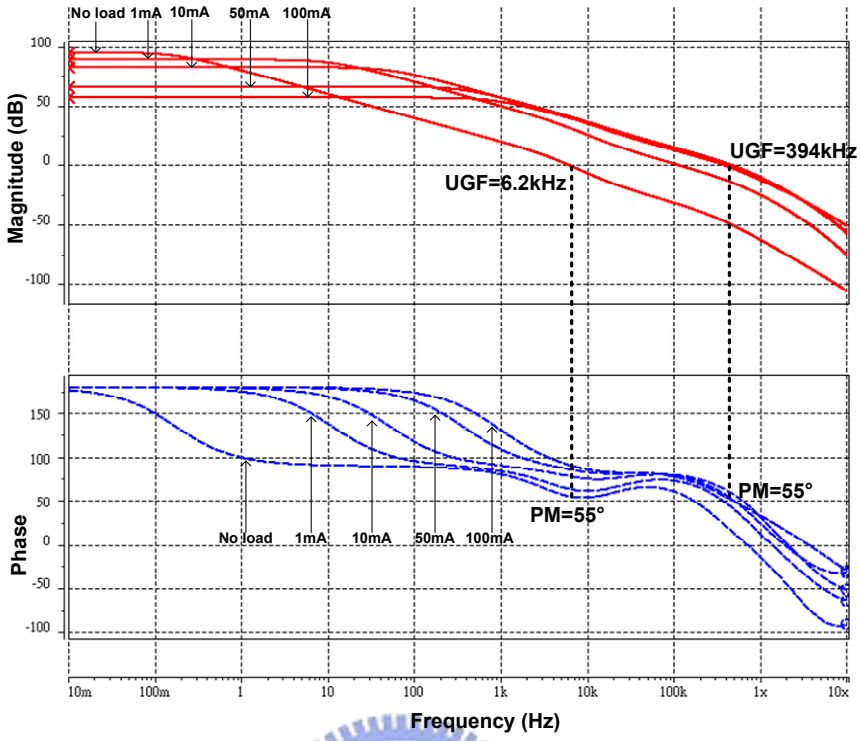


Fig. 54. Loop responses under different load conditions with off-chip capacitor.

According to the theorem described in Chapter 3.2.2, the ESR zero is used to compensate the first non-dominant pole. Since the first non-dominant pole moves faster than dominant pole, the worse case stability occurs at no load condition. But the second non-dominant pole will move to lower frequency when the power MOS is operated from saturation region to linear region. The stability is degenerated at heavy load condition. So the ESR zero must maintain the stability in no load and heavy load conditions.

TABLE VII

POLES AND ZERO LOCATIONS WITH OFF-CHIP CAPACITOR 10μF AND ESR 1Ω.

Load	P_{-3dB}	$P_{1st\text{-}non}$	$P_{2nd\text{-}non}$	Z_{ESR}	A_{vo}	*UGF*	*PM*
No load	0.17 Hz	4.4 kHz	283 kHz	15.9 kHz	95.1dB	6.2 kHz	55
1mA	11 Hz	5.7 kHz	603 kHz	15.9 kHz	89.1dB	116 kHz	72
10mA	53 Hz	9.5 kHz	1.0 MHz	15.9 kHz	82.6dB	400 kHz	63
50mA	370 Hz	11.7 kHz	770 kHz	15.9 kHz	66.3dB	471 kHz	52
100mA	910 Hz	11.8 kHz	465 kHz	15.9 kHz	57.2dB	394 kHz	55

4.1.2 Bandgap Reference

The bandgap reference structure is shown in Fig. 55. For layout symmetry conveniently, the size ratio is set to 8. The TC of V_{BE} is about -2.2 mV and the positive TC of the difference between their base-emitter voltages is about 0.18 mV. Therefore, the ratio between R_1 and R_2 is set about 12. Since the desired reference voltage is about 1.2V, the resistor R_1 is set to 1.5kΩ, which results in a PTAT current 4.27 μA, and the resistor R_2 is set to 155kΩ.

Because the power integrated IC always is operated at higher temperature, the temperature cancellation is set at 75°C to get a stable reference under operating. P type diffusion resistor is used by tradeoff between sheet resistance and fabricated variation. The simulation of reference voltage with temperature varied from 0°C to 100°C and supply voltage varied from 3V to 4.5V is shown in Fig. 56. The simulation result shows that the TC is 18 ppm/°C at supply voltage 3V and 21 ppm/°C at supply voltage 4.5V.

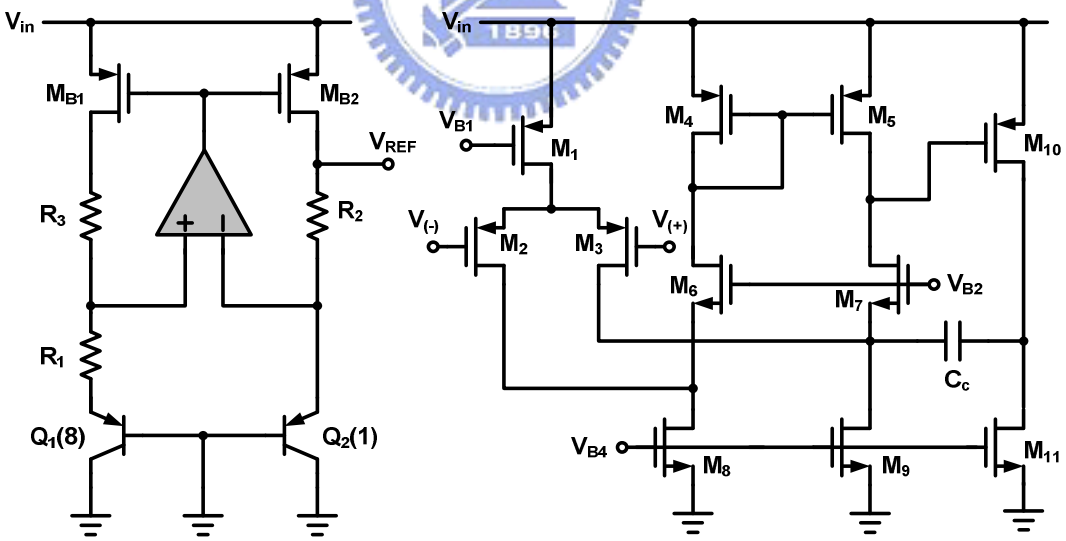


Fig. 55. Circuit schematic of bandgap reference.

In order to get higher PSR of bandgap reference, the cascade CMOS op amp is used [33]. Since the Miller capacitor is connected to a ground reference by using ground gate cascade

technique, the feed though path of supply noise is eliminated. The PSR bandwidth can be improved. Meanwhile, since the RHP zero occurs at higher frequency, the RHP zero removal technique is not required.

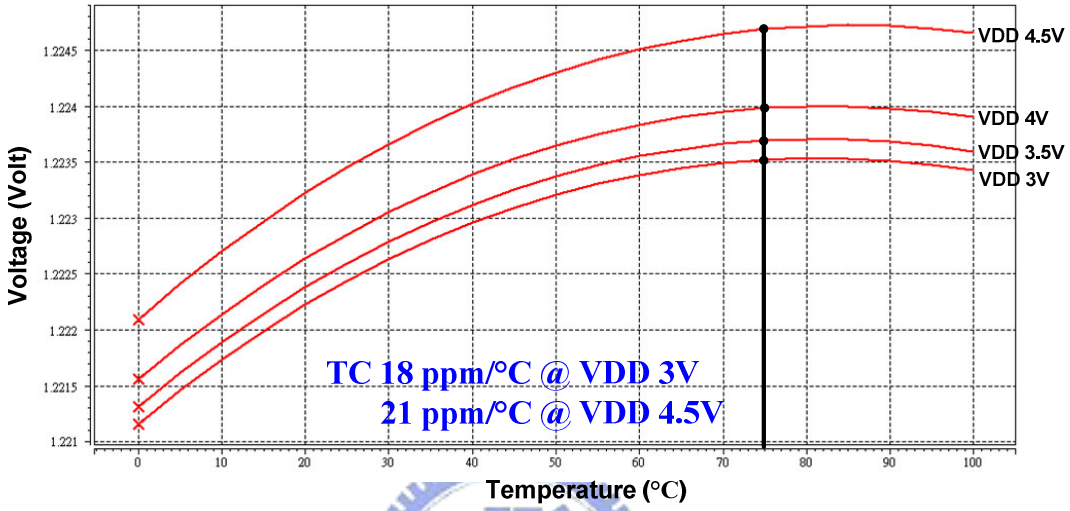


Fig. 56. Simulation of reference voltage at different supply voltages.

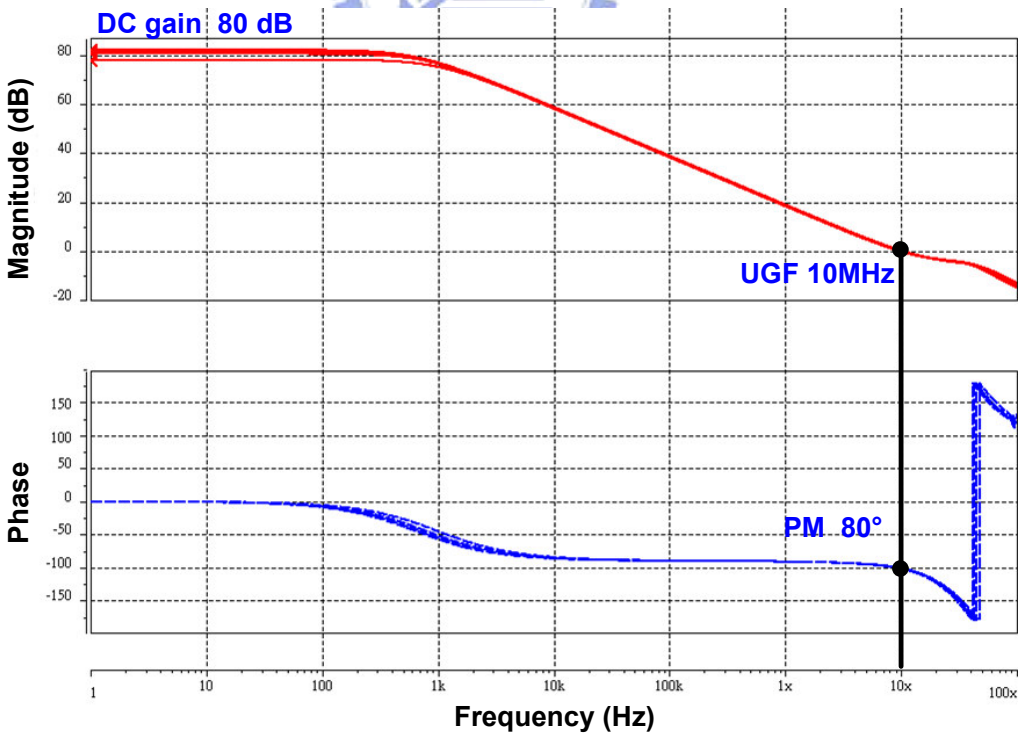


Fig. 57. Simulation of bandgap op amp.

The bandgap op amp in this design is about 80 dB dc gain with unit gain frequency 10MHz and phase margin 80°. The compensation capacitor C_c is 0.2 pF. The power consumption of this op is 6 μA. The simulation result of this op amp with supply voltage varied from 3V to 4.5V is shown in Fig. 57.

The PSR of this bandgap can be show in equation (80). Since the PSR is relative to the op amp power supply rejection ratio, the PSR is deteriorated as supply voltages increased [34].

$$PSR = \frac{1}{1-\frac{\beta_2}{\beta_1}}\left[\frac{1}{A_1} + \frac{g_{o2}}{g_{m2}}\frac{1}{A_1} - \frac{1}{PSRR_1}\right]\frac{1}{\beta_1} \tag{80}$$

where $PSRR_1$ is the power supply rejection ratio of op amp, β_1 andβ_2 are positive and negative feedback factors, and A_1 is open loop differential gain of OP amp.

The PSR performance of bandgap reference is shown in Fig. 58. The PSR is -70dB at DC and -18dB at 100 kHz with minimum supply voltage 3V.

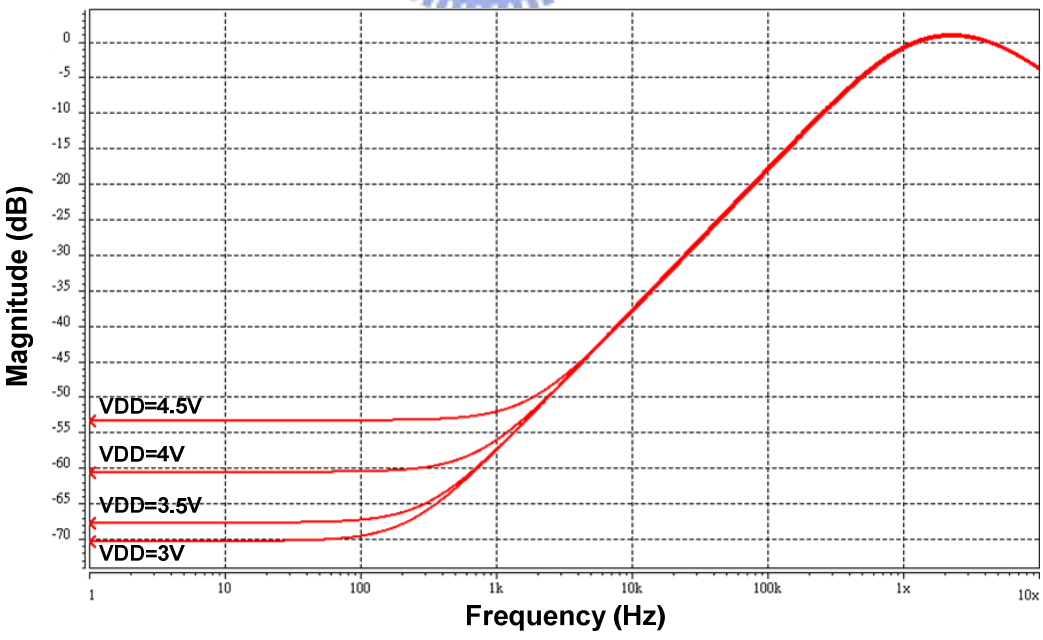


Fig. 58. Simulation of PSR of bandgap reference.

4.1.3 Biasing Circuit

In the above circuit, one biasing circuit which exhibits little dependence on supply, process parameters and temperature is needed. In order to arrive less sensitive solutions, this circuit must be bias itself. The supply-independent or named as constant G_m circuit is the most common biasing circuit [35]. By using cascode topology to increase output resistance, the biasing circuit will be more insensitive due to the second order effects [36][37]. The biasing circuit is shown in Fig. 59. The supply-independent circuit consists of M_{B1}~M_{B8}. M_{B15}~M_{B17} produces another biasing voltage. The transistor M_{B9}~M_{B14} give the bias for $M_{B3\text{-}6}$. The biasing current can be determined by the loop of M_{B1}, M_{B2} and R_s which is given in equation (81)

$$I_{REF} = \frac{2}{\mu_p C_{ox} (\frac{W}{L})_P} \cdot \frac{1}{R_s^{\,2}} (1 - \frac{1}{\sqrt{K}})^2 \tag{81}$$

where $(W/L)_p$ is the size of M_{B1} and K is the ratio of M_{B2} to M_{B1}.

An important issue in supply-independent biasing is the existence of degenerate bias points. If all of transistors carry zero current, that's an operating point for this circuit. The circuit can settle in one of two different operating conditions. Therefore, the start-up circuit is

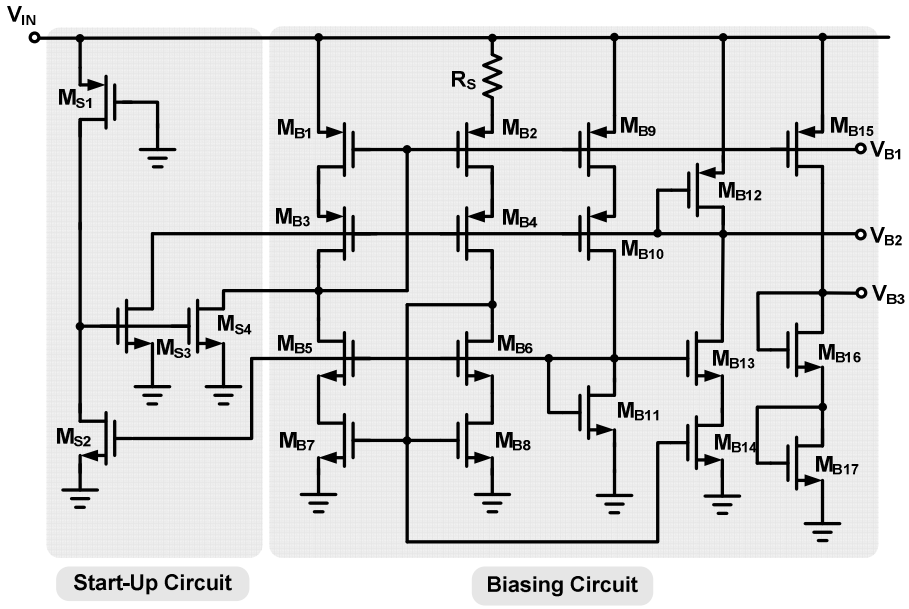


Fig. 59. Circuit schematic of biasing circuit.

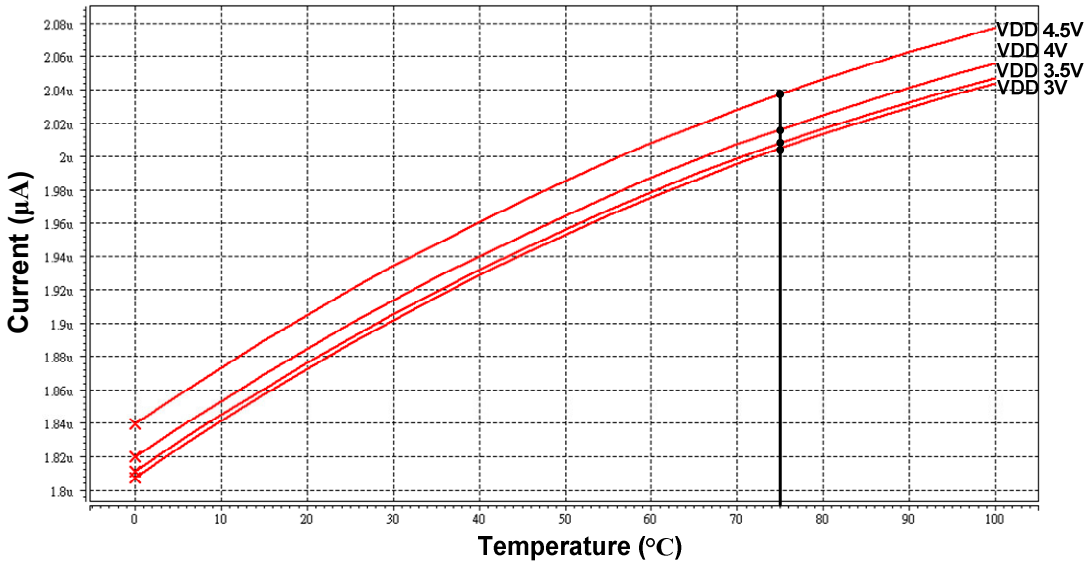


Fig. 60. Simulation of biasing current versus temperature and supply voltage.

needed. The start-up circuit consists of $M_{S1\text{-}4}$. If biasing circuit is zero, M_{S2} will be turned off. And the transistor $M_{S3\text{-}4}$ will be turned on to discharge the gate of $M_{B1\text{-}4}$. When the transistor $M_{B5\text{-}8}$ are turned on, M_{S2} will be turned on to turn off the start-up circuit.

In this design, the biasing current is set to 2 µA. According to equation (81), the resistor R_s is about 37 kΩ in this process. The bias current variation is about 12% at supply 3V and 12% at supply 4.5V which is acceptable for this system. The simulation of biasing current versus temperature and supply voltage is shown in Fig. 60.

4.2 Simulation Results of CFC LDO Regulator

The load transient test method is shown in Fig. 61. The light load condition is realized by resistor R_{L1}, and heavy load condition is realized by resistor R_{L1} which is controlled by a NMOS switch. When the switch is turned on, the resistor R_{L2} will be in parallel with resistor R_{L1} to form heavy load condition.

For capacitor-free design, the load current is changed from 50µA to 100mA and 100mA to 50µA within 1µs. Since there is minimum load restriction without proposed compensation,

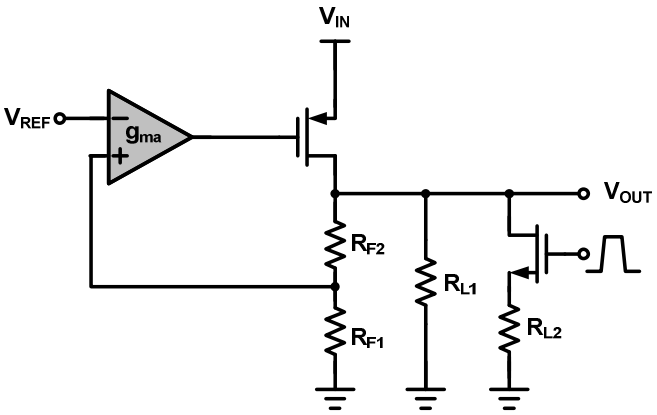


Fig. 61. Load transient test method.

the compensation capacitor C_m must be large enough and the tranconductance g_{m2} of second must be set small enough to ensure the stability. In this design, the compensation capacitor C_m is 20 pF and the tranconductance g_{m2} is 0.8mS while the compensation capacitors are 5pF and 1.5pF respectively and the tranconductance g_{m2} is 1.175mS.

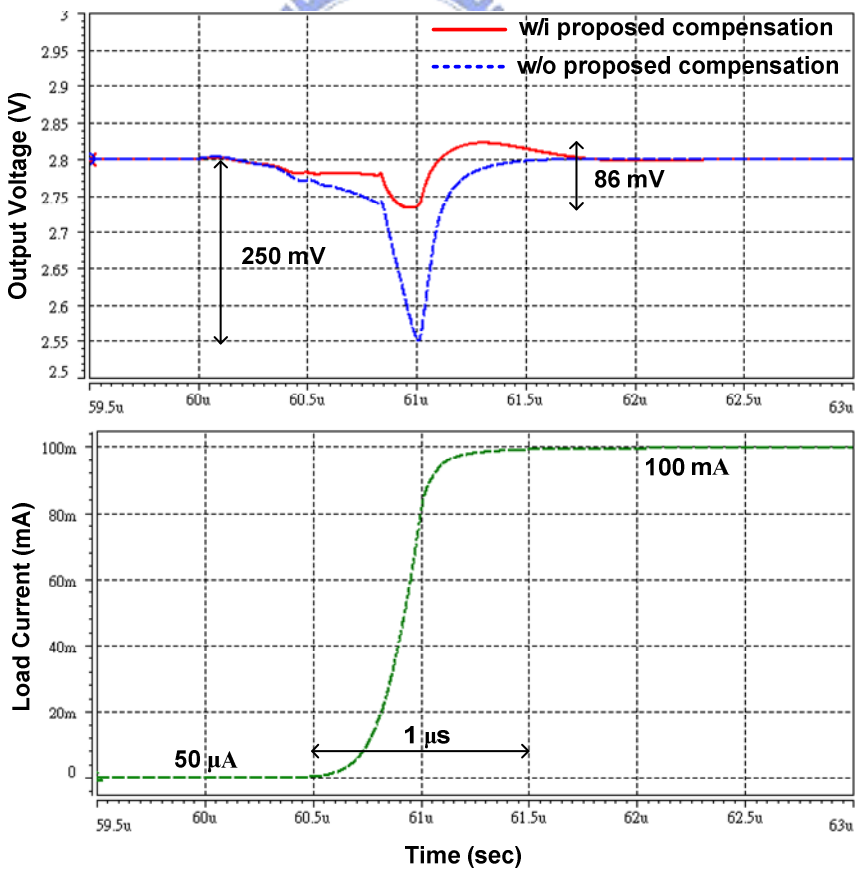


Fig. 62. Load transient of CFC capacitor-free LDO under light load to heavy load.

As shown in Fig. 62, the load current is varied from 50μA to 100mA. The voltage drop without proposed compensation is 250 mV with settling time 1μs, and with proposed compensation is 86 mV with settling time 1μs. The voltage drop is improved 250%.

As shown in Fig. 63, the load current is varied from 100mA to 50μA. The voltage variation without proposed compensation is 123 mV with settling time 2.5 μs, and with proposed compensation is 98 mV with settling time 1μs. The voltage variation is improved 20% and the settling time is improved 150%.

Comparison of load transient comparisons without and with CFC technique is summarized in TABLE VIII. With the CFC technique, the compensation capacitors are greatly reduced and transconductance g_{m2} can be designed largely to help the load transient response.

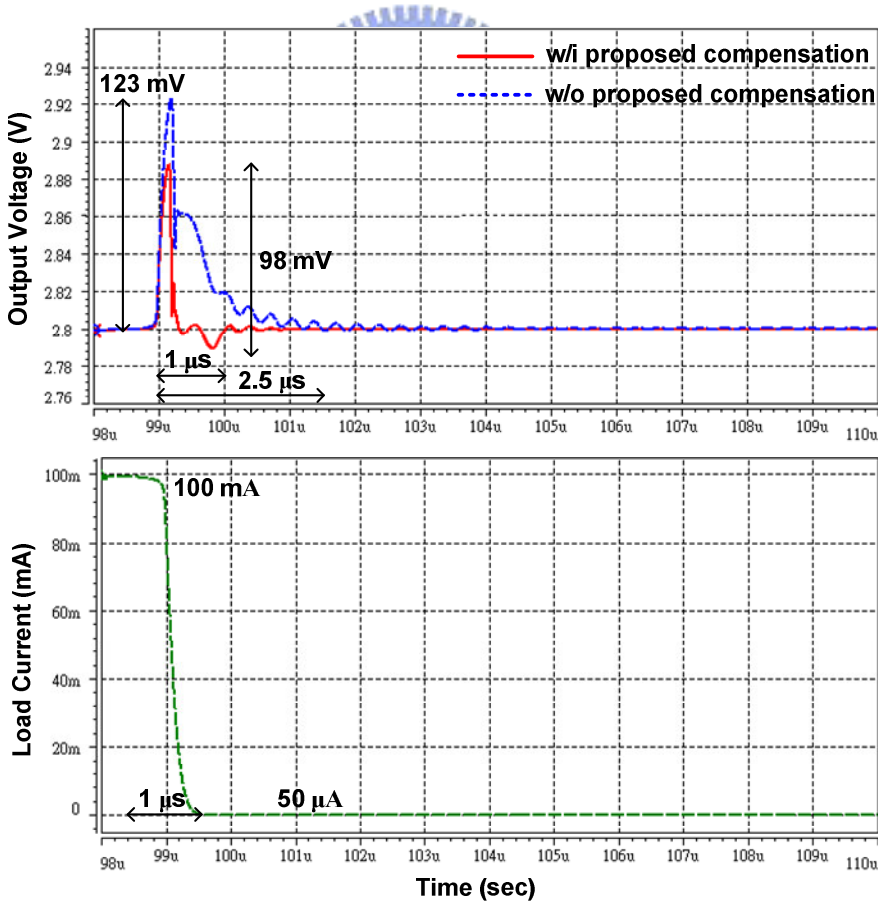


Fig. 63. Load transient of CFC capacitor-free LDO under heavy load to light load.

TABLE VIII

LOAD TRANSIENT COMPARISONS W/O AND W/I CFC TECHNIQUE.

	w/o CFC Technique	*w/i CFC Technique*	*Improvement*
Compensation capacitors	C_m=20pF	C_m=5pF, C_a=1.5pF	Smaller Capacitors
Tranconductance g_{m2}	0.8 mS	1.175 mS	Larger g_{m2}
50μA-100mA	250 mV	88.7 mV	250 %
Settling time	1 μs	1 μs	--
100mA-50μA	123 mV	98 mV	20 %
Settling time	2.5 μs	1 μs	150 %

The load transient test with off-chip capacitor is shown in Fig. 64. The load current step is from 0 mA to 100 mA and 100mA to 0 mA with 1μs and supply voltage 3V with output voltage 2.8V. When load is changed from light load to heavy load, the voltage drop is 60mV and the settling time is 1.5μs. When load is changed from heavy load to light load, the voltage variation is 40mV and the settling time is 1μs.

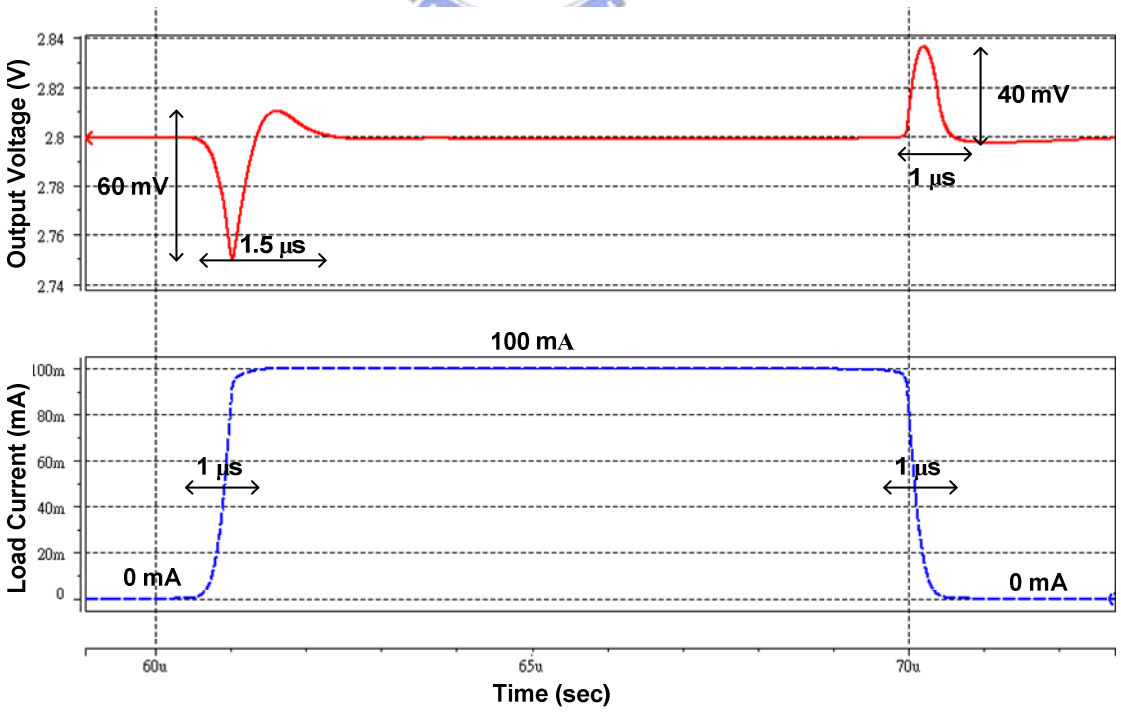


Fig. 64. Load transient of CFC LDO with off-chip capacitor.

The PSR performance of capacitor-free LDO is shown in Fig. 65. The DC PSR is -63dB and -53dB under load current 1mA and 100mA respectively. The PSR at 1MHz is -8dB and -11dB under load current 1mA and 100mA respectively.

The PSR performance of off-chip capacitor LDO is shown in Fig. 66. The DC PSR is -63dB and -53dB under load current 1mA and 100mA respectively. The PSR at 1MHz is -12.5dB and -35dB under load current 1mA and 100mA respectively.

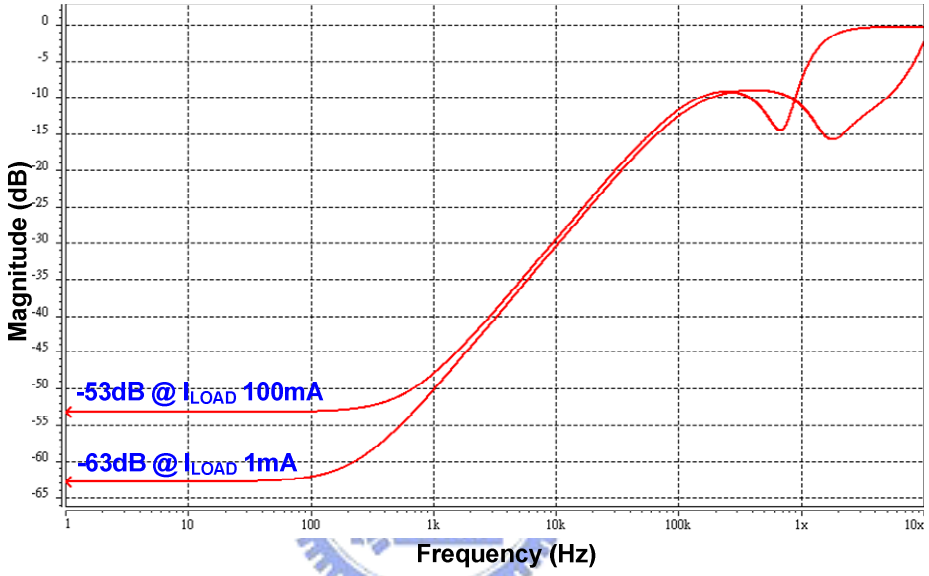


Fig. 65. PSR performance of CFC capacitor-free LDO.

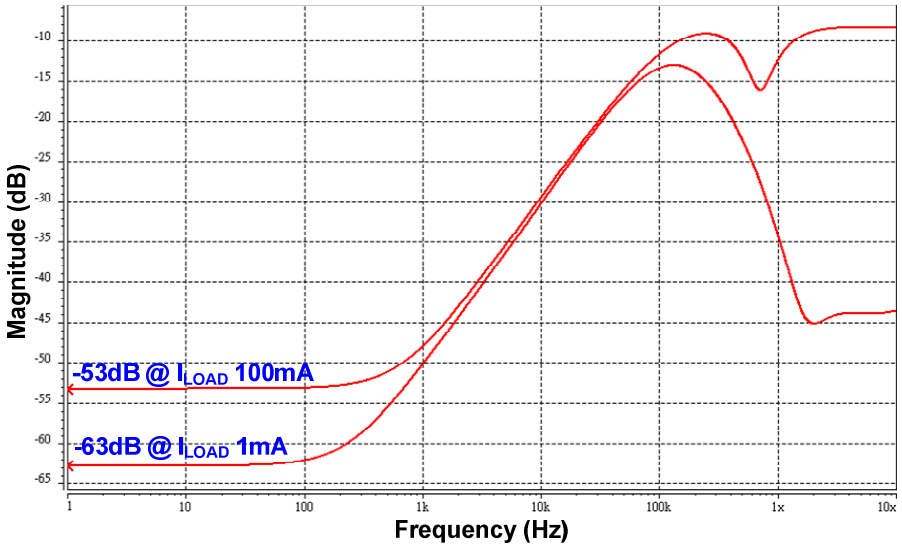


Fig. 66. PSR performance of CFC LDO with an off-chip capacitor.

4.3 Performance of CFC LDO Regulator

This LDO is fabricated by TSMC 0.35μm 2P4M process. The input range is 3V to 4.5V and the output voltage is 2.8V with typical operation. There are two capacitive load conditions, which one is capacitor-free condition and the other is off-chip capacitor condition.

For capacitor-free condition, the load range is 50μA to 100mA. The load regulation is 4μV/mA with load current ranged from 50μA to 100 mA. The line regulation is 2mV/V with supply ranged from 3V to 5V and load current 100 mA. The load transient settling time is smaller than 1μs whenever heavy load to light load or light load to heavy load. The voltage drop is smaller than 100mV when load current is changed from light load to heavy load or light load to heavy load rapidly.

TABLE IX
PERFORMANCES OF CFC LDO REGULATOR.

	Capacitor-Free	*With Capacitor*	*Units*
Technology	TSMC 0.35μm 2P4M		
Supply voltage	3 – 5		*V*
Output voltage	2.8		*V*
Load range I_{Load}	50μ-100m	0m-100m	*A*
Load Regulation	4 @ I_o= 0.05-100mA	4 @ I_o= 0-100mA	*μV/mA*
Line Regulation	2 @ V_{in}= 3~5V, I_o= 100mA	2 @ V_{in}= 3-5V, I_o= 100mA	*mV/V*
Settling Time	1 @ I_o= 0.05-100mA 1 @ I_o= 100-0.05mA	1.5 @ I_o= 0-100mA 1 @ I_o= 100-0mA	*μs*
Voltage variation	89 @ I_o= 0.05-100mA 98 @ I_o= 100-0.05mA	60 @ I_o= 0-100mA 40 @ I_o= 100-0mA	*mV*
Power Consumption	170		*μA*
Active Area	570 × 600		μm^2

For off-chip capacitor condition, the load range is 0 mA to 100 mA. The load and line regulation is the same as capacitor-free condition since the dc loop gain is the same. The load transient settling time is smaller than 1.5μs whenever heavy load to light load or light load to

heavy load. The voltage variations are 60 mV when load current is changed from light load to heavy load rapidly and 40mV when load current is changed from heavy load to heavy light rapidly.

The power consumption of proposed LDO is 170 μA with typical supply 3V. The overall chip area is about 1182 × 1282 μm^2. The performance of proposed is summarized in TABLE IX.

The layout of proposed LDO regulator is shown in Fig. 67. The chip area is about 1182 × 1282 $\mu m^2$and active area is about 570 × 600 μm^2.

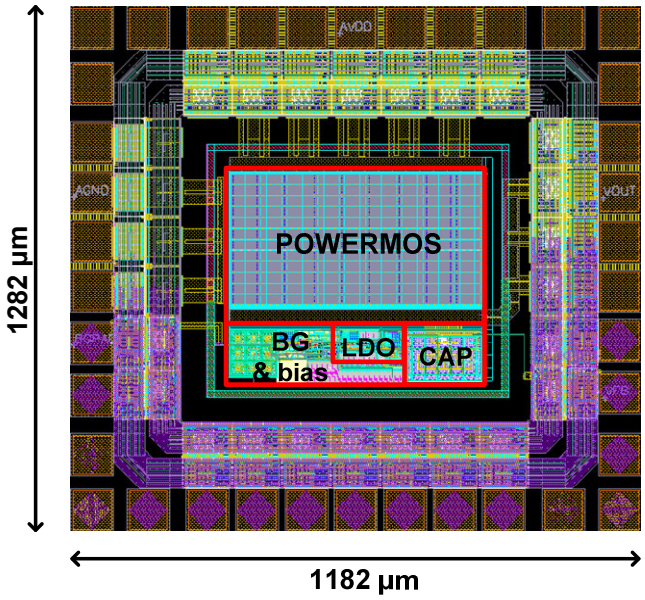


Fig. 67. Layout of CFC LDO regulator.

Chapter 5

Measurement Results and Conclusions

In this Chapter, the measurement results are shown in Chapter 5.1. And conclusions are made in Chapter 5.2. Finally, the future work is shown in Chapter 5.3.

5.1 Measurement Methods and Results

The CFC capacitor-free LDO regulator is fabricated by TSMC 0.35μm2P4M CMOS process supporting by Chip Implementation Center (CIC). The chip die photograph is shown in Fig. 68.

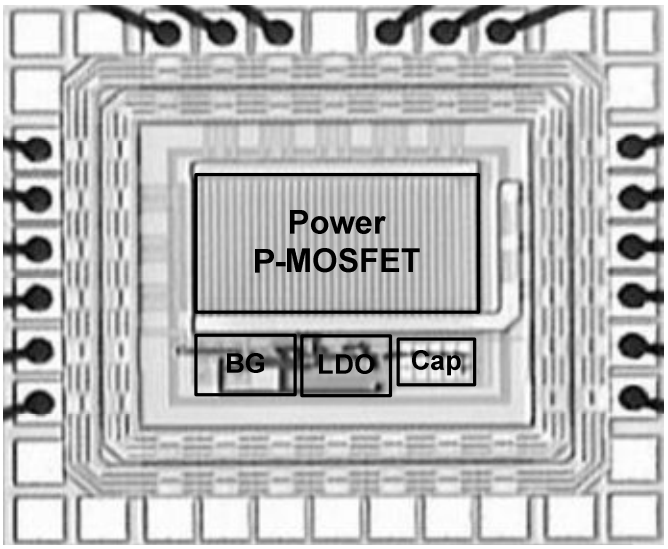


Fig. 68. Die photograph of CFC LDO regulator.

5.1.1 Measurement Methods

The measurement methods of CFC capacitor-free LDO regulator will be demonstrated in this section. The measurement results can be separated into two parts. One is dynamic performance tests, such as load and line transient. The other is static performance tests, such load and line regulation.

The load transient test method is shown in Fig. 69. The load step is realized by the switching load circuit controlling by the clock of function generator and output voltage variation is observed by the oscilloscope. The load regulation is tested with different load conditions.

The line transient test is method shown in Fig. 70. The line step is realized by the switching line circuit controlling by the clock of function generator and output voltage variation is observed by the oscilloscope. The line regulation is tested by different supply voltages.

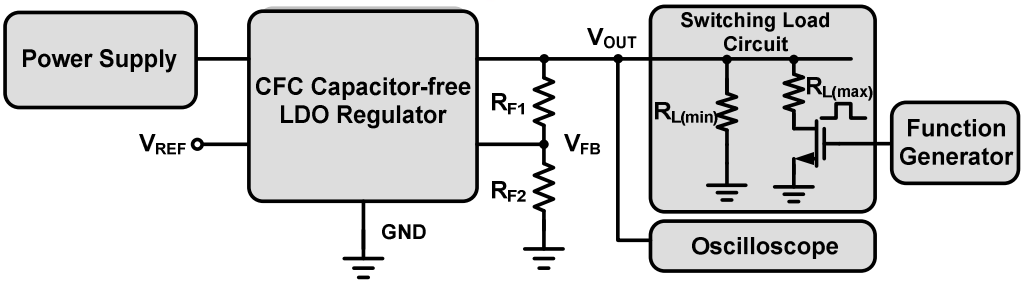


Fig. 69. Load performance tests of CFC Capacitor-free LDO Regulator.

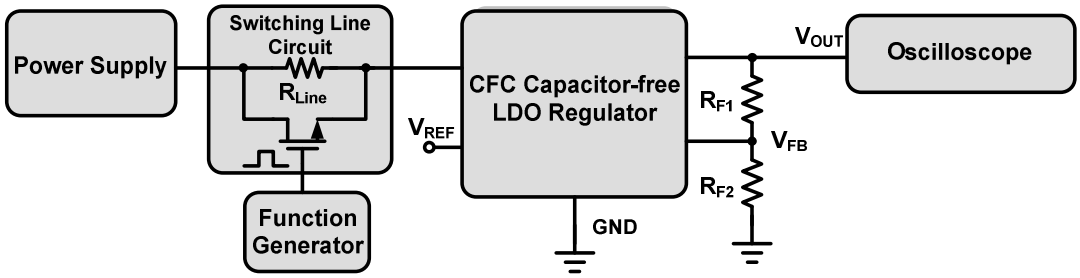


Fig. 70. Line performance tests of CFC Capacitor-free LDO Regulator.

5.1.2 Measurement Results

The measurement results of CFC capacitor-free LDO regulator will be demonstrated in this section.

The load parameter testing is under the condition with supply voltage 3V and load current ranged from 50μA to 100mA. The measured load regulation is about 20μV/mA. The load transient response from 50μA to 100mA is shown in Fig. 71. The output voltage variation is about 60mV with recovery time 2.5μs. The load transient response from 100mA to 50μA is shown in Fig. 72. The output voltage variation is about 80mV with recovery time 4μs.

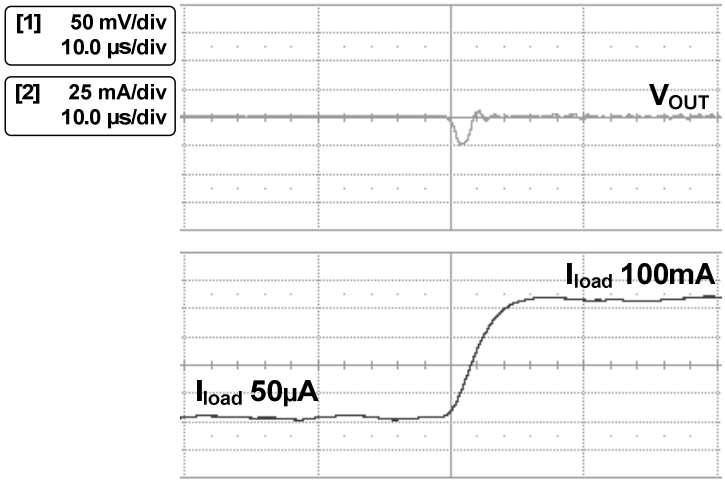


Fig. 71. Measured load transient response from 50μA to 100mA at Vin 3V.

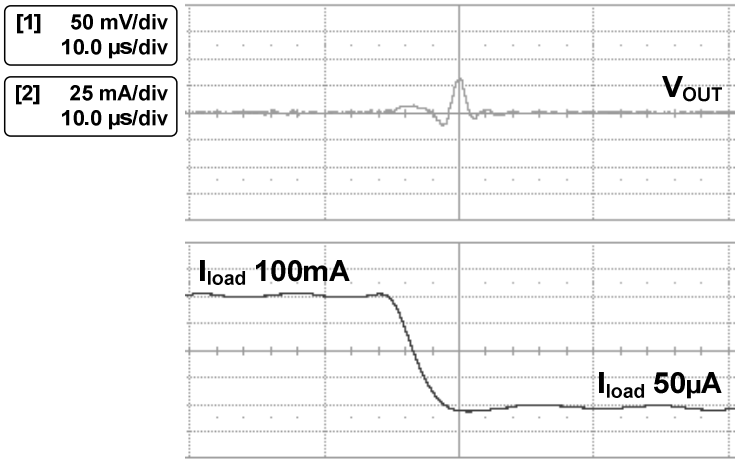


Fig. 72. Measured load transient response from 100mA to 50μA at Vin 3V.

The line parameter testing is under the condition with supply voltage ranged from 3V to 5V and load current 100mA. The measured line regulation is about 3.3mV/V. The line transient response from 3V to 5V within 5μs is shown in Fig. 73. The output voltage variation is about 90mV. The line transient response from 5V to 3V within 5μs is shown in Fig. 74. The output voltage variation is about 110mV.

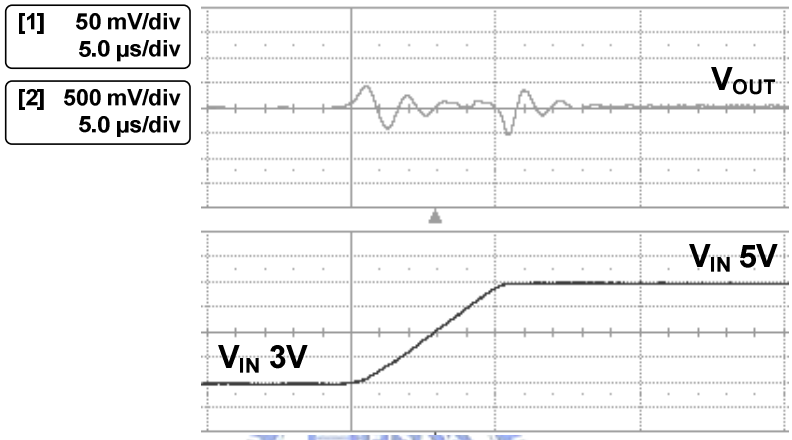


Fig. 73. Measured line transient response from 3V to 5V at load current 100mA.

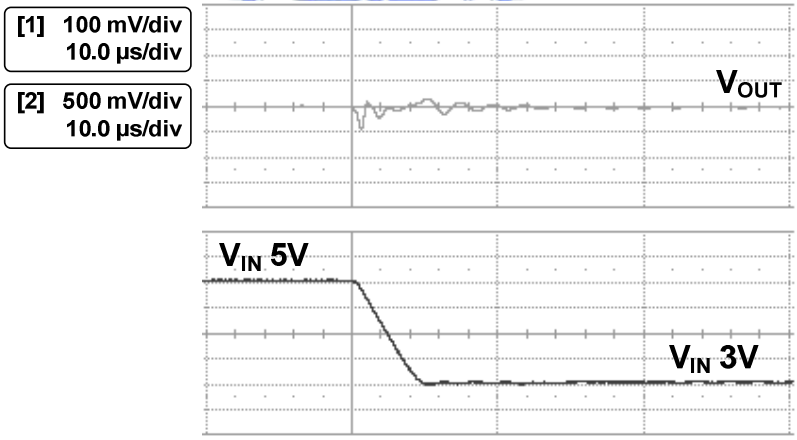


Fig. 74. Measured line transient response from 5V to 3V at load current 100mA.

The measurement results of CFC capacitor-free LDO regulator are summarized in TABLE X. The supply voltage is ranged from 3V to 5V and the output voltage is 2.8V. The measured minimum load current is 50μA. The measured load regulation is about 20μV/mA. The measured line regulation is about 3.3mV/V.

TABLE X

MEASUREMENT RESULTS OF CFC CAPACITOR-FREE LDO REGULATOR.

	Simulation Results	*Measurement Results*	*Units*
Supply voltage	3 – 5		*V*
Output voltage	2.8		*V*
Load range I_{Load}	50μ-100m	50μ-100m	*A*
Load Regulation	4 @ I_o= 50μA-100mA	20 @ I_o= 50μA -100mA	*μV/mA*
Line Regulation	2 @ V_{in}= 3~5V, I_o= 100mA	3.3 @ V_{in}= 3-5V, I_o= 100mA	*mV/V*
Settling Time	1 @ I_o= 0.05-100mA 1 @ I_o= 100-0.05mA	2.5 @ I_o= 0-100mA 4 @ I_o= 100-0mA	*μs*
Voltage variation	89 @ I_o= 0.05-100mA 98 @ I_o= 100-0.05mA	60 @ I_o= 0-100mA 80 @ I_o= 100-0mA	*mV*

5.2 Conclusions

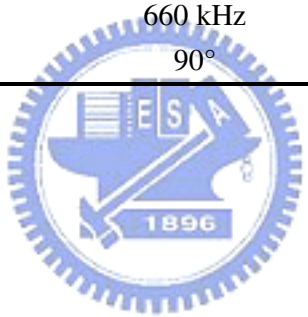
A current feedback compensation (CFC) technique for capacitor-free LDO regulators with adaptively adjusting the phase margin is proposed in this thesis. CFC technique can adaptively adjust the phase margin for achieving better transient response than that with variant phase margin at different load current conditions. With proposed technique, the minimum load limitation is greatly reduced to 50μA. Meanwhile, the overall loop bandwidth can be designed largely with proper phase margin to achieve fast transient response. Besides, CFC technique can have high PSRR bandwidth with compatible compensation capacitors compared to the Q-reduction technique. This capacitor-free linear regulator is fabricated by TSMC 0.35μm2P4M CMOS process with compensation capacitor only 5pF and 1.5pF, transient response time smaller than 4μs.

Comparisons between different capacitor-free LDO are shown in TABLE XI. The DFCFC capacitor-free LDO proposed in [17] has minimum load restriction and the phase margin is 90 degree. The minimum load limitation of Q-reduction capacitor-free LDO proposed in [18] is reduced to 100μA. But the phase margin is still 90 degree, and the PSR performance is degenerated by additional compensation capacitor. Without proposed

compensation, i.e. single Miller compensation, the minimum load is about 1mA with variable phase margin. If the minimum load must be down to 50 μA, the compensation capacitor must be up to 20μF and the second stage transconductance must be designed smaller instead. Finally, the minimum load of CFC capacitor-free LDO is down to 50 μA without using too large additional capacitor. And the phase margin is 60 degree to achieve faster response.

TABLE XI
COMPARISONS BETWEEN DIFFERENT CAPACITOR-FREE LDO REGULATORS

	DFCFC [17]	*Q-Reduction [18]*	*This work w/o CFC*	*This work*
Compensation Capacitor	$C_{m1}+C_{m2}$=5pF	$C_{m1}+C_{cf}$=6pF	C_m =5pF	C_m+C_a=6.5pF
Minimum load	--	100 μA	1 mA	50 μA
UGF	--	660 kHz	850 kHz	850 kHz
Phase Margin	90°	90°	85°-63°	60°



5.3 Future work

Although a current feedback compensation technique is proposed in this thesis, the capacitor-free LDO still cannot be operated in no-load condition with smaller compensation capacitor. There may be another way to achieve no-load capacitor-free LDO design without too large compensation capacitor or too complex circuit topology. Meanwhile, a high PSRR bandgap is required for capacitor-free LDO. Since the PSR of LDO system is dominant by PSRR of bandgap, how to design a high PSRR bandgap without using too large off-chip capacitor for reference voltage is essential.

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