Chapter 4

Reducing AC Power Consumption by Three-Dimensional Integration of Ge-On-Insulator CMOS on 1-Poly-6-Metal 0.18-μm Si MOSFETs

4.1 Introduction

The relentless scaling down of transistor dimensions, leading to increasing circuit densities, results in the power consumption becoming the major limitation for integrated circuits (ICs). The gate leakage current in the ultra-thin gate dielectric of individual transistors is the major source of the DC power consumption. However, by using high-κ oxynitride and metal-oxides this issue can be addressed [4.1]-[4.9]. The AC power in the backend interconnects ($CV^2f/2$) then becomes an important power consumption issue, particularly when both the operation frequency and interconnect density increases. For example, operation frequencies can be as high as 10.6 GHz (for Ultra-Wide Band access circuits) when using the high integration density and 9-Metal interconnect layers available in the 90-nm technology node. Although this AC power consumption has been extensively discussed (e.g. panel session of *Int'l Electron Devices Meeting (IEDM)*, 2003), no clear solution or approach is evident. Here, we suggest that three-dimensional (3D) integration can resolve this AC power consumption issue. Electro-Magnetic (EM)

simulations, using IE3D software, suggest that both the AC power consumption and maximum operation frequency can be improved by integrating an additional IC layer. However, the key issue for 3D integration is how to create a high performance upper layer on the CMOSFETs without degrading lower layer devices and interconnects [4.10]-[4.12]. This challenge also involves the high thermal budget (>1000^{o}C RTA) requirement for ion implant activation in the Si CMOSFETs, the low thermal budget required for the lower layer shallow junction, silicide [4.4], and the backend interconnect stability. Here we demonstrate a new 3D solution, using low thermal budget (500^{o}C RTA) Ge-on-Insulator (GOI) CMOSFETs. Little performance degradation was measured in lower layer 0.18-μm 1-poly-Si-6-metal (1P6M) Si CMOSFETs [4.13]-[4.15]. In addition, the drive currents for 3D GOI n- and p-MOSFETs were more than double those of the Si control, due to higher electron and hole mobilities. The AC power consumption was reduced with little degradation of the lower layer 0.18-μm MOSFETs. This, together with the improved current drive for the GOI CMOSFETs, should find application in future high frequency, large integration density ICs.

4.2 Experimental Procedure

To calculate the AC power consumption in multiple layered interconnects, we used

the 3D EM method reported previously [4.16]-[4.20] rather than analyzing the complicated parasitic circuits. The parasitic elements causing AC power consumption were treated using the 3D EM software, IE3D, which was calibrated through well-matched measured and modeled data for the RF signal loss and power loss [4.16]-[4.20]. The reason using 3D EM simulator is to include the RF loss effect in low resistivity (10 Ω-cm) Si substrate [4.16]-[4.20]. An isolation thickness >100-μm into high loss Si substrate is required to reduce the loss [4.16]-[4.20], which makes the 3D calculation more accurate than 2D case. The 3D GOI integration [4.5]-[4.7] was created using H^+ implantation of the Ge wafer, at a 5×10^{16} cm^{-2} dose and 200-keV energy, and depositing 100 nm PECVD SiO_2 on both the Ge and 1P6M 0.18-μm CMOS wafers, O_2 plasma enhanced bonding, a "smart cut" [4.21]-[4.22]at 300°C, an extended 400°C annealing for 0.5 hour and slight polishing [4.5]-[4.7], [4.21]-[4.24]. The p- and n-GOI MOSFETs were then formed using a high-κ $LaAlO_3$ gate dielectric deposited on the GOI [4.21]-[4.22], followed by PVD deposited IrO_2 and IrO_2/Hf dual metal gates [4.5]-[4.6], self-aligned B^+ and P^+ ion implantation and a 500°C RTA. A schematic diagram (Fig. 4-1(a)) shows the 3D integration and the features described above. As shown in Fig. 4-1(b), the 3D integration can increase the circuit density and also reduce the interconnect distance by 1/2 by folding the 2D IC into 3D. For the multi-level parallel interconnect

lines, the AC power is $Cv^2f/2$, $Li^2f/2$, and $i^2Rf/2$ for the parasitic C, L, and R circuits.

4.3 Results and discussion

Fig. 4-2(a) shows the equivalent circuit of the parasitic interconnect lines as a distributed circuit with 3D parasitic C, R, and L components. It is noticed that although the active MOSFETs consume AC power, the dominant dynamic power consumption is from the backend interconnects. The large parasitic effect in interconnect also dominates the circuit delay rather than the active MOSFETs. In addition, the AC power in MOSFETs can further be reduced by using the Si-on-Insulator (SOI) wafer. Therefore, we focus the AC power consumption by backend interconnect only. Because of the distributed nature of the circuit and the complicated parasitic effects, it is difficult to extract exact values for the parasitic R, L, and C components and to solve the AC power consumption correctly. Since circuit theory relies on Kirchhoff principles derived from the Maxwell's equations, we have calculated the AC power consumption directly using an EM wave approach. The EM software has the added capability of giving a 3D solution of the complicated structure depicted in Fig. 4-1(a). Fig. 4-2(b) shows the calculated S-parameters of 1-mm long parallel lines having a separation of 0.5-μm (close to the metal-to-metal separation of the 0.18-μm technology). The EM calculation is based the interconnect structure in Fig. 4-1(a), where the thicknesses of backend interconnect for

Field-Oxide (FOX), Inter-Layer Dielectric (ILD) and Inter-Metal Dielectric (IMD, from IMD1 to IMD5) are 0.35, 0.7, and 1.4-μm, respectively. The metal thickness for respective M1-M5 and M6 are 0.5 and 1.0-μm. The equivalent circuit simulation is also shown for comparison. The reasonably good match between the EM calculation and the equivalent circuit simulation justifies using the EM method to calculate the AC power consumption of the 3D parallel lines. The slight mismatch between is most probably due to the distributed nature of parallel lines. This is difficult to simulate using a simple lumped circuit model. The AC power consumption can be calculated by $1-|S_{21}|^2-|S_{11}|^2$ rather than solving the complicated circuit, and adding the power consumption of $Cv^2f/2$, $Li^2f/2$, and $i^2Rf/2$ in each parasitic C, L, and R.

The signal coupling loss is severe for parallel lines at high frequency. Fig. 4-3(a) shows the measured S_{21} signal coupling loss of 1-mm long parallel lines, with various spacings from 0.5 to 8-μm using M6. The maximum allowed 3 dB coupling (50% signal loss to the second line) limits the highest IC operation frequency, using high density parallel lines. The operation frequency increases with increasing line separation and thus limits the interconnect line separation and density. For the 1 mm long line with a 0.5-μm separation, a maximum operating frequency of <20 GHz was obtained, according to the technology data provided by the foundry. From this result, further reducing the

interconnect metal distance in the 90 nm node is not useful for high frequency circuits. The power loss of the 1-mm long 0.5-μm spaced parallel lines is also shown in Fig. 4-3(b). The power loss is more severe than the coupling loss of parallel lines shown in Fig. 4-3(a). For 1-mm long parallel lines with the 0.5-μm gap, the maximum frequency allowed for 3 dB AC power consumption is 20 GHz and can be increased to 40 GHz if 2 layers are used in the 3D integration. A much larger improvement can be achieved using 3 layers (2 layers in GOI plus a single one from the Si CMOSFETs). This reduces the AC power consumption to ≤0.25 dB at 40 GHz, since it is related to parasitic effects as well as being nonlinear with the line length.

The results above indicate that the 3D integration is effective in reducing the AC power consumption. However, the main challenge is how to realize such 3D integration with little performance degradation of the Si devices in lower layer. Figs. 4-4(a) and 4-4(b) show a plan view image of the 1P6M 0.18 μm MOSFETs before and after the 3D GOI formation respectively, where the GOI was formed on the 0.18 μm Si devices by using the “smart-cut” techniques [4.21]-[4.22] described above. The dark area on the pad after bonding is due to the selectively bonded Ge. This is evident from the surface profile shown in Fig. 4-5, where there is no Ge beyond the metal pads. This is related to the top M6 (2 μm thick) without planarization, where the Ge bonding can only be attached to

these higher M6 metal pads. A Ge thickness of 1.6 μm was measured from the surface profile and is consistent with previous H^+ implantation and smart cut GOI [4.21]-[4.22]. Although void free bonding was achieved previously [4.6]-[4.7] and selective bonding was formed in this work, further large size void and defect-free bonding needs to be demonstrated. However, such large scale bonding has been used for 12-inch SOI wafer manufacture, which may not cause the problem for large size GOI bonding on Si IC.

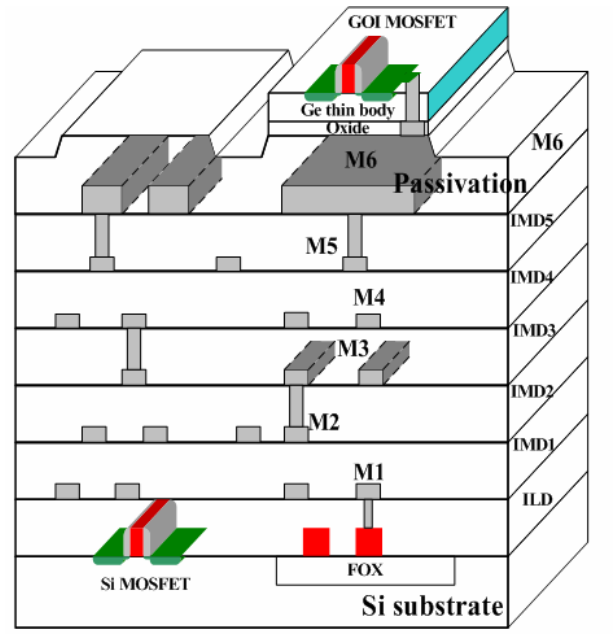
Figs. 4-6(a) and 4-6(b) show cross-sectional Transmission Electron Microscopy (TEM) views of the bottom 1P6M 0.18μm Si MOSFETs and the top GOI, respectively. After the 500°C RTA thermal cycle for GOI CMOSFET fabrication, no observable degradation can be seen in the cross-sectional TEM of the lower layer 0.18-μm Si MOSFETs. This is due to the low RTA process temperature of 500°C for the GOI CMOSFETs. The cross-sectional TEM shows a dislocation-free, smooth Ge/SiO_2 interface, similar to our previous GOI results [4.5]-[4.7]. The top Ge layer thickness of 1.6 μm is the same as that measured from the surface profile.

We measured the characteristics for the lower layer 1P6M 0.18 μm Si MOSFETs, before and after the thermal cycle for 3D GOI fabrication, to determine if there was any degradation. Figs. 4-7(a) and 4-7(b) show the I_d-V_d and I_d-V_g characteristics of the bottom layer 0.18-μm Si MOSFETs, where a comparable sub-threshold swing and off-state

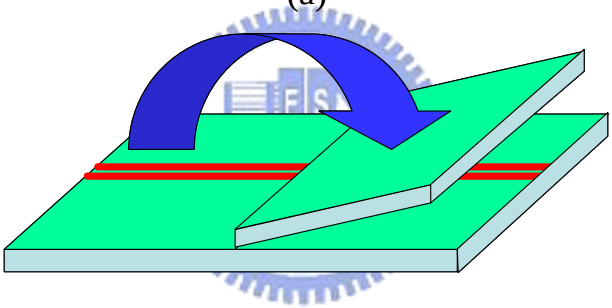
current were measured. Little degradation was observed even after the 500^{o}C RTA required for activating the source and drain ion implantation of the top GOI CMOSFETs.

4.4 Conclusion

From our EM calculations, calibrated by well matched simulation and experiment data, we have shown that the AC power consumption in a circuit can be significantly reduced using 3D integration. The 3D integration was realized by low temperature GOI process technology, which produced little degradation of the lower level Si 0.18–μm devices. The self-aligned process is fully compatible with current VLSI technology.

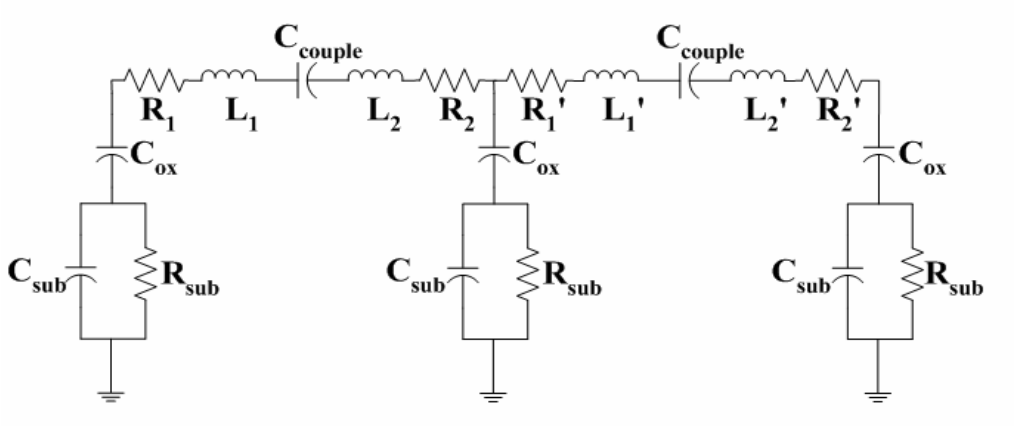


(a)

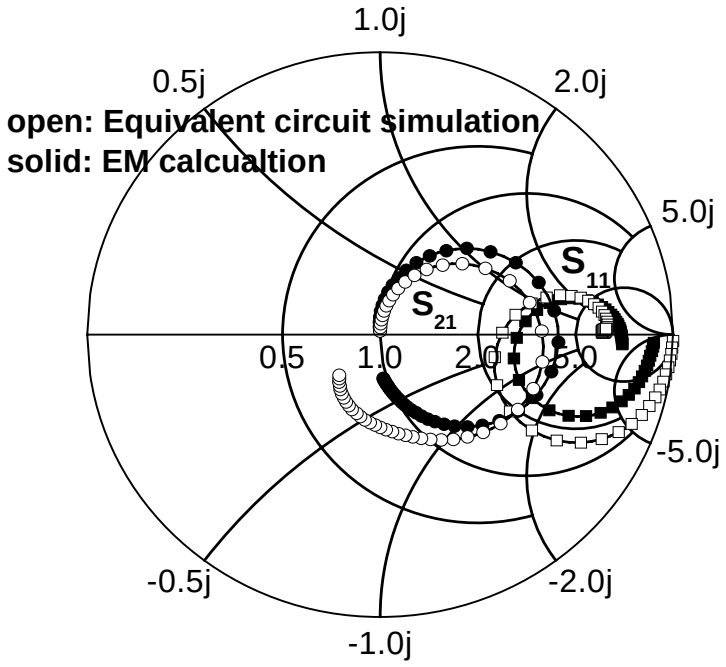


(b)

Fig. 4-1 (a) Schematic of the 3D VLSI showing the lower layer Si MOSFETs, multi-level (1P6M) parallel interconnect lines and top layer GOI CMOS. (b) The equivalent folding 2D IC to form the 3D IC.

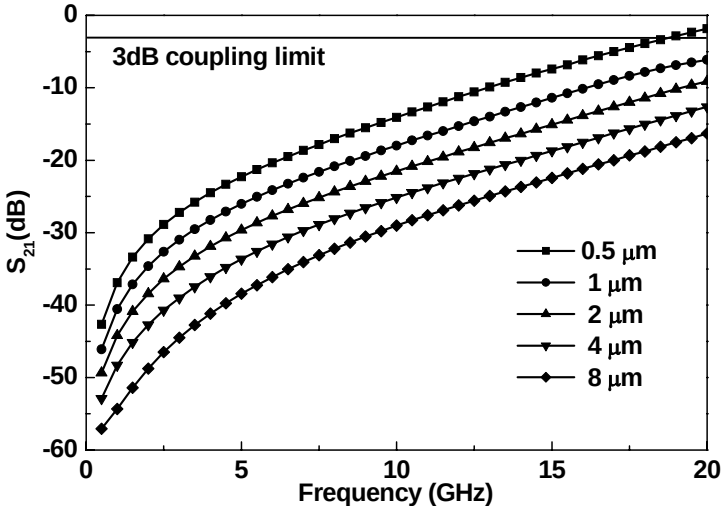


(a)

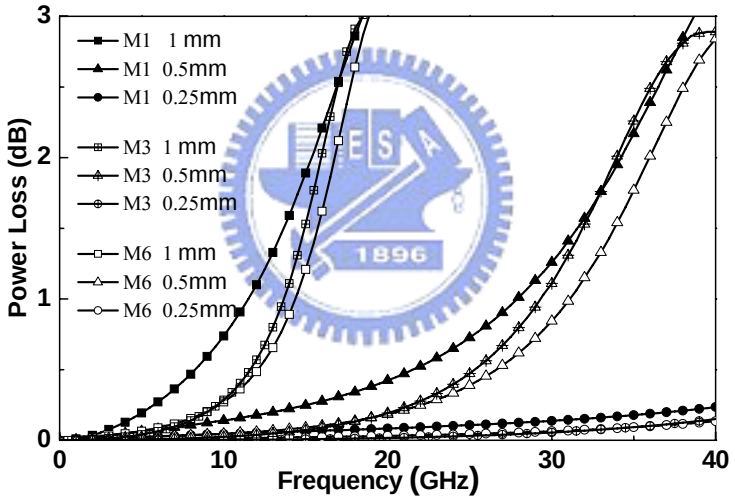


(b)

Fig. 4-2 (a) The equivalent circuit of the interconnect lines of the 0.18-μm MOSFETs. (b) The simulated and IE3D EM calculated S_{21} and S_{11} for 1-mm long, 0.5-μm spaced, parallel lines.

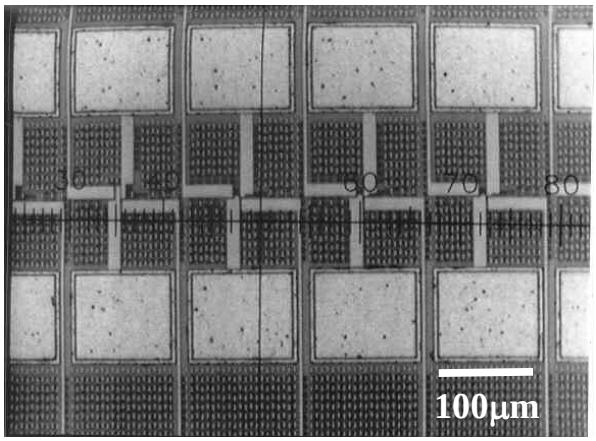


(a)

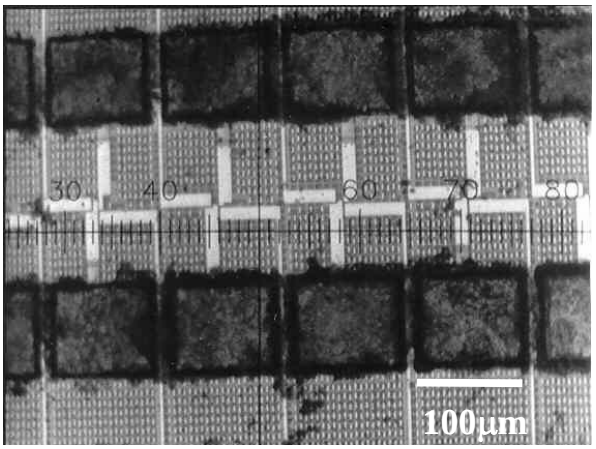


(b)

Fig. 4-3 (a) Measured S_{21} coupling of 1-mm long two parallel lines with various spacings from 0.5- to 8-μm using M6, and (b) calculated power loss of 0.5-μm spaced, parallel lines of different lengths.



(a)



(b)

Fig. 4-4 Images of 0.18-μm MOSFETs with probing pads (M6 and 2-μm thickness) (a) before and (b) after the GOI bonding. The “dark” area on the pad after bonding is due to the selectively bonded Ge by “smart cut”.

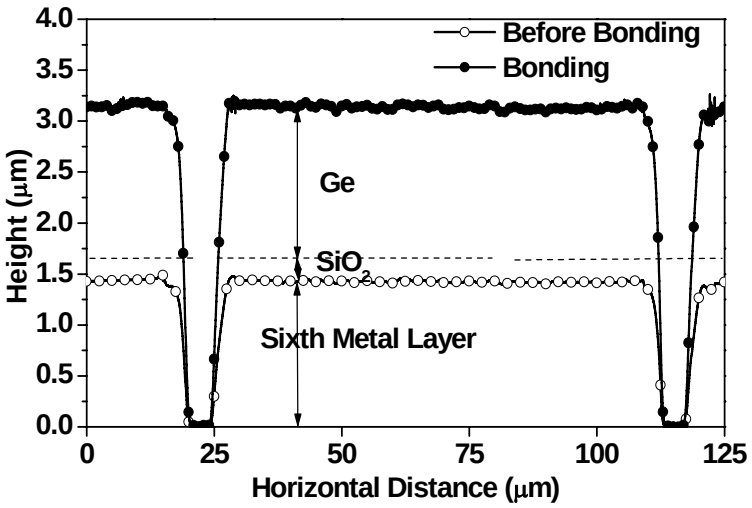
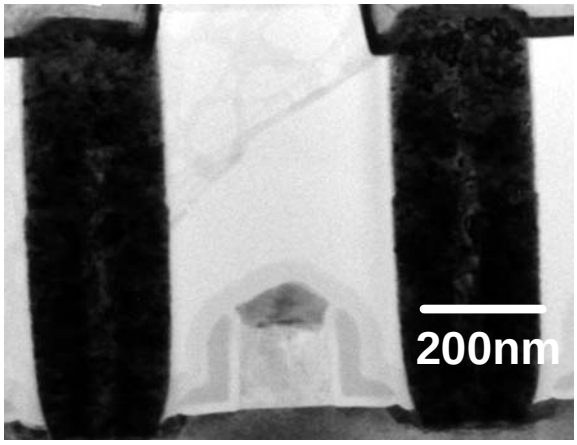
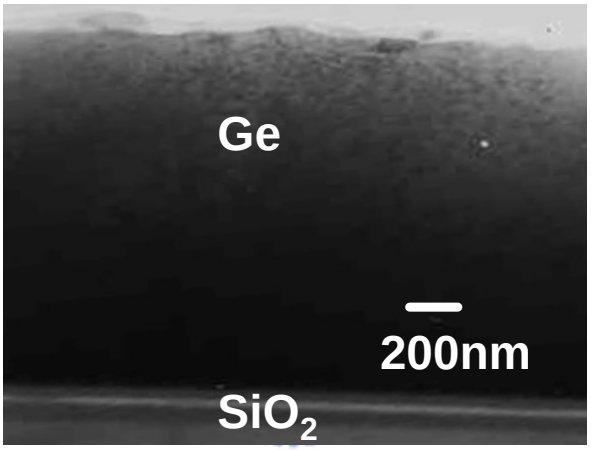


Fig. 4-5 The surface profiles of the fabricated wafer, before and after GOI bonding.

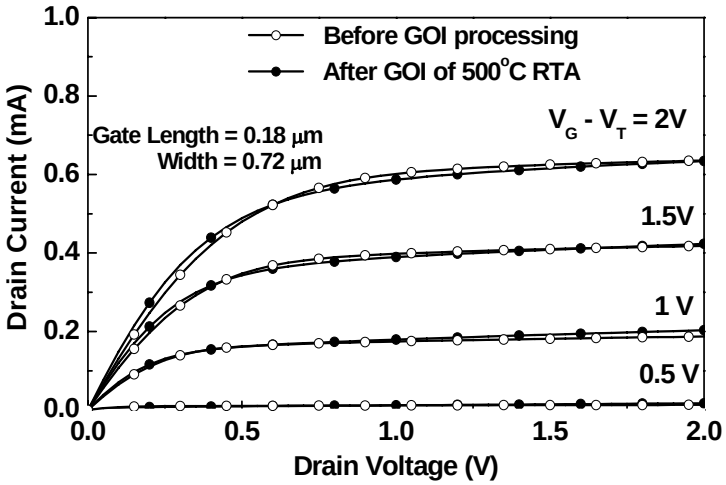


(a)

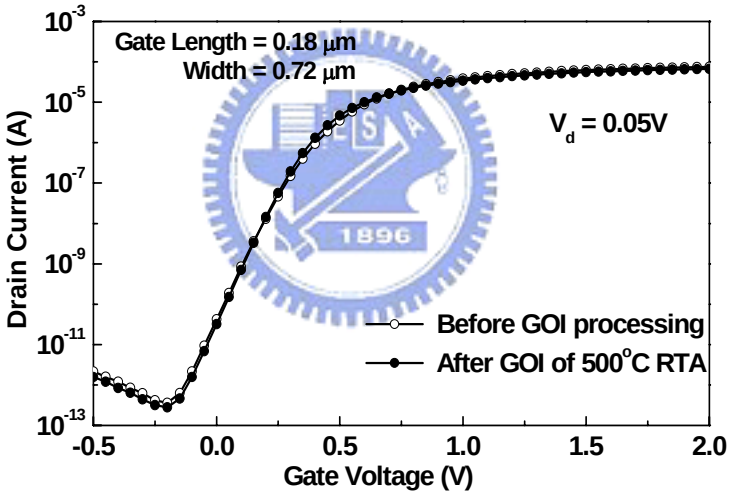


(b)

Fig. 4-6 Cross-sectional TEMs of: (a) the lower 0.18-μm MOSFET and (b) the selectively bonded and smart cut Ge-on-Insulator on a pad. The Ge/SiO_2 interface appears to be dislocation free and smooth.



(a)



(b)

Fig. 4-7 The Ge/SiO_2 interface appears to be dislocation free and smooth. (a) The I_d -V_d and (b) the I_d -V_g characteristics of lower layer Si 0.18-μm MOSFETs, before and after GOI bonding.