Chapter 5

3D Metal-Gate/High-κ/GOI CMOSFETs on 1-Poly-6-Metal 0.18-μm Si Devices

5.1 Introduction

One of the biggest challenges for VLSI technology is the AC power consumption [5.1] caused by the interconnect parasitic capacitance ($Cv^2f/2$), which becomes a major limit for VLSI ICs beyond the implementation of metal-gates and high-κ nano-CMOS to solve the DC power in gate leakage [5.2]. Increasing operational frequency (f) of circuits with denser interconnects makes the AC power consumption even worse. A potential solution is three-dimensional (3D) integration which can effectively shorten the interconnect distances and therefore reduce the AC power consumption. Such 3D integration can also provide a way to increase the IC density [5.3] (equivalent to scaling down) once the quantum-mechanical scaling barrier is reached. However, the technology challenges are how to realize 3D ICs [5.4]-[5.6] with a low thermal budget and small impact on lower multiple interconnect and CMOSFET layers. Using the inherent low temperature process of the Ge-on-Insulator (GOI) technology [5.7]-[5.13], we have integrated self-aligned IrO_2-IrO_2/Hf dual-gated/$LaAlO_3$/GOI CMOSFETs on 1-Poly-6-Metal (1P6M) 0.18-μm Si devices. The process yields GOI CMOSFETs with

high hole and electron mobilities, without degrading the underlying Si devices. This approach is promising for future high performance VLSI ICs. However, unlike SiO_2, high-κ gate dielectrics exhibit significant charge trapping, causing the threshold voltage (V_t) to shift under applied voltage and raised temperature conditions. Such Bias-Temperature-Instability (BTI) [5.14], [5.15]-[5.16] of V_t with time creates a severe reliability concern for ICs, where the use of high-κ gate dielectrics is more problematic than oxynitrides in devices [5.17]-[5.18]. In addition to the charge trapping, the poor BTI in high-κ CMOSFETs may be related to impurity diffusion from the gate [5.19], and from the use of processing water and/or hydrogen annealing after device fabrication [5.17]-[5.18]. In this paper we report the BTI of three-dimensional (3D) self-aligned metal-gate/high-κ/Germanium-on-insulator (GOI) CMOSFETs and compare the results with those from control Si devices.

5.2 Experimental Procedure

The self-aligned 3D GOI CMOSFETs were formed by depositing 200-nm PECVD oxide on both H^+-implanted Ge (5×10^{16} cm^{-2} dose at 200 KeV) and 1P6M 0.18-μm MOSFETs wafers, O_2 plasma enhanced bonding, a 300 ^oC "smart cut", 400^oC annealing for 0.5 hour, and then slight polishing [5.7]-[5.9], [5.12]-[5.13]. Both (100) and (110) n-Ge and (100) p-Ge substrates were used for the 3D GOI. The $LaAlO_3$ gate

dielectric was deposited by PVD from a $LaAlO_3$ source (κ = 25.1) followed by 400^oC oxidation [5.12]-[5.13]. Then a 150-nm IrO_2 or 150-nm IrO_2/15-nm Hf gate was deposited on the $LaAlO_3$ by PVD for the p- or n-MOSFETs respectively. Low work-function Hf was used for n-MOSFETs, similar to fully silicided NiSi:Hf/Al_2O_3 devices [5.12]-[5.13]. The IrO_2/$LaAlO_3$ p-MOSFETs or IrO_2/Hf/$LaAlO_3$ n-MOSFETs was formed by self- aligned 25 keV boron or 35 keV phosphorus implantation, followed by a 500^oC RTA.

5.3 Results and discussion

Fig. 5-1 plots the flat band voltage (V_{fb}) as a function of different EOT thickness of $LaAlO_3$ gate dielectric with IrO_2 and IrO_2/Hf gates after 550^oC-950^oC RTA. The Ir gate on $LaAlO_3$/Si MOS capacitor was also measured as reference, where the low temperature 550^OC RTA was used to minimize the possibility of Ir oxidization by the residual moisture or oxygen under a nitrogen ambient. It is noticed that the extracted work-function for IrO_2 on $LaAlO_3$ is 5.1 eV and the increasing RTA temperature from 750 to 950^oC only cause a small work-function reduction. In addition, the work-function is reduced to 4.4 eV by adding 15nm-Hf on $LaAlO_3$.

Fig. 5-2(a) shows the comparison of gate dielectric leakage current of IrO_2/$LaAlO_3$ and Ir/$LaAlO_3$ capacitors as a function of V_g-V_{fb}. The gate leakage current is ~one order

of magnitude lower using IrO_2 than Ir. Similar lower dielectric leakage current is also reported in ferro-electric capacitors [5.20], which is most probably due to smaller metal diffusion in more thermal-dynamic stable IrO_2 than pure metallic Ir. Fig. 5-2(b) shows the J_g-V_g curves of IrO2/Hf or IrO2 on Si or GOI MOSFETs using LaAlO3 gate-dielectrics. The LaAlO3 gate-dielectrics can minimize the residual moisture or oxygen under a nitrogen ambient from 750 to 950^{o}C and only cause J_g-V_g curves a small variable.

Figs. 5-3(a) and 5-3(b) show the C-V characteristics of self-aligned of IrO2/Hf or IrO2 on Si or GOI CMOSFETs using LaAlO3 gate-dielectrics. The same inversion and accumulation capacitance value indicates the metal-like IrO_2 gate without gate depletion. An EOT thickness of 1.4 nm is obtained from the measured capacitance for IrO_2 or IrO2/Hf gates on $LaAlO_3$/Si CMOSFETs.

Figs. 5-4(a) and 5-4(b) show I_d-V_d characteristics for a family of /V_g-V_t/ values of 3D $LaAlO_3$/GOI CMOSFETs and 2D $LaAlO_3$/Si CMOSFETs with metal-like IrO_2/Hf and IrO_2 dual gates. An EOT of 1.4-nm was obtained from the *C-V* measurements. To the best of our knowledge these good results are the first demonstration of 3D integration, using a process compatible with current VLSI technology, which does not degrade the lower layer MOSFETs. The (110) p-MOSFETs had higher drive current than the (100) devices - such hole mobility enhancement has been reported in the literature [5.21].

Figs. 5-5(a) and 5-5(b) show $I_d - V_g$ characteristics of 3D $LaAlO_3$/GOI CMOSFETs and 2D $LaAlO_3$/Si CMOSFETs with metal-like IrO_2/Hf and IrO_2 dual gates. The threshold voltage of ~0.25V is measured in (110)Ge, reflecting high work-function and little Fermi-level pinning. Future work, we must reduce the work-function of n-MOSFETs to show lower threshold voltages.

The IrO_2/Hf/$LaAlO_3$/GOI n-MOSFETs have a peak electron mobility of 357 cm^2/Vs and values close to universal electron mobility at higher E_{eff} (Figs. 5-6(a)). Peak hole mobilities of 181 and 234 cm^2/Vs were measured for the IrO_2/$LaAlO_3$/GOI p-MOSFETs on (100) and (110) substrates, respectively(Fig. 5-6(b)). These hole mobilities are higher than universal mobility values. The 136 and 156 cm^2/Vs values at E_{eff} of 1 MV/cm are 2.2- and 2.5-times higher than that of the universal hole mobility. Such mobility enhancement reflects the smaller Ge effective mass than Si [5.11].

In Figs. 5-7(a) and 5-7 (b) we show the ΔV_t with BT stress time at 10 MV/cm and 85^{o}C for the 3D GOI and control 2D Si p- and n-MOSFETs, respectively. After 1 hour of BT stress, the ΔV_t of 3D metal-gate/high-κ/GOI CMOSFETs was -30 and 21 mV for the p- and n-MOSFETs respectively, which is slightly larger than the control 2D Si CMOSFETs. These results are comparable with TaN/HfAlO [5.19] and poly-Si/HfSiON [5.22] devices, suggesting that the major BTI issue is related to the metal-gate/high-κ

dielectric rather than the low-temperature processed 3D GOI. The observed BTI is much better than that for TiN/HfO_2 devices [5.22], indicating that the strong bonding of AlO in $LaAlO_3$ most probably plays a key role in the BTI improvement. This is also consistent with the better BTI for TaN/HfAlO devices compared with those using TiN/HfO_2[5.19]. In this case the improvements were at the expense of a lower κ for HfAlO compared with HfO_2.

We measured the BTI at other gate electric fields to estimate the 10-year lifetime. Fig. 5-8 shows the lifetime ($|\Delta V_t|$=50 mV) as a function of $|V_{gs}|$ for various metal-gate/high-κ MOSFETs, BT stressed at 85°C. The extrapolated $V_{max\text{-}10years}$ values are -1.2 and 1.4 V for p- and n-MOSFETs, respectively. These values can meet the BTI reliability requirements at 1 V operation, with a 20% safety margin. Note that the $V_{max\text{-}10years}$ value from the time-to-breakdown (t_{BD}) is much higher than that from BTI measurements, and is an over-estimate of the reliability of the high-κ CMOSFETs. The high $V_{max\text{-}10years}$ for BTI in these metal-gate/high-κ 3D GOI and control 2D CMOSFETs is related the absence of impurities in gate [5.19], the presence of a good IrO_2 diffusion barrier, and the avoidance of hydrogen annealing or process water [5.17]-[5.18] in the device fabrication.

5.4 Conclusion

We have fabricated the [IrO_2-IrO_2/Hf]/$LaAlO_3$/GOI CMOSFETs on 1P6M 0.18-μm Si devices. At the 1.4-nm EOT, the peak electron and hole mobilities are 357 and 234 cm^2/Vs, the hole mobility being 2.5-times higher than the universal mobility at 1 MV/cm E_{eff}. Good NBTI and PBTI performance was shown by the relatively small $|\Delta V_t|$ of -30 and 21 mV, and the high extrapolated $V_{max\text{-}10years}$ value of -1.2 V under 10 MV/cm, 85°C stress. These high performances self-aligned 3D metal-gate/high-κ/GOI devices and their successful 3D integration are promising for future VLSI. 3D GOI CMOSFETs with full process compatibility with current VLSI lines.

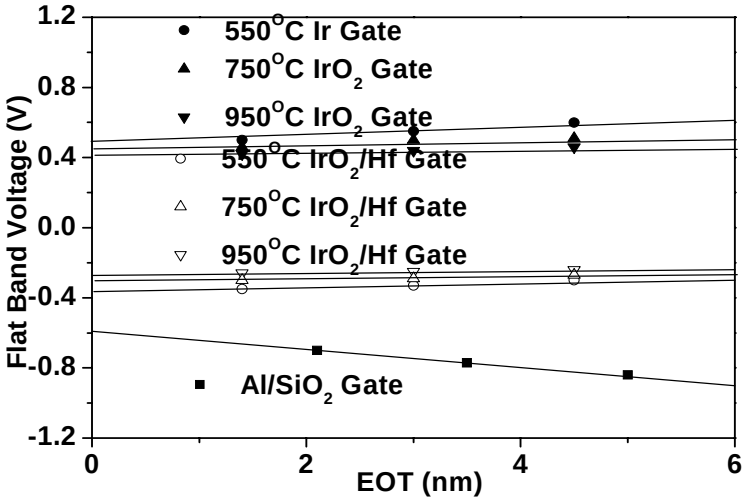
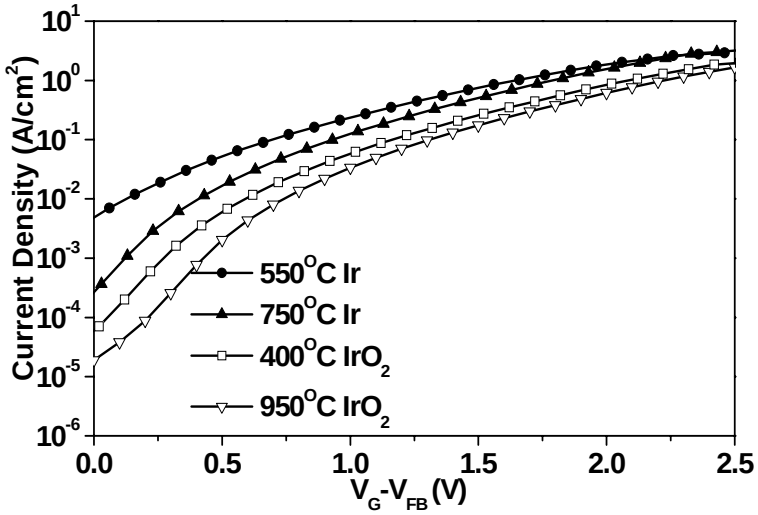
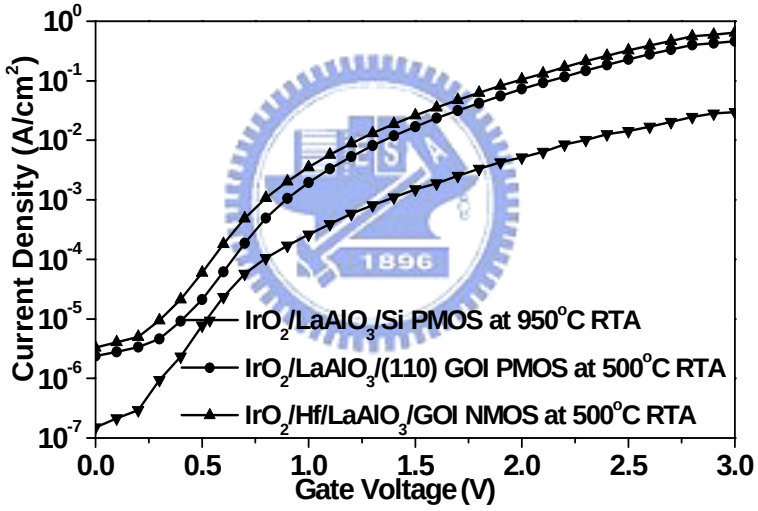


Fig. 5-1 The V_{fb} and EOT plot for IrO_2 and IrO_2/Hf gates on $LaAlO_3$/Si after different RTA condition from 550 to 950°C.

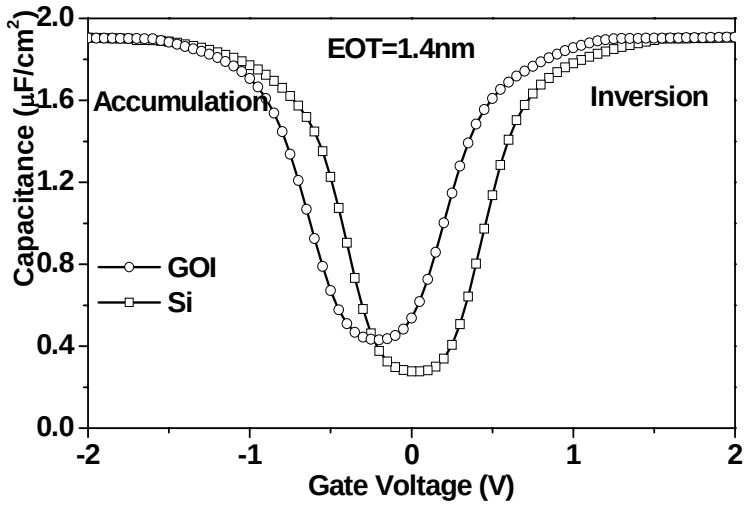


(a)



(b)

Fig. 5-2 (a) J_g-V_g curves of IrO_2/$LaAlO_3$/Si MOSFETs. The J_g is ~10^4X-10^5X lower than SiO_2 at 1.4nm EOT due to the uniform $LaAlO_3$ after 950°C RTA. (b) The J_g-V_g curves of IrO_2/Hf or IrO_2 on $LaAlO_3$ MOSFETs on Si or GOI at 1.4nm EOT with different RTA temperature.



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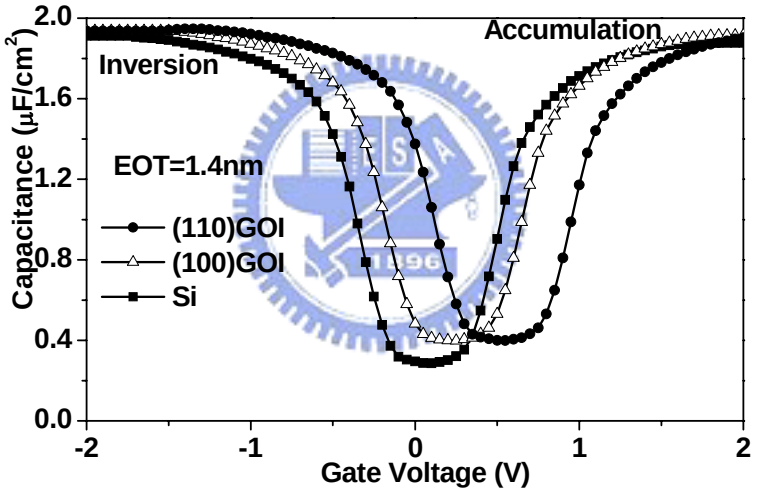
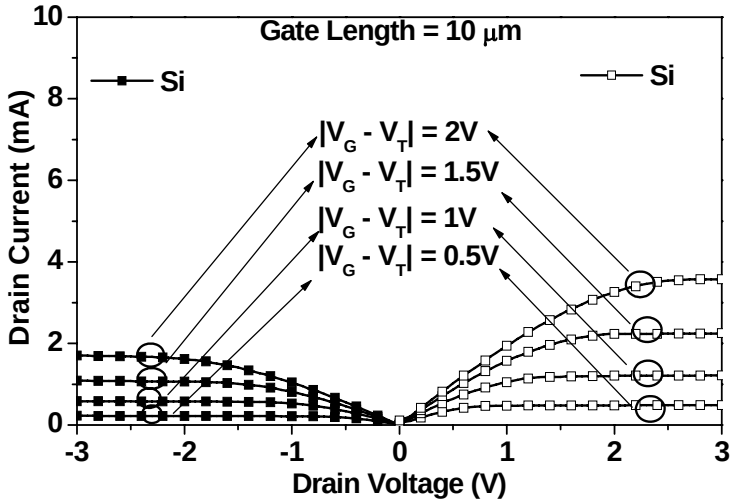


(b)

Fig. 5-3 The C-V characteristics of (a) IrO_2/Hf on $LaAlO_3$ gate-dielectrics n-MOSFETs on Si and GOI. (b) 150nm-IrO_2 on $LaAlO_3$ gate-dielectrics p-MOSFETs on Si and GOI.



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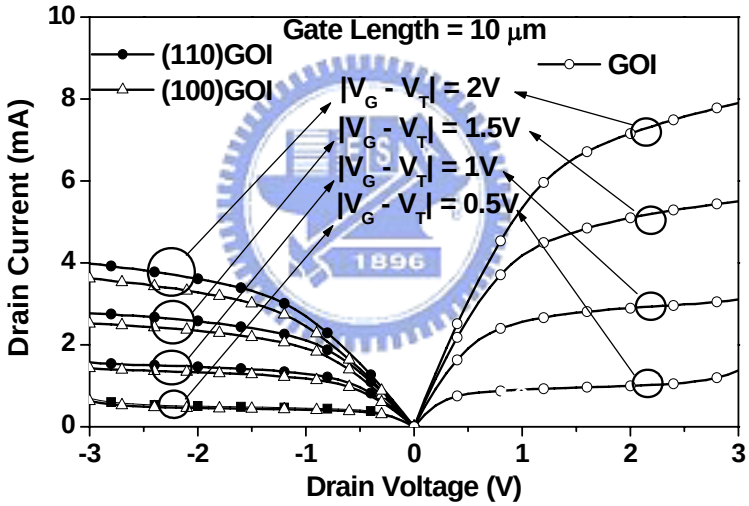
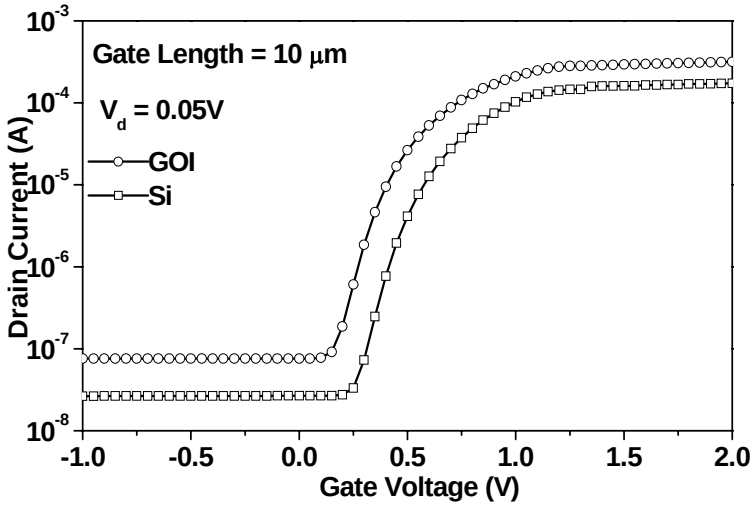


(b)

Fig. 5-4 The I_d-V_d characteristics of (a) IrO_2/Hf or IrO_2.on $LaAlO_3$ gate-dielectrics n- and p-MOSFETs on Si (b) IrO_2/Hf or IrO_2 on $LaAlO_3$ gate-dielectrics n- and p-MOSFETs on GOI.



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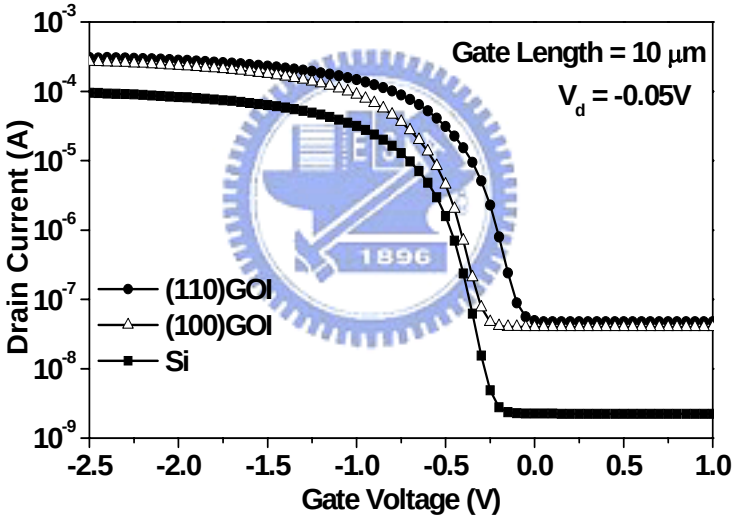
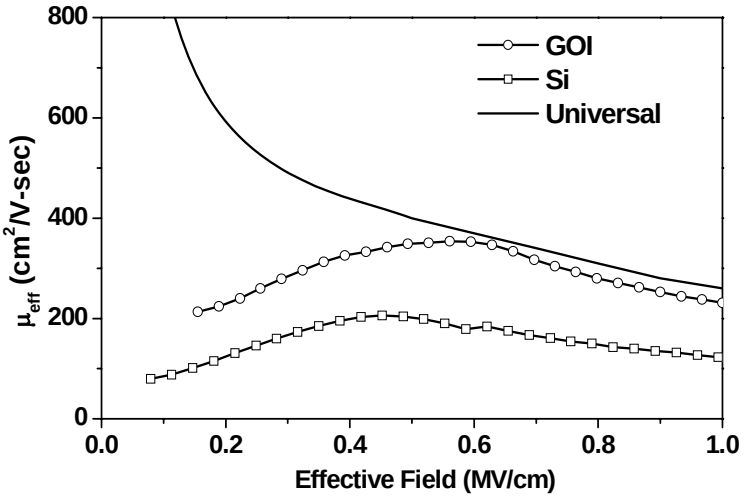
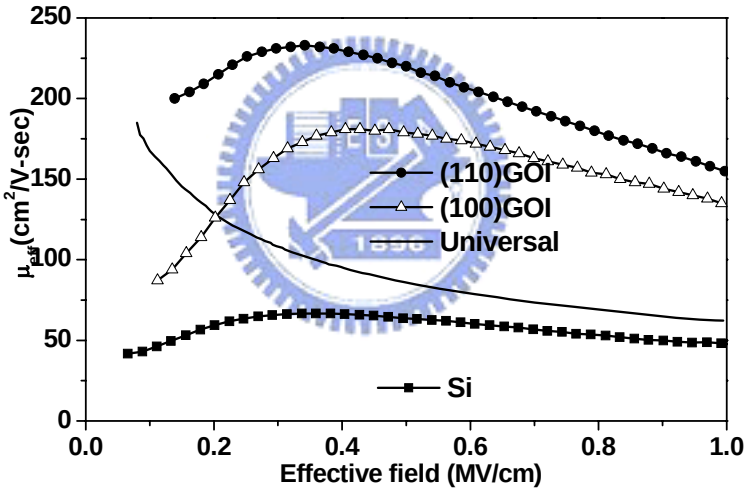


(b)

Fig. 5-5 The I_d-V_g characteristics of (a) IrO_2/Hf on $LaAlO_3$ gate-dielectrics n-MOSFETs on Si or GOI. (b) IrO_2 on $LaAlO_3$ gate-dielectrics p-MOSFETs on Si or GOI.

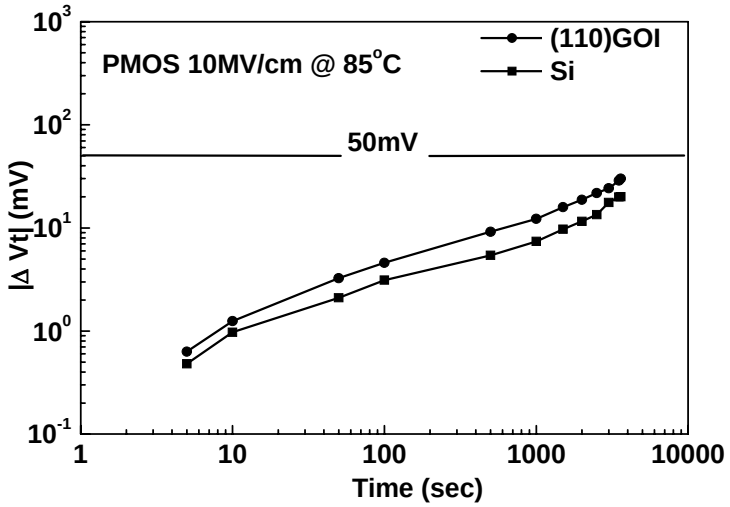


(a)

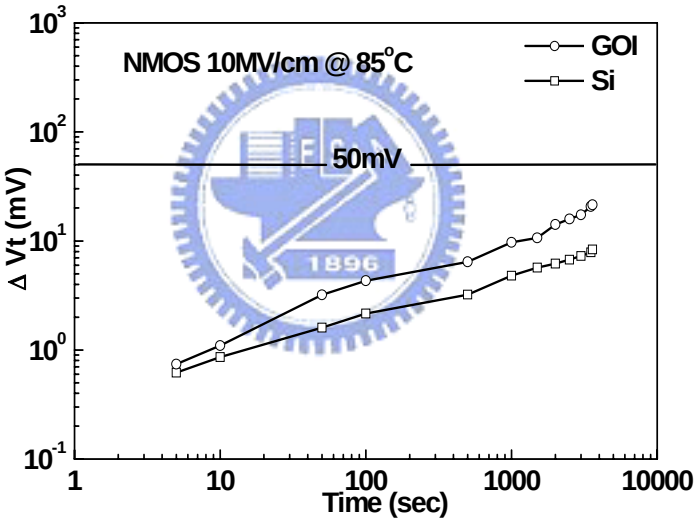


(b)

Fig. 5-6 (a) The electron mobility of IrO_2/Hf on $LaAlO_3$ n-MOSFETs on Si or GOI. (b) The hole mobility of IrO_2 on $LaAlO_3$ p-MOSFETs on Si or GOI.



(a)



(b)

Fig. 5-7 Vt shift as a function of time during (a) NBTI measurement of $IrO_2/LaAlO_3$ on 3D GOI or 2D Si PMOS at 85°C and 10MV/cm. (b) PBTI measurement of $IrO_2/Hf/LaAlO_3$ on 3D GOI or 2D Si NMOS at 85°C and 10MV/cm.

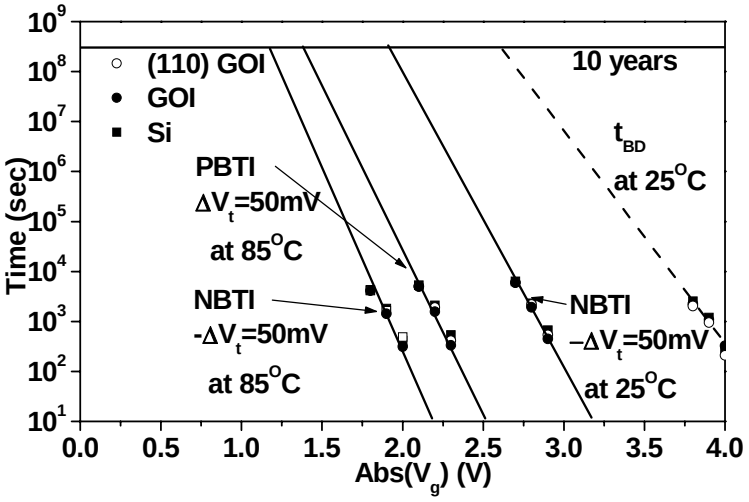


Fig. 5-8 The extrapolated max operation voltage V_{max} from BTI and t_{BD} for 10 years lifetime. The V_{max} is limited by NBTI that is reduced from 1.9 V at RT to 1.2 V at 85°C.