Chapter 6

Conclusions

We have demonstrated metal gate/high-κ/GOI CMOSFETs for the first time. The integration of dual work function metal gate and high-κ gate dielectric on GOI is also realized in our previously works, where no high-κ gate dielectric crystallization and EOT reduction were found. The 3D integration was realized by Ge-On-Insulator (GOI) CMOSFETs on 1-Poly-6-Metal (1P6M) 0.18-μm Si devices, where little performance degradation was measured in the lower layer 0.18-μm Si MOSFETs, due to the inherent low thermal budget of the GOI processing. The process with maximum 500^{o}C RTA is ideal for integrating metallic gates with high-κ to minimize interfacial reactions and crystallization of the high-κ material, and oxygen penetration in high- MOSFETs. The drive current of the 3D GOI n- and p-MOSFETs was more than double that of the control Si devices, providing another advantage of the approach.

This demonstrates that the GOI is the excellent candidate for metal-gate and high-κ gate dielectric integration, in additional to the merits of small effective mass and high mobility. It is noticed that the low temperature process is not an issue for real manufacture, since the low temperature processed InP and GaAs transistors and ICs

have shown good reliability and been used for very tight reliability specification of space and military applications.