The Investigation of GOI MOSFETs using Metal-gate electrodes and High-κ gate-dielectrics

Student: Dian-Sheng Yu **Advisor: Dr. Albert Chin**

Department of Electronics Engineering

& Institute of Electronics

National Chiao Tung University

Abstract

To continuously improve the MOSFET performance, both higher drive current and smaller leakage current are required. Although the high-κ MOSFETs can reduce the gate leakage current by orders of magnitude, the much degraded mobility is unacceptable for high performance circuits. To overcome this problem, we have developed a low temperature GOI process to fully utilize the merit of SiGe and achieve low dislocation simultaneously. Therefore, both hole and electron mobility can be largely improved in GOI with unique merits of dislocation free property for high yield, no high-κ crystallization, nor interface reaction or EOT reduction. In addition, the mobilities of the low temperature GOI devices are ~2-times higher than universal mobility values.

Extending the GOI process, we also integrated self-aligned metal gate/high-κ/GOI on 1-Poly-6-Metal (1P6M) 0.18-μm Si devices to reduce the AC power consumption in interconnects, which is the most severe issue beyond the DC

power arising from the gate dielectric leakage current. From a direct calculation of the AC power consumption, using an Electro-Magnetic method, we show that both the AC power consumption and maximum operation frequency can be improved by integrating an additional IC layer. These promising results are due to the low temperature GOI device process, which is well-matched to the low thermal budget requirements of three-dimensional (3D) integration. The good 3D CMOS may also provide equivalent scaling extension after 2D CMOS approaches the quantum mechanics limit, in addition to the advantage of low AC power consumption. The high performance GOI devices and simple 3D integration process, compatible to current VLSI technology, should be useful for future VLSI.