Figure Captions

Chapter 1 Introduction

Chapter 2 Al_2O_3/Ge-On-Insulator CMOSFETs with Fully NiSi and NiGe Dual Gates

Fig. 2-1 Cross-sectional TEM of GOI (a)without oxygen plasma treatment before bonding. (b) with oxygen plasma enhanced bonding.

Fig. 2-2 The fully silicided NiSi or germanided NiGe gate on SiO_2 or Al_2O_3 MOSFET.

Fig. 2-3 The V_{FB} versus SiO_2-thickness plot of n-MOS capacitors with fully NiSi, NiGe and Al gates.

Fig. 2-4 Cross-sectional TEM of NiGe/Al_2O_3 /Si structure.

Fig. 2-5 The C-V characteristics of Al_2O_3/Si and Al_2O_3/GOI p-MOSFETs with fully silicided NiSi, fully germanided NiGe, and control Al gates.

Fig. 2-6 The J_G-V_G and J_G-(V_G-V_T) characteristics of Al_2O_3/Si and Al_2O_3/GOI capacitors with fully silicided NiSi and fully germanided NiGe gates.

Fig. 2-7 The I_D-V_D characteristics of Al_2O_3/Si and Al_2O_3/GOI n- and p-MOSFETs with fully silicided NiSi, fully germanided NiGe, and control Al gates.

Fig. 2-8 The (a) electron and (b) hole mobilities from I_D-V_G characteristics of Al_2O_3/Si and Al_2O_3/GOI n- and p-MOSFETs with fully silicided NiSi, fully germanided NiGe, and control Al gates

Chapter 3 Fully Silicided NiSi:Hf/$LaAlO_3$/ Smart-Cut-Ge-On-Insulator n-MOSFETs With High Electron Mobility

Fig. 3-1 (a) The top view of SC-GOI substrate. (b) The TEM of ~1.6-μm thick smart cut GOI limited by the polishing.

Fig. 3-2 The measured resistivity of Si:Hf, TiSi, NiSi:Hf and NiTiSi gates.

Fig. 3-3 The SIMS profile of NiSi:Hf on SiO_2/Si.

Fig. 3-4 The V_{FB} versus SiO_2-thickness plot of n-MOS capacitors with fully NiTiSi, NiSi:Hf and Al gates..

Fig. 3-5 The C-V characteristics of (a) SiO_2 gate dielectric n-MOSFETs on Si with fully NiTiSi, NiSi:Hf and Al gates. (b) $LaAlO_3$ gate dielectric n-MOSFETs on Si and GOI with fully NiSi:Hf and Al gates.

Fig. 3-6 The measured J-V characteristics of (a) SiO_2/Si n-MOSFETs with different NiTiSi, NiSi:Hf and Al gates. (b) NiSi:Hf/$LaAlO_3$ /[Si or GOI] n-MOSFETs.

Fig. 3-7 The I_d-V_d characteristics of (a) SiO_2/Si n-MOSFETs with different NiTiSi, NiSi:Hf and Al gates. (b) $LaAlO_3$/Si and $LaAlO_3$/GOI n-MOSFETs with

different NiSi:Hf and Al gates.

Fig. 3-8 The I_d-V_g characteristics of (a) SiO_2/Si n-MOSFETs with different NiTiSi, NiSi:Hf and Al gates. (b) $LaAlO_3$/Si and $LaAlO_3$/GOI n-MOSFETs with different NiSi:Hf and Al gates.

Fig. 3-9 The electron mobility of (a) SiO_2/Si n-MOSFETs with different NiTiSi, NiSi:Hf and Al gates. (b) $LaAlO_3$/Si and $LaAlO_3$/GOI n-MOSFETs with different NiSi:Hf and Al gates

Chapter 4 Reducing AC Power Consumption by Three-Dimensional Integration of Ge-On-Insulator CMOS on 1-Poly-6-Metal 0.18-μm Si MOSFETs

Fig. 4-1 (a) Schematic of the 3D VLSI showing the lower layer Si MOSFETs, multi-level (1P6M) parallel interconnect lines and top layer GOI CMOS. (b) The equivalent folding 2D IC to form the 3D IC.

Fig. 4-2 (a) The equivalent circuit of the interconnect lines of the 0.18-μm MOSFETs. (b) The simulated and IE3D EM calculated S_{21} and S_{11} for 1-mm long, 0.5-μm spaced, parallel lines.

Fig. 4-3 (a) Measured S_{21} coupling of 1-mm long two parallel lines with various spacings from 0.5- to 8-μm using M6, and (b) calculated power loss of 0.5-μm spaced, parallel lines of different lengths.

Fig. 4-4 Images of 0.18- m MOSFETs with probing pads (M6 and 2-μm thickness) (a) before and (b) after the GOI bonding. The “dark” area on the pad after bonding is due to the selectively bonded Ge by “smart cut”.

Fig. 4-5 The surface profiles of the fabricated wafer, before and after GOI bonding.

Fig. 4-6 Cross-sectional TEMs of: (a) the lower 0.18-μm MOSFET and (b) the selectively bonded and smart cut Ge-on-Insulator on a pad. The Ge/SiO_2 interface appears to be dislocation free and smooth.

Fig. 4-7 The Ge/SiO_2 interface appears to be dislocation free and smooth. (a) The I_d -V_d and (b) the I_d-V_g characteristics of lower layer Si 0.18-μm MOSFETs, before and after GOI bonding.

Chapter 5 3D Metal-Gate/High-κ/GOI CMOSFETs on 1-Poly-6-Metal 0.18-μm Si Devices

Fig. 5-1 The V_{fb} and EOT plot for IrO_2 and IrO_2/Hf gates on $LaAlO_3$/Si after different RTA condition from 550 to 950^{o}C.

Fig. 5-2 (a) J_g-V_g curves of IrO_2/$LaAlO_3$/Si MOSFETs. The J_g is ~10^4X-10^5X lower than SiO_2 at 1.4nm EOT due to the uniform $LaAlO_3$ after 950^{o}C RTA. (b) The J_g-V_g curves of IrO_2/Hf or IrO_2 on $LaAlO_3$ MOSFETs on Si or GOI at 1.4nm EOT with different RTA temperature.

Fig. 5-3 The C-V characteristics of (a) IrO_2/Hf on $LaAlO_3$ gate-dielectrics n-MOSFETs on Si and GOI. (b) 150nm-IrO_2 on $LaAlO_3$ gate- dielectrics

p-MOSFETs on Si and GOI.

Fig. 5-4 The I_d-V_d characteristics of (a) IrO_2/Hf or IrO_2.on $LaAlO_3$ gate- dielectrics n- and p-MOSFETs on Si (b) IrO_2/Hf or IrO_2 on $LaAlO_3$ gate-dielectrics n- and p-MOSFETs on GOI.

Fig. 5-5 The I_d-V_g characteristics of (a) IrO_2/Hf on $LaAlO_3$ gate-dielectrics n-MOSFETs on Si or GOI. (b) IrO_2 on $LaAlO_3$ gate-dielectrics p-MOSFETs on Si or GOI.

Fig. 5-6 (a) The electron mobility of IrO_2/Hf on $LaAlO_3$ n-MOSFETs on Si or GOI.

(b) The hole mobility of IrO_2 on $LaAlO_3$ p-MOSFETs on Si or GOI.

Fig. 5-7 Vt shift as a function of time during (a) NBTI measurement of IrO_2/$LaAlO_3$ on 3D GOI or 2D Si PMOS at 85^{o}C and 10MV/cm. (b) PBTI measurement of IrO_2/Hf/$LaAlO_3$ on 3D GOI or 2D Si NMOS at 85^{o}C and 10MV/cm.

Fig. 5-8 The extrapolated max operation voltage V_{max} from BTI and t_{BD} for 10 years lifetime. The V_{max} is limited by NBTI that is reduced from 1.9 V at RT to 1.2 V at 85^{o}C.

Chapter 6 Conclusions