Chapter 1

Introduction

1.1 Motivation to Study Metal-gate electrodes

The poly depletion reduces the gate capacitance in the inversion regime and hence the inversion charge density, leading to a lower gate over drive and thus degrading the device performance. As the result, metal-gate electrodes will be required for complementary metal–oxide–semiconductor (CMOS) transistors to eliminate the gate depletion and dopant penetration problems that are associated with the conventional polycrystalline silicon (poly-Si) gate electrode [1.1]. In selecting metal-gate materials for device integration, the metal work function is an important consideration since it directly affects the threshold voltage and the performance of a transistor [1.2]- [1.4].

However, thermal instability of the effective metal electrode work function (Φ) on underlying gate dielectric as well as the equivalent oxide thickness (EOT) of the gate stack remains a major concern for CMOS integration. In addition, an understanding of how the gate dielectric affects Φ of the metal gate stack is scientifically and technologically important. Although the interfacial dipole theory was proposed to describe the dependence of Φ on underlying gate dielectrics [1.5], it

is not clear whether it can be applied to explain the work functions instability during high-temperature source/drain annealing. The high-temperature annealing could lead to the creation of extrinsic states at the metal-dielectric interface for particular combinations of metal-gate and gate-dielectric materials, and result in metal Fermi-level pinning [1.6]. The Fermi-level pinning shifts the original low or high work-function to midgap that causes the intolerable $|V_T|$ increase. The possible mechanism of Fermi-level pinning is due to the interface reaction and dipole creation of high-κ dielectric with poly-Si or metal-nitride at high RTA temperatures. Recently, the Fermi-level pinning effect caused by the threshold voltage (V_t) shifts has been reported for poly-Si gate CMOS processes with hafnium dioxide (HfO_2) [1.7]–[1.13], hafnium silicate $HfSi_XO_Y$ [1.14], hafnium oxynitride HfO_XN_Y [1.15], [1.16] and hafnium silicate oxynitride $HfSi_XO_YN_Z$ [1.17], [1.18] follow the same trend.

1.2 Motivation to Study High-κ dielectrics

To reduce the gate leakage current related power consumption in highly integrated circuit, high-κ gate dielectric will be used in 45-nm technology node at 2007 [1.19]-[1.22]. The physical thickness of the dielectric in the devices can be increased without the reduction of capacitance density. Since the leakage current is related to the physical thickness, the increasing thickness of high-κ dielectric can reduce the leakage current of the devices. According to the ITRS (International

Technology Roadmap for Semiconductor) of SIA [1.1], the thickness of gate oxide have to be below 15 Å after 2005. Moreover, the gate length and bias voltage reduces by 11 % every year while the drive current has to be maintained. Therefore, the continual scaling of gate dielectric is an inevitable trend in current VLSI technologies.

Although a large amount of effort that has been invested toward high-κ gate dielectrics, many of critical problems still remain. These problems include of high-κ against crystallization, phase separation, and interfacial reaction with underlying Si, charges/traps in high-κ as well as at interfaces, channel carrier mobility degradation, equivalent-oxide-thickness(EOT) control and scaling, work-function control for dual-gate CMOS integration, and gate stack reliability [1.23]-[1.25].

The high-κ dielectrics have been widely studied the characteristics and issues of those materials that have also been reported. The high-κ dielectrics show good performances are always accompanied by other drawbacks. To find out the most suitable high-κ dielectric for the use of device and altering the device structure or process to meet the requirement of the high-speed device are significant tasks to implant high-κ dielectrics in the next VLSI generation.

1.3 Background of Three-Dimensional Metal gate/High-κ/GOI

The high-κ gate-dielectric is required to reduce the gate leakage current at small EOT; the metal gate electrode can eliminate the gate depletion effect and increase the

transistor drive current. Recently, the Ge substrate has attracted much attention due to the inherent merit of both much higher electron and hole mobility than Si (two times higher mobility for electrons and four times for holes)[1.26] -[1.27]. At the same time, it is also a candidate for supply voltage scaling due to its narrower band-gap than that of silicon.

. To fully utilize this advantage, metal-gates on high-κ gate-dielectrics and on Ge-On-Insulator (GOI) [1.28]-[1.32] are required to optimize the performance of transistors in advanced C-MOSFETs, where the GOI can reduce the source-drain leakage current similar to SOI. However, the depositions of high-ķ material usually occurs in an oxidation ambient [1.28]-[1.29], where germanium substrate could be oxidized and form the unstable germanium oxide [1.30]-[1.31], because the native Ge oxide is water soluble. It is a challenge to fabricate high-quality gate dielectrics on germanium substrate.

As the results, the gate leakage current in the ultra-thin gate dielectric of individual transistors is the major source of the DC power consumption. However, by using high-κ oxynitride and metal-oxides this issue can be addressed. However, the AC power in the backend interconnects ($CV^2f/2$) then becomes an important power consumption issue, particularly when both the operation frequency and interconnect density increases. For example, operation frequencies can be as high as 10.6 GHz (for

Ultra-Wide Band access circuits) when using the high integration density and 9-Metal interconnect layers available in the 90 nm technology node. Although this AC power consumption has been extensively discussed (e.g. panel session of *Int'l Electron Devices Meeting (IEDM)*, 2003), no clear solution or approach is evident. Here, we suggest that three-dimensional (3D) integration can resolve this AC power consumption issue. Such 3D integration can also provide a way to increase the IC density [1.32] (equivalent to scaling down) once the quantum-mechanical scaling barrier is reached. However, the technology challenges are how to realize 3D ICs [1.33]-[1.35] with a low thermal budget and small impact on lower multiple interconnect and CMOSFET layers.

1.4 Innovation and Contribution

In this thesis, we have developed a process technique for the formation of 3D metal gate /high-κ/GOI CMOSFETs. There are a lot of advantages of the GOI devices and is consistent with previous reports. Such improvement is due to the smaller effective mass of Ge than Si. Similar better device performance is also obtained in small effective mass III-V FETs than Si MOSFETs, which also gives better high frequency performance at radio frequency (RF) regime. Therefore, the smaller effective mass is the key factor for both DC drive current and RF performance improvements. A further advantage of the 3D integration would be the high circuit density, and also that a 3D memory with a record high density can be realized by 3D

integration. Although there are other approaches to realize the 3D integration, such as using chip-stacking from a packaging approach, unique advantages of this work are the ~2 times higher drive current and potential high interconnect density using wafer-level process technology. The higher circuit density and better device drive current are equivalent to scaling down the VLSI technology – this may provide another useful approach when quantum-mechanical scaling limits occur. Further challenge of this approach is the formation of ultra-thin body Ge at the limited thermal budget, which is also useful to reduce the junction leakage of GOI CMOSFETs. The large leakage current is the biggest challenge of small energy bandgap materials such as Ge and InGaAs, although that also give high mobility and transistor drive current.