Chapter 2

Al_2O_3/Ge-On-Insulator CMOSFETs with Fully NiSi and NiGe Dual Gates

2.1 Introduction

Metal-gates on high-κ gate-dielectrics [2.1]-[2.4] and on strained Si [2.5] or on Ge-On-Insulator (GOI) [2.6] are required to optimize the performance of transistors in advanced C-MOSFETs. The high-κ gate-dielectric is required to reduce the gate leakage current at small equivalent-oxide-thickness (EOT); the metal gate electrode [2.5], [2.7]-[2.12] can eliminate the gate depletion effect and increase the transistor drive current; strained Si or GOI can improve carrier mobility and thus increase the drive current. In this work, high-κ Al_2O_3 gate dielectrics on GOI C-MOSFETs [2.6] were integrated with metal-like fully silicided NiSi [2.5], [2.10]-[2.12] and germanided NiGe dual gates. The advantages of GOI are that Ge has lower both hole and electron effective mass than Si, and GOI is free of defects [2.6], meeting the VLSI manufacturing requirement (<1 cm^{-2}) with much lower value than the ~10^4-10^6 cm^{-2} density in globally strained Si on SiGe. Fully NiSi and NiGe gates are formed at the same low temperature of 400^oC by RTA, which is required to reduce the diffusion of metal into the gate

dielectric [2.12]-[2.13]. Besides, the fully NiSi and NiGe gates have the advantages of being compatible with current VLSI processes, while providing a large work function difference [2.14]. At 1.7-nm EOT, the Al_2O_3/GOI C-MOSFETs with fully NiSi and NiGe gates have comparable gate leakage currents but 1.94 and 1.98 times higher electron and hole mobilities, respectively, than those of Al_2O_3/Si control devices.

2.2 Experimental Procedure

GOI wafers were formed by depositing 75-nm SiO_2 on both Ge and Si wafers, followed by bonding SiO_2/Ge and SiO_2/Si at 500^{o}C for ten hours. An O_2 plasma was used to activate the SiO_2 surface before bonding and a constant pressure was applied during bonding. After the GOI wafers were thinned down, a 400 nm isolating layer of SiO_2 was deposited on the GOI. The source and drain regions were implanted with 35 KeV phosphorus or 25 KeV boron to form n- and p-MOSFETs, respectively. The RTA activation was performed at 500^{o}C or 950^{o}C for GOI and Si, respectively. Then, the Al_2O_3 gate dielectric was grown on the GOI [2.6]. The dual fully silicided NiSi and germanided NiGe were formed on both the Al_2O_3 gate dielectric and opened contact regions of the source-drain. The NiSi or NiGe is formed by depositing 15-nm amorphous Si or Ge on Al_2O_3/GOI; depositing 15-nm Ni on the Si/Al_2O_3/GOI or Ge/Al_2O_3/GOI, and then annealing at 400^{o}C for 30s for silicidation [2.12] or germanidation, respectively. For

comparison, control Al_2O_3/Si MOSFETs with Al metal gates were fabricated.

2.3 Results and discussion

The GOI wafers were formed at 500^{o}C low temperature for 10 hrs using O_2 plasma and pressure enhanced bonding [2.6]. As shown in the cross-sectional TEM of Figs. 2-1(a) and 2-1(b), good bonding interface can only be seen using O_2 plasma treatment to avoid forming the irregular nm-scale voids, although dislocation free top Ge and smooth Ge-SiO_2 interface are achieved in both cases. Such nm-scale voids have weaker mechanical strength and may fail the bonding after subsequent thinning down.

Fig. 2-2 plots the fully silicided NiSi or germanided NiGe gate on SiO2 or Al2O3 MOSFET. The NiSi or NiGe gate and raised source-drain are formed at the same time.

Fig. 2-3 shows the VFB versus SiO2-thickness plot of n-MOS capacitors with fully NiSi, NiGe and Al gates. Work functions of 4.55 and 5.2eV are obtained from extrapolated V_{FB}.

The good gate dielectric integrity is also shown in the cross-sectional TEM of Fig. 2-4, where no Ni diffusion into or through Al_2O_3 can be seen. This is due to the low silicidation and germanidation temperature of 400^{o}C RTA. It is important to note that further tuning the work function for SiO_2/Si, Al_2O_3/Si, and Al_2O_3/GOI are possible using $NiSi_{1-x}Ge_x$ reported previously [2.14].

Fig. 2-5 plots the C-V characteristics of Al_2O_3/Si and Al_2O_3/GOI p-MOSFETs with fully silicided NiSi, fully germanided NiGe and control Al gates. That the capacitances measured under inversion and accumulation are the same suggests that the NiSi and NiGe gates are fully silicided or germanided, free from poly gate depletion. A κ value of 9 and an EOT of 1.7-nm are obtained from the C-V characteristics, and the large shifts in the C-V curves is due to the different flat band voltages (V_{fb}).

Fig. 2-6 shows the gate dielectric leakage currents of Al_2O_3/Si and Al_2O_3/GOI NMOS capacitors with fully NiSi and NiGe gates. The higher leakage current than expected from the J_G vs. V_G- V_T plot may be related to slight Ni diffusion [2.13], [2.15] into the 1.7-nm EOT Al_2O_3 gate oxide. Similar findings are also observed for fully NiSi and NiGe gates on 1.9-nm-SiO_2/Si MOSFETs, although these leakage currents are lower than those of the Al control devices obtained from the J_G vs. V_G plot [2.15]. Further improvement may be obtained by adding N into the gate dielectric to form an oxynitride. For the same EOT of 1.7-nm, the leakage current at V_G=1 V is three to four orders of magnitude lower than that of SiO_2, because of the thicker high-κ material. A high-quality Al_2O_3 gate dielectric can also be formed on GOI at 1.7-nm EOT, based on the measured comparable leakage current. Additionally, GOI is ideal for high-κ MOSFETs since the highest thermal budget for device fabrication is only 500^{o}C RTA for implant annealing.

At such a low temperature, the problems of interface reaction, high-κ crystallization, and penetration of oxygen, often found in high-κ/Si MOSFETs, are all suppressed.

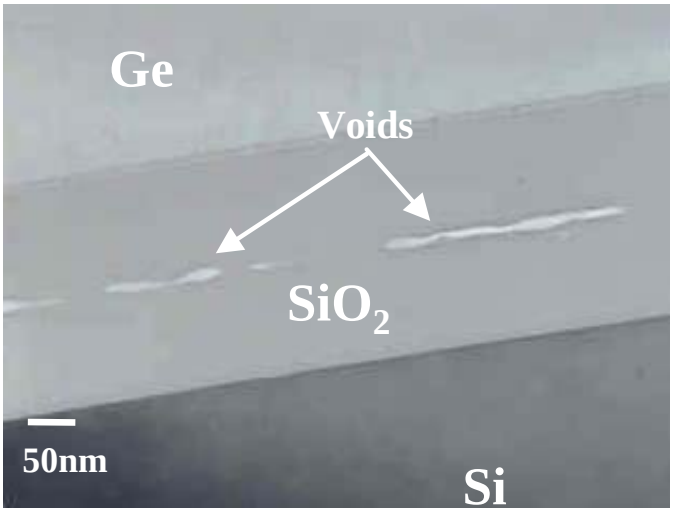
Fig. 2-7 compares the I_D-V_D characteristics for Al_2O_3/Si and Al_2O_3/GOI C-MOSFETs with fully NiSi, NiGe and control Al gates. GOI has significantly higher I_D than Si devices, because Ge has smaller electron and hole effective masses than Si. The I_D-V_D curves of Al_2O_3/Si MOSFETs are almost the same as those of the control Al gate, implying that the device performance is negligibly degraded when using fully NiSi and NiGe gates. This is because the low silicide/germanide formation temperature, 400^{o}C, prevents the diffusion of excess Ni into Al_2O_3/Si and Al_2O_3/GOI [2.12]-[2.13]; such excess Ni must be used to ensure the complete reaction of Si or Ge on the gate dielectric to avoid gate depletion.

Figs. 2-8(a) and 2-8(b) present the electron and hole mobilities obtained from the measured I_D-V_G curves of n- and p-MOSFETs, respectively. A mobility lower than the universal mobility is typical for high-κ Al_2O_3/Si MOSFETs. Further improvement, using novel high-κ with lower interface and bulk dielectric charges, is currently under development. The peak electron and hole mobilities for Al_2O_3/GOI with fully NiSi and NiGe gates are increased by factors of 1.94 and 1.98 to 350 and 100 cm^2/V-s, respectively. The slightly lower hole mobility than obtained in our previously developed Al/Al_2O_3/GOI

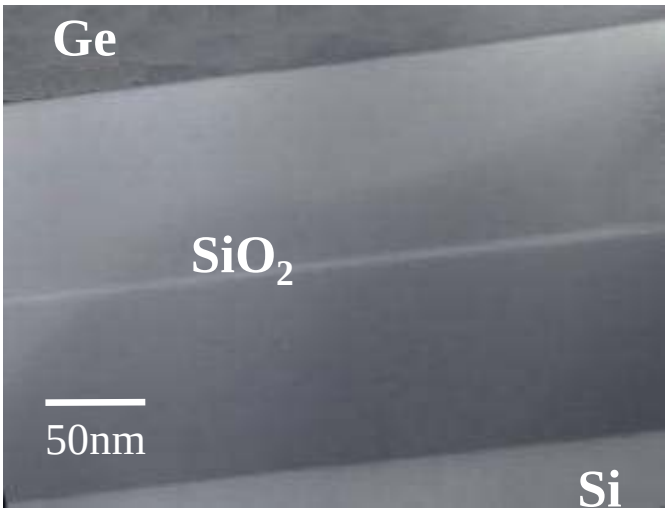
MOSFET [2.6] may be associated with the non-optimized source-drain NiSi or NiGe contact formed at the same time as the gate.

2.4 Conclusion

High-κ Al_2O_3/GOI C-MOSFETs were integrated with fully silicided NiSi and germanided NiGe dual gates. The capacitances and leakage currents obtained using fully NiSi and NiGe gates were similar to those obtained using Al metal gates on 1.7-nm EOT Al_2O_3 gate dielectric. These devices have approximately twice the electron and hole mobilities as Al_2O_3/Si devices, and a process which can be compatible with current VLSI technologies.



(a)



(b)

Fig. 2-1 Cross-sectional TEM of GOI (a)without oxygen plasma treatment before bonding. (b) with oxygen plasma enhanced bonding.

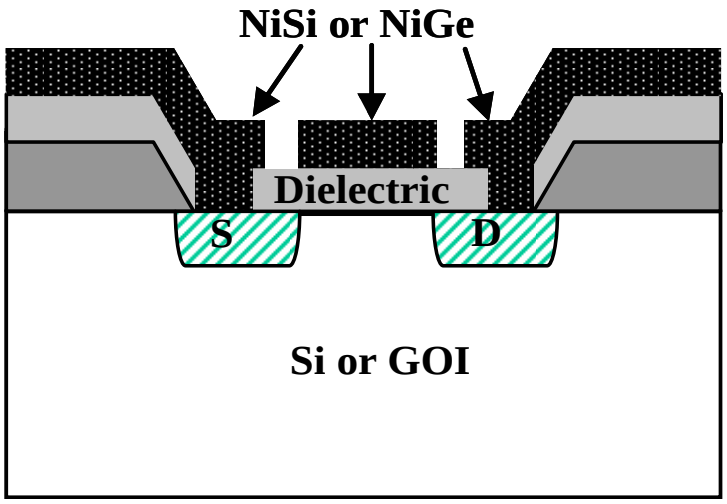


Fig. 2-2 The fully silicided NiSi or germanided NiGe gate on SiO_2 or Al_2O_3 MOSFET.

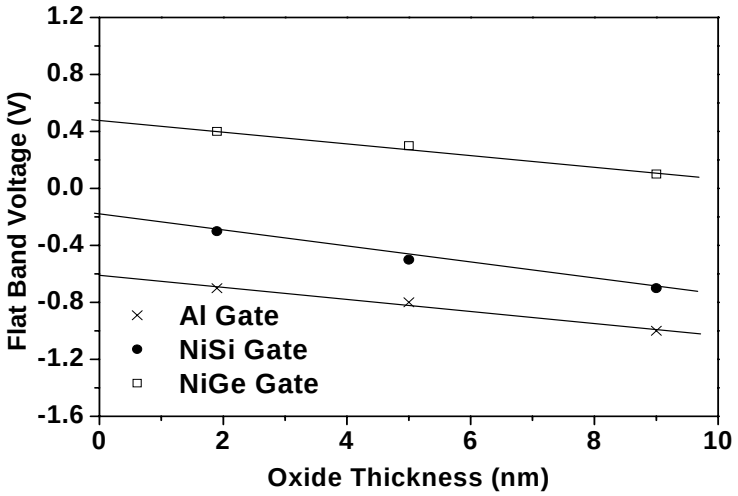


Fig. 2-3 The V_{FB} versus SiO_2-thickness plot of n-MOS capacitors with fully NiSi, NiGe and Al gates.

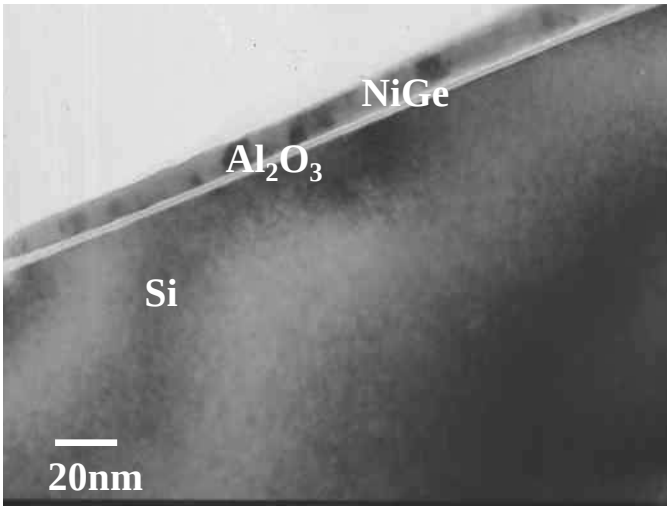


Fig. 2-4 Cross-sectional TEM of NiGe/Al_2O_3 /Si structure.

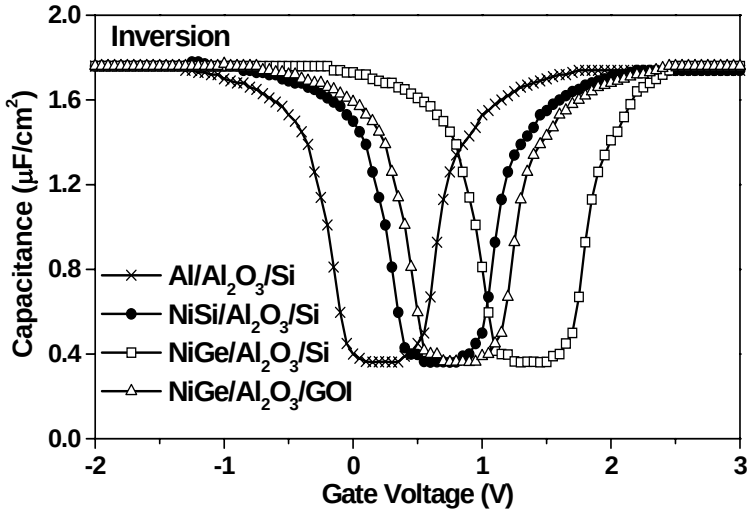


Fig. 2-5 The C-V characteristics of Al_2O_3/Si and Al_2O_3/GOI p-MOSFETs with fully silicided NiSi, fully germanided NiGe, and control Al gates.

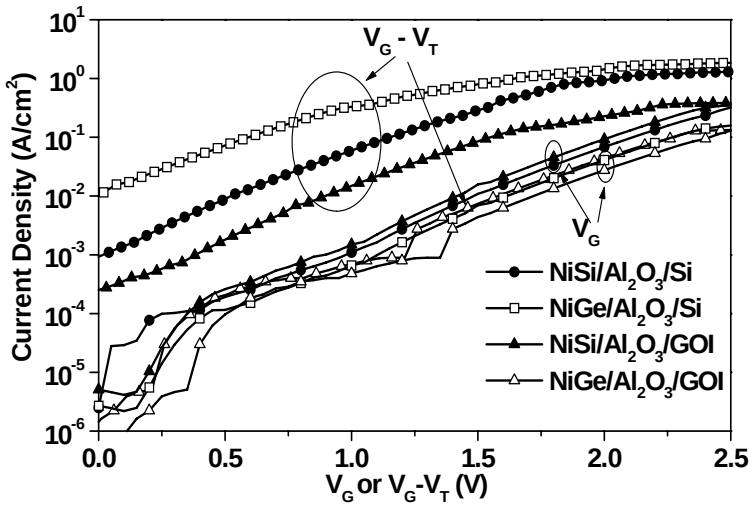


Fig. 2-6 The J_G-V_G and J_G-(V_G-V_T) characteristics of Al_2O_3/Si and Al_2O_3/GOI capacitors with fully silicided NiSi and fully germanided NiGe gates.

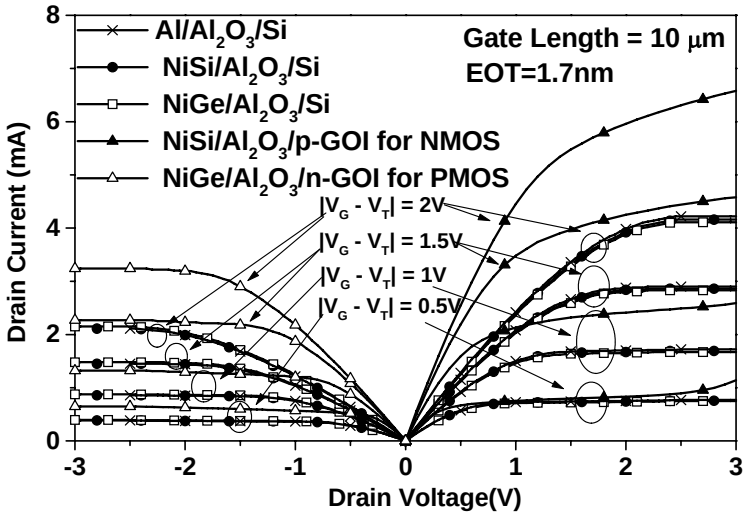
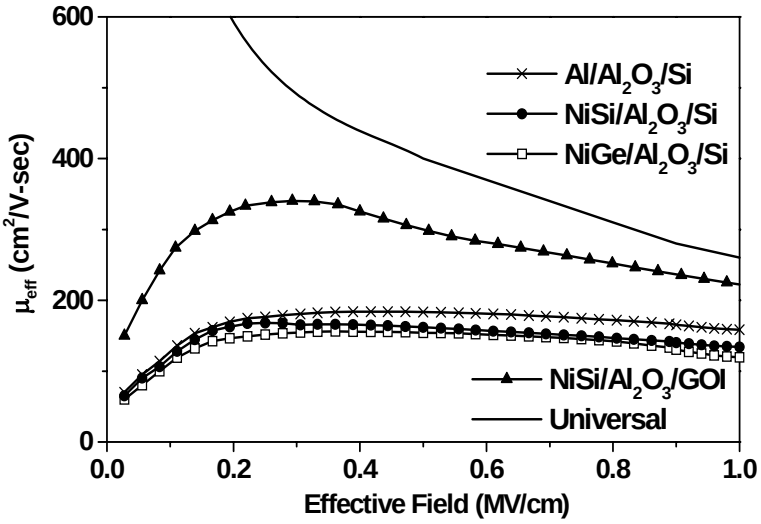
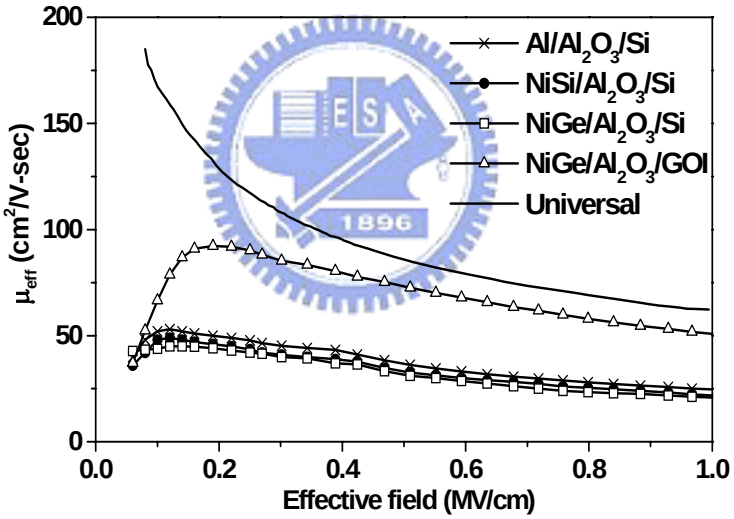


Fig. 2-7 The I_D-V_D characteristics of Al_2O_3/Si and Al_2O_3/GOI n- and p-MOSFETs with fully silicided NiSi, fully germanided NiGe, and control Al gates.



(a)



(b)

Fig. 2-8 The (a) electron and (b) hole mobilities from I_D-V_G characteristics of Al_2O_3/Si and Al_2O_3/GOI n- and p-MOSFETs with fully silicided NiSi, fully germanided NiGe, and control Al gates.