Chapter 3

Fully Silicided NiSi:Hf/$LaAlO_3$/ Smart-Cut-Ge-On-Insulator n-MOSFETs With High Electron Mobility

3.1 Introduction

The Ge substrate has attracted much attention due to the inherent merit of both much higher electron and hole mobility than Si [3.1]. To fully utilize this advantage, the integration of dual metal-gates/high-κ gate dielectric on Ge-on-Insulator (GOI) C-MOSFETs [3.2]-[3.3] is required, where the GOI can reduce the source-drain leakage current similar to SOI. Previously, we have developed the fully silicided NiSi and germanided NiGe dual workfunction gates [3.4] on high-κ/GOI C-MOSFETs [3.3], but the NiSi workfunction is too high for n-MOSFET. In this work, we have developed the low workfunction NiSi:Hf gate on high-κ $LaAlO_3$/smart-cut (SC)-GOI (SC-GOI) n-MOSFETs. The Hf was deposited on amouphous-Si/$LaAlO_3$ and driven-in by first 500^oC RTA for low workfunction control and the NiSi metal-like gate [3.5]-[3.7] was subsequently formed by depositing Ni and second 400^oC RTA silicidation for low gate resistivity. The high-κ $LaAlO_3$ gate dielectric is also improved from previous La_2O_3 [3.8]-[3.9] of free from moisture degradation, preserving high-κ value near La_2O_3 by

adding Al_2O_3 [3.2]-[3.3], [3.10] and available commercially. This is quite different from the $HfAlO_x$ [3.11] where the κ is largely lowered by AlO_x for improving thermal stability. The good device performance of NiSi:Hf/$LaAlO_3$/SC-GOI n-MOSFET is evidenced from the ~5 orders of magnitude lower leakage current than SiO_2 at 1.4-nm EOT and 1.7 times higher mobility than Si device with process compatible to current VLSI.

3.2 Experimental Procedure

The SC-GOI was formed by using H^+ implantation with 5×10^{16} cm^{-2} dose at 200 KeV to Ge wafer, depositing 75-nm SiO_2 on both Ge and Si wafers, O_2 plasma enhanced bonding [2]-[3], smart cut at 500°C for 0.5 hour, extended annealing at 500°C for 12 hours and slight polishing. The substrate doping of top Ge in SC-GOI is 5×10^{16} cm^{-3} with 1.6-μm thickness from cross-sectional TEM. Further thinner down the GOI to fully depleted body is possible by reducing the proton implantation energy similar to SOI. Because the top Ge on GOI is still relatively thick, we have used the PECVD SiO_2 for device isolation. After patterning, the source and drain regions were implanted with 35 KeV and 5×10^{15} cm^{-2} phosphorus and RTA activation at 500°C (1 min) for GOI and 950°C (30 s) for control Si. Then, the $LaAlO_3$ gate dielectric was deposited by PVD from a $LaAlO_3$ source followed by 400°C oxidation. The thickness of formed $LaAlO_3$ gate dielectric is 8.1-nm from TEM. The NiSi:Hf on $LaAlO_3$ was formed by depositing 30-nm

un-doped amorphous Si, then 10 nm Hf and 500°C (30 s) RTA for drive-in, and 30 nm Ni and second RTA at 400°C (30 s) for silicidation. No Hf silicide was formed during first RTA as examined by XRD. Control $LaAlO_3$/Si n-MOSFET with Al gate was also fabricated for comparison.

3.3 Results and discussion

Figs. 3-1(a) and 3-1(b) show the top view and the TEM of SC-GOI wafer. However, the ~1.6-μm thick smart cut GOI limited by the polishing in university lab.

Fig. 3-2 shows the measured resistivity. The Hf can not form silicide at 600°C as measured by XRD and further increasing temperature will cause Hf penetration to 1.9-nm SiO_2 (Fig. 3-3). The resistivity is lowed in TiSi but still too high. We have used the additional Ni to form NiTiSi or NiSi:Hf and resistivity is lowered to only 45-52 μΩ-cm close to NiSi.

Fig. 3-4 plots the flat band voltage (V_{fb}) vs. SiO_2 gate dielectric thickness with fully NiTiSi, NiSi:Hf and Al gates. The NiTiSi and Al gates are controlled devices. The extracted work function for NiSi:Hf is reduced from 4.55 eV of NiSi [3]-[4] to 4.2 eV and the resistivity is also lowered from ~2000 μΩ-cm for Hf:Si gate to 52 μΩ-cm for NiSi:Hf and close to that of NiSi fully silicided gate. This is a strong advantage of NiSi:Hf gate.

Fig. 3-5(a) shows C-V of NiTiSi/SiO_2/Si, NiSi:Hf/SiO_2/Si, and Al/SiO_2/Si

n-MOSFETs. Fig. 3-5(b) shows C-V of NiSi:Hf/$LaAlO_3$/Si, NiSi:Hf/$LaAlO_3$/SC-GOI, and Al/$LaAlO_3$/Si n-MOSFETs. The same inversion and accumulation capacitance value indicates that the NiSi:Hf gate is fully silicided without poly-Si depletion. An EOT of 1.4-nm is obtained from the measured gate capacitance of n-MOSFETs that give a κ-value of 22.6 close to the original κ of 25 in the target. The slight variation from target κ value may be due to the forming interfacial oxide and changing stoichiometry. The sharper C-V turn-on slope near inversion than others [3.12]-[3.14] is due to the higher capacitance/area. The V_{fb} of NiSi:Hf on SiO_2/Si and $LaAlO_3$/Si are -0.58 V and -0.47 V respectively, which gives close workfunction of 4.2 eV and 4.3 eV due to the high fixed charge of -1×10^{12} cm^{-2} in $LaAlO_3$. This result suggests less Fermi-level pinning in NiSi:Hf/$LaAlO_3$.

Figs. 3-6(a) and 3-6(b) show the comparison of gate dielectric leakage current of controlled devices, NiSi:Hf/$LaAlO_3$/Si, NiSi:Hf/$LaAlO_3$/SC-GOI and Al/$LaAlO_3$/Si capacitors. Comparable leakage current of fully NiSi:Hf with Al gate devices is observed that suggests very small metal diffusion related excess leakage current [3.3]-[3.4], [3.15] of ultra-thin 1.4-nm thick gate oxide. For the same EOT of 1.4-nm, the leakage current at V_g of 1 V is ~five orders of magnitude lower than that of SiO_2 gate dielectric [3.16].

Figs. 3-7(a) and 3-7(b) show the I_d-V_d characteristics plotted at the same V_g-V_t,

which $LaAlO_3$ on SC-GOI and $LaAlO_3$/Si n-MOSFETs with fully NiSi:Hf or controlled devices. The I_d of $LaAlO_3$/Si MOSFETs with fully NiSi:Hf gate are almost the same as those of the control Al gate, implying no device performance degradation when using fully NiSi:Hf gate. This is because the low process temperature to prevent the Hf and Ni diffusion through the $LaAlO_3$ gate dielectric [3.3]-[3.4], [3.15]. The NiSi:Hf/$LaAlO_3$ on SC-GOI has significantly higher I_d than that on Si substrate because of the smaller electron effective mass of Ge than Si.

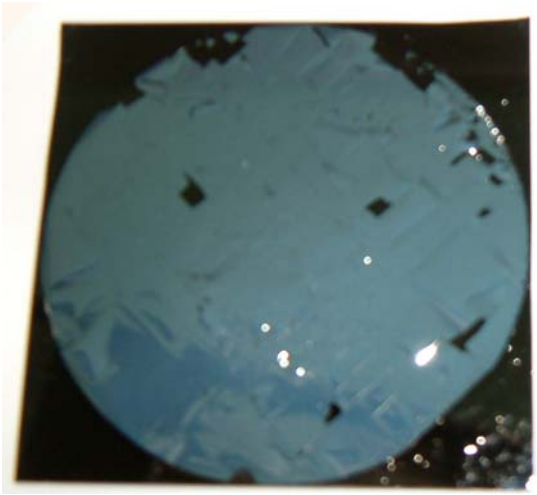
Figs. 3-8(a) and 3-8(b) show the I_d-V_d characteristics plotted at the same V_g-V_t, which $LaAlO_3$ on SC-GOI and $LaAlO_3$/Si n-MOSFETs with fully NiSi:Hf or controlled devices. The very low V_t of only 0.13 V in NiSi:Hf/$LaAlO_3$/Si n-MOSFET also indicates the less Fermi-level pinning.

Figs. 3-9(a) and 3-9(b) show the electron mobility which $LaAlO_3$ on SC-GOI and $LaAlO_3$/Si n-MOSFETs with fully NiSi:Hf or controlled devices. The $LaAlO_3$/Si n-MOSFETs with NiSi:Hf gate has close mobility with controlled Al gate due to the low process temperature with few gate metal diffusion. The NiSi:Hf/$LaAlO_3$/Si n-MOSFETs has high peak electron mobility of 235 cm^2/Vs and comparable with metal-gate/HfO_2 [3.17], which also shows the good $LaAlO_3$ dielectric integrity. The peak mobility is further increased by 1.7 times to 398 cm^2/Vs for NiSi:Hf/$LaAlO_3$ MOSFET on SC-GOI

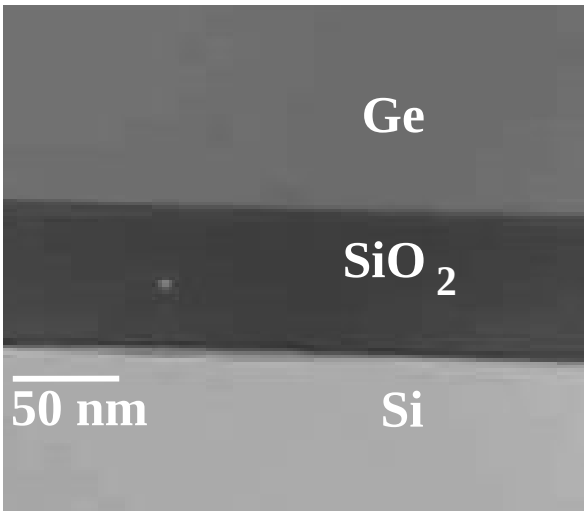
at 1.4-nm EOT. Such mobility enhancement is due to the much smaller effective mass of Ge than Si, which will become more important in ultra-thin body MOSFET due to the degraded mobility [3.18]. This high mobility and low temperature process SC-GOI is ideal for high-κ MOSFET with important merits of small impurity diffusion, no high-κ crystallization or interface reaction, and dislocation free property for high circuit yield.

3.4. Conclusion

We have fabricated the NiSi:Hf/$LaAlO_3$/SC-GOI n-MOSFETs. At the 1.4-nm EOT, the peak electron mobility in GOI is 1.7 times higher than in Si to 398 cm^2/Vs. The low 500^{o}C RTA can greatly minimize high-κ crystallization, interfacial reaction, and impurity diffusion in source-drain and gate for advanced high-κ MOSFETs.



(a)



(b)

Fig. 3-1 (a) The top view of SC-GOI substrate. (b) The TEM of ~1.6-μm thick smart cut GOI limited by the polishing.

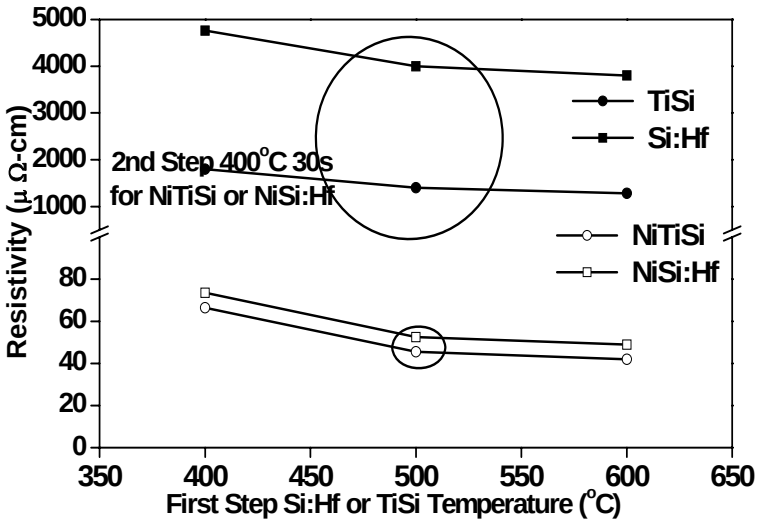


Fig. 3-2 The measured resistivity of Si:Hf, TiSi, NiSi:Hf and NiTiSi gates.

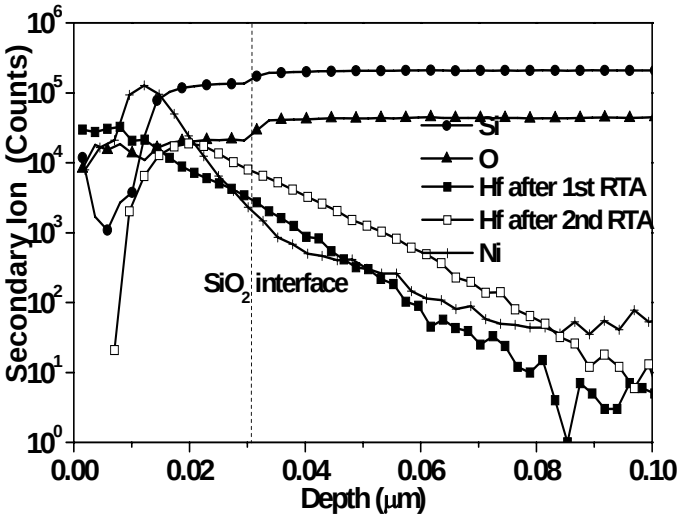


Fig. 3-3 The SIMS profile of NiSi:Hf on SiO_2/Si.

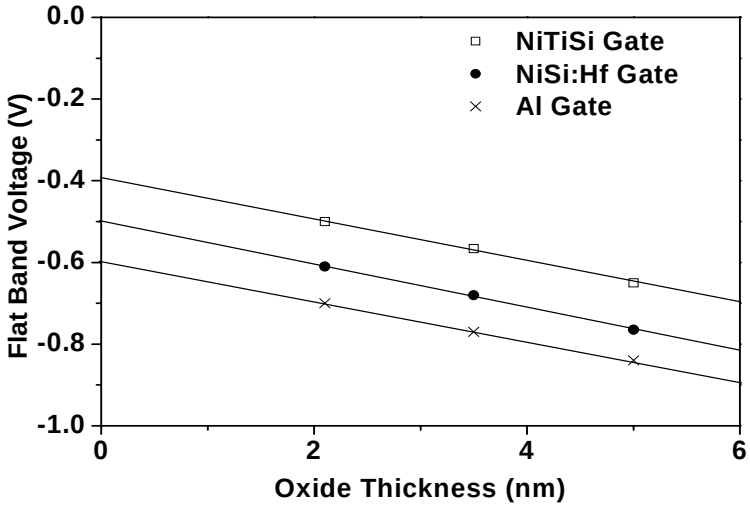
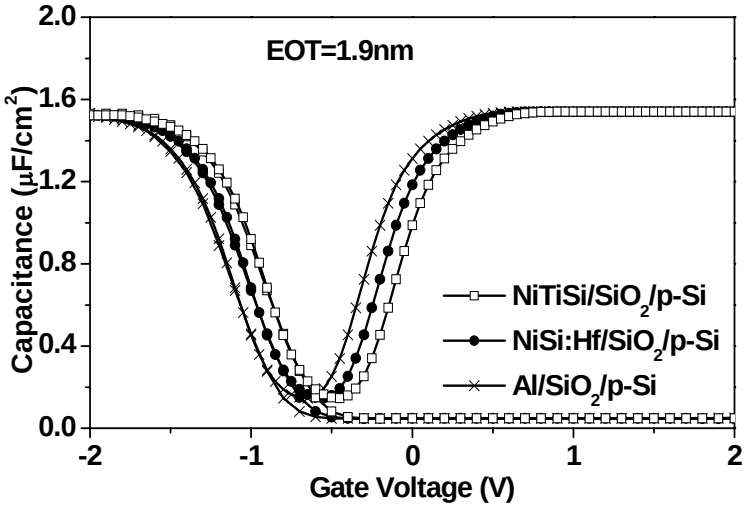


Fig. 3-4 The V_{FB} versus SiO_2-thickness plot of n-MOS capacitors with fully NiTiSi, NiSi:Hf and Al gates.



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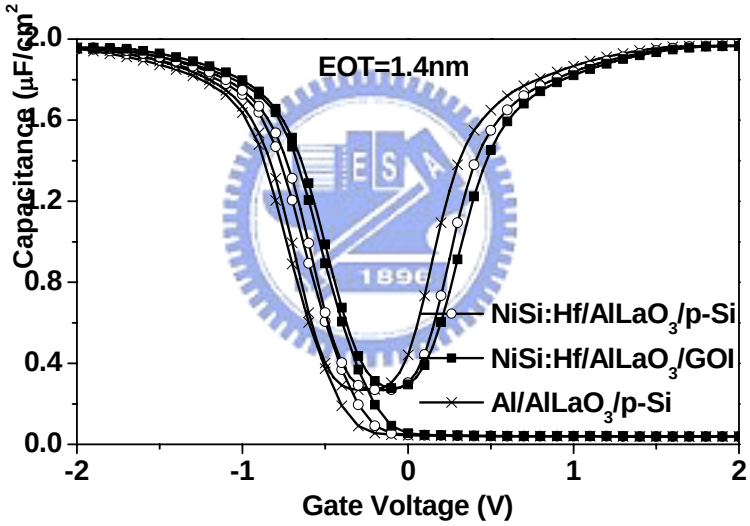
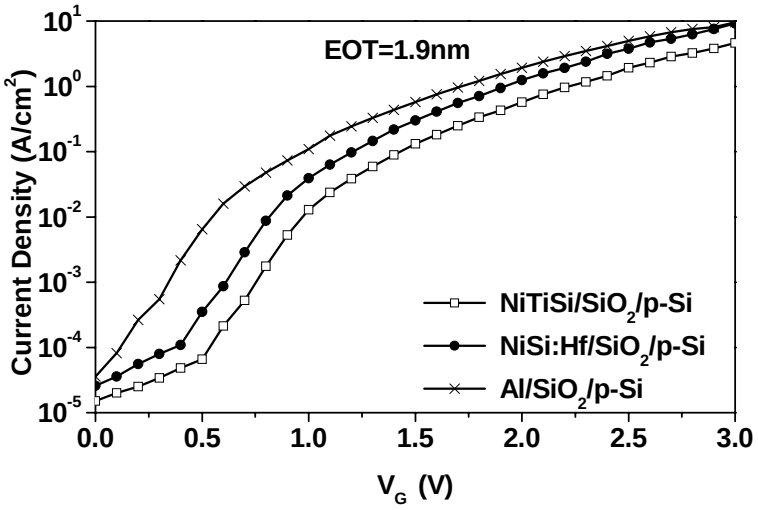


(b)

Fig. 3-5 The C-V characteristics of (a) SiO_2 gate dielectric n-MOSFETs on Si with fully NiTiSi, NiSi:Hf and Al gates. (b) $LaAlO_3$ gate dielectric n-MOSFETs on Si and GOI with fully NiSi:Hf and Al gates.



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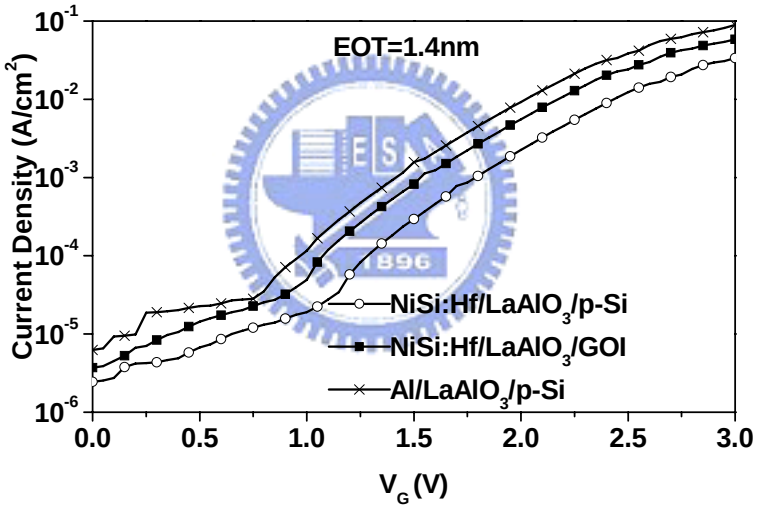
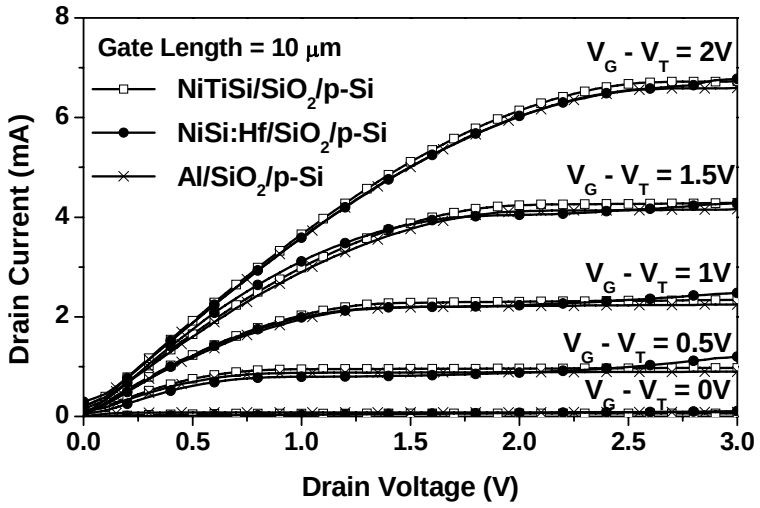


(b)

Fig. 3-6 The measured J-V characteristics of (a) SiO_2/Si n-MOSFETs with different NiTiSi, NiSi:Hf and Al gates. (b) NiSi:Hf/$LaAlO_3$ /[Si or GOI] n-MOSFETs.



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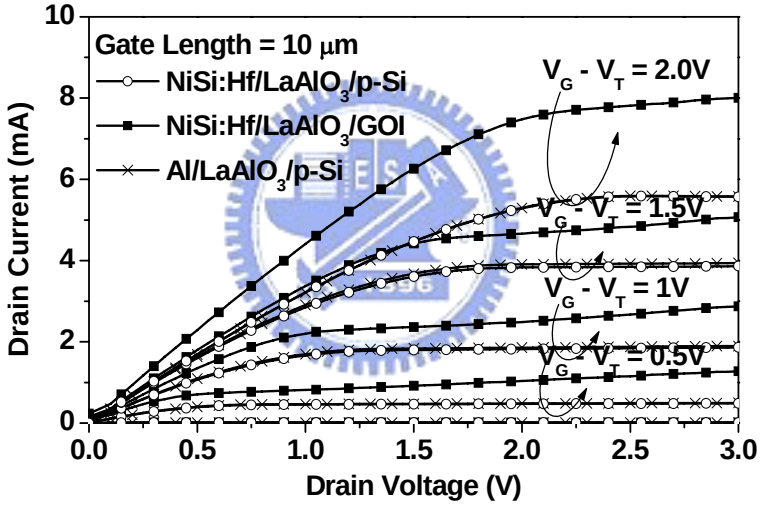
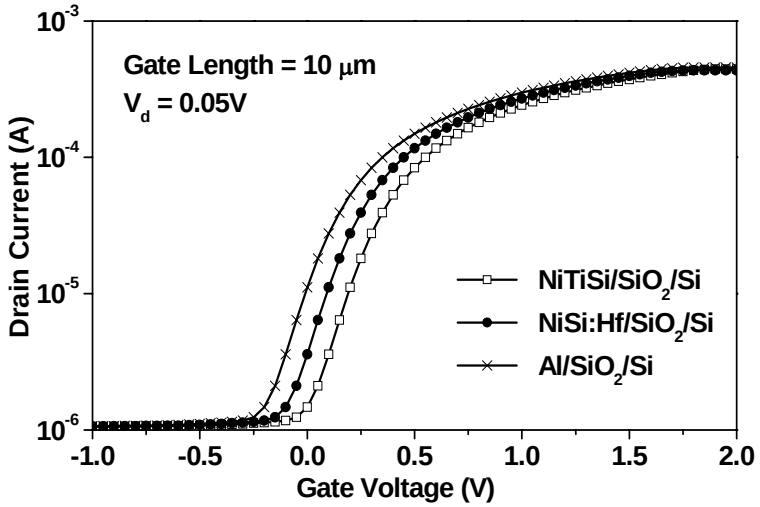
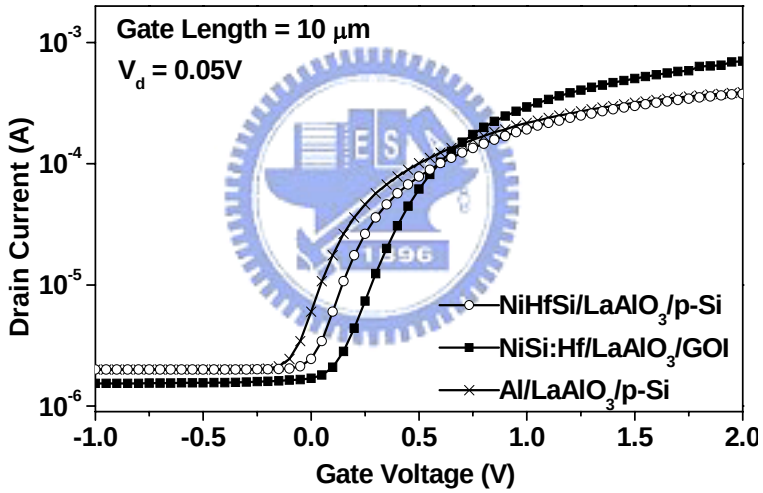


(b)

Fig. 3-7 The I_d-V_d characteristics of (a) SiO_2/Si n-MOSFETs with different NiTiSi, NiSi:Hf and Al gates. (b) $LaAlO_3$/Si and $LaAlO_3$/GOI n-MOSFETs with different NiSi:Hf and Al gates.

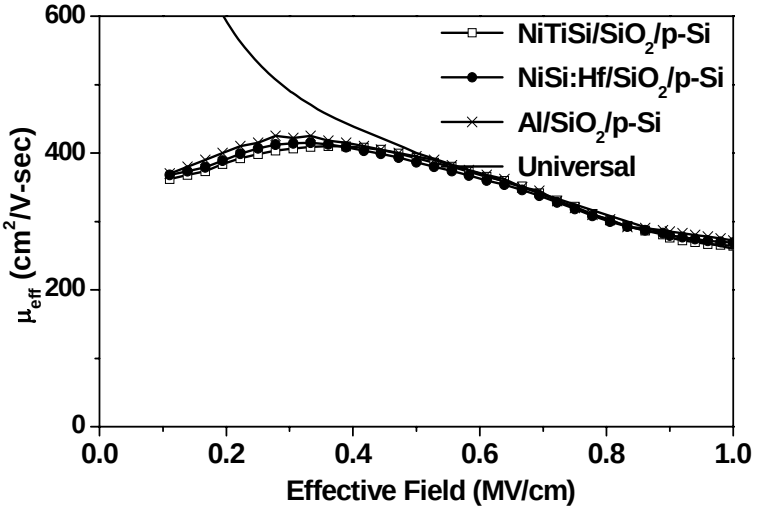


(a)

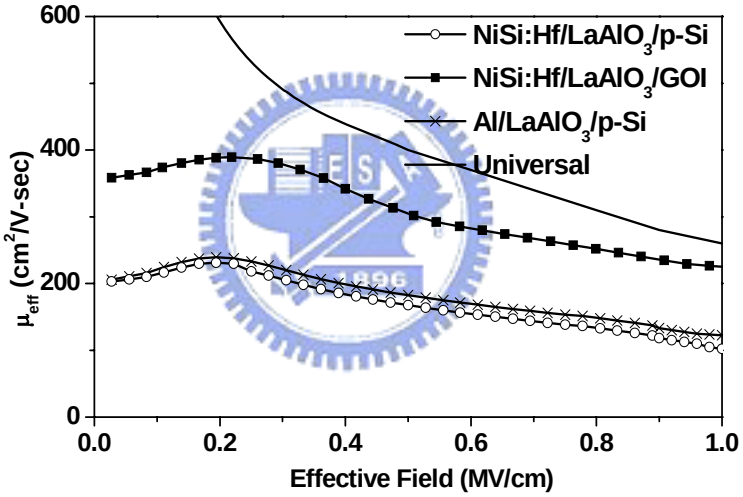


(b)

Fig. 3-8 The I_d-V_g characteristics of (a) SiO_2/Si n-MOSFETs with different NiTiSi, NiSi:Hf and Al gates. (b) $LaAlO_3$/Si and $LaAlO_3$/GOI n-MOSFETs with different NiSi:Hf and Al gates.



(a)



(b)

Fig. 3-9 The electron mobility of (a) SiO_2/Si n-MOSFETs with different NiTiSi, NiSi:Hf and Al gates. (b) $LaAlO_3$/Si and $LaAlO_3$/GOI n-MOSFETs with different NiSi:Hf and Al gates.