A 2.4–5.4-GHz Wide Tuning-Range CMOS Reconfigurable Low-Noise Amplifier

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***Abstract*—A 2.4–5.4-GHz CMOS reconfigurable low-noise amplifier (LNA) is designed. It consists of two stages: a broadband input stage for a steady input matching and noise performance, and a reconfigurable band-selective stage which provides a wide-range frequency tuning from 2.4 to 5.4 GHz and a 12-dB stepped gain with linearity adjustment. The frequency tuning is conducted by a multitapped switching inductor and varactors. Careful design of the switching inductor achieves consistent performance among frequency configurations. The stepped gain and linearity adjustment are provided by a size-switchable transistor with a variable biasing. Fabricated in 0.13 μm CMOS technology this LNA exhibits performance including up to 25 dB power gain, 2.2–3.1 dB noise figure and less than 5 mW power consumption under 1 V power supply.**

***Index Terms*—Dual reactive feedback, low-noise amplifier (LNA), multistandard, reconfigurable, switching inductor.**

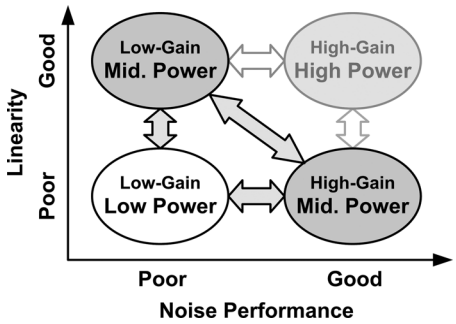

Fig. 1. Performance matrix for reconfiguration of LNA. In this study, the three corner states of low power and middle power are pursued.

I. Introduction

MULTISTANDARD radio is a trend for next generation wireless systems. As wireless standards are evolving to meet the need in various scenarios, it is highly expected that a transceiver is reconfigurable in specification accommodating different standards. Such specifications for a receiver RF front-end include carrier frequency, bandwidth, voltage gain, noise figure, and linearity. Moreover, the power consumption shall be controllable accordingly.

At the input of a reconfigurable receiver, a low-noise amplifier (LNA) is expected to provide good input impedance matching, high voltage gain and low noise figure in dynamically specified frequency bands. The frequency operation of such an LNA can be in either concurrent multiband or tunable single band. To date there are several approaches for concurrent multiband operation. First proposed in 2002, an LNA utilizes dual-band *LC*-networks to provide concurrent dual-band input matching and output gain response [1]. This approach becomes cumbersome when handling multiple bands. The more adequate solution is a broadband design with comprehensive band coverage. Numerous broadband LNA design techniques have been developed by applying the input *LC* bandpass filtering [2], [3], the dual reactive feedback [4], the resistive/source–follower feedback [5]–[7], and the common-gate topologies [8]. In compare with the tunable single band approach, the broadband input matching avoids the use of tunable devices in input network that easily degrades noise performance. The broadband gain response, however, is unfavorable because it allows undesired interferers to pass through such that stringent linearity is required in the succeeding stages (e.g., mixer). As such, a tunable single band gain response is preferred for out-of-band interferer suppression [9], [10].

Besides the frequency issues, the tradeoff between LNA performances can be outlined by the performance matrix as shown in Fig. 1, giving insight for performance reconfiguration. Typically the higher gain provides the lower noise figure, whereas the lower gain brings the better linearity. Power consumption further affects the circuit dynamic range.[1] If higher performance of a larger dynamic range is in need, the LNA shall be configured to consume more power to meet the requirement. For example, a large dynamic range demanding both low noise figure and high linearity is required in the ultra-wideband (UWB) system, whereas the low power consumption is of the primary concern in Bluetooth connection. Techniques including bias control, current steering, feedback switching, and attenuation switching can be used for gain control [11], [12].

This paper proposes a wide tuning-range performance-reconfigurable LNA. It consists of two stages featuring broadband input matching and low noise amplification at the first stage,

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[1]The circuit dynamic range is defined as the allowed input power range, typically from its sensitivity to 1-dB compression point.

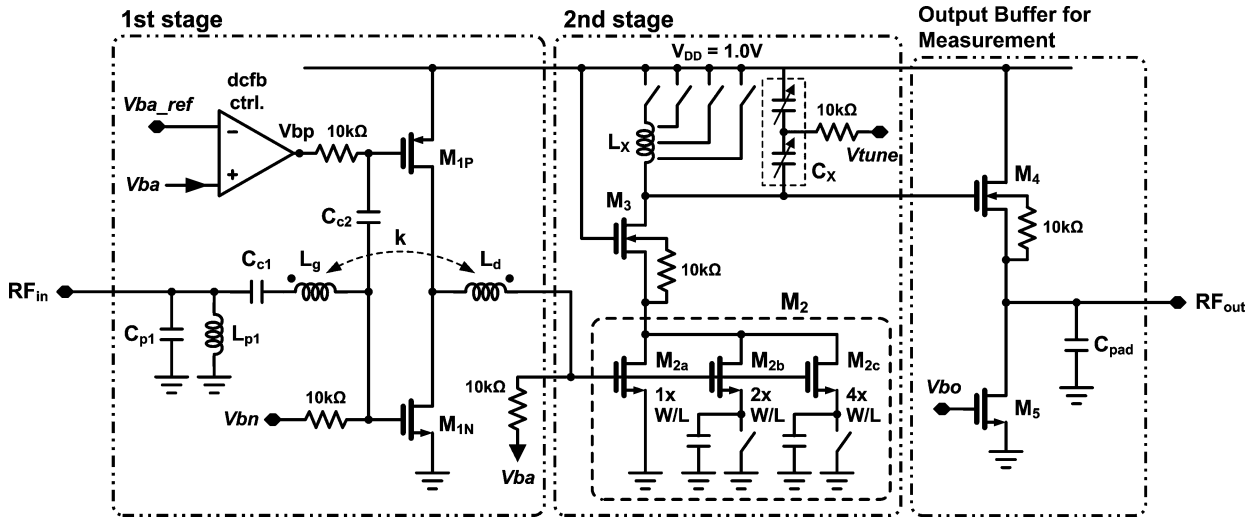

Fig. 2. Proposed reconfigurable LNA.

TABLE I
DEVICE VALUES OF THE DESIGNED LNA

Transistor	M_{1N}	M_{1P}	M_{2a}	M_{2b}	M_{2c}	M_3	M_4
Width (μm) (Length:0.13μm)	120	120	10	20	40	60	30

Device	C_{p1}	L_{p1}	C_{c1}&C_{c2}	L_g	L_d	k	C_X
Value	460fF	4.9nH	2.7pF	3.2nH	4.9nH	0.17	240–510fF

Note: The inductance of the switching inductor L_X is as shown in Fig. 13.

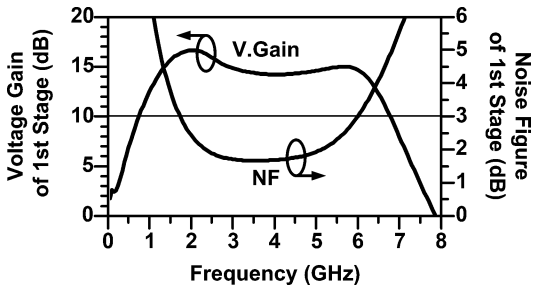

Fig. 3. Voltage gain and noise figure of the first stage in simulation result.

and a wide tuning-range band-limited gain response with adjustable performance at the second stage. The 0.13 μm technology CMOS LNA is designed to operate from 2.4 to 5.4 GHz. A new switched inductor configuration provides wide-range frequency tuning while gain and noise figure are maintained at the same level. With bias control and transistor size switching, performance is reconfigurable to approach the lower left three corner states as shown in Fig. 1. This paper provides theoretical extension for [13], including a related design concept for wide range tuning and switching inductor. The error of linearity performance listed in [13] is also amended.

This paper is constructed as follows. In Section II the proposed reconfigurable LNA design is discussed in detail. As the key component for wide tuning range, the design of switching inductor is discussed in Section III. Section IV demonstrates the chip implementation and shows measurement results. Finally, this work is concluded in Section V.

II. PROPOSED RECONFIGURABLE LNA

The schematic of the proposed reconfigurable LNA is as shown in Fig. 2. The first stage is a broadband amplifier with dual-reactive feedback, based on the circuitry in [4]. The second stage is a cascode amplifier providing gain, linearity, and wide-range frequency tuning. The output buffer stage is for measurement purpose. The parameters of key devices are listed in Table I and the design concepts of the first and the second stages are detailed as follows.

A. Broadband Amplifier With Controllable Output DC Level

The first stage performs broadband low noise amplification and input matching. The basic amplifier is a CMOS inverter amplifier (M_{1N} and M_{1P}) featuring large trans-conductance and dc-current reuse. The gate bias of each transistor is fed via a 10 kΩ resistor and isolated by capacitors C_{c1} and C_{c2}. By employing dual reactive transformer and capacitive feedback along with an input shunt $L_{p1} - C_{p1}$ tank, this architecture can achieve broadband simultaneous noise and impedance matching as shown in [4]. The two reactive feedback networks facilitate impedance and noise matching at two different frequencies, extending the frequency band of simultaneous input power match and noise optimization [14]. In this project, this stage is designed for the entire 2–6 GHz frequency band. The input impedance matching is designed having less than -15 dB input reflection and the noise figure is very close to $\mathrm{NF}_{\min}$ in this wide frequency range.

As to the voltage gain response, the L_d provides a series peaking boosting the gain at the high frequency corner. At frequencies lower than 1-GHz L_{p1} introduces a low impedance path to ground thus suppressing out-of-band interferers. As the design result, the simulated frequency responses of voltage gain and noise figure of the first stage are shown in Fig. 3.

The biasing of M_{1N} and M_{1P} is separated to provide a controllable output dc level to bias transistor M_2, conducting the performance reconfiguration at the second stage. The dc level,

Vba, is clamped equal to a reference voltage Vba_ref by a dc feedback loop, including M_{1P} and an OP-Amp. The M_{1P} itself provides a 24 dB dc voltage gain and the OPAmp, consuming less than 80 μW power, has 37 dB voltage gain. Thus, the gate voltage of M_{1P}, Vbp, varies within 12.5 mV for the demanded 200 mV dc dynamic range of Vba, introducing tiny impact on performance of the first stage. Meanwhile the error between Vba and Vba_ref is less than 0.2 mV. In a fully integrated receiver, the Vba_ref and the M_{1N} bias voltage Vbn can be configured by a current-mode DAC and a constant-gm bias circuit, respectively. In this prototype both of them are driven externally for laboratory test purpose.

B. Performance Reconfiguration by Switching Transistor

Performance reconfiguration is realized by the common-source amplifier (M_2) at the second stage, including gain and linearity control. The noise figure is generally correlated to the gain level; that is, higher gain brings a lower noise figure. The design target is implementation of three operation modes, one in high gain (HG) and two in low gain (LG_1 and LG_2). Gain difference of at least 10 dB is expected between the high-gain and the low-gain modes. Besides, this LNA exhibits an improved linearity in LG_1 mode while the even lower power consumption is achieved with degraded linearity in LG_2 mode.

Being the transconductor of the cascode amplifier at the second stage, M_2 is found to be the linearity bottleneck of this LNA. Its transconductance g_m is the primary nonlinearity source as M_2 is loaded by a common-gate stage of low input impedance [15]. Hence, linearity control mainly relies on M_2 gate biasing. Linearity performance can be inspected by the second and third input interception point voltages, V_{IIP2} and V_{IIP3} as

$$V_{\mathrm{IIP2}} = \left|\frac{g_m}{g_m{}'}\right| \tag{1}$$

and

$$V_{\mathrm{IIP3}} = \sqrt{\left|\frac{4}{3}\frac{g_m}{g_m{}''}\right|} \tag{2}$$

where the g_m' and the g_m'' are the first and the second derivative of g_m, respectively. Because M_2 receives very wideband input, the second-order distortion is found as critical as the third-order in some application cases. Transistor linearity is characterized by the simulated results of g_m, g_m'/g_m' and $\sqrt{|g_m''/g_m|}$ versus V_{gs}, as plotted in Fig. 4. As can be seen, larger V_{gs} gives higher gain g_m, better V_{IIP2}, and larger drain current, while V_{IIP3} varies insignificantly. The second-order distortion is chosen as the primary linearity index to be improved in this LNA.

The actual design is according to Fig. 4. Gate bias is first chosen corresponding to different linearity performances in each operation mode. Then the transistor size is set regarding to gain requirement. The design result is summarized in Table II. The 12 dB stepping difference is produced on g_m and g_m'/g_m between the HG and the LG_1 modes. In practice the drain current I_{DS}, instead of V_{gs}, is controlled to alleviate the impact of process variation.

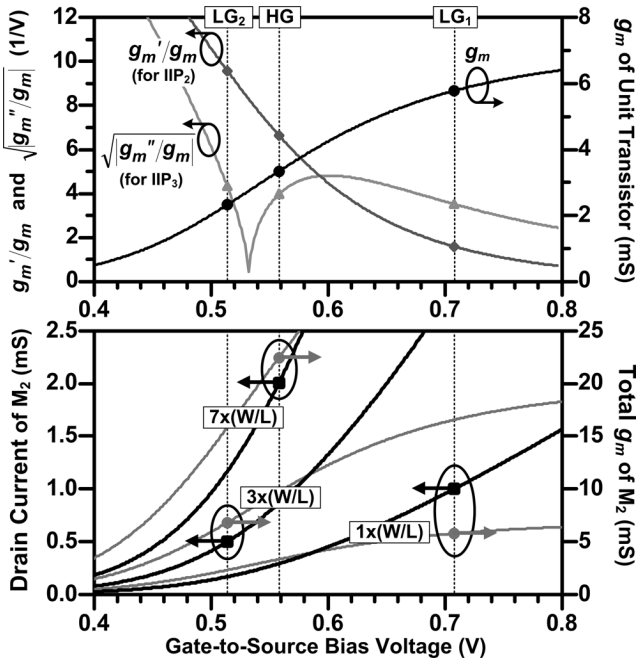

Fig. 4. Simulated g_m'/g_m and g_m of transistor M_2 in response to V_{gs} under different gain modes.

TABLE II
DESIGN PARAMETERS IN EACH OPERATION MODE

Mode	V_{gs}	Size	I_{DS}	$^*g_m$	$^*g_m'/g_m$
HG	0.56V	7x	2.0mA	0dB	0dB
LG_1	0.71V	1x	1.0mA	-12dB	-12dB
LG_2	0.51V	3x	0.5mA	-12dB	+4dB

*The g_m and g_m'/g_m are normalized to their values in HG mode.

As shown in Fig. 2, the M_2 transistor actually consists of three transistors, M_{2a}, M_{2b} and M_{2c} with the size ratio of 1:2:4. Transistors M_{2b} and M_{2c} are switched on and off by the switches at their source nodes. This allows larger switch size for smaller on-resistance. The input capacitance of M_2 should not be changed significantly by size switching as it is an important parameter for LNA input matching, which is expected to be similar among all considered configurations. For the sake of this, the source nodes of M_{2b} and M_{2c} are ac bypassed to ground to alleviate the impact of switching to the input capacitance.

Switching transistor M_2 controls the voltage gain and linearity, as well as the power consumption. Compared to the conventional current steering variable-gain schemes in which gain is adjusted by the common-gate transistor M_3, our approach is more power-efficient because at lower gain the LNA requires smaller drain current.

C. Frequency Tuning by Switching Inductor and Varactor

Band-selective filtering is provided by an *LC* resonance tank at the second stage as shown in Fig. 2. The resonator consists of a multitapped switching inductor and two on-chip varactors. The former provides coarse frequency stepping, while the latter is for fine tuning. Coarse frequency stepping is realized by switching control of tapping points so as to obtain different inductances,

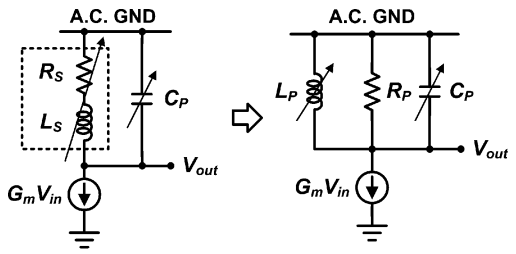

Fig. 5. Wide continuous frequency tuning by adjusting both the inductor and capacitor. (a) Practical circuitry. (b) Equivalent parallel resonance tank.

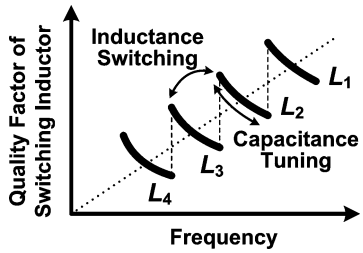

Fig. 6. Quality factor profile of switching inductor as required for good voltage gain consistency.

yielding to several sub-bands. This *LC* tank is demanded to be tunable over the entire frequency range of interest. Meanwhile it shall provide a quite consistent voltage gain for each tuned band. This calls for the quality factor requirement of the switching inductor as described as follows.

The resonator tank can be generally represented by an equivalent circuit as shown in Fig. 5(a), in which the inductance is switchable and the capacitance is tunable. The resistance R_S in series to inductor L_S includes the inductor parasitic resistance and the switch on-resistance, and dominates the quality factor of this tank. As the inductance L_S is changed by turning on distinct switches, the R_S value can actually be changed accordingly. To get the insight to achieve the aforementioned gain consistency requirement, the resonator circuit is transformed to the parallel *RLC* tank in Fig. 5(b), with the equivalent parallel inductance and resistance derived, respectively, as

$$L_P = L_S\left(1+\frac{1}{Q_L^2}\right) \tag{3}$$

and

$$R_P = \frac{L_S}{R_S}\cdot\frac{1}{C_P} = \frac{Q_L}{\omega_0}\cdot\frac{1}{C_P}. \tag{4}$$

Here Q_L stands for the quality factor of the switching inductor which equals to $\omega_0 L_S/R_S$, and ω_0 is the resonance frequency as

$$\omega_0 = \sqrt{\frac{1}{L_S C_P}\cdot\frac{Q_L^2}{1+Q_L^2}} = \sqrt{\frac{1}{L_S C_P}-\frac{R_S^2}{L_S^2}}. \tag{5}$$

The 3-dB bandwidth (BW) of this resonance tank is

$$\mathrm{BW(in\ Hertz)} = \frac{1}{2\pi}\frac{\omega_0}{Q_L} = \frac{1}{2\pi}\frac{R_S}{L_S}. \tag{6}$$

At resonance the voltage gain of this circuit can be expressed as

$$A_v = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = G_m R_P. \tag{7}$$

The design guideline is revealed from these equations. Given the typical condition of a flat G_m response over the frequency range of interest, the voltage gain consistency fully corresponds to the frequency dependency of R_P. In discussion of the fine capacitance tuning, the switching inductor is assumed frozen with a fixed inductance. As $C_P \propto 1/\omega_0^2$, it leads to the frequency dependency of Q_L for consistent R_P from (4) as

$$Q_L \propto \omega_0^{-1}. \tag{8}$$

This condition can be partially met by a practical inductor, of which quality factor Q declines in the frequency region higher than the peak-Q frequency. Note that a consistent BW calls for the condition of $Q_L \propto \omega_0$ by (6), opposite to (8). For LNA the consistency on voltage gain is more important than bandwidth so the design generally follows (8). Nevertheless, the bandwidth variation is still acceptable if the frequency range of each sub-band remains small enough.

The condition for consistent R_P among coarse inductance stepping can also be obtained from (4), by freezing the tuning of C_P, as

$$\frac{Q_L}{\omega_0} = \frac{L_S}{R_S} \approx \mathrm{const.} \tag{9}$$

That is, when inductance L_S is switched smaller for a higher resonance frequency, the corresponding quality factor of switching inductor should be proportionally higher, which necessitates a smaller R_s. In general this can be fulfilled by design of the switch on-resistance for each inductance.

Combined together, the conditions in (8) and (9) give the quality factor requirement of the switching inductor as the profile shown in Fig. 6. In practical implementation of the on-chip switching inductor, the rule of (9) is actually difficult to realize because it demands an unacceptable large switch transistor for the smallest inductance. To overcome this difficulty, an alternative switching configuration for the inductor is proposed, as discussed in the next section.

III. Multitapped Switching Inductor

A. Switching Configuration

The basic idea of inductor switching is to enable or disable sections of inductor coils to obtain different inductance values. The conventional switching configuration for a multitapped inductor is shown in Fig. 7(a) [16], [17]. Both ends of the coil are directly connected to the application circuit at the nodes **a** and **b**. Switches are attached to the tapping nodes, of which one can be turned on to bypass the remaining coils. The switch on-resistance is known to degrade the inductor quality factor. The degradation becomes worse in a spiral configuration that all the coil sections are winded together with magnetic mutual coupling. This coupling magnifies the degrading effect of switch on-resistance. An alternative switching configuration is proposed as

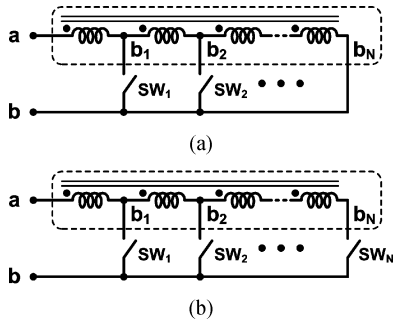

Fig. 7. Different switching configurations for multitapped inductor. (a) Conventional. (b) Proposed.

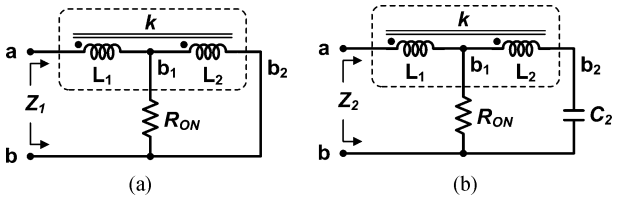

Fig. 8. Equivalent circuits of double-tapped inductor in different switching configurations. (a) Conventional. (b) Proposed.

shown in Fig. 7(b), in which an additional switch is attached at the end node of the coil $\mathbf{b_N}$ to convert the difficulty that the conventional configuration faces.

Consider the representative case of double-tapped switching inductor, i.e., $\mathbf{N} = 2$ in Fig. 7. When the inductors in Fig. 7(a) and (b) are switched for the smaller inductance, they can be modeled as circuits shown in Fig. 8(a) and (b), respectively. The $R_{\rm ON}$ is on-resistance of the switch at node $\mathbf{b_1}$, typically much larger than the intrinsic resistance of coil. The C_2 in Fig. 8(b) is parasitic capacitance of the switch at node $\mathbf{b_2}$ in OFF state. The two sections of coil, L_1 and L_2, form a transformer with coupling factor of k.

In the desired ideal case without effect of L_2 and k, only the primary loop of L_1 and $R_{\rm ON}$ is considered such that the inductor quality factor is limited by $R_{\rm ON}$ as

$$Q_0 = \frac{\omega L_1}{R_{\rm ON}}. \tag{10}$$

When L_2 and k are considered, the input impedance Z_1 in the conventional case of Fig. 8(a) can be derived as

$$Z_1 = j\omega {L_1}' + \frac{{R_{\rm ON}}' \cdot j\omega {L_2}'}{{R_{\rm ON}}' + j\omega {L_2}'} \tag{11}$$

in which

$$\begin{aligned} {L_1}' &= (1-k^2)L_1 \\ {L_2}' &= k^2 L_1 + L_2 + 2k\sqrt{L_1 L_2} \\ {R_{\rm ON}}' &= R_{\rm ON}\left(\frac{{L_2}'}{L_2}\right). \end{aligned} \tag{12}$$

The issue of Z_1 can be addressed in twofold. At the low frequency that $\omega L_2' \ll R_{\rm ON}'$, the inductance approximates to $L_1' + L_2'$, equal to inductance of the entire coil and hence the inductance switching function fails. At the high frequency that $\omega L_2' \gg R_{\rm ON}'$, the Q_1 can be derived as

$$Q_1 \approx \frac{\omega {L_1}'}{{R_{\rm ON}}'} = \frac{\omega L_1}{R_{\rm ON}} \cdot \frac{1-k^2}{\left(1+k\sqrt{\dfrac{L_1}{L_2}}\right)^2} \tag{13}$$

which is less than the Q_0 for $k > 0$.

On the other hand, the input impedance Z_2 in the proposed configuration can be derived as

$$Z_2 = j\omega(L_1+M) + \frac{(R_{\rm ON} - j\omega M)[\,1-\omega^2(L_2+M)\,C_2]}{1+j\omega R_{\rm ON} C_2 - \omega^2 L_2 C_2} \tag{14}$$

in which $M = k\sqrt{L_1 L_2}$. As the frequency approaches to

$$\omega_Q = \frac{1}{\sqrt{(L_2+M)\cdot C_2}} \tag{15}$$

Z_2 becomes as $j\omega_Q \cdot (L_1 + M)$, independent of $R_{\rm ON}$, and thus the quality factor Q_2 is limited only by the intrinsic resistance of coil. The quality factor boosting conducted by the auxiliary resonance of $L_2 + M$ and C_2 is therefore obtained in the high frequency region around ω_Q.

A test case compares these two configurations. Set L_1 and L_2 as 1 and 2 nH along with parasitic resistances 2 and 4 Ω, respectively. The coupling factor k is 0.5, $R_{\rm ON}$ is 10 Ω, and C_2 is 0.3 pF. The calculated results are shown in Fig. 9(a) and (b). Also included is Q_0 as a reference. The calculated ω_Q of (15) is 5.58 GHz. The Q_2 by the proposed configuration is boosted near ω_Q, close to the intrinsic coil quality factor and much larger than Q_1.

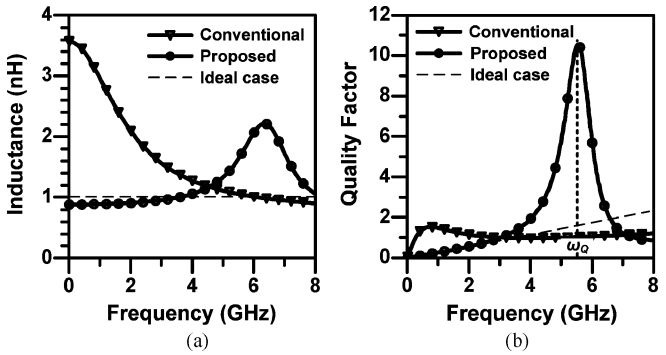

Fig. 9. Calculated results compared for the test cases in the conventional (—▽—) and the proposed configurations (—•—). The ideal switch operation of only the primary loop (– – –) is included as a reference. (a) Effective inductance. (b) Quality factor.

B. Tuning Ratio of Resonance Frequency

When the switching inductor is applied to an *LC* resonator with a capacitor, the wide-range resonance frequency tuning is the primary expectation. The frequency tuning ratio is mainly determined by the inductance tuning ratio provided by the switching inductor. In the case using conventional switching configuration, the frequency tuning ratio is unlimited because the effective inductance can be switched to an arbitrarily small value, though the quality factor can be severely degraded to

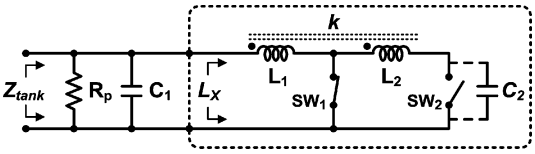

Fig. 10. Equivalent model to calculate the achievable frequency tuning ratio.

unusable. In the use of the proposed configuration, however, the frequency tuning ratio is limited as the consequence of quality factor boosting by the auxiliary resonance.

The analysis of the limited tuning ratio is by using the equivalent model of *LC* resonance tank as shown in Fig. 10, in which the L_X is the effective inductance of switching inductor and the C_1 is the external capacitor to resonate with L_X. This model discusses the two extreme cases of the maximum and minimum L_X with the switching of SW_1 and SW_2. The switch on-resistance is chosen to be ignored in this analysis so as to identify the primary limiting factor.

When the SW_1 is open and the SW_2 is short, the maximum effective inductance $L_{X,\mathrm{MAX}}$ is

$$L_{X,\mathrm{MAX}} = L_1 + L_2 + 2k\sqrt{L_1 L_2} \tag{16}$$

in which k is the magnetic coupling factor between L_1 and L_2. On the other hand, when the SW_1 is short and the SW_2 is open, the minimum inductance $L_{X,\mathrm{MIN}}$ can be derived as

$$L_{X,\mathrm{MIN}} = L_1 \cdot \left[\left(1-k^2\right) + \frac{k^2}{1-\omega^2 L_2 C_2}\right] \tag{17}$$

which is frequency dependent. When resonating with C_1, the $L_{X,\mathrm{MAX}}$ and $L_{X,\mathrm{MIN}}$ give the minimum and maximum resonance frequencies $\omega_{\min}$ and $\omega_{\max}$, respectively. The $\omega_{\min}$ can be easily derived as

$$\omega_{\min} = \frac{1}{\sqrt{\left(L_1 + L_2 + 2k\sqrt{L_1 L_2}\right) C_1}}. \tag{18}$$

The $\omega_{\max}$ can be obtained by solving the equation

$$\omega_{\max}^2 L_1 C_1 \cdot \left[\left(1-k^2\right) + \frac{k^2}{1-\omega_{\max}^2 L_2 C_2}\right] = 1 \tag{19}$$

of which solutions are

$$\omega_{\max}^2 = \frac{\dfrac{1}{L_1 C_1} + \dfrac{1}{L_2 C_2} \pm \sqrt{\left(\dfrac{1}{L_1 C_1} - \dfrac{1}{L_2 C_2}\right)^2 + \dfrac{4k^2}{L_1 C_1 L_2 C_2}}}{2\left(1-k^2\right)}. \tag{20}$$

The solutions in (20) indicate two resonance frequencies at which peak value of Z_{tank} can be found. As discussed in the Appendix , the lower frequency applying the minus sign in (20) is the one of interest for $0 < k < 1$.

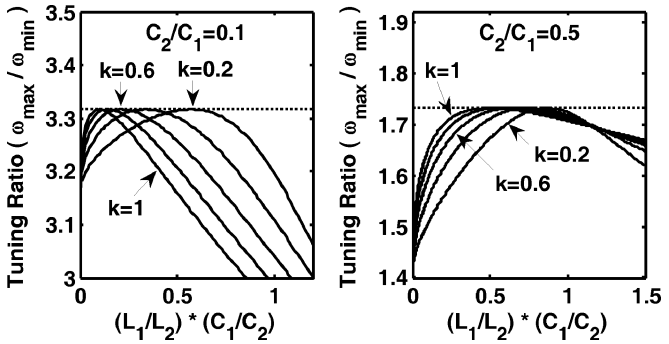

Fig. 11. Frequency tuning ratio of the proposed switching inductor configuration in different C_2/C_1 ratio. The dotted horizontal asymptotes are located at the maximum value of tuning ratio given in (21).

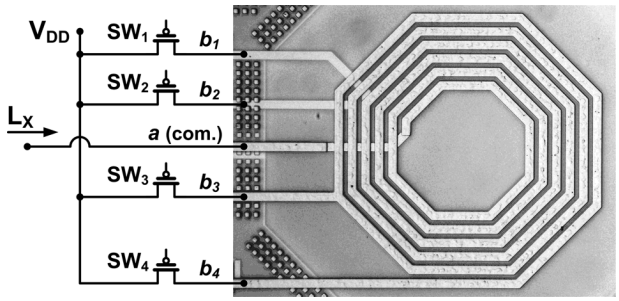

Fig. 12. Designed switching inductor using PMOS as switches.

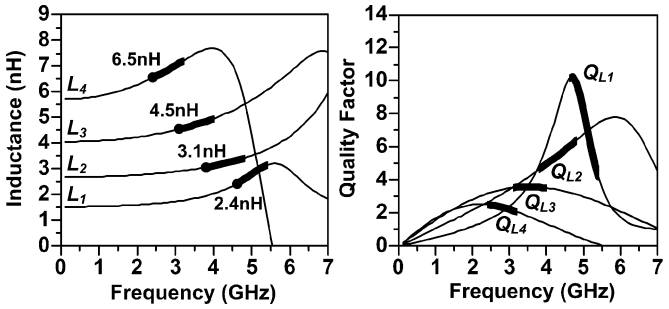

Fig. 13. Simulation results of the designed switching inductor with designed PMOS switches.

The frequency tuning ratio is defined as $\omega_{\max}/\omega_{\min}$. As the L_2 is inductance of the remaining coil bypassed by SW_1, the intuitive design of a smaller L_1 with a larger L_2 cannot always promise a larger frequency tuning ratio because the increase of $L_2 C_2$ can also decrease the $\omega_{\max}$. The optimal L_1/L_2 arrangement for maximum $\omega_{\max}/\omega_{\min}$ depends on k and C_2/C_1 ratio. It is difficult to derive directly but can be traced from the calculation results, as shown in Fig. 11. Also included is the special case of $k = 1$ as discussed in Appendix .

Fig. 11 reveals important insight. First, for a given C_2/C_1 ratio the peak value of $\omega_{\max}/\omega_{\min}$ is constant for $0 < k \leq 1$. Second, a smaller C_2/C_1 ratio allows a larger peak $\omega_{\max}/\omega_{\min}$ value. What of interest is the relationship between the peak $\omega_{\max}/\omega_{\min}$ value and the C_2/C_1 ratio as a design guide for the switching inductor. This can be obtained by finding the peak $\omega_{\max}/\omega_{\min}$ for $k = 1$, as

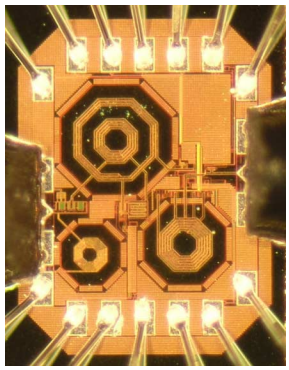

Fig. 14. Micrograph of the fabricated reconfigurable LNA under test.

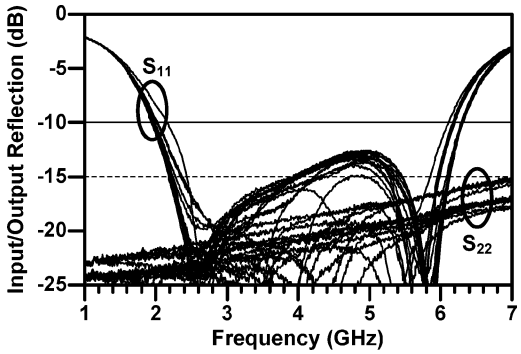

Fig. 15. Measured input and output reflection ratio (S_{11} and S_{22}) of the LNA in all listed configurations under test.

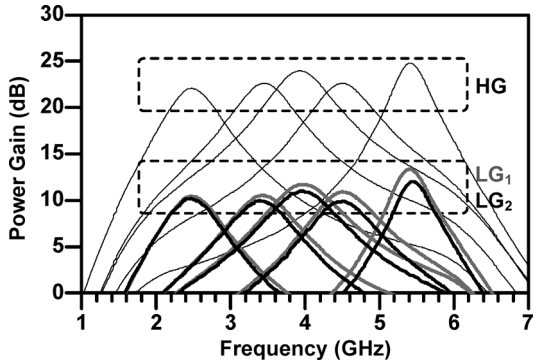

Fig. 16. Measured power gain of LNA under typical bias condition.

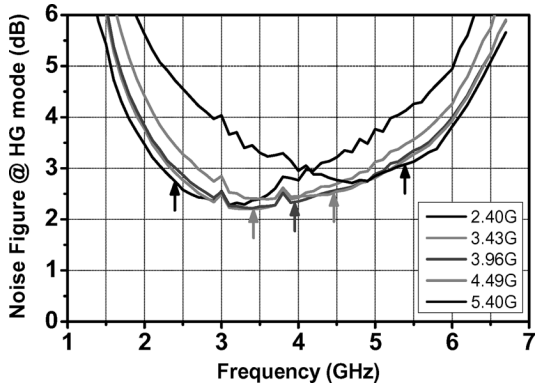

Fig. 17. Measured noise figure for the five frequency configurations in HG mode. Most of them are lower than 3 dB.

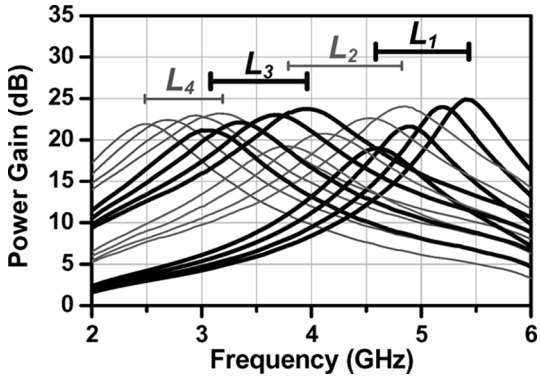

Fig. 18. Continuous frequency tuning with coarse inductor switching and fine varactor tuning.

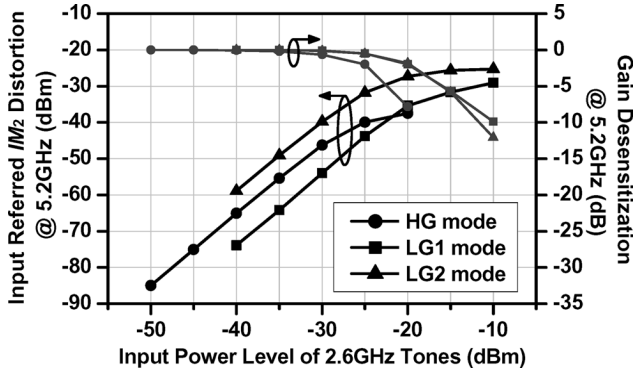

Fig. 19. Measurement result of the second-order intermodulation distortion and the gain desensitization at 5.2 GHz because of the 2.6 GHz interferers.

$$\max\left\{\frac{\omega_{\max}}{\omega_{\min}}\right\} = \sqrt{1+\frac{C_1}{C_2}}. \tag{21}$$

Therefore, the primary factor limiting the achievable frequency tuning ratio in the proposed switching inductor is identified to be C_2/C_1 ratio, and can be designed according to (21).

C. Switching Inductor Design of This LNA

The switching inductor in this project is implemented by a spiral inductor with three additional tapping points, as shown in Fig. 12. The simulation results with the designed switches are shown in Fig. 13. The bold faced section of the inductances and quality factors correspond to the sub-bands they are employed. The proposed switching configuration improves the quality factor, allows a smaller size of the SW_1 and SW_2, and ensures the quality factor increased as the inductance switched smaller for higher frequency operation. The C_2 for (15) is the parasitic capacitance of SW_4 in OFF state as 115 fF, leading to a quality factor boosting at about 4.5 GHz. The quality factors for each sub-band has been quite close to the required profile depicted in Fig. 6, except the local profiles of inductance L_1 and L_2 affected by the boosting. As to the frequency tuning ratio, the C_1 and C_2 for (21) are, respectively, 324 $\sim$ 592 and 115 fF, in which the C_1 is a variable capacitance. The actual designed

TABLE III
PERFORMANCE SUMMARY

Frequency (GHz)	2.40			3.43			3.96			4.49			5.40		
Performance Mode	HG	LG_1	LG_2	HG	LG_1	LG_2	HG	LG_1	LG_2	HG	LG_1	LG_2	HG	LG_1	LG_2
S_{11} (dB)	-14	-20	-20	-30	-18	-18	-28	-16	-16	-18	-14	-14	-17	-16	-18
S_{22} (dB)	< -18dB														
Peak S_{21} (dB)	22.1	10.5	10.2	22.6	10.5	10.0	24.0	11.7	11.0	22.6	10.9	9.95	24.8	13.3	12.0
S_{21} BW_{3dB} (MHz)	740	780	790	820	910	900	850	1010	1010	850	920	900	500	540	530
NF (dB)	2.8	4.3	3.9	2.2	4.4	3.9	2.4	4.6	4.0	2.5	4.8	4.5	3.1	4.9	4.4
IIP_3 (dBm)	-18.2	-11.2	-10.5	-15.3	-10.3	-10.2	-18.5	-10.1	-9.7	-18.7	-11.0	-11.0	-20.4	-11.5	-12.3
IIP_2 (dBm)	HG: -15.0 dBm; LG_1: -5.8 dBm; LG_2: -20.9 dBm														
Technology	TSMC 0.13μm RF CMOS process with UTM														
DC Power of 2nd Stage	HG: 2 mW; LG_1: 1 mW; LG_2: 0.5 mW														
Total DC Power (mW)	HG: 4.6 mW; LG_1: 3.6 mW; LG_2: 3.1 mW (1.0V supply voltage, buffer stage excluded)														

frequency tuning ratio in this LNA is 2.3 with sub-bands overlapped, which ensures a full coverage over the entire tuning range and a less than 3-dB gain variation.

IV. Chip Implementation and Measurement Results

This LNA is designed with 1.0 V supply voltage and fabricated in TSMC 0.13 μm RF CMOS process. Fig. 14 shows the micrograph of the LNA under test. The core circuit without pads occupies 0.49 mm^2 chip area. RF signals are measured with on-wafer probing while all dc voltage is provided via bonding wires. In the test cases, small signal S-parameters are obtained with Agilent 8364B network analyzer, and noise figure from Agilent 8974A noise figure analyzer with cable loss compensation. Two-tone tests are performed to test the linearity performances of IIP_2 and IIP_3. The accurate power level at LNA input is calibrated by use of a power meter.

Performances of this LNA are measured in three configured performance modes in five frequency bands, carrying out 15 test cases. The five frequency bands include the designed upper and lower tuning limits and three MB-UWB mode-1 bands, listed as 2.4, 3.43, 3.96, 4.49, and 5.4 GHz. The performance modes include one 20-dB high-gain mode (HG) and two 10-dB low-gain modes (LG_1, and LG_2), representing the three operation modes shown in Fig. 1, in which the LG_1 mode is for better linearity, whereas the LG_2 mode toward the lowest power consumption.

The S-parameter test results are shown in Figs. 15 and 16. The broadband input/output reflection performances for the 15 configurations are successfully kept consistent. The power gains at the HG mode are in the range from 22 to 25 dB whereas at the LG_1 and the LG_2 modes from 10 to 13 dB. Gains at different frequency bands for each gain configuration are within 3-dB variation and approximately consistent. Noise figures are lower than 3.1 dB for HG mode and lower than 5 dB for LG_1 and LG_2 modes. The tested curves for the HG mode are shown in Fig. 17 as representative. The capability of continuous frequency tuning is verified as shown in Fig. 18, in which L_1 to L_4 represent the different switched inductance values.

The linearity of this LNA is characterized by the two-tone test for IIP_2 and IIP_3. For the IIP_2 test two CW interferer tones are input at the frequencies of 2.599 and 2.601 GHz, while the LNA is configured to operate at 5.2 GHz where the IM_2 lands. The output IM_2 is measured and referred to the input by dividing the measured power gain at 5.2 GHz to calculate the corresponding IIP_2. The measurement results are shown in Fig. 19, in which the gain desensitization at 5.2 GHz due to the two 2.6 GHz interferers is also included. The measured IIP_2 and IIP_3 both range from -21 to -5 dBm, depending on which gain mode is chosen. The IIP_2 control for the three gain modes is consistent with the design in Fig. 4.

The measured performance is summarized in Table III. The performance corner matrices are shown in Figs. 20 and 21, using

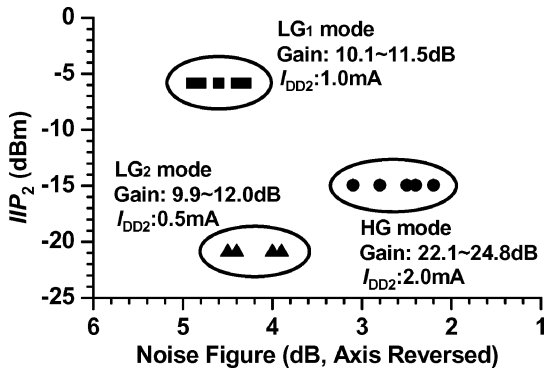

Fig. 20. Performance corner matrix with IIP_2 as the linearity indicator.

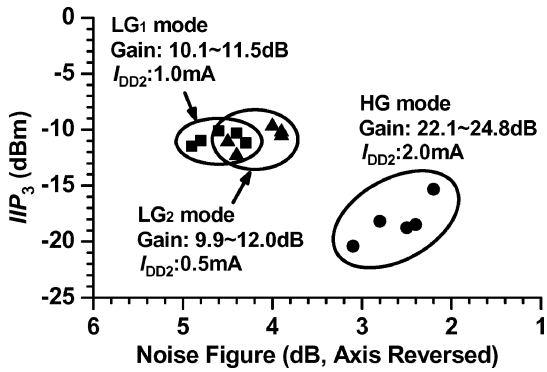

Fig. 21. Performance corner matrix with IIP_3 as the linearity indicator.

TABLE IV
COMPARISON OF LNAS FOR MULTISTANDARD APPLICATIONS

Ref.–Year	Technology	Frequency Response of S_{11} / S_{21} [a]	Frequency Coverage (GHz)	S_{21} Bandwidth (GHz)	Noise Figure (dB)	Max. S_{11} (dB)	Gain (dB)	Vari.Gain Range (dB)	IIP_3 (dBm)	Max. Power (mW)
[8] –2005	0.13μm CMOS	BB / BB	DC – 6.5	6.5	2.9 – 4.2	-10	19	N/A	+1	11.7
[18] –2006	0.18μm BiCMOS	BB / BB	1.5 – 2.2	> 2.2	1.5 – 1.9	-14	16.2 – 17	N/A	+2	26
[5] –2007	90nm CMOS	BB / BB	DC – 6.0	6.0	2.5 – 3.2	-10	17.4	N/A	N/C	9.8
[6] –2007	0.13μm CMOS	BB / BB	1.0 – 7.0	7.0	2.4 – 3.0	-10	17	N/A	-4.1	25
[7] –2007	90nm CMOS	BB / BB	0.5 – 7.0	7.5	2.3 – 2.9	-7.2	22	N/A	-10.5	12
[19] –2007	0.18μm CMOS	BB / MB	0.95/2.4/5.25	0.5/2.5/1.0	4.4 – 4.6	-7/-15/-10	18/24/23	N/A	-12.8 – -15.3	32.4
[20] –2006	0.35μm SiGe	MB / TSB	2.4/4.9–5.9	1.0	2.9/3.1–3.6	-17.5	20 – 29	N/A	-13 – -18	16
[9] –2005 [b,c]	0.25μm SiGe	BB / TSB	4.9 – 5.8 [d]	0.7	2.3 – 2.5 [b]	-10	31 – 31.5 [b,c]	11 [b]	-9.5	40 [b]
[10] –2006 [b]	0.13μm CMOS	BB / TSB	1.8/2.1/2.4	0.4/0.6/0.5	5.2/5.6/5.8 [b]	-20	23.4 – 29.5 [b,c]	15 [b]	-7.5 – 0	24 [b]
[21] –2007	0.18μm CMOS	BB / TSB	0.9/1.8/5.2	0.2/0.4/0.6	2.3 – 2.9	-12	13 – 16	N/A	-14	7.5
This work [13] [c]	**0.13μm CMOS**	**BB / TSB**	**2.4 – 5.4 [d]**	**0.5 – 1.0**	**2.2 – 3.1**	**-12**	**22 – 24**	**12**	**-16 – -21**	**4.6**

[a] In frequency response, BB: broadband, MB: concurrent multiband, TSB: tunable/switchable single band.
[b] Performance of entire receiver front-end including LNA and quadrature mixer.
[c] Performance in high gain mode as representation. [d] Continuous frequency tuning.

IIP_2 and IIP_3 as the linearity indicator, respectively. Performances at the five representative frequencies with the same performance configuration are grouped. With the linearity control on IIP_2 the Fig. 20 shows a nearly consistent result as illustrated in Fig. 1. Therefore the performance reconfiguration conducted by switching transistor with bias control is verified. Finally, Table IV compares works of multistandard LNAs published to date.

V. CONCLUSION

A 2.4–5.4-GHz wide tuning-range performance reconfigurable LNA is demonstrated. The broadband input stage is verified to be adequate in providing steady input matching and noise performance. The performance reconfiguration on gain, linearity, and power consumption is achieved. By use of the proposed inductance switching configuration, the multitapped switching inductor can be well designed to provide wide tuning range with good performance consistency. The proposed switching configuration is advantageous with the quality factor boosting but suffers from limited frequency tuning ratio. This limitation has been identified and the design reference is given in (21). As a result, this prototype has proven the high performance flexibility and wide-range tuning of LNA within the below-average low power consumption.

APPENDIX

As the L_X in Fig. 10 is switched to $L_{X,\mathrm{MIN}}$, the Z_{tank} can be derived as

$$Z_{\mathrm{tank}}\big|_{L_{X,\mathrm{MIN}}} = \frac{j\omega L_1\left[1-\omega^2(1-k^2)L_2C_2\right]}{1-\omega^2\left(L_1C_1+L_2C_2\right)+\omega^4(1-k^2)L_1C_1L_2C_2} = \frac{j\omega L_1[1-\omega^2(1-k^2)L_2C_2]}{[1-\omega^2(1-k^2)L_2C_2](1-\omega^2L_1C_1)-\omega^2k^2L_2C_2} \quad \text{(A1)}$$

in which two poles and one zero can be found on the positive ω-axis. The two poles are located at frequencies as solved in (20). We can determine which pole frequency is our case by testing their continuity to $\omega_{\min}$ as $L_{X,\mathrm{MIN}}$ is approaching $L_{X,\mathrm{MAX}}$, by setting $L_1 \to L_{X,\mathrm{MAX}}$ and $L_2 \to 0$. In this test the higher pole frequency can be found approaching infinity whereas the lower pole meets the $\omega_{\min}$. Therefore the minus sign is applied in (20).

There are two singular cases not applicable to the above discussion, $k = 0$ and $k = 1$. In the case of $k = 0$, i.e., no mutual coupling between coil sections, the pole dominated by L_2C_2 is cancelled by the zero in (A1) so that the resonance frequency is determined only by L_1C_1. Thus the frequency tuning ratio discussed in Section III-B is unlimited as the L_1 can be designed arbitrarily small. In the case of $k = 1$, the denominator in (A1) is diminished contributing only one pole, which makes the $\omega_{\max}$ in Section III-B to be

$$\omega_{\max}\big|_{k=1} = \frac{1}{\sqrt{L_1C_1+L_2C_2}}. \quad \text{(A2)}$$

Given a fixed $L_{X,\mathrm{MAX}}$, the achievable frequency tuning ratio in this case is limited by the complementary relationship between L_1 and L_2 in (16). These two special cases, though not practical to this work, also roughly show how the mutual coupling affects the frequency tuning ratio in the use of the proposed switching inductor.

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