

氧化鈰奈米微晶粒非揮發性

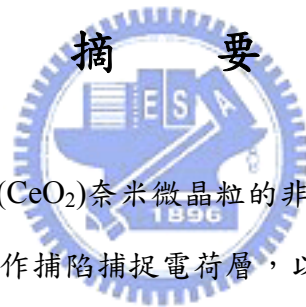
記憶體元件之研究

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此論文主要製作氧化鈰(CeO_2)奈米微晶粒的非揮發性快閃記憶體，將使用不同的退火條件製程方法來製作捕陷捕捉電荷層，以取代現今傳統氮化矽 (Si_3N_4) 材料。在低電壓下來操作快閃記憶體元件使用不同的寫入/抹除的操作方式。達成電荷捕捉效率佳、有快速的寫入/抹除速度、大的記憶窗口、儲存資料持久性、以及寫入、清除操作造成的性能退化少的非揮發性快閃記憶體。

首先，我們利用氧化鈰奈米微晶粒當作捕陷電荷層來製做SONOS型非揮發性快閃記憶體。此氧化鈰奈米微晶粒快閃記憶體元件在一萬次的寫入/抹除下，仍然擁有好的儲存資料持久性、和寫入、清除操作造成的性能退化少。其電荷儲存方式亦可以很區域性的，利用元件製作的對稱性使其一個單元儲存2個位元，達到高密度之優點，適用於相關記憶體元件及半導體產業中。

其次，沉積氧化鈰薄膜隨著後處理環境的不同來作為捕陷電荷層製作SONOS型非揮發性快閃記憶體。我們發現到隨著退火的環境的差異，氧化鈰奈米微晶粒會產生的不同深能量的捕陷電荷，造成儲存資料持久性變化但是基本電

性的寫入、清除操作的性能沒有太大變化。此為退火的環境的差異下造成不同結晶額外產生的淺能量的捕陷電荷所造成。

接著，我們使用堆疊結構的穿隧氧化層來取代傳統的二氧化矽氧化層，同樣使用氧化鈣奈米微晶粒當作捕陷電荷層來製做非揮發性快閃記憶體。主要在於改善記憶體元件在清除操作造成的二氧化矽氧化層性能退化而影響其電性。

在論文的最後，我們針對記憶體元件的寫入、清除操作在基板浮接情況下，其元件操作上的差異性，在寫入操作可以降低 1 伏特電壓亦可有相同的操作數目，對於資料保存特性不會有很大的影響。也利用電荷汲引技術(Charge-Pumping technology)，來觀察不同的寫入操作模式在 SONOS 記憶體元件的邊緣缺陷(border traps)進行分析。



Characteristics of Cerium Oxide Nanocrystal Nonvolatile Memory Devices

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In this thesis, we utilize cerium oxide nanoparticle as a charge-trapping layer to fabricate nonvolatile memory. The cerium oxide nanocrystals formed self-assembled under different rapid-thermal annealing (RTA) ambient. This high-k nanocrystals layer replaces the silicon nitride layer in the SONOS-type memory structure. Different program/erase (P/E) methods are also proposed low power applications. This nanocrystals nonvolatile memory device will have good properties in terms of considerably large memory window, higher P/E speed, long data retention, and good endurance.

First, we present a nonvolatile SONOS-type flash memory that using cerium oxide (CeO_2) nanocrystals as the trapping storage layer. These CeO_2 nanocrystal memories exhibit long data retention, and good reliability, even for the cells subjected to 10k P/E cycles. These features suggest that such cells are very useful for high-density two-bit nonvolatile flash memory applications.

Then, we demonstrate the effects of the post-deposition different annealing ambient for the CeO_2 trapping layer on the performance of SONOS-type flash memories. It was found that the CeO_2 nanocrystals memory with different retention time caused by annealing ambient influence the deep-trapping level. However, the basic electrical operation characteristics are similar. This was ascribed to the larger amount and the shallower energy levels of the crystallization-induced traps. Finally, in the aspect of disturbances, we show only insignificant disturbances properties presented in the normal operation.

Next, we utilized the stack tunneling layer to replace conventional SiO_2 tunneling layer. A nonvolatile SONOS-type flash memory device also used CeO_2 nanocrystals as a charge trapping layer. It was demonstrated that the fabricated memories exhibit

higher program/erase speed and long retention time. In particular, two-bit per cell operation has been successfully demonstrated.

Finally, we study nonvolatile CeO_2 nanocrystal memory with no body contact (substrate floating). The operating voltage can reduce 1 V at program mode. Nevertheless, the data retention is similar. We also measure charge-pumping current for different programming methods to observe the SONOS-type memory border traps.



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Contents

Abstract (in Chinese)	I
Abstract (in English)	III
Acknowledgements (in Chinese)	V
Contents	VII
Figure Captions and Table Lists	X
Chapter 1 Introduction	1
1.1 Background.....	1
1.1.1 Overview of cerium oxide.....	1
1.1.2 Overview of nonvolatile memory.....	1
1.2 Motivation.....	7
1.3 Thesis Organization	10
Chapter 2 Cerium oxide nanocrystals for nonvolatile memory application and two-bits operation	19
2.1 Introduction	19
2.2 Experimental	20
2.3 Results and Discussion.....	22
2.3.1 Material analysis of CeO ₂ nanocrystals.....	22
2.3.2 Electrical characteristics.....	22
2.3.3 Two-bit per cell operation.....	24
2.4 Summary.....	29

Chapter 3 Annealing ambient effects on the performance of CeO₂ nanocrystal memory.....	47
3.1 Introduction	47
3.2 Experimental	49
3.3 Results and Discussion.....	49
3.3.1 Material Analysis.....	49
3.3.2 Device operation characteristics.....	50
3.3.3 Comparison of different annealing ambient.....	51
3.4 Summary.....	53
Chapter 4 Characteristics of CeO₂ nanocrystals on O/N tunnel layer nonvolatile memory.....	66
4.1 Introduction	66
4.2 Experimental	67
4.3 Results and Discussion.....	68
4.3.1 Material analysis of CeO ₂ nanocrystals on Si ₃ N ₄	68
4.3.2 Electrical Characteristics	69
4.4 Summary.....	71
Chapter 5 Substrate effects and Charge-Pumping characteristics for CeO₂ nonvolatile nanocrystal memory.....	80
5.1 Introduction	80
5.2 Substrate floating effects.....	81
5.3 Charge pumping characteristics.....	83
5.4 Summary.....	85

Chapter 6 Conclusions and Further Recommendations..... 101

6.1 Conclusions.....101

6.2 Further Recommendations.....103

References.....104

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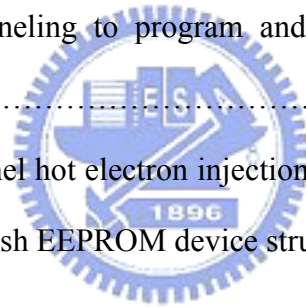
Publication list



Figure Captions

Chapter 1

Fig. 1-1 The semiconductor memory tree.....	12
Fig. 1-2 (a) Charge trapped in floating gate. (b) I-V characteristics of a memory device in the programmed and erased state. Threshold voltage shifted when the charges are trapping in floating gate.....	13
Fig. 1-3 The typical floating gate (FG) memory device structure.....	14
Fig. 1-4 (a) Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) memory cell structure. (b) Band gap diagram of Silicon-Oxide-Nitride-Oxide-Silicon structure.....	15
Fig. 1-5 The Drain-side tunneling to program and erase EEPROM memory cell structure.....	16
Fig. 1-6 The Drain-side channel hot electron injection to program and source-side FN tunneling to erase Flash EEPROM device structure.....	17



Chapter 2

Fig. 2-1 Schematic representation of CeO ₂ nanocrystal flash memory devices with main process conditions. CeO ₂ nanocrystals were formed by RTA 900°C in O ₂ ambient for 60 s.....	31
Fig. 2-2 HRTEM Cross-sectional images of CeO ₂ nanocrystal trapping layers with TO thickness of 4.0 nm. The average nanocrystal size was ca. 8-10 nm and obviously visible lattice fringes indicated crystallization of inside nanocrystals.....	32
Fig. 2-3 AFM image of CeO ₂ nanocrystals; white dots indicate the formation of CeO ₂ nanocrystals after O ₂ RTA at 900°C. The nanocrystal density was ca. 5 × 10 ¹¹	

cm⁻² and the average nanocrystal space was ca. 14 nm, which ensures the electrical insulation between two nanocrystals.....33

Fig. 2-4 I_{ds} - V_{gs} curves of CeO₂ nanocrystal memory cell under different programming and erasing conditions. The channel width and length of the memory devices were respectively measured to be 10 and 0.35 μm, at which the thickness of the TO is 4.0nm. A memory window with a voltage larger than 3.1 V can be achieved at $V_g = V_d = 9$ V.....34

Fig. 2-5 Programming speed characteristics of CeO₂ nanocrystal flash memory devices with different TO thicknesses and programming conditions as function of time. A memory window of ca. 5 V was achieved at $V_g = V_d = 10$ V, and the working time was determined to be 1 ms in programming operation.....35

Fig. 2-6 Erasing speed characteristics of CeO₂ nanocrystal flash memory devices with (a) TO=2.5 nm and (b) TO=4.0 nm under different erasing conditions as function of time. An excellent erasing speed of around 1 ms was obtained and a little overerasing was observed.....36

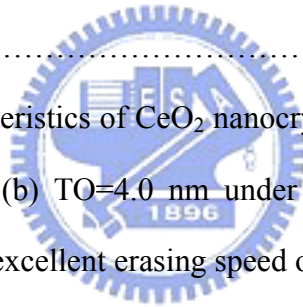


Fig. 2-7 Schematic cross-sectional structure of CeO₂ nanocrystal localized charge storage memory cell with programming by CHE injection. Bit-D: drain side; Bit-S: source side. Each memory cell stored two-bit for a high-density flash memory device.....37

Fig. 2-8 I_{ds} - V_{gs} curves with CeO₂ nanocrystal memory devices demonstrated two-bit per cell operation. Two schemes for reading the four states of these were used. These schemes are the forward and reverse read schemes for recognizing the information stored in the program states of Bit-D and Bit-S, respectively.....38

Fig. 2-9 The schematic illustration of disturb condition. Cell A is the programming

cell. Cell B and C are the drain disturbance and gate disturbance, respectively.....	39
Fig. 2-10 Read disturbance characteristics of CeO ₂ nanocrystal flash memory devices with different TO thicknesses. No significant V_{TH} occurred at $V_d < 3$ V, even after 1000 s at $T = 25^\circ\text{C}$	40
Fig. 2-11 Gate disturbance characteristics of the CeO ₂ nanocrystal memory devices with two different tunnel oxide thickness samples. After 1000 sec at 25°C , small 0.6V gate disturb margin was observed.....	41
Fig. 2-12 Drain disturbance characteristics of the CeO ₂ nanocrystal memory devices with two different tunnel oxide thickness samples.....	42
Fig. 2-13 Retention characteristics of CeO ₂ nanocrystal flash memory devices for (a) different programming states and temperatures, and (b) different TO thicknesses and temperatures.....	43
Fig. 2-14 Endurance characteristics of CeO ₂ nanocrystal memory devices. The P/E window with a thick TO does not show any closure even after 10^5 cycles compared with that with a thin TO.....	44
Fig. 2-15 Lateral charge migration characteristics of CeO ₂ nanocrystal flash memory cell after 10k P/E cycling.....	45

Chapter 3

Fig. 3-1 Schematic representation of CeO ₂ nanocrystal flash memory devices with main process conditions.....	55
Fig. 3-2 Cross-sectional TEM images of the CeO ₂ nanocrystals embedded in SiO ₂ dielectric matrix. (a)without RTA process; (b) with RTN ₂ annealing at 900°C for 1 min; (c) with RTO ₂ annealing at 900°C for 1 min, where the average nanocrystal size was 8-10 nm and obviously visible lattice fringes indicated	

crystallization of nanocrystals.....	56
Fig. 3-3 Ideal energy band diagram for CeO ₂ nanocrystal SONOS-type structures.	57
Fig. 3-4 Programming speed characteristics of CeO ₂ nanocrystal flash memory devices with different programming conditions as a function of time. The fact the programming speed is independent of annealing condition of the charge trapping centers, indicating that the programming speed is primarily dependent on the tunneling oxide.....	58
Fig. 3-5 The erasing speed characteristics of the CeO ₂ nanocrystal memory cell at different erasing voltages. As observed, an increase in the negative gate bias resulted in a high erasing speed due to a higher electrical field for the BBHH injection.....	59
Fig. 3-6 Retention characteristics of CeO ₂ nanocrystal flash memory devices with different RTA treatments and programming states.....	60
Fig. 3-7 The endurance characteristics of CeO ₂ nanocrystal flash memory devices with two different treatment devices. The memory window of the NC devices does not show any closure behavior even after 10 ⁴ P/E cycles.....	61
Fig. 3-8 Read disturbance characteristics of CeO ₂ nanocrystal flash memory devices with different annealing ambient. (a) with RTN ₂ at 900°C for 1 min; (b) with RTO ₂ at 900°C for 1 min. No significant V _{TH} occurred at V _d < 3 V, even after 1000 s at T = 25°C.....	62
Fig. 3-9 Drain disturbance characteristics of the CeO ₂ nanocrystal memory devices with two different annealing ambient. (a) with RTN ₂ at 900°C for 1 min; (b) with RTO ₂ at 900°C for 1 min. No significant V _{TH} occurred at RTN ₂ sample, even after 1000 s at T = 25°C.....	63
Fig. 3-10 I _{ds} -V _{gs} curves with CeO ₂ nanocrystal memory devices demonstrated two-bit per cell operation. (a) with RTN ₂ at 900°C for 1 min; (b) with RTO ₂ at 900	

°C for 1 min. Two schemes for reading the four states of these were used.64

Chapter 4

- Fig. 4-1 Schematic representation of CeO₂ nanocrystal flash memory devices on O/N tunneling layer with main process conditions.....72
- Fig. 4-2 Cross-sectional TEM images of the CeO₂ nanocrystals embedded in Si₃N₄ dielectric matrix with (a) RTN₂ annealing at 900°C for 1 min; (b) RTO₂ annealing at 900°C for 1 min.....73
- Fig. 4-3 (a)Programming speed and (b) erasing speed characteristics of CeO₂ nanocrystal flash memory devices with RTO₂ annealing as a function of time.....74
- Fig. 4-4 (a)Programming speed and (b) erasing speed characteristics of CeO₂ nanocrystal flash memory devices with RTN₂ annealing as a function of time.....75
- Fig. 4-5 Retention characteristics of CeO₂ nanocrystal flash memory devices at programming states with different treatments.76
- Fig. 4-6 Endurance characteristics of CeO₂ nanocrystal memory devices with different annealing ambient. The P/E window with two samples do not show any closure even after 10⁴ cycles.....77
- Fig. 4-7 I_{ds} - V_{gs} curves with CeO₂ nanocrystal memory devices demonstrated two-bit per cell operation at RTN₂ annealing. These schemes are the forward and reverse read schemes for recognizing the information stored in the program states of Bit-D and Bit-S, respectively.....78

Chapter 5

- Fig. 5-1 Illustration of flash memory can be operated $V_g=V_d$ for channel hot electrons injection to program and no body contact (substrate is floating). Parasitical

n-p-n bipolar increased drain avalanche to enhance hot electrons.....	87
Fig. 5-2 (a) I_d-V_d curve of CeO ₂ nanocrystal memory devices with different body contact condition. After sweep I_d-V_d , (b) the threshold voltage shift with floating body is larger than $V_b = \text{GND}$	88
Fig. 5-3 I_d-V_d curve of CeO ₂ nanocrystal memory devices with (a) body is floating and (b) body is ground. Parasitical bipolar device early increased drain current at body is floating.....	89
Fig. 5-4 Program speed characteristics of CeO ₂ nanocrystals memory devices with different programming conductions and no body contact (substrate floating). The mechanism is due to the floating body induced drain avalanche with parasitic n-p-n bipolar in the flash memory device.....	90
Fig. 5-5 Erasing speed characteristics of CeO ₂ nanocrystals memory devices with different erasing voltage conductions and no body contact (substrate floating).....	91
Fig. 5-6 Retention characteristics of CeO ₂ nanocrystals memory devices at (a) T=25°C and (b) 85°C with/without body contact.....	92
Fig. 5-7 Drain disturbance characteristics of the CeO ₂ nanocrystals memory devices with/without body contact at (a) erasing state; (b) programming state.....	93
Fig. 5-8 Endurance characteristics of the CeO ₂ nanocrystals memory devices with/without body contact after 10 ⁴ cycles.....	94
Fig. 5-9 Schematic diagrams the flash memory cell setup for charge-pumping measurement.....	95
Fig. 5-10 Schematic diagrams illustrating (a) the pulse waveform and (b) the stepping pulse base voltage with fixed pulse amplitude for charge-pumping measurement.....	96
Fig. 5-11 Conventional charge-pumping current versus base voltage with different	

pulse amplitude voltage.....97

Fig. 5-12 (a) Rise time dependence of charge-pumping curves for fixed fall time of 100ns, respectively. (b) Fall time dependence of charge-pumping curves for fixed rise time of 100ns conduction.....98

Fig. 5-13 (a) I_d - V_g curves of the CeO₂ nanocrystal nonvolatile memory at different programming state under FN-programmed method to operate and (b) the charge-pumping current versus base voltage under FN-programmed method.99

Fig. 5-14 (a) I_d - V_g curves of the CeO₂ nanocrystal nonvolatile memory at different programming state under CHE-programmed method to operate and (b) the charge-pumping current versus base voltage under CHE-programmed method.....100



Table Lists

Chapter 1

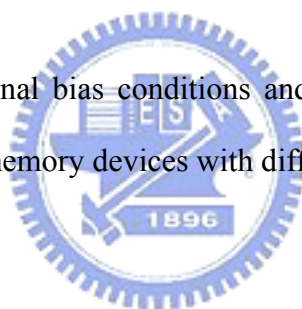
Table. 1-1 Tunnel oxide and operation voltage scaling predicted by 2007 International Technology Roadmap for Semiconductors.....	18
--	----

Chapter 2

Table. 2-1 Summary of terminal bias conditions and operation principles for CeO ₂ nanocrystal flash memory cell (unit: V).....	47
---	----

Chapter 3

Table. 3-1 Summary of terminal bias conditions and operation principles for CeO ₂ nanocrystal flash memory devices with different annealing (unit: V).....	65
---	----



Chapter 4

Table. 4-1 Summary of terminal bias conditions and operation principles for CeO ₂ nanocrystal with RTN ₂ annealing on O/N tunnel layer nonvolatile memory cell (unit: V).....	79
---	----