Chapter 1

Introduction

1-1 Background

1-1.1 Overview of cerium dioxide

In recent years, cerium dioxide (CeO_2) has been extensively worked on the research of it to be the buffer layer for $YBa_2Cu_3O_{(7-x)}$ (YBCO) on sapphire[1.1], an electrolyte material of solid oxide fuel cells[1.2-1.3], buried insulator for silicon-on-insulator (SOI)[1.4] and $PbZrTiCeO_3$ (PZT) ceramics[1.5], is used for gate dielectric materials lately[1.6], etc. Epitaxial CeO_2 thin films are currently of interest for diverse applications in several key areas of thin film technology ranging from semiconductors to superconductors and solid oxide fuel cells. CeO_2 has the cubic fluorite-type crystal structure (lattice spacing 0.5411 nm) and its material properties combine a large band gap (~6 eV) with a high dielectric constant (~26), [1.7-1.8] high ionic conductivity and high-temperature stability. Many studies on optical properties have been performed for single [1.9] and poly [1.10] crystals, as well as thin films [1.11-1.14] of cerium oxides. However, few optical investigations of nanocrystalline particles exist. [1.15-1.18]

1-1.2 Overview of nonvolatile memory

Nowadays, semiconductor flash memories are widely used in modern electronic systems, such as personal computers, cell phones, personal digital assistants, and digital cameras, etc. Memory chips with low power consumption and low cost have attracted more and more application due to portable electronic devices such as MP4, MP3 player, cell phones and digital cameras. Memory can be split into two main categories: volatile and nonvolatile. Volatile memory loses any data as soon as the system is turned off; it requires constant power to remain viable. Figure 1-1 shown the semiconductor memory tree. Most types of random access memory (RAM) such as DRAM (Dynamic Random Access Memory) and SRAM (Static Random Access Memory) fall into this category. Nonvolatile memory included ROM (Read-Only-Memory), EPROM (Electrically Programmable Read Only Memory), and EEPROM (Electrically Erasable Programmable ROM) do not lose its data when the system or device is turned off. These require the memory to have ten years data retention time, so that the nonvolatile memory devices have become indispensable.

S. M. Sze and D. Kahng, proposed the first floating-gate (FG) nonvolatile semiconductor memory in 1967. The gate stack consists of an 8nm thermal oxide as the tunnel layer, a 150nm poly-silicon floating gate and a 13nm (EOT) inter-poly oxide layer. The EOT of the whole gate stack is 21nm. The conventional FG memory used polycrystalline silicon as a charge storage layer surrounded by the dielectric

shown in Fig. 1-2(a). Figure 1-2 (b) was shown that storage of the charge on the floating gate allows the threshold voltage (V_T) to be electrically altered between a low and a high value to represent logic 0 and 1, respectively. The first gate is the floating gate that is buried within the gate oxide and the inter-polycrystalline silicon dielectric (IPD) beneath the control gate is show in Fig 1-3. The IPD isolates the floating gate and can be oxide or oxide-nitride-oxide, ONO. The SiO_2 dielectric surrounding the transistor serves as a protective layer from scratches and defects. The second gate is the control gate which is the external gate of the memory transistor. Floating gate devices are typically used in EPROM (Electrically Programmable Read Only Memory) and EEPROM (Electrically Erasable and Programmable Read Only Memory).

The FG structure can achieve high densities, good program/erase speed and good reliability for Flash memory application. However, the FG memory has several drawbacks. First, the Flash memory needs thick tunnel oxide (8~10nm) to provide superior retention and endurance characteristics, so it causes high operation voltage, slow P/E speed, and poor scalability. Second, because the polycrystalline silicon floating-gate is conductive, the total charges stored in floating-gate will be easily leaked directly through the tunnel oxide when the tunnel oxide is damaged during P/E cycles. In order to improve the write/erase speed of a floating-gate device, the thickness of the tunnel oxide must be reduced. The tunnel oxide must be less than

25Å in order to achieve 100 ns write/erase time for a reasonable programming voltage (<10 V). Unfortunately, the retention time will be too short. Stress- induced leakage current (SILC) will further degrade the retention time.

The floating gate memory requires thick tunnel oxide to prevent charge loss through the defect. In order to solve the scaling issue of FG memory, the Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) memory has been studied recently. SONOS memory has better charge retention than floating gate memory when floating gate tunneling oxide is below 10nm due to its isolated deep-level traps. Hence, a leakage path in the tunneling oxide will not cause the discharge of the memory cell. The structure of SONOS memory is shown in Fig. 1-4 (a). The SONOS memory uses silicon nitride as charge trapping layer, and the band diagram is shown in Fig. 1-4(b).

In the SONOS memory, electrons are stored in the physically discrete traps (labeled with the trap energy level of E_t) below the nitride conduction band. In this device, the electrons cannot move freely between the discrete trap locations, hence the SONOS memory device is very robust against the defects inside the tunnel oxide and has better endurance than the floating gate flash memory. Electrons can be thermally de-trapped into the nitride conduction band and then tunnel back to the channel. This thermal de-trapping rate is exponentially reduced with a deep trap energy level. For these reasons, the SONOS flash memory can have much better retention time than the

floating gate flash memory. A tunnel oxide of 3nm is thick enough to guarantee 10 years retention time in the SONOS flash memory. When we apply a positive voltage on the gate, the band will bend downward, the electrons in the Si-sub conduction band will tunnel through the tunneling oxide and trapped in the charge trapping layer. Before electrons are trapped in the nitride, they must degrade the program speed. Besides this, the trapped electron back tunneling may also occur. To solve these problems, the high-k materials are the possible candidates to replace the traditional silicon nitride as charge trapping layer.

EPROM is the first one that can program the memory cell by electrical method. Generally, it programs the memory cell by using channel hot electron (CHE) that was injected into floating gate. However, EPROM can't erase by electrical method. Illuminate the UV light erases it. So a quartz window is necessary on the package of the EPROM. However illuminate the UV light will erase entire memory cell; we can't select the cell which we want to erase it. Figure 1-5 was shown the drain-side tunneling to program and erase EEPROM memory cell structure. The appearances of EEPROM solve the problem of EPROM that we described above. It can both program and erase by electrical method. But in order to achieve this merit, a select transistor is needed. So the memory cell density of EEPROM is lower than the EPROM. This shortage let the EEPROM only apply in lower storage capacity equipment. Flash

memory follows the basic structure of EPROM. It can both program and erase by electrical method, but the select transistor isn't needed. So the memory cell size of flash memory is smaller than EEPROM. For this reason, it have huge amount of competitiveness in memory market.

Figure 1-6 shows the drain-side tunneling to program and source-side tunneling to erase Flash EEPROM device structure. There are mainly four types of nonvolatile memory technology: flash memory, Ferro-electric Random Access Memory (FeRAM), Magnetic Random Access Memory (MRAM) and phase change memory. Flash memory is presently the most suitable choice for nonvolatile applications for the following reasons:

(1) Flash memory can achieve the highest chip density. A flash memory cell consists of only one transistor [1.19].

(2) Flash memory possesses the multi-bit per cell storage property [1.20]. Two-bits/cell (with four V_T states) flash memory cells have already been commercialized.

(3) Flash memory fabrication process is compatible with the current CMOS process and is a suitable solution for embedded memory applications.

Since flash memory possesses these three key advantages, it has become the mainstream nonvolatile memory device nowadays. However, flash memory exhibits

some evident disadvantages that the device has a slow program/erase speed and requires a high voltage to program/erase its data. Additionally, its endurance also needs to be improved, although 10^5 program/erase cycles is enough for most applications. This thesis will investigate several ways to improve the program/erase speed and reduce the operation voltage.

The scaling of the gate stack and operation voltages is often related to each other. A tunnel oxide thickness of more than 8nm is currently used in the commercial flash memory chip to meet the ten years data retention time requirement. If the tunnel oxide were to be scaled below 2nm, the operation voltage could be reduced from more than 10V to below 4V [1.21]. Unfortunately, the retention time would also be reduced, from 10 years to several seconds. Table 1.1 shows the 2005 International Technology Roadmap for Semiconductor flash memory [1.22]. The channel length of the NOR type flash memory will still be longer than 100nm by the year 2016. Short channel effects prevent the channel length from being aggressively scaled. The operation voltage and the tunnel oxide will not scale at all in the coming five technology generations.

1-2 Motivation

In this thesis the aforementioned topic of cerium oxide nanocrystal application

for charge trapping layer of semiconductor flash memory is compatible with the current CMOS process flow. This nonvolatile memory structure will have superior characteristics in terms of considerably large memory window, high speed program/erase, long retention time, and excellent endurance. We discuss the cerium oxide of semiconductor nanocrystal memory devices. The nanocrystal charge-trapping layer can be fabricated by annealing high-k materials, such as CeO_2. After applying a rapid thermal anneal process to self-assemble CeO_2 nanocrystals are formed and blocking oxide (BO) was deposited using a low-pressure tetraethoxysilane system surrounded by SiO_2. The stored charges will be trapped in/around the nanocrystals and isolated by silicon dioxides. Less opportunity of charge loss is expected.

For the memory device operation, we use channel hot-electron injection for the programming and band-to-band hot-hole injection for the erase. Staying in oxide trapping states or high-k nanocrystals, the stored charges are separated at different trapping sites. A local defect of tunnel oxide won't cause a severe charge loss. Thus we can achieve 2 bits storage in one memory device by reversing source and drain. Using band-to-band hot-hole injection can alleviate the drawback of over-erase, which is a problem when FN-tunneling is utilized. We will study the influences of different program/erase operations on the reliability issues of nonvolatile memories.

In Chapter 3, we demonstrate the effects of the post-deposition different annealing ambient for the CeO_2 trapping layer on the performance of the SONOS-type flash memories. It was found that the CeO_2 nanocrystals memory different storage time caused by annealing ambient influence the deep-trapping level. However, the basic electrical operation characteristics are similar. This was ascribed to the larger amount and the shallower energy levels of the crystallization-induced traps. Finally, in the aspect of disturbances, we show only insignificant disturbances properties presented in the normal operation. It was demonstrated that the fabricated memories exhibit higher program/erase speed, long retention time. In particular, two-bit per cell operation has been successfully demonstrated. The device fabrication and characterization are presented. Although the thermal silicon nitride is thinner than required due to fabrication limitations (so the memory is not nonvolatile), initial results show that high quality silicon nitride can still be a promising tunnel dielectric for trap based nonvolatile memory applications.

Instead of scaling the tunnel oxide, the stack gate of O/N tunneling layer can be improved the programming speed at low operation voltage and improved the retention at the same time. In Chapter 4, a stack gate of O/N tunneling layer is investigated as a tunneling layer to replace the conventional silicon dioxide tunneling layer in the CeO_2 nonvolatile nanocrystal memory. It was demonstrated that the fabricated memories

exhibit higher program/erase speed, long retention time. In particular, two-bit per cell operation has been successfully demonstrated.

Chapter 5 proposes substrate effects and Charge-Pumping for CeO_2 nonvolatile nanocrystal memory. The flash memory operating with no body contact (substrate floating) better performance than the bulk SONOS flash memory. The operation voltage can be reduced 1 V at program model. Nevertheless, the date retention is similar. The FN programmed for I_{cp} curve shifted increasingly toward the right upon increasing the value of V_{th} as a result of an increase in the amount of injected charge in the CeO_2 nanocrystal trapping layer. Interestingly, a hump appeared in the left-hand edge of the curve by CHE programmed.

1-3 Thesis Organization

We will propose a simple, reproducible, and reliable technique for the design of high-density CeO_2 nanocrystal through the self-assemble of thin CeO_2 film in chapter 2. Then, in chapter 3, we have investigated the effect of post-deposition annealing different ambient on the performance of the resultant CeO_2 nanocrystal and HfO_2 SONOS-type flash memories. In chapter 4, we have studied CeO_2 nanocrystal on O/N tunnel layer for nonvolatile memory devices. In chapter 5, we have investigated

substrate effects and Charge-Pumping for CeO_2 nonvolatile nanocrystal memory. Conclusions follow in chapter 6.

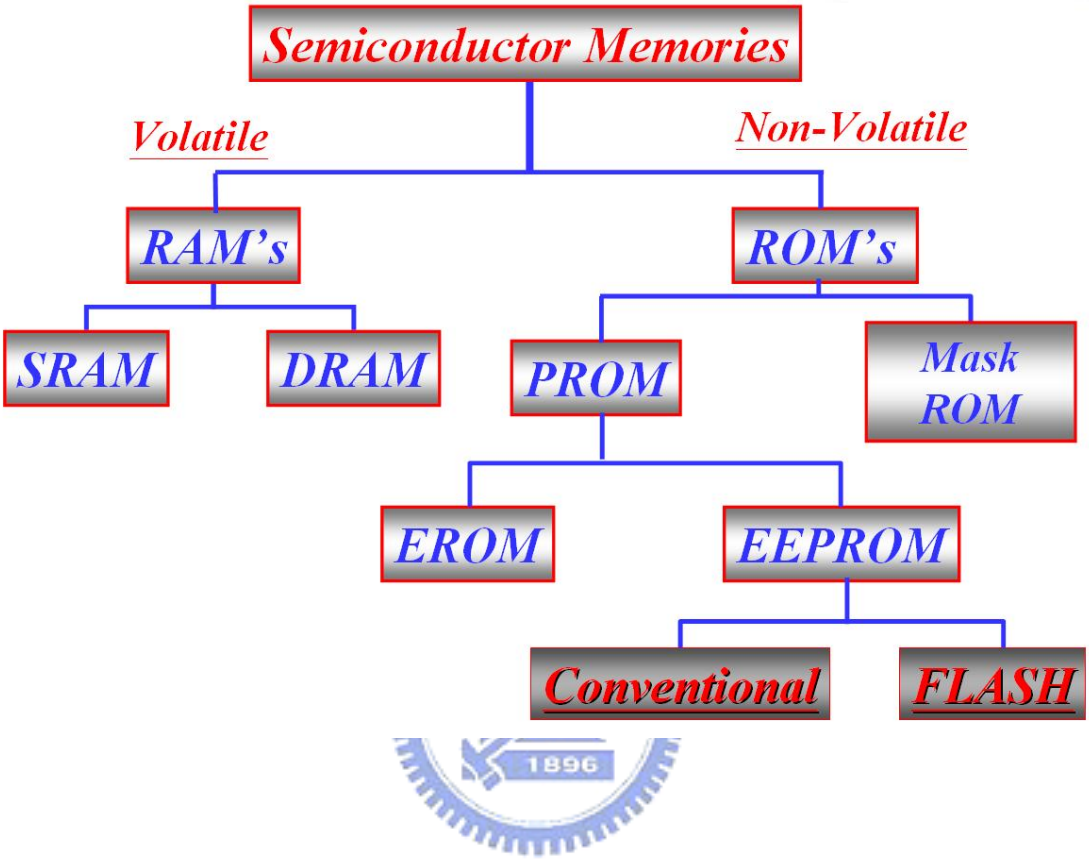
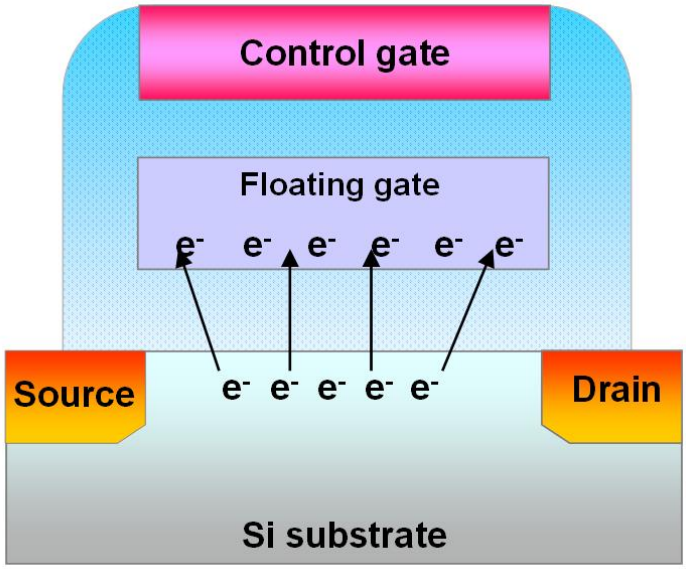
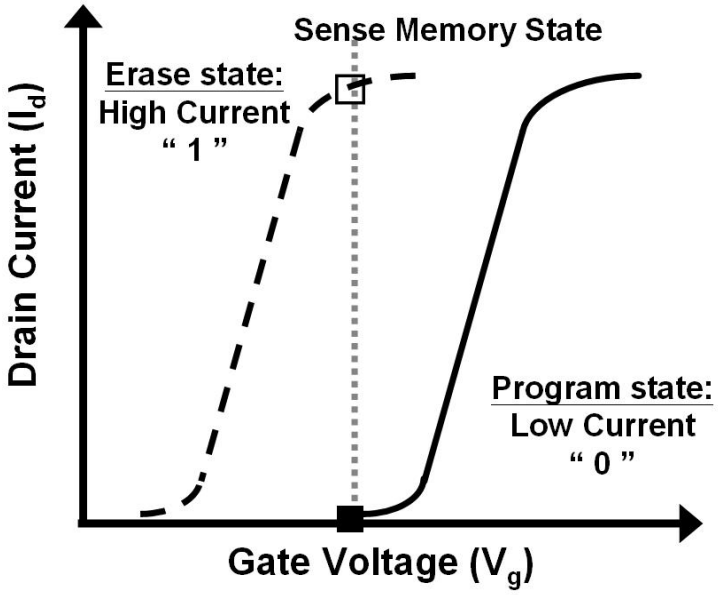


Fig. 1-1 The semiconductor memory tree.



(a)



(b)

Fig. 1-2 (a) Charge trapped in floating gate. (b) I-V characteristics of a memory device in the programmed and erased state. Threshold voltage shifted when the charges are trapping in floating gate.

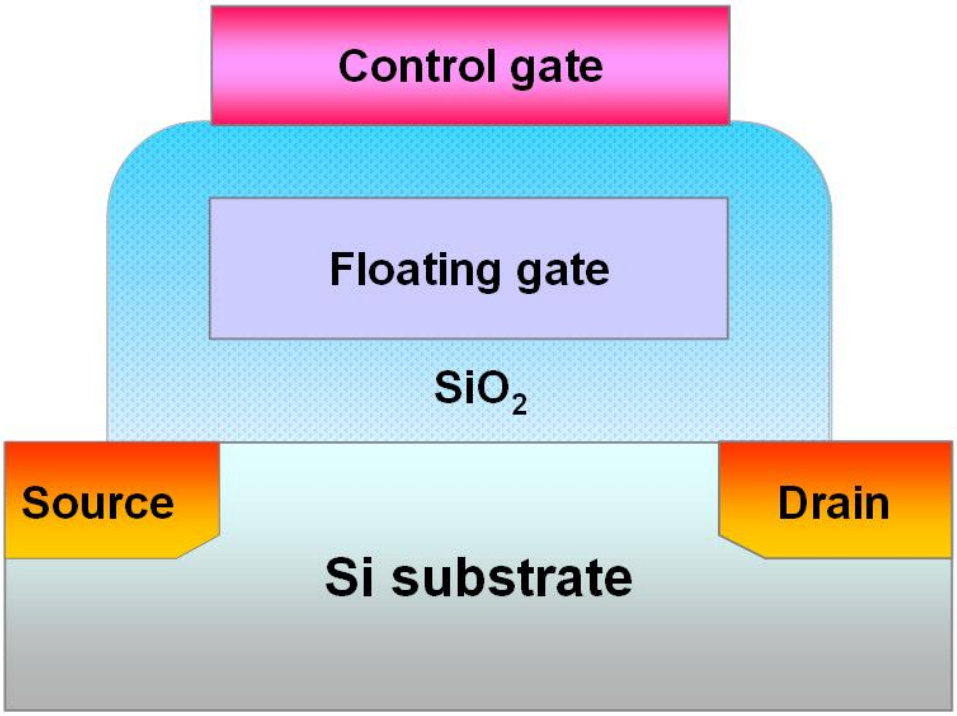
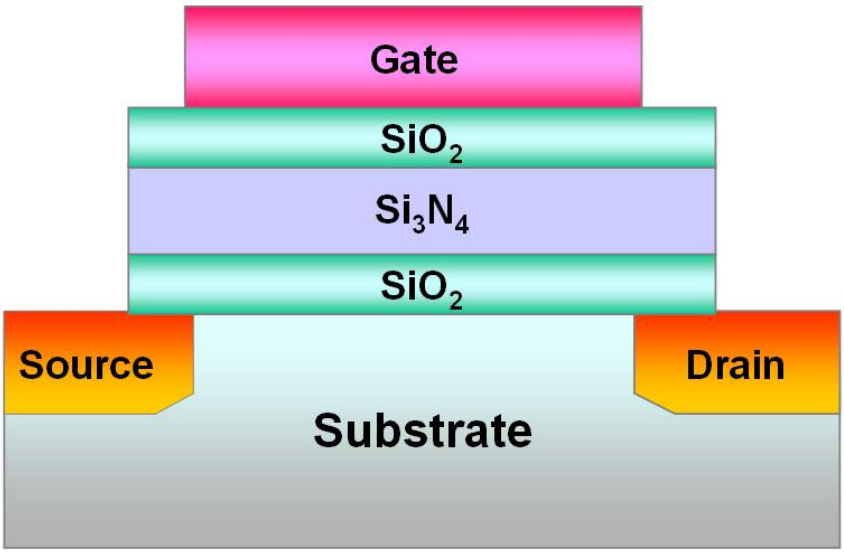
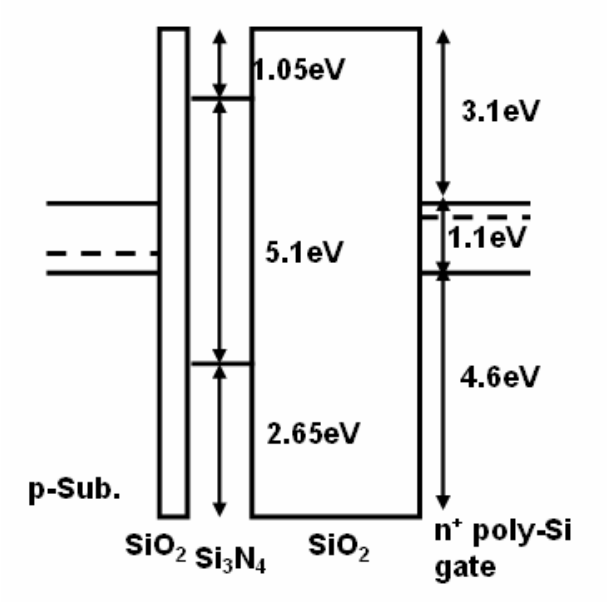


Fig. 1-3 The typical floating gate (FG) memory device structure.



(a)



(b)

Fig. 1-4 (a) Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) memory cell structure. (b) Band gap diagram of Silicon-Oxide-Nitride-Oxide-Silicon structure.

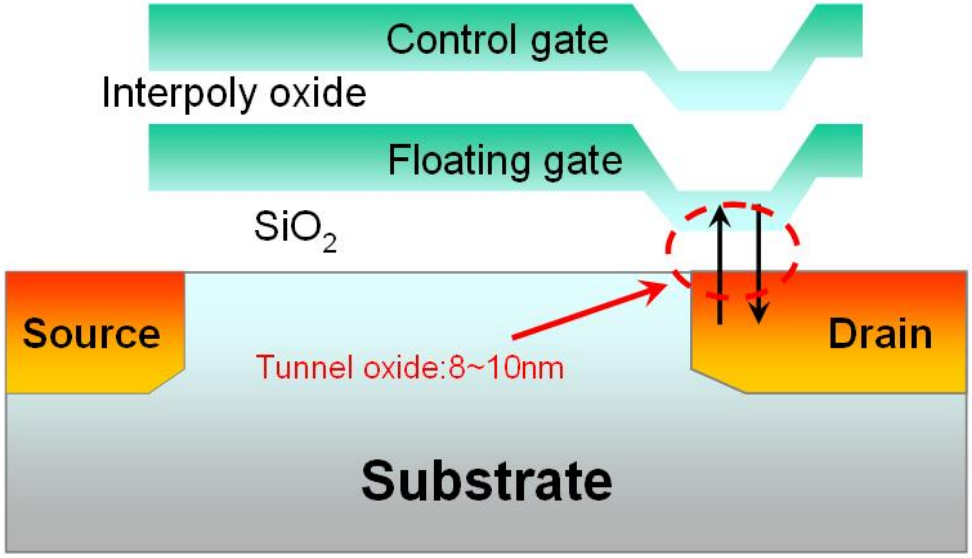


Fig. 1-5 The Drain-side tunneling to program and erase EEPROM memory cell structure.

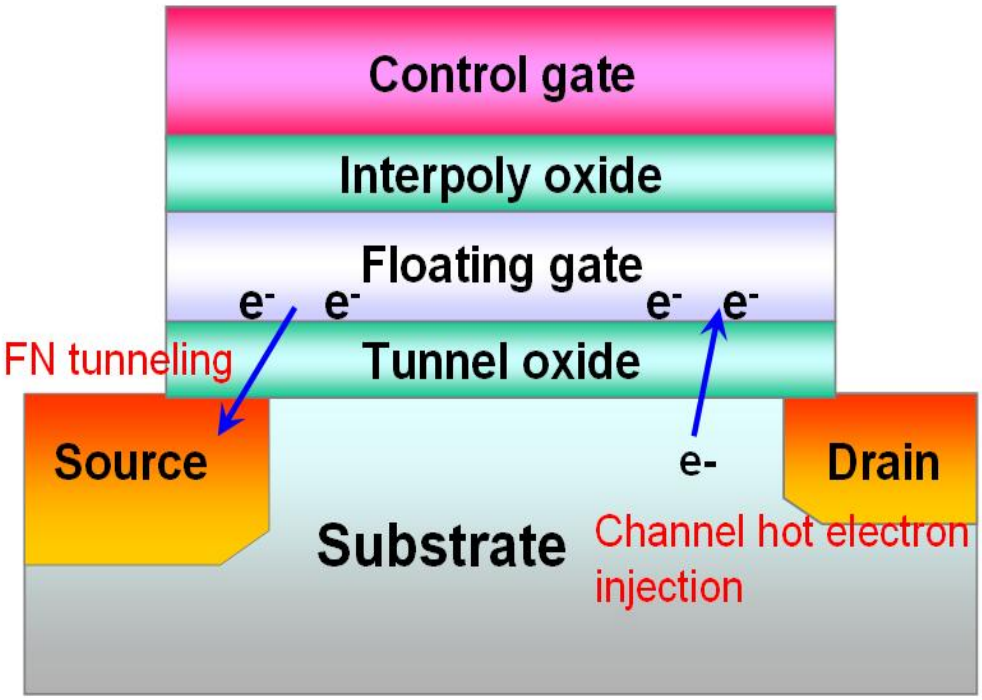


Fig. 1-6 The Drain-side channel hot electron injection to program and source-side FN tunneling to erase Flash EEPROM device structure.

Table. 1-1 Tunnel oxide and operation voltage scaling predicted by 2007 International Technology Roadmap for Semiconductors.

Year	2008		2011		2016	
	NOR	NAND	NOR	NAND	NOR	NAND
Technology Node (nm)	57	51	40	36	22	20
Cell size (λ^2)	9-12	4/2	9-12	4/1	10-13	4/1
Coupling ratio	0.6-0.7					
Tunnel oxide EOT (nm)	8-9	6-7	8	6-7	7-8	6-7
Interpoly oxide EOT (nm)	13-15	10-13	10-12	10-13	8-10	9-10
NOR L_g-stack (physical µm)	0.12		0.11		0.08	
Highest W/E Voltages (V)	7-9	15-17	6-8	15-17	6-8	15-17
Endurance (# cycles)	1E5		1E6		1E7	
Retention (years)	10-20				20	
NOR Iread (uA)	26-34		27-33		22-28	
Max. # bits/cell	2		4			

ITRS 2007 Solutions exist Solutions known Solutions NOT known

Chapter 2

Cerium oxide nanocrystals for nonvolatile memory application and two-bits operation

2.1 Introduction

Nowadays, semiconductor flash memories are widely used in modern electronic systems, such as personal computers, cell phones, personal digital assistants, and digital cameras. The first floating-gate (FG) nonvolatile semiconductor memory was invented by Sze and Kahng in 1967.[2.1] A gate stack consists of a 10-nm-thick thermal oxide as a tunnel layer, a 150-nm-thick polysilicon as a charge storage layer, and a 13-nm-thick inter-polyoxide layer.[2.2] FG flash memories are typically described to have a much slower operation than dynamic random access memories (DRAMs) and static random access memories (SRAMs). A further decrease in thickness of the tunnel oxide (TO) aids in improving the program/erase (P/E) speed of the FG flash memories. However, as the TO thickness is decreased to a value below 8 nm, the storage charges in the FG easily leak away either through direct tunneling or via a defect chain in the TO due to the repeated P/E cycles. For alleviating this scaling issue in the FG flash memories, an increasing attention is being focused on the study of a poly-Si oxide nitride oxide silicon (SONOS) flash memory.[2.3] As well known, a SONOS memory cell employs nitride as a charge trapping layer owing to the fact

that nitride possesses many discrete charge storage traps. Moreover, since a single defect chain in the TO only causes a tiny fraction of the stored charge loss from the memory cell,[2.4] SONOS memories exhibit a higher retention performance as the TO decrease (<8 nm). However, the conduction band offset of nitride is only 1.05 eV with respect to oxide and the back tunneling of the trapped electrons may occur, reflecting that this memory cell still suffers from an insufficient long-term data retention.[2.5-2.6] Considering the above-mentioned problems, high-κ materials and nanocrystals with sufficiently large band offset and deep trap energy levels are possible candidates for replacing nitride as a conventional charge trapping layer.[2.7-2.10]

In this study, we showed the characteristics of the SONOS-type memories with the CeO_2 nanocrystals in detail observed that these memories exhibit good electrical properties. In particular, we also demonstrated the feasibility of two-bit per cell operation for fabricated the CeO_2 nanocrystal memory devices. The obtained experimental results suggest that the technique of forming the CeO_2 nanocrystals is simple and reliable, which can be applied to the fabrication of future fast and high-density nonvolatile flash memories.[2.11-2.12]

2.2 Experimental

The CeO_2 nanocrystal memory devices were fabricated by LOCOS (Local Oxidation of Silicon) isolation on (100) p-type Si substrates with a resistivity of ca. 5–10 Ω·cm. A schematic representation of an n-channel metal oxide semiconductor field effect transistor (MOSFET) with a CeO_2 nanocrystal flash memory structure is shown in Fig. 2-1. The TO thermally grown at 1000°C in a vertical furnace system was designed with two thicknesses of 2.5 and 4.0 nm. We employed an evaporator gun (E-gun) system to deposit a thin CeO_2 layer at 10^{-6} Torr with pure CeO_2 (99.9%) sources. All samples subsequently underwent rapid thermal annealing (RTA) at 900 °C for 60 s in O_2 ambient to form self-assemble CeO_2 nanocrystals. A 24-nm-thick blocking oxide (BO) was deposited using a low-pressure tetraethoxysilane system followed by RTA at 900 °C for 60 s in N_2 ambient to densify the gate stack film structure. A 200-nm-thick polycrystalline silicon (poly-Si) gate was deposited by low-pressure chemical vapor deposition (LPCVD) and then defined by lithography and gate etching. Subsequently, the poly-Si gate and source/drain (S/D) region were implanted using arsenic (5×10^{15} /cm^2, 20 keV) and dopant activation was performed at 950 °C for 15 s. Finally, substrate contact patterning and the rest of the standard CMOS procedure were completed to fabricate the CeO_2 nanocrystal memory devices. The electrical properties of such devices were measured using an HP 4156B

semiconductor parameter analyzer and an HP 41501A pulse generator expander.

2.3 Results and Discussion

2.3.1 Material analysis of CeO_2 nanocrystals

Figure 2-2 shows high-resoluation transmission electron microscopy (HRTEM) cross-sectional images of the CeO_2 nanocrystal trapping layer. Clearly, a well-ordered spherical structure with the CeO_2 nanocrystals was well embedded between the TO (ca 4.0 nm) and the BO (ca. 24.1 nm) without an additional interface layer. We determined that the average size is ca. 8-10 nm and that obviously visible lattice fringes indicate the crystallization of in the nanocrystals. In the nanocrystal flash memories, dot density is an important factor that affects electrical performance. In the Atomic force microscopy (AFM) image shown in Fig. 2-3, white dots indicate the formation of the CeO_2 nanocrystals after O_2 RTA at 900 °C. We estimated that the nanocrystals density is ca. 5×10^{11} cm^{-2} and that the average nanocrystal space is ca. 14 nm, which ensures the electrical insulation between two nanocrystals.

2.3.2 Electrical characteristics

Figure 2-4 shows the I_{ds}–V_{gs} curves of the CeO_2 nanocrystal memory cell under different programming and erasing conditions. The channel width and length of the

memory devices were respectively to be 10 and 0.35 μm, at which the thickness of the grown TO is 4.0 nm. We employed channel-hot-electron (CHE) injection with a duration of 0.1 ms and band-to-band hot-hole (BBHH) injection with a duration of 1 ms as the program and erase methods, respectively. Threshold voltage (V_{TH}) is defined as the applied voltage at which the drain current is 0.1 μA during forward curve sweep. Accordingly, the "V_{TH} shift" of the memory cell can be determined from the V_{TH} change in the programming/erasing state with respect to the fresh state. A consideraly large memory window indicated that V_{TH} shifts from 1.2 V in the fresh state to 4.3 V under the program conditions of $V_g = V_d = 9$ V. The resultant memory window is 3.1 V, which satisfies the basic requirement (> 0.7 V) of typical memory devices. In Fig. 2-5, the programming speed characteristics of the CeO_2 nanocrystal memory cell with two different TO thicknesses are shown. Similar high programming speeds were observed in these two samples in a CHE-program mode. When the programming gate/drain voltage was increased to 10 V, the V_{TH} shift increased rapidly and a memory window of at least 5 V was achieved for 1 ms. These were induced by the applied large gate voltage V_g and a large number of "hot" electrons overcoming the barrier height, and further trapped either in the CeO_2 nanocrystals or at the interface states between the nanocrystals and SiO_2. Figure 2-6(a) and 2-6(b) show the corresponding erasing characteristics of the CeO_2 nanocrystal memory cell at different

erasing voltages. We increased the electrical field between the gate and the drain by changing V_g with a fixed V_d of 10 V in our measurements. As observed, an increase in negative gate bias resulted in a high erasing speed due to a higher electrical field for BBHH injection. A fully erasing behavior was fulfilled within 1 ms when operating two samples at V_g = -6 V and V_d = 10 V however, these samples displayed a little overerasing in the obtained erase curves. We concluded that using the CHE for programming and the BBHH for erasing results in high P/E efficiency in the CeO_2 nanocrystal memory devices.

2.3.3 Two-bits per cell operation

We show the cross-sectional sketch of two-bit per cell operation for the fabricated CeO_2 nanocrystal memory devices in Fig. 2-7. The two localized charge storage systems in the memory cell were programmed by the CHE injection; the charges stored near the drain and source are denoted as Bit-D and Bit-S, respectively.[2.13-2.15] Two schemes namely, the forward and reverse read schemes were employed to recognize the four states in the two-bit operation. In Fig. 2-8, we demonstrated the feasibility of two-bit per cell operation in the I_{ds}–V_{gs} characterisitcs. We injected the CHE (V_g = V_d = 9 V) to program Bit-D for 0.1 ms and then measured the charge stored in Bit-D by forward scanning at V_d = 0.1 V and V_s = 0 V. That is, the

forward read scheme was used to realize Bit-D in the program state or erase state. Furthermore, in order to obtain information regarding Bit-S when Bit-D is in the programming state, we should to apply V_d greater than 2 V; thus, the depletion region formed on the drain side can cover the charge effect of Bit-D. This read operation is called the reverse read scheme. Accordingly, all manipulation steps for Bit-D can be employed in a symmetrical Bit-S and similar results can be obtained. Hence, each memory cell stores two-bit for a high-density flash memory and exhibits higher data retention ability than a conventional SONOS cell. Table 2-1 shows a summary of corresponding terminal bias conditions for the manipulation of the CeO_2 nanocrystal flash memory cell.

Disturbance characteristics are very important reliability characteristics of flash memory. Figure 2-9 is the schematic circuitry of the NOR flash memory array architectures, some failure phenomenon “disturbance” often takes place under operation when the electrical stress applied to those neighboring cells during programming a specific cell in the array for NOR flash applications. For the cell reading, the unwanted electron injection would happen while the wordline voltage and bitline voltage are under read operation. This phenomenon would result in a significant threshold voltage shift of our selected reading cell. Figure 2-10 shows the read disturbance characteristics of the fabricated CeO_2 nanocrystal memory devices.

These characteristics did not show a serious V_{TH} (<0.4 V) for V_d < 3 V, even after 1000 s at T = 25 °C. These evidence the instability of erase-state V_{TH} in a localized CeO_2 nanocrystal trapping storage flash memory cell under several operation conditions. For two-bit operation, the bit-line voltage applied in the reverse read mode must be sufficiently large to "read through" the trapping charges in the adjacent bit. A relatively large bit-line voltage may cause unwanted channel hot-electron injection, therby resulting in a significant shift in the V_{TH} of the reverse-read bit.[2.16]

During charge programming at cell A, drain disturbance occurs in cell B and same for those cells connected with the same bitline because the drain stress is applied to the same bitline (BL). In the fig. 2-11, drain disturbance characteristics of the CeO_2 nanocrystal memory devices were shown two different tunnel oxide thickness samples. The sample of thick TO did not show a serious V_{TH} (<0.5 V) for V_d < 9 V, even after 1000 s at T = 25 °C. On the other hand, gate disturbance occurs in cell C and same for those cells connected with the same wordline (WL) because the gate stress is applied to the same wordline. Gate disturbance characteristics of the CeO_2 nanocrystal memory devices with two different tunnel oxide thickness samples are shown in fig. 2-12. After 1000 sec at 25℃, small 0.6V gate disturb margin was observed.

Figure 2-13(a) shows the temperature-dependent retention characteristics of the CeO_2 nanocrystal memory device with a TO thickness of 4.0 nm. As observed, the

memory device showed small amount of charge loss at RT at measuring times up to 10^4 s for both programming states; this phenomenom can be ascribed to the fact that sufficiently deep trap energy levels exist in CeO_2 nanocrystals.[2.17]-[2.19] Consequently, a greater part of electrons can be trapped in these bulk defect states within an energy band gap. However, a portion of electrons still stayed in the conduction band of the CeO_2 nanocrystals and/or in the interface states between the CeO_2 nanocrystals and SiO_2. We suggest that these trapped charges have a high probability of espcaping with a further increase in temperature due to a low activation energy, such that the amount of charge loss in memory cells is large at T = 85 °C. Subsequently, we compared the CeO_2 memory devices with different TO thicknesses after being programmed at the same V_{TH}, as shown in Fig. 2-13(b). Clearly, the devices with large TO thicknesses exhibited a relatively small amount of charge loss at high temperatures. We suggest that high data retention ability of the thick TO samples arises owing to (a) the low probability of direct tunneling from the CeO_2 trapping layer to the Si substrate and (b) the small trap-assisted tunneling current due to the defect drain in the tunnel oxide. Figure 2-14 shows the endurance characteristics after 10^5 P/E cycles for these two devices. It was found that the memory window of the 4.0-nm-thick-TO nanocrystal devices does not show any closure behavior even after 10^5 P/E cycles. By reducing TO thickness to 2.5 nm, a

simultaneously small increase in programming and erasing V_{TH} was observed with respect to the P/E cycles. This is due to the formation of deep trap levels in the CeO_2 nanocrystal memory cell with the thin TO that makes it difficult to erase all the trapped electrons or misalignment of the CHE and BBHH distribution profiles at the CeO_2 charge trapping sites. In addition, programming the memory cells causes electron trapping; therefore, the I_{ds}-V_{gs} curve moves rightward, which is accompanied by an increase in V_{TH}. However, the erased I_{ds}-V_{gs} curves no longer recover to the original fresh curve and the deterioration of the subthreshold slope is also examined, which may strongly be correlated to the degradation of the TO quality during BBHH injection.[2.20-2.21] By discarding the onset of memory narrowing in the 2.5-nm-thick-TO nanocrystal devices, the memory window is still larger than 0.7 V after 10^5 P/E cycles, which meets the essential demand in the application of flash memory devices.

We can measure the degrees of migration from the cells aftert cycling. One method for characterizing the lateral extent of the trapped electrons is to monitor the variation of the threshold voltage (V_{th}) for a programmed memory cell in the presence of a changing drain current (V_d) [2.22]. Fig. 2-15 Lateral charge migration characteristics of CeO_2 nanocrystal flash memory cell after 10k P/E cycling. Here, V_{th} is defined as the applied gate voltage at which the drain current is 1 μA. Since the cell

is used channel hot-electron injection for programming, the trapped electrons in the CeO_2 nanocrystal trapping layer are more likely to be located near the n^+ drain junction. These trapped electrons will raise the potential barrier near the drain side and increase the value of $V_{th.}$ The degree of the V_{th} shift is believed to be proportional to the trapped electron density if the drain terminal is maintained at a relatively low potential (e.g., V_d = 0.1 V). When a sufficiently high drain bias (e.g., V_d = 2.6 V) is applied, however, the drain depletion region will be extended toward the channel and, consequently, block the influence from the trapped electrons for the measured I_d–V_g characteristics [2.23]. Therefore, this proposed technique can detect the lateral profile of the trapped electrons. To enhance the storage charge movement in the CeO_2 nanocrystal trapping layer, the programmed samples were subjected to high-temperature baking at 80 for 2000 s, respectively.

2.4 Summary

In this chapter, we have demonstrated the high performance of CeO_2 nanocrystal memory devices. Our CeO_2 nanocrystal memory exhibits better characteristics in term of negligible lateral migration of stored charges and good disturbance. The CeO_2 nanocrystal trapping layers showed a large charge storage capacity and a long retention time. The memory devices had good characteristics in terms of high P/E

speed and excellent endurance. We also chose two schemes for reading the four states of accomplish two bit operation in CeO_2 nanocrystal memory devices. Therefore, a CeO_2 nanocrystal can be used as a charge trapping site for replacing the ONO stack in conventional SONOS-type Flash memories.

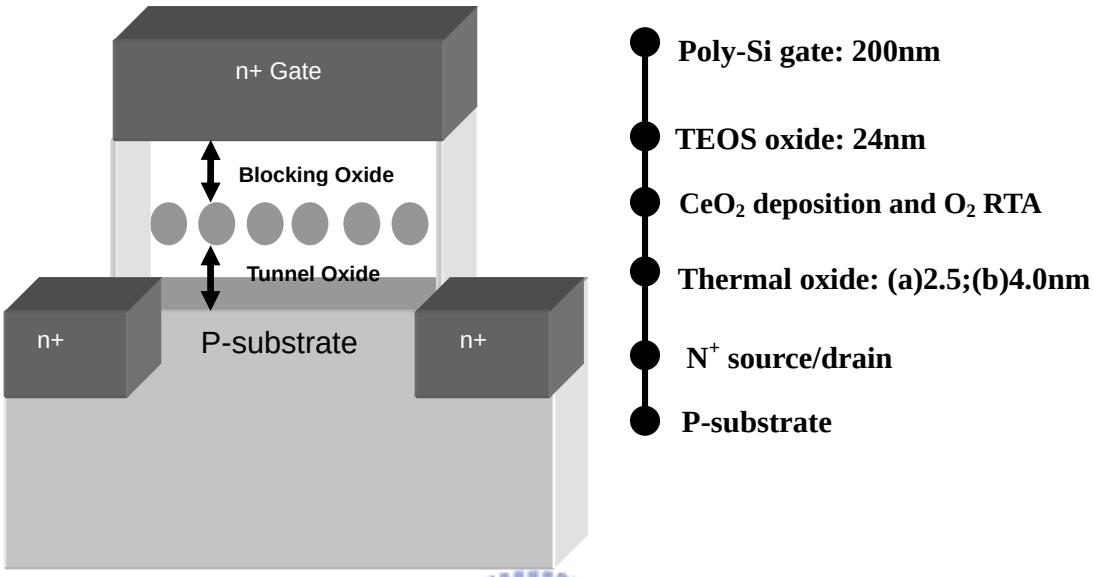


Fig. 2-1 Schematic representation of CeO_2 nanocrystal flash memory devices with main process conditions. CeO_2 nanocrystals were formed by RTA 900℃ in O_2 ambient for 60 s.

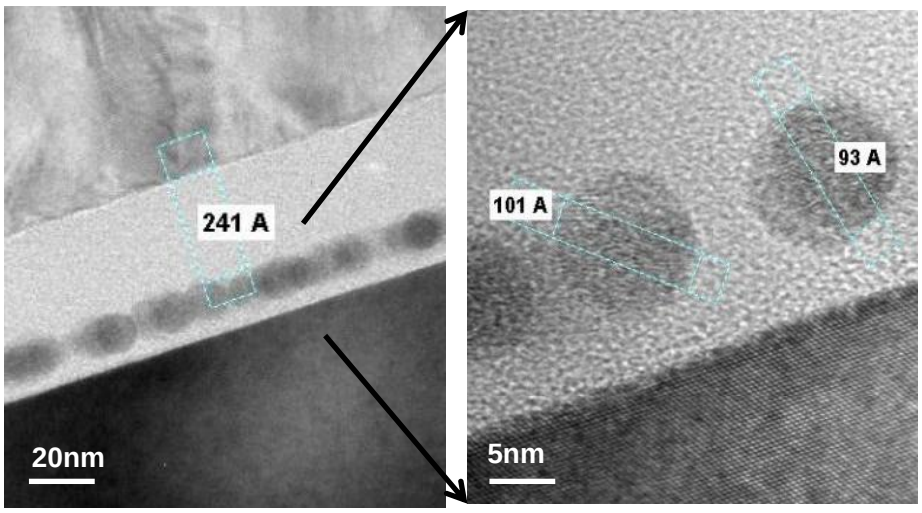


Fig. 2-2 HRTEM Cross-sectional images of CeO_2 nanocrystal trapping layers with TO thickness of 4.0 nm. The average nanocrystal size was ca. 8-10 nm and obviously visible lattice fringes indicated crystallization of inside nanocrystals.

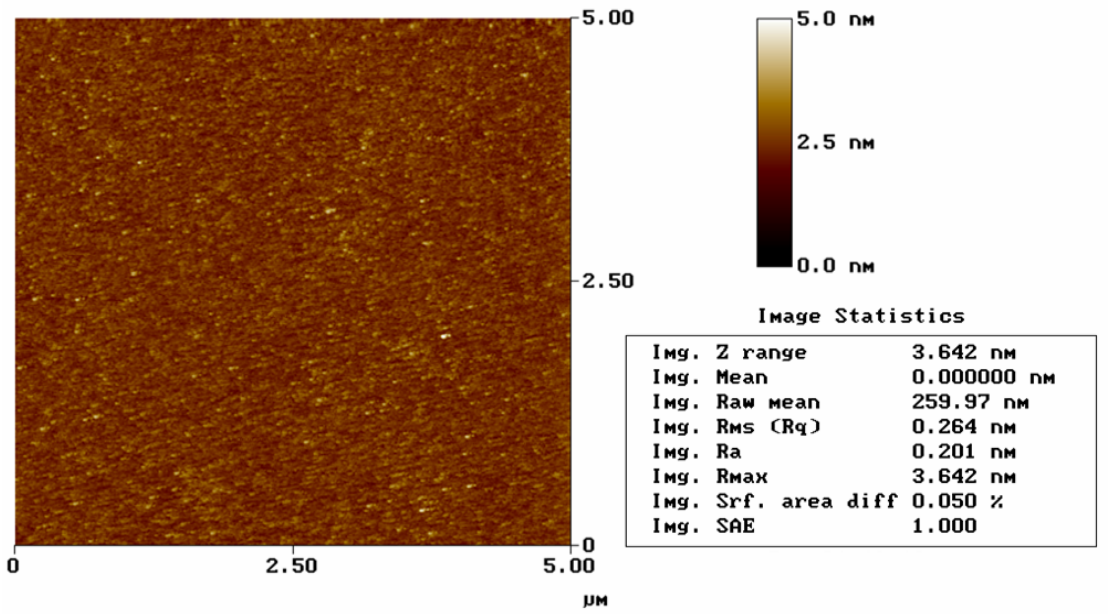


Fig. 2-3 AFM image of CeO_2 nanocrystals; white dots indicate the formation of CeO_2 nanocrystals after O_2 RTA at 900℃. The nanocrystal density was ca. 5×10^{11} cm^{-2} and the average nanocrystal space was ca. 14 nm, which ensures the electrical insulation between two nanocrystals.

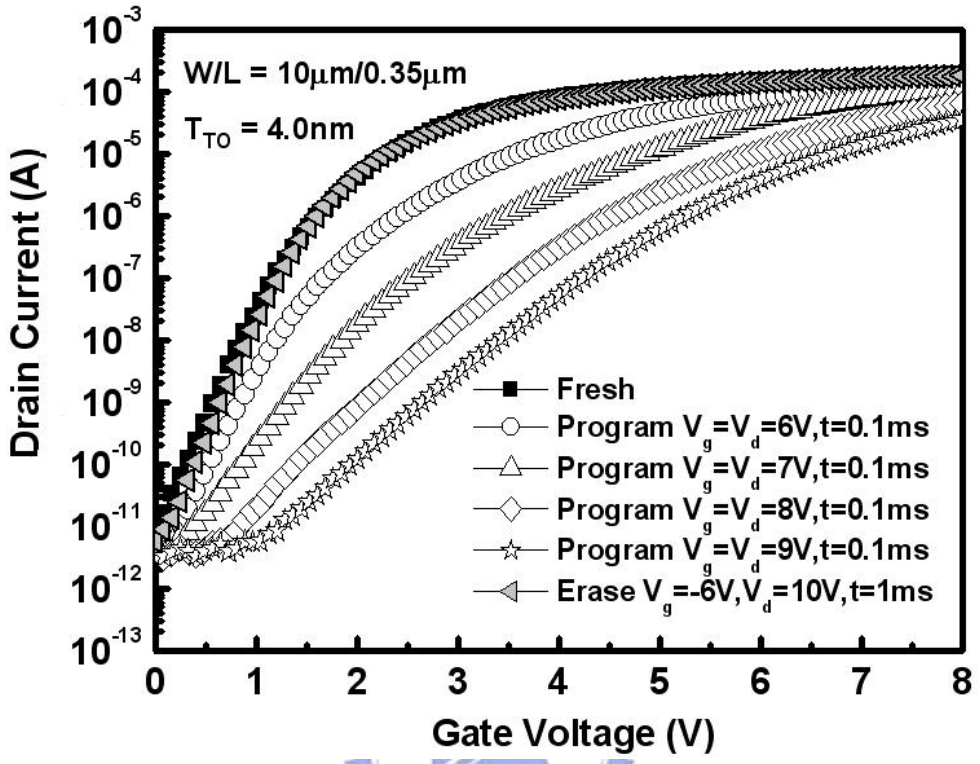


Fig. 2-4 I_{ds}-V_{gs} curves of CeO_2 nanocrystal memory cell under different programming and erasing conditions. The channel width and length of the memory devices were respectively measured to be 10 and 0.35 μm, at which the thickness of the TO is 4.0nm. A memory window with a voltage larger than 3.1 V can be achieved at $V_g = V_d = 9$ V.

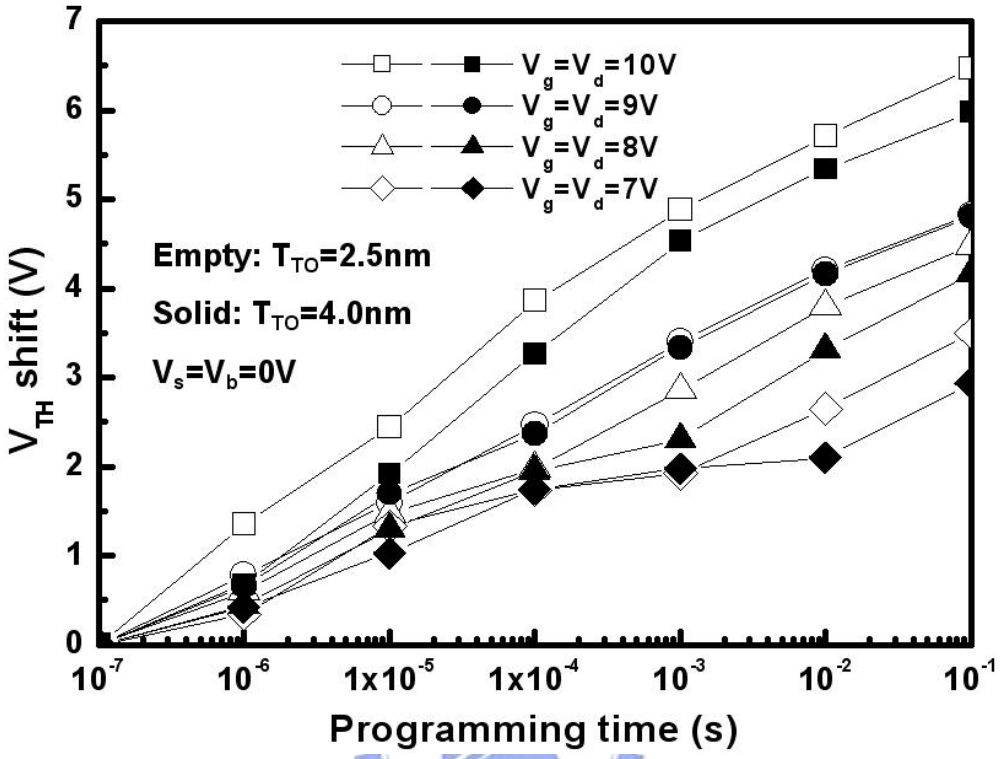
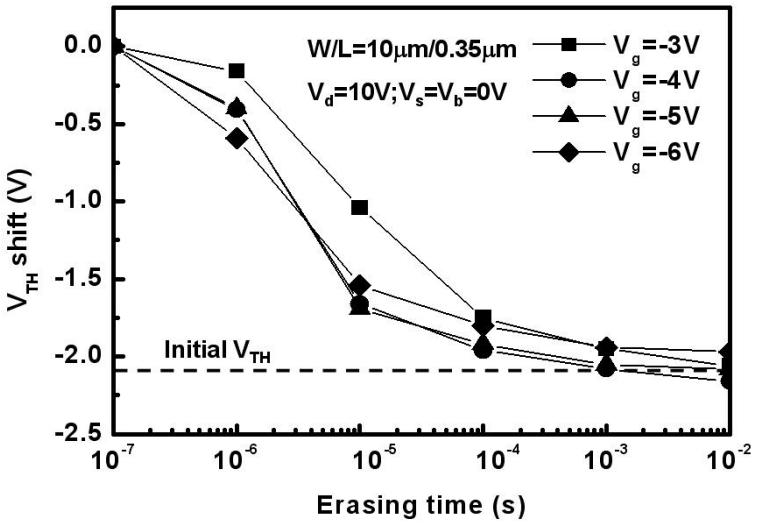
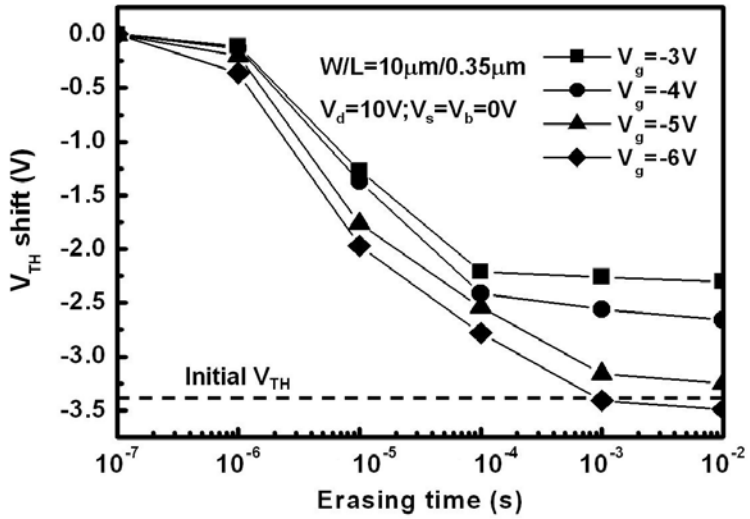


Fig. 2-5 Programming speed characteristics of CeO_2 nanocrystal flash memory devices with different TO thicknesses and programming conditions as function of time. A memory window of ca. 5 V was achieved at $V_g = V_d = 10$ V, and the working time was determined to be 1 ms in programming operation.



(a)



(b)

Fig. 2-6 Erasing speed characteristics of CeO_2 nanocrystal flash memory devices with (a) TO=2.5 nm and (b) TO=4.0 nm under different erasing conditions as function of time. An excellent erasing speed of around 1 ms was obtained and a little overerasing was observed.

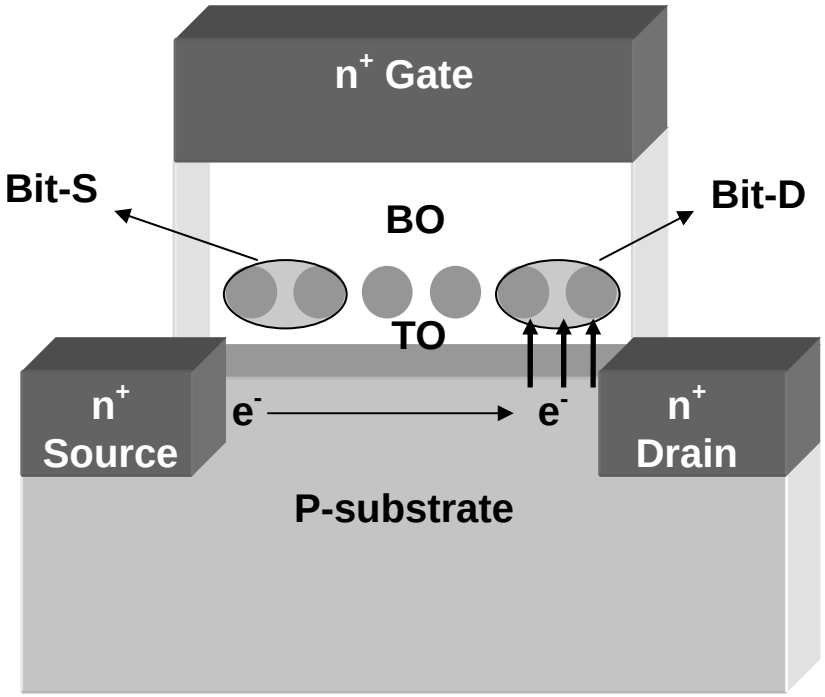


Fig. 2-7 Schematic cross-sectional structure of CeO_2 nanocrystal localized charge storage memory cell with programming by CHE injection. Bit-D: drain side; Bit-S: source side. Each memory cell can store two-bit for a high-density flash memory device.

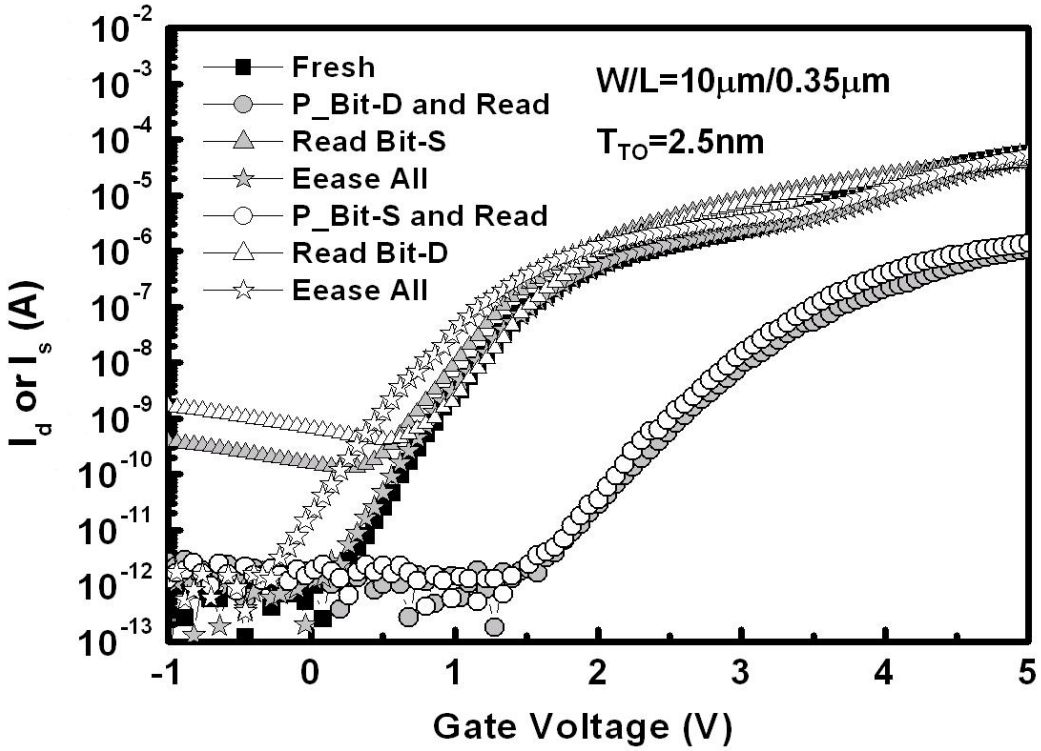


Fig. 2-8 I_{ds}-V_{gs} curves with CeO_2 nanocrystal memory devices demonstrated two-bit per cell operation. Two schemes for reading the four states of these were used. These schemes are the forward and reverse read schemes for recognizing the information stored in the program states of Bit-D and Bit-S, respectively.

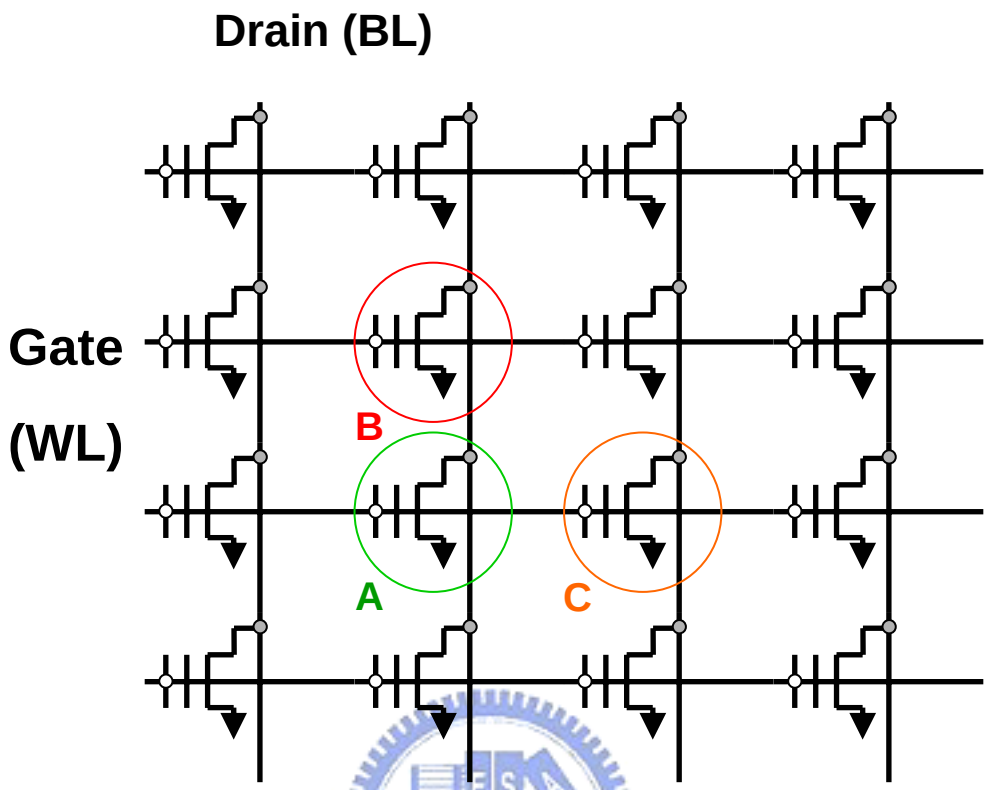


Fig. 2-9 The schematic illustration of disturb condition. Cell A is the programming cell. Cell B and C are the drain disturbance and gate disturbance, respectively.

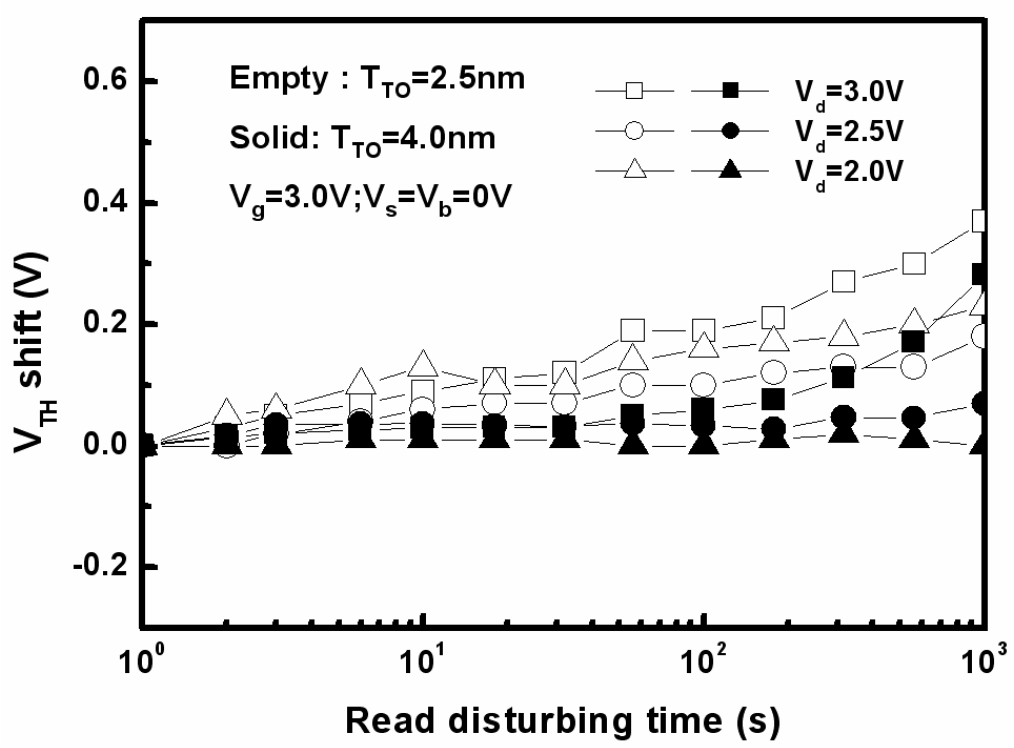


Fig. 2-10 Read disturbance characteristics of CeO_2 nanocrystal flash memory devices with different TO thicknesses. No significant V_{TH} occurred at V_d < 3 V, even after 1000 s at T = 25°C.

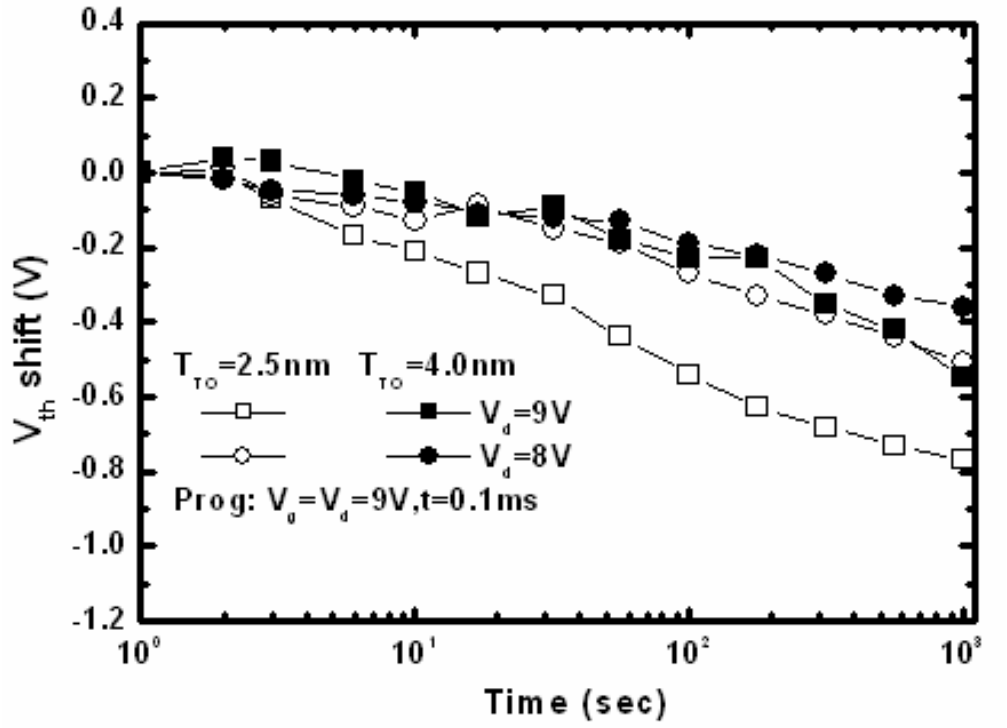


Fig. 2-11 Drain disturbance characteristics of the CeO_2 nanocrystal memory devices with two different tunnel oxide thickness samples.

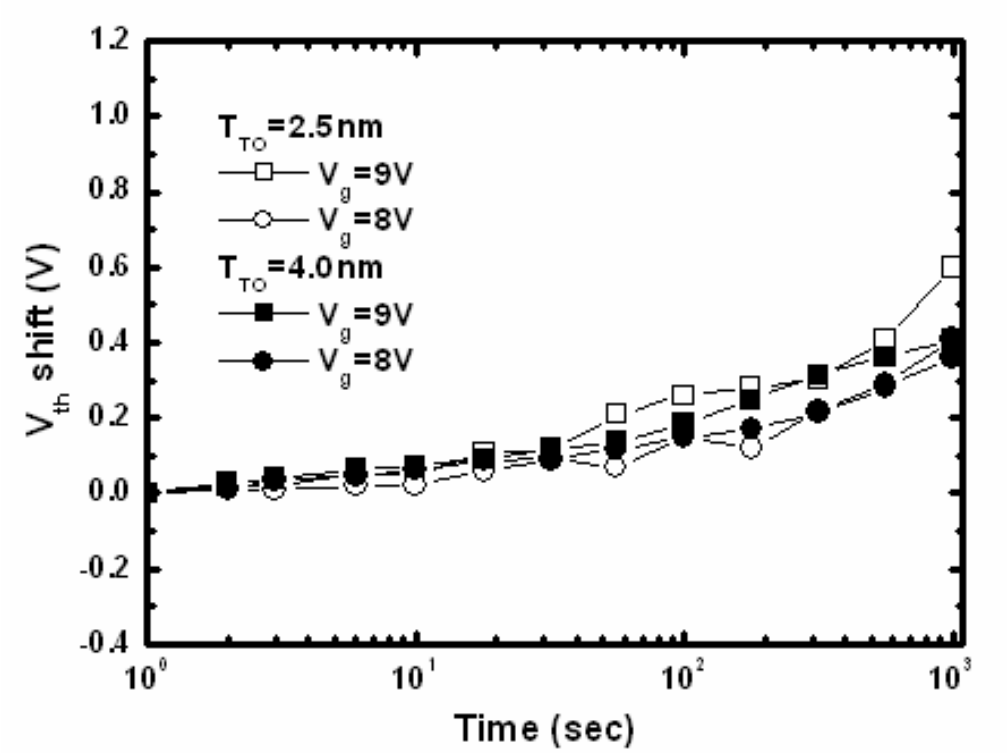
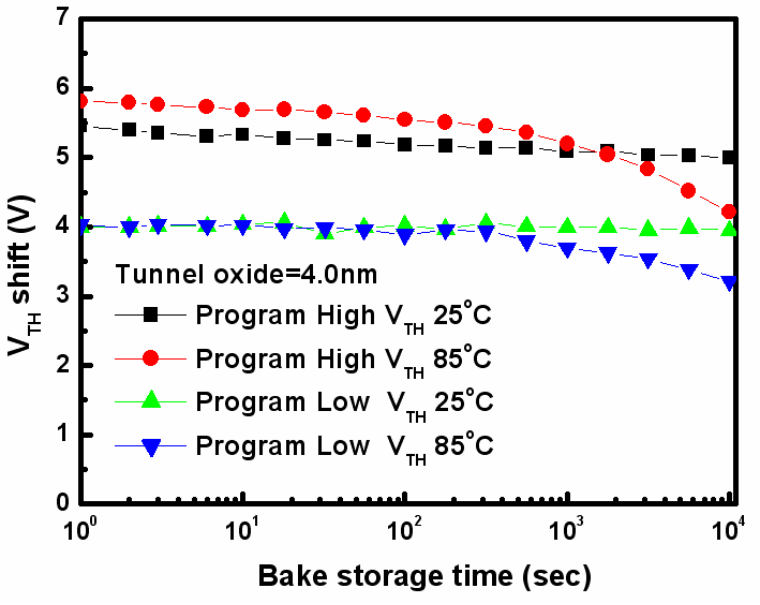
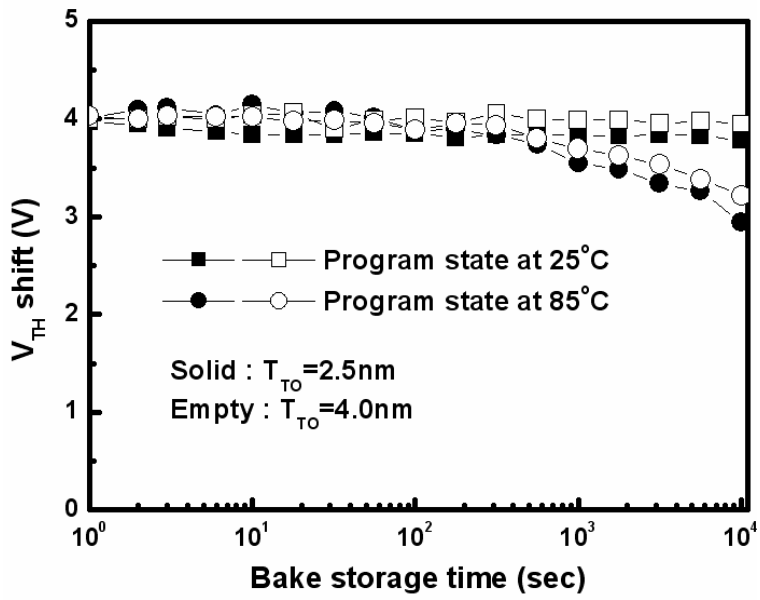


Fig. 2-12 Gate disturbance characteristics of the CeO_2 nanocrystal memory devices with two different tunnel oxide thickness samples. After 1000 sec at 25℃, small 0.6V gate disturb margin was observed.



(a)



(b)

Fig. 2-13 Retention characteristics of CeO_2 nanocrystal flash memory devices for (a) different programming states and temperatures, and (b) different TO thicknesses and temperatures.

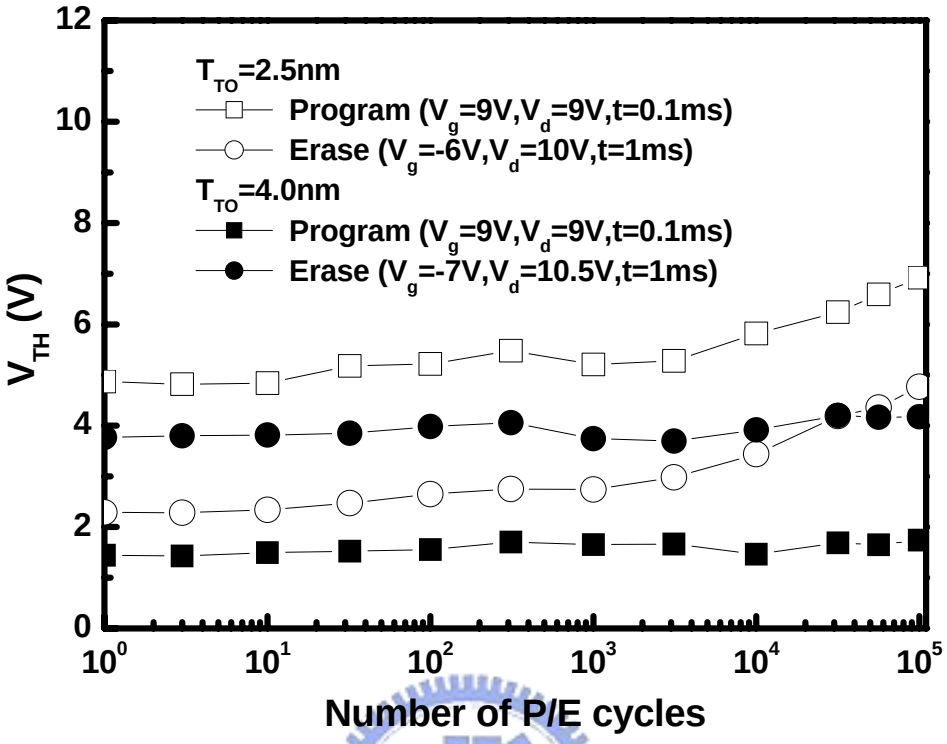


Fig. 2-14 Endurance characteristics of CeO_2 nanocrystal memory devices. The P/E window with a thick TO does not show any closure even after 10^5 cycles compared with that with a thin TO.

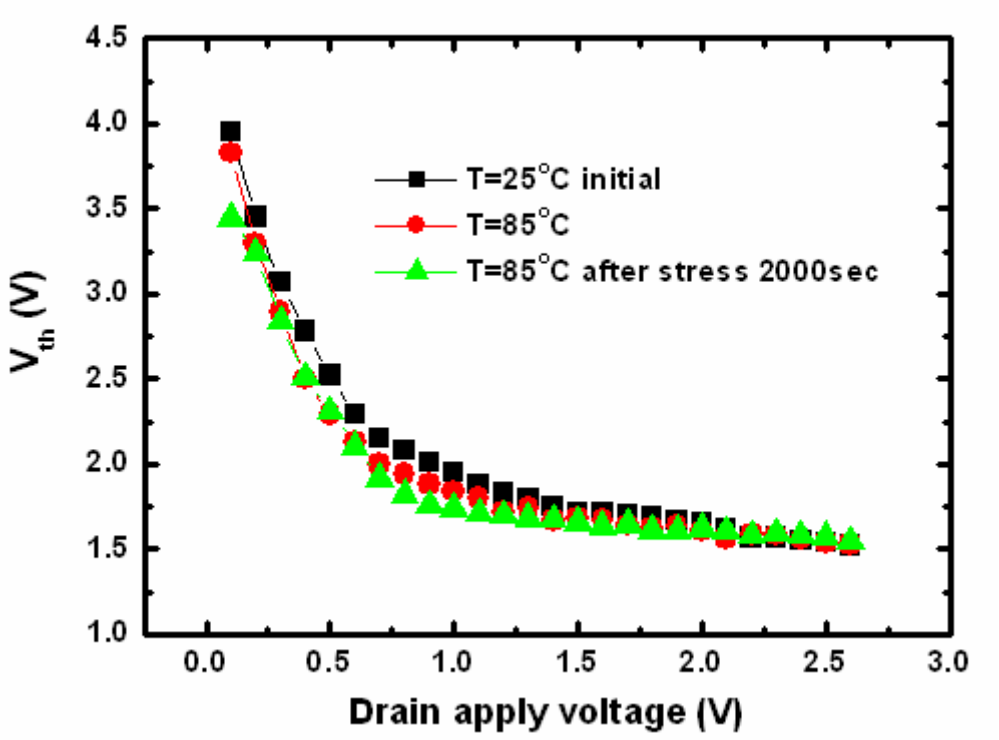


Fig. 2-15 Lateral charge migration characteristics of CeO_2 nanocrystal flash memory cell after 10k P/E cycling.

Table. 2-1 Summary of terminal bias conditions and operation principles for CeO_2 nanocrystal flash memory cell (unit: V).

		Program *(CHE)*	Erase *(BBHH)*	Read *(reverse)*
Bit-D	V_g	9	-6	3
	V_d	9	10	0
	V_s	0	0	>2
Bit-S	V_g	9	-6	3
	V_d	0	0	>2
	V_s	9	10	0

Chapter 3

Annealing ambient effects on the performance of CeO_2 nanocrystal memory

3.1 Introduction

The characteristics of silicon-oxide-nitride-oxide-silicon (SONOS)-type memories embedded with cerium oxide nanocrystals were demonstrated. They were fabricated by depositing a thin CeO_2 film on the SiO_2 tunneling layer and subsequently rapid-thermal annealing process. The mean size and aerial density of the CeO_2 nanocrystals embedded in SiO_2 are estimated to be about 8~10 nm and $3\sim7\times10^{11}$ cm^{-2} after a high-temperature annealing with different ambient at 900 ℃. The program/erase behaviors and data retention characteristics were described to demonstrate its advantages for nonvolatile memory device applications.

In recent years, cerium dioxide (CeO_2) which has been extensively researched on as the buffer layer for $YBa_2Cu_3O_{(7-x)}$ (YBCO) on sapphire[3-1], an electrolyte material of solid oxide fuel cells[3-2][3-3], buried insulator for silicon-on-insulator (SOI)[3-4] and $PbZrTiCeO_3$ (PZT) ceramics[3-5], is used for gate dielectric materials lately[3-6], etc. Many superior properties such as lattice nearly matched to silicon (a=0.5411 nm) and sufficiently high dielectric constant (~26) (Refs. 3-7 and 3-8) for cerium dioxide led to the high thermal stability on silicon and high scaling capacity. Silicon and metal

nanocrystals (NCs) are widely studied as potential solutions to overcome the scaling limitations of the conventional flash memories for future nonvolatile, high density, and low power memory devices[3-9]-[3-13]. Recently, high-κ dielectric NCs on the SiO_2 tunneling layer for silicon-oxide-nitride-oxide-silicon(SONOS)-type memories have been proposed Lin *et al*. [3-14] have reported a method of cosputtering Hf and Si in oxygen followed with high-temperature annealing to form the high-κ NCs for SONOS-type memory devices. However, the HfO_2 nanocrystal memory exhibits saturation windows in channel-hot-electron (CHE) program mode. You *et al.*[3-15],[3-16] have proposed the sol-gel spin-coating method to form the high-κ NCs. This method may increase thickness of tunnel oxide and results in high operation voltage.

In this study, the CeO_2 NCs were produced by a thermal annealing in different ambients. SONOS-type memories were fabricated and the electrical properties were investigated. The CeO_2 NC memory devices have shown good electrical properties in terms of large memory window (>2 V) at P/E speed of 10 / 10μs and a retention time up to 10^4 s with only 10% charge loss. Our results suggest that the CeO_2 NC formation technique is simple and reliable, which shows a good potential for the application of the future fast nonvolatile memories[3-17]-[3-19].

3.2 Experimental

At fig. 3-1 was shown schematic representation of CeO_2 nanocrystal flash memory devices with main process conditions. P-type Si (100) substrates with a resistivity of 5–10 Ω·cm were used.A thin CeO_2 layer was deposited on SiO_2 tunneling layer by an electron-beam evaporator at 10^{-6} Torr. The some samples subsequently underwent rapid-thermal annealing (RTA) at 900 °C for 1 min in either O_2 or N_2 ambient to form self-assembled CeO_2 NCs. The other sample is without RTA process. Afterward, all samples were deposited with a 25-nm-thick blocking oxide layer by using a low-pressure tetraethoxysilane system at 700 °C.Then, a 200-nm-thick polycrystalline silicon (poly-Si) gate was deposited and patterned. The poly-Si gate and source/drain regions were implanted with arsenic (5×10^{15} cm^{-2}, 20 keV), and the subsequent dopant activation annealing was performed at 950 °C for 15 s. Finally, the CeO_2 NC memory devices were completed after the substrate contact patterning and metallization. The electrical properties of such devices were measured using HP 4156B semiconductor parameter analyzer and HP 41501A pulse generator.

3.3 Results and Discussion

3.3.1 Material Analysis

Figure 3-2 (a) was the cross-sectional transmission electron microscopy (TEM)

images shown that deposited thin CeO_2 film on SiO_2 layer subsequently without RTA process. The cross-sectional TEM images of the CeO_2 NCs embedded in the SiO_2 dielectric matrix for rapid-thermal N_2 (RTN_2) and O_2 (RTO_2) samples are shown in Figs. 3-2(b) and 3-2(c), respectively. No obvious difference in microstructure in terms of NC size and distribution are formed between annealed samples. They showed a NC density of $3\sim7\times10^{11}$ /cm^2. The average NC size was 8-10 nm. Crystallized NCs with obviously visible lattice fringes were evident in the insets. Fig. 3-3 shows the ideal energy band diagrams of the CeO_2 NC memory devices. The charges may be trapped in electron and hole traps in the CeO_2 NCs or by charge confinement in the quantum well[3-17]. Zhang *et al.*[3-20] have reported that the CeO_2 band gap is 3.15 eV and Engström *et al.*[3-21] have indicated that the conduction band offset between cerium oxide and silicon is 2.7 eV. The quantum well formed by the conduction band is deeper for CeO_2 NC structure than SONOS structure (2.7 eV compared to 1.05 eV)[3-22].

3.3.2 Device operation characteristics

The programming speed of the CeO_2 NCs memory devices with RTN_2 and RTO_2 annealing are shown in Fig. 3-4. The memory device is programmed by CHE injection. When the program voltage increases to 10 V, the V_{th} shift increases rapidly

and a memory window greater than 5 V was achieved within 1 ms. The large memory windows make the multilevel operation possible. The fact the programming speed is independent of annealing condition of the charge trapping centers, indicating that the programming speed is primarily dependent on the tunneling oxide. Fig. 3-5 shows the erasing speeds at different gate voltages with a fixed V_d of 10 V. The device is erased by band-to-band hot-hole (BBHH) injection. For the erasing speed operation, the device was programed under V_g = 10 V, V_d = 9 V with a duration of 0.1 ms. As observed, an increase in the negative gate bias resulted in a high erasing speed due to a higher electrical field for the BBHH injection. A fully erased state was fulfilled within 1 ms when operating two samples at V_g = -7 V and V_d = 10 V. We concluded that using the CHE for programming and the BBHH for erasing has achieved high P/E efficiency in the CeO_2 NC memory devices.

3.3.3 Comparison of different annealing ambient

Fig. 3-6 illustrates the data retention characteristics of the CeO_2 NC memory devices with different RTA treatments and programming states. The RTN_2 sample showed a smaller amount of charge loss at room temperature for a retention times up to 10^4 s than the RTO_2 sample. It is conjectured that the bulk traps of RTN_2 sample are deeper than RTO_2 sample so that the charge loss of RTN_2 sample is less than RTO_2

sample. This phenomenon can be ascribed to the fact that sufficiently deep trap energy levels exist in the CeO_2 NCs. At high temperature (85 ^oC), RTN_2 sample increased charge loss rapidly after 10^3 s. The result is because the charge loss of RTN_2 sample comes from the charge in the bulk traps. The electrons can be either trapped in these bulk defects or stay in the conduction band of the CeO_2 NCs and/or in the interface states between the CeO_2 NCs and SiO_2[3-17],[3-22]. The endurance performance after 10^4 P/E cycles for the CeO_2 NC memory devices with different annealing ambient are shown in Fig. 3-7. It was found that the memory window of the NCs devices did not show any closure behavior even after 10^4 P/E cycles. As we know, the different device have the same TO and BO due to the same elecrtic field. A simultaneously small increase in programmed and erased V_{th} was observed with respect to the P/E cycles due to the difficulties of erasing all the trapped electrons or the misalignment of the CHE and BBHH distribution profiles at the CeO_2 charge trapping sites. By discarding the onset of memory narrowing in NCs devices, the memory window is still larger than 0.7 V after 10^4 P/E cycles, which meets the essential demand in the application of flash memory devices.

Disturbance characteristics are very important reliability characteristics of flash memory. Fig. 3-8 are shown the read disturbance characteristics of CeO_2 nanocrystal flash memory devices with different annealing ambient, (a) with RTN_2 at 900℃ for 1

min; (b) with RTO_2 at 900℃ for 1 min. No significant V_{TH} occurred at V_d < 3 V, even after 1000 s at T = 25°C. The RTO_2 sample did not show a serious V_{TH} (<0.4 V) for V_d < 3 V, even after 1000 s at T = 25 °C. These evidence the instability of erase-state V_{TH} in a localized CeO_2 nanocrystal trapping storage flash memory cell under several operation conditions. Drain disturbance characteristics of the CeO_2 nanocrystal memory devices with two different annealing ambient. Fig. 3-9 (a) is RTN_2 at 900℃ for 1 min and Fig. 3-9 (b) is RTO_2 at 900℃ for 1 min. No significant V_{TH} occurred at RTN_2 sample after 1000 s at T = 25°C. In the Fig. 3-10, I_{ds}-V_{gs} curves with CeO_2 nanocrystal memory devices demonstrated two-bit per cell operation. (a) with RTN_2 at 900℃ for 1 min; (b) with RTO_2 at 900℃ for 1 min. Two schemes for reading the four states of these were used. Table 3.1 Summary of terminal bias conditions and operation principles for CeO_2 nanocrystal flash memory devices with different annealing Therefore, each nanocrystal memory cell stores two-bit for a high-density flash memory and exhibits higher data retention ability than a conventional SONOS memory cell.

3.4 Summary

We have investigated the annealing ambient effect on the performance of the resultant CeO_2 nanocrystal memory devices and demonstrated higher P/E speed of 10

/ 10μs with CeO_2 NC memory devices. Moreover, we found that the RTN CeO_2 NC trapping layers have a larger charge storage capacity and a longer retention time up to 10^4 s with only 10% charge loss than the RTO sample due to deeper trap center. No significant read, drain and gate disturbance were obaerved for the RTN CeO_2 NC sample. It is concluded that the RTN CeO_2 NCs can be used a promising canadidate as discrete charge trapping sites for the Flash memory devices application.

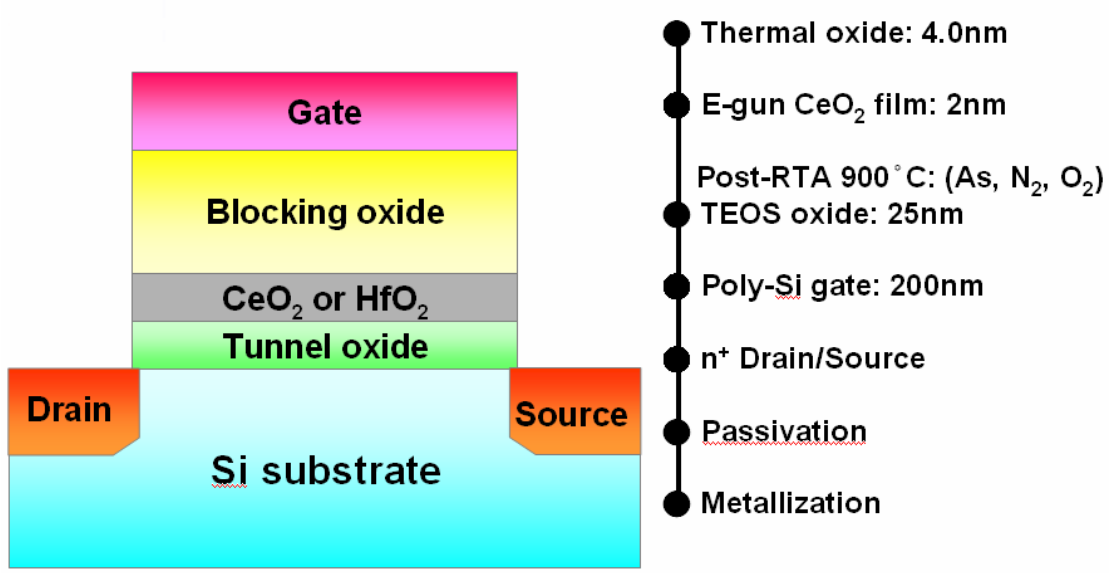


Fig. 3-1 Schematic representation of CeO_2 nanocrystal flash memory devices with main process conditions.

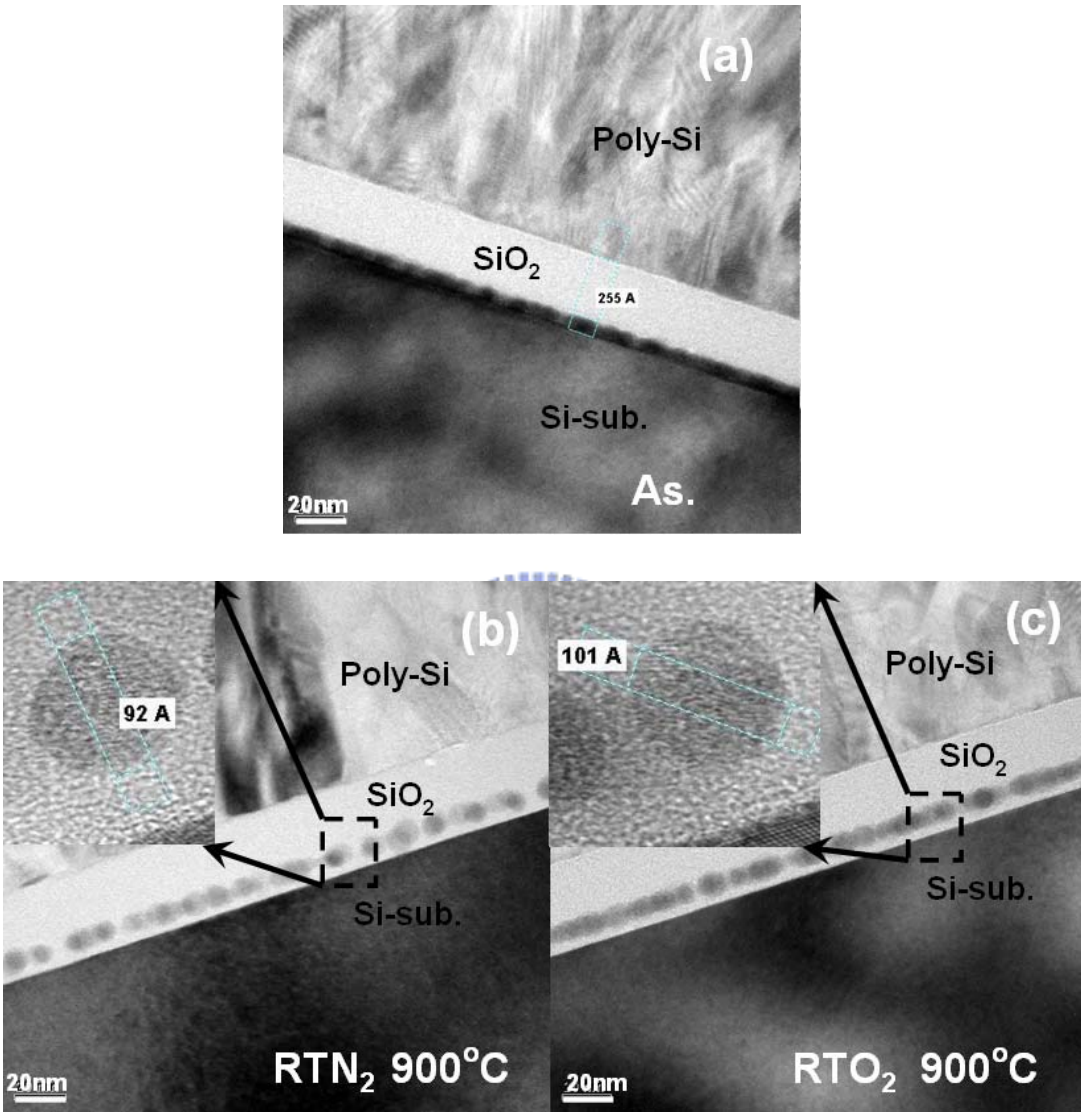


Fig. 3-2 Cross-sectional TEM images of the CeO_2 nanocrystals embedded in SiO_2 dielectric matrix. (a)without RTA process; (b) with RTN_2 annealing at 900℃ for 1 min; (c) with RTO_2 annealing at 900℃ for 1 min, where the average nanocrystal size was 8-10 nm and obviously visible lattice fringes indicated crystallization of nanocrystals.

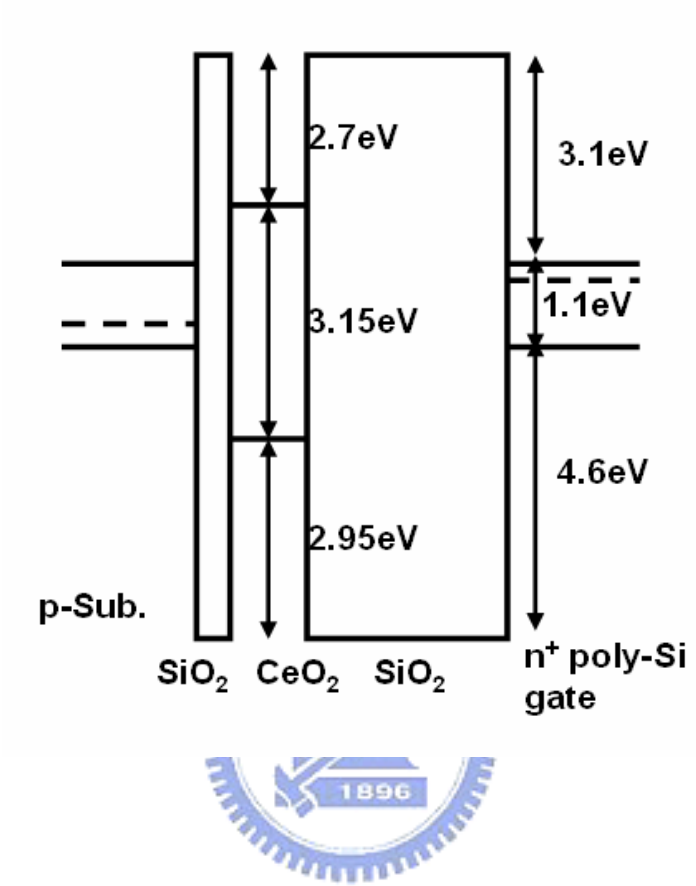


Fig. 3-3 Ideal energy band diagram for CeO_2 nanocrystal SONOS-type structures.

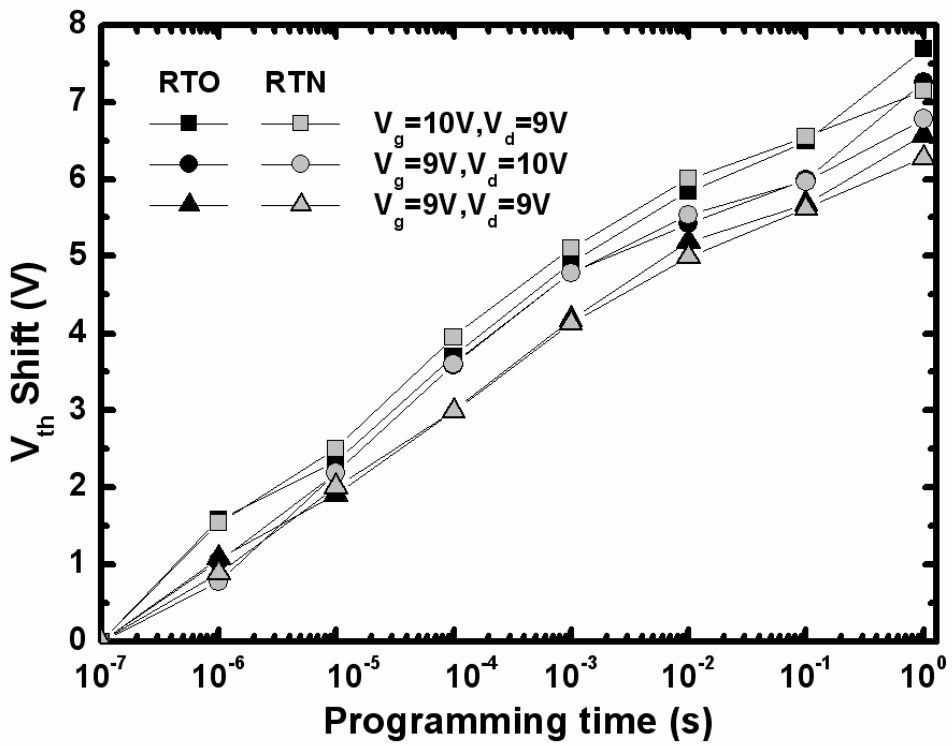


Fig. 3-4 Programming speed characteristics of CeO_2 nanocrystal flash memory devices with different programming conditions as a function of time. The fact the programming speed is independent of annealing condition of the charge trapping centers, indicating that the programming speed is primarily dependent on the tnunneling oxide.

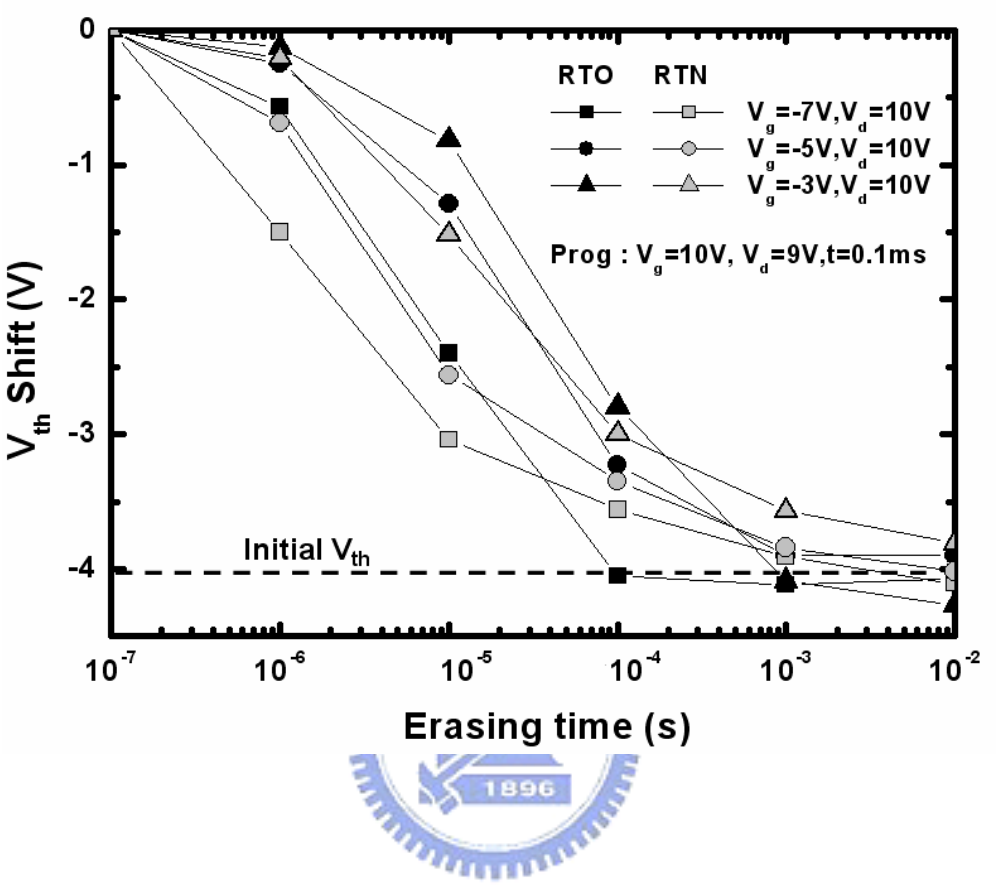


Fig. 3-5 The erasing speed characteristics of the CeO_2 nanocrystal memory cell at different erasing voltages. As observed, an increase in the negative gate bias resulted in a high erasing speed due to a higher electrical field for the BBHH injection.

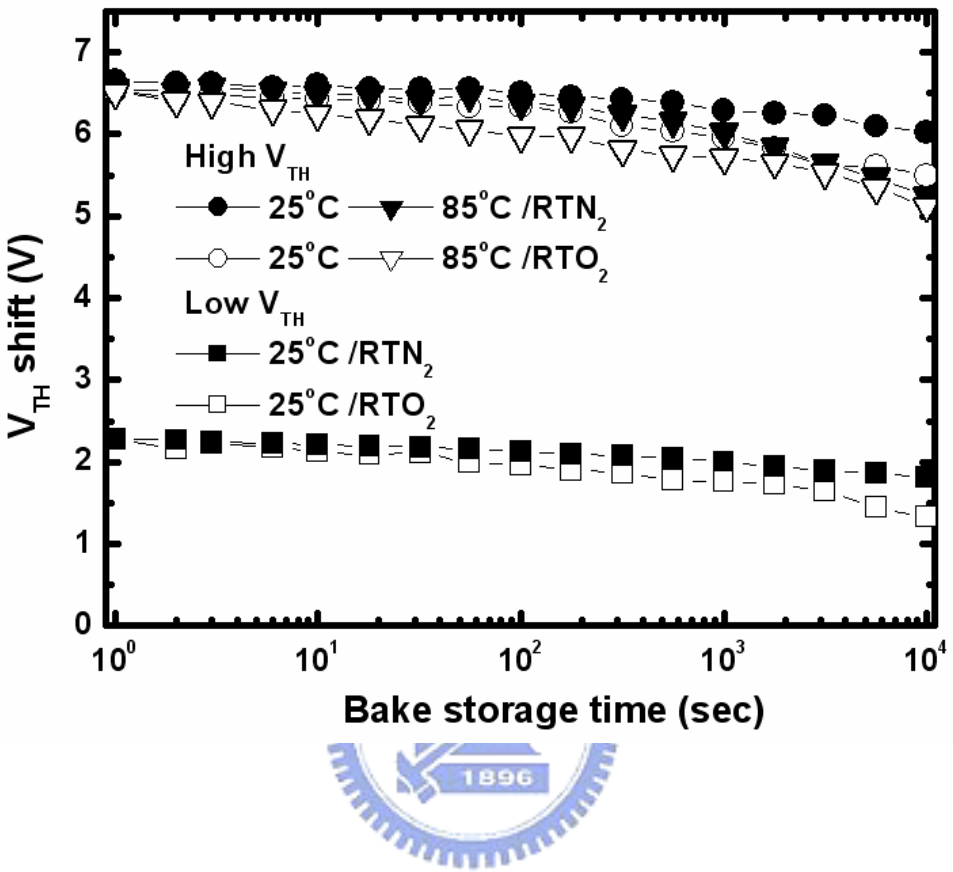


Fig. 3-6 Retention characteristics of CeO_2 nanocrystal flash memory devices with different RTA treatments and programming states.

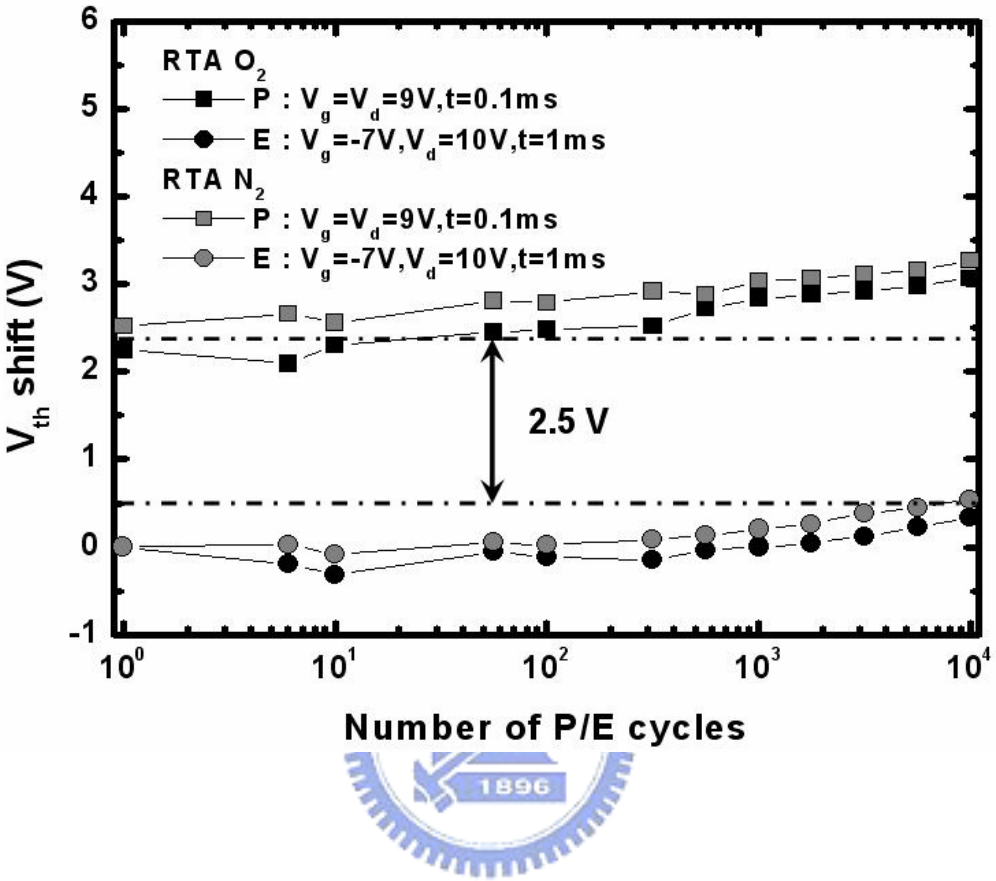
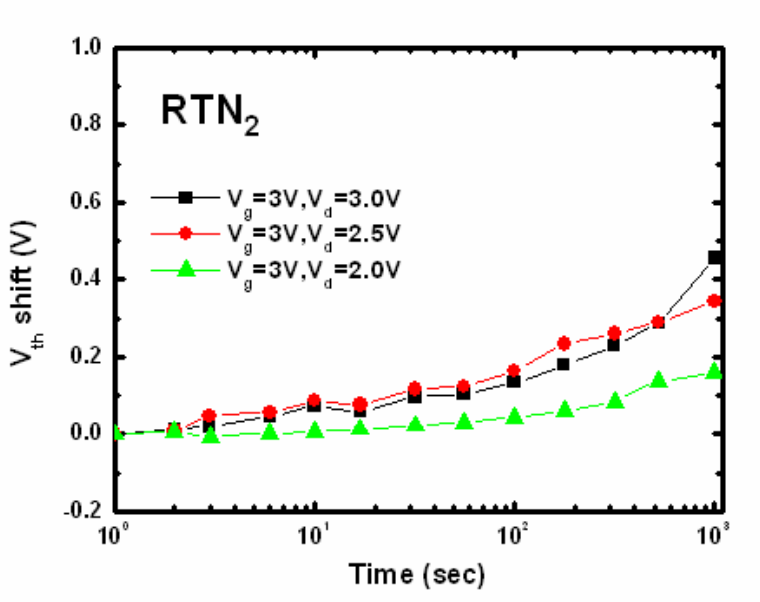
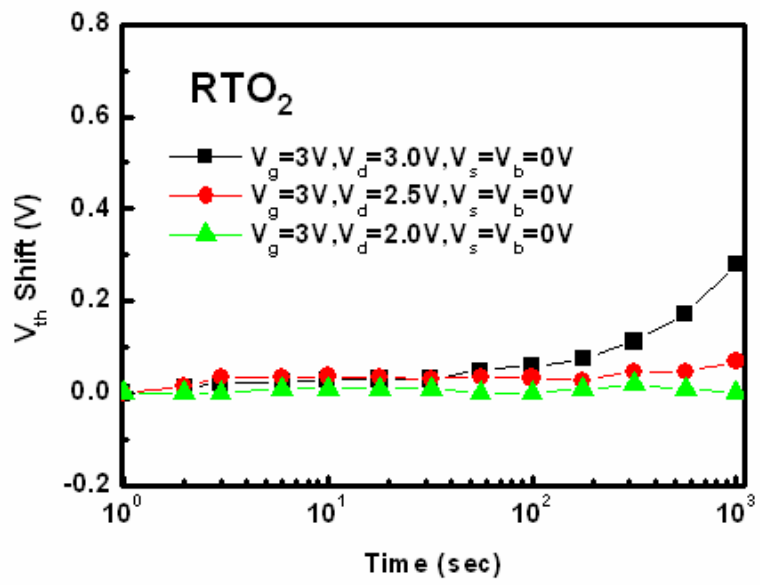


Fig. 3-7 The endurance characteristics of CeO_2 nanocrystal flash memory devices with two different treatment devices. The memory window of the NC devices does not show any closure behavior even after 10^4 P/E cycles.

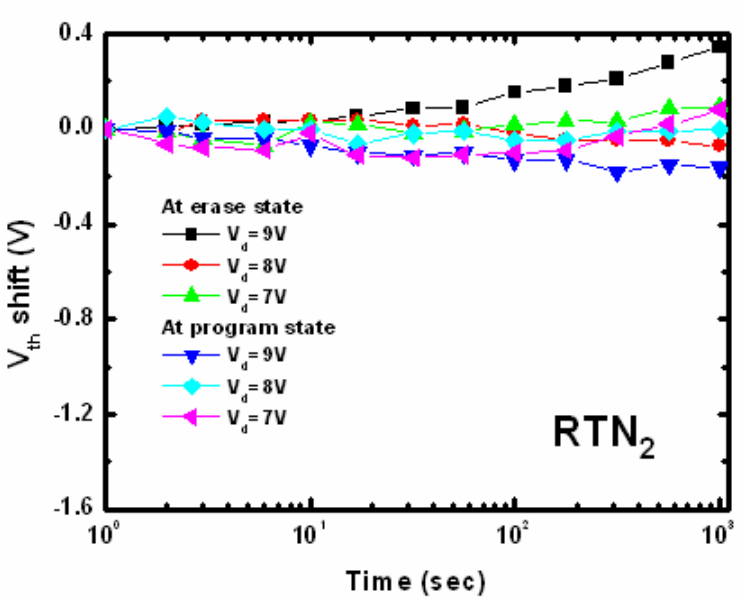


(a)

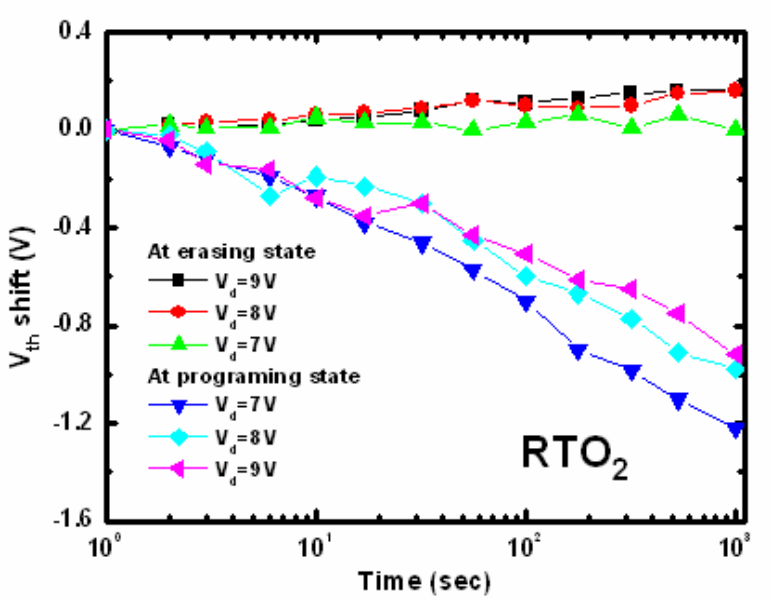


(b)

Fig. 3-8 Read disturbance characteristics of CeO_2 nanocrystal flash memory devices with different annealing ambient. (a) with RTN_2 at 900℃ for 1 min; (b) with RTO_2 at 900℃ for 1 min. No significant V_{TH} occurred at $V_d < 3$ V, even after 1000 s at T = 25°C.

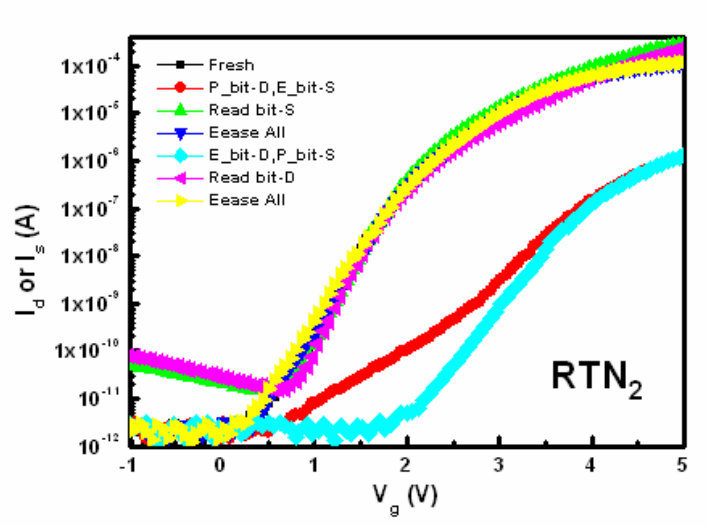


(a)

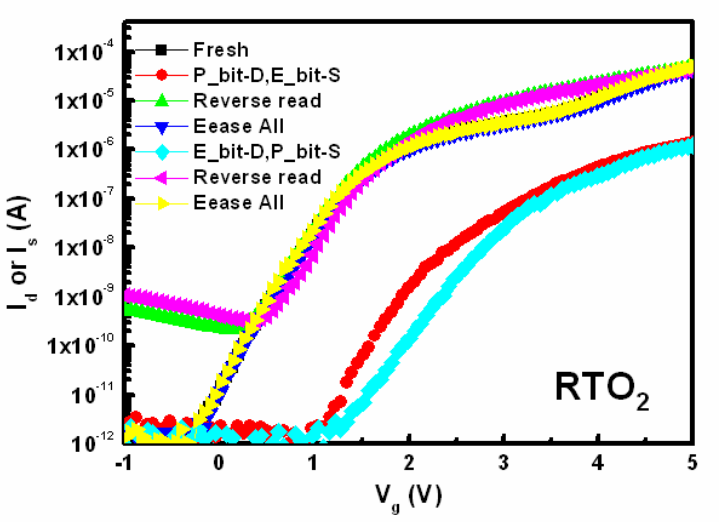


(b)

Fig. 3-9 Drain disturbance characteristics of the CeO_2 nanocrystal memory devices with two different annealing ambient. (a) with RTN_2 at 900℃ for 1 min; (b) with RTO_2 at 900℃ for 1 min. No significant V_{TH} occurred at RTN_2 sample, even after 1000 s at T = 25°C.



(a)



(b)

Fig. 3-10 I_{ds}-V_{gs} curves with CeO_2 nanocrystal memory devices demonstrated two-bit per cell operation. (a) with RTN_2 at 900℃ for 1 min; (b) with RTO_2 at 900℃ for 1 min. Two schemes for reading the four states of these were used.

Table. 3-1 Summary of terminal bias conditions and operation principles for CeO_2 nanocrystal flash memory devices with different annealing (unit: V).

		Program *(CHE)*	Erase *(BBHH)*	Read *(reverse)*
Bit-D	V_g	9	-7	3
	V_d	9	10	0
	V_s	0	0	>2.5
Bit-S	V_g	9	-7	3
	V_d	0	0	>2.5
	V_s	9	10	0

Chapter 4

Characteristics of CeO_2 nanocrystal on O/N tunnel layer nonvolatile memory

4.1 Introduction

Conventional Flash memory device uses floating gate structure and charge is stored in poly-silicon floating gate [4.1]. But when tunnel oxide is below 3nm, floating gate structure faces scaling issues [4.2]. The storage charge is leakage easily due to defects in the tunneling oxide formed by repeated program / erase cycles. So discrete trap memory devices like SONOS structure, nanocrystal memory is widely studied to replace floating gate structure for semiconductor memory application [4.3-4.6]. The CeO_2 NCs memories were fabricated and the electrical properties were investigated at prior chapter. The CeO_2 NC memory devices have shown good electrical properties in terms of large memory window (>2 V) at P/E speed of 10 / 10μs and a retention time up to 10^4 s with only 10% charge loss. Floating gate devices are rapidly approaching serious scaling challenges due to inter-floating gate coupling, while nitridetrapping device is free from such limitations. Nitride-trapping device consists of two main types: SONOS [4.7] which uses channel program/erase, and NROM [4.8] which store charges locally. SONOS memory suffers from retention problems due to direct tunneling leakage through the thin tunnel oxide, and NROM is

sensitive to hot-hole induced damages [4.9]-[4.10]. There has been several proposals that promise the further scaling of NROM [4.11]-[4.12], however, new solutions that do not invoke hot holes are still desirable.

In this study, we explore a double-tunneling (SiO_2/Si_3N_4) layer for SONOS-type memory devices with CeO_2 NC as a charge storage layer. Taking advantage of the high charge storage of CeO_2 NC and enhanced hole tunneling current through the SiO_2/Si_3N_4 tunneling layer, fast P/E and wide memory window can be achieved.

4.2 Experimental

The CeO_2 nanocrystals memory devices were fabricated by LOCOS (Local Oxidation of Silicon) isolation on (100) p-type Si substrates with a resistivity of ca. 5–10 Ω·cm. A schematic representation of an n-channel metal oxide semiconductor field effect transistor (MOSFET) with a CeO_2 nanocrystal memory structure is shown in Fig. 4-1. The thermal oxide grown at 1000°C in a horizontal furnace system was designed a thicknesses of 2.0 nm. Subsequently, a 2.0 nm-thick nitride was deposited using a low-pressure tetraethoxysilane system. The thickness of double-tunneling layer checked with ellipsometer. We employed an evaporator gun (E-gun) system to deposit a thin CeO_2 layer at 10^{-6} Torr with pure CeO_2 (99.9%) sources. All samples

subsequently underwent RTA at 900 °C for 60 s in N_2 or O_2 ambient to form self-assembled CeO_2 nanocrystals. A 15-nm-thick BO was deposited using a low-pressure tetraethoxysilane system. A 200-nm-thick polycrystalline silicon (poly-Si) gate was deposited by low-pressure chemical vapor deposition (LPCVD) and then defined by lithography and gate etching. Subsequently, the poly-Si gate and source/drain (S/D) region were implanted using arsenic (5×10^{15} /cm^2, 20 keV) and dopant activation was performed at 950 °C for 15 s. Finally, substrate contact patterning and the rest of the standard CMOS procedure were completed to fabricate the CeO_2 nanocrystal memory devices. The electrical properties of such devices were measured using an HP 4156B semiconductor parameter analyzer and an HP 41501A pulse generator expander.

4.3 Results and Discussion

4.3.1 Material analysis of CeO_2 nanocrystals on Si_3N_4

In the Atomic force microscopy (AFM) image shown in Fig. 4-2(a) and 4-2(b), white dots indicate the formation of the CeO_2 nanocrystals after O_2 and N_2 RTA at 900 °C. We estimated that the nanocrystals density is ca. 5×10^{11} cm^{-2} and that the average nanocrystal space is ca. 14 nm, which ensures the electrical insulation between two nanocrystals.

4.3.2 Electrical characteristics

The programming speed of the CeO_2 NCs memory devices with RTO_2 annealing are shown in Fig. 4-3. The device is programed by CHE injection. When the program voltage increases to 10 V, the V_{th} shift increases rapidly and a memory window greater than 5 V was achieved within 1 ms. The large memory windows make the multilevel operation possible. The fact the programming speed is independent of annealing condition of the charge trapping centers, indicating that the programming speed is primarily dependent on the tunneling oxide.

Figure 4-4(a) shows the erasing speeds at different voltages operation. The device is erased band-to-band hot-hole (BBHH) injection. For the erasing speed operation, the device was programed under V_g = 9 V, V_d = 9 V with a duration of 1 ms. As observed, an increase in the negative gate bias resulted in a high erasing speed due to a higher electrical field for the BBHH injection. A fully erased state was fulfilled within 1 ms when operating at V_g = -6 V and V_d = 10 V. We concluded that using the CHE for programming and the BBHH for erasing has achieved high P/E efficiency in the CeO_2 NC memory devices. Figure 4-5 shows the data retention characteristics of the CeO_2 NC memory devices with different RTA treatments and programming states. The RTN_2 sample showed a smaller amount of charge loss at room temperature for a retention times up to 10^4 s than the RTO_2 sample. It is conjectured that the bulk traps

of RTN_2 sample are deeper than RTO_2 sample so that the charge loss of RTN_2 sample is less than RTO_2 sample. This phenomenon can be ascribed to the fact that sufficiently deep trap energy levels exist in the CeO_2 NCs. The electrons can be either trapped in these bulk defects or stay in the conduction band of the CeO_2 NCs and/or in the interface states between the CeO_2 NCs and SiO_2.

Fig. 4-6 Endurance characteristics of CeO_2 nanocrystal memory devices with different annealing ambient. The P/E window with two samples do not show any closure even after 10^4 cycles. The programming and erasing conditions are $V_g = V_d =$ 8 V for 0.1 ms and V_g = -6 V, V_d = 10V for 0.1 ms for different annealing samples. We find that the memory windows narrowing increases with increasing P/E cycles. The RTN_2 CeO_2 nanocrystal memory windows is about 2 V after 10^4 P/E cycles better than RTO_2 CeO_2 nanocrystal memory device. It may be due to channel hole-tunneling erase is a uniform erase thus electrons cannot pile up at the channel center region. We believe that endurance characteristics can be improved by nitride / oxide tunneling layer. Fig. 4-7 I_{ds}-V_{gs} curves with CeO_2 nanocrystal memory devices demonstrated two-bit per cell operation at RTN_2 annealing. These schemes are the forward and reverse read schemes for recognizing the information stored in the program states of Bit-D and Bit-S, respectively. Table 4.1 summarizes terminal bias conditions and operation principles for CeO_2 nanocrystal with RTN_2 annealing on O/N tunnel layer

nonvolatile memory cell.

4.4 Summary

In this chapter, we utilized the stack tunneling layer replaces conventional SiO_2 tunneling layer. The CeO_2 nanocrystals also can form self-assembled on nitride layer under different RTA ambient. The CeO_2 nanocrystals on O/N tunnel layer flash memory device also used CeO_2 nanocrystals as a charge trapping layer. It was demonstrated that the fabricated memories exhibit higher program/erase speed, long retention time with RTN_2 memory device. In particular, two-bit per cell operation has been successfully demonstrated.

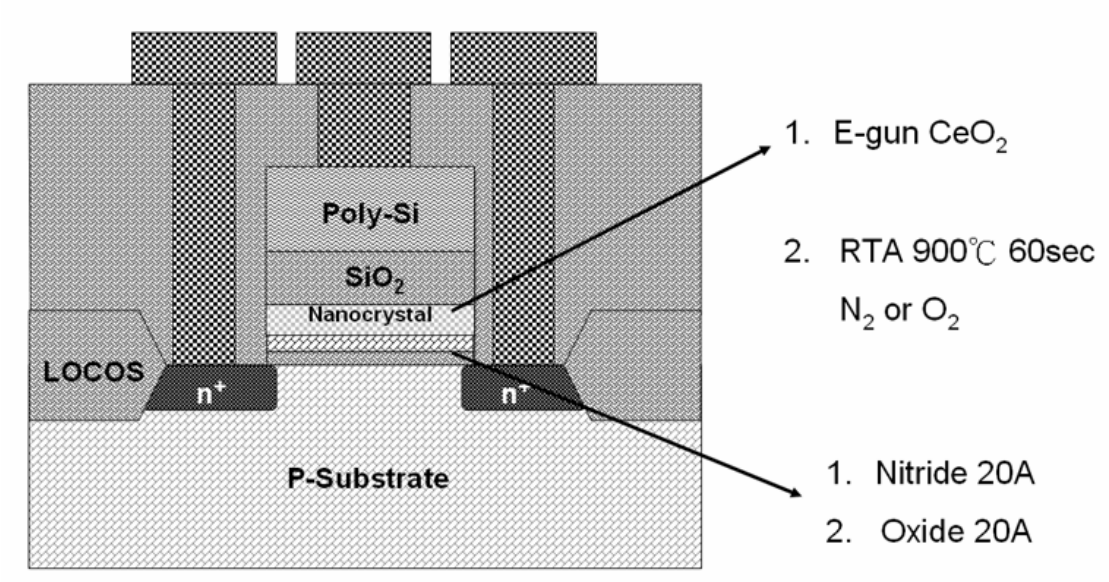
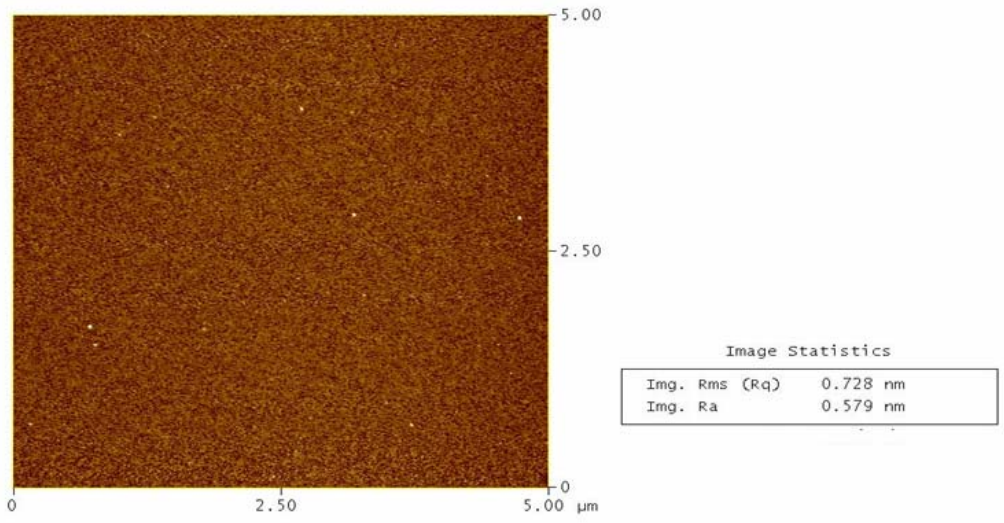
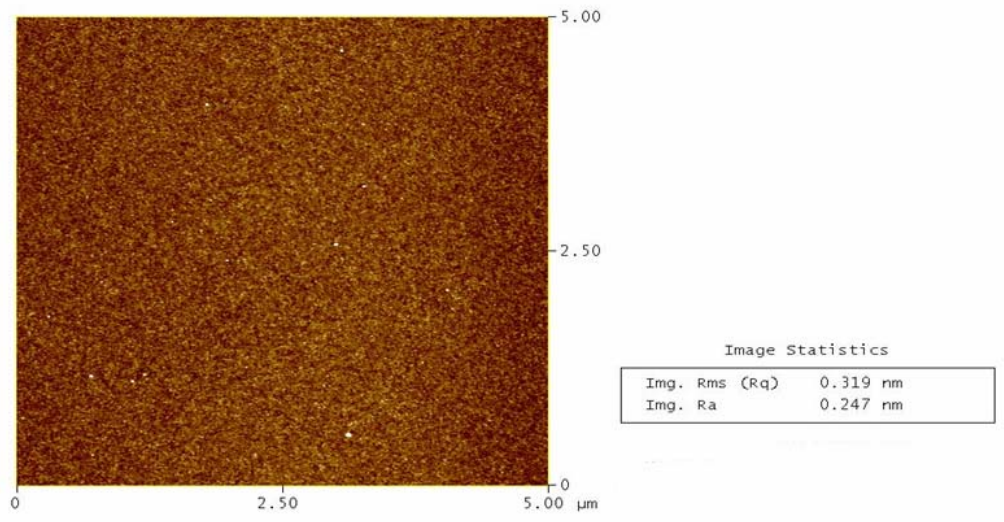


Fig. 4-1 Schematic representation of CeO_2 nanocrystal flash memory devices on O/N tunneling layer with main process conditions.

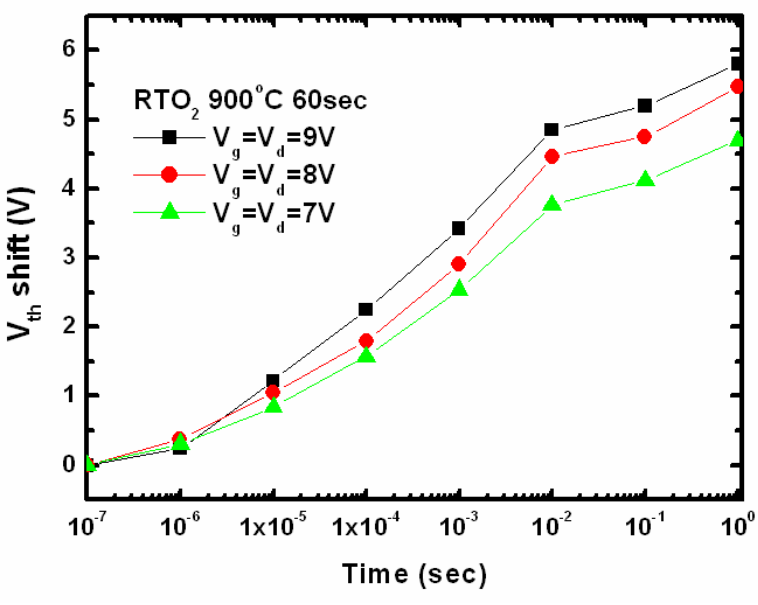


(a)

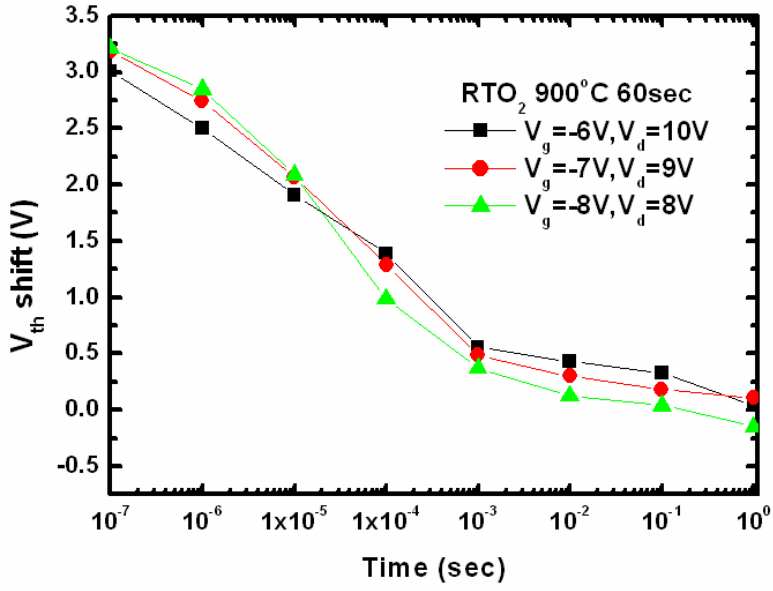


(b)

Fig. 4-2 Cross-sectional TEM images of the CeO_2 nanocrystals embedded in Si_3N_4 dielectric matrix with (a) RTN_2 annealing at 900℃ for 1 min; (b) RTO_2 annealing at 900℃ for 1 min

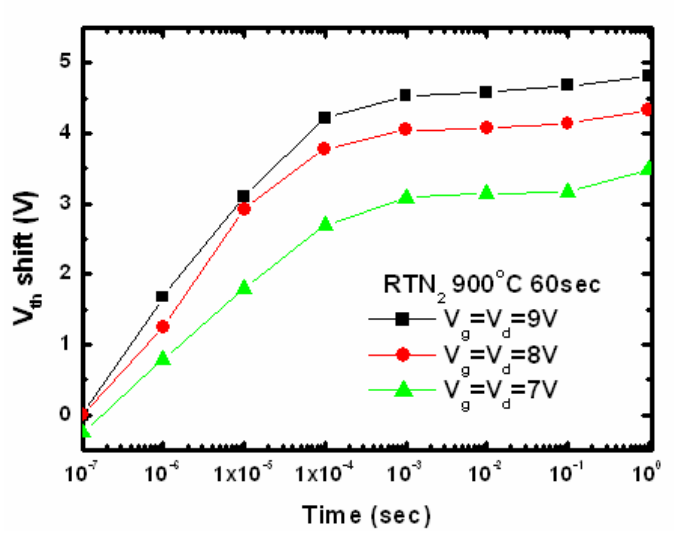


(a)

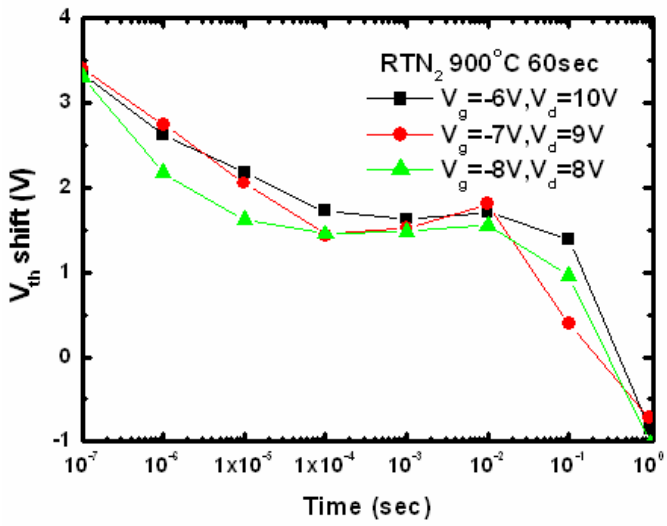


(b)

Fig. 4-3 (a)Programming speed and (b) erasing speed characteristics of CeO_2 nanocrystal flash memory devices with RTO_2 annealing as a function of time.



(a)



(b)

Fig. 4-4 (a)Programming speed and (b) erasing speed characteristics of CeO_2 nanocrystal flash memory devices with RTN_2 annealing as a function of time.

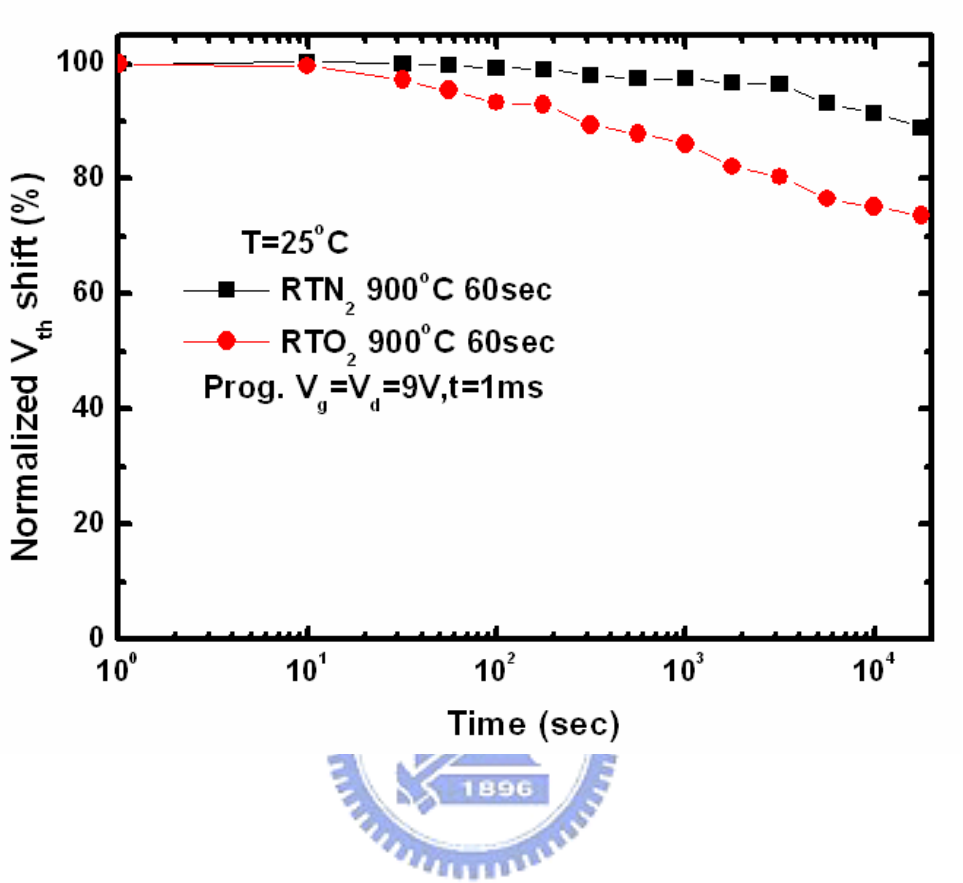


Fig. 4-5 Retention characteristics of CeO_2 nanocrystal flash memory devices at programming states with different treatments.

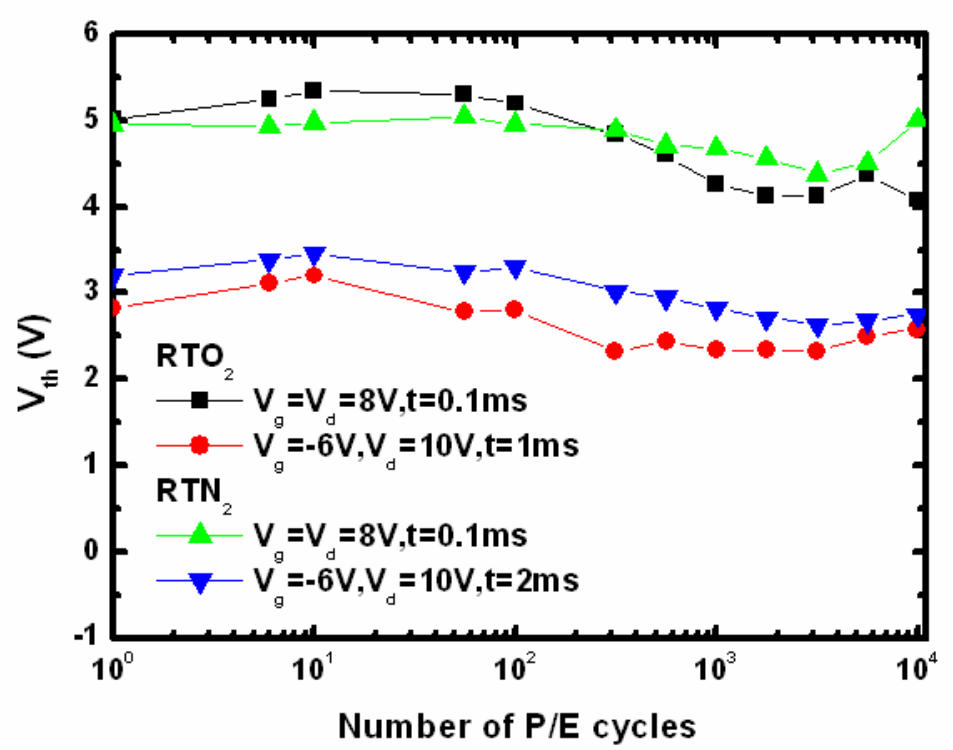


Fig. 4-6 Endurance characteristics of CeO_2 nanocrystal memory devices with different annealing ambient. The P/E window with two samples do not show any closure even after 10^4 cycles.

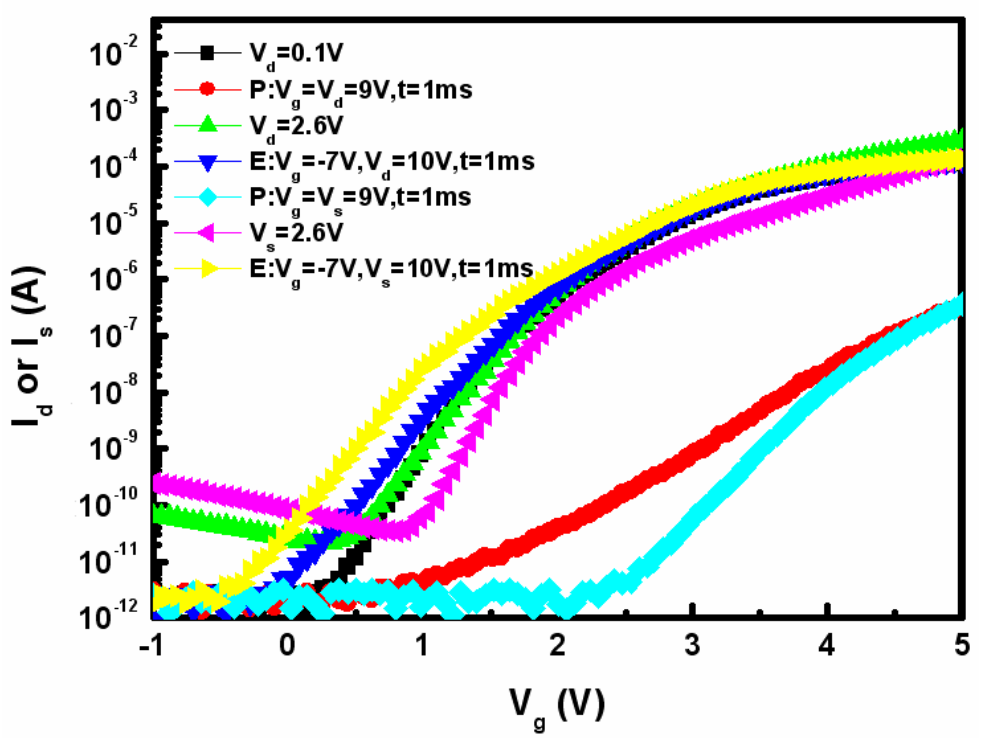


Fig. 4-7 I_{ds}-V_{gs} curves with CeO_2 nanocrystal memory devices demonstrated two-bit per cell operation at RTN_2 annealing. These schemes are the forward and reverse read schemes for recognizing the information stored in the program states of Bit-D and Bit-S, respectively.

Table. 4-1 Summary of terminal bias conditions and operation principles for CeO_2 nanocrystal with RTN_2 annealing on O/N tunnel layer nonvolatile memory cell (unit: V).

		Program *(CHE)*	Erase *(BBHH)*	Read *(reverse)*
Bit-D	V_g	9	-7	3.5
	V_d	9	10	0
	V_s	0	0	>2.6
Bit-S	V_g	9	-7	3.5
	V_d	0	0	>2.6
	V_s	9	10	0

Chapter 5

Substrate effects and Charge-Pumping of CeO_2 nonvolatile nanocrystal memory

5.1 Introduction

SONOS-type memory has long been considered as the promising candidate for flash memory due to its simple structure, lowoperation voltage, excellent cell scalability and compatible process with CMOS. We find that drain voltage is the key point to improve P/E efficiency in nonvolatile memory devices[5.1]-[5.6]. The mechanism is due to the floating body induced drain avalanche with parasitic n-p-n bipolar in the devices. We can reduce the applied drain voltage to achieve higher P/E efficiency by this floating body effect compared with bulk memory devices.

Different from the floating gate devices, the programmed charges in nanocrystal storage devices are more likely to be localized trapped and this results in the much higher threshold voltage of the area than that elsewhere along the channel. The charge-pumping (CP) technique is a well-known methods used for profiling trapped charge and interface states in MOSFETs, after a hot-carrier stress[5.7]-[5.13]. This technique was proposed to extract the threshold voltage (V_t) profile and thus the distribution of interface states and trapped charges in ref. 10. There're two ways of CP test: the constant V_b (the base level of the gate pulse) and constant V_h (the high level

of the gate pulse) charge pumping methods, which are defined as CV_b and CV_h, respectively. CeO_2 nanocrystal memory has the localized charge trapping character, which has different on FN-programming and CHE-programming with charge-pumping (CP) measurement. The trapped charges can be stored in a very narrow region close to drain side after CHE-programming [5.14], and affected by different programming bias. Studies have also shown that the charge distribution is a key factor related to the reliability of memory devices [5.15] and two-bit characteristics [5.16]. Therefore, it's essential to study the distribution of the trapped charges.

In the study, we demonstrate reduce the applied drain voltage to achieve higher P/E efficiency by this floating body effect compared with bulk memory devices. With different programming operation, it is clear that one peak of Icp curve at FN-programming and two peak of I_{cp} curve at CHE-programming. The different charge distribution due to the charge storage in the nanocrystal memory.

5.2 Substrate floating effects

Flash memory for Channel hot-electron (CHE) programming is achieved by applying high voltage to both drain and gate simultaneously. With the control gate high, the high voltage across the drain to source gives a high channel current and

channel field which generates hot electrons. The high voltage on the control gate couples a voltage to the floating gate and attracts hot electrons to the floating gate. Fig. 5-1 Illustration of flash memory can be operated V_g=V_d for CHE injection to program and no body contact (substrate is floating). Parasitical bipolar increased drain current to enhance hot electrons. Fig. 5-2 (a) I_d-V_d curve of CeO_2 nanocrystal memory devices with different body contact condition. After sweep I_d-V_d, (b) the threshold voltage shift with floating body is larger than V_b = GND. Fig. 5-3 I_d-V_d curve of CeO_2 nanocrystal memory devices with (a)body is floating and (b) body is ground. Parasitical n-p-n bipolar device early increased drain avalanche at body is floating.

Program characteristics of CeO_2 nanocrystals memory devices with different programming conductions and no body contact (substrate floating) were shown in Fig. 5-4. The mechanism is due to the floating body induced drain avalanche with parasitic n-p-n bipolar in the flash memory devices. We can reduce the applied drain voltage to achieve higher P/E efficiency by this floating body effect compared with bulk memory devices. In the Fig. 5-5, it shows erase characteristics of CeO_2 nanocrystals memory devices at different erasing voltage conductions and with no body contact (substrate floating) with a fixed V_d of 10 V. As observed, the nanocrystal memory with no body contact resulted in the high erasing speed due to drain avalanche with parasitic n-p-n bipolar. A fully erasing behavior was fulfilled within 1 ms at V_g = -6 V

and V_d = 10 V. These results displayed a little overerasing in the obtained erase curves. We concluded that using the CHE for programming and the BBHH for erasing results in high P/E efficiency with substrate floating in the CeO_2 nanocrystal memory devices.

Retention characteristic of CeO_2 nanocrystals memory devices at T=25°C and T=85°C with/without body contact are shown in Fig.5-6(a) and (b), respectively. As observed, the memory device showed the same amount of charge loss at RT at measuring times up to 10^4 s for with/without body contact; this phenomenon can be ascribed to the fact that Frenkel-Poole emission charge independ on with/without body contact. In the Fig. 5-7(a) and (b), it shows drain disturbance characteristics of the CeO_2 nanocrystals memory devices with/without body contact. The drain disturbance characteristics at erase state display small V_{th} but at program state display large V_{th}. Fig. 5-8(a) and (b) is the endurance characteristics of the CeO_2 nanocrystals memory devices with/without body contact after 10^4 cycles.

5.3 Charge pumping characteristics

Schematic diagrams the flash memory cell setup for charge-pumping measurement is shown in Fig. 5-9, respectively. It will known that the charge pumping measurement is used to quantify the interface state density by monitoring the

substrate current. We used a trapezoidal gate pulse having a fixed pulse amplitude with a varying V_{gbl}. The substrate current (the so-called "charge pumping current," I_{cp}) as a function of V_{gbl} was measured. The gate pulses have a frequency of 1 MHz and a 50% duty cycle; the rising and falling times were both 100ns. In this work, Fig. 5-10 (a) is schematic diagrams illustrating the pulse waveform and Fig. 5-10(b) show the stepping pulse base voltage with fixed pulse amplitude for charge-pumping measurement. Conventional charge-pumping current versus base voltage with different pulse amplitude voltage was shown in Fig.5-11, respectively. We found that the pulse amplitude voltage increase the charge-pumping current increasing. Then, we choose small pulse amplitude voltage in order that without affect the charge injection. Fig. 5-12 (a) rise time dependence of charge-pumping curves for fixed fall time of 100ns and Fig. 5-12 (b) fall time dependence of charge-pumping curves for fixed rise time of 100ns conduction[5.18], respectively. It found the rise time and fall time depent on charge-pumping current weakly. Then, it illustrate the interface traps density may be at half of Si bandgap. The I_d-V_g curves of the CeO_2 nanocrystal nonvolatile memory at different programming state under FN-programmed method to operate is shown in Fig. 5-13(a), respectively. Fowler–Nordheim tunneling was used to program the cell with V_{th} levels from 1.32 to 5.61 V[5.17]. Figure 5-13 (b) is the charge-pumping current versus base voltage under FN-programmed method. The

program state I_{cp} curve shifted increasingly toward the right upon increasing the value of V_{th} as a result of an increase in the amount of injected charge in the CeO_2 nanocrystal trapping layer. We demonstrated that the injection charge storage the CeO_2 nanocrystal trapping layer. Fig. 5-14 (a) was shown I_d-V_g curves of the CeO_2 nanocrystal nonvolatile memory at different programming state under CHE-programmed method to operate and Fig. 5-14 (b) was shown the charge-pumping current versus base voltage under CHE-programmed method. Interestingly, two humps appeared in I_{cp} curve due to two different V_{th} at drain-side and source-side. We traced the measured curve to a horizontally shifted curve that large charge injection to the CeO_2 nanocrystal trapping layer. In addition, we also analyzed the devices formed from a pure CeO_2 trapping layer on top of a SiO_2 tunnel oxide structure. Consequently, we conclude that CeO_2 nanocrystals can behave as an excellent local charge trapping centers.

5.4 Summary

We research the CeO_2 nanocrystal nonvolatile memory operated with no body contact (substrate floating). The operation voltage of memory cell can be reduced 1 V at program model to decrease disturbance. Nevertheless, the date retention characteristic is similar. We demonstrated the charge-pumping current is depend on

interface traps and bulk traps for different programming methods affect the SONOS-type memory border traps. The different programming method shows different charge-pumping curves. Under CHE-programmed operation, two humps appeared in I_{cp} curve due to two different V_{th} at drain-side and source-side. We concluded that CeO_2 nanocrystals can behave as an excellent local charge trapping centers.

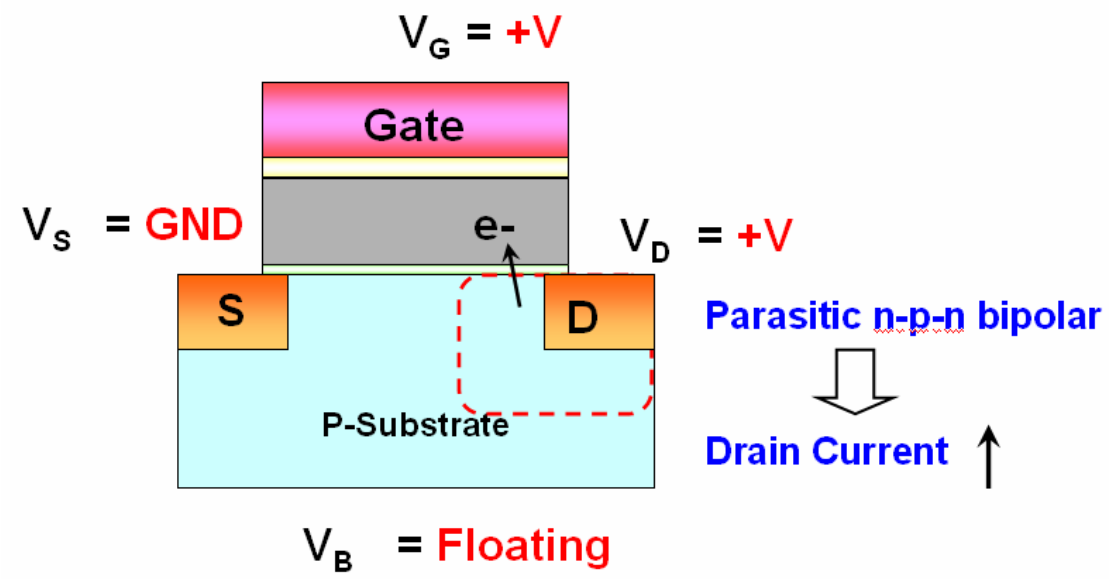
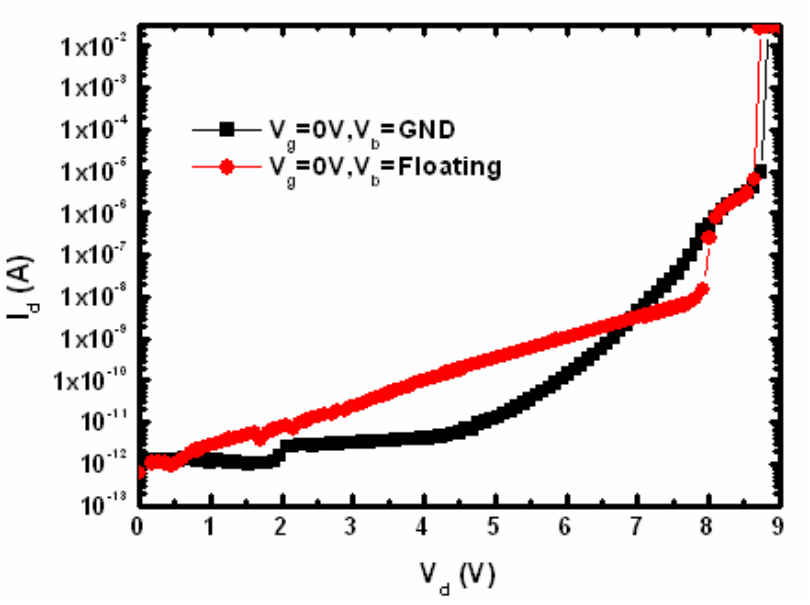
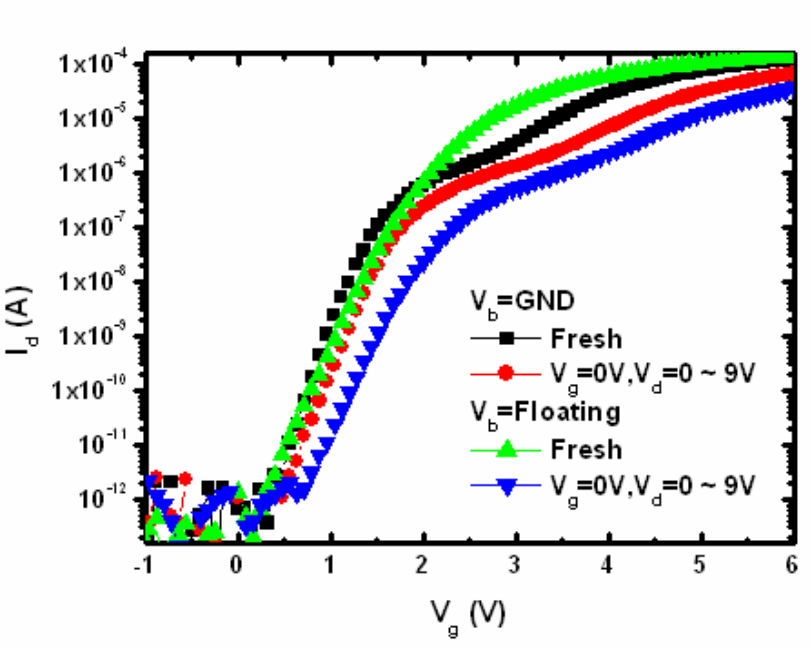


Fig. 5-1 Illustration of flash memory can be operated V_g=V_d for channel hot electrons injection to program and no body contact (substrate is floating). Parasitical bipolar increased drain current to enhance hot electrons.

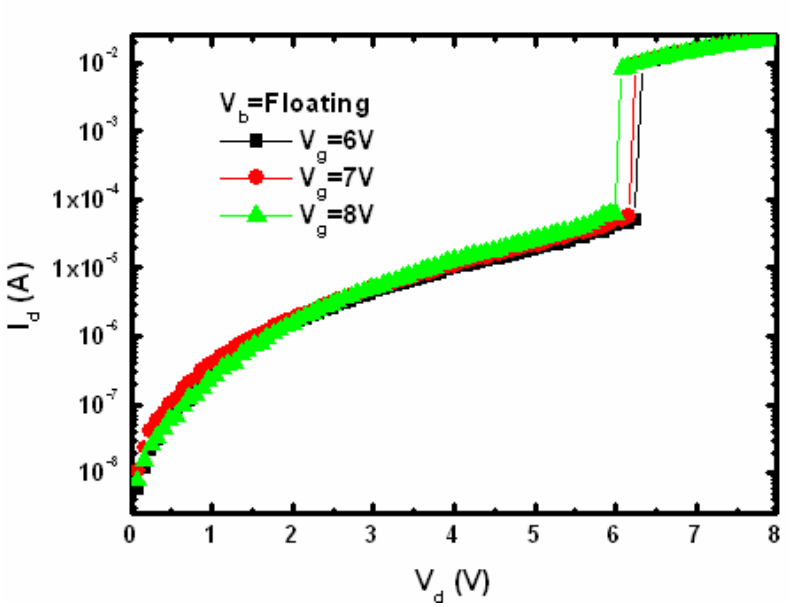


(a)

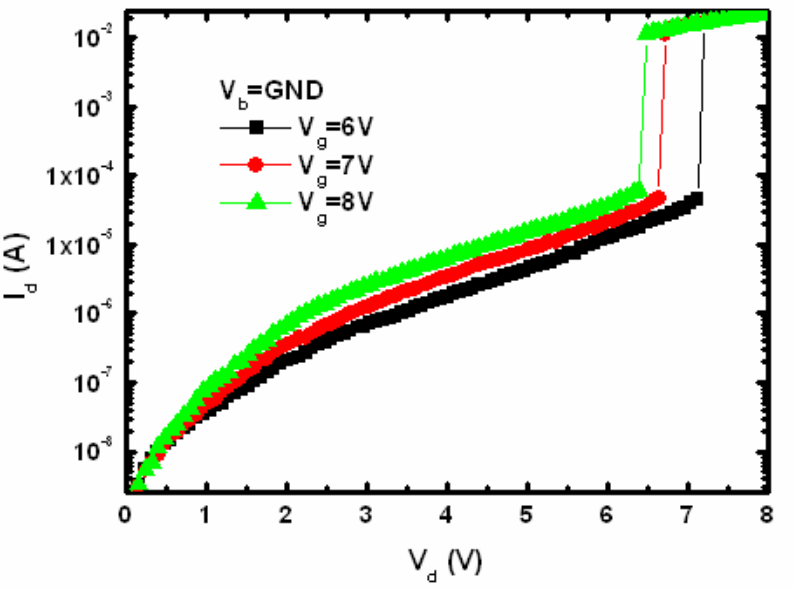


(b)

Fig. 5-2 (a) I_d-V_d curve of CeO_2 nanocrystal memory devices with different body contact condition. After sweep I_d-V_d, (b) the threshold voltage shift with floating body is larger than V_b = GND.



(a)



(b)

Fig. 5-3 I_d-V_d curve of CeO_2 nanocrystal memory devices with (a)body is floating and (b) body is ground. Parasitical n-p-n bipolar device early increased drain avalanche at body is floating.

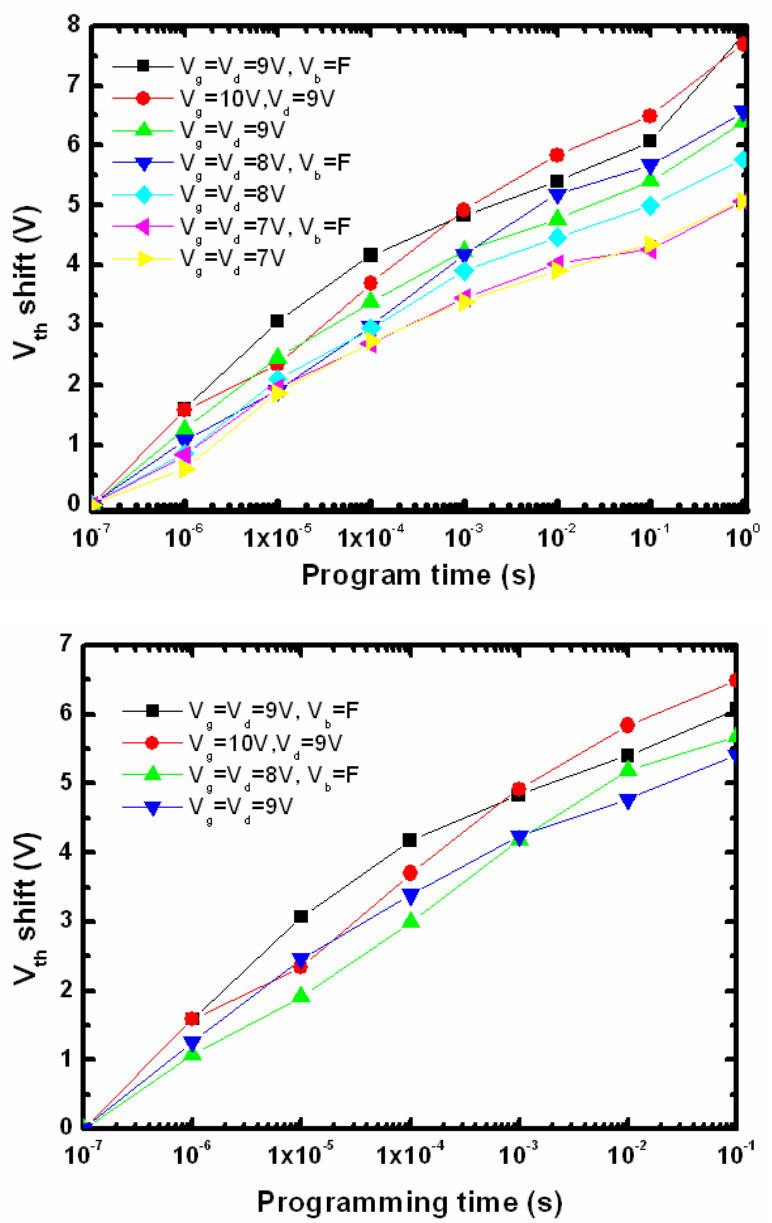


Fig. 5-4 Program speed characteristics of CeO_2 nanocrystals memory devices with different programming conductions and no body contact (substrate floating). The mechanism is due to the floating body induced drain avalanche with parasitic n-p-n bipolar in the flash memory device.

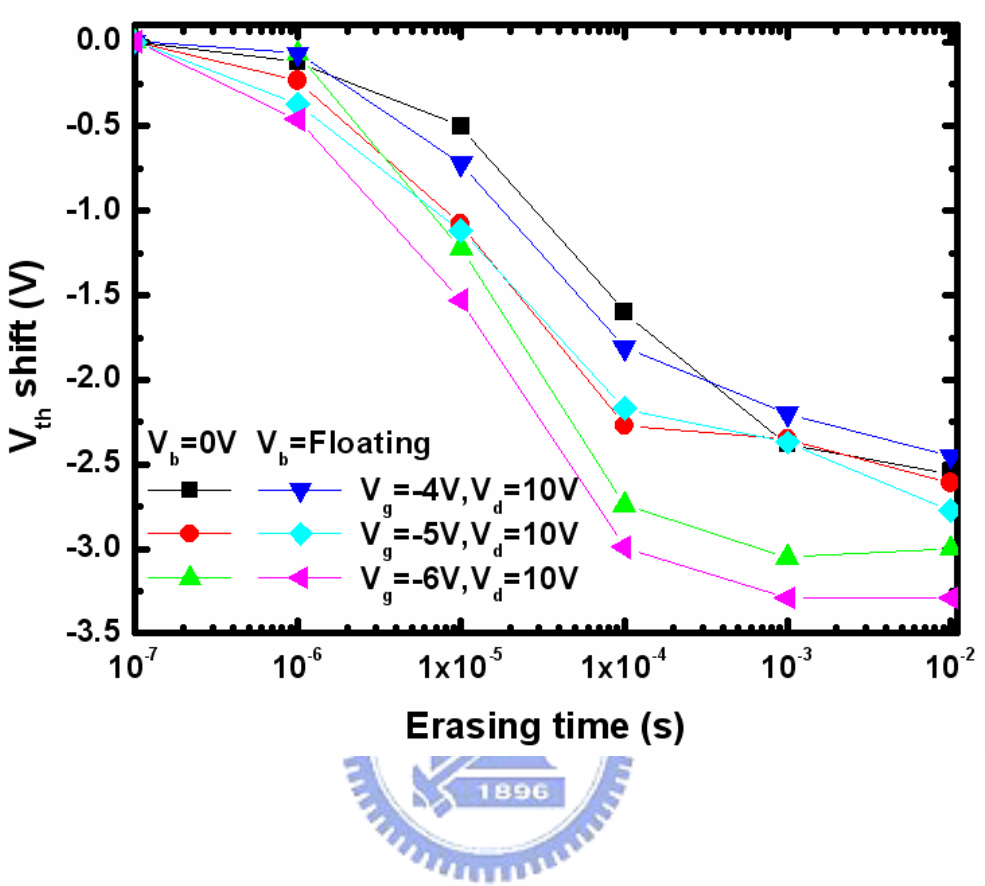
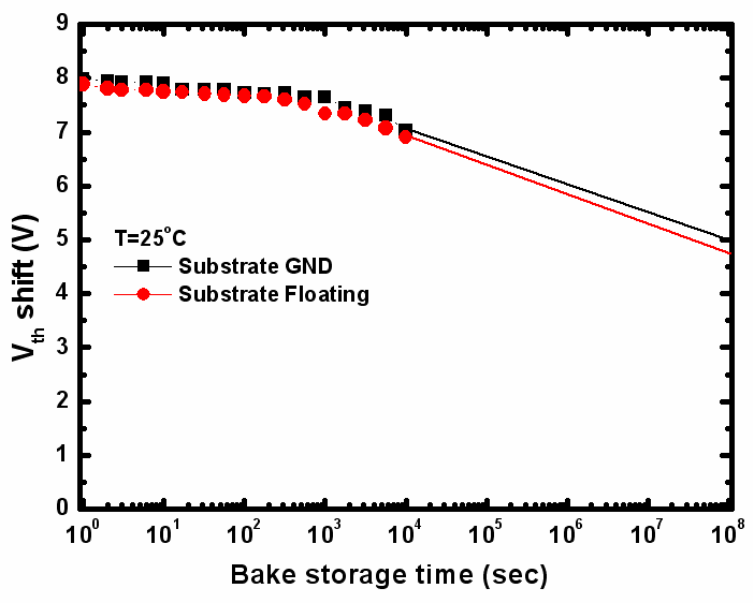
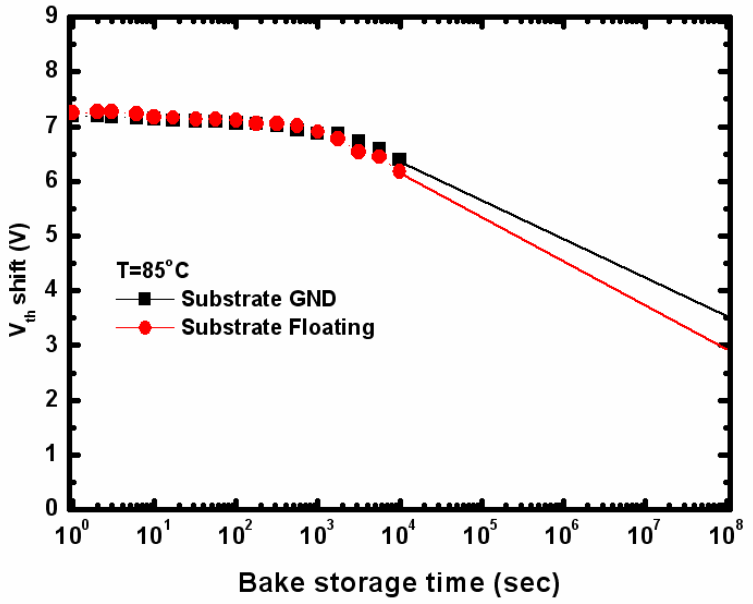


Fig. 5-5 Erasing speed characteristics of CeO_2 nanocrystals memory devices with different erasing voltage conductions and no body contact (substrate floating).

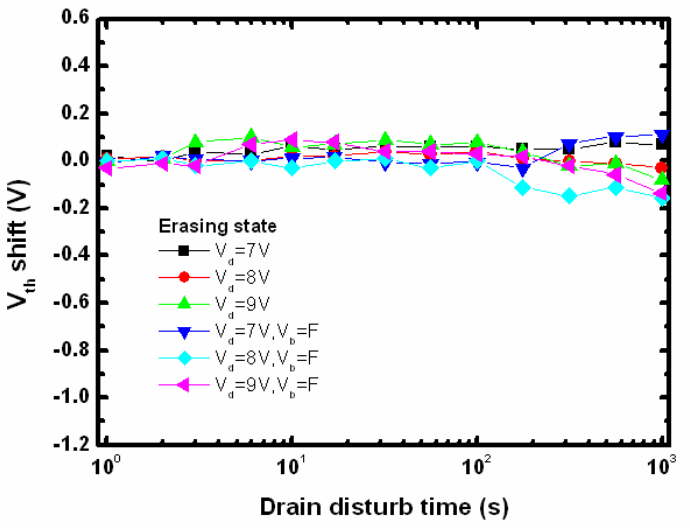


(a)

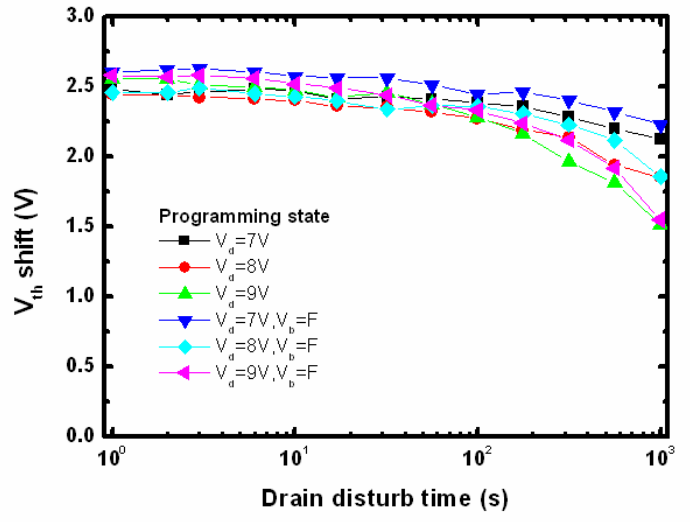


(b)

Fig. 5-6 Retention characteristics of CeO_2 nanocrystals memory devices at (a) T=25°C and (b) 85°C with/without body contact.

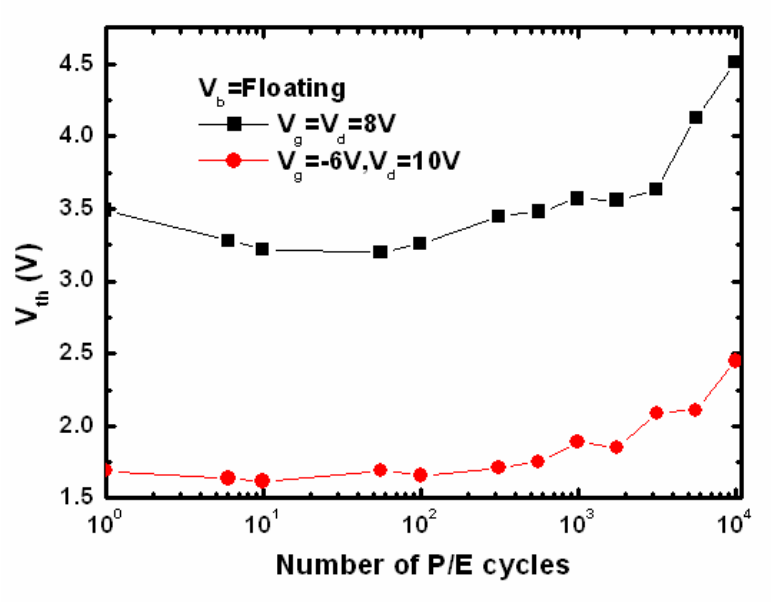


(a)

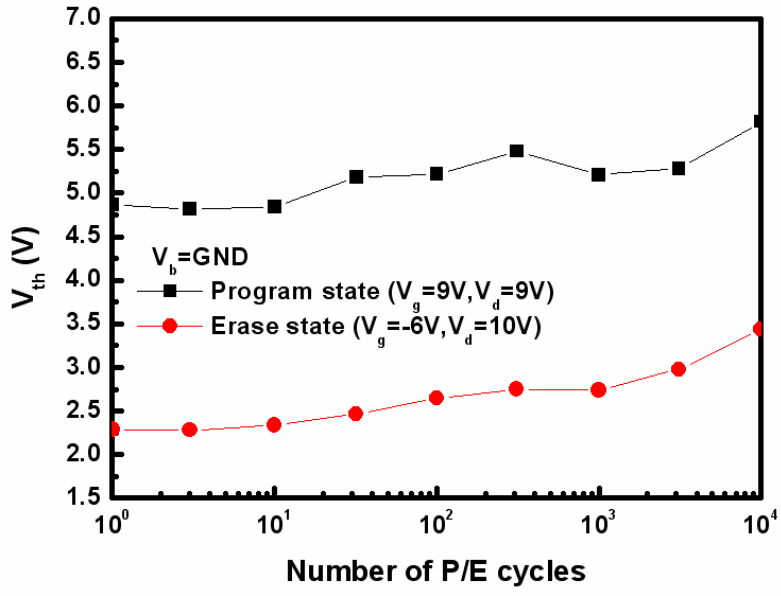


(b)

Fig. 5-7 Drain disturbance characteristics of the CeO_2 nanocrystals memory devices with/without body contact at (a)erasing state; (b) programming state.



(a)



(b)

Fig. 5-8 Endurance characteristics of the CeO_2 nanocrystals memory devices with/without body contact after 10^4 cycles.

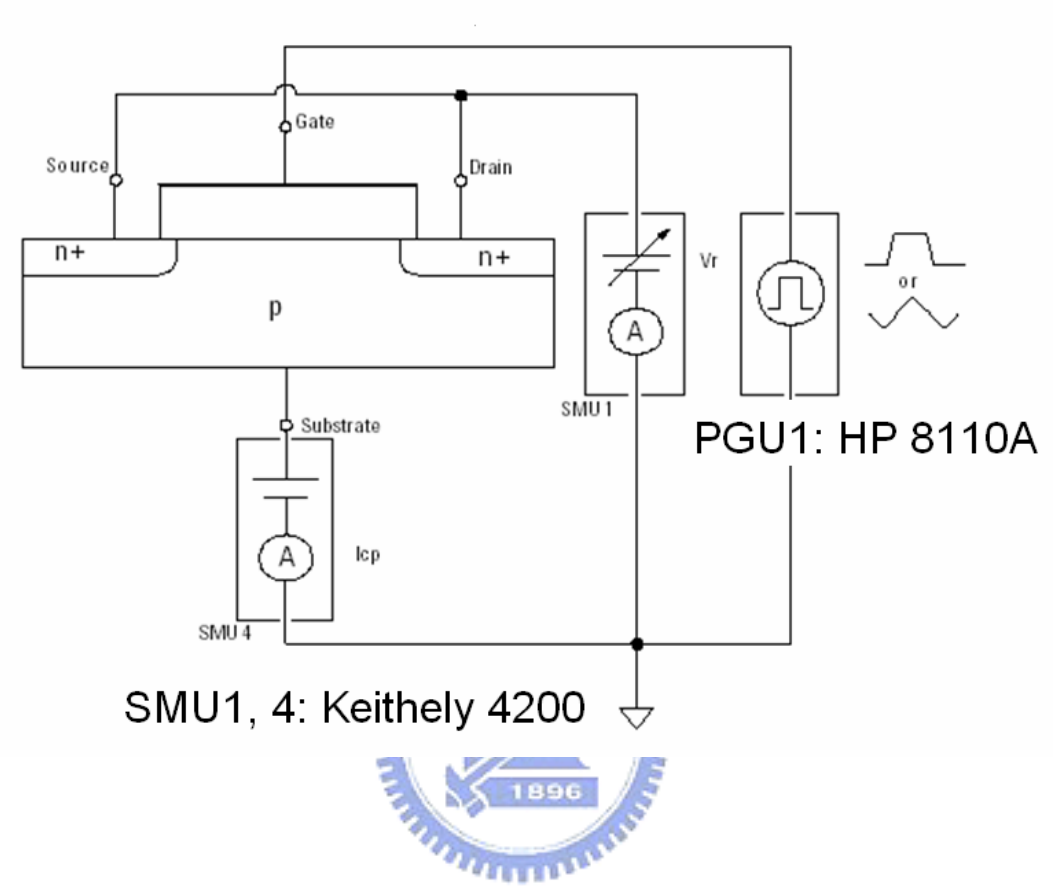
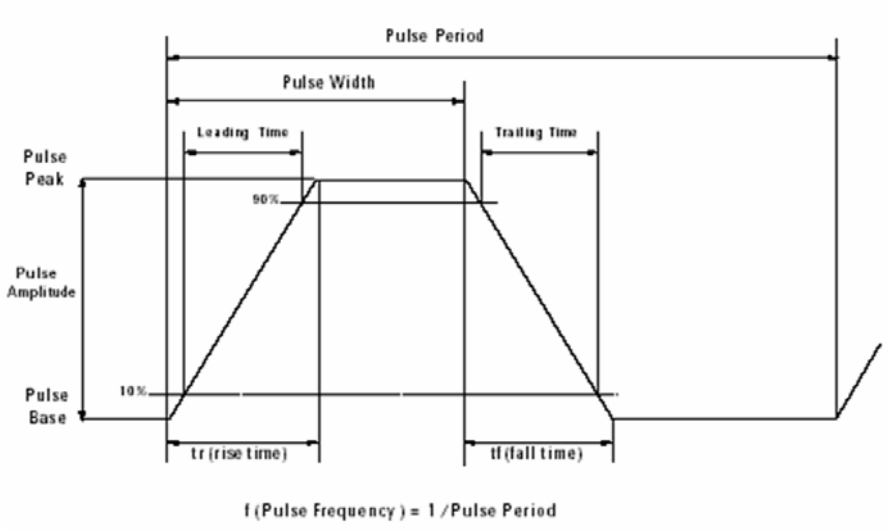
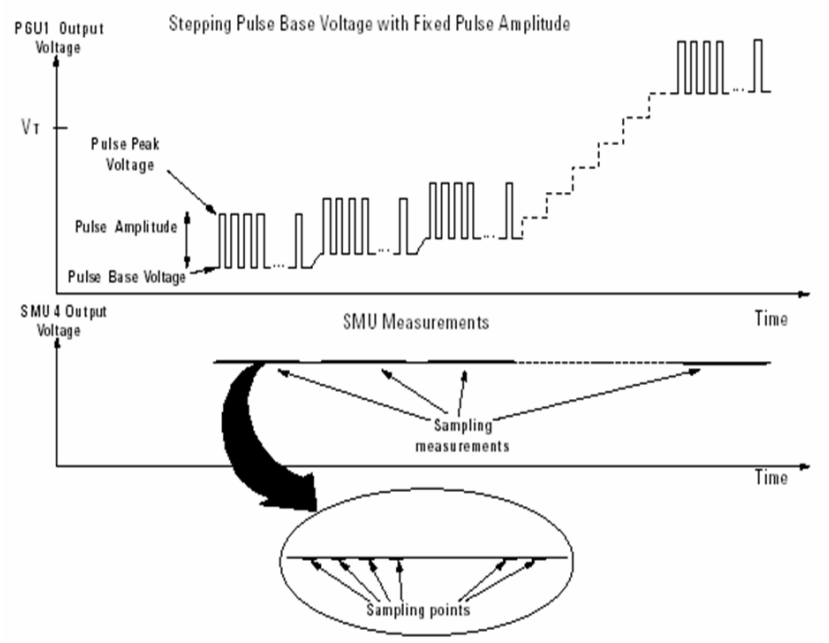


Fig. 5-9 Schematic diagrams the flash memory cell setup for charge-pumping measurement.



(a)



(b)

Fig. 5-10 Schematic diagrams illustrating (a) the pulse waveform and (b) the stepping pulse base voltage with fixed pulse amplitude for charge-pumping measurement.

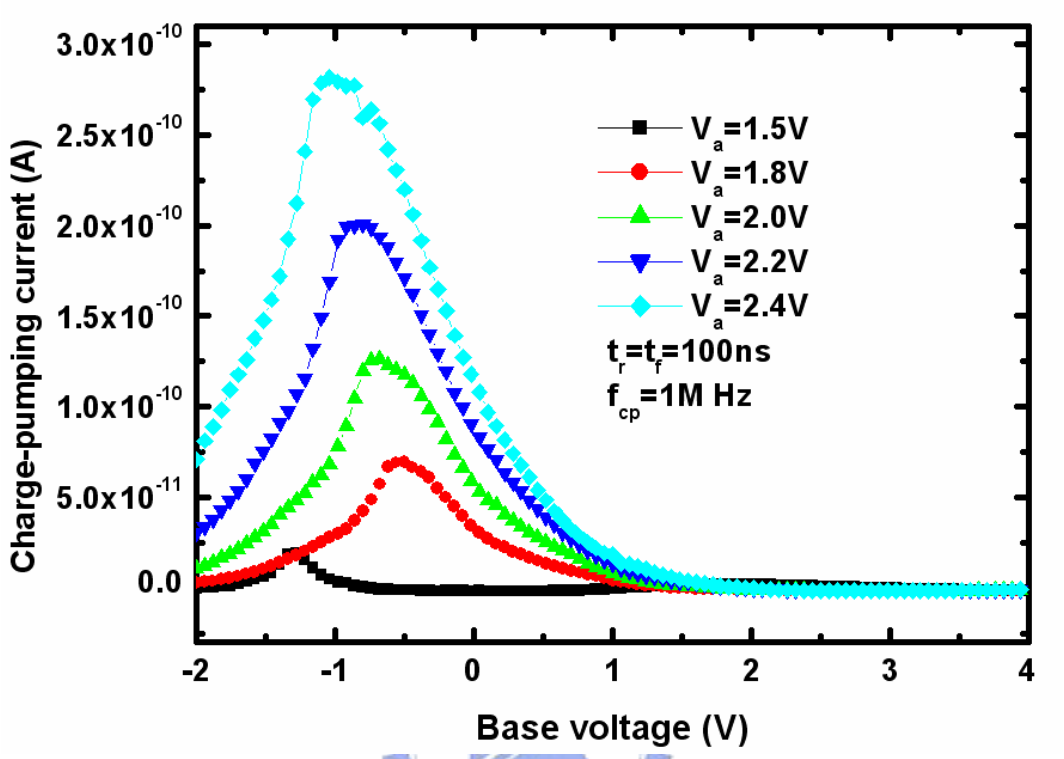
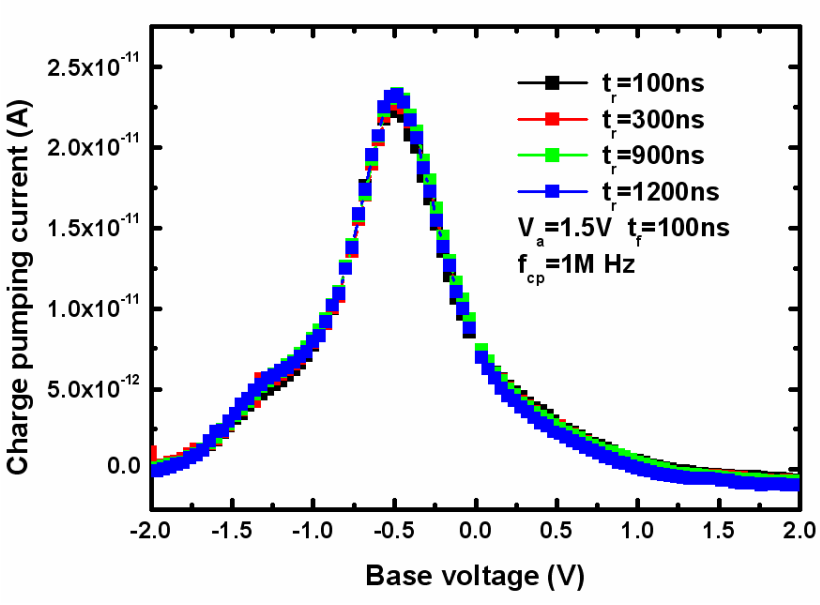
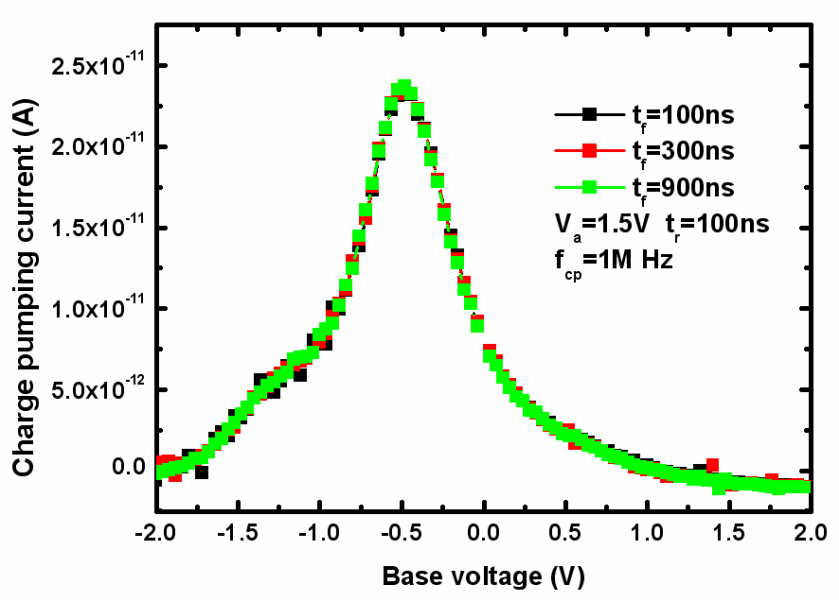


Fig. 5-11 Conventional charge-pumping current versus base voltage with different pulse amplitude voltage.

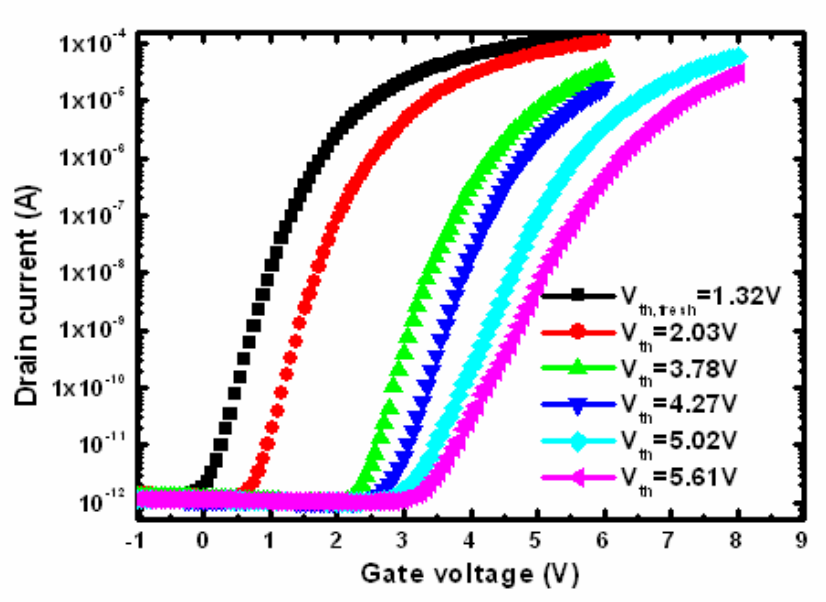


(a)

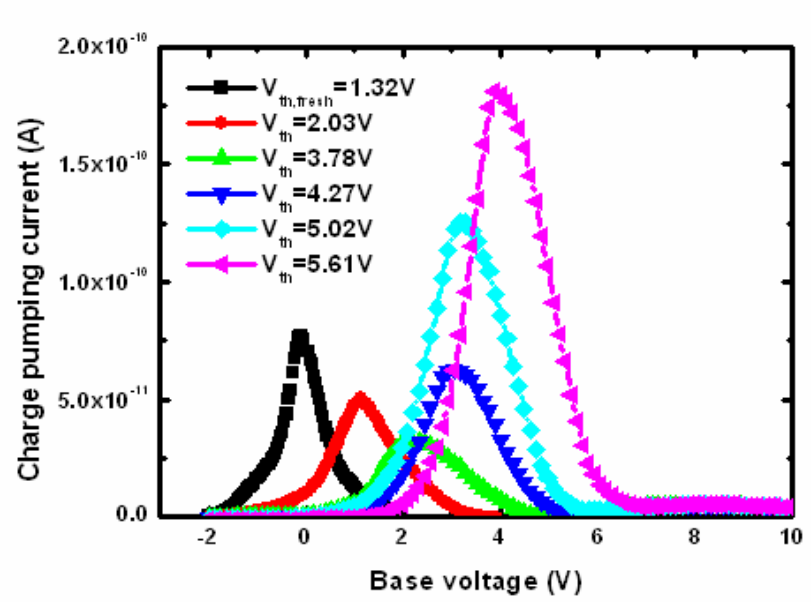


(b)

Fig. 5-12 (a) Rise time dependence of charge-pumping curves for fixed fall time of 100ns, respectively. (b) Fall time dependence of charge-pumping curves for fixed rise time of 100ns conduction.

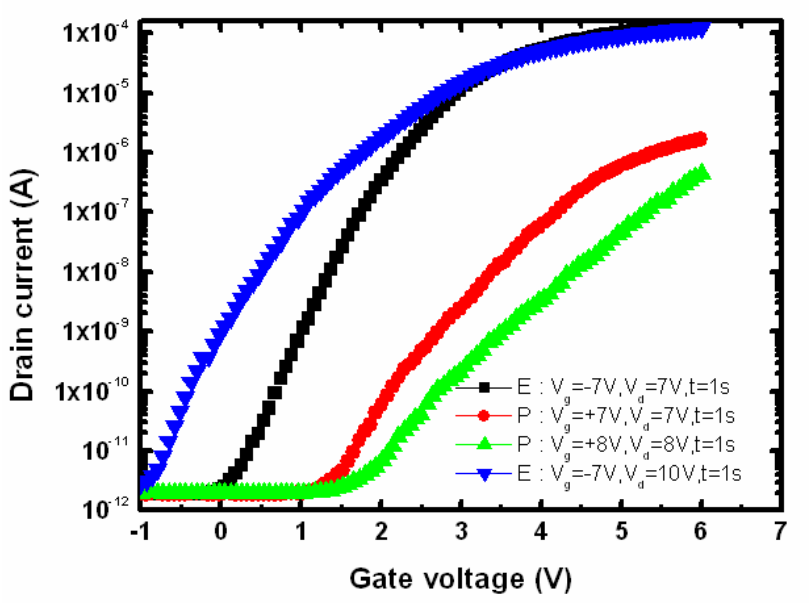


(a)

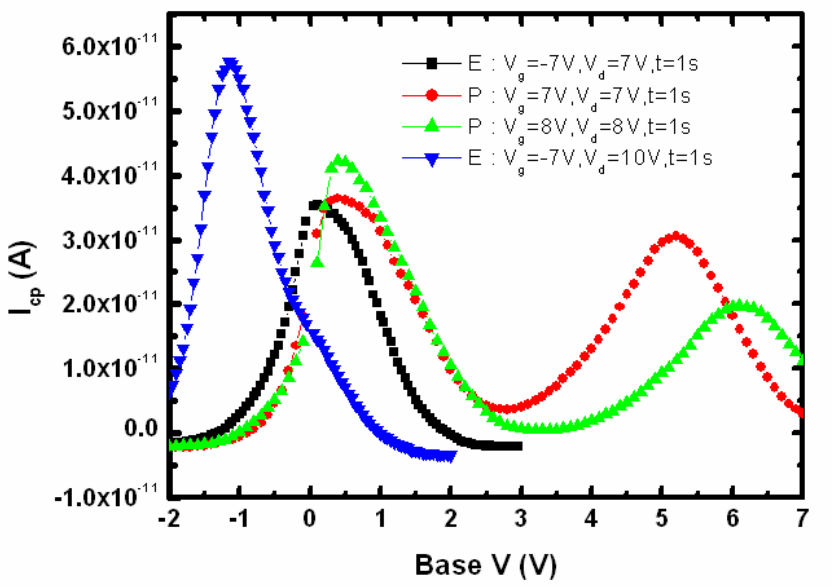


(b)

Fig. 5-13 (a) I_d-V_g curves of the CeO_2 nanocrystal nonvolatile memory at different programming state under FN-programmed method to operate and (b) the charge-pumping current versus base voltage under FN-programmed method.



(a)



(b)

Fig. 5-14 (a) I_d-V_g curves of the CeO_2 nanocrystal nonvolatile memory at different programming state under CHE-programmed method to operate and (b) the charge-pumping current versus base voltage under CHE-programmed method.

Chapter 6
Conclusions and Further Recommendations

6.1 Conclusions

In this thesis, we propose a simple, reproducible and reliable technique for cerium oxide nanoparticle as a charge-trapping layer to fabricate nonvolatile memory. The cerium oxide nanocrystals formed self-assembled by different rapid-thermal annealing (RTA) ambient. This CeO_2 high-k nanocrystals layer replaces the silicon nitride layer in the SONOS-type memory structure. Different program/erase (P/E) methods are also proposed at low power applications. This CeO_2 nanocrystals nonvolatile memory device will have good properties in terms of considerably large memory window, higher P/E speed, long data retention, and good endurance. This memory device is quite suitable for two-bit operation application.

Then, in chapter 3, we have demonstrated the effects of the post-deposition different annealing ambient for the CeO_2 trapping layer on the performance of the SONOS-type flash memories. The memory devices show higher P/E speed of 10 / 10μs. It was found that the CeO_2 nanocrystals memory different retention time caused by annealing ambient influence the deep-trapping level. Moreover, we found that the RTN CeO_2 NC trapping layers have a larger charge storage capacity and a longer retention time up to 10^4 s with only 10% charge loss than the RTO sample due to

deeper trap center. However, the basic electrical operation characteristics are similar. This was ascribed to the larger amount and the shallower energy levels of the crystallization-induced traps. Finally, in the aspect of disturbances, we show only insignificant disturbances properties presented in the normal operation. It was indicated that the fabricated memories exhibit higher program/erase speed, long retention time. In particular, two-bit per cell operation has been successfully demonstrated. We concluded that the RTN_2 CeO_2 NCs can be used a promising canadidate as discrete charge trapping sites for the Flash memory devices application.

In this chapter 4, a stack gate of O/N tunneling layer is investigated as a tunneling layer to replace the conventional silicon dioxide tunneling layer in the CeO_2 nonvolatile nanocrystal memory. The CeO_2 nanocrystals also self-assembly on nitride layer with different RTA annealing ambient. It was demonstrated that the RTN_2 CeO_2 NCs memory exhibit higher program/erase speed, long retention time than the RTO_2 CeO_2 NCs memory. These memory devices also have been successfully demonstrated two-bit per cell operation.

In chapter 5, proposes substrate effects and charge-pumping for CeO_2 nonvolatile nanocrystal memory. The flash memory operates no body contact (substrate floating) better performance than the bulk SONOS flash memory. The operation voltage can reduce 1 V at program model. Nevertheless, the date retention is similar. We

demonstrated the charge-pumping current is depend on interface traps and bulk traps for different programming methods affect the SONOS-type memory border traps. The different programming method shows different charge-pumping curves. Under CHE-programmed operation, two humps appeared in I_{cp} curve due to two different V_{th} at drain-side and source-side. We concluded that CeO_2 nanocrystals can behave as an excellent local charge trapping centers.

6.2 Further Recommendations

There are some interesting topics that are suggested for future work:

(1) About CeO_2 nanocrystal size, we can try to reduce the nanocrystal size and increase the nanocrystal density for next technology node.

(2) We can use CeO_2 or stack high-k materials as tunnel layer to obtain high speed operation in memory device.

(3) Cerium dioxide lattice is nearly matched to silicon (a=0.5411 nm) and sufficiently high dielectric constant (~26) for led to the high thermal stability on CMOS fabrication.

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Publication Lists

1. International Journal:

[1] **Shao-Ming Yang**, Chao-Hsin Chien, Jiun-Jia Huang, and Tan-Fu Lei, "Nonvolatile flash memory devices using CeO_2 nanocrystal trapping layer for two-bit per cell applications," *Japanece Journal of Applied Physics*, vol. 46, no. 6A, pp.3291–3295, June 2007.

2. International Letter:

[1] **Shao-Ming Yang**, Chao-Hsin Chien, Jiun-Jia Huang, Ming-Jinn Tsai, Lurng-Shehng Lee and Tan-Fu Lei, " Cerium oxide nanocrystals for nonvolatile memory applications," in *Applied Physics Letters,*vol. 91, no.262104, December 2007 .

3. International Conference:

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[2] **Shao-Ming Yang**, Chao-Hsin Chien, Jiun-Jia Huang , Yu-Hsien Lin and Tan-Fu Lei," Nonvolatile flash memory devices using CeO_2 nanocrystal trapping layer for two-bit/cell applications," *2006 International Workshop on Dielectric Thin Films for ULSI: Science and Technology (IWDTF2006)*, pp. 137–138.

[3] **Shao-Ming Yang**, Chao-Hsin Chien and Tan-Fu Lei," Thermal Stability and electrical properties of HfON gate dielectric with HfO_2 using N_2O treatment," *2006 International Workshop on Dielectric Thin Films for ULSI: Science and Technology (IWDTF2006)*, pp. 105–106.

[4] **Shao-Ming Yang**, Chao-Hsin Chien, Jiun-Jia Huang, Ming-Jinn Tsai, Lurng-Shehng Lee and Tan-Fu Lei, " High charge storage characteristics of CeO_2 nanocrystals for nonvoliate memory applications," accepted to 2008VLSI-TSA.

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論文題目:

氧化鈰奈米微晶粒非揮發性記憶體元件之研究

Characteristics of Cerium Oxide Nanocrystal Nonvolatile Memory Device