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電子工程學系 電子研究所

博 士 論 文

應用新穎微影及奈米微晶粒技術於奈米元件與記憶體之研究

Application of novel lithography and nano-crystal technique in the fabrication of nano-devices and memories

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摘　要

首先我們研發出一種新的製程技術包括:電子束寫入、化學微縮以及二氧化矽蝕刻用來製作低於 60 奈米的接觸孔洞。接著使用CHF_3/CF_4混合的氣體蝕刻二氧化矽以形成奈米尺度大小的接觸孔洞。在蝕刻過程中，化學微縮阻劑在電漿蝕刻時側壁會形成高分子聚合物使得奈米孔洞縮小。孔洞的周長面積比例反應出經過蝕刻後孔洞尺寸的縮小情形，尤其對於小尺寸的接觸孔洞。蝕刻時在側壁形成的高分子聚合物可有效的縮小奈米孔洞尺寸。

再者將碳六十和碳七十加入電子束阻劑，稱為電子束阻劑修飾法，藉由加入少量的碳六十和碳七十，即可得到高解析度、小線寬以及高抗蝕刻能力之阻劑。使用阻劑修飾法可定義出低於 50 奈米的接觸孔洞及線、亦可應用在定義自我對準金屬矽化物的複晶矽以得到較低奈米線的片電阻值。本方法亦可增加阻劑對二氧化矽及複晶矽的選擇蝕刻比。

接著，我們使用鎳金屬自我對準矽化物和氨電漿處理來製作 50 奈米閘極長度的奈米鰭型元件。我們發現元件特性使用深層鎳金屬自我對準矽化物製程與沒有使用鎳金矽化物製程比較可以得到有效的改善，包括：次臨界擺動、汲極引發位能障降低、提升元件電流導通關閉比，。深層鎳金屬自我對準矽化物元件可以有效的抑制浮接基體效應和寄生 BJT 效應。

再來，我們發展一個非常簡單製備二氧化鋯薄膜的方法，包含：在冰浴中製備$ZrCl_4$前驅物、溶膠-凝膠法沉積、烘烤以及退火等步驟。我們可使用前驅物的濃度控制薄膜厚度。關於薄膜的電性方面，如：有大的崩潰電場、低的閘極漏電流密度顯示出經過了 900 度的快速熱退火後，具有絕佳的絕緣體特性。使用溶膠-凝膠法製備的二氧化鋯薄膜可應用在電容的絕緣材料上。

最後我們使用簡單的溶膠法以及 900 度的快速熱退火來製備三種 SONOS 型記憶體元件, 其一為以二氧化鉿薄膜作為 SONOS 型記憶體元件的陷捕電荷層, 其二為以氧化鉿奈米微晶粒作為 SONOS 型記憶體元件的陷捕電荷層, 其三為以氧化鋯和氧化鉿奈米微晶粒共存作為 SONOS 型記憶體元件的陷捕電荷層。這是溶膠法第一次使用在奈米微晶粒的記憶體元件製備上。SONOS 型記憶體元件以氧化鋯和氧化鉿奈米微晶粒共存作為陷捕電荷層有較大的臨限電壓漂移和較快的寫入、清除。此外這三種 SONOS 型記憶體元件電性方面都有不錯的特性表現，如: 長時間的資料持久性，以及好的寫入、清除操作造成的性能退化少特性。

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ABSTRACT

First, we have developed a fabrication technique, comprising electron-beam writing, chemical shrinking, and silicon dioxide etching, for the fabrication of sub-60-nm contact holes. We carefully evaluated the critical process parameters, such as mixing-bake temperature, mixing-bake time, plasma etch selectivity, and the profile shapes. A fluorinated mixture of gases (CHF_3/CF_4 = 1:1) was used to etch the nano-scale contact holes in the silicon dioxide layer. The formation of side-wall polymers during the plasma etch phase contributed further to the contact hole shrinkage in addition to resist chemical shrinkage.

Second, the fullerene molecules (i.e., C60 and C70) were incorporated in the electron beam resist to investigate the lithographic and etching performances of the resist. The sensitivity, process window and contrast of the modified resist were found to be improved. And the electron beam dose affected the designed holes dimension, and the adulterated resist could print sub-50 nm holes pattern. We found the small amount (0.01-0.02% w/v) of fullerene molecules very effectively promoted the etch resistance and selectivity.

Next, we have fabricated 50nm gate length nano-SOI FinFETs with deep Ni-salicidation and NH_3 plasma treatment. We found that device performances, including subthreshold slope (S.S.), drain-induced barrier lowering (DIBL) and off-state leakage current, can be greatly improved by using deep Ni-salicidation process compared to no Ni-salicidation process.

Next, we have developed a very simple method for the preparation of ZrO_2 ultrathin films; it involves a sequence of $ZrCl_4$ precursor preparation in an ice bath, sol–gel spin-coating processing, baking, and annealing. These ZrO_2 thin films are expected to behave as capacitors and as coatings for insulating films.

Finally, we fabricate a very simple and cheap sol-gel spin coating method, together with RTA, to fabricate three different SONOS-type memories, such as HfO_2 charge trapping layer memory, hafnium silicate nanocrystal memory, and coexisted hafnium silicate and zirconium silicate nanocrystal memory. The coexisted nanocrystal hafnium silicate and zirconium silicate nanocrystal memory exhibits larger Vth shift and faster program/erase speed than hafnium silicate nanocrystal memory and HfO_2 charge trapping layer memory. Furthermore, all devices possess the long charge retention time and good endurance performance for program/erase cycles up to 10^5 without memory window narrowing.

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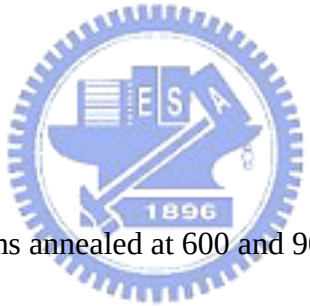

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Chapter 1

Introduction

1.1 Background

The progress of research into integrated circuits (ICs) is focused mainly on two goals: (1) increasing circuit performance (mainly by increasing circuit speed) and (2) increasing the functional complexity of the circuits. Scaling down device sizes is considered a very effective means of achieving these goals, but discovering technologies for achieving sub-60-nm contact holes is still a challenge [1]-[2].

The ITRS 2002 Update predicts that, for ASIC fabrication, the critical dimensions (CDs) for contact holes after etching will be required to be 65 and 45 nm by 2007 and 2010, respectively. Technologies that use chemical shrinkage for patterning sub-100-nm contact holes in resists have been reported previously [3]. In that report, the authors proposed using a polymeric shrinking agent that cross-links on the pattern's sidewalls at a suitable mixing-bake temperature, but such a shrinkage technique faces the problem of defect formation in the resist pattern at higher mixing-baking temperature. Therefore, such chemical shrinkage technology has not been used previously for the generation of sub-60-nm features. Solving this problem, and to achieve the goal of preparing sub-60-nm contact holes in a silicon dioxide layer, requires controlling the shrinkage temperature for the ca. 90-nm contact holes in the resist and improving the etch process that allows further shrinkage to occur.

During the past two decades, there has been an extremely rapid growth in both the technology and the application of microelectronics, to the point that it now pervades virtually all aspects of commercial and military business. The size and performance of microelectronic devices has been improved substantially, especially in the past few years [4]-[5]. In the updated International Technology Roadmap for

Semiconductors, the 50 nm contact hole in the resist will be used in year 2011. The electron beam direct writing (EBDW), in comparison with optical lithography, is a promising means for controlling and patterning small features, down to sub-100nm [6]. This technology has a cost advantage for production volumes below 100 lots in the future [6]. In EBDW, the Gaussian beam has better resolution than shaped beam. But, the shaped beam has an at least 10-fold higher throughput than Gaussian beam due to imposing several pixels per shot [7]. In order to achieve the better resolution and high throughput for shaped beam technology, the utilization of thin resist film is inevitable [8]. However, the thin resist will face the challenge of poor etching resistance and serious line edge roughness. Nano-scale molecules are the possible means to solve the unaffordable etching resistance and enhance the lithographic performance for the thin resist film generation.

In the last few years, the industries focus on the planar CMOS scaling. However, scaling planar CMOS to short gate length will face many problems like electrostatics, excessive leakages, and mobility degradation. Non-planar CMOS MOSFETs provide potential advantages in packaging density, carrier transport, and device scalability [9]. SOI FinFETs technology has a lot of advantages such as the reduction of parasitic capacitances, the feasibility of diffusion resistors and capacitors free of junction effects, better device isolation leading to absence of latch up, substrate coupling and good gate control ability. But the floating body effect is a main problem of the SOI MOSFET devices. It will cause drain current “kink”, abnormal subthreshold slope, and low breakdown voltage [10]-[11]. The metal salicidation method has been used to suppress the floating body effect and DIBL [12]-[13] and reduce parasitic S/D resistances in the thin-film SOI devices.

Silicon technology has formed the basis of microelectronics and electronics systems for more than 30 years. In terms of productivity, the density of devices on a

silicon chip has followed Moore's law, doubling about every two or three years since about 1980. Many researchers are interested in scaling down electronics devices so that they may perform at higher speeds and be prepared at lower costs. Conventional SiO_2 gate dielectrics are reaching their physical thickness limit (1.5 nm); they cannot be used as CMOS devices because the high direct tunneling current and poor reliability. For further scaling of devices, it has been proposed that SiO_2 be replaced by high-k dielectric constant materials, such as ZrO_2, HfO_2, Ta_2O_5, Al_2O_3, TiO_2, and silicates ($ZrSi_xO_y$ and $HfSi_xO_y$) [14]–[21]. In fact, dielectric films having higher permittivity allow the use of thicker films of equivalent electrical thickness as silicon dioxide; this situation will reduce the leakage current and improve the reliability of the dielectric films.

The most important properties of high-k dielectric materials that are necessary to maintain continuous increases in device performance and density are their low leakage current, low equivalent oxide thickness (EOT), high breakdown strength, high thermal stability, and gate electrode compatibility. The EOT, t_{eq}, of an alternative high-k dielectric employ can be obtained from the simple equation

$$t_{eq} = (K_{ox} / K_{high\text{-}k})\, t_{high\text{-}k}.$$

Where K_{ox} and $K_{high\text{-}k}$ are the dielectric constants of silicon oxide and the high-k dielectric, respectively, and $t_{high\text{-}k}$ is the physical thickness of the high-k material. Future downscaling will require high-k materials in which EOT values are reduced to nearly 0.7 nm [22]. We must bear in mind that many of the characteristics of these high-k dielectrics—such as their breakdown mechanism and hysteresis phenomena—are quite different from those of conventional silicon dioxide. When the gate dielectric materials experience high-temperature conditions (> 800 °C), the thermal stability of the high-k dielectric on silicon is an important issue that must be addressed for future MOSFET devices. The most suitable range of dielectric constants

is between 20 and 40. If the material has an extremely high k-value (> 80), it will induce a large fringing effect. For the purposes of achieving a low leakage current, it is desirable to choose a dielectric material that possesses a large band gap energy and a large band offset with respect to the Si substrate. ZrO_2 has a dielectric constant of 25, a wide band gap, good thermal stability, a high hardness, a high melting point, chemical hardness, and a high refractive index.

Recently, numerous technologies have been developed for the preparation of various high-k films [23]-[25]. To prepare insulating thin films, atomic layer deposition (ALD), physical vapor deposition (PVD), and chemical vapor deposition (CVD) methods have all been used to prepare films for new technologies. In the ALD process, $ZrCl_4$ and H_2O are used to prepare the ZrO_2 films. For the PVD process, a zirconium metal target is used for sputtering under ambient oxygen to deposit the ZrO_2 films. In the CVD method, $ZrCl_4$ precursor is used to deposit ZrO_2 films. The sol–gel method is a very interesting simple technique for preparing ceramic films [27]-[31].

1.2 Motivation

In this thesis, we investigate chemical shrinkage process parameters that are used in conjunction with electron beam lithography for preparing contact holes during ASIC fabrication. We have evaluated the various bake processes and process stabilities, and we discuss the cross-sectional images of holes formed by the chemical shrinkage process at various mixing temperatures. Upon completing the chemical shrinkage procedure, we also evaluated a series of dry etch recipes for the silicon dioxide layer.

In order to achieve the better resolution and high throughput for shaped beam

technology, the utilization of thin resist film is inevitable. However, the thin resist will face the challenge of poor etching resistance and serious line edge roughness. Nano-scale molecules are the possible means to solve the unaffordable etching resistance and enhance the lithographic performance for the thin resist film generation. The molecules can be incorporated into the resist to alter its performance. The use of fullerene molecules possesses the advantage of extremely small and monodisperse. In our study, the sensitivity curve of resists after spiking with C60 and C70 molecules are investigated. The film stress, etch resistance and the effect of shaped electron beam dose on the contact hole sizes are carefully studied. In addition, the titanium nitride gap-filling and step coverage on contact holes by 0.02% w/v C70-incorporated resists are also evaluated.

Plasma treatment has long been used in TFT devices. The suitable plasma treatment can improve the electrical characteristics of the TFT devices because it can repair the defects in the devices. However, plasma treatment has not been proposed in the nano-SOI FinFETs fabrication. In this paper, we propose the 50nm gate length nano-SOI FinFETs with deep Ni-salicidation and NH_3 plasma treatment. This is the first time to apply NH_3 plasma treatment on thin-film SOI devices. The NH_3 plasma treatment is expected to repair the process-induced defects in thin-film SOI devices.

The sol–gel method can provide colloidal solvents or precursor compounds when metal halides are hydrolyzed under controlled conditions. In the sol–gel process, hydrolysis, condensation, and polymerization steps occur to form metal oxide networks. These reactions play fateful roles in modifying the final material's properties. The most interesting feature of sol–gel processing is its ability to synthesize new types of materials that are known as "inorganic–organic hybrids." The film formation with spin-coating is a simple method than ALD, PVD or CVD due to its cheaper precursor and tool. In addition, the film can be fabricated in the normal

pressure system instead of high vacuum system. Typically, ZrO_2 is an excellent heat-resistant and chemically durable material that is used, for example, as a material for furnaces [19]. Although ZrO_2 generally provides good electrical insulation, no reports exist that describe the electrical insulation properties of sol–gel-derived ZrO_2 ultrathin film. In this thesis, we used the different annealing conditions on the sol–gel ZrO_2 ultrathin films on silicon. The resulting material properties and electrical performance of these deposited films were also evaluated by various characterization techniques.

In this paper, we use the sol-gel spin coating method to fabricate three SONOS-type flash memory devices. One is used HfO_2 as charge trapping layer, and one of the other two is hafnium silicate nanocrystal memory. We use sol-gel method to combine three high-k precursors, i.e. $HfCl_4$, $ZrCl_4$ and $SiCl_4$ together to form hafnium silicate and zirconium silicate co-existed in a memory device for the first time.

1.3 Thesis Organization

We will developed a fabrication technique, comprising electron-beam writing, chemical shrinking, and silicon dioxide etching, for the fabrication of sub-60-nm contact holes in chapter 2. Then, in the chapter 3, we will incorporate the fullerene molecules in the commercial electron beam resist to investigate the performances for patterning and filling the contact holes at nanometer scale. In the chapter 4, we will fabricate 50nm gate length nano-SOI FinFETs with deep Ni-salicidation and NH_3 plasma treatment. Next in chapter 5, we will developed a simple method, including a sequence of $ZrCl_4$ precursor preparation under ice bath, sol-gel spin-coating processing, baking and annealing was developed for the preparation of

ZrO_2 ultrathin films. Finally in chapter 6, we fabricate a very simple and cheap sol-gel spin coating method, together with RTA, to fabricate three different SONOS-type memories, such as HfO_2 charge trapping layer memory, hafnium silicate nanocrystal memory, and coexisted hafnium silicate and zirconium silicate nanocrystal memory.

Chapter 2

Fabrication of Sub-60-nm Contact Holes in Silicon Dioxide Layers

2.1 Introduction

The progress of research into integrated circuits (ICs) is focused mainly on two goals: (1) increasing circuit performance (mainly by increasing circuit speed) and (2) increasing the functional complexity of the circuits. Scaling down device sizes is considered a very effective means of achieving these goals, but discovering technologies for achieving sub-60-nm contact holes is still a challenge [1,2].

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In this paper, we investigate chemical shrinkage process parameters that are used in conjunction with electron beam lithography for preparing contact holes during

ASIC fabrication. We have evaluated the various bake processes and process stabilities, and we discuss the cross-sectional images of holes formed by the chemical shrinkage process at various mixing temperatures. Upon completing the chemical shrinkage procedure, we also evaluated a series of dry etch recipes for the silicon dioxide layer.

2.2 Experimental

Table 2.1 lists the experimental flows and parameters used for preparing the sub-60-nm contact holes in the silicon dioxide layer. Electron beam exposure was performed on a Leica Weprint 200 stepper. The silicon dioxide layer was grown by wet oxidation using a mixture of hydrogen (8000 cm^3/min) and oxygen (4999 cm^3/min) gases at 978 °C in a low-pressure furnace. The electron beam energy was 40 keV, the beam size was 20 nm, and the exposure dose was 14 $\mu C/cm^2$. The developer for the JSR positive electron beam resist (MES-1EG) was an aqueous 2.38% tetramethylammonium hydroxide (TMAH) solution. A positive-tone electron beam resist was spin-coated on a silicon wafer (150 mm diameter) and baked at 110 °C for 120 sec. The thickness of the resist film was ca. 650 nm. After exposure and a post-exposure bake (110 °C for 120 sec), the wafer was developed using the TMAH solution. Again, a hard-bake was applied to the wafer (110 °C for 120 sec). A chemical shrinkage procedure was then applied. The chemical shrinking agent (AZ R-200, Clariant) was coated over the resist pattern, and the wafer was again soft-baked. The film thickness was ca. 400 nm. A mixing-bake step at 110 °C for 70 sec was then undertaken. The chemical shrinking agent reacted with the resist acid that diffused from the resist pattern. A cleaning step, using AZ R-2, which can wash away unreacted materials, was applied to the process. A hard-bake step was

performed at 110 °C for 2 min. Finally, we applied a plasma process using a mixture of CHF_3 and CF_4 gases to etch the underlying silicon dioxide layer. Critical dimensions were evaluated using either an in-line scanning electron microscope (SEM, Hitachi S-6280) or a cross-sectional SEM (Hitachi S-4000).

2.3. Results and Disussion

2.3.1 Chemical shrinkage processes for the electron-beam resist

As has been reported previously [3], the mixing-bake temperature and time are the critical factors for fabricating sub-100-nm contact holes in a resist when using the chemical shrinkage technique. Basically, the residual acid in the resist pattern diffuses into the side-wall regions of the shrinkage agent, which leads to cross-linkage reactions of the shrinkage agent. The extent of hole shrinkage in the positive resist depends upon the intrinsic acid diffusion behavior, such as its diffusion coefficient, and the time. Figure 2.1 illustrates the effect of mixing-bake temperature on the CDs of various contact holes for the positive E-beam resist. Characterization using top-down SEM clearly indicates that the CDs of contact holes at any size gradually narrow as the mixing-bake temperature is increased from 100 to 120 °C. An initial hole size of 140 nm formed by electron-beam patterning is suitable for shrinking down to the sub-100-nm level. We evaluated the profile of the contact holes at various mixing-bake temperatures by using cross-sectional SEM. The SEM pictures in Fig. 2.2 clearly illustrate the profile of the contact holes. Initially (prior to applying the chemical shrinkage agent), the contact holes have vertical sidewalls and a smooth surface. After a 105 °C mixing-bake (subsequent to applying the chemical shrinkage agent), the sidewalls and surface covered with shrinkage agent appear to be slightly

distorted. When the mixing-bake temperature was increased to 110 °C, the contact holes remain open, but we observe an overhang effect in the contact holes formed after heating at either 115 or 120 °C. We attribute this finding to the effect of thermal flow of the shrinkage agent on the resist's sidewalls at higher bake temperatures. This type of defect is not observed when viewing from by SEM from above the surface, but is very apparent from the cross-sectional SEM image. Clearly, the upper limit of the mixing-bake temperature for the chemical shrinkage technique is 110 °C.

Figure 2.3 demonstrates the effect of mixing-bake times on the CDs of various contact holes for the positive resist at 110 °C. We observe that the hole dimensions decrease rapidly during the first 60 sec, but then gradually reach a plateau. Therefore, we believe that the optimal time for the mixing-bake process in this study is 70 sec. The reason for this trend with respect to mixing-bake time is that the process is dependent on the abundance of diffusion acid in the resist pattern, which is limited. If the amount of acid in the resist is increased, the CD will become narrower. The initial 140-nm hole formed by electron-beam patterning is the only one of the holes that we have studied that is suitable for being shrunk down to a sub-100-nm hole. Next, we compare the effects of the soft-bake, mixing-bake, and hard-bake processes after applying the chemical shrinkage agent. The control conditions for soft-baking, mixing-baking, and hard-baking are 85 °C for 70 sec, 110 °C for 70 sec, and 110 °C for 2 min, respectively. Figure 2.4 clearly indicates that the hard-bake temperature has no significant effect on the hole shrinkage ratio. The soft-bake temperature does have a significant effect above 110 °C, which we ascribe to the thermal flow effect discussed earlier. Among these baking processes, the mixing-bake temperature exhibits the most significant effect on the hole shrinkage ratio.

The hole shrinkage mechanism is closely dependent on the abundance of residual acid in the resist pattern. We exposed the wafer in the cleanroom environment (class

10) after initial contact hole definition for various delay hours. Figure 2.5 indicates that the shrinkage ratio fluctuates between 33 and 34% after various delay times. Although not illustrated here, the SEM images for these holes taken from above are very similar. It has been reported in the literature that a chemically amplified resist is sensitive to the molecular base, and leads to T-top and footing problems for the positive resist when not immediately developed (post-exposure delay)[4]. The molecular base in the cleanroom might have reacted to some extent with the surface acid. Most acids under the resist film, however, are not influenced by the molecular base from the air in the cleanroom. Therefore, the diffusion of the acids out of the resist still occurs during the mixing-bake process and the delay time has no effect.

2.3.2 Fabrication of 53-nm contact holes

The fabrication of sub-60-nm contact holes in a silicon dioxide layer by the chemical shrinkage technique has not been reported previously. To ensure the applicability to nano-fabrication techniques, the resist should tolerate the etching process. Figure 2.6 depicts the etch selectivity that we estimate from the ratio of the plasma etch rates of silicon dioxide and the positive resist under various mixtures of gases. The selectivity gradually increases upon increasing the ratio of CHF_3 from 0 to 0.75, and then increases abruptly upon a further increase in the gas ratio to 1. It has been suggested in the literature [5] that oxygen byproducts formed during silicon dioxide etching can react with carbon residues, especially at fluorine/carbon ratio < 2. Hence, the polymer formation blocks any further etching process.

The positive resist (650 nm thick) was coated onto a wafer upon which a silicon dioxide film had been grown. A variably shaped electron beam was used to pattern a 140-nm hole in the positive resist (Fig. 2.7a). The chemical shrinkage process was

then undertaken by spin-coating the shrinkage agent onto the resist pattern, followed by a soft-bake at 85 °C for 70 sec. The wafer was then subjected to a mixing-bake at 110 °C for 70 sec. The residual acid diffuses out from the resist pattern into the shrinkage agent, which leads to acid-induced cross-linkage reactions taking place. After washing off the unreacted shrinkage agent and baking again at 110 °C for 2 min, the contact hole in the resist layer now has a 93-nm diameter (Fig. 2.7b). At the stage, the shrinkage ratio is ca. 33.6%. After the resist pattern had shrunk, the wafer was sent for plasma etching to fabricate a contact hole. Interestingly, the dimension of the contact hole in the silicon dioxide is not 93 nm: Figure 2.8 indicates that the hole size is 53 nm. The total shrinkage ratio of the hole diameter after the chemical shrinkage and plasma etch processes is 62.1%. What happens to the contact holes in the silicon dioxide layer during the plasma etch process? The sidewall deposition of residual polymers during the plasma etch process plays a significant role in narrowing the contact hole dimensions.

The etch mechanism for contact hole fabrication in a silicon dioxide layer is very complicated, with the dimensions of the pattern formed during the etch process being controlled by a balance between the amount of polymer deposited and the etch conditions. Explanations have been proposed in the literature [6-9] regarding micro-loading and aspect ratio-dependent etching (ARDE) to explain the observations made during etch processes. Micro-loading describes the variations of the etch rate between areas having different pattern densities, with features in low-pattern-density areas etching faster than features in high-pattern-density areas. Effects that are due to the pattern dimensions, which includes effects related to transport of etchant species into the pattern, or transport of etch products out of the pattern, are generally referred to as ARDE. Table II lists a series of data for the contact holes obtained after the chemical shrinkage and dry etch processes. The smaller holes exhibit a higher

shrinkage percentage for the etch process than the larger holes. We attribute this observation to the pattern dimension effect. As the pattern size is reduced, the probability for the flux of incoming polymer species to interact with the sidewall of the contact hole increases. Figure 2.9 depicts the relationship between the ratio of the hole dimension before and after etching and the ratio of the hole perimeter to the hole area of these nano-scale contact holes. We find that a linear dependence exists for the series of holes studied. This finding suggests the pattern reduction arising from sidewall polymer deposition during the etch process has an inverse relationship to the pattern diameter. The probability of transportation of a polymer species onto the sidewall of a contact hole is related linearly to the inverse of the contact hole size (after chemical shrinking). As a consequence, the contact hole in the silicon dioxide layer becomes smaller than expected after the etching process. We estimate that the uniformities (1 sigma) of the proposed method for contact hole formation after the processes of lithography, chemical shrinkage, and plasma etching are 3.21, 3.16, and 2.76 nm, respectively.

2.4 Summary

We have established a successful fabrication technique for preparing sub-60-nm contact holes in a silicon dioxide layer by electron-beam lithography. We have discussed in detail the many factors that influence the performance of the shrinkage process, such as the mixing-bake temperature, mixing-bake time, and hole dimensions before and after chemical shrinkage. Using this chemical shrinkage technique (mixing-bake of 110 °C for 70 sec) and an etch gas of CHF_3/CF_4 (1:1), we obtained a minimum hole dimension of 53 nm. This technology meets the requirements[2] for contact hole fabrication in the year 2009. We propose that a nano-hole effect occurs

during the etch-assisted shrinkage reaction because smaller holes have a higher percentage of polymer deposition in the resist sidewall than do larger holes.

Table 2.1 Process conditions for the fabrication of sub-60-nm contact holes in a silicon dioxide layer.

Oxidation Processes	
Oxidation temperature	978 °C,
SiO_2 thickness	150 nm
Gas components	H_2 (8000 cm^3/min)/O_2 (4999 cm^3/min)
Lithography Processes	
Spin speed	**2500–5000 rpm, 30 sec**
Resist thickness	**650 nm**
Exposure dose	14 μC/cm^2
soft-bake	110 °C, 120 sec
Post-exposure bake	110 °C, 120 sec
Development	**TMAH, 60 sec**
Hard-bake	110 °C, 120 sec
Chemical Shrink Processes	
Soft-bake	85 °C, 70 sec
Mixing-bake	110 °C, 70 sec
AZ remover (R-2)	10% IPA and 90% H_2O, two puddles 40s/20s
Hard-bake	110 °C, 120 sec
Etch and Resist Stripping Processes	
Etch time	**60 sec**
Gas components	CF_4, 20 sccm/CHF_3, 20 sccm
Chemicals	H_2SO_4/H_2O_2 = 3:1, 120 °C, 10 min

Table 2.2 The diameters of contact holes formed after the processes of chemical shrinkage and plasma etching in SiO_2, and their ratios (R = hole radius).

Hole diameter after chemical shrinkage (x)	Hole diameter after dry etching in SiO_2 (y)	y/x (percentage)	Perimeter/area ($2\pi R/\pi R^2$)
246 nm	233 nm	94.7%	0.0163
149 nm	128 nm	85.9%	0.0268
133 nm	98 nm	73.6%	0.0301
119 nm	79 nm	66.6%	0.0336
93 nm	53 nm	53.3%	0.0430

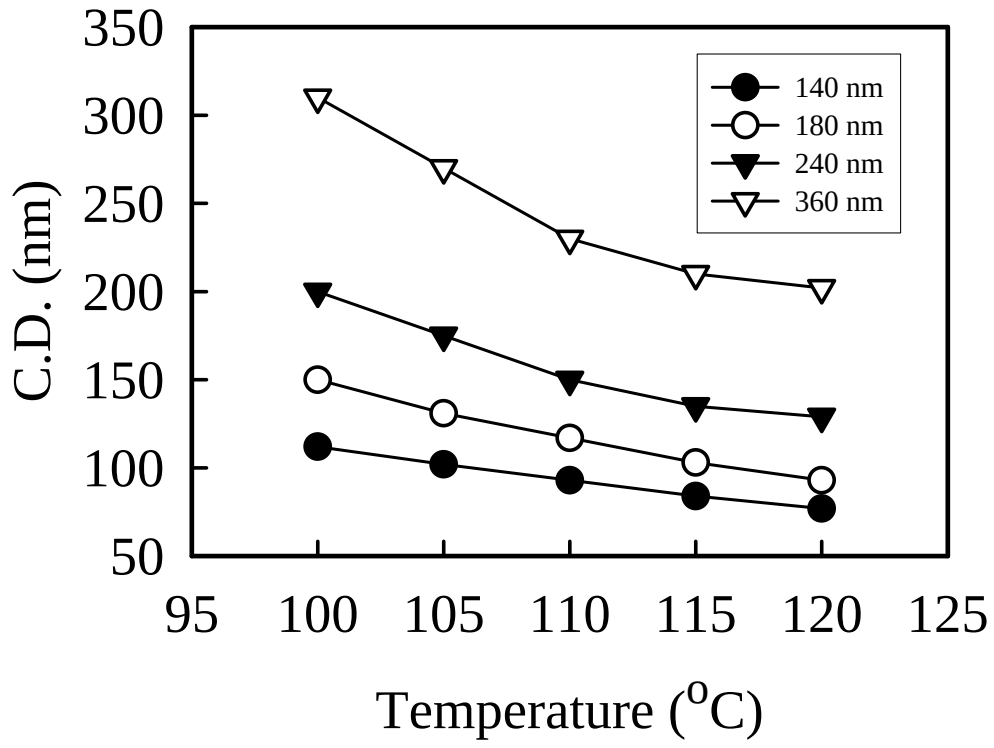


Figure 2.1 Dependence of various mixing-bake temperatures for 70 sec on the critical dimensions (CDs) of contact holes formed by the chemical shrinkage technique. The initial hole sizes were 140, 180, 240, and 360 nm, respectively; top-down SEM was used to measure CD.

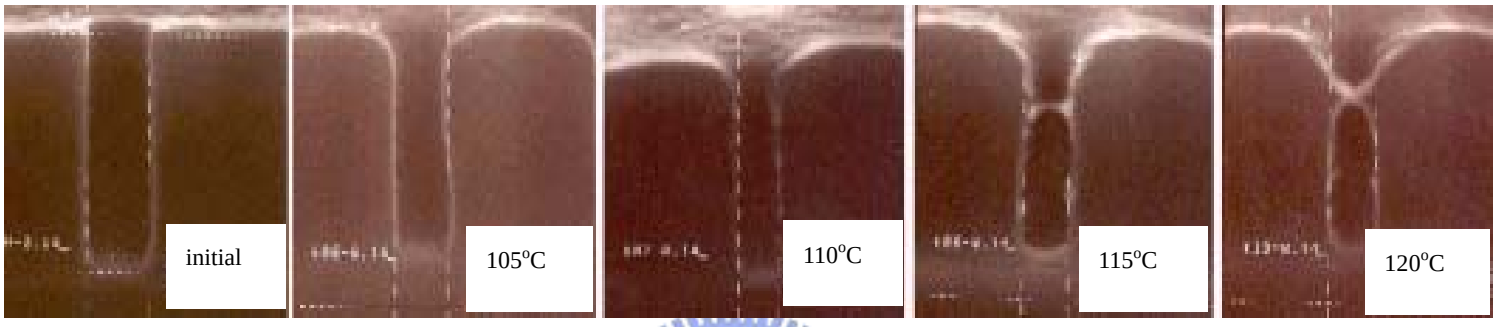


Figure 2.2 Cross-sectional SEM image of contact holes in the resist after various mixing-bake temperatures.

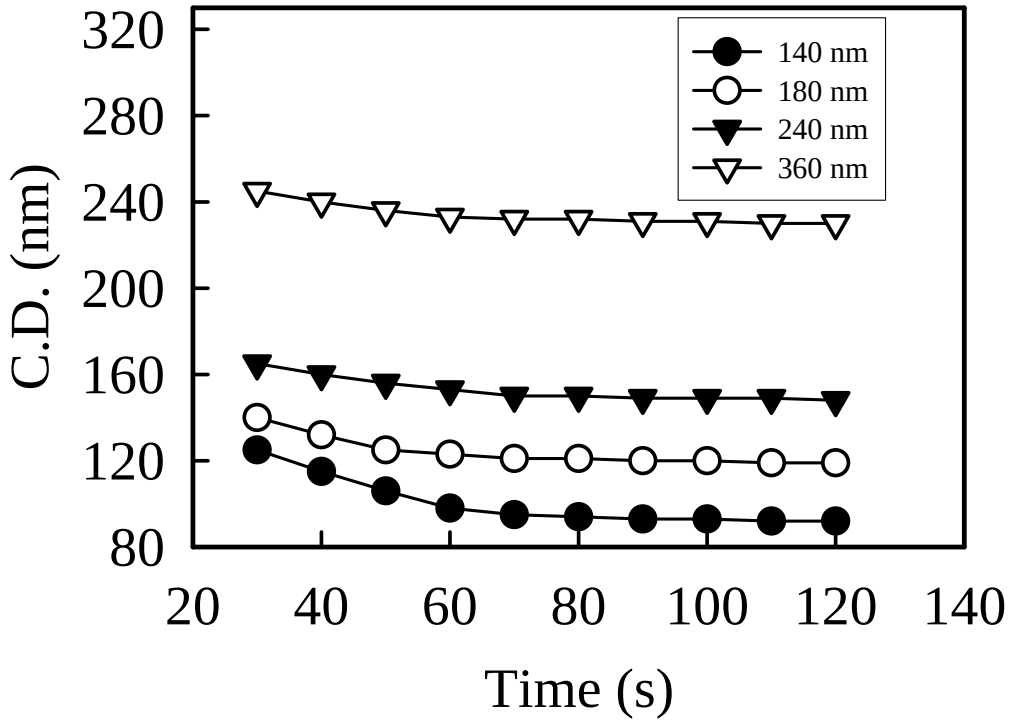


Figure 2.3 Dependence of various mixing-bake times on the CDs of contact holes formed by the chemical shrinkage technique. The initial hole sizes were 140, 180, 240, and 360 nm, respectively; top-down SEM was used to measure CD.

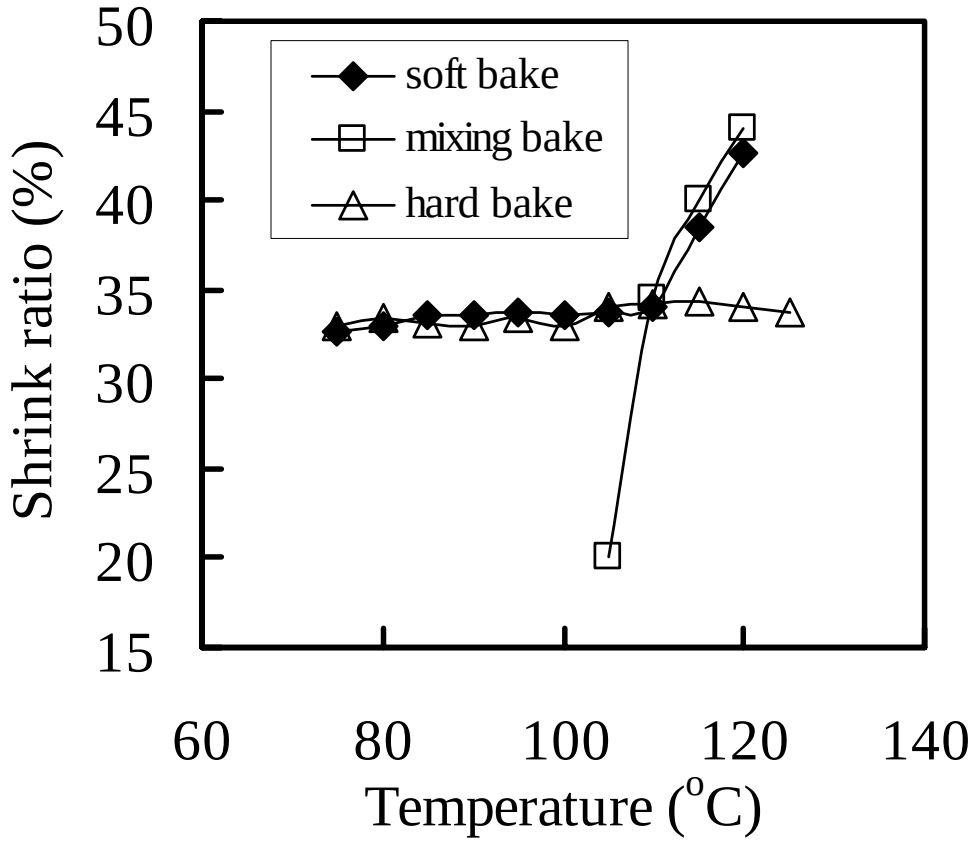


Figure 2.4 The effects of the various bake processes and temperatures on the shrinkage ratios of the contact holes.

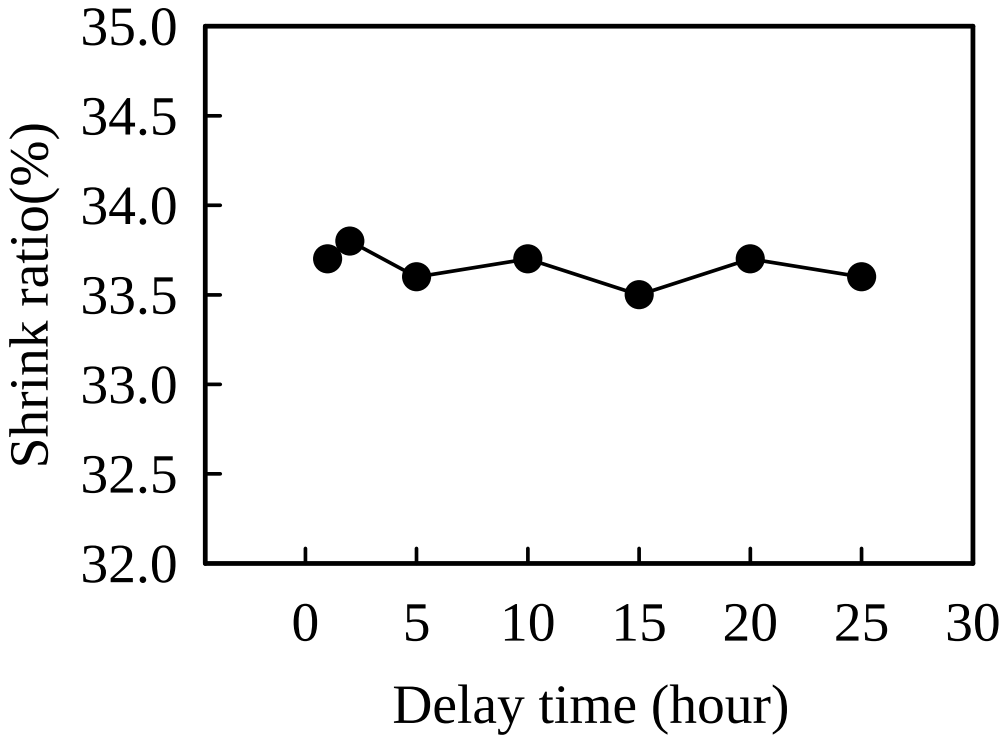


Figure 2.5 The effect of delay time on the shrinkage ratio (delay time = the period of time between the formation of the initial hole in the resist and the application of the shrinkage agent).

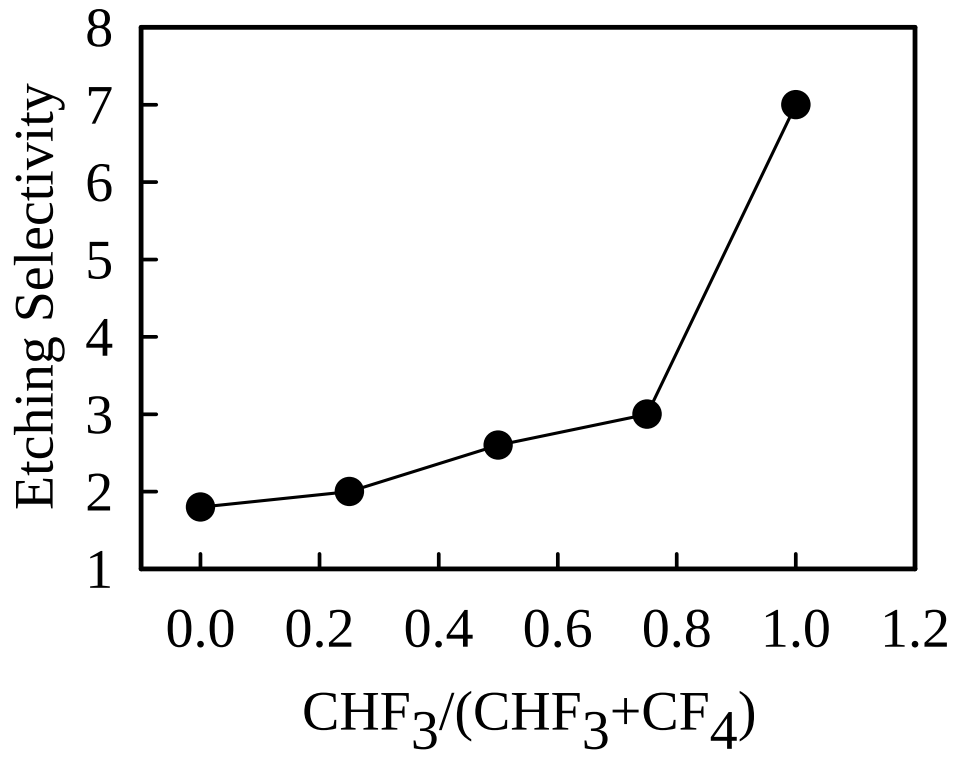


Figure 2.6 The dry etch selectivity of SiO_2 to resist at different CHF_3 ratios.

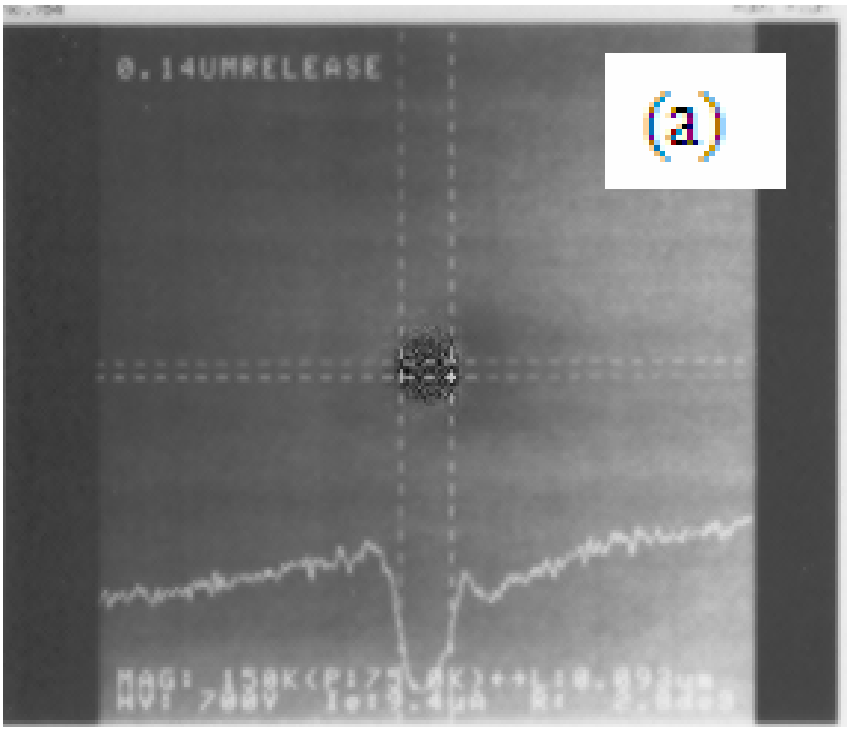


Figure 2.7 (a) The 140-nm contact hole in the resist.

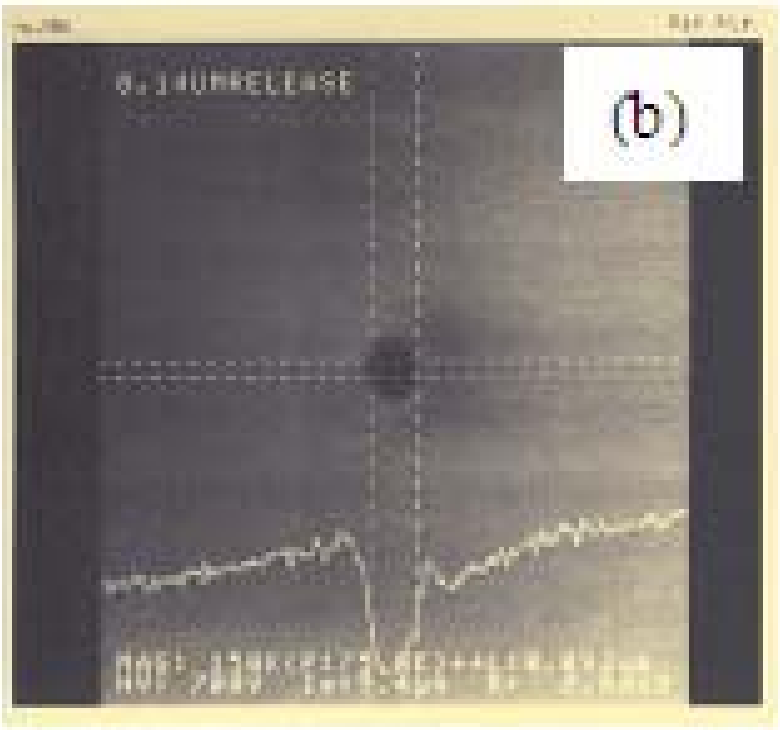


Figure 2.7 (b) The 93-nm contact hole formed in the resist after chemical shrinkage.

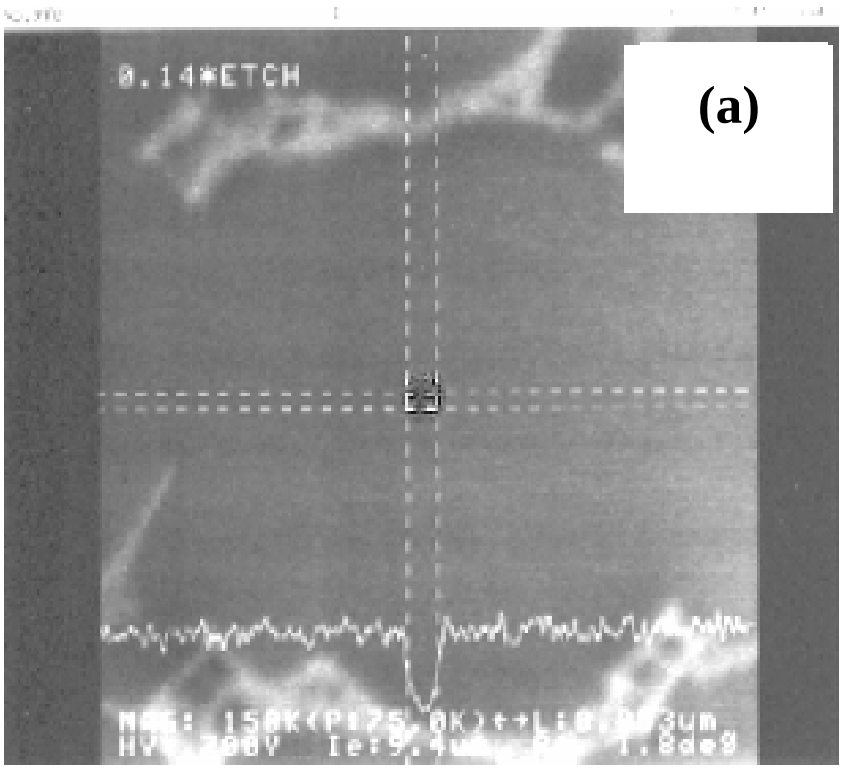


Figure 2.8 (a) 53nm contact hole in SiO_2 layer without resist stripping (image from top-down SEM).

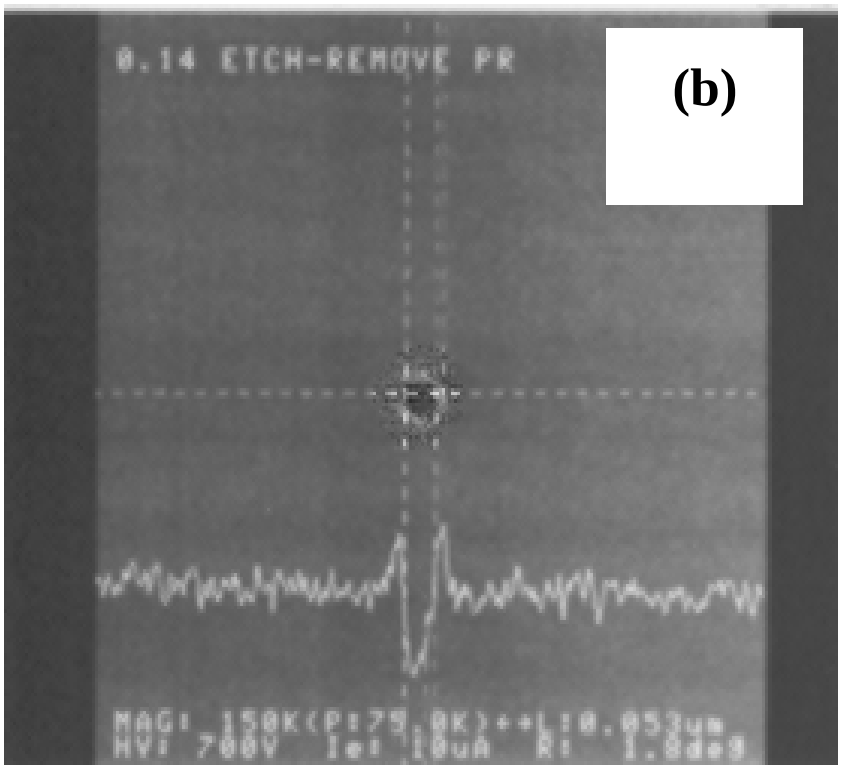


Figure 2.8 (b) 53nm contact hole in SiO_2 layer after resist stripping (image from top-down SEM).

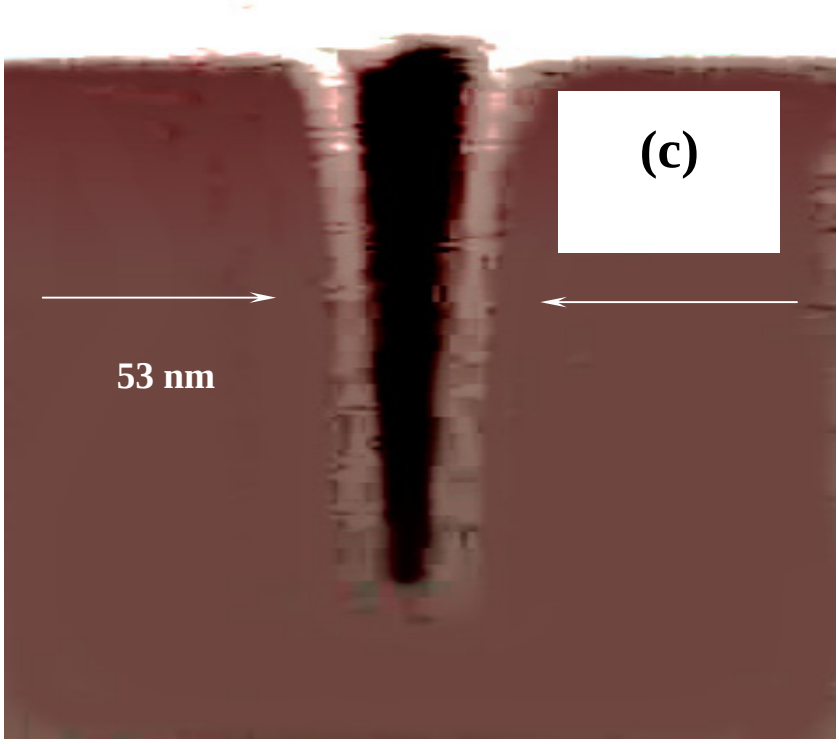


Figure 2.8 (c) 53nm contact hole in SiO_2 layer after resist stripping (image from cross-sectional SEM).

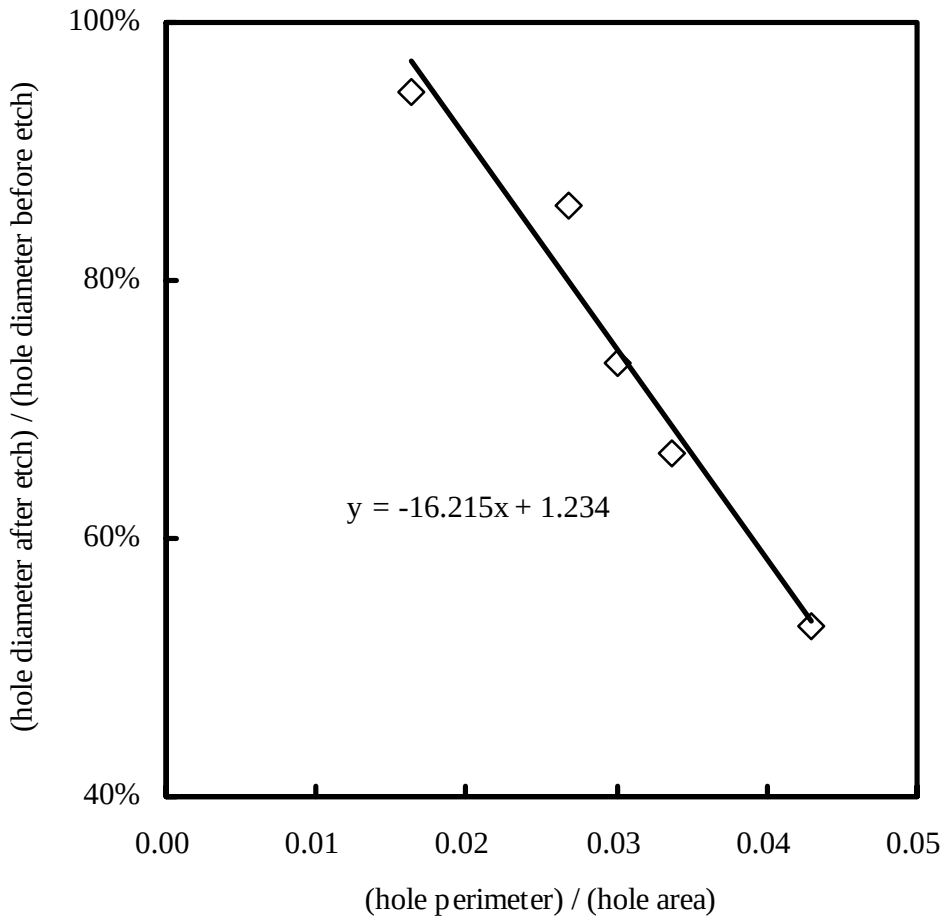


Figure 2.9 Linear dependence between the ratio of the hole dimension after and before etching and the ratio of the hole perimeter to hole area during the etching of the nano-scale contact holes.

Chapter 3

Resist Nano-modification Technology for Enhancing the Lithography and Etching Performance for Nano Contact Hole and Line

3.1 Introduction

During the past two decades, there has been an extremely rapid growth in both the technology and the application of microelectronics, to the point that it now pervades virtually all aspects of commercial and military business. The size and performance of microelectronic devices has been improved substantially, especially in the past few years [1,2]. In the updated International Technology Roadmap for Semiconductors, the 50 nm contact hole in the resist will be used in year 2011. The electron beam direct writing (EBDW), in comparison with optical lithography, is a promising means for controlling and patterning small features, down to sub-100nm [3]. This technology has a cost advantage for production volumes below 100 lots in the future [3]. In EBDW, the Gaussian beam has better resolution than shaped beam. But, the shaped beam has an at least 10-fold higher throughput than Gaussian beam due to imposing several pixels per shot [4]. In order to achieve the better resolution and high throughput for shaped beam technology, the utilization of thin resist film is inevitable [5]. However, the thin resist will face the challenge of poor etching resistance and serious line edge roughness.

Nano-scale molecules are the possible means to solve the unaffordable etching

resistance and enhance the lithographic performance for the thin resist film generation. The molecules can be incorporated into the resist to alter its performance. The use of fullerene molecules possesses the advantage of extremely small and monodisperse. Ishii et al. [6] have been used fullerene molecule (i.e., 5 wt% C60) to modify positive tone resist, and found the fullerene can enhance the 6% etching resistance and not alter the sensitivity. In addition, they claim the negative tone chemically amplified resist incorporated with 3 wt% C60 exhibits strong environmental stabilization in postexposure delay. In the latter report [7], they find the resist sensitivity is degraded by the C60 due to the dissolution-inhibiting effect. Dentinger and Taylor [8] spike 7.9 wt% C60 into poly(methylmethacrylate) resist, and the etching resistance is promoted 8% and 26% for CF_4 and Cl_2 plasmas, respectively. However, the use of 3-7.9 wt% C60 in the resists and the deterioration of resist sensitivity elevate the fabrication cost and restrict the further application of this technology.

In this study, the sensitivity curve of resists after spiking with C60 and C70 molecules are investigated. The film stress, etch resistance and the effect of shaped electron beam dose on the contact hole sizes are carefully studied. In addition, the titanium nitride gap-filling and step coverage on contact holes by 0.02% w/v C70-incorporated resists are also evaluated.

3.2 Experimental

The fullerene molecules of C60 and C70 were purchased from Alfa Aesar Company. The toluene solvent was obtained from E. Merck (Darmstadt, Germany). The negative NEB-22 resist used in this study was obtained from SUMITOMO Chemical Co., Ltd. (Japan). The resist samples in this study have four types, named NEB, NEB+Toluene, NEB+C60, and NEB+C70, respectively. The NEB means the

NEB-22 resist without any modification. The “NEB+Toluene” means the mixture of 50mL NEB-22 resist and 50mL toluene solvent. For the “NEB+C60-0.01%” sample, the 0.01g C60 fullerene is first dissolved in 50mL toluene, and then mixes with 50mL NEB-22 resist. The final concentration of C60 molecule in the resist is 0.01% w/v. In the same manner, the “NEB+C70-0.02%” uses 0.02g C70 fullerene to prepare the sample.

And the DSE-1010 positive resist used in this study was obtained from DONGJIN Chemical Co., Ltd. (Korea). There are four types of resist samples in this study, named DSE, DSE + Toluene, DSE + C60, and DSE + C70, respectively. The DSE means the DSE-1010 resist without any modification. The “DSE + Toluene” means the mixture of 50mL DSE-1010 resist and 50mL toluene solvent. For the “DSE + C60-0.01%” sample, the 0.01g C60 fullerene is first dissolved in 50mL toluene, and then mixes with 50mL DSE-1010 resist. The final concentration of C60 molecule in the resist is 0.01% w/v. In the same manner, the “DSE + C70-0.02%” uses 0.02g C70 fullerene to prepare the sample.

Electron beam exposure was performed on a Leica Weprint 200 stepper. The electron beam energy was 40 keV, and the beam size was 20 nm. The developer for the electron beam resist was an aqueous 2.38% tetramethylammonium hydroxide (TMAH) solution. A electron beam resist was spin-coated on a silicon wafer (150 mm diameter) and baked at 95 °C for 120 sec. After exposure and a post-exposure bake (115 °C for 120 sec), the wafer was developed using the TMAH solution for 60 sec. Again, a hard-bake was applied to the wafer (115 °C for 120 sec). Critical dimensions were evaluated using either an in-line scanning electron microscope (SEM, Hitachi S-6280) or a cross-sectional SEM (Hitachi S-4000). The stress of resist film was measured by TENCOR FLX-2320 instrument. In the stress measurement, the curvatures of bare silicon wafers, resist-coated wafers were determined.

Silicon dioxide film was etched using a reactive-ion etcher (RIE, Tokyo Electron Limited, Model TE5000, Japan). There are two steps for silicon dioxide etching. The operating conditions for step 1 are- 0.2 Torr pressure, 0 W RF power, 400 cm^3min^{-1} Ar gas, and etching gases of CHF_3 and CF_4 (CHF_3+CF_4=40 cm^3min^{-1}). The operating conditions for step 2 are- 0.2 Torr pressure, 500 W RF power, 400 cm^3min^{-1} Ar gas, and etching gases of CHF_3 and CF_4 (CHF_3+CF_4=40 cm^3min^{-1}).

The thermal oxide was grown under dry O_2 at 900^oC in quartz reactor to a thickness of 100nm. After coating the fullerene-incorporated resist onto the thermal oxide and resist patterning, the plasma process of mixing CHF_3 and CF_4 gases was used to etch the underlying silicon dioxide layer. Then, the contact holes defined by 0.02% w/v C70-incorporated resist were deposited with the titanium nitride (TiN) plug by physical vapor deposition (PVD) and chemical vapor deposition (CVD). The TiN PVD sputter system (ULVAC SBH-3308 RDE system) was used to deposit 200-nm TiN film, and argon and nitrogen were used as process gases. For the film deposition by CVD method, the tool from Materials Research Corporation (MRC) was used to deposit TiN film by gas mixture of $TiCl_4$ and NH_3 at 630 ^oC. The chemical reaction is as follows: $6TiCl_4 + 8NH_3 \rightarrow 6TiN + 24HCl + N_2$.

The other the polysilicon gates with spacer were fabricated with the 0.01% w/v C60-incorporated resist on 6 inch silicon wafer. First, the gate oxide was grown under dry O_2 at 900^oC in quartz reactor to a thickness of 1.5nm. After a 50nm poly-Si film was deposited by low pressure chemical vapor deposition system (LPCVD) and doped by ion implantation, and then patterned to from a gate. The poly-SiGe is also deposited by LPCVD. A 50nm tetraethyl orthosilicate film was also deposited by LPCVD. The gate spacer was formed by reactive ion etching. Prior to remove native oxide before cobalt deposition, all wafers were dipped in the HF solution. The 5nm cobalt was deposited by physical vapor deposition system (PVD). The first annealing

step for the cobalt silicide ($CoSi_2$) formation was operated at 550 ^oC in N_2 ambient for 30 sec. The un-reacted cobalt was removed by selective wet etching in the mixture of H_2SO_4 and H_2O_2. The second step annealing step was performed at 750 ^oC in N_2 ambient for 30 sec. For the nickel silicide (NiSi) formation, the wafer was deposited 5nm Ni by PVD. The annealing step used only one step for the sample was operated at 500 ^oC in N2 ambient for 30 sec. The un-reacted Ni was also removed by wet etching in the mixture of H_2SO_4 and H_2O_2.

3.3. Results and Discussion

3.3.1. Enhancement of lithographic performance

In the electron beam writing technology, the negative tone resist is usually used to fabricate the line or low density patterns, especially for the gate line. In this study, the commercial NEB-22 resist is a negative type, and the fullerene molecules such as C60 and C70 are incorporated into the commercial resist. Figure3.1(a) depicts the resist sensitivity curve. The dose (D_C) for the "NEB" sample that the polymer constituent begins cross-linkage is 5.2 μC/cm^2, while the dose (D_O) that the polymer can achieve 100% cross-linkage is 6.2 μC/cm^2. As to the "NEB+Toluene" sample, both the D_C and D_O are increased. This observation is attributed to the dilution of acid generator in the sample, and therefore, reduces the sensitivity. Interestingly, the sensitivity for 0.01% w/v "NEB+C60" or "NEB+C70" sample is significantly enhanced after nano-material modification. Both the D_C and D_O are decreased to 4.6μC/cm^2 and 5.4μC/cm^2, respectively. This finding suggests that the incorporation of fullerene molecules into resist can effectively enhance the process throughput.

Another the electron beam writing technology, positive tone resist is usually used to fabricate the contact hole [3]. In this study, the commercial DSE-1010 electron

beam resist is a positive type, and the fullerene molecules such as C60 and C70 are incorporated into the commercial resist. Figure3.1(b) depicts the resist sensitivity curve. The irradiation dose (D_i) for the "DSE" resist that the acid generator and functional group in the polymer begins reaction is 2.3 μC/cm^2, while the dose (D_c) that the polymer film can fully dissolve is 3.4 μC/cm^2. As to the "DSE+Toluene" sample, both D_i and D_c are increased. This observation is attributed to the dilution of acid generator by toluene solvent, and therefore, reduces the sensitivity. Interestingly, the sensitivity for 0.01% w/v "DSE+C60" or "DSE+C70" sample is significantly enhanced after spiking the fullerene molecules. Both D_i and D_c are decreased to 1.4 μC/cm^2 and 2.2 μC/cm^2, respectively. This finding suggests that the incorporation of fullerene molecules into resist can effectively enhance the process throughput.

What happens to the decrease of addressing dose for the resist after spiking with fullerene molecules? In the resist, the electron beam activates the bond of acid generator to produce acid, and the acid induces the functional group reaction of the polymer. The irradiated electron beam easily penetrates through the void region embedded in the resist film, and degrades the throughput. We infer the fullerene molecules with sub-nanometer sizes (0.7-0.8 nm) are embedded into the void of resist sample (in Fig. 3.2) The C60 or C70 fullerene embedded in the void region has a higher electron affinity ~2.6 eV, and therefore, facilitate the bond activation for the acid generator. As we know the electron accelerating voltage can influence the sensitivity, the higher accelerating voltage can improve the resist resolution but deteriorate the resist sensitivity [4]. However, the incorporation of fullerene molecules can shorten the resist exposure time

Figure3.3 indicates the line width increases with the exposure dose. We define the dose range for the "nominal line ± (10%)(nominal line)" as the process window. Table 3.1 suggests the fullerene-incorporated resist has wider dose window than

unadulterated resist. The resist with C60 modification in Fig. 3.3 can fabricate sub-50nm line with respect to C70. This phenomenon implies the C60 with smaller size is better for the resist void filling. The SEM images for the resist with 0.02% w/v fullerene modification are illustrated in Fig. 3.4. The print of sub-50nm lines can not achieve from Fig. 3.4a. The line without fullerene tends to pattern collapse at aspect ratio of 5.75 due to the insufficient adhesion at interface. Figure 3.4b demonstrates the resist without fullerene can resolve 53nm lines at aspect ratio of 4.3, but the line has serious line edge roughness problem. The line edge roughness can lead to higher leakage current for the future nano-devices. However, the resist with 0.02% C60 modification can print 46nm lines (Fig. 3.4c), and 0.02% C70 can print 51nm lines (Fig. 3.4d). The problem of line edge roughness is not seen for the resist with fullerene modification. This observation is dependent on the void of resist polymer of which is filled with fullerene. The fullerene on the sidewall also can minimize the extent of protrusion of polymer. In addition, the interfacial adhesion between fullerene-incorporated resist and the substrate is stronger than the unadulterated resist and the substrate.

Figure 3.5a indicates the hole dimension is significantly influenced with the exposure dose, while the fullerence-incorporated resists in Fig. 3.5b and 3.5c are not. The resist without embedded fullerene molecules can not resolve 60 nm contact hole. The electron beam doses at 7 μC/cm^2 and 8.5 μC/cm^2 can resolve 50 nm contact hole for the resist with 0.01% C60 and C70 modification, respectively. We define the dose range for the “nominal hole ± 10% x (nominal hole)” as the process window. The fullerene-incorporated resists have wider dose windows (i.e. 8-9.5 μC/cm^2 for 0.01% C60, and 9.5-11.5 μC/cm^2 for 0.01% C70) for 60 nm contact hole formation than unadulterated resist. These phenomena are all attributed to the high electron affinity of fullerene molecules.

The C70 fullerene molecule is chosen for further studies due to its better process window. The SEM images for the resist with 0.01% w/v fullerene modification are illustrated in Fig. 3.6. The fabrication yield of 60 nm nominal hole in Fig. 3.6a is not satisfactory due to the lack of electron affinity fullerene. Figure 3.6b demonstrates the resist with C70 fullerene molecules can resolve 53 nm hole.

The stress for various fullerene-incorporated films is demonstrated in Fig.3.7. The resist film without spiking fullerene has large tensile stress. The spiking of fullerene molecules such as C60 or C70 can prevent the stress, and is beneficial for the surface flatness. The fullerene molecules can fill the void of resist and minimize the deformation as spin-coating the resist.

3.3.2. Enhancement of etching performance

In this study, we use RIE to evaluate the etching resistance for the fullerene-incorporated resist on a silicon dioxide layer. The feeding gas is a mixture of Ar, CHF_3, and CF_4. The etching rates of these resists and the oxide film both decrease upon increasing the CHF_3 content. This observation explains the role CHF_3 in the plasma. The species generated from CHF_3 in the plasma are H^+ and CF_3^-, and the CF_3^- species can quench the activity of CF_3^+ in the plasma. Hence, the etching rate decreases. Figure 3.8a depicts the etching selectivity for these resists. The selectivity gradually increases upon increasing the relative CHF_3 content. And figure 3.8b depicts the etching selectivity for these resists. The selectivity is defined as the etch rate of silicon dioxide film to the resist film. The selectivity gradually increases upon increasing the relative CHF_3 content.

In addition, the increase of amount of fullerene molecules can also enhance the selectivity than the unadulterated resist. This observation supports the assumption that

the fullerene molecules can effectively fill the free volume of the resist film. The fullerene molecules consolidate the film, and therefore, the resist film is more resistance to the etching gases. We also find the incorporation of C70 has better etch resistance than C60. This finding is attributed to the higher molecular of C70. It should be noted that the amount of fullerene spiking is only 0.01-0.02%, and is quite low than literature [6-8] report (i.e. 3-50%).

The etching behavior of these resists on the polysilicon film is evaluated using an ECR etcher. The feeding gas is a mixture of Cl_2 and O_2. The etch rate of these resists decrease upon increasing the amount of Cl_2. This observation can be explained by considering the relative amount of O_2 in the plasma: a decrease in O_2 ratio decreases its reaction with the carbon-based ingredients of the resist. For the poly-Si film, the etching rate is very small as if the Cl_2 ratio is below 0.8. However, it increases abruptly at the ratio higher than 0.8. This finding indicates that an O_2 ratio greater than 0.2 is required to oxidize the poly-Si film quickly. The silicon dioxide that forms is resistant to Cl_2 etching. Figure 3.9 depicts the etching selectivity for these resists. The selectivity significantly increases upon increasing the Cl_2 to higher than 0.8. In addition, the increase of amount of fullerene molecules can also enhance the selectivity than the unadulterated resist. This observation also strengthens the role of fullerene molecules mentioned early.

3.3.3. Application of fullerene-incorporated resists for nano-silicide gate and the electrical properties

The various metal silicided lines, such as self-aligned cobalt silicide ($CoSi_2$)/poly-Si, nickel silicide (NiSi)/poly-Si, and NiSi/poly-SiGe, are fabricated with the 0.01% w/v C60-incorporated resist. The cross-sectional SEM image of 60nm

cobalt silicide line is depicted in Fig.3.10 The silicon nitride spacer, self-aligned cobalt silicide, poly-Si and the underlying silicon dioxide layer are successfully fabricated in the Kelvin structure. Then, the sheet resistance (in unit of Ω/sq) of the designed line is determined at probe station. Figure 3.11a illustrates the sheet resistance of $CoSi_2$ has no significant difference in the range 100-200nm. However, the resistance increases dramatically as the line narrowing than 100nm. The phenomenon has been reported to be linked with the presence of infrequent voids in narrow silicide lines [10]. As to the NiSi/poly-Si line in Fig. 3.11b, the sheet resistance gradually decreases with narrowing the line from 200nm to 60nm. However, the range of sheet resistance is only 0.7 Ω/sq, and is insignificance. The sheet resistance of NiSi/poly-Si is quit lower than $CoSi_2$/poly-Si. This observation is attributed to the lower Si content in the NiSi than in the $CoSi_2$. The underlying poly-Si of NiSi has changed to poly-SiGe for evaluating the electrical property. Figure 3.11c demonstrates the sheet resistance gradually increases with shrinking the line width. In addition, the electrical property of NiSi on poly-SiGe is deteriorated than on the poly-Si. We suppose the NiSiGe film is formed between the NiSi and poly-SiGe, and has lower Ni percentage.

3.3.4. Application of fullerene-incorporated resists for patterning and filling the contact hole

Figure 3.12a depicts the 56 nm contact hole in the silicon dioxide film can be fabricated by 0.02% w/v C70 fullerene modification. The cross section SEM in Fig.3 12b suggests the surface diameter of the hole is wider than the bottom diameter of the hole due to reactive-ion plasma etching. The average aspect ratio for the contact hole is ~2. In order to evaluate the hole filling process of TiN plug, the PVD and CVD

methods are chosen in this study. The reactive sputtering is used to deposit 200-nm TiN film onto the silicon dioxide pattern. The PVD method uses argon and nitrogen as process gases, and titanium as the target. In plasma, parts of both gases are ionized, and some nitrogen molecules dissociate, which generates chemically reactive free nitrogen radicals. Titanium atoms sputtered off from the target surface by argon ions react with nitrogen when they pass through the argon-nitrogen plasma, and titanium nitride is formed and deposited on the wafer surface. Even some titanium atoms can pass through the plasma and deposit on the wafer surface. They react with nitrogen radicals and form titanium nitride there. Nitrogen radicals can also react with titanium target and form a titanium nitride layer on the target surface. Argon ions sputter the TiN molecules off the target surface and deposit them on the wafer surface. Figure 3.13a clearly illustrates the hole can not fill with the TiN. The sidewall in the hole is partially covered with TiN, and the surface diameter of hole is thinner than the bottom diameter of hole. The gap-filling and step coverage of the contact hole is not satisfactory by PVD method. The metal CVD is widely used to deposit metal in IC processing. CVD metal films have proven to be very good step coverage and gap-filling capability and can fill tiny contact holes to make the connections between metal layers. CVD metal thin films normally have poorer quality and higher resistivity than those of PVD metal thin films. Therefore, they are mainly used for plug and local interconnection and not applied for the global interconnection. The Fig. 3.13b depicts the nanometer contact hole can be effectively filled by CVD TiN processes without any void problem. These observations from Fig. 313b suggest CVD method can apply to fill the ~50 nm contact

3.4 Summary

We have established a successful fabrication technique that incorporated the fullerene molecules in the resist for preparing sub-50nm lines and sub-50 nm holes by electron beam lithography. The improvement of throughput is attributed to the better electron affinity of the fullerene. The prevention of line edge roughness and pattern collapse is also an advantage of this modification technology. Together with the above nanofabrication technique, the contact hole at nanometer scale is successfully filled with the CVD TiN. The proposed method can be applied to fabricate the nano-plugs in the future. In addition, the technique significantly enhances the etching selectivity of resist for plasma gases of CHF_3/CF_4 or Cl_2/O_2. We have used this resist to fabricate various metal silicide gates, and the NiSi on poly-Si has the better electrical performance.

Table 3.1. The dose and process window for the resists to print various designed lines.

	NEB	NEB with 0.02% C60	NEB with 0.02% C70
Dose for 100nm line ($\mu C/cm^2$)	**14**	**12**	**11.5**
Dose for 80nm line ($\mu C/cm^2$)	**14**	**12**	**11.5**
Dose for 60nm line ($\mu C/cm^2$)	**14.5**	**12.5**	**11.5**
Dose for 40nm line ($\mu C/cm^2$)	**Not print**	**18**	**17**
Process window for 60nm line ($\mu C/cm^2$)	**1.5**	**2**	**2**

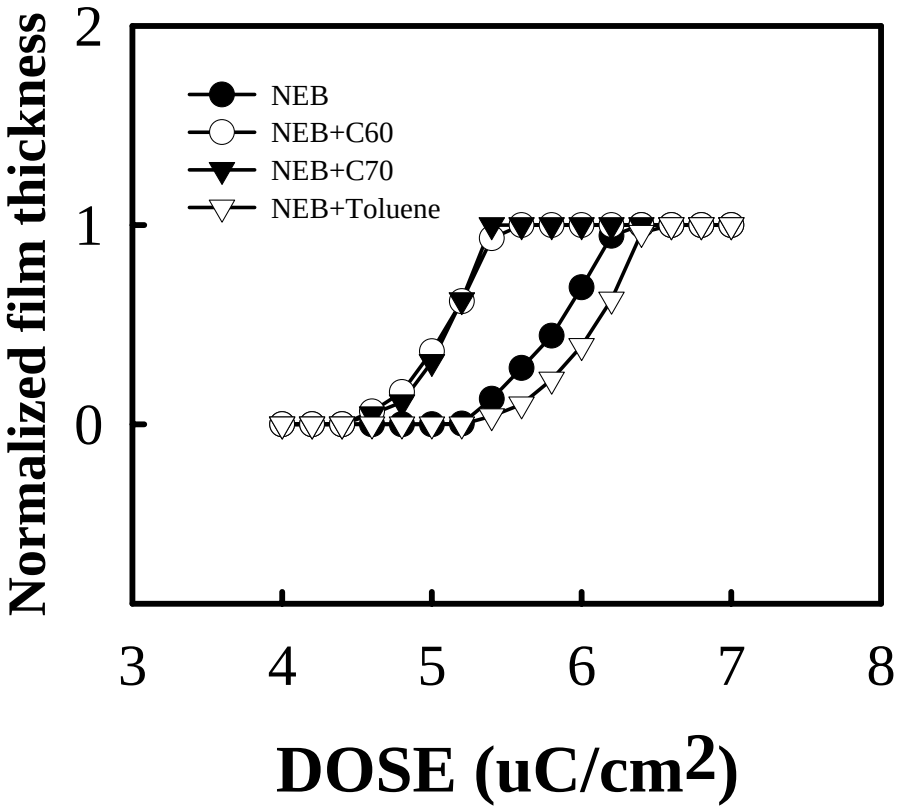


Figure 3.1(a) The sensitivity curves for various resists.

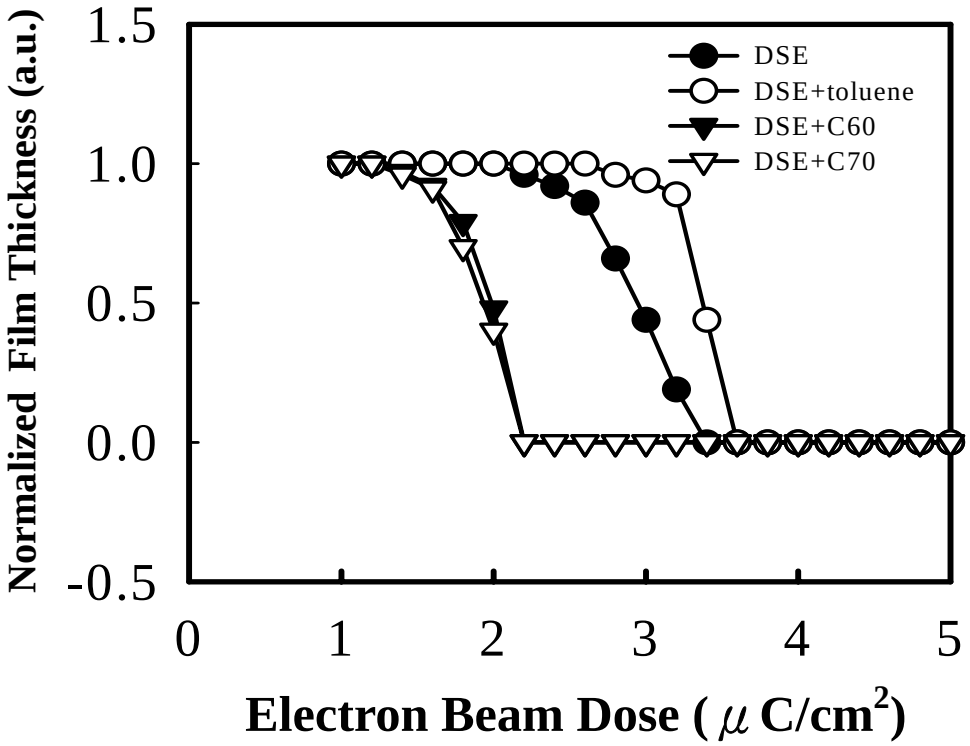


Figure 3.1(b) The effect of the electron beam dose on the normalized resist film thickness.

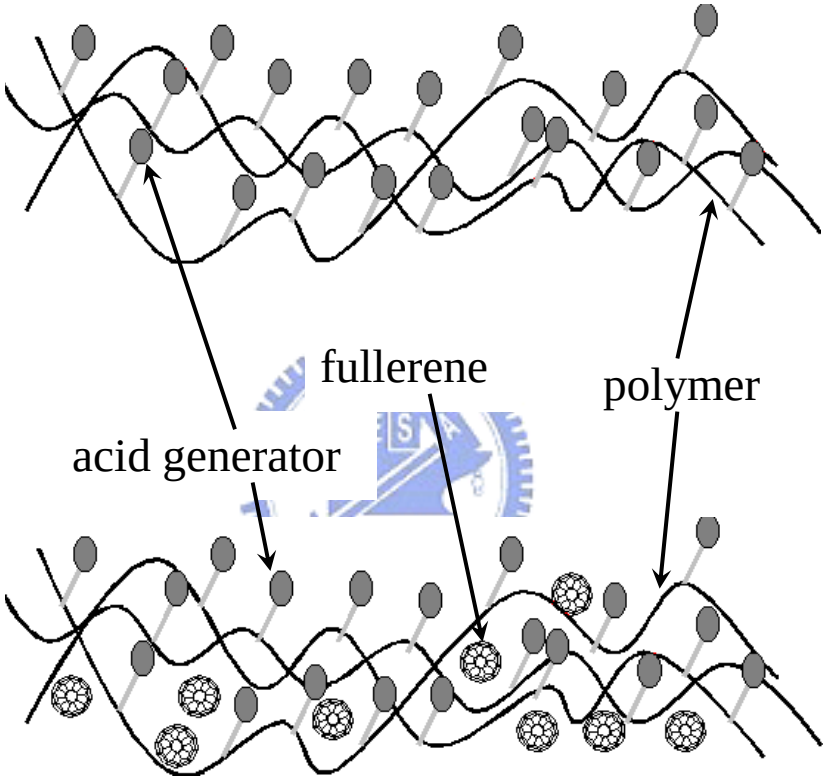


Figure 3.2 The model for incorporation of fullerene molecules in the void of resist polymer.

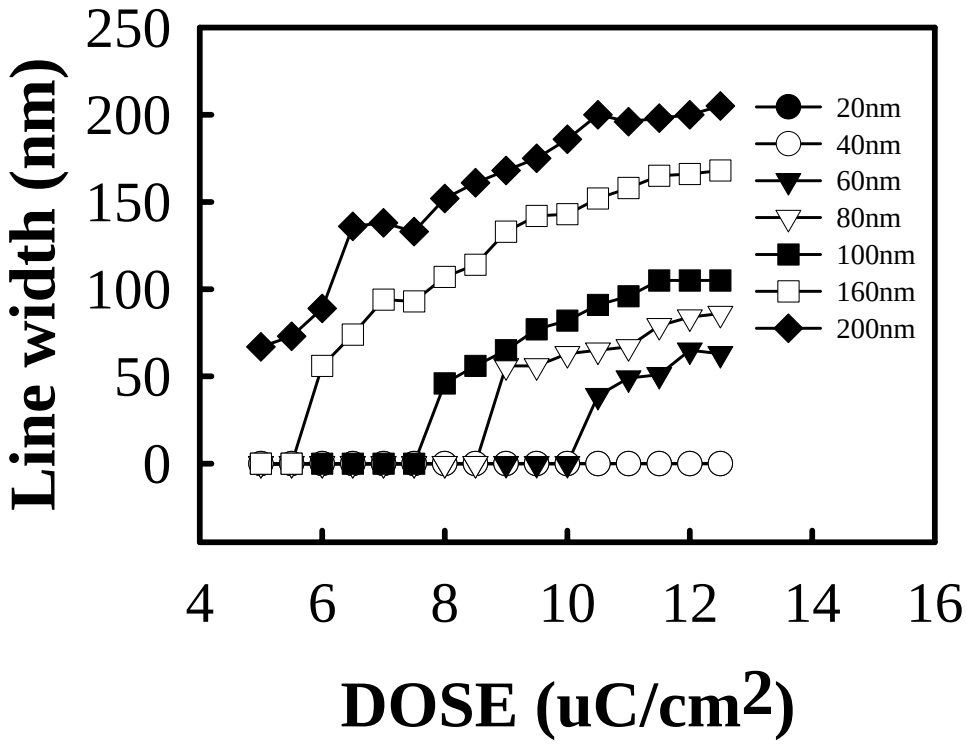


Figure 3.3 The effect of electron beam dose on the line width for various designed lines: (a) NEB resist with 0.02% w/v C60

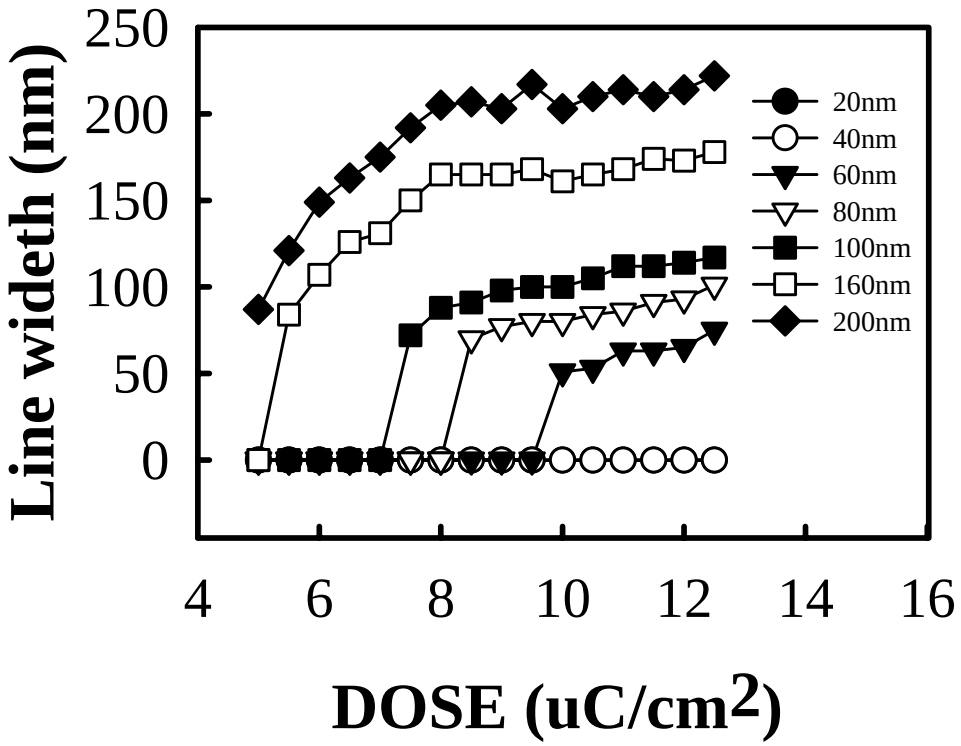
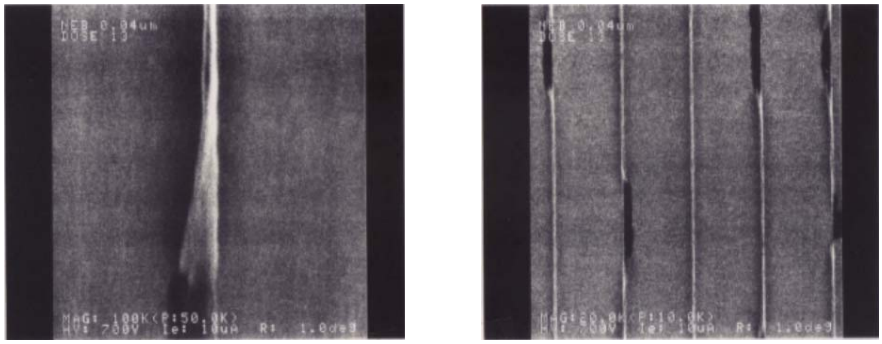
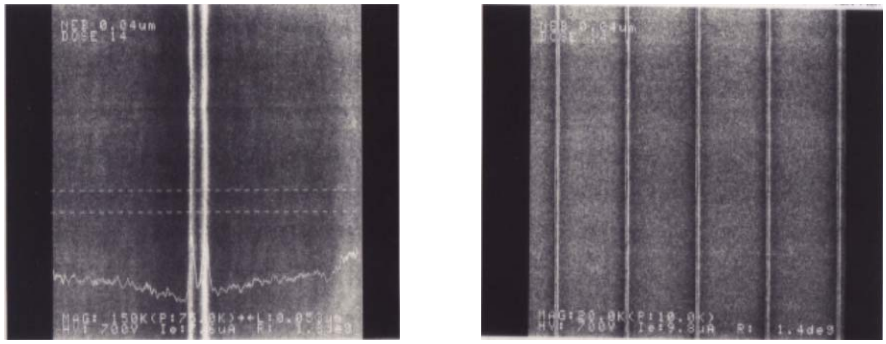


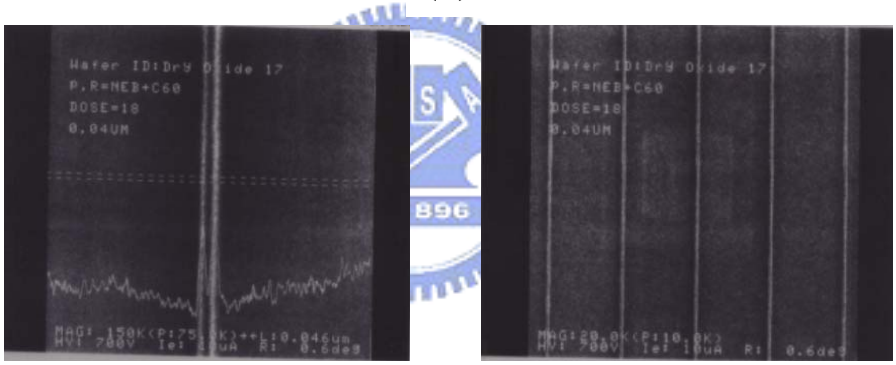
Figure 3.3 The effect of electron beam dose on the line width for various designed lines: (b) NEB resist with 0.02% w/v C70



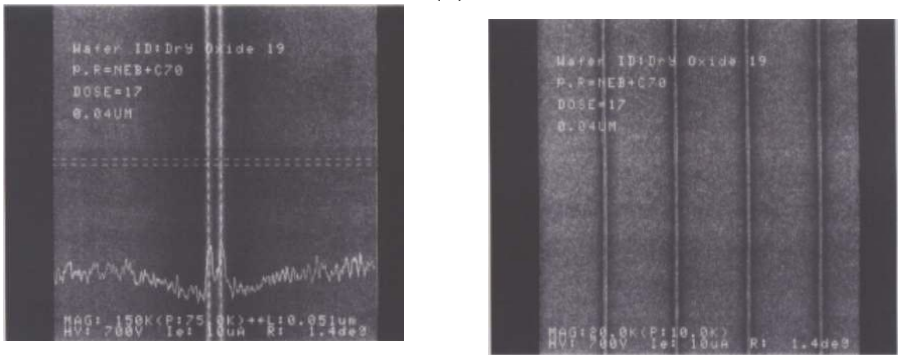
(a)



(b)



(c)



(d)

Figure 3.4 Top-down SEM images of resist: (a) the sub-50nm line without fullerene modification; (b) the 53nm line without fullerene modification; (c) the 46nm line with 0.02% C60 modification; (d) the 51nm line with 0.02% C70 modification.

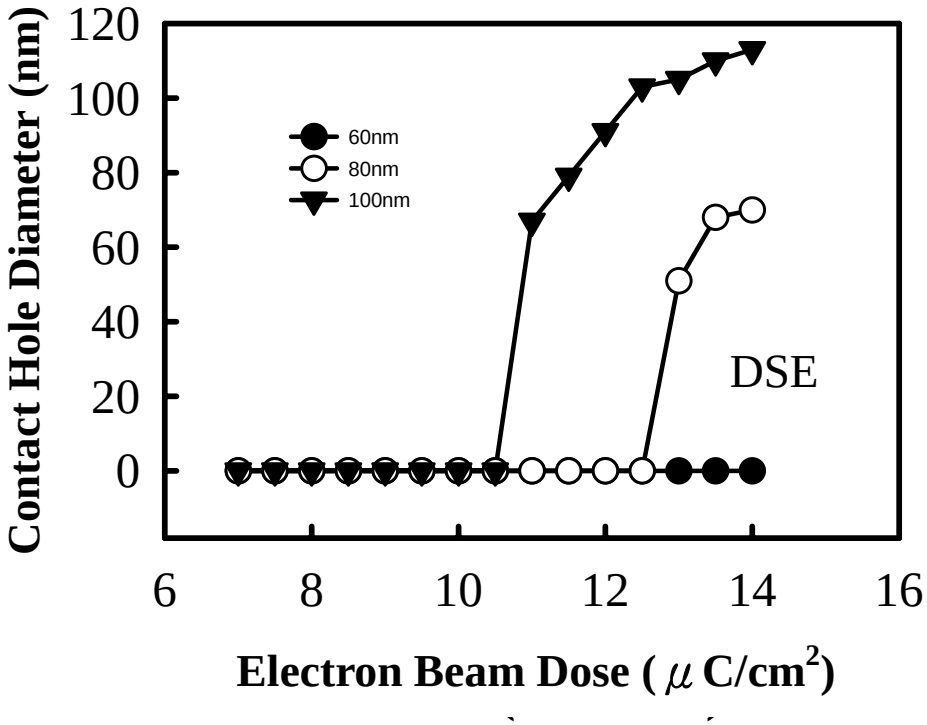


Figure 3.5 The effect of electron beam dose on the final hole dimension for target hole dimensions of 60, 80, and 100 nm: (a) DSE resist

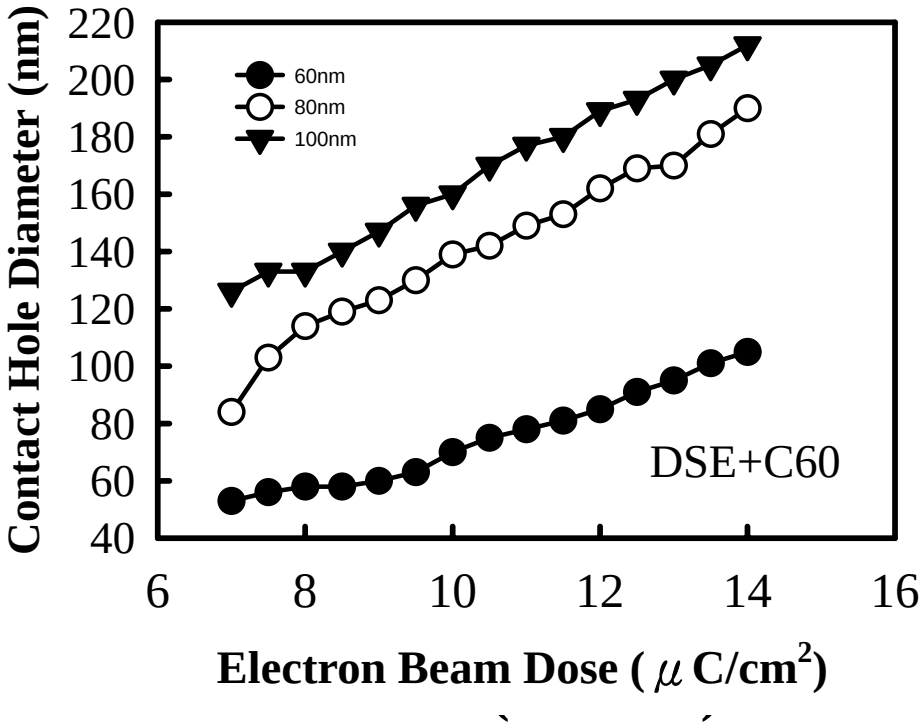


Figure 3.5 The effect of electron beam dose on the final hole dimension for target hole dimensions of 60, 80, and 100 nm: (b) DSE resist with 0.01% w/v C60

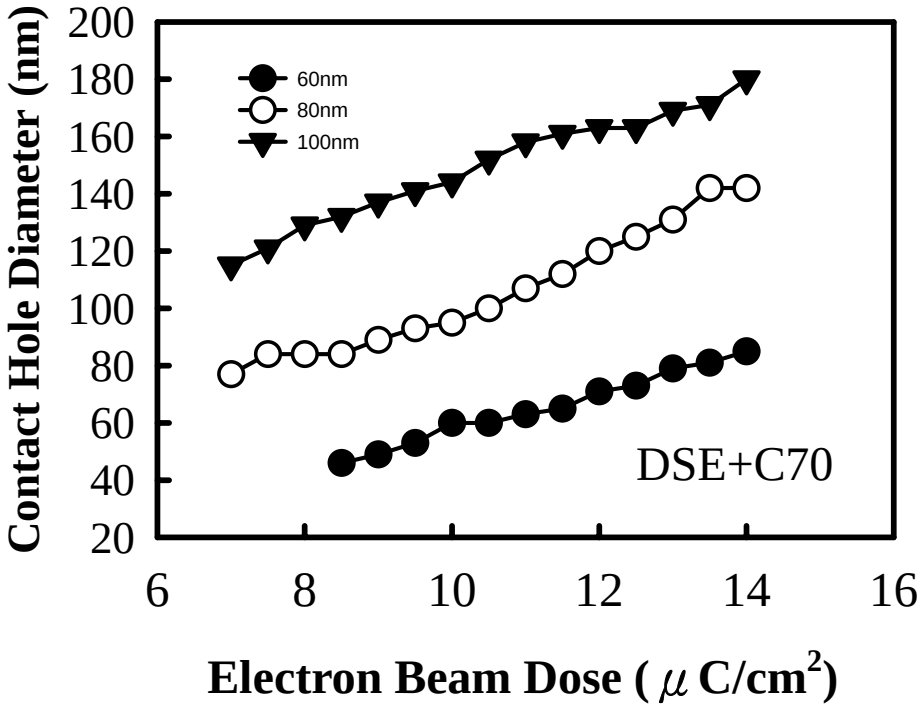


Figure 3.5 The effect of electron beam dose on the final hole dimension for target hole dimensions of 60, 80, and 100 nm: (c) DSE resist with 0.01% w/v C70.

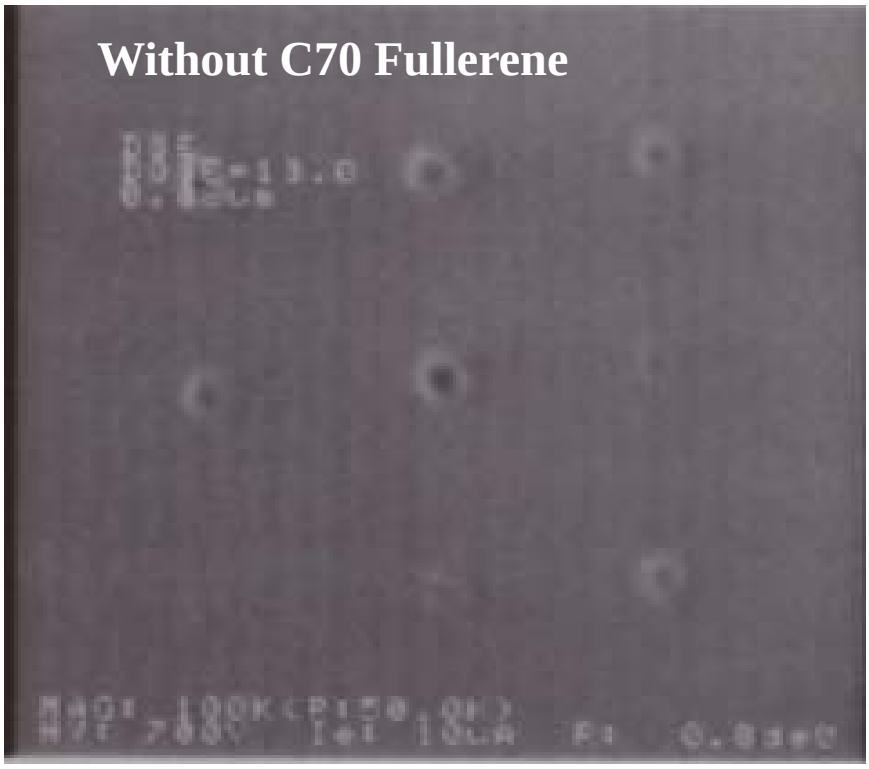


Figure 3.6 Top-view SEM images of 60 nm nominal hole (a) without C70 fullerene in the electron beam resist.

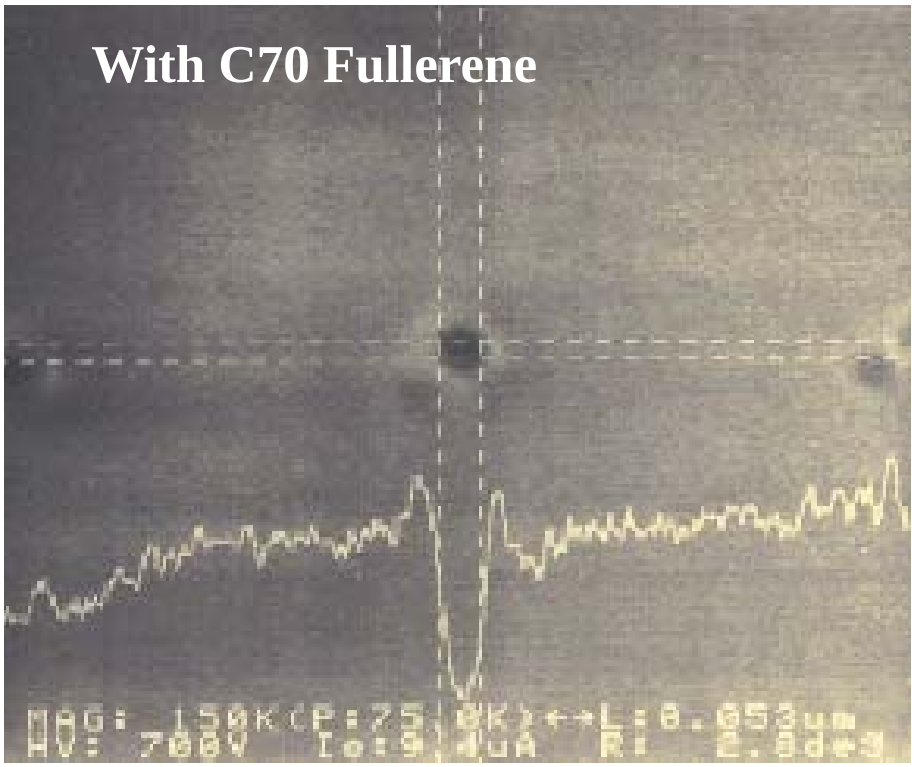
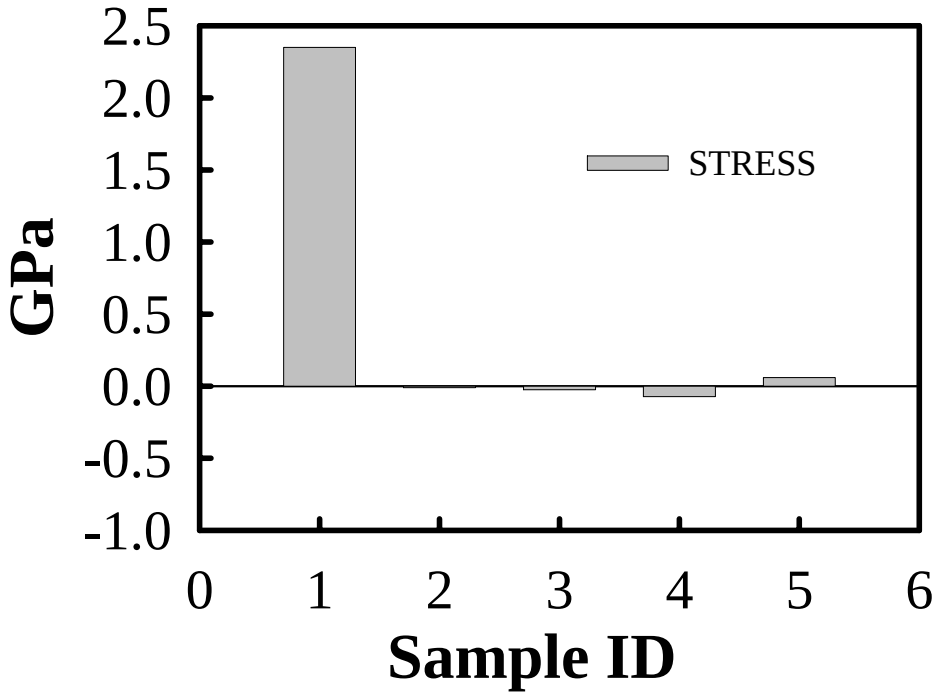
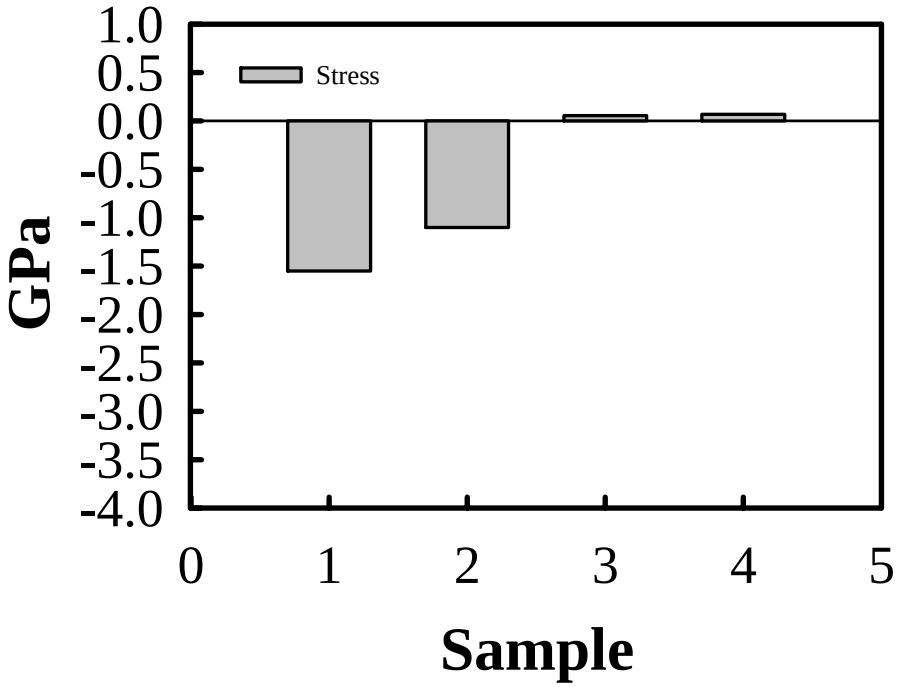


Figure 3.6 Top-view SEM images of 60 nm nominal hole (b) with C70 fullerene in the electron beam resist.



1	**NEB+Toluene**
2	**NEB + C60-0.01%**
3	**NEB + C60-0.02%**
4	**NEB + C70-0.01%**
5	**NEB + C70-0.02%**

Figure 3.7 The stress of resist film on the silicon wafer (a) NEB resist



1	**DSE**
2	**DSE+Toluene**
3	**DSE + C60-0.01%**
4	**DSE + C70-0.01%**

Figure 3.7 The stress of resist film on the silicon wafer (b) DSE resist

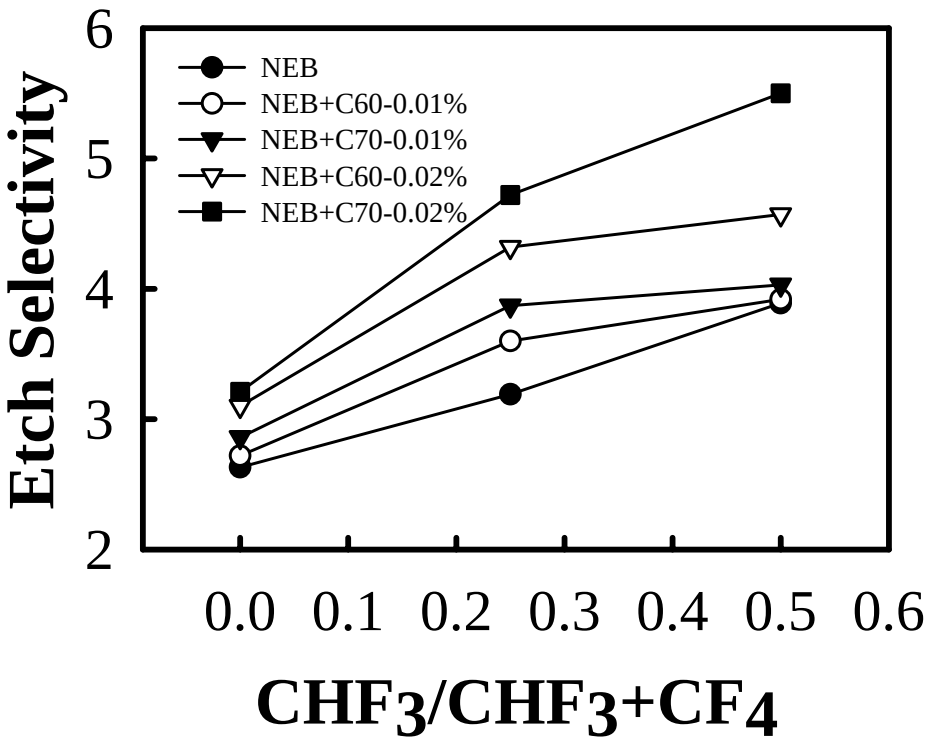


Figure 3.8a Etching selectivity of NEB resist with respect to silicon dioxide

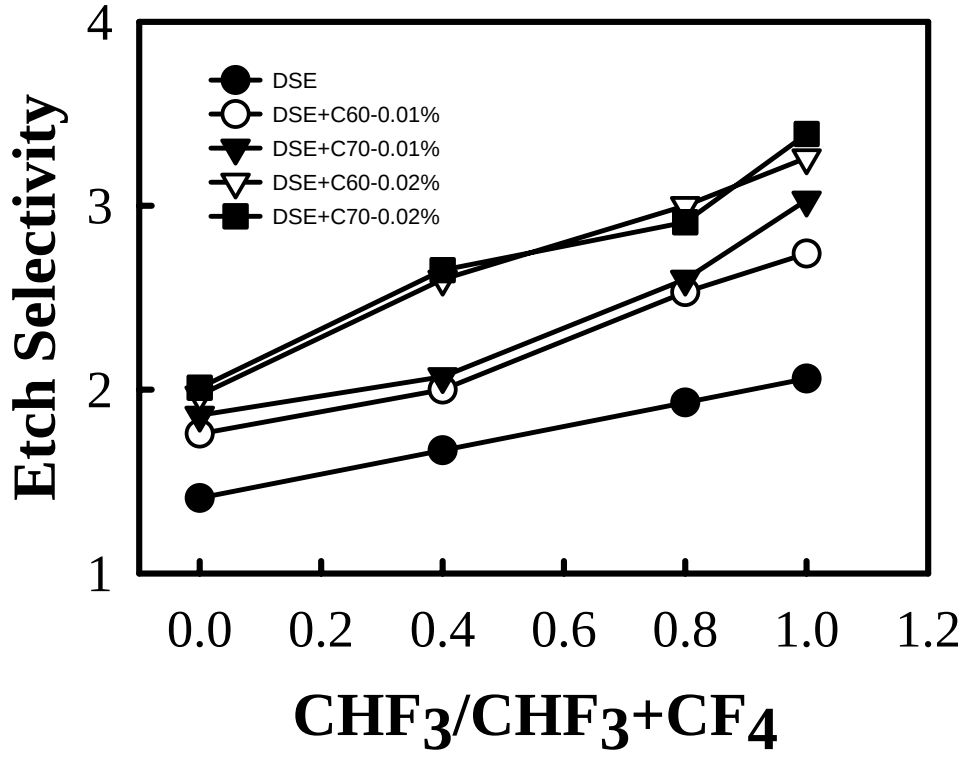


Fig. 3.8b Etching selectivity of DSE resist with respect to silicon dioxide.

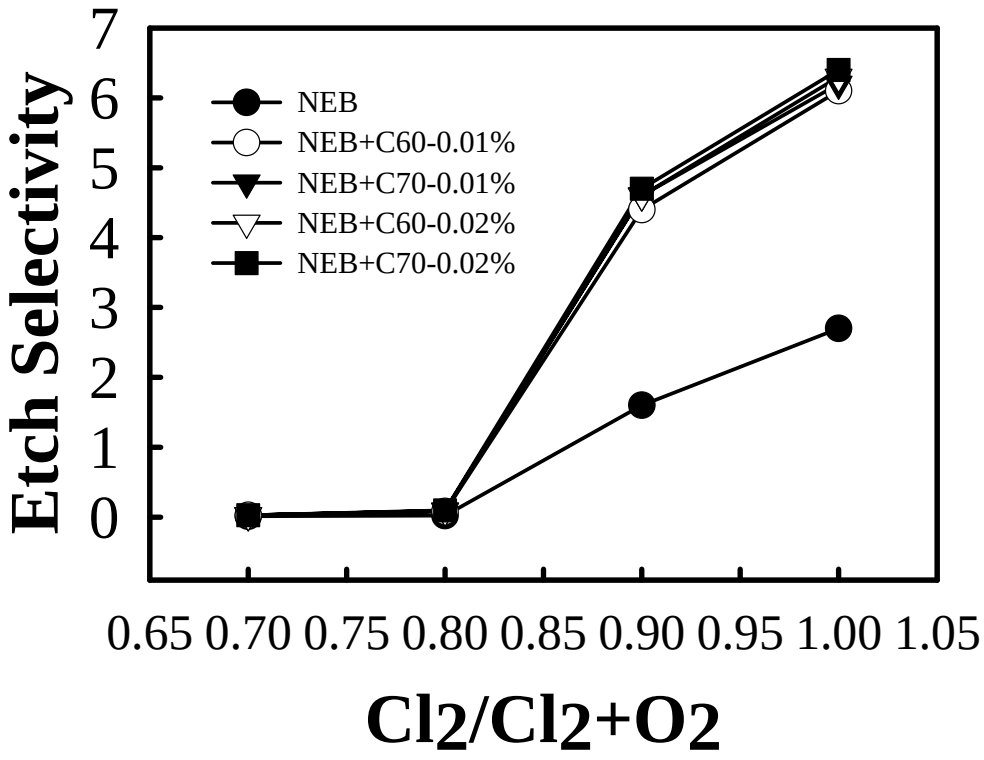


Figure 3.9 Etching selectivity of NEB resist with respect to polysilicon.

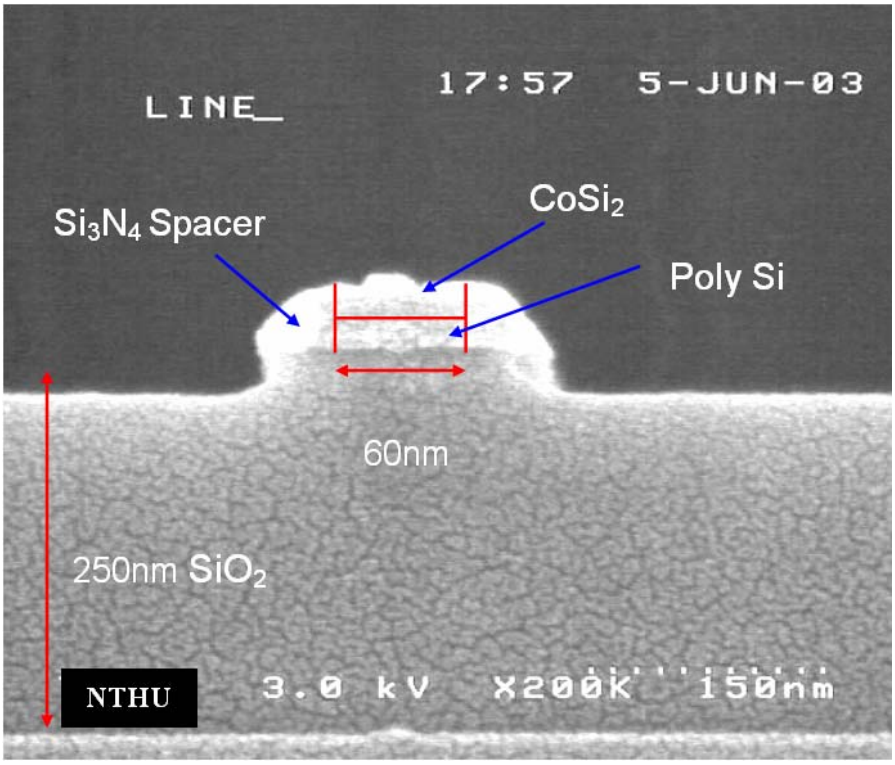


Figure 3.10 The cross-sectional SEM image of 60nm cobalt silicide line.

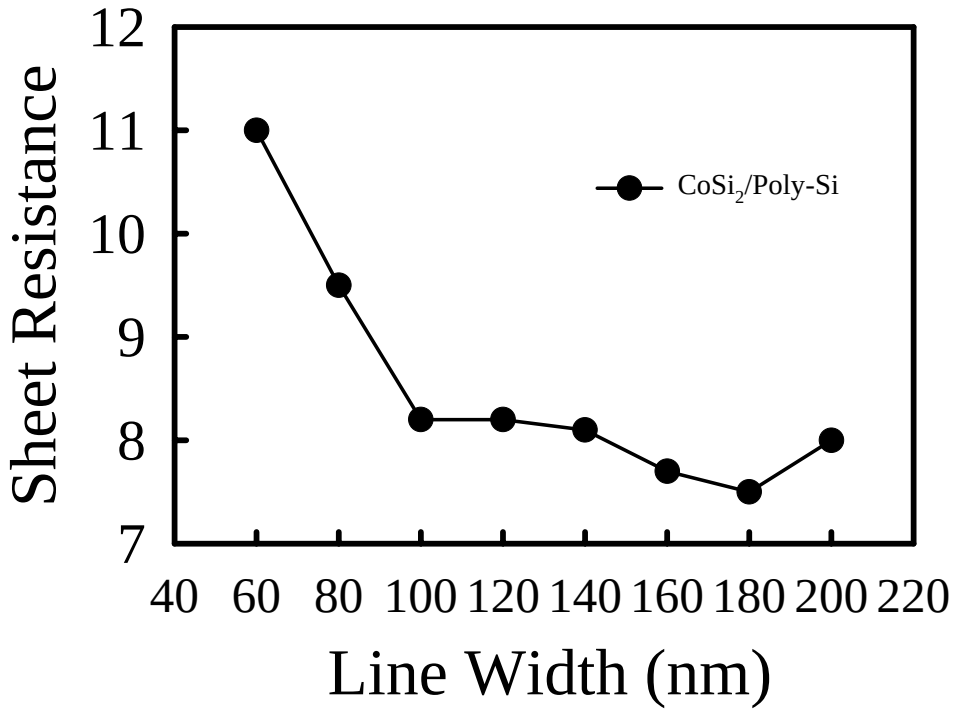


Figure 3.11 Sheet resistance of (a) $CoSi_2$ on polysilicon

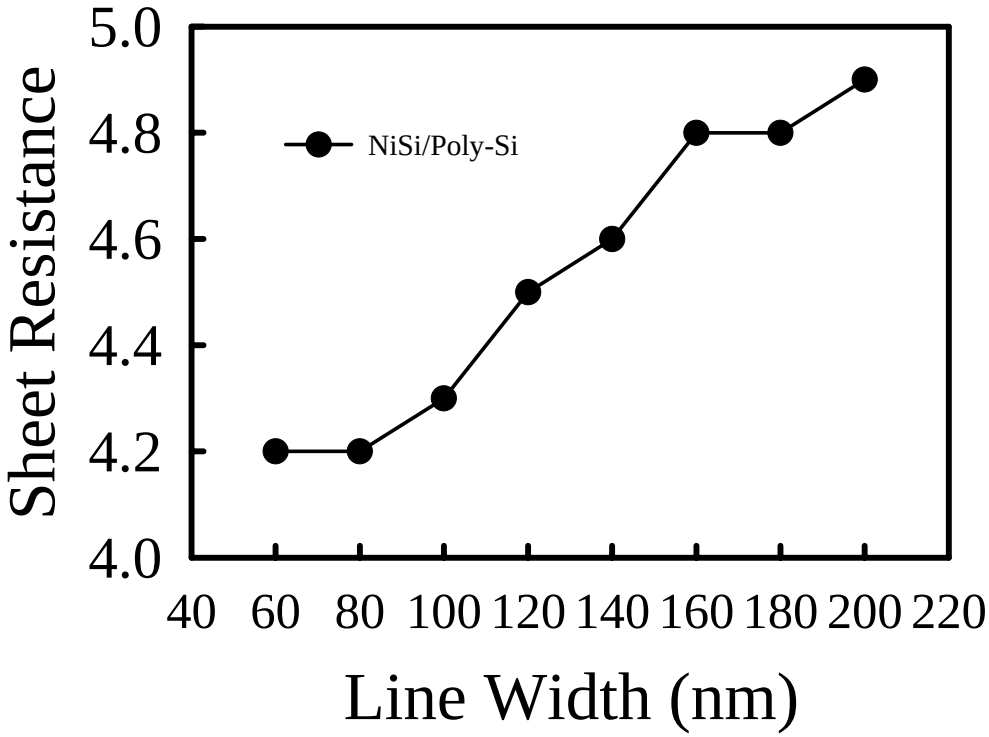


Figure 3.11 Sheet resistance of (b) NiSi on polysilicon

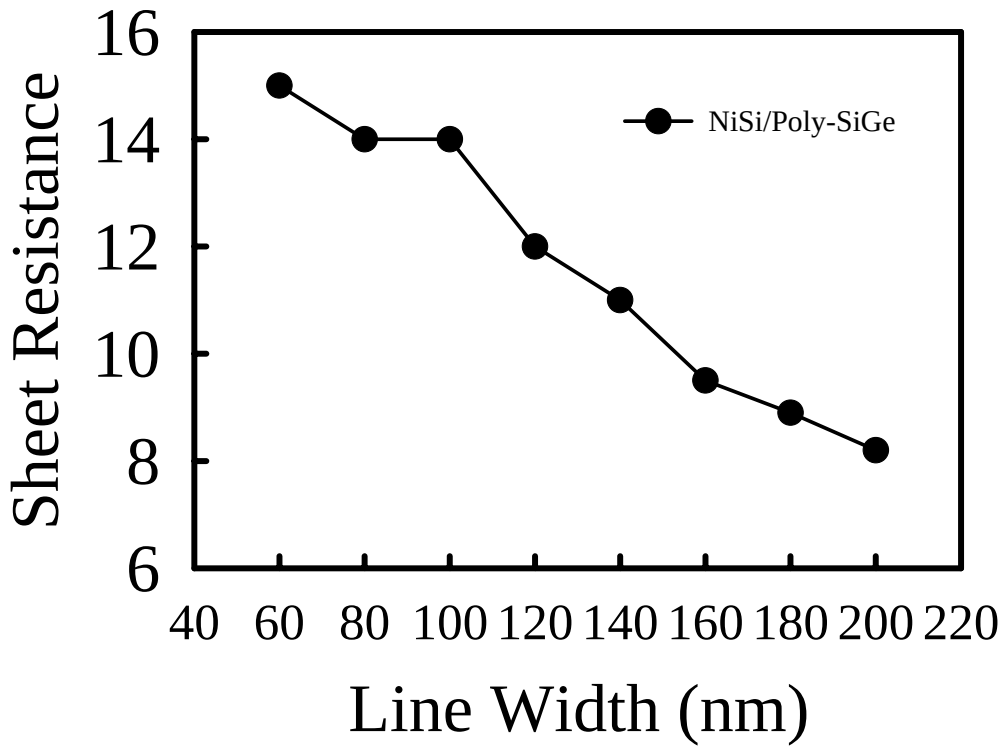


Figure 3.11 Sheet resistance of (c) NiSi on poly-SiGe.

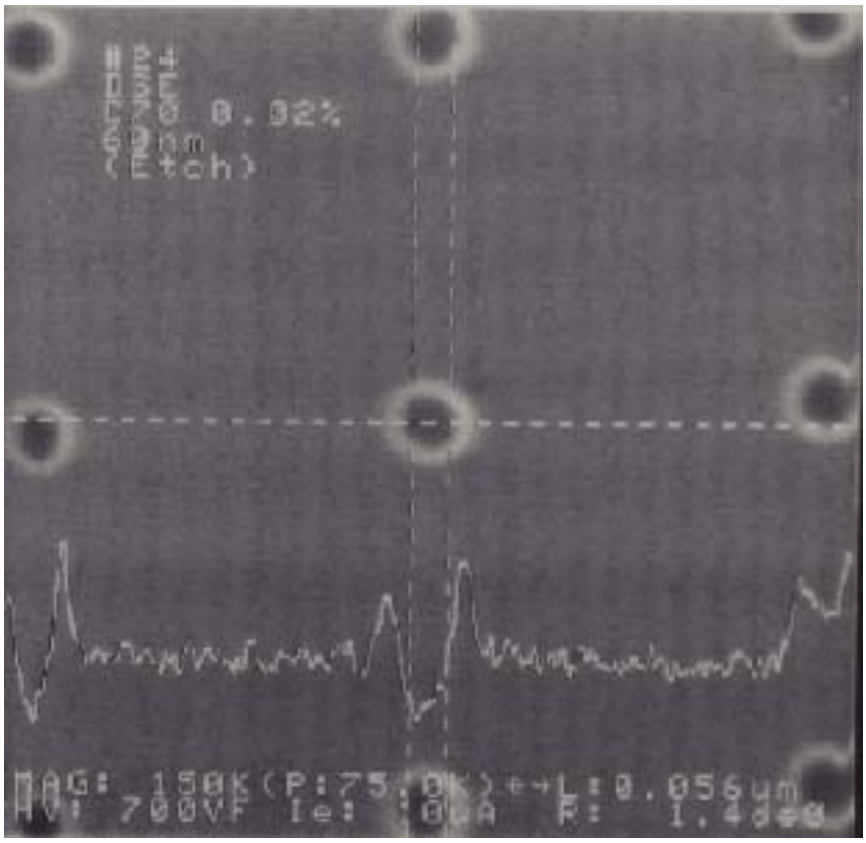


Figure 3.12a Top view SEM images of a 56 nm contact hole in SiO_2 layer.

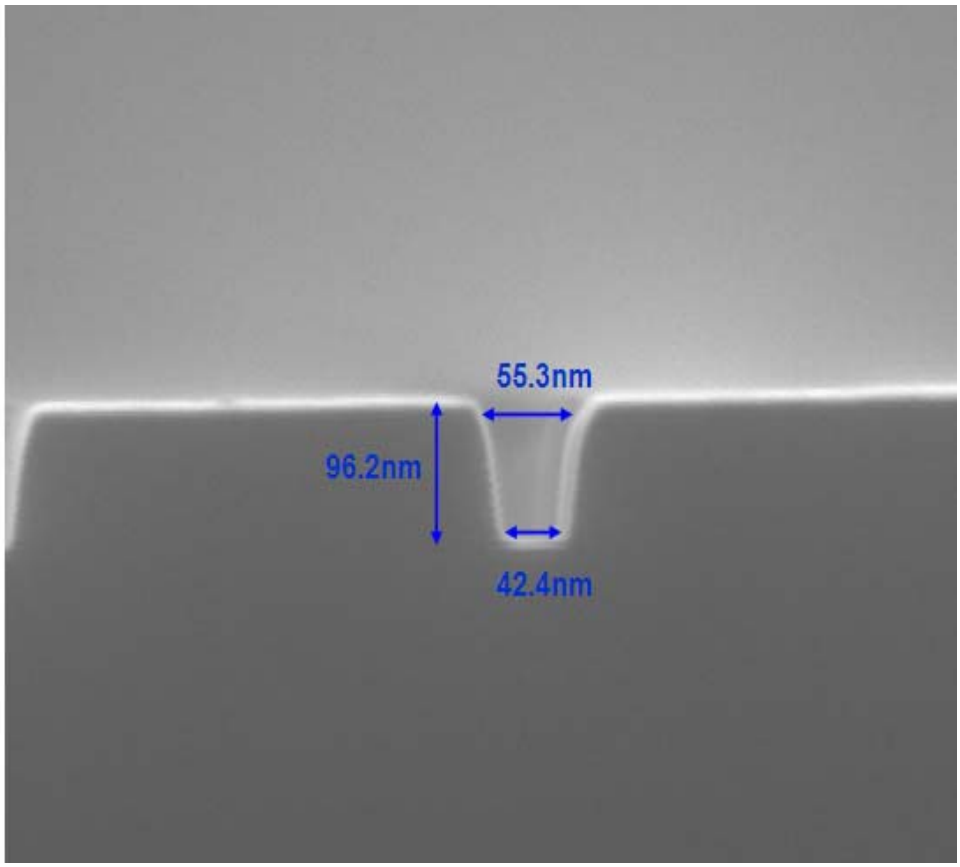


Figure 3.12b Cross section SEM images of a 56 nm contact hole in SiO_2 layer.

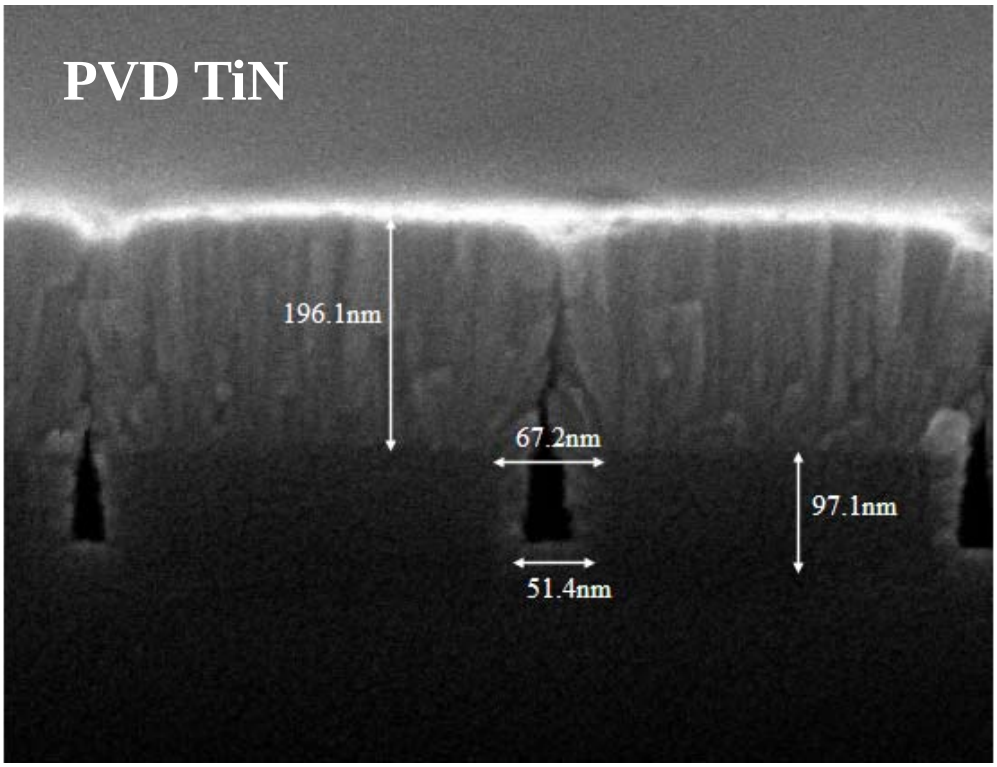


Figure 3.13 Cross section SEM images of ~50-nm contact hole with 200-nm TiN film deposited by (a) PVD.

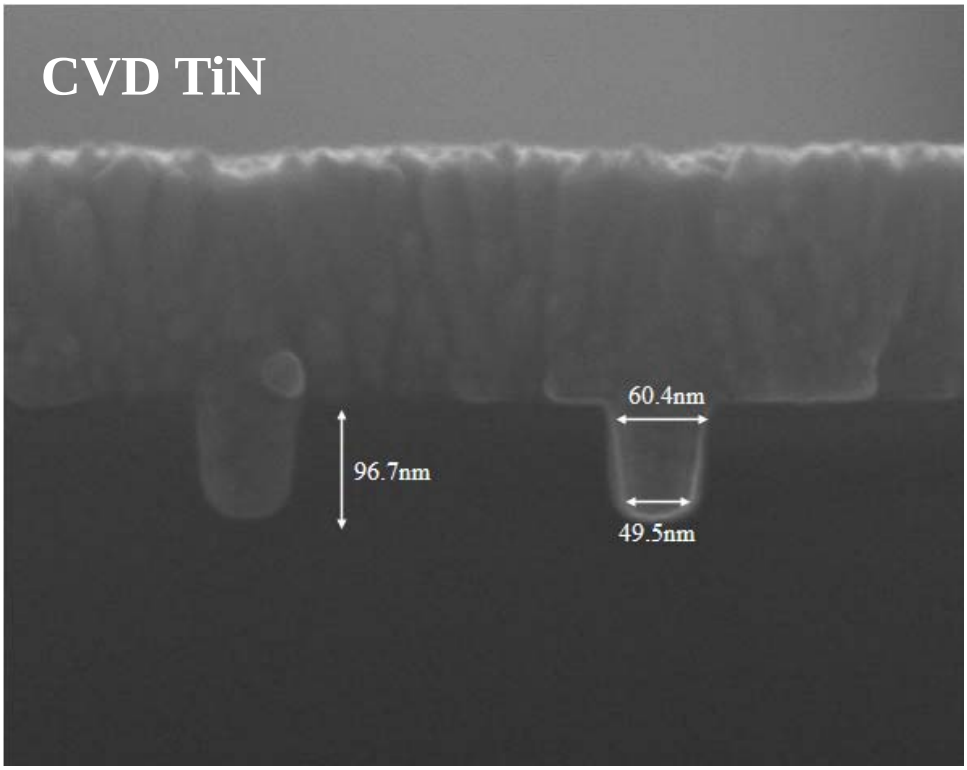


Figure 3.13 Cross section SEM images of ~50-nm contact hole with 200-nm TiN film deposited by (b) CVD.

Chapter 4

The impact of deep Ni salicidation and NH_3 plasma treatment on nano-SOI FinFETs

4.1 Introduction

In the last few years, the industries focus on the planar CMOS scaling. However, scaling planar CMOS to short gate length will face many problems like electrostatics, excessive leakages, and mobility degradation. Non-planar CMOS MOSFETs provide potential advantages in packaging density, carrier transport, and device scalability [1]. SOI FinFETs technology has a lot of advantages such as the reduction of parasitic capacitances, the feasibility of diffusion resistors and capacitors free of junction effects, better device isolation leading to absence of latch up, substrate coupling and good gate control ability. But the floating body effect is a main problem of the SOI MOSFET devices. It will cause drain current “kink”, abnormal subthreshold slope, and low breakdown voltage [2]-[3]. The metal salicidation method has been used to suppress the floating body effect and DIBL [4]-[5] and reduce parasitic S/D resistances in the thin-film SOI devices.

Plasma treatment has long been used in TFT devices. The suitable plasma treatment can improve the electrical characteristics of the TFT devices because it can repair the defects in the devices. However, plasma treatment has not been proposed in the nano-SOI FinFETs fabrication. In this paper, we propose the 50nm gate length nano-SOI FinFETs with deep Ni-salicidation and NH_3 plasma treatment. This is the first time to apply NH_3 plasma treatment on thin-film SOI devices. The NH_3 plasma treatment is expected to repair the process-induced defects in thin-film SOI devices.

4.2 Experimental

The schematic device structure of transmission electron microscopy (TEM) and the top view scanning electron micrograph (SEM) micrograph for the nano-SOI FinFETs are shown in Fig.4.1. The channel length, the thickness and the fin width of nano-SOI FinFETs is about 50nm, 40nm and 42nm, respectively. Hence, the channel width of device is about 122nm (fin width + 2 × fin height = 42nm + 2 × 40nm).

The schematic structure of nano-SOI FinFETs is shown in Fig.4.2. The nano-SOI FinFETs were fabricated by the following process steps. First, active region was patterned and a 4-nm thermal gate oxide layer was grown by furnace. Next, a 100-nm *in-situ* n^+ phosphorus doped a-Si gate layer was deposited by LPCVD. After gate patterning, the remaining oxide on source/drain regions was removed by diluted HF and then a 150-nm TEOS oxide sidewall spacer was formed by deposition and etching. A self-aligned implantation was used to perform the n^+ source/drain extension with As^+ to dose $1 \times 10^{15}\ cm^{-2}$ and energy 20 keV, tilt 20^o. Then, a self-aligned implantation was used to perform the n^+ source/drain with As^+ to dose $5 \times 10^{15}\ cm^{-2}$ and energy 15 keV, tilt 7^o. Dopants were activated by RTA at 950°C for 15s. A Ni film of about 10-nm was deposited by sputtering after a dilute HF-dip and then Ni-salicidation was carried out at 450°C for 60-sec by one-step rapid thermal annealing (RTA) in the N_2 ambient. Unreacted Ni was removed by the mixture of H_2SO_4 and H_2O_2 solutions. After contact and metallization processes, NH_3 plasma procedures were implemented after sintering at 400°C for 30-min. Conventional devices without Ni-salicidation and NH_3 plasma were also fabricated to serve as control ones.

4.3. Results and Discussion

The measured transistor characteristics of the no Ni-salicided SOI devices with W / L = 122nm / 50nm (SOI FinFETs) and W / L = 180nm / 50nm (SOI MOSFETs) are shown in Fig. 4.3. Figure 4.3(a) shows the S.S. and DIBL of SOI FinFETs are 379 mv/dec and 0.397 V, respectively. Figure 4.3(b) shows the S.S. and DIBL of SOI MOSFETs are 267mv/dec and 0.24 V, respectively. The device performance of SOI MOSFETs is very poor because the very short gate length (50nm). The subthreshold swing is relatively large due to the short channel effect and poor gate control ability. However, the SOI FinFETs show the good gate control ability and improved subthreshold swing [6]. We believe that dopants were activated by RTA at 950°C for 15s and therefore the defects of S/D are not fully eliminated. The high leakage currents of device are caused by the defects of S/D.

The measured transistor characteristic of the deep Ni-salicided SOI FinFETs with W / L = 122nm / 50nm is illustrated in Fig. 4.4. This Figure indicates the deep Ni-salicided SOI FinFETs have smaller S.S. (112mv/dec) and less DIBL (0.11V) compared with no Ni-salicided SOI devices. Figure 4.4 also exhibits the improvement of off-state leakage currents observed in deep Ni-salicided SOI FinFETs. The definition of DIBL is the V_{TH} shift between two drain voltages in the same device. The V_{TH} shift is caused by the DIBL effect. The reduced V_{TH} shift strongly supports that the BJT effect was significantly suppressed in the deep Ni-salicided SOI FinFETs. Similar suppression of the floating body effect was reported for deep silicidation of partially-depleted SOI devices, where the thick silicide layer worked as a sink for holes [4]-[5]. We demonstrate that Ni salicidation is highly effective in suppressing floating body effects. Besides, the Ni salicidation can reduce parasitic S/D resistances in the nano-SOI FinFETs. We think that the improved S.S. is due to the reduced

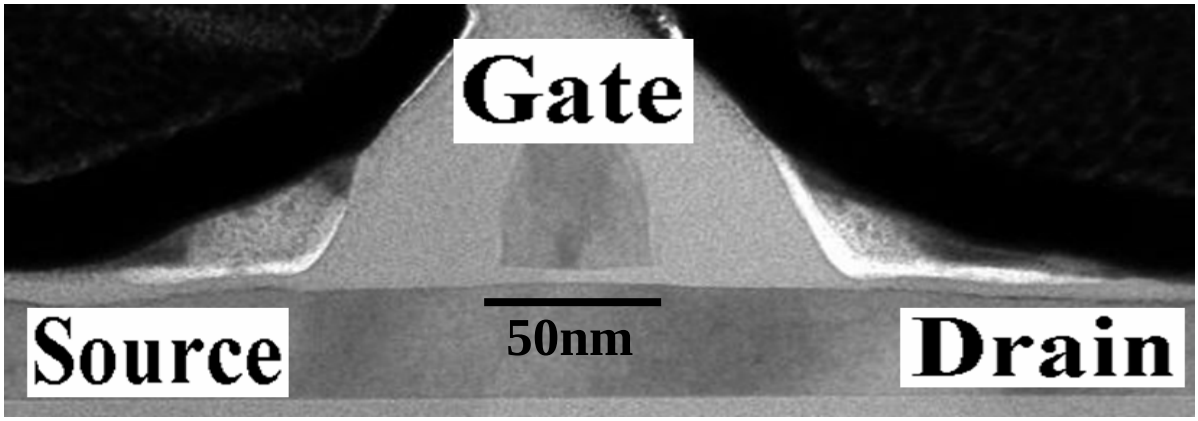
parasitic S/D resistances in the nano-SOI FinFETs.

Figure 4.5 displays the measured transistor characteristic of the deep Ni-salicided SOI FinFETs after state-of-the-art NH_3 plasma treatment with W / L = 122nm / 50nm. The S.S. and DIBL of deep Ni-salicided SOI FinFETs after NH_3 plasma treatment are 66mv/dec and 0.03V, respectively. We note the improvement of off-state leakage current observed in deep Ni-salicided SOI FinFETs after suitable NH_3 plasma treatment. The S.S., DIBL and off-state leakage current of the deep Ni-salicided SOI FinFETs after NH_3 plasma treatment are better than that in the deep Ni-salicided SOI FinFETs without NH_3 plasma treatment. The NH_3 plasma treatment exhibits high defect passivation ability for deep Ni-salicided SOI FinFETs. We believe this improvement is due to the generation of H atoms in NH_3 plasma, which can passivate process-induced defects in thin-film SOI devices [7]-[8]. In this figure, we can see that the defects of S/D junction (leakage currents) and Si/SiO_2 interface (S.S.) can be passivated by NH_3 plasma. However, the DIBL also can be improved by NH_3 plasma because the true device characteristics will be screened by defects in S/D junction, channel, Si/SiO_2 interface. In our study, we think that the improvement of DIBL is due to the passivation of deep Ni salicidation process-induced defects in the S/D junction.

4.4 Summary

In this paper, we have fabricated 50nm gate length nano-SOI FinFETs with deep Ni-salicidation and NH_3 plasma treatment. From the measured transistor characteristics, the narrow width device is performed better than the long width device. We also discuss the effect of Ni-salicidation and state-of-the-art NH_3 plasma treatment on the nano-SOI FinFETs. The deep Ni-salicided SOI FinFETs after NH_3

plasma treatment can achieve high performances like S.S = 66mv/dec and DIBL= 0.03V. The floating body effect and process-induced defects can be improved by deep Ni-salicidation and NH_3 plasma treatment in nano-SOI FinFETs. We believe that these key technologies are suitable and compatible for future nano-devices manufacturing.



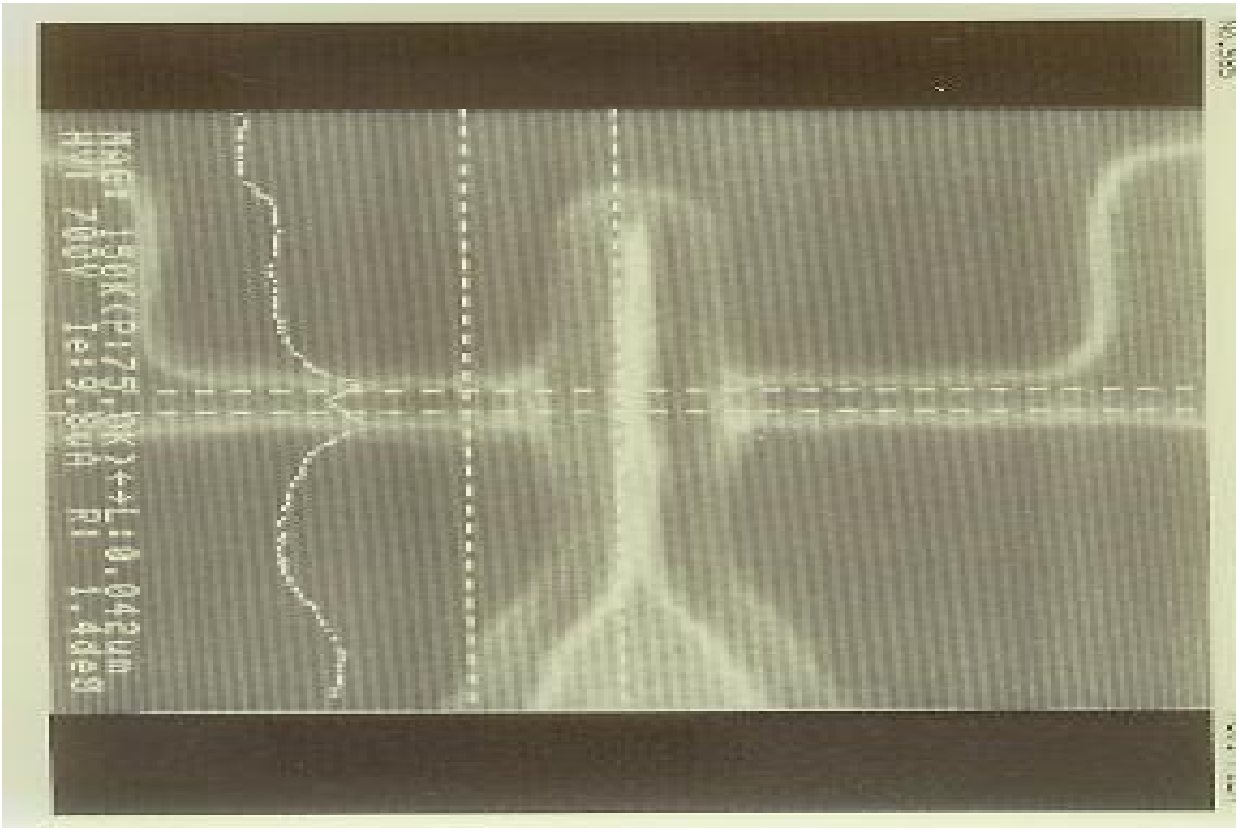


Figure 4.1. The TEM and top view SEM micrographs of nano-SOI FinFETs. The gate length is 50nm, and the Si channel thickness is 40nm.

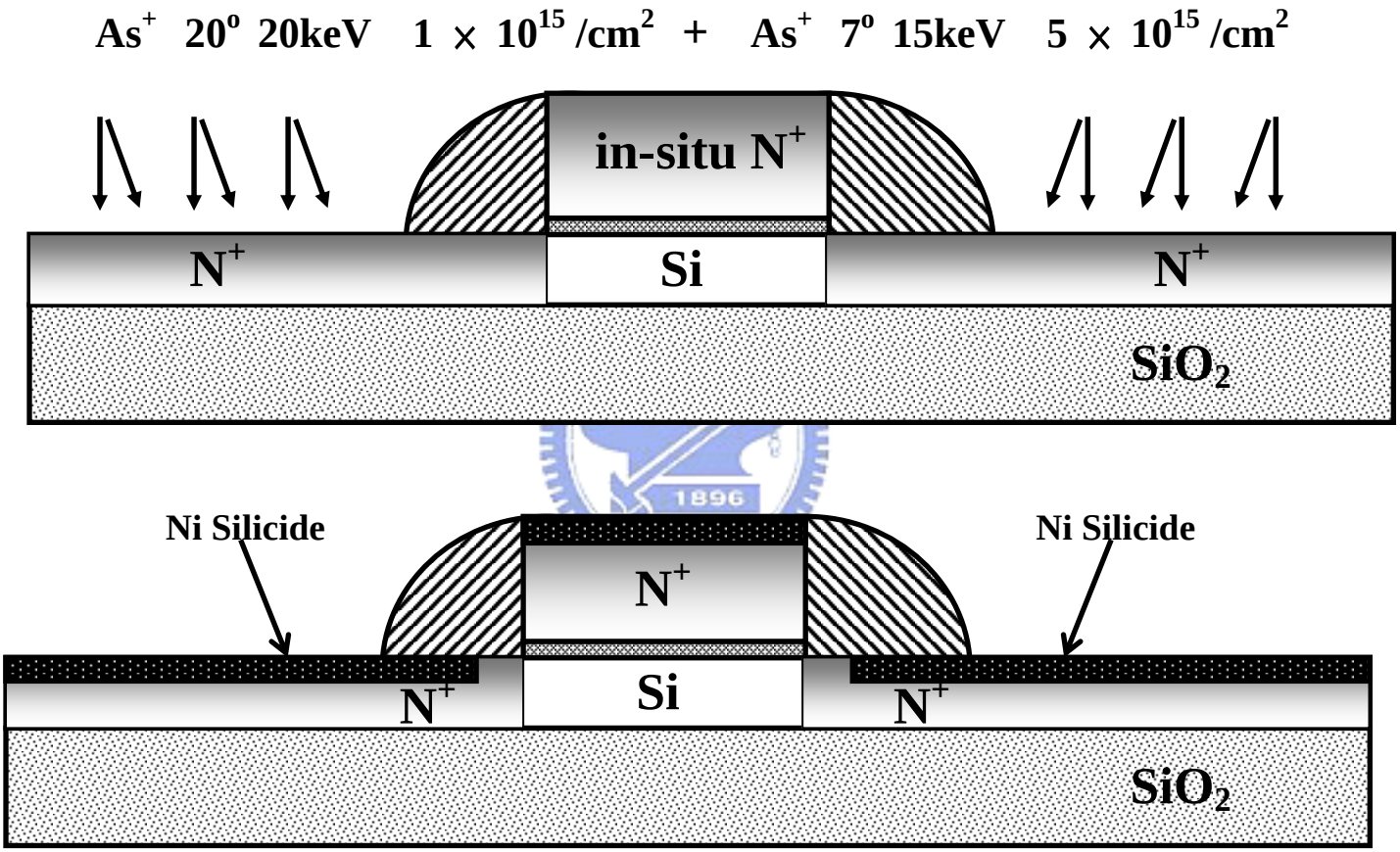


Figure 4.2. The device structure of nano-SOI FinFETs. The gate length is 50nm, and the Si channel thickness is 40nm.

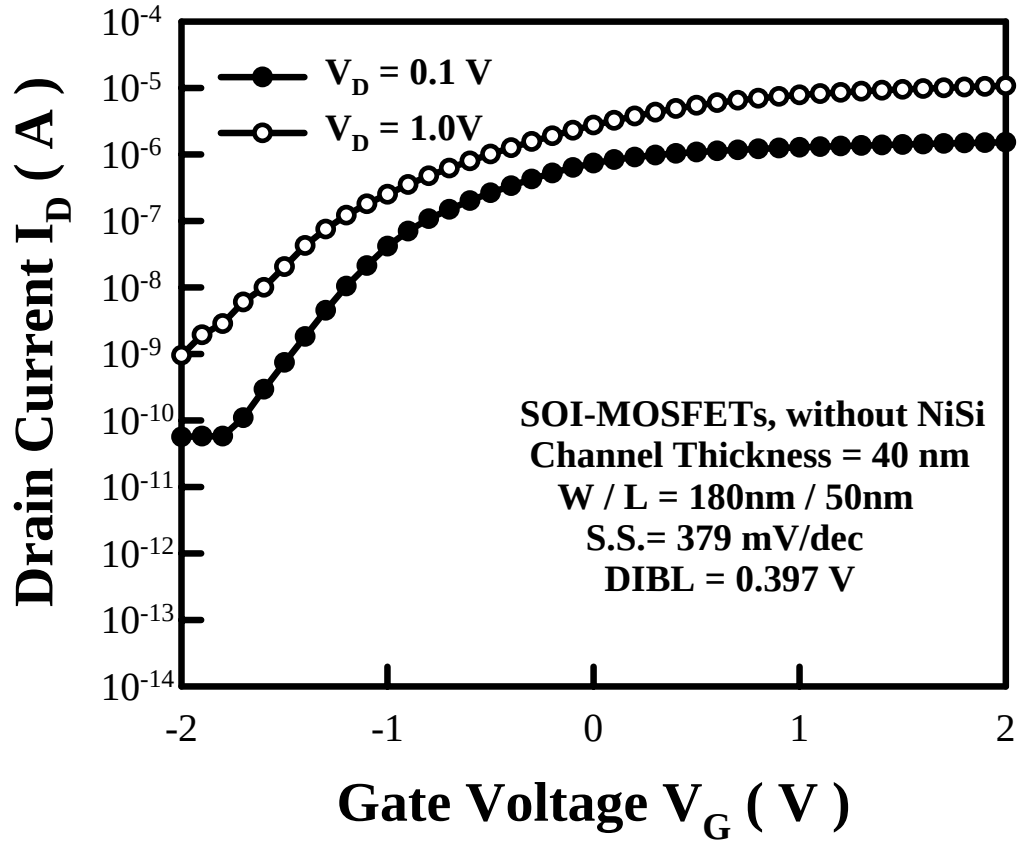


Figure 4.3(a) The measured transistor characteristic of the no Ni-salicided SOI devices with W / L = 180nm / 50nm (SOI MOSFETs).

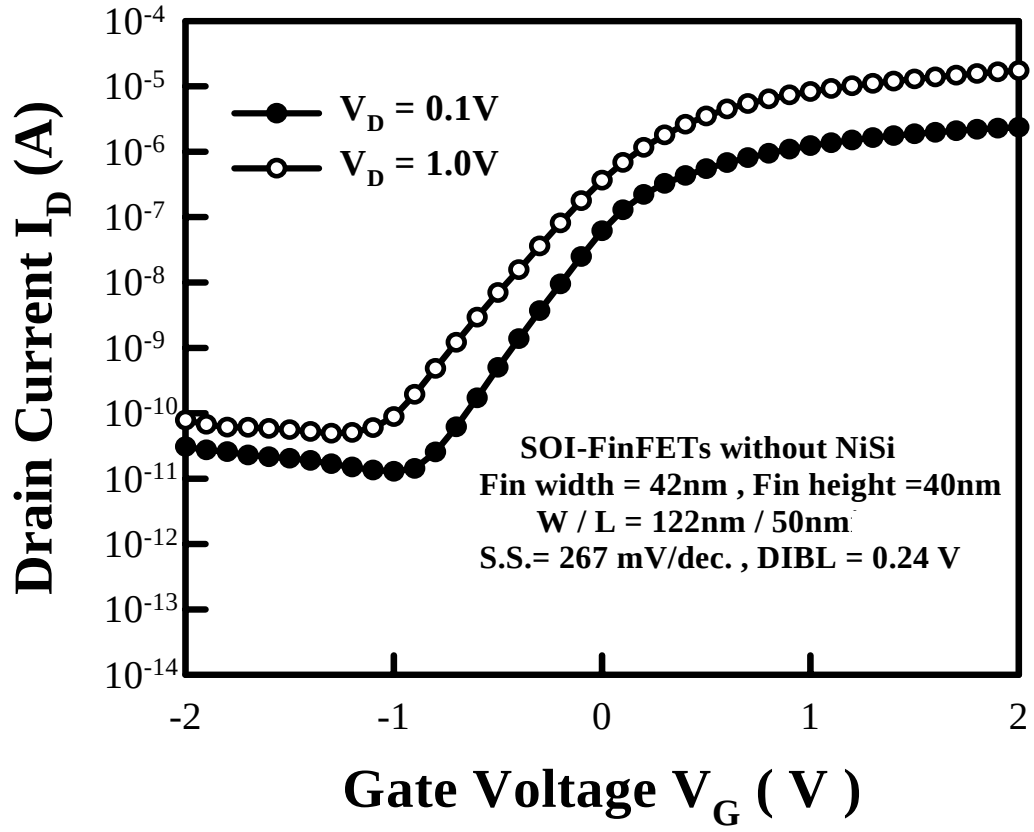


Figure 4.3(b) The measured transistor characteristic of the no Ni-salicided SOI devices with W / L = 122nm / 50nm (SOI FinFETs).

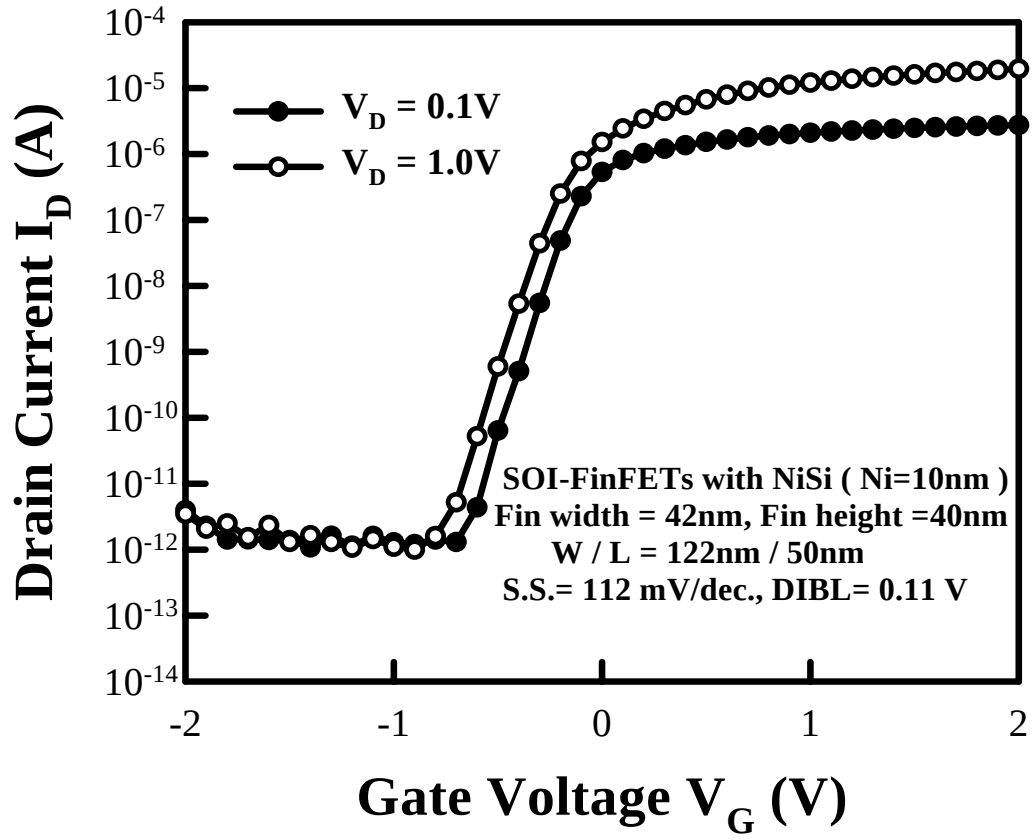


Figure 4.4 The measured transistor characteristic of the deep Ni-salicided SOI FinFETs with W / L = 122nm / 50nm and no plasma treatment.

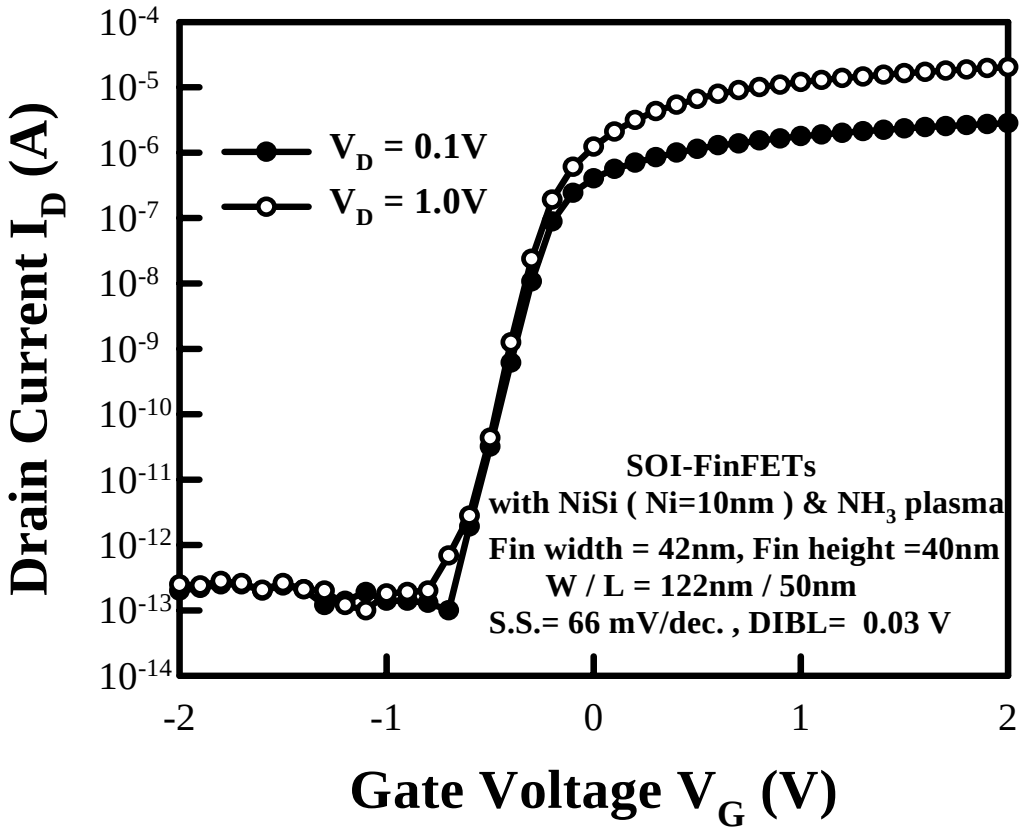


Figure 4.5 The measured transistor characteristic of the deep Ni-salicided SOI FinFETs after state-of-the-art NH_3 plasma treatment with W / L = 122nm / 50nm

Chapter 5

Physical Characterization and Electrical Properties of Sol-Gel-Derived Zirconia Films

5.1 Introduction

Silicon technology has formed the basis of microelectronics and electronics systems for more than 30 years. In terms of productivity, the density of devices on a silicon chip has followed Moore's law, doubling about every two or three years since about 1980. Many researchers are interested in scaling down electronics devices so that they may perform at higher speeds and be prepared at lower costs. Conventional SiO_2 gate dielectrics are reaching their physical thickness limit (1.5 nm); they cannot be used as CMOS devices because the high direct tunneling current and poor reliability. For further scaling of devices, it has been proposed that SiO_2 be replaced by high-k dielectric constant materials, such as ZrO_2, HfO_2, Ta_2O_5, Al_2O_3, TiO_2, and silicates ($ZrSi_xO_y$ and $HfSi_xO_y$) [1–8]. In fact, dielectric films having higher permittivity allow the use of thicker films of equivalent electrical thickness as silicon dioxide; this situation will reduce the leakage current and improve the reliability of the dielectric films.

The most important properties of high-k dielectric materials that are necessary to maintain continuous increases in device performance and density are their low leakage current, low equivalent oxide thickness (EOT), high breakdown strength, high thermal stability, and gate electrode compatibility. The EOT, t_{eq}, of an alternative high-k dielectric employ can be obtained from the simple equation

$t_{eq} = (K_{ox} / K_{high\text{-}k})\, t_{high\text{-}k}$.

Where K_{ox} and $K_{high\text{-}k}$ are the dielectric constants of silicon oxide and the high-k dielectric, respectively, and $t_{high\text{-}k}$ is the physical thickness of the high-k material. Future downscaling will require high-k materials in which EOT values are reduced to nearly 0.7 nm [9]. We must bear in mind that many of the characteristics of these high-k dielectrics—such as their breakdown mechanism and hysteresis phenomena—are quite different from those of conventional silicon dioxide. When the gate dielectric materials experience high-temperature conditions (> 800 °C), the thermal stability of the high-k dielectric on silicon is an important issue that must be addressed for future MOSFET devices. The most suitable range of dielectric constants is between 20 and 40. If the material has an extremely high k-value (> 80), it will induce a large fringing effect. For the purposes of achieving a low leakage current, it is desirable to choose a dielectric material that possesses a large band gap energy and a large band offset with respect to the Si substrate. ZrO_2 has a dielectric constant of 25, a wide band gap, good thermal stability, a high hardness, a high melting point, chemical hardness, and a high refractive index.

Recently, numerous technologies have been developed for the preparation of various high-k films [10-13]. To prepare insulating thin films, atomic layer deposition (ALD), physical vapor deposition (PVD), and chemical vapor deposition (CVD) methods have all been used to prepare films for new technologies. In the ALD process, $ZrCl_4$ and H_2O are used to prepare the ZrO_2 films. For the PVD process, a zirconium metal target is used for sputtering under ambient oxygen to deposit the ZrO_2 films. In the CVD method, $ZrCl_4$ precursor is used to deposit ZrO_2 films. The sol–gel method is a very interesting simple technique for preparing ceramic films [14-18].

The sol–gel method can provide colloidal solvents or precursor compounds when metal halides are hydrolyzed under controlled conditions [18]. In the sol–gel

process, hydrolysis, condensation, and polymerization steps occur to form metal oxide networks. These reactions play fateful roles in modifying the final material's properties. The most interesting feature of sol–gel processing is its ability to synthesize new types of materials that are known as "inorganic–organic hybrids." The film formation with spin-coating is a simple method than ALD, PVD or CVD due to its cheaper precursor and tool. In addition, the film can be fabricated in the normal pressure system instead of high vacuum system. Typically, ZrO_2 is an excellent heat-resistant and chemically durable material that is used, for example, as a material for furnaces [19]. Although ZrO_2 generally provides good electrical insulation, no reports exist that describe the electrical insulation properties of sol–gel-derived ZrO_2 ultrathin film.

In this paper, we used the different annealing conditions on the sol–gel ZrO_2 ultrathin films on silicon. The resulting material properties and electrical performance of these deposited films were also evaluated by various characterization techniques.

5.2 Experimental

We studied these properties using atomic force microscopy (AFM), electron spectroscopy for chemical analysis (ESCA), X-ray diffractometry (XRD), thermal desorption spectrometry – atmosphere ionization mass spectrometry (TDS-APIMS), and high-resolution transmission electron microscopy (HRTEM), and performed capacitance–voltage (C–V) and current density–voltage (J–V) analyses.

ZrO_2 thin films were prepared using a sol–gel spin-coating method. $ZrCl_4$ (99.5%, Aldrich, USA) was used as the precursor for the synthesis of zirconia. Prior to the film fabrication, the purity of $ZrCl_4$ was checked with the inductivity couple plasma optical emsssion spectrometry. Except for the Zr signal, the impurity was lower than

1000ppm. The thin films were prepared through polymerization in an organic solution. A mother sol solution was first prepared by dissolving $ZrCl_4$ in isopropanol (IPA; Fluka; water content < 0.1%) and hexanol (Fluka, water content < 5%) under vigorous stirring in an ice bath. The sol solution was obtained by fully hydrolyzing $ZrCl_4$ with a stoichiometric quantity of water in IPA and hexanol to yield a Zr:IPA:hexanol molar ratio of 1:500:1000. The metal halide solution was then subjected to ultrasonication at 0 °C for 20 min to accelerate the gelling rate. The film thickness was determined from the ellipsometer.

The n-Type wafers (10-15 Ω-cm, made in Japan), which were used as substrates for the metal insulator semiconductor (MIS) structure, were RCA cleaned to remove the native silicon oxide. ZrO_2 films were deposited by spin-coating at 3000 rpm for 60 s at ambient temperature (25 °C) to give a thickness of ~9.3 nm on the n-Si(100) substrate. The spin-coater used was TEL Clean Track Model-MK8 (Japan). These films were initially baked at 200 °C for 10 min. One of the samples was then maintained at 200 °C for 1 min for densification; the others were rapid thermal annealed (RTA) at different temperatures (500, 600, or 900 °C) for 1 min under an oxygen atmosphere. ZrO_2/n-Si structures were used in our experiments for the physical characterization of the zirconia.

Next, Al top electrodes having an area of 7.85×10^{-5} cm^2 were deposited onto the top surface of the ZrO_2 by using a shadow mask and vaporizing a pure Al target. The thickness of the top electrode was 400 nm. A buffered oxide etch (BOE) was performed to remove the silicon back oxide and then the sample was thoroughly rinsed with deionized water. Finally, bottom electrodes were attached on the reverse side of the n-Si (100) substrates by vaporizing a pure Al target. The thickness of the bottom electrode was 100 nm. The dielectric properties were then determined for the MIS capacitors having an Al/ZrO_2/n-Si/Al structure. Figure 5.1 displays the main

process flow for the sample preparation. Al/ZrO_2/n-Si MIS capacitors were used in our experiments to determine the electrical properties of the zirconia. This deposition technique allows the production of very ultrathin gate dielectric films under excellent thickness control.

5.3 Results and discussion

The thickness of smooth ZrO_2 films as a function of the Zr/hexanol ratios is displayed in Figure 5.2 During the sol–gel process, the IPA solvent is more hydrophilic than hexanol. For this reason, we fixed the mole ratio of the IPA solvent with respect to the Zr ions at 1/500 ($ZrCl_4$:IPA). We varied the hexanol content to provide various film thicknesses. The film thickness increased linearly upon decreasing the Zr/hexanol ratio from 1/1000 to 1/750 to 1/500 to 1/250. We obtained a smooth nano-film (thickness: 9.3 nm) at a Zr/hexanol ratio of 0.001. Prior to annealing, the real thicknesses of the smooth films obtained at Zr/hexanol ratios of 1/750, 1/500, and 1/250 were 10.7, 12.6, and 22.5 nm, respectively. The semi-impirical fitting between the thickness and Zr/hexanol ratio can be expressed as thickness T (nm) = 4.55 + 4425.90 × (Zr/hexanol) and the correlation coefficient R^2 = 0.9919. This linear observation suggests that the film thickness is controllable and tunable by the Zr/hexanol ratio.

Figures 5.3a, 5.3b and 5.3c display cross-sectional TEM images of the interfaces of the ZrO_2/Si structures annealed at 200, 600 and 900 °C, respectively. The TEM image and its diffraction pattern in Fig 5.3a indicate that the sol–gel-deposited film consists of a ~0.82-nm-thick interfacial layer (Zr-silicate) [9, 11] and a 9.3-nm-thick bulk ZrO_2 film, and the ZrO_2 is exhibited as amorphous structure from the diffraction pattern. Very smooth interfaces exist in the sample. If we increase the annealing

temperature to 600 and 900 ^{o}C in Figs. 5.3b and 5.3c, the intefcaces are also smooth. The ZrO_2 film is still amorphous structure.

The surface morphology of the ultrathin film plays an important role in defining its further electrical and mechanical properties. Figures 5.4a–d display the AFM images of the sol-gel-derived ZrO_2 films. The as-deposited (200 °C) sample possessed a whole area film RMS roughness of 0.306 nm (Figure 5.4a). After annealing at 500, 600, and 900 °C under ambient oxygen for 1 min, the RMS roughnesses were 0.157, 0.165, and 0.189 nm, respectively. The value of surface roughness of the as-deposited ultrathin film is very low by spin-coating method, and these films become more smoothness after annealing treatment. We have chosen five different regions for each sample to determine the roughness, and found the annealing samples are still smooth.

Next, we investigated the ZrO_2 crystallinity using 1.5^{o} glancing-angle XRD. High-k dielectric crystallinity is a concern because of the possible problems arising from leakage paths and dopant/impurity diffusion along grain boundaries, as well as for the control of device uniformity. The XRD patterns of the ZrO_2 films in Fig. 5.5 grown on silicon over the temperature range 200–900 °C indicate the morphology of the sol–gel-derived ZrO_2. Broad features are present for the as-deposited film and they do not change significantly upon annealing at up to 900 °C; these results, together with the diffraction pattern from Fig. 5.3, clearly identify the amorphous phase of the sol–gel-derived ZrO_2 films and suggest that they have high thermal stability. The treatment with RTA at 900 °C for 1 min under oxygen atmosphere still can prevent the ZrO_2 crystallization. This phenomenon is related to the preparation solvent and $ZrCl_4$ precursor. This amorphous structure is beneficial for the electrical property than crystallization.

To determine the bulk properties of the deposited films, we used ESCA to examine the nature of the chemical bonding structures of these films. From the Zr 3d

spectrum of the RTA samples in Fig. 5.6a, we observed clearly two typical peaks—Zr $3d_{5/2}$ (183.2 eV) and Zr$3d_{3/2}$ (185.6 eV)—of ZrO_2. RTA annealing under O_2 at 500, 600, and 900 °C for 1 min led to remarkable changes in the ESCA spectra (Fig. 5.6a). This change, which is apparent from the increase in the signal of the Zr–O bonds upon increasing the annealing temperature. The as-deposited zirconia film is mainly $ZrO_{2-\delta}$ ($\delta \geq 0$), while the annealing under oxygen ambient can decrease the δ value. This finding indicates that structural composition of the ZrO_2 has occurred [8]. The electron binding energy of C 1s orbital is 284 eV, and increases to 286.5 eV as if Cl bound to C in Fig. 5.6b [20]. The C and Cl are both come from the precursor or the preparation solvents. The annealing at 900 ^{o}C in the oxygen environment effectly reduces the C-Cl signal, as depicted from Figs. 5.6b and 5.6c. This observation suggests the annealing treatment is beneficial for enhancing the film quality and improving the electrical property.

The surface of these samples was sputtered away with 2kV argon for ESCA analysis (Scanning X-ray Microprobe, Quantera SXM^{TM}, ULVAC). Each sample was then eroded ~7 nm from the surface. In the Fig. 5.7, a Si 2p peak corresponding to the binding energy of SiO_2 (103.3 eV) appears in the spectra of the RTA samples, and a Si 2p peak at 99.3 eV (Si–Si bonds) is visible [8]. It is obviously that the 99.3 eV peak represents the silicon substrate. We find that the peak representing the Si–O bonds in the annealed thin films increases upon increasing the annealing temperature (Fig. 5.7). This finding also consists with the observation in above TEM images in Fig. 5.3 The color in the interface region (ZrO_2/Si) becomes light as increasing the annealing temperature. This finding suggests that Zr silicate in the interface lead to phase separation at 900 ^{o}C, forming an amorphous SiO_2 [8].

As mentioned early, the C-Cl bond is existed in the ZrO_2 film, and the annealing at 900 ^{o}C in the oxygen environment can reduces it. In order to verify this observation,

these samples were analyzed by TDS-APIMS measurements. We ramped the desorption temperature of the TDS-APIMS system from room temperature to 800 °C at 20 °C/min under a N_2 carrier gas. We analyzed the surface out-gasses at molecular weights of 16, 44, and 82 (Figs. 5.8a–c). The film basically comprises Zr, Cl, C, H, and O elements from the preparation solvents and precursor. The out-gassing molecular weights of 16 and 44 possibly represent carbon elements combined in the forms of CH_4 and CO_2 molecules. Likewise, the chlorine component combines with C and other Cl atoms to form CCl_2. We find that the organic elements dissipate violently around 400 °C for all of the samples. As the annealing temperature increases, the intensity of TDS-APIMS desorption peak gradually reduced. This result suggests the oxygen treatment at higher temperature is benefical for the separation of unstable carbon-containing compounds from the sol-gel fabricated ultrathin film.

Figure 5.9 illustrates the high-frequency (1 MHz) capacitance versus gate voltage characteristics (C–V curves) for the MIS capacitors prepared from sol–gel-derived ZrO_2 dielectrics under the various annealing conditions. For a high-k dielectric material, a high-frequency C–V characteristic is a very important measurement for calculating the equivalent oxide thickness (EOT). From Figure 9a, we find that the C–V curve of the sample annealed at 500 °C is poor; several steps exist in the curve, which is not very stable. In other words, the sample annealed at 500 °C does not appear to have excellent electrical properties because of the unstable organic compounds still present in the film. This observation is convinced with the finding in Figs. 5.6b and 5.8a. When we raised the annealing temperature up, the ZrO_2 films exhibited good electrical properties: low current density and better capacitance ability. Figure 5.9b provides detailed information for the sample annealed at 600 °C. The value of the capacitance of the RTA 600 °C sample was 390 pF and the capacitor appears to be very stable. Table 5.1 lists the C–V characteristics of the RTA 600 °C

sample, which has an EOT value of 3.04 nm and a dielectric constant of 13.9. In addition, Figure 5.9b displays hysteresis in the C–V characteristics of the samples without light illumination. The solid line represents the C–V characteristics for measuring the curve by sweeping the voltage from accumulation to inversion and sweeping back (from +2.0 to –2.0 to +2.0 V); we observe that the shift is only 35 mV. This observation is attributed the reduction of unstable carbon-containing compounds after annealing.

The capacitance of the film annealed at 900 °C under an O_2 atmosphere is 310 pF (Fig. 5.9c). Thus, the capacitance of the RTA 900 °C sample is lower than that of the RTA 600 °C sample. From the ESCA signals of these samples, we find that the intensity of the peak for the Si–O bond in the annealed thin film increased upon increasing the annealing temperature (see Fig. 5.7). The interfacial oxide (SiO_2) influences the capacitance ability and the EOT, which is unfavorable property. Nevertheless, the sol–gel-derived ZrO_2 films annealed at 900 °C display an improved breakdown field (>12 MV/cm^2) from Fig. 5.10 Table 5.1 lists the C–V characteristics of the sample annealed at 900 °C; the EOT value is 3.91 nm and the dielectric constant is 12.8. We observe that as the annealing temperature increases, the EOT increases (from 3.07 to 3.91 nm) and the dielectric constant decreases (from 13.9 to 12.8). The solid line in the inset of Fig. 5.9c represents the C–V characteristic for measuring the curve by sweeping the voltage from accumulation to inversion and sweeping back (from +2.0 to –2.0 to +2.0 V). We observe a shift of 20 mV for the hysteresis phenomenon for the sample annealed at 900 °C. Thus, the hysteresis phenomenon is lower than the dielectrics of the sol–gel-derived ZrO_2 film annealed at 600 °C.

The electric field (E) in the J–E curve of Fig. 5.10 is obtained by using the equation $E = V/t_{ox}$, where V is the applied voltage and t_{ox} is the EOT determined

through C–V measurement. The samples annealed at 200 and 500 °C did not have sufficiently high thermal budgets and so their breakdown electric fields were relatively low. The breakdown electric fields increased upon increasing the annealing temperature. A high annealing temperature leads to remove the unstable carbon-containing compounds from ZrO_2 film and stabiliz the thin film. It should be noted that the sol–gel-derived ZrO_2 displays excellent electrical performance even after high-temperature annealing up to 900 °C. It is attributed that the ZrO_2 films do not crystallize during their high-temperature RTA treatment. In addition, the samples subjected to RTA treatment at 600 and 900 °C displayed the lowest leakage current densities ($<10^{-7}$ A/cm^2) than the literature report [8, 11].

Thin layers of zirconium dioxide that are used as a dielectric for capacitors or as a gate oxide for MIS devices are subject to a mechanism known as time dependent dielectric breakdown (TDDB). This mechanism causes the dielectric to break down and electrically short after a certain duration of operation. The expected lifetime of a thin gate oxide under normal operating conditions should be several million years. Figure 5.11 displays a projected lifetime operation of ~1.1 MV/cm for the Zr + IPA + hexanol RTA 500 °C sample (5 replicates for each point). The projected lifetime operation of the Zr + IPA + hexanol RTA 600 °C sample is ~2.1 MV/cm and that of the Zr + IPA + hexanol RTA 900 °C sample is ~10.4 MV/cm. In this Figure, we observe a large increment in the projection voltage for the 10-year lifetime when the Zr + IPA + hexanol sample was annealed at 900 °C. This result occurs because the high annealing temperature stabilizes the ZrO_2 film.

5.4 Summary

We have proposed an attractive sol–gel method for preparing ultrathin films due

to the advantages of low cost, and better thermal and electrical properties. The sol–gel method requires a lower degree of processing and provides highly homogeneous materials and the possibility of using annealing process to stabilize the film. We have prepared ZrO_2 ultrathin films of an amorphous phase by using the sol–gel method with $ZrCl_4$ as the metal halide. The electrical properties of the ZrO_2 thin films not only display their good electrical insulation with breakdown field up to 12.5 MV/cm, but also their improved thermal stability up to 900 ^oC against the crystallization. These ZrO_2 ultrathin films are readily produced by the sol–gel method and behave as suitable capacitors and coatings for insulating films.

Table 5.1. Properties of the films annealed at 600 and 900 °C.

Heat treatment condition	Dielectric constant (K)	EOT (nm)
Zr +IPA+ hexanol, RTA 600 °C, 1 min	**13.9**	**3.04**
Zr +IPA+ hexanol, RTA 900 °C, 1 min	**12.8**	**3.91**

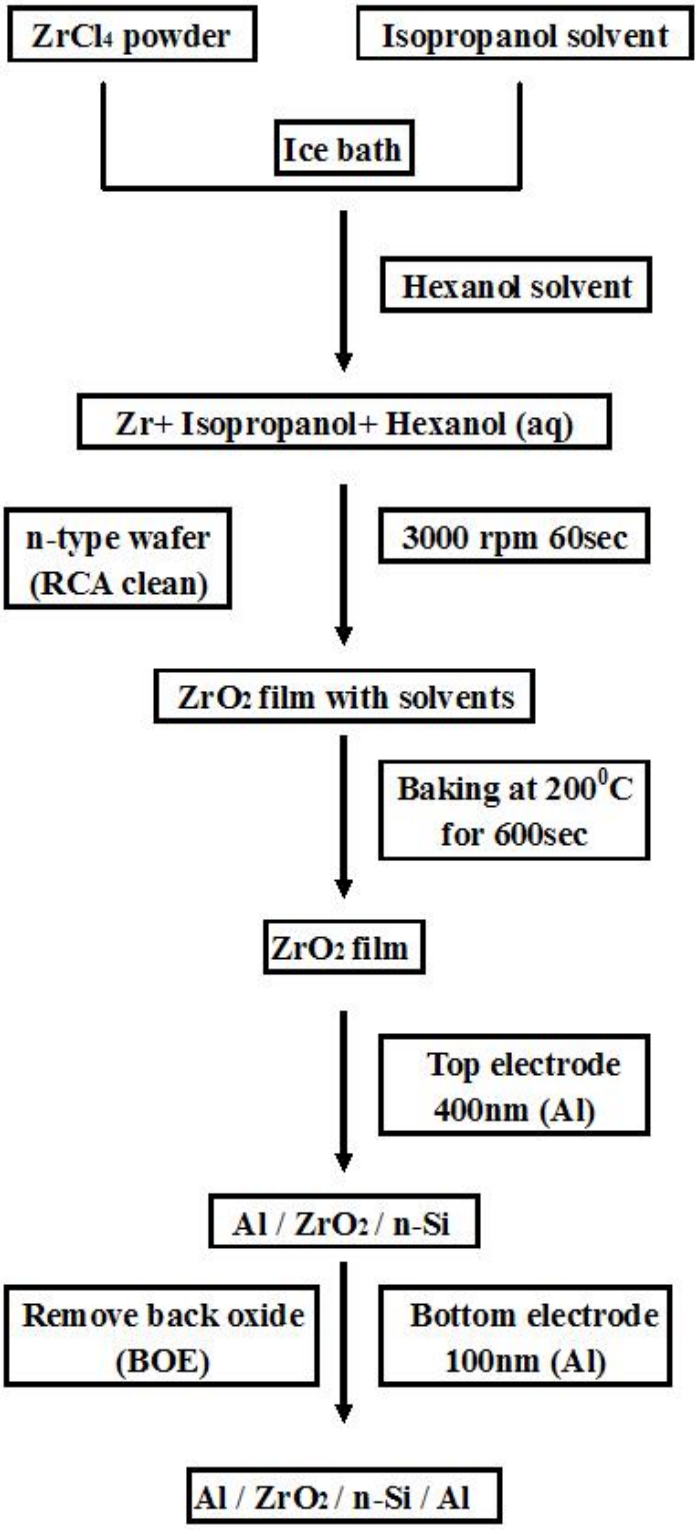


Figure 5.1 The sol–gel process used for the preparation of the ZrO_2 films.

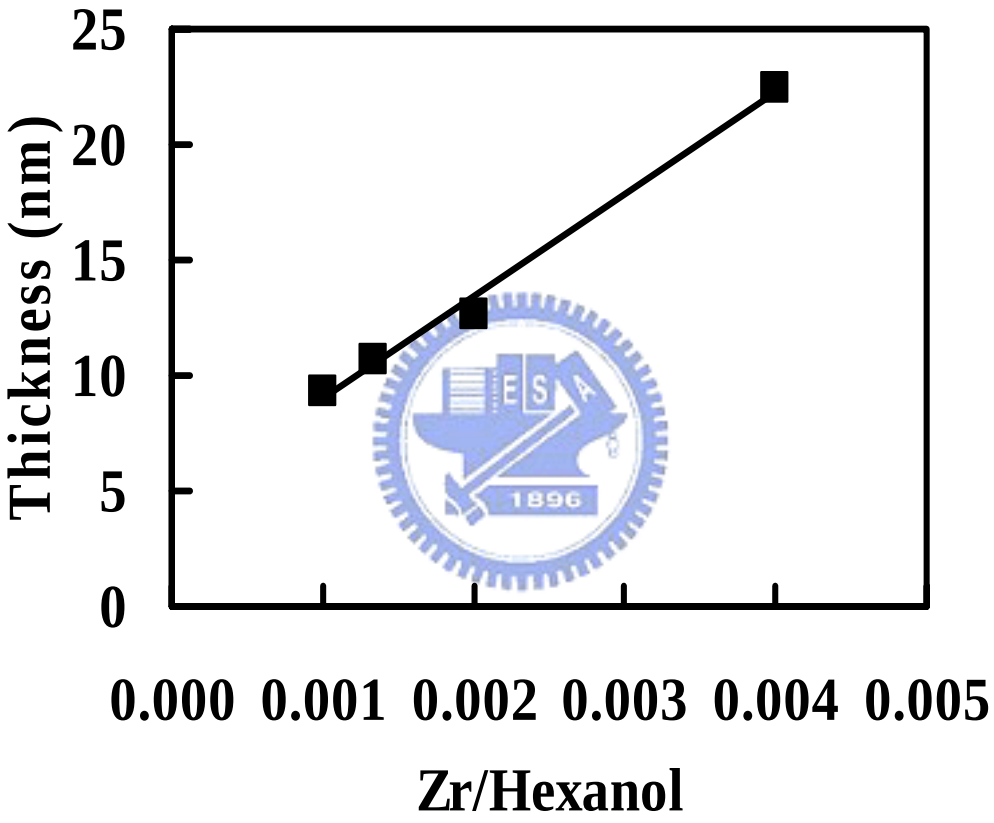


Figure 5.2 The film thickness of sol–gel-derived ZrO_2 films plotted as a function of the Zr/hexanol ratio.

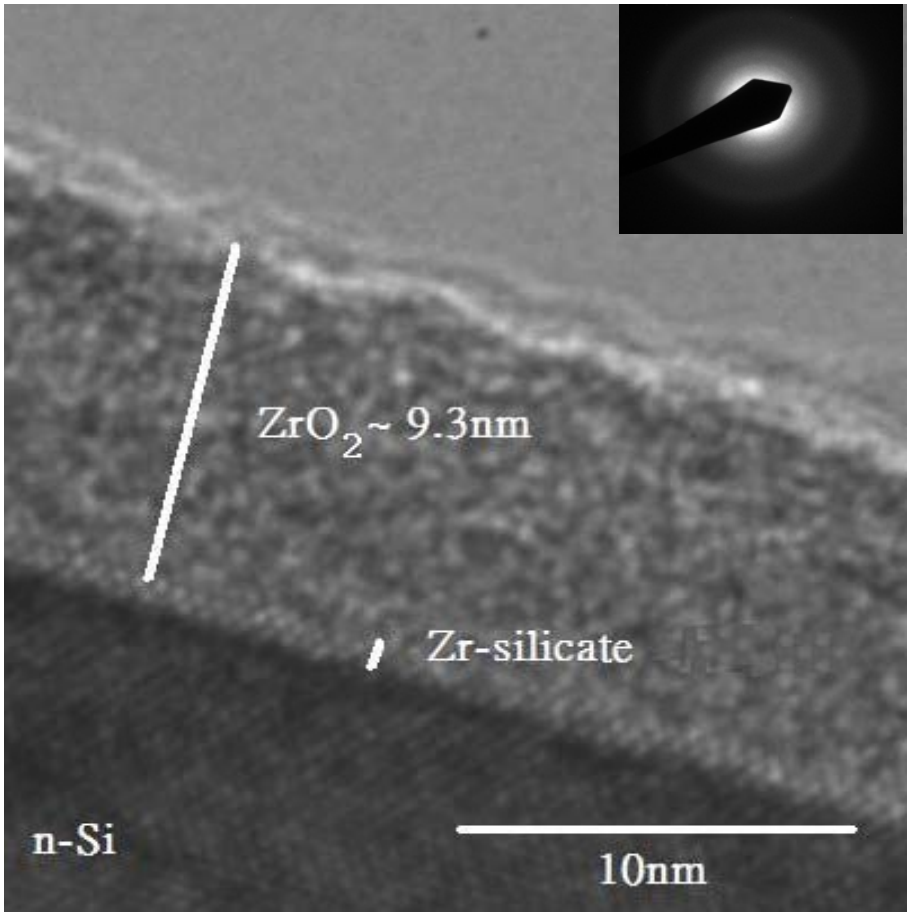


Figure 5.3 Cross-sectional TEM images of sol–gel-derived (Zr + IPA + hexanol) ZrO_2/Si structures annealed under an O_2 atmosphere at (a) 200 °C.

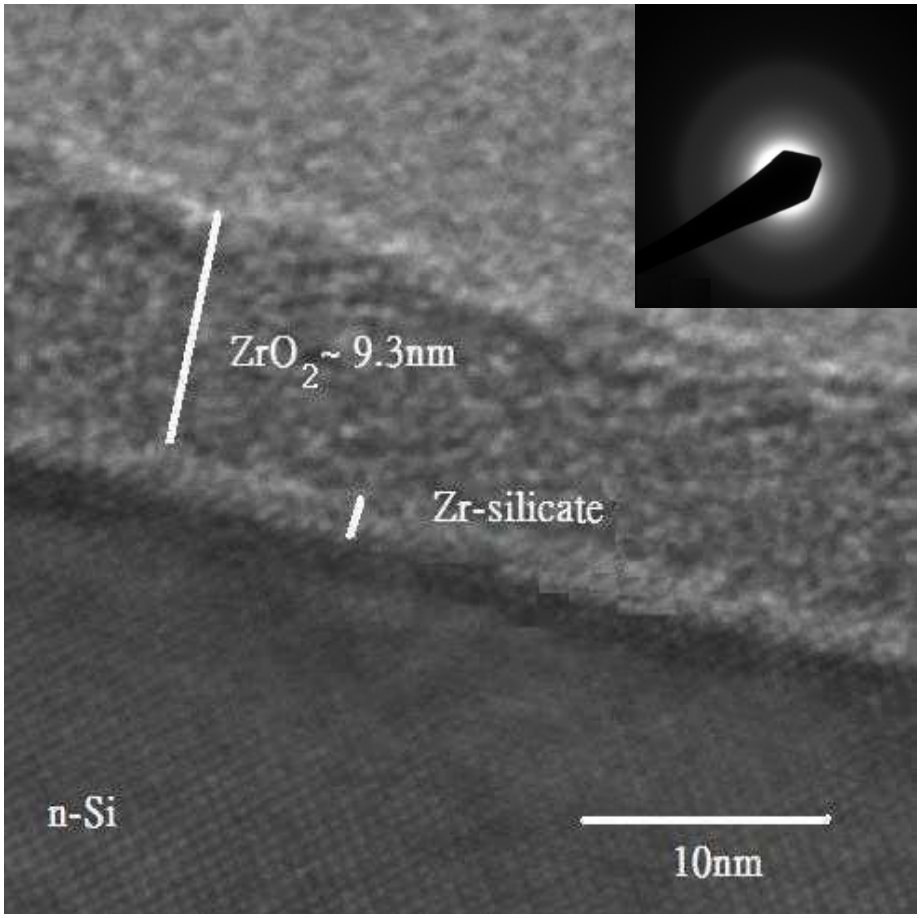


Figure 5.3 Cross-sectional TEM images of sol–gel-derived (Zr + IPA + hexanol) ZrO_2/Si structures annealed under an O_2 atmosphere at (b) 600 °C.

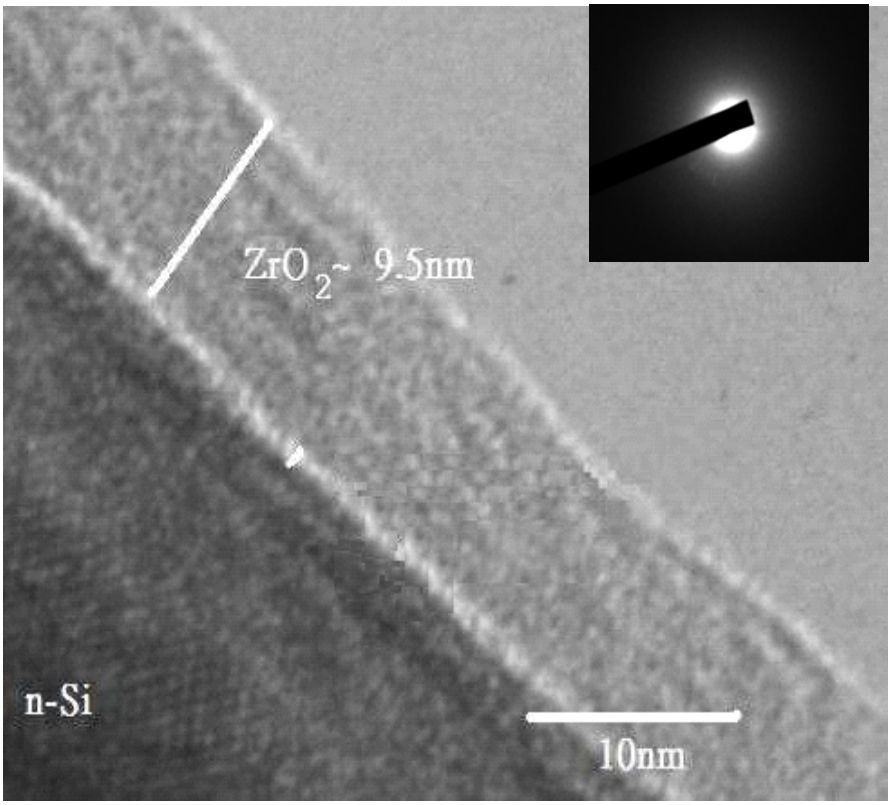


Figure 5.3 Cross-sectional TEM images of sol–gel-derived (Zr + IPA + hexanol) ZrO_2/Si structures annealed under an O_2 atmosphere at (c) 900 °C.

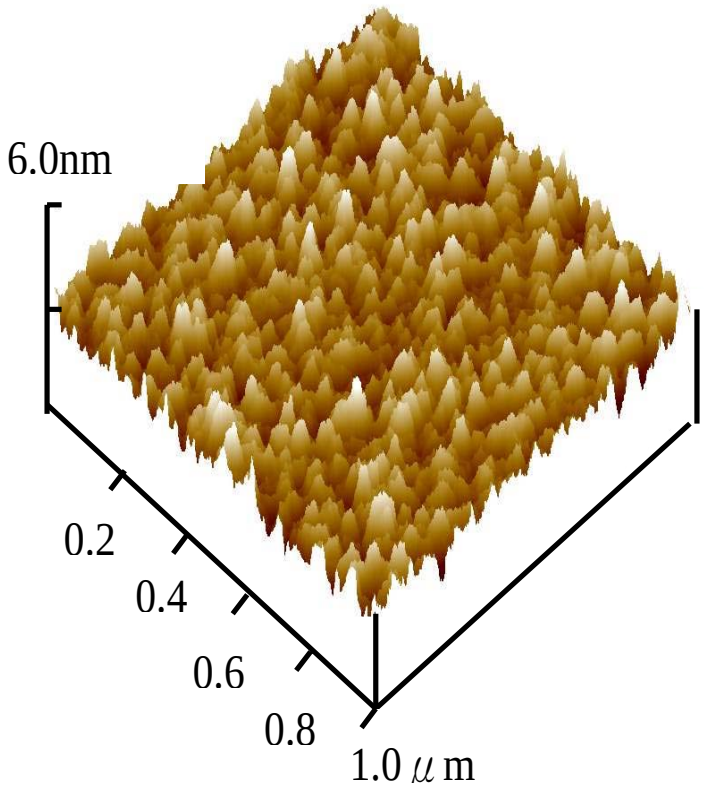


Figure 5.4 AFM images of the ZrO_2 thin films prepared at different temperatures. (a) 200 °C. These images were recorded using a scanning speed of 1 lateral scanning line/second, 256 × 256 data points, and a scanning area of 1 μm^2.

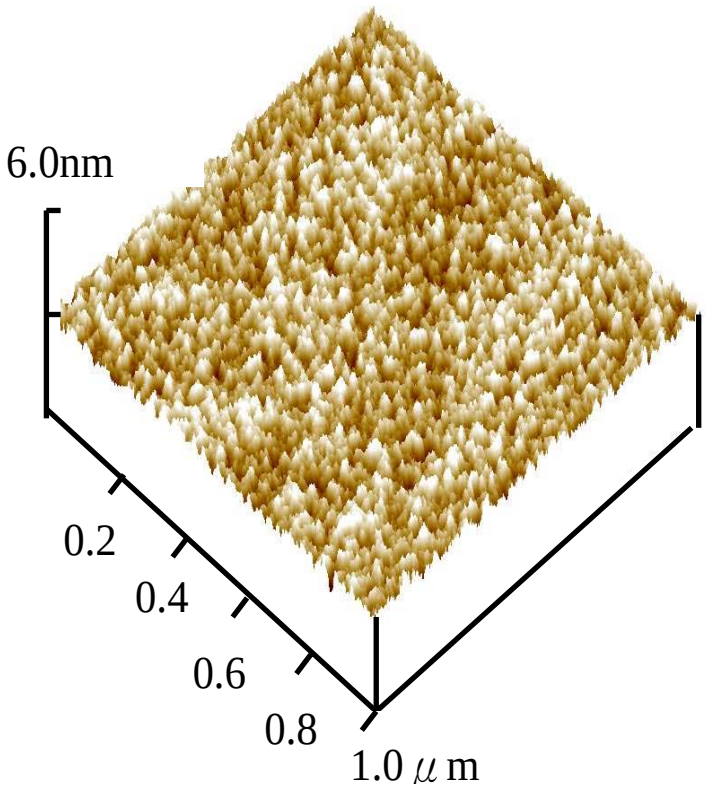


Figure 5.4 AFM images of the ZrO_2 thin films prepared at different temperatures. (b) 500 °C. These images were recorded using a scanning speed of 1 lateral scanning line/second, 256 × 256 data points, and a scanning area of 1 μm^2.

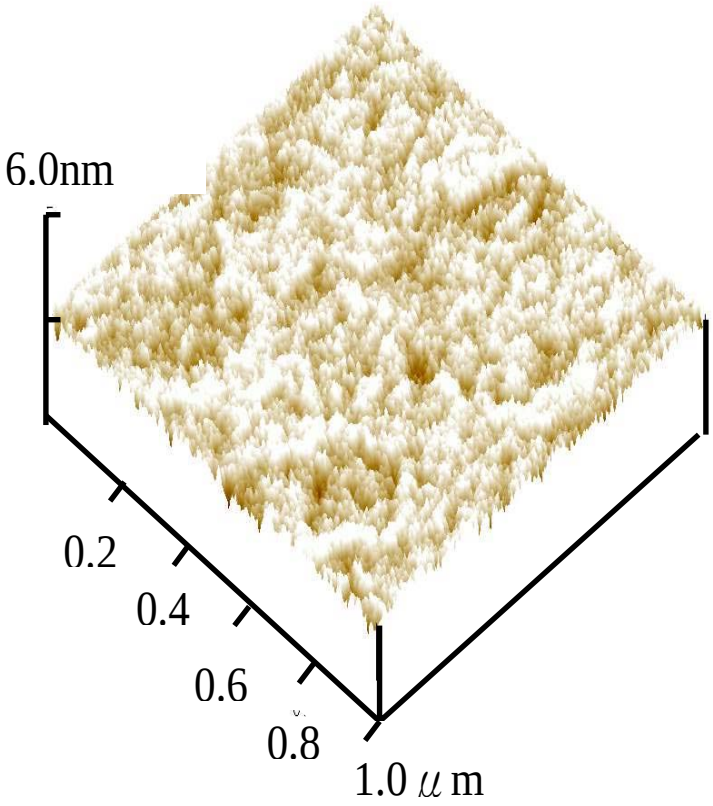


Figure 5.4 AFM images of the ZrO_2 thin films prepared at different temperatures. (c) 600 °C. These images were recorded using a scanning speed of 1 lateral scanning line/second, 256 × 256 data points, and a scanning area of 1 μm^2.

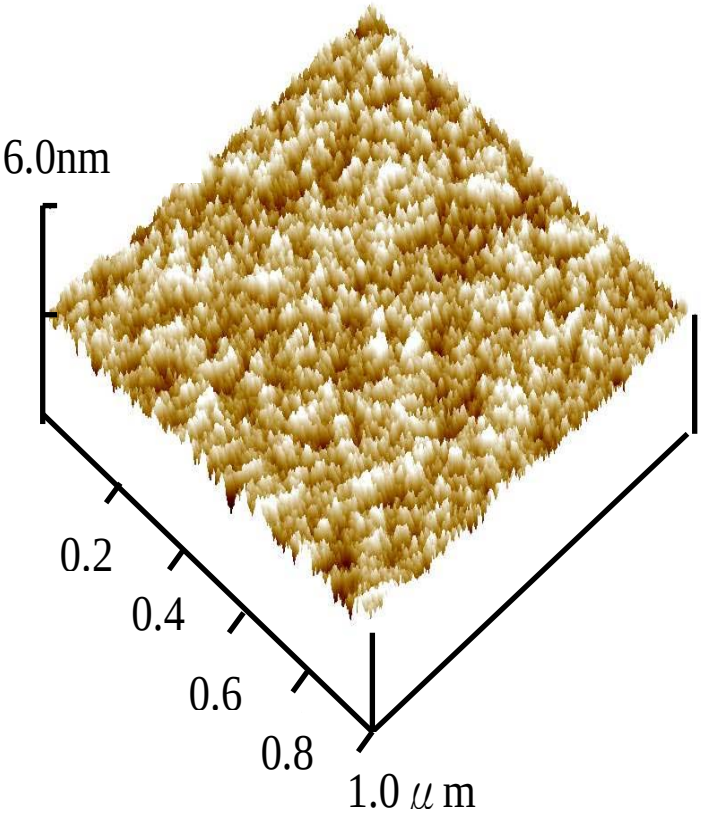


Figure 5.4 AFM images of the ZrO_2 thin films prepared at different temperatures. (d) 900 °C. These images were recorded using a scanning speed of 1 lateral scanning line/second, 256 × 256 data points, and a scanning area of 1 μm^2.

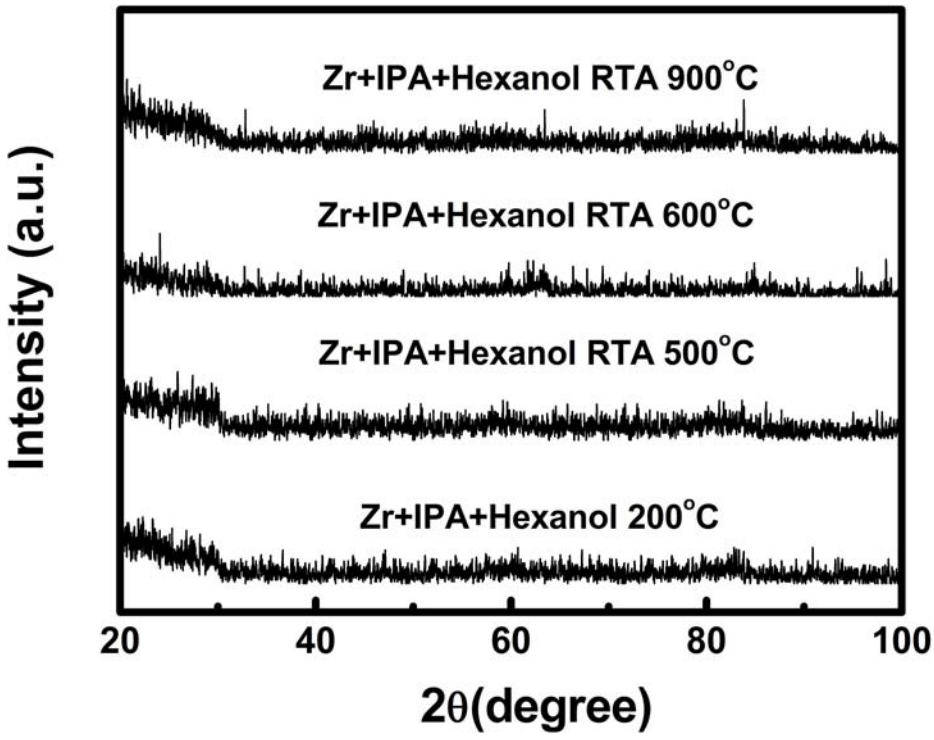


Figure 5.5 XRD data for ZrO_2 films of different conditions, as deposited and after annealing at the temperatures indicated.

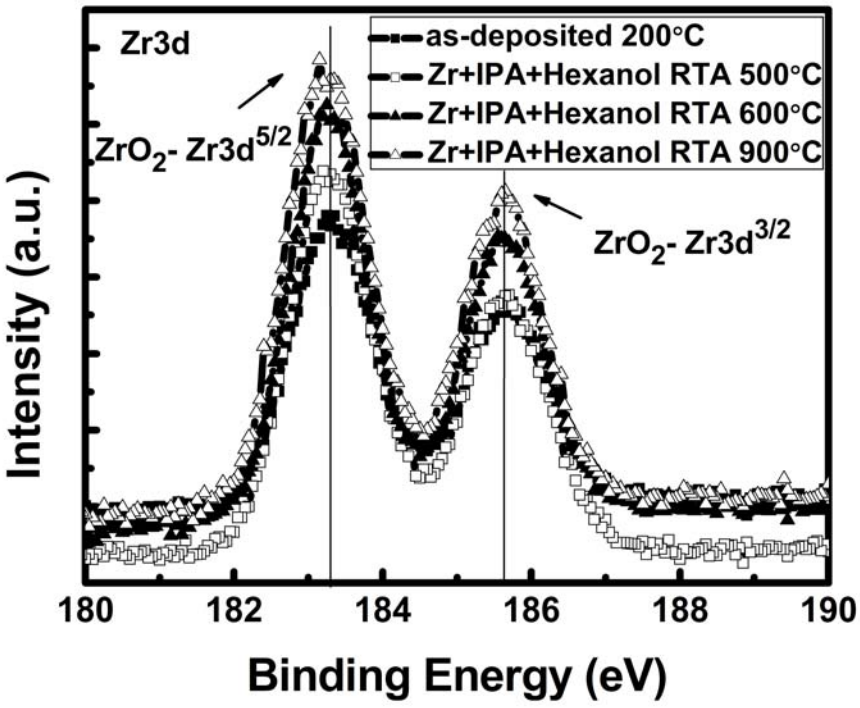


Figure 5.6 (a) ESCA spectra of ZrO_2 films as-deposited and RTA annealing at 500ºC, 600 ºC, and 900^0C in O_2 for 1min (Zr 3d).

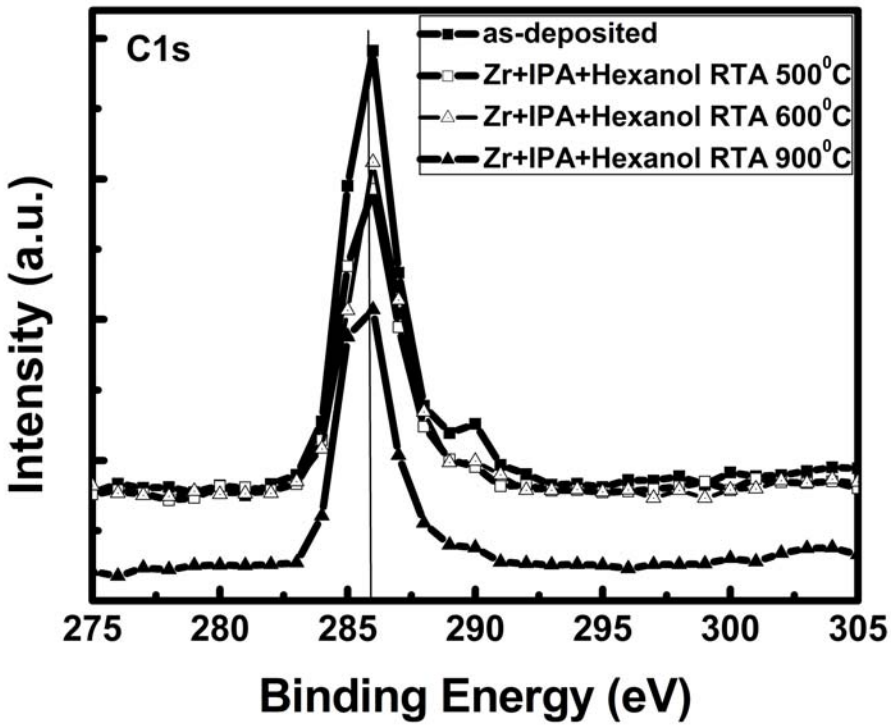


Figure 5.6 (b) ESCA spectra of Cl element vary at different annealing conditions.

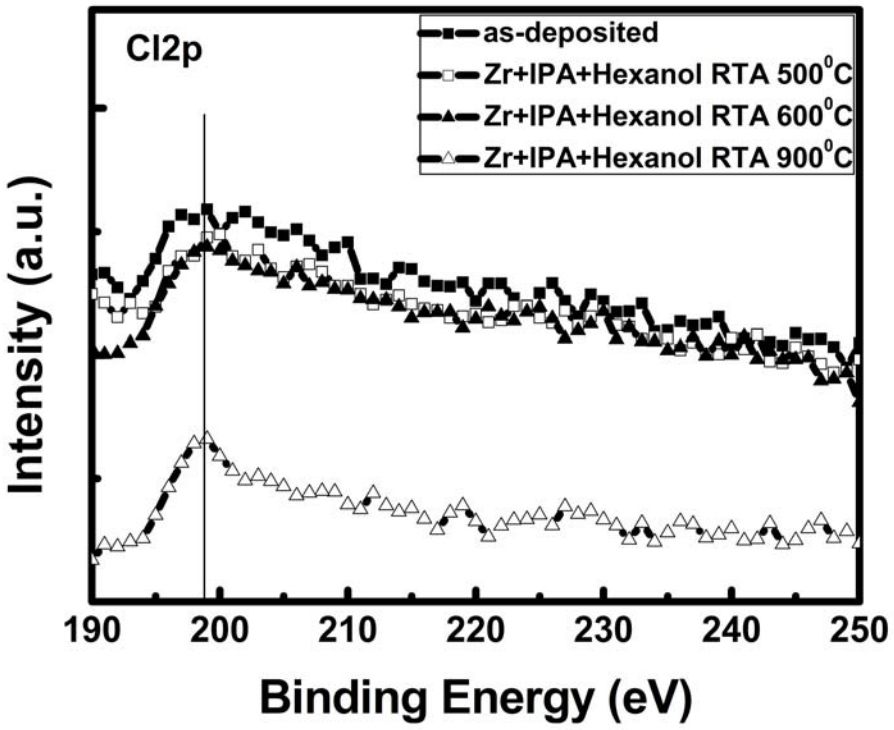


Figure 5.6 (c) ESCA spectra of C element vary at different annealing conditions.

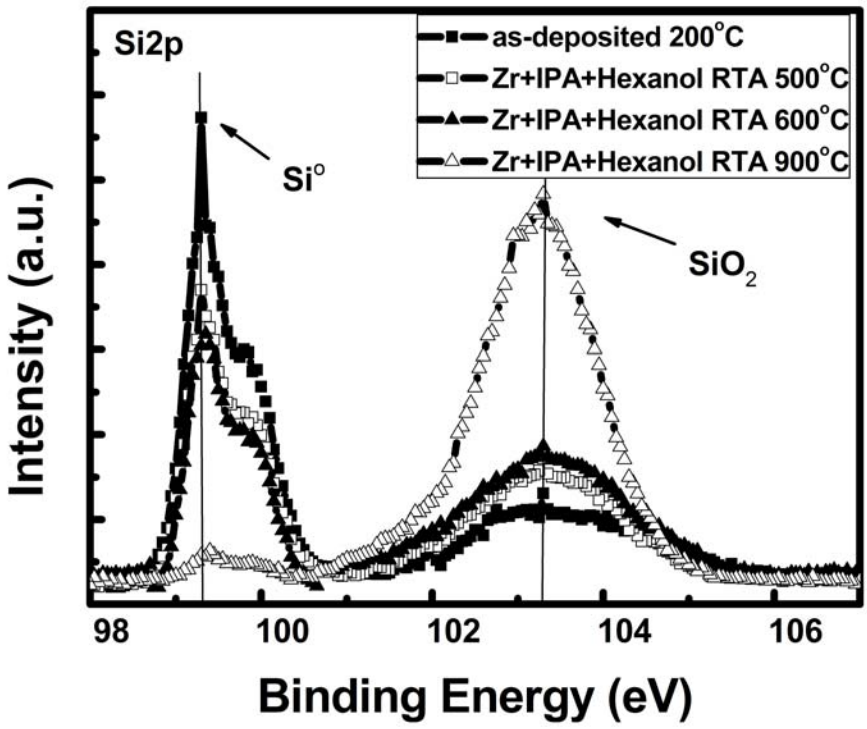


Figure 5.7 ESCA spectra of Si 2p of ZrO_2 films eroded ~7 nm by argon sputter.

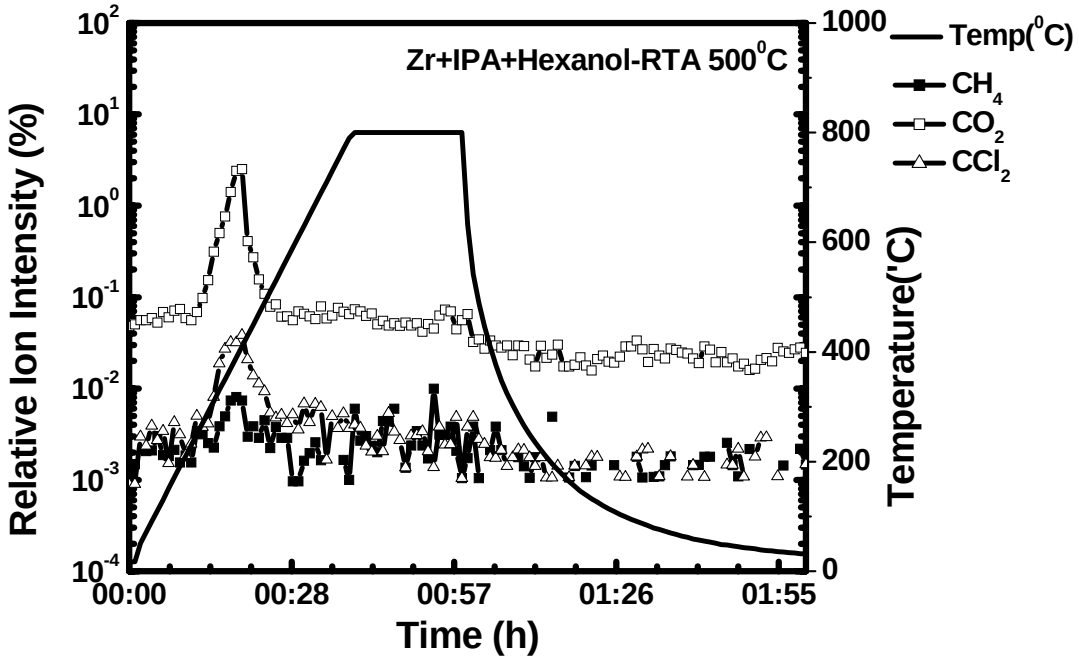


Figure 5.8 TDS-APIMS analyses of (a) the RTA 500 °C sample.

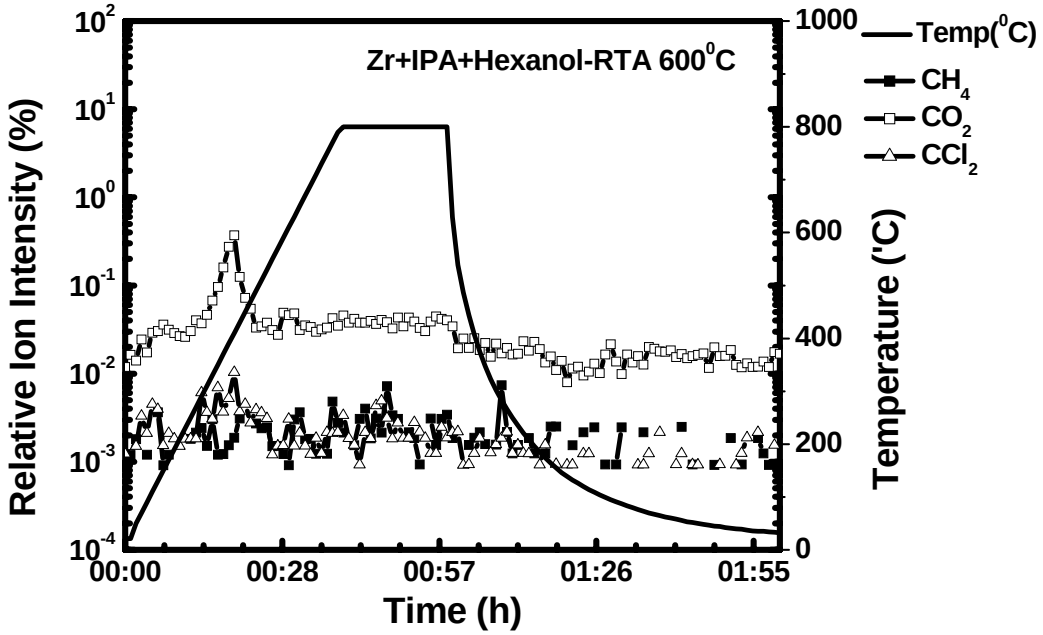


Figure 5.8 TDS-APIMS analyses of (b) the RTA 600 °C sample.

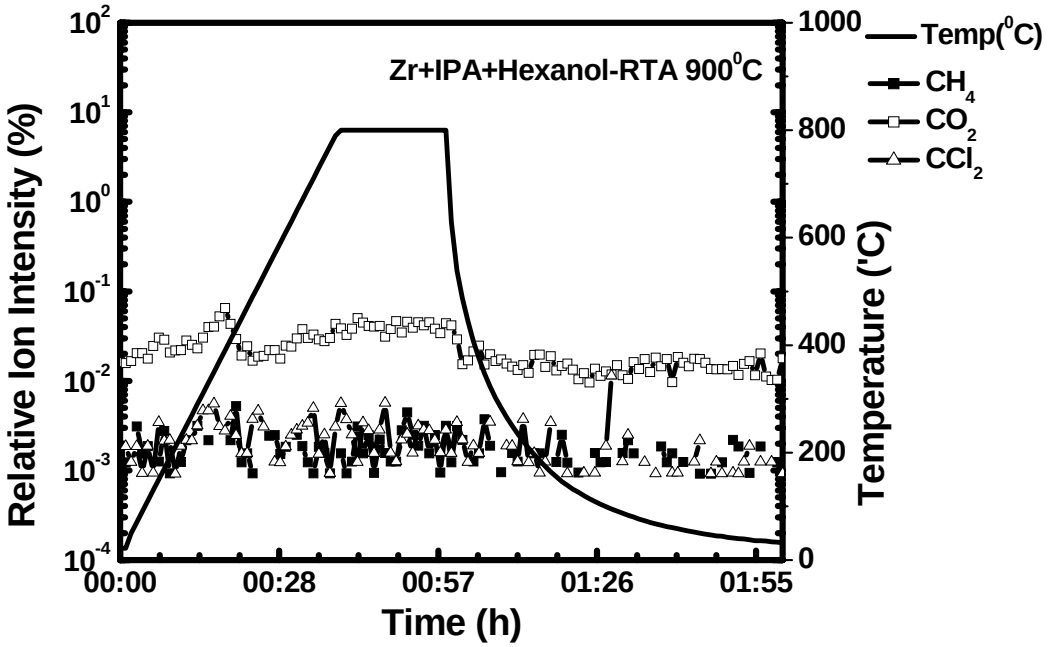


Figure 5.8 TDS-APIMS analyses of (c) the RTA 900 °C sample.

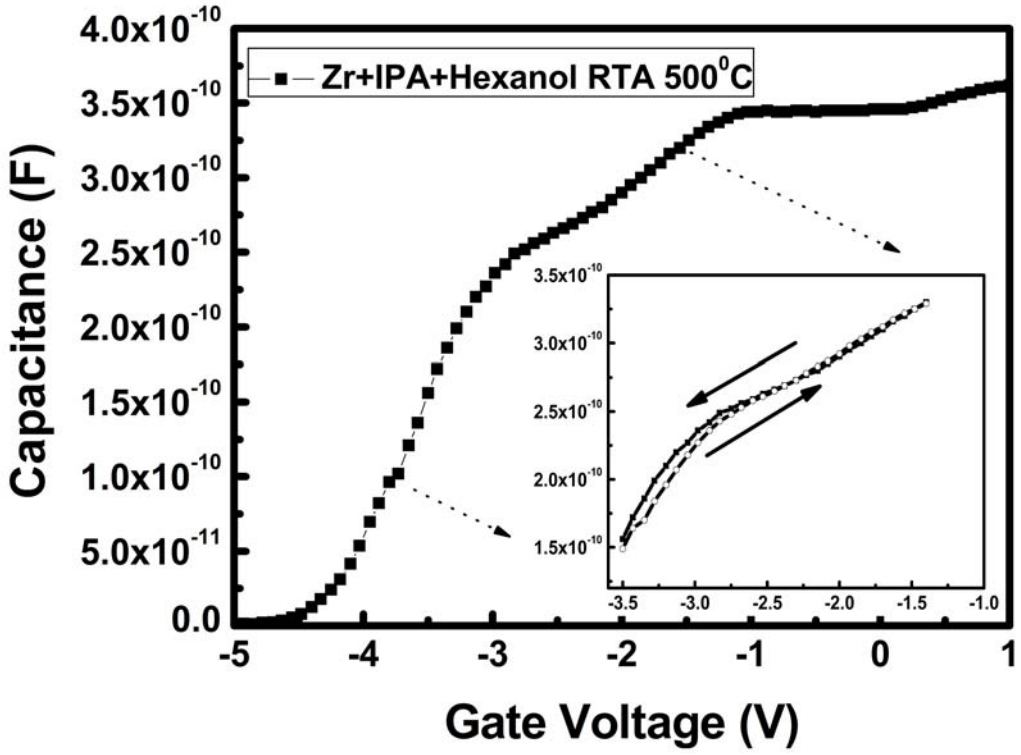


Figure 5.9 High-frequency (1 MHz) C–V characteristics of the sol–gel-derived ZrO_2 dielectric after RTA at (a) 500 °C under an O_2 atmosphere.

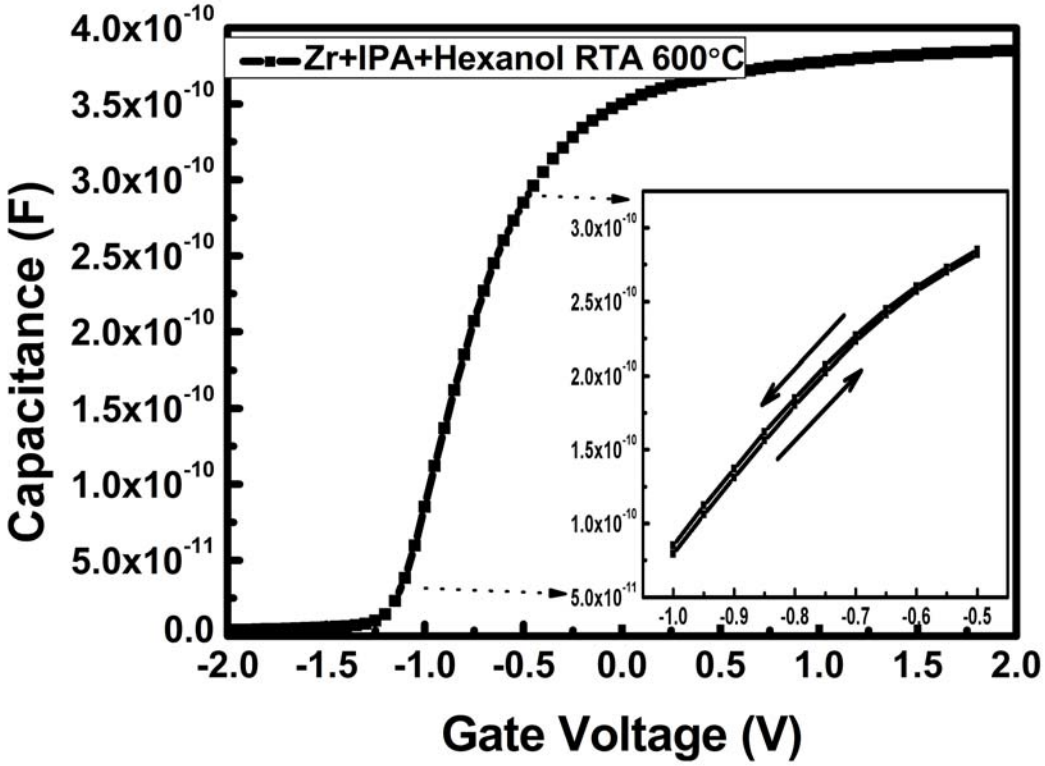


Figure 5.9 High-frequency (1 MHz) C–V characteristics of the sol–gel-derived ZrO_2 dielectric after RTA at (b) 600 ^oC under an O_2 atmosphere.

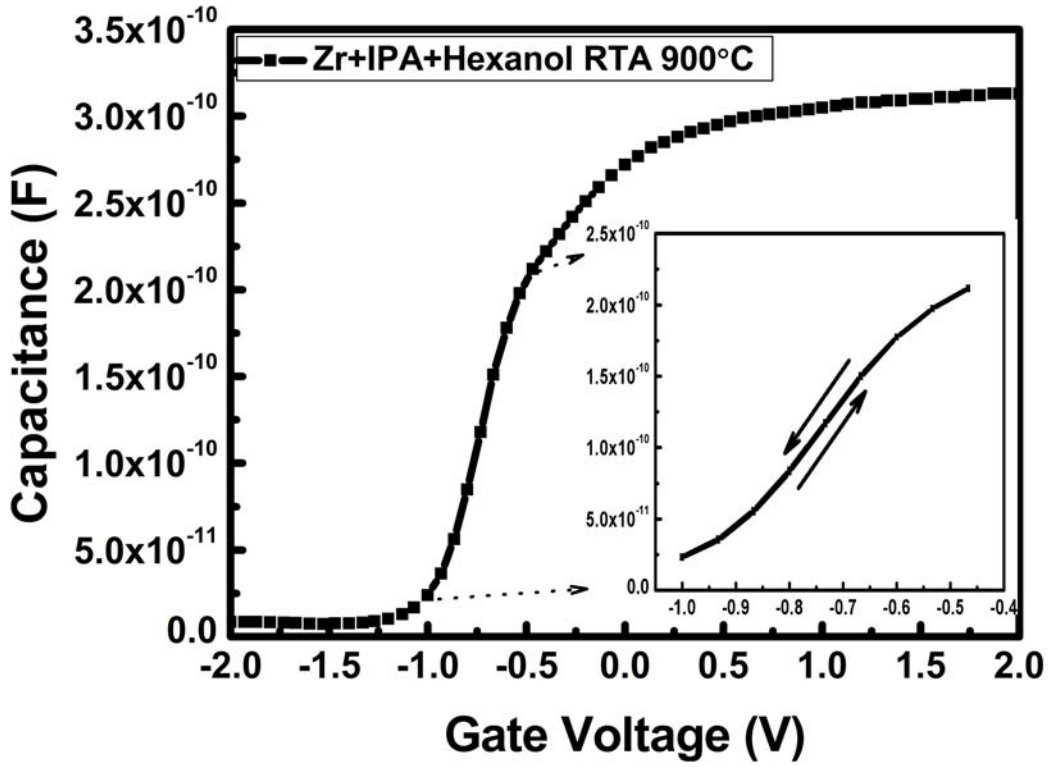


Figure 5.9 High-frequency (1 MHz) C–V characteristics of the sol–gel-derived ZrO_2 dielectric after RTA at (c) 900 ^oC under an O_2 atmosphere.

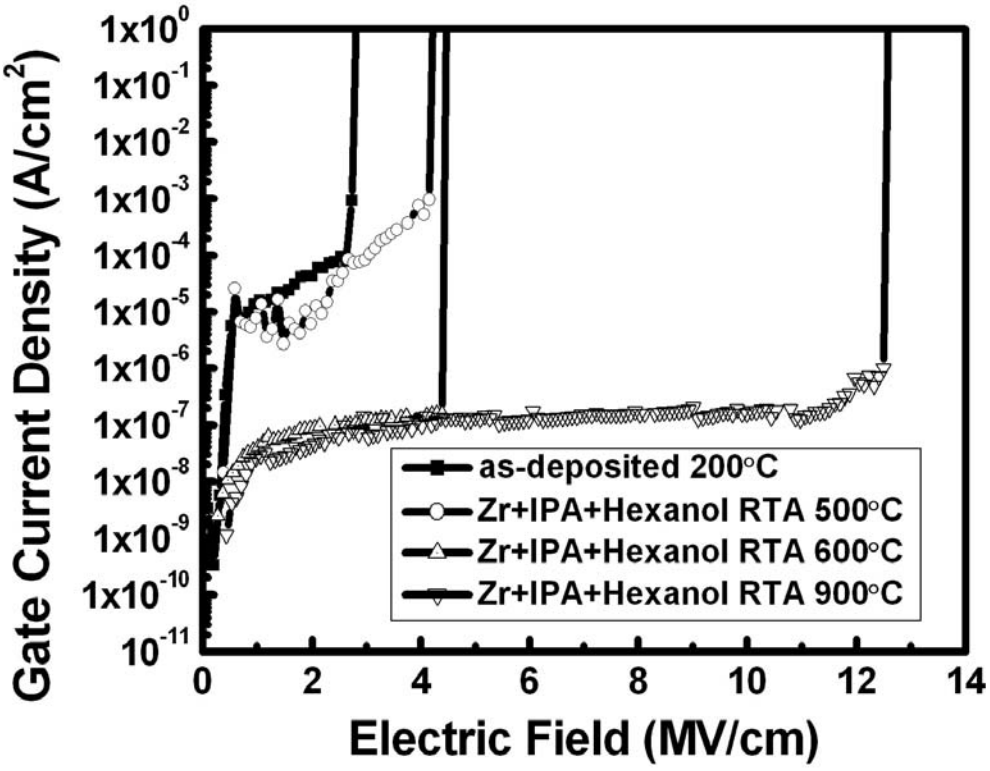


Figure 5.10 Gate current density vs electric field (J–E) characteristics of the ultrathin film after RTA treatment.

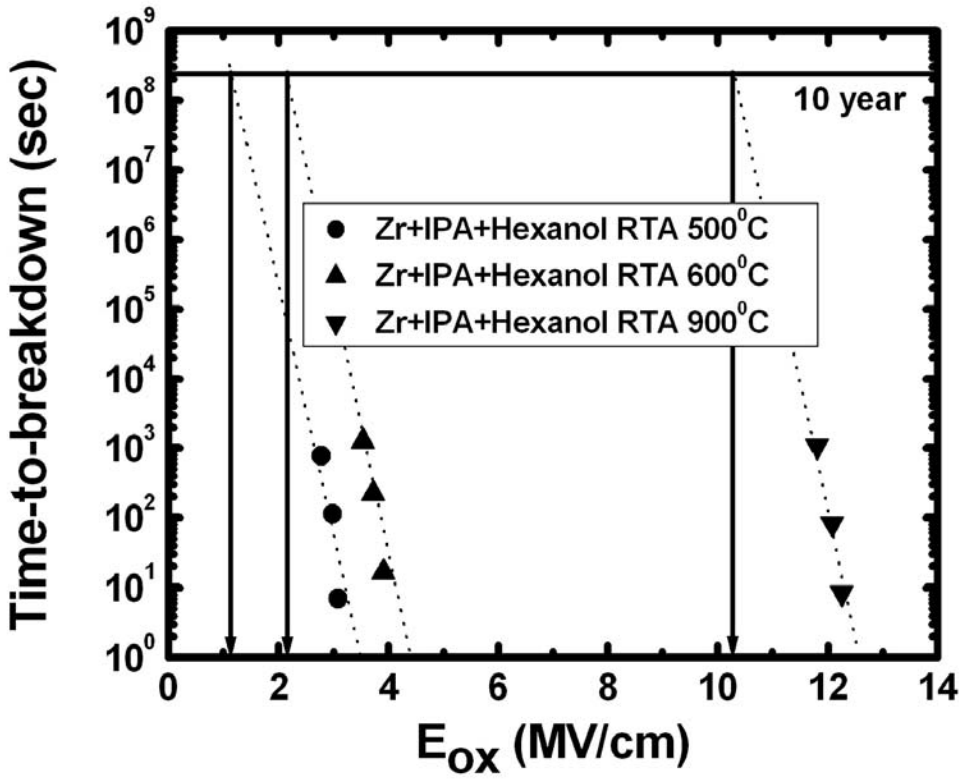


Figure 5.11 TDDB lifetime projection for the Zr + IPA + hexanol samples after RTA at 500, 600, and 900 °C, respectively.

Chapter 6

Novel Sol-Gel Derived SONOS-Type Memory

6.1 Introduction

Conventional Flash memory device uses floating gate structure and charge is stored in poly-silicon floating gate [1]. But when tunneling oxide is below 85nm, floating gate structure faces scaling issues [2]. The storage charge is leakage easily due to defects in the tunneling oxide formed by repeated program / erase cycles. So discrete trap memory devices like SONOS structure, nanocrystal memory is widely studied to replace floating gate structure for semiconductor memory application [3-7]. The charge trapping layer of traditional SONOS memory is silicon nitride (Si_3N_4). High-k materials are considered as charge storage material to get faster programming speed and better charge retention performance. But SONOS high-K memory has the electron migration problem in the charge trapping layer [5], this will cause the charge loss and degrade the charge retention performance. The nanocrystal memory can keep the trapped charge tightly to avoid the charge loss problem of SONOS memory and also achieve the advantages like: fast program/erase speed, low programming voltage and good endurance as SONOS memory [8]-[9].

Recently, numerous technologies have been developed for the preparation of various high-k films. To prepare insulating thin films, atomic layer deposition (ALD), physical vapor deposition (PVD), and chemical vapor deposition (CVD) methods have all been used to prepare films for new technologies. The sol-gel method is a very interesting simple technique for preparing ceramic films [10]. However, no reports

exist that describe the fabrication of SONOS type memory with sol-gel spin coating method.

The sol-gel method can provide colloidal solvents or precursor compounds when metal halides are hydrolyzed under controlled conditions. In the sol–gel process, hydrolysis, condensation, and polymerization steps occur to form metal oxide networks. These reactions play fateful roles in modifying the final material's properties. The most interesting feature of sol-gel processing is its ability to synthesize new types of materials that are known as "inorganic-organic hybrids." The film formation with spin coating is a more simple method than ALD, PVD or CVD due to its cheaper precursor and tool. In addition, the film can be fabricated in the normal pressure system instead of high vacuum system.

In this paper, we use the sol-gel spin coating method to fabricate three SONOS-type flash memory devices. One is used HfO_2 as charge trapping layer (Device A), and one of the other two is hafnium silicate nanocrystal memory (Device B). We use sol-gel method to combine three high-k precursors, i.e. $HfCl_4$, $ZrCl_4$ and $SiCl_4$ together to form hafnium silicate and zirconium silicate co-existed in a memory device (Device C) for the first time.

6.2 Experimental

In the beginning, we use $HfCl_4$ (99.5%, Aldrich, USA), $ZrCl_4$ (99.5%, Aldrich, USA), and $SiCl_4$ (99.5%, Aldrich, USA) as precursors and dissolve into isopropanol (IPA; Fluka; water content < 0.1%) to fabricate three high-k material mother solutions. $HfCl_4$ was used as the precursor for the synthesis of hafnium oxide. The sol solution was obtained by fully hydrolyzing $HfCl_4$ with a stoichiometric quantity of water in IPA to yield a Hf:IPA molar ratio of 1:1000 for charge trapping layer deposition.

$HfCl_4$ and $SiCl_4$ were used as the precursors for the hafnium silicate nanocrystal memory and we add some IPA to yield the molar ratio of $HfCl_4$: $SiCl_4$: IPA is 1:1:1000 for charge trapping layer deposition. At last, we combine $HfCl_4$, $ZrCl_4$, and $SiCl_4$ to fabricate hafnium silicate and zirconium silicate co-existed nanocrystal memory and we add some IPA to yield the molar ratio of $HfCl_4$: $ZrCl_4$: $SiCl_4$: IPA is 1:1:1:1000 for charge trapping layer deposition.

The fabrication of sol-gel spin coating nanocrystal memory is started with LOCOS isolation process on p-type (100) 150-mm silicon substrate. At the beginning, a 4-nm tunneling oxide was thermally grown at 925^{o}C by furnace. The charge trapping layer was deposited by spin coating at 3000rpm for 60 sec at ambient temperature (25^{o}C). The spin-coater used was TEL Clean Track Model-MK8 (Japan). After spin coating, the wafer was under rapid thermal annealing (RTA) at 900^{o}C for 60 sec in O_2 ambient to form HfO_2 layer, hafnium silicates and hafnium silicates and zirconium silicates co-existed nanocrystal memory. The 30nm-thick blocking oxide was deposited by LPCVD TEOS followed by poly-Si gate 200nm deposition. After the LPCVD TEOS deposition, the TEOS oxide is densified in N_2 ambient under 900^{o}C for 30s anneal. We think this can repair the defects and decrease the number of traps in the TEOS oxide. Finally, gate pattering, source/drain (S/D) implant, and the rest of the subsequent CMOS processes were used to fabricate this SONOS-like memory. Figure 6.1 shows the structure of the fabricated device.

6.3. Results and Discussion

6.3.1 Physical Characteristics

In order to analyze the chemical composition of hafnia film, elements are

detected by X-ray photoemission spectroscopy (XPS). Figure 6.2 demonstrates the high-resolution spectrum of Hf 4f peak for the sol-gel film. The Hf $4f_{7/2}$ peak was approximately 16.8 eV with a difference of 1.7 eV in binding energy between the Hf $4f_{5/2}$ and Hf $4f_{7/2}$ peaks at RTA treatment temperature of 900^{o}C. This observation suggests the sol-gel film is HfO_2 and is similar with the literature identification for HfO_2 film from ALD method [11].

From the Hf 4f spectrum, we observe clearly RTA annealing under 900 °C in O_2 treatment leads to remarkable changes in the XPS spectra. This change, which is apparent from the increase in the signal of the Hf–O bonds upon increasing the annealing temperature. The as-deposited hafnia film is mainly $HfO_{2-\delta}$ ($\delta>0$), while the annealing under oxygen ambient can decrease the δ value. This finding indicates that structural composition of the HfO_2 has occurred.

The high-resolution transmission electron microscopy (HRTEM) image in Fig. 6.3 depicts the nanocrystal on SiO_2 film after annealing at 900°C for 60s. The average nanocrystal size is around 5nm. The clearly visible lattice fringes denote crystallization into a well-ordered nanostructure. Chemical characterization of the $HfSi_xO_y$ film was accomplished by x-ray photoelectron spectroscopy (XPS) in Fig. 6.4. The literature [12] also suggests the similar Hf 4f peaks for the hafnium silicate film. Specifically, as the film is heated, the shift from 17.4 eV (as-dep) to 18.0 eV (900 °C annealing) and the enlargement of peak height are observed. Cho et al. [13] reports the peak shift to higher binding energy for $HfSi_xO_y$ and can be caused by the formation of Hf-O bonding in the vicinity of Si. Thus, these relationships of bonding between Hf-O and Hf-Si suggest that Hf and Si atoms are bonded to O atoms as nearest neighbors. Wilk and Kirsch also observe a similar behavior [14]-[15], and they attribute to the increased hafnium silicate formation.

The high-resolution transmission electron microscopy (HRTEM) image in Fig.

6.5 depicts the nanocrystal on SiO_2 film after annealing at 900°C for 60s. The average nanocrystal size is around 5nm. We observed two kinds of different colors nanocrystals in the TEM image. To analyze chemical characterization of the nanocrystals, additional x-ray photoelectron spectroscopy (XPS) analysis was done.

Fig. 6.6 shows the comparison XPS data of the (a)Hf 4f and (b)Zr 3d features for as-dep and after 900 °C annealing. The Hf 4f XPS is mentioned above. Similar data were obtained for zirconium silicate formation in Zr 3d feature. Wilk and Kirsch also observe a similar behavior [14 -15], and they attribute to the increased hafnium and zirconium silicate formation. Therefore, we suppose that the darker nanocrystals in Fig. 6.5 are hafnium silicate nanocrystals and the opposites are zirconium silicate nanocrystals due to their xps features and different atomic weight.

6.3.2 Electrical Characteristics

Figure 6.7-6.9 show the Id-Vg curve of the Device A, B, and C. We use channel hot electron injection to program, and band to band tunneling induced hot hole injection (BTBHHI) to erase. The program condition is Vg = 15V, Vd = 10V for 10 msec. The erase condition is Vg = -10V, Vd = 10V for 1 sec. The memory window of Device A, B, and C are 3V, 3.3V, and 4V respectively. The Device C has larger Vth shift than A and B due to more nanocrystals existed in the charge trapping layer.

Figure 6.10-6.12 show the program speed curve of the Device A, B, and C. We use channel hot electron (CHE) to program, and the program conditions are (i) Vg= 10V, Vd= 10V; (ii) Vg= 12V, Vd= 10V; (iii) Vg= 15V, Vd= 10V, respectively. The Vth shift increases as increasing the applied gate voltage due to more “hot” electrons generated to reach the trapping layer and to be trapped in the charge trapping layer.

Figure 6.13-6.15 shows the program speed comparison of the Device A, B, and

C. We can see Device C shows larger Vth shift than A and B even under the same stress conditions. This is due to more trapping site embedded in the Device C.

Figure 6.16-6.18 shows the erase speed curve for Device A, B, and C. We use band to band hot hole (BTBHH) to erase, and the erase conditions are (i) Vg= -10V, Vd= 10V; (ii) Vg= -12V, Vd= 10V; (iii) Vg= -15V, Vd= 10V, respectively. As the gate voltage becomes more negative, the erase effect becomes much fast. Figure 6.19 shows the erase speed comparison of Device A, B and C with Vg= -12V, Vd=10V stress condition. We can see Device C exhibits larger Vth shift due to more trapping site to trap "hot" holes.

The charge retention characteristic of the Device A, B, and C are demonstrated in Fig. 6.20-6.22 respectively. The normalized Vth shift is defined as the ratio of Vth shift at the time of interest and at the beginning. Using this as an indicator, we can see the charge loss for the nanocrystal memory. The data retention is measured under the room temperature 25^{o}C and 85^{o}C for 10^4 sec, respectively. The room temperature retention curve shows only 6% charge loss as measure time up to 10^4 sec and ~20% charge loss at 85^{o}C for Device A. For the Device B, the charge loss at 25^{o}C and 85^{o}C are 6% and 18%, respectively. For the Device C, the charge loss at 25^{o}C and 85^{o}C are 5% and 13%, respectively. This result indicates the nanocrystals in the charge trapping layer can tightly catch the tunneling electrons. Hence, the trapped electrons by the sol-gel-derived nanocrystal devices are not easily to escape, and the exhibited charge loss percentage is quite low. The Device C has better retention than Device B due to two layer nanocrystal. Because electrons are trapped in upper nanocrystals, this will increase the equivalent tunneling oxide thickness. This will lower the direct tunneling current from the nanocrystals to silicon substrate. So the Device C has best retention among Device A and B.

Endurance measurement of Device A, B, and C are shown in Fig. 6.23-6.25. The

measured condition is - program: Vg = 15V, Vd = 10V, 1 msec; erase: Vg = -10V, Vd = 10V, 10 msec. As the figure shows, the memory window is about 2.8V, 2.8V and 3V for Device A, B, and C after 10^5 P/E cycles. No significant window narrowing is observed. This finding suggests the simple sol-gel process can be incorporated into the SONOS-like memory fabrication.

Drain disturbance measurement is depicted in Fig. 6.26-6.28. We measured the program state devices and applied Vd=5V or 10V with Vg=Vs=Vb=0V to the device for 10^3 sec stress. The program state Vth loss of Vd=5V are about 0.3~0.4V and 0.6V for the Vd=10V. Gate disturbance is shown in Fig. 6.29-6.31. We measure the erased state devices and applied Vg=10V or 12V with Vd=Vs=Vb=0V to the device. From the figures, we can see the HfO_2 charge trapping layer with the worst gate disturbance and nanocrystal memory like Device B and Device C have negligible gate disturbance. This is because the nanocrystal is surrounded by SiO_2 and this will increases the equivalent tunneling oxide thickness. When the tunneling oxide thickness increased, the electrons in the substrate are hard to tunnel to nanocrystal by FN tunneling. Figure 31-33 shows the read disturbance measurement of the three devices. We measured the erased state device and applied Vg=6V, with Vd=3V, 4V, and 5V to the devices. We can see the read disturbance is worse when larger drain voltage is applied. From the Fig. 6.32-6.33, the worst case is Vg=6V, Vd=5V. But the Vth shift increases no more than 0.5V. In Fig. 6.34, we can see Devices C with negligible read disturbance. So the co-existed hafnium silicate and zirconium silicate nanocrystal memory devices have better electrical performance than HfO_2 layer or hafnium silicates. This is because the nanocrystal is surrounded by SiO_2 and this will increases the equivalent tunneling oxide thickness. When the tunneling oxide thickness increased, the electrons in the substrate are hard to tunnel to be trapped in the nanocrystal. So the Device C has good read disturb. The electrical characteristics comparison of Device A, B and C is listed

in Table 6.1.

6.4 Summary

In this paper, we use sol-gel spin coating method to fabricate HfO_2 layer, hafnium silicates nanocrystal, and co-existed hafnium silicates and zirconium silicates nanocrystal memory. The XPS analysis indicates the formation of HfO_2 layer, hafnium silicate and zirconium silicate after 900^{o}C 1min RTA. From the TEM image, we also demonstrate the co-existed hafnium silicate nanocrystal and zirconium silicate nanocrystal and the size of one nanocrystal is 5nm. We have verified the device performance with the P/E speed, charge retention, endurance and disturbance measurement. The quality of the co-existed hafnium silicate and zirconium silicate nanocrystals formed by the sol-gel spin coating method and RTA treatment exhibits better properties in terms of larger Vth shift due to more trapping site existed, long charge retention time (5% loss at 10^4sec), good endurance (up to 10^5 P/E cycles) with no memory window narrowing and negligible gate and read disturbance due to SiO_2 surrounded the nanocrystal increased the tunneling oxide thickness.

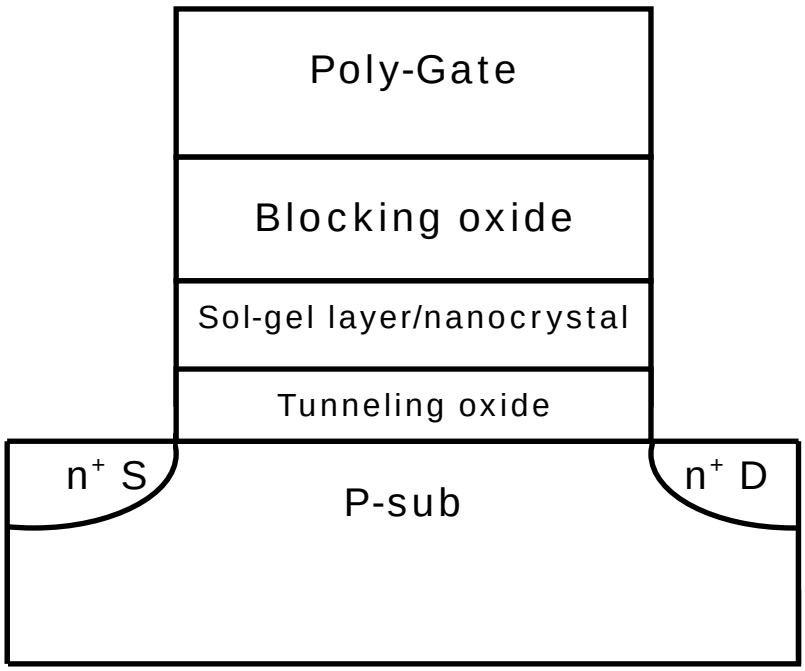


Figure 6.1 Schematic diagram of the device structure for the spin coating charge trapping film/nanocrystal memories.

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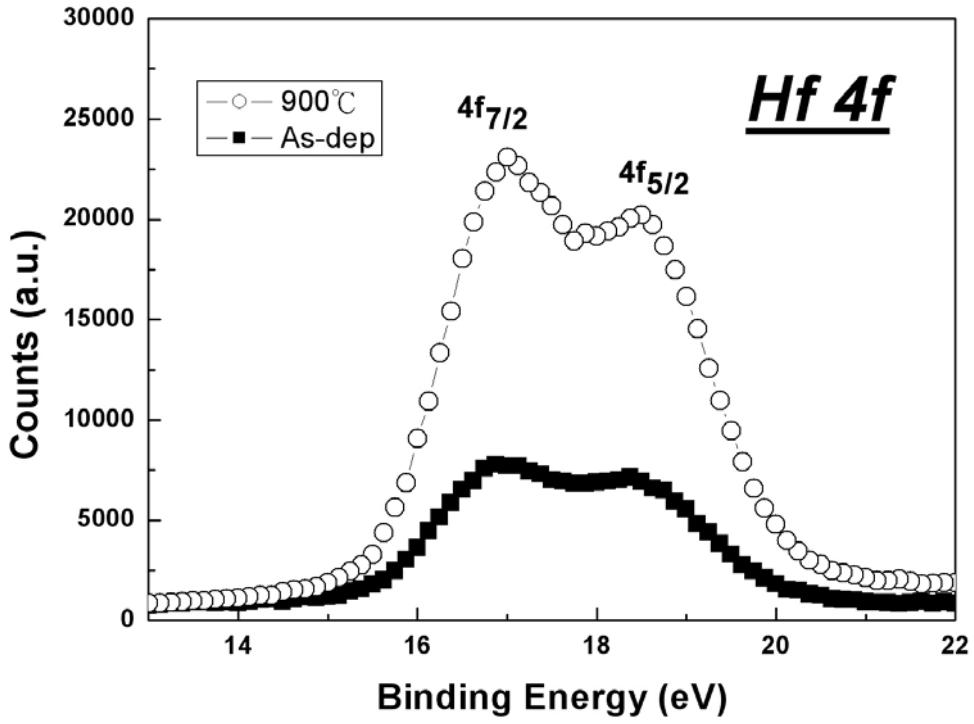

Fig. 6.2 XPS spectra of sol-gel spin coating and 900 ^{o}C RTA for the HfO_2 films.

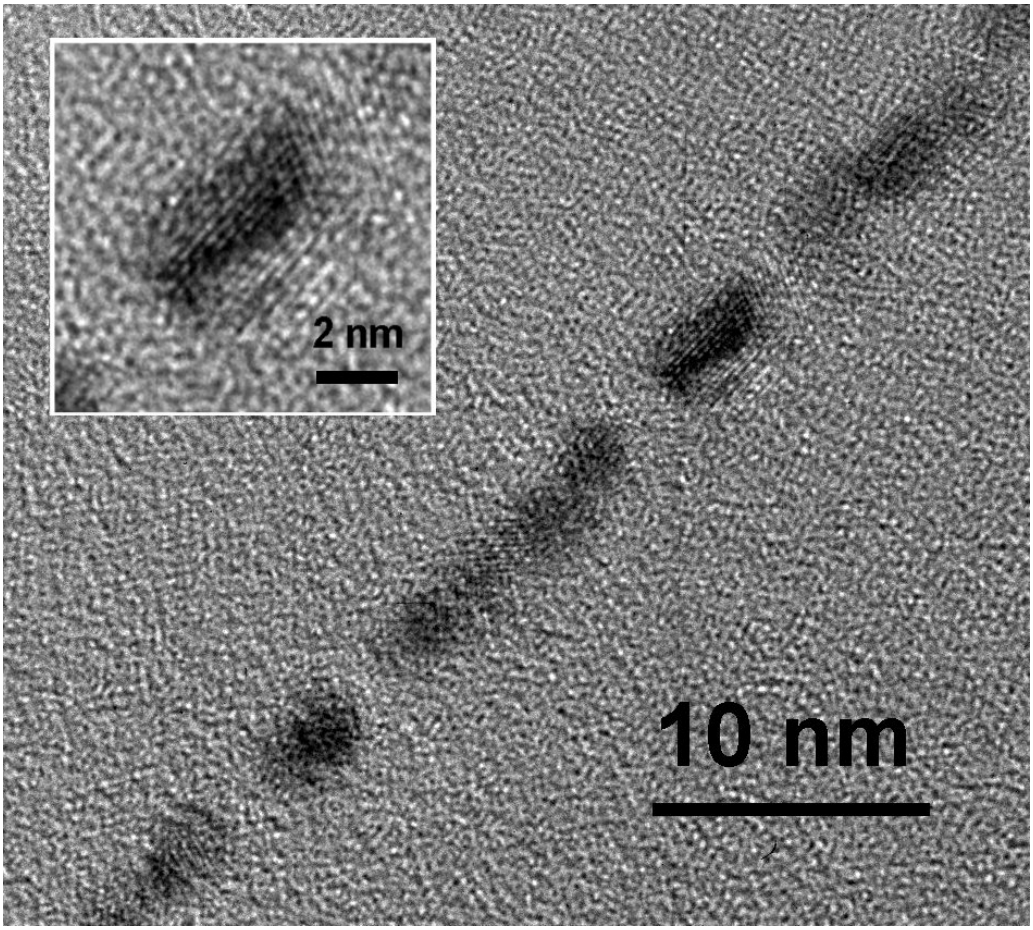

Figure 6.3 Cross-sectional HRTEM of the hafnium silicate nanocrystals. The inset is the magnification of nanocrystal.

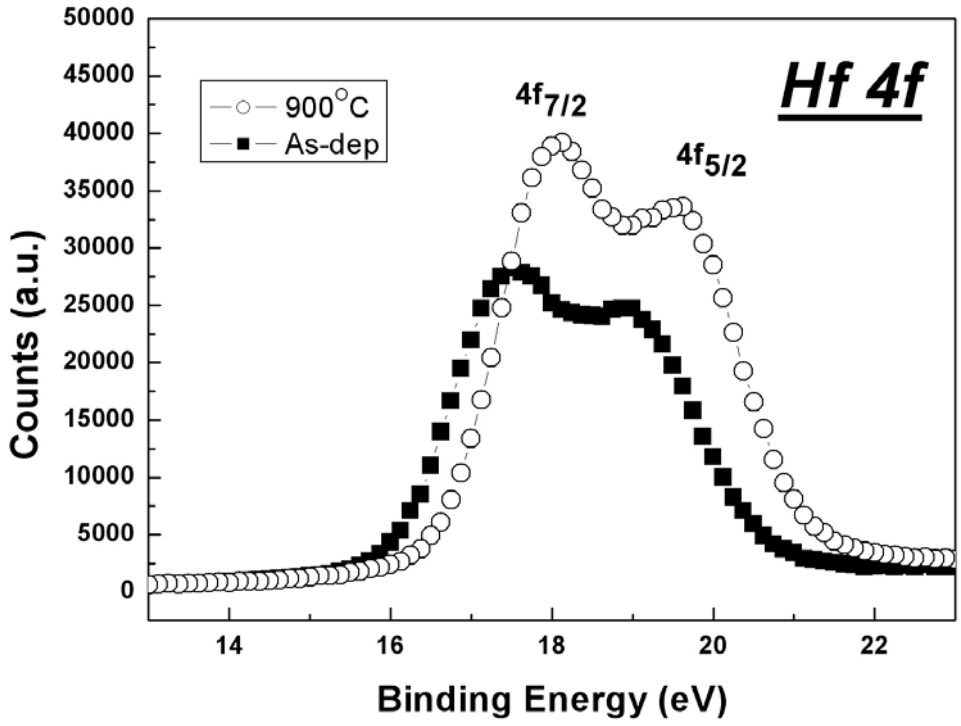

Figure 6.4 XPS spectra of sol-gel spin coating and 900 ^{o}C RTA for the hafnium silicate.

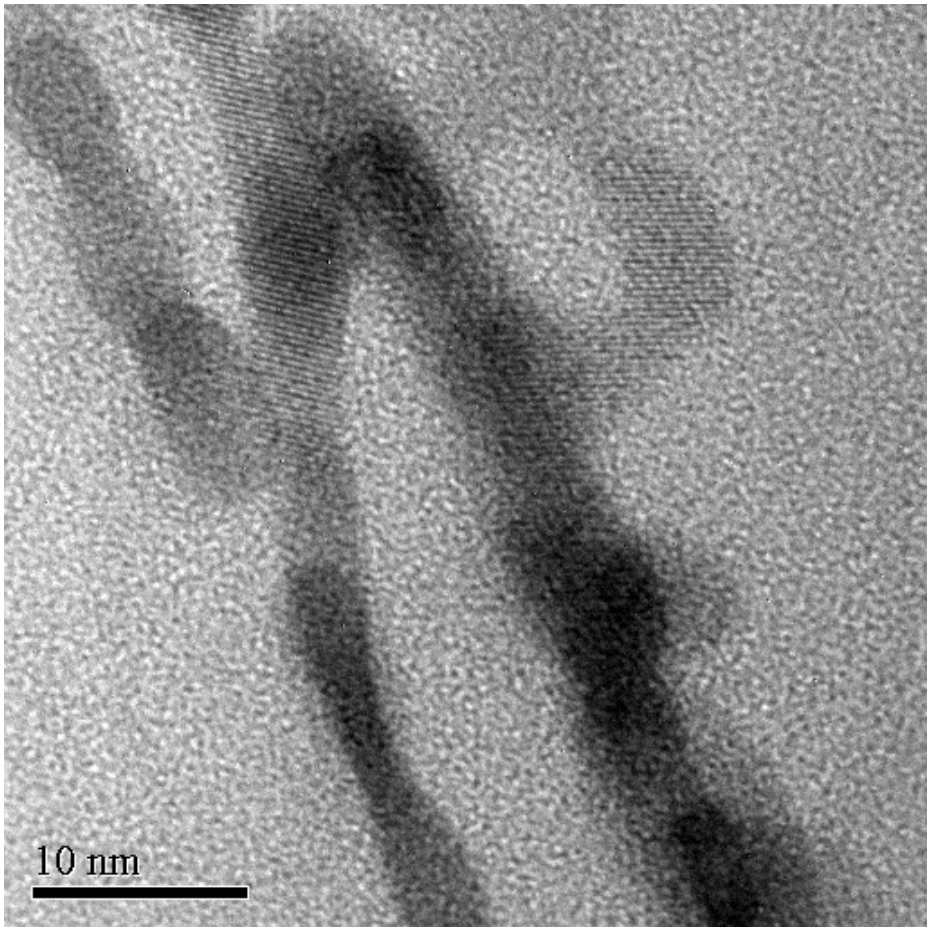

Figure 6.5 Cross-sectional HRTEM of the hafnium silicate and zirconium silicate nanocrystals. The dark area is hafnium silicate, and the light image of crystal is the zirconium silicate.

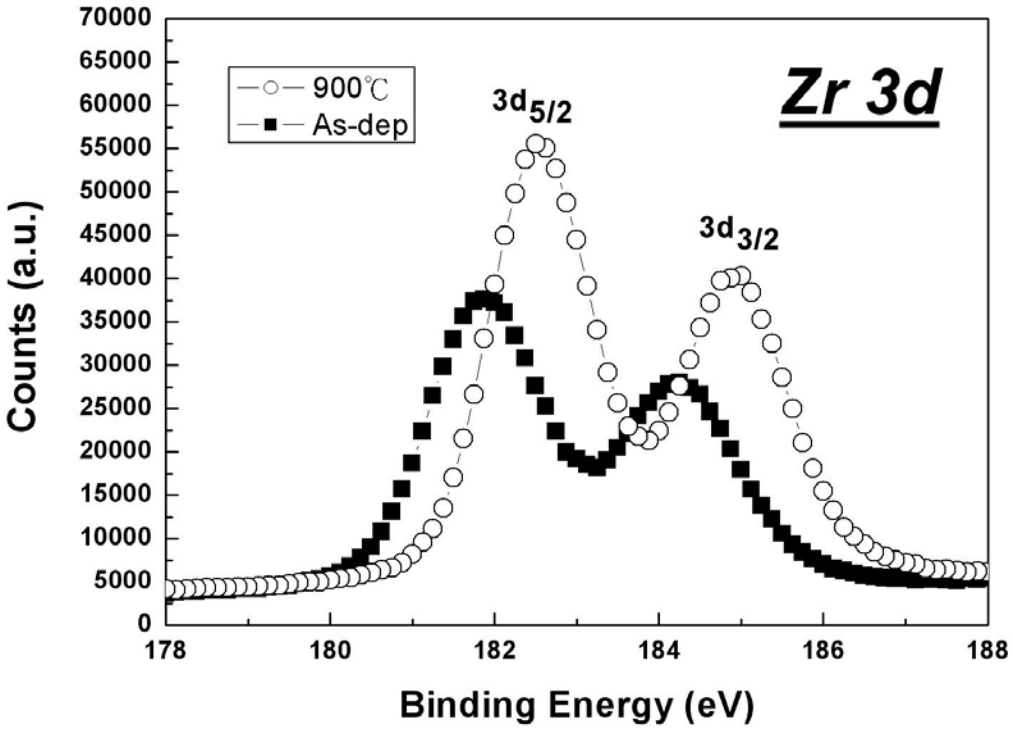

Figure 6.6 XPS spectra of sol-gel spin coating and 900 ^{o}C RTA for the nanocrystals (a) zirconium silicate

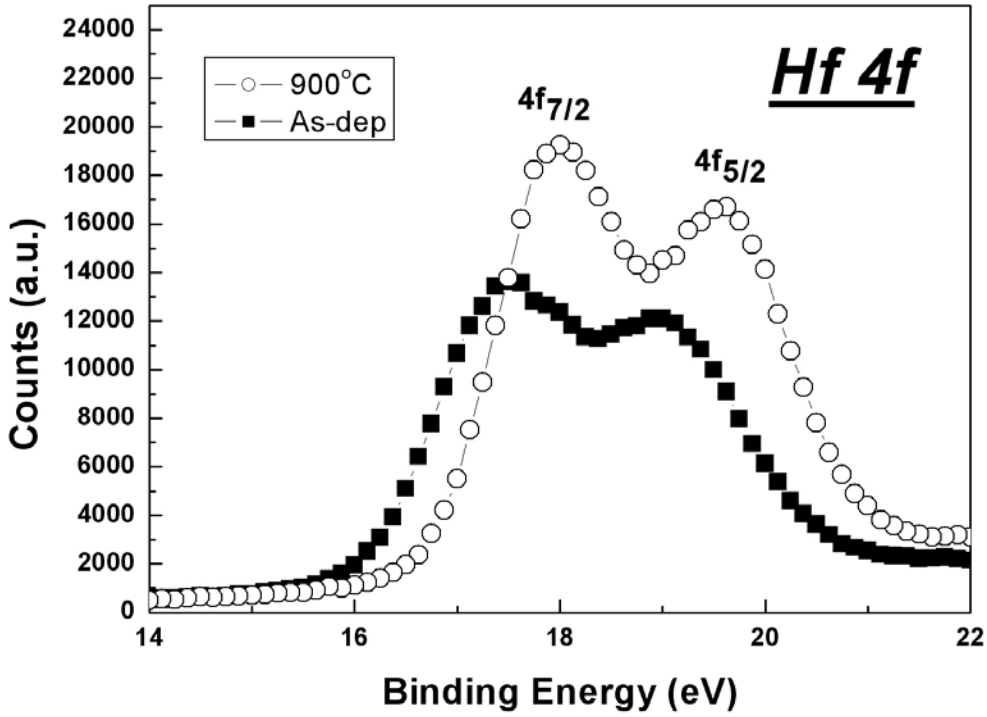

Figure 6.6 XPS spectra of sol-gel spin coating and 900 ^{o}C RTA for the nanocrystals (b) hafnium silicate.

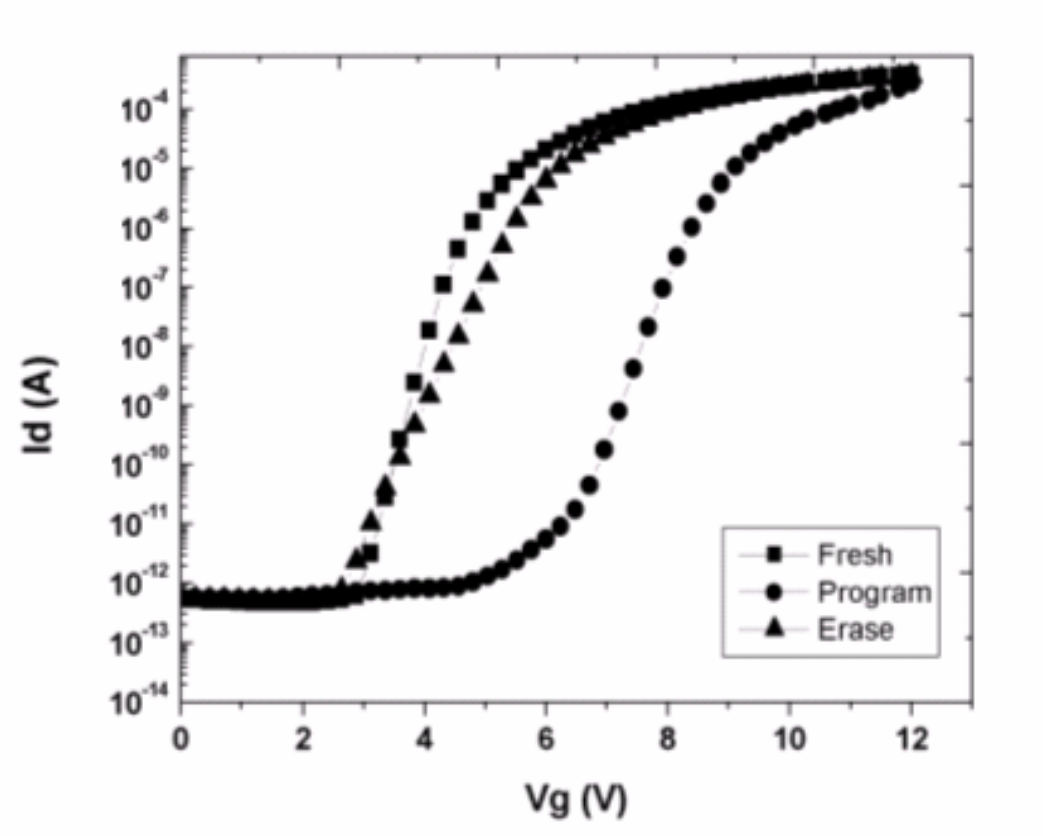

Fig.6.7 The Id-Vg curve of Device A, the memory window is 3V.

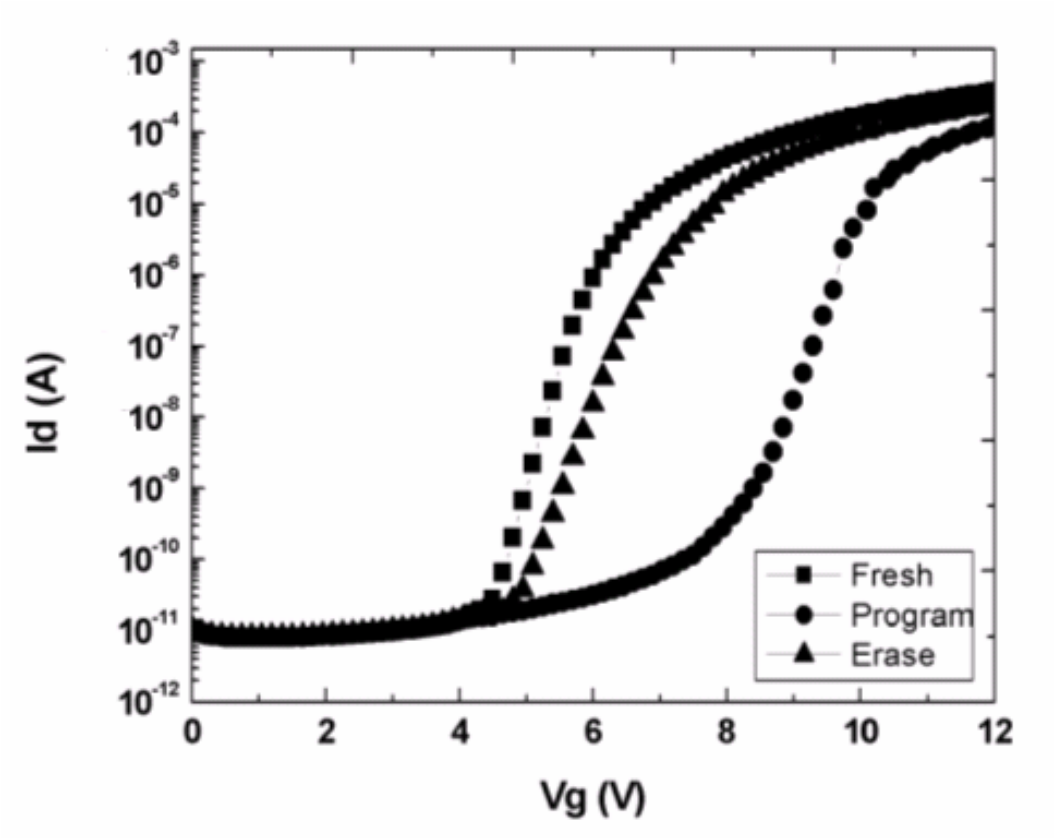

Fig.6.8 The Id-Vg curve of Device B, the memory window is 3.3V.

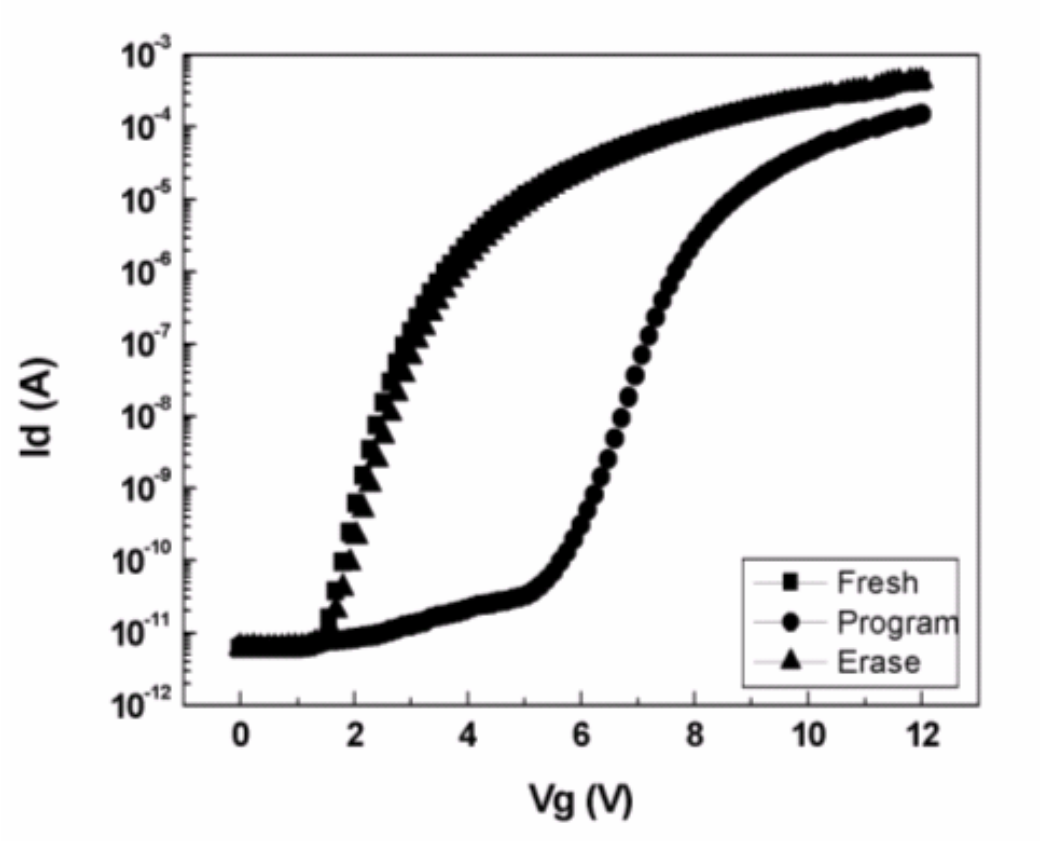

Fig.6.9 The Id-Vg curve of Device C, the memory window is 4V.

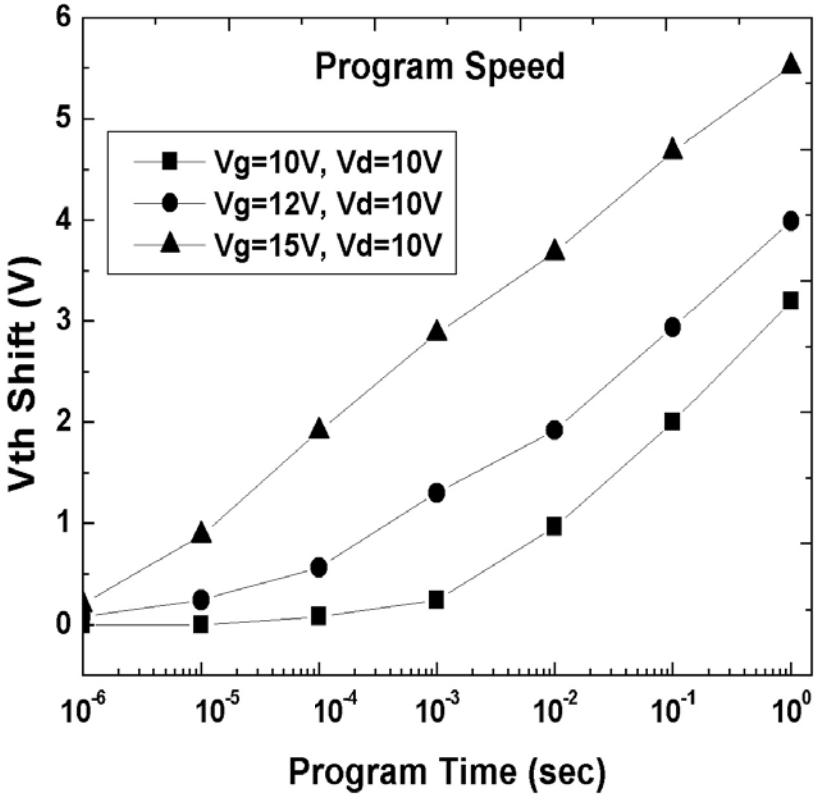

Figure 6.10 The program speed of Device A.

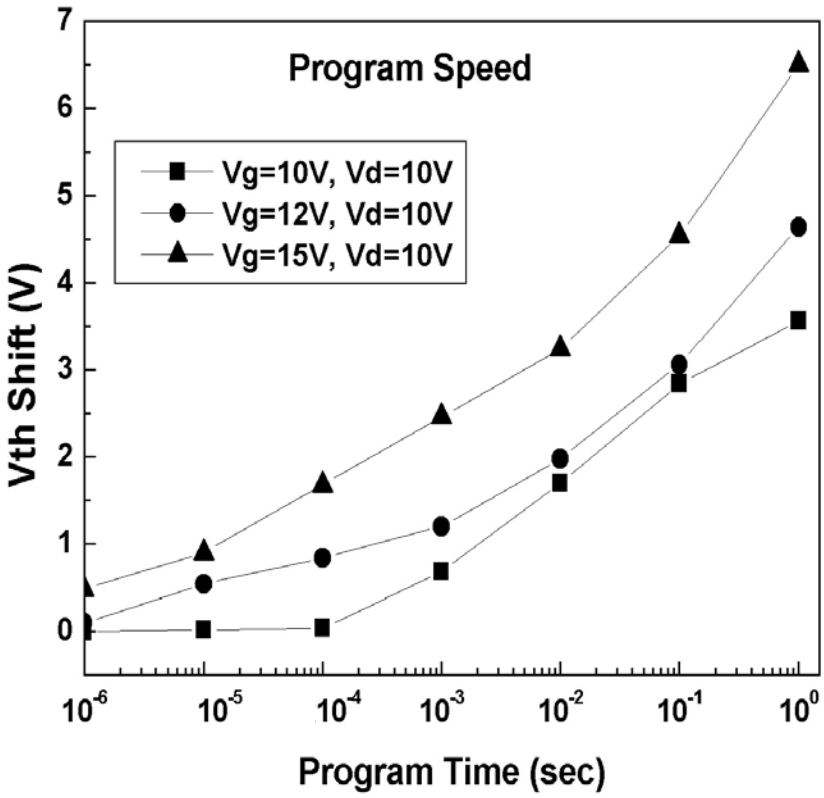

Figure 6.11 The program speed of Device B.

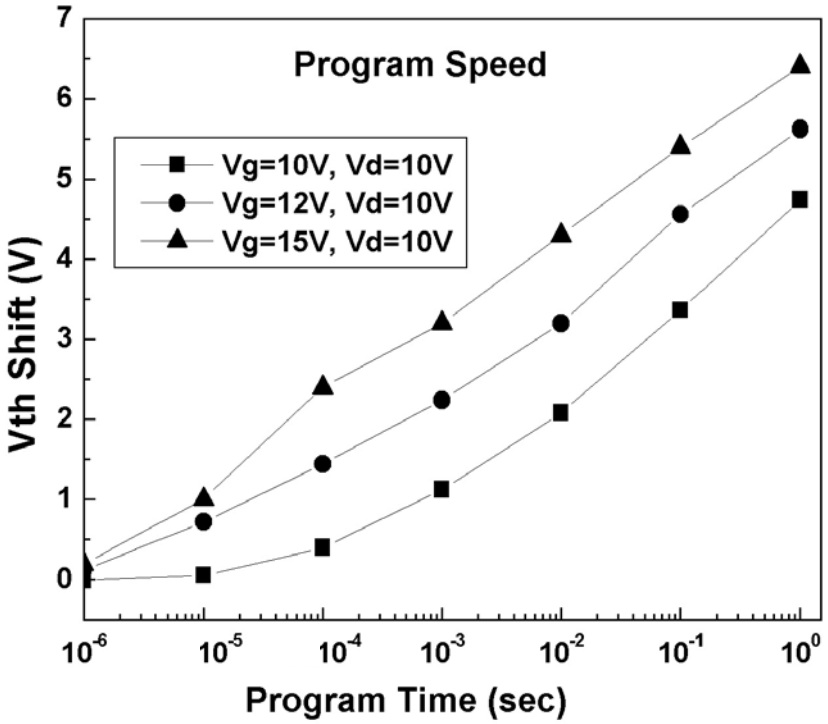

Figure 6.12 The program speed of Device C.

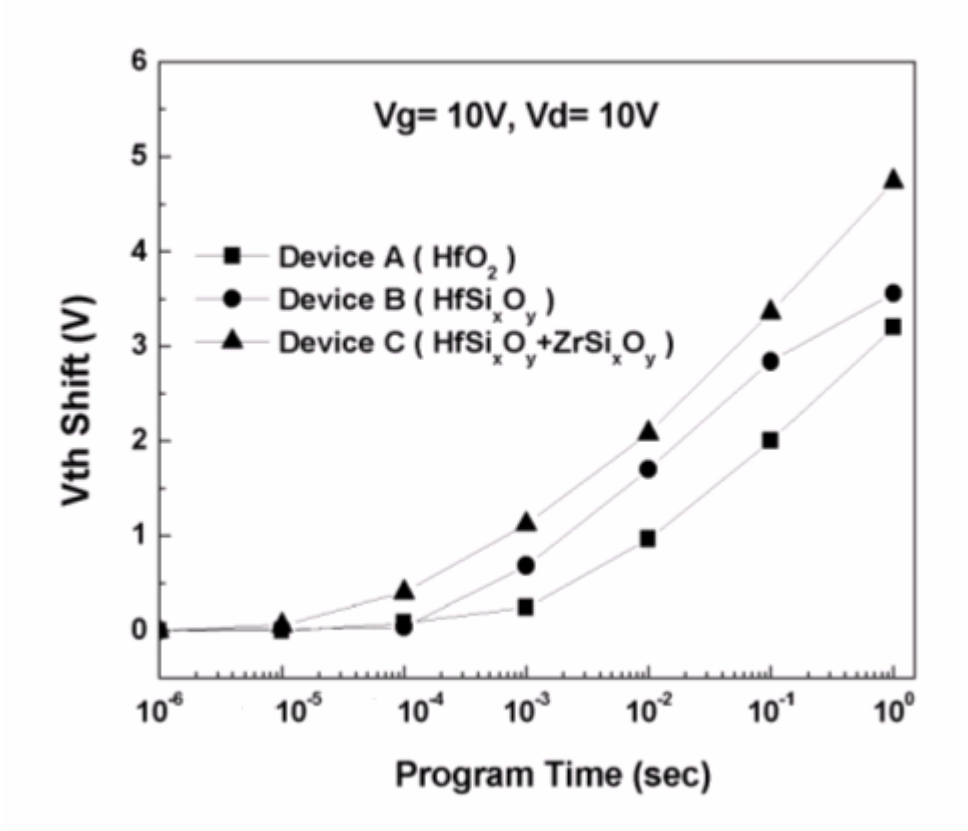

Figure 6.13 The program speed comparison of Device A, B, and C for Vg=10V, Vd=10V.

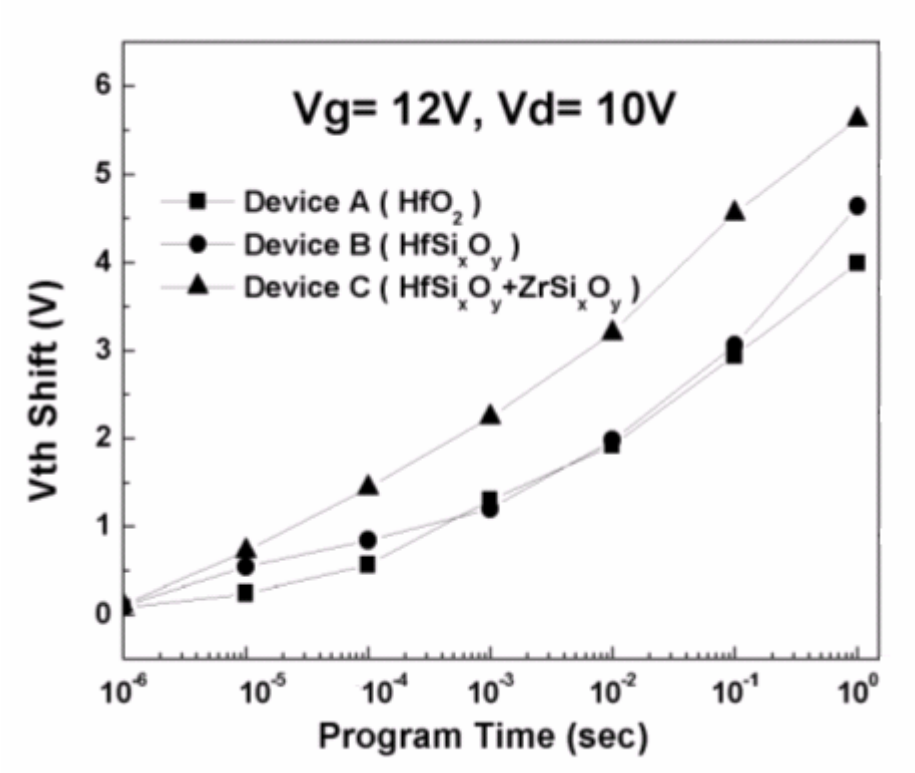

Figure 6.14 The program speed comparison of Device A, B, and C for Vg=12V, Vd=10V.

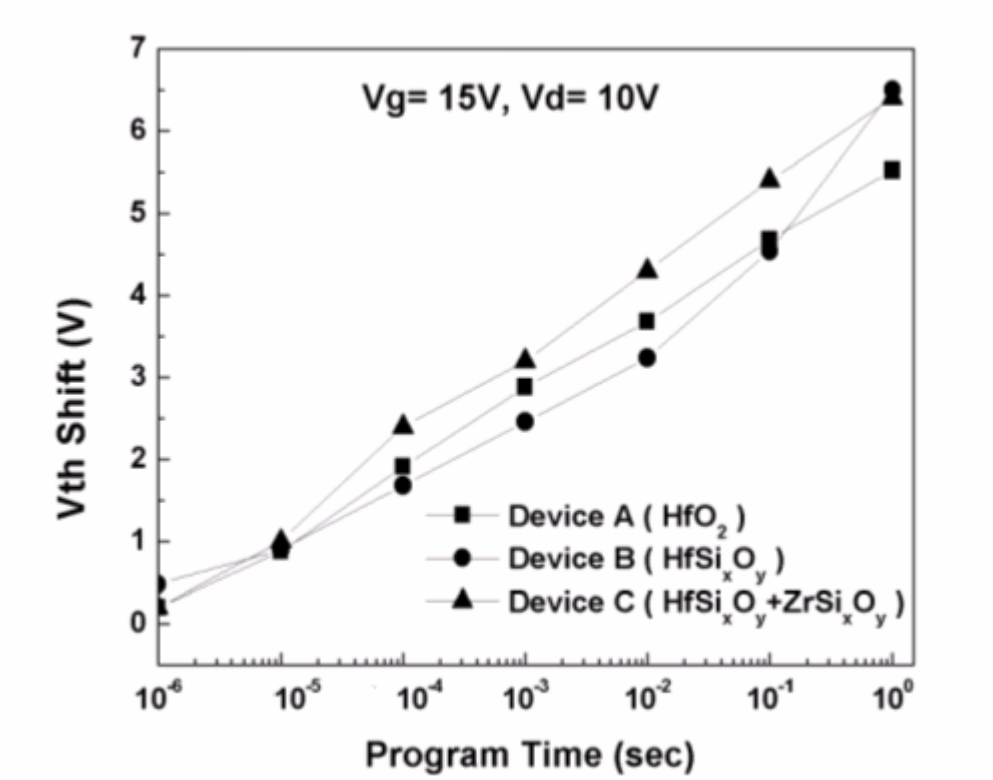

Figure 6.15 The program speed comparison of Device A, B, and C for Vg=15V, Vd=10V.

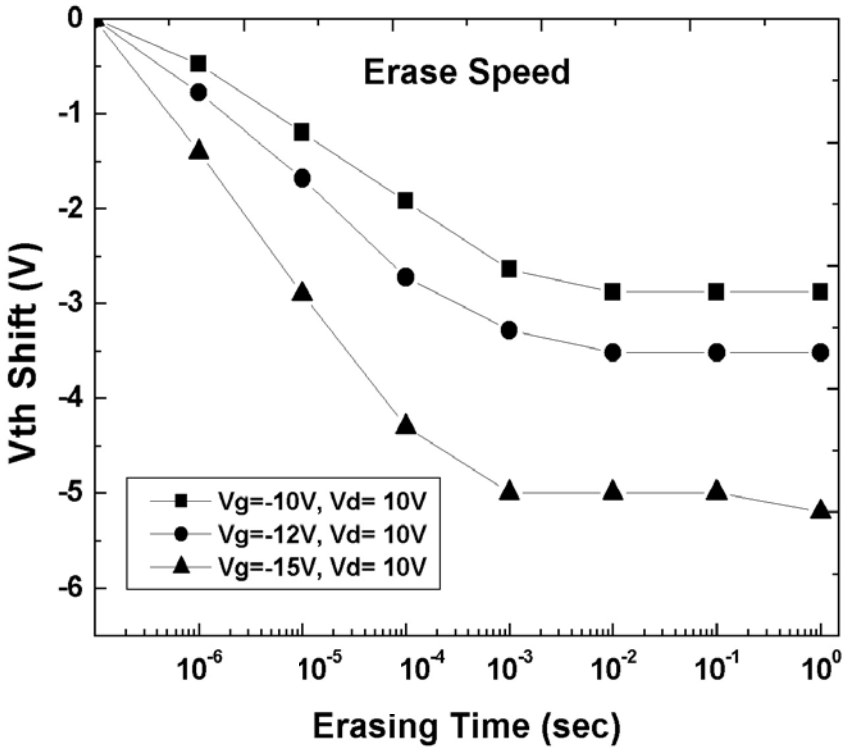

Figure 6.16 The erase speed of Device A.

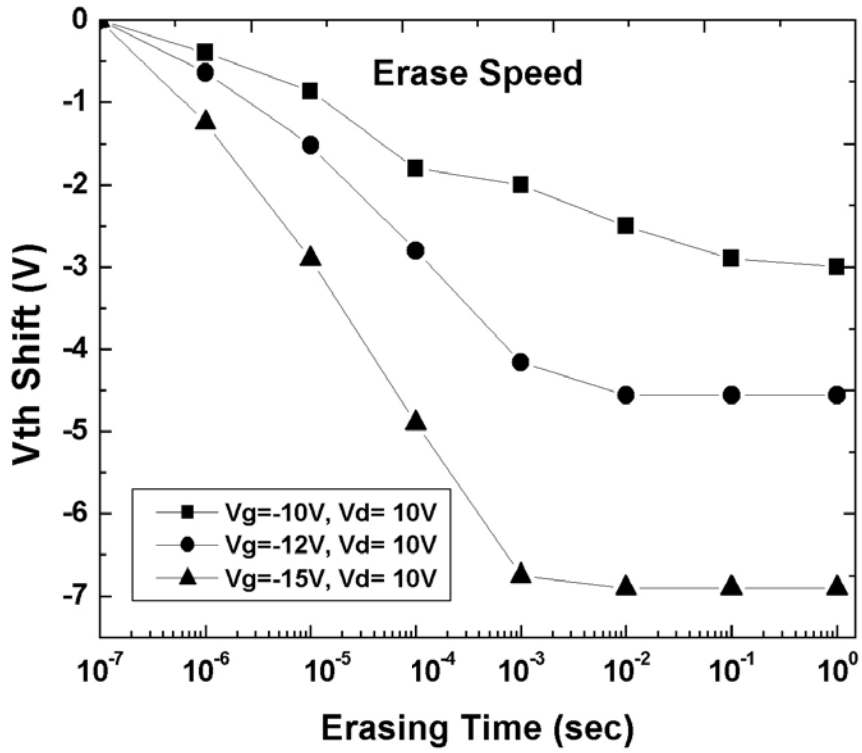

Figure 6.17 The erase speed of Device B.

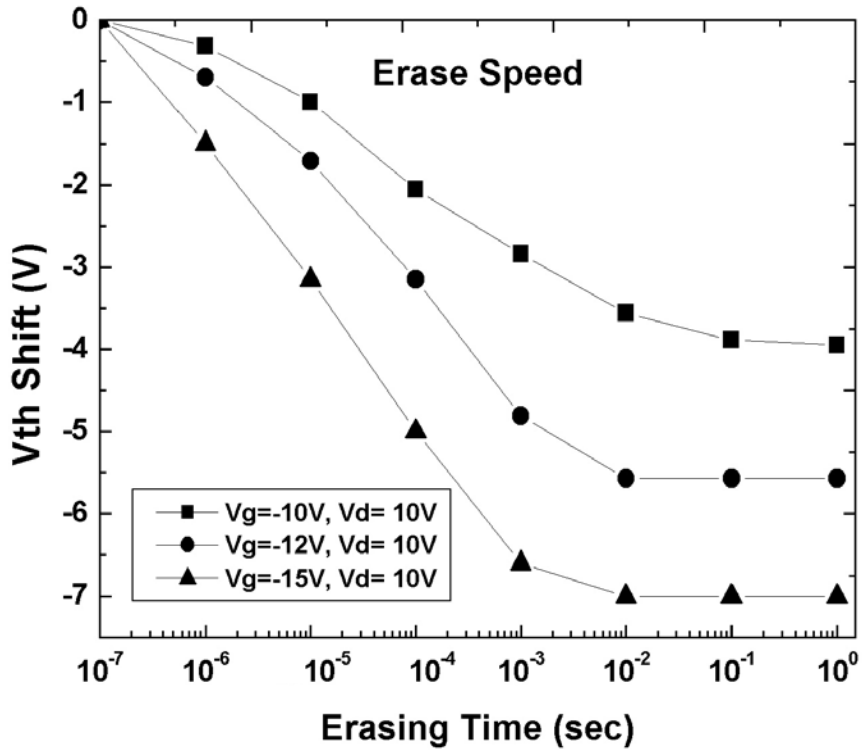

Figure 6.18 The erase speed of Device C.

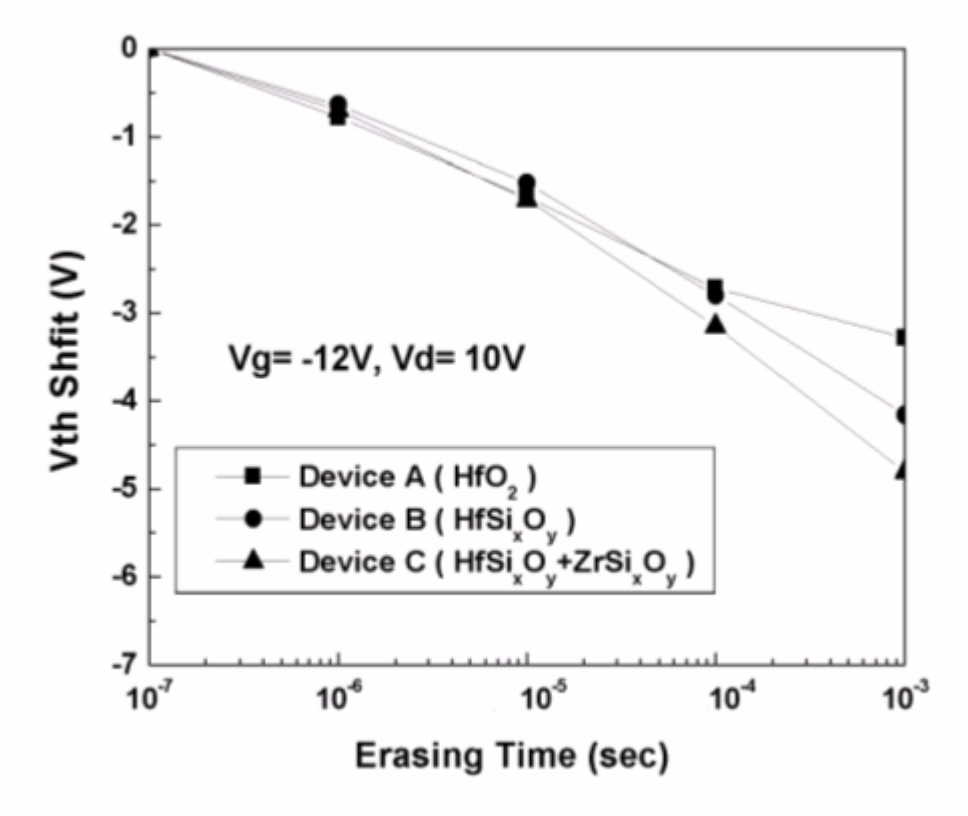

Figure 6.19 The erase speed comparison of Device A,B and C.

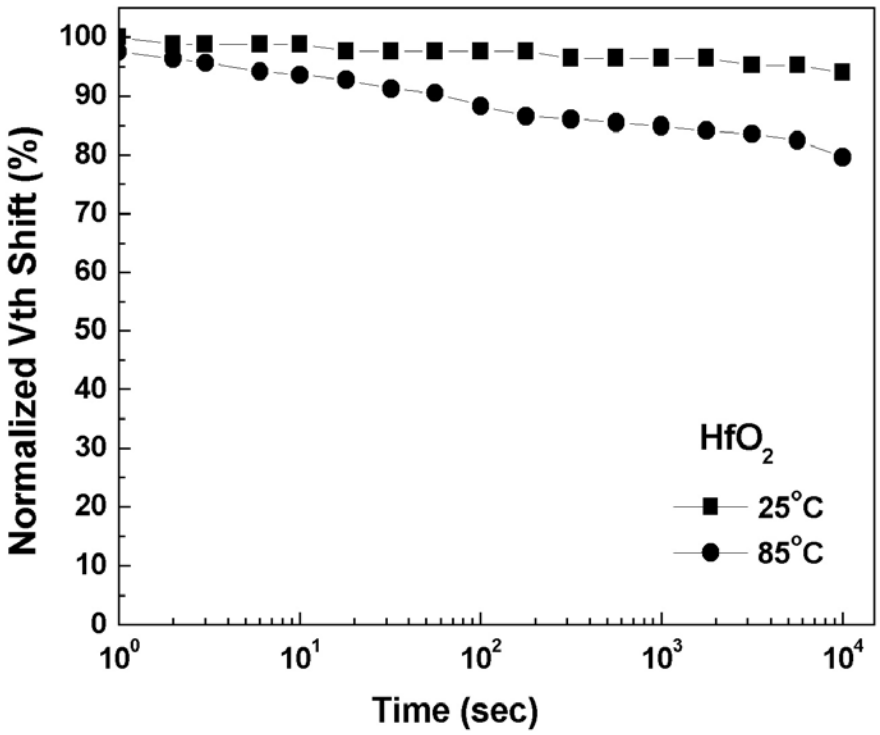

Figure 6.20 The data retention of Device A. The room temperature retention is only 6% charge loss as measure time up to 10^4 sec and ~20% charge loss at 85°C.

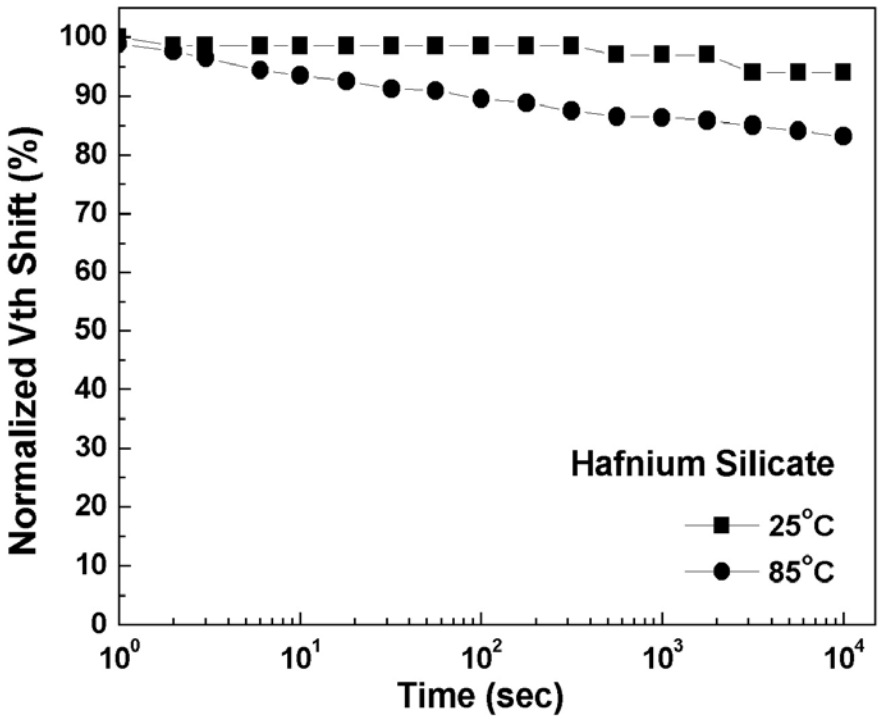

Figure 6.21 The data retention of Device B. The room temperature retention is only 6% charge loss as measure time up to 10^4 sec and ~18% charge loss at 85°C.

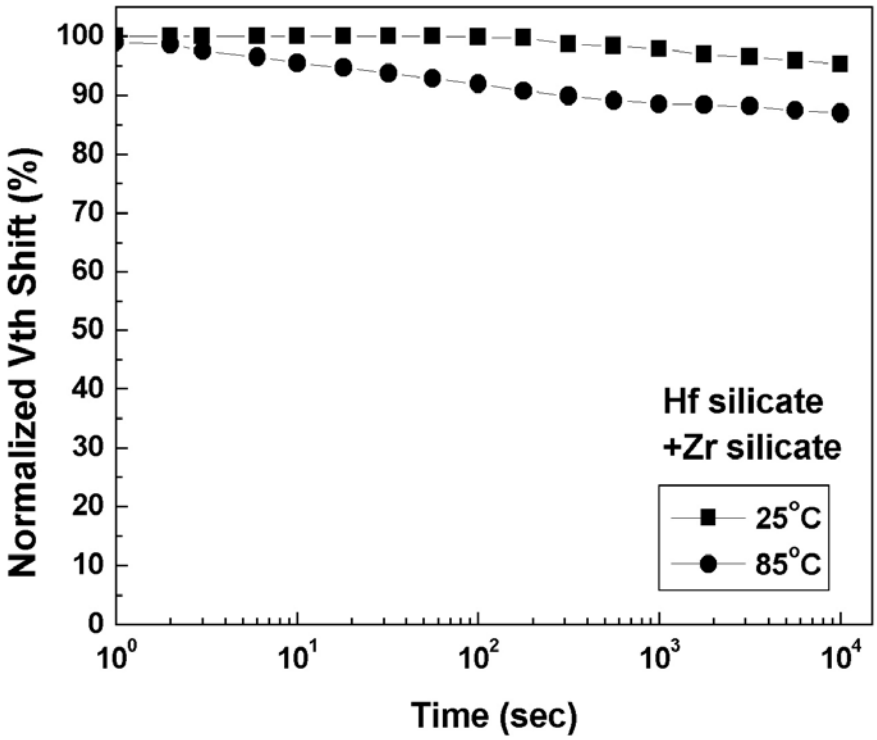

Figure 6.22 The data retention of Device A. The room temperature retention is only 5% charge loss as measure time up to 10^4 sec and ~13% charge loss at 85^{o}C.

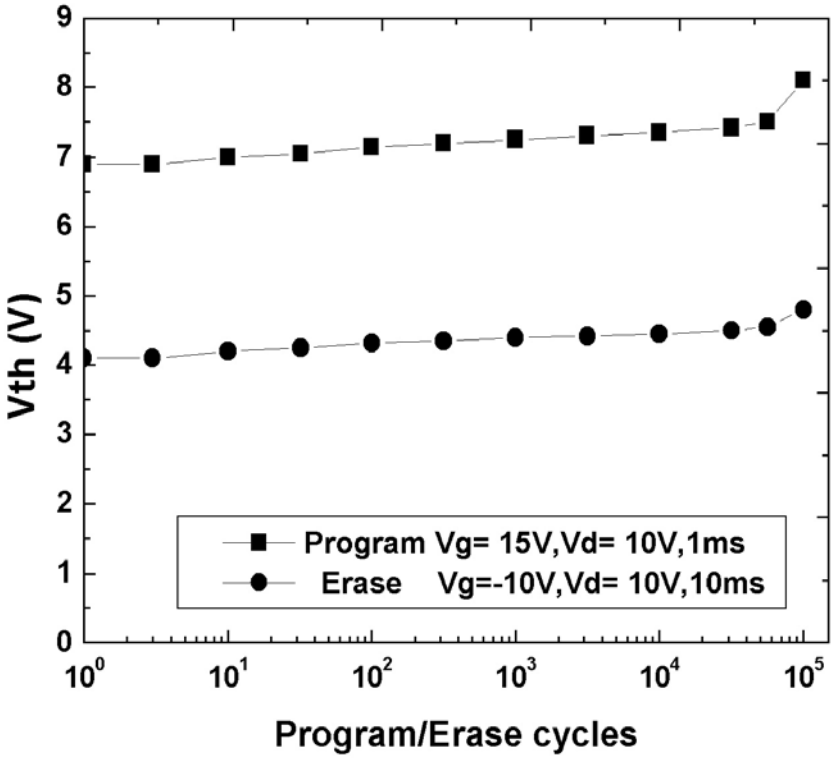

Figure 6.23 Endurance of Device A. The memory window is about 2.8V after 10^5 P/E cycles

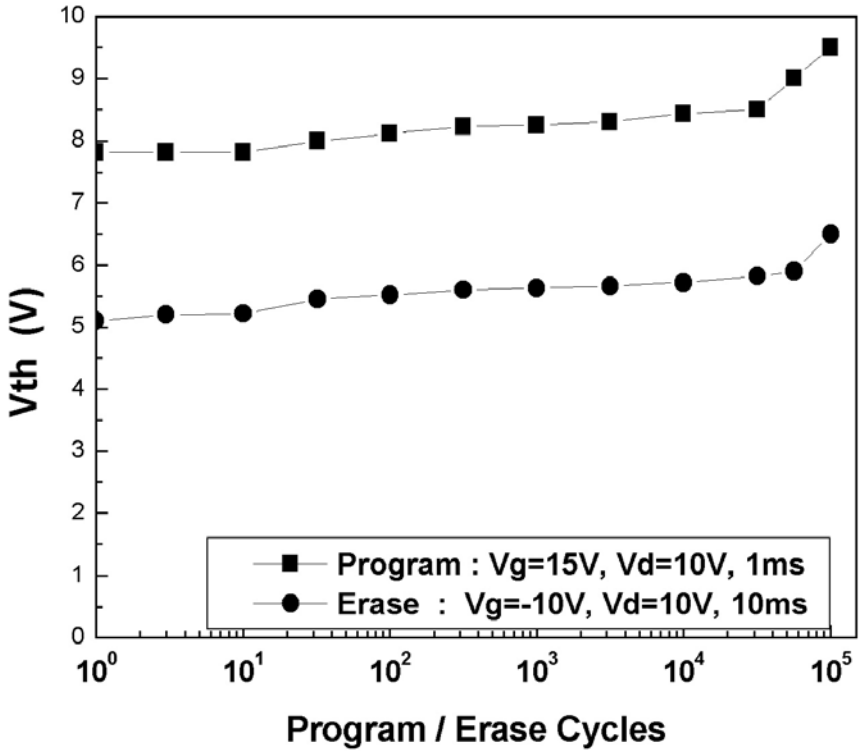

Figure 6.24 Endurance of Device B. The memory window is about 2.8V after 10^5 P/E cycles.

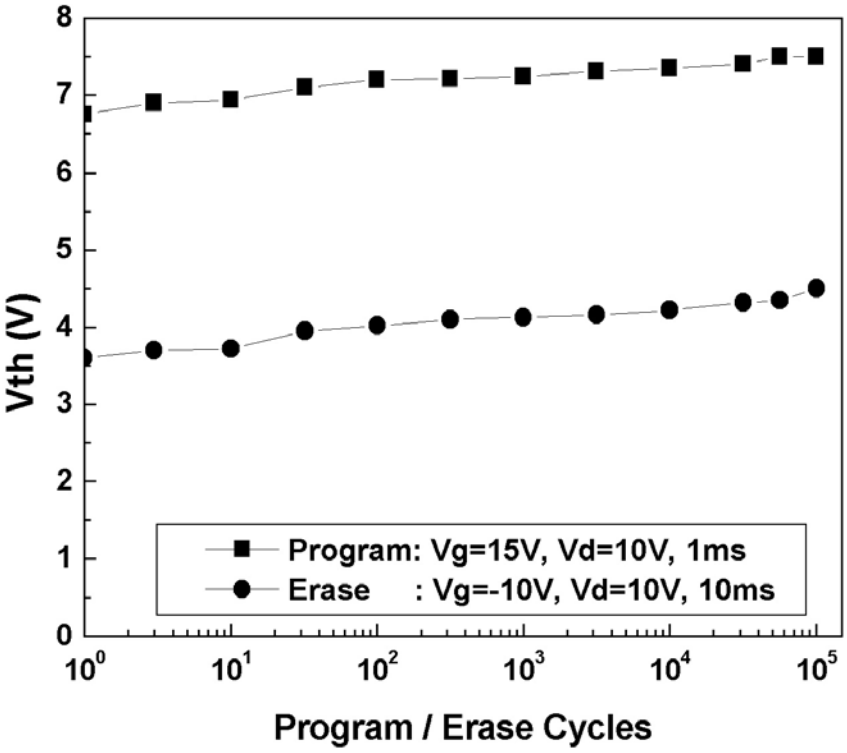

Figure 6.25 Endurance of Device C. The memory window is about 3V after 10^5 P/E cycles.

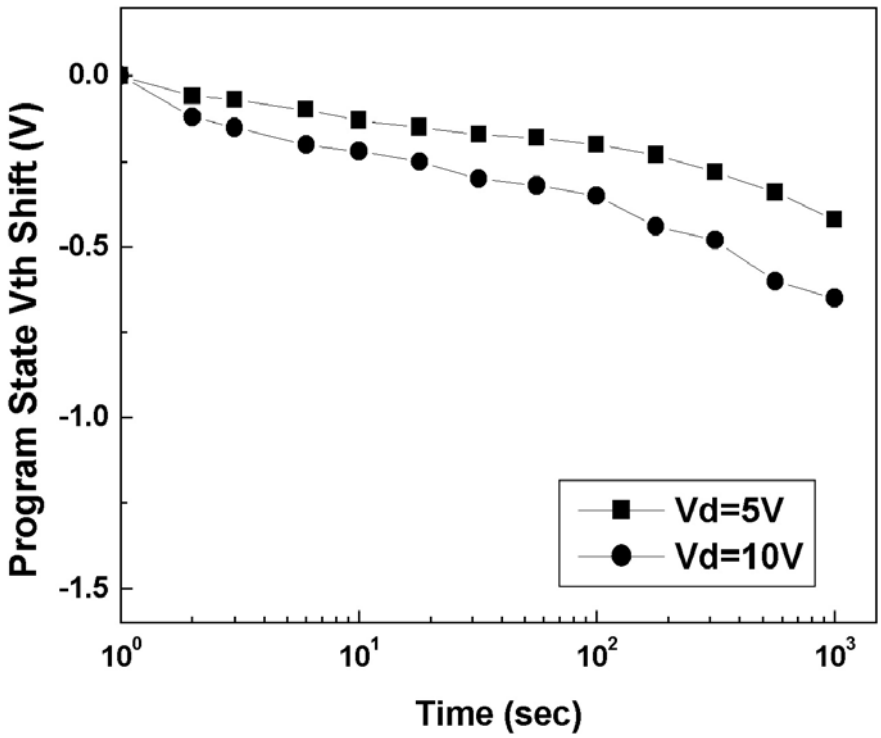

Figure 6.26 Drain disturbance of Device A.

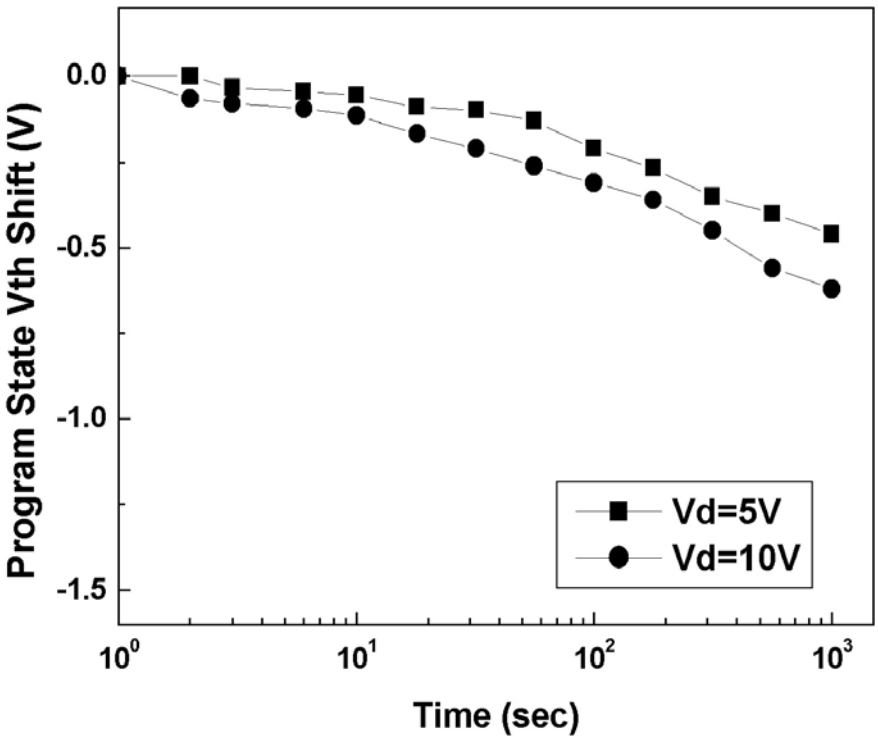

Figure 6.27 Drain disturbance of Device B.

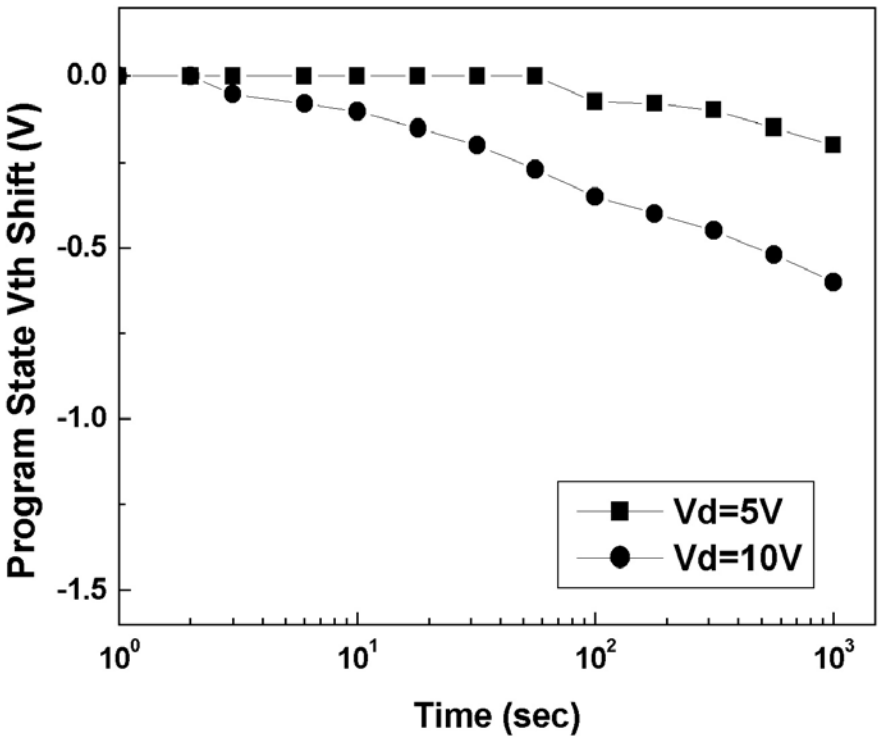

Figure 6.28 Drain disturbance of Device C.

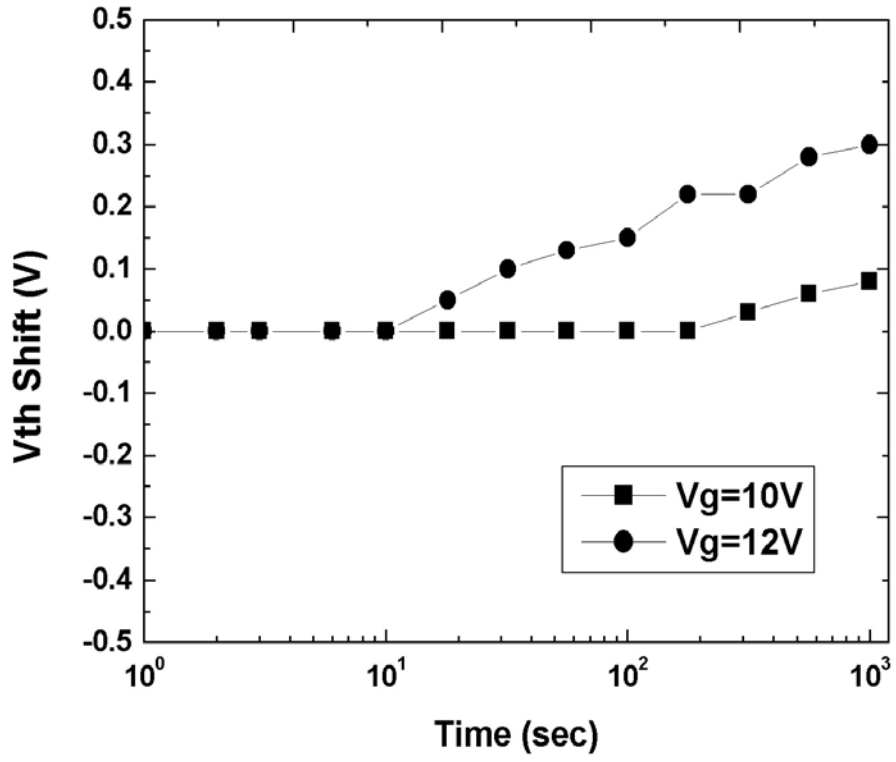

Figure 6.29 Gate disturbance of Device A.

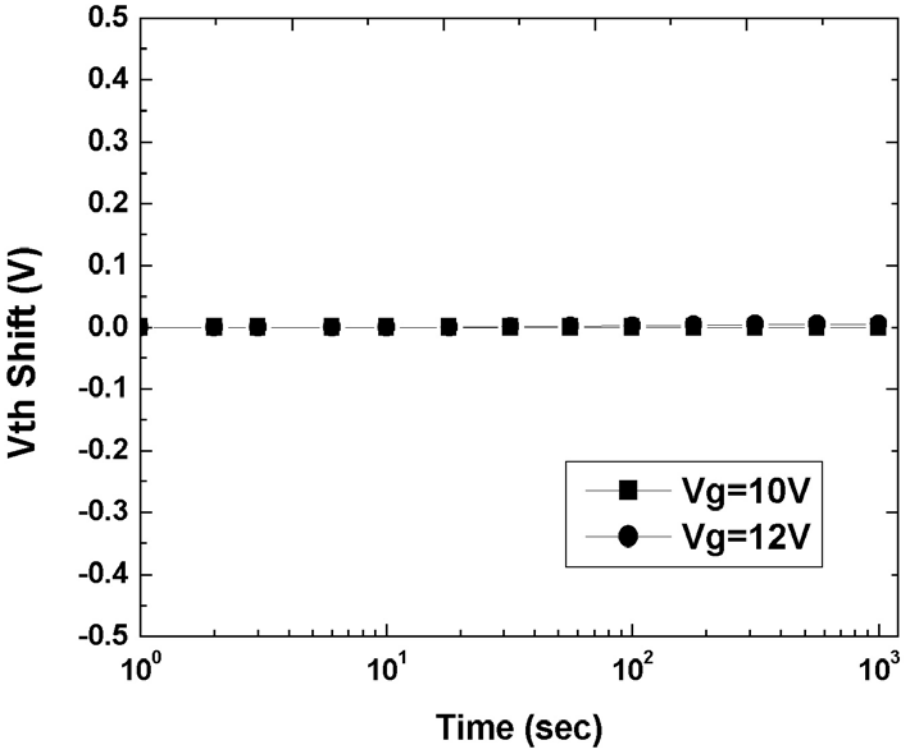

Figure 6.30 Gate disturbance of Device B.

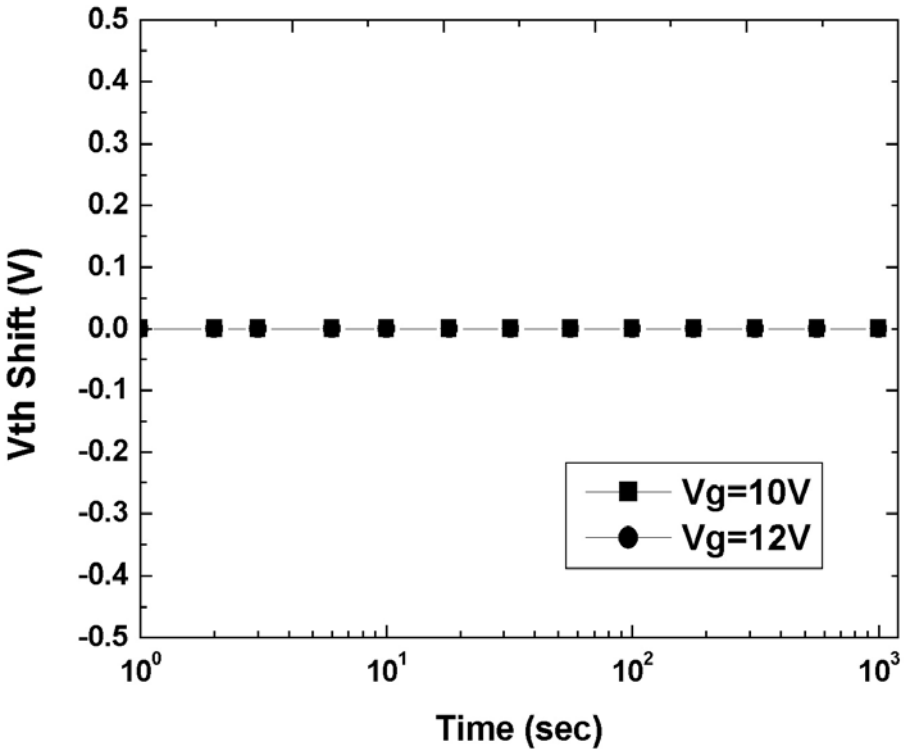

Figure 6.31 Gate disturbance of Device C.

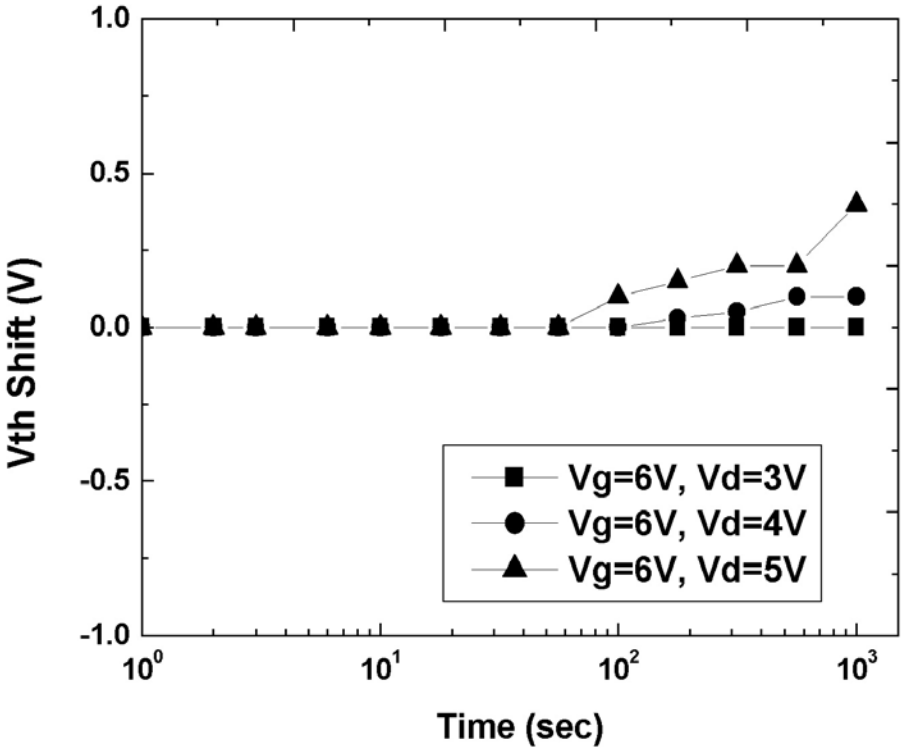

Figure 6.32 Read disturbance of Device A.

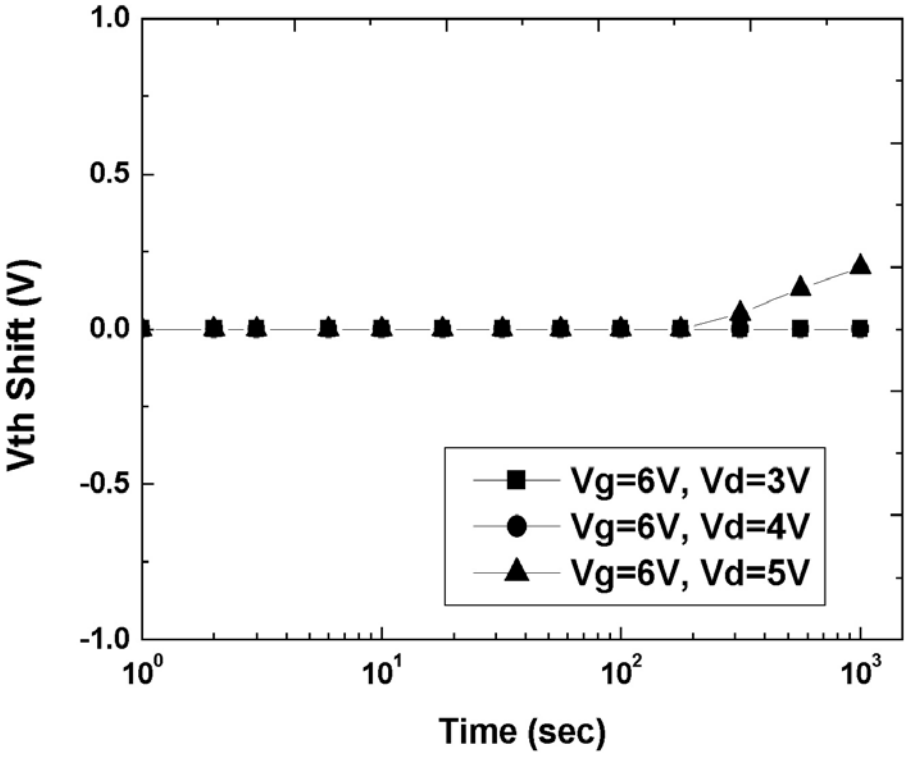

Figure 6.33 Read disturbance of Device B.

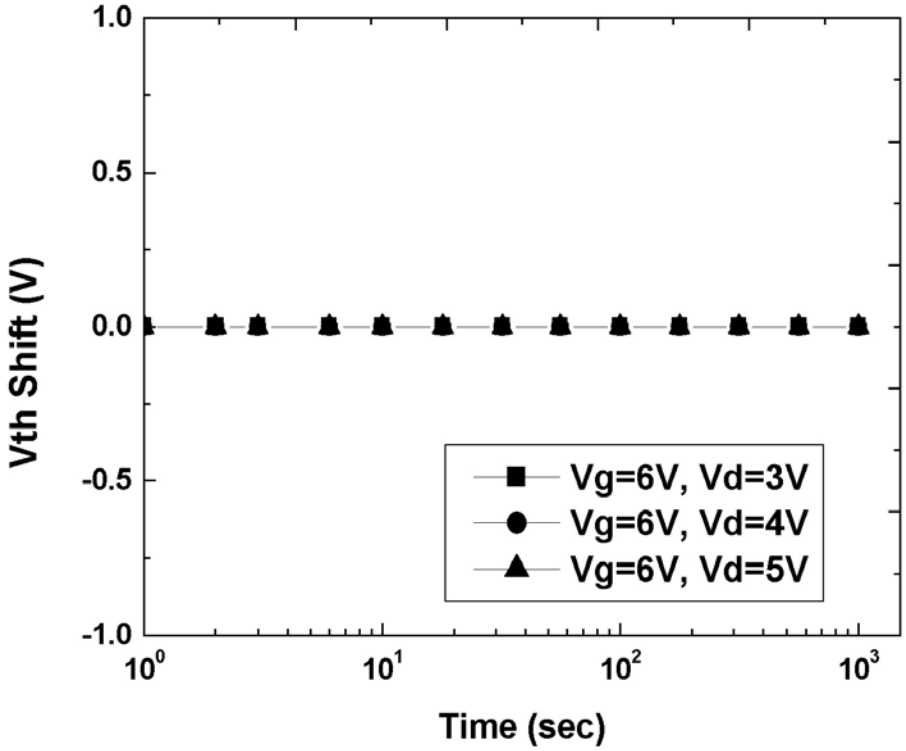

Figure 6.34 Read disturbance of Device C.

Table 6.1 The electrical characteristics comparison of Device A, B and C.

	A HfO_2	**B** Hf Silicate	**C** Hf Silicate + Zr Silicate
Id-Vg memory window	~ 3V	~ 3.3 V	~ 4V
Program Speed (1V Vth shift)	10 us ~ 100 us	10 us ~ 100 us	< 10 us
Retention charge loss @ 25°C	~ 6%	~ 6%	~5%
Retention charge loss @ 85°C	~ 20%	~ 18%	~ 13%
Endurance	up to 10^5 cycles	up to 10^5 cycles	up to 10^5 cycles

Chapter 7

Conclusions and Recommendations for Future Works

7.1 Conclusions

In this thesis, we propose a successful fabrication technique for preparing sub-60-nm contact holes in a silicon dioxide layer by electron-beam lithography. We have discussed in detail the many factors that influence the performance of the shrinkage process, such as the mixing-bake temperature, mixing-bake time, and hole dimensions before and after chemical shrinkage. Using this chemical shrinkage technique (mixing-bake of 110 °C for 70 sec) and an etch gas of CHF_3/CF_4 (1:1), we obtained a minimum hole dimension of 53 nm. This technology meets the requirements[2] for contact hole fabrication in the year 2009. We propose that a nano-hole effect occurs during the etch-assisted shrinkage reaction because smaller holes have a higher percentage of polymer deposition in the resist sidewall than do larger holes.

Then, in the chapter 3, we have established a successful fabrication technique that incorporated the fullerene molecules in the resist for preparing sub-50nm lines and sub-50 nm holes by electron beam lithography. The improvement of throughput is attributed to the better electron affinity of the fullerene. The prevention of line edge roughness and pattern collapse is also an advantage of this modification technology. Together with the above nanofabrication technique, the contact hole at nanometer scale is successfully filled with the CVD TiN. The proposed method can be applied to fabricate the nano-plugs in the future. In addition, the technique significantly enhances the etching selectivity of resist for plasma gases of CHF_3/CF_4 or Cl_2/O_2.

We have used this resist to fabricate various metal silicide gates, and the NiSi on poly-Si has the better electrical performance.

In the chapter 4, we have fabricated 50nm gate length nano-SOI FinFETs with deep Ni-salicidation and NH_3 plasma treatment. From the measured transistor characteristics, the narrow width device is performed better than the long width device. We also discuss the effect of Ni-salicidation and state-of-the-art NH_3 plasma treatment on the nano-SOI FinFETs. The deep Ni-salicided SOI FinFETs after NH_3 plasma treatment can achieve high performances like S.S = 66mv/dec and DIBL= 0.03V. The floating body effect and process-induced defects can be improved by deep Ni-salicidation and NH_3 plasma treatment in nano-SOI FinFETs. We believe that these key technologies are suitable and compatible for future nano-devices manufacturing.

Next, in chapter 5, we have proposed an attractive sol–gel method for preparing ultrathin films due to the advantages of low cost, and better thermal and electrical properties. The sol–gel method requires a lower degree of processing and provides highly homogeneous materials and the possibility of using annealing process to stabilize the film. We have prepared ZrO_2 ultrathin films of an amorphous phase by using the sol–gel method with $ZrCl_4$ as the metal halide. The electrical properties of the ZrO_2 thin films not only display their good electrical insulation with breakdown field up to 12.5 MV/cm, but also their improved thermal stability up to 900 ^oC against the crystallization. These ZrO_2 ultrathin films are readily produced by the sol–gel method and behave as suitable capacitors and coatings for insulating films.

Finally, in chapter 6, we use sol-gel spin coating method to fabricate HfO_2 layer, hafnium silicates nanocrystal, and co-existed hafnium silicates and zirconium silicates nanocrystal memory. The XPS analysis indicates the formation of HfO_2 layer, hafnium silicate and zirconium silicate after 900^oC 1min RTA. From the TEM image, we also demonstrate the co-existed hafnium silicate nanocrystal and zirconium silicate

nanocrystal and the size of one nanocrystal is 5nm. We have verified the device performance with the P/E speed, charge retention, endurance and disturbance measurement. The quality of the co-existed hafnium silicate and zirconium silicate nanocrystals formed by the sol-gel spin coating method and RTA treatment exhibits better properties in terms of larger Vth shift due to more trapping site existed, long charge retention time (5% loss at 10^4sec), good endurance (up to 10^5 P/E cycles) with no memory window narrowing and negligible gate and read disturbance due to SiO_2 surrounded the nanocrystal increased the tunneling oxide thickness.

7.2 **Recommendations for Future Works**

There are some topics that are suggested for future work:

(1) About Resist Nano-modification Technology, we will apply it on the conventional photoresist.

(2) Measure the contact resistance of nano-holes.

(3) Study the formation mechanism of sol-gel derived nanocrystal.

(4) Study other metal halides to form nanocrystals.

(5) Combine nanodevice fabrication technology with sol-gel derived nanocrystal to fabricate 50nm memory device.

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博士論文題目:

應用新穎微影及奈米微晶粒技術於奈米元件與記憶體之研究

Application of novel lithography and nano-crystal technique in the fabrication of nano-devices and memories

Publication Lists

1. International Journal:

[1] Wen Luh Yang, Wen-Fa Wu, **Hsin Chiang You,** Keng-Liang Ou, Tan Fu Lei, and Chang-Pin Chou,"Improving the Electrical Integrity of Cu–$CoSi_2$ Contacted n^+p Junction Diodes Using Nitrogen-Incorporated Ta Films as a Diffusion Barrier", *IEEE Trans. Electron Devices*, vol. 49, pp. 1947 – 1954, Nov. 2002

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[3] **Hsin-Chiang You,** Fu-Hsiang Ko, Tan-Fu Lei,"Resist Nano-modification Technology for Enhancing the Lithography and Etching Performance", *Microelectronic Engineering* pp.521-527, 2005

[4] **Hsin-Chiang You,** Fu-Hsiang Ko, Tan-Fu Lei,"Fullerene-Incorporated Technology on Enhancing the Electron Beam Resist Performance for Contact Hole Patterning and Filling", *Thin Solid Film*, vol.500, pp.214-218, 2006.

[5] **Hsin-Chiang You,** Fu-Hsiang Ko, Tan-Fu Lei,"Physical Characterization and Electrical Properties of Sol–Gel-Derived Zirconia Films", *Journal of the Electrochemical Society*, vol.153, pp.F94-F99, 2006.

[6] Tze-Hsiang Hsu, **Hsin-Chiang You**, Fu-Hsiang Ko, Jiang-Wen Huang, Tan-Fu Lei,"A PolySi-SiO_2-ZrO_2-SiO_2-Si Flash Memory using Novel Sol-Gel ZrO_2 Charge Trapping Layer", accepted for publication in *Journal of the Electrochemical Society*.

2. International Letter:

[1] **Hsin-Chiang You**, Tze-Hsiang Hsu , Fu-Hsiang Ko, Jiang-Wen Huang, Wen-Luh Yang, Tan-Fu Lei,"SONOS Type Flash Memory Using an HfO_2 as a Charge Trapping Layer Deposited by the Sol-Gel Spin Coating Method", accepted for publication in *IEEE Electron Device Letters*.

[2] **Hsin-Chiang You**, Tze-Hsiang Hsu , Fu-Hsiang Ko, Jiang-Wen Huang, Tan-Fu Lei,"Hafnium Silicate Nanocrystal Memory Using Sol-Gel Spin Coating Method", accepted for publication in *IEEE Electron Device Letters*.

[3] **Hsin-Chiang You,** Po-Yi Kuo, Fu-Hsiang Ko, Tien-Sheng Chao, Tan-Fu Lei,"The impact of deep Ni salicidation and NH_3 plasma treatment on nano-SOI FinFETs", accepted for publication in *IEEE Electron Device Letters*.

3. International Conference:

[1] **Hsin-Chiang You,** Fu-Hsiang Ko, Tan-Fu Lei, Chun-Chen Hsu, Tieh-Chi Chu, "Chemical shrink Techniques for Sub-100nm Contact Hole Fabrication in Electron Beam Lithography", *International Electron Devices and Materials Symposium (IEDMS)*, pp. 457-460, Dec. 2002

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4. Local Conference:

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5. Patents

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