國立交通大學

電機與控制工程系

碩士論文

利用雜訊功率模型、非線性失真模型
與功率消耗模型，以最佳化離散時間
單迴路積分三角類比數位轉換器

Design Optimization of Discrete-Time Single-Loop Sigma-Delta ADCs based on Analytical Models of Noises, Nonlinear Distortions, and Power Consumptions

研 究 生：李孟學

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中 華 民 國 九 十 六 年 八 月

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摘要

傳統的積分三角類比數位轉換器電路規格設計是一個相當耗時的工作，且需要不斷的嘗試各種電路規格，以達到所需要的解析度。本篇論文分析了積分三角類比數位轉換器的主要雜訊來源與非線性特性所造成的失真問題。藉由分析推導出的失真功率模型、雜訊功率模型及絕對功率消耗模型，並以訊號對雜訊和失真比(SNDR)來當作我們的設計規格，以做最佳化的設計。此最佳化設計意指在特定系統規格下(如頻寬、訊號對雜訊和失真比)，找到一組最佳化的設計參數，使得類比數位轉換器的功率消耗最小以及訊號對雜訊和失真比最大，並節省龐大制定電路規格的時間成本。最後我們將針對已發表的設計結果來做驗證的工作。雖然現今已存在相當多行為模擬工具以自動化制定電路規格，但較之下，本論文所提出的最佳化方法將快上許多。

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ABSTRACT

The conventional sigma-delta ADC design approach is a time consuming process and needs much trials and errors. This paper analyze the mainly noise sources and nonlinear distortions. Utilizing the noise power models, nonlinear distortion power models and accurate power consumption models derived in this paper, and the assigned signal to noise and distortion ratio (SNDR) to be the design goal, we can forward to do design optimization under the specific specifications. Design optimization means that under the specific specifications (signal bandwidth, SNDR), we find a set of optimal design parameters such that the power consumption of ADCs is minimum and SNDR is maximum, and reduce the huge time-cost to set up the circuit specifications. Finally, design optimization is tested against a published design result. Although design automation issues have been partially addressed by recent behavior- simulation–based methods, yet such methods can be slower than our analytical approach far.

誌謝 Acknowledgment

我要將此論文獻給

我親愛的母親-廖甚 女士

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我今生的摯愛-潘昭佑 小姐

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Contents

Lists of Tables

Lists of Figures

List of Symbols

Symbols

V_{LSB}	Quantizer step size
V_{OS}	Maximum output swing of op-amp
OSR	OverSampling Ratio
n	Order of the Sigma-Delta modulator
B	Number of bits in the quantizer
f_S	Sampling Frequency
f_B	Signal Bandwidth
V_{ref}	Reference Voltage of the quantizer
A_0	Finite Gain of OTA
f_{in}	Frequency of the input signal
ϕ_i	ith phase of a nonoverlap clock
A_{in}	Amplitude of input signal
$\sigma_{jit.}$	standard deviation of clock jitter
C_S	Sampling capacitor
C_I	Integrating capacitor
C_L	Load capacitor of OTA
C_{Logic}	The loading capacitors of CMOS logic gates
C_{gate}	The gate capacitances of all CMOS transmission gates
C_{OX}	The capacitance per unit area of the gate oxide
V_S	Input signal plus feedback DAC signal
τ_1	Time constant of input branch
σ_{VS}	Standard deviation of V_S
τ_2	Time constant of integrator output settling
a_i	gain coefficient of i th integrator

η	percentage of the bottom plate parasitic
T	Absolute temperature
R	Switch ON resistance
N	quantizer levels
gm1	Amplifier transconductance
Pr()	Probability of some condition
$\sigma_{cap.}$	Mismatch of unit capacitance
k	Boltzmann's constant (1.38×10^{-23}) J/K
α	OTA noise factor
$Erf[]$	Error Function
I_{OTA}	Total current of the OTA
I_B	Bias current of each transistor of the input differential pair of OTA
k_{OTA}	The ratio of the total current of the OTA to this bias current
f_{cl2}	The *GBW* of the OTA
V_{reff}	The overdrive voltage of the transistor of the input differential pair of OTA
k_{Cs}	The ratio between the summation capacitance of C_S in all stages and the one in the first stage
ε_0	The permittivity of free space
N_S	The number of the CMOS transmission gate in $\Sigma\Delta$ modulator

1
Introduction

1.1 Current Status and Background

Sigma-Delta A/D converters have become popular for high-resolution medium-to-low-speed applications such as digital audio [Bos 88][Nor 89], voice codec, and DSP chip. Recently, ΣΔ ADCs have been applied to higher bandwidth signals, and low power designs are frequently emphasized. For example, in ×DSL [Gag 03][Rio 04] applications, signals up to several MHz must be handled. Since significantly increasing the sampling rate is difficult, designers either seek to increase the order or the cascade stages [Oli 02][Vle 01], or employ multi-bit quantization [Gri 02][Mil 03], or both, in order to achieve the required dynamic range. DAC linearity can be improved due to process technology advances, making the multi-bit architecture more popular. The ΣΔ modulator design is a complex and time consuming process because many coupled design parameters must be determined. Coming up with an acceptable design is very challenging with increasing design specification demands, previously described. Even an acceptable design may not be the best one. We propose an optimization approach to increase automation and reduce complexity in the single-loop ΣΔ ADCs design.

1.2 Motivation and Aims

To propose the design optimization for single-loop ΣΔ modulators, we need a complete set of important nonideality models and the power consumption model. Some issues concerning ΣΔ modulator noise and error modeling appeared in [Bos 88][Nor 89][Mal 03]. The performance of the ΣΔ ADCs is usually expressed in terms of SNR and SNDR. Circuit designers must take into consideration the nonidealities and decide the circuit and system

parameters to meet the desired specifications. A design optimization procedure is proposed in [Chu 05] to meet design specifications while minimizing power consumption. However, it didn't consider the nonlinear distortions, so that the effectiveness of the proposed design optimization is limited. In this work, we discuss all the important nonlinear distortions, and incorporate relevant distortion powers into the optimization process in order to achieve more realistic designs.

In a ΣΔ modulator, common causes for harmonic distortions are nonlinear finite-OTA-gain, settling error, nonlinear capacitances, quantizer nonlinearity, nonlinear switch resistance and unit-DAC mismatch. Operational amplifiers (op-amps) are the critical part of the ΣΔ modulators and its nonidealities such as nonlinear finite-OTA-gain and settling error may produce distortions significantly. Some analyses of the distortions resulting from nonlinear finite-OTA-gain and settling error are given in [Med 94][Dia 94]. In [Med 94], the settling distortion has been modeled. However, the model provides little insight on how settling distortion are related to circuit and system parameters and it had a mistake. In this work, we correct this mistake and discuss the harmonic distortion how to vary with circuit and system parameters and what condition it can be ignored. Then we will apply the model and discuss to our design optimization. The nonlinear finite-OTA-gain distortion is caused by the gain variation of op-amp, whose power model is not complete in [Med 94] [Dia 94][Gee02] and [Lee85], so we build the complete distortion power model for 0.18μm process, and involve it in optimization

Recently, with the advanced technology, multi-bit modulators are used often because it offers many advantages. However, multi-bit modulators can introduce significant distortion into the modulator loop due to the unit-DAC mismatch. Any error in the DAC response will be directly subtracted from the input signal and hence it appears at the output without the benefit of noise shaping. Therefore any nonlinearity of the DAC will introduce a corresponding nonlinear signal distortion into the overall ADC response. Some analyses about

DAC nonlinearity appeared in [Stu 01][Bru 99]. The derived distortion models in [Stu 01][Bru 99] are not expressed in harmonic power forms, and the relations between circuit parameters and distortion powers are not clear. In this work, we derive the harmonic distortions in terms of quantization level and standard deviation of capacitor mismatch, and the distortion model can help us do design optimization to determine the quantizer output level.

One straightforward approach to improve the accuracy of the internal DAC is to improve the matching of the individual elements. The most common approach for improving the accuracy of a DAC is dynamic element matching (DEM). Many dynamic element matching algorithms have been proposed to convert the static error into a wide-band noise signal [Bai 01][Kuo 95][Car 89]. ΣΔ modulators using DEM can reduce the distortion but it increases the extra hardware and consumes more power.

These nonidealities described above are important when the specifications of the modulator are demanding because they can become the dominant error sources. In this work, we have the noise and distortion models of all important nonidealities and power consumption model for design optimization. The design of ΣΔ modulators is a complex and time consuming process. With these models for design optimization, we can increase the automation and reduce complexity in the single-loop ΣΔ ADCs design.

1.3 Organization

This work is organized as follows. In Chapter 2 and Chapter 3, systematic studies of fundamental theory and various architectures of ΣΔ modulator are presented first. In Chapter 4, analyses of several errors which may degrade system performance are proposed. In Chapter 5, analyses of several distortions are proposed. The accurate power consumption model is derived in Chapter 6. A design optimization scheme is proposed in Chapter 7. It essentially combines system and circuit level designs, and optimizes all design parameters at

the same time. The optimization scheme is verified in Chapter 8, and various issues are discussed. Conclusions and future works are presented in Chapter 9.

2

Fundamental Theorems of Sigma-Delta Modulators

Before we establish the error models of ΣΔ modulators, several important theorems and concepts must be known, such as Nyquist sampling theorem, quantization error and the two most critical techniques in a ΣΔ modulator: oversampling and noise shaping. All topologies of ΣΔ modulators are based on these two techniques. There also have some parameters we must to understand, such as OSR, SNR, and SNDR …etc. This chapter starts from fundamental theorems, and introduces several topologies of ΣΔ modulators.

We will illustrate quantization error and analyze quantization noise in an ideal A/D converter and then derives the peak signal-to-noise ratio. The resolution of an A/D converter is determined by signal-to-noise ratio, which is a very important specification in an A/D converter.

2.1 Nyquist Sampling Theorem

In an analog-to-digital converter, the analog signal from external environment must be converted to discrete-time signal by sampling. However, the sampling rate (fs) and signal bandwidth (f_B) must follow the Nyquist sampling theorem in (2.1):

$$f_S \geqq 2f_B \qquad (2.1)$$

The sampling rate must be higher or equal to twice of signal bandwidth in order to prevent from aliasing. We will illustrate the phenomenon of aliasing by Fig. 2.1. Fig. 2.1(a) and (b) are the spectrums of signal and sample function respectively; from fig. 2.1(c), when sampling rate is twice higher than signal bandwidth, the signal after sampling has no aliasing and it can be perfectly reconstructed by using low pass filters. However, in Fig. 2.1(d), when the

sampling rate is lower than twice of signal bandwidth, aliasing will appear in the signal after sampling. The signal having aliasing is difficult to reconstruct to original signal [Mach 96], like Fig. 2.1(e).

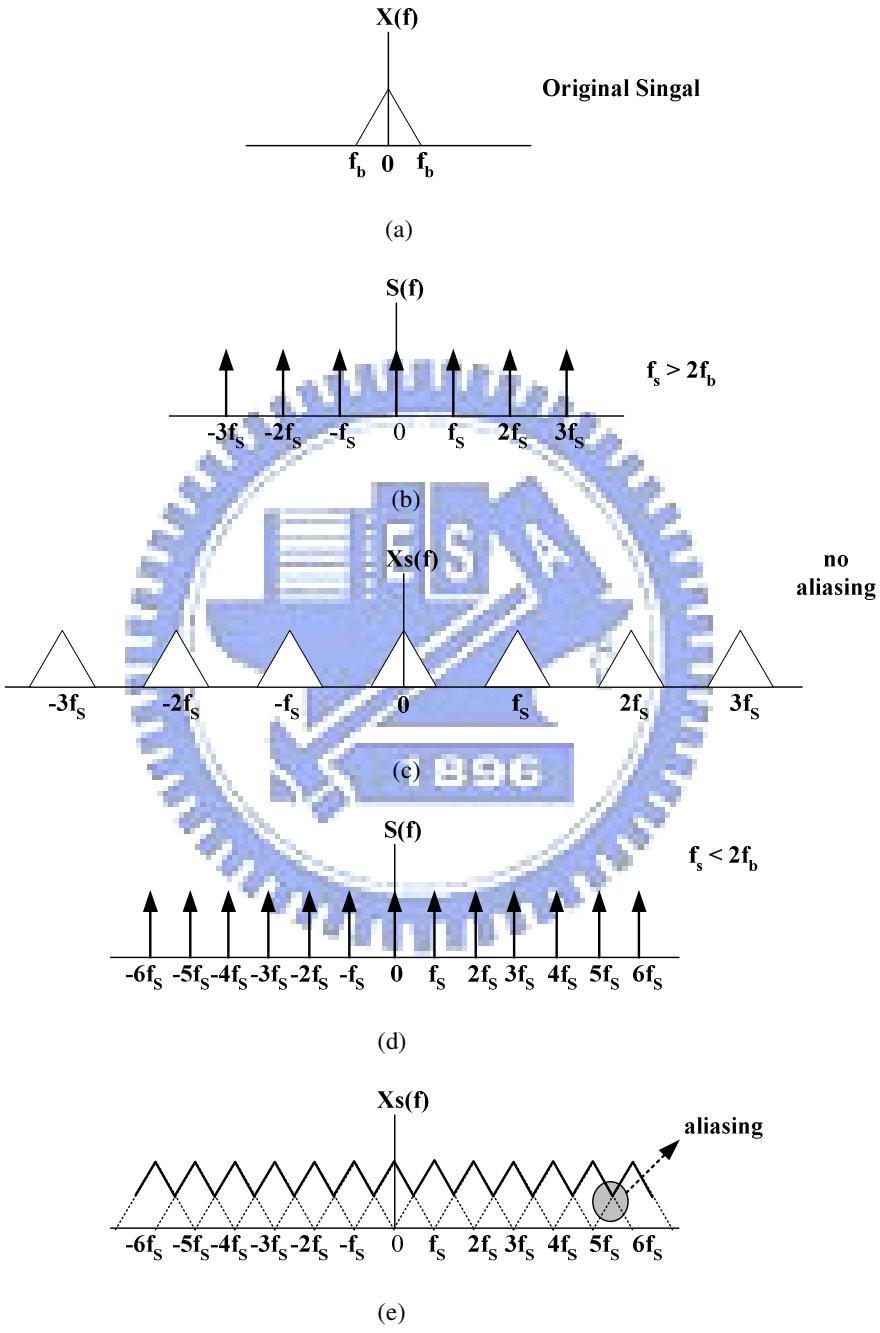


Fig. 2.1（a）Original signal spectrum（b）Sample function when fs > 2fB（c）Signal spectrum that' sampled by (b)（d）Sample function when fs < 2fB（e）Signal spectrum that sampled by (d)

2.2 Quantization noise and Peak SNR

We can get a discrete-time signal by sampling a continuous-time signal, and this sampled signal can be converted to digital signal. Quantization will appear in this process, the basic concept of quantization is to classify the original signal to different levels according to its level to determine the bit number of this signal, as shown in Fig. 2.2

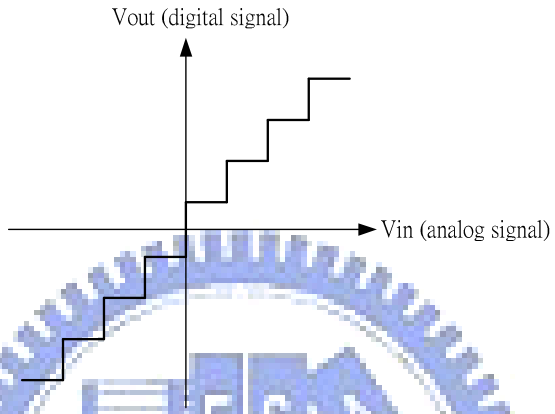


Fig. 2.2 Quantization process

It will have quantization error even in an ideal analog-to-digital converter. As shown in Fig .2.3, we convert the digital signal B to analog signal V_I by a D/A converter, and then the signal V_I is subtracted by input signal Vin. The result is the quantization error V_Q, as in (2.2) [Joh 97].

$$V_Q = V_{in} - V_I \qquad (2.2)$$

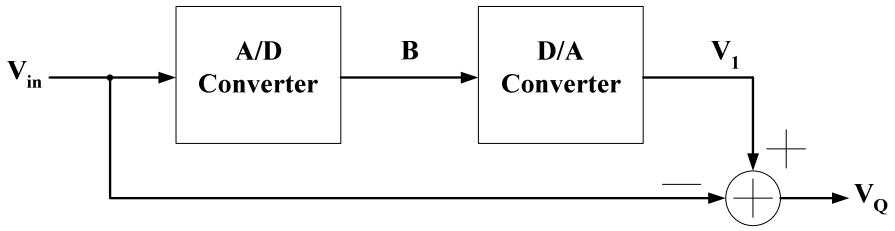


Fig. 2.3 Quantization error caused by A/D converter

The range of quantization error is limited in $\pm V_{LSB}/2$ (as in Fig. 2.4), and we assume the

probability density function of quantization error is uniformly distributed between $\pm V_{LSB}/2$ and its mean is zero, as shown in Fig. 2.5. From this assumption, we can easily get the quantization noise power $V_{Q(rms)}^2$ in (2.3).

$$V_{Q(rms)}^2 = \int_{-\infty}^{\infty} x^2 \cdot f_Q(x) \cdot dx = \frac{1}{V_{LSB}} \int_{-VLSB/2}^{VLSB/2} x^2 \cdot dx = \frac{V_{LSB}^2}{12} \qquad (2.3)$$

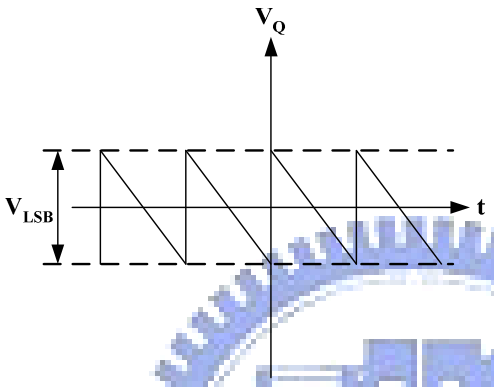


Fig. 2.4 Quantization error range

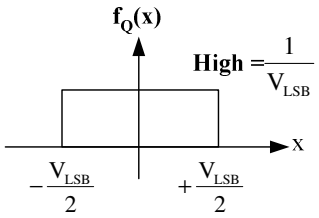


Fig. 2.5 P.D.F of quantization error

From (2.3) we can know the quantization noise power is proportional to square of V_{LSB}, and V_{LSB} can be represented as in (2.4). Therefore, we can say that the quatization noise will reduce by increasing quantization bit number.

$$V_{LSB} = \frac{FS}{2^B} \qquad (2.4)$$

FS=Full scale = $V_{ref+} - V_{ref-}$ B：Quantization bit number

Assume that input signal is sinusoidal, expressed as $V_{in}(t) = A \sin\omega t$, so the input signal power $V_{in(rms)}^2$ is as （2.5）. In （2.5）, we define the amplitude of input signal is the full scale of reference voltage, and from (2.3), (2.4) and (2.5), the peak SNR(Peak Signal-to-Noise Ratio) can be derived as in (2.6).

$$V_{in(rms)}^2 = \frac{1}{T} \int_{-T/2}^{T/2} (A \cdot \sin \omega t)^2 \cdot dt = \frac{A^2}{2} = \frac{(2A)^2}{8} = \frac{FS^2}{8} \qquad (2.5)$$

$$PSNR = 10 \log \left(\frac{V_{in(rms)}^2}{V_{Q(rms)}^2} \right) = 6.02B + 1.76 \text{ dB} \qquad (2.6)$$

(2.6) is the result obtained by Nyquist sampling rate. From (2.6), we can know that each

additional bit number in quantizer increases 6dB in SNR. In Nyquist A/D converters, increasing the resolution of quantizer (decrease V_{LSB}) while reducing the quantization noise is a general method to reach higher SNR, but this method is sensitive to mismatches of analog device. Therefore, the general Nyquist A/D converter is not easily to implement with high resolution.

2.3 Techniques of Sigma-Delta Modulator

ΣΔ A/D converters are based on oversampling and noise shaping to reach high resolution. Oversampling means the sampling rate is much higher than Nyquist rate, about 8~512 times in general applications. The goal of oversampling is to expand quantization noise to wider range. It can reduce the quantization noise in signal bandwidth and increase the DR (Dynamic range) of input signal. Noise shaping is a technique that moves noise to high frequency, which is done by using discrete time filter and feedback technique. After noise shaping, the noise in high frequency can be filtered out by a digital filter [Nor 97].

2.3.1 Oversampling Technique

First, we made the assumption that quantization noise is a uniform distribution in sampling spectrum so its mean is zero and is a white noise [Raz 01]. The system in Fig. 2.6 just has oversampling function and does not have noise shaping effect. If a A/D converter is sampled in Nyquist rate, then the quantization noise is uniform distributed between $\pm f_B$; if it is sampled by oversampling technique, then quantization noise is uniform distributed between$\pm$ $f_{S2}/2_s$, which is much larger than f_B. As shown in Fig. 2.7, if the signal bandwidth is between $\pm f_B$, then quantization noise in this bandwidth will be reduced by using oversampling technique, which will raise PSNR significantly.

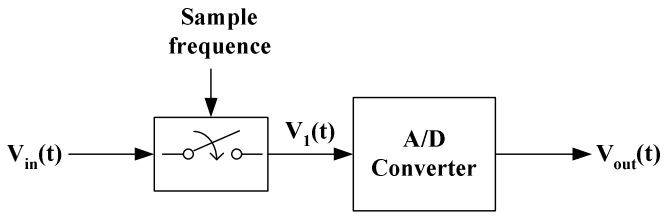


Fig. 2.6 Sampling system

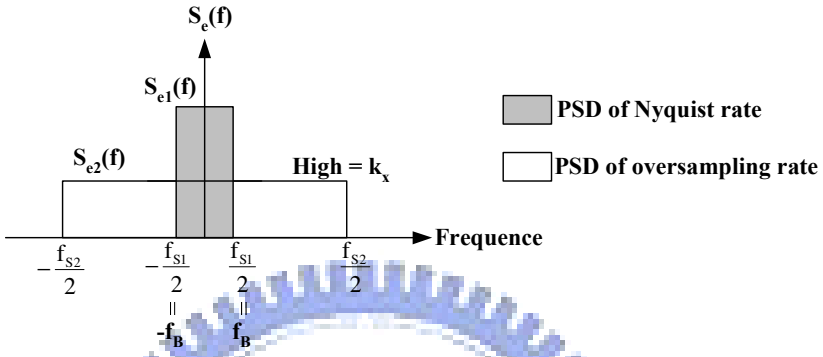


Fig. 2.7 Noise distribution after sampling

In the condition of oversampling, the PSD (Power Spectrum Density) of quantization noise is as $S_{e2}(f)$ in Fig. 2.7 and can be represented as:

$$k_x^2 = \frac{V_{LSB}^2}{12 \cdot f_s} = S_{e2}^2(f) \qquad (2.7)$$

From (2.7) we can estimate the quantization noise in $2f_B$ after oversampling

$$P_Q = \int_{-f_B}^{f_B} k_x^2 \cdot df = \frac{2f_B}{f_s} \cdot \frac{V_{LSB}^2}{12} = \frac{FS^2}{12 \cdot 2^{2B} \cdot OSR} \qquad (2.8)$$

In (2.8), we define a parameter OSR (Oversampling Ratio) as

$$OSR = \frac{f_s}{2f_B} \qquad (2.9)$$

Finally, we can get PSNR from (2.5) and (2.8)

$$PSNR = 10 \log \left(\frac{P_{signal}}{P_Q} \right) = 6.02B + 1.76 + 10 \log (OSR) \qquad (2.10)$$

From (2.10), we can find that doubling OSR will increase 3dB in PSNR, which is about 0.5 bit increase in resolution. Although oversampling can reduce quantization noise, it is difficult

to reach high SNR when using a low bit quantizer. For example, if we need a 16bit A/D converter, then SNR must be equal to 98dB, if the signal bandwidth is 20KHz, then the sampling rate must equal to $2 \times 10^9 \times 20\text{KHz}$, it is impossible to implement. Because at such high frequency, quantization noise is no longer a white noise, it is correlated with input signal. So there is not only oversampling technique, we must add noise shaping technique also, if we want to achieve high resolution.

2.3.2 Noise Shaping

We can model a general ΣΔ modulator and its linear model as shown in Fig. 2.8.

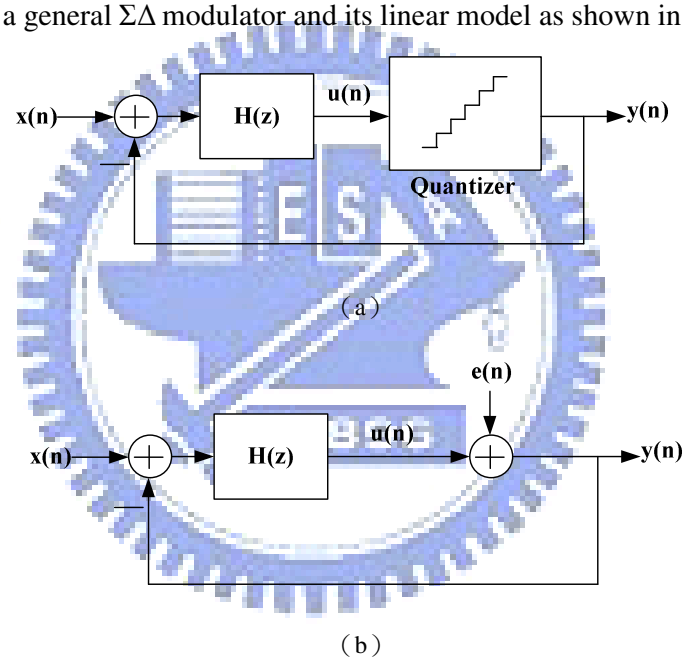


Fig. 2.8 (a) General ΣΔ modulator (b) Linear model with quantization noise

From Fig. 2.8(a), we can derive output Y(z) as (2.11)

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z) \qquad (2.11)$$

and define Signal Transfer Function S_{TF} and Noise transfer function N_{TF} as

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \qquad (2.12)$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \qquad (2.13)$$

where H(z) is the transfer function of a discrete time filter. There have two important meanings in (2.12), (2.13). If we want to obtain highest SNR, S_{TF} must be equal to 1, that means the input signal can transfer to output without attenuating; and N_{TF} (z) must be equal to 0, because the quantization noise will not affect output SNR.

In order to make N_{TF} (z) be a high pass filter, so at DC(z = 1), N_{TF} must be 0, and z = 1 is a pole of H(z), so the transfer function H(z) of the discrete filter is as

$$H(z) = \frac{1}{Z-1} = \frac{Z^{-1}}{1-Z^{-1}} \qquad (2.14)$$

Substitute (2.14) into (2.12) and (2.13), we can get

$$S_{TF}(z) = \frac{1}{z} \qquad (2.15)$$

$$N_{TF}(z) = 1-\frac{1}{z} \qquad (2.16)$$

And we substitute z with $e^{j\frac{2\pi f}{fs}}$, then we can plot $|S_{TF}(f)|^2$ and $|N_{TF}(f)|^2$ in frequency domain, as Fig. 2.9. We can find $|N_{TF}(f)|^2$ also increases with frequency, and $|S_{TF}(f)|^2$ is always equal to 1, if we choose signal bandwidth in low frequency, then we can get highest signal power and lowest noise power, from this figure we see that quantization noise is moved to higher frequency significantly, this is the noise shaping effect.

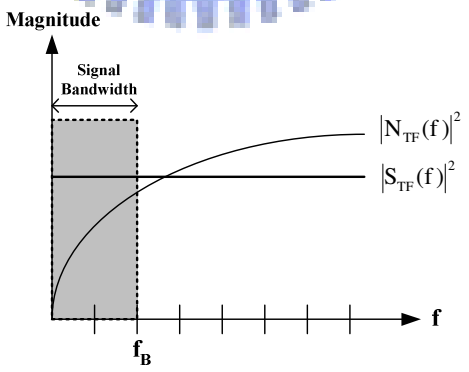


Fig. 2.9 Noise shaping

After noise shaping, we can filter out the noise in high frequency by using digital filter, and we will illustrate its architecture more detail in the next chapter.

3
Architectures of Sigma-Delta Modulator

Before we introduce various architectures of ΣΔ modulators, we must to realize the basic architecture of a general ΣΔ A/D converter. Fig. 3.1 is a complete block diagram of a ΣΔ A/D converter [Joh 97], and we can divide it into two different parts. First part is the ΣΔ modulator. The main function of this part is doing oversampling and noise shaping to the input analog signal. Second part is the decimation filter. The main function of this part is to remove noise in high frequency and down sampling the sampling frequency to base band frequency.

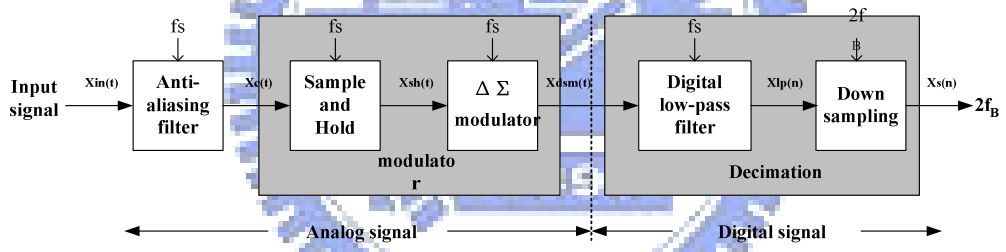


Fig. 3.1 Block diagram of ΣΔ A/D converter

First, the input signal Xin(t) pass an Anti-aliasing filter, the 3dB frequency of this filter is about few times of Nyquist frequency, so signal and noise out of Nyquist frequency is filtered roughly, and this signal goes into the ΣΔ modulator after goes through a S/H circuit. However, in the circuits implement situation, the sample and hold function is included in the circuits of ΣΔ modulator, so the signal Xc(t) will pass this modulator and produces a high speed data code Xdsm(n), because of noise shaping, the quantization noise will appear in high frequency. Finally, we must filter the noise in high frequency and reduce the sampling frequency to Nyquist frequency by a decimator, and passes the digital signal to the output

[Joh 97].

In this chapter, we will focus on the architectures of ΣΔ modulator, because that the noise model and optimal method is focus on this part, we must understand the theorem, benefits and drawbacks of each kinds of ΣΔ modulators. In addition, the implement of decimator is very typical [Ner 02][Mok 94]. In today's technology, DSP processors are also used to replace decimators, so we will introduce this part roughly.

3.1 First-Order Sigma-Delta Modulator

We recall that H(z) in (2.14) is $\frac{Z^{-1}}{1-Z^{-1}}$, substitute it into Fig. 2.8, then we can get a first-order ΣΔ modulator; Analyze transfer function H(z) from time-domain, it indicates that output signal m(t) is obtained by adding the delayed input signal n(t-1) and the delayed output signal m(t-1), so we can express a complete first-order ΣΔ modulator as Fig. 3.2.

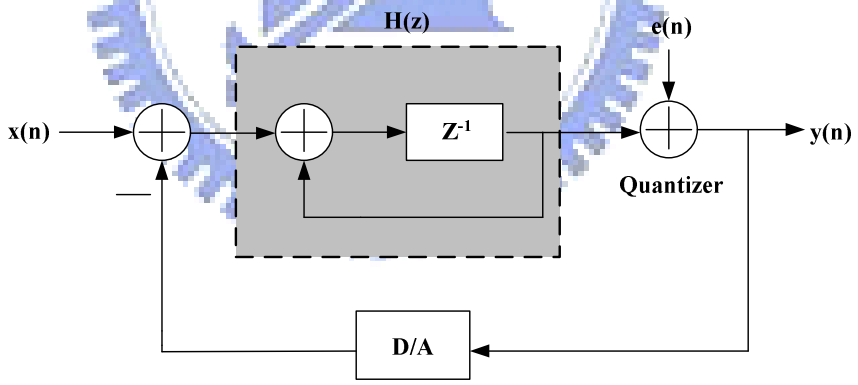


Fig. 3.2 First-order ΣΔ modulator

H(z) in Fig. 3.2 is indicated the effects of delay and accumulation, this is equivalent with an integrator in circuit design, so the three circuits components of ΣΔ modulator are integrator, quantizer and DAC in the feedback path. A first order ΣΔ modulator's output can represent as

$$Y(z) = z^{-1}X(z) + (1-z^{-1})E(z) \qquad (3.1)$$

From (3.1) we can find the signal transfer function is as a delay function, and noise transfer function is as a high pass filter, moves the noise to high frequency. In order to derive PSNR of first order ΣΔ modulator, we must get the magnitude of $N_{TF}(z)$ and $S_{TF}(z)$ in the frequency domain, so we substitute z with $e^{j2\pi \cdot f/f_s}$, and get $|S_{TF}(f)|$ and $|N_{TF}(f)|$ respectively as:

$$|S_{TF}(f)| = |z^{-1}| = |e^{-j2\pi \cdot f/f_s}| = 1 \qquad (3.2)$$

$$N_{TF}(f) = 1 - e^{-j2\pi \cdot f/f_s} = \sin(\frac{\pi f}{f_s}) \times 2j \times e^{-j\pi \cdot f/f_s}$$

$$\Rightarrow \quad |N_{TF}(f)| = 2 \cdot \sin(\frac{\pi f}{f_s}) \qquad (3.3)$$

So the quantization noise in base band $\pm f_B$ can obtain by (2.7) and (3.3)

$$P_Q = \int_{-f_B}^{f_B} S_e^2(f) \cdot |N_{TF}(f)|^2 df = \int_{-f_B}^{f_B} \frac{V_{LSB}^2}{12 \cdot f_s} \cdot \left[2\sin\left(\frac{\pi f}{f_s}\right) \right]^2 \cdot df \qquad (3.4)$$

Because that f_B is much lower than f_s, so $\sin(\pi f/f_s)$ is approximate equal to $(\pi f/f_s)$, and P_Q is as

$$P_Q = \frac{V_{LSB}^2 \pi^2}{36} \cdot (\frac{1}{OSR})^3 = \frac{FS^2 \cdot \pi^2}{36 \cdot 2^{2B} \cdot OSR^3} \qquad (3.5)$$

From (2.5) and (3.5), if we have the maximum signal power, then PSNR is as (3.6)

$$PSNR = 10 \log(\frac{P_{signal}}{P_Q}) = 10 \log(\frac{3}{2} 2^{2B}) + 10 \log[\frac{3}{\pi^2}(OSR)^3]$$

$$= 6.02B + 1.76 - 5.17 + 30 \log(OSR) \qquad (3.6)$$

(&)From (3.6), we find that each octave of OSR, PSNR will increase 9dB, increase 1.5 bit in resolution. Compare (3.6) with (2.10) that only has oversampling effect; we can find that 1st order noise shaping increases the performance of ΣΔ modulator.

3.2 Single-Loop Second-Order Sigma-Delta Modulator

When the discrete time filter in Fig. 2.8 is replaced by two cascade integrator, then it is a second order ΣΔ modulator, output of the first integrator is only connecting with the input of the second integrator, it is shown in Fig. 3.3

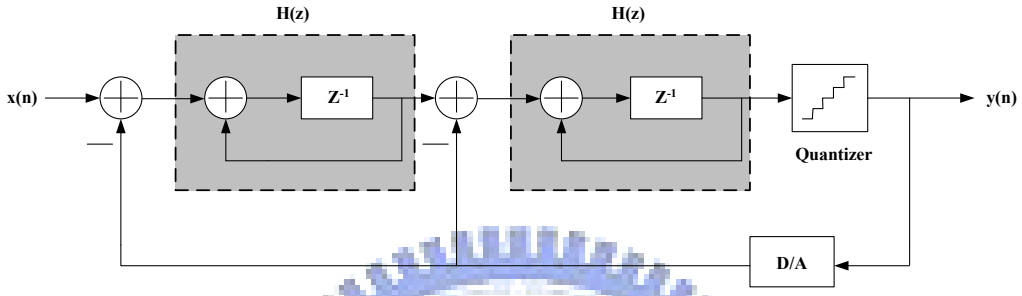


Fig. 3.3 Single loop second order ΣΔ modulator

Then the output of it can easily be derived as

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2E(z) \quad (3.7)$$

where S_{TF} and N_{TF} is as

$$S_{TF}(z) = z^{-2} \quad (3.8)$$

$$N_{TF}(z) = (1- z^{-1})^2 \quad (3.9)$$

Using the same method in (3.3) (3.4), we can obtain

$$|S_{TF}(f)| = 1 \quad (3.10)$$

$$|N_{TF}(f)| = \left[2 \cdot \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \quad (3.11)$$

$$P_Q = \frac{V_{LSB}{}^2 \cdot \pi^4}{60 \cdot OSR^5} = \frac{FS^2 \cdot \pi^4}{2^{2B} \cdot 60 \cdot OSR^5} \quad (3.12)$$

So finally, PSNR of the second order ΣΔ modulator is as

$$PSNR = 10\log\left(\frac{P_{signal}}{P_Q}\right) = 10\log\left(\frac{3}{2}2^{2B}\right) + 10\log\left[\frac{5}{\pi^4}(OSR)^5\right]$$

$$= 6.02B + 1.76 - 12.9 + 50\log(OSR) \qquad (3.13)$$

In the single loop second order architecture, each octave of OSR can increase PSNR by 15 dB, it is equivalent to 2.5 bit in resolution. If we compare (3.13), (3.11) with $|NTF(f)|=1$ that without noise shaping, as Fig. 3.4, we can find that in our needed signal bandwidth, the quantization noise is highest when $|NTF(f)|=1$, and that with second order noise shaping is smallest among this figure [Joh 97].

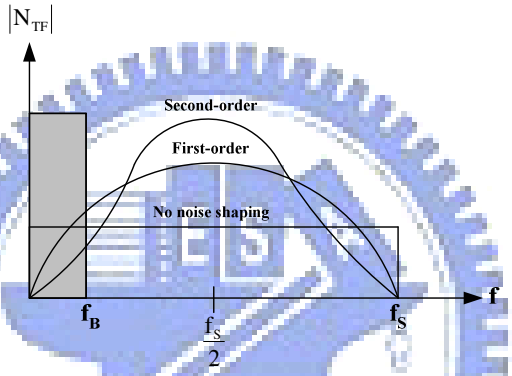


Fig. 3.4 Comparison of noise shaping techniques

3.3 Single-Loop High Order Sigma-Delta Modulator

Fig. 3.5 is a single loop high order ΣΔ modulator, from the derivation in Section 3.1 and Section 3.2, we can get the quantization noise P_Q in signal bandwidth is as

$$P_Q = \frac{V_{LSB}^{\ 2}}{12} \cdot \frac{\pi^{2L}}{2L+1} \cdot \left(\frac{1}{OSR}\right)^{2L+1} \quad , L: \text{order} \qquad (3.14)$$

and its PSNR is

$$PSNR = 6.02B + 1.76 - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \qquad (3.15)$$

In the application of high order ΣΔ modulator, (6L+3)dB increases in SNR when OSR is octave, so PSNR can be raised by increasing the order of the system, especially at large oversampling ratio. But sometimes in high order architecture, the performance will be worsen

than result predicted by (3.13), because of the stability problem, it will make less effective noise shaping function, so the quantization noise will not be suppressed completely.

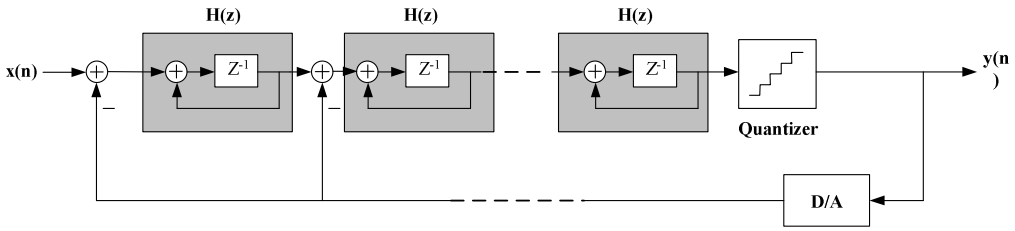


Fig 3.5 Single-loop high order $\Sigma\Delta$ modulator

3.4 Interpolative Sigma-Delta Modulator

Interpolative is a kind of high order $\Sigma\Delta$ modulator, it changes connection of some stages, adds some feedforward paths and feedback paths in order to suppose more aggressive noise shaping effect, Fig. 3.6 is a four-order interpolative architecture $\Sigma\Delta$ modulator [Cha 90].

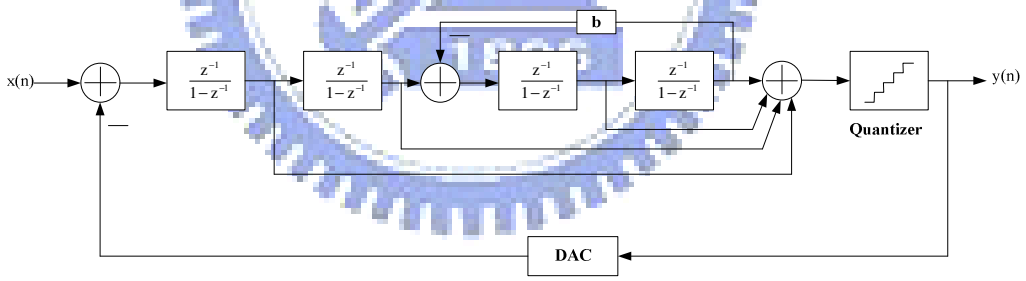


Fig. 3.6 Four-order interpolative architecture

This architecture also has stability problem, when the order L increases, each integrator produces one pole, and when the order is higher, poles of this system will also increase, and it will cause unstable situation, so the range of integrator gain will be limited; if the range of integrator gain is small, oscillation will appear in the circuits. Another is the considerations of clock control, when we use SC (switched-capacitor) to implement the integrator, each integrator needs two clocks to control its operation, and we will need more clock to control

the integrator when the order of system increases, it will produce more problems.

3.5 MASH Architecture

MASH (Multi-stage noise shaping) architecture is also called cascade architecture, which is a method that cascades several low order loops modulator in order to get high order noise shaping effect. The fundamental ideal of MASH is delivering quantization noise of front stage to input of next stage, and combining the digital outputs of all the stages with proper transfer function in digital domain, only the quantization noise of last stage will appear at the output, and the orders of N_{TF} is the same with total orders in the cascade $\Sigma\Delta$ modulator. Fig 3.7 is a three-order cascade $\Sigma\Delta$ modulator, its is the combination of a second-order and first-order $\Sigma\Delta$ modulator, so also called 2-1 cascade architecture [Wil 94].

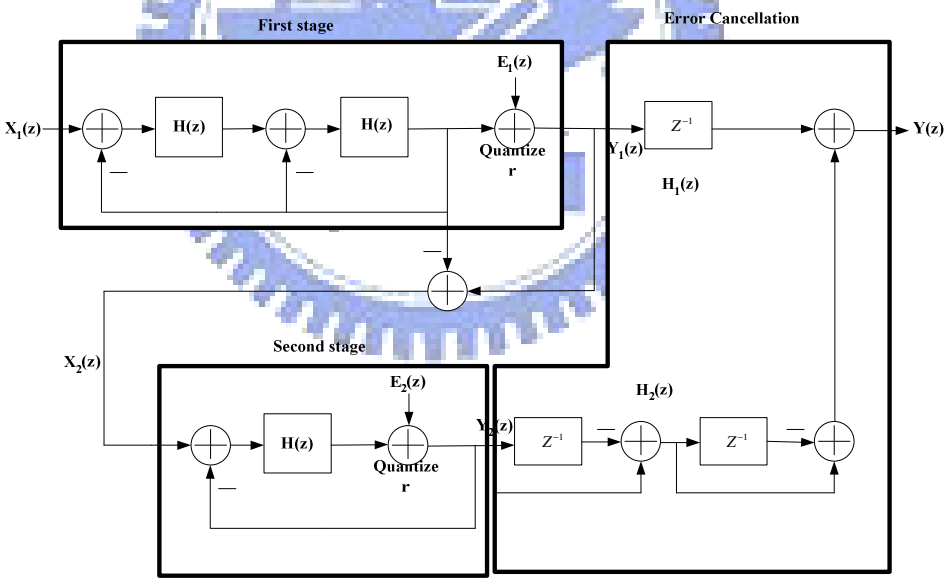


Fig. 3.7 2-1 architecture MASH $\Sigma\Delta$ modulator

From Fig. 3.7, we can derive the first stage output $Y_1(z)$ can be represented as

$$Y_1(z) = z^{-2}X_1(z) + (1-z^{-1})^2E_1(z) \qquad (3.16)$$

Output of second stage $Y_2(z)$ is as

$$Y_2(z) = z^{-1}X_2(z) + (1-z^{-1})E_2(z) \qquad (3.17)$$

and overall output of MASH Y(z) is as

$$Y(z) = H_1(z)Y_1(z) + H_2(z)Y_2(z) \qquad (3.18)$$

and we can say that second stage input $X_2(z)$ is almost the same with $E_1(z)$, in order to eliminate first stage quantization noise $E_1(z)$, from (3.16) ~ (3.18), we can define the error cancellation functions $H_1(z)$ and $H_2(z)$ as

$$H_1(z) = z^{-1} \qquad (3.19)$$

$$H_2(z) = (1-z^{-1})^2 \qquad (3.20)$$

From (3.16)~(3.20), $E_1(z)$ can be eliminated, and second stage quantization noise $E_2(z)$ is shaped by third-order noise shaping function, and the MASH output Y(z) is as

$$Y(z) = z^{-3}X_1(z) + (1-z^{-1})^3E_2(z) \qquad (3.21)$$

The most significant advantage of this architecture is that stability is not an issue, because it is composed by several low-order systems, and the quantization noise will not be amplified stage by stage, so its stability is good. Most important, the noise shaping function is equivalent as high order ΣΔ modulator, so it is popular in recent publications [Rio 04][Vle 01]. However, there also have some drawbacks of this topology; it is sensitive to the circuits' imperfections, such as finite DC gain of OTA, variance of integrator gain due to capacitor mismatch and non-zero switch resistance. These are all practical considerations when we design a MASH architecture ΣΔ modulator [Gag 03].

3.6 Multi-bit Quantizer Sigma-Delta Modulator

The demands of high resolution and high bandwidth ADC are more and more in recent years. In a high signal bandwidth, OSR of ΣΔ ADC can't be too high, and the peak SNR of a ΣΔ modulator with such limited OSR can't satisfy of high resolution applications, if we use higher order architecture, then the performance will degrade due to instability. So the most general method to increase performance is to use multibit quantizer. The most obvious advantage of using multibit quantizer is that the distance between quantizer level V_{LSB} in (2.4)

is much smaller due to increasing of B, and according to (2.3), the power of quantization noise is attenuated. Fig. 3.8 is the results of theoretical peak SNR of ΣΔ modulator versus oversampling ratio, with different order and quantizer bits, it is noted that peak SNR of the same OSR is increase 6 dB with each additional bit number in quantizer, and at low OSR, low order higher bit number architecture has equivalent performance as high order architecture. This result is usable for high bandwidth applications, and the power consumption of digital circuit in ΣΔ modulator is reduced due to lower sampling rate [Pel 99].

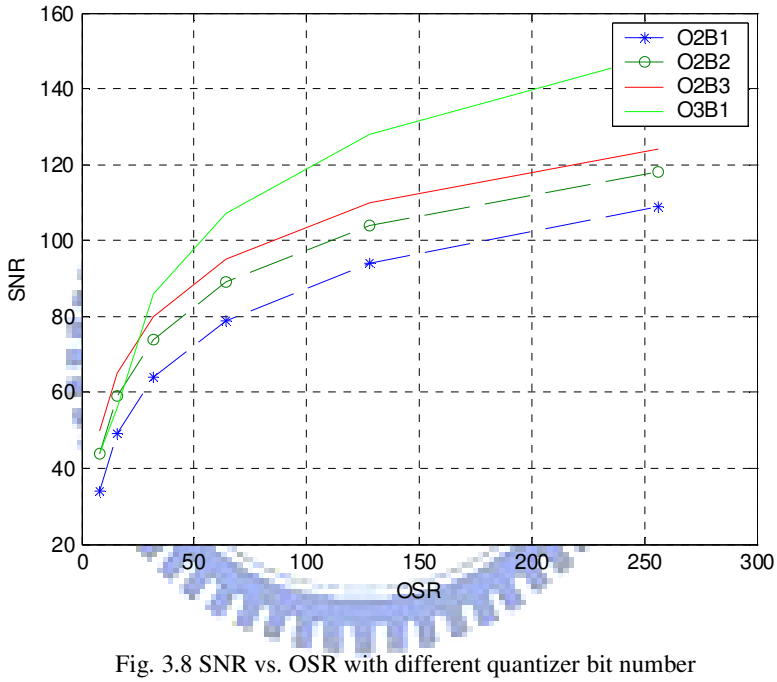


Fig. 3.8 SNR vs. OSR with different quantizer bit number

Because of using multi-bit quantizer, so we also need to use multi-bit DAC(Digital-to Analog Converter) to transfer the digital output to analog signal, and feed it back to integrator. The most significant disadvantage is the non-linearities introduced by multi-bit DAC can degrade the performance of ΣΔ converter, like Fig. 3.9. It is a linear model of multi-bit ΣΔ modulator, where E(Q) and E(D) represent the quantization noise and feedback DAC noise respectively. The values of these capacitor elements in DAC will not equal to ideal values that we need, it is due to process variation, typical value of mismatch in modern CMOS technology is about 0.05% ~ 0.5%. In recent years, so many researches are make efforts on

reduce DAC noise due to mismatch, such as trimming [Nor97], Dynamic element matching(DEM)[Mil 03][Reb 90], although trimming is effective, but it has a expensive production step. So, DEM becomes more and more popular because of its efficiency and cheaper cost.

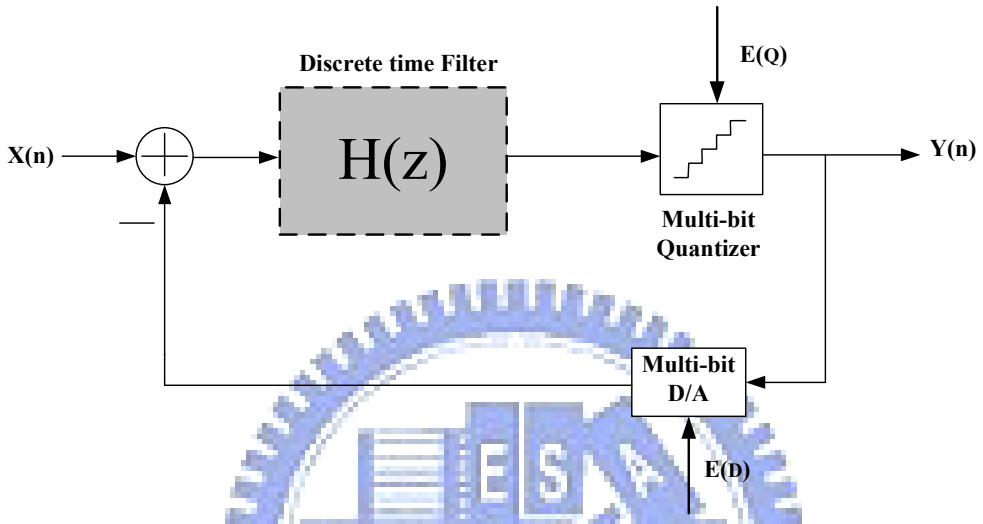


Fig. 3.9 Multi-bit architecture

3.7 Multi-bit Sigma-Delta Modulator use DEM Technique

Dynamic element matching is a different approach to decrease the DAC noise, it is used to improve the linearity of pure DACs [Pla 79], but now it is most used in inner DAC of multi-bit ΣΔ modulator. A DAC with DEM technique is illustrated in Fig. 3.10, 2^B bits thermometer code is put into the element selection logic block, and the function of element selection logic is try to select DAC elements in such way let the errors introduced by DAC average to zero for several operation periods. Because the DEM block is located in feedback loop, so its delay must be very small prevent to degrade the performance of ΣΔ converter, therefore the algorithm used in the DEM block must be simple. There are several techniques of DEM, such as Randomization [Car 89], Clocked Averaging (CLA) [Pla 79], Individual Level Averaging (ILA) [Che 95], Data Weighted Averaging (DWA) [Bai 95], Randomization

is the first approach to use DEM technique in ΣΔ ADC, and DWA offers a good performance to reduce DAC error, in this section, an overview introduction of these two algorithms will be presented, and the operation principle of them will be explained.

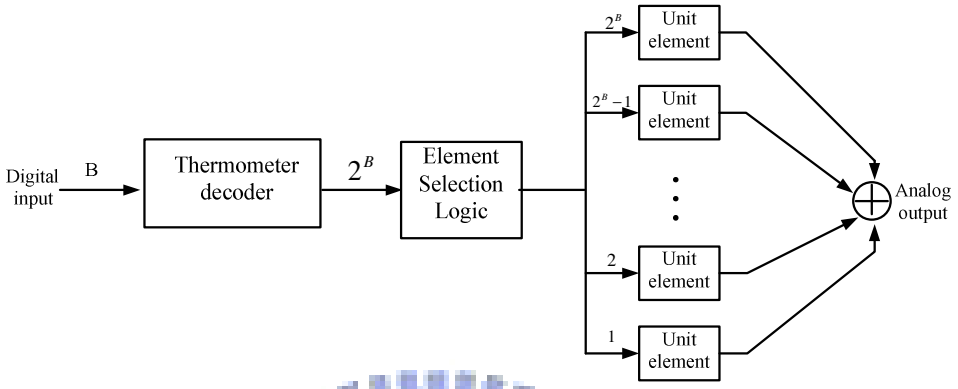


Fig. 3.10 A B-bit DAC with DEM technique

3.7.1 Randomization Technique

The main operation principle of randomization is that the element selection logic performs as a randomizer. In each clock period, the randomizer selects DAC elements randomly to generate the output of DAC. If the randomizer is ideal, then the DAC noise will become uncorrelated with each other. Simulation results show that randomization DEM technique reduces the noise floor from DAC error by several dB, but it still be a white noise in low frequency. Fig. 3.12 is the output spectrum of a second-order ΣΔ modulator with a 0.1% capacitor mismatch, it is notable that the noise floor of randomization DEM is lower than that without any calibration technique in the feedback DAC.

3.7.2 Data Weighted Averaging (DWA)

DWA is a efficiently method to reduce DAC mismatch noise, it uses one register to remember the capacitor last time used, and always points to the first unused unit capacitor in this clock, so DWA rotates through all the unit capacitors such that all capacitors are used at the maximum possible rate. From this algorithm, each elements is used the same number of

times in long interval, this ensures that the errors caused by the DAC average to zero quickly. In Fig. 3.11, it is a 4-bit DAC and the shaded boxes are the number of 1's in the thermometer code. Assumes that the input codes sequence is 8, 8, 10, 9, 10, 10, 11, 11, 12, 11, 14, 11, 14, 13, 12, 15... Fig. 3.12 is the simulation results of a third order ΣΔ modulator, we can see that without DEM has highest noise floor and DWA works as a first order noise shaping function of DAC noise, ideal DAC only with quantization noise has third-order noise shaping.

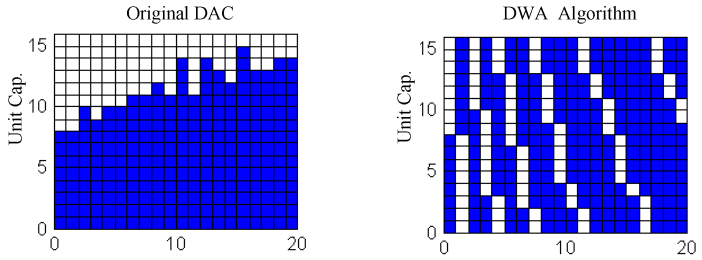


Fig. 3.11 Operation principle of the DWA algorithm

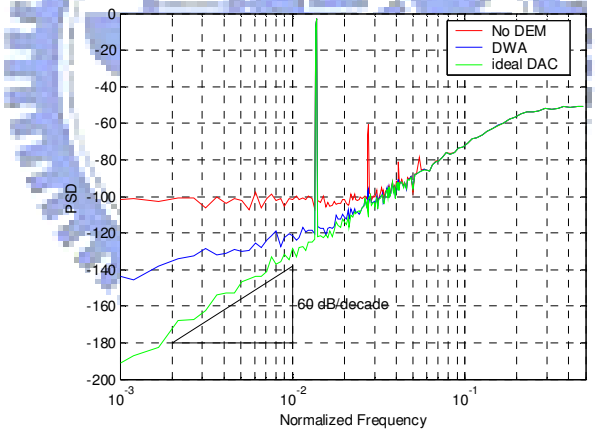


Fig. 3.12 Output spectrum with three kinds of DAC

Another consideration is the sub-ADC(quantizer) of the ΣΔ modulator, we usually use Flash A/D as the multi-bit quantizer because of its high speed, but Flash A/D has a significant disadvantage is that the number of comparators of it is proportional to 2^B. That means a 6 bit quantizer needs 64 comparators, the occupied area of comparator may not much, but in modern SOC applications, the problems of power and area are important, so it becomes one

limitation of multi-bit quantization.

ΣΔ A/D converter is attractive for high resolution application, for higher signal bandwidth, we increase system order to raise SNR, but it still have stability problem. So people develop MASH and multi-bit architecture to improve its performance. Finally, we classify they into low order, high order, MASH and multi-bit four kinds of architecture, and compare their advantage and disadvantage as Fig. 3.13 [Med 99]

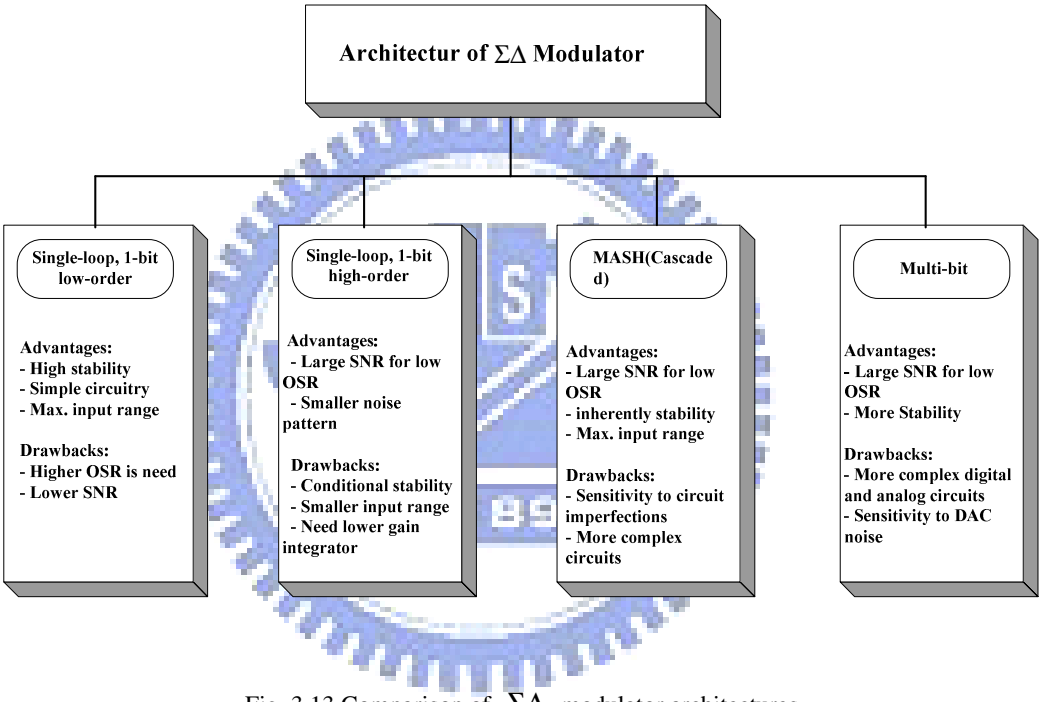


Fig. 3.13 Comparison of ΣΔ modulator architectures

3.8 Decimator

In ΣΔ A/D converter, digital decimator is used to process digital signal of the quantizer output, the high speed data word after oversampling modulation can't be used directly. Because there have original signal and quantization noise among it, so the main function of decimator is to convert the oversampled B-bit output words of the quantizer at a sampling rate of fs to N-bit words at Nyquist rate of input, and removes the noise out of signal band. In order to prevent the noise introduced by other frequency, the decimator filter must have very

flat signal pass-band, and sharp transition region and enough signal attenuation in stop band. Two-stage decimator is used in a general situation, because that single stage decimator is difficult to convert sampling rate to Nyquist rate in 1 time and without degrading SNR. In the first stage, we can down-sample the sample frequency to 2~4 times of Nyquist frequency, and in the second stage, we can use IIR or FIR filter that have high linearity [Nor 97]. For a large OSR, multi-stage decimator is used.

3.9 Performance Metrics for a ΣΔ Modulator

In order to understand the performance merits used to specify the behavior of ΣΔ modulator, several specifications concerning the performance are discussed [Gee 02].

- **Signal to Noise Ratio:** The SNR of a data converter is the ratio of the signal power to the noise power, measured at the output of the converter for a certain input amplitude. The maximum SNR that a converter can achieve is called the peak SNR.
- **Signal to Noise and Distortion Ratio:** The SNDR of a converter is the ratio of the signal power to the power of the noise and the distortion components, measured at the output of the converter for a certain input amplitude. The maximum SNDR that a converter can achieve is called the peak SNDR.
- **Dynamic Range at the input:** The DR_i is the ratio between the power of the largest input signal that can be applied without significantly degrading the performance of the converter, and the power of the smallest detectable input signal. The level of significantly degrading the performance is defined as the point where the SNDR is 6 dB bellow the peak SNDR. The smallest detectable input signal is determined by the noise floor of the converter.
- **Dynamic Range at the output:** The dynamic range can also be considered at the output of the converter. The ratio between maximum and minimum output power is the dynamic range at the output DR_o, which is exactly equal to peak SNR.
- **Effective Number of Bits:** ENOB gives an indication of how many bits would be required in an ideal quantizer to get the same performance as the converter. This numbers also

includes the distortion components and can be calculated from (2.6) as

$$\text{ENOB} = \frac{SNR - 1.76}{6.02} \tag{3.22}$$

- **Overload Level:** OL is defined as the relative input amplitude where the SNDR is decreased by 6dB compared to peak SNDR

Typically, these specifications are reported using plots like Fig. 3.14. This figure shows the SNR and SNDR of the ΣΔ converter versus the amplitude of the sinusoidal wave applied to the input of the converter. For small input levels, the distortion components are submerged in the noise floor of the converter. Consequently, the SNDR and SNR curves coincide for small input levels. When the input level increases, the distortion components start to degrade the modulator performance. Therefore, the SNDR will be smaller than the SNR for large input signals. Note that these specifications are dependent on the frequency of the input signal and the clock frequency of the converter. Fig. 3.14 also shows that SNDR curves drop very fast once the overload point is achieved. This is due to the overloading effect of the quantizer which results in instabilities.

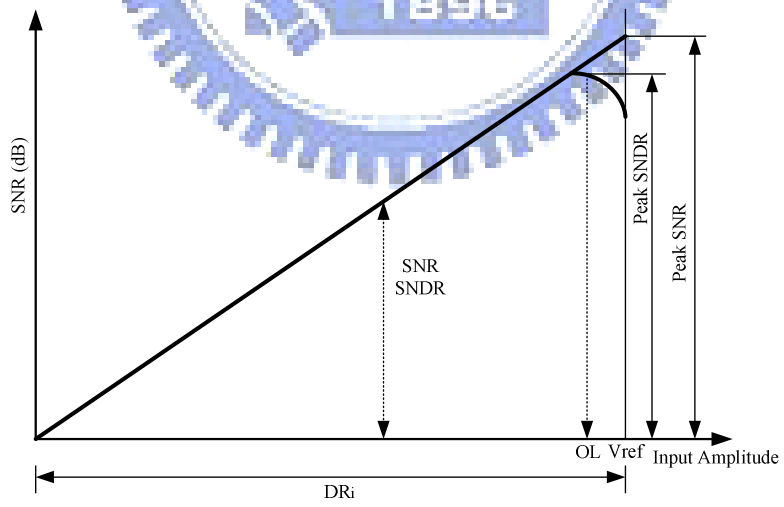


Fig. 3.14 Performance characteristic of a ΣΔ converter

4

Models of Sigma-Delta Modulator Noises and Power

Proposing an optimization algorithm for searching design parameters which maximize ΣΔ ADC SNR while minimize power consumption, is one of the primary purposes of this paper. Related model completeness determines success of this goal. The ΣΔ modulator nonidealities are categorized into five parts in this chapter; finite OTA gain error, thermal noise, settling error, multi-bit DAC noise, and jitter noise. All nonideality models are expressed in noise power form, which can directly add to ideal quantization noise power. All noise power models discussed in the following are based on the integrator scheme, as shown in Fig. 4.1. In Fig. 4.1, C_u is the unit capacitor whose capacitance value is $\frac{C_S}{2^B}$. The power consumption model is presented as the last part of this chapter.

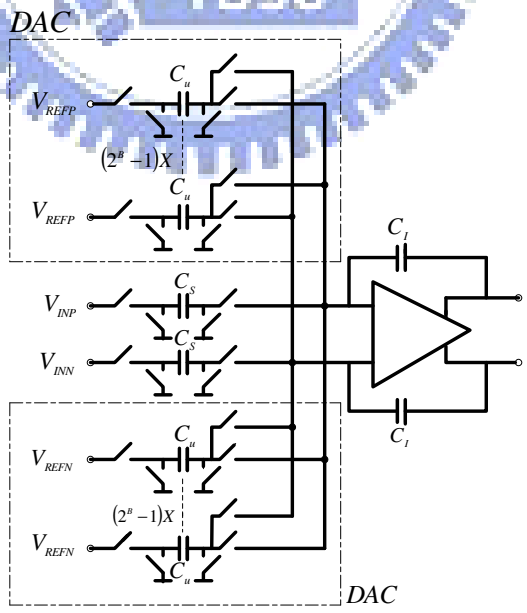


Fig. 4.1 Integrator and the DAC branches

4.1 Finite OTA Gain Error

Finite OTA Gain is an important error when we analyze a real integrator. Typical value of OTA gain is about 50 ~ 80 dB in modern CMOS technology. For a general single-loop n th order $\Sigma\Delta$ modulator with finite OTA gain A_0, the modified quantization noise is expressed as [Med 99]:

$$P_{Q(\text{mod.})} \cong \frac{\Delta^2}{12} \cdot \left[\frac{\pi^{2n}}{(2n+1) \cdot OSR^{2n+1}} + \left(\frac{a_1}{A} \right)^2 \cdot \frac{\pi^{2n-2} \cdot n}{(2n-1) \cdot OSR^{2n-1}} \right]$$

$$= P_Q + P_{AV} \qquad (4.1)$$

where P_Q is the original quantization noise, and Δ is the quantizer step size. The P_{AV} in (4.1) is due to finite OTA gain, and can be considered as an additive quantization noise power. It can be verified using (4.1) that, for a single-loop topology, $A = 50$ dB is sufficient to avoid SNR degrades, in the sense that a higher A_0 would not significantly reduce $P_{Q(\text{mod.})}$.

4.2 Thermal noise (Switch, OTA, Reference circuits)

There are three thermal noise sources in the $\Sigma\Delta$ modulator, in MOS switches, OTAs and reference voltage. We will analyze them separately as follows.

For a fully differential implementation, the in band switch thermal noise during the sampling phase results in output noise power [Med 99]

$$P_{sw1} = \frac{1}{OSR} \cdot \left(\frac{4\text{kT}}{\text{C}_\text{S}} \right) \qquad (4.2)$$

where k is Boltzman constant and T is the absolute temperature. Additional thermal noise is introduced by the switches during the integration phase, resulting in the output noise power [Gee 02]

$$P_{sw2} \cong \frac{1}{OSR} \cdot \left(\frac{4\mathrm{kT}}{\mathrm{C_S}} \right) \qquad (4.3)$$

Since the thermal noise voltages introduced during these two phases are uncorrelated, the total output switches thermal noise power from the switched capacitor integrator is

$$P_{sw} = P_{sw1} + P_{sw2} \cong \frac{1}{OSR} \cdot \left(\frac{8\mathrm{kT}}{\mathrm{C_S}} \right) \qquad (4.4)$$

Half of P_{sw} is from the input branch, and the other half is from the DAC branch.

The OTA transistor thermal noise can be modeled as an equivalent noise source $\mathrm{V_{no}}$ at OTA input shown in Fig. 4.2. In deep submicron process $\mathrm{V_{no}} \cong \frac{\alpha \cdot 10\mathrm{kT}}{\mathrm{gm1}}$ $\mathrm{V^2/Hz}$ [Gra 01], where α is a noise factor depending on OTA topology. In a two-stage OTA, $\alpha \approx 2$. During the sampling phase (Fig. 4.2(a)), the circuit looks like a voltage follower. However, due to OTA finite gain bandwidth, noise at $\mathrm{V_O}$ has an equivalent bandwidth, so thermal noise power at integrator output in the sampling phase is

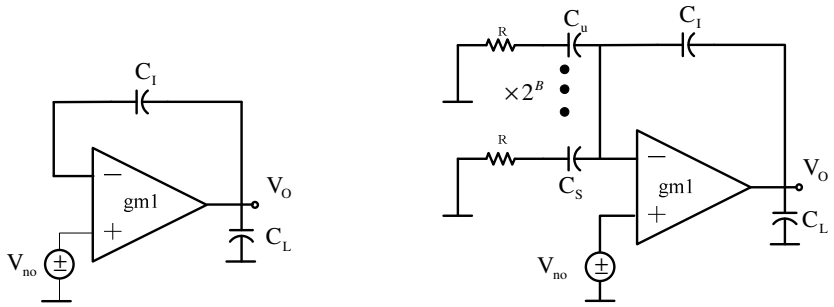
$$P_{OTA}(samp) \cong \mathrm{V_{no}} \cdot \frac{\mathrm{GBW_{samp}}}{A \cdot 2\pi} \cdot \frac{\pi}{2} = \frac{10\alpha \cdot \mathrm{kT}}{4AC_L} \qquad (4.5)$$

During the integration phase (Fig. 4.2(b)), the circuit looks like a non-inverting amplifier, with

$$\frac{\mathrm{V_O}}{\mathrm{V_{no}}}(s) \cong \left(\frac{2a_1 + 1 + 2sC_S R}{1 + 2sC_S R} \right) \Big/ \left(1 + \frac{s}{GBW/A} \right) \qquad (4.6)$$

where GBW/A is the 3dB frequency of the non-inverting amplifier. Then the OTA noise power at the first integrator output can be expressed as

$$P_{OTA}(\mathrm{int}) \cong \int_0^\infty \mathrm{V_{no}} \cdot \left| \frac{\mathrm{V_O}}{\mathrm{V_{no}}}(f) \right|^2 df \qquad (4.7)$$



(a) sampling phase (b) Integration phase

Fig. 4.2 Equivalent circuits of sampling and integration phases

Finally, the total OTA thermal noise power at the ΣΔ ADC output can be obtained as

$$P_{OTA} = \frac{1}{OSR}\cdot\left(\frac{1}{a_1}\right)^2\cdot(P_{OTA}(samp)+P_{OTA}(\text{int}))$$

$$=\frac{1}{OSR\cdot a_1^{\,2}}\cdot\left(\frac{10\alpha\cdot \text{kT}}{4AC_L}+\int_0^{\infty}\text{V}_{\text{no}}\cdot\left|\frac{\text{V}_{\text{O}}}{\text{V}_{\text{no}}}(f)\right|^2 df\right) \qquad (4.8)$$

The reference voltage circuit is implemented by transistors, so the thermal noise device will appear at the reference circuit output and influence the system directly. Consider the bandgap reference circuit in Fig. 4.3 [Raz 01]. Reference output noise is nearly equivalent to OTA input referred noise [Raz 01], so we can express it as $\overline{V_{ref}^{\,2}} \approx \text{V}_{\text{no}} = \frac{10\text{kT}\cdot\alpha}{\text{gm1}}$. Different integrator schemes can introduce reference noise in different ways [Gag 03][Mil 03][Gee 00]. We consider the case shown in Fig. 4.4, where this noise is introduced only in the sampling phase. If the reference noise is unbuffered, its noise power at the ΣΔ ADC output can be derived as

$$P_{ref} = \frac{1}{OSR}\cdot\int_0^{\infty}\frac{\overline{V_{ref}^{\,2}}}{1+4\pi^2\text{R}^2\text{C}_\text{S}^2 f^2}df = \frac{\overline{V_{ref}^{\,2}}}{OSR\cdot 4\text{RC}_\text{S}} \qquad (4.9)$$

We usually add buffers between the bandgap circuits [Pie 02] and the DAC paths. Denote the 3dB buffer bandwidth as BW_b. If BW_b is smaller than $\frac{1}{4RC_S}$, the P_{ref} in (4.9) is changed to be

$$P_{ref} = \overline{V_{ref}^{\,2}} \cdot \frac{\pi \cdot BW_b}{2OSR} \qquad (4.10)$$

If BW_b is larger than $\frac{1}{4RC_S}$, the P_{ref} in (4.9) is applied.

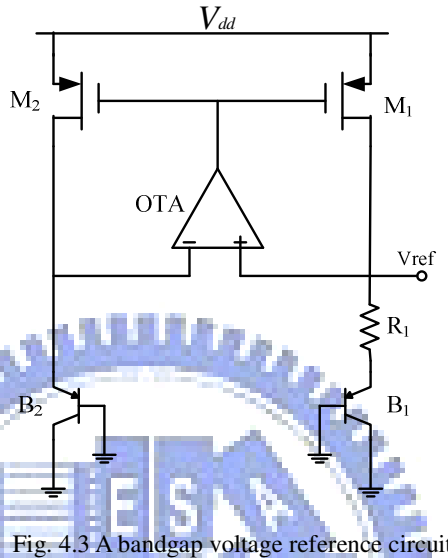


Fig. 4.3 A bandgap voltage reference circuit

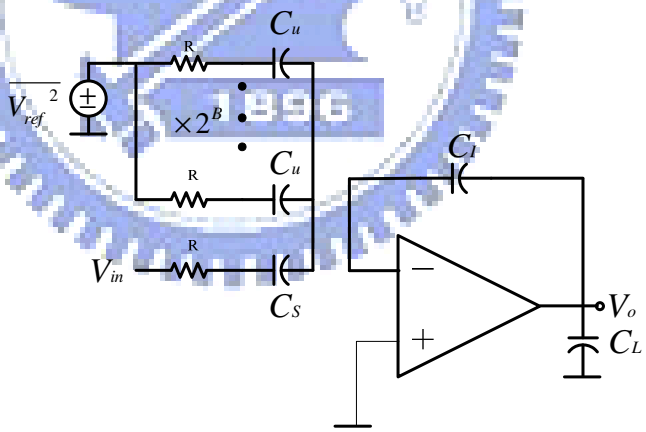


Fig. 4.4 Equivalent circuit while considering reference voltage noise

4.3 Settling Problem

As ΣΔ modulator sampling frequency increases, and multi-bit quantization becomes a high resolution and high-speed application trend, the dynamic settling problem of switched capacitor integrator becomes a more dominant factor. Previous articles have mentioned the settling error [Mal 03][Gri 02][Rio 00]. References [Mal 03] and [Rio 00] provide behavior

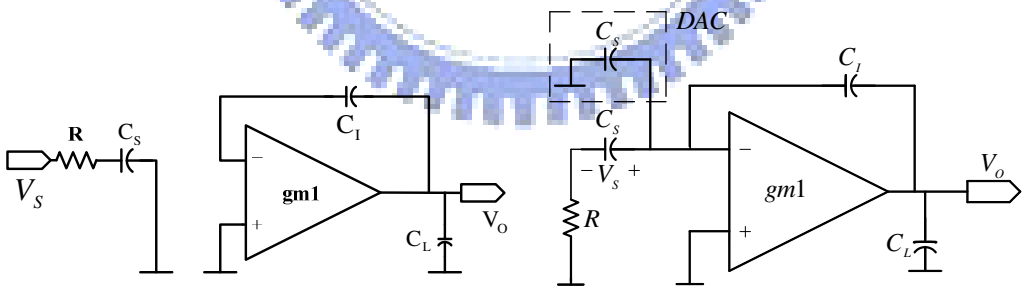
models, which are tedious and integrate poorly with noise-power models of other noises or errors. The noise-power model of [Gri 02] is very primitive since it assumes the pdf (probability density function) settling error is uniformly distributed, and does not consider multi-bit quantization. We only consider the integrator at the first stage. Settling errors at later stages are less influential due to noise shaping.

Now consider a switched capacitor integrator in Fig. 4.5. Assume the MOS switch has an on-resistance *R*, and gm1 is the transconductance of OTA. Let the output parasitic capacitor $C_L \cong \eta \cdot C_I$, where η is the percentage of bottom plate parasitic, assumed to be 20% [Rab 99]. In Fig. 4.5(a), the voltage V_S represents the difference between the sinusoid input signal and the feedback signal from DAC. It is sampled by C_S, so C_S is charged in the half clock period $\frac{T}{2}$ to the voltage V_{CS}:

$$V_{CS} = V_S \cdot [1 - \exp(-\frac{T}{2 \cdot \tau_1})] \qquad (4.11)$$

where $\tau_1 = R \cdot C_S$ is the time constant in the input branch. So the setting error during the sampling phase is:

$$\varepsilon_1 = V_S \cdot \exp(-\frac{T}{2 \cdot \tau_1}) \qquad (4.12)$$



(a) Sampling phase (b) Integration phase

Fig. 4.5 Switched capacitor integrator diagrams

In order to obtain settling noise power during the sampling phase from（4.12）, we need to find the V_S statistical property. Simulations results (using SIMULINK) on a second-order $\Sigma\Delta$ modulator with $a_1 = 0.5$, $a_2 = 2$, 10-level quantization, reference voltage $V_{ref} = \pm 1$, and a full scale sinusoidal input signal, are shown in Fig. 4.6. The result is close to a Gaussian

distribution. Therefore, we assume V_S is Gaussian distributed with a zero mean. The standard deviations σ_{VS} of V_S under different quantizer levels are tabulated in Table 4.1. We observed that when the quantizer level N increases, σ_{VS} decreases. From this table, the relation between standard deviation σ_{VS} and quantizer levels 2^B can be approximated by

$$2^B \cdot \sigma_{vs} \approx 1.4 \cdot |V_{ref}| \qquad (4.13)$$

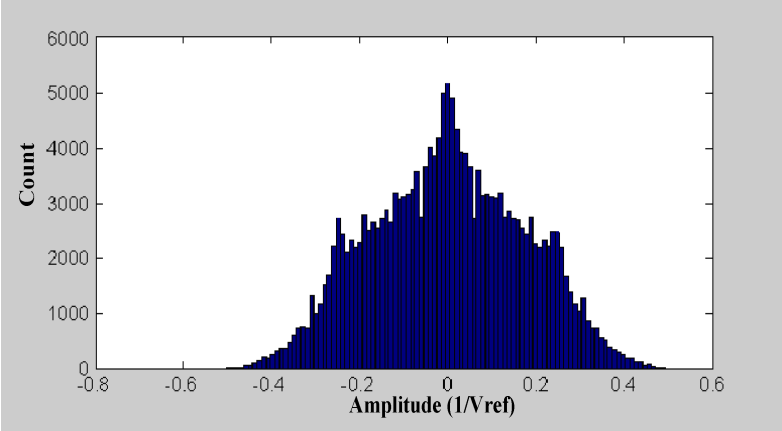


Fig. 4.6 Simulated results of V_S distribution

Std. deviation (σ_{VS})	Variance	Quantizer level (N)	Bit number (B)
0.706	0.498	2	1
0.476	0.227	3	1.585
0.282	0.080	5	2.322
0.198	0.040	7	2.808
0.152	0.023	9	3.17
0.124	0.016	11	3.46
0.047	0.002	31	4.95

TABLE 4.1 Standard deviations of V_S vs. different quantizer bit numbers

The settling noise can reasonably assumed to be white, and its power spectral density constant and distributed over $(-f_S/2, f_S/2)$ as:

$$S_{\varepsilon 1} = \frac{1}{f_S} \cdot \left(\frac{1.4 \cdot \mathrm{V_{ref}}}{2^B} \right)^2 \cdot \exp(\frac{-T}{\tau_1}) \qquad (4.14)$$

Due to oversampling, noise power can be obtained by integrating (4.14) in the signal band $(-f_B, f_B)$, which is:

$$P_{\varepsilon 1} = \frac{1}{OSR} \cdot \left(\frac{1.4 \cdot \mathrm{V_{ref}}}{2^B} \right)^2 \cdot \exp(\frac{-T}{\tau_1}) \qquad (4.15)$$

Next, we consider the integration phase shown in Fig 4.5(b), where the 2^B unit capacitors are combined into C_S, and the 2^B DAC switches are neglected. The charge stored in sampling capacitor will be added to the integration capacitor and this charge current is supplied by OTA. So when the slew rate and gain bandwidth are not large enough, the settling error ε_2 will be produced. The statistical properties of V_S have been summarized in Table I. Then, according to Fig. 4.7, three types of settling conditions can happen in the integrator output during this phase, and the corresponding voltage errors of these three conditions are [Mal 03]:

1. Linear settling: When the initial change rate of the integrator output voltage ($\mathrm{V_O}$) is smaller than the OTA slew rate (SR).

   $$\varepsilon_2 = a_1 \cdot |V_S| \cdot \exp(-\frac{T}{2 \cdot \tau_2}), \text{ when } 0 < |V_S| < \frac{1}{a_1} \cdot SR \cdot \tau_2 \qquad (4.16)$$

2. Partial slewing: The initial change rate of $\mathrm{V_O}$ is larger than SR, but it gradually decreases until it is below the slew rate.

   $$\varepsilon_2 = SR \cdot \tau_2 \cdot \exp(\frac{a_1 \cdot |V_S|}{SR \cdot \tau_2} - \frac{T}{2\tau_2} - 1), \text{ when } \frac{1}{a_1} \cdot SR \cdot \tau_2 < |V_S| < (\frac{T}{2} + \tau_2) \frac{SR}{a_1} \qquad (4.17)$$

3. Fully slewing: The initial change rate of $\mathrm{V_O}$ is larger than SR, and it maintains above SR in the $T/2$ interval.

   $$\varepsilon_2 = a_1 \cdot |V_S| - SR \cdot \frac{T}{2}, \text{ when } |V_S| > \frac{SR}{a_1} (\frac{T}{2} + \tau_2) \qquad (4.18)$$

where SR is the slew rate of OTA, and $\tau_2 = \frac{1 + 2\pi \cdot GBW \cdot R \cdot Cs}{2\pi \cdot GBW}$ [Gee 99a] is the time

constant in the integration phase, with GBW being the equivalent gain bandwidth in the integration phase. The capacitor loading in OTA output during this phase is heavier than in the sampling phase, and is [Gee 02]

$$C_{L2} = 2C_S + C_L \cdot \frac{C_I + (2C_S)}{C_I} \qquad (4.19)$$

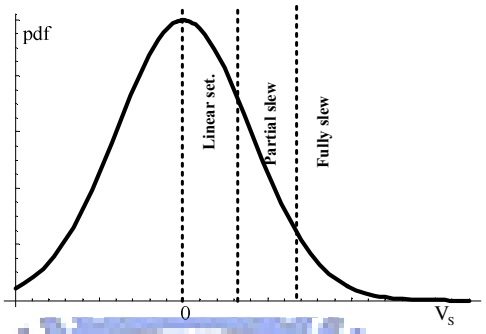


Fig. 4.7 Three types of settling conditions in integration phase

The GBW is given by

$$GBW = \frac{\text{gm1}}{C_{L2} \cdot 2\pi} \qquad (4.20)$$

In order to estimate settling noise in this phase, we must analyze the occurrence probability for each of the three conditions defined by(4.16)-(4.18). The probability of V_S in the linear settling region is

$$\Pr_{lin} = \int_0^{\frac{1}{a_1} \cdot SR \cdot \tau_2} \frac{2}{\sqrt{2\pi} \cdot \sigma_{VS}} \exp\left(\frac{-V_S^{\,2}}{2 \cdot \sigma_{VS}^{\,2}}\right) dV_S = Erf\left[\frac{SR\tau_2}{\sqrt{2}a_1\sigma_{VS}}\right] \qquad (4.21)$$

Let $\varepsilon_{2\max}$ be the maximum linear settling error, and it can be obtained by substituting $|V_S| = \frac{1}{a_1} \cdot SR \cdot \tau_2$ into (4.16). Since V_S is approximately Gaussian, it is reasonable to assume that the linear settling error in (4.16) also has a Gaussian distribution in $(-\varepsilon_{2\max}, \varepsilon_{2\max})$. So the average linear settling noise power in the integration phase is approximately

$$P_{lin} \approx \frac{\varepsilon_{2\max}^{\,2}}{9} = \frac{1}{9}\left(SR \cdot \tau_2 \exp\left(\frac{-T}{2\tau_2}\right)\right)^2 \qquad (4.22)$$

Before calculating the partial settling probability, we must check the possibility of this

condition. If $\frac{1}{a_1}\cdot SR\cdot\tau_2 \geq 2\mathrm{V}_{\mathrm{ref}}$, a partial and fully slewing condition does not need to be considered. If $\frac{1}{a_1} SR\tau_2 < 2\mathrm{V}_{\mathrm{ref}}$, partial slewing probability is

$$\Pr_{par} = Erf[\frac{SR(T+2\tau_2)}{2\sqrt{2}a_1\sigma_{VS}}] - Erf[\frac{SR\tau_2}{\sqrt{2}a_1\sigma_{VS}}] \qquad (4.23)$$

Now we calculate noise power under the partial slewing condition. The pdf of V_S when $\frac{1}{a_1}\cdot SR\cdot\tau_2 < |V_S| < (\frac{T}{2}+\tau_2)\frac{SR}{a_1}$ is

$$f_{par}(V_S) = \frac{1}{\Pr_{par}}\cdot\frac{2}{\sqrt{2\pi}\cdot\sigma_{VS}}\exp(\frac{-V_S{}^2}{2\cdot\sigma_{VS}{}^2}) \qquad (4.24)$$

The ε_2 here is no longer Gaussian distributed, and its pdf can be computed from

$$f_{par}(\varepsilon_2) = f_{par}(V_S)\cdot\frac{dV_S}{d\varepsilon_2} \qquad (4.25)$$

where $\frac{dV_S}{d\varepsilon_2}$ can be obtained by(4.17), and its value is $\frac{SR\tau_2}{a_1\varepsilon_2}$. Then the average noise power of partial slewing is

$$P_{par} = \int_{\varepsilon_2|V_S=\frac{1}{a_1}SR\tau_2}^{\varepsilon_2|V_S=(\tau_2+\frac{T}{2})\frac{SR}{a_1}} f_{par}(\varepsilon)\cdot\varepsilon^2 d\varepsilon = \int_{V_S=\frac{SR\tau_2}{a_1}}^{V_S=\left(\tau_2+\frac{T}{2}\right)\frac{SR}{a_1}} f_{par}\left(V_S\right)\cdot\varepsilon_2{}^2 dV_S \qquad (4.26)$$

Finally, we analyze the settling noise in a fully slewing condition using the same procedure. First, if $(\tau_2+\frac{T}{2})\frac{SR}{a_1} > 2\mathrm{V}_{\mathrm{ref}}$, this condition will never occur. If $(\tau_2+\frac{T}{2})\frac{SR}{a_1} < 2\mathrm{V}_{\mathrm{ref}}$, then the fully slewing probability is

$$\Pr_{ful} = Erf[\frac{2\mathrm{V}_{\mathrm{ref}}}{\sigma_{VS}}] - Erf[\frac{SR(T+2\tau_2)}{2\sqrt{2}a_1\sigma_{VS}}] \qquad (4.27)$$

The p.d.f of V_S when $|V_S| > (\tau_2+\frac{T}{2})\frac{SR}{a_1}$ is

$$f_{ful}(V_S) = \frac{1}{\Pr_{ful}}\cdot\frac{2}{\sqrt{2\pi}\cdot\sigma_{VS}}\exp(\frac{-V_S{}^2}{2\cdot\sigma_{VS}{}^2}) \qquad (4.28)$$

The p.d.f of ε_2 is

$$f_{ful}(\varepsilon_2) = f_{Vs}(V_S)\cdot\frac{dV_S}{d\varepsilon_2} \qquad (4.29)$$

So, the average noise power of fully slewing is

$$P_{ful} = \int_{\varepsilon_2|V_S=(\tau_2+\frac{T}{2})\frac{SR}{a_1}}^{\varepsilon_2|V_S=2V_{ref}} f_{ful}(\varepsilon)\cdot\varepsilon^2 d\varepsilon = \int_{V_S=\left(\tau_2+\frac{T}{2}\right)\frac{SR}{a_1}}^{V_S=2V_{ref}} f_{ful}(V_S)\cdot\varepsilon_2^{\,2} dV_S \qquad (4.30)$$

The total average settling noise in the integration phase can be obtained by (4.21), (4.22), (4.23), (4.26), (4.27) and (4.30) as

$$P_{\varepsilon_2} = \frac{P_{lin}\cdot \mathrm{Pr}_{lin} + P_{par}\cdot \mathrm{Pr}_{par} + P_{ful}\cdot \mathrm{Pr}_{ful}}{OSR} \qquad (4.31)$$

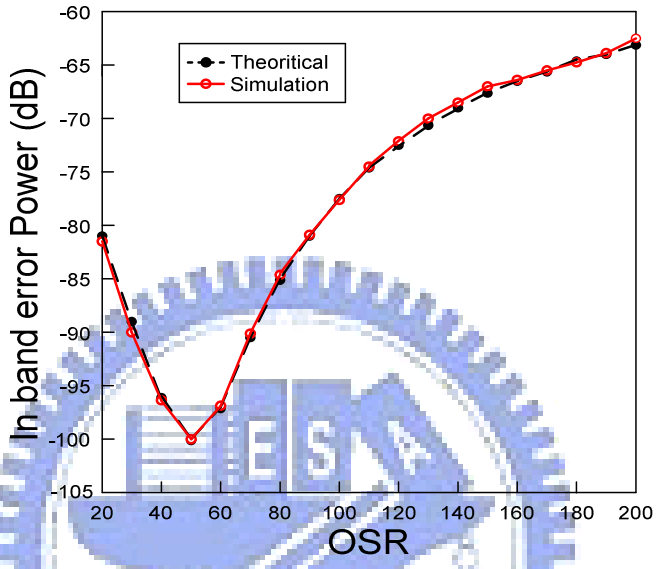


Fig. 4.8 Comparison of our theoretical result with behavior simulation result

In order to verify the result in (4.31), we use SIMULINK to build a second-order ΣΔ modulator with a 4-bit quantizer. The behavioral settling model in [Mal 03] is used. We assume that $a_1 = 0.5$, $R = 300\Omega$, $C_s = 1.7\,\mathrm{pF}$, $GBW = 100\,\mathrm{MHz}$, $f_B = 300\,\mathrm{kHz}$ and SR = 100V/μs, and use a 300 kHz sinusoidal input signal. In an ideal behavior simulation with a sinusoidal input, the error ε_2 can not be observed at modulator output, because ε_2 is highly correlated with V_S, so that ε_2 is compensated in the steady state by the integrator. However, adding a small noise to the input signal can eliminate the effects of feedback and integration. The Gaussian white noise added to the input has a small variance 0.04. After performing FFT to the ΣΔ modulator output data which exclude the input signal and Gaussian noise, we obtain simulated noise power, which is a combination of quantization noise and settling noise. The theoretical noise power is obtained by adding the theoretical settling noise power from

（4.31）to the theoretical quantization noise power. The simulated and theoretical noise powers are both shown in Fig. 4.8 v.s. *OSR*. The two lines are closely related. When *OSR*<50, quantization noise dominates. When *OSR*>50, settling noise dominates. Notice that increasing *SR* and *GBW* will reduce settling noise and increase *SNR*, but will also increase analog power consumption and the design challenges. On the other hand, multi-bit quantizers can reduce the slew rate requirement, since a multi-bit structure makes the output feedback signal closer to the input signal.

4.4 Multi-bit DAC noise

There are several advantages in using a multi-bit structure. One is that when the quantization step Δ decreases, quantization and settling noise reduce. Another is that a multi-bit structure improves stability and provides a higher overload level and more aggressive noise shaping function. However, due to CMOS process variations, there can be mismatches in the 2^B unit capacitors C_u of a *B*-bit DAC shown in Fig. 4.4. Assume that each unit capacitor distribution is Gaussian [Pel 89] around a nominal value. Let the normalized capacitance be

$$c_i = \frac{C_i}{\sum_{k=1}^{2^B} C_k}, \qquad 1 \le i \le 2^B \tag{4.32}$$

where C_i is the capacitance of the i th unit capacitor. Define the deviation of c_i as $e_i = c_i - c_m$, where

$$c_m = \frac{\sum_{i=1}^{2^B} c_i}{2^B} \tag{4.33}$$

Then voltage error caused by unit capacitor mismatches is given by [Gee 02]

$$e_{dac}(k) = \mathrm{V_{ref}} \left(\sum_{i=1}^{x(k)} e_i - \sum_{i=x(k)+1}^{2^B} e_i \right) \tag{4.34}$$

where $x(k)$ represents the number of 1's in the feedback thermometer code at the time step

k. The $e_{dac}(k)$ can be treated as an additive Gaussian noise in the $\Sigma\Delta$ modulator feedback path, the variance of which is

$$\sigma^2[e_{dac}] = \mathrm{V_{ref}}^2\left(x(k)\cdot\sigma^2[e_i] + (2^B - x(k))\cdot\sigma^2[e_i]\right)$$

$$= \mathrm{V_{ref}}^2\cdot 2^B\cdot\sigma^2[e_i] = \mathrm{V_{ref}}^2\cdot 2^B\cdot{\sigma_{cap}}^2 \qquad (4.35)$$

where σ_{cap} is the standard deviation of unit capacitor. Assuming the $e_{dac}(k)$ is also white, the average DAC noise power at the modulator output becomes

$$P_{dac} = \frac{1}{OSR}\cdot\mathrm{V_{ref}}^2\cdot 2^B\cdot{\sigma_{cap}}^2 \qquad (4.36)$$

Apparently the dominating factor is *B*, since P_{dac} increases exponentially with respect to *B*. In order to reduce DAC error due to unit capacitor mismatch, several techniques have been proposed. The most efficient among these is the Data Weighted Averaging (DWA) [Bai 95], and it is shown in [Nys 96] that the DWA effect is a first-order noise shaping of the DAC noise. If the DWA is employed, the average DAC noise power at the modulator output is modified to be

$$P_{dac}(DWA) \cong \mathrm{V_{ref}}^2\cdot 2^B\cdot{\sigma_{cap}}^2\cdot\frac{\pi^2}{3\cdot OSR^3} \qquad (4.37)$$

Equations (4.36) and (4.37) will be used to estimate the DAC noise power in the optimization process.

4.5 Clock Jitter Effects

As both the signal bandwidth and the required output SNR increase, clock jitter problems become more obvious. Jitter is usually defined as a random variation in clock signal period around the ideal value, and the value of jitter can be reasonably assumed as a Gaussian random variable with zero mean and standard deviation σ_{jit}. If there is some variation in clock high time, the input signal will be sampled at the wrong instant and receive a consequent voltage error. For a sinusoidal input signal with maximum amplitude A_i and

frequency f_{in}, if it is sampled by a clock which has a jitter variation, then the voltage error is [Bos 88]:

$$\Delta V \cong 2\pi \cdot f_{in} \cdot A_i \cos(2\pi \cdot f_{in} \cdot t)\Delta T \qquad (4.38)$$

where ΔT is the variation of clock period with standard deviation σ_{jit}. Then the jitter noise power becomes:

$$P_{jitter} = \frac{(2\pi \cdot f_{in} \cdot A_i)^2}{2} \cdot \frac{\sigma_{jit}^{\ 2}}{OSR} \qquad (4.39)$$

We consider the worst case in this work. That is, f_{in} and A_i are replaced by f_B and V_{ref} respectively.

Before discussing power consumption modeling, we summarize the nonideality modeling as follows. The leakage noise due to finite OTA gain can be considered as an additional quantization noise, so the total quantization noise will be higher than theoretical quantization noise, appearing at D2 in Fig. 4.9. All other nonidealities are modeled at D1 in Fig. 4.9, because we have modeled them as input-referred noise in the integrator input.

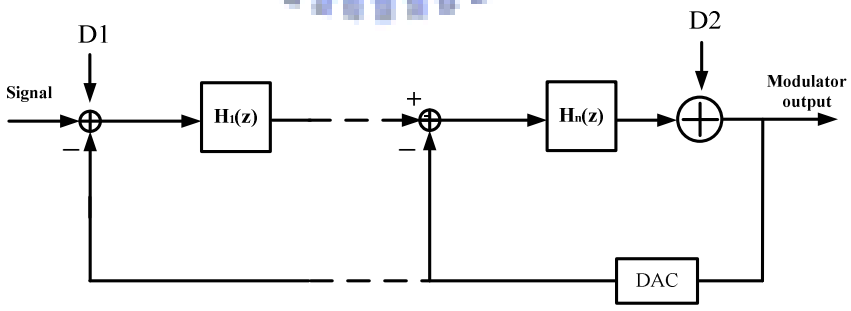


Fig. 4.9 Main nonidealities sources in the $\Sigma\Delta$ modulator

5

Models of Sigma-Delta Modulator Nonlinear Distortion

5.1 Settling Distortion

We analyze incomplete transfer of charge in a SC integrator to obtain analytical models to represent harmonic distortion as function of the operational amplifier finite gain-bandwidth (*GBW*), slew-rate (*SR*). The model developed here assumes the effect of the *SR* in a SC integrator may be interpreted as a nonlinear gain. Consider the integrator operates in the integration phase. As discussed in Chapter 4, there are three settling conditions depending on the absolute value of V_S [Mal 03].

1. Linear settling $\left(|V_S| < \frac{1}{a_1} \cdot SR \cdot \tau_2\right)$:

We can represent integrator output voltage during the *n*th integration interval as

$$V_o(t) = V_o(nT - T) + a_1 V_S \left(1 - e^{\frac{-(t - nT + \frac{T}{2})}{\tau_2}}\right) \quad , \quad nT - \frac{T}{2} < t < nT \qquad (5.1)$$

2. Partial slewing $\left(\frac{1}{a_1} \cdot SR \cdot \tau_2 < |V_S|\right)$:

$$V_o(t) = V_o(nT - T) + SR \cdot (t_0 - nT + \frac{T}{2}) + \left[a_1 V_S - SR \cdot (t_0 - nT + \frac{T}{2})\right]\left(1 - e^{\frac{-(t - t_0)}{\tau_2}}\right) \qquad t > t_0 \qquad (5.2)$$

where t_0 is the time instant when V_o rate becomes less than *SR*. The full slewing case is not considered here because it is not significant. Note that(5.1)and(5.2)at end of each integration interval can be rewritten as

$$V_o(nT) = V_o(nT - T) + a_1 V_S \left(1 - e^{-\left(\frac{T}{2\tau_2} + 1\right)} \cdot e\right) = V_o(nT - T) + a_1 V_S (1 - \beta \cdot e) \quad , \quad |V_S| \le V_L$$

$$V_O(nT) = V_O(nT-T) + a_1 V_S \left[1 - \frac{SR\tau_2}{a_1 V_S} \cdot e^{-\left(\frac{T}{2\tau_2} - \frac{a_1 V_S}{SR\tau_2} + 1 \right)} \right]$$

$$= V_O(nT-T) + a_1 V_S \left[1 - \frac{V_L}{V_S} \cdot \beta e^{|V_S|/V_L} \right] \quad , \qquad |V_S| > V_L \qquad (5.3)$$

where $\beta = e^{-(T/(2\tau_2)+1)}$; $V_L = SR\tau_2 / a_1$

Let $$g_i(V_S) = \begin{cases} a_1(1-\beta e) \ ; & |V_S| \le V_L \\ a_1(1 - \frac{V_L}{V_S}\beta e^{|V_S|/V_L}) \ ; & |V_S| > V_L \end{cases} \qquad (5.4)$$

which is the integrator gain. Harmonic distortions are produced at the modulator output when op-amps operate in the partial slewing region, because in the partial slewing region the integrator gain is a function of input V_S. In order not to produce harmonic distortion, op-amps should always operate in the linear region. From (5.4), we can see that if $|V_S| \le V_L$ is satisfied all the time, the modulator always operates in linear region and harmonic distortion would not be produced. $|V_S| \le V_L$ can be further derived as:

$$|V_S| \le V_L$$

$$\Rightarrow 2A\omega T \le \frac{SR\tau}{0.5}$$

$$\Rightarrow 2A \cdot 2\pi \cdot f_{in} \cdot \frac{1}{2 \times BW \times OSR} \le \frac{SR}{0.5} \cdot \frac{1 + 2\pi \cdot GBW \cdot RC_S}{2\pi \cdot GBW}$$

Assuming $f_{in} = BW$, $R = 300\Omega$, $C_S = 2 \times 10^{-12} F$, it leads to the following equation:

$$OSR \ge \frac{\pi}{SR\left(\frac{1}{2\pi \cdot GBW} + 6 \times 10^{-10} \right)} \qquad (5.5)$$

We then plot (5.5) as shown in Fig. 5.1 which shows that *OSR* is inverse proportional to *SR* and is almost independent to *GBW*.

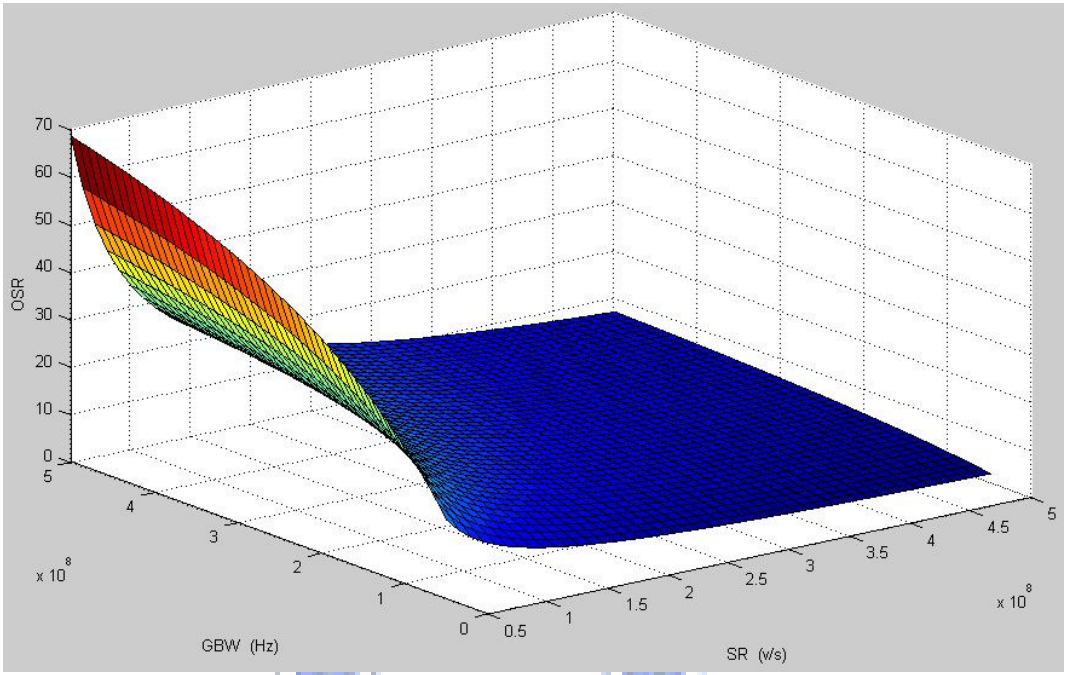


Fig. 5.1 3D plot of（5.5）

Fig. 5.1 indicates that if we design *SR* and *GBW* above the curve with desired *OSR*, the modulator would have no harmonic distortion. It shows that the op-amp slew rate needs to be at least 200V/us, then the modulator can have no harmonic distortions with *OSR* larger than 15. Although op-amps operate in linear region can have no harmonic distortion, it may consume more power dissipation (because large slew rate). Therefore, there has a trade off between power consumption and harmonic distortion. In general, one can choose smaller slew rate to let power consumption lower and have negligible harmonic distortions. In the following, we analyses the influences of slew rate on harmonic distortion when op-amps operate in partial slewing region.

Assume that $g_i(v)$ can be approximated by

$$p_i(v) = a_1 \cdot (\alpha_1 + \alpha_3 v^2 + \alpha_5 v^4) \qquad (5.6)$$

In this point, the problem of estimating harmonic distortion consists of searching for the curve with the form shown in （5.6） which best fits （5.4） for a specific interval. We will use the

least square method to determine the coefficient α_1, α_3 and α_5 to fit （5.4）. The $p_i(v)$ should be fitted through all the points in that specific interval so that the sum of the squares of the distances of those points from the $p_i(v)$ is minimum. The sum of the squares is

$$q = \sum_{j=1}^{n} \left[g_i(x_j) - p(x_j) \right]^2$$

$$= \sum_{j=1}^{n} \left[g_i(x_i) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right]^2$$

q depends on α_1, α_3 and α_5. A necessary condition for q to be minimum is

$$\begin{cases} \dfrac{\partial q}{\partial \alpha_1} = \sum_{j=1}^{n} 2\left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right](-a_1) = 0 \\ \dfrac{\partial q}{\partial \alpha_3} = \sum_{j=1}^{n} 2\left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right](-a_1 x_j^2) = 0 \\ \dfrac{\partial q}{\partial \alpha_5} = \sum_{j=1}^{n} 2\left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right](-a_1 x_j^4) = 0 \end{cases}$$

With this method, the calculation of the coefficients in （5.6） becomes the solution of the following system of linear equations:

$$\begin{cases} \sum_{j=1}^{n} \left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right] = 0 \\ \sum_{j=1}^{n} \left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right](x_j^2) = 0 \\ \sum_{j=1}^{n} \left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right](x_j^4) = 0 \end{cases}$$

$$\Rightarrow \begin{cases} a_1\left(\sum_{j=1}^{n} \alpha_1 + \sum_{j=1}^{n} \alpha_3 x_j^2 + \sum_{j=1}^{n} \alpha_5 x_j^4 \right) = \sum_{j=1}^{n} g_i(x_j) \\ a_1\left(\sum_{j=1}^{n} \alpha_1 x_j^2 + \sum_{j=1}^{n} \alpha_3 x_j^4 + \sum_{j=1}^{n} \alpha_5 x_j^6 \right) = \sum_{j=1}^{n} g_i(x_j) \cdot x_j^2 \\ a_1\left(\sum_{j=1}^{n} \alpha_1 x_j^4 + \sum_{j=1}^{n} \alpha_3 x_j^6 + \sum_{j=1}^{n} \alpha_5 x_j^8 \right) = \sum_{j=1}^{n} g_i(x_j) \cdot x_j^4 \end{cases}$$

$$\Rightarrow \begin{cases} a_1\left(\int_0^{Vh} \alpha_1 + \int_0^{Vh} \alpha_3 x_j^2 + \int_0^{Vh} \alpha_5 x_j^4 \right) = \int_0^{Vh} g_i(x_j) \\ a_1\left(\int_0^{Vh} \alpha_1 x_j^2 + \int_0^{Vh} \alpha_3 x_j^4 + \int_0^{Vh} \alpha_5 x_j^6 \right) = \int_0^{Vh} g_i(x_j) x_j^2 \\ a_1\left(\int_0^{Vh} \alpha_1 x_j^4 + \int_0^{Vh} \alpha_3 x_j^6 + \int_0^{Vh} \alpha_5 x_j^8 \right) = \int_0^{Vh} g_i(x_j) x_j^4 \end{cases}$$

where V_h is the maximum distribution range of the first integrator input V_s, which is assumed in worst case as [Med 94]

$$V_h = 2 \cdot V_{ref} \tag{5.7}$$

$$\Rightarrow \begin{cases} a_1\left(\int_0^{Vh}\alpha_1 + \int_0^{Vh}\alpha_3 x_j^2 + \int_0^{Vh}\alpha_5 x_j^4\right) = \int_0^{VL} a_1(1-\beta e)\, dV_S + \int_{VL}^{Vh} a_1\left(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L}\right) dV_S \\ a_1\left(\int_0^{Vh}\alpha_1 x_j^2 + \int_0^{Vh}\alpha_3 x_j^4 + \int_0^{Vh}\alpha_5 x_j^6\right) = \int_0^{VL} a_1(1-\beta e)\cdot V_S^{\,2}\, dV_S + \int_{VL}^{Vh} a_1\left(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L}\right) V_S^{\,2}\, dV_S \\ a_1\left(\int_0^{Vh}\alpha_1 x_j^4 + \int_0^{Vh}\alpha_3 x_j^6 + \int_0^{Vh}\alpha_5 x_j^8\right) = \int_0^{VL} a_1(1-\beta e)\cdot V_S^{\,4}\, dV_S + \int_{VL}^{Vh} a_1\left(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L}\right) V_S^{\,4}\, dV_S \end{cases}$$

$$\begin{bmatrix}\alpha_1\\ \alpha_3\\ \alpha_5\end{bmatrix} = \begin{bmatrix} \frac{225}{64\cdot Vh} & \frac{-525}{32\cdot Vh^3} & \frac{945}{64\cdot Vh^5} \\ \frac{-525}{32\cdot Vh^3} & \frac{2205}{16\cdot Vh^5} & \frac{-4725}{32\cdot Vh^7} \\ \frac{945}{64\cdot Vh^5} & \frac{-4725}{32\cdot Vh^7} & \frac{11025}{64\cdot Vh^9} \end{bmatrix} \begin{bmatrix} \int_0^{VL}(1-\beta e)\, dV_S + \int_{VL}^{Vh}\left(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L}\right) dV_S \\ \int_0^{VL}(1-\beta e)\cdot V_S^{\,2}\, dV_S + \int_{VL}^{Vh}\left(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L}\right) V_S^{\,2}\, dV_S \\ \int_0^{VL}(1-\beta e)\cdot V_S^{\,4}\, dV_S + \int_{VL}^{Vh}\left(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L}\right) V_S^{\,4}\, dV_S \end{bmatrix} \tag{5.8}$$

The amplitudes of the third and fifth harmonics of the modulator output are:

$$A_3 \cong \frac{|\alpha_3| A_{VS}^3}{4} \quad ; \quad A_5 \cong \frac{|\alpha_5| A_{VS}^5}{16} \tag{5.9}$$

where A_{VS} is the amplitude of V_S. However, in [Med 94], A_{in} instead of A_{VS} is employed in (5.8), where A_{in} is the amplitude of a sinusoidal modulator input signal. It is intuitively clear that using A_{in} is not correct, and our simulation shows that (5.8) is correct and precise. Next we need to obtain an expression for A_{VS}.

$$V_s(z) = X(z) - Y(z) \tag{5.10}$$

In a second-order ΣΔ modulator, modulator output signal *Y(z)* is the time delay version of *X(z)* plus high-pass filtered (noise shaped) quantization noise E(z). Therefore,

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2 E(z) \tag{5.11}$$

Combining (5.10) and (5.11), $V_s(z)$ can be written as

$$V_s(z) = X(z)\left[1-z^{-2}\right] - (1-z^{-1})^2 E(z)$$

Ignoring the quantization noise and taking the inverse z-transform, one obtains

$$V_S(t) = x(t) - x(t-2T)u(t-2T)$$
$$= A_{in}\sin(\omega t) - A_{in}\sin(\omega(t-2T)) \cdot u(t-2T) \qquad (5.12)$$

Then, the amplitude of V_S can be obtained as

$$A_{VS} = V_S(2T) = x(2T) = A_{in}\sin(\omega \cdot 2T) \cong 2A_{in} \cdot \omega \cdot T \qquad (5.13)$$

Note that A_{VS} is not related to quantizer bit number B which can only affect the level of noise floor $E(\omega)$. The result (5.13) has been verified by behavior simulation under different B values, as shown in Fig. 5.2. From(5.9)(5.13), we can see that input signal amplitude A_{in}, input signal frequency ω and sampling time T are the critical parameters to impact the harmonic distortion.

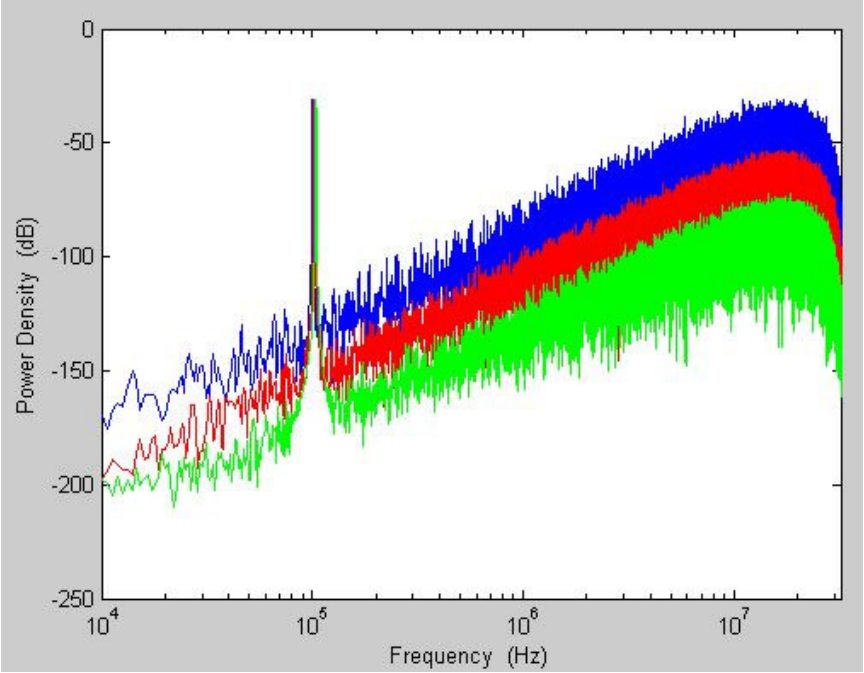


Fig. 5.2 Spectrum of V_S with different quantizer bit number

In order to verify the result in (5.9), we use SIMULINK to build a second-order ΣΔ modulator with a multi-bit quantizer. The behavioral settling model in [Mal 03] is employed. We assume that $SR = 70V/\mu s$, GBW = 100MHz, $R = 300\Omega$, OSR = 16, f_B = 1MHz and C_S = 2pF, and a 1MHz sinusoidal input signal is used. After performing FFT to the output data of the ΣΔ modulator, we obtain the simulated PSD (Power Spectrum Density) which is

shown in Fig. 5.3. It shows that HD3 is -112.5dB and HD5 is -117.5dB. The theoretical harmonic powers calculated from (5.8) and (5.9) are HD3 = -112.4dB and HD5 = -117.3dB. The simulated and theoretical results are very close, and this confirms that our settling distortion model is reasonably precise.

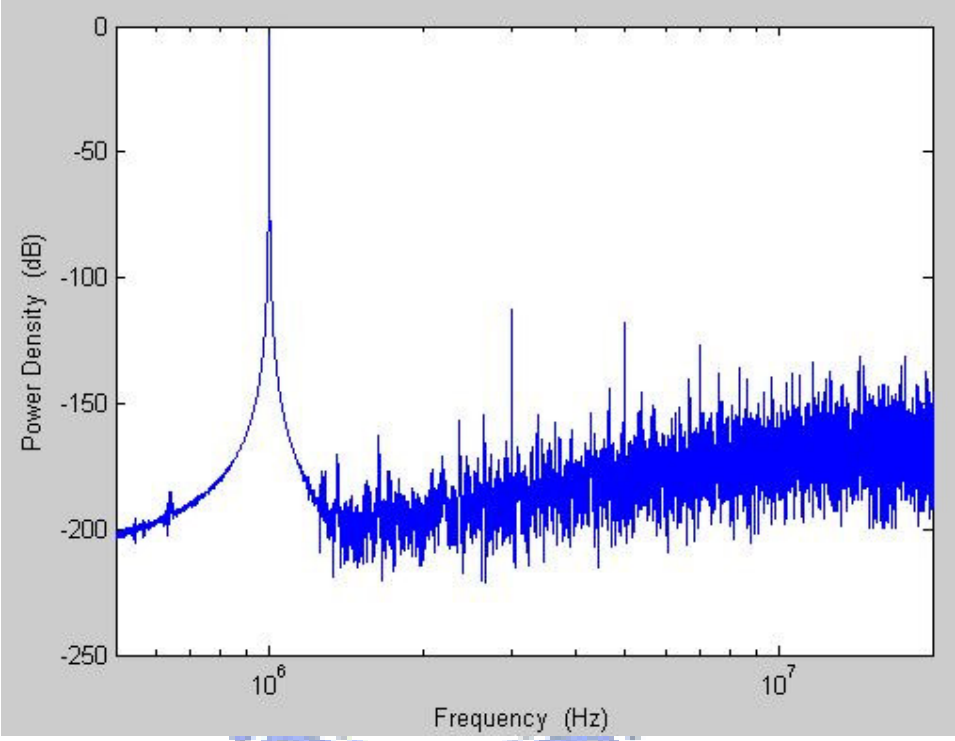


Fig. 5.3 Output spectrum of a second-order $\Sigma\Delta$ modulator with harmonic distortion

In order to provide insight on how settling distortions are related to circuit and system parameters, we further analyze the 3rd and 5th harmonic powers as follows:

$$HD3_{settling}(dB) = 20\log\left(\frac{1}{\sqrt{2}}\left(\frac{|\alpha_3|A_{VS}^3}{4}\right)\right)$$

$$= 20\left[\log|\alpha_3| + \log(2A\omega T)^3 - \log 4\sqrt{2}\right]$$

$$= 20\log|\alpha_3| - 60\log OSR + 30.095 \qquad (5.14)$$

$$HD5_{settling}(dB) = 20\log|\alpha_5| - 100\log OSR + 48.15$$

From （5.14） we can see that *OSR* can effectively influence settling harmonic powers. The （5.8）reveals that α_3 and α_5 are functions of *T*, *GBW*, *R*, C_S and *SR*. Using the parameters designed in Chapter 8 with f_S = 52MHz, *R* = 300ohm, C_S= 1.7pF, and setting *GBW* and *SR* at medium values as *GBW* = 250MHz and *SR* = 250V/μs, we plot $20\log|\alpha_3|$ vs. *SR* in Fig. 5.4 and $20\log|\alpha_3|$ vs. *GBW* in Fig. 5.5.

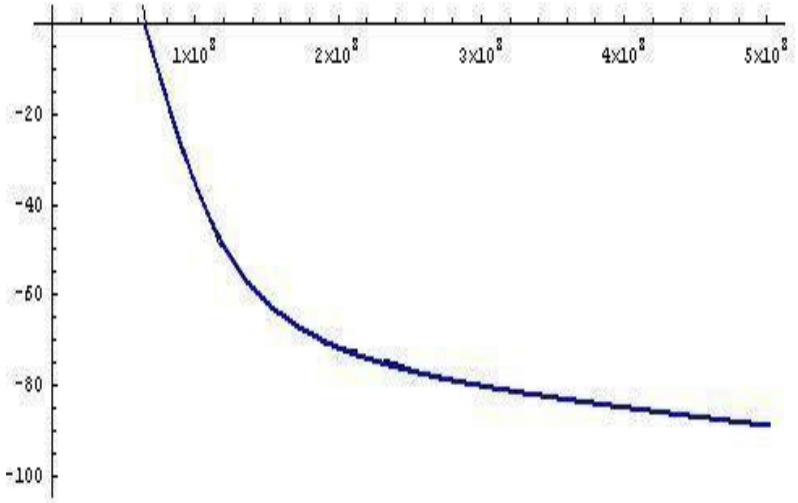


Fig. 5.4 $20\log|\alpha_3|$ vs. *SR*

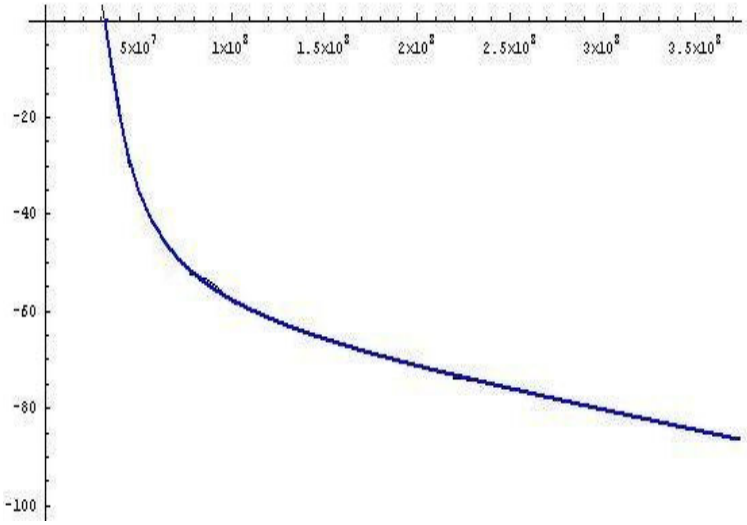


Fig. 5.5 $20\log|\alpha_3|$ vs. *GBW*

In general, harmonic distortion less than -110dB can be ignored because it is below the noise floor of modulator output spectrum. From（5.14）, Fig. 5.4 and Fig. 5.5, we can obtain the minimum required *SR* and *GBW* w. r. t. a specific *OSR*. The results are summarized in Table 5.1.

OSR	**HD3(dB)**	***SR*** $(V/\mu s)$	***GBW*** **(MHz)**
8	$20\log\lvert\alpha_3\rvert$ **-24**	≥ 500	≥ 380
16	$20\log\lvert\alpha_3\rvert$ **-42**	≥ 200	≥ 180
32	$20\log\lvert\alpha_3\rvert$ **-60**	≥ 120	≥ 70
50	$20\log\lvert\alpha_3\rvert$ **-72**	≥ 110	≥ 60
64	$20\log\lvert\alpha_3\rvert$ **-78**	≥ 100	≥ 50
96	$20\log\lvert\alpha_3\rvert$ **-89**	≥ 90	≥ 40

Table 5.1 Minimum *SR* and *GBW* required w. r. t. *OSR*

It is clear from Table 5.1 that as *OSR* decreases, *SR* and *GBW* have to increase dramatically so that the effect of settling distortion can be contained. This can be explained by(5.13), since *T* increases when *OSR* decreases.

5.2 Nonlinear Finite OTA Gain Distortion

An ideal OTA with infinite gain doesn't introduce any noise or distortion. Practical OTAs not only have the characteristics of finite DC gain, but also the gain is nonlinear. Fig. 5.6 shows general behavior of MOSFET output resistance based on BSIM3v3.2.2 [Bsi99]. Different DC biases $|V_{DSQ}|$ and $|V_{GSQ}|$ determine different R_{out}. This makes DC gain of OTAs changes with $|v_{DS}|$ and $|v_{GS}|$ of the output-stage transistors since the DC gain is directly related to R_{out} [Gee02].

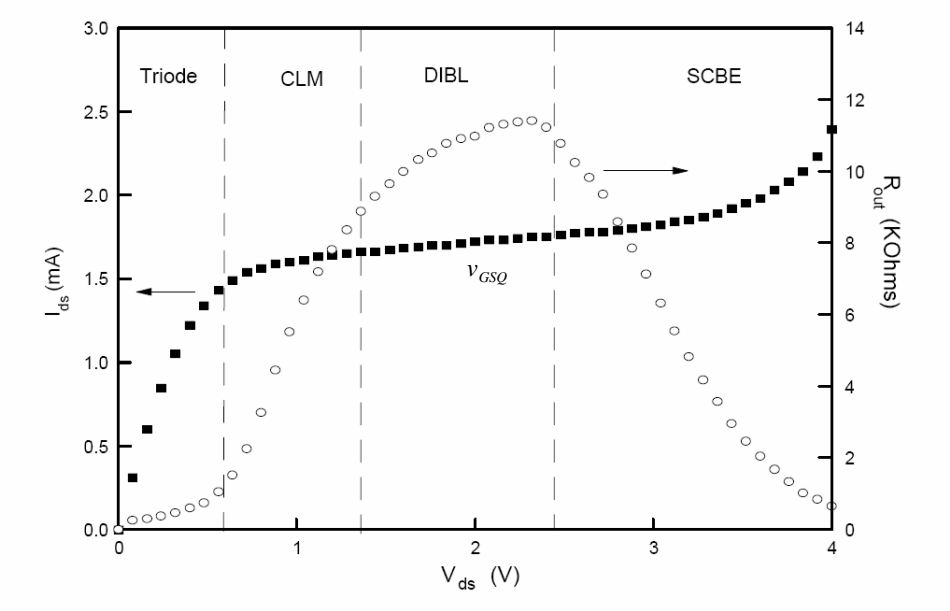


Fig. 5.6. General behavior of MOSFET output resistance

A typical OTA's configuration schematic considering nonlinear DC gain is shown in Fig. 5.7 [Zar05]. In this figure R_{out} of the output-stage transistors are the functions of output voltage V_o since V_o directly affects $|v_{DS}|$ of the output-stage transistors, hence the nonlinearity of the gain is manifested by its dependency on amplifier output voltage V_o. Fig. 5.7 shows a typical relationship between DC gain and V_o, in which the maximum DC gain A_0 appears at

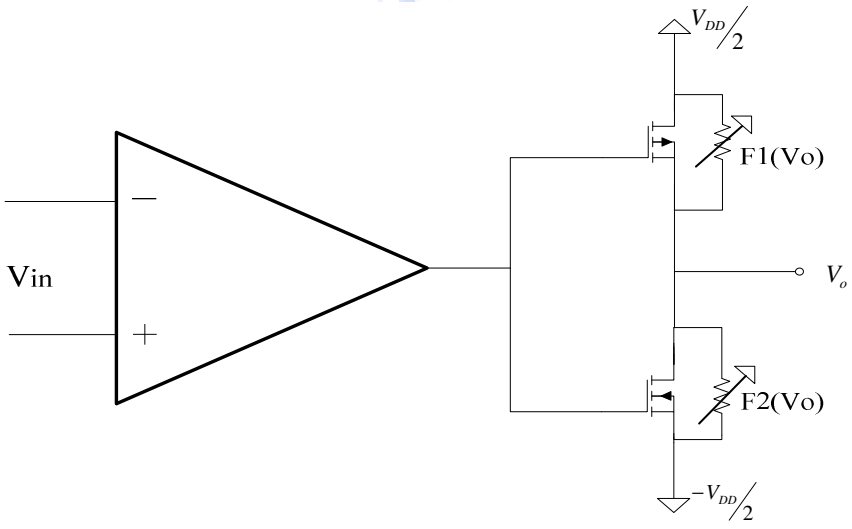


Fig. 5.7. A typical op-amp's configuration schematic considering nonlinear DC gain

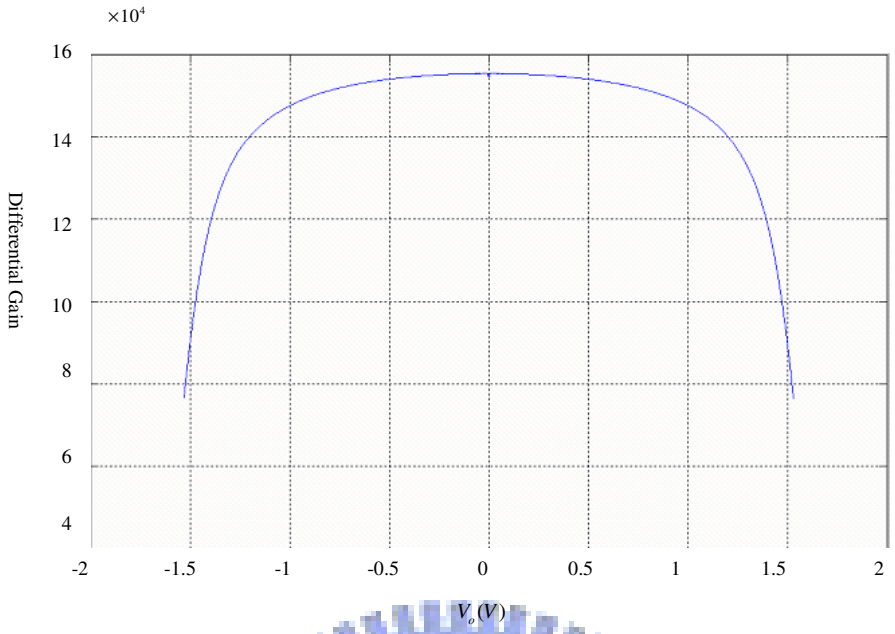


Fig. 5.8. A typical relationship between DC gain and V_o

center of scale and decreases as the magnitude of output voltage increases. This nonlinear gain introduces error components as distortion in the sigma-delta modulator output spectrum. Furthermore our HSPICE simulation based on TSMC 0.18μm process model reveals that $|V_{GSQ}|$ of the output-stage transistors and the maximum DC gain A_0 also affect the shape of

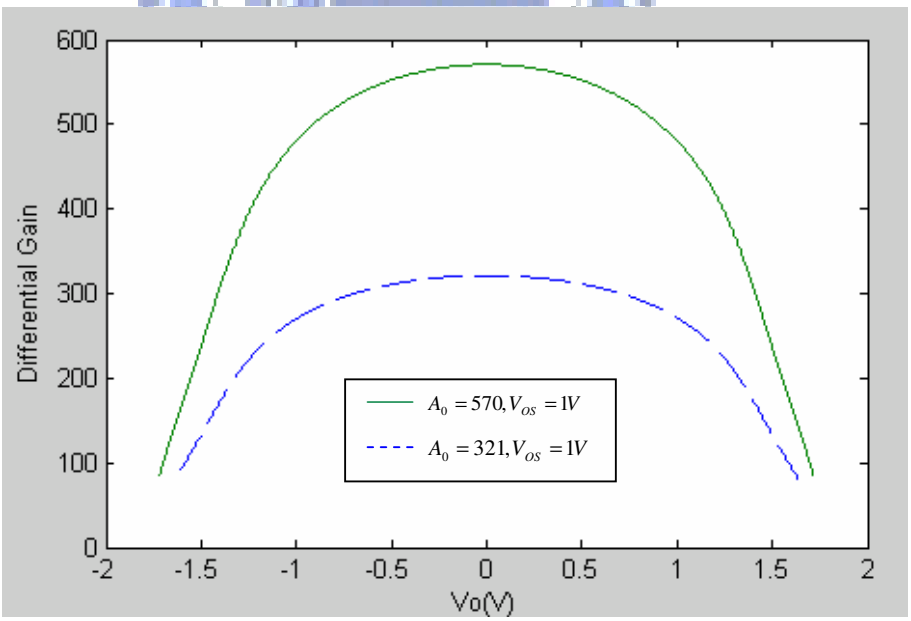


Fig. 5.9. Two nonlinear gain curves with identical V_{OS} but different A_0

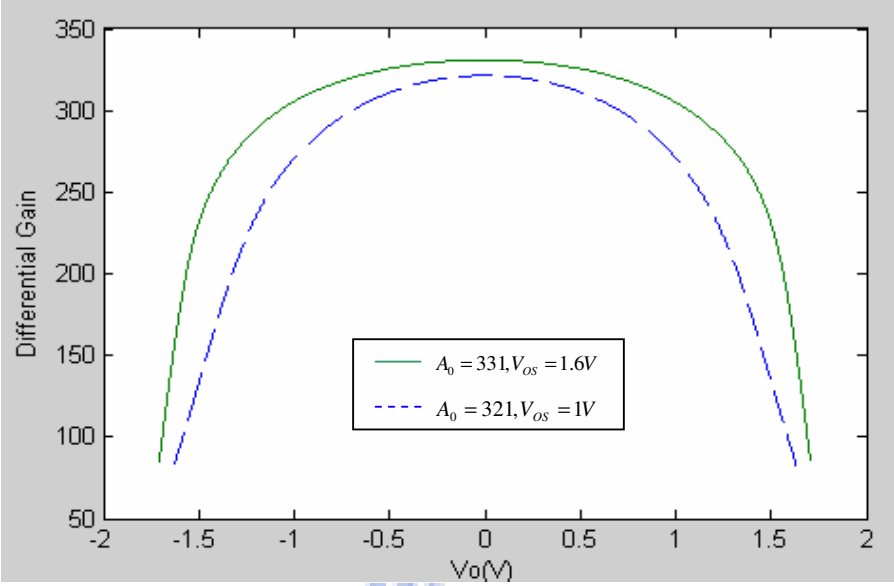


Fig. 5.10. Two nonlinear gain curves with similar A_0 but different V_{OS}

the nonlinear curves. The relationship between the range of maximum output swing (V_{os}) and nonlinear curves replace the one between $|V_{GSQ}|$ and nonlinear curves. Thus, in dealing with OTA distortions, we are basically faced with a family of nonlinearities.

It is discussed in [Gee02] and [Lee85] about the distortion due to a particular nonlinear curve approximated by the polynomial

$$A_V(V_o) = A_0(1 + q_1 V_o + q_2 V_o^2 + q_3 V_o^3 + q_4 V_o^4 + \cdots) \tag{5.15}$$

where $A_V(v_o)$ is finite DC gain of OTAs, and A_0 is the maximum finite DC gain when V_o is in the neighborhood of 0V. Although some expressions for harmonic distortions are derived in [Gee02] and [Lee85], these result are not completed. They are also of little use for optimization purpose since they did not relate harmonic distortions to design parameters. In this subsection, we will drive a complete OTA gain distortion model for 0.18μm process. There are two steps. In the first step, we try to model the family of nonlinear curves. Next, based on this nonlinear curve model, we derive the distortion model. The behavior simulation model offered by [Zar05] is applied to verify this model.

For the first step, our HSPICE simulation based on TSMC 0.18μm process model reveals that, in addition to output voltage V_o, both the $|V_{GS}|$ of output stage transistors and the maximum DC gain A_0 can affect the shape of the nonlinear curves. Thus, in dealing with OTA distortions, we are basically faced with a family of nonlinearities. Since $|V_{GSQ}|$ is inversely proportional to the range of maximum output swing V_{OS}, we identify V_o, A_0 and V_{OS} as the three parameters that can affect OTA DC gain A_V. We simulated on a simple two-stage operation amplifier shown in Fig. 5.11 to produce two specific cases shown in Fig. 5.9 and Fig. 5.10. Figure 5.9 shows how variation in A_0 can affect the curve shape. Figure 5.10 demonstrate the case when variation is mainly in V_{OS}. In order to model the nonlinear DC gain A_V, we tried various combination of A_0 and V_{OS} to the curve shape. In order to model the nonlinear DC gain A_V, we tried various combination of A_0 and V_{OS} to create a set of representative curves for the family of nonlinear DC gain curves. Then, after intensive

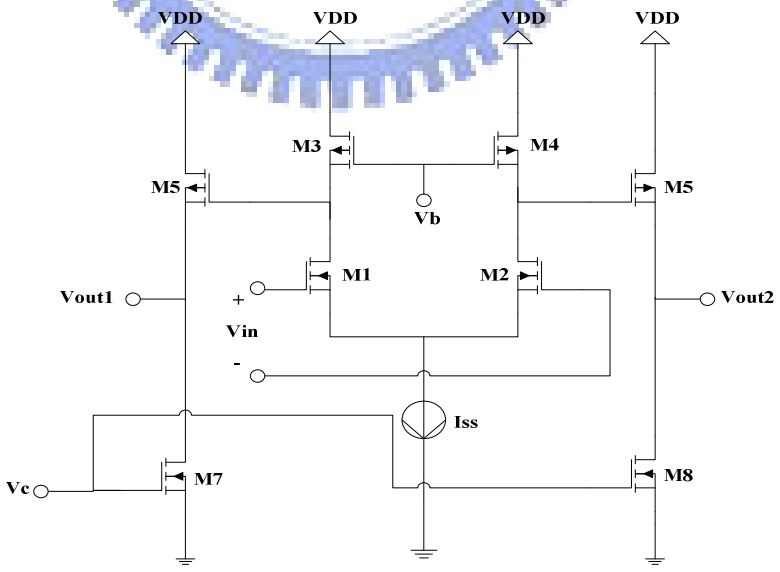


Fig. 5.11. A simple two-stage operation amplifier

trials we tried various combination of A_0 and V_{OS} to the curve shape. In order to model the nonlinear DC gain A_V, we tried various combination of A_0 and V_{OS} to create a set of representative curves for the family of nonlinear DC gain curves. Then, after intensive trials and errors, we come up with the following function to fit the nonlinear curves.

$$A_V(A_0, V_{OS}, V_o) = A_0 \cdot \{1 - 0.5 \cdot [EXP(0.443 \cdot \frac{A_0^{0.03}}{V_{os}^{1.2}} V_o) + EXP(-0.443 \cdot \frac{A_0^{0.03}}{V_{os}^{1.2}} V_o) - 2]\} \quad (5.16)$$

After performing Taylor's series expansion on (14) over V_o, the model we arrive at is of the form

$$A_V(V_o) = A_0(1 + q_2 V_o^2 + q_4 V_o^4) \quad (5.17)$$

where q_2 and q_4 in (5.17) are

$$q_2 = -\frac{1}{2} \cdot (0.443 \cdot \frac{A_0^{0.03}}{V_{OS}^{1.2}})^2 \quad (5.18)$$

$$q_4 = -\frac{1}{24} \cdot (0.443 \cdot \frac{A_0^{0.03}}{V_{OS}^{1.2}})^4 \quad (5.19)$$

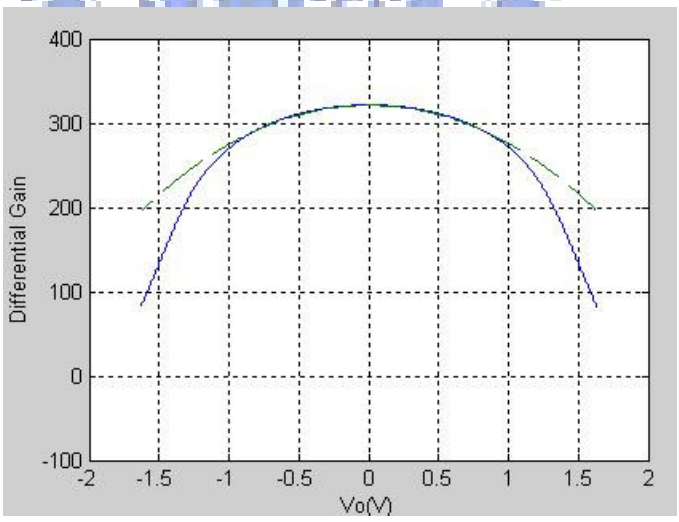
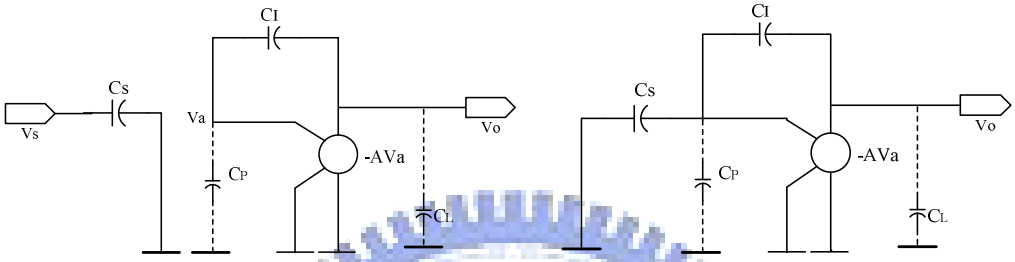


Fig. 5.12. A comparison between simulation of nonlinear curve function and practical design

In Fig. 5.12, $A_0 = 331, V_{OS} = 1.6V$, when V_o swing in (+1V ~ -1V), the simulation result of nonlinear curve function is close to the practical one. Although the two curves swing in (+1V

~ -1V) shown in this figure seems close, the 2nd order nonlinear coefficient of the nonlinear curve function $q_2 = -0.1387$ is close to that of the practical case $q_2 = -0.1106$, but the 4th order nonlinear coefficient of the nonlinear curve function $q_4 = -0.0032$ is much larger than that of practical case $q_4 = -0.0451$ since q_4 is very sensitive and difficult to be estimated, it causes that the 5th harmonic distortion estimation is not accurate, and we shall discuss later.



(a) sampling phase (b) integration phase

Fig. 5.13. Switch-capacitor integrator with finite-gain amplifier

The next work is to obtain the expressions to estimate harmonic distortions introduced by integrators with a nonlinear finite OTA gain OTA. Fig. 5.13 shows a model of a switched-capacitor integrator with a finite OTA gain amplifier [Gee02]. If C_P and C_L in Fig. 5.13. are neglected, the charge transfer can be expressed as

$$C_I \cdot (V_o^+ - V_a^+) - C_S \cdot V_a^+ = C_I \cdot (V_o^- - V_a^-) + C_S \cdot V_S \tag{5.20}$$

Notations $V_o^{\pm}$, $V_a^{\pm}$ and V_S represent $V_o((n \pm \frac{1}{2})T)$, $V_a((n \pm \frac{1}{2})T)$ and the difference between modulators input and feedback signal respectively [Gee02]. The relationship between the input and output voltage of the OTA is given by

$$V_o^{\pm} = -A(V_o^{\pm}) \cdot V_a^{\pm} \tag{5.21}$$

Substituting (5.16) and (5.21) into (5.20), one obtains the following expression

$$\frac{C_S}{C_I} \cdot V_s = (1 + \frac{1 + C_S / C_I}{A_0}) \cdot V_o^+ - (1 + \frac{1}{A_0}) \cdot V_a^- - \frac{q_2}{A_0}[(1 + \frac{C_S}{C_I}) \cdot (V_o^+)^3 - (V_o^-)^3]$$

$$-\frac{q_4}{A_0}[(1+\frac{C_S}{C_I})\cdot(V_o^+)^5-(V_o^-)^5] \tag{5.22}$$

In order to simplify (5.22), it is assumed in [Gee02] that $(1+\frac{1+C_S/C_I}{A_0})\cong 1$, $(1+\frac{1}{A_0})\cong 1$, $(1+\frac{C_S}{C_I})\cong 1$ and the final expression can be derived as

$$V_o^+-V_o^-\cong\frac{C_S}{C_I}\cdot\{1+\frac{q_2}{A_0}[(V_o^+)^2+(V_o^-)^2+V_o^+V_o^-]$$

$$+\frac{q_4}{A_0}[(V_o^+)^4+(V_o^+)^3V_o^-+(V_o^+)^2(V_o^-)^2+V_o^+(V_o^-)^3+(V_o^-)^4]\}\cdot V_s \tag{5.23}$$

In (5.23) the nonlinear term is

$$\frac{C_S}{C_I}\cdot\left(\frac{q_2}{A_0}[(V_o^+)^2+(V_o^-)^2+V_o^+V_o^-]+\frac{q_4}{A_0}[(V_o^+)^4+(V_o^+)^3V_o^-+(V_o^+)^2(V_o^-)^2+V_o^+(v_o^-)^3+(V_o^-)^4]\right)\cdot V_s \tag{5.24}$$

In order to build a mathematical expression related to input signal magnitude for estimating the distortion caused by nonlinear DC gain, $V_o^{\pm}$ and V_S must be expressed as functions of A_{in}. In single-loop second-order sigma-delta modulator, when a signal $Sin(wnT)$ apply to modulator input and quantization noise is not considered, V_S can be represented as

$$V_S(nT)=A_{in}\sin(wnT)-A_{in}\sin(w(n-2)T)$$

$$=A_{in}\left[(1-\cos(\frac{2\pi}{OSR}))\cdot\sin(wnT)-\sin(\frac{2\pi}{OSR})\cdot\cos(wnT)\right] \tag{5.25}$$

The output signal of the first integrator can be represented as [Gee02]

$$V_o^+=A_{in}\sin(w(n+\frac{1}{2})T)\cong A_{in}\left[\sin(wnT)+\sin(\frac{\pi}{2\cdot OSR})\cdot\cos(wnT)\right] \tag{5.26}$$

$$V_o^-=A_{in}\sin(w(n-\frac{1}{2})T)\cong A_{in}\left[\sin(wnT)-\sin(\frac{\pi}{2\cdot OSR})\cdot\cos(wnT)\right] \tag{5.27}$$

From (5.26) and (5.27) we can obtain the following equations

$$(V_o^{\pm})^2\equiv A_{in}^2[\frac{1}{2}(1-\cos(2wnT))\pm\sin(\frac{\pi}{2\cdot OSR})\cdot\sin(2wnT)] \tag{5.28}$$

$$(V_o^{\pm})^3\equiv A_{in}^3[\frac{1}{4}(3\sin(wnT)-\sin(3wnT))\pm\frac{3}{4}\sin(\frac{\pi}{2\cdot OSR})\cdot(\cos(wnT)-\cos(3wnT))] \tag{5.29}$$

$$(V_o^{\pm})^4 \equiv A_{in}^4[\frac{3}{8}-\frac{1}{2}\cos(2wnT)+(\frac{1}{8}-\sin^2(\frac{\pi}{2\cdot OSR}))\cdot\cos(4wnT)$$

$$\pm\sin(\frac{\pi}{2\cdot OSR})\cdot(\sin(2wnT)-\frac{1}{2}\sin(4wnT))] \quad (5.30)$$

$$V_o^+V_o^- = \frac{A_{in}^2}{2}[1-\cos(2wnT)] \quad (5.31)$$

$$(V_o^+)^2(V_o^-)^2 \equiv A_{in}^4[\frac{3}{8}-\frac{1}{2}\cos(2wnT)+(\frac{1}{8}+\frac{1}{2}\sin^2(\frac{\pi}{OSR}))\cdot\cos(4wnT)] \quad (5.32)$$

$$(V_o^{\pm})^3(V_o^{\mp}) \equiv A_{in}^4[\frac{3}{8}-\frac{1}{2}\cos(2wnT)+(\frac{1}{8}+\frac{3}{8}\sin^2(\frac{\pi}{2\cdot OSR}))\cdot\cos(4wnT)]$$

$$\pm\frac{1}{2}\sin(\frac{\pi}{2\cdot OSR})\cdot\sin(2wnT)\mp\frac{1}{4}\sin(\frac{\pi}{2\cdot OSR})\cdot\sin(4wnT)] \quad (5.33)$$

Substituting (5.25)-(5.33) into (5.24), the harmonic distortion formulas are

$$HD3 = A_{HD3\_1}\sin(3wnT)+A_{HD3\_2}\cos(3wnT) \quad (5.34)$$

$$HD5 = A_{HD5\_1}\sin(5wnT)+A_{HD5\_2}\cos(5wnT) \quad (5.35)$$

where

$$A_{HD3\_1} = \frac{C_S}{C_I}\{-\frac{3\cdot q_2\cdot A_{in}^3}{4\cdot A_0}[1-\cos(\frac{2\pi}{OSR})] \quad (5.36)$$

$$+q4\cdot A_{in}^5[-\frac{5}{16}(1-\cos(\frac{2\pi}{OSR}))-\frac{1}{8}\sin^2(\frac{\pi}{OSR})\cdot(1-\cos(\frac{2\pi}{OSR}))]\}$$

$$A_{HD3\_2} = \frac{C_S}{C_I}\{-\frac{3\cdot q_2\cdot A_{in}^3}{4\cdot A_0}\sin(\frac{2\pi}{OSR})$$

$$+q4\cdot\sin(\frac{2\pi}{OSR})\cdot A_{in}^5[-\frac{5}{4}+\frac{5}{16}\sin(\frac{2\pi}{OSR})+\frac{1}{8}\sin^2(\frac{\pi}{OSR})]\} \quad (5.37)$$

$$A_{HD5\_1} = \frac{C_S}{C_I}\cdot\frac{q_4\cdot A_{in}^5}{A_0}[\frac{5}{16}+\frac{1}{8}\cdot\sin^2(\frac{\pi}{2\cdot OSR})\cdot(1-\cos(\frac{2\pi}{OSR}))] \quad (5.38)$$

$$A_{HD5\_2} = \frac{C_S}{C_I}\cdot\frac{q_4\cdot A_{in}^5}{A_0}[\frac{5}{16}+\frac{1}{8}\cdot\sin^2(\frac{\pi}{2\cdot OSR})\cdot\sin(\frac{2\pi}{OSR})] \quad (5.39)$$

Substituting (5.18) and (5.19) into (5.36), (5.37), (5.38), (5.39) can obtain the complete 3rd and 5th harmonic distortion expressions as

$$A_{HD3\_1} = \frac{C_S}{C_I}\{\frac{3\cdot A_{in}^3}{8\cdot A_0}\cdot(0.443\cdot\frac{A_0^{0.03}}{V_{os}^{1.2}})^2\cdot[1-\cos(\frac{2\pi}{OSR})]$$

$$-\frac{1}{24}\cdot(0.443\cdot\frac{A_0^{0.03}}{V_{os}^{1.2}})^4\cdot A_{in}^5[-\frac{5}{16}(1-\cos(\frac{2\pi}{OSR}))-\frac{1}{8}\sin^2(\frac{\pi}{OSR})\cdot(1-\cos(\frac{2\pi}{OSR}))]\}\quad(5.40)$$

$$A_{HD3\_2}=\frac{C_S}{C_I}\{\frac{3\cdot A_{in}^3}{8\cdot A_0}\cdot(0.443\cdot\frac{A_0^{0.03}}{V_{os}^{1.2}})^2\cdot\sin(\frac{2\pi}{OSR})\quad(5.41)$$

$$-\frac{1}{24}\cdot(0.443\cdot\frac{A_0^{0.03}}{V_{os}^{1.2}})^4\cdot\sin(\frac{2\pi}{OSR})\cdot A_{in}^5[-\frac{5}{4}+\frac{5}{16}\sin(\frac{2\pi}{OSR})+\frac{1}{8}\sin^2(\frac{\pi}{OSR})]\}$$

$$A_{HD5\_1}=-\frac{1}{24}\cdot\frac{C_S}{C_I}\cdot\frac{A_{in}^5}{A_0}\cdot(0.443\cdot\frac{A_0^{0.03}}{V_{os}^{1.2}})^4[\frac{5}{16}+\frac{1}{8}\cdot\sin^2(\frac{\pi}{2\cdot OSR})\cdot(1-\cos(\frac{2\pi}{OSR}))]\quad(5.42)$$

$$A_{HD5\_2}=-\frac{1}{24}\cdot\frac{C_S}{C_I}\cdot\frac{A_{in}^5}{A_0}\cdot(0.443\cdot\frac{A_0^{0.03}}{V_{os}^{1.2}})^4\cdot[\frac{5}{16}+\frac{1}{8}\cdot\sin^2(\frac{\pi}{2\cdot OSR})\cdot\sin(\frac{2\pi}{OSR})]\quad(5.43)$$

The power of the 3rd and 5th harmonic distortions are

$$HD3_{NFDCG}(dB)=10\log\frac{(A_{HD3\_1}{}^2+A_{HD3\_2}{}^2)}{2}$$

$$HD5_{NFDCG}(dB)=10\log\frac{(A_{HD5\_1}{}^2+A_{HD5\_2}{}^2)}{2}\quad(5.44)$$

In (5.40)-(5.43) we can obtain the relationships between the each parameter and power of the harmonic distortions, which are listed in Table 5.2.

	$C_I\uparrow$	$C_S\uparrow$	$A_{in}\uparrow$	$A_0\uparrow$	$V_{os}\uparrow$	$OSR\uparrow$
Distortion size	↓	↑	↑	↓	↓	↓

Table 5.2 The relationship between the each parameter and power of the harmonic distortions

For a single-loop second-order sigma-delta modulator the behavior simulation result with input signal bandwidth=0.1MHz and $A_{in}=1\text{V}$, V_{os}=1.38V, A_0=52.5dB, OSR=24 and very small quantization interval is shown in Fig 5.14. It is clearly to observe that the even harmonic distortions are eliminated by fully differential output. Using behavior simulation for two cases to verify the above distortion models, the simulation based on a second-order ΣΔ ADC with input bandwidth 0.1 MHz, A_0 of case A and case B are 55.1 dB and 63.8 dB respectively,

and V_{os} of case A and case B are 1V and 1.38V respectively. The simulation results are listed in Table 5.3 and Table 5.4. In these tables, $HD3_{NFDCG}$ represents the power of the 3rd harmonic distortion, $HD5_{NFDCG\_A}$ and $HD5_{NFDCG\_B}$ represent the powers of the 5th harmonic distortions, $HD5_{NFDCG\_A}$ employ (5.18) and (5.19) to estimate q_2 and q_4, the practical nonlinear coefficients q_2 and q_4 are employed in $HD5_{NFDCG\_B}$. The two tables show that $HD5_{NFDCG\_A}$ and simulation results for SIMULINK are not close, because it (5.19) difficultly approach to q_4 closely. It is clearly observe that $HD5_{NFDCG\_B}$ and simulation results for SIMULINK are closer. Although $HD5_{NFDCG\_A}$ is not accurate, the power of HD5 can be neglected since it is too small and usually covered by noise floor. Fig. 5.14 shows the simulation results based on A_0 =52.7dB, V_{OS} =1.38V, OSR=16 and A_{in} =0.7v. In Table 5.3 and Table 5.4, $HD5_{NFDCG}$ is too small and covered by noise floor when $A_{in} = 0.2V$.

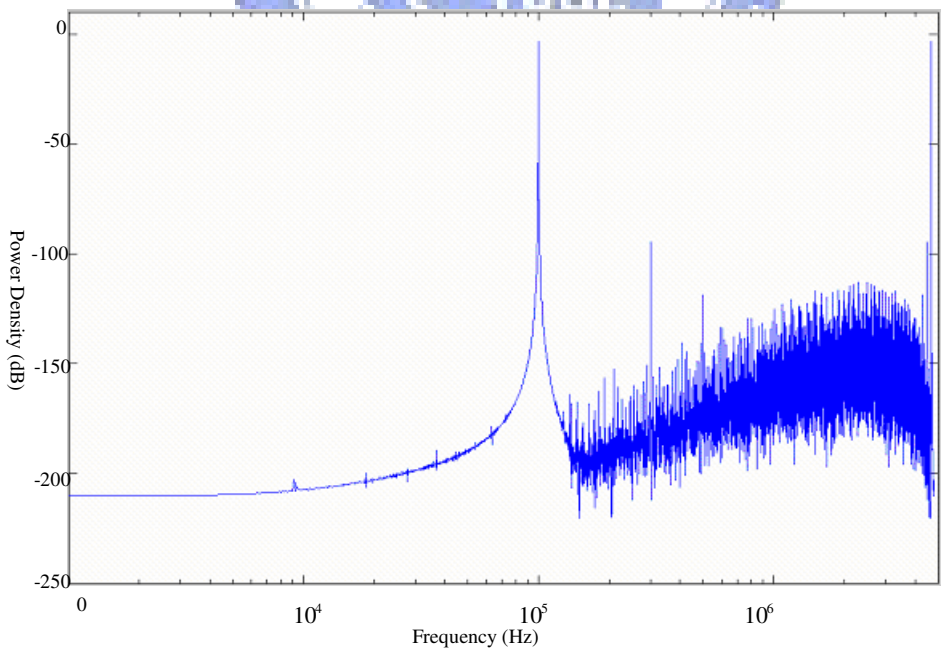


Fig. 5.14 Output spectrum of a second-order ΣΔ modulator with 3rd and 5th harmonic distortion

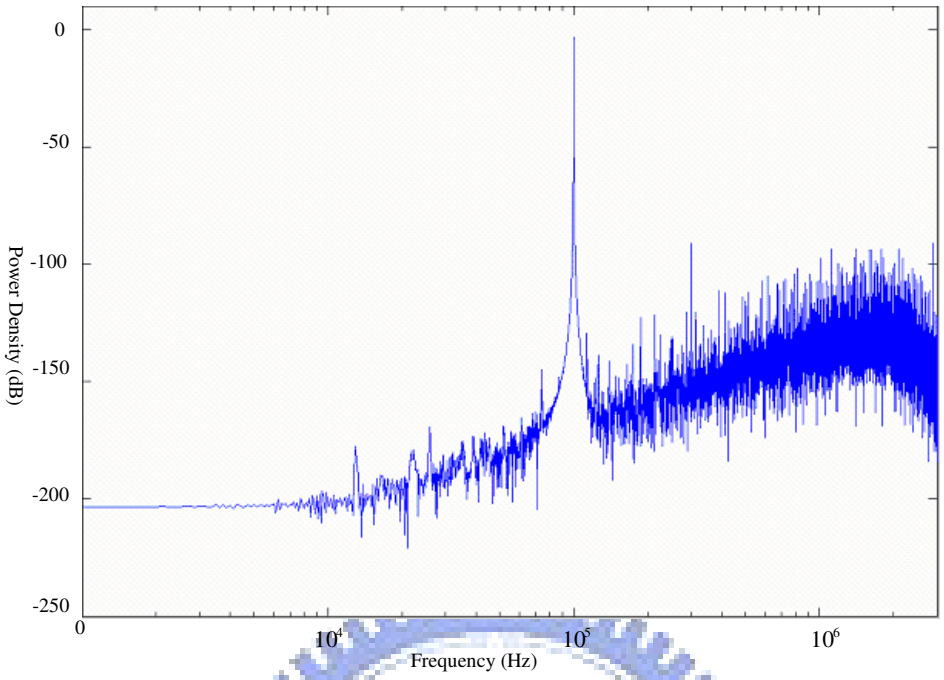


Fig. 5.15 Output spectrum of a second-order ΣΔ modulator with obvious 3rd harmonic distortion

$A_0 = 55.1dB$ $V_{os} = 1V$	Theoretic (dB)	SIMULINK (dB)
Ain = 0.2V OSR = 24	$HD3_{NFDCG} = -137.1$	$HD3_{NFDCG} = -139.2$
Ain = 0.2V OSR = 60	$HD3_{NFDCG} = -145$	$HD3_{NFDCG} = -148$
Ain = 0.2V OSR = 100	$HD3_{NFDCG} = -149.5$	$HD3_{NFDCG} = -152.1$
Ain = 0.5V OSR = 24	$HD3_{NFDCG} = -113.2$ $HD5_{NFDCG\_A} = -165.3$ $HD5_{NFDCG\_B} = -143.1$	$HD3_{NFDCG} = -115$ $HD5_{NFDCG} = -147.7$
Ain = 0.5V OSR = 60	$HD3_{NFDCG} = -121.2$ $HD5_{NFDCG\_A} = -173.2$ $HD5_{NFDCG\_B} = -151$	$HD3_{NFDCG} = -123.6$ $HD5_{NFDCG} = -156$
Ain = 0.5V OSR = 100	$HD3_{NFDCG} = -125.6$ $HD5_{NFDCG\_A} = -177.6$ $HD5_{NFDCG\_B} = -155.9$	$HD3_{NFDCG} = -127.1$ $HD5_{NFDCG} = -158$

Table 5.3 Comparison of theoretic result and behavior simulation for case A

$A_0 = 63.8dB$ $V_{os} = 1.38V$	Theoretic (dB)	Simulation (dB)
Ain = 0.2V OSR = 24	$HD3_{NFDCG} = -151.9$	$HD3_{NFDCG} = -151$
Ain = 0.2V OSR = 60	$HD3_{NFDCG} = -159.9$	$HD3_{NFDCG} = -159.8$
Ain = 0.2V OSR = 100	$HD3_{NFDCG} = -164.3$	$HD3_{NFDCG} = -163.5$
Ain = 0.5V OSR = 24	$HD3_{NFDCG} = -128.1$ $HD5_{NFDCG\_A} = -186.3$ $HD5_{NFDCG\_B} = -150.4$	$HD3_{NFDCG} = -126.3$ $HD5_{NFDCG} = -155$
Ain = 0.5V OSR = 60	$HD3_{NFDCG} = -136$ $HD5_{NFDCG\_A} = -194.3$ $HD5_{NFDCG\_B} = -158.4$	$HD3_{NFDCG} = -135$ $HD5_{NFDCG} = -163.4$
Ain = 0.5V OSR = 100	$HD3_{NFDCG} = -140.4$ $HD5_{NFDCG\_A} = -198.7$ $HD5_{NFDCG\_B} = -162.8$	$HD3_{NFDCG} = -138.6$ $HD5_{NFDCG} = -168$

Table 5.4 Comparison of theoretic result and behavior simulation for case B

5.3 Multi-bit DAC Distortion

Recently, multi-bit modulators are used often because it offers many advantages. However, multi-bit modulators using multi-bit DACs can introduce significant distortion into the modulator loop. Any error in the DAC response will be directly subtracted from the input signal and hence it appears at the output without the benefit of noise shaping. And any nonlinearity of the DAC will introduce a corresponding nonlinear signal distortion into the overall ADC response.

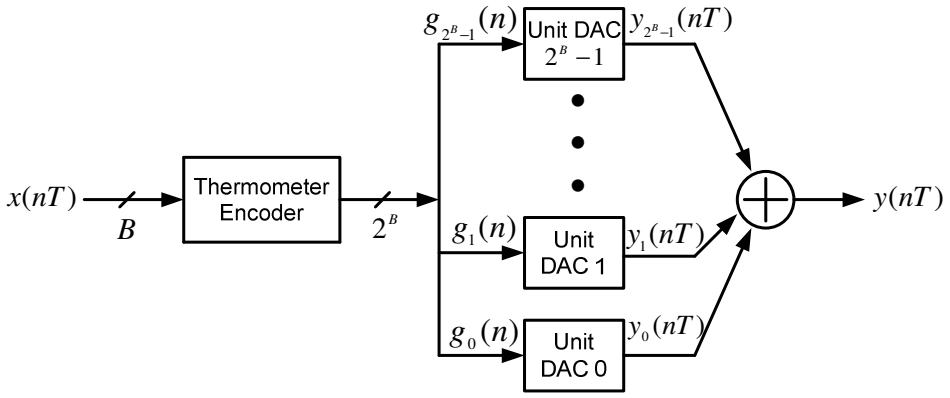


Fig. 5.16 A block diagram of a B-bit flash DAC

Fig. 5.16 shows a block diagram of a common B-bit flash DAC that relies on matched components between the unit DACs [Stu 01]. We define the output $y_k(nT)$ of the *k*th unit DAC as

$$y_k(nT) = \begin{cases} a_k, & g_k(n) = 1 \\ d_k, & g_k(n) = 0 \end{cases}$$

where a_k and d_k are the values of the activated and deactivated *k*th unit DAC, respectively. If $\bar{a}$ and $\bar{d}$ are defined as the average values of the activated and deactivated unit DACs, respectively, $y_k(nT)$ can also be rewritten as

$$y_k(nT) = \begin{cases} \bar{a} + h_k, & g_k(n) = 1 \\ \bar{d} + l_k, & g_k(n) = 0 \end{cases}$$

where h_k is the activated mismatch error of the kth unit DAC, and l_k is the deactivated mismatch error of the kth unit DAC. These errors h_k and l_k are random variables and they have the same standard deviations. The DAC's analog output $y(nT)$ can be written as

$$y(nT) = \sum_{k=0}^{2^B-1} y_k(nT) \qquad (5.45)$$

For a particular DAC input level, the DAC output will produce a corresponding value which is the sum of the unit DACs. Therefore, the DAC output value will contain the sum of the random variables h_k and l_k. Assuming the thermometer encoder activates $\chi(n)$ unit DACs

and deactivates the remaining $2^B - \chi(n)$ unit DACs, （5.45）can be written as

$$y(nT) = \chi(n) \cdot \left[\overline{a} + h_k\right] + \left(2^B - \chi(n)\right) \cdot \left[\overline{d} + l_k\right]$$

$$= \chi(n) \cdot \left(\overline{a} - \overline{d}\right) + 2^B \overline{d} + \chi(n) h_k + \left(2^B - \chi(n)\right) l_k \qquad (5.46)$$

Because h_k and l_k are random variables and have the same standard deviations, （5.46）can be written as

$$y(nT) = \chi(n) \cdot \left(\overline{a} - \overline{d}\right) + 2^B \overline{d} + 2^B l_k \qquad (5.47)$$

where $2^B l_k$ is the DAC output error and it is proportional to the unit DAC number 2^B and mismatch error l_k. As shown in Fig. 5.17 (a) is an ideal DAC and Fig. 5.17(b) is a DAC with mismatch. The DAC output level is the DAC unit number plus one. From Fig. 5.17(b) we can see that the DAC output levels are not equally spaced which results in the harmonic distortion, undesirable tones, as well as noise.

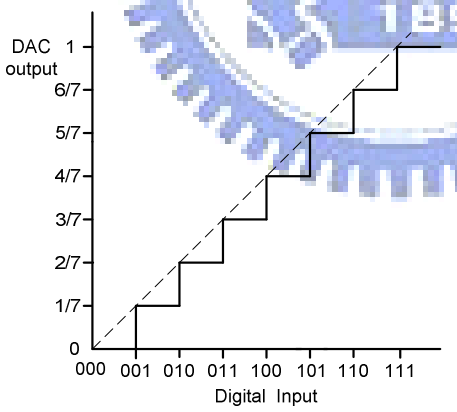


Fig. 5.17(a) Ideal DAC

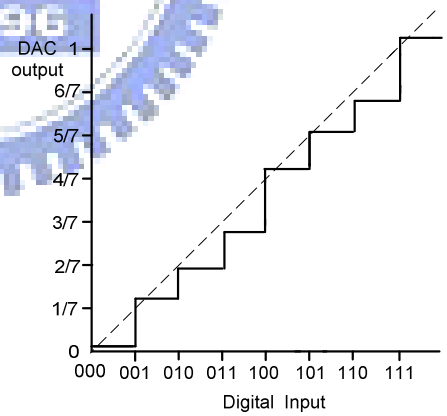
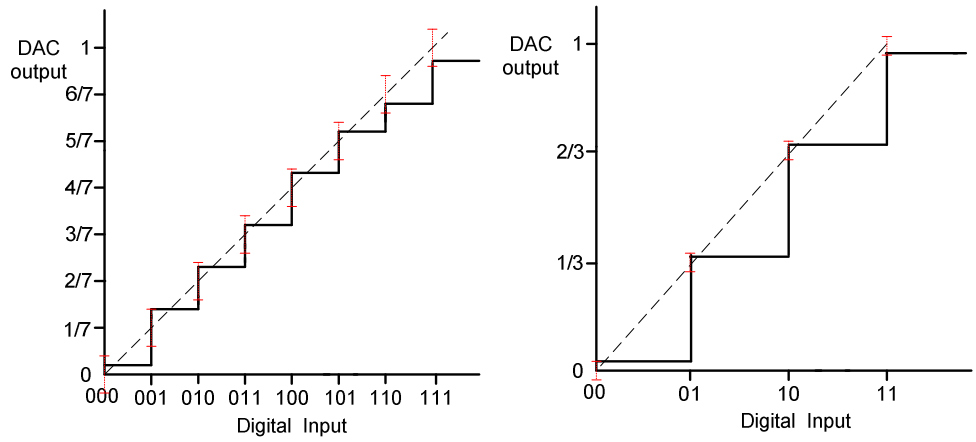
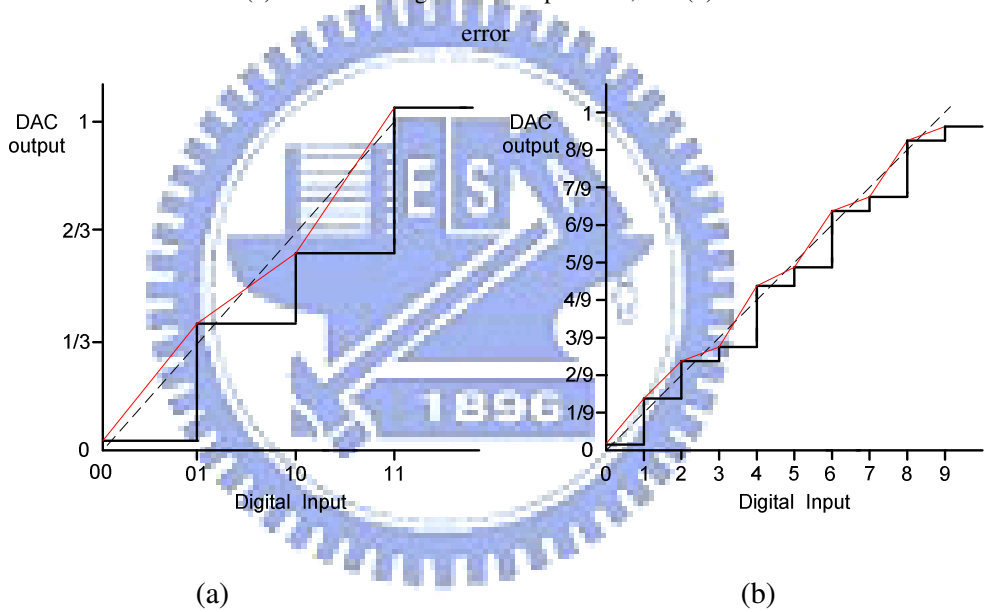


Fig. 5.17(b) DAC with mismatch



(a) (b)

Fig. 5.18 DAC transfer curve: (a) DAC with larger DAC output error, and (b) DAC with smaller DAC output



(a) (b)

Fig. 5.19 DAC transfer curve: (a) DAC with smaller output level, and (b) DAC with larger output level

Fig. 5.18 describes the DAC transfer curves with different DAC output error $2^B l_k$. From Fig. 5.18 we can see that the deviation of the non-ideal output level from the ideal one is equal to the DAC output error so that the deviation is related to the mismatch error h_k, l_k and unit DAC number 2^B. The larger the DAC output error is, the larger the deviation. Fig. 5.19 describes DAC transfer curves with different output levels. From Fig. 5.19 we can see that the frequency of levels oscillating up or below the ideal ones is relative to DAC output level. The larger the output level is, the larger the oscillation frequency, but they are

independent of the deviations. The discussions in Fig. 5.18 and Fig. 5.19 can provide us the tendency of deviations and frequencies of DAC transfer curves and what parameters they related to.

Therefore, assuming the deviation is *A* and frequency is *a*, from the above discussions, we assume the DAC output value can be written as

$$y(nT) = x(nT) + A\sin(a \cdot x(nT) + \theta) \qquad (5.48)$$

where $x(nT)$ is the DAC input, θ is a uniformly distributed random variable in $[0,2\pi]$ and $A\sin(a \cdot x(nT) + \theta)$ represent the effect of random variables h_k and l_k on the transfer curve. In ΣΔ modulator, $x(nT)$ is also the modulator output so it is usually a sinusoid $A_{in}\sin(\omega nT)$. From Fig. 5.18 and the DAC output error $2^B l_k$, we can expect the value of *A* is a function of the unit DAC number and standard deviation of capacitor mismatch, and the larger the DAC output error is, the larger the *A*. From Fig. 5.19 we expect a is a function of DAC output level and in a fixed input range the larger the output level is, the larger the radian frequency a.

In (5.48), $A\sin(ax + \theta)$ representing mismatches errors h_k and l_k can be further derived as:

$$\begin{aligned} A\sin(ax + \theta) &= A(\sin ax\cos\theta + \cos ax\sin\theta) \\ &= A\cos\theta\sin ax + A\sin\theta\cos ax \end{aligned} \qquad (5.49)$$

Utilizing Taylor's series, (5.49) can be expanded as follows:

$$A\cos\theta \times \sum_{n=0}^{\infty}(-1)^n \frac{(ax)^{2n+1}}{(2n+1)!} + A\sin\theta \times \sum_{n=0}^{\infty}(-1)^n \frac{(ax)^{2n}}{(2n)!}$$

$$= a_0 + a_1 x + a_2 x^2 + a_3 x^3 + a_4 x^4 + a_5 x^5 + \cdots$$

where $a_2 = A\sin\theta\left(-\frac{a^2}{2}\right), a_3 = A\cos\theta\left(-\frac{a^3}{6}\right), a_4 = A\sin\theta\frac{a^4}{24}, \cdots$

Therefore, when a sine-wave is applied to the modulator input such that $x(nT) = A_{in}\sin(\omega nT)$, the modulator output will produce harmonics due to the high order terms. These harmonics

are represented in power form below:

$$HD2_{DAC} = \frac{1}{2}\left(\frac{a_2}{2}A_{in}^2 + \frac{a_4}{2}A_{in}^4 + \frac{15a_6}{32}A_{in}^6 + \cdots\right)^2 = \frac{1}{2}\left(\frac{a_2'}{2}A_{in}^2 + \frac{a_4'}{2}A_{in}^4 + \frac{15a_6'}{32}A_{in}^6 + \cdots\right)^2 \cdot \sin^2\theta$$

$$HD3_{DAC} = \frac{1}{2}\left(\frac{a_3}{4}A_{in}^3 + \frac{5a_5}{16}A_{in}^5 + \cdots\right)^2 = \frac{1}{2}\left(\frac{a_3'}{4}A_{in}^3 + \frac{5a_5'}{16}A_{in}^5 + \cdots\right)^2 \cdot \cos^2\theta$$

$$HD4_{DAC} = \frac{1}{2}\left(\frac{a_4}{8}A_{in}^4 + \frac{3a_6}{16}A_{in}^6 + \cdots\right)^2 = \frac{1}{2}\left(\frac{a_4'}{8}A_{in}^4 + \frac{3a_6'}{16}A_{in}^6 + \cdots\right)^2 \cdot \sin^2\theta$$

where $a_2' = A\left(-\frac{a^2}{2}\right), a_3' = A\left(-\frac{a^3}{6}\right), a_4' = A\cdot\frac{a^4}{24}, \cdots$

Because θ is a uniformly distributed random variable in $[0,2\pi]$, the expected value of these harmonic powers can be further represent

$$E[HD2_{DAC}] = \frac{1}{2}\left(\frac{a_2'}{2}A_{in}^2 + \frac{a_4'}{2}A_{in}^4 + \frac{15}{32}a_6'A_{in}^6 + \cdots\right)^2 \cdot E[\sin^2\theta]$$

$$E[HD3_{DAC}] = \frac{1}{2}\left(\frac{a_3'}{4}A_{in}^3 + \frac{5}{16}a_5'A_{in}^5 + \cdots\right)^2 \cdot E[\cos^2\theta]$$

$$E[HD4_{DAC}] = \frac{1}{2}\left(\frac{a_4'}{8}A_{in}^4 + \frac{3}{16}a_6'A_{in}^6 + \cdots\right)^2 \cdot E[\sin^2\theta]$$

where $E[\sin^2\theta]$, $E[\cos^2\theta]$ is equivalent to 0.5. Finally, we further derive these harmonic distortions as a function of *A* and *a* and express in dB as follows.

$$E[HD2_{DAC}] \cong 20\log A\cdot\left|-0.125a^2A_{in}^2 + 0.010415a^4A_{in}^4 - 0.0003255a^6A_{in}^6\right|$$

$$E[HD3_{DAC}] \cong 20\log A\cdot\left|-0.02083a^3A_{in}^3 + 0.00130208a^5A_{in}^5\right|$$

$$E[HD4_{DAC}] \cong 20\log A\cdot\left|0.002604a^4A_{in}^4 - 0.00013021a^6A_{in}^6\right| \qquad (5.50)$$

In order to obtain *A* and *a*, we build a behavioral model of DAC including the mismatch of unit-elements and the unit-elements mismatches are assigned a Gaussian distribution with a specific standard deviation. By use of this DAC model and behavior simulation, simulations results on a second-order ΣΔ modulator with input frequency 0.1MHz, input amplitude 1V, 9-level quantization and standard deviation σ_{cap} = 0.316%, are shown in Fig. 5.20. Simulation results of the standard deviations of capacitance mismatch under different unit DAC number are tabulated in Table 5.5. These harmonic distortions are obtained by averaging

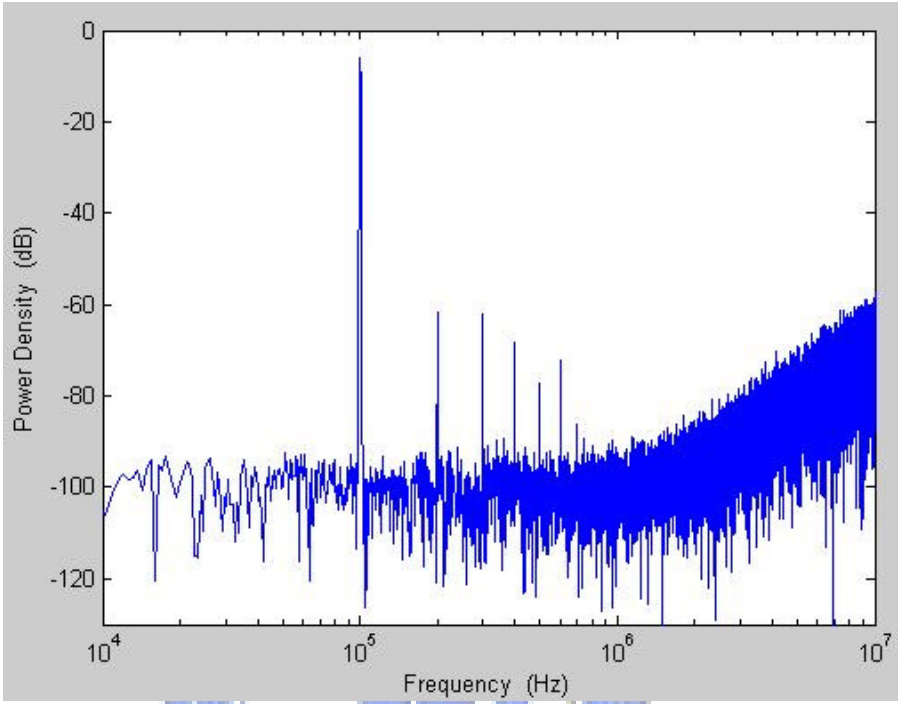


Fig. 5.20 Simulation results of DAC harmonic distortion

ten simulation results in a specific standard deviation and unit DAC number. We observe that when the unit DAC number increases, the harmonic distortions increase. Comparing（5.50）with Table 5.5 and expecting A is a function of the unit DAC number and standard deviation of capacitor mismatch and a is a function of unit DAC number, we conclude the following equations:

$$A = 0.566 \times \sqrt{u} \times \sigma_{cap}$$

$$a = 1.4667 + 0.0625 \cdot u + 0.0021 \cdot u^2 \qquad (5.51)$$

where u is the unit DAC number, σ_{cap} is the standard deviation of capacitor mismatch.

Std. deviation (σ_{cap})	Unit DAC number (u)	HD2 (dB)	HD3 (dB)	HD4 (dB)
0.316%	8	-54.59	-60.315	-67.63
0.316%	10	-53.93	-59.13	-61.69
0.316%	12	-50.3	-58.62	-60.29
0.316%	16	-48.97	-53.82	-61.635
0.1%	8	-65.79	-74.42	-74.48
0.1%	10	-63.39	-70.63	-80.70
0.1%	12	-62.98	-67.26	-73.49
0.1%	16	-59.62	-65.22	-73.44

Table 5.5 Simulation results of standard deviation of capacitor mismatch vs. unit DAC number with A_m=1

Next, in order to check our model if it is correct in other cases, we calculate our model (5.50) (5.51) and simulate the behavior DAC model to see if they are equal to each other. Theoritical results of harmonic distortion according to our model (5.50) (5.51) are tabulated in Table 5.6 and the corresponding simulation results are tabulated in Table 5.7. From Table 5.6 and Table 5.7, the two results are mostly close and they confirm that our DAC distortion model is reasonably precise. From (5.50) (5.51), we can plot $E[HD]$ vs. standard deviation of capacitance mismatch and DAC output level. It is shown in Fig. 5.21 and Fig. 5.22.

Std. deviation (σ_{cap})	Unit DAC number (u)	HD2 (dB)	HD3 (dB)	HD4 (dB)
0.05%	8	-79.945	-94.89	-112.4
0.05%	12	-75.39	-88.69	-104.56
0.05%	16	-71.58	-83.27	-97.51
0.025%	8	-85.97	-100.915	-118.42
0.025%	12	-81.41	-94.71	-110.58
0.025%	16	-77.60	-89.29	-103.53

Table 5.6 Theoretical results of standard deviation of capacitor mismatch vs. unit DAC number with A_m=0.5

Std. deviation (σ_{cap})	Unit DAC number (u)	HD2 (dB)	HD3 (dB)	HD4 (dB)
0.05%	8	-77.02	-90.77	-98.80
0.05%	12	-76.34	-86.75	-97.98
0.05%	16	-70.88	-78.53	-77.80
0.025%	8	-89.46	-102.44	-110.64
0.025%	12	-79.88	-89.56	-93.61
0.025%	16	-74.13	-87.48	-91.5

Table 5.7 Simulation results corresponding to Table 5.6

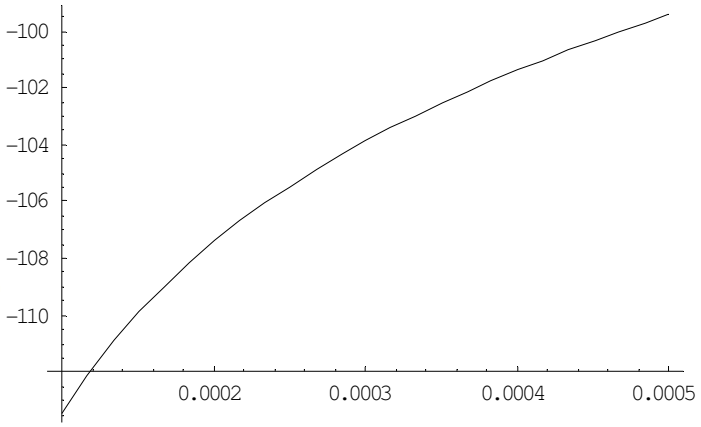


Fig. 5.21 HD2 vs. std. of mismatch with 3 Bit DAC and $A_{in} = 0.2$

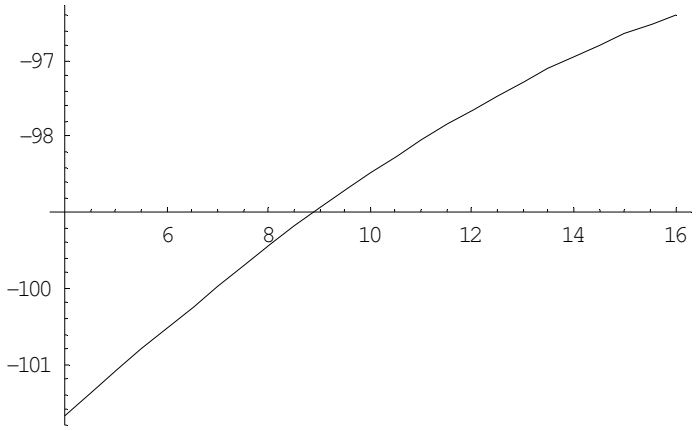


Fig. 5.22 HD2 vs. DAC output level with std. = 0.04% and $A_{in} = 0.2$

From Fig. 5.22, we can see that multi-bit DACs produce significant harmonic distortion when its output level is large.

5.4 Quantizer Nonlinearity Distortion

The quantization operation is inherently nonlinear because the quantizer error is determined from the quantizer input signal. For convenience, we usually model the quantizer as a linear model and approximate the quantization noise as a white noise. This approximation is made when the quantization error has the following properties, which we refer to collectively as the "input-independent additive white noise approximation" [Nor 97]:

Property 1. ε_n is statistically independent of the input signal or ε_n is uncorrelated with the input signal.

Property 2. ε_n is uniformly distributed in $[-\Delta/2, \Delta/2]$.

Property 3. ε_n is an independent identically distributed sequence or ε_n has a flat power spectral density.

where ε_n is the error sequence and Δ is the distance between output levels. Therefore, the quantization error from $\Sigma\Delta$ modulators is typically not white. For dc inputs, the quantization error is periodic, generating idle channel tones or pattern noise. For ac inputs, the quantization error is also periodic, containing components harmonically related to the input frequency and amplitude. One can view this effect as a time-domain distortion and therefore argue that the converter actually has less resolution than rms measurements. From the properties described above, one can see that multi-bit quantizers are closer to the linear model than single-bit ones and the time-domain distortions of multi-bit quantizers can be ignored, as shown in Fig. 5.23. From Fig. 5.23, we can see that the quantization noise is almost white and harmonic distortion is unapparent.

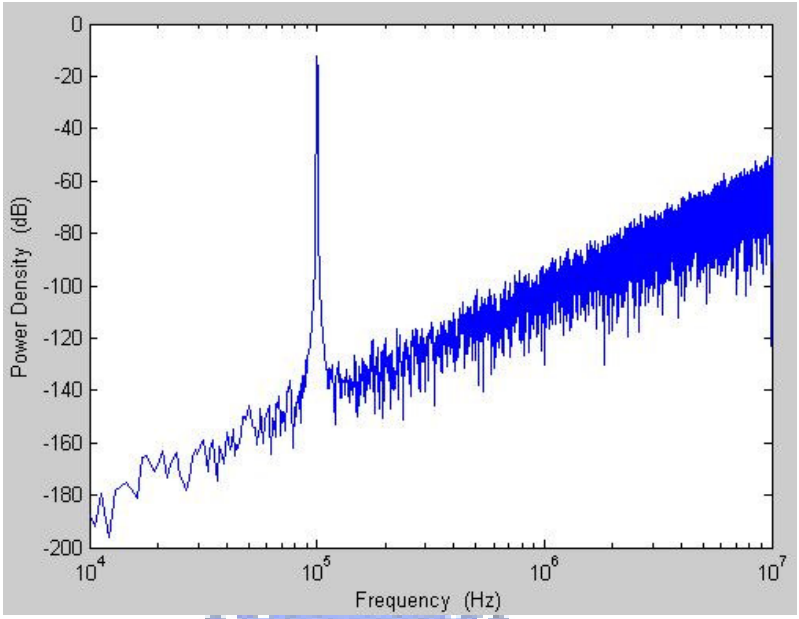


Fig. 5.23 PSD of second-order $\Sigma\Delta$ modulator with 5 quantization levels

5.5 Nonlinear Capacitance Distortion

Recently metal-insulator-metal(MIM) capacitor structure is the most popular capacitor fabrication in integrated circuits, which are widely used in analog, mixed-signal and RF circuits [Chu 05a]. Due to MIM capacitors in integrate circuits occupy a large portion of chip area, hence the high-K dielectrics into MIM capacitors is highly expected in near future [Kim 04a]. The stability of MIM capacitances are affected by three factors, which are bias voltage, operation frequency and temperature. Harmonic distortions occur at modulator output spectrum while these nonlinearities appear at integrators in $\Sigma\Delta$ modulators. Fortunately, there are several popular high-K dielectric materials studied to substitute the conventional SiO_2 and Si_3N_4, which are Ta_2O_5, HfO_2 and Al_2O_3. They suppress these nonlinearities effectively [Jeo 04]. In addition to the above mentioned three materials, [Kim 04b] provides a multi-layered dielectric, which is $HfO_2 - SiO_2$ stacked dielectric. Fig. 5.24 shows the capacitance variation versus bias voltage can be reduced by employing $HfO_2 - SiO_2$, the capacitance versus bias voltage is the most stable while $HfO_2(12\,nm)/SiO_2(4\,nm)$ is

employed. Fig. 5.25 shows that capacitance is increased follow the rise of temperature. This structure dielectric also offers an excellent improvement to reduce the impact of temperature for HfO_5 / S_iO_2. Due to the existing technique of capacitors fabrication exhibits the excellent linearity, hence the distortion cause by nonlinear capacitance in $\Sigma\Delta$ modulators can be neglected reasonable.

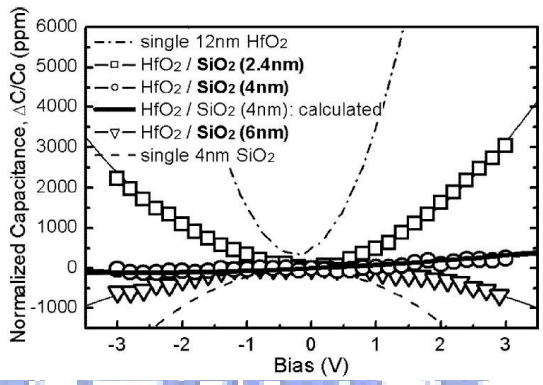


Fig. 5.24. Normalized C-V curves (△C/C) of MIM capacitors with single $HfO_2(12nm)$, single $SiO_2(4nm)$ and HfO_2 / SiO_2 stack.

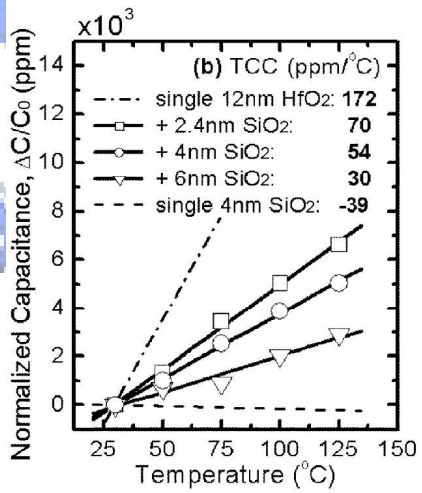


Fig. 5.25. Normalized capacitance vs. temperature

5.6 Nonlinear Switch Resistance Distortion

In $\Sigma\Delta$ modulators, the MOS switches in integrators introduce harmonic distortion since the resistances of the MOS switches depends on the voltages across the terminals. Fig. 26(a) shows a simple sample and hold circuit for NMOS [Hun04], and its resistance is given by

$$R_{on} = \frac{1}{\mu_n C_{OX} \frac{L}{W}(V_{gs} - V_{tn})} \tag{5.52}$$

where $V_{tn} = V_{t0} + \gamma\left(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}\right)$. (5.52) shows that the resistance varies with V_{in} and the body effect (V_{SB}) also contribute nonlinearity, especially in low voltage. There several techniques for improving this nonlinearity were proposed in [Hun04], [Ste99] and [Ong00]. [Hun04] mention a new sample-and-hold circuit, which is shown in Fig. 26(b). In order to avoid the variation of resistance, this proposed circuit can fix V_{gs} in V_{dd} and $V_{SB} = 0V$. Hence the resistance of the switch can be given by

$$R_{on} = \frac{1}{\mu_n C_{OX} \frac{L}{W}(V_{dd} - |V_{t0}|)} \tag{5.53}$$

[Ste99], [Ong00] and [Kim02] also proposed several techniques to improve the effects of V_{in}. According to the above discussion, due to there are several existed methods to reduce this nonlinear phenomenon effectively, hence we don't involve the distortion into final optimization.

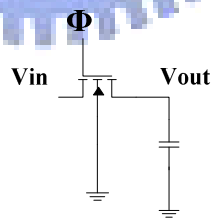


Fig. 5.26(a). A simple sample and hold circuit.

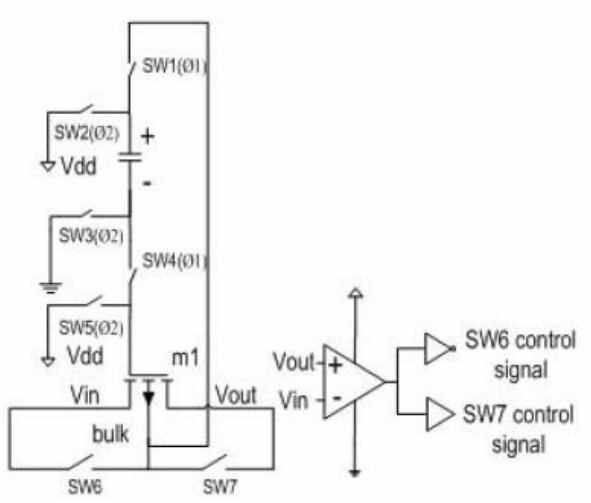


Fig. 26(b). The proposed switch circuit

6

Models of Sigma-Delta Modulator Power Consumption

The power estimation can be derived into the analog power consumption and the digital power consumption. The analog power consumption mainly is from the OTAs of the integrators, quantizer, and DAC. The digital power consumption is mainly from CMOS switches and clock generator.

Basic OTA structures	Single-stage telescope	Folded cascade	two-stage Miller -compensated
k_{OTA}	2	4	7.76

Table 6.1. k_{OTA} for three common OTA structures.

6.1 Analog Power Consumption

In $\Sigma\Delta$ modulator, the power dissipation from integrators occupies the largest portion of analog power consumption. The power consumption of OTAs can be presented as

$$POW_{OTA} = I_{OTA} \cdot V_{DD} = k_{OTA} \cdot I_B \cdot V_{DD}$$

where I_{OTA} represents the total current of the OTA, I_B represents the bias current of each transistor of the input differential pair of OTA, k_{OTA} represents the ratio of the total current of the OTA to this bias current, and it depends on the chosen OTA architecture. The values of k_{OTA} for three common OTA structures are listed in Table 6.1[Hsu 07]. V_{DD} represents the supply voltage of the OTA. I_B can be written as

$$I_B = \frac{1}{2} \cdot gm \cdot V_{reff} = f_{cl2} \cdot \pi \cdot C_{L2} \cdot V_{reff}$$

where f_{cl2} is the *GBW* of the OTAs, C_{L2} is the effective close-loop capacitance, and V_{reff}

is the overdrive voltage of the transistor of the input differential pair of OTA. Hence the power consumption of an integrator can be written as

$$POW_{OTA} = V_{DD} \cdot k_{OTA} \cdot f_{cl2} \cdot \pi \cdot C_{L2} \cdot V_{reff}$$

The total power consumption of integrators in $\Sigma\Delta$ modulator can be presented as

$$POW_{\Sigma\Delta\_OTA} = V_{DD} \cdot k_{OTA} \cdot f_{cl2} \cdot \pi \cdot C_{L2} \cdot V_{reff} \cdot k_{\Sigma\Delta} \quad (6.1)$$

where $k_{\Sigma\Delta}$ represents the ratio between the total power consumption of all the integrators and the first integrator. Observing clearly that it increases significantly as the order of the converter increases since an extra integrator is required.

A common DAC branch in $\Sigma\Delta$ modulator is shown in Fig. 6.1. If the sampling period and integration period are both assumed by $T/2$, the power consumption of an unit capacitor C_u in the multi-bit DAC is

$$POW_{Cu} = \frac{1}{T}\left(\int_0^{T/2} V_{Cu}(t) \cdot I_{Cu}(t)dt - \int_{T/2}^{T} V_{Cu}(t) \cdot I_{Cu}(t)dt\right) \quad (6.2)$$

Employing $I_{Cu} = C_u \cdot \frac{dV_{Cu}}{dt}$ to replace I_{Cu} in (6.2), then (6.2) can be simplified as

$$POW_{Cu} = V_{ref}{}^2 \cdot C_u \cdot f_s$$

If $C_u = \frac{1}{2^{B-1}} \cdot C_S$ is assumed, then the total power consumption of DAC in $\Sigma\Delta$ modulator can be written as

$$POW_{DAC} = 2 \cdot k_{Cs} \cdot V_{ref}{}^2 \cdot C_S \cdot f_s \quad (6.3)$$

where k_{Cs} is the ratio between the summation capacitance of C_S in all stages and the one in the first stage.

For quantizer power consumption, [Lau02] offers an good accuracy model as

$$POW_{Quantizer} = \frac{V_{DD}{}^2 \times L_{\min} \times (f_S + f_B)}{10^{(-0.1525 \times B + 4.838)}} \quad (6.4)$$

where $L_{\min}$ is the minimum channel length of the technology associated. According to the above discussion, the total analog power consumption of $\Sigma\Delta$ modulator is

$$POW_{ana\log} = POW_{OTA} + pOW_{DAC} + POW_{Quantizer} \tag{6.5}$$

6.2 Digital Power Consumption

The digital power consumption is mainly from the clock generator when decimation filter and anti-filter doesn't be considered. As we know the dynamic power dissipation is the mainly power dissipation of CMOS logic gates and related to their loading capacitors. Fig. 6.1 shows a clock generator with non-overlapping clocks which is connected to an external oscillator, and observing obviously that it is mainly composed of a lot of inverters [Gee02]. The average dynamic power consumption of a CMOS inverter gate can be written as

$$POW_{dynamic} = f_S \cdot C_{Logic} \cdot V_{DD}^2$$

where C_{Logic} is the loading capacitors of CMOS logic gates. Assuming a clock generator has N_C CMOS inverters and all inverters have identical capacitance of C_{Logic}, then the dynamic power consumption of clock generator is

$$POW_{CLOCK} \cong N_C \cdot f_S \cdot C_{Logic} \cdot V_{DD}^2$$

Another important source of the digital power dissipation is from CMOS transmission gates in the switched-capacitor circuits. The output of the clock generator is connected to the gate of the CMOS switches in the switched-capacitor circuits. The CMOS switch is shown in Fig. 6.2. Assuming that the number of the CMOS transmission gate in $\Sigma\Delta$ modulator is N_S and the gate capacitances of all CMOS transmission gates are C_{Logic}, and which can be written as

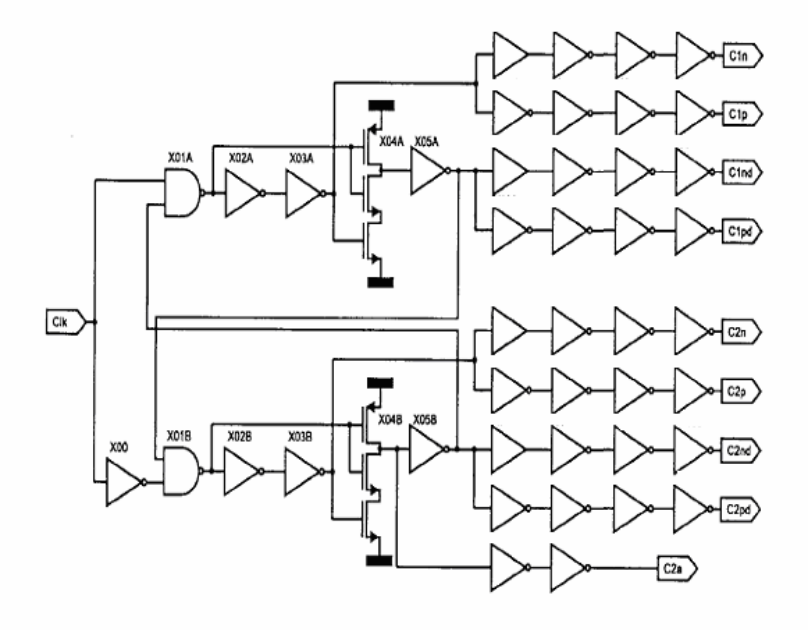


Fig. 6.1. A clock generator with non-overlapping clocks

$$C_{gate} = C_{OX} \cdot W \cdot L \tag{6.6}$$

where C_{OX} is the capacitance per unit area of the gate oxide. W and L are the width and length of the gate oxide respectively. C_{OX} can be written as

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

where the permittivity $\varepsilon_{OX} = 3.9\varepsilon_0$ for S_iO_2 and ε_0 is the permittivity of free space, 8.85×10^{-14} F/cm. The parallel resistance for the of NMOS and PMOS is

$$R_{switch} = \frac{1}{\mu_n \cdot C_{OX} \cdot \left(\frac{W}{L}\right)_n \cdot \left(V_{DD} - V_{tn} - |V_{tp}|\right)} \tag{6.7}$$

(6.6) employs the supposition as

$$\mu_n \cdot C_{OX} \cdot \left(\frac{W}{L}\right)_n = \mu_p \cdot C_{OX} \cdot \left(\frac{W}{L}\right)_p$$

Combining (6.6) with (6.7) C_{gate} can be expressed as

$$C_{gate} = \frac{L_{\min}^2}{\mu_n \cdot R_{CMOS} \cdot \left(V_{DD} - V_{tn} - \left|V_{tp}\right|\right)}$$

The power consumption for all the transmission gates is

$$POW_{Switch} = N_S \cdot f_S \cdot C_{gate} \cdot V_{DD}^2 \tag{6.8}$$

Finally, the total digital power consumption is

$$POW_{digital} = POW_{CLOCK} + POW_{Switch} \tag{6.9}$$

The total power consumption in signal-loop $\Sigma\Delta$ modulator is

$$POW_{total} = POW_{analog} + POW_{digital} \tag{6.10}$$

7

Design Optimization of Sigma-Delta ADCs Design

Power, noise and distortion models derived in Chapter 4, 5 and 6 are employed to systematically discuss how each design parameter affects the *SNDR* and power consumption. After identifying critical parameters, we will use them to do design optimization, in order to search for parameter optimal combinations. Before the discussions, we formally define the peak *SNDR* at ΣΔ ADC output as

$$SNDR = \frac{(2A_{in})^2/2}{P_Q + P_{AV} + P_{\varepsilon 1} + P_{\varepsilon 2} + P_{dac} + P_{jitter} + P_{sw} + P_{OTA} + HD_{settling} + HD_{NFDCG} + HD_{DAC}} \quad (7.1)$$

7.1 Design Parameters Discussions

Based on models in Chapter 4, 5, and 6 the influences of each design parameter to the *SNDR* and *Power* are discussed in the following:

1. ***OSR*** can influence the behavior of all nonidealities and power consumption. Higher OSR is helpful to reduce settling distortion. But, OSR is proportional to the digital power consumption according to（4.42）.
2. ***B*** is an important system parameter. Higher bit number results in smaller quantizer level and relaxes the dynamic requirement of OTA. But, the settling distortion doesn't change with B and higher B will introduce significant DAC distortion. Both the DAC noise power （4.36）and the digital power consumption（4.43）increase exponentially with B.
3. ***n*** is the order of a ΣΔ modulator. Increasing *n* will increase the value of A_{VS} such that it will increase the settling distortion.

4. A_0 is the open loop gain of OTA. Finite A_0 will cause nonlinear op-amp gain distortion. Simulation shows that a minimum required *A* is about 60 dB.

5. $a_1 = C_S / C_1$ is the gain coefficient of the first integrator, and usually varies from 0.1 to 1.

6. ***R*** is the on-resistance of switches. The on-resistance of switch S1 is dependent on the input signal, so it produces harmonic distortions. Appropriate design can be obtained to have negligible harmonic distortions.

7. ***GBW*** means the effective gain bandwidth of OTA during integration phase. A larger *GBW* can reduce the settling distortion, but increase analog power consumption（4.41）.

8. C_S is the capacitance of sampling capacitor. Its value depends on the stored voltage slightly so it produces little harmonic distortions.

9. V_{OS} is the maximum output swing of OTA. It effects nonlinear finite OTA gain distortion size.

10. ***SR*** is the OTA slew rate and plays an important role in integrator output settling performance. The larger *SR*, the smaller settling noise and distortion is.

11. σ_{cap} is the standard deviation of unit capacitor and its value depends on process technology. Recently, double poly and metal-insulator-metal (MIM) capacitor are the two main methods to implement capacitors in analog integrators circuits. These two types of capacitors have high linearity and good matching accuracy, and σ_{cap} of them are all below 0.05%. The main influence of σ_{cap} on ΣΔ modulators is the multi-bit DAC linearity.

	$B\uparrow$	$OSR\uparrow$	$n\uparrow$	$R\uparrow$	$GBW\uparrow$	$C_S\uparrow$	$SR\uparrow$	$V_{OS}\uparrow$	$\sigma_{cap}\uparrow$
P_Q	↓	↓	↓	—	—	—	—	—	—
P_{AV}	↓	↓	↓	—	—	—	—	—	—
$P_{\varepsilon 1}$	↓	↑	—	↑	—	↑	—	—	—
$P_{\varepsilon 2}$	↓	↑	—	—	↓	↑	↓	—	—
P_{dac}	↑	↓	—	—	—	—	—	—	↑
P_{jitter}	—	↓	—	—	—	—	—	—	—
P_{sw}	—	↓	—	—	—	↓	—	—	—
P_{OTA}	—	↓	—	—	↑	—	—	—	—
P_{ref}	—	↓	—	↓	↓	↓	—	—	—
$HD_{settling}$	↓	↓	↑	↑	↓	↑	↓	—	—
HD_{NFDCG}	—	↓	—	—	—	↑	—	↓	—
HD_{DAC}	↑	—	—	—	—	—	—	—	↑
$Power$	↑	↑	↑	↓	↑	↑	↑	—	—

Table 7.1 Summary of noise and distortion-power and power-rating when design parameters increase

In Table 7.1, P_Q is the quantization noise. P_{AV} is the leaky quantization noise. P_{ε_1} is the setting error during the sampling phase. P_{ε_2} is the setting error during the integration phase. P_{dac} is the DAC noise. P_{jitter} is the jitter noise. P_{sw} is the switch thermal noise. P_{OTA} is the OTA thermal noise. P_{ref} is the reference circuits thermal noise. $HD_{settling}$ is the settling distortion. HD_{NFDCG} is the nonlinear finite-OTA-gain distortion. HD_{DAC} is the DAC distortion. Table 7.1 summarizes the above discussions. Basically we identify *B*, *OSR*, *n*, *R*, *GBW*, C_S and *SR* as the optimization process design parameters. Table 7.1 shows qualitatively how distortion and power are affected when a particular design parameter increases, and it reveals that the ΣΔ ADC design task is a very complex one.

7.2 Design Optimization

In the following we describe the design optimization approach and it will help designers reach an optimal design quickly. It is based on the noise, distortion and power models described in Chapter 4, 5 and 6. The complete flow of the optimization methodology is shown in Fig. 7.1. The input signal bandwidth (Hz) and the output signal *SNDR* (dB) are treated as design specifications. We modify the figure-of-merit (FOM) [Sch 05] function by multiplying a variable *K* to the *SNDR* term of FOM, to become our weighting function.

$$\text{Weighting Function} = K \cdot SNDR_{\text{dB}} + 10\log\left(\frac{f_B}{Power}\right) \qquad (7.2)$$

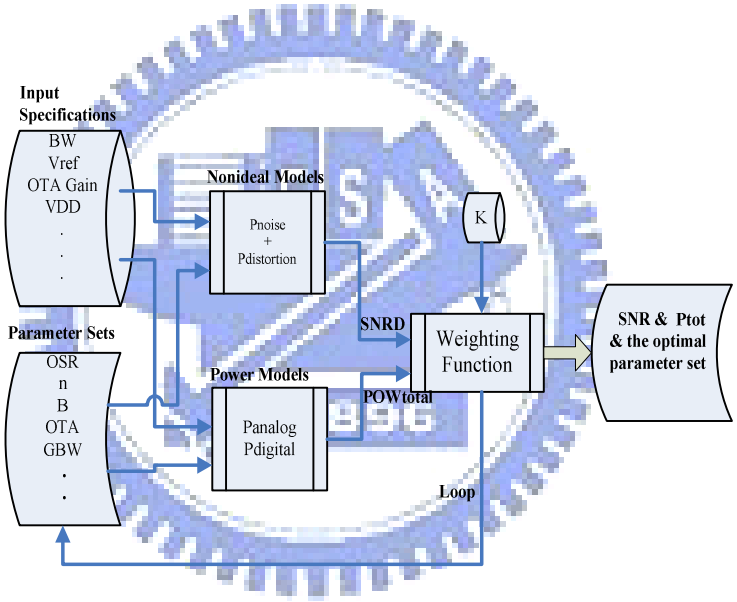


Fig. 7.1 Proposed design optimization for the $\Sigma\Delta$ modulator design

In (7.2) the *SNDR* and the inverse of *Power* are both expressed in log scale. The design optimization approach basically searches through the entire parameter space to find the set of design parameters which maximize the Weighting Function. By maximizing the Weighting Function we can increase *SNDR*(7.1)and reduce *Power*(4.45)at the same time. The constant *K* serves as the relative weighting between *SNDR* and *Power*. A larger *K* would result in a larger *SNDR* and *Power*. Some optimization iterations may be required. Typically, if we prefer high resolution designs, we set *K* higher and *SNDR* plays a more important role than *Power*;

on the other hand, if we prefer low power designs, we can set K lower. After an optimization process, the set of design parameters resulting in the largest Weighting Function value is the process outcome and is evaluated. If not acceptable, the K is adjusted and the optimization process is repeated. The parameter searching space is specified to be

- OSR : 8 ~ $\dfrac{80\ \text{MHz}}{2 \cdot f_B}$
- B : 1 ~ 6
- n : 1 ~ 3
- R : 100 Ω ~ 300 Ω
- GBW : 50 MHz ~ 500 MHz
- SR : 50 V/μs ~ 500 V/μs
- C_S : 1 pF ~ 10 pF

The parameters σ_{cap} and V_{ref} depend on the technology, so they are set before the optimization. During the optimization process, the gain coefficients a_i are specified according to the rules provided in [Mar 98b]. The optimization algorithm systematically searches the entire parameter space listed above.

8
Simulation Results

The design optimization described above is implemented by Mathematica®. In order to demonstrate the accuracy and practicability of our models, we apply it to a published design case, which is a ΣΔ modulator in 0.18-um CMOS technology for ADSL-CO application [Gag 03]. Its peak *SNDR* can reach 78dB over 276kHz signal bandwidth.

To compare with the design of [Gag 03], the optimization algorithm uses the same specifications as those in [Gag 03]. They are:

- Peak *SNDR* : 78 dB
- Signal bandwidth : 276 kHz

The OTA gain A_0 is set at 60 dB and the V_{ref} is set at 0.9 V for a 1.8 V power supply in 0.18-μm CMOS technology. The matching of capacitor σ_{cap} is set at 0.04% for the MIM capacitance. V_{OS} is set at 1V. The parameter variable ranges are also specified as follows. For the signal bandwidth of 276 kHz, the range of *OSR* is set between 8 ~ 128, and the quantizer bit *B* is between 1 ~ 5. The order n is between 1 ~ 3, since using a n higher than 3 may cause instability. The *R* range is between 100 Ω ~ 300Ω. C_S is between 1 pF and 10 pF. The minimum size of C_S is usually determined by process technology. Finally, *GBW* and *SR* are between 50 MHz ~ 500 MHz and 50 V/μs ~ 500 V/μs respectively. The results published in [Gag 03] and those obtained from our optimization methodology are all listed in Table 8.1, which includes three optimization results corresponding to *K*=0.5, *K*=2, and *K*=5.

circuit parameters	Ref [Gag03]	*K*=0.5	*K*=2	*K*=5	Unit
OSR	96	32	64	128	-
B	3	3	3	3	-
n	2	2	2	2	-
R	300	300	100	100	Ω
C_S	1.7	1	1	1.2	Pf
C_{L2}	7.2	5.8	5.8	6.2	pF
GBW	400	70	130	280	MHz
SR	500	88	163	352	V/μs
σ_{jit}	9	9	9	9	Ps
A_{in} at peak SNDR	0.75	0.9	0.9	0.75	V
Peak SNDR	77.2	74.5	76.4	77.7	dB
SNDR (SIMULINK)	78	75	77.2	78.2	dB
POW_{total}	14	3.4	6.7	13.9	mW

Table 8.1. Comparisons of our design results with the measurement in [6]

From Table 8.1, when *K* = 0.5 and *K*=2, the *SNDR* are lower than the specification. In order to increase *SNDR*, we need to increase *K*. When *K*=5, the theoretic result of *SNDR* = 77.7dB approach the specification, and the behavior simulation result of *SNDR* = 78.2dB satisfy the specification. The POW_{total} = 13.9mW for *K*=5 is almost equal to POW_{total} for Ref[Gag03]. When *K*=5, although *OSR* needs to be larger than the one in Ref[Gag03], but the demands for GBW and SR are much lower, and reduce the complexity for OTA design.

Table 8.2 shows the corresponding noise and distortion powers for the four design cases shown in Table 8.1. In the design of [Gag 03], and in our designs for K=0.5, 2, 5, the dominating power is P_{dac} and $HD2_{DAC}$. Due to the DEM is not employed, so the above two nonlinearities power can't be reduced effectively. Although *SNDR* of our theoretic result can't be higher obviously in this case, but our proposed optimization result offers another way to obtain the suitable circuit specifications fast.

Nonlinearities Power	Ref [Gag06]	*K*=0.5	*K*=2	*K*=5	Unit
P_Q	- 109.8	- 84.9	- 89.8	- 105.8	dB
P_{AV}	-141.1	- 123.6	- 126.5	- 141.0	dB
$P_{\varepsilon 1}$	- 196.5	- 681.7	- 551.5	- 258.4	dB
$P_{\varepsilon 2}$	- 119.3	- 103.9	- 104.5	- 120.0	dB
P_{sw}	- 96.9	- 90.8	- 91.8	- 95.6	dB
P_{ref}	- 114.7	- 101.0	- 103.1	- 109.1	dB
P_{OTA}	- 117.0	- 110.9	- 111.9	- 115.7	dB
P_{dac}	-79.6	-74.9	-78	-81	dB
$HD3_{NFDCG}$	-108	-91.2	-96.6	-110.5	dB
$HD3_{settling}$	-130.6	-108.6	-17.6	-110.7	dB
$HD5_{settling}$	-145	-131	-126.6	-127.6	dB
$HD2_{DAC}$	-80.1	-77.7	-77.7	-80.1	dB
$HD3_{DAC}$	-91.7	-87.6	-87.7	-91.8	dB
$HD4_{DAC}$	-106	-100.2	-100.2	-106.1	dB

Table 8.2. The corresponding noise powers for the design parameters listed in Table 8.1

	Ref [Gag06]	*K*=0.5	*K*=2	*K*=5	Unit
POW_{analog}	8	1.4	2.7	5.9	mW
$POW_{digital}$	6	2	4	8	mW

Table 8.3 Listing the details of power consumption.

Table 8.3 lists the power consumption details. In POW_{analog}, $POW_{\Sigma\Delta\_OTA}$ consumes the most much power, hence we analysis the analog power consumption for OTAs. From（6.1）, we can see that the $POW_{\Sigma\Delta\_OTA}$ is proportional to the *GBW* and C_{L2}. The C_{L2} （4.19）is proportional to the sampling capacitance C_S. From Table 8.1, we can see that the *GBW* of [Gag 03] is larger than that of *K*=0.5, *K*=2 and *K*=5 and C_S of [Gag 03] is larger than those of the all theoretic results. Hence, the $POW_{\Sigma\Delta\_OTA}$ of [Gag 03] is the largest among the four cases. From（6.8）, we can see that the POW_{Clock} and POW_{Switch} are both proportional to the sampling frequency f_S, hence $POW_{digital}$ for *K=5* is the largest among the for cases since

which has the largest *OSR*.. If *SNDR* must to be increased, P_{dac} can be reduced effectively and HD_{DAC} can be eliminated by employing DEM techniques, but $POW_{digital}$ becomes larger.

9
Conclusions and Future Works

In order to increase the speed of circuit design for ΣΔ ADCs, this paper offers an efficient optimization method to obtain the most suitable circuit specifications. All the nonlinearity power also can be obtained after an complete optimization, and the dominating nonlinearity power can be reduced by adjusting the design specifications. Our proposed method has acceptable accuracy and nice speed, and the flexibility can be enhanced by building more nonlinearity models for different circuit structures.

Further, in order to reduce the time-cost for optimization, the algorithm efficiently search the entire design parameters space to find the parameter set which satisfies the specifications must to be established.

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