國立交通大學

電機與控制工程學系

碩士論文

以 TSMC CMOS-0.35μm 製程設計一電容式感測器電路

Design of A Capacitive Sensor Circuit Using TSMC CMOS-0.35μm Process

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摘要

在許多應用中, 電容式感應器爲有著高精確度與可實行的感應器中的一種。一般而言, 電容式感測器電路包含著一個電容電壓轉換器與類比數位轉換器。其中電容電壓轉換器被直接的與感應器相連接, 且用來放大感應器的感應訊號; 接著, 電容電壓轉換器的輸出訊號被一類比數位轉換器所量化以獲得數位化的資料, 以便於運用在複雜的數位訊號處理上。本論文設計了一個包含電容電壓轉換器與Σ-Δ調變器 (或稱Σ-Δ類比數位轉換器) 的電容式感應器電路; 該電路不止是保持著簡單性而且也符合12位元解析度要求。

一直以來電容電壓轉換器與積分三角調變器兩者皆需要一個含有輸出共模回授能力的全差動在放大器, 我們將共模回授差動對中的電晶體以體極驅動方式來設計該放大器。我們更進一步的設計將該共模回授的差動對操作在次臨界區。由此, 該差動放大器能有著較高的輸出訊號範圍。我們實行了將參數在三個標準差的變化量下的模擬且得到了在供應電壓 Vdd: 3.3 V 時共模電壓爲1.63∼1.67 V。在這樣的選擇與設計讓共模回授對於元件不匹配達到強健的設計, 使得輸出操作電壓維持在 Vdd/2: 1.65 V 附近。

在積分三角調變器中, 我們提出了一個新的架構去實現取樣與加法功能。我們稱之爲電容分享技術。這樣的技術使得已被發展完善的積分三角調變器能免於由取樣電容的不匹配或者輸入訊號的共模電壓漂移造成的影響而降低電路性能。

該電容式感應器在1 MHz 的時脈下被量測。感應器的容值變化可達60 fF 與1 KHz 的頻寬。在正弦波改變量爲42 fF 與頻率爲869 Hz 的變化下, 電容電壓轉換器達到了74 dB 的訊號雜訊失眞比; 在相同的測試條件下, 積分三角調變器獲得了 80.5 dB 的訊號雜訊失眞比。因此, 該感應器電路有著12位元的解析度。此電容感測器電路面積爲1.5 mm^2且在供應電壓爲3.3 V 時, 整個系統的消耗功率爲2.4 mW。

Design of A Capacitive Sensor Circuit Using TSMC CMOS-0.35μm Process

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Abstract

Capacitive sensor is one of highly accurate and feasible sensors in many applications. Capacitive sensor circuit, in general, consists a capacitance to voltage converter (CV-C) and an analog to digital converter (ADC). CV-C is connected directly with the sensor and served to amplify the sense signal of sensor; its output signal is then quantized by ADC to yield digital data so that sophisticated digital signal processing algorithms can be applied. This thesis designs a capacitive sensor circuit which consists a CV-C and a Σ-Δ Modulator(SDM, or called Σ-Δ ADC); the circuit not only keeps the simplicity but also meets the resolution of 12-bits.

Since both CV-C and SDM need a fully differential amplifier with output common-mode feedback (CMFB) capability, we use bulk-driven transistors in CMFB differential pairs to design the amplifier. We further design the CFMB differential pairs operate in the subthreshold region. Hence, the obtained differential amplifier can have a higher output signal swing. We perform simulations with the 3σ parameter variations and obtain the common-mode voltage of 1.63$\sim$1.67 V for supply voltage Vdd: 3.3 V. This choice and design make the CMFB robust to device mismatch such that the output operating voltages remains at about Vdd/2.

In the SDM, we propose a new configuration to realize the functions of both sampling and addition. We call it the capacitor-sharing technique. This technique makes the developed SDM immune to degrade the circuit performance from either sampling capacitance mismatch or the variation of common mode voltage of input signals.

The final capacitive sensor is measured using 1 MHz clock. It can measure the capacitance variation of sensor up to 60 fF and the bandwidth 1 KHz. Individually, the CV-C achieves 74 dB SNDR at 42 fF sine wave variation with frequency 869 Hz; at the same test condition, the

SDM obtains 80.5 dB SNDR. Hence, the total resolution of the sensor circuit is 12-bits. The power consumption of the whole system is 2.4 mW at a 3.3 V supply voltage and the chip area is 1.5 mm^2.

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新竹-交大, July 2008

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Chapter 1

Introduction

1.1 Motivation

Capacitive sensor circuit is discussed here due to capacitive sensor can be more unaffected than resistive one by temperature, humidity, or mechanical mis-alignment, and shielding against stray electric fields is simple compared to shielding an inductive sensor against magnetic disturbances. Also, the capacitive transducer accuracy is excellent as the plate patterns which determine accuracy can be reproduced photographically with micron precision. Capacitive sensors consume very little power; battery life for small portable products may be several years [1]. A capacitive sensing circuit usually consists of two part: CV-C (Capacitance to voltage converter): the read-out of sensor signal, and ADC: the signal converted from analog to digital. This simply frame shows in Fig. 1.1.

For CV-C, fundamentally, there are two ways to monitor the difference in capacitance. The first (voltage-mode) is just to monitor the voltage with a voltage buffer. The second (current-mode) is to monitor the charge or signal current, with an inverting amplifier architecture. The inverting amplifier, with its summing node at an essentially constant voltage, makes capacitive signal detection less sensitive to parasitic capacitance variations but requires considerably higher bandwidth amplifiers, depending on the gain desired, to accomplish this parasitic ca-

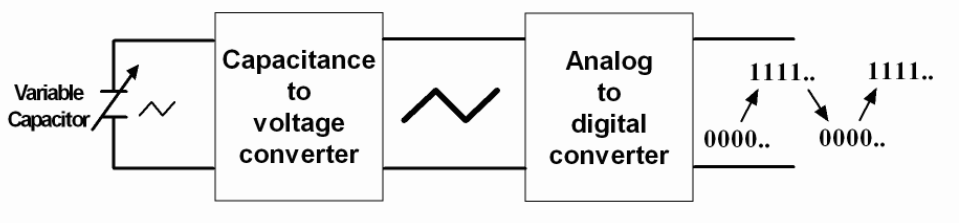


Figure 1.1: A simply capacitive sensing system.

pacitance immunity compared with using the voltage buffer method [2]. Current-mode is usually preferred. For current-mode, there are basically two methods to realize: sensing with AC modulation (continuous-time approach) and switched-capacitor (SC) using correlated double-sampling (discrete-time approach). SC interface circuitry of using correlated double-sampling is probably the most popular approach to reading out capacitive sensors [2] due to the continuous time implementation is hard and costing area for which needs generating a carrier signal with low phase noise and additional analog pre-filter.

For ADC, the most important specifications for single-sensor ADCs are accuracy and linearity. The conversion rate is usually less critical because most sensors (except for, e.g., particle detectors) monitor slowly changing environmental signals. Σ-Δ modulators (SDMs) with a single-bit quantizer are the most popular choice because of the following features [2]:

1. High accuracy can be achieved without reference-voltage scaling;
no accurate matching of resistors or capacitors is required.

2. No calibration is required.

3. They are faster than single-slope and dual-slope converters.

4. They are strictly monotonic.

5. They contain only a small number of elements (small area).

6. The specifications of the anti-aliasing filter are relaxed because of the oversampling.

Therefore, a capacitive sensor circuit which consists a switched-capacitor CV-C by using correlated double-sampling and a SDM is chosen here.

In now days, capacitive sensing system is more and more popular for many applications of life (e.g., gaming, position, detection, ..., and so on.). A high sensitivity sensing system is thus developed and used. For designing a high resolution sensing circuit system, a continuous-time common-mode feedback (CMFB) circuit is a better choice than switched-capacitor one for less noise sourse while a fine linearity SDM is also necessary.

In this thesis, we proposed a improved continuous-time CMFB structure by using bulk-driven technique, and a SDM by using capacitor-sharing technique. The proposed CMFB has a wider signal swing range and less power consumption than using two differential pairs of traditional CMFB; also, the proposed SDM has perfect anti-variation from common mode level of input signal and better anti-mismatch of the input capacitors than traditional one. While

achieving a capacitive sensor circuit of 12-bits resolution is our goal.

1.2 Organization

The organization of the thesis is as follows:

In Chapter 2, we describes the introduction of a capacitive sensor interface circuits and the principle of the charge transfer of capacitance-voltage converter (CV-C); finally, it presents that a improved output common-mode feedback circuit can be used in universal amplifier to gain a wider output swing and less power consumption than original structure.

Chapter 3 begins with the consideration of the quantization noise properties, the principle of the oversampling technique, and the introduction of Σ-Δ noise shaping. In the last section of this chapter, we propose that a less effect from input common-mode variation , a better performance for suppressing capacitor mismatch effect, and a half size of the input sampling capacitor than usual Σ-Δ configurations idealistically.

Chapter 4 describes a detail description of non-idealities affecting then considers avoidable or non-considerations methods for these effects to achieve a fine design.

Chapter 5 presents the components and layouts of this sensing system and its post-layout simulations by HSpice. It also discusses that the skills and considerations of layout can be discussed in detail for system realization. Finally, We show the totally layout view of this capacitive sensing system and the simulation results of the worst case.

Chapter 6 draws conclusions about this work and makes recommendations for future work.

Chapter 2

Design of A Capacitance-Voltage Converter

2.1 Introduction

This chapter presents a switched-capacitor interface circuitry of capacitance-voltage converter (CV-C) of current mode. This CV-C consists an operational transconductor amplifier (OTA) with a CMFB structure of bulk-driven. The bulk-driven CMFB has the wider input range, better linearity and less power consumption than gate-driven. The considerations for practical design, simulation, and layout of the bulk-driven CMFB will detailed describe later. The totally simulations and layout of the CV-C will present in chapter 5.

This chapter is organized as follows. The front-end circuits of the sensing system is presented in section 2.2. Section 2.3 shows CMFB structures and consists of both the comparison between the gate- and bulk-driven, and a improved CMFB for universal OTA in section 2.3.1.

2.2 Front-End Circuits of The Sensing System

2.2.1 Capacitance-Voltage Converter

In capacitive-sensing system, a CV-C (capacitance-voltage converter) is needed for transferring the capacitor charge of the difference in voltage difference whose simple function block is shown in Fig. 2.1. The CV-C structure of current mode is used here.

Generally, it has several kinds of different number of inherent capacitor in external capacitive sensor (the variable capacitor is not only appearing by single but also appearing by symmetry in natural world; e.g., a single-, one pair-, and two-pair variable capacitors..., and go on). We discuss here with three popular kinds of different number of capacitor which can be com-

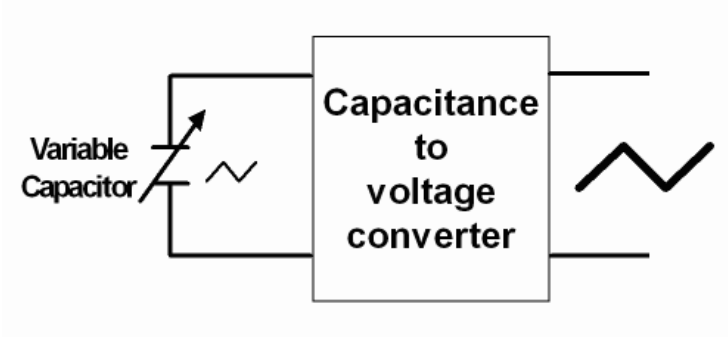
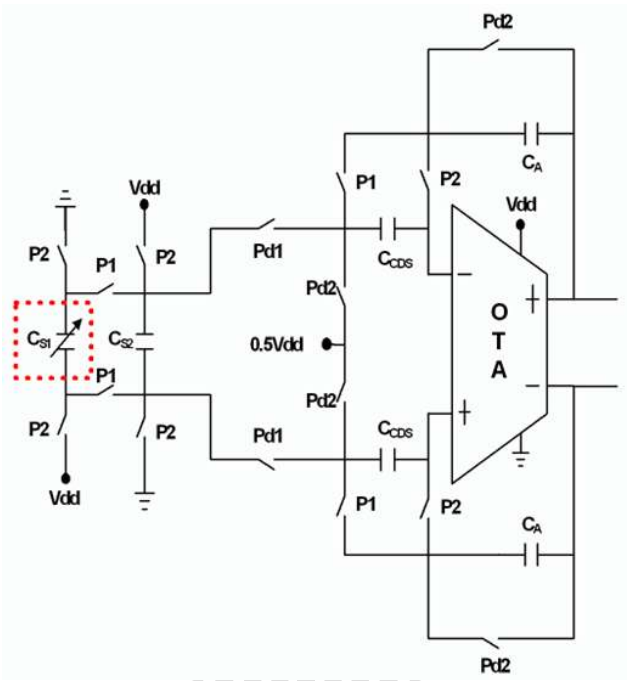


Figure 2.1: The simple CVC function block.

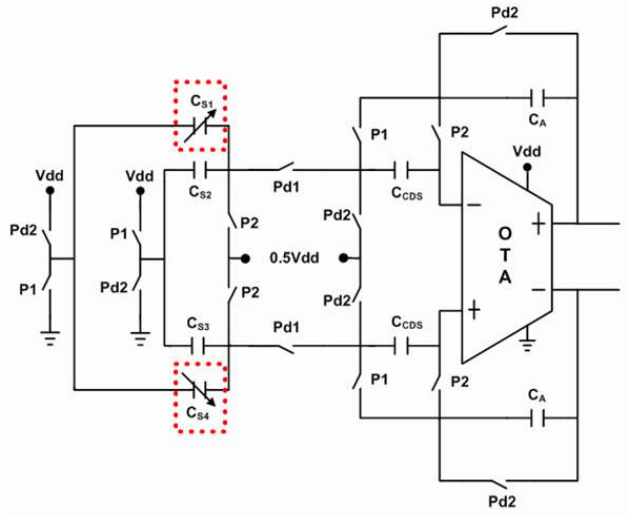
bined with charge transfer circuit are shown in Fig. 2.2. Where the C_{s1}=C_{normal}+$\Delta C_s/2$ and C_{s2}=C_{normal} of the Fig. 2.2(a), the C_{s1}=C_{normal}+$\Delta C_s/2$, C_{s2}=C_{s3}=C_{normal}, and C_{s4}=C_{normal}-$\Delta C_s/2$ of the Fig. 2.2(b), and the C_{s1}=C_{s3}=C_{normal}+$\Delta C_s/2$ and C_{s2}=C_{s4}=C_{normal}-$\Delta C_s/2$ of the Fig. 2.3(a). These structures can be used to detect the difference of the capacitance by clock switching. The detail equations of the switch operating will be discussed later for a representative structure.

In this thesis, we use a two-pair variable capacitors to present and achieve a CV-C. In this work, the two-pair variable capacitors are performing a sensor of acceleration sensing, which are built by using TSMC CMOS-0.35μm process (also called CMOS-MEMS). At the same time, some papers present that they also use variable capacitor sensor which is almost manufactured in special process (e.g., SOI process) due to this kind of variable capacitors of sensor has more large variable capacitance by using a big area, and better noise isolated between variable capacitor architecture and circuits. However, using this process usually follows high cost and no popularity. The CMOS process is thus considered and proposed for lower costs and smaller die area, and connected directly between sensor and circuits of the signal process on chip. The CV-C structure and its differential mode equivalent half-circuit of the CV-C show in Fig. 2.3(a) and Fig. 2.3(b), respectively. The CV-C has variable capacitance of four (C_{s1-4}) which exist in MEMS sensor itself where the schematic of the sensor and its equivalent model show in Fig. 2.3(c).

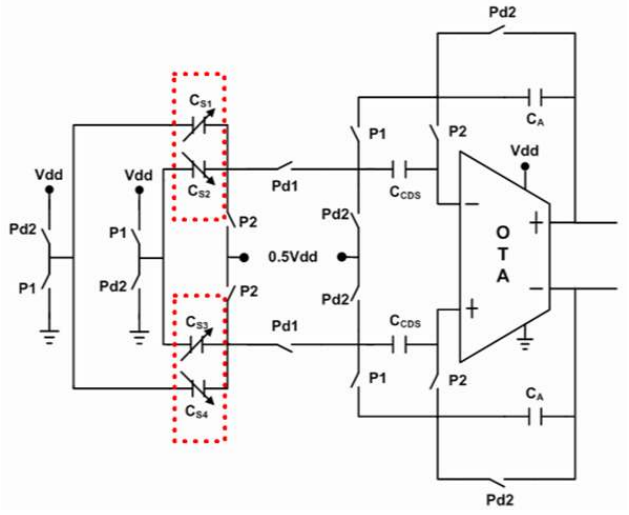
In Fig. 2.3, a finite gain (A) of the OTA and an input refer offset voltage (V_{OS}) of the OTA due to the OTA's components is easily changed by the process variation is assumed. At the cycle of the clock phase (e.g. the sampled and held phase operated), the charge of all capacitors and node voltage evidenced in Table 2.1. Where C_{s1}=C_{s3}=C_{normal}+$\Delta C_s/2$ and C_{s2}=C_{s4}=C_{normal}-



(a)

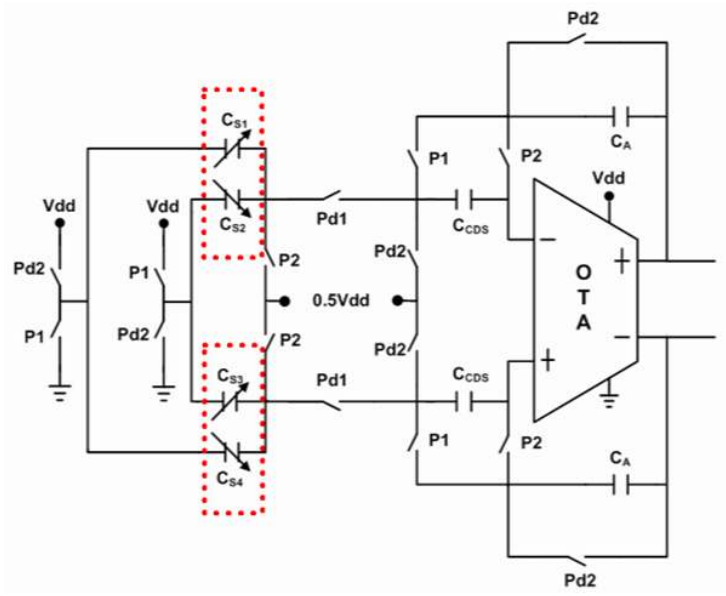


(b)

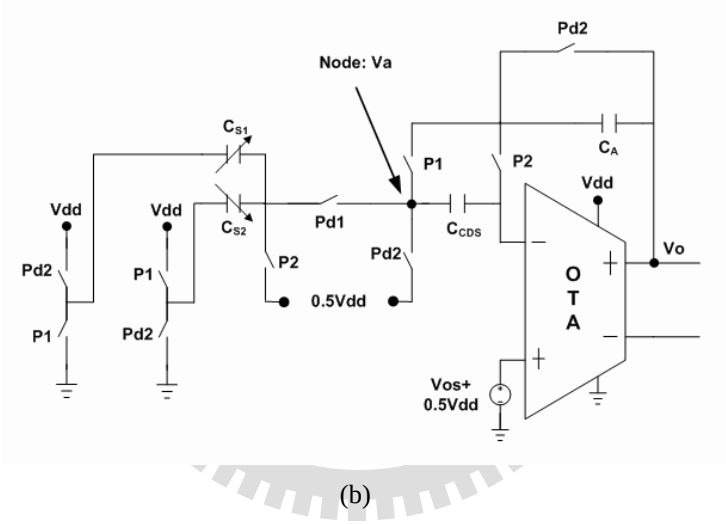


(c)

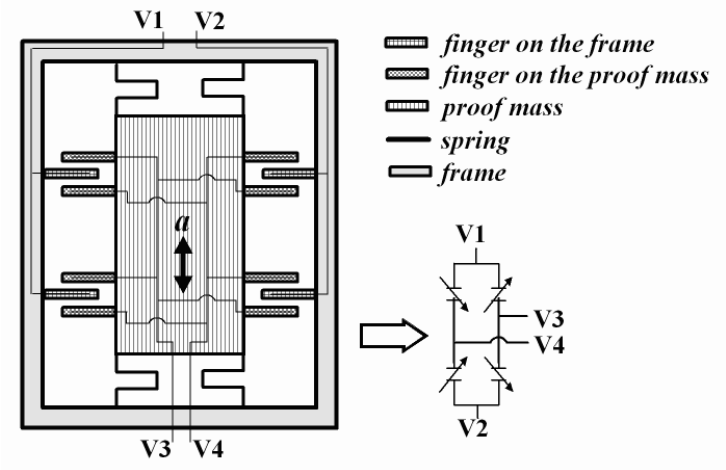
Figure 2.2: Structures of the three kinds of CV-C: (a) a single variable capacitor, (b) one-pair variable capacitors, and (c) two-pair variable capacitors.



(a)



(b)



(c)

Figure 2.3: (a) The structure of CV-C, (b) its half circuit, and (c) a simple graph of MEMS sensor.

Table 2.1: Charge distribution correspond with clock phase of the CV-C.

Capacitor Charges and Node Vlotage	At P1, Pd1: "H"; P2, Pd2: "L"	At P1, Pd1: "L"; P2, Pd2: "H"
$Q_{C_{S1}}$	$-C_{S1}V_a(n-1/2)$	$C_{S1}0.5V_{dd}(n)$
$Q_{C_{S2}}$	$C_{S2}(V_{dd}(n-1/2)-V_a(n-1/2))$	$-C_{S2}0.5V_{dd}(n)$
Q_{C_A}	$C_A(V_o(n)-V_a(n-1/2))$	0
$Q_{C_{CDS}}$	$C_{CDS}(V_{os}(n-1/2)+0.5V_{dd}(n-1/2)-$ $V_o(n-1/2)/A-V_a(n-1/2))$	$C_{CDS}V_{os}(n)$
Q_{C_P}	$-C_PV_a(n-1/2)$	$-C_P0.5V_{dd}(n)$
$V_a(n)$	$-V_{os}(n-1/2)+0.5V_{dd}(n+1/2)-$ $-V_o(n-1/2)/A-V_{os}(n)$ $\simeq 0.5V_{dd}(n+1/2)-V_o(n-1/2)/A$	$0.5V_{dd}(n)$

Note: The $V_a(n-1/2)$ is similarly equal to $-V_o(n-1/2)/A$ due to the charge of the C_{CDS} is no leakage, while the $V_{os}(n)$=$V_{os}(n-1/2)$ can be assumed. The C_P is a parasitical capacitance at Node V_a.

$\Delta C_s/2$ can be ideally assumed. Thus, according to Table 2.1, the relational equation can be combined and written as below

$$-C_{S1}V_a(n-1/2)+C_{S2}(V_{dd}(n-1/2)-V_a(n-1/2))+C_A(V_o(n)-V_a(n-1/2))+$$
$$C_{CDS}(V_{os}(n-1/2)+0.5V_{dd}(n-1/2)-V_o(n-1/2)/A-V_a(n-1/2))-C_PV_a(n-1/2)$$
$$=C_{S1}0.5V_{dd}(n)-C_{S2}0.5V_{dd}(n)+C_{CDS}V_{os}(n)-C_P0.5V_{dd}(n)$$

where the $V_o(n-1/2)$ consists of a signal component $V_o^{'}(n-1/2)$ and a DC bias $0.5V_{dd}(n-1/2)$, hence, above equation can be simplified and combined equal to

$$V_o^{'}(n-1/2)=(1/((AC_A+C_{S1}+C_{S2}+C_A+C_P)/A))[(C_{S1}-C_{S2})0.5(V_{dd}(n)+$$
$$V_{dd}(n-1/2))+C_P0.5(V_{dd}(n-1/2)-V_{dd}(n))]$$

from this equation, it can be knew that the CV-C output is not only changed by difference of MEMS capacitance in vibration but also varied by power supply and a finite OTA gain. There is simply equation with C_{S1}-C_{S2}=C_S+$\Delta C_S/2$-C_S-$\Delta C_S/2$=ΔC_S, $V_{dd}(n-1/2)$-$V_{dd}(n)$=ΔV_{dd}, C_{S1}+C_{S2}+C_A+C_P=C_T and non-consideration for time-sequence be assumed. It shows as

$$V_o^{'}=\frac{\Delta C_S}{(C_A+C_T/A)}(V_{dd}-0.5\Delta V_{dd})+\frac{C_P}{(C_A+C_T/A)}0.5\Delta V_{dd} \quad (2.1)$$

In a vibrating motion, it is our goal to get the ΔC_S. The variation of the supply voltage ΔV_{dd} can be avoided or reduced from layout placement by using independent supply voltage pads,

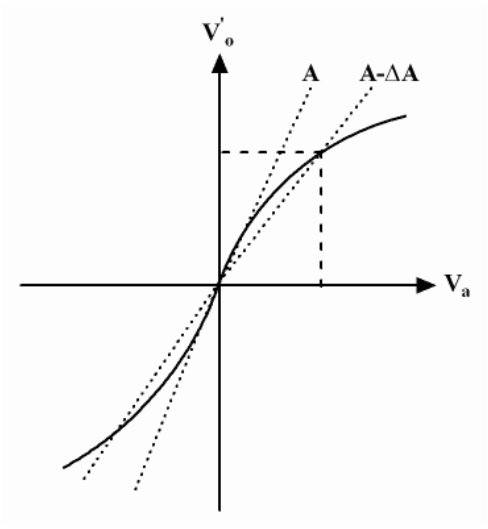


Figure 2.4: OTA gain variation and nonlinearity: the output $V_o^{'}$ versus the input V_a.

while this effect can be ignored here. The simply equation as

$$\begin{aligned} V_o^{'} =& \frac{\Delta C_S}{(C_A + C_T/A)} V_{dd} = \frac{\Delta C_S}{C_A} \frac{1}{1 + C_T/(AC_A)} V_{dd} \\ =& \frac{\Delta C_S}{C_A} \frac{1}{1 + e_{rr}} V_{dd} \simeq \frac{\Delta C_S}{C_A} (1 - e_{rr}) V_{dd} \end{aligned} \tag{2.2}$$

For achieving a high resolution or SNDR that the linearity of the CV-C is more important to regard than accuracy due to the OTA gain is not always a constant while how much gain and the amount of the gain varied are necessary for a more 10-bit resolution to obtain. In (2.2), the OTA gain A can be replaced by $(A - \Delta A)$, where ΔA is a function of $V_o^{'}$ like as Fig. 2.4. It has

$$e_{rr} = \frac{1}{A - \Delta A} \frac{C_T}{C_A} \simeq \left(\frac{1}{A} + \frac{\Delta A}{A^2} \right) \frac{C_T}{C_A} \tag{2.3}$$

$$V_o^{'} = \frac{\Delta C_S}{C_A} (1 - e_{rr}) V_{dd} \simeq \frac{\Delta C_S}{C_A} \left[1 - \left(\frac{1}{A} + \frac{\Delta A}{A^2} \right) \frac{C_T}{C_A} \right] V_{dd} \tag{2.4}$$

From above equation, neglecting linear gain error, to achieve N-bit resolution want

$$\frac{\Delta A}{A^2} \frac{C_T}{C_A} < \frac{1}{2(N+1)} \quad \Rightarrow \quad \frac{\Delta A}{A^2} < \frac{1}{2(N+1)} \frac{C_A}{C_T} \tag{2.5}$$

where the size of these capacitors can be estimated and computed for considerations of the KT/C noise (that will be described in the noise consideration of chapter 4) margin of 3 to 4 times and the CV-C output swing. The (2.5) will be a criterion of gain requirement for our OTA design. For non-linearity considerations, a different point with gain variation is the bandwidth

of the OTA that affects the accuracy of the final value for transient response. This consideration will be discussed on chapter 4.

Assuming the gain A is infinite for ideal analysis, the I/O relational equation of the fully differential CV-C is given by

$$\Delta V_o^{'} = \frac{2\Delta C_S}{C_A} V_{dd} \tag{2.6}$$

where the $\Delta V_o^{'}$ means that the difference voltage of the CV-C differential output. Comparison with this result and the (6) of the [3], the CMOS-MEMS has a amplitude of 2 times than SOI if the amount of different of each capacitance is the same in vibration detection of the same conditions due to the CMOS-MEMS which is not a signal layer process for comparison between the equation of the CV-C here and the (7) of [3] from mathematics. Another advantage for CMOS-MEMS has finer matching than SOI-MEMS, the reason for such result is that the CMOS-MEMS can be realized a symmetric differential capacitance of two-pair to reduce the fabricative mismatch.

Another important point for back to the OTA design is the decision of output common mode level which is almost set by a common-mode feedback structure. In following sections represent that how to find a suitable structure for our work and using an improved structure.

2.3 Proposed An Improved CMFB Used In Universal OTA

For considerations of swing and performance, a fully differential topology is more popular, therefore, the CM level of the fully differential topology I/O ports is mostly defined with a half supply voltage due to achieved maximum swing. Also, the input signal CM level of next stage is coming from the previous stage, an unbalance common voltage always leads the performance of the next stage out of control or degradation. Hence, achieving a balance and correctness CM level is set by a CMFB (common-mode feedback) scheme. About CMFB schemes are discussed on several textbooks, which have classified with two kinds from whose operational mode as CT (continuous-time) and SC (switched-capacitor). The SC-CMFB scheme always exists some issues as clock feed-through and charge injection from switches, more poor PSRR, and increasing capacitive loading at the output of the fully differential amplifier when it is compared to CT-CMFB [4]. Hence, the SC-CMFB scheme will not be used and discussed here. More detail about CT-CMFB will be presented in following subsections.

2.3.1 Comparisons

Up to now, many kinds of the CT-CMFB were presented in many bibliographies, they are usually evolved from four popular frames [5] of CT-CMFB structure which are shown in Fig. 2.5. Some disadvantages are like that the sensing resistors load at the OTA output, and the resistor and the input capacitor of the CM-sense amplifier introduce a pole in the CMFB loop (Fig. 2.6(a)), in Fig. 2.6(b), the OTA output swing is limited since each source-follower transistor that connects to an OTA output must remain in the saturation region over the entire output voltage swing, and the non-constant overdrive voltage of the source-follower transistors leads non-linearity issue; another scheme in Fig. 2.5(c) is limited by that the CMFB loop will not function properly whenever the output voltage swing is large enough to turn off either transistor 5 or 6 while the transconductance of 5 and 6 in the triode region is smaller than it is in the saturation region. Then, this structure thus has a lower CMFB loop-gain. The fourth scheme in Fig. 2.6(d) has also limitation on the output voltage swing of the opamp but it does not need sensing resistors and using some transistors operate in the triode region.

On the above, the structure of using resistive divider is not considered in our work due to the resistor be often chosen large to increase the area while to increase the cost. Then, the CMFB using two differential pairs has faster speed and better accuracy than using transistors in the triode region one[6]. Therefore, the structure of using two differential pairs is chosen and used in our work. However, the input swing region and the power consumption of the using two differential pairs structure are the key issues. An improved CMFB structure will be presented later.

A bulk-driven transistor, the signal irrigates from bulk region of transistor, which is used and avoided the inherently limitative swing range of input voltage. Others benefits are more flat transconductor g_m that leads a better linearity operating result, and a wide ICMR (input-common-mode-range) by using bulk-driven technique. Also for obtaining a high gain of the CMFB loop and low power consumption, the transistors of input differential pair are used in weak-inversion region (also called subthreshold region; the drain current of a mos is based on the channel diffusion current) which perform a higher bulk-transconductor g_{mb} (or said high gain) than the transistors are operated in the saturation region. For above benefits, which can be verified in simulation results from simple circuits (the circuits are also shown in Fig. 2.6)

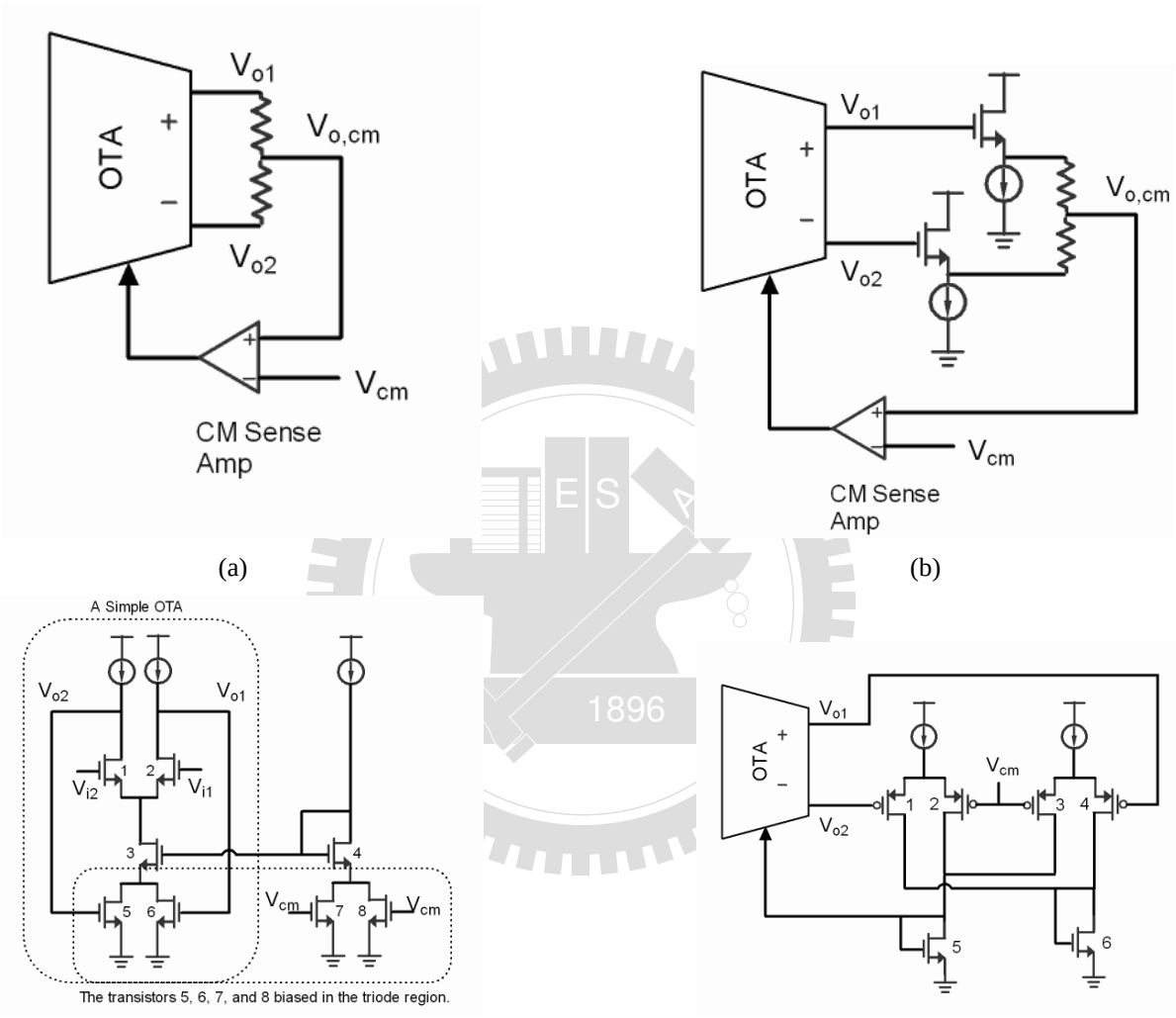


Figure 2.5: (a) CMFB using resistive divider and amplifier, (b) the scheme of (a) with source followers as buffers between the OTA outputs and resistors, (c) using transistors in the triode region, and (d) using two differential pairs.

which are shown in Fig. 2.6. These circuits were simulated in HSpice using BSIM3v3 model of the standard 0.35-μ m n-well CMOS process from TSMC while they compared in the same conditions (supply voltage, V_{ov} (over-drive voltage), tail-current, temperature, and so on.) for each other.

From the simulation results, a CMFB using two differential pairs by bulk-driven is proposed while the differential pairs operated in weak-inversion region, the structure is shown in Fig. 2.7(a), where the OTA can be a universal structure and the node V_a is a control voltage which connected to a voltage-controlled-current source of the OTA. The node V_a maintains that the OTA output voltage keeps in a set common level, while the loop is a negative feedback. At the same time, the CMFB structure can be analogized a opamp, we thus care whose DC gain and bandwidth from view points of designing a opamp. A scheme consists of a pmos input differential pair folded-cascode OTA of bulk-driven and CMFB shown in Fig. 2.7(b) which is used in our work. In [7] which indicates the voltage gain of the operation of circuits in the weak-inversion region approaches a constant value; this result will be appeared more clear due to the V_{ov} is more less variate than non-using bulk-driven technology. Therefore, we can say that the large-signal gain approximates the small-signal gain. At first for the small-signal analysis of the CMFB, we have to get DC operated points, disconnect the CMFB input from the OTA output, and add a large inductance between the two terminals, which inductance keeps the OTA output DC level maintain the set level before the analysis of the CMFB gain. By using typical circuit analysis techniques, it can be found that the small-signal parameters (e.g. gate-transconductor g_m and bulk-transconductor g_{mb}) and the loop gain (e.g. differential-input to single-output (at V_{o+})) of the proposed CMFB shown in Fig. 2.7(b). In saturation and weak-inversion region, the approximate relation between drain current and gate-to-source voltage are given by [5, 8]

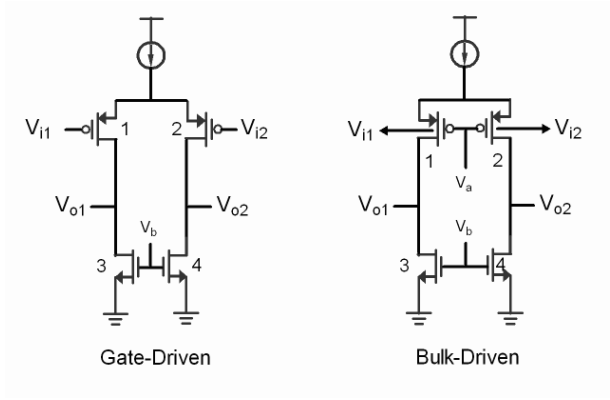
saturation region:

$$I_D = \frac{\mu C_{ox} W}{2L}[V_{GS} - V_T]^2 \tag{2.7}$$

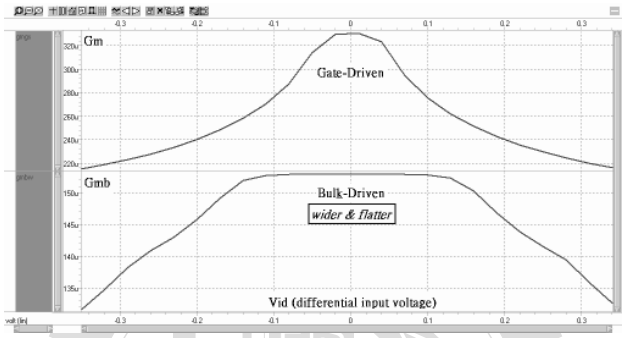
$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu C_{ox} W}{L}(V_{GS} - V_T) \tag{2.8}$$

weak-inversion region:

$$I_D = \frac{I_S W}{L} exp\left[\frac{q(V_{GS} - V_T)}{nkT}\right]\left[1 - exp\left(-\frac{qV_{DS}}{kT}\right)\right]$$



(a)



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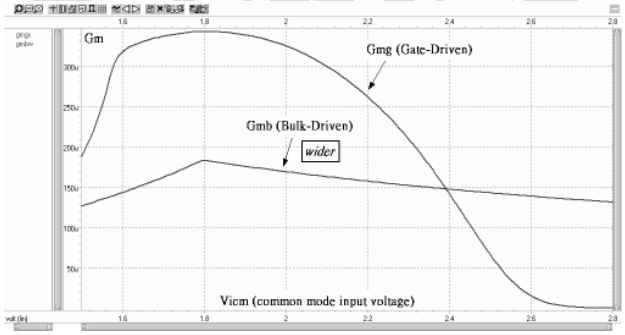

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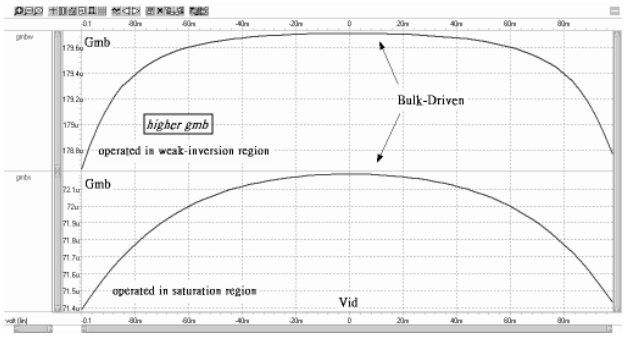
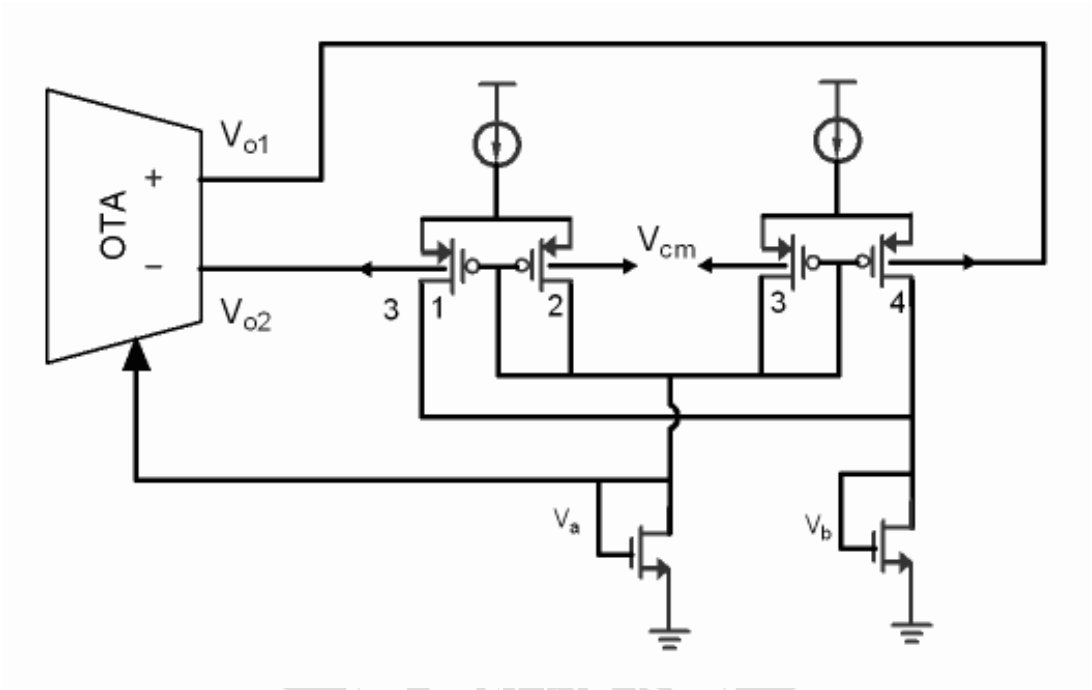
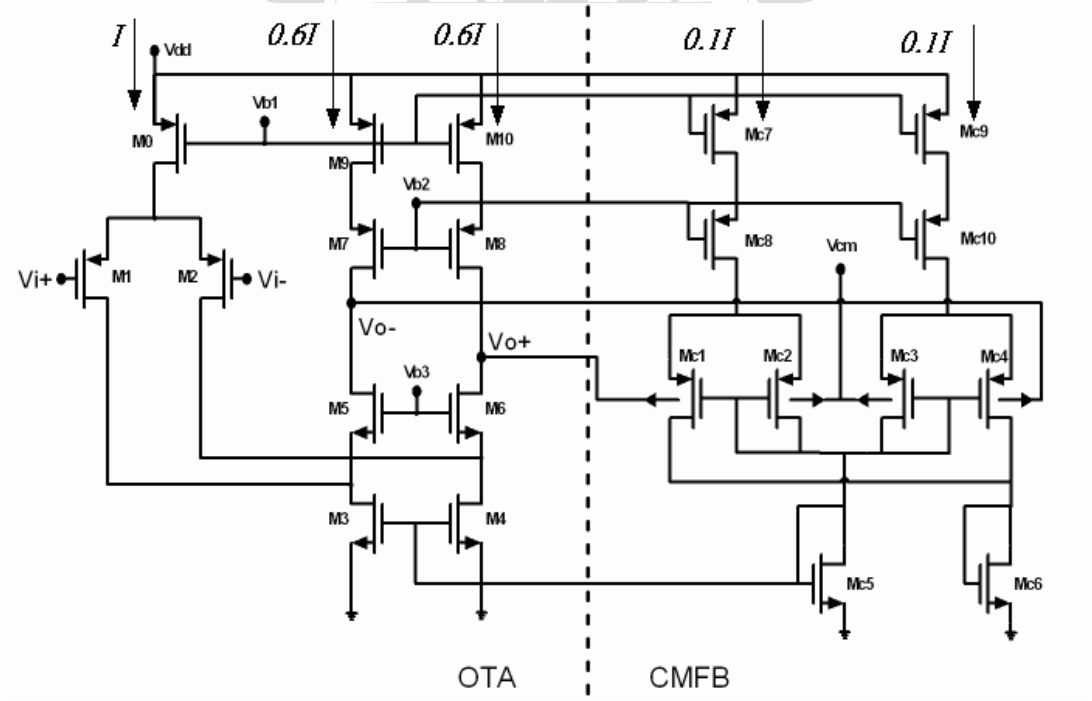


(d)

Figure 2.6: Comparison between gate-driven and bulk-driven: (a) two kinds simply structure of different input terminal, (b) whose transconductance versus input differential swing range, (c) also versus common mode input voltage, and (d) comparison of transconductance between operated in saturation region and weak-inversion region for using bulk-driven.



(a)



(b)

Figure 2.7: (a) An improved CMFB can be used in universal OTA and (b) a full scheme be used in our work.

the linearity is quite poor for V_{DS} small than $3kT/q$; hence, it usually chooses $V_{DS} \geq 3kT/q$

$$I_D \simeq \frac{I_S W}{L} exp\left[\frac{q(V_{GS}-V_T)}{nkT}\right] \tag{2.9}$$

$$g_{mb} = -\frac{\partial I_D}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2|\phi_F| + |V_{SB}|}} g_m \tag{2.10}$$

where I_S is the characteristic current, T the absolute temperature, n the inclination of the curve in weak inversion, k Boltzmann constant, q the charge of the electron or hole, γ the body effect coefficient and ϕ_F the Fermi potential. Those parameters will be used in the CMFB gain expression. The function of the CMFB gain expression which is gotten by by using the skill of open-circuit time constants method [9] is as following

$$H_{CMFB}(s) = A_{CMFB}\left(\frac{p_1}{s+p_1}\right)\left(\frac{p_2}{s+p_2}\right)\left(\frac{p_3}{s+p_3}\right)\left(\frac{s+z_1}{z_1}\right) \tag{2.11}$$

DC gain:

$$A_{CMFB} = \left(\frac{1/g_{m,c5}}{1/g_{mb,c1}+1/g_{mb,c2}} + \frac{1/g_{m,c5}}{1/g_{mb,c3}+1/g_{mb,c4}}\right) \left(1 + \frac{g_{mb,c1} - g_{mb,c2} + g_{mb,c4} - g_{mb,c3}}{g_{m,c5}}\right)(-g_{m,4}R_{out}) \tag{2.12}$$

Assuming that $g_{mb,c1}$=$g_{mb,c2}$=$g_{mb,c3}$=$g_{mb,c4}$ if the Mc1-Mc4 are matching each and the input level is the same as V_{cm}, thus, the formular can be approximated as

$$\begin{aligned} A_{CMFB} &= -g_{mb,c1}\frac{g_{m,4}}{g_{m,c5}}R_{out} \text{ ; where the } g_{m,4}=M \cdot g_{m,c5} \\ &= -M \cdot g_{mb,c1} R_{out} \end{aligned} \tag{2.13}$$

Dominant pole: at the OTA output node

$$p_1 = \frac{1}{R_{out}C_{out}} \tag{2.14}$$

$$C_{out} = C_L + C_{gd,M6} + C_{db,M6} + C_{gd,M8} + C_{db,M8} + C_{gb,Mc1} + C_{sb,Mc1} + C_{db,Mc1} \tag{2.15}$$

Non-dominant pole 1: at the gate of M4

$$p_2 = \frac{g_{m,c5}}{C_A} \tag{2.16}$$

$$C_A = 2C_{gs,M4} + 2C_{gd,M4}(1 + \frac{g_{m,M4}}{g_{m,M6}}) + 2C_{gb,M4} + C_{gs,Mc5} + C_{gb,Mc5} + 4C_{gs,Mc1} + 2C_{gd,c1}(1 + \frac{g_{m,Mc1}}{g_{m,Mc6}}) + 4C_{gb,Mc1}$$

Non-dominant pole 2: at the source of M6

$$p_3 = \frac{g_{m,6}}{C_B} \tag{2.17}$$

$$C_B = C_{gd,M2} + C_{db,M2} + C_{gd,M4} + C_{db,M4} + C_{gs,M6} + C_{sb,M6} \tag{2.18}$$

Zero: at the drain of M4

$$z_1 = \frac{g_{m,M4}}{C_{gd,M4}} \in RHP \tag{2.19}$$

where C_L and R_{out} are the load capacitance and resistance at the output of the folded-cascode opamp. Notice from (2.14-2.19) that poles p_1, p_2, and p_3 are common to both the CMFB and the differential path of the amplifier itself. On the other hand, z_1 is a right half-plane zero and always of higher frequency than p_{1-3}. The CMFB is in contrast with folded-cascode opamp, which adds additional poles that degrade the CMFB loop bandwidth and phase margin. The CMFB GBW (gain-bandwidth) product has to far enough to obtain a less enough settling time; further, a fine CMFB design should suppress the ac CM output signal, hence, the CMFB GBW product makes the GBW product of the opamp differential mode gain about equal or over it. Although this goal is difficult to achieve in practice[5], the CMFB GBW product must as far as enough to let the common-mode voltage settle in a time interval. Therefore, poles (p_{1-3}) position of the CMFB will care for guaranteeing an enough GBW and the loop stability.

The differential mode open-loop gain of the opamp and the CMFB open-loop gain are obtained from circuit post-layout simulations along with their corresponding phase responses for a load capacitance of C_L=1.3pF, respectively. The performance parameters of the opamp and the proposed CMFB are listed in Table 2.2. Where the post-layout simulations of the CMRR and PSSRR performed by using Monte Carol analysis of 1000 times in HSpice. The parameters for simulator are supplied from the TSMC CMOS-0.35-μ m n-well CMOS process while the variation parameters for Monte Carol analysis are obtained from [10]. Another important issue about using bulk-driven technique is the leakage current from bulk terminal due to the

Table 2.2: Specifications of the opamp and the CMFB for of all corner at Vdd: 3.3 V, and dimension of mosfet and Vdd varied in 3σ of 10% at TT corner.

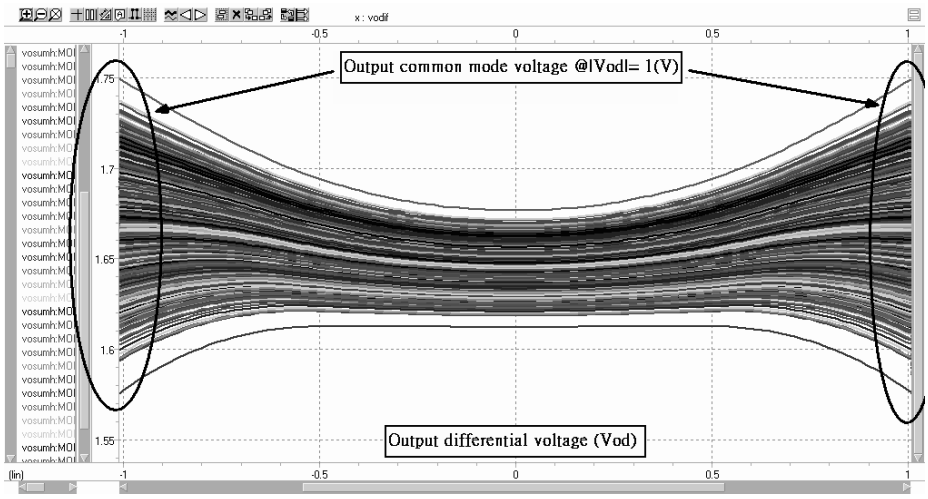
Parameter	OPAmp @C_L=$1.3pF$	Unit	Note
Differential DC gain (@$\|V_{od}\|$ = 0∼1 V)	60∼75	dB	-
$\frac{\Delta A}{A^2}$ (max.)	$< 162.76\mu$	-	the value is referring to (2.5) for 10-bit linearity
GBW product (min.)	40	MHz	-
Phase margin (min.)	73	deg	-
Voltage swing of the V_{od} (min.)	1	Volt	-
CMRR (min. @DC $V_{o+/-} = V_{cm}$)	80	dB	-
PSRR+/- (min. @DC $V_{o+/-} = V_{cm}$)	75	dB	-
Slew rate+/- (min.)	30	V/μs	-
Power consumption (max.)	850	μW	-

Parameter	CMFB @C_L=$1.3pF$	Unit	Note
Loop DC gain (@$\|V_{od}\|$ = 0∼1 V)	55∼70	dB	-
GBW product (min. @$\|V_{od}\|$ = 0∼1 V)	50	MHz	-
Phase margin (min.)	70	deg	-
$V_{o,cmR1}$ (max. range)	1.63∼1.67	Volt	-
$V_{o,cmR2}$ (max. range)	1.58∼1.75	Volt	-
Bulk leakage current (max.)	500	pA	-
Power consumption (max.)	96	μW	-

Note: The $V_{o,cmR1}$ and $V_{o,cmR2}$ are mean that the variation range of the output common mode voltage due to the process variation common output and differential output at (@V_{od}=0∼1 V), respectively. The max power consumption values of the OTA and CMFB are measured at Vdd: 3.6 V with TT corner At the CMFB part of the table, the data of the output common mode voltage and bulk leakage current are also plotted in Fig. 2.8.

leakage current is loss from the parasitical diode between source- and bulk-terminal. Hence, the transistor M_{c1} and M_{c4} is critical for if these diodes turned on that leads to the leakage current increasing. Thus, performing Monte Carol and the input signal of CMFB DC sweep analyses are necessary for ensuring the parasitical diodes between source- and bulk-terminal are not turned on; the simulation results are shown in Fig. 2.8.

According to the results of the above analyses, using bulk-driven technique has a wider input swing range, better linearity, and less power consumption than gate-driven one. However, it also has disadvantages as more easier mismatch on input differential pairs of CMFB, much bigger area cost, and leakage current from bulk-terminal. For noise consideration of the CMFB circuits, it is not important here due to the OTA output noise sources are dominated by the OTA itself which are consisting of the input-differential pair part and the cascode part of



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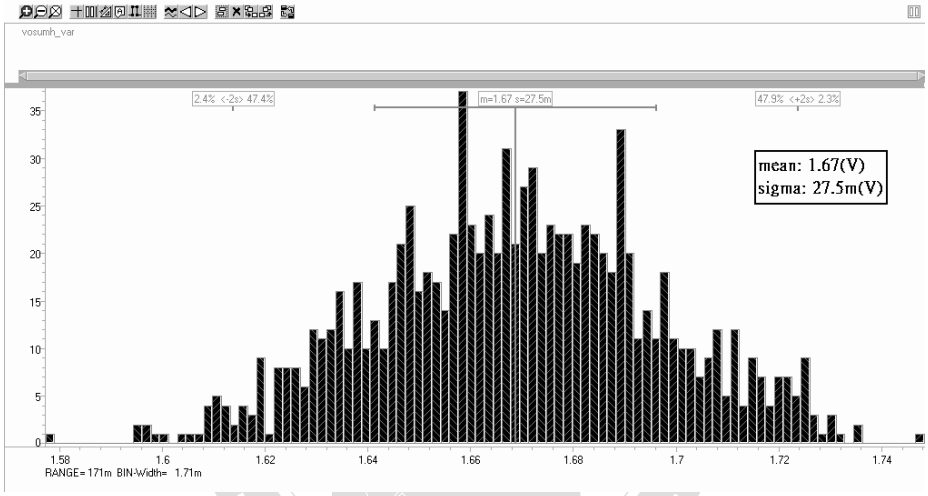

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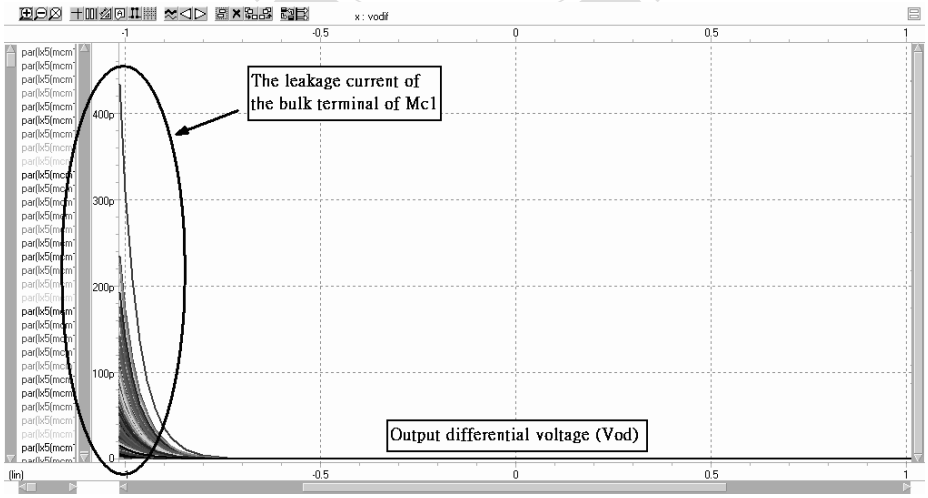
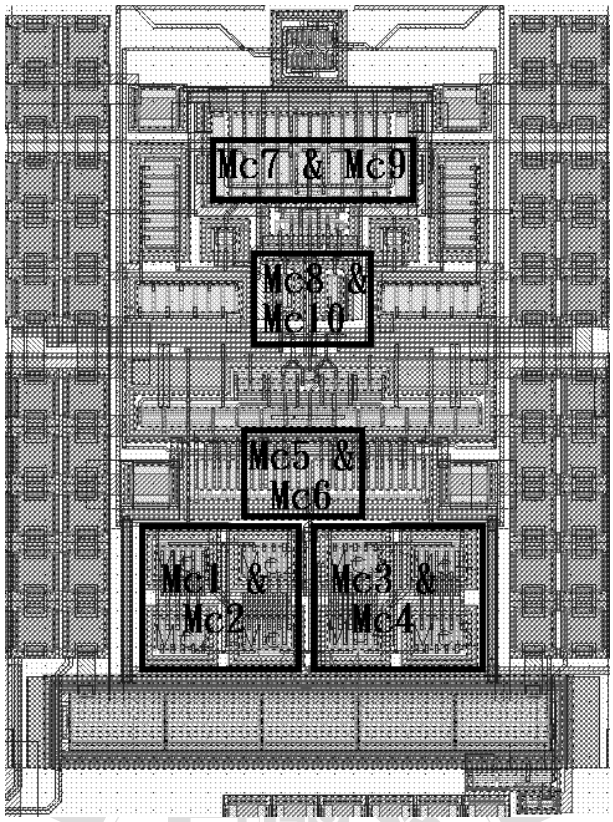


(c)

Figure 2.8: The variation range of output common mode voltage and its histogram (@Vod=1 V) versus the differential output of OTA are plotted in (a) and (b), respectively, and the leakage current from bulk terminal shows in (c); these figures are also generated by Monte Carol of 1000 times in HSpice for post-layout simulations.

the folded-cascode OTA. Consequently, these results show that the bulk-driven CMFB using two input differential pairs in weak-inversion region is achieved after it should ensure that the leakage current and common mode voltage can be tolerated in all of the mismatching analyses. Finally, the layout view of the improved CMFB shows in Fig. 2.9(a), and another one of the OTA shows in Fig. 2.9(b). The layout of the OTA with the CMFB is shown in Fig. 2.10.



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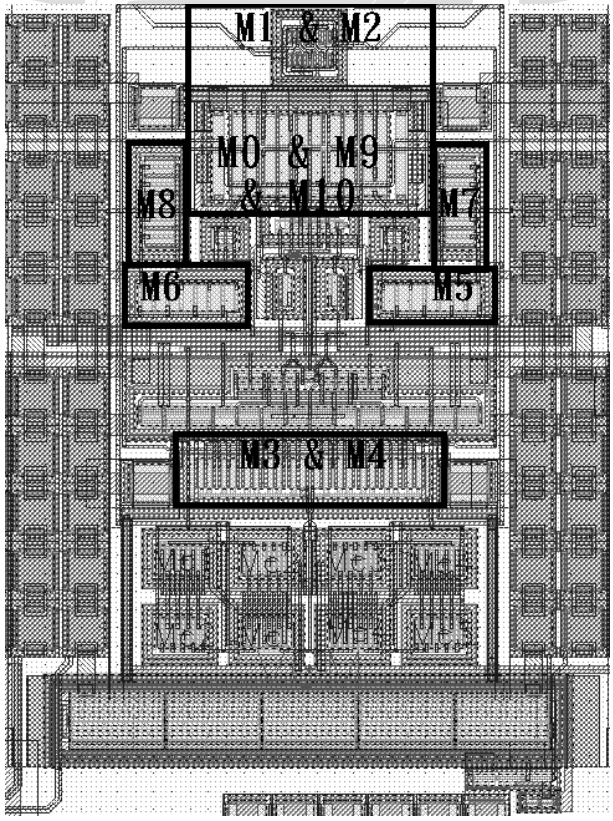


(b)

Figure 2.9: Layout view: (a) the CMFB components are shown in white line blocks, and (b) the OTA components are shown in white line blocks.

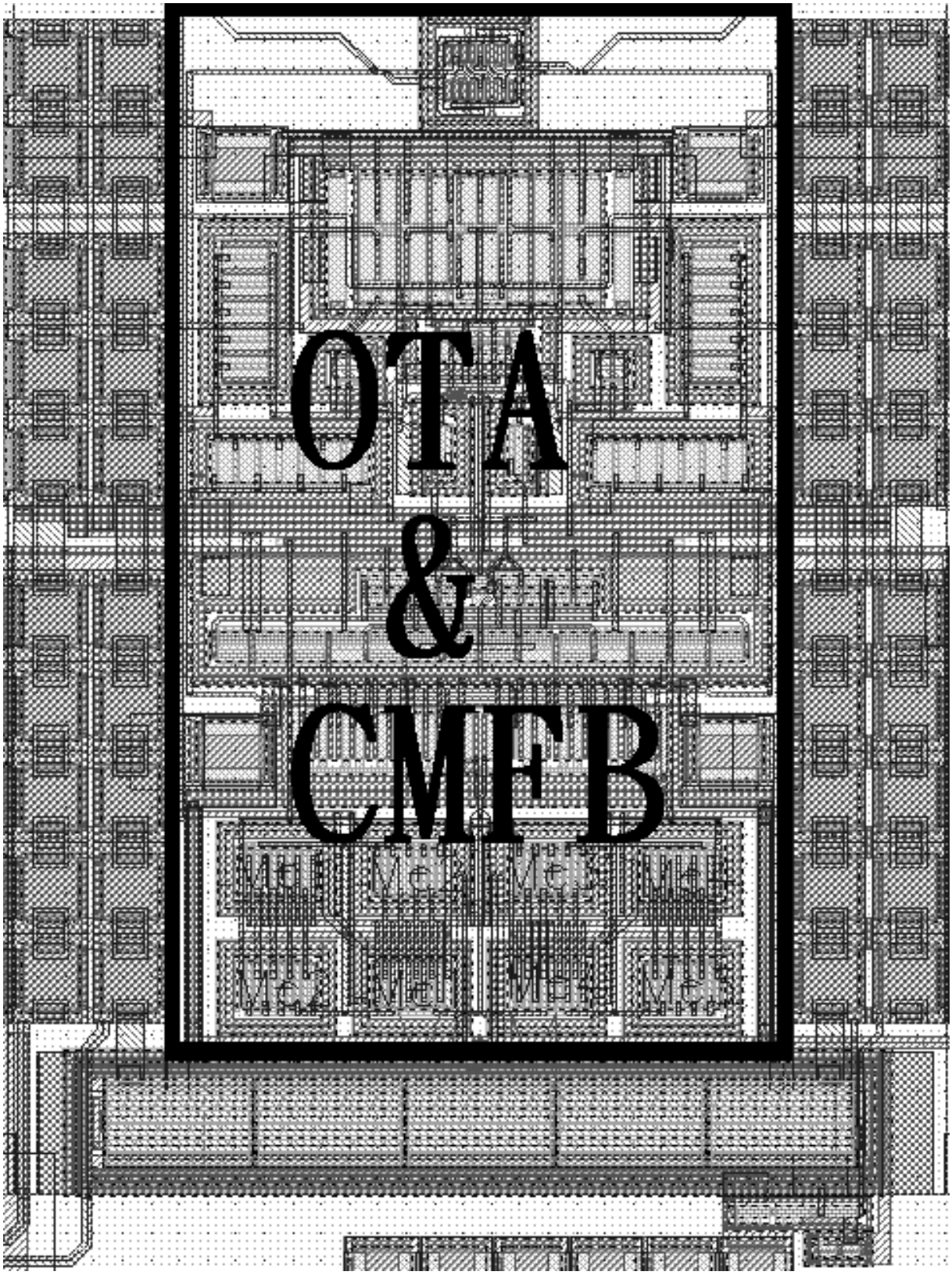


Figure 2.10: The layout view in the white line blocks is consisted of OTA and CMFB, and the else components also in this view are biasing circuits and bypass capacitors.

Chapter 3

Design of A Σ-Δ Modulator

3.1 Introduction

As mentioned in Chapter1, the switched capacitor Σ-Δ modulator (SDM) is essential components to quantify the capacitive sensing system. Therefore, in this chapter some fundamental in the design of SDM are reviewed first. Then, the concept of how a SDM behaviors and the basic linear models are discussed and correlated with performance issues. About the consideration of the SC circuit noise, bias circuit, and comparator circuit will be all conferred in the last chapter.

In this chapter, the design of a SDM is described which takes some advantages by the capacitor-sharing structure. Like as achievable lower input capacitor size and lower capacitor mismatch error, which be compared with the similar structure and specification.

The chapter is organized as follows. The SDM fundamentals are presented in section 3.2, which is consisted of several subsections as quantization noise in Section 3.2.1, oversampling technique in section 3.2.2, and the basic concepts of the noise shaped SDM in section 3.2.3.

About the circuit configurations of a tradition type and a new proposed type for first-order SDM is discussed in section 3.3, whose subsection is combined the comparisons of circuit level systems in section 3.3.1.

3.2 Σ-Δ Modulator Fundamentals

3.2.1 Quantization Noise

Generally speaking, the quantization error signal types can be separate from uniform and non-uniform. In this thesis case amd more popular A/D converter, the quantization error signal is uniform type. Fig. 3.1 shows a quantization noise behavior model, where both N-bit converter

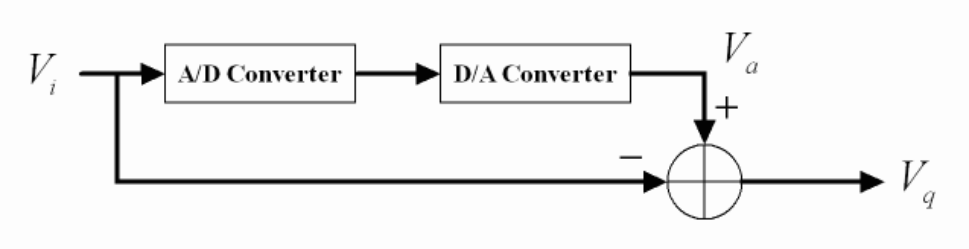


Figure 3.1: Quantization noise behavior model

are considered in ideal case. From this model, a equation is expressed as below(3.1). Where the quantized signal, input signal, and quantization error signal are represented as V_a, V_i, V_q, respectively.

$$V_a = V_i + V_q \tag{3.1}$$

Now we assume the input signal, V_i is a ramp. The results in the output from the DAC, V_a, which be appearing as a staircase signal in such an input signal, as shown in Fig. 3.2. The result of quantization error signal is difference between V_a and V_i which is represented as V_q, as also shown in Fig. 3.2. The range of quantization error signal is the boundary between $+V_{LSB}/2$ and $-V_{LSB}/2$ for all input signals (not just ramps). Clearly, the quantization error signal V_q has zero mean. For these to be true, we have to ensure that the quantizer no overloading occurs. The V_{LSB} is defined the voltage change when one LSB changes. Also, a namely, LSB units is definition of a new "unit". There represents in Mathematically is shown as

$$V_{LSB} \equiv \frac{V_{ref}}{2^N} \tag{3.2}$$

$$1LSB = \frac{1}{2^N} \tag{3.3}$$

where V_{ref} and N represent the reference signal and N-bit converter, respectively.However, the rms value of the quantization error, $V_{q(rms)}$, is given by

$$\begin{aligned} V_{q(rms)} &= \left[\frac{1}{T}\int_{-T/2}^{T/2} V_q^2 dt\right]^{1/2} = \left[\frac{1}{T}\int_{-T/2}^{T/2} V_{LSB}^2 (\frac{-t}{T})^2 dt\right]^{1/2} \\ &= \frac{V_{LSB}}{\sqrt{12}} \end{aligned} \tag{3.4}$$

Thus, we can see that the rms power of a quantization error signal is proportional to the V_{LSB}. Previously, we presented a uncomplicated notion to see some properties of the quantization error signal. Presently, we have to consider with the more general input signal case is used by a stochastic approach in typically. Hence, we assume a varying rapidly signal is used as

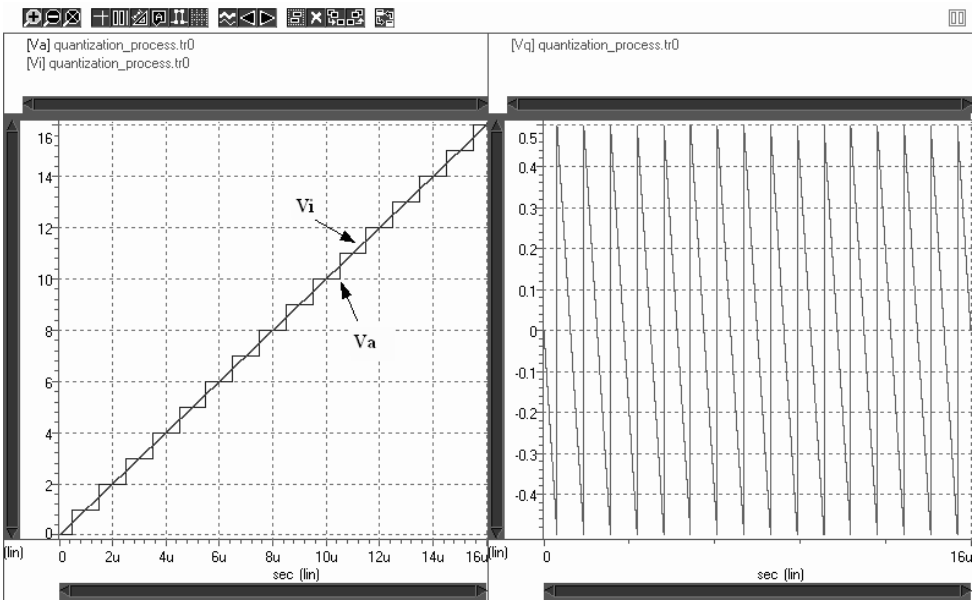


Figure 3.2: Quantization process.

input signal such that the quantization error signal, V_q, is a random variable distributed between $(-V_{LSB}/2, V_{LSB}/2)$ uniformly. The Fig. 3.3(a) shows the probability density function for such an error signal, $f_q(x)$, will be a constant value. In this approach, the average of the quantization error signal , $V_{q(avg)}$, and the rms of the quantization error signal, $V_{q(rms)}$, are found to be zero and $V_{LSB}/\sqrt{12}$ as follows, respectively.

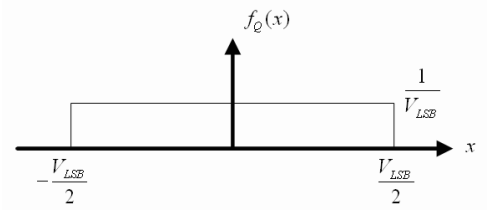
$$V_{q(avg)} = \int_{-\infty}^{\infty} x f_q(x) dx = \frac{1}{V_{LSB}} \left(\int_{-V_{LSB}/2}^{V_{LSB}/2} x dx \right) = 0 \tag{3.5}$$

$$\begin{aligned} V_{q(rms)} &= \left[\int_{-\infty}^{\infty} x^2 f_q(x) dx \right]^{1/2} = \left[\frac{1}{V_{LSB}} \left(\int_{-V_{LSB}/2}^{V_{LSB}/2} x^2 dx \right) \right]^{1/2} \\ &= \frac{V_{LSB}}{\sqrt{12}} \end{aligned} \tag{3.6}$$

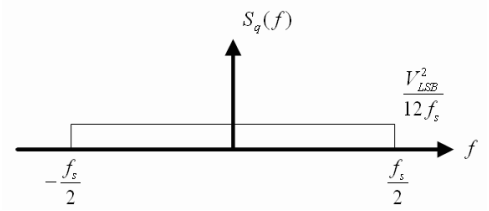
If we transfer the probability density function to the power spectral density (PSD) which is extended by sampling frequency, f_s, the sum of the PSD is always not changed where the high of the PSD is inversely proportional with f_s which is given by (3.7). The PSD for quantization noise is shown in Fig. 3.3(b).

$$V_{q(rms)}^2 = \frac{V_{LSB}^2}{12} = \int_{-f_s/2}^{f_s/2} S_q(f) df = \int_{-f_s/2}^{f_s/2} \frac{V_{LSB}^2}{12 f_s} df \tag{3.7}$$

From previous consideration, we assume V_i is a sawtooth(or equivalently, a random signal) of height V_{ref} distributed between 0 and V_{ref} and calculate only the AC r.m.s. value of V_i, the



(a) Probability density function for quantization noise, V_q



(b) Power spectral density for quantization noise, S_q

Figure 3.3: Probabilit density function and power spectral density for quantization noise.

SNR is given by

$$SNR = 20\log\left(\frac{V_{i(rms)}}{V_{q(rms)}}\right) = 20\log\left(\frac{V_{ref}/\sqrt{12}}{V_{LSB}/\sqrt{12}}\right) = 20\log(2^N) = 6.02N\ dB \tag{3.8}$$

Alternatively, a more common SNR formula is to assume V_i is a sinusoidal waveform between 0 and V_{ref}. Thus, the AC r.m.s. value of the sinusoidal wave is $V_{ref}/(2\sqrt{2})$, then, the SNR is given by

$$\begin{aligned} SNR &= 20\log\left(\frac{V_{i(rms)}}{V_{q(rms)}}\right) = 20\log\left(\frac{V_{ref}/(2\sqrt{2})}{V_{LSB}/\sqrt{12}}\right) = 20\log\left(\sqrt{\frac{3}{2}}2^N\right) \\ &= 6.02N + 1.76\ dB \end{aligned} \tag{3.9}$$

Note that (3.9) gives the best possible SNR for an N-bit A/D converter. Therefore, while we reduce the input signal levels, the idealized SNR will be decreased from the best possible value. However, it should be noted that these SNR values could be improved through the use of oversampling techniques if the input signal bandwidth is lower than the Nyquist-rate.

3.2.2 Oversampling Technique

In (3.7) it is discussed to the PSD height of quantization noise relation to sampling frequency, Hence, it can be known that obtaining much higher dynamic-range improvements in signal bandwidth as the sampling rate is increased; in other words, consider oversampling, subsequent discrete-time filter and downsampling also permit an increase step size V_{LSB} of the quantizer or, equivalently, a reduction in the number of bits required in the quantizer. Oversampling is mean that the signals of interest are band-limited to f_0 yet the sample rate is at f_s, where $f_s > 2f_0$ ($2f_0$ being the Nyquist rate or, equivalently, the minimum sampling rate for signals band-limited to f_0)[11]. We define the oversampling ratio, OSR, as

$$OSR \equiv \frac{f_s}{2f_0} \tag{3.10}$$

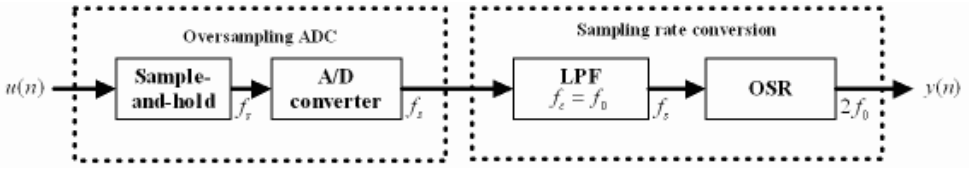


Figure 3.4: Oversampling ADC with sampling rate conversion.

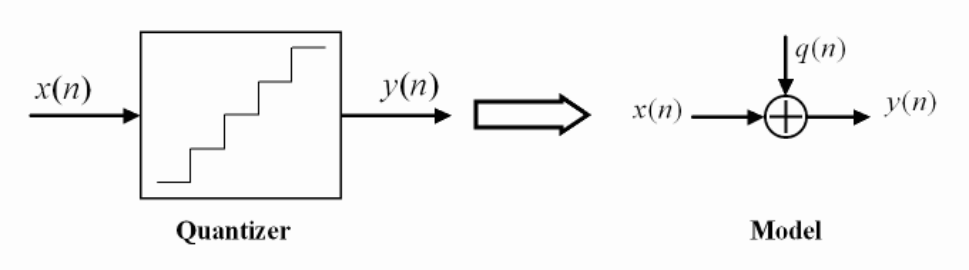
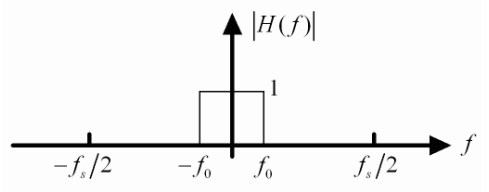


Figure 3.5: Quantizer and its linear additive model.

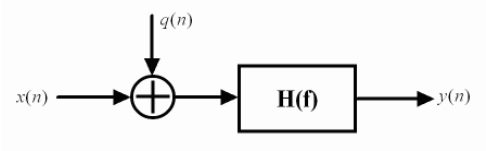
An oversampling system with a A/D converter, discrete-time lowpass filter and downsampling as shown in Fig. 3.4. A linear quantizer additive model can be created from concept of the quantization noise behavior model (Fig. 3.1) to analyze the effect of oversampling where $u(n)$ is already band-limited to f_0 at initially and the system shows in Fig. 3.5. The lowpass filter in Fig.3.6(a) can be implemented by a decimation filter ($H(f)$) with unity gain and cutoff frequency $f_c = f_o$ which shows in Fig.3.6(a). We can replace Fig. 3.4 by Fig.3.6(b). We know that the quantization noise is independent of the input signal in Fig. 3.6(b), thus, calculate the powers of the input signal and noise component is allowed by separately. Now assuming the maximum sinusoidal wave peak value of input signal is V_{ref}, the AC r.m.s. value is $V_{ref}/(2\sqrt{2})$ which is band-limited below the f_0. Thus, the signal power P_s, is

$$P_s = \left(\frac{V_{ref}}{2\sqrt{2}}\right)^2 = \left(\frac{2^N V_{LSB}}{2\sqrt{2}}\right)^2 = \frac{(2^N V_{LSB})^2}{8} \tag{3.11}$$

In this the noise component is dominated by quantization noise and we consider that the noise will be reduced by lowpass filter. Recalling the (3.7) then we can obtain the quantization noise



(a) Frequency response of the lowpass filter



(b) Simply oversampling system

Figure 3.6: A simplified oversampling model.

power at the oversampling output.

$$P_q = \int_{-f_s/2}^{f_s/2} |H(f)|^2 \cdot S_q(f)df = \int_{-f_0}^{f_0} 1 \cdot S_q(f)df$$
$$= \frac{2f_0}{f_s}\frac{V_{LSB}^2}{12} = \left(\frac{1}{OSR}\right)\frac{V_{LSB}}{12} \tag{3.12}$$

Therefore, the quantization noise power P_q has been reduced by increasing OSR or(and) decreasing quantizr step size. For example, want to decrease the quantization noise power by one-half (or, equivalently, 3 dB (0.5 bits)) that the OSR should be increased by doubling. We can calculate the maximum SNR(in dB) to be the ratio of the maximum sinusoidal power to the quantization noise power at the output of the oversampling system in Fig. 3.6(b). Mathematically, we have through the use of (3.11) and (3.12)

$$SNR = 10\log\left(\frac{P_s}{P_q}\right) = 10\log\left(\frac{OSR \cdot 3 \cdot 2^{2N}}{2}\right)$$
$$= 10\log(OSR) + 10\log\left(\frac{3 \cdot 2^{2N}}{2}\right) dB \tag{3.13}$$

Compare (3.9) with (3.13), and we can know that the OSR term is the SNR enhancement obtained from oversampling technique. Here we see that straight oversampling gives a SNR imprvement of 3 dB/octave or, equivalently 0.5 bits/octave.

3.2.3 Noise-Shaped Σ-Δ Modulator

In the previous section, we can know that the sampling frequency have to greater than 168GHz by using oversampling technique which form 1-bit quantizer bit-stream out to achieve a 12-bit resolution in normally audio band about 20kHz and that is unreasonable, hard to implement and rather high cost. Thus, the noise shaping technique usually be used for oversampling A/D converter which is called Σ-Δ **Analog-to-Digital Converter** (e.g. it pushes the quantization noise outside the signal band as its shown in Fig 3.7). The system architecture of an oversampling A/D converter is shown in Fig. 3.8. The first stage is a continuous-time anti-aliasing filter and is required to band-limit the input signal frequencies less than one-half the oversampling frequency, f_s. The anti-aliasing filter can often be quite simple such as a simple RC low-pass filter when the oversampling ratio is large. Following the anti-aliasing filter, the continuous-time signal, $X_C(t)$, is sampled by a sample-and-hold. This signal is then processed by the SDM, which cinverts the analog signal into a noise-shaped low-resolution digital signal. The

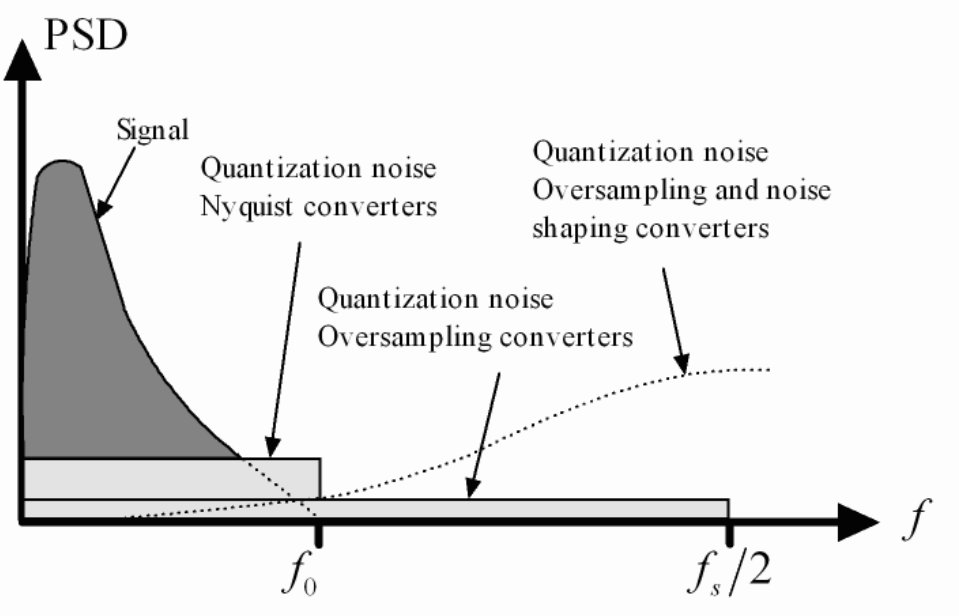


Figure 3.7: Spectral at the output of a noise shaping quantizer loop compared to those obtained from Nyquist and Oversampling converters.

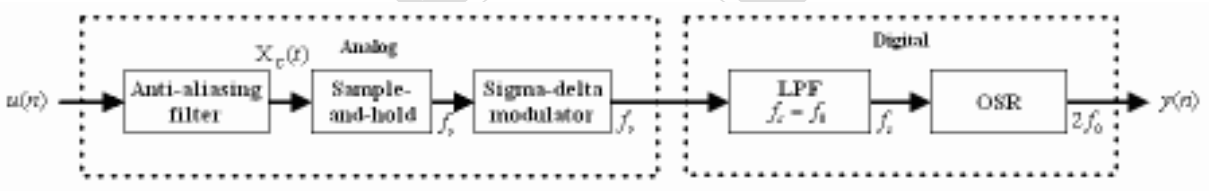


Figure 3.8: Block diagram of an oversampling Σ-Δ A/D converter.

third block in the system is a decimator. It converts the oversampled low-resolution digital signal into a high-resolution digital signal at a lower sampling rate usually equal to twice the desired bandwidth of the input signal. The decimation filter can be conceptually thought of as a low-pass filter followed by a down sampler, although in many systems the decimation is performed in a number of stages. It should be mentioned that in many realization where the SDM is realized using switched-capacitor circuitry, a separate sample-and-hold is not required, as the continuous-time signal is inherently sampled by the switches and input capacitors of the switched capacitor SDM. In Fig. 3.3(b), the PSD of the quantization noise was indicated as a constant over the entire frequency band. The concept of noise shaping is modifying the quantization noise distribution type from uniform to no longer uniform, and shaping the most of the quantization noise outside the signal band. Then, the decimation filter removes more of the quantization noise from out of the signal band. A general noise-shaped SDM and its linear model are shown in Fig. 3.10. In Fig. 3.9(a) shows the feedback system is implemented with

(a) (b)

Figure 3.9: A modulator and its linear model: (a) a general SDM; (b) linear model of the SDM.

a integrator $H(z)$ and a quantizer, in which, the integrator structure is a switch-capacitor form. Treating the approximation linear model is shown in Fig. 3.9(b) as having two independent inputs, input signal $U(z)$ and quantization noise $Q(z)$. We can derive a signal transfer function, $S_{TF}(z)$, and a noise transfer function, $N_{TF}(z)$, by setting $Q(z) = 0$ and $U(z) = 0$, respectively.

$$S_{TF}(Z) \equiv \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \tag{3.14}$$

$$N_{TF}(Z) \equiv \frac{Y(z)}{Q(z)} = \frac{1}{1 + H(z)} \tag{3.15}$$

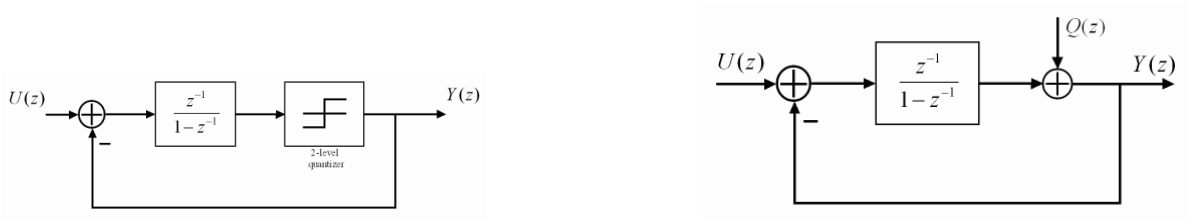
From (3.15), as we have seen, when $H(z)$ goes to infinity, we see that the noise transfer function, N_{TF}, will go to zero. In other words, the zeros of the N_{TF} will be equal to the poles of $H(z)$. We can also write the output signal as the combination of the input signal and the noise signal, with each being filtered by the corresponding transfer function. In the frequency domain, we have

$$Y(z) = S_{TF}(z)U(z) + N_{TF}(z)Q(z) \tag{3.16}$$

To noise-shape the quantization noise in a useful manner, $H(z)$ is properly chosen such that its magnitude is large from 0 to f_0 (e.g. over the frequency band of interest). With such a choice, the signal transfer function, $S_{TF}(z)$, will approximate unity over the frequency band of interest very similarly to an opamp in a unity-gain feedback configuration. Furthermore, the noise transfer function, $N_{TF}(z)$, will approximate zero over the same band. Thus, the quantization noise is reduced over the frequency band of interest while the signal itself is mostly unaffected[12].

A. First-Order Σ-Δ Modulators

The SDM was briefly introduced in Sec. 3.2.3. This modulator employs oversampling to spread the quantization noise over the $[0, f_s/2]$ frequency band, as well as noise shaping in order to



(a) (b)

Figure 3.10: Block diagram of a first-order SDM (a) and its linear model (b).

push most of the in-band noise out of this band to higher frequencies. In Fig. 3.10(a) shows the block diagram of first-order SDM, while for the sake of analysis its linear model is shown in Fig. 3.10(b). The sampler and the encoder are omitted as they have no impact on the analysis at this level, while the quantizer is replaced by its linear model. Consideration for $H(z)$ which is shown in Fig. 3.10(b) that we can put it into (3.14) and (3.15) both, and then we can easily obtain the following:

$$S_{TF}(Z) = \frac{H(z)}{1+H(z)} = \frac{\frac{z^{-1}}{1-z^{-1}}}{1+\frac{z^{-1}}{1-z^{-1}}} = z^{-1} \tag{3.17}$$

$$N_{TF}(Z) = \frac{1}{1+H(z)} = \frac{1}{1+\frac{z^{-1}}{1-z^{-1}}} = 1-z^{-1} \tag{3.18}$$

Combining (3.17) and (3.18) with (3.16) that the total transfer function of this system is

$$Y(z) = z^{-1} \cdot U(z) + (1-z^{-1}) \cdot Q(z) \tag{3.19}$$

Clearly, the $S_{TF}(z)$ leaves the signal unaltered, just delayed by the period of a single bit, whereas the $N_{TF}(z)$ high-passes the quantization noise which has be shaped to high frequencies and suppressed in the low-frequency range. Note that the transfer function of the quantization noise, $N_{TF}(z) = (1-z^{-1})$, is first order; furthermore, the order of modulator is defined by how many order of $N_{TF}(z)$ it is, so, the modulator is called first-order SDM.

To find the magnitude of the noise transfer function, $|N_{TF}(z)|$, we let $z = e^{jwT} = e^{j2\pi f/f_s}$ substitute into (3.15) and write the following as

$$\begin{aligned} N_{TF}(f) &= 1 - e^{-2\pi f/f_s} = 2j \cdot e^{-j\pi f/f_s} \cdot \frac{e^{j\pi f/f_s} - e^{-j\pi f/f_s}}{2j} \\ &= 2j \cdot e^{-j\pi f/f_s} \cdot sin\left(\frac{\pi f}{f_s}\right) \end{aligned} \tag{3.20}$$

Thus, we can obtain the magnitude of the noise transfer function as

$$|N_{TF}(f)_{1st}| = 2sin\left(\frac{\pi f}{f_s}\right) \tag{3.21}$$

The in-band noise power(i.e, the quantization noise in the frequency range $[-f_0, f_0]$) at the output of a first order Σ-Δ modulator is

$$P_q = \int_{-f_0}^{f_0} |N_{TF}(f)_{1st}|^2 \cdot S_q(f)df = \frac{V_{LSB}^2}{12f_s} \int_{-f_0}^{f_0} \left[2sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \tag{3.22}$$

In this which is an oversampling system, f_s has much larger than f_0. We can approximate $sin((\pi f)/f_s)$ to be $(\pi f)/f_s$ and then obtain as

$$P_q \simeq \left(\frac{V_{LSB}^2 \cdot \pi^2}{12 \cdot 3}\right)\left(\frac{2f_0}{f_s}\right)^3 = \frac{V_{LSB}^2 \cdot \pi^2}{36}\left(\frac{1}{OSR}\right)^3 \tag{3.23}$$

Assuming the maximum input signal power is a sinusoid waveform,thus it's power is the same as that obtained before in (3.11), the maximum SNR for a first-order SDM is given by

$$\begin{aligned} SNR_{max} &= 10\log\left(\frac{P_s}{P_q}\right) = 10\log\left(\frac{9 \cdot 2^{2N} \cdot OSR^3}{2\pi^2}\right) \\ &= 10\log(OSR^3) + 10\log\left(\frac{3 \cdot 2^{2N}}{2}\right) + 10\log\left(\frac{3}{\pi^2}\right) \\ &= 30\log(OSR) + 6.02N + 1.76 - 5.17\ dB \end{aligned} \tag{3.24}$$

From (3.24), we sense that each doubling of the OSR improves the SNR by 9 dB or, equivalent, a gain of 1.5 bits for a first-order modulator.

We consider the total quantization noise power of a first-order modulator on the side. We can obtain the total quantization noise power of a first-order modulator as

$$\begin{aligned} P_{q,total} &= \frac{V_{LSB}^2}{12f_s} \int_{-f_s/2}^{f_s/2} \left[2sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \\ &= \frac{V_{LSB}^2}{6f_s} \int_{-f_s/2}^{f_s/2} 1 - cos(2\pi f/f_s)df = \frac{V_{LSB}^2}{6} \end{aligned} \tag{3.25}$$

We can easy to recognize that the quantization noise total power is increased from $V_{LSB}^2/12$ at the output of the oversampling system to $V_{LSB}^2/6$ at the output of the noise-shaping system. We can find this result clearly from observing in Fig. 3.7,too. However, we make sure that the quantization noise power of inside the signal band, f_0, is lower than the only using oversampling technique system.

B. Second-Order Σ-Δ Modulators

Including one more integrator in the modulator loop increases the noise transfer function order to two. The linear model of the resulting architecture shows in Fig. 3.11. According to the linear

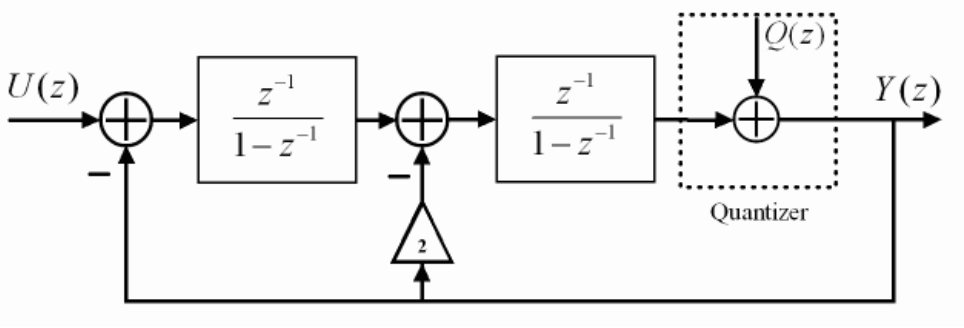


Figure 3.11: A second-order oversampling Σ-Δ A/D converter.

model of the second-order SDM, the Z-domain expression of the second-order SDM output can be written as

$$Y(z) = z^{-2} \cdot U(z) + (1 - z^{-1})^2 \cdot Q(z) \tag{3.26}$$
$$= S_{TF} \cdot U(z) + N_{TF} \cdot Q(z)$$

The N_{TF} term has a second order highpass filter characteristics. From previously equation, we can obtain the magnitude of the second-order noise transfer function as

$$|N_{TF}(f)_{2nd}| = \left[2sin\left(\frac{\pi f}{f_s}\right)\right]^2 \tag{3.27}$$

In Fig. 3.12 points out the advantages of the second-order modulator with respect to the first-order one by comparing both quantization noises in the frequency domain. Note that for the second-order modulator, the spectral density significantly diminishes in the low frequency region, at the price of an increase in the high frequency region. Consequently, the result leads to a lower total in-band quantization noise than the first-order one's, calculated the total in-band PSD of the quantization noise as

$$P_q = \int_{-f_0}^{f_0} |N_{TF}(f)_{2nd}|^2 \cdot S_q(f) df = \frac{V_{LSB}^2}{12 f_s} \int_{-f_0}^{f_0} \left[2sin\left(\frac{\pi f}{f_s}\right)\right]^4 df$$
$$\simeq \left(\frac{V_{LSB}^2 \cdot \pi^4}{12 \cdot 5}\right)\left(\frac{2f_0}{f_s}\right)^5 = \frac{V_{LSB}^2 \cdot \pi^4}{12 \cdot 5}\left(\frac{1}{OSR}\right)^5 \tag{3.28}$$

Again, assuming the maximum signal power is that obtained in (3.11), the maximum SNR for a second-order Σ-Δ modulator is given by

$$SNR_{max} = 10\log\left(\frac{P_s}{P_q}\right) = 10\log\left(\frac{15 \cdot 2^{2N} \cdot OSR^5}{2\pi^4}\right)$$
$$= 10\log(OSR^5) + 10\log\left(\frac{3 \cdot 2^{2N}}{2}\right) + 10\log\left(\frac{5}{\pi^4}\right)$$
$$= 50\log(OSR) + 6.02N + 1.76 - 12.9\, dB \tag{3.29}$$

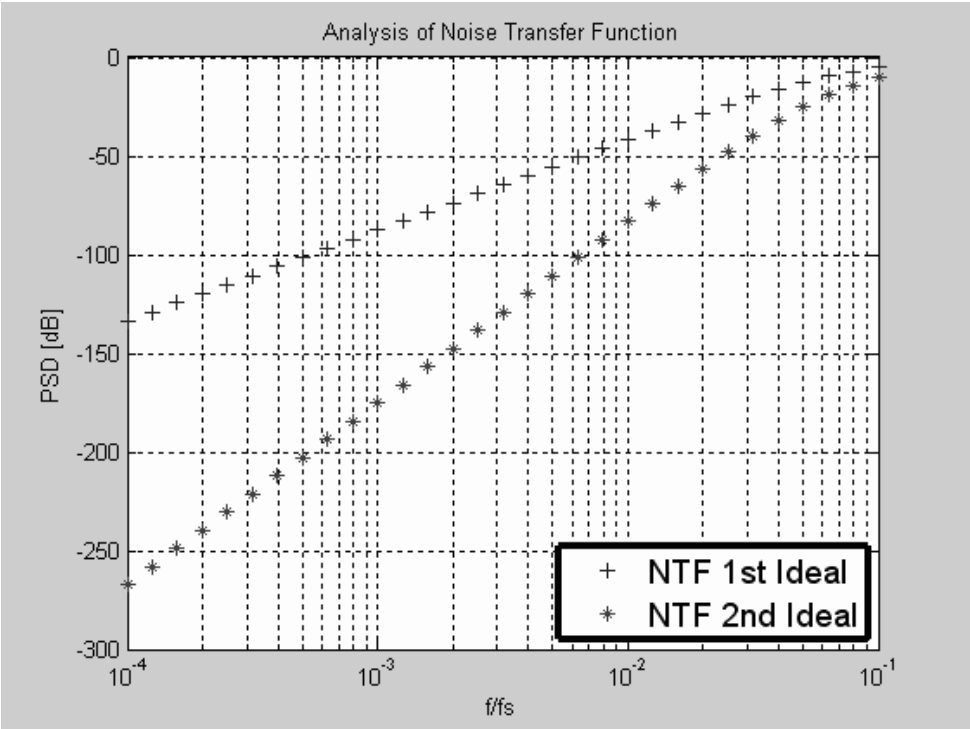


Figure 3.12: Noise transfer functions of a first- and second-order SDM as a function of the frequency.

Clearly, each doubling of the OSR improves the SNR by 15 dB or, equivalent, a gain of 2.5 bits for a second-order modulator. Not only does the second-order SDM provide better SNR but also does a better job of decoloring the quantization noise and de-correlating the quantization noise from the input signal.

Again, we consider the total quantization noise power of a second-order modulator on the side. We can obtain the total quantization noise power of a second-order modulator as

$$\begin{aligned} P_{q,total} &= \frac{V_{LSB}^2}{12f_s}\int_{-f_s/2}^{f_s/2}\left[2sin\left(\frac{\pi f}{f_s}\right)\right]^4 df = \frac{2V_{LSB}^2}{3f_s}\int_{-f_s/2}^{f_s/2}(1-cos^2(2\pi f/f_s)df \\ &= \frac{2V_{LSB}^2}{3f_s}\int_{-f_s/2}^{f_s/2}(1-cos(2\pi f/f_s)+cos^2(2\pi f/f_s)df \\ &= \frac{2V_{LSB}^2}{3f_s}\left[\frac{3}{2}f_s+\frac{1}{2}\int_{-f_s/2}^{f_s/2}cos(4\pi f/f_s)df\right] \\ &= V_{LSB}^2 \end{aligned} \tag{3.30}$$

Comparing (3.30) and (3.25), although the total quantization noise power of the second-order SDM is greater than the first-order one, less of the quantization noise inside the signal band for second-order case. The general shape of zero-,first-,second-order noise-shaping curves are shown in Fig. 3.13. Note that the in-band quantization noise decreases as the noise-shaping or-

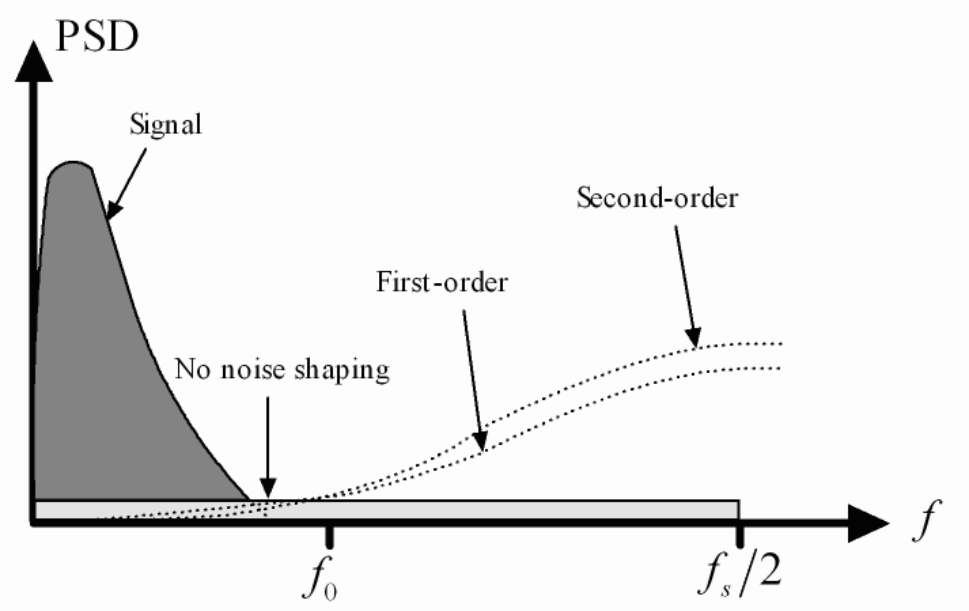


Figure 3.13: Noise transfer functions for some different noise-shaping modulators.

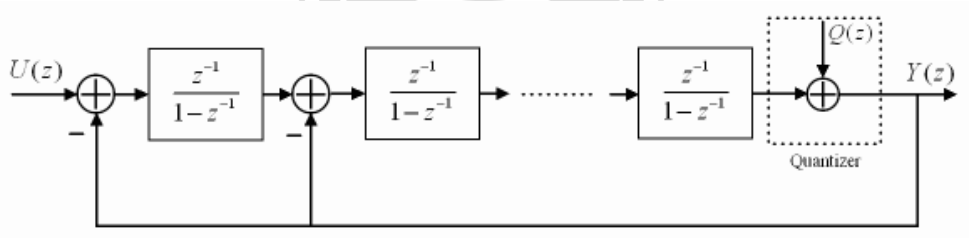


Figure 3.14: Lth-order single-loop SDM.

der increase. However, the out-of-band and total quantization noise powers increase for higher-order modulators.

C. Single-Loop High-Order Σ-Δ Modulators

The above expression for a 1st- and 2nd-order can be extended to a modulator of order L, whose more direct implementation consists of including L integrators before the quantization[13]. A block diagram of a generalized single-loop modulator is shown in Fig. 3.14 whose expression of the L-order SDM output in Z-domain can be written as

$$Y(z) = z^{-L} \cdot U(z) + (1 - z^{-1})^L \cdot Q(z) \tag{3.31}$$
$$= S_{TF} \cdot U(z) + N_{TF} \cdot Q(z)$$

From previous section, we can easily get the magnitude of the L-order noise transfer function

and the total in-band PSD of the quantization noise, and show these as flowing, respectively.

$$|N_{TF}(f)_{2nd}| = \left[2sin\left(\frac{\pi f}{f_s}\right)\right]^L \tag{3.32}$$

$$\begin{aligned} P_q &= \int_{-f_0}^{f_0} |N_{TF}(f)_{Lth}|^2 \cdot S_q(f)df = \frac{V_{LSB}^2}{12f_s}\int_{-f_0}^{f_0}\left[2sin\left(\frac{\pi f}{f_s}\right)\right]^{2L} df \\ &\simeq \frac{V_{LSB}^2}{12f_s}\int_{-f_0}^{f_0}\left[2\left(\frac{\pi f}{f_s}\right)\right]^{2L} df = \left(\frac{V_{LSB}^2\cdot\pi^{2L}}{12\cdot(2L+1)}\right)\left(\frac{2f_0}{f_s}\right)^{2L+1} \\ &= \left(\frac{V_{LSB}^2\cdot\pi^{2L}}{12\cdot(2L+1)}\right)\left(\frac{1}{OSR}\right)^{2L+1} \end{aligned} \tag{3.33}$$

Assuming the maximum signal power is the same as the previous present, then we can obtain the maximum SNR of the L-order modulator as

$$\begin{aligned} SNR_{max} &= 10\log\left(\frac{P_s}{P_q}\right) = 10\log\left(\frac{3\cdot(2L+1)\cdot 2^{2N}\cdot OSR^{2L+1}}{2\pi^{2L}}\right) \\ &= 10\log(OSR^{2L+1}) + 10\log\left(\frac{3\cdot 2^{2N}}{2}\right) + 10\log\left(\frac{2L+1}{\pi^{2L}}\right) \\ &= (20L+10)\log(OSR) + 10\log(\frac{2L+1}{\pi^{2L}}) + 6.02N + 1.76\ dB \end{aligned} \tag{3.34}$$

In general, each doubling of the OSR improves the SNR by $3(2L+1)$ dB or, equivalent, a gain of $L+0.5$ bits for a second-order modulator. For a given OSR, a high-order SDM is capable of much greater SNR than a second-order one.

However, a drawback of the SDMs with $L > 2$ is their tendency to instability[14]. A modulator is considered stable if, for bounded inputs and whatever integrator initial conditions, the internal state variables (integrator outputs) remain also bounded over time. It can be shown that a first-order modulator is intrinsically stable for whatever input in the range $(-V_{ref}/2, V_{ref}/2)$. In the same way, the stability of the second-order modulator of Fig. 3.11, with feedback-loop gain divide by feedforward-loop gain equals 2, which guarantees the stability of the loop[15].

3.3 Circuit Configurations And Comparisons of First-Order Σ-Δ Modulator

In the chapter 2, we know that the C-V converter of the capacitive sensing system is performing a capacitance detection. The variation frequency of the capacitance is always varied at a low frequencies range (about 1 KHz) in nature world. For avoiding the low frequency effects (e.g.,

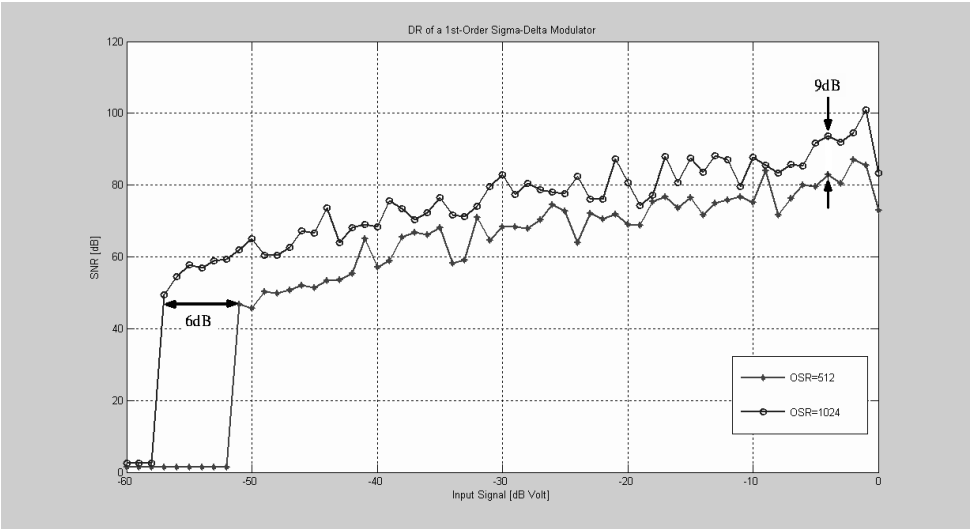


Figure 3.15: The DR of Considerations for the OSR is equal to 512 and 1024, respectively.

filker noise.), the sampling clock rate, f_S=1MHz is used. Where about the skill of reducing the low frequency noise will be discussed in following chapter.

Clearly, a high OSR (f_S=1MHz) is obtained such that a high resolution (SNR) of a vibrational motion detection system is easily achieved that are supposed for prior inferences. Hence, there has several SDM can be chosen from up to know. However, to use high-order architecture that usually follows complex design and more detail cogitation for stability.

Furthermore, we know that the amplitude of the input signal always proportional to its frequency in a vibrational motion sensing system. Apparently, a first-order SDM should be chosen although it has a intrinsic restriction such as its dynamic range is directly proportioned to OSR that shows in Fig. 3.15. Continuously, for our goal, the primary performance is to perform a peak-SNR more than 72 dB for a around 1K-Hz signal band-limited with $OSR = 512$, while a first-order SDM is exactly decided through (3.34) to meet objective.

In this section, we discuss about with the system architecture design of a traditional single-bit first-order single-loop Σ-Δ modulator and a new one. Note that the new proposed structure can reduce the capacitor size and the error from capacitor mismatch which due to the process variation of differential input-capacitor(C_S) ,feedback capacitor(C_F) and integrator capacitor(C_I); this structure is called capacitor-sharing type of SDM. It has two advantages of lesser capacitor area and lesser capacitor mismatch effect than traditional type.

Whereas the impact of the implementation non-idealities, including non-idealities OTA gain, slew rate, integrator settling, and so on, which are also considered by each one expressed

Table 3.1: Charge distribution correspond with clock phase for traditional type.

Capacitor Charges and Node Vlotage	At P1, Pd1: "H"; P2, Pd2: "L"	At P1, Pd1: "L"; P2, Pd2: "H"
Q_{C_S}	$C_S V_S(n)$	$-C_S V_a(n-1/2)$
Q_{C_F}	0	$C_F(Y_{bar}(n+1/2) - V_a(n-1/2))$
Q_{C_I}	$C_I(V_o(n+1/2) - V_a(n+1/2))$	$C_I(V_o(n-1/2) - V_a(n-1/2))$
$Q_{C_{CDS}}$	$C_{CDS}V_{os}(n)$	$C_{CDS}(V_{os}(n-1/2) -$ $V_o(n-1/2)/A - V_a(n-1/2))$
Q_{C_P}	0	$-C_P V_a(n-1/2)$
V_a	0	$V_{os}(n-1/2) -$ $V_o(n-1/2)/A - V_{os}(n)$ $\simeq -V_o(n-1/2)/A$

Table 3.2: Charge distribution correspond with clock phase for capacitor-sharing type.

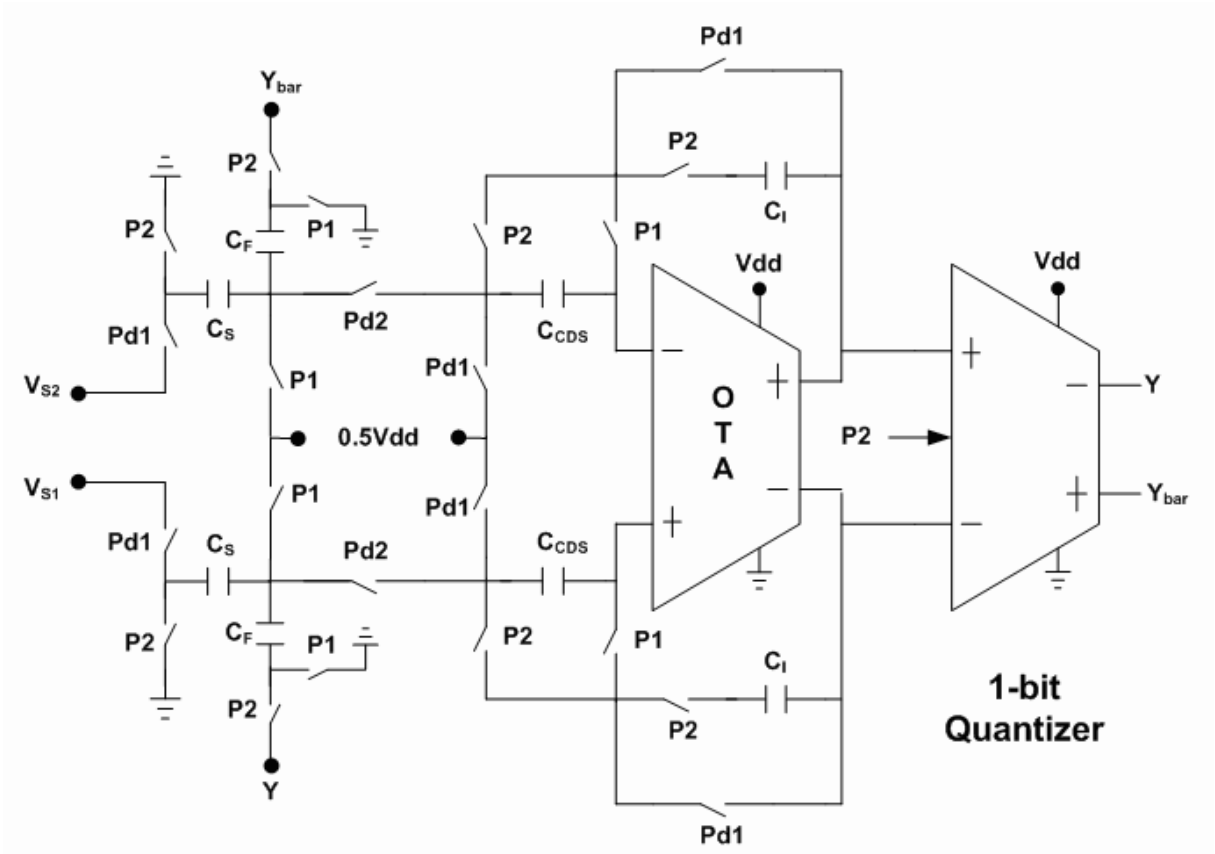
Capacitor Charges and Node Vlotage	At P1, Pd1: "H"; P2, Pd2: "L"	At P1, Pd1: "L"; P2, Pd2: "H"
Q_{C_S}	$-2C_S V_S(n)$	$-2C_S V_a(n-1/2)$
Q_{C_F}	$-2C_F Y_{bar}(n+1/2)$	$-2C_F V_a(n-1/2)$
Q_{C_I}	$C_I(V_o(n+1/2) - V_a(n+1/2))$	$C_I(V_o(n-1/2) - V_a(n-1/2))$
$Q_{C_{CDS}}$	$C_{CDS}V_{os}(n)$	$C_{CDS}(V_{os}(n-1/2) -$ $V_o(n-1/2)/A - V_a(n-1/2))$
Q_{C_P}	0	$-C_P V_a(n-1/2)$
V_a	0	$V_{os}(n-1/2) -$ $V_{os}(n) - V_o(n-1/2)/A$ $\simeq -V_o(n-1/2)/A$

Note: The $V_a(n-1/2)$ is similarly equal to $-V_o(n-1/2)/A$ due to the charge of the C_{CDS} is no leakage, while the $V_{os}(n) = V_{os}(n-1/2)$ can be assumed. The C_P is a parasitical capacitance at Node V_a.

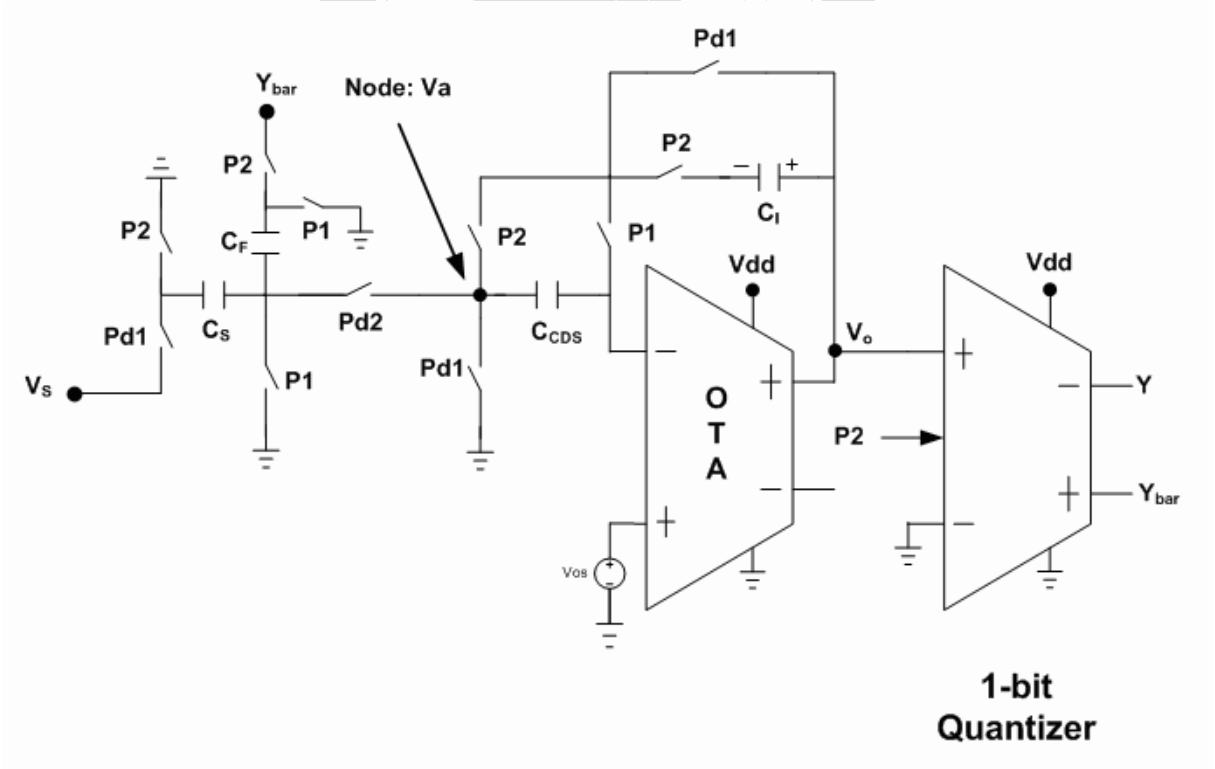
in following section (Considerations of Some Non-Idealities Conditions).

3.3.1 Comparisons of The Circuit Level System

There are shows of a traditional single-bit first-order single-loop SDM and a capacitor-sharing type of one in Fig. 3.16(a) and Fig. 3.17(a). Which can be equalized as differential mode equivalent half-circuit with a finite gain A of the OTA, and a input refer offset voltage(V_{OS}). The equivalent half-circuit of them shows in Fig. 3.16(b) and Fig. 3.17(b); where a few differences like as that the sizes of the C_S, C_F and clock phase which can be discovered easily. Presently, we consider that the charge distribution of each capacitor for the traditional type and capacitor-sharing type is shown in Table 3.1 and Table 3.2, respectively.

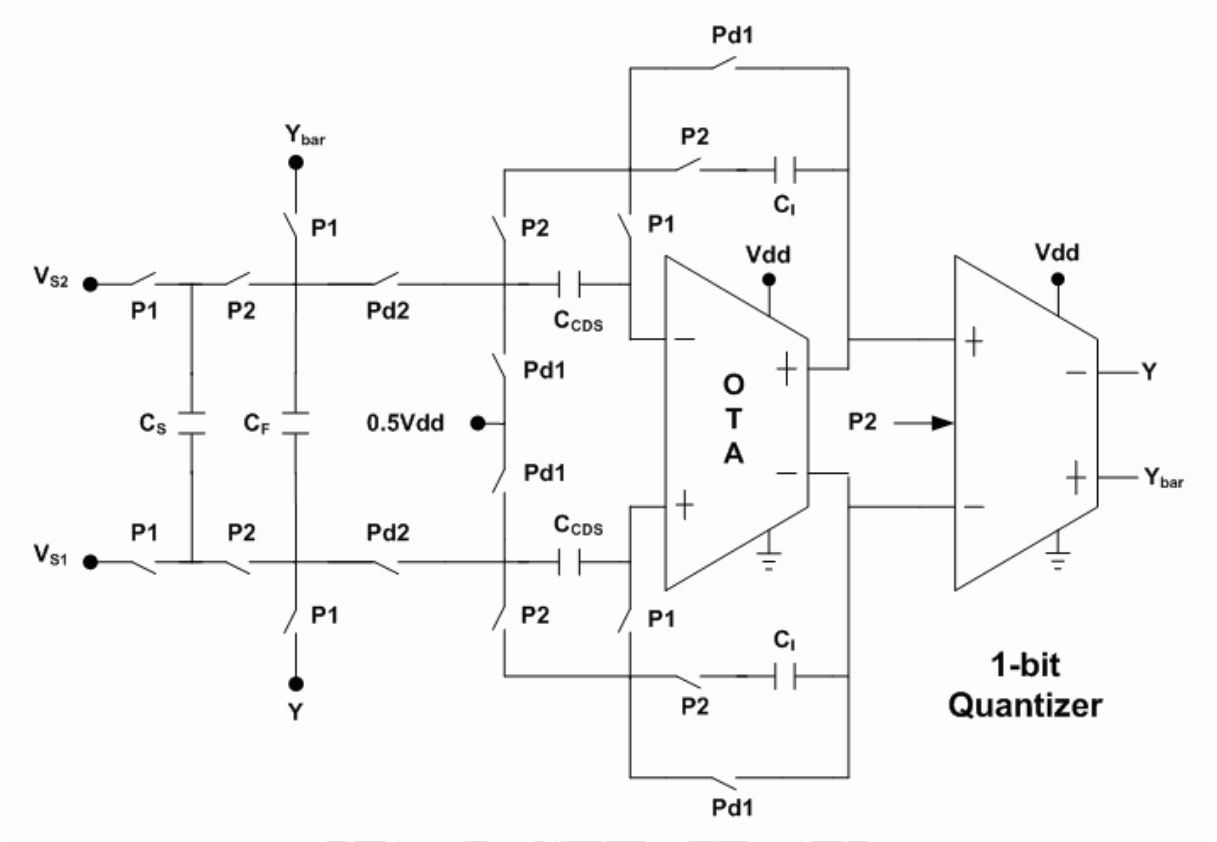


(a)

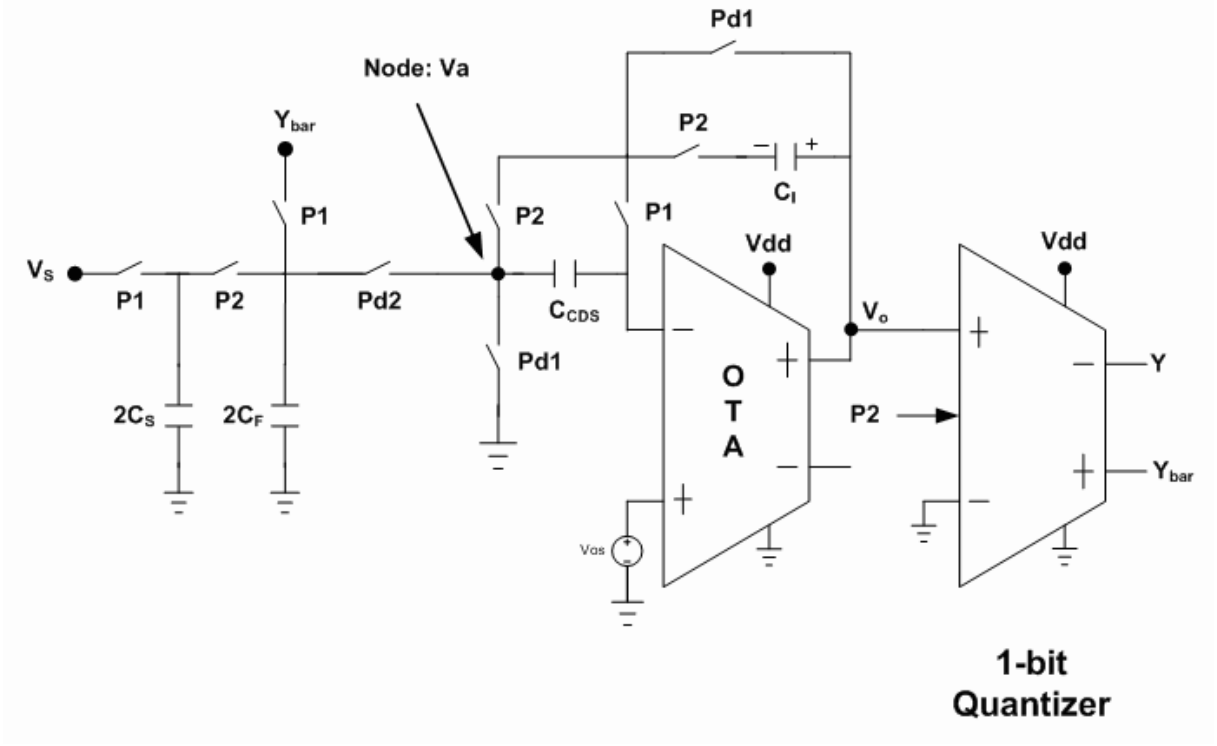


(b)

Figure 3.16: Schemes of a traditional first-order SDM(a) and its differential mode half circuit(b).



(a)



(b)

Figure 3.17: Schemes of a capacitor-sharing type of first-order SDM(a) and its differential mode half circuit(b).

Thus, according to Table 3.1, the relational equation can be combined and written as below

$$C_S V_S(n) + C_I(V_o(n+1/2) - V_a(n+1/2)) + C_{CDS}V_{os}(n) =$$
$$- C_S V_a(n-1/2) + C_F(Y_{bar}(n+1/2) - V_a(n-1/2)) + C_I(V_o(n-1/2) -$$
$$V_a(n-1/2)) + C_{CDS}V_{os}(n-1/2) - C_P V_a(n-1/2)$$

similar equal to

$$C_F Y_{bar}(n+1/2) =$$
$$C_S V_S(n) + (C_I + C_I/A)V_o(n+1/2) - (C_I + (C_S + C_F + C_I + C_P)/A)V_o(n-1/2)$$

using z-transformation, we obtain

$C_F Y_{bar}(z) z^{1/2} =$

$C_S V_S(z) + (C_I + C_I/A)V_o(z)z^{1/2} - (C_I + (C_S + C_F + C_I + C_P)/A)V_o(z)z^{-1/2}$

assumed $C_S + C_F + C_I + C_P = C_T$ and multiplied by $z^{-1/2}$ on two side of the equal mark.

$\Rightarrow$

$C_F Y_{bar}(z) = C_S V_S(z)z^{-1/2} + (C_I + C_I/A)V_o(z) - (C_I + C_T/A)V_o(z)z^{-1}$

$$Y_{bar}(z) = \frac{C_S}{C_F}V_S(z)z^{-1/2} + \frac{C_I + C_T/A}{C_F}V_o(z)\left(\frac{C_I + C_I/A}{C_I + C_T/A} - z^{-1}\right) \tag{3.35}$$

Also similarly above, the capacitor-sharing type can be analysed by the same way for using the information of the Table 3.2, the procedure is shown in below as

$$- 2C_S V_S(n) - 2C_F Y_{bar}(n+1/2) + C_I(V_o(n+1/2) - V_a(n+1/2)) + C_{CDS}V_{os}(n) =$$
$$- 2C_S V_a(n-1/2) - 2C_F V_a(n-1/2) + C_I(V_o(n-1/2) - V_a(n-1/2)) +$$
$$C_{CDS}V_{os}(n-1/2) - C_P V_a(n-1/2)$$

similar equal to

$$2C_F Y_{bar}(n+1/2) =$$
$$- 2C_S V_S(n) + (C_I + C_I/A)V_o(n+1/2) - (C_I + (2C_S + 2C_F + C_I + C_P)/A)V_o(n-1/2)$$

using z-transformation, we obtain

$2C_F z^{1/2} Y_{bar}(z) =$

$-2C_S V_S(z) + (C_I + C_I/A)z^{1/2}V_o(z) - (C_I + (2C_S + 2C_F + C_I + C_P)/A)z^{-1/2}V_o(z)$

assumed $2C_S + 2C_F + C_I + C_P = C_T$ and multiplied by $z^{-1/2}$ on two side of the equal mark.

$\Rightarrow$

$2C_F Y_{bar}(z) = -2C_S z^{-1/2} V_S(z) + (C_I + C_I/A)V_o(z) - (C_I + C_T/A)z^{-1}V_o(z)$

$$\begin{aligned} Y_{bar}(z) &= -\frac{C_S}{C_F} z^{-1/2} V_S(z) + \frac{C_I + C_T/A}{2C_F}\left(\frac{C_I + C_I/A}{C_I + C_T/A} - z^{-1}\right) V_o(z) \\ &\equiv S_{TF}(z)U(z) + N_{TF}(z)Q(z) \end{aligned} \tag{3.36}$$

Both of the equations of related to Y_{bar} can be clearly represented at (3.35) and (3.36). Continually, we consider about that the system design carefully by using these equations.

In practice, the stability of first-order SDM is never considered because it is a one-pole system. Another important consideration in the design of a SDM is the size of the integrator output swing as the modulator input approaches full scale. Unfortunately, the output swing of the integrator is usually limited by the linear region of the operational amplifier in the integrator which the $V_{PP.}$ peak to peak voltage of the integrator linear output range is typically only a fraction of the supply voltage (V_{dd}), it is normally equal to one. Thus, the system simulation should include the output swing of the integrator. Assuming the OTA has a infinite gain to simply the analysis, the (3.35) and (3.36) can be rewritten as

traditional case:

$$Y_{bar}(z) = \frac{C_S}{C_F} z^{-1/2} V_S(z) + \frac{C_I}{C_F}(1 - z^{-1})V_o(z) \tag{3.37}$$

$$(1 - z^{-1})V_o(z) = -\frac{C_S}{C_I} z^{-1/2} V_S(z) + \frac{C_F}{C_I} Y_{bar}(z) \tag{3.38}$$

Capacitor-sharing case:

$$Y_{bar}(z) = -\frac{C_S}{C_F} z^{-1/2} V_S(z) + \frac{C_I}{2C_F}(1 - z^{-1})V_o(z) \tag{3.39}$$

$$(1 - z^{-1})V_o(z) = \frac{2C_S}{C_I} z^{-1/2} V_S(z) + \frac{2C_F}{C_I} Y_{bar}(z) \tag{3.40}$$

The traditional and capacitor-sharing type modulator can be simplified to its linear model from

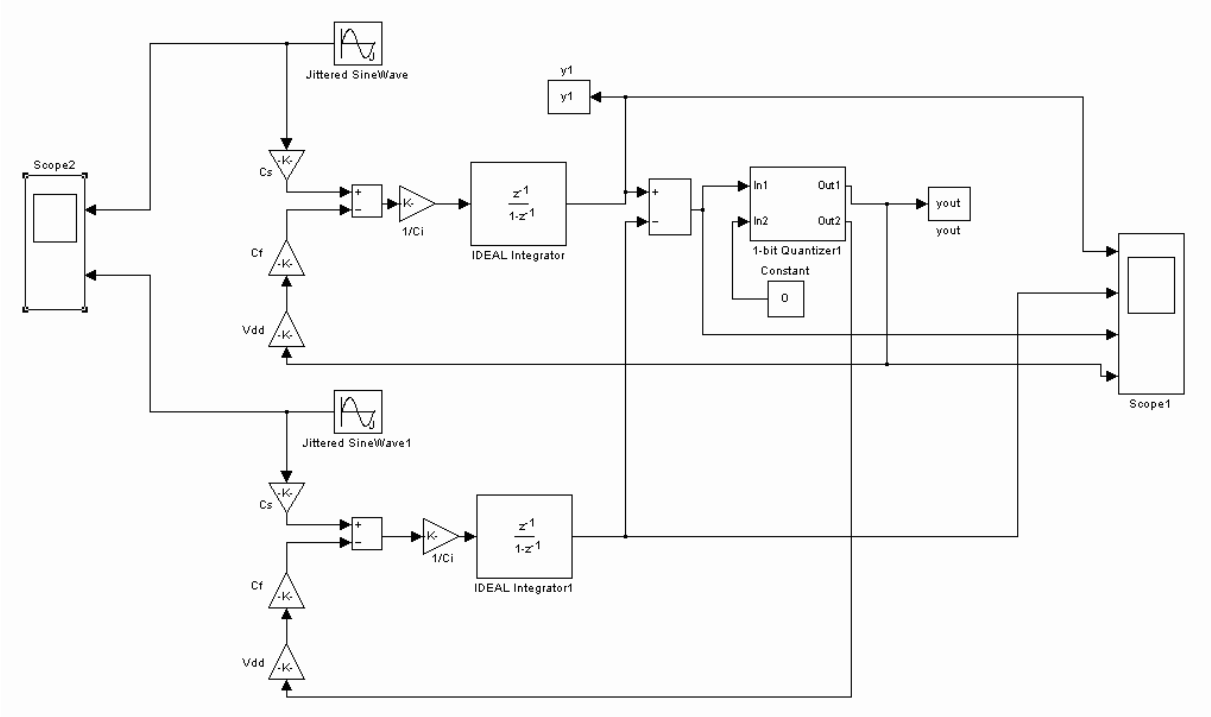
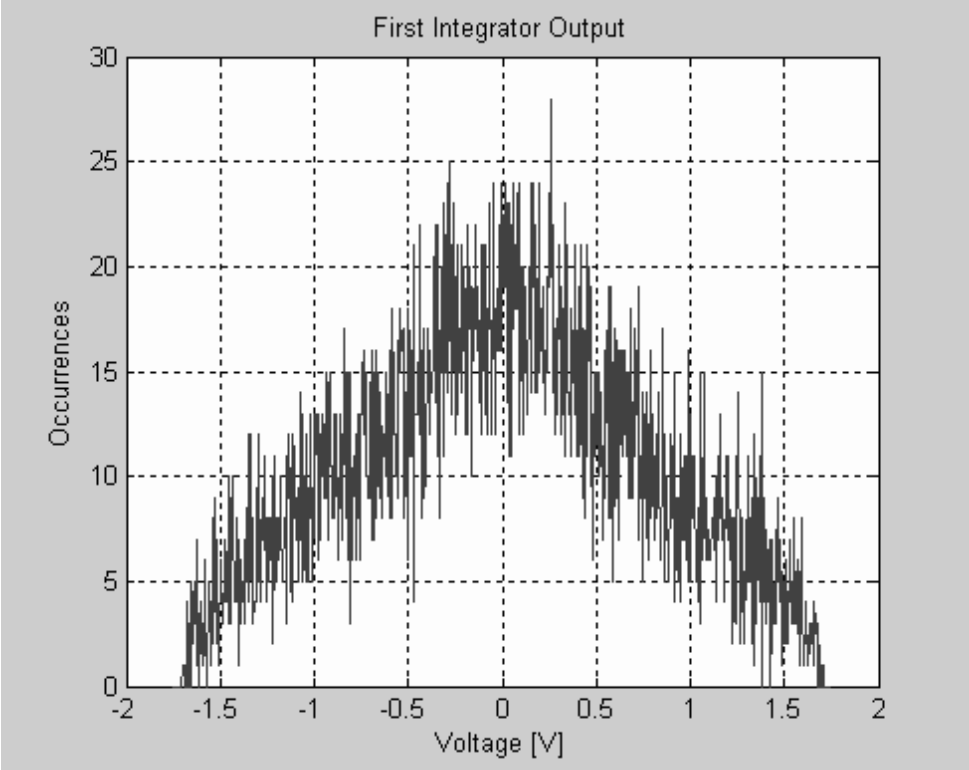
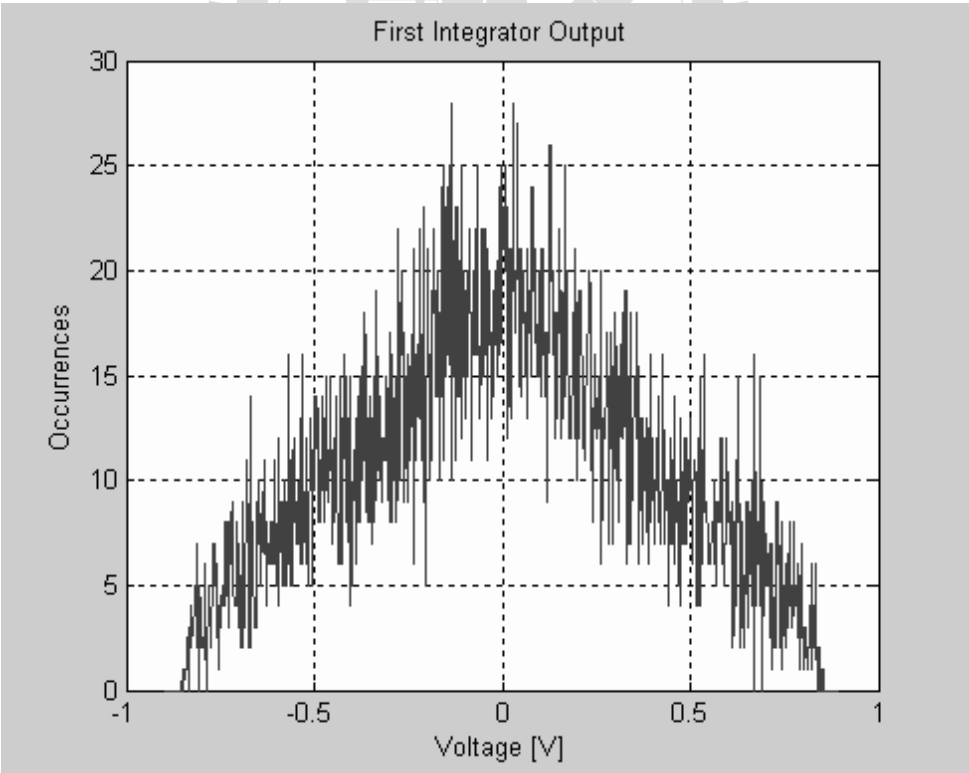


Figure 3.18: A fully differential first-order SDM created by using Matlab-Simulink.

(3.38) and (3.40), both of the fully differential equivalent models that can be equalized by using the concept of equivalent half circuit are shown in Fig. 3.18. The equivalent models are created by Matlab-Simulink. Where the capacitors are affecting the integrator output swing which is clearly indicated in (3.38) and (3.40). The differential output distribution range of the integrator is shown in Fig. 3.19(a) when the feedback reference levels are normalized to $\pm 0.5V$. It shows clearly that the without scaling differential output of integrator is out of the linear range of the integrator differential output lead to more of the harmonic noise if our integrator differential output range is set in $\pm 1V$. Therefore, we can reset the capacitors size , C_I, especially. The size of C_I is bigger than C_S two times is usefully to lead the integrator differential output range stay in linear range of our setting. We can obtain the differential output distribution range of the integrator shown in Fig. 3.19(b). As the results and equations, comparing the structure for traditional and capacitor-sharing type, we can easily to conscious of that the size of C_S and C_F for the capacitor-sharing type is less than traditional type two times. From the results, the capacitor ratio can be shown in Table 3.3. Where the C_F is set equal to $C_S \cdot V_S$ over V_{dd} due to that the feedback factor is multiply by $Y_{bar} = V_{dd}$. We can setup the capacitor ratios of both of traditional and capacitor-sharing case; where we let that the C_F of the traditional case is equal to one be a reference. The one of the benefits of the capacitor-



(a)



(b)

Figure 3.19: The integrator output of a first-order SDM scaling: its probability occurrences of for under 3 dB of full scale input without signal scaling (a), and its probability occurrences for under 3 dB of full scale input with signal scaling (b).

Table 3.3: Capacitor ratio for traditional and capacitor-sharing case with scaling output range of the integrator of SDM.

Type	C_F	C_S	C_I
Traditional Type	1	$\frac{Y_{bar}}{V_S} = V_{dd}$	$\frac{2Y_{bar}}{V_S} = 2 \cdot V_{dd}$
Capacitor-Sharing Type	$\frac{1}{2}$	$\frac{Y_{bar}}{2V_S} = \frac{V_{dd}}{2}$	$\frac{2Y_{bar}}{V_S} = 2 \cdot V_{dd}$

In usually, $Y_{bar} = V_{dd}$ and $V_S = 1v(V_{pp.})$.

sharing type is reducing the input capacitor size at ideal consideration. Other one of the benefits is lesser harmonic distortions than traditional type due to the capacitor-sharing type has more better symmetrization for input capacitors. Another one benefit is that the capacitor-sharing type can ignore the common-mode level variations of the input signal while using this type can achieve a better linearity than traditional type one. The comparisons of the error due to capacitor mismatching and CM (common-mode) voltage unbalance between traditional type and capacitor-sharing one discussed with following, respectively.

In SC circuits, the gain factors are mapped into capacitor ratio. Though these relationships can be obtained with much more precision than the absolute values of the capacitor itself, they are not exempted from error during the fabrication process so that the gains differ from their nominal ratio. This kind of the mismatch error causes that the harmonics are generated which leads to degrading the SNDR. Presently, we will simulate that the appearance of the capacitor mismatch error by using Matlab-Simulink which also uses a mentioned first-order SDM frame which shows in Fig. 3.18. Assuming any Layout skills is not used, the standard deviations of the capacitor size as large as about 3% for worst-case in nowadays process technique. Therefore, we assume that the integrating capacitors (C_I) are varied by process and others are not, its PSDs of the simulation is exhibited in Fig. 3.20 with ideal case simulation. This figure shows that the similar performance of the SDM between C_I size of varying 3% and ideal case [16]. Hence, in continuously, we do not need considering the effects of the C_I variation.

Before the simulations for forced on input capacitors variations, we only consider the traditional case simulations for following discussion. The input capacitors variation can be assumed by two kinds: one is that the input capacitors of one side are both increased and the other side is on the contrary, the other is that the input capacitors of one side are not varied the same with each other and the other side is the same. These phenomena are shown in Fig. 3.21, they are indicated that the variations by the same direction are not important at the same side, however,

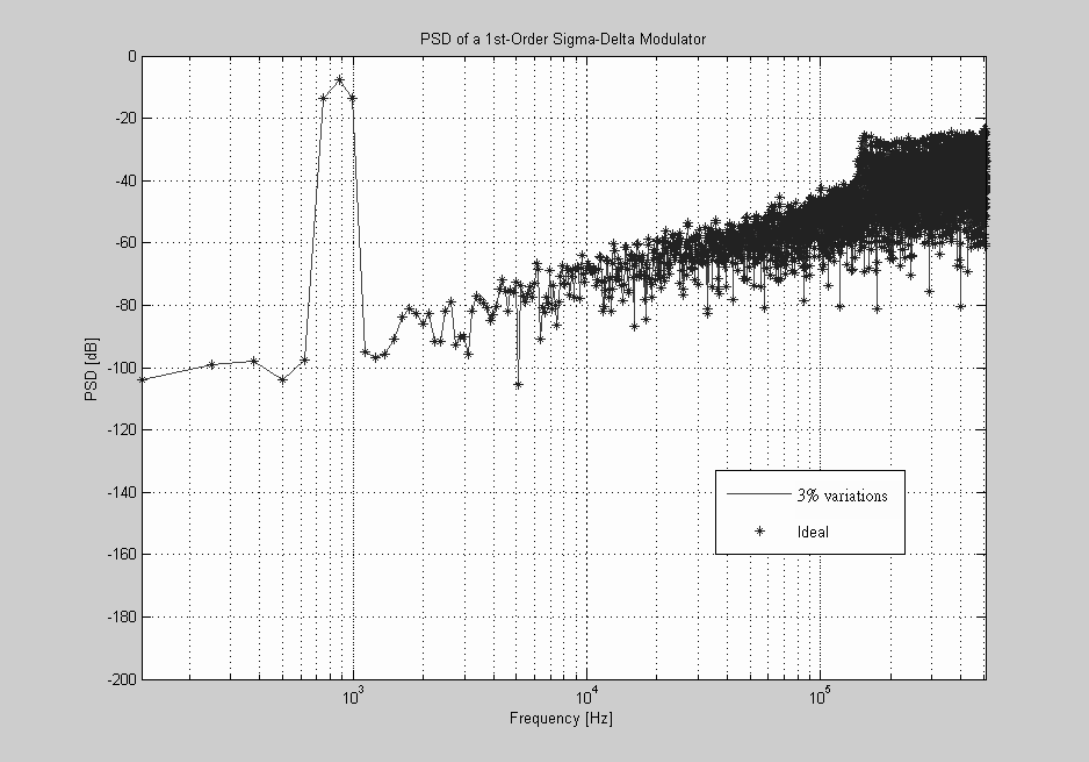


Figure 3.20: The PSDs of the SDM output compared in the process variation of integrating capacitors C_I for ideal-case and the variation of 3% case.

the process variations are not controlled. At the same time, the Fig. 3.21 aslo indicates the variations of difference directions at the same side that induces some harmonic tones to degrade the performance, thus, this kind variation are much more regarded. For showing in time domain, the results from that the output bit-streams of the quantizer output at the ideal case and the the variations of difference dimensions at the same side case pass through a 1024-order moving-average system show in Fig. 3.22 can be easily taken these difference. These phenomena are simulated at a variation of 3% is assuming here.

For these results, we also can make sense that the variation of the input signal common-mode level is like that the input- and feedback-capacitor are varied by different direction. It also induces some harmonic tones which is shown in Fig. 3.23. The common-mode level variation is assuming as a sinusoidal form of input signal frequency of two time with a amplitude of 1 mV and zero mean. For capacitor-sharing type, its performance is like as ideal cease because its input- and feedback-capacitors are always varied by one direction. At the same time, the input capacitors of the capacitor-sharing type are only storing the input differential-mode signal while it is skipping the input common-mode signal. Therefore, we can say that the capacitor-sharing type can achieve an excellent performance for anti-mismatch and anti-CM level variation.

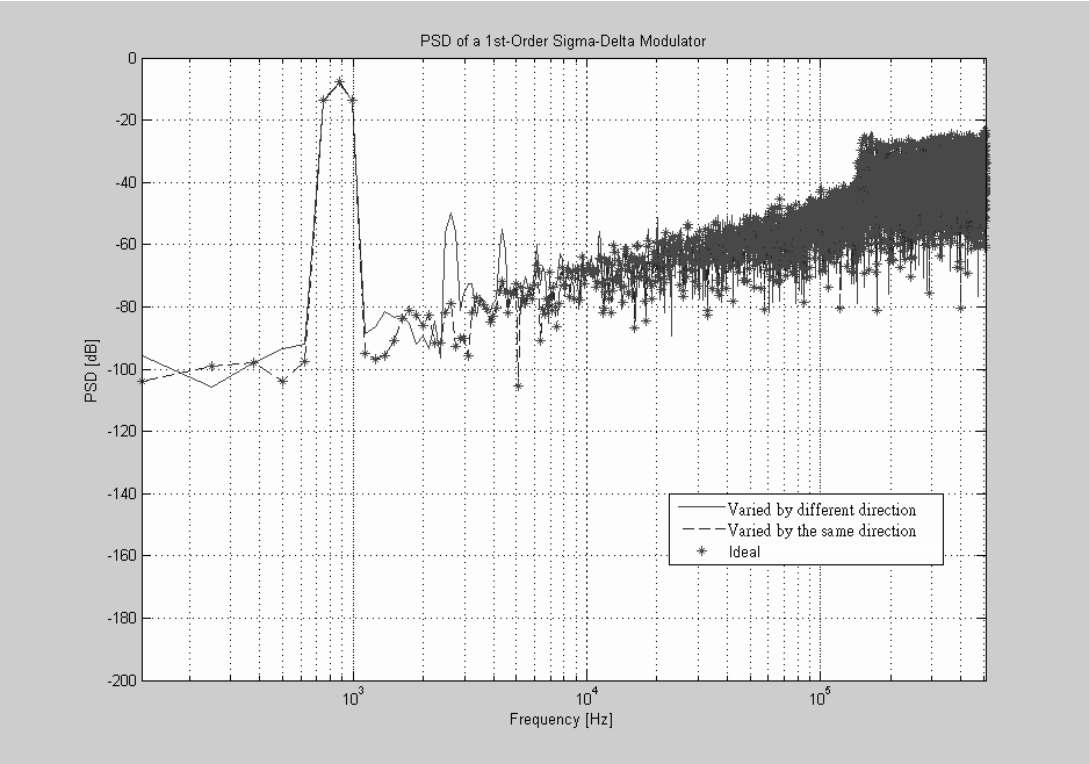


Figure 3.21: The PSDs of the SDM output compared in the process variation of the input- and feedback-capacitors; the variation of 3% is assumed for worst case.

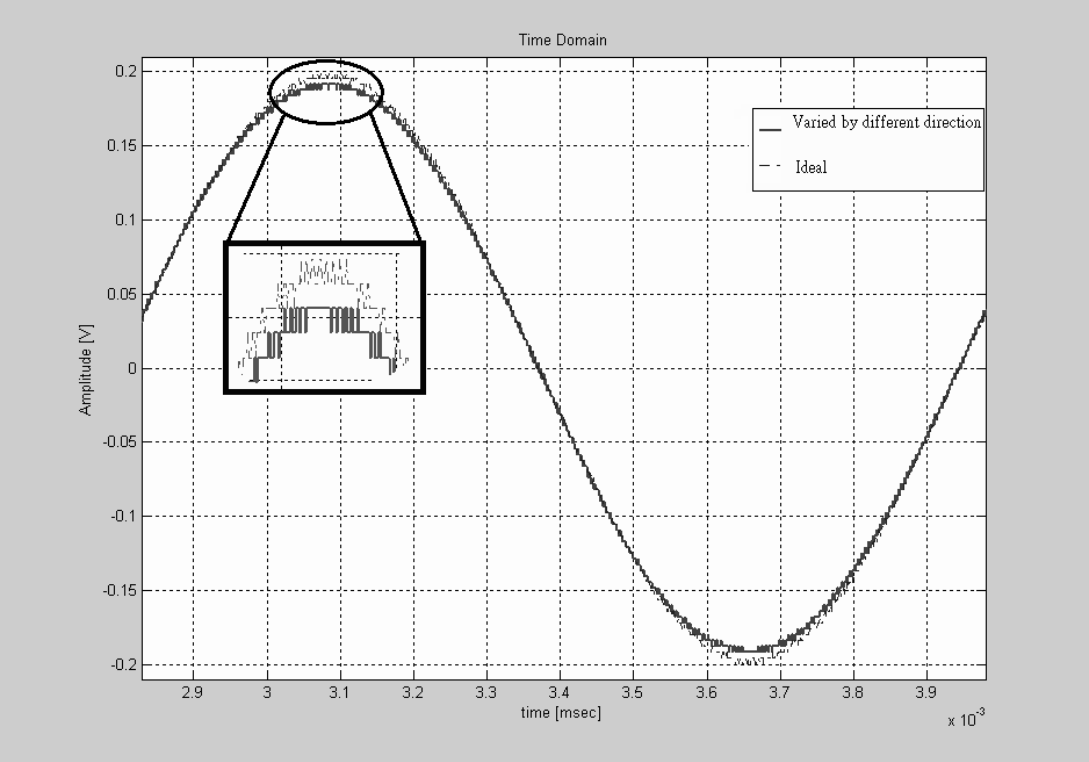


Figure 3.22: Analysis of the time domain: the bit-stream of the quantizer output pass through a moving-average system at the ideal case and the worst-case.

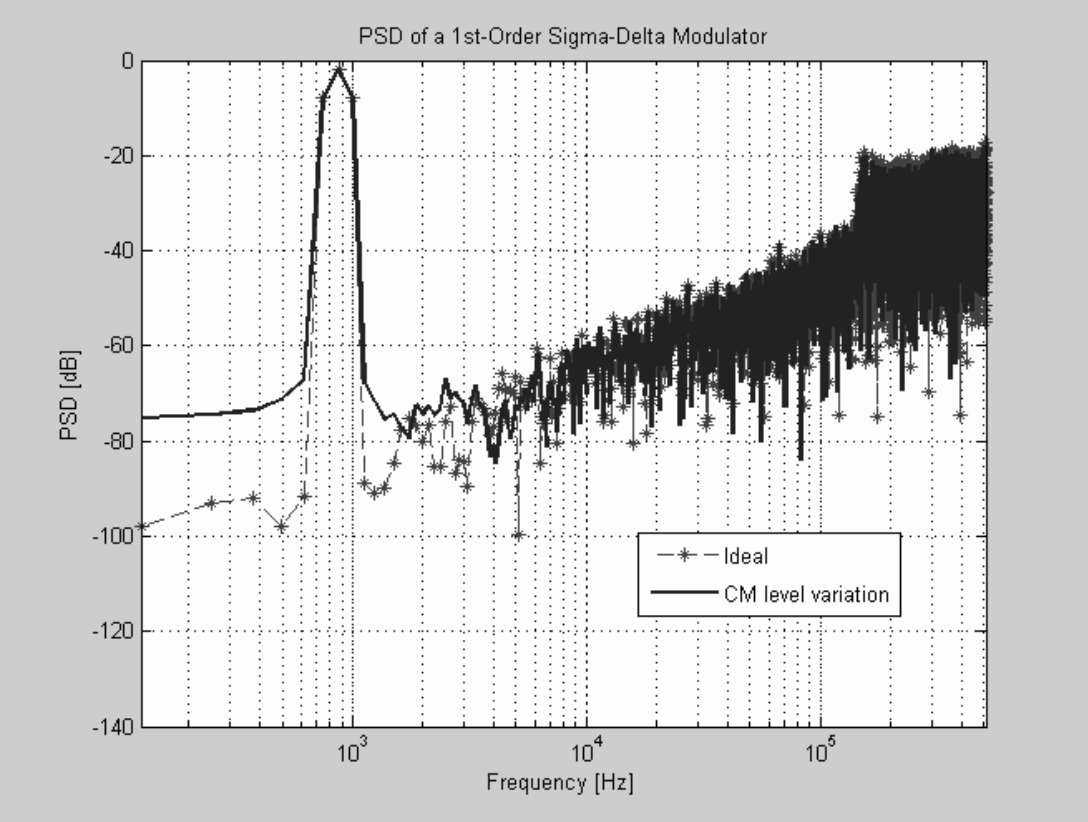


Figure 3.23: Analysis of the input signal common-mode level.

Continually, another error factor about capacitor is origin of voltage-dependence which also affects the SNDR of the SDM. Usually, this kind effect is easily neglected which leads to the SNDR degrade a amount. As the same as the mismatch error from process variations, a error due to the voltage-dependence of capacitor is similar as previous analysis; it also can be reduced by using capacitor-sharing type modulator.

Furthermore, for a consideration of an unbalance CM level between the input signal and circuit block, this affection can be also mathematical sorted from time sequences, this kind error as similar to mismatch of capacitors shows some harmonic tones in spectra; which is always appeared in using traditional type. In instinctively for using capacitor-sharing type, the unbalance CM level is not leading the harmonic emerged due to the both terminal of whose input capacitor are direct connected with a differential signal source, hence, the error from unbalance CM level is not considered here. However, a fine CM level definition always follows maximum swing for signal, although the CM level is not pondered in our work.

Consequently, to comparison between the traditional type and capacitor-sharing type, the capacitor-sharing type has better performance to against several issues as the mismatching,

capacitance of the voltage-dependence, and an unbalance CM level than traditional type due to the input capacitors are used by sharing. It means that the capacitor-sharing type has less considerations for design.

Chapter 4

Others Non-Idealities

4.1 Introduction

Up to now, we have explained CV-C and SDM circuits. However, these are not enough considered to ensure a fine system performance due to others non-ideality are proved to be sensitive to circuit. For any system considerations, the first stage of system is more important than others stage because the coming signal of system is always made distortion from non-ideality factors of the first stage which can lead to next stage input or modulator output immediately results in a performance degradation. For our using blocks (show in Fig. 2.3(b) and Fig. 3.17(b), those others non-ideality result from non-ideal OTA, reference voltage error, offset and hysteresis of comparator, and switch noise that will be discussed below. Another important issue for realization of modulator is the circuit layout which will be discussed in chapter 5, layout realizations are key issue for keeping system performance after foundry producing process.

4.2 Non-Ideal OTA

4.2.1 Actual Gain Effect

About a finite and non-linearity OTA gain effect in CV-C architecture presented in Chapter 2 which will not here again while it will only show the effect of the non-ideal $N_{TF}(z)$ of the chapter 4 (3.36). Where the A is the OTA gain, and the capacitor C_T and C_I are all of the input and parasitical capacitance, and integrating capacitors, respectively. When A is finite which leads to that the zero of the $N_{TF}(z)$ is slightly less than one so the magnitude of the $N_{TF}(z)$ at zero frequency is no longer zero at zero frequency. This demonstrated graphically in Fig. 4.1. The figure shows that the PSD of the shaped noise for an ideal OTA (infinite gain) and a real

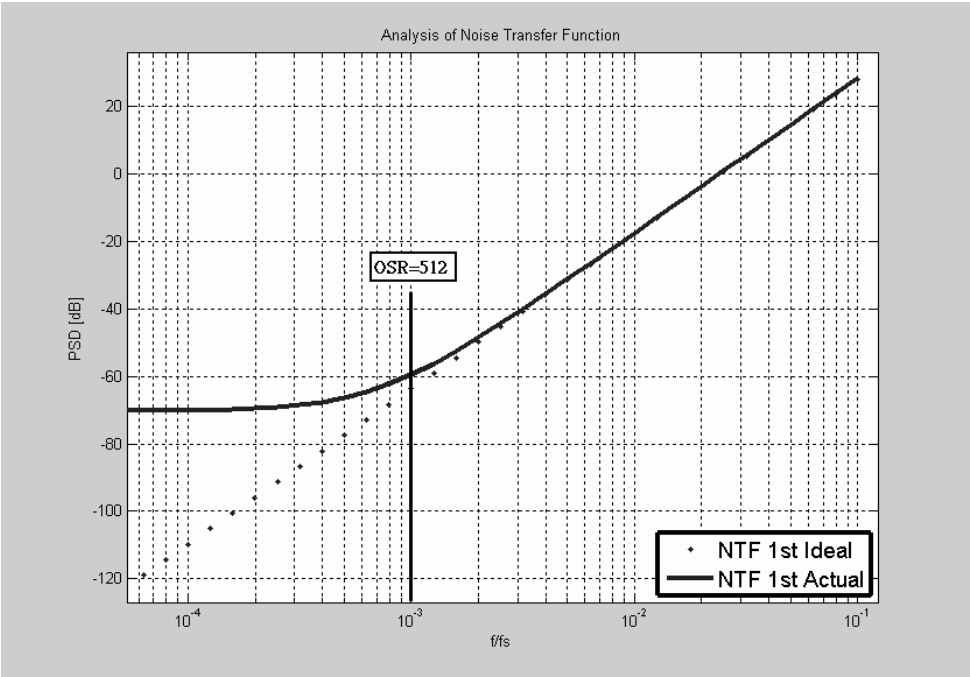


Figure 4.1: Noise shaping function with ideal infinite and actual finite OTA gain affecting.

OTA (finite gain). The quantization noise in the signal band f_0 is essentially the area under each curve up to frequency f_0. The finite gain curve levels off at low frequency as opposed to decline to zero in the infinite gain curve. This allows the integrator to pick up more quantization noise in the signal band while it causes the SNR degradation. Therefore, for obtaining enough SNR (more than $72dB$), the OTA gain A must be larger than $45dB$ at least when the OSR=512 which is easily found from Fig. 4.1 which is plotted from $N_{TF}(z)$ using MATLAB. Additionally, we consider again that the zero position of the $N_{TF}(z)$ from the (3.36). The zero near $z = 1$ results in the 3-dB break frequency being approximately equal to $1/(2\pi A)$ Hz/sample, where such unit is usually used and applied for normalization results in discrete-time signal system. Presently, we note that if the frequency band of interest, f_0, is less than $1/(2\pi A)$ Hz/sample since the quantization noise is flat equivalently the 3-dB break frequency level. The (4.1) shows that how much the OTA gain is enough.

$$A > \frac{f_S}{2\pi f_0} = \frac{OSR}{\pi} = \frac{512}{\pi} \simeq 45dB \tag{4.1}$$

We can sense that the results of the above comparison between the conditions of the actual case shown in Fig. 4.1 and the (4.1) are direct corresponded with each other. Of course, some approximations have been made here, such as having the 3-dB break frequency being sharp,

as well as allowing noise to be flat from DC to f_0. Consequentially, we will typically ensure that the OTA gain is at least two times the oversampling ratio, which is not usually a difficult to design.

As mentioned (2.5) in Chapter 2, this equation can show the gain requirement for the non-linear DC gain effect. Another method for considerations of the harmonic distortion in a SC integrator is shown here. In [17], the non-linear gain of amplifier is expressed by a non-linear transfer function between the input voltage and output voltage which is

$$V_o = \alpha_1 V_i + \alpha_2 V_i^2 + \alpha_3 V_i^3 + \alpha_4 V_i^4 + \alpha_5 V_i^5 \ \cdot \ \cdot \ \cdot \tag{4.2}$$

At the same time, it is well known that it is advantageous to utilize a fully differential opamp so that even order harmonic can be suppressed by common mode rejection ratio (CMRR). Therefore, we ignore the second order and only consider the third order term. The (4.2) is now reduced to

$$V_o = \alpha_1 V_i + \alpha_2 V_i^2 + \alpha_3 V_i^3 \tag{4.3}$$

Using numerical iteration technique, we can obtain an approximate solution for (4.3) as shown in (4.4). By definition, the DC gain can be written as $V_o/V_i \equiv A$ which like as (4.5).

$$\begin{aligned} V_i &= \frac{V_o - \alpha_3 V_i^3}{\alpha_1} \simeq \frac{V_o - (\alpha_3/\alpha_1^3) V_o^3}{\alpha_1} \\ &= V_o \frac{1 - (\alpha_3/\alpha_1^3) V_o^2}{\alpha_1} \end{aligned} \tag{4.4}$$

$$\begin{aligned} A &= \frac{\alpha_1}{1 - (\alpha_3/\alpha_1^3) V_o^2} \simeq A_0 (1 + (\alpha_3/\alpha_1^3) V_o^2) \\ &\triangleq A_0 (1 + \gamma_2 V_o^2) \end{aligned} \tag{4.5}$$

where $A_0 = \alpha_1$ and $\alpha_3/\alpha_1^3 = \gamma_2$ are used. By application for these results, a circuit configuration shows in Fig. 3.17(b) whereas the feedback path is not considered here. The charge conservation equation is shown in

$$C_I(1 + 1/A)[V_o(n) - V_o(n-1)] = -2C_S[V_o(n)/A + V_S(n - 1/2)] \tag{4.6}$$

The above equation indicates that the dependent of the DC gain on the output voltage will result in harmonic distortion (HD). Therefore, the difference equation is transformed into a differential equation[18]. e.g.,

$$V(n) - V(n-1) \Longleftrightarrow T\frac{dV(t)}{dt} \tag{4.7}$$

where T is the clock period. The (4.6) could not only be transformed but also the $V_o(t)/A(t)$ can be approximated by $V_o(t)(1-\gamma_2 V_o^2(t))/A_0$ since γ_2 is small. The evolution equation is shown as

$$C_I T\frac{dV_o(t)}{dt}[(1+1/A_0)-\gamma_2 V_o(t)^2/A_0] = -2C_S[V_o(t)(1-\gamma_2 V_o^2(t))/A_0 + V_S(t)] \tag{4.8}$$

This equation describes the dynamic non-linear behavior of the integrator with DC gain non-linearity. When an input takes the signal following form

$$V_S(t) = V_{in}\cos(\omega t) \tag{4.9}$$

then the output signal can be written as

$$V_o(t) = \sum_j V_k \cos(k\omega t + \phi_k) \tag{4.10}$$

By definition, the kth order harmonic distortion HD_K is equal to V_k/V_1. The value of V_k can be found with the help of the Volterra Series theory.

$$V_k = \frac{1}{2^k-1}\frac{|\zeta_k|}{|\zeta_1|}V_{in}^k \tag{4.11}$$

$$\phi_k = arg(\zeta_k) \tag{4.12}$$

where ζ_k is the coefficient appearing in following,

$$V_o(t) = \sum_k \zeta_k e^{jk\omega t} \tag{4.13}$$

where $V_o(t)$ is the output signal when a hypothetical input signal $V_i = e^{j\omega t}$ is applied to the integrator. Inserting the $V_o(t)$ and $V_i = e^{j\omega t}$ into (4.8) results in a simple algebra equation. Arraying the coefficients of the algebra equation is

$$\begin{aligned}
\zeta_1 &\simeq \frac{1}{2\pi}\frac{2C_S}{C_I} \\
\zeta_2 &= 0 \\
\zeta_3 &= \frac{6j\pi + 2C_S/C_I}{6j\pi A_0}\gamma_2\zeta_1^3
\end{aligned} \tag{4.14}$$

Therefore, the corresponding HD coefficients are

$$\begin{aligned}
HD_2 &= 0 \\
HD_3 &= \frac{\gamma_2}{16\pi^2 A_0}\left(\frac{2C_S}{C_I}\right)V_{in}^2
\end{aligned}$$

Consequentially, it is shown that a large DC gain is essential to minimize the DC gain non-linearity and a smaller value of input capacitor size compared to the integrating capacitor is helpful to reduce the 3rd order harmonic distortion[19].

4.2.2 Slew-Rate Limiting And Finite Bandwidth

Different from the static error (e.g. gain error...etc) is the dynamic error whose settling error is considered from the previously ideal equation as (2.6) and (3.39). The settling behavior may have two parts: slew-rate limit and linear settling. To achieve a maximum clock rate which must suffer from slew-rate due to the slew-rate limit prolongs the total settling time. Usually, the slewing time, t_{slew}, cost about a clock periodic time of 0.1 percentage. If the slew-rate limitation does not affect here, as mention above equations can be rewritten to include this constant gain error of the settling results in

$$\Delta V_o^{'} = \frac{2\Delta C_S}{C_A}(1 - e_{rr,settle})V_{dd} \tag{4.15}$$

$$Y_{bar}(z) = -\frac{C_S}{C_F}z^{-1/2}V_S(z) + \frac{C_I}{2C_F}(1 - e_{rr,settle})(1 - z^{-1})V_o(z) \tag{4.16}$$

$$e_{rr,settle} = exp\left(-\frac{t_{settle}}{\tau}\right) \text{ where } \tau = \frac{1}{2\pi f_{-3dB}} = \frac{1}{2\pi f_u \beta} \tag{4.17}$$

where β, f_u, f_{-3dB}, and t_settle are the feedback factor of CV-C or integrator, the OTA unity gain frequency, the frequency at the closed-loop circuit gain degraded $3dB$, and the time for settling, respectively. For complete settling requirement, the f_u be much larger than the sampling frequency, f_s. Thus, to achieve N-bit resolution, the $e_{rr,settle}$ must be less than $1/2^{N+1}$ [12, 10] which requires

$$f_u > \frac{0.69(N+1)}{2\pi\beta \cdot t_{settle}} \tag{4.18}$$

where the t_{settle} is usually set by $0.3/f_s$. The totally maximum delay can be estimated by t_d=$t_{slew} + t_{settle}$=$0.4/f_s$ in a clock of duty-cycle 50% while the remained time is $0.1/f_s$ which be a margin for using a non-overlap clock whose duty-cycle less than 50%. The (4.18) can be a design criterion for unit gain frequency of OTA in the CV-C. About used that in the first-order SDM, the settling error can be tolerated because the integrator is directly followed by a comparator. Hence, the incomplete settle is not more important for designing the unit gain frequency of OTA in first-order SDM.

4.3 Reference Voltage Error

The imperfect reference voltages due to finite inductance and the finite capacitance of the reference line lead to a supply current spike will result in reference ringing can cause the non-linear phenomena in SDM whereas the reference voltage is the power supply voltage in our work. The supply voltage ringings from sampling-induced and OTA-induced lead to two non-linear error appearances. Would let the non-linear occurrence understood easily, the supply voltage ringing can be made several assumptions in order to make the problem tractable. The first assumption is the power supply ringing can be modeled by a linear differential equation, the second one is the power supply voltage is only disturbed during the sampling period, the third one is the ringing repeats itself in every sampling period, and the fourth is the power supply voltage is restored to its stable value at the end of every sampling period. Whereas the third and the fourth assumptions imply that the settling error at the end of the sampling period is a constant and dependent on neither any others error nor the input signal. Form [19] indicates, the sampling-induced supply voltage error can be treated as a gain error which can be easily calibrated out, hence this error does no contribute to the overall nonlinearity of the SDM. Also according to [19], the OTA-induced reference error is an odd symmetrical function with zeroes occurring at zero input, and the lower and upper limits of the input. Which also indicates that the error is quadratically proportional to the reference voltage. Whose nonlinearity shape resembles that resulting from the non-linear settling.

4.4 Comparator Forethought

In this work, the comparator serves as a one bit quantizer and generates a stream of digital outputs. In a practical comparator, it has the intrinsic offset voltage and device noise which can be treated as an additive noise superimposed on the quantization noise which likes as an ideal comparator is replaced by an additive white noise source in the linear model. The comparator hysteresis can also be modeled as additive white noise[20]. This means that the non-ideality of the comparator can be reduced in the signal bandwidth due to the noise-shaped.

4.5 SC Circuit Noise

The output voltage of a SC circuit is always contaminated by noise, originating from a variety of sources. This noise is much larger than what is usually found in comparable active-RC filters, and hence it is important to understand its origin and dependence on circuit parameters.

There are four main sources of noise in a SC circuit:

1. Charge injection noise.

2. Clock feed-through noise.

3. Thermal and flicker (1/f) noise generated in the switches and OTA.

4. Noise coupled directly or capacitively from the clock lines, power lines and ground lines, and from the substrate.

The first of these noise sources can not be considered due to there are four kinds of clock phase for switches in SC circuit (Fig. 4.4). Where P_1, P_{d1}, and P_2, and P_{d2} lead to that the switch's charge can not inject into sampling capacitor. Furthermore, P_{d1} and P_{d2} are transiting later than P_1 and P_2, respectively, and P_1 and P_{d1} are inverting with P_2 and P_{d2}. That use to avoid the charge injection noise method is called bottom-plate sampling. In additionally, we can use transmission gate to reduce charge injection noise. The second noise is generated by capacitive coupling of the clock signal from the parasitic capacitors of switch into signal path. There are dual method to reduce the effect that is using transmission gate or dummy switch, and performing the processing circuit in fully differential type. This kind of effect is like a constant offset cancelled by fully differential circuits.

Before we investigate the third noise induced by switch and OTA, we must to sensing that noise effects are not only affected by thermal noise but the 1/f noise is also affecting. In generally, the 1/f noise is meaning that it is generated from the OTA. Because the flicker noise of the OTA is the dominating. But it is can be reduced by CDS technique that is introduced in the Table 3.1 and Table 3.2. In here, we can discuss the overall effect of the CDS technique in a transfer function as

$$\begin{aligned} H_{CDS}(z)|_{z=e^{2\pi f/f_s}} &= 1 - z^{-1/2} \\ &= e^{(-j\pi f)/(2f_s)} 2j \sin(\frac{\pi f}{2f_S}) \end{aligned} \tag{4.19}$$

In (4.19), the H_{CDS} is like a high-pass filter; this function suppresses noise not only at DC, but also at low frequencies as well as around the frequencies $2f_S$, $4f_S$,..., where f_S is the clock

frequency. Hence, for the usual case when $f \ll f_S$, the $1/f$ noise is essentially eliminate near $f = 0$ by the CDS technique (Fig. 4.2)[21, 22, 23]. So, the consideration of $1/f$ noise is ignore here. Consequently, the thermal noises from switches and OTA are discussed in this subsection. The fourth noise will be discussed in following section. Furthermore, it not only has four kinds of noise to affect circuit, but the aperture jitter due to the switch is not actually tuned off while the end of the sampling time reached, or the clock jitter that also affects. However, these affecting results can be disregarded as a result of the oversampling technique is operated. Especially, the OSR is equal to 512 in this work.

Firstly, we apply some noise analysis skills[24, 25, 26, 18] to calculate the equivalent noise at the output of SC integrator, and use a simple SC circuit to present the amount of thermal noise. From some backgrounds, We know that the overall thermal noise PSD $S^T(f)$=$S^d(f)$+$S^{S/H}(f)$ since the direct thermal noise PSD $S^d(f)$ and sample-and-hold thermal noise PSD $S^{S/H}(f)$ of a SC circuit are essentially un-correlated. So, we can compute these noise PSD by each.

To calculate the direct thermal noise PSD $S^d(f)$, we note that when Clk="H" or "1", the simple SC stage and its equivalent circuit is shown in Fig. 4.3 where $\overline{v_{n,s}^2}$ is the equivalent thermal noise value of on-resistance R_{on}, and the $two\text{-}sided$ $(-\infty \leq \omega \leq \infty)$ PSD $S(f)$ of v_C is obtained as follows

$$S(f) = \frac{\overline{v_{n,s}^2}}{\Delta f} = 2kT \left| \frac{1/j\omega C}{R_{on} + 1/j\omega C} \right|^2 = \frac{2kTR_{on}}{1 + (2\pi f T_{on})^2} \tag{4.20}$$

The mean-square value of v_C for all frequencies is hence

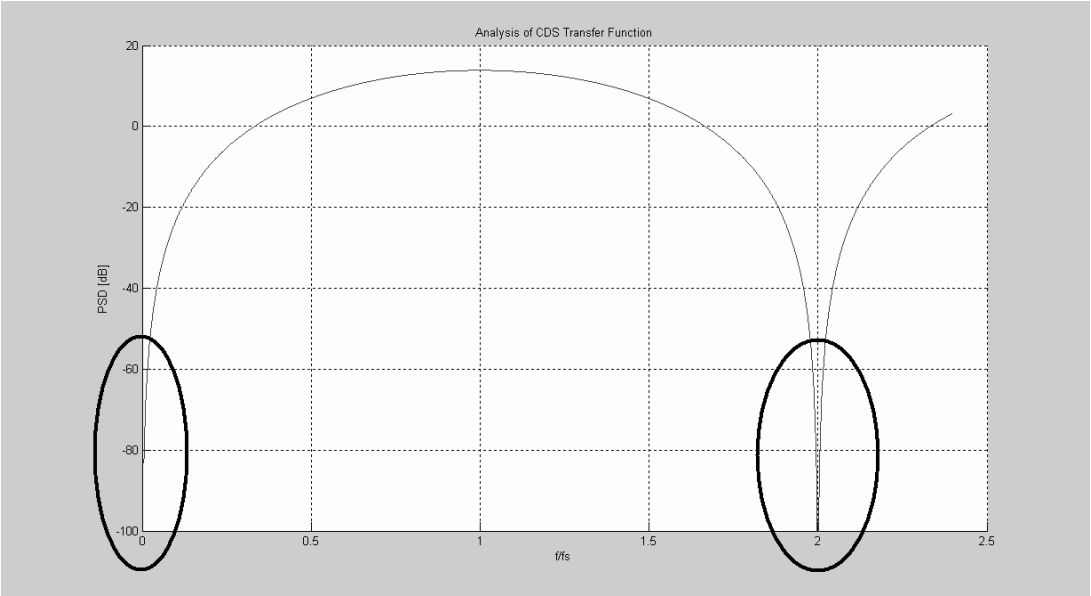
$$\overline{v_C^2} = \int_{-\infty}^{\infty} S(f)df = \frac{22kTR_{on}}{2\pi} \int_0^{\infty} \frac{1}{1 + \omega^2 T_{on}^2} d\omega = \frac{4kTR_{on}}{2\pi} \frac{\pi}{2T_{on}} = \frac{kT}{C} \tag{4.21}$$

where T_{on}=$R_{on}C$, k and T are the time constant of the switch during its "on" time, the Boltzman constant (e.g. $1.38 * 10^{-23}$) and the absolute temperature (e.g. room temperature $27\ ^\circ C$+273).

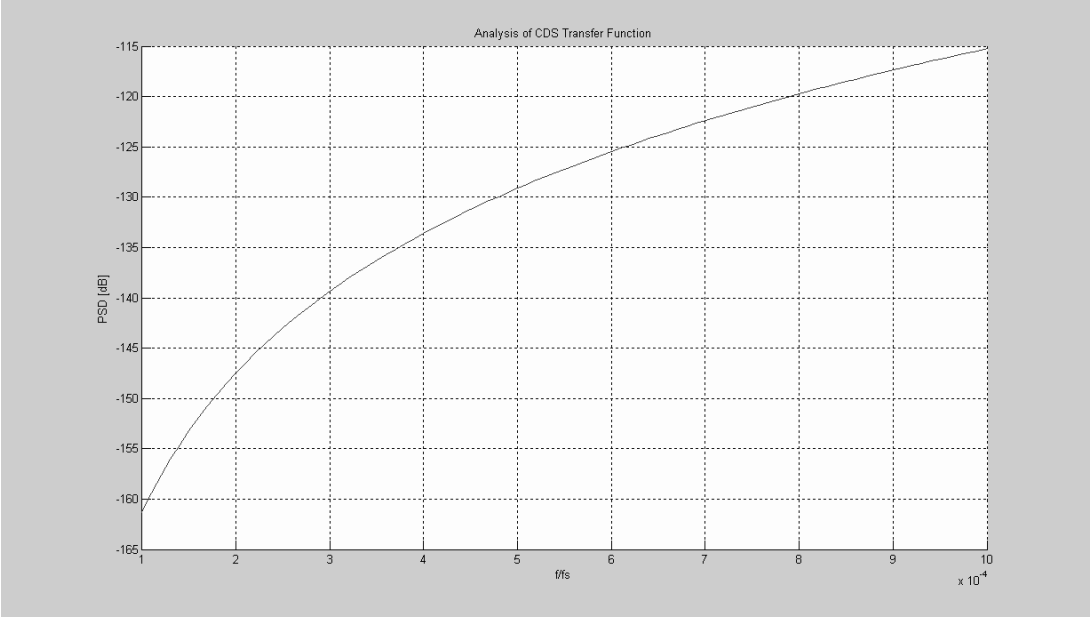
However, the thermal noise of resistor R_{on} feeds the capacitor C only during the duty cycles when Clk="H"or "1"; hence the direct thermal noise power v_C^d of v_C must be multiplied by $0 < m < 0.5$, giving as

$$\overline{(v_C^d)^2} = \frac{mkT}{C} \tag{4.22}$$

At the same as, the direct thermal noise PSD $S^d(f)$ of v_C^d is $mS(f)$, where $S(f)$ is given by (4.20).



(a)



(b)

Figure 4.2: White noise after correlated double sampling: (a) the over view and (b) zoom in for the lower frequencies region.

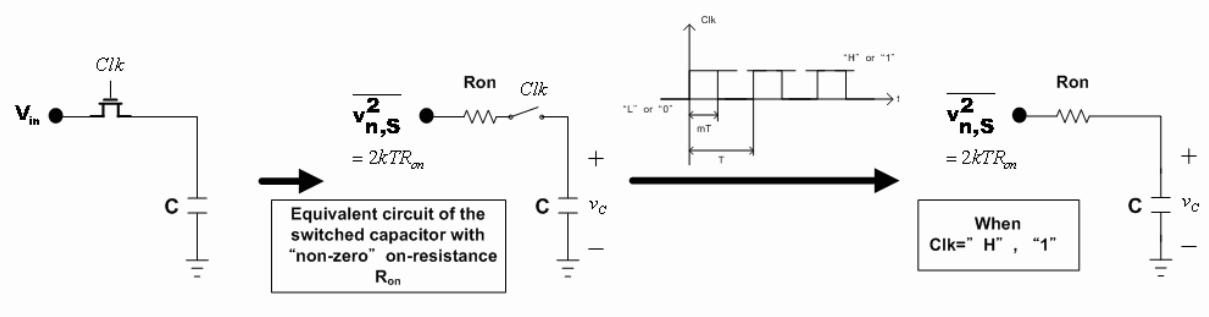


Figure 4.3: Thermal noise in a turn-on switch.

Next, to calculate the PSD $S^{S/H}(f)$ of the sampled-and-held wave $v_C^{S/H}(t)$ will be given. As the sample-and-hold technique background, we know that the $v_C^{S/H}(t)$ is obtained by sampling the direct thermal noise $v_C^d(t)$ at every constant time period T=$1/f_S$ as mT, $mT+T$, $mT+2T$, and so on, and holding these samples for intervals of x=$(1-m)T$. By using an argument for sample-and-hold process refer to that presented in signal processing books and papers. At the sample-and-hold mode, we can show that $S^{S/H}(f)$ and $S(f)$ are related by as below, where the values of $S(f)$ are also un-correlated and the same as (4.20).

$$S^{S/H}(f) = \frac{\overline{(v_C^{S/H})^2}}{\Delta f} = \left(\frac{x}{T} \cdot \frac{\sin(\pi x f)}{\pi x f}\right)^2 \sum_{k=-\infty}^{\infty} S(f - k f_S) \tag{4.23}$$

From (4.21), we know that a thermal noises cross a RC low-pass filter, the total area under the low-pass frequencies response curve is kT/C. Now, the curve may be approximated by the rectangle which means that the rectangle response is an ideal low-pass frequencies response. The bandwidth associated with the idealized response is $-f_B \sim f_B$ where f_B=$1/(4T_{on})$. According to (4.23), this response must be shifted by integer multiples of f_S, and the resulting replica added. From these theoretical results, some practical assumptions must also be made which are like as the switching transistor in the circuit Fig. 4.3, its ratio W/L is presumably chosen such that it makes a (nearly) complete charging of C from the input voltage V_{in} and lets the charging time constant is T_{on}=$R_{on}C$, for a 0.1% settling accuracy possible during the time interval $0 \le t \le mT$, where $0 < m < 0.5$ was used. In practice, usually $f_B \ge 5f_S$. Now, we can add all the un-correlated replicas according to (4.23), hence in general, the $S^{S/H}(f)$ can be rewritten as

$$\begin{aligned} S^{S/H}(f) &= \left(\frac{x}{T}\frac{\sin(\pi x f)}{\pi x f}\right)^2 \sum_{k=-f_B/f_S}^{f_B/f_S} S(f - k f_S) \\ &= \left((1-m)\frac{\sin((1-m)\pi f/f_S)}{(1-m)\pi f/f_S}\right)^2 \frac{2f_B}{f_S} S(f) \end{aligned} \tag{4.24}$$

In this thesis, we use the system in low-frequency range where $f \ll f_S$, the two-sided S/H noise power density is

$$\begin{aligned} S^{S/H}(f) &= \left((1-m)\frac{\sin((1-m)\pi f/f_S)}{(1-m)\pi f/f_S}\right)^2 \frac{2f_B}{f_S} S(f) \\ &\simeq (1-m)^2 \frac{1}{2f_S R_{on} C} 2kTR_{on} \\ &= (1-m)^2 \frac{kT}{f_S C} \end{aligned} \tag{4.25}$$

where $(2f_B/f_S)S(f) \simeq kT/(f_S C)$ disperse in the base-band $[-f_S/2, f_S/2]$ due to the sum of all replicas is kT/C, while the two-sided direct noise power density is for low frequencies

$$S^d(f) = mS(f) \simeq 2mkTR_{on} \tag{4.26}$$

Therefore, the total thermal noise of the switched capacitor can be given as

$$S^T(f) = S^d(f) + S^{S/H}(f) = 2mkTR_{on} + (1-m)^2 \frac{kT}{f_S C} \tag{4.27}$$

In fact, we can conclude that the S/H noise dominates the noise effect at low frequencies through two views. One is the noise ratio which is r=$S^{S/H}(f)/S^d(f) \simeq (1-m)^2/(2mf_S R_{on}C)$; Since, for a 0.1% settling accurately condition, $mT \geq 7T_{on}$. For m=0.4, we can obtain the $r \simeq 8$. For this thesis, the other one is that the corner frequency of a MOS's noise distribution is less than $f_S/2$, the $1/f$ noise contributes significantly only to the direct noise in the base-band $[-f_S/2, f_S/2]$,hence it is usually much less important than the S/H noise and the power of the S/H noise $\overline{(v_C^{S/H})^2}$ is of the same order of magnitude as that of the direct noise $\overline{(v_C^d)^2}$, its PSD is mostly at low frequencies due to the sin^2x/x^2 factor in $S^{S/H}(f)$ while that of v_C^d is spread over a much wider frequency range. Thus, the PSD of the direct noise occupies a broad frequency band while that of the S/H noise is a narrow-band spectral density.

The concepts of the preceding analysis can now be extended to the complete integrator of the first-order SDM of a capacitor-sharing type which is shown in Fig. 4.4(a). Let us center on Fig. 4.4(b), which corresponds to the sampling phase. During this phase the noise from the switches S_1 and S_3 is sampled by the input capacitors C_S and C_F, respectively. Applying the previous presumptive results, the noise power spectral densities in both capacitors are

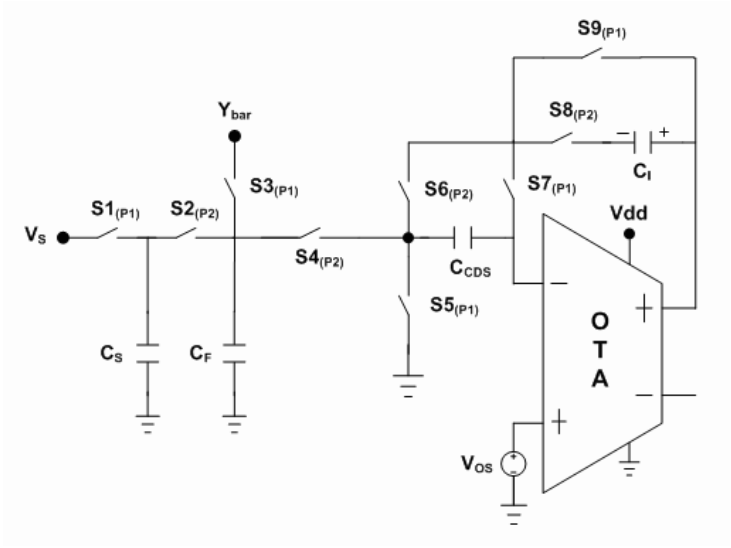
$$S_{C_S,1}(f) = 4mkTR_{on} + (1-m)^2 \frac{kT}{f_S C_S} \tag{4.28}$$

$$S_{C_F,1}(f) = 4mkTR_{on} + (1-m)^2 \frac{kT}{f_S C_F} \tag{4.29}$$

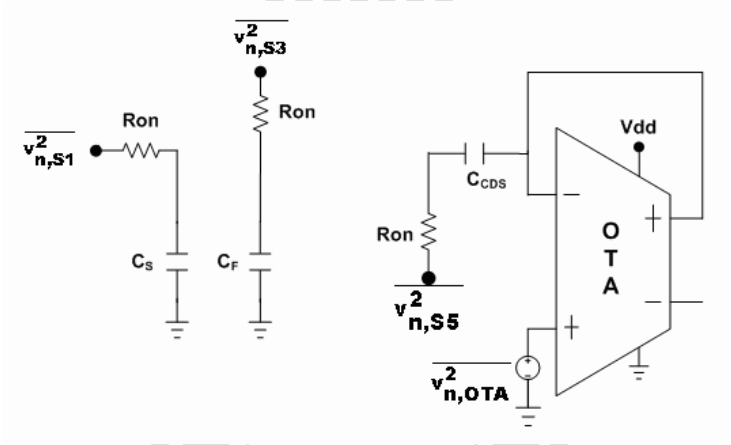
where both of the noise power spectral densities in both capacitors are un-correlated. However, the switches, S_1 and S_2, are never connected by a direct path to the output, therefore the direct noise of these switches is not considered. Hence, we can simply the expression of the total thermal noise of the switched capacitor as resulting in

$$S_{C_S,1}(f) \simeq (1-m)^2 \frac{kT}{f_S C_S} \tag{4.30}$$

$$S_{C_F,1}(f) \simeq (1-m)^2 \frac{kT}{f_S C_F} \tag{4.31}$$



(a)



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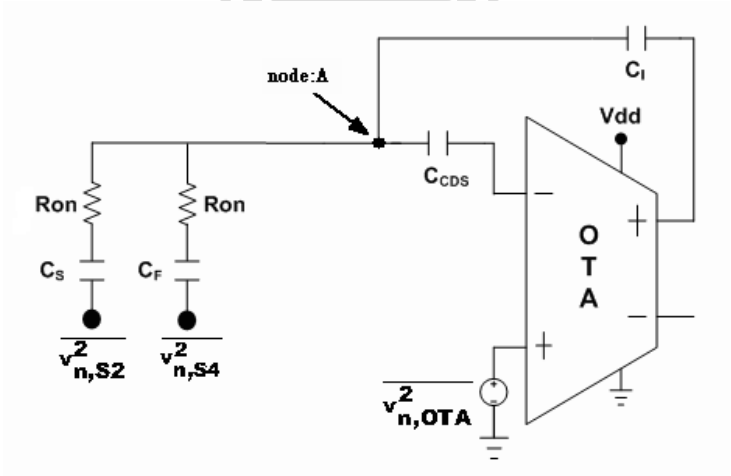


(c)

Figure 4.4: Model for the noise analysis of SC integrator: (a) two-branch SC integrator, (b) during the sampling phase, and (c) during the integration phase.

Consideration of these, we can use superposition to equivalent the power spectral density in C_S will be

$$S_{eq,C_S,1}(f) = (1-m)^2 \left(1 + \frac{C_F}{C_S}\right) \frac{kT}{f_S C_S} \tag{4.32}$$

Continuously, we consider that the noise densities correspond to integration phase which is shown in Fig. 4.4(c). During this phase the noise from the switches S_1 and S_3 is sampled by the input capacitors C_S and C_F, respectively, and the noise of OTA is also sampled by both of the input capacitors C_S and C_F. Where the noises of the OTA consist of three parts: thermal noise of the gate resistance of MOS R_G, $1/f$ noise and thermal noise from channel of MOS. However, the thermal noise of R_G can be ignored by appropriate purpose of design and layout and the $1/f$ noise is disregarded due to using CDS technique. Thus, we now only consider the contribution of thermal noise from channel of MOS. In usual case for OTA has a MOSFET input stage, the input current noises can often be ignored in low frequencies since their values are small; the input voltage noises of the OTA can only be considered and be modeled by noise source $\overline{v_{n,OTA}^2}$=$2kT(2\alpha/(3g_m)) \triangleq 2kTR_{eq}$, shown in Fig. 4.4(b) and Fig. 4.4(c). Where α is the effective number of devices that contribute to the input referred noise, g_m is the transconductance of the input transistors, and the R_{eq} is the hypothetical resistor which would generate as much thermal noise.

From discussion of above, the integrator input referred noise contain some broad-band direct noise, and also some S/H noise due to noise charges trapped on the switched capacitors, C_S and C_F when both of them are disconnected from a noise source. To calculation of these PSDs from circuits of Fig. 4.4(c) is straightforward obtained from previous hypothesis that are computed by superposition theory. Now, the direct PSD of the OTA input referred noise is obtained as (4.33) there are some assumed for OTA (i.e, $A_0 \gg 1$ and $s \ll s_1$. Where The OTA will be described by the one-pole model, so that its output-input relation is given as (4.34).

$$\begin{aligned} S_{eq,C_S}^d(f) &= 2mkT \left\{ \left[1 + \left(\frac{C_F}{C_S}\right)^2\right] R_{on} + \left[\left(1 + \frac{C_A}{C_I}\right)\frac{C_I}{C_S}\right]^2 R_{eq} \right\} \\ &= 2mkT \left\{ \left[1 + \left(\frac{C_F}{C_S}\right)^2\right] R_{on} + \left(\frac{C_T}{C_I}\frac{C_I}{C_S}\right)^2 \frac{2}{3g_m} \right\} \\ &= 2mkT \left\{ \left[1 + \left(\frac{C_F}{C_S}\right)^2\right] R_{on} + \left(\frac{C_T}{C_S}\right)^2 \frac{2}{3g_m} \right\} \end{aligned} \tag{4.33}$$

$$A_v(s) = \frac{A_0}{1 + s/\omega_1} \tag{4.34}$$

In Fig. 4.4(c), we can write the output-input relation expression of the closed-loop circuit in (4.35).

$$\begin{aligned} A_v, cl(s) &= \frac{A_0/(1 + A_0\beta)}{1 + s/[(1 + A_0\beta)\omega_1]} \simeq \frac{1/\beta}{1 + s/(A_0\beta\omega_1)} \\ &= \frac{1/\beta}{1 + s/(\beta\omega_u)} \end{aligned} \tag{4.35}$$

where the β is the feedback factor of the closed-loop circuit, β=$C_I/(C_I$+C_S+C_F+$C_P)$ $\triangleq$ C_I/C_T whereas the C_P is the parasitical capacitor of the node A indicated in Fig. 4.4(c), C_T is the sum of all capacitors, the ω_u is the unit-gain frequency of the OTA which is also equal the gain-bandwidth product as $A_0\omega_1$, and the C_A is the sum of the input capacitors as C_A=$(C_S + C_F + C_P)$. As mentioned earlier, the S/H noise is caused by the sampling-and-holding operation which causes an aliasing of the spectrum, and concentrates the noise power in the base-band. Therefore, a wide bandwidth will cause the more serious the aliasing effect. For Fig. 4.4(c), the R_{on}-C_S, R_{on}-C_F section, and the finite unity-gain bandwidth ω_u of the OTA contribute to the band-limiting operation. Usually, the OTA band limits the signal since $\omega_u < \omega_B$=$\pi/(2R_{on}C_S)$. Hence, the S/H PSDs is

$$\begin{aligned} S_{eq,C_S}^{S/H}(f) &= 2kT\frac{2f_{B,OTA}}{f_S}\left[1 + \left(\frac{C_F}{C_S}\right)^2\right]\left[(1-m)^2(R_{eq} + R_{on})\right] \\ &= (1-m)^2\left[1 + \left(\frac{C_F}{C_S}\right)^2\right]\frac{kTg_m}{f_S C_A}\left(\frac{2}{3g_m} + R_{on}\right) \end{aligned} \tag{4.36}$$

where the $f_{B,OTA}$ is the equivalent noise bandwidth of the closed-loop circuit. Here, the term containing g_m in (4.36) is directly proportional to $S_{eq,C_S}^{S/H}(f)$, which is important in reducing the aliasing noise and enhancing the S/H noise. Hence, g_m should be chosen as low as possible while still allowing the adequate settling of the OTA due to ω=g_m/C_L is directly relationship with settling accuracy where the C_L is the loading capacitor on the both sides of OTA output port.

Supposing that all the noises are not correlated, the spectral density of the input referred

noise can be approximated by

$$\begin{aligned}
S_{eq,C_S,total}(f) =& S_{eq,C_S,1}(f) + S^{S/H}_{eq,C_S}(f) + S^{d}_{eq,C_S}(f) \\
=& (1-m)^2 \left(1+\frac{C_F}{C_S}\right)\frac{kT}{f_S C_S} + \\
& (1-m)^2 \left[1+\left(\frac{C_F}{C_S}\right)^2\right]\frac{kTg_m}{f_S C_A}\left(\frac{2}{3g_m}+R_{on}\right) + \\
& 2mkT\left\{\left[1+\left(\frac{C_F}{C_S}\right)^2\right]R_{on} + \left(\frac{C_T}{C_S}\right)^2\frac{2}{3g_m}\right\} \\
=& (1-m)^2\frac{kT}{f_S C_S}\left\{\left(1+\frac{C_F}{C_S}\right) + \left[1+\left(\frac{C_F}{C_S}\right)^2\right]\frac{g_m C_S}{C_A}\left(\frac{2}{3g_m}+R_{on}\right)\right\} + \\
& 2mkT\left\{\left[1+\left(\frac{C_F}{C_S}\right)^2\right]R_{on} + \left(\frac{C_T}{C_S}\right)^2\frac{2}{3g_m}\right\} \qquad (4.37)
\end{aligned}$$

From the previous presentation (i.e, for m=0.4, $r \simeq 8$) indicated that the direct noise is usually much less important than the S/H noise due to the S/H noise density $S^{S/H}(f)$ is mostly at low frequencies while the direct noise density $S^{d}(f)$ is spread over a much wider frequency range. Hence, we can ignore the direct noise part from (4.37) which is adapted as

$$S_{eq,C_S,total}(f) = (1-m)^2\frac{kT}{f_S C_S}\left\{\left(1+\frac{C_F}{C_S}\right) + \left[1+\left(\frac{C_F}{C_S}\right)^2\right]\frac{g_m C_S}{C_A}\left(\frac{2}{3g_m}+R_{on}\right)\right\} \qquad (4.38)$$

For this thesis, we know that the signal bandwidth is $[-f_0, f_0]$. Thus, the total power of the thermal noise after decimation is calculated by integrating $S_{eq,C_S,total}(f)$, given by (4.39),

$$\begin{aligned}
P_{th,total} &= \int_{-f_0}^{f_0} S_{eq,C_S,total}(f)df \\
&= (1-m)^2\frac{2f_0kT}{f_S C_S}\left\{\left(1+\frac{C_F}{C_S}\right) + \left[1+\left(\frac{C_F}{C_S}\right)^2\right]\frac{g_m C_S}{C_A}\left(\frac{2}{3g_m}+R_{on}\right)\right\} \\
&= (1-m)^2\frac{kT}{C_S OSR}\left\{\left(1+\frac{C_F}{C_S}\right) + \left[1+\left(\frac{C_F}{C_S}\right)^2\right]\frac{g_m C_S}{C_A}\left(\frac{2}{3g_m}+R_{on}\right)\right\} \qquad (4.39)
\end{aligned}$$

Furthermore, $R_{on} \ll R_{eq}$ normally, so that $S^{S/H}(f)$ is essentially independent of R_{on} as long as the above-stated condition on $R_{on}C_S$ hold, and it is dominated by R_{eq} term. Therefore, the (4.39) can be more simplified as follows

$$\begin{aligned}
P_{th,input\ referred} &\simeq (1-m)^2\frac{kT}{C_S OSR}\left\{\left(1+\frac{C_F}{C_S}\right) + \left[1+\left(\frac{C_F}{C_S}\right)^2\right]\frac{g_m C_S}{C_A}\frac{2}{3g_m}\right\} \\
&= (1-m)^2\frac{kT}{C_S OSR}\left\{\left(1+\frac{C_F}{C_S}\right) + \left[1+\left(\frac{C_F}{C_S}\right)^2\right]\frac{2C_S}{3C_A}\right\}
\end{aligned}$$

where the C_A is equal to (C_S+C_F+C_P) that C_F is equal to C_S over 3.3, the $m = 0.4$ should be assumed, and the C_P can be disregarded so that to calculation here.

$$\begin{aligned} &\simeq 0.36\frac{kT}{C_S OSR}\left[\left(\frac{4.3}{3.3}\right)+\left(\frac{1+3.3^2}{3.3^2}\right)\frac{2\cdot 3.3}{3\cdot 4.3}\right] \\ &\simeq 0.67\frac{kT}{C_S OSR} \end{aligned} \tag{4.40}$$

Thus, an estimable noise of the input referred, $P_{n,total}$, can be presented as $P_{th,input\ referred}$ add to a noise, $P_{n,in}$, considered that which is always following with input signal due to the input signal is not spotlessly clean. Clearly, we can compute the peak SNR as

$$\begin{aligned} SNR_{peak} &= 10\log\left[\frac{P_S}{P_{n,total}}\right] = 10\log\left[\frac{P_S}{P_{n,in}+P_{th,input\ referred}}\right] \\ &< 10\log\left[\frac{P_S}{P_{th,input\ referred}}\right] = 10\log\left[\frac{V_{ref}^2/8}{0.67kT/(C_S OSR)}\right] \\ &= 10\log\left[\frac{V_{ref}^2 C_S OSR}{5.36kT}\right] \end{aligned} \tag{4.41}$$

where the $P_{n,in}$ is mostly less than the $P_{th,input\ referred}$. Hence, the $P_{n,in}$ can once be neglected. Consequently, we obtain the specification of the input sampling capacitor as

$$C_S > \frac{5.36kT\cdot 10^{(SNR_{peak}/10)}}{V_{ref}^2 OSR} \tag{4.42}$$

(4.42) is our basic design equation for the capacitors of the integrator in the first-order SDM implemented in this work. Also, the same as above process of the circuit noise analysis can be considered in CV-C.

Chapter 5

System Integration And Simulations

5.1 Introduction

As mentioned in previous chapters, the capacitive-sensing system performance was considered and decided; this chapter presents that the layout issues and floor-planning of the system are important key point for keeping the system pre-simulation performance. Also, it discusses and considers some useful skills for reducing noise coupling and external noise effects. Continuously, this chapter shows and introduces that supporting circuits and system simulations of this capacitive-sensing system. At the same time, the supporting circuit components show each in Fig. 5.1.

This chapter is organized as follows. The considerations of the layout is discussed in section 5.2. The introductions and layout views of the supporting circuit blocks, and simulations and layouts of the whole system are presented in section 5.3 and section 5.4, respectively.

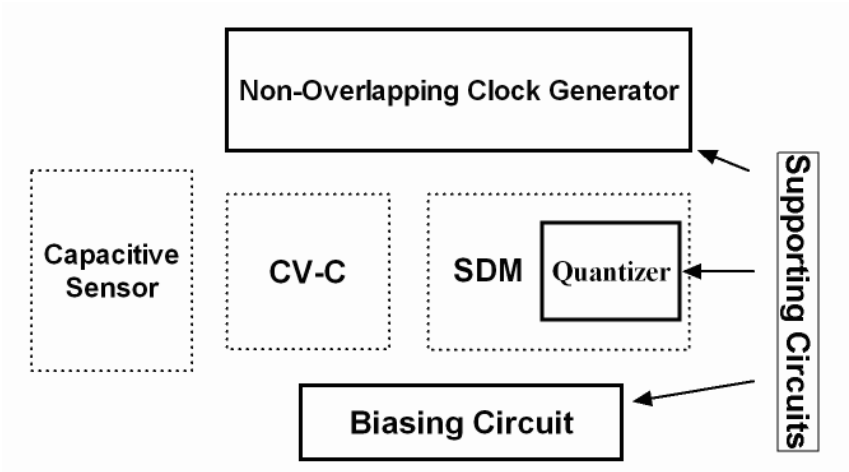


Figure 5.1: Supporting circuit blocks.

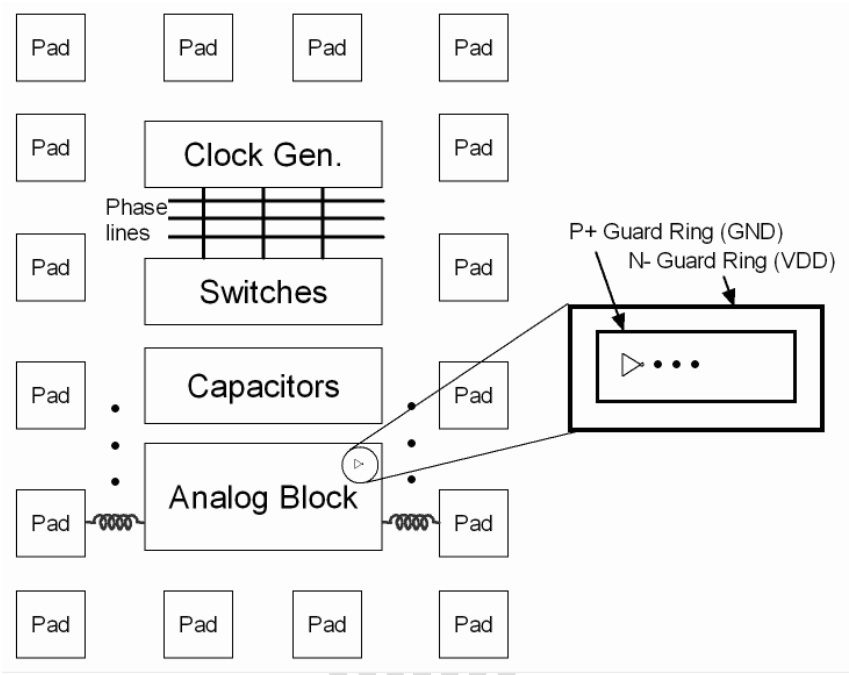
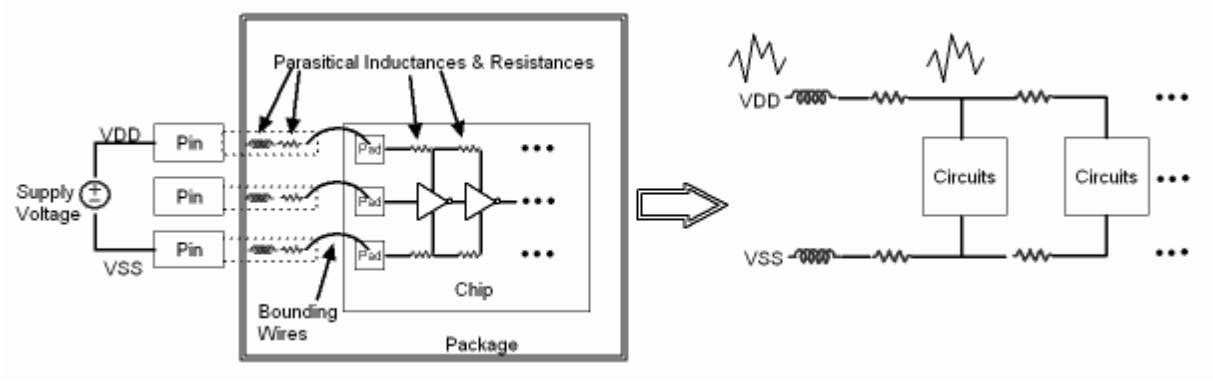


Figure 5.2: The floorplanning for switched-capacitor circuits.

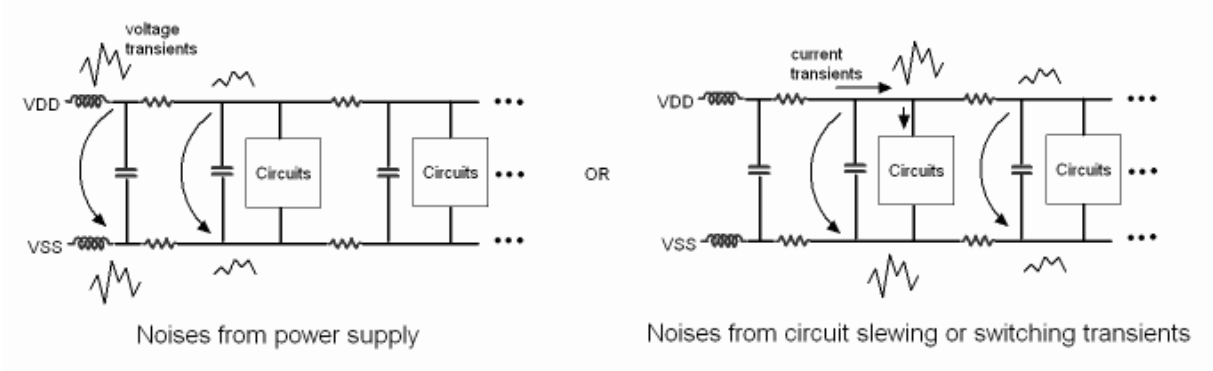
5.2 Layout Considerations

While any integrated circuit is to some extent sensitive to the physical arrangement of its components and their interconnections, mixed-signal ICs are more sensitive than most others. Thus, some critical points concerning the optimal layout of switched-capacitor circuits will be discussed in this subsection. The considerations and the basic principles of layout to be described are of great practical importance, and should not be ignored even in simple circuits.

In switched-capacitor circuits, these circuit blocks of the floor-planning almost are set as Fig. 5.2[16, 28, 10]. Generally, there are three major issues in switched-capacitor circuits which are the noise coupling, IR drop (voltage drop), and device mismatches. Such floorplanning has more minimize coupling between analog and digital blocks due to whose power supply sources are connected to pad by oneself and whose analog block and digital block are given a wide berth each other to avoid the noise coupling from substrate. Also, the clean voltage lines for the substrates and wells can also be connected to the analog supply pads without introducing any digital noises into the substrate or wells. These substrate bias lines must have as many contacts to the substrate or well as possible. These contacts will collect the electrons or holes injected into the substrate or well, keep the substrate or well at a fixed potential, and will thus prevent the occurrence of latch-up. A difference from substrate coupling is that noise coupling



(a)



(b)

Figure 5.3: (a) Package interface and its simple diagram and (b) added bypass capacitors.

through power lines which also lead to noise aliasing effects. The whole chip is packaged and connected between pads and pins; its package interface is illustrated in Fig. 5.3(a). At the same time, assuming a noise is generated from power supply or circuit block which are due to the switching transients of digital logic circuits or current driven of analog circuits (e.g. slewing), the noise induce to the circuits directly from power line. In Fig. 5.3(b) shows that adding bypass capacitors can reduce such noises due to stabilize the difference between Vdd and GND bounce in unison. Furthermore, the noise injection from the power supply lines can be also reduced by using differential structures due to they have a more high PSRR (power-supply-rejection-ratio) performance.

Also, another noise effect is not alike noises coupling from substrate and power lines which is passing through parasitical capacitance from the signal line and clock line cross over each other or parallel metal lines. To prevent some crucial signals or clock lines either from pick up or injecting noise, they can be shielded from their environments. A possible shielding arrangement for a metal line is shown in Fig. 5.4, where the shield consists of two grounded metal lines and a grounded polysilicon layer. Such shielding can also be used to separate the analog lines and

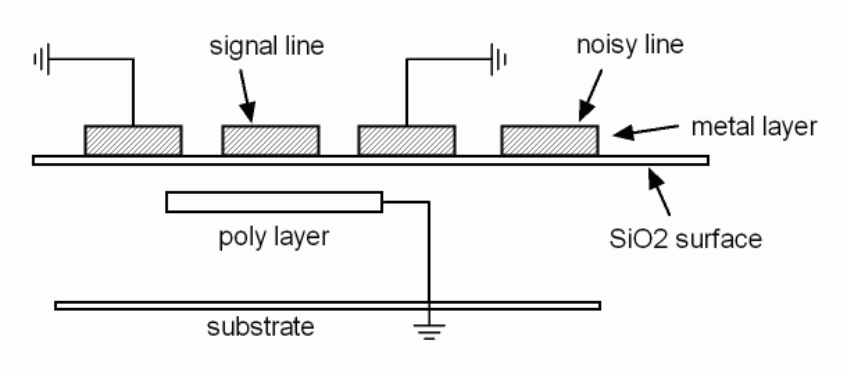


Figure 5.4: Shielding arrangement for a signal line.

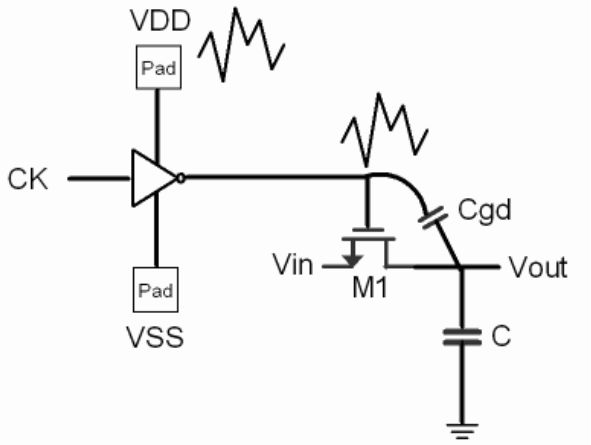


Figure 5.5: Noise from the clock buffer's supply bounce to the output.

digital lines, and to prevent noise from coupling into or out of the substrate. Although there are several manners to prevent the noise coupling, the power-line or clock-line noise can also enter into the signal path through the switches. For example, supposing a sampling circuit is clocked by an inverter (Fig. 5.5). The gate-to-drain overlap capacitance C_gd is also shown. Clearly, any noise will be coupled to the output of the simple circuit. In this work a multiphase-clock generator is be used, it is normally fed only by the digital supply lines; however, it is a better arrangement to use the analog power lines for biasing the last inverter of all clock signal path. This arrangement will reduce the digital noise in the clock signals and thus (as Fig. 5.5 shows) also in V_{out}.

In whole system, the bias currents and voltages of various building blocks are derived from one or more voltage reference generators. If the matching to Ir from current-mirror circuit is critical, then the voltage drop along the ground line must be taken into account; where the example depicted in Fig. 5.6. In fact, for a large number of circuits connected to the same

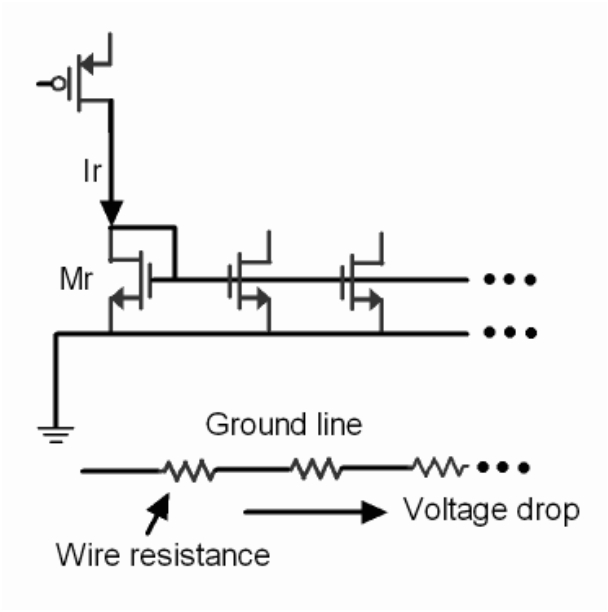


Figure 5.6: Distribution of a reference voltage for current-mirror.

ground line, the systematic mismatch between the current sources and Ir may be unacceptable. To remedy the above difficulties, the reference can be distributed in the current domain rather than in the voltage domain. An ideal is to route the reference current to the vicinity of the building blocks and perform the current mirror operation locally which is illustrated in Fig. 5.7. This arrangement has lower systematic errors if the building blocks appear in dense groups in different regions on the chip. Furthermore, in large system, it may be advantageous to employ several local voltage reference circuits so as to alleviate routing problems.

Another issue in current-mirror circuit relates to the orientation of the transistors. For example, if the transistors in current-mirror have different orientations, then substantial mismatches arise. Hence, the orientation of transistors is particular attention due to the orientation their current sources before and after the entire chip is composed since circuits 1, 2,..., n may be laid out individually. In a local, the current-mirror match up each other, they are almost placed together, whose placement likes as Fig. 5.8. This kind of placement is called **common-centroid** configuration. It is not only used in current mirror but the cascode part of any circuit or passive components (e.g. resistance and capacitance) are also. Furthermore, for drawing layout in critical part, it must be considered by itself for more better matched or not placing all of components together, especially for the input differential pair of amplifier due to reducing the offset voltage. A consideration to reduce the offset voltage of the differential pair (as Fig. 5.9 shows) that is not use minimum size for process variation. Also, an improved method of the element matching is

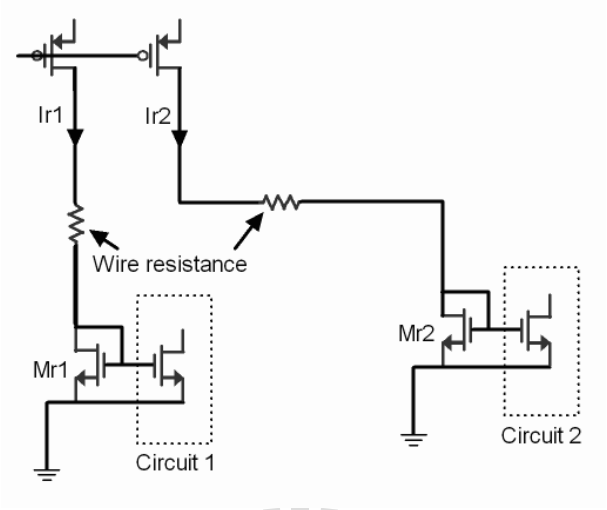


Figure 5.7: Distribution of current to reduce the effect of its wire resistance.

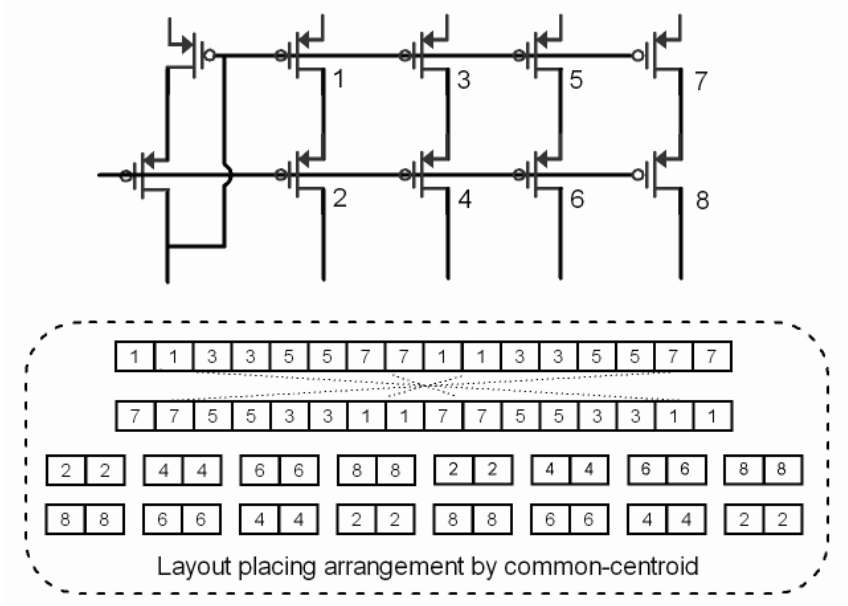
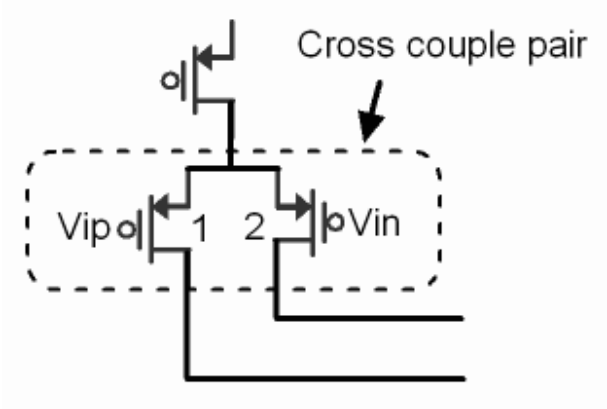
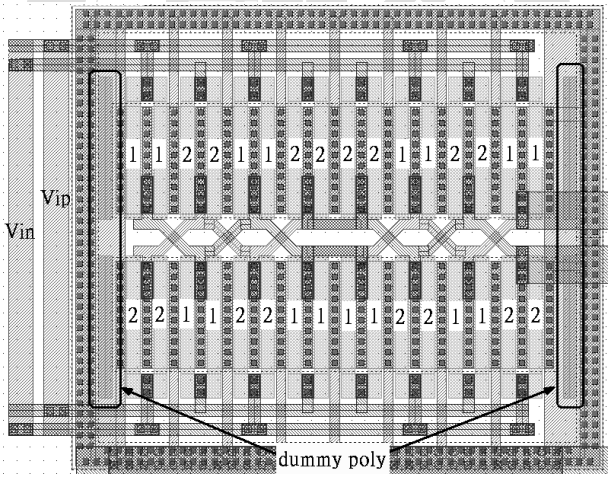


Figure 5.8: Layout placement for the mirrored cascode part of a current-mirror.



(a)



(b)

Figure 5.9: (a) A simple differential pair and (b) its layout.

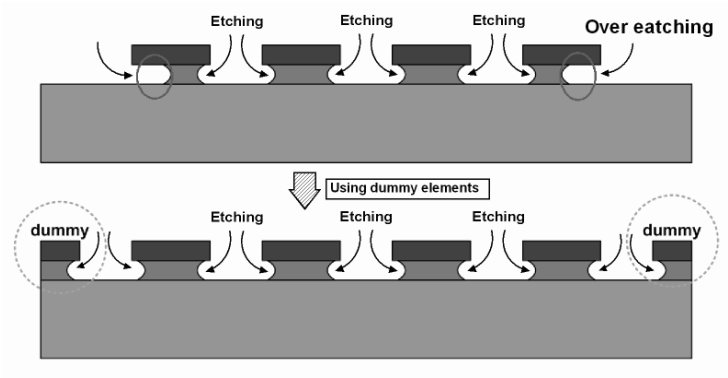


Figure 5.10: Compensation of boundary dependent etching with dummy elements.

added dummy cells which is also shown in Fig. 5.9(b). In Fig. 5.10 shows, using dummy cells can efficient in element matching, its basic concept is suppressing for etching (the process of removing material from a semiconductor wafer using reactive chemicals) unbalance. Further, it is very important to space the dummy components at the same spacing as the rest elements. Likewise, all the elements should be spaced the same to ensure they see same conditions. In this subsection, these considerations will be practiced in our work however only using these considerations in switched-capacitor are not enough to ensure that the performance of the circuit is keep as pre-simulation. Other effects are like as parasitical capacitance of used materials, parasitical resistance of used materials,..., and so on. Though these effects can affecting circuit performance but which are not crucially. Therefore, they are not mentioned here.

5.3 The Supporting Circuit Blocks And Layouts

5.3.1 Biasing Circuit

For achieving a fine system performance, a stable biasing current of the system circuits should be expected while it is always independent of any varying factor. A unstable biasing current is easy to let the biased circuit mistake. Such as this mistake is like noise which can degrade the circuit performance. Therefore, a feasible biasing structure is very important. According to [27], the biasing circuit, constant-Gm biasing, which is shown in Fig. 5.11(a) is chosen and considered here. This circuit exhibits little supply-dependence if channel-length modulation is negligible and can easily decide the bias current through the chosen resistor size. For a lower supply voltage varying effect, the relatively long length are used for all of the transistor in the circuit. Furthermore, the resistor must be chosen in poly- or diffusion-type for the lower T.C.

Table 5.1: The information of the post-layout simulation by HSpice simulator for constant-Gm at Vdd: 3.3 V with TT corner.

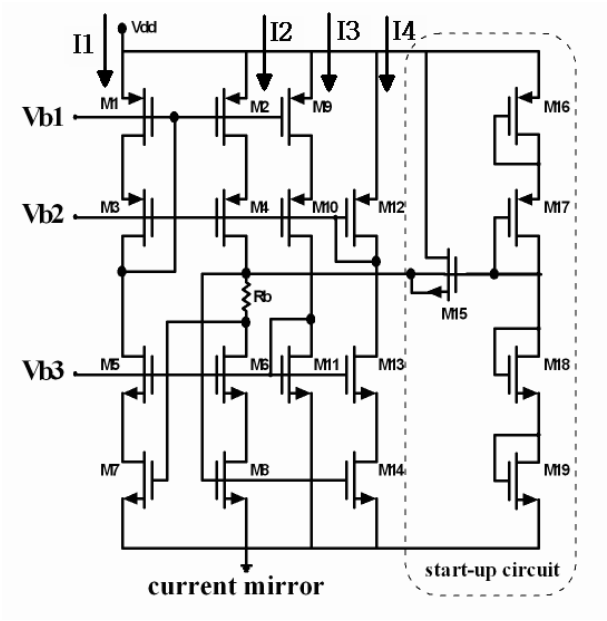
Parameter	-	Unit
Supply voltage	3.3	Volt
Path current (I_{1-2})	5	μA
Path current (I_{3-4})	10	μA
Vb1	2.18	Volt
Vb2	1.8	Volt
Vb3	1.34	Volt
Power consumption	100	μW

(temperature coefficient) to decrease the temperature effect. The resistor of the n plus diffusion type is decided for the lowest absolute error and a higher resistance of per squre μm than others consideration type, while the biasing current (e.g., path current I_1) varied by the resistor error will be ensured in a tolerant range (it means that keeping the biased circuit work correctly) and be ignored if the resistance that is 5 Kohm here is varied in $\pm 10\%$; the simulation of path current I_1 shows in Fig. 5.12(a).

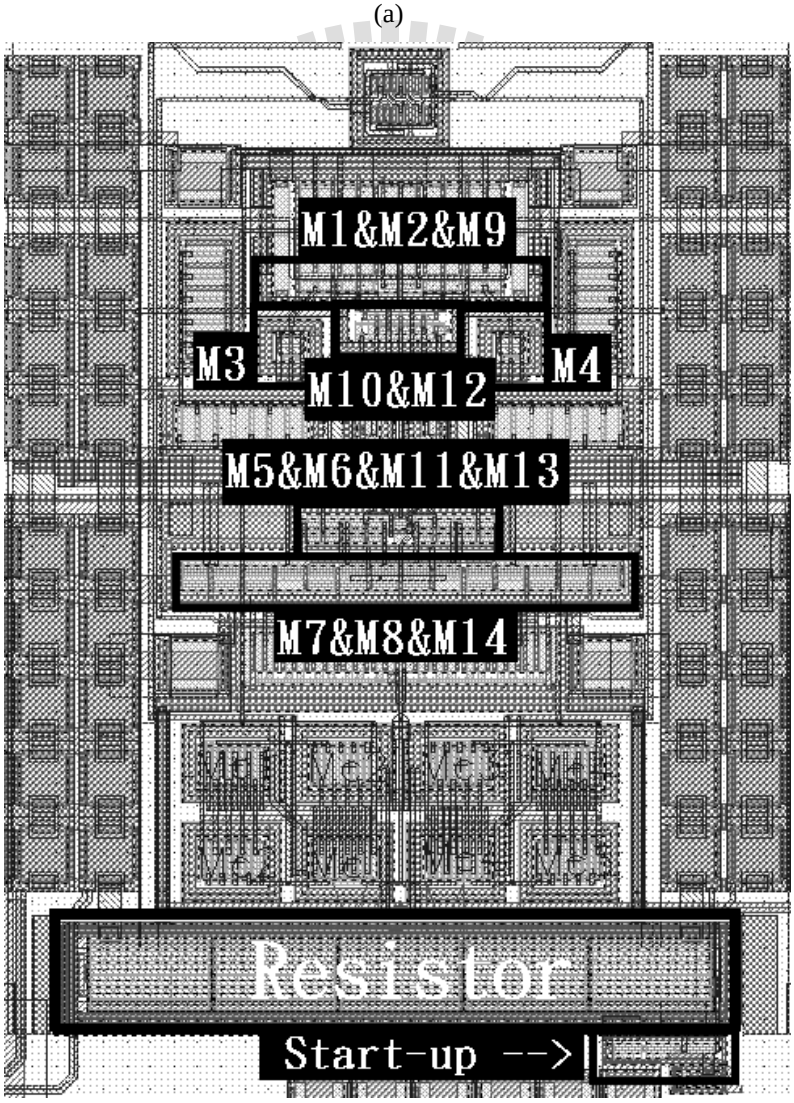
Another issue is the settling speed of the biasing circuit which may experience "crosstalk" through reference lines by various building blocks. Therefore, adding large capacitors at critical nodes (e.g. node Vb1, Vb2, and Vb3) which can be bypassed to ground so as to suppress the effect of external disturbance. The value of bypass capacitors must be much greater than capacitance that couples the disturbance to critical node so that it can quickly recover from transients. However, the difference from the issues of the bias current accuracy and recover speed is the bias circuit start-up at suddenly power on. Therefore, it shows and tests that the bias current I_1 (I_1 is shown in Fig. 5.11(a)) of the biasing circuit works yes or not in the Fig. 5.12(b) at suddenly turn on the supply voltage. Also, the simulations that is generated with the temperature from 0 to125 deg.C while the supply voltage varied from 2 V to 3.6 V are shown in Fig. 5.12(c). Both of the simulation figures (Fig. 5.12(b) and Fig. 5.12(c)) represent that the bias circuit is work correctly, it ensures that the OTA is biased exactly. In Table 5.1, it shows the detail specifications of the biasing circuit at Vdd: 3.3 V with TT corner.

5.3.2 Quantizer

The quantizer consists of a comparator and a transmission gate D-latch flip-flop. The fully scheme shows in Fig. 5.13(a). The digital output will be latched in the falling edge of P2.

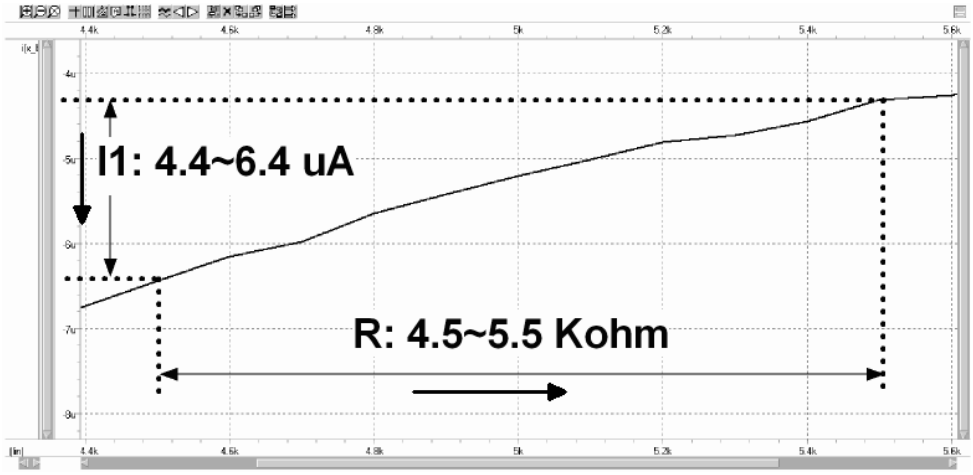


(a)

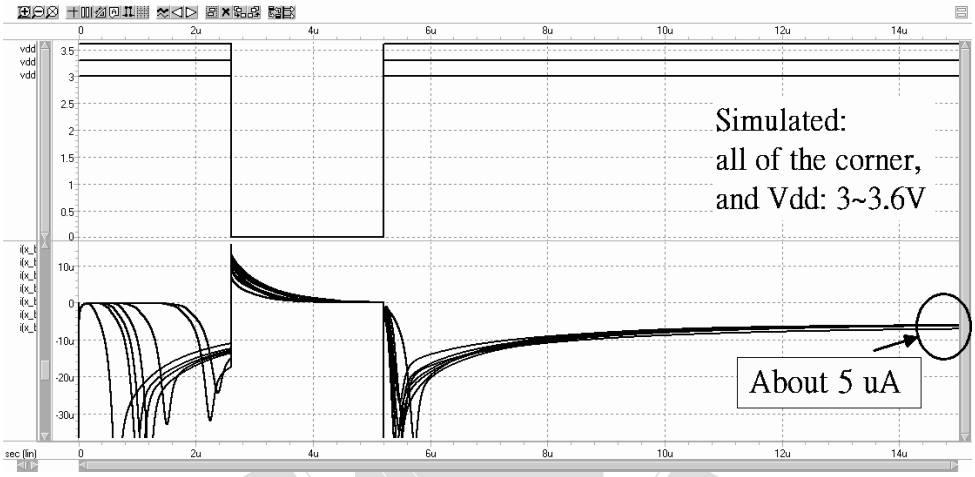


(b)

Figure 5.11: Biasing circuit: (a) the scheme of the constant-Gm and (b) its layout view; the layout is set with the biased circuit (OTA).



(a)



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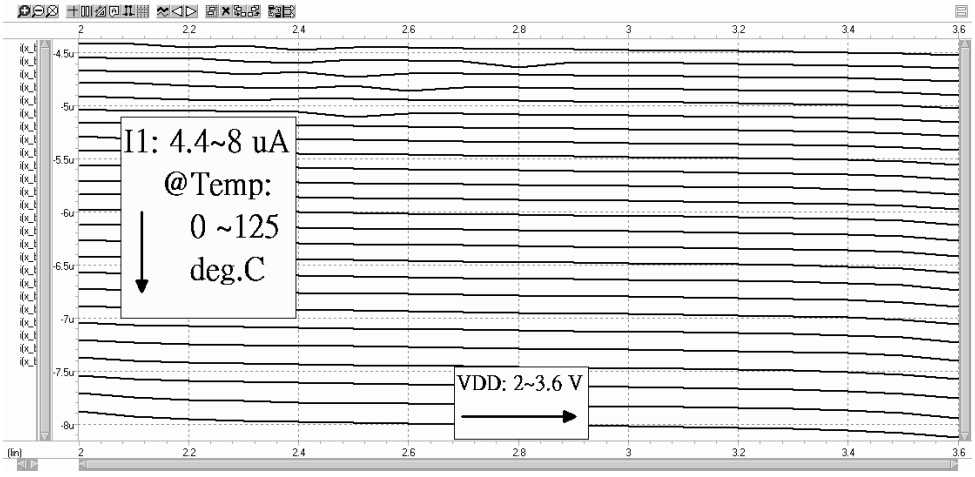


(c)

Figure 5.12: The constant-Gm post-layout simulations for path current I_1: (a) the resistance variation from 4.5∼5.5 Kohm, (b) a suddenly power on simulation at Vdd: 3 V, 3.3 V, and 3.6 V, and all of the corner at Vdd: 3.3 V, and (c) I_1 is measured at Vdd: 2∼3.6 V and temperature: 0∼125 deg.C.

In this work, a clock frequency of 1M-Hz is used. The comparator of the quantizer has more enough time for comparing than others high speed applications, thus, a lower transient power consumption comparator will be considered. Therefore,an un-compensation two-stage opa (shows in Fig. 5.13(b)) is feasible to choose where the biasing current of the comparator is generated from constant-Gm with a simply current mirror (the layout view of the comparator with a simply current mirror shows in Fig. 5.13(c)). The un-compensation two-stage opa only costs less supply current to perform comparing. It has another advantages such as no kickback-noise effects and easy to design. The layout of the quantizer shows in Fig. 5.14.

5.3.3 Non-Overlapping Clock Generator

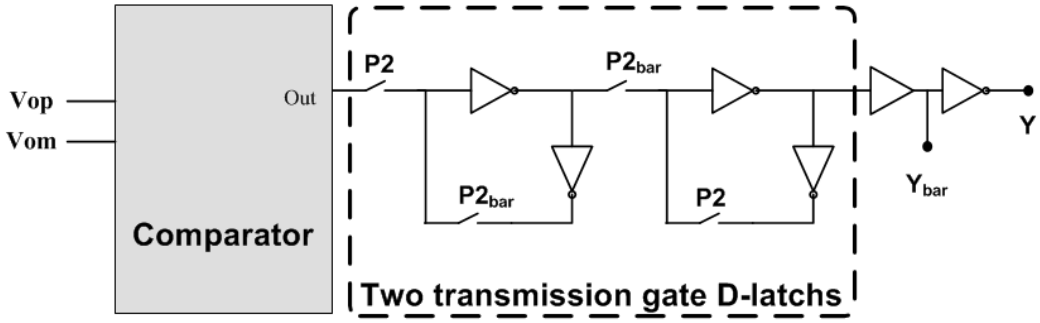
Up to now, a non-overlapping clock generator has to be used to realize a fine system performance for achieving two techniques in our work such as bottom-plate sampling and complementary switches. The simply scheme and the layout show in Fig. 5.15(a) and Fig. 5.15(b), respectively. The phase P1bar, P2bar, Pd1bar, and Pd2bar are inverse with the phase P1, P2, Pd1, and Pd2. Also, the phase Pd1, Pd2, Pd1bar, and Pd2bar are slightly delayed than the phase P1, P2, P1bar, and P2bar. About these post-layout clock phase waveforms shown in Fig. 5.16 by HSpice simulator.

5.4 System Simulations

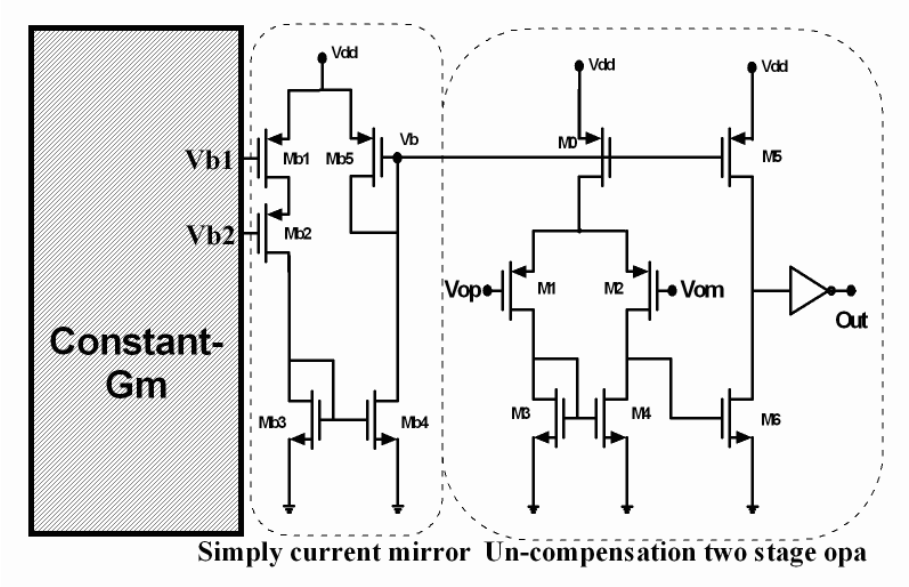
According to that the introduction of the above components, the layout of the CV-C and the SDM can be combined with these components and shown in Fig. 5.17 and Fig. 5.18, respectively. The capacitive sensor circuit system that consists of a CV-C and a first-order SDM is integrated and shown in Fig. 5.19. The system layout view shows a MEMS-sensor, a CV-C, a SDM, and a non-overlapping clock generator. The area cost is $1.5(mm)^2$.

As mentioned in chapter 2, the capacitive sensor that is here performed as a accelerometer detection achieves by using CMOS-MEMS technique. Its capacitance of the maximum difference value is 30 fF which is corresponding to vibration acceleration of $\pm$5g, while it is corresponded and designed to a $\pm$1V CV-C differential output swing.

The simulated sensing system operates at Vdd: 3.3 V with TT corner. The Fig. 5.20(a) and Fig. 5.20(b) plot a periodic waveform of the CV-C differential output in time-domain and plot its PSD of 8192-point FFT in frequency-domain, respectively. The Fig. 5.20(a) and Fig. 5.20(b)



(a)



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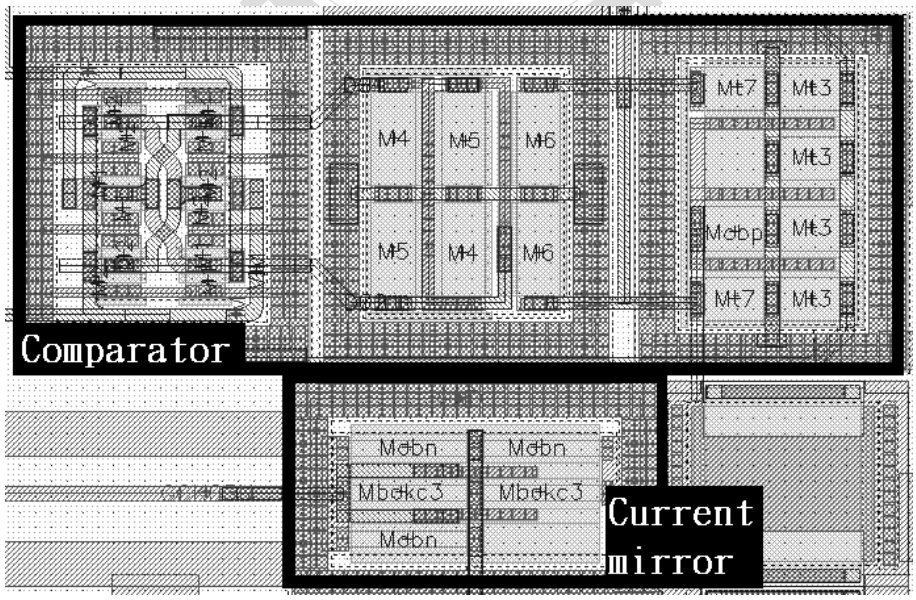


(c)

Figure 5.13: 1-bit quantizer: (a) a simple scheme, (b) the comparator is realized by an un-compensated opamp, and (c) the layout of the comparator with the simple current mirror.

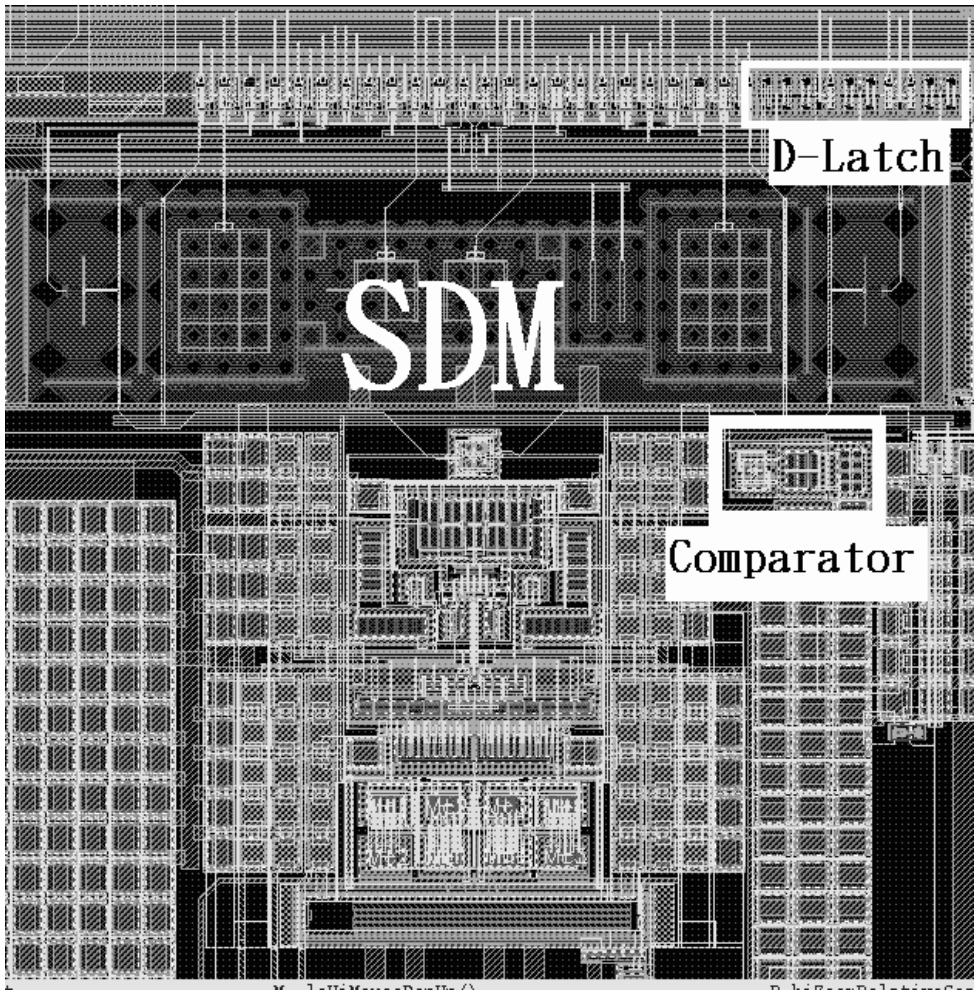
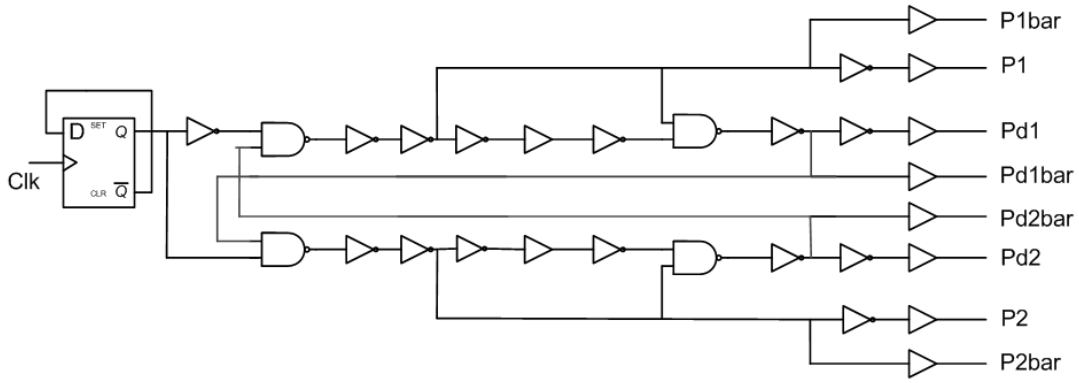
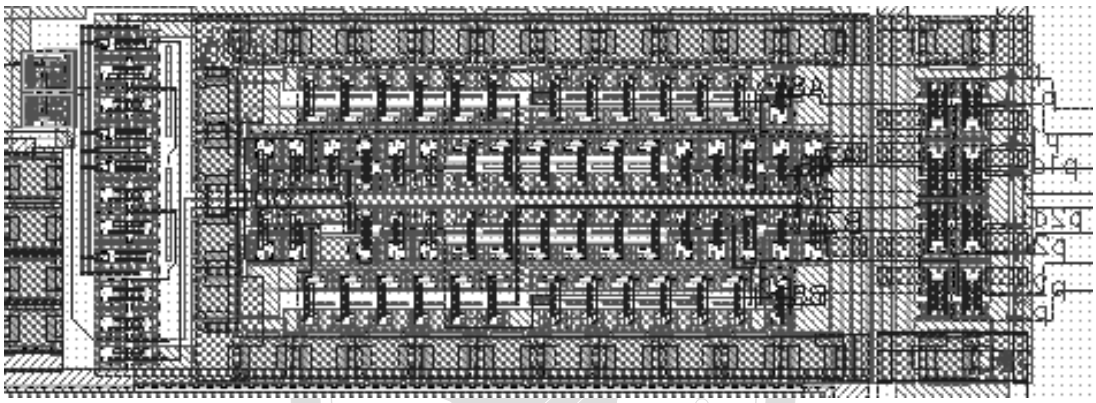


Figure 5.14: The quantizer layout shown in the white line blocks consists of a comparator and a D-latch.



(a)



(b)

Figure 5.15: Non-overlapping clock generator: (a) a simply scheme and (b) its layout view.

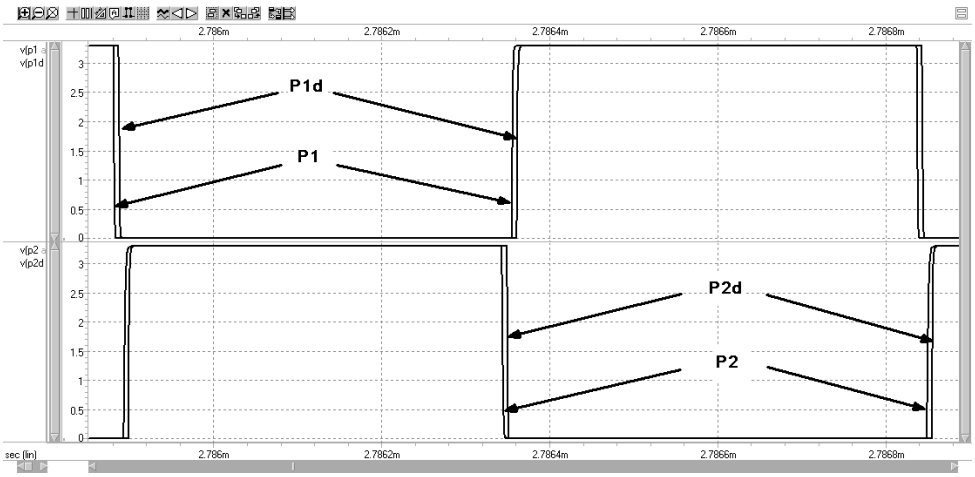


Figure 5.16: The non-overlapping clocks generated by HSpice post-layout simulation.

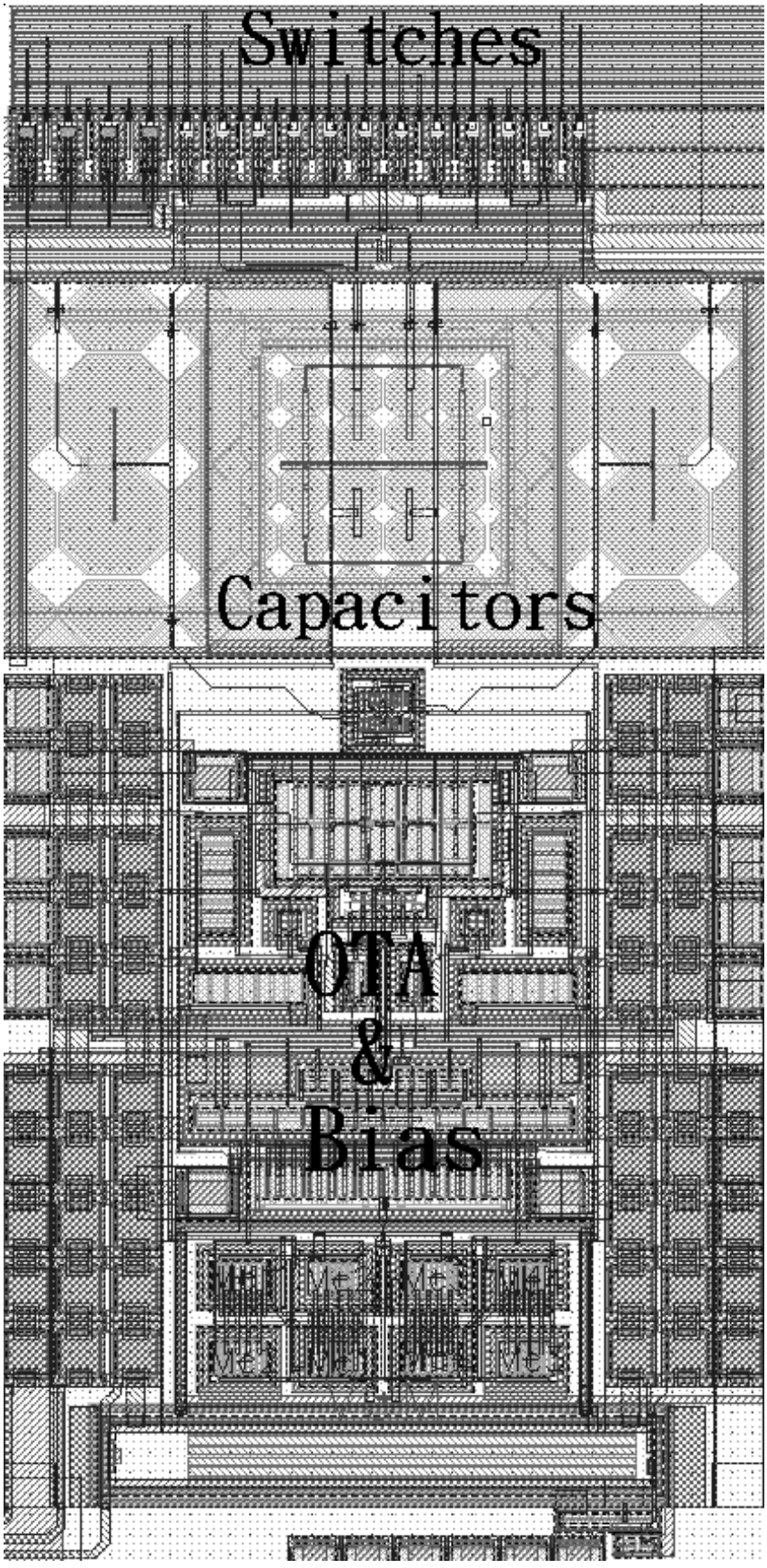


Figure 5.17: The layout of the CV-C.

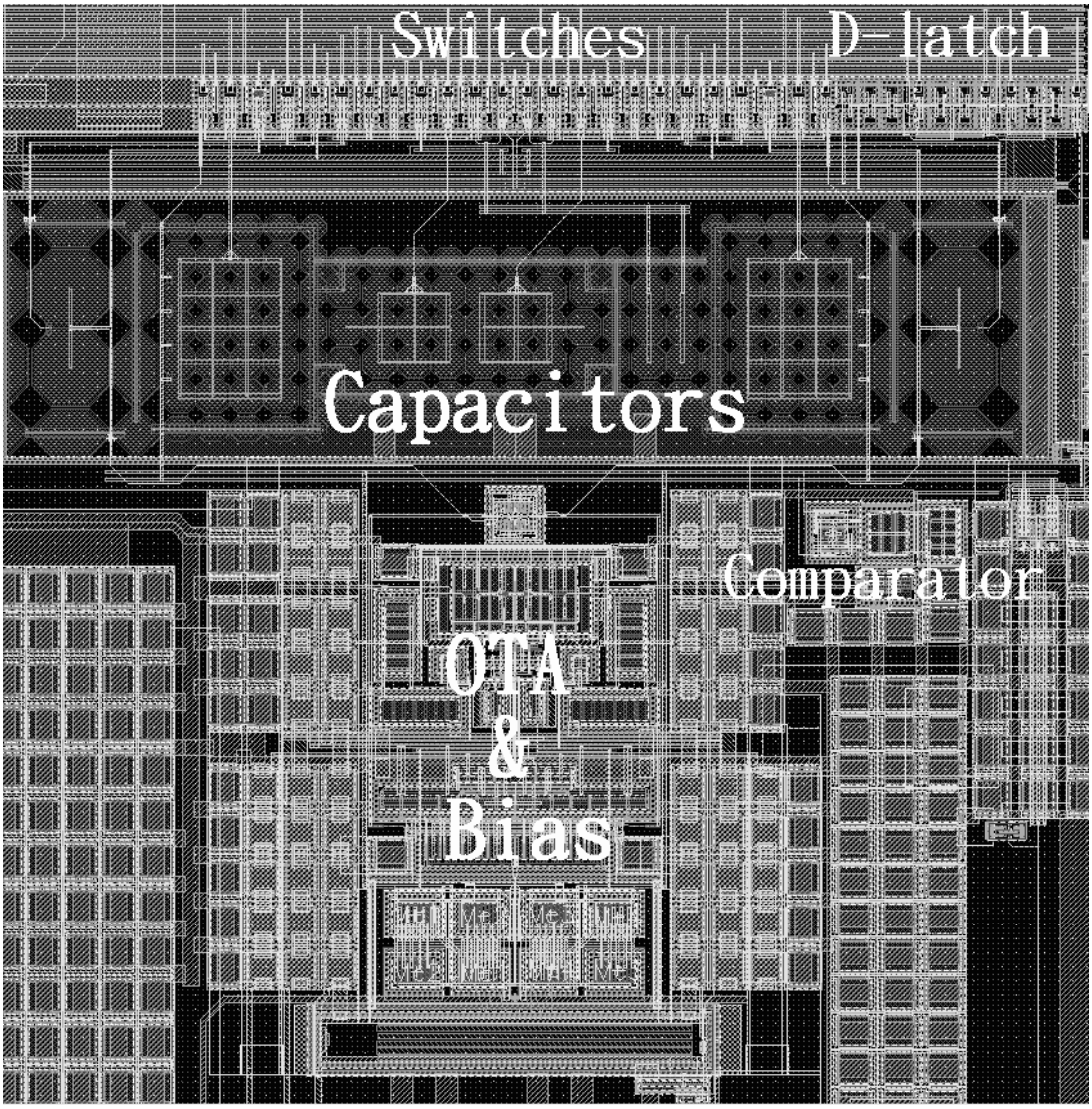


Figure 5.18: The layout of the first-order SDM.

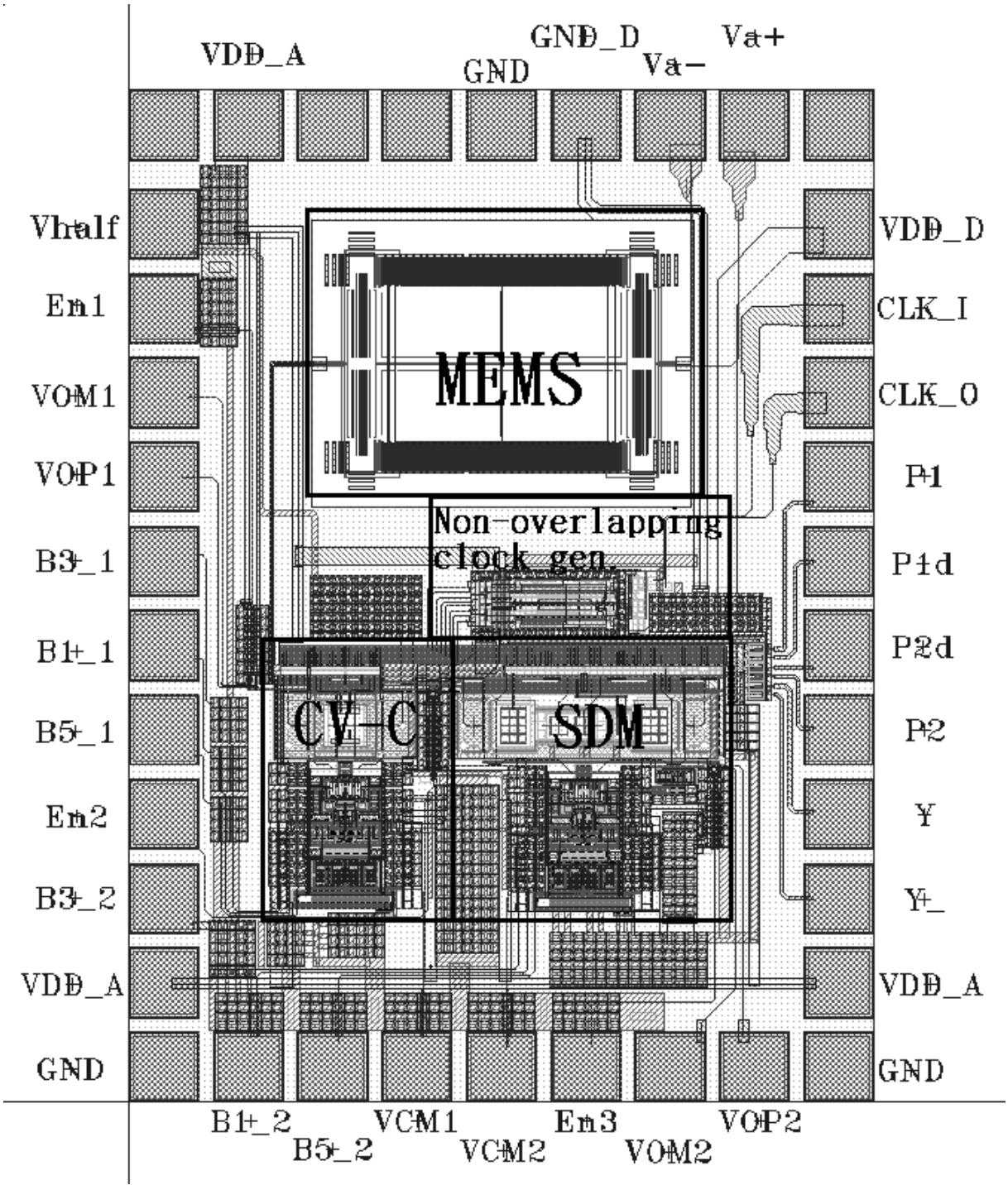
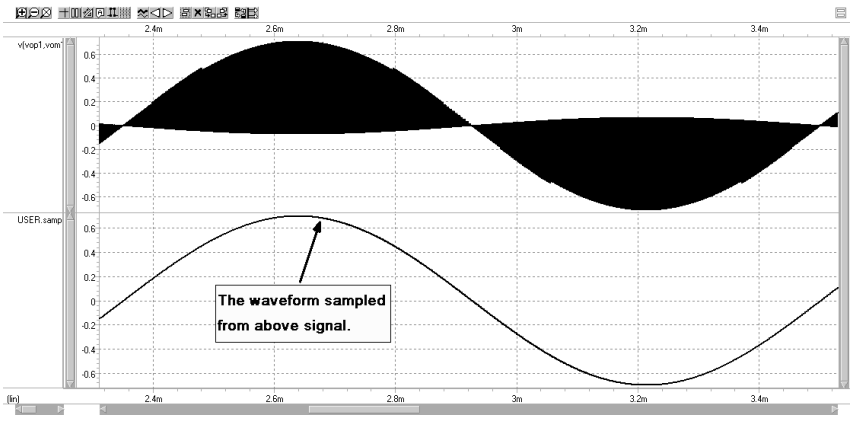
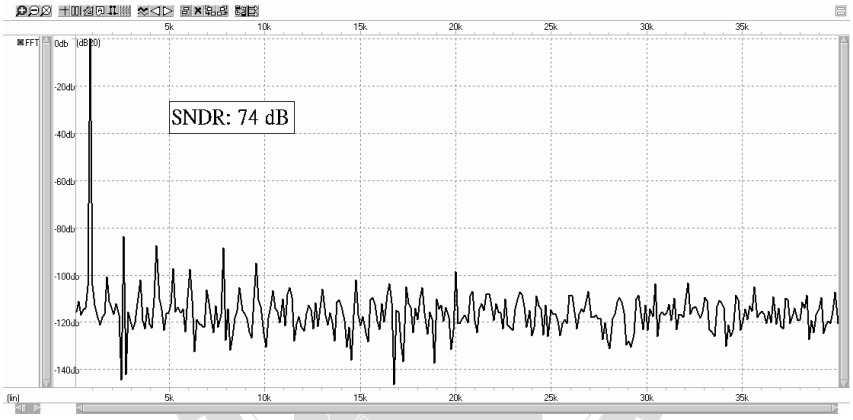


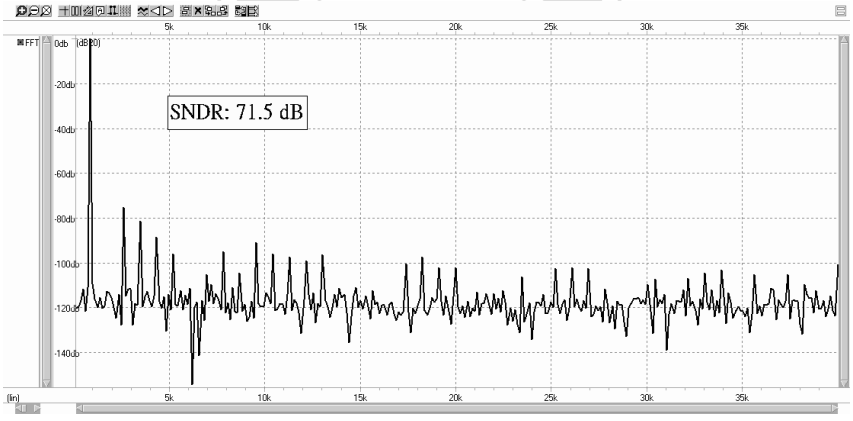
Figure 5.19: The floor-plan of the capacitive sensor circuit system layout .



(a)



(b)



(c)

Figure 5.20: The post-layout simulations of the CV-C: (a) the time-domain plot, (b) the PSD plot, and (c) the PSD plot of the worst case at Vdd: 3.0 V with TT corner.

Table 5.2: The simulation setup of the sensing circuit.

Simulations setup	-	Unit
Vdd	3∼3.6 (Simulated at TT corner)	Volt
Sampling clock	1	MHz
Frequency of the variable capacitors	869	Hz
Amplitude of each variable capacitors	10.6 (full scalar of -3 dB)	fF
Process corner	TT, FF, SS, SF, FS (Simulated at Vdd: 3.3 V)	-

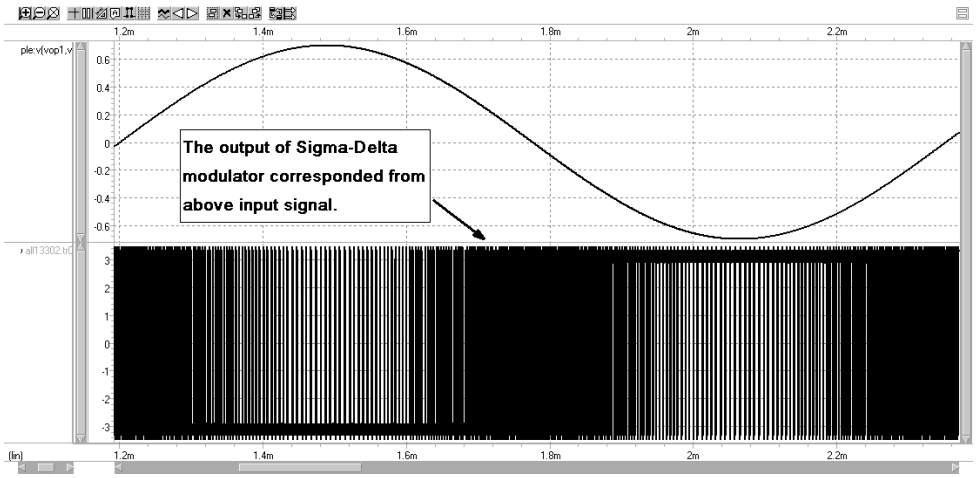
Note: The worst simulation results of the CV-C and SDM are obtained from these setup.

Table 5.3: Performance parameter summary of the sensing circuit.

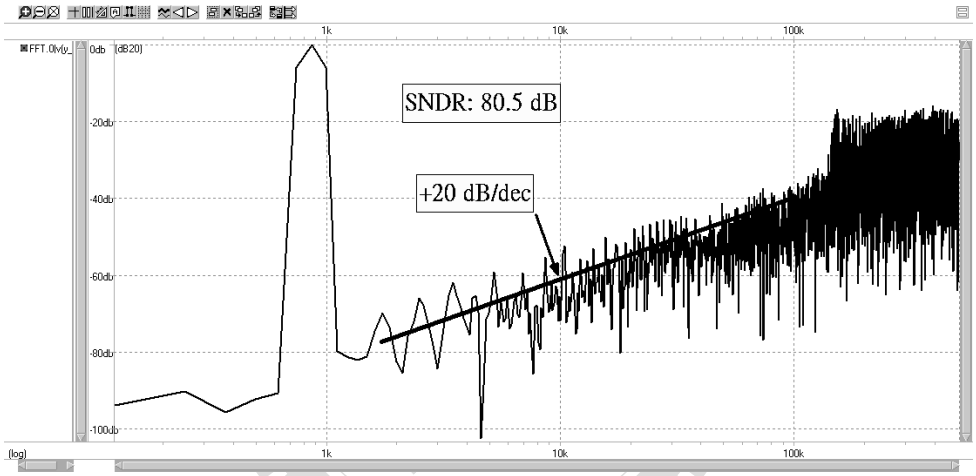
Parameters of the CV-C	-	Unit
THD	-73	dB
SNR	71.5	dB
SNDR	71.5	dB
ENOB	11.6	bit
Parameters of the SDM	**-**	**Unit**
SNR	73.1	dB
SNDR	73.1	dB
ENOB	11.8	bit

Note: The parameters of the CV-C and SDM are considered and obtained at worst case.

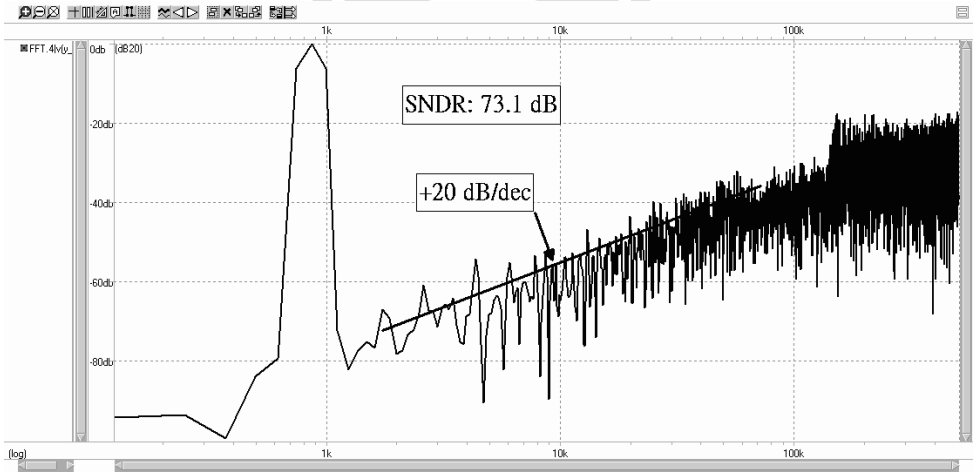
also show the waveform of the time-domain and its PSD of the first-order SDM output with a signal bandwidth of 1.2 K-Hz. The input signal power that is generated by a supposed vibrated motion is -3 dB full scale and its frequency is 869 Hz. At the same time, we are also showing the worst case simulations for CV-C and SDM where the simulations setup of the sensing system is shown in Table 5.2. Both of them which are shown in Fig. 5.20(c) and Fig. 5.21(c) are measured from simulations setup, respectively. According to these results, the sensing system is achieved successfully for 10-bits resolution (about SNDR of 60 dB). Finally, the performance parameter summary of the sensing system are shown in Table 5.3. The maximum rms power consumption of the accelerometer detection system is 2.7 mW at Vdd: 3.6 V with TT corner.



(a)



(b)



(c)

Figure 5.21: The post-layout simulations of the SDM: (a) the time-domain plot, (b) the PSD plot, and (c) the PSD plot of the worst case at Vdd: 3.3 V with FF corner.

Chapter 6

Conclusions And Future Work

In this thesis, we focus on a capacitive sensor circuit design for capacitive sensing applications. Capacitive sensor (e.g., pressure gauge sensor, gyroscope, accelerometer,..., and so on) can be combined with our proposed interface system to performing a capacitive sensing system (this frame is like as silicon IP applications). A sensor circuit which is successfully designed here combines with a MEMS accelerometer (the two pair variable capacitors are used here) fabricated via TSMC CMOS-0.35μm process. The maximum capacitance variation is 60 fF. Post-layout simulation indicates that the designed capacitive sensing system can obtain about 12-bits resolution. The maximum power consumption of 2.7 mW at a signal 3.6 V supply voltage. The die area is 1.5 mm^2.

However, since the adopted first-order SDM has an inherent limitation of poor dynamic range, it is necessary to have a high OSR in order to obtain a high SNR performance. To improve the performance without increasing the OSR, a high order SDM or multi-bits SDM may be the better choice for gaining a wider dynamic range in the future. At the same time, the feedback structure should be implemented to achieve calibration of static error for totally sensing system design.

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