國立交通大學

電子工程學系 電子研究所

博士論文

應用於超寬頻及多通訊標準無線接收機之

互補式金氧半低雜訊前端電路

CMOS Low Noise Front-End for Ultra Wideband and Multi-Standard Wireless Receiver

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指導教授：郭 建 男 Chien-Nan Kuo

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摘要

本篇論文主要探討達到寬頻同時雜訊及輸入阻抗匹配的低雜訊放大技術。在此針對傳統的 Y-參數雜訊分析方式進行改良，發展出較為準確的雜訊分析式，並依此定出設計低雜訊放大器的最佳策略。在本論文中所提出之雙重電抗性迴授電路架構在配合 LC 梯狀阻抗匹配網路之後，可達成寬頻同時雜訊及輸入阻抗匹配的最佳低雜訊放大器之設計條件。其中電感性部分迴授電路可以以變壓器迴授電路方式實現，大幅降低所需的晶片面積。本技術應用在設計一個 3–11-GHz 超寬頻低雜訊放大器，以及一個 2.4–5.4-GHz 可程式帶限低雜訊放大器。在可程式帶限低雜訊放大器的應用中我們亦發展出電晶體及電感之切換電路技術。前者提供電路性能的可程式特性，後者提供超寬可調頻率範圍並有效維持一致的電路性能。

在低雜訊放大器之前，射頻收發切換器直接影響整體收發器的性能。在此發展出針對 CMOS 特性的電路設計技術以提高切換器的線性度及耐受度。所設計出的 4.9–6.0-GHz 收發切換器可達到+30dBm 線性度以及低於 1-dB 的損耗。

CMOS Low Noise Front-End Circuit for Ultra Wideband and Multi-Standard Wireless Receiver

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Abstract

The technique of low noise amplification with broadband simultaneous noise and impedance matching (BSNIM) was developed. The conventional noise theory for MOSFET devices is revised to be more accurate. Strategies are addressed how to achieve low noise amplifier design. A dual reactive feedback topology along with an LC ladder matching network was proposed for BSNIM realization. The inductive feedback was implemented with a transformer feedback to reduce the circuit form factor. This technique was utilized to develop a 3–11-GHz ultra-wideband (UWB) LNA and a 2.4–5.4-GHz reconfigurable band-selection LNA. In the latter work the techniques of transistor switching and shunt inductor switching were developed. The transistor switching provides reconfiguration of performance including gain, linearity, and power consumption. The inductor switching provides a wide frequency tuning range while the voltage gain is consistent within the tuning range.

An RF T/R switch in front of LNA directly affects transceiver performance. Circuit design techniques were developed specifically for CMOS process to overcome the shortcoming of MOSFET when handling high power. In this thesis a 4.9–6.0-GHz T/R switch is demonstrated with sub-dB insertion loss and >30dBm power handling capability.

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In 2003, at Dr. Wu's suggestion the author joined Dr. Kuo's research group and assisted Dr. Kuo to administrate Ding-Hsiun High Frequency Laboratory. Since then, Dr. Kuo has been not only an advisor but also the best mentor and friend to the author. He provided a complete training, technical and non-technical, trying to make the author a qualified PhD. As an innovative research is typically full of risk and uncertainty, Dr. Kuo's advices and encouragements strongly backed the author moving forward. As the result of his thoughtful guidance, the author has had the preliminary capability to execute a quality research independently from stem to stern. In 2006 Dr. Kuo encouraged the author to go abroad experiencing an internship in Intel Corp., Oregon, USA. To the author it has been the highest privilege having the chance to do research with the smartest engineers in the world. The author would like to express million of thanks to Dr. Kuo for all his considerate advises and those critically important favors in his PhD program.

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Finally, the author wishes this thesis could be helpful to all those students / researchers / engineers who may meet the similar problems.

Chang-Tsung Fu
Aug 01, 2009

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Chapter 1

Introduction

1.1 Motivation

In the past few decades, wireless communication has become a very convenient and widely used technology in people's usual life. Those facilitation applications include voice communication, data transmission, identification, radar detection, and other emerging new applications. The wireless data transmission is more and more important with the evolution of internet applications. People want to instantly access internet for sending/receiving messages/emails, surveying helpful information, making decision/transaction, anywhere and anytime, fixed or mobile. In a high level philosophic statement, wireless communication makes possible a new type of freedom: people can make information exchange without constraints of physical position.

The general application requirements on wireless communication in people's usual life can be categorized in two types: indoor and outdoor. In the office or at home, the wireless

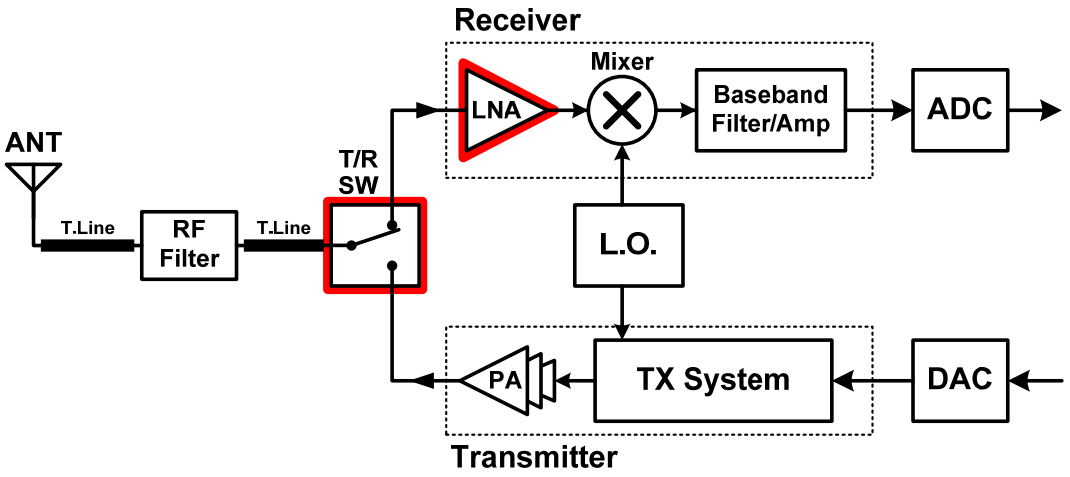


Figure 1-1. A general TDM wireless transceiver.

connection is expected to provide high volume data transmission to reduce the mess of physical cable connections. This demands a *short-range broadband* data transmission. The 3.1- to 10.6-GHz ultra-wideband (UWB) system provides one of such connection. Furthermore, a broadband wireless system can be utilized for various applications other than data transmission, such as radar detection and position detection …etc. Those derivative applications can be very useful.

When outdoor, the wireless connection is expected to access any service seamlessly and dynamically. As such the mobile device, a handheld or a laptop, is expected able to support *multiple communication standards*.

To make wireless communication in an economy scale, hardware features such as low cost, low power (for long battery life), and small form factor are essential. CMOS integrated circuit technology is the preferred choice for a low cost high volume manufacture. Advanced circuit design techniques and system design play the critical roles toward these targets. Circuit design techniques pursuing performances such as broadband, low noise, low power, high linearity, and high efficiency dominate the feasibility of a communication specification. A sophisticated

system planning according to the state-of-the-art circuit design techniques can maximize the performance of the entire system. Furthermore, the integration and co-design of discrete circuit blocks can provide an even higher degree of performance optimization.

Whereas a bi-directional wireless communication necessitates multiplexing technique, a wireless transceiver typically applies either frequency division multiplexing (FDM) or time-domain multiplexing (TDM). From the power consumption point of view, a TDM transceiver is preferred as it consumes less power whereas the power-hungry power amplifier in the transmitter side is not turned-on all the time. Data is concentrated to be transmitted only in a small duty cycle. A general RF front-end of a TDM wireless transceiver is shown in Figure 1-1. In the transmitter side it is composed of a transmitter modulation system and a power amplifier (PA). The transmitted signal of large power (>20dBm) is delivered via a RF transmit/receive (T/R) switch into the antenna and emits. In the receiver side, a mono-heterodyne receiver is shown as an example. It composes of a low noise amplifier (LNA), a down-converter, and the baseband filter/amplifier. The wanted baseband received signal is amplified to the full-scale of the ADC, converted to digital signal and demodulated with the digital signal process.

To achieve a sufficiently low bit error rate (BER) after demodulation, the signal to be demodulated should have a signal-to-noise ratio (SNR) higher than a certain value. The sources of noise degrading the signal integrity include the thermal noise introduced by the T/R switch and the LNA at RF frequency, the flicker noise by the mixer and baseband filter/amplifier, the quantization error of ADC, and the interferers from other out-of-band signals, attributed to the imperfect receiver linearity. Among them, the thermal noise at RF frequency is the dominant noise contributor. Hence to the low-noise performance on the T/R switch and the LNA is the major task to achieve.

In compare to LNA, the noise factor of a T/R switch is directly related to its insertion loss

as it works as a passive device. Besides the low insertion loss in receive mode, the high isolation between the antenna and the LNA in transmit mode, and the low insertion loss from PA to antenna are demanded as the fundamental requirements of a T/R switch. Another basic requirement of a T/R switch is the good linearity to handle the high power signal from PA, typically larger than +24dBm, which showes a 10Vp-p voltage swing over a 50Ohm load. To date only the GaAs T/R switches can well meet all the performance requirements. It's challenging to implement a decent T/R switch in CMOS technology.

1.2 Thesis Overview

In this thesis we are focused on implementing two of the most critical RF front-end circuit blocks – the low noise amplifier (LNA) of a wireless receiver and the RF T/R switch, as shown in Figure 1-1, in CMOS technology. The study of LNA is focused on the broadband and reconfigurable/wide-tuning techniques. The T/R switch is focused on making a CMOS T/R switch of performance comparative to the expensive GaAs counterpart.

Our study toward broadband LNA indicates the limit of the conventional low noise amplifier theory. The conventional Y-parameter noise analysis [1], [2] is found insufficient in today's CMOS technology: effect of the induced gate current noise is over exaggerated and other dominant terms such as gate resistance and gate-to-drain capacitance are improperly ignored. The conventional derivation is also found unfavorable to the broadband LNA theory development with the erroneous frequency dependency interpretation. A series of discussions are conducted to propose an accurate formulation and a reasonable simplified form for noise analysis.

1.3 Thesis Organization

In Chapter 2 the complete theory of broadband simultaneous noise and impedance matching is developed. In the beginning the channel thermal noise of a MOS transistor in deep sub-micron is reviewed. Then the key factors affecting the noise performance of a common-source amplifier is discussed. According to the derived theory, the optimal condition of broadband simultaneous noise and impedance matching (BSNIM) for LNA is developed.

A dual reactive feedback composing of a shunt capacitive feedback and a series inductive feedback was invented. Three inductors in the topology were further refined into a transformer feedback form, which occupies only one transformer area and reduce the form factor.

In Chapter 3, a 3–11-GHz UWB LNA utilizing the BSNIM technique of LC-ladder matching and dual reactive feedback was developed and silicon verified in TSMC 0.18um CMOS process. It demonstrates a good broadband noise performance (< 5dB NF) over the entire pass band, while only 9mW DC power is consumed.

A 2.4–5.4-GHz reconfigurable LNA for multi-standard purpose was developed in TSMC 0.13um CMOS process, detailed in Chapter 4. The switching of transistor and inductor provide reconfigurable performance and operation frequency, respectively. New inductor switching technique was proposed utilizing switch parasitic capacitance to boost inductor quality factor at high frequency. The tuning range limitation is analyzed and the design guideline is developed. The noise figure is less than 3.1dB (high gain mode) for all the frequency options, while a less than 5mW DC power is consumed.

A 4.9–6.0-GHz T/R switch was developed as shown in Chapter 5. By utilizing body isolation technique the CMOS switch can handle RF power over +30dBm. Inductor in parallel improves switch isolation in OFF state. The ON-state insertion loss is 0.9dB, of the same order

as GaAs switch. Switch transistors are placed inside inductor coil to save area.

Chapter 2

Theory of Broadband Simultaneous Noise and Impedance Matching for Low Noise Amplifier Design

2.1 Introduction

A low noise amplifier (LNA) is an essential component at receiver input for wireless communication. It is expected having a high gain with a low noise figure to provide a sufficient signal-to-noise ratio for signal demodulation. Among various MOSFET LNA circuit topologies, the common-source (CS) based amplifier is generally preferred as it performs better noise performance within limited power consumption. It is especially popular for extreme applications in which ultra low power or very high frequency is demanded.

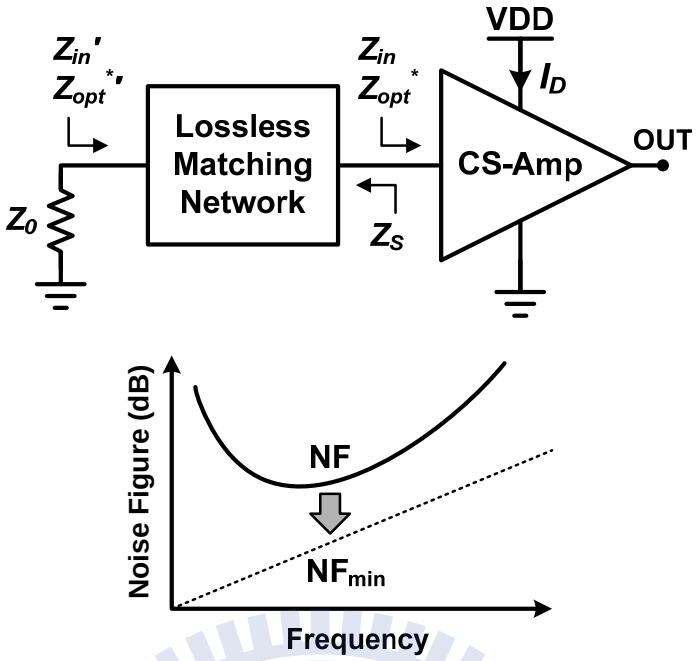


Figure 2-1. SNIM approaching for a common-source LNA.

To exploit the best noise performance from a CS amplifier, the optimal design condition of simultaneous noise and impedance matching (SNIM) should be achieved to reach the minimum noise factor (Fmin) a transistor can provide, while keeping a low voltage standing wave ratio (VSWR) at the input [3], [4]. It's a condition that the input impedance (Z_{in}) and the conjugate of the noise optimized source impedance (Z_{opt}^{*}) of a CS amplifier are simultaneously conjugate matched to an impedance Z_S, and then matched to the source impedance Z_0 by a lossless matching network, as shown in Figure 2-1. As such, the amplifier noise figure approaches to the minimum level. Typically the SNIM condition can occur with a feedback technique. A widely used one for narrowband LNA design is a CS amplifier with inductive source degeneration, which has been well analyzed [1], [5], [6]. In those papers the induced gate noise of a MOS transistor was emphasized as the root cause of mismatch between Z_{in} and Z_{opt}^{*}. Because the frequency dependency of the derived Z_{opt} is different from that of Zin, broadband SNIM (BSNIM) is not feasible using that technique. This is observed in the broadband amplifier

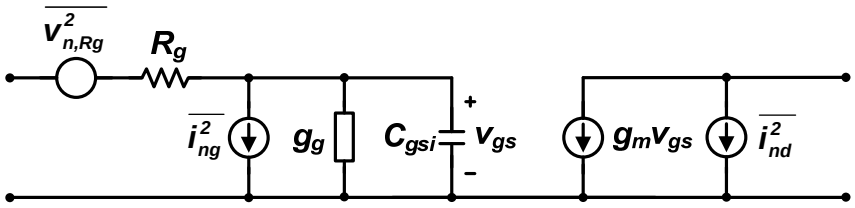


Figure 2-2. The conventional noise model for common-source based LNA design.

realized by employing a multi-order LC matching network [7], of which noise performance is still band-limited. In 2006, two UWB LNAs utilizing distinct transformer feedback structures were reported [8], [9], both showing broadband noise performance. In [8] we demonstrated the first BSNIM LNA by employing dual reactive feedback topology. We infer the work in [9] might also achieve BSNIM as two reactive feedback paths are employed in the first stage, although this was not discussed by the authors.

In this chapter the theory for BSNIM realization is discussed in details. Before the derivation it's meaningful to understand the noise model of a MOS transistor in deep submicron CMOS technology, and keep in mind under what condition the derived equations for BSNIM are valid and accurate. This will be discussed in the next section. Then we will analyze the practical mechanisms jeopardizing the ideal SNIM condition inside a CMOS transistor, including the effects of the gate resistance, gate-to-drain capacitance, and induced gate noise. Based on the derived four noise parameters, the strategies to achieve SNIM are proposed for both narrowband and broadband applications as design guidelines. In the following section a dual reactive feedback amplifier with LC ladder matching network is proposed to achieve BSNIM. The feedback circuit converges to a transformer for area compactness. This circuit topology is applied to realize a 3-11GHz ultra-wideband LNA and a 2-6GHz reconfigurable LNA [10], which will be detailed in the following chapters.

2.2 Noise Model of a MOS Transistor in Deep Submicron MOS Technology

The noise model of a long channel MOS transistor, as shown in Figure 2-2, has been widely used in the common-source based LNA design [1], [2]. Three major noise sources are indicated in this model: the channel thermal noise $\overline{i_{nd}^2}$, the induced gate noise $\overline{i_{ng}^2}$, and the gate resistance (R_g) associated noise $\overline{v_{Rg}^2}$, of which values are formulated as

$$\overline{i_{nd}^2} = 4kT\gamma g_{do} \cdot \Delta f \,, \tag{2-1}$$

$$\overline{i_{ng}^2} = 4kT\delta g_g \cdot \Delta f = 4kT\delta \frac{\omega^2 C_{gsi}^2}{5g_{do}} \cdot \Delta f \,, \tag{2-2}$$

and

$$\overline{v_{Rg}^2} = 4kTR_g \cdot \Delta f \,. \tag{2-3}$$

Here g_{do} is the drain-to-source channel conductance in **strong inversion** with zero V_{DS}. The C_{gsi} is the intrinsic gate-to-source capacitance via channel. The γ and δ are derived as 2/3 and 4/3 respectively for long channel MOS transistor. Because $\overline{i_{nd}^2}$ and $\overline{i_{ng}^2}$ are introduced by the same channel resistance, they are partially correlated to each other with the correlation factor defined as

$$corr. = \frac{\overline{i_{ng} i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} = jc_i \,, \tag{2-4}$$

in which the c_i is derived as $\sqrt{5/32}$ for long channel devices and the imaginary unit j comes from

the capacitive coupling via C_{gsi}. The directions of $\overline{i_{nd}^2}$ and $\overline{i_{ng}^2}$ in Figure 2-2 decide the sign of the correlation factor.

For deep submicron MOS transistors, short channel effects such as channel length modulation (CLM), carrier velocity saturation, and drain induced barrier lowering (DIBL) should be considered in noise model. These effects are manifest in a significant rise of the γ in (2-1). In the beginning such rise of γ was inferred attributed to the hot carrier effect [11]. In 2002 Chen and Deen showed that the increase of γ can be modeled in charge sheet model with CLM and is irrelevant to the hot carrier [12]. To include short channel effects in a simplified equation for circuit designers, Cui *et al.* tried to replace the $\gamma \cdot g_{do}$ with $\gamma_{gm} \cdot g_m$ in (2-1) [13]. However, with an increased V_{gs}, the channel thermal noise was found keeping increasing while the g_m has been saturated. This makes the γ_{gm} dependent to V_{gs} as well as transistor spice model hence not able to be predicted by hand calculation. In this section, we qualitatively interpret short channel effects in noise model to gain some insight.

Figure 2-3 is a cross-sectional view of a deep submicron MOS transistor in saturation mode with channel in moderate to strong inversion. The channel can be divided into two regions: a gradual charged region of length $L_{elec} = L_{eff} - \Delta L$ (the region I in Figure 2-3) and the velocity saturated region of length ΔL (the region II), which emerges when V_{DS} is larger than V_{DSsat}. It is found, while the region I follows Ohm's law with associated thermal noise, the region II doesn't introduce noise [12]. The noise level of a MOS transistor is determined by the charge in region I only.

If the saturation is simply caused by pinch-off, i.e., $V_{DG} > -V_{th}$, such that no charge resides in region II, the charge distribution is as the curve *a* in Figure 2-3. In such case, if $\Delta L \sim 0$, the γ,

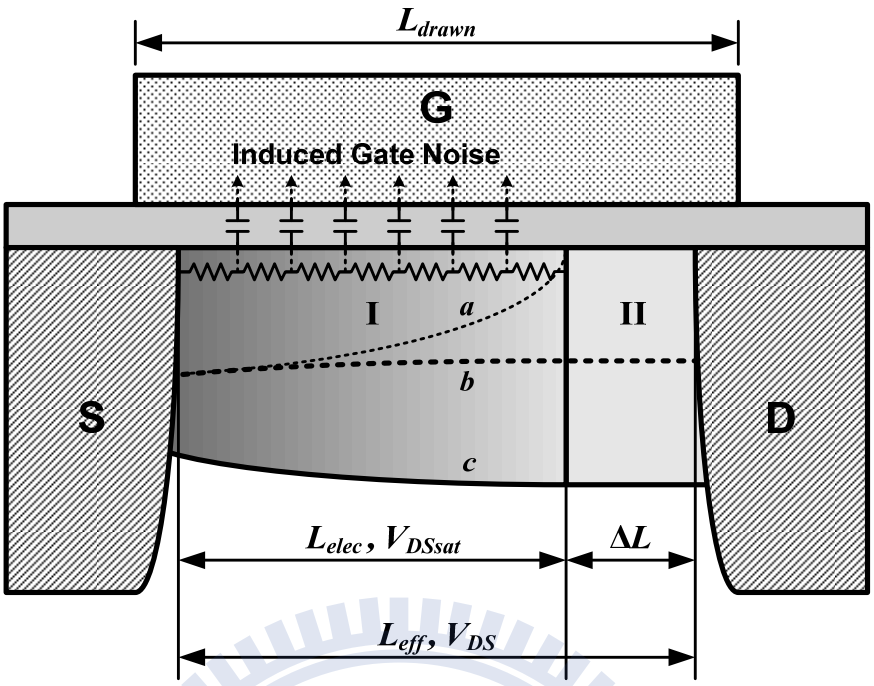


Figure 2-3. Short channel effects on FET thermal noise.

δ, and c_i of 2/3[1], 4/3, and $\sqrt{5/32}$, respectively, can be obtained for (2-1), (2-2) and (2-4). In presence of carrier velocity saturation, the drain current saturates before the pinch-off occurs, i.e., $V_{DG} < V_{th}$. There are charges resident in region II in such case but those charges are confined to the speed limit hence contribute no noise, either. The charge distribution in region I is relatively plane, like the curve *b* in Figure 2-3, such that the γ is close to 1 if $\Delta L \sim 0$.

The more significant increase in γ is caused by DIBL: the electric field by the drain voltage actually increase the charge in region I, like the curve *c* in Figure 2-3. The effect of drain voltage on the charge, as well as the corresponding γ, also saturates when $V_{DS} > V_{DSAT}$ because

[1] The γ of 2/3, derived by integrating the inverted charge, is the same 2/3 in the expression of $C_{gsi} = (2/3) \cdot WLC_{ox}$ in saturation mode.

the region II absorbs the excessive voltage drop. Therefore the γ value by DIBL depends on the CMOS process and channel length. For circuit designers the γ value can be obtained via simulation at $V_{DS}=V_{DSAT}$, if the spice model provides an accurate noise model.

The last effect to be considered is CLM. When $\Delta L > 0$ by CLM, the channel noise is also increased as

$$\overline{i_{nd}^2} = \frac{L_{eff}}{L_{elec}} \cdot \overline{i_{nd}^2}\Big|_{V_{DSAT}} . \tag{2-5}$$

With the relationship [14]

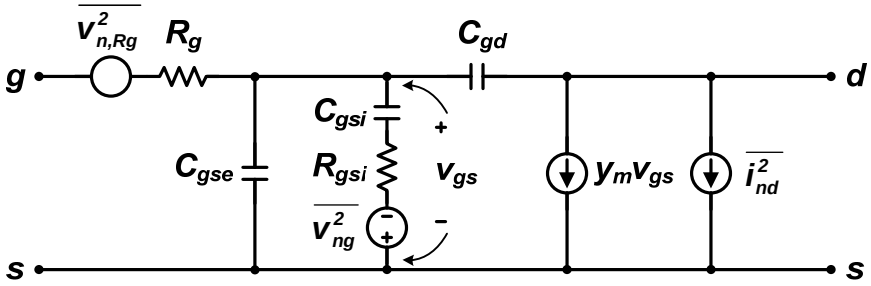
$$\frac{L_{eff}}{L_{elec}} = \frac{I_D}{I_{DSAT}}, \tag{2-6}$$

the γ in (2-1) can be rewritten to be

$$\gamma = \frac{I_D}{I_{DSAT}} \cdot \gamma\Big|_{V_{DSAT}}, \tag{2-7}$$

where I_{DSAT} is the I_D when $V_{DS} = V_{DSsat}$. The relationship in (2-6) also holds in carrier velocity saturation situation.

The induced gate noise, in contrast to the channel thermal noise, is decreased by short channel effects as the effective channel resistance in region I is decreased by the increased charge. The decrease of δ in (2-2) can be inferred in proportional to the increase of γ. Hence the induced gate noise has been argued ignorable in deep submicron process [15], [16]. However in this thesis we still preserve the effect of induced gate noise for the possible case of very high frequency applications.



$$y_m \approx g_m/(1+j\omega 2R_{gsi}C_{gsi})$$

Figure 2-4. Simplified non-quasi-static transistor model of a MOS transistor;

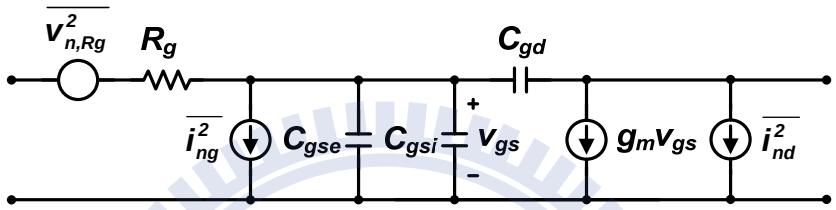


Figure 2-5. The approximated model for hand calculation.

In SPICE model the induced gate noise is the associated noise of the non-quasi-static (NQS) effect of a MOS transistor in high frequency operation [14]. Figure 2-4 shows the simplified noise model in non-quasi-static (NQS) form. The R_{gsi} is equal to the inverse of g_g in (2-2) with associated voltage noise

$$\overline{v_{ng}^2} = 4kT\delta R_{gsi} \cdot \Delta f = 4kT\delta \frac{1}{5g_{do}} \cdot \Delta f \,. \tag{2-8}$$

In addition to the associated noise sources, the metal overlap parasitic capacitances such as the gate-to-drain (C_{gd}) and the extrinsic gate-to-source (C_{gse}) capacitances are also included in this model as they are very significant in advanced CMOS technologies. The model in Figure 2-4 is useful for noise analysis in circuit simulator. However for hand calculation the approximated version with the term of induced gate noise in Figure 2-5 is more convenient. The difference between Figure 2-4 and Figure 2-5 is ignorable at frequency much smaller than $5 \cdot f_T$.

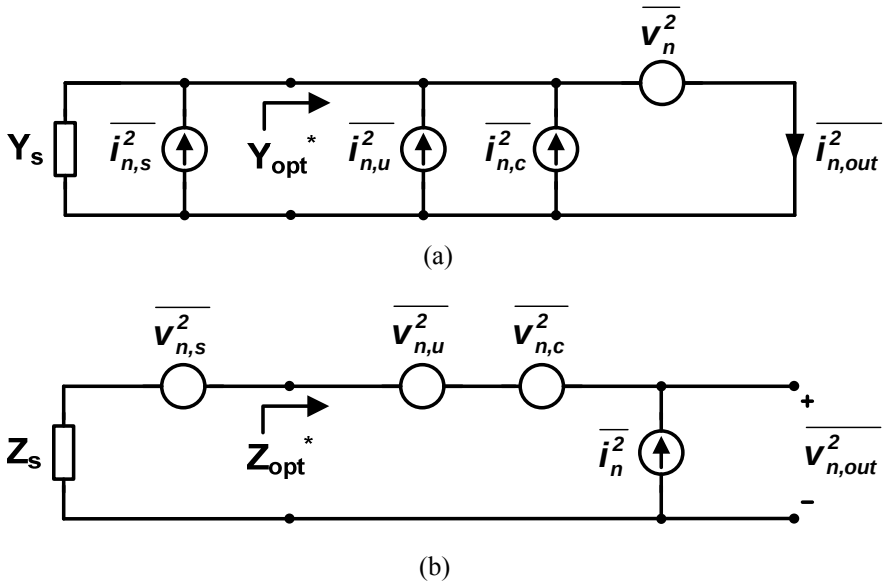


Figure 2-6. The two different representations of noise parameters: (a) Y-parameter representation; (b) Z-parameter representation.

The model in Figure 2-5 will be used for noise derivation in the succeeding sections.

One should keep in mind that the equations (2-1) and (2-2) are only valid for a MOS transistor biased in strong inversion. When it is biased in moderate inversion or weak inversion, the g_{do} is no longer adequate to evaluate the channel noise. This is because the drain voltage affects channel charge (DIBL) so significantly, sometimes even overwhelms the effect by gate voltage. In consequence, the γ associated with g_{do} becomes a function of drain voltage. In such case, the $\gamma_{gm} \cdot g_m$ instead of the conventional $\gamma \cdot g_{do}$ could be a better representation of channel noise [13].

2.3 Noise Analysis Technique for Noise Parameters

Noise parameter analysis is the most critical step to explore the solution for BSNIM. Noise parameters are those parameters indicating the effect of source impedance to noise factor. The widely used Y-parameter representation of noise parameters is derived by analyzing the output

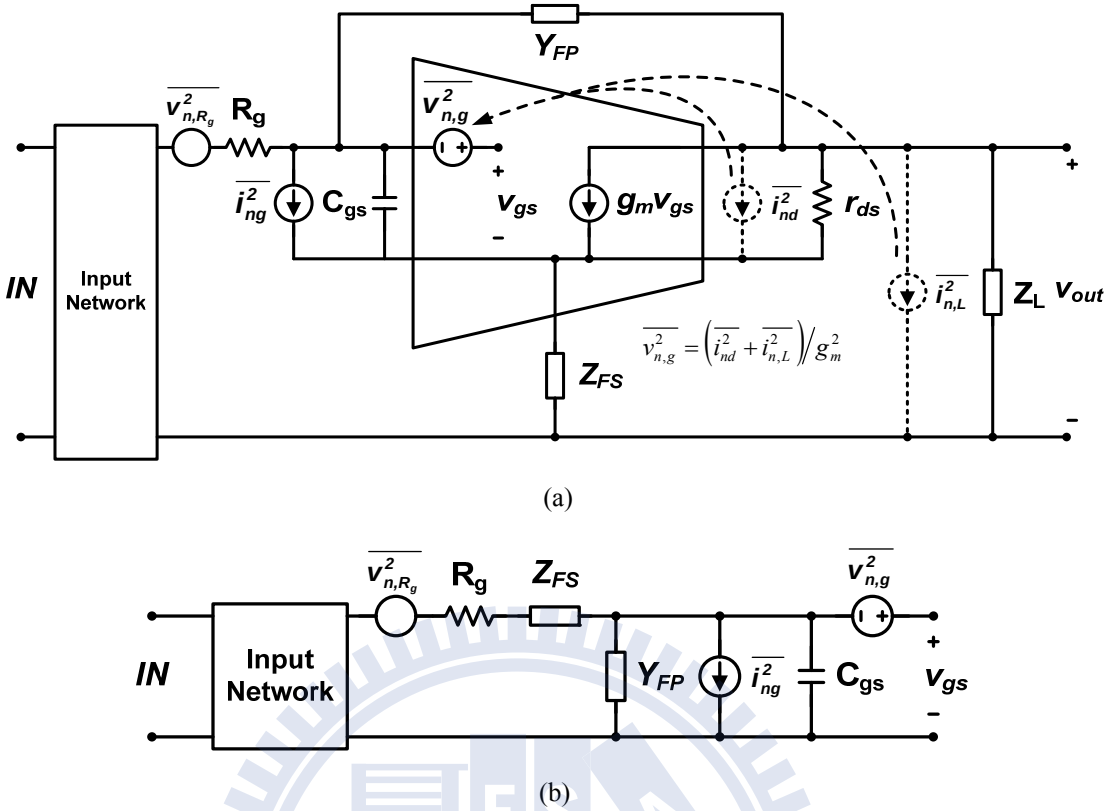


Figure 2-7. The proposed derivation technique for noise parameters: (a) The general case for the CS amplifier with lossless feedback network; (b) Equivalent circuit for noise derivation.

noise current, as shown in Figure 2-6(a). The noise factor (F) equation in noise parameters is [3]

$$F = F_{\min} + \frac{R_n}{G_S} \cdot \left| Y_S - Y_{opt} \right|^2 . \tag{2-9}$$

Here the R_n is equal to $\overline{v_n^2} / 4kT$. On the other hand noise factor can also be represented in Z-parameter by analyzing the output voltage noise, as shown in Figure 2-6(b), such that

$$F = F_{\min} + \frac{G_n}{R_S} \cdot \left| Z_S - Z_{opt} \right|^2 , \tag{2-10}$$

in which the G_n is equal to $\overline{i_n^2} / 4kT$. Shooting for BSNIM solution, the $Y_{opt}{}^*$ or $Z_{opt}{}^*$ is the term we are mostly interested with.

To accurately derive the noise parameters of an amplifier, the input-referred noise sources should be obtained first. The general measure is to calculate the corresponding output noise voltages for the short-circuited and open-circuited input individually first, then divide them by signal gain to obtain the input-referred voltage and current noise sources, respectively [17]. This generalized method, however, is not favorable to hand derivation because it makes the equations very complicated hence one is easy to loss the physical insight of components for the Z_{opt}^{*} (or Y_{opt}^{*}).

The proposed noise analysis technique for a CS amplifier with reactive feedback includes the noise model simplification and the equivalent noise source conversion. The former is illustrated in Figure 2-7. In Figure 2-7(a) is the general case of a CS amplifier with reactive feedback networks, in which the $\overline{v_{n,g}^2}$ is the equivalent gate noise source representing the noise contribution by the $\overline{i_{nd}^2}$ and $\overline{i_{n,L}^2}$, which is.

$$\overline{v_{n,g}^2} = \left(\overline{i_{nd}^2} + \overline{i_{n,L}^2}\right) \Big/ g_m^2 \ . \tag{2-11}$$

If $|Y_{FP}|$ and $|Z_{FS}|$ are much smaller than g_m and $1/g_m$, respectively, the noise model in Figure 2-7(a) can be approximated to the equivalent circuit shown in Figure 2-7(b). The derivation of input referred noise sources therefore can be simplified and starts from the input of the voltage controlled current source, i.e. the v_{gs}. It is obvious that the real parts of Y_{FP} and Z_{FS} contribute noise to the input network and deteriorate noise performance directly hence a pure reactive feedback is preferred for LNA design. When this model is projected to the transistor noise model in Figure 2-5, the C_{gd} plays the role of Y_{FP}, and the Z_{FS} is equal to 0. Noted that the equivalent circuit in Figure 2-7(b) is only for noise analysis – it cannot be used for input impedance analysis.

When referring these noise sources in Figure 2-7(b) to the input, the equivalent noise

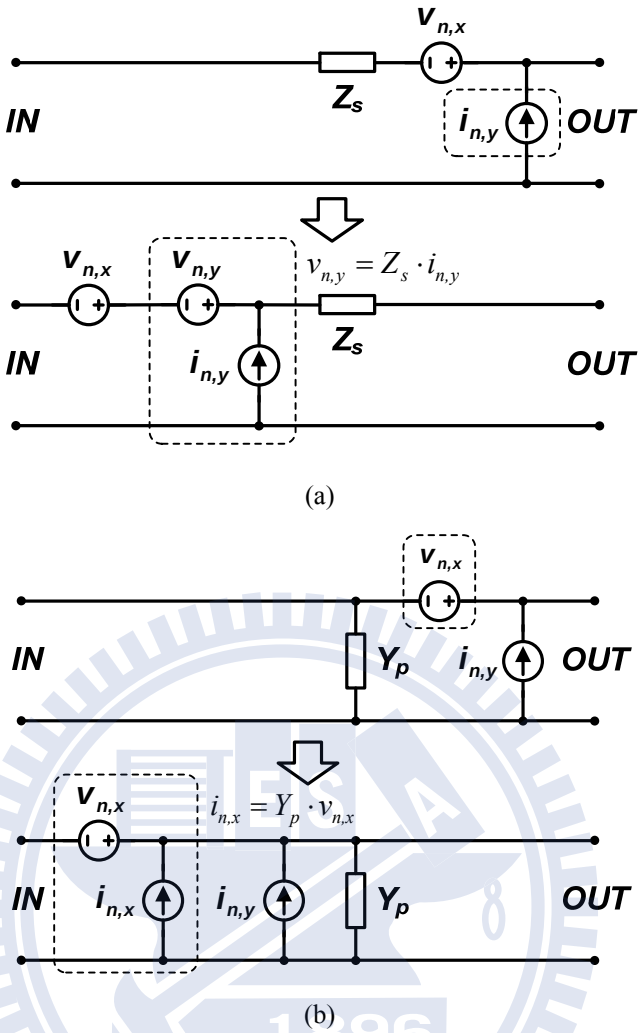


Figure 2-8. Two fundamental cases of equivalent noise sources conversion over passive devices: (a) series device; (b) shunt device.

source conversion, a derivative concept of equivalent noise fourpoles [18], can be applied. As shown in Figure 2-8(a), the shunt current noise source $i_{n,y}$ after a series passive device Z_p has input-referred noise sources including the original $i_{n,y}$ and a series voltage noise source $v_{n,y}$ fully correlated to $i_{n,y}$, whereas the series voltage noise source $v_{n,x}$ remains unchanged at input. Then the total input-referred voltage noise source $v_{n,i}$ can be obtained by combining $v_{n,x}$ and $v_{n,y}$. Note that the direction of the noise sources in Figure 2-8 carries the correlation information between noise sources.

The combination of $v_{n,x}$ and $v_{n,y}$ should be proceeded by employing vector operation, as

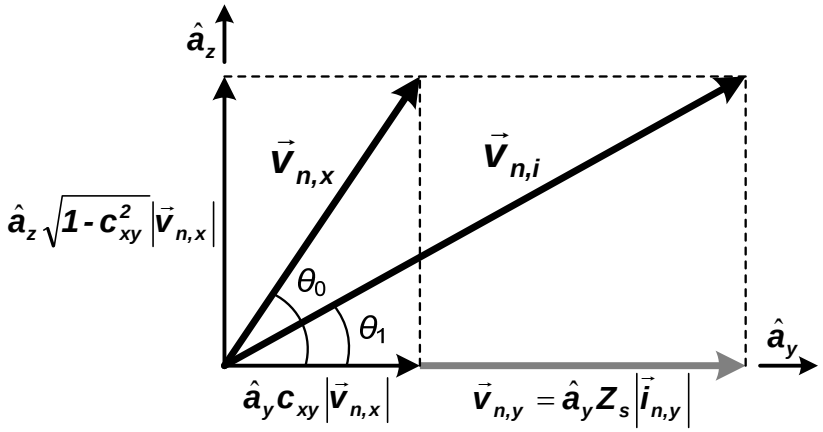


Figure 2-9. Vector operation to combine two partially correlated noise sources.

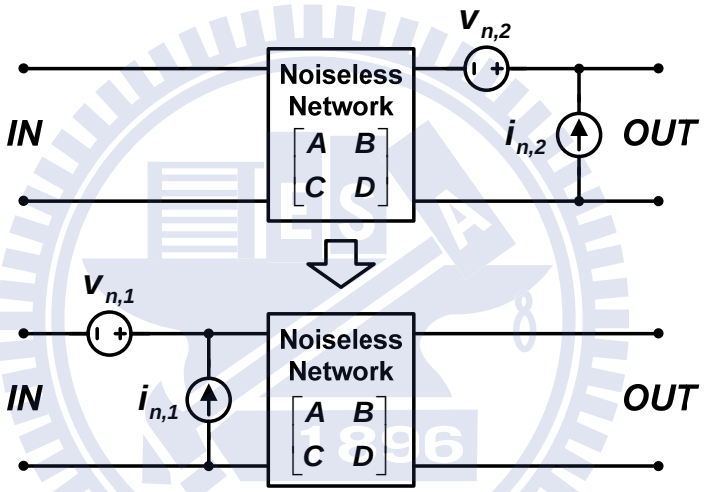


Figure 2-10. General case of equivalent noise sources conversion.

shown in Figure 2-9, whether the $v_{n,x}$ and $i_{n,y}$ are correlated to each other or not. Assume any vector along the direction of unit vector $\hat{a}_y$ is fully correlated to $i_{n,y}$, then the $v_{n,x}$ can be seen as combination of two orthogonal vectors along directions $\hat{a}_y$ and $\hat{a}_z$, in which vectors along $\hat{a}_z$ have no correlation to $i_{n,y}$. The correlation factor c_{xy} between $v_{n,x}$ and $i_{n,y}$ is equal to $\cos\theta_0$. After vector addition with $\vec{v}_{n,y}$, as shown in Figure 2-9, the total voltage noise source $v_{n,i}$ can be obtained with the correlation to $i_{n,y}$ of factor c_{iy} equal to $\cos\theta_1$.

The equivalent noise sources conversion over a shunt passive device can be derived in the

same manner, as shown in Figure 2-8(b). Noise contribution from Z_s and Y_p in Figure 2-8 can be included in the $v_{n,x}$ and $i_{n,y}$, respectively. The general form of this conversion is shown in Figure 2-10, in which

$$\begin{bmatrix} \vec{v}_{n,1} \\ \vec{i}_{n,1} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} \vec{v}_{n,2} \\ \vec{i}_{n,2} \end{bmatrix} \tag{2-12}$$

with correlation factor

$$corr. = \frac{\overline{v_{n,1} \cdot i_{n,1}^*}}{\sqrt{\overline{v_{n,1}^2} \cdot \overline{i_{n,1}^2}}} = \frac{\vec{v}_{n,1} \cdot \vec{i}_{n,1}}{\left|\vec{v}_{n,1}\right| \left|\vec{i}_{n,1}\right|} . \tag{2-13}$$

In (2-13) the dot in the numerator is the symbol of vector inner product. To reduce the unnecessary calculation complexity, it is better to keep those independent noise sources apart during derivation of the total input referred noise sources, i.e., retain noise sources in either fully correlated or uncorrelated types. Only combine those sources when necessary in the derivation. After the input referred noise sources obtained, Z_{opt}^* (or Y_{opt}^*) and other noise parameters can be accurately derived with the two-port noise theory introduced in [3].

2.4 SNIM for a CS Amplifier – The Problem and the Solution

In the microwave theory, a CS amplifier is designed either gain-optimized by impedance matching or noise-optimized by noise matching [3]. In LNA design the latter is more important since a low noise figure is demanded. The impedance matching of an LNA is simply for a minimized input reflection for a low VSWR such that the random length of a transmission line before the LNA causes no problem. Hence, the SNIM for an LNA is not to make both gain and

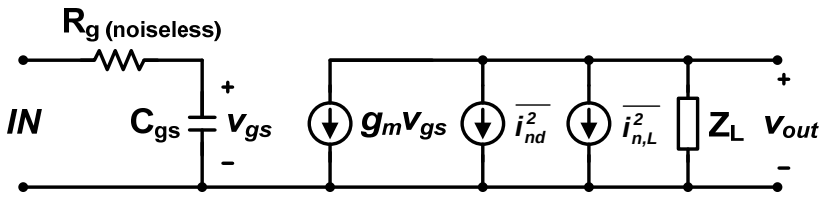


Figure 2-11. Special case of a common-source amplifier satisfying SNIM condition at all frequency.

noise optimized – it is to optimize the noise performance first, then design for a small input reflection with a feedback technique, by which the gain is slightly suppressed.

The exploration toward the BSNIM design necessitates derivation of input-referred noise sources for the noise parameters. All the noise parameters in this section are derived based on the analysis technique described in the previous section. Some reasonable simplification can be applied with the numerical approximation in the noise parameter equations. Then by analyzing Z_{in} and Z_{opt}^* the strategies for BSNIM can be mapped out.

2.4.1 Mismatch between Z_{in} and Z_{opt}^* of a CS MOS Amplifier

The mismatch between Z_{in} and Z_{opt}^* of a CS amplifier is well known but was not well analyzed. To identify the factors causing such mismatch we start our discussion from a special case that always meets the SNIM condition, i.e., $Z_{in} = Z_{opt}^*$. Consider the ideal hybrid-π model of a MOS transistor, shown in Figure 2-11, which includes $\overline{i_{nd}^2}$, $\overline{i_{n,L}^2}$, and a *noiseless* gate resistor R_g. By applying the noise analysis technique in the previous section, Z_{opt}^* of this ideal transistor can be derived to be

$$Z_{opt}^* = R_g + 1/j\omega C_{gs}, \tag{2-14}$$

and Z_{in} is

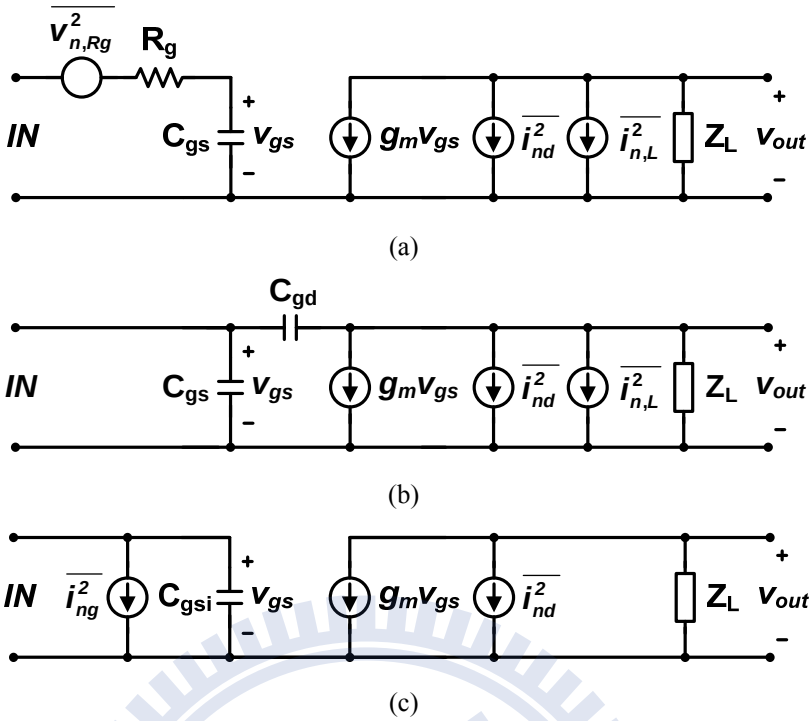


Figure 2-12. Simplified MOS transistor noise models testing effects of: (a) gate resistance; (b) C_{gd}; (c) gate induced current noise.

$$Z_{in} = R_g + 1/j\omega C_{gs}. \tag{2-15}$$

Obviously Z_{opt}^* equals to Z_{in} at all frequency. Therefore Z_{opt}^* and Z_{in} can be both tuned and matched to Z_0 (typically 50Ω) simultaneously with a lossless matching network to meet the SNIM condition.

In the practical case, as shown in Figure 2-5, Z_{opt}^* and Z_{in} are found apart from each other by three major factors, referred to as Z_{in}-*to*-Z_{opt}^* *discrepancy factors*: 1) independent noise sources at the gate, 2) gate-to-drain capacitance, and 3) induced gate noise. Effects of these three factors can be observed individually by the three test cases as shown in Figure 2-12.

The first one is the independent noise sources at the gate port. The typical one is the gate resistance noise $\overline{v_{n,Rg}^2}$. Using the noise model as shown in Figure 2-12(a), the analysis shows that Z_{opt}^* is significantly changed and derived as

$$Z_{opt}^{*} = \sqrt{R_g^2 + \frac{4kTR_g\Delta f}{\overline{i_{n,d}^2} + \overline{i_{n,L}^2}} \cdot \left(\frac{g_m}{\omega C_{gs}}\right)^2} + \frac{1}{j\omega C_{gs}}. \tag{2-16}$$

In comparison to (2-14), the noise source $\overline{v_{n,Rg}^2}$ increases the real part of Z_{opt}^{*} with a frequency-dependent term and thus makes Z_{opt}^{*} larger than Z_{in}. This factor is found to be the primary factor to Z_{in}-*to*-Z_{opt}^{*} discrepancy in most CMOS LNA design. The noise from a non-ideal input matching network also contributes the same effect.

The second factor is the parasitic feedback via gate-to-drain capacitance C_{gd}. The feedback loop gain changes Y_{in} (the inverse of Z_{in}) without affecting Y_{opt}^{*} (the inverse of Z_{opt}^{*}). Consider the simplified transistor noise model with R_g= 0 as in Figure 2-12(b). It can be found that

$$Y_{opt}^{*} = j\omega\,(C_{gs} + C_{gd}), \tag{2-17}$$

and

$$Y_{in} = j\omega C_{gs} + j\omega C_{gd}\frac{1 + g_m Z_L}{1 + j\omega C_{gd} Z_L}. \tag{2-18}$$

With Miller effect, the loading of impedance Z_L modifies C_{gd} in Y_{in} via the C_{gd} feedback.

The third factor is the induced gate noise. Consider the noise model with R_g= 0 as in Figure 2-12(c). C_{gse}, C_{gd}, and $\overline{i_{n,L}^2}$ are ignored. The derived Y_{opt}^{*} is approximately as

$$Y_{opt}^{*} \approx \omega C_{gsi} \cdot \alpha\sqrt{\frac{\delta}{5\gamma}\left(1 - c_i^2\right)} + j\omega C_{gsi}\left(1 - c_i \cdot \alpha\sqrt{\frac{\delta}{5\gamma}}\right), \tag{2-19}$$

in which α=g_m/g_{do}. It is beneficial to define the output noise contribution ratio of $\overline{i_{ng}^2}$ to $\overline{i_{nd}^2}$ as

$$\kappa = \sqrt{\frac{\overline{i_{ng}^2} \cdot \left(g_m / \omega C_{gsi}\right)^2}{\overline{i_{nd}^2}}} = \alpha \sqrt{\frac{\delta}{5\gamma}}. \tag{2-20}$$

Y_{opt}^* in (2-19) then can be simplified as

$$Y_{opt}^* \approx \omega C_{gsi} \kappa \sqrt{1 - c_i^2} + j\omega C_{gsi}\left(1 - c_i \kappa\right). \tag{2-21}$$

By comparing this Y_{opt}^* with the corresponding Y_{in}, equal to $j\omega C_{gs}$, the induced gate noise is found reducing the effective capacitance of Y_{opt}^* and introduces a frequency dependent real part on Y_{opt}^*.

Now consider the equivalent circuit in Figure 2-5 with R_g and Z_L both equal to zero. Define ρ as the noise contribution ratio,

$$\rho = \sqrt{\overline{i_{nd}^2} \Big/ \left(\overline{i_{nd}^2} + \overline{i_{n,L}^2}\right)}, \tag{2-22}$$

a value smaller than 1. Y_{opt}^* can be derived as

$$Y_{opt}^* \approx \omega C_{gsi} \rho \kappa \sqrt{1 - \left(\rho c_i\right)^2} + j\omega\left(C_{gs} + C_{gd} - \rho^2 c_i \kappa C_{gsi}\right). \tag{2-23}$$

By comparing (2-23) with (2-21) it can be observed that C_{gse}, C_{gd}, and $\overline{i_{n,L}^2}$ all mitigate the effect of $\overline{i_{ng}^2}$ on Y_{in}-*to*-Y_{opt}^* discrepancy.

With all the three factors and $\overline{i_{n,L}^2}$ considered, it can be derived that

$$Z_{opt}^* = \sqrt{R_g^2 + \left(\frac{4kTR_g \Delta f}{\overline{i_{nd}^2} + \overline{i_{n,L}^2}} g_m^2 + 1 - c_1^2\right) \frac{1}{\omega^2 C_N^2}} + \frac{c_1}{j\omega C_N}, \tag{2-24}$$

in which

$$C_N = \sqrt{\left(C_{gs} + C_{gd}\right)^2 - 2\rho^2 c_i \kappa C_{gsi}\left(C_{gs} + C_{gd}\right) + \rho^2 \kappa^2 C_{gsi}^2} \tag{2-25}$$

and

$$c_1 = \sqrt{1 - \frac{\left(1 - \rho^2 c_i^2\right)\rho^2 \kappa^2 C_{gsi}^2}{C_N^2}}\,. \tag{2-26}$$

With the typical device values in 0.18um CMOS technology, C_N and c_1 are about $0.94\cdot(C_{gd}+C_{gd})$ and 0.98, respectively. More than 99.5% of $Re\{Z_{opt}^{*}\}$ comes from its second term in (2-24). Hence Z_{opt}^{*} can be approximated as

$$Z_{opt}^{*} \approx \frac{g_m}{\omega(C_{gs} + C_{gd})}\sqrt{\frac{4kTR_g\Delta f}{\overline{i_{nd}^2} + \overline{i_{n,L}^2}}} + \frac{1}{j\omega(C_{gs} + C_{gd})}\,. \tag{2-27}$$

If $\overline{i_{n,L}^2}$ is assumed frequency-independent, Z_{opt}^{*} has a *frequency-independent quality factor*. Hence in Smith Chart the S_{opt}^{*} curve follows the constant-Q contour, completely different to the behavior of a normal RC network.

The other noise parameters are obtained as well. In the Z-parameter representation of the noise factor of

$$F = F_{\min} + \frac{G_n}{R_S}\cdot\left|Z_S - Z_{opt}\right|^2, \tag{2-28}$$

the G_n and F_{min} are

$$\begin{aligned} G_n &= \frac{\overline{i_{nd}^2} + \overline{i_{n,L}^2}}{4kT\Delta f}\cdot\frac{\omega^2 C_N^2}{g_m^2} \\ &= \frac{\gamma}{\alpha}\frac{\omega^2 C_N^2}{g_m} + \frac{\overline{i_{n,L}^2}}{4kT\Delta f}\cdot\frac{\omega^2 C_N^2}{g_m^2} \end{aligned} \tag{2-29}$$

and

$$\begin{aligned} F_{\min} &= 1 + 2G_n\left(\mathrm{Re}\{Z_{opt}\} + R_g\right) \\ &\approx 1 + 2G_n\,\mathrm{Re}\{Z_{opt}\} \end{aligned}. \tag{2-30}$$

For quick evaluation, $F_{\min}$ can be simplified by ignoring $\overline{i_{n,L}^2}$ as

$$F_{\min} \approx 1 + 2\frac{\omega\left(C_{gs} + C_{gd}\right)}{g_m}\sqrt{\frac{\gamma}{\alpha}g_m R_g}\ . \tag{2-31}$$

From (2-31) we can see R_g not only introduces Z_{in}-to-Z_{opt}^* discrepancy but also directly deteriorates $F_{\min}$. R_g is therefore identified as the dominant noise contributor to an LNA. On the other hand, Z_{in} is derived as

$$Z_{in} = R_g + \frac{1}{j\omega C_{gs} + j\omega C_{gd}\dfrac{1 + g_m Z_L}{1 + j\omega C_{gd} Z_L}}. \tag{2-32}$$

The accuracy of (2-24)–(2-26) was verified with several test cases by MATLAB and Agilent ADS. The calculated S_{opt}^* (S-parameter of Z_{opt}^*) well matches the simulated S_{opt}^*. Representative results are plotted in Figure 2-13. In this test case the component parameters in the model of Figure 2-5 were extracted from a 0.18μm NMOS transistor operated in strong inversion and saturation mode, then applied to (2-24) for calculation and the model in Figure 2-5 for simulation. The simulation result with the foundry noise model is also included as reference. Different test conditions are applied to analyze the factor effects. As can be seen, the calculation result fits the simulation results very well. The S_{opt}^* curve behaves as a constant-Q curve, showing a strongly frequency-dependent $\mathrm{Re}\{Z_{opt}^*\}$, not matched to the S_{11} curve at all. The R_g dominates the real part discrepancy, whereas the induced gate noise $\overline{i_{ng}^2}$ has just marginal effect on S_{opt}^*. Different values of Z_L are used to observe the effect of C_{gd} feedback on

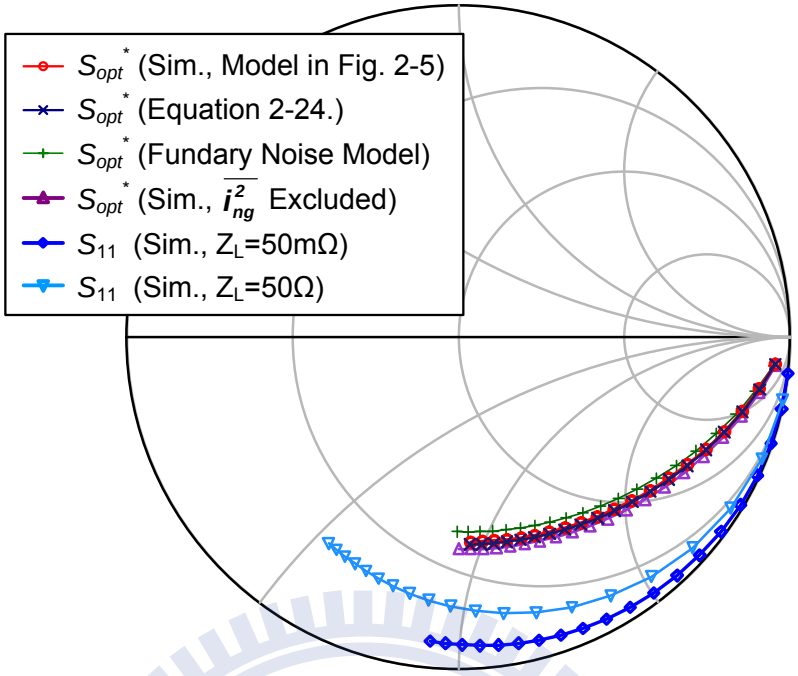


Figure 2-13. Equation verification of Zopt* and the analysis of discrepancy facter effects on Smith Chart. Frequency swept from 1 to 20GHz with 1GHz step.

Z_{in}. It can be observed that Im$\{Z_{in}\}$ is significantly affected by a resistive Z_L because of the C_{gd} feedback, while the Re$\{Z_{in}\}$ is also slightly affected, as can be predicted from (2-32). In addition, if a reactive Z_L is applied, a capacitive Z_L provides an additional noiseless resistance whereas an inductive Z_L conducts a positive feedback causing an unstable resonance. The former can be utilized for BSNIM as described in next section.

By comparing Z_{opt}^* and Z_{in} among (2-24), (2-27) and (2-32), respectively, their difference can be briefly summarized as:

1) To the real part, the noise contributed by R_g makes $Re\{Z_{opt}^*\}$ much larger than $Re\{Z_{in}\}$ by a frequency-dependent amount.

2) To the imaginary part, with a resistive Z_L the C_{gd} feedback makes $Im\{Z_{in}\}$ smaller than $Im\{Z_{opt}^*\}$. When represented by series capacitance, the equivalent series capacitance in Z_{in}

is larger than that in Z_{opt}^{*}.

The other important factor concerned is the gain of the first amplifying stage. If the gain is not high enough to suppress noise contribution of succeeding stages, a larger $\overline{i_{n,L}^2}$ will be introduced and in consequence $F_{\min}$ is deteriorated, too.

2.4.2 Strategies to Achieve BSNIM

With the mechanism of Z_{in}-to-Z_{opt}^{*} discrepancy identified, strategies to achieve BSNIM for minimized noise figure can be mapped out. For the real part, because $Re\{Z_{in}\}$ is smaller than $Re\{Z_{opt}^{*}\}$, the difference can be compensated by introducing a noiseless resistance with a reactive feedback technique. As to the imaginary part, it is critical to minimize the impact on the series capacitance expansion of Z_{in} induced by C_{gd} and the real part of Z_L. From (2-27) and (2-32), it is necessary to meet the following condition as

$$\mathrm{Re}\{Z_L\} << \frac{1}{g_m} \text{ and } \mathrm{Re}\{Z_L\} << \frac{1}{\omega C_{gd}}. \tag{2-33}$$

The proposed SNIM strategy matches Z_{opt}^{*} to the source impedance Z_0 first, then uses reactive feedback to match Z_{in} to Z_0 without affecting Z_{opt}^{*} and the minimum noise figure. For a narrowband LNA at frequency f_0, the design criteria for SNIM are summarized as follows:

1) Apply the least channel length for the best transistor performance. From (2-31) the $F_{\min}$ increases roughly with $\left(C_{gs}+C_{gd}\right)\sqrt{R_g/g_m}$, which can be minimized with the least channel length.

2) The real part of Z_L should be as small as possible, not to expand the difference between $Im\{Z_{in}\}$ and $Im\{Z_{opt}^{*}\}$. This difference introduces a frequency offset between the impedance and noise matching.

3) Given specified drain current, co-design the transistor size and matching network to make Z_{opt}^{*} matched to the source impedance Z_0 at f_0.

4) Increase $Re\{Z_{in}\}$ to match Z_0 without adding noise and changing $Re\{Z_{opt}^{*}\}$. This can be achieved by employing reactive feedback technique. The well known is the *inductive source degeneration* technique.

For a prescribed DC drain current (power constraint), Z_{opt}^{*} is adjusted by varying the transistor size. If the transistor size is increased, g_m increases, R_g decreases, and f_T decreases. From (2-27) and (2-31), $Re\{Z_{opt}^{*}\}$ decreases but F_{min} increases. Nonetheless, such F_{min} increase is insignificant as compared to the noise factor improvement by noise matching[2]. For applications of $f_0 << f_T$, such adjustment leads to an extremely low transistor current density (weak inversion), which may severely suffer from process variation and induce unacceptable non-linearity. In such case an external capacitor in parallel to the transistor C_{gs} to lower f_T is favorable. Similarly it increases F_{min} slightly but helps keep noise matching with a transistor in moderate inversion.

For broadband applications, both Z_{opt}^{*} and Z_{in} need to be close to Z_0 over the entire bandwidth. This requires a high-order input matching network. Equation (2-27) and (2-32) show the frequency dependencies of $Re\{Z_{opt}^{*}\}$ and $Re\{Z_{in}\}$ are different. Hence the reactive feedback, as described in the item *4)* above, needs to increase $Re\{Z_{in}\}$ by a frequency dependent amount. This can be realized by employing *multiple reactive feedbacks* to make $Re\{Z_{in}\}$ close to $Re\{Z_{opt}^{*}\}$ in different frequency regions. Consequently, the design criteria for BSNIM are proposed as follows:

---

[2] If large amount of DC power is employed such that the G_n in (2-29) is very small, the noise matching is less appreciable. However, this is not the power efficient case that the SNIM approach is pursuing.

1) Same as the item *1)* in narrowband case.

2) Minimize Z_L or employ a capacitive Z_L.

3) With the drain current specified, the transistor size is chosen to make $Re\{Z_{opt}^*\}$ of the transistor close to the source impedance Z_0 at the center frequency f_c of the pass band. Apply a high-order input matching network (typically a ladder LC network structure) to make Z_{opt}^* close to Z_0 in the entire band.

4) Increase $Re\{Z_{in}\}$ to match Z_0 by employing *multiple reactive feedbacks*.

While multiple reactive feedbacks are necessary for BSNIM, they actually create a high-order impedance function of Z_{in} as a consequence. However the order of Z_{opt}^* is not changed because Z_{opt}^* is not affected by the noiseless reactive feedbacks. As such Z_{in} and Z_{opt}^* behave differently on the frequency response. Nevertheless, such difference can be taken care of by the high order input matching network if Z_{in} and Z_{opt}^* are both designed close to Z_0.

The procedure described above creates a BSNIM LNA which ensures power-efficient noise performance. In the next section an exemplary *dual reactive feedbacks technique* will be proposed as a BSNIM solution, which has been proven effective for broadband LNA design from 3- to 11-GHz (fractional bandwidth larger than 130%). In comparison to the area-saving but power-hungry resistive/ source-follower feedback amplifier [19]–[22], a SNIM/BSNIM LNA saves lots of power.

2.5 The Proposed BSNIM Amplifier

As discussed above, a BSNIM LNA necessitates a high-order matching network and multiple reactive feedbacks. The proposed BSNIM solution is a LC-ladder matching network

[23] along with a dual reactive feedback topology, composed of a capacitive shunt feedback and an inductive series feedback, as shown in Figure 2-14. The LC-ladder matching network and the dual reactive feedback are co-designed following the BSNIM design criteria in the previous section. Of the dual reactive feedback each feedback attains SNIM in different frequency region for BSNIM. They are seamlessly combined by employing an inductor L_d at the transistor drain port to obtain different loading conditions for each feedback structure. To quantitatively illustrate the design concept, the 3.1 to 10.6GHz UWB LNA designed in 0.18μm CMOS is applied as an example.

2.5.1 The Proposed Dual Reactive Feedback Topology

The proposed dual reactive feedback structure and the LC ladder input matching network results in Z_{opt}^* represented by the equivalent circuit as shown in Figure 2-15. Z_{opt}^* is not affected by the lossless reactive feedbacks[3]. The Z_{opt}^*-to-Z_0 matching bandwidth is extended by the second-order band-pass LC-ladder structure. The choice of component values follows the guideline as

$$L_1 \cdot C_1 = (L_g + L_s) \cdot (C_{gs} + C_{gd}) = 1/(2\pi f_c)^2 , \tag{2-34}$$

in which f_c is located at 5.76GHz, the geometric mean of 3.1GHz and 10.6 GHz, in this design. The bandwidth expansion is determined by the L/C ratios, of which the preliminary values can be obtained by the traditional filter design technique such as Chebyshev filter design. Slight

[3] Z_{opt}^* is slightly affected by lossless feedbacks because of the degraded gain if the noise from loading stages, i.e. $\overline{i_{n,L}^2}$, is included. Nonetheless, such effect is ignorable if this stage provides a sufficient gain.

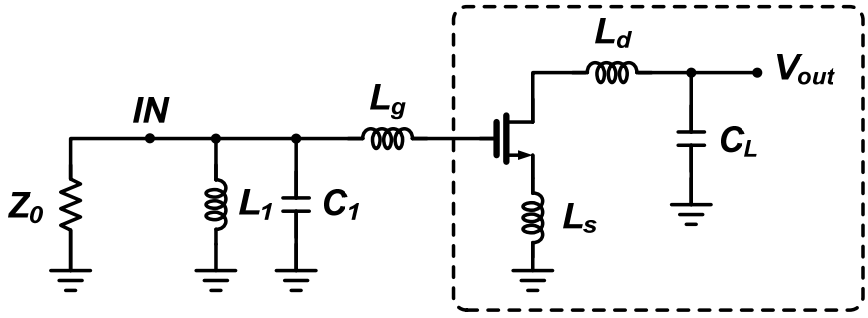


Figure 2-14. Proposed BSNIM solution. It consists of a LC ladder matching network and a dual reactive feedback structure, a combination of capacitive shunt feedback and inductive series feedback. The drain inductor L_d is employed for feedback selection and provides band extension on v_{out}.

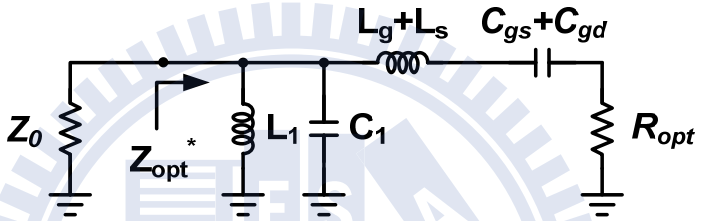
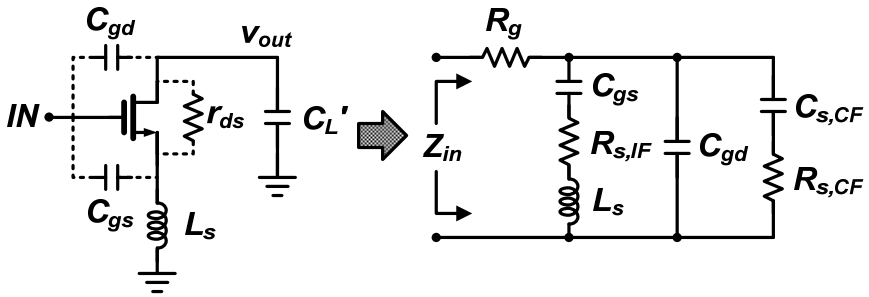


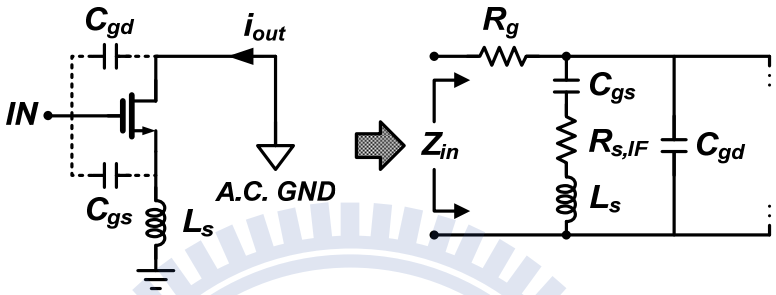
Figure 2-15. Equivalent circuit of Z_{opt}^*.

trimming on LC values can compensate for the frequency dependency of R_{opt} without problem. For the optimal broadband matching result, R_{opt} is in general designed slightly less than Z_0 to make the S_{opt}^* curve circling the Smith Chart center over the entire pass-band. The design of L_1 and C_1 also takes into account the gain response as described later.

While the broadband noise matching is achieved, the input impedance is also matched to Z_0 by the proposed dual reactive feedback circuit, as shown in the dashed-line box of Figure 2-14. A similar circuit structure was proven having the capability of broadband input impedance matching [24]. But different from [24], the proposed approach here is to utilize each reactive feedback in different frequency regions. Such configuration can well minimize the difference between $Re\{Z_{in}\}$ and $Re\{Z_{opt}^*\}$ over a wide frequency range and therefore enables BSNIM. In the frequency region much lower than the L_d-C_L series resonance frequency, the



(a)



(b)

Figure 2-16. Input impedance changed among the two feedbacks with frequency: (a) capacitive shunt feedback in lower frequency region; (b) inductive series feedback in higher frequency region.

L_d-C_L tank behaves like a capacitor C_L' to the transistor. Hence Z_{in} can be represented by the equivalent circuit shown in Figure 2-16(a), in which

$$R_{s,IF} = \frac{g_m \cdot L_s}{C_{gs}}, \tag{2-35}$$

$$R_{s,CF} = \frac{C_L'+C_{gd}}{g_m C_{gd}} \approx \frac{C_L + C_{gd}}{g_m C_{gd}}, \tag{2-36}$$

and

$$C_{s,CF} = g_m r_{ds} \cdot C_{gd}. \tag{2-37}$$

Two noiseless resistances can be found: $R_{s,IF}$ from the series inductive feedback of L_s, and $R_{s,CF}$ from the shunt capacitive feedback of C_{gd} with C_L'. Because $C_{s,CF}$ in (2-37) is much larger

than C_{gs}, the branch of $C_{s,CF}$ dominates the input impedance in this frequency region such that $R_{s,CF}$ is the noiseless resistance contributing to $Re\{Z_{in}\}$ to match with R_{opt}.

In the higher frequency region close to the L_d-C_L resonance, the output appears as a short circuit to the drain. Z_{in} can be represented by the equivalent circuit as shown in Figure 2-16(b). The $C_{s,CF}$ branch becomes open because the C_{gd} feedback loop gain is approximately zero. The series inductive feedback is significant under such a condition such that $R_{s,IF}$ is the dominant noiseless resistance in this frequency region.

As shown in (2-27), R_{opt} of the transistor is inversely proportional to frequency. The variation ratio is larger than 3 over the entire frequency range of interest. To make $Re\{Z_{in}\}$ match with R_{opt}, $R_{s,IF}$ is designed about a half of $R_{s,CF}$, yielding to the required $Re\{Z_{in}\}$ variation. In practice, the $C_{s,CF}$ branch in Figure 2-16(a) has a low Q property such that the capacitive feedback is active over a good portion of the frequency range.

The placement of L_1, C_1, and L_g takes care of $Im\{Z_{in}\}$, making Z_{in} also close to Z_0 over the entire frequency range. Actually L_g results in two resonance frequencies with the transistor circuit. At low frequencies of capacitive feedback, L_g and $C_{s,CF}$ constitute a resonance tank with the resonance frequency of

$$f_{0,CF} = 1/2\pi\sqrt{L_g C_{s,CF}} = 1/2\pi\sqrt{L_g \cdot g_m r_{ds} \cdot C_{gd}}\ . \tag{2-38}$$

For the inductive feedback, the resonance frequency is located at a higher frequency at

$$f_{0,IF} = 1/2\pi\sqrt{(L_g + L_s)\cdot(C_{gs} \,||\, C_1)}\ . \tag{2-39}$$

Therefore the frequency dependence of Z_{in} turns out to be an order higher than that of Z_{opt}. In this design $f_{0,CF}$ and $f_{0,IF}$ are located at 5GHz and 9GHz, respectively. As to the choice of L_d, it is expected to tune out C_L to accommodate the inductive feedback hence

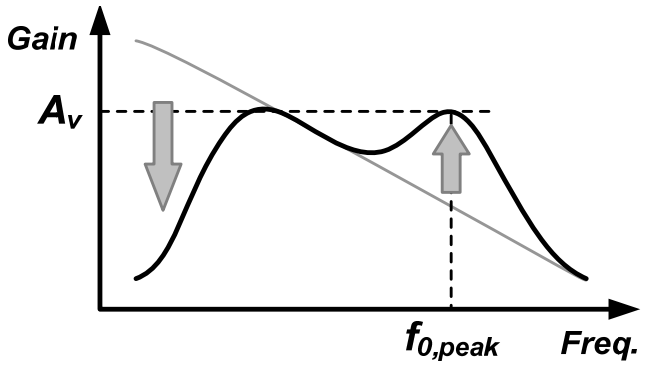


Figure 2-17. Gain response of the proposed BSNIM amplifier. The low-frequency gain is suppressed by L_1 and the high-frequency gain is enhanced by L_d.

$$L_d \cdot C_L \approx 1/(2\pi f_{0,IF})^2 . \tag{2-40}$$

2.5.2 Gain Response

As mentioned in the previous section, a sufficiently high gain over the entire band is necessary to suppress the noise contribution of $\overline{i_{n,L}^2}$. The proposed BSNIM amplifier is expected to fulfill such a gain requirement. Its design concept is shown in Figure 2-17. The gain response is mainly shaped by the drain network in Figure 2-14 as the input network is a broadband structure. Based on the low-pass response by C_L (the gray curve in Figure 2-17), L_d conducts a series gain peaking at the frequency

$$f_{0,Peak} = 1/2\pi\sqrt{L_d \cdot (C_{gd} \parallel C_L)} , \tag{2-41}$$

which is higher than $f_{0,IF}$ in (2-39). The voltage gain at this frequency can be derived with the circuit approximation as shown in Figure 2-18, in which

$$R_d' \approx \frac{C_{gs} + C_{gd}}{g_m C_{gd}} . \tag{2-42}$$

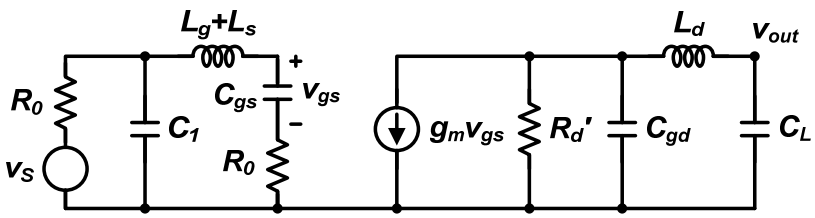


Figure 2-18. Equivalent circuit for gain derivation at $f_{0,Peak}$.

As to the gain in the lower out-of-band frequency, it is suppressed by the input shunt inductor L_1. As a result a gain peak is formed at the lower band edge. The magnitude of this peak is designed close to the peak gain at the higher band edge such that the expected gain response is as the solid curve in Figure 2-17. With this design guideline the voltage gain is determined at $f_{0,Peak}$, which is designed at 11GHz.

The gain response of this amplifier is composed of the two gain peaks at both band edges. Hence if a flat gain over a very wide bandwidth is demanded, an additional mid-band gain expansion by the next stage is necessary to compensate the mid-band depression. Such a case applies to the 3–11GHz UWB LNA. On the other hand, if the required bandwidth is just moderately wide such like the 2–6GHz application in [10], a flat gain response is obtainable by this stage itself as the two gain peaks can be designed fairly close to each other.

2.5.3 Transformer for Inductive Series Feedback

The proposed dual reactive feedback amplifier as shown in Figure 2-14 demands four inductors, which may occupy huge die area. To reduce the inductor number, the transformer feedback topology is proposed to replace the three inductors L_g, L_d, and L_s, as shown in Figure 2-19(a). In transformer feedback the L_g' and L_d are overlapped, sharing the same die area and having a mutual inductance M to constitute a transformer. The mutual inductance M senses the drain current and contributes a series voltage feedback at the input, which provides the same

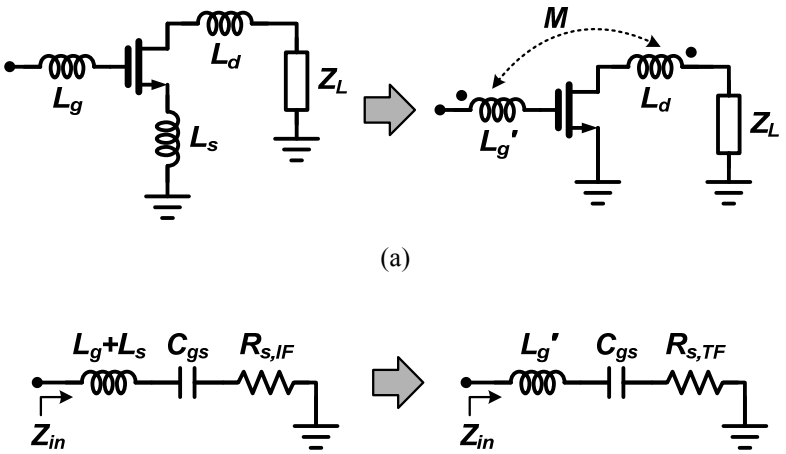


Figure 2-19. Substitution of the inductive source degeneration by the transformer feedback: (a) The topologies; (b) Their equivalent circuit for input impedance.

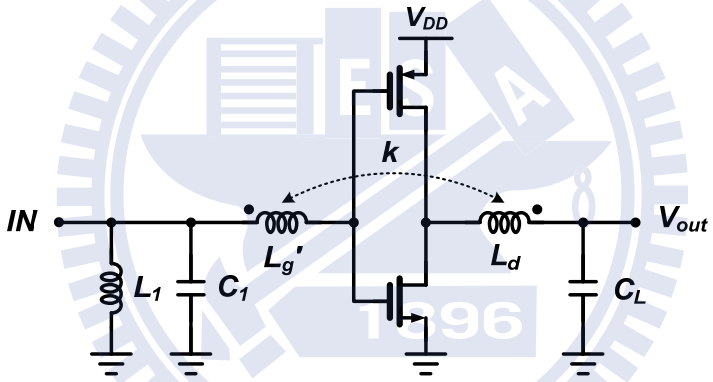
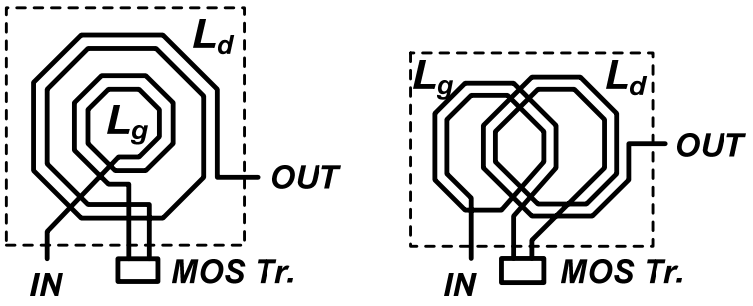


Figure 2-20. The proposed BSNIM amplifier with transformer feedback.

series-series feedback function as L_s in the inductive source degeneration amplifier. By assuming the C_{gd} feedback effect and the transformer feed-forward coupling effect both ignorable at the frequency of interest, the input impedance can be approximately represented by the equivalent circuit as shown in Figure 2-19(b), in which $L_g' = L_g + L_s$ and

$$R_{s,TF} = \frac{g_m \cdot M}{C_{gs}}, \tag{2-43}$$

which provides the wanted noiseless resistance. The above assumption is valid for the general



(a) (b)

Figure 2-21. Possible layout schemes of a weak coupling transformer: (a) common- centroid coil; (b) overlapping coil.

source inductive degenerated amplifier design.

The transformer feedback topology is also advantageous that the transistor source is connected to ground directly. This allows the amplifier be implemented in CMOS inverter structure, which employs both NMOS and PMOS to reuse drain current for a larger transconductance. The final shape of the proposed BSNIM amplifier is therefore shown in Figure 2-20. Here the mutual inductance is represented by the coupling factor k with the relation $M = k\sqrt{L_g' \cdot L_d}$.

Because M is generally much smaller than L_g' and L_d, the coupling factor k is much smaller than 1. Based on design simulations, the optimal k value is slightly less than 0.2. Possible layout schemes of such a weak coupling transformer include the common-centric coils and the overlapped coils, as shown in Figure 2-21. Generally the common-centric coils have a better quality factor but occupy more die area. In the design example in the next section, the common-centric coil was adopted for a better performance.

2.6 Summary

The SNIM technique is important to power-efficient noise performance of a LNA, especially for those critical applications. A successful approach for broadband simultaneous noise and impedance matching (BSNIM) on a CS amplifier is demonstrated. The root causes of Z_{in}-to-Z_{opt}^{*} discrepancy of a MOS transistor are analyzed and the SNIM/BSNIM design criteria are mapped out accordingly. Reactive feedbacks to equalize the real part of Z_{in} and Z_{opt}^{*} are the essential solution for SNIM. The proposed BSNIM technique employs dual reactive feedbacks and a LC ladder matching network to handle a wide bandwidth. Band handover between the two reactive feedbacks is conducted by a drain inductor L_d. A transformer feedback is further developed to provide the same series-series feedback with a reduced form factor. In the succeeding chapters, LNAs utilizing the proposed BSNIM amplifier will be demonstrated.

Chapter 3

A 3–11GHz Ultra-Wideband Low-Noise Amplifier

3.1 Introduction

As approved by FCC, the Ultra-Wideband (UWB) system using the unlicensed frequency band from 3.1- to 10.6-GHz is bringing up much interest of broadband wireless communications. For such broadband applications, the low noise amplifier (LNA) in the UWB receiver must provide input impedance matching and gain flatness over the entire frequency band. Furthermore its noise figure performance shall meet broadband noise matching such that the nominal system noise figure of the UWB receiver shall be less than 7dB as required [25].

In this chapter a CMOS UWB LNA utilizing the BSNIM amplifier proposed in the previous chapter is demonstrated. The LNA circuit achieves almost the same noise figure level to the minimum noise figure (NFmin) over the entire frequency band of interest.

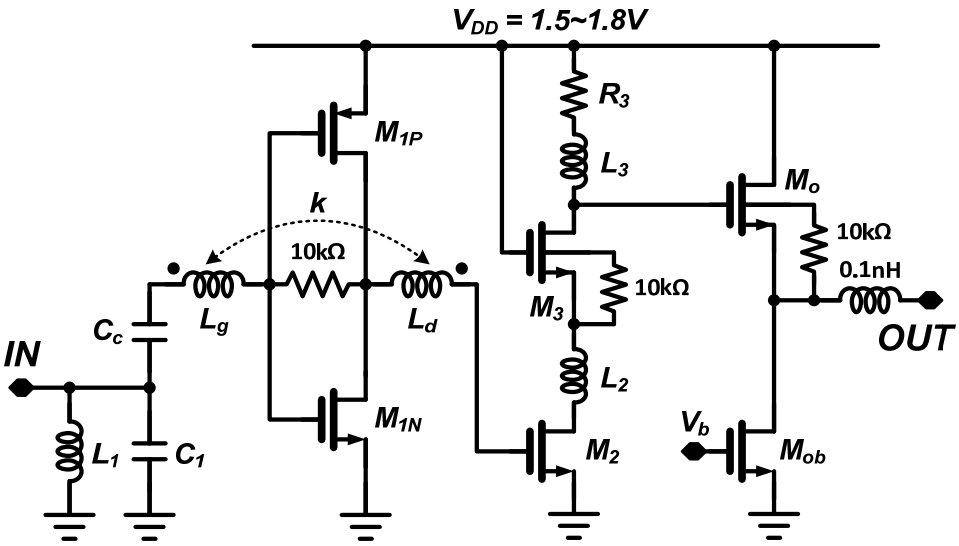


Figure 3-1. The proposed 3–11GHz UWB LNA.

3.2 The Proposed 3–11GHz UWB LNA

The proposed 3–11GHz UWB LNA employs the proposed BSNIM amplifier, as shown in Figure 3-1 [8]. In this prototype design the inverter amplifier (M_{1P}–M_{1N}) is self-biased with a 10kΩ feedback resistor. C_{gs} of M_2 plays the role of C_L in Figure 2-16. L_2 between M_2 and M_3 further increases the gain expansion at the higher band edge. The body of M_3 is biased to its source with a 10kΩ resistor. L_3 and R_3 provide a voltage gain with a low-Q shunt peaking at the center frequency to compensate the mid-band gain depression by the first stage. The M_o and M_{ob} constitute the output buffer and the 0.1nH output inductor improves the output matching to 50Ω. The detailed design parameters of the practical devices are listed in Table 3-1.

The simulation was performed by Agilent ADS. The S_{11} and S_{opt}^* of the designed LNA on Smith Chart is shown in the left of Figure 3-2. In the right of Figure 3-2 is the result without L_1 and C_1 to show how the dual reactive feedback enables BSNIM. The frequency dependence of $\mathrm{Re}\{Z_{opt}^*\}$ can be observed that it decreases as the frequency increases. At low frequencies the

TABLE 3-1
DEVICE VALUES OF THE 3-11GHZ UWB LNA

Transistor	**M_{1N}**	**M_{1P}**	**M_2**	**M_3**	**M_o**	**M_{ob}**
Width (μm) (Length:0.18μm)	80	160	35.2	35.2	70	35

Device	**L_1**	**C_1**	**C_c**	**L_g**	**L_d**	**k**	**L_2**	**L_3**	**R_3**
Value	2.4nH	262fF	4pF	1.4nH	2.6nH	0.18	1.3nH	4.7nH	128Ω

Note: The values here are of the practical device with parasitic effects.

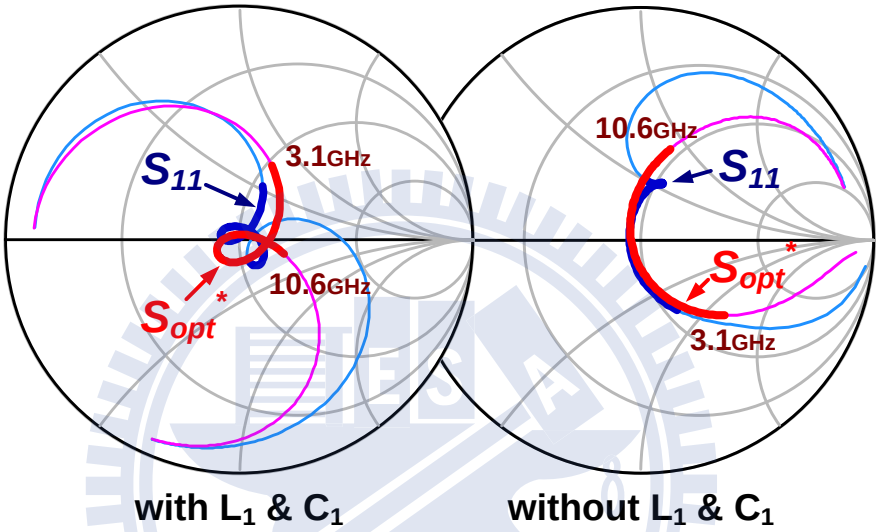


Figure 3-2. BSNIM on Smith Chart. In the left is the simulated S11 and Sopt*. The bold face section of each curve represents the results in frequency range from 3.1 to 10.6 GHz. In the right is the result without L_1 and C_1 to give insight of BSNIM.

plot shows that $\mathrm{Re}\{Z_{11}\}$ appears close to $\mathrm{Re}\{Z_{opt}^{*}\}$ over a large frequency range, but begin to deviate around 7.5GHz. The resonance in (2-39) due to the inductive feedback helps reduce such deviation. As shown in the plot, however, the improvement is limited to a small frequency region up to 11GHz.

The $\mathrm{Re}\{Z_{opt}^{*}\}$ and the $\mathrm{Re}\{Z_{11}\}$ in the higher frequency region are slightly larger than the expected values because of the parasitic shunt capacitance of L_g. Then with L_1 and C_1 the order of matching network is increased such that both the S_{11} and S_{opt}^{*} move towards the center of Smith Chart, achieving broadband matching. With this high-order matching network, the noise

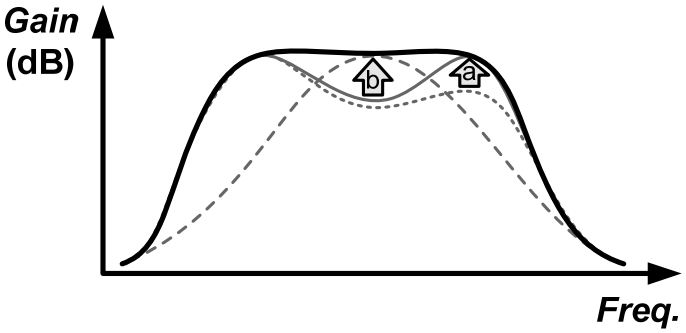


Figure 3-3. Gain response trimming in the second stage: (a) High-band expansion by L_2; (b) Mid-band compensation by L_3 and R_3. The bold black curve is the expected result.

matching and input matching performance are also robust among different corner conditions.

The second stage of this LNA plays the role of gain response trimming to have a flat in-band response. The L_2 further expands the gain response at the higher band edge with series peaking, and the L_3 and R_3 provide a low-Q shunt peaking at mid-band to compensate for the flat gain response, as shown in Figure 3-3. This makes the in-band gain variation less than 1-dB. The third stage in the right of Figure 3-3 is an output buffer.

This LNA was designed in TSMC 0.18um CMOS process with aluminum as metal material. In simulation it was designed to target >15dB return loss, < 4dB maximum in-band noise figure, >15dB power gain with less than 0.5dB in-band variation, and <0.1ns maximum group delay variation, while draws <10mW DC power from a 1.5V supply. With the high-order matching network, the noise matching and input matching are robust among corner conditions, while the noise figure is slightly affected by 1dB. The broadband noise performance is found mainly limited by the input matching network, of which the resistive loss substantially increases the F_{min}.

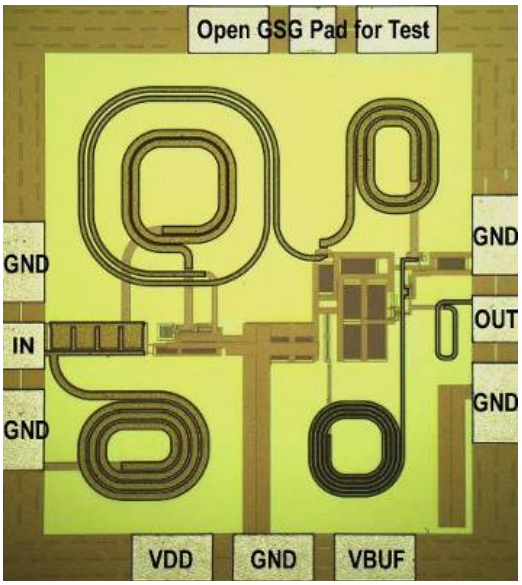


Figure 3-4. Chip micrograph of the fabricated UWB LNA.

3.3 Chip Implementation

In chip implementation non-ideal factors must be taken into account. Simplified simulation models of inductive devices are built with the EM simulation results. We utilized the optimization utility of Agilent ADS to find the optimal structure, dimension, and parameters for real devices. The practical parameters of the transformer, including L_g, L_d and M, are 1.4nH, 2.6nH and 0.35nH respectively. The circuit floor plan is well arranged to minimize lengths of extra interconnect lines. For those transistors not connected to ground at the source node, a bias resistor of large value is placed in between the source and the body nodes to minimize body effect. Fabricated in 0.18um CMOS process this prototype chip consumes 9mW from a 1.5V power supply. The power consumption of the output buffer stage is not taken into account.

The chip micrograph is shown in Figure 3-4. The parasitic shunt capacitance of the coupling capacitor C_C in Figure 3-1 is utilized as the C_1 of the matching network. Figures 3-5 to 3-7 show the measurement results. Also included are the post-layout simulation results with the transistor model in the slow-slow (SS) corner, which are found closer to the measured results. The noise

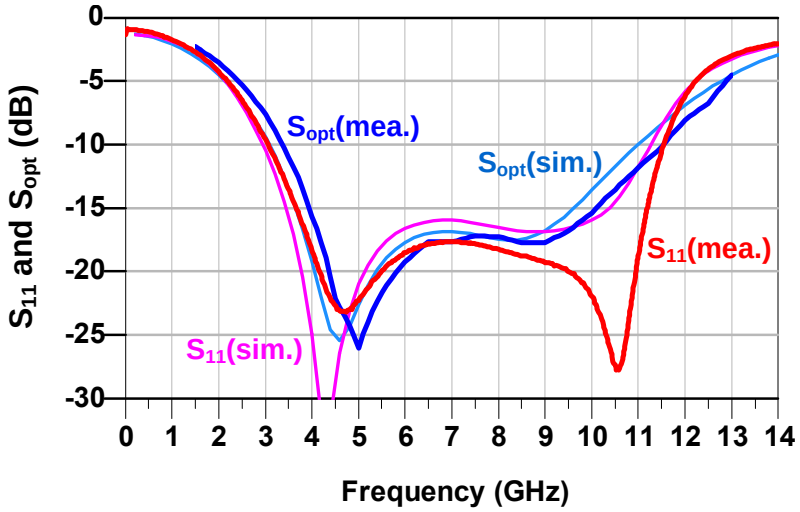


Figure 3-5. Measured and simulated S_{11} and S_{opt}.

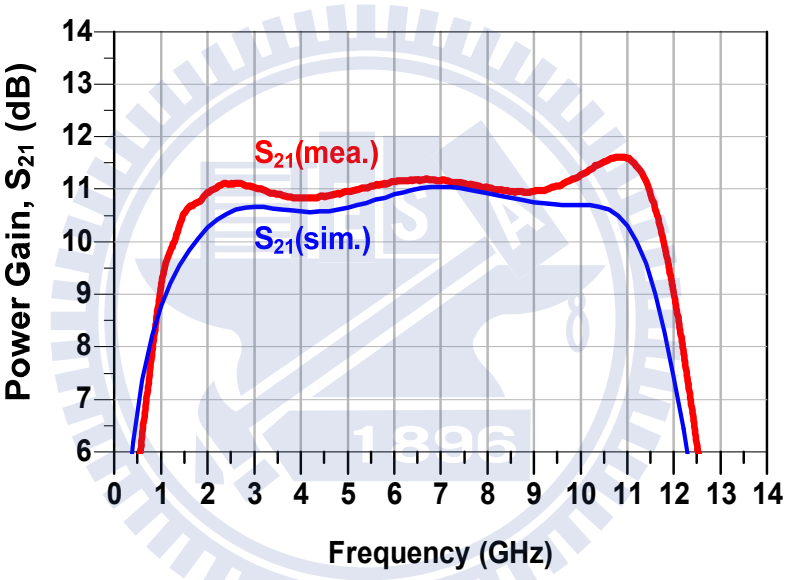


Figure 3-6. Measured and simulated S_{21}.

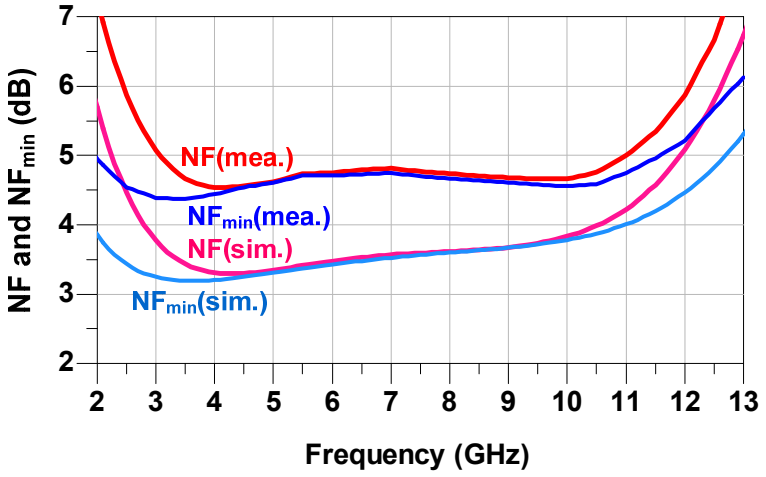


Figure 3-7. Measured and simulated noise figure and NFmin.

TABLE 3-2
COMPARISON OF BROADBAND LOW NOISE COMMON-SOURCE AMPLIFIERS

Ref.–Year	CMOS Tech.	Feedback Topology	Frequency Coverage (GHz)	Max. NF (dB)	Min. Power Gain (dB)	Max. S_{11} (dB)	Min. IIP_3 (dBm)	Supply Voltage (V)	DC Power (mW)	Active Area (mm^2)
[7] –2004	0.18µm	Source Inductive Deg.	2.3 – 9.2	8	9.3	-9.4	-16	1.8	9	0.66
[19] –2007	90nm	Source-Follower	DC – 6.0	3.2	17.4	-10	N/C	1.2	9.7[a]	0.019
[20] –2007	0.13µm	Resistive/Source-Follower	1.0 – 7.0	3.0	17	-10	-4.1	1.2	25	0.0017
[21] –2007	90nm	Resistive/Source-Follower	0.5 – 7.0	2.9	21	-7.2	-10.5	1.2	12	0.012
[22] –2008	90nm	Resistive	0.2 – 9.0	7.8	7	-11	-9.5	1.2	20[a]	0.066
[9] –2007	0.13µm	Source Ind. Deg. & Shunt-Series Transformer feedback	3.1 – 10.6	3.0	-13.7	-9.9	-8.5	1.2	9	0.4
This work [8]	**0.18µm**	**Shunt Capacitive & Series Transformer feedbacks**	**3.1 – 10.6**	**5.1 / 4.5**	**11 / 14**	**-11**	**-12**	**1.5 / 1.8**	**9 / 21**	**0.46**

[a] Differential LNA.

parameters were measured with ATN NP-5 noise parameter analysis system. Figure 3-5 shows the measured S_{11} and S_{opt}. Both of them have good in-band matching to 50Ω. Figure 3-6 shows the power gain S_{21}. The measured S_{21} meets the simulated result with the model in the SS corner, but is about 5-dB lower than that in the typical-typical (TT) corner. The noise figure (NF) and the circuit minimum noise figure (NF_{min}) are shown in Figure 3-7, in which NF is very close to the NF_{min} in the pass band. The measured in-band noise figure is less than 5dB. The measured NF_{min} higher than the simulated one is due to the degraded power gain. If a 1.8V instead of 1.5V is applied as supply voltage, it achieves < 4dB NF with less than 20mW DC power consumption. The measured IIP3 is about -12dBm. The linearity performance is degraded by the voltage gain of the first stage driving the gate of M_2 (Figure 3-1), such that the nonlinear effect of M_2 is magnified. The performance is summarized and compared with other UWB LNAs in Table 3-2. The simulation and the measurement results successfully validated the proposed BSNIM solution.

3.4 Summary

A LNA architecture using capacitive feedback and series-series transformer feedback simultaneously for broadband purpose is reported. In experimental results the function of broadband simultaneous noise and impedance matching is proven. This design not only lowers the noise figure but also provides flat high gain throughout the UWB band. With the utilization of weakly coupled transformer the chip size is slimmed down dramatically. This design well utilized those device parasitic effects such as transistor gate-to-drain capacitance (C_{gd}) and the shunt capacitance of coupling capacitor (C_1) as part of design.

Chapter 4

Reconfigurable LNA for Multi-Standard Receiver

4.1 Introduction

As more and more wireless applications have come into people's life for better convenience, many communication standards are widely used currently. For roaming among different access technologies including cellular network, personal area network (PAN), wireless local area network (WLAN) and the upcoming wireless metropolitan area network (WiMAX), there rises strong motivation on using a single radio system to support multi-bands and multi-standards to lower the hardware cost and enable wireless access anywhere and anytime. As such, it is highly expected that a transceiver is reconfigurable in specification accommodating different standards. Such specifications for a receiver RF front-end include carrier frequency, bandwidth, voltage gain, noise figure, and linearity. Moreover, the power consumption shall be controllable accordingly.

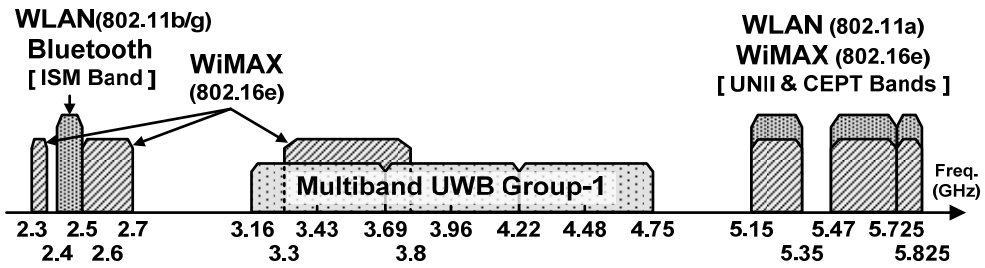


Figure 4-1. Spectra of Bluetooth, WLAN, MB-UWB mode-1 and WiMAX.

In such a multistandard RF system, one of the most critical issues is a large dynamic range to cover various needs of different standards. Among sub-blocks of a reconfigurable receiver front-end, the low-noise amplifier (LNA) is the most difficult part to design as it is expected to provide good input impedance matching, high voltage gain and low noise figure in dynamically specified frequency bands. Figure 4-1 shows the spectra of Bluetooth, Wireless LAN (802.11a/b/g), multiband ultra-wideband (MB-UWB), and WiMAX (802.16e), which are the standards of interest in this project. To accommodate such diversified frequency specifications, the frequency operation of a reconfigurable LNA can be in either concurrent multiband or tunable single band. To date there are several approaches for concurrent multiband operation. First proposed in 2002, an LNA utilizes dual-band LC-networks to provide concurrent dual-band input matching and output gain response [26]. This approach becomes cumbersome when handling multiple bands. The more adequate solution is a broadband design with comprehensive band coverage. Numerous broadband LNA design techniques have been developed by applying the input LC band-pass filtering [7], [23], the dual reactive feedback [8], the resistive/ source-follower feedback [19]–[22], and the common-gate topologies [27]. In compare with the tunable single band approach, the broadband input matching avoids the use of tunable devices in input network that easily degrades noise performance. The broadband gain response, however, is unfavorable because it allows undesired interferers to pass through such that stringent linearity is required in the succeeding stages (e.g., mixer). As such, a tunable

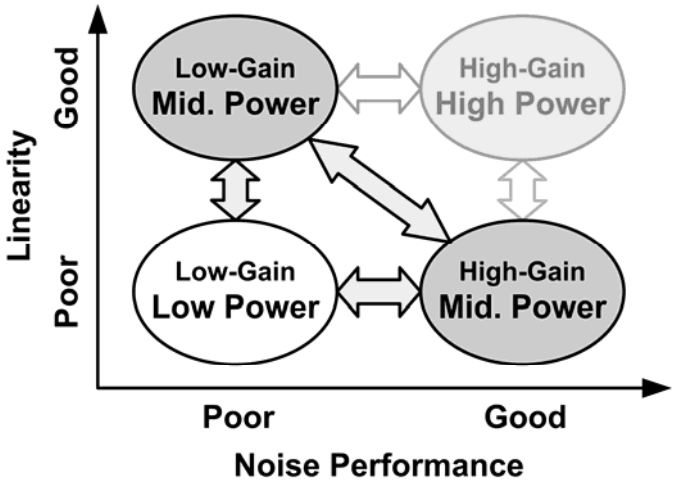


Figure 4-2. The performance matrix for reconfiguration of LNA. In this work the three corner states of low power and middle power are pursued.

single band gain response is preferred for out-of-band interferer suppression [28], [29].

Besides the frequency issues, the trade-off between LNA performances can be outlined by the performance matrix as shown in Figure 4-2, giving insight for performance reconfiguration. Typically the higher gain provides the lower noise figure, whereas the lower gain brings the better linearity. Power consumption further affects the circuit dynamic range[4]. If higher performance of a larger dynamic range is in need, the LNA shall be configured to consume more power to meet the requirement. For example, a large dynamic range demanding both low noise figure and high linearity is required in the ultra-wideband (UWB) system, whereas the low power consumption is of the primary concern in Bluetooth connection. Techniques including bias control, current steering, feedback switching, and attenuation switching can be used for gain control [30], [31].

This chapter proposes a wide-tuning-range, performance-reconfigurable LNA. It consists of two stages featuring broadband input matching and low noise amplification at the first stage,

[4] The circuit dynamic range is defined as the allowed input power range, typically from its sensitivity to 1-dB compression point.

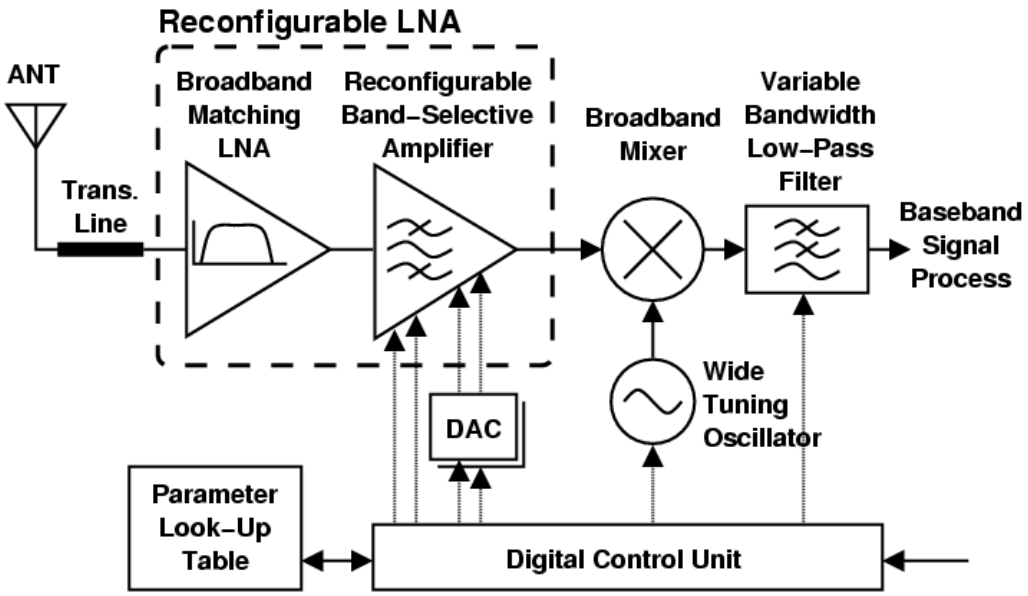


Figure 4-3. Reconfigurable receiver front-end architecture.

and a wide-tuning-range band-limited gain response with adjustable performance at the second stage. The 0.13um technology CMOS LNA is designed to operate from 2.4- to 5.4-GHz. A new inductor switching configuration provides wide-range frequency tuning while gain and noise figure are maintained at the same level. With bias control and transistor size switching, performance is reconfigurable to approach the lower left three corner states as shown in Figure 4-2.

4.2 General Considerations on the Proposed Reconfigurable LNA

Figure 4-3 shows a possible receiver front-end architecture for multistandard radio. The LNA, local oscillator and low-pass filter are controlled digitally for different specifications by the digital control unit referring to a parameter look-up table. The receiver allows the signal of interest to pass through the receiving path, while the others turn into spurious noise to be

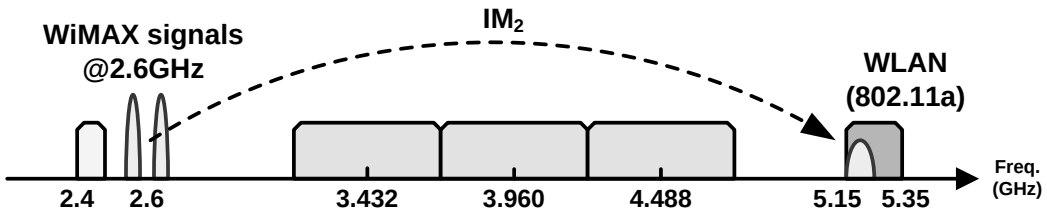


Figure 4-4. An exemplary case of IM_2 interference.

excluded. To alleviate the issue of broadband noise, the LNA is reconfigurable to meet the required circuit performance at the tuned operating frequency over the specified 3GHz frequency range. The dashed box in Figure 4-3 shows a two-stage LNA solution pursued in this work. Circuit property is fixed at the first stage, which provides broadband responses of input impedance matching, high voltage gain and low noise figure. This stage is set to have high voltage gain so as to achieve better system noise performance with low power consumption. Frequency tuning function is implemented at the second stage, which also provides variable gain/ linearity control to enhance the dynamic range.

In general coarse tuning functions are realized using switching components controlled by open-loop digital control signals, while fine and continuous tuning using analog control signals available in current mode generated by simple low-speed digital-to-analog converters (DACs). All the digital control signals and DAC inputs refer to a look-up table which is obtained from calibration process

While the two-stage LNA as shown in Figure 4-3 is employed, the non-linearity of the broadband stage actually introduces more inter-modulation distortions (IMDs) than a regular narrowband LNA – it generates IMDs from all the passed signals. And in addition to the odd-order IMDs, the even-order IMDs emerges when the fractional bandwidth is larger than 2. Signal at frequency f_0 will be interfered by the second- or third-order inter-modulation of strong signals at frequency f_1 and f_2 if $f_0 = |f_1 \pm f_2|$, $(2f_1 - f_2)$ or $(2f_2 - f_1)$. Examples of such frequency

combinations include $\{f_0, f_1, f_2\}$={2.48, 2.68, 5.16} for the 2nd-order IMD (IM_2), and {2.42, 2.54, 2.66} and {5.16, 3.79, 2.42} for the 3rd-order IMD (IM_3), all in the unit of GHz. Figure 4-4 shows the IM_2 from the two blockers around 2.6GHz landing at 5.2GHz as an example. When operating at 5.2GHz, the band selective second stage of the LNA cannot filter out the IM_2 from 2.6GHz blockers at all. And in most design case, the power level of IM_2 is larger than IM_3 with the same blocker power level.

The even-order IMD in general can be minimized with a fully differential circuit structure. However when a single-in differential-out receiver frontend is considered with the inclusion of a broadband active BALUN after the single-end LNA, the even-order IMD is not ignorable and should be taken into account in the design.

4.3 A 2.4 – 5.4GHz Wide Tuning range Performance Reconfigurable LNA

The schematic of the proposed reconfigurable LNA is as shown in Figure 4-5. The first stage is a broadband amplifier with dual-reactive feedback, based on the BSNIM amplifier described in chapter 2. The second stage is a cascode amplifier providing gain, linearity, and wide-range frequency tuning. The output buffer stage is for measurement purpose. The parameters of key devices are listed in Table 4-1 and the design concepts of the first and the second stages are detailed as follows.

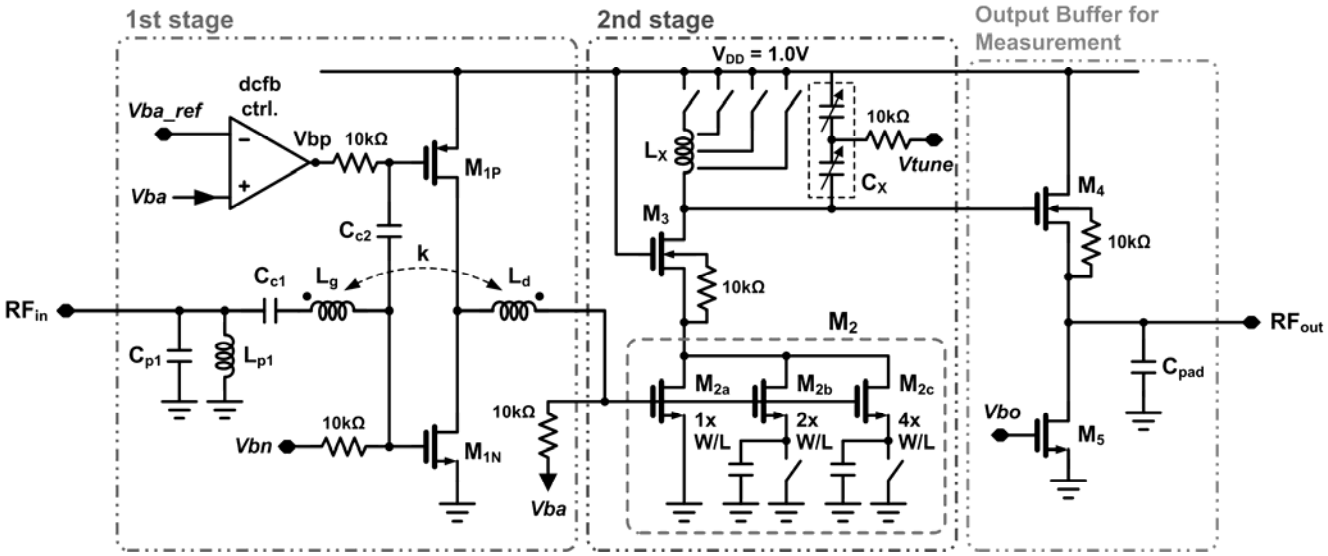


Figure 4-5. The proposed reconfigurable LNA.

TABLE 4-1
DEVICE VALUES OF THE DESIGNED RECONFIGURABLE LNA

Transistor	**M_{1N}**	**M_{1P}**	**M_{2a}**	**M_{2b}**	**M_{2c}**	**M_3**	**M_4**
Width (μm) (Length:0.13μm)	120	120	10	20	40	60	30

Device	**C_{p1}**	**L_{p1}**	**C_{c1}&C_{c2}**	**L_g**	**L_d**	**k**	**C_X**
Value	460fF	4.9nH	2.7pF	3.2nH	4.9nH	0.17	240–510fF

Note: The inductance of the switching inductor L_X is as shown in Figure 4-16.

4.3.1 Broadband Amplifier with Controllable Output DC Level

The first stage employs the BSNIM amplifier described in Chapter 2. In this project this stage is designed for the entire 2–6 GHz frequency band. The input impedance matching is designed having less thn -15dB input reflection and the noise figure is very close to NF_{min} in this wide frequency range. The voltage gain is about 15dB. As the design result, the simulated frequency responses of voltage gain and noise figure of the first stage are shown in Figure 4-6.

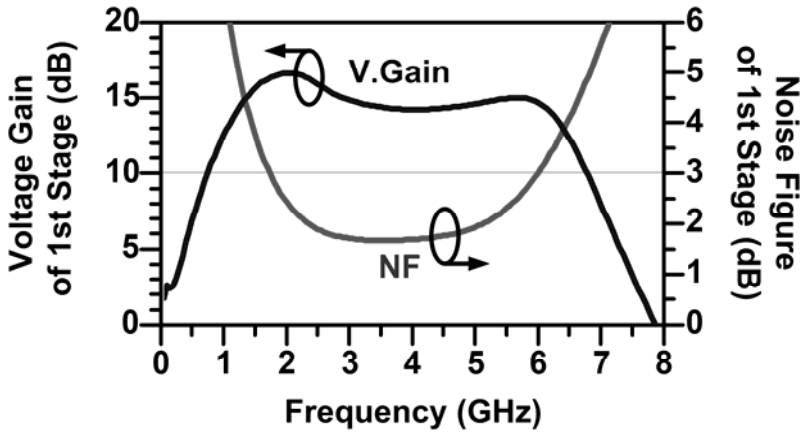


Figure 4-6. Voltage gain and noise figure of the first stage in simulation result.

The biasing of M_{1N} and M_{1P} is separated to provide a controllable output DC level to bias transistor M_2, conducting the performance reconfiguration at the second stage. The DC level, *Vba*, is clamped equal to a reference voltage *Vba_ref* by a DC feedback loop, including M_{1P} and an OP-Amp. The M_{1P} itself provides a 24dB DC voltage gain and the OPAmp, consuming less than 80μW power, has 37dB voltage gain. Thus the gate voltage of M_{1P}, *Vbp*, varies within 12.5mV for the demanded 200mV DC dynamic range of *Vba*, introducing just marginal impact on input matching and noise performance of the first stage. Meanwhile the error between *Vba* and *Vba_ref* is less than 0.2mV. In a fully integrated receiver, the *Vba_ref* and the M_{1N} bias voltage *Vbn* can be configured by a current-mode DAC and a constant-gm bias circuit, respectively. In this prototype both of them are driven externally for laboratory test purpose.

4.3.2 Performance Reconfiguration by Switching Transistor

Performance reconfiguration is realized by the common-source amplifier (M_2) at the second stage, including gain and linearity control. The noise figure is generally correlated to the gain level; that is, higher gain brings a lower noise figure. The design target is implementation of three operation modes, one in high-gain (HG) and two in low-gain (LG_1 and LG_2). Gain difference of at least 10-dB is expected between the high-gain and the low-gain modes. Besides,

this LNA exhibits an improved linearity in LG_1 mode while the even lower power consumption is achieved with degraded linearity in LG_2 mode.

Being the transconductor of the cascode amplifier at the second stage, M_2 is found to be the linearity bottleneck of this LNA. Its transconductance g_m is the primary nonlinearity source as M_2 is loaded by a common-gate stage of low input impedance [32]. Hence linearity control mainly relies on M_2 gate biasing. Linearity performance can be inspected by the 2nd and the 3rd input interception point voltages, V_{IIP2} and V_{IIP3}, as

$$V_{IIP2} = \left| g_m / g_m' \right| \tag{4-1}$$

and

$$V_{IIP3} = \sqrt{\left| \frac{4}{3} \frac{g_m}{g_m''} \right|}, \tag{4-2}$$

Where the g_m' and the g_m'' are the first and the second derivative of gm, respectively. Because M_2 receives very wideband input, the second-order distortion is found as critical as the third-order in some application cases. Transistor linearity is characterized by the simulated results of g_m, g_m'/g_m, and $\sqrt{\left| g_m'' / g_m \right|}$ vs. V_{gs}, as plotted in Figure 4-7. As can be seen, larger V_{gs} gives higher gain g_m, better V_{IIP2}, and larger drain current, while V_{IIP3} varies insignificantly. The second-order distortion is chosen as the primary linearity index to be improved in this LNA.

The actual design is according to Figure 4-7. Gate bias is first chosen corresponding to different linearity performances in each operation mode. Then the transistor size is set regarding to gain requirement. The design result is summarized in Table 4-2. The 12dB stepping difference is produced on g_m and g_m'/g_m between the HG and the LG_1 modes. In practice the drain current I_{DS}, instead of V_{gs}, is controlled to alleviate the impact of process variation.

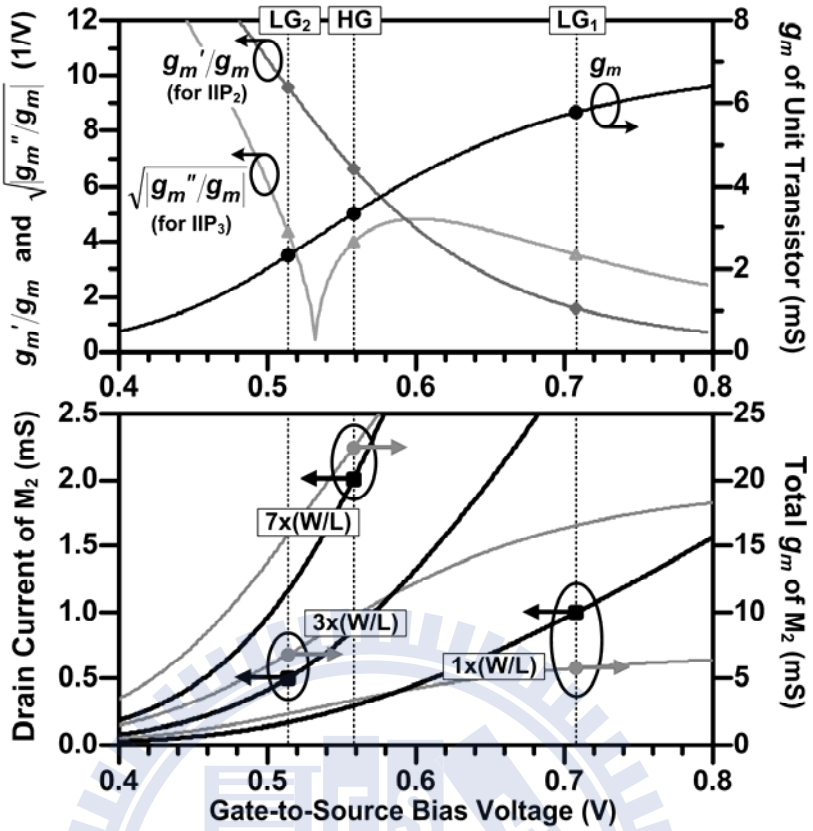


Figure 4-7. Simulated g_m'/g_m and g_m of transistor M_2 in response to V_{gs} under different gain modes.

TABLE 4-2
DESIGN PARAMETERS AND PERFORMANCE IN EACH OPERATION MODE

Mode	V_{GS}	*SIZE*	I_{DS}	$^*G_M$	$^*G_M'/G_M$
HG	0.56V	7x	2.0mA	0dB	0dB
LG_1	0.71V	1x	1.0mA	-12dB	-12dB
LG_2	0.51V	3x	0.5mA	-12dB	+4dB

* The g_m and g_m'/g_m are normalized to their values in HG mode.

As shown in Figure 4-5, the M_2 transistor actually consists of three transistors, M_{2a}, M_{2b} and M_{2c}, with the size ratio of 1:2:4. Transistors M_{2b} and M_{2c} are switched on and off by the switches at their source nodes. This allows larger switch size for smaller on-resistance. The input capacitance of M_2 should not be changed significantly by size switching as it is an important parameter for LNA input matching, which is expected to be similar among all considered configurations. For the sake of this, the source nodes of M_{2b} and M_{2c} are AC

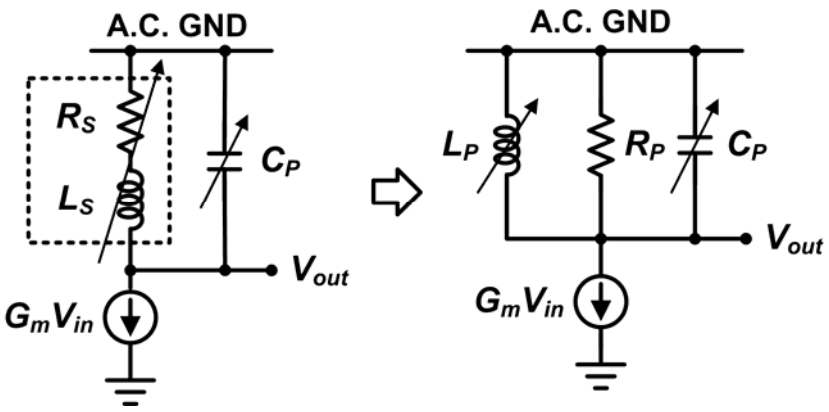
bypassed to ground to alleviate the impact of switching to the input capacitance.

Switching transistor M_2 controls the voltage gain and linearity, as well as the power consumption. Compared to the conventional current steering variable-gain schemes in which gain is adjusted by the common-gate transistor M_3, our approach is more power-efficient because at lower gain the LNA requires smaller drain current.

4.3.3 Frequency Tuning by Switching Inductor and Varactor

Band-selective filtering is provided by an LC resonance tank at the second stage as shown in Figure 4-5. The resonator consists of a multi-tapped switching inductor and two on-chip varactors. The former provides coarse frequency stepping, while the latter is for fine tuning. Coarse frequency stepping is realized by switching control of tapping points so as to obtain different inductances, yielding to several sub-bands. This LC tank is demanded to be tunable over the entire frequency range of interest. Meanwhile it shall provide a quite consistent voltage gain for each tuned band. This calls for the quality factor requirement of the switching inductor as described as follows.

The resonator tank can be generally represented by an equivalent circuit as shown in Figure 4-8(a), in which the inductance is switchable and the capacitance is tunable. The resistance R_S in series to inductor L_S includes the inductor parasitic resistance and the switch on-resistance, and dominates the quality factor of this tank. As the inductance L_S is changed by turning on distinct switches, the R_S value can actually be changed accordingly. To get the insight to achieve the aforementioned gain consistency requirement, the resonator circuit is transformed to the parallel RLC tank in Figure 4-8(b), with the equivalent parallel inductance and resistance derived respectively as



(a) (b)

Figure 4-8. Wide continuous frequency tuning by adjusting both the inductor and capacitor: (a) Practical circuitry; (b) Equivalent parallel resonance tank.

$$L_P = L_S\left(1+\frac{1}{Q_L^2}\right) \tag{4-3}$$

and

$$R_P = \frac{L_S}{R_S}\cdot\frac{1}{C_P} = \frac{Q_L}{\omega_0}\cdot\frac{1}{C_P}. \tag{4-4}$$

Here Q_L stands for the quality factor of the switching inductor which equals to $\omega_0 L_S/R_S$, and ω_0 is the resonance frequency as

$$\omega_0 = \sqrt{\frac{1}{L_S C_P}\cdot\frac{Q_L^2}{1+Q_L^2}} = \sqrt{\frac{1}{L_S C_P}-\frac{R_S^2}{L_S^2}}. \tag{4-5}$$

The 3-dB bandwidth, BW, of this resonance tank is

$$\text{BW (in Hz)} = \frac{1}{2\pi}\frac{\omega_0}{Q_L} = \frac{1}{2\pi}\frac{R_S}{L_S}. \tag{4-6}$$

At resonance the voltage gain of this circuit can be expressed as

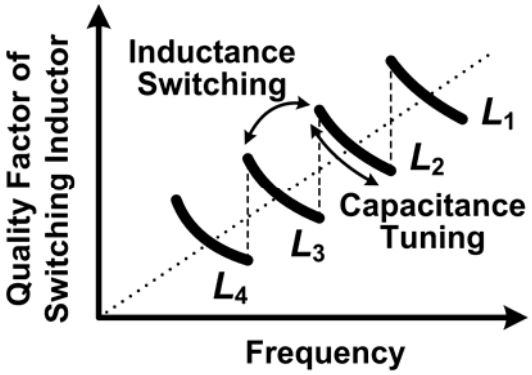


Figure 4-9. Quality factor profile of switching inductor as required for good voltage gain consistency.

$$A_v = V_{out} / V_{in} = G_m R_P \,. \tag{4-7}$$

The design guideline is revealed from these equations. Given the typical condition of a flat G_m response over the frequency range of interest, the voltage gain consistency fully corresponds to the frequency dependency of R_P. In discussion of the fine capacitance tuning, the switching inductor is assumed frozen with a fixed inductance. As $C_P \propto 1/\omega_0^2$, it leads to the frequency dependency of Q_L for consistent R_P from (4-4) as

$$Q_L \propto \omega_0^{-1} \,. \tag{4-8}$$

This condition can be partially met by a practical inductor, of which quality factor Q declines in the frequency region higher than the peak-Q frequency. Note that a consistent BW calls for the condition of $Q_L \propto \omega_0$ by (4-6), opposite to (4-8). For LNA the consistency on voltage gain is more important than bandwidth so the design generally follows (4-8). Nevertheless the bandwidth variation is still acceptable if the frequency range of each sub-band remains small enough.

The condition for consistent R_P among coarse inductance stepping can also be obtained from (4-4), by freezing the tuning of C_P, as

$$\frac{Q_L}{\omega_0} = \frac{L_S}{R_S} \approx const. \tag{4-9}$$

That is, when inductance L_S is switched smaller for a higher resonance frequency, the corresponding quality factor of switching inductor should be proportionally higher, which necessitates a smaller R_s. In general this can be fulfilled by design of the switch on-resistance for each inductance.

Combination of the conditions in (4-8) and (4-9) gives the quality factor requirement of the switching inductor as the profile shown in Figure 4-9. In practical implementation of the on-chip switching inductor, the rule of (4-9) is actually difficult to realize because it demands an unacceptable large switch transistor for the smallest inductance. To overcome this difficulty, an alternative switching configuration for the inductor is proposed, as discussed in the next section.

4.4 Multi-Tapped Switching Inductor

4.4.1 Inductor Switching Configuration

The basic idea of inductor switching is to enable or disable sections of inductor coils to obtain different inductance values. The conventional switching configuration for a multi-tapped inductor is shown in Figure 4-10(a) [33], [34]. Both ends of the coil are directly connected to the application circuit at the nodes **a** and **b**. Switches are attached to the tapping nodes, of which one can be turned on to bypass the remaining coils. The switch on-resistance is known to degrade the inductor quality factor. The degradation becomes worse in a spiral configuration that all the coil sections are winded together with magnetic mutual coupling. This coupling magnifies the degrading effect of switch on-resistance. An alternative switching configuration

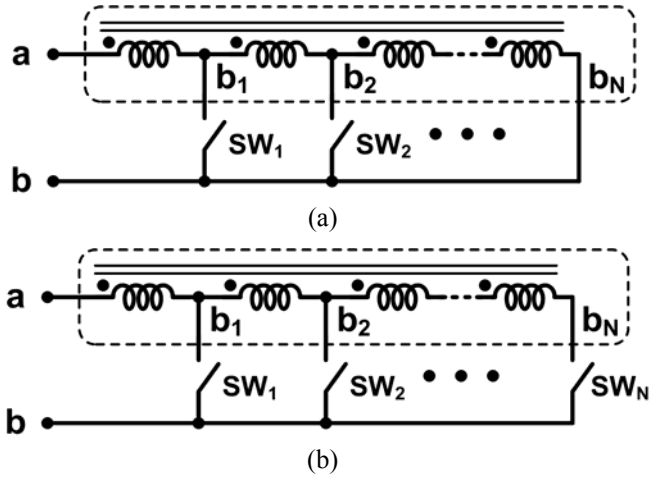


Figure 4-10. Different switching configurations for multi-tapped inductor: (a) Conventional; (b) Proposed.

is proposed as shown in Figure 4-10(b), in which an additional switch is attached at the end node of the coil $\mathbf{b_N}$ to convert the difficulty that the conventional configuration faces.

Consider the representative case of double-tapped switching inductor, i.e., **N**=2 in Figure 4-10. When the inductors in Figure 4-10(a) and 4-10(b) are switched for the smaller inductance, they can be modeled as circuits shown in Figure 4-11(a) and 4-11(b), respectively. The R_{ON} is on-resistance of the switch at node $\mathbf{b_1}$, typically much larger than the intrinsic resistance of coil. The C_2 in Figure 4-11(b) is parasitic capacitance of the switch at node $\mathbf{b_2}$ in OFF state. The two sections of coil, L_1 and L_2, form a transformer with coupling factor of k.

In the desired ideal case without effect of L_2 and k, only the primary loop of L_1 and R_{ON} is considered such that the inductor quality factor is limited by R_{ON} as

$$Q_0 = \omega L_1 / R_{ON} \ . \tag{4-10}$$

When L_2 and k are considered, the input impedance Z_1 in the conventional case of Figure 4-11(a) can be derived as

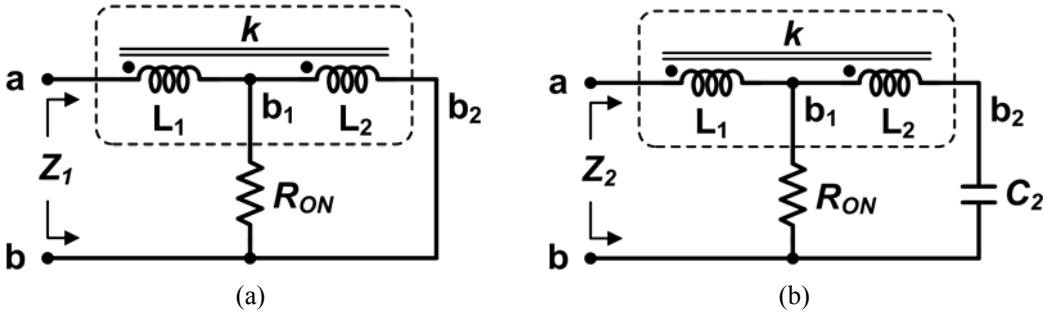


Figure 4-11. Equivalent circuits of double-tapped inductor in different switching configurations: (a) the conventional, and (b) the proposed.

$$Z_1 = j\omega L_1' + \frac{R_{ON}' \cdot j\omega L_2'}{R_{ON}' + j\omega L_2'}, \tag{4-11}$$

in which

$$L_1' = (1-k^2)L_1, \quad L_2' = k^2 L_1 + L_2 + 2k\sqrt{L_1 L_2},$$

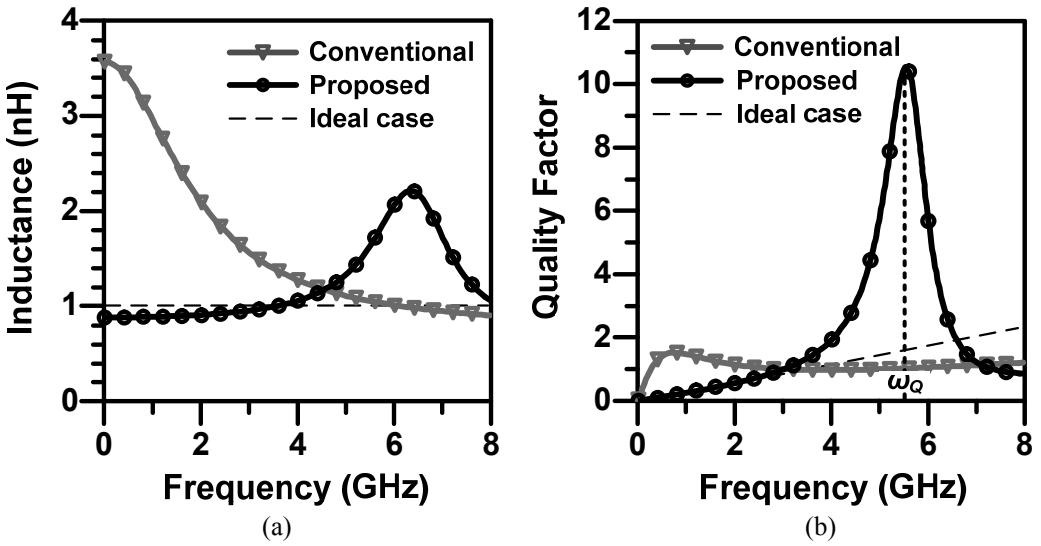
$$\text{and} \quad R_{ON}' = R_{ON}\left(L_2'/L_2\right). \tag{4-12}$$

The issue of Z_1 can be addressed in twofold. At the low frequency that $\omega L_2' << R_{ON}'$, the inductance approximates to $L_1'+L_2'$, equal to inductance of the entire coil and hence the inductance switching function fails. At the high frequency that $\omega L_2' >> R_{ON}'$, the Q_1 can be derived as

$$Q_1 \approx \frac{\omega L_1'}{R_{ON}'} = \frac{\omega L_1}{R_{ON}} \cdot \frac{1-k^2}{\left(1+k\sqrt{L_1/L_2}\right)^2}, \tag{4-13}$$

which is less than the Q_0 for $k > 0$.

On the other hand, the input impedance Z_2 in the proposed configuration shown in Figure 4-11(b) can be derived as



(a) (b)

Figure 4-12. Calculated results compared for the test cases in the conventional (—▽—) and the proposed configurations (—●—). The ideal switch operation of only the primary loop (– – –) is included as a reference. (a) effective inductance; (b) the quality factor.

$$Z_2 = j\omega(L_1 + M) + \frac{(R_{ON} - j\omega M)\left[1 - \omega^2 (L_2 + M) C_2\right]}{1 + j\omega R_{ON} C_2 - \omega^2 L_2 C_2}, \tag{4-14}$$

in which $M = k\sqrt{L_1 L_2}$. As the frequency approaches to

$$\omega_Q = 1/\sqrt{(L_2 + M) \cdot C_2}, \tag{4-15}$$

Z_2 becomes as $j\omega_Q \cdot (L_1+M)$, independent of R_{ON}, and thus the quality factor Q_2 is limited only by the intrinsic resistance of coil. The quality factor boosting conducted by the auxiliary resonance of L_2+M and C_2 is therefore obtained in the high frequency region around ω_Q.

A test case compares these two configurations. Set L_1 and L_2 as 1nH and 2nH along with parasitic resistances 2Ω and 4Ω, respectively. The coupling factor k is 0.5, R_{ON} is 10Ω, and C_2 is 0.3pF. The calculated results are shown in Figure 4-12(a) and 4-12(b). Also included is Q_0 as a reference. The calculated ω_Q of Eq. (4-15) is 5.58GHz. The Q_2 by the proposed configuration is boosted near ω_Q, close to the intrinsic coil quality factor and much larger than Q_1.

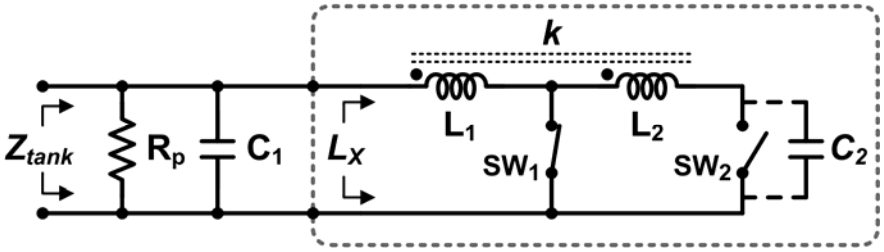


Figure 4-13. Equivalent model to calculate the achievable frequency tuning ratio.

4.4.2 Tuning Ratio of Resonance Frequency

When the switching inductor is applied to an LC resonator with a capacitor, the wide-range resonance frequency tuning is the primary expectation. The frequency tuning ratio is mainly determined by the inductance tuning ratio provided by the switching inductor. In the case using conventional switching configuration, the frequency tuning ratio is unlimited because the effective inductance can be switched to an arbitrarily small value, though the quality factor can be severely degraded to unusable. In the use of the proposed configuration, however, the frequency tuning ratio is limited as the consequence of quality factor boosting by the auxiliary resonance.

The analysis of the limited tuning ratio is by using the equivalent model of LC resonance tank as shown in Figure 4-13, in which the L_X is the effective inductance of switching inductor and the C_1 is the external capacitor to resonate with L_X. This model discusses the two extreme cases of the maximum and minimum L_X with the switching of SW_1 and SW_2. The switch on-resistance is chosen to be ignored in this analysis so as to identify the primary limiting factor.

When the SW_1 is open and the SW_2 is short, the maximum effective inductance $L_{X,MAX}$ is

$$L_{X,MAX} = L_1 + L_2 + 2k\sqrt{L_1 L_2}\ , \tag{4-16}$$

in which k is the magnetic coupling factor between L_1 and L_2. On the other hand, when the SW_1 is short and the SW_2 is open, the minimum inductance $L_{X,MIN}$ can be derived as

$$L_{X,MIN} = L_1 \cdot \left[\left(1-k^2\right) + \frac{k^2}{1-\omega^2 L_2 C_2} \right], \tag{4-17}$$

which is frequency dependent. When resonating with C_1, the $L_{X,MAX}$ and $L_{X,MIN}$ give the minimum and maximum resonance frequencies ω_{min} and ω_{max}, respectively. The ω_{min} can be easily derived as

$$\omega_{\min} = 1 \Big/ \sqrt{\left(L_1 + L_2 + 2k\sqrt{L_1 L_2}\right) C_1} \ . \tag{4-18}$$

And the ω_{max} can be obtained by solving the equation

$$\omega_{\max}^2 L_1 C_1 \cdot \left[\left(1-k^2\right) + \frac{k^2}{1-\omega_{\max}^2 L_2 C_2} \right] = 1 , \tag{4-19}$$

of which solutions are

$$\omega_{\max}^2 = \frac{\dfrac{1}{L_1 C_1} + \dfrac{1}{L_2 C_2} \pm \sqrt{\left(\dfrac{1}{L_1 C_1} - \dfrac{1}{L_2 C_2} \right)^2 + \dfrac{4k^2}{L_1 C_1 L_2 C_2}}}{2\left(1-k^2\right)} . \tag{4-20}$$

The solutions in (4-20) indicate two resonance frequencies at which peak value of Z_{tank} can be found. As discussed in Appendix of this chapter, the lower frequency applying the minus sign in (4-20) is the one of interest for $0 < k < 1$.

The frequency tuning ratio is defined as $\omega_{max}/\omega_{min}$. As the L_2 is inductance of the remaining coil bypassed by SW_1, the intuitive design of a smaller L_1 with a larger L_2 cannot always promise a larger frequency tuning ratio because the increase of L_2C_2 can also decrease the ω_{max}. The optimal L_1/L_2 arrangement for maximum $\omega_{max}/\omega_{min}$ depends on k and C_2/C_1 ratio.

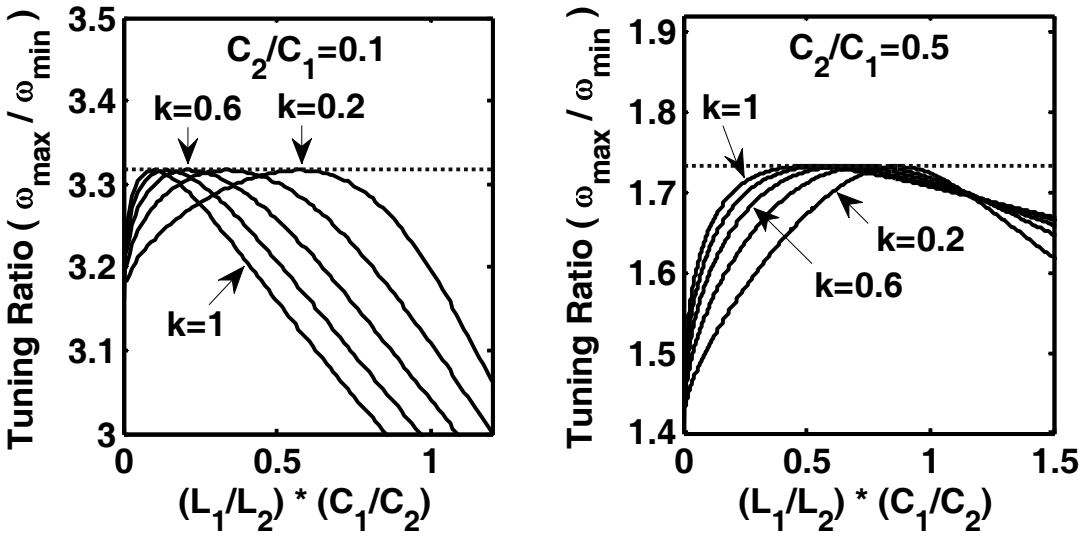


Figure 4-14. The frequency tuning ratio of the proposed switching inductor configuration in different C2/C1 ratio. The dotted horizontal asymptotes are located at the maximum value of tuning ratio given in (4-21).

It is difficult to derive directly but can be traced from the calculation results, as shown in Figure 4-14. Also included is the special case of $k = 1$ as discussed in Appendix.

Figure 4-14 reveals important insight. First, for a given C_2/C_1 ratio the peak value of $\omega_{max}/\omega_{min}$ is constant for $0 < k \leq 1$. Second, a smaller C_2/C_1 ratio allows a larger peak $\omega_{max}/\omega_{min}$ value. What of interest is the relationship between the peak $\omega_{max}/\omega_{min}$ value and the C_2/C_1 ratio as a design guide for the switching inductor. This can be obtained by finding the peak $\omega_{max}/\omega_{min}$ for $k = 1$, as

$$\max\left\{\frac{\omega_{\max}}{\omega_{\min}}\right\} = \sqrt{1+\frac{C_1}{C_2}}\,. \tag{4-21}$$

Therefore, the primary factor limiting the achievable frequency tuning ratio in the proposed switching inductor is identified to be C_2/C_1 ratio, and can be designed according to (4-21).

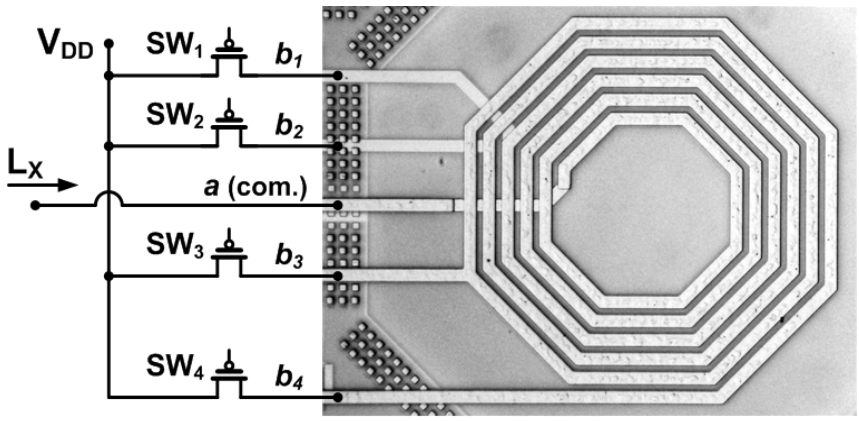


Figure 4-15. Designed switching inductor using PMOS as switches.

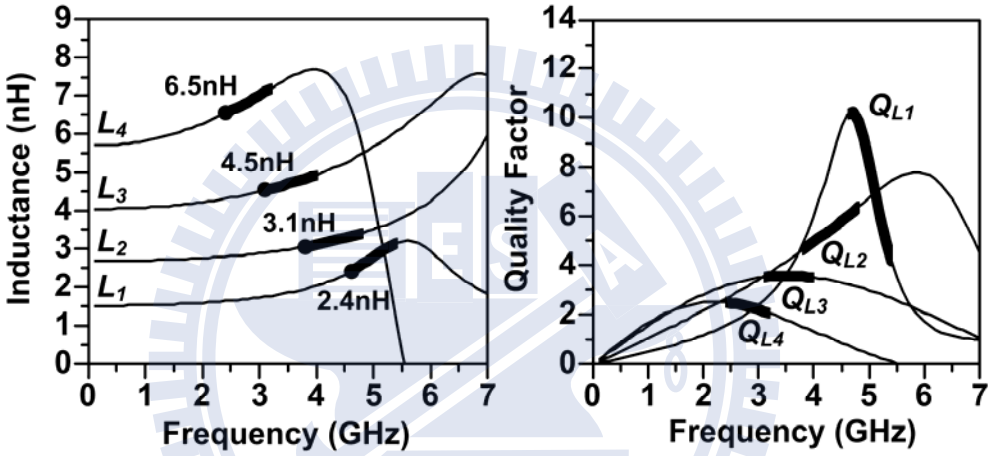


Figure 4-16. Simulation results of the designed switching inductor with designed PMOS switches.

4.4.3 Switching Inductor Design of This LNA

The switching inductor in this project is implemented by a spiral inductor with three additional tapping points, as shown in Figure 4-15. The simulation results with the designed switches are shown in Figure 4-16. The bold faced section of the inductances and quality factors correspond to the sub-bands they are employed. The proposed switching configuration improves the quality factor, allows a smaller size of the SW_1 and SW_2, and ensures the quality factor increased as the inductance switched smaller for higher frequency operation. The C_2 for (4-15) is the parasitic capacitance of SW_4 in OFF state as 115fF, leading to a quality factor

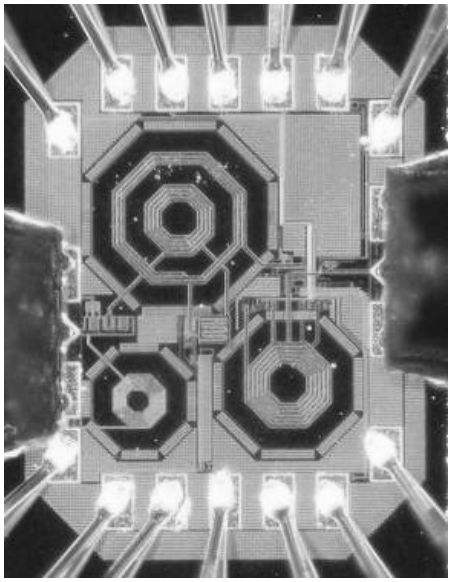


Figure 4-17. Micrograph of the fabricated reconfigurable LNA under test.

boosting at about 4.5GHz. The quality factors for each sub-band has been quite close to the required profile depicted in Figure 4-9, except the local profiles of inductance L_1 and L_2 affected by the boosting. As to the frequency tuning ratio, the C_1 and C_2 for (4-21) are respectively 324fF~592fF and 115fF, in which the C_1 is a variable capacitance. The actual designed frequency tuning ratio in this LNA is 2.3 with sub-bands overlapped, which ensures a full coverage over the entire tuning range and a less than 3-dB gain variation.

4.5 Chip Implementation and Measurement Results

This LNA is designed with 1.0V supply voltage and fabricated in TSMC 0.13μm RF CMOS process. Figure 4-17 shows the micrograph of the LNA under test. The core circuit without pads occupies 0.49 mm^2 chip area. RF signals are measured with on-wafer probing while all DC voltage is provided via bonding wires. In the test cases, small signal S-parameters are obtained with Agilent 8364B network analyzer, and noise figure from Agilent 8974A noise figure analyzer with cable loss compensation. Two tone tests are performed to test the linearity

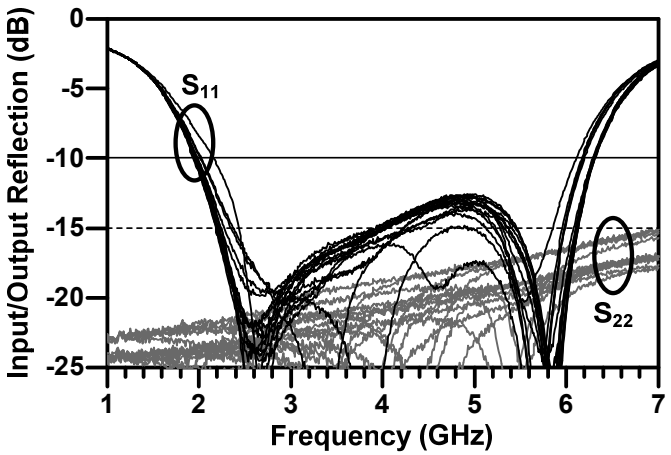


Figure 4-18. Measured input and output reflection ratio (S_{11} & S_{22}) of the LNA in all listed configurations under test.

performances of IIP_2 and IIP_3. The accurate power level at LNA input is calibrated by use of a power meter.

Performances of this LNA are measured in three configured performance modes in five frequency bands, carrying out 15 test cases. The five frequency bands include the designed upper and lower tuning limits and three MB-UWB mode-1 bands, listed as 2.4-, 3.43-, 3.96-, 4.49-, and 5.4-GHz. The performance modes include one 20-dB high-gain mode (HG) and two 10-dB low-gain modes (LG_1, and LG_2), representing the three operation modes shown in Figure 4-2, in which the LG_1 mode is for better linearity whereas the LG_2 mode toward the lowest power consumption.

The S-parameter test results are shown in Figure 4-18 and 4-19. The broadband input/output reflection performances for the 15 configurations, the 5 frequency bands tuning with 3 gain modes switching, are successfully kept consistent. The power gains at the HG mode are in the range from 22- to 25-dB whereas at the LG_1 and the LG_2 modes from 10- to 13-dB. Gains at different frequency bands for each gain configuration are within 3-dB variation and approximately consistent. Noise figures are lower than 3.1-dB for HG mode and lower than

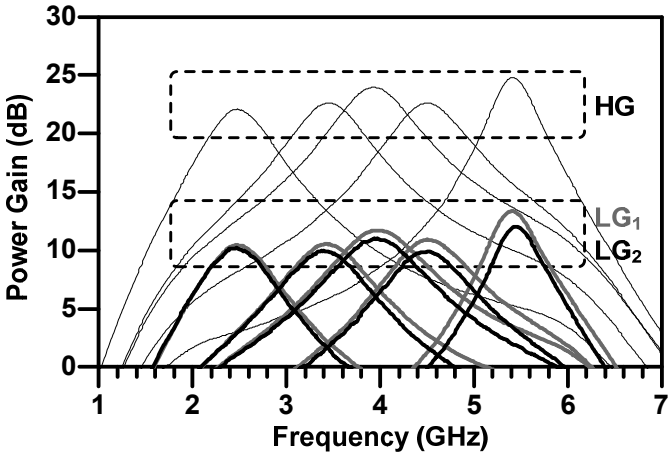


Figure 4-19. Measured power gain of LNA under typical bias condition.

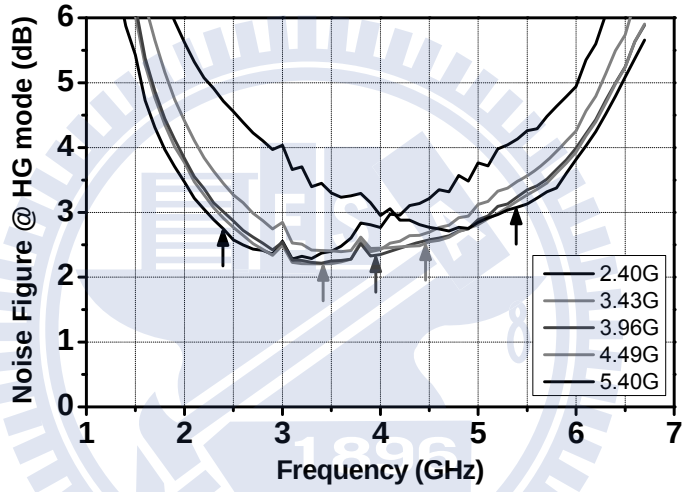


Figure 4-20. Measured noise figure for the five frequency configurations in HG-mode. Most of them are lower than 3-dB.

5-dB for LG_1 and LG_2 modes. The tested curves for the HG mode are shown in Figure 4-20 as representative. The capability of continuous frequency tuning is verified as shown in Figure 4-21, in which L_1 to L_4 represent the different switched inductance values.

The linearity of this LNA is characterized by the two-tone test for in-band IIP_3 and out-of-band IIP_2 and IIP_3. For the IIP_2 test two CW interferer tones are input at the frequencies of 2.599- and 2.601-GHz, while the LNA is configured to operate at 5.2 GHz where the IM_2 lands. The output IM_2 is measured and referred to the input by dividing the measured power

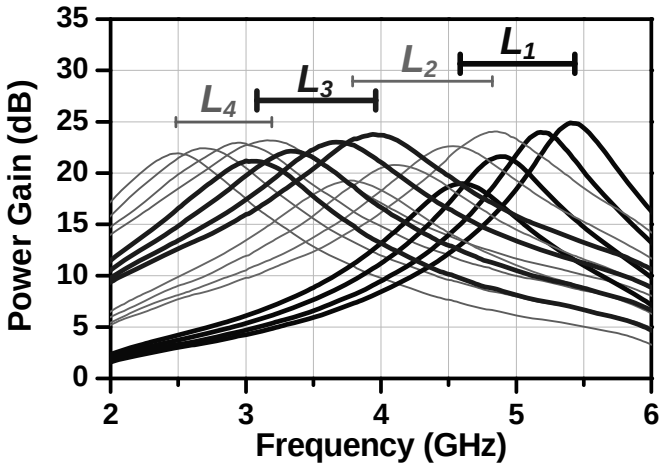


Figure 4-21. Continuous frequency tuning with coarse inductor switching and fine varactor tuning.

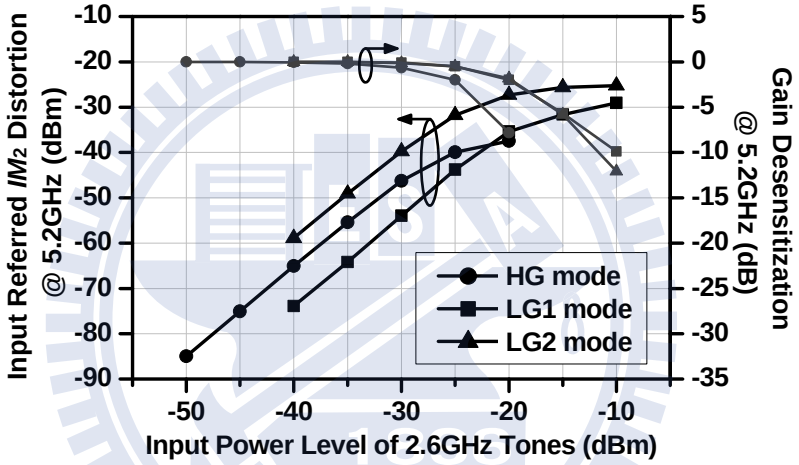


Figure 4-22. Measurement result of the 2nd order inter-modulation distortion and the gain desensitization at 5.2GHz because of the 2.6GHz interferers.

gain at 5.2 GHz to calculate the corresponding IIP_2. Similar procedure applies to characterize the out-of-band IIP_3 with the frequency set of $\{f_0, f_1, f_2\}=\{2.4, 3.8, 5.2\}$ and $\{5.2, 3.8, 2.4\}$, in which the f_0 is the configured operation frequency of the LNA. The IIP_2 measurement results are shown in Figure 4-22, in which the gain desensitization at 5.2 GHz due to the two 2.6 GHz interferers is also included. The measured IIP_2 and in-band/out-of-band IIP_3 all range from -21 to -5 dBm, depending on which gain mode is chosen. The IIP_2 control for the three gain modes is consistent with the design in Figure 4-7.

When comparing the in-band and out-of-band IIP_3, we don't see a significant difference

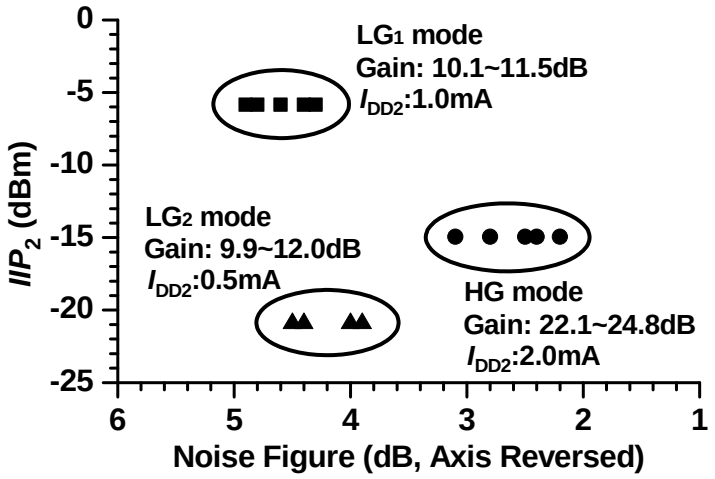


Figure 4-23. Performance corner matrix with IIP_2 as the linearity indicator.

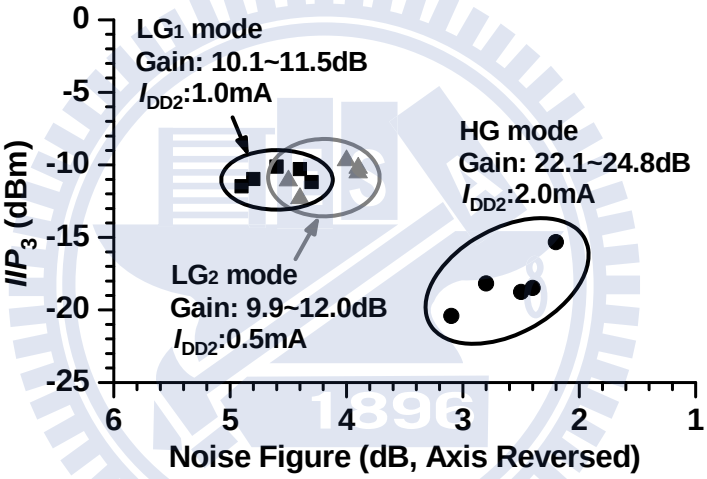


Figure 4-24. Performance corner matrix with IIP_3 as the linearity indicator.

correlated to the band-selective character of the LNA. This is because the linearity bottleneck of this LNA is in stage before the LC band-selective filter. However the band-selective filtering of LNA should be still favorable to alleviate the stringent linearity requirement of the succeeding stages.

The measured performance is summarized in Table 4-3. The performance corner matrices are shown in Figure 4-23 and Figure 4-24, using IIP_2 and in-band IIP_3 as the linearity indicator respectively. Performances at the five representative frequencies with the same performance

TABLE 4-3
PERFORMANCE SUMMARY OF RECONFIGURABLE LNA

Frequency (GHz)	2.40			3.43			3.96			4.49			5.40		
Performance Mode	HG	LG_1	LG_2	HG	LG_1	LG_2	HG	LG_1	LG_2	HG	LG_1	LG_2	HG	LG_1	LG_2
S_{11} (dB)	-14	-20	-20	-30	-18	-18	-28	-16	-16	-18	-14	-14	-17	-16	-18
S_{22} (dB)	< -18dB														
Peak S_{21} (dB)	22.1	10.5	10.2	22.6	10.5	10.0	24.0	11.7	11.0	22.6	10.9	9.95	24.8	13.3	12.0
S_{21} BW_{3dB} (MHz)	740	780	790	820	910	900	850	1010	1010	850	920	900	500	540	530
NF (dB)	2.8	4.3	3.9	2.2	4.4	3.9	2.4	4.6	4.0	2.5	4.8	4.5	3.1	4.9	4.4
In-Band IIP_3 (dBm)	-18.2	-11.2	-10.5	-15.3	-10.3	-10.2	-18.5	-10.1	-9.7	-18.7	-11.0	-11.0	-20.4	-11.5	-12.3
Out-Band IIP_3 (dBm)	-14.0	-11.3	--	--	--	--	--	--	--	--	--	--	-17.0	-15.7	--
Out-Band IIP_2 (dBm)	--	--	--	--	--	--	--	--	--	--	--	--	-15.0	-5.8	-20.9
Technology	TSMC 0.13μm RF CMOS process with UTM														
DC Power of 2nd Stage	HG: 2 mW; LG_1: 1 mW; LG_2: 0.5 mW														
Total DC Power (mW)	HG: 4.6 mW; LG_1: 3.6 mW; LG_2: 3.1 mW (1.0V supply voltage, buffer stage excluded)														

configuration are grouped. With the linearity control on IIP_2 the Figure 4-23 shows a nearly consistent result as illustrated in Figure 4-1. Therefore the performance reconfiguration conducted by switching transistor with bias control is verified. Finally, Table 4-4 compares works of multistandard LNAs published to date.

4.6 Summary

A 2.4- to 5.4-GHz wide-tuning-range performance- reconfigurable LNA is demonstrated. The broadband input stage is verified to be adequate in providing steady input matching and noise performance. The performance reconfiguration on gain, linearity, and power consumption is achieved. By use of the proposed inductance switching configuration, the multi-tapped switching inductor can be well designed to provide wide tuning range with good performance consistency. The proposed switching configuration is advantageous with the quality factor boosting but suffers from limited frequency tuning ratio. This limitation has been identified and the design reference is given in (4-21). As a result, this prototype has proven the high

TABLE 4-4
COMPARISON OF LNAS FOR MULTISTANDARD APPLICATIONS

Ref.–Year	Technology	Frequency Response of S_{11} / S_{21} [a]	Frequency Coverage (GHz)	S_{21} Bandwidth (GHz)	Noise Figure (dB)	Max. S_{11} (dB)	Gain (dB)	Vari.Gain Range (dB)	IIP_3 (dBm)	Max. Power (mW)
[27] –2005	0.13μm CMOS	BB / BB	DC – 6.5	6.5	2.9 – 4.2	-10	19	N/A	+1	11.7
[35] –2006	0.18μm BiCMOS	BB / BB	1.5 – 2.2	> 2.2	1.5 – 1.9	-14	16.2 – 17	N/A	+2	26
[19] –2007	0.13μm CMOS	BB / BB	1.0 – 7.0	7.0	2.4 – 3.0	-10	17	N/A	-4.1	25
[20] –2007	90nm CMOS	BB / BB	DC – 6.0	6.0	2.5 – 3.2	-10	17.4	N/A	N/C	9.8
[21] –2007	90nm CMOS	BB / BB	0.5 – 7.0	7.5	2.3 – 2.9	-7.2	22	N/A	-10.5	12
[36] –2007	0.18μm CMOS	BB / MB	0.95/2.4/5.25	0.5/2.5/1.0	4.4 – 4.6	-7/-15/-10	18/24/23	N/A	-12.8 – -15.3	32.4
[37] –2006	0.35μm SiGe	MB / TSB	2.4/4.9–5.9	1.0	2.9/3.1–3.6	-17.5	20 – 29	N/A	-13 – -18	16
[28] –2005 [b,c]	0.25μm SiGe	BB / TSB	4.9 – 5.8 [d]	0.7	2.3 – 2.5 [b]	-10	31 – 31.5 [b,c]	11 [b]	-9.5	40 [b]
[29] –2006 [b]	0.13μm CMOS	BB / TSB	1.8/2.1/2.4	0.4/0.6/0.5	5.2/5.6/5.8 [b]	-20	23.4 – 29.5 [b,c]	15 [b]	-7.5 – 0	24 [b]
[38] –2007	0.18μm CMOS	BB / TSB	0.9/1.8/5.2	0.2/0.4/0.6	2.3 – 2.9	-12	13 – 16	N/A	-14	7.5
This work [9] [c]	**0.13μm CMOS**	**BB / TSB**	**2.4 – 5.4 [d]**	**0.5 – 1.0**	**2.2 – 3.1**	**-12**	**22 – 24**	**12**	**-16 – -21**	**4.6**

[a] In frequency response, BB: broadband, MB: concurrent multiband, TSB: tunable/switchable single band.
[b] Performance of entire receiver front-end including LNA and quadrature mixer.
[c] Performance in high gain mode as representation. [d] Continuous frequency tuning.

performance flexibility and wide-range tuning of LNA within the below-average low power consumption.

4.7 Appendix

As the L_X in Figure 4-13 is switched to $L_{X,MIN}$, the Z_{tank} can be derived as

$$Z_{\text{tank}}\Big|_{L_{X,MIN}} = \frac{j\omega L_1\left[1-\omega^2(1-k^2)L_2C_2\right]}{1-\omega^2\left(L_1C_1+L_2C_2\right)+\omega^4(1-k^2)L_1C_1L_2C_2} = \frac{j\omega L_1\left[1-\omega^2(1-k^2)L_2C_2\right]}{\left[1-\omega^2(1-k^2)L_2C_2\right]\left(1-\omega^2L_1C_1\right)-\omega^2k^2L_2C_2}, \quad (4\text{-}22)$$

in which two poles and one zero can be found on the positive ω-axis. The two poles are located at frequencies as solved in (4-20). We can determine which pole frequency is our case by testing their continuity to ω_{min} as $L_{X,MIN}$ is approaching $L_{X,MAX}$, by setting $L_1 \rightarrow L_{X,MAX}$ and $L_2 \rightarrow 0$. In this test the higher pole frequency can be found approaching infinity whereas the lower pole meets the ω_{min}. Therefore the minus sign is applied in (4-20).

There are two singular cases not applicable to the above discussion, k = 0 and k = 1. In the

case of k = 0, i.e. no mutual coupling between coil sections, the pole dominated by L_2C_2 is cancelled by the zero in (4-22) so that the resonance frequency is determined only by L_1C_1. Thus the frequency tuning ratio discussed in Section III-B is unlimited as the L1 can be designed arbitrarily small. In the case of k = 1, the denominator in (4-22) is diminished contributing only one pole, which makes the ωmax in Section III-B to be

$$\omega_{\max}\big|_{k=1} = 1\Big/\sqrt{L_1C_1 + L_2C_2}\ . \tag{4-23}$$

Given a fixed $L_{X,MAX}$, the achievable frequency tuning ratio in this case is limited by the complementary relationship between L_1 and L_2 in (4-16). These two special cases, though not practical to this work, also roughly show how the mutual coupling affects the frequency tuning ratio in the use of the proposed switching inductor.

Chapter 5

RF T/R Switch

5.1 Introduction

Wireless communications in multi-gigahertz frequency bands have explosive growth that requires low cost components for mass markets. Integrating critical off-chip RF devices into the CMOS chip of the transceiver system is essential. One important component is the transmit/receive (T/R) switch that routes the antenna to either the transmitter or receiver. The major obstacle to making a high-performance CMOS T/R switch is the conductive substrate and the relatively large on-resistance of CMOS transistors. The former limits the power handling capability while the latter increases insertion loss. Thus, new techniques need to be developed and applied to improve the performance of T/R switches that are superior to series-shunt switch structures [39] for integration.

Techniques developed for MMIC design can be applied to CMOS with appropriate modifications. Transistor stacking can be used to increase power handling capability. This

requires, however, an isolated body for each transistor. In CMOS technology, this can be achieved by the use of either a special process [40] or by creating a high isolation body connection [41]. Inductors in parallel with the transistors can be used for narrowband applications to tune-out the parasitic capacitance to improve the isolation and the input matching at high frequencies [42]. The LC-resonance technique can further be exploited to eliminate the large voltage swing across transistors during transmission [43], [44]. When integrated with an LNA and PA, this technique can improve performance significantly [45], [46].

In this chapter we present a low-cost T/R switch fabricated in 90nm CMOS employing thick oxide NMOS transistors with 0.32μm channel length. The switch achieves greater than 30dBm power handling capability with less than 1dB insertion loss in the frequency band from 4.9GHz to 6.0GHz. The switching transistors are placed inside the inductors to save die area.

5.2 Design Considerations

A typical single-pole double-throw (SPDT) T/R switch is composed of two switches: one for the transmitter (TX) to the antenna (ANT) and one for the ANT to the receiver (RX). The functional requirements are described separately in transmit and receive modes. In transmit mode, the TX-side switch is required to pass the large RF signal from the power amplifier (PA) to ANT with low insertion loss, and the RX-side switch has to protect the low noise amplifier (LNA) of receiver from the large PA voltage swing. This voltage swings 20V peak-to-peak when a signal of 30dBm, the target signal level in this design, is transmitted into 50Ω. Thus, the RX-side switch in “OFF”-state should tolerate this voltage swing and ensure the voltage swing appearing at the LNA input is sufficiently low. Additionally, it should not dissipate significant signal power. In receive mode, the RX-side switch should have a low insertion loss so as not to

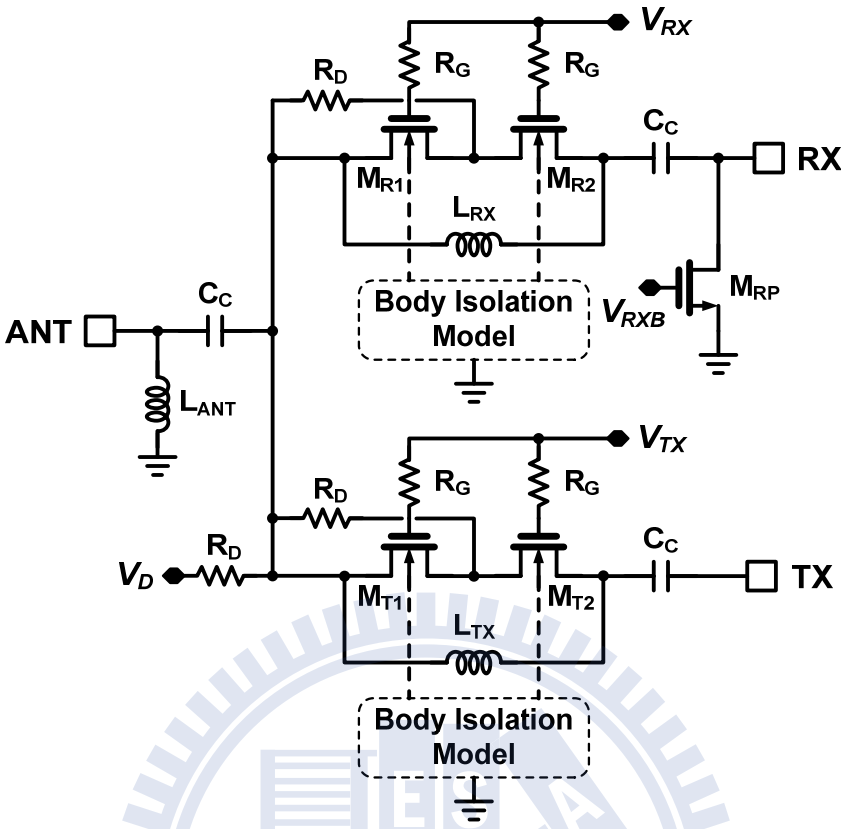


Figure 5-1. Schematic of the proposed SPDT T/R switch.

significantly degrade noise figure (typically less than 1dB). The TX-side switch also needs to have good isolation in receive mode so as not to draw power from the ANT, which would increase insertion loss.

5.3 A 4.9 – 6.0 GHz T/R Switch

5.3.1 Circuit Design

The schematic of the T/R switch is shown in Figure 5-1. The TX and RX-side switches are nearly identical for extension to multi-pole multi-throw applications. On the RX side, an additional shunt transistor (M_{RP}) improves isolation to the LNA during transmit mode. In this

mode, the RX node voltage swing is very small. Two transistors are stacked in series (M_{R1}–M_{R2}) to absorb the large voltage swing from the ANT node. Thick-oxide NMOS transistors with a highly isolated body are employed (M_{R1}, M_{R2}, M_{T1}, and M_{T2}). The gate voltages are controlled through large-valued resistors (R_G). Thus, the body and gate nodes are AC bootstrapped and follow the drain/source node voltages, reducing the voltage across the drain/source-to-body junctions and drain/source-to-gate oxide. Therefore, power handling capability is improved without breakdown.

The body isolation is a key technique enabling the MOS transistors to handle high power. In CMOS technology this can be achieved by using a mask which blocks a high dosage P implant. This is sometimes referred to as an "RF block" and used for the implementation of on-chip high-Q inductors. The P region underneath an NMOS transistor is approximately "isolated" from the global P implant, as shown in Figure 5-2(a). Therefore, the connection of the body to ground is via the P-substrate beneath, which has a higher resistivity of about 80Ω-cm.

An accurate impedance model of the body isolation was created/verified since the P region is still of finite resistance. An EM simulator was used to accomplish this. For this design, the body isolation impedance was analyzed as a two-port network because there are two transistors in series which have body connections to model. The frequency-independent equivalent circuit model is shown in Figure 5-2(b). The values of the elements in this model correlate closely to the geometric parameters in Figure 5-2(a), including the *clearance*, *space*, and *body area* of the P region. It is interesting that a larger *clearance* doesn't ensure a higher R_{sub}: the maximal R_{sub} value appears for a *clearance* close to 100μm in the process we use. By varying the geometric parameters, their optimal values can be obtained as well. The actual geometric optimization also takes die area into account.

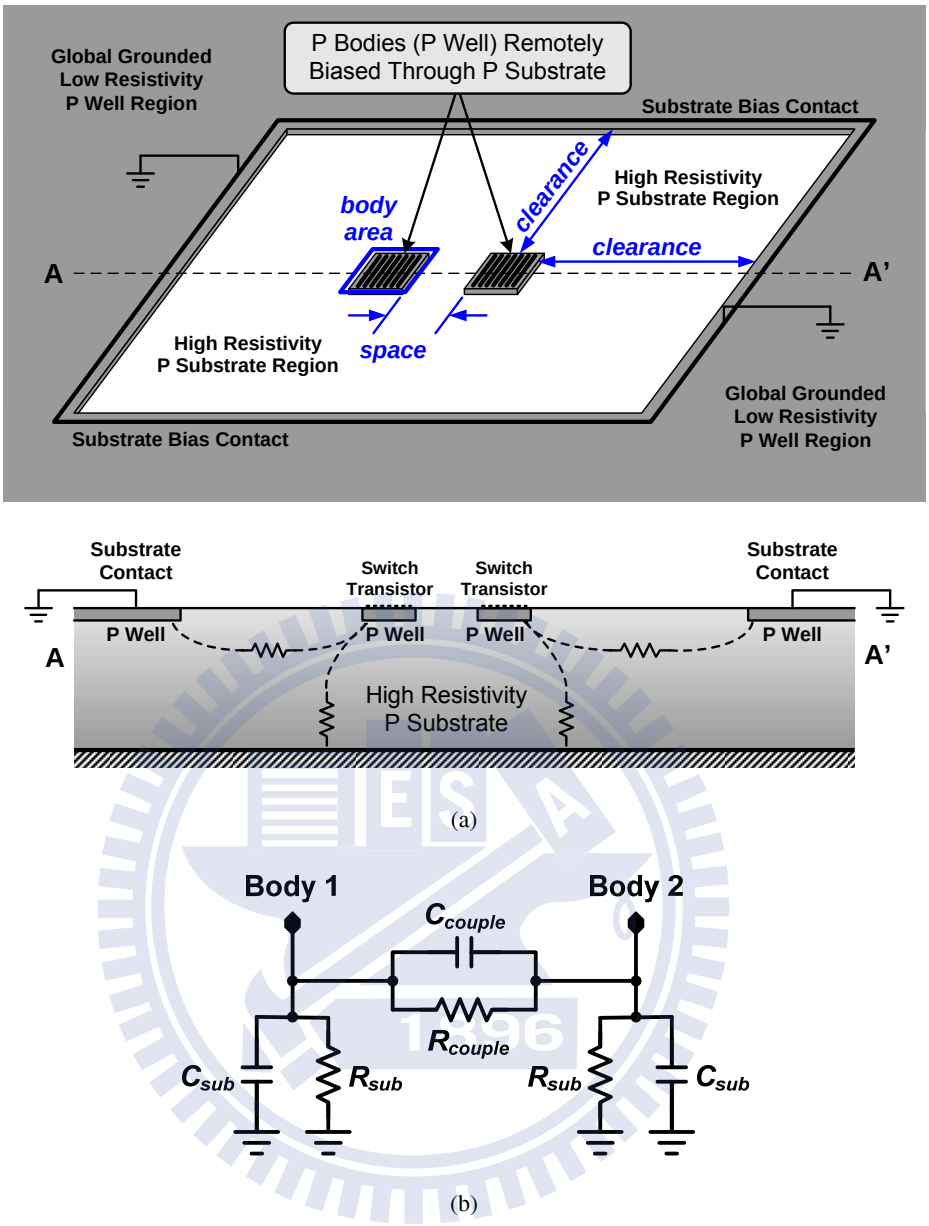


Figure 5-2. Fulfillment of body isolation technique. (a) Layout of P-bodies for sufficient isolation; (b) Frequency-independent circuit model for parameter extraction.

The other important performance metric for a T/R switch is the low insertion loss. To achieve less than 1dB insertion loss a very large NMOS transistor is typically required, particularly when a longer gate, thick-oxide device is employed. When these transistors are turned off, their significant parasitic capacitance severely deteriorates the isolation of the switch. Inductors (L_{TX}, L_{RX}) in parallel with the series transistors are introduced to solve this problem.

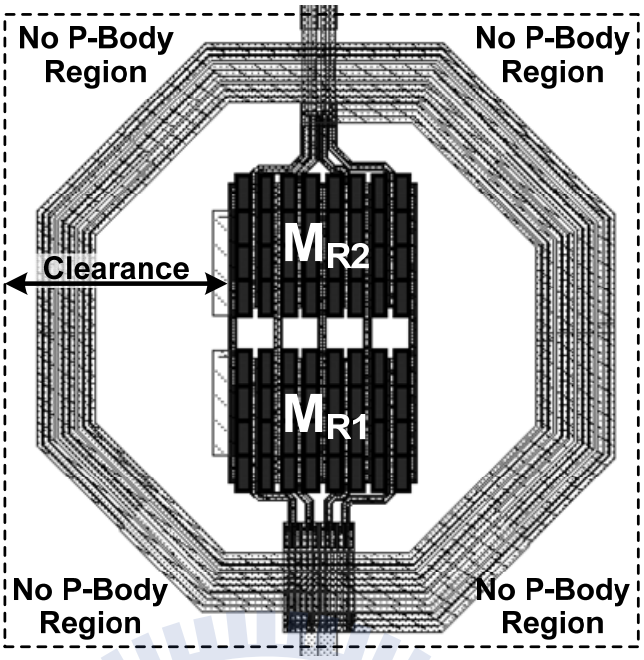


Figure 5-3. Transistor inside inductor coil for chip area reuse.

Therefore, isolation and insertion loss are managed to an acceptable level.

Degraded isolation in RX-mode can also be caused when switch transistors that are off are turned on by a large RF signal. In this case, the source and drain of the transistors are reversed and the large RF signal turns the off transistors on. This can be avoided or postponed by biasing the drain and source terminals to a relatively large voltage (2.5V) while biasing the gates at a low voltage (0V). The control-"ON" voltage is consequently elevated to a higher voltage (5V). This arrangement also helps to prevent the drain/source-to-body junction from forward biasing, which leads to additional nonlinearity.

At the ANT node there's an additional shunt inductor, L_{ANT}. This inductor improves input/output matching and provides ESD protection. The three tank circuits associated with the three inductors in this switch design were targeted for the same resonance frequency at 5.5GHz.

The switching speed of the T/R switch is set by the gate resistors R_G. These were chosen to be 10kΩ to provide less than 25ns turn-on and turn-off time, which is acceptable for WLAN

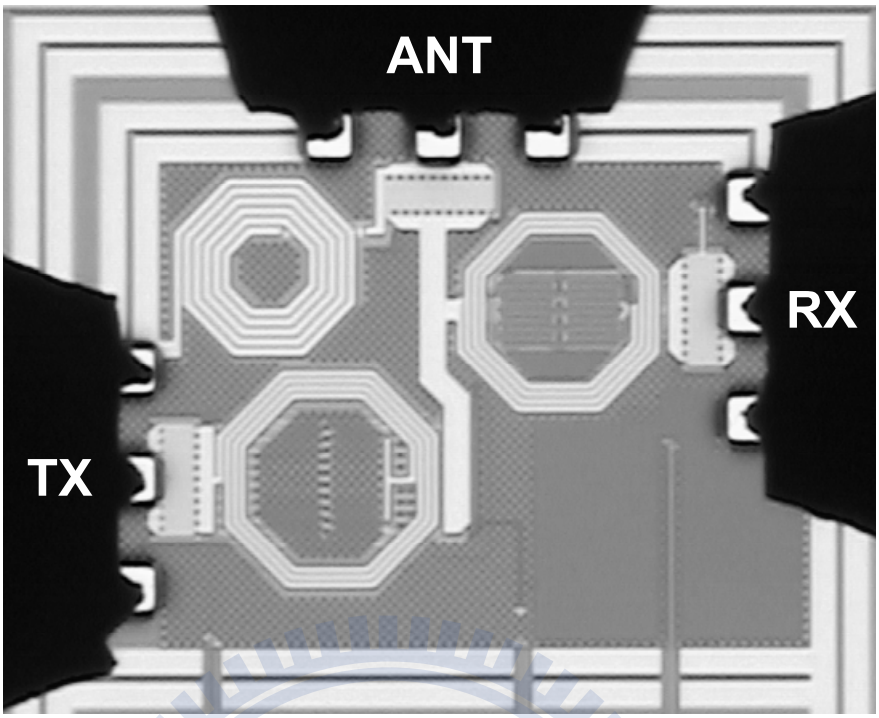


Figure 5-4. Micrograph of the fabricated chip under test.

applications. The turn-on/turn-off time is defined as the time from 50% control signal to when the 90%/10% signal power level is achieved. The simulated turn-on/turn-off time are both less than 15ns.

5.3.2 Chip Implementation and Measurement Results

The T/R switch is fabricated in a 90nm, seven metal CMOS process where the NMOS switch transistors coexist in a common P substrate. From the previous section it was mentioned that the isolated-body transistors and the parallel inductors both occupy large chip area but don't operate simultaneously. Thus, they can share the same chip area in layout as shown in Figure 5-3. The layout of the transistors inside the inductor coils do not form closed loops, which would increase losses from eddy currents and degrade the quality factor of the inductors. Metal current density is important with a 30dBm signal, which gives rise to a peak current of

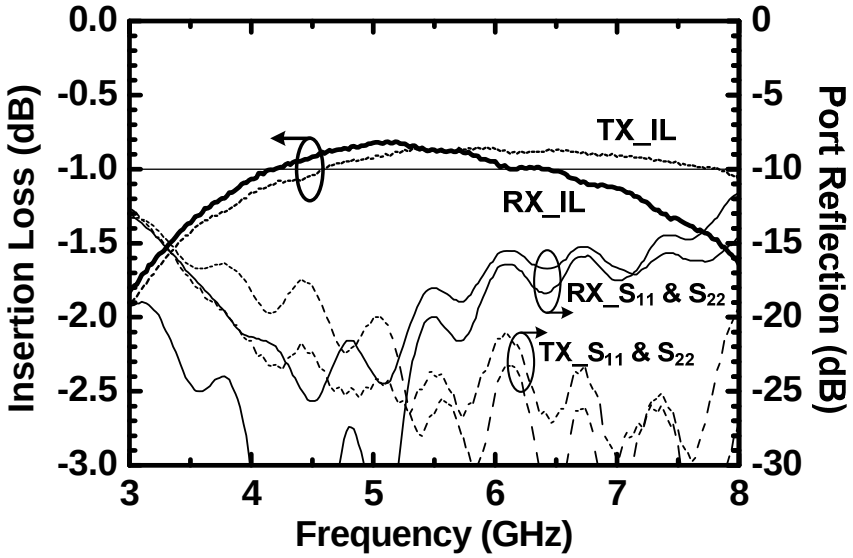


Figure 5-5. Insertion losses in TX and RX modes.

200mA. The current in the resonance tank was also evaluated carefully and considered in the inductor design. Finally, a full-chip EM simulation was performed as part of a post-layout simulation for best accuracy.

A micrograph of the fabricated T/R switch is shown in Figure 5-4. The active die area is approximately 0.5×0.4 mm^2. All the performance tests, including insertion loss, isolation, and linearity are conducted with an Agilent E8362B network analyzer. A PA is used for compression testing and the signal power fed into the switch input is calibrated with a power meter. Figure 5-5 shows the insertion loss and the input/output port reflection of the T/R switch. Each port in the turned-on path in both transmit (TX) and receive (RX) modes is well matched to 50Ω. Figure 5-6 shows the isolation in TX and RX modes. It can be seen that the resonance of the RX switch transistor is approximately 500MHz lower than the deign value of 5.5GHz. The input/output power sweep is shown in Figure 5-7. We speculate that punch-through or other mechanism may be occurring at an input power higher than 29.6dBm. At an input power range of 29.6dBm to 30.3dBm, the output power is relatively constant, which might be caused by

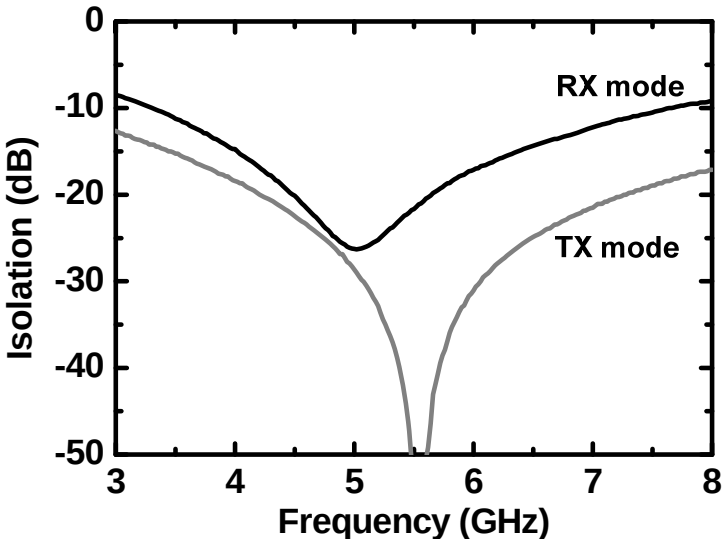


Figure 5-6. Isolation in TX and RX modes.

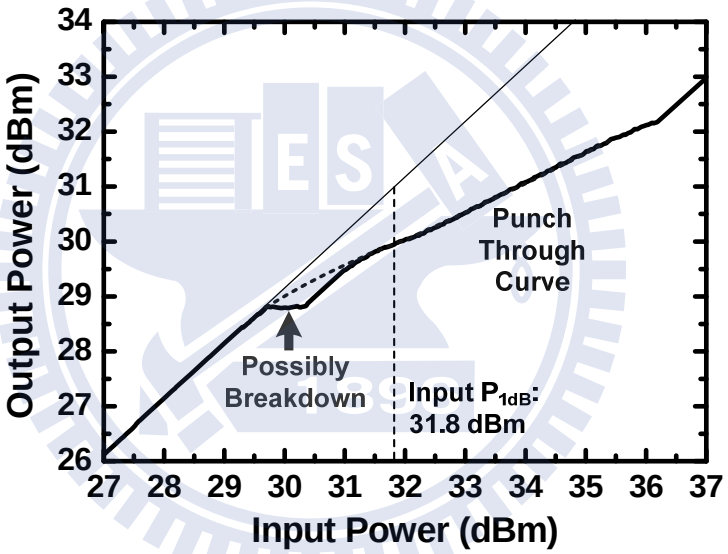


Figure 5-7. Power sweep test result at 5.6GHz.

breakdown of the drain-body-source parasitic NPN BJT. The measured input P_{1dB} is 31.8dBm. The performance of the T/R switch is summarized and compared with other works in Table 5-1.

5.4 Summary

A CMOS T/R switch based on a series-shunt resonant switch structure has been designed

TABLE 5-1 PERFORMANCE COMPARISON OF T/R SWITCHES

T/R Switches	This Work		Xu [41]		Talwalkar [44]	
Freq. (GHz)	4.9~6.0		0.9		2.4	
Operation Mode	TX	RX	TX	RX	TX	RX
Insertion Loss (dB)	0.86	0.82	0.5	1.0	1.5	1.6
Isolation (dB)	> 27	> 17	37	29	32	17
Reflection (dB)	> 20		> 20		> 12	
IP_{1dB} for TX (dBm)	31.8		31.3		28.5	
Chip Area (mm^2)	0.2		0.11		0.56	
CMOS Technology	90nm		0.13μm		0.18μm	

and tested at 4.9–6.0GHz. Techniques including stacked transistor, body isolation, parallel inductor resonance, and transistors inside inductor coils have been presented. Body isolation was carefully analyzed with an EM simulator and characterized to obtain the optimal design parameters. Parallel inductor resonance improves isolation and insertion loss. Transistors inside inductor coils are executed to save area without introducing additional losses. 0.9dB insertion loss and 30dBm power handling capability are achieved from 4.9–6.0GHz in a 90nm CMOS process. Measurement results verify the performance and demonstrate the feasibility of integrating a 4.9–6.0GHz T/R switch in a CMOS transceiver chip.

Chapter 6

Conclusion & Future Works

In this thesis we successfully developed BSNIM solution for LNA design. As shown in Chapter 3 and 4, the good input matching and noise performances are obtained within low DC power consumption. The device parasitic effects are also well utilized as part of design. Switching techniques for reconfigurable LNA were developed and verified of very consistent performance among different configurations. The CMOS RF T/R switch project demonstrates the feasibility of high performance RF switch in CMOS process.

The trend of transceiver front-end is to integrate the RF T/R switch with LNA and PA of receiver and transmitter, respectively. As shown [46], we have obtained very promising results of such integration. In the future we expect more and more integration at transceiver front-end with the optimized performance. Low-cost, low-power, and small form factor of transceiver are always the clear and meaningful targets to pursue.

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Publication List

(A) *Journal Papers:*

(1) Chang-Tsung Fu, Chiun-Lin Ko, Chien-Nan Kuo, and Ying-Zong Juang, "A 2.4–5.4-GHz Wide Tuning-Range CMOS Reconfigurable Low-Noise Amplifier," *IEEE Trans. Microw. Theory Tech.*, vol.56, no.12, pp.2754-2763, Dec. 2008.

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(B) *Conference Papers:*

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(C) *Issued Patents:*

(1) US 7,339,436
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Inventors: Chang-Tsung Fu and Chien-Nan Kuo.

(D) *Pre-granted Patents:*

(1) US 20080272824
"CMOS RF switch for high-performance radio systems"
Inventors: Chang-Tsung Fu and Stewart S. Taylor.

(2) US 20090021295
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"Using radio frequency transmit/receive switches in radio frequency communications,"
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