國立交通大學

電機與控制工程學系

碩士論文

用於可選擇式多輸出直流-直流轉換器

之改良雙相位交錯式電荷幫浦技術

Improved Dual Phase Cross-Coupled Charge Pump Techniques

for Selectable Multi-Output DC-DC Converters

研 究 生：林立家

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摘 要

液晶顯示面版越來越普及，應用的範圍越來越廣。從掌上型電玩，手機等小型液晶顯示面版到液晶電視甚至戶外液晶顯示看板之大型液晶顯示面版。因此液晶面版的電源供應也越來越重要。電源供應區塊也希望能夠整合至驅動電路之內，因此朝著縮小晶片面積以及外部元件的縮小方向前進。

液晶顯示器的電源需要多組不同位准的電壓來對液晶進行充放電的動作。而在直流電壓轉換器當中，電感式直流電壓轉換器需要外部元件電感，而電荷幫浦需要外部元件電容。比較之下，電感較電容佔較大面積，而在應用上，液晶顯示面版需要一個負的電壓位准來對液晶電容做放電動作，電感式直流電壓轉換器無法產生負的電壓位准。因此在成本與面積的考量之下，我們利用電荷幫浦取代了常見的電感式直流電壓轉換器。而電荷幫浦在操作時會產生的漣波利用改良式的雙相位交錯式電荷幫浦架構來減少漣波。

本論文實現了一個使用改良的雙相位控制電荷幫浦對輸出做可切換式選擇的多輸出直流-直流電源轉換器。輸入為 10V 的高電壓，可以提供四組不同的電壓選擇，分別為 10V、20V、-10V 以及 0V，最大電流負載為 50mA。利用 TSMC 0.25um BCD 2.5V/5V/12V/40V 1P5M 製程進行模擬以及製作驗證。

Improved Dual Phase Cross-Coupled Charge Pump Techniques for Selectable Multi-Output DC-DC Converters

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Abstract

LCD panels are going more and more popular. The applications of the LCD panels are widely spread in our daily life. From the small LCD panels on palmtop entertainment machine and cell phone to the large LCD panels on LCD TV or outdoor display screen. Therefore, the power supply blocks for LCD panels are more and more important. The needs to integrate the power supply block into the LCD driver circuits are rise in great demands. In other words, it is necessary to reduce the size of the power supply block chip and reduce the number of the external components.

The power sources for LCD panels need different voltage scale to charge and discharge the liquid crystal capacitors. Among the DC-DC power converters, inductive switching converters need external components as inductors and charge pumps need external components as capacitors. Compare these two external components inductors and capacitors, inductors occupy larger board area than that of capacitors. Besides, LCDs need a negative voltage to discharge the liquid crystal capacitors. It is difficult for Inductive switching converters to generate a negative voltage. Therefore, for cost and area considerations, we use charge pumps to replace inductive switching converters. In this thesis, the ripple of the charge pump is further reduced by an improved double phase cross-coupled charge pump structure.

This thesis implements a switchable multi output DC-DC converter utilize improved dual phase cross-coupled charge pumps. The input voltage is a high voltage 10V. The circuit can supply 4 different output voltages, 10V, 20V, -10V and 0V. The maximum current load is 50mA. The chip is simulated and fabricated by TSMC 0.25um 2.5V/5V/12V/40V 1P5M BCD process CMOS technology.

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Chapter 1

Introduction

1.1 Background

Today, the electronic devices are widely used in modern society. Any one of us is using more and more electronic devices in our daily life. Especially the portable electronic devices are growing in great demands. The devices which was not carryon in the past, now all can be portable. Such as laptops, DVD players, MP3/MP4 players, digital cameras, PDAs, even iPods. All these devices need a battery for providing the voltage. But the battery only provides single voltage level. Though, in these devices there are different components needing different voltage levels. Many of these devices have built-in memories which need a negative voltage level. That's why we need DC-DC converters. For example, there are LCD monitors, chipsets, hard drives and flash memories in multimedia players. Especially in the LCD monitors, it needs many different voltages to control the gate driver. And all these components need different voltage levels and currents. A DC-DC converter can provide different levels of voltage and transfer different currents for components inside the portable devices. With an input voltage, a DC-DC converter will provide an output voltage whose level is higher or lower than the input voltage, even more, lower than the ground voltage. The DC-DC converters in modern days are expected to be as small as possible, so that on-chip DC-DC

converters are more and more popular. Since DC-DC converters provides the power that the devices need, the power consumption of the DC-DC converter itself must be as small as possible. So the designs of DC-DC converters nowadays are toward small chip area, low power consumption and high efficiency.

1.2 Overview of DC-DC converters

There are different types of DC-DC converters. In all of the DC-DC converters, the most well-known types are linear regulators, switching regulators and charge pumps. We use them for different needs, such as small chip area, low power consumption, high conversion efficiency, low output ripple, low quiescent current consumption and sufficient output regulation. Each of the DC-DC converters mentioned above has its own advantages and drawbacks, for different needs we use different types.

1.2.1 Linear Regulators

The advantage of linear regulators among all DC-DC converters is that it has much smaller output ripple, lower output noise and smaller chip area. The advantage of its small output ripple makes it much important in the power management design. To use this advantage, we often cascade linear regulators behind the switching regulators to further reduce the output ripple of the switching regulators. Fig. 1 is the block level diagram of a generic linear regulator. The circuit of the generic linear regulator is composed of an error amplifier, a pass element, feedback block and a voltage reference generated by a zener diode or a bandgap reference. The voltage reference needed to provide a stable DC bias voltage with suitable current driving capabilities. When choosing the voltage reference, the zener diodes are usually used in high voltage circuits which the voltage is greater than approximately 7V.

The bandgap voltage references are better when working in low voltage environment and have higher accuracy. The regulation is made by a loop of the error amplifier, the pass element and the feedback block to generate a regulated voltage.

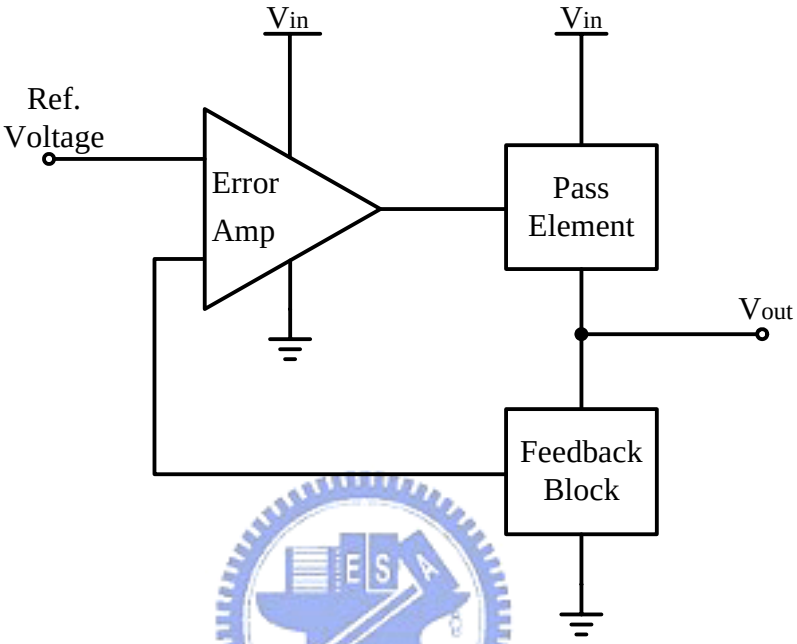


Fig. 1. Generic linear regulator architecture

There are different types of linear regulators, such as the linear regulator using NPN BJT as the pass element, the low drop-out regulator using NMOS as the pass element and the low drop-out regulator using PMOS as the pass element. The linear regulators which use MOS transistor as the pass element are called low drop-out regulators because they have smaller drop-out voltage. Drop-out voltage is the voltage difference between input voltage and output voltage. If we want to have the highest efficiency, the drop-out voltage needs to be small. The lower the drop-out voltage is, the higher the efficiency can be achieved.

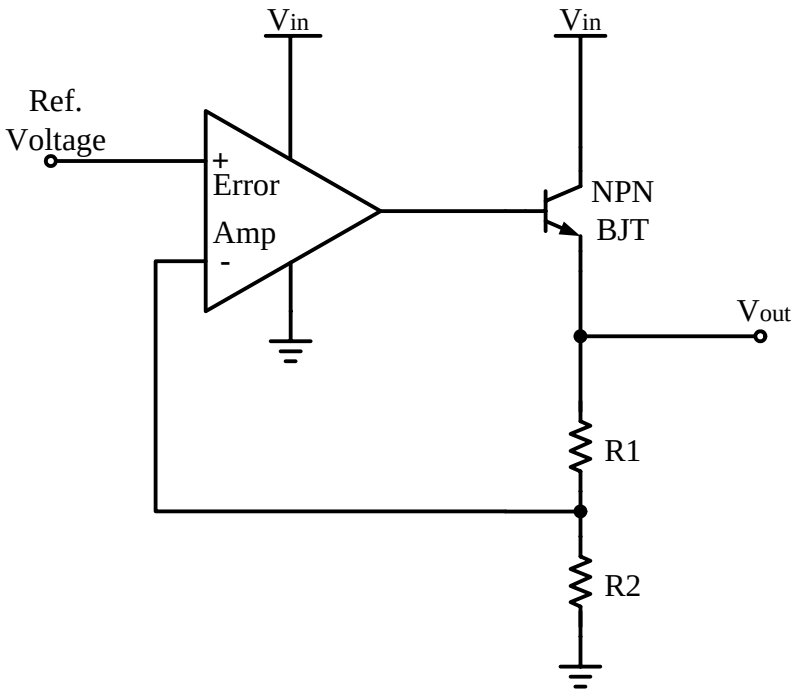


Fig. 2. Linear regulator using NPN BJT as the pass element

There are many configurations for the pass element, such as NPN Darlington, common emitter lateral PNP, NPN emitter follower (NPN BJT), NMOS source follower and common source PMOS transistor [1]. And in these configurations, the most common used are NPN emitter follower, NMOS source follower and common source PMOS transistor. Fig. 2 shows a linear regulator which uses a NPN BJT (Bipolar Junction Transistor) as its pass element. When a BJT is used as the pass element, the output current of error amplifier controls the base of the BJT. As the emitter terminal is connected to output, makes it an emitter follower. And use this emitter follower controlled by error amplifier to regulate the output voltage. The issue of this type of linear regulators is that it will face the stability problem. Because the output impedances of linear regulators those use emitter followers as the pass elements are small. Therefore, the pole created by output node's RC constant is very large under any loading conditions. The drop-out voltage of NPN BJT is larger than the MOS transistor type, which leads to lower efficiency. And the bipolar junction transistor is more difficult to integrate it into CMOS processes.

The MOS transistor used as the linear regulator's pass element will decrease the drop-out voltage and makes the linear regulator a low drop-out linear regulator (LDO). Fig. 3 shows a low drop-out linear regulator using a NMOS pass transistor where source follower architecture is formed. The issue of this type low drop-out linear regulator is that the voltage at gate terminal of the NMOS transistor should be higher than the voltage of source terminal. When the drop-out voltage is small, it means that the voltage between drain terminal and source terminal is small. It makes that the voltage of gate terminal even higher than the voltage of drain terminal. So the supply voltage of error amplifier needs to have an additional boost converter to provide a higher voltage level than Vin.

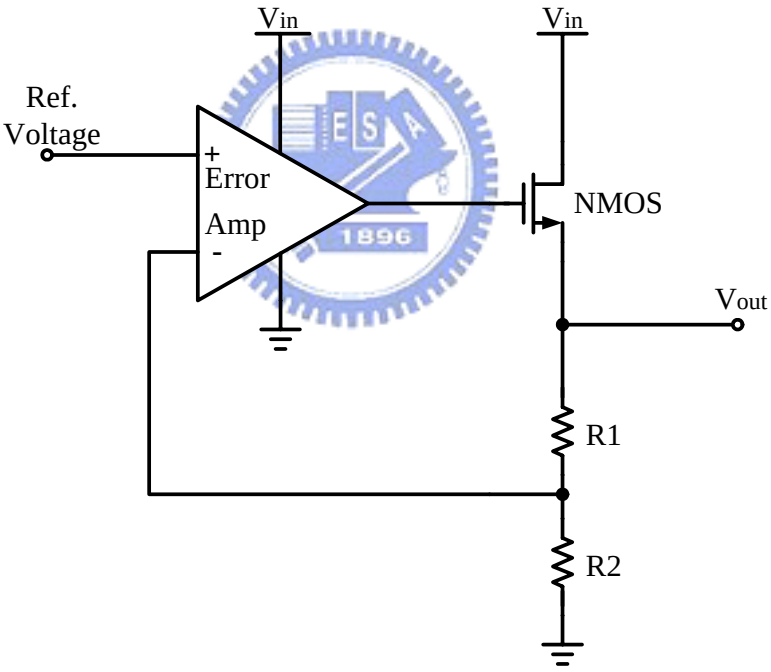


Fig. 3. Low drop-out regulator using NMOS as the pass element

Because of the extra boost converter is extended in the NMOS type low drop-out linear regulator. So the low drop-out linear regulators using PMOS as pass element are widely used. The low drop-out linear regulator using PMOS does not need an additional boost converter such as charge pumps to provide a high voltage level. Fig. 4 shows the architecture of a low

drop-out linear regulator using PMOS as its pass element.

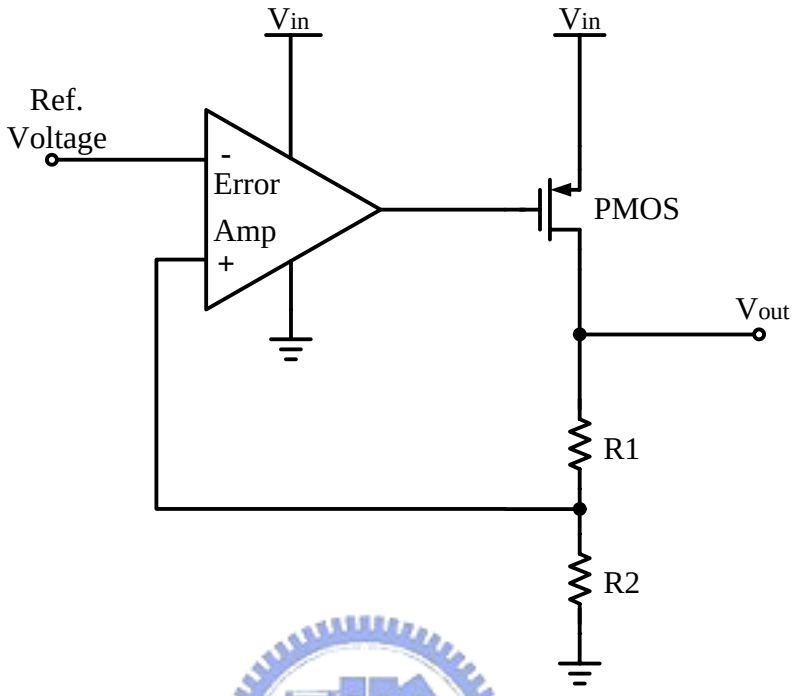


Fig. 4. Low drop-out regulator using PMOS as the pass element

The drain terminal of the PMOS transistor is connected to the output of the linear regulator, such that output impedance of the linear regulator is much larger. Such that a low frequency pole occurred by the load will pop. So the stability problem will be the issue of this type low drop-out linear regulator.

1.2.2 Switching Regulators

Switching regulators are popular power management devices. It utilize switches to transfer energy and use inductors and capacitors to conserve and deliver energy. The output voltage is controlled by the ON time and OFF time of switches. The output of the switching regulator is an unregulated voltage. The ripple is larger than the linear regulator mentioned above. Switching regulators have different structures which can generate different output

voltage levels. They can variously generate step-up, step-down and combination of step-up and step-down. The step-up switching converters are called boost converters. The step-down switching converters are called buck converters. And the switching converters combine step-up and step-down are called buck-boost converters [2].

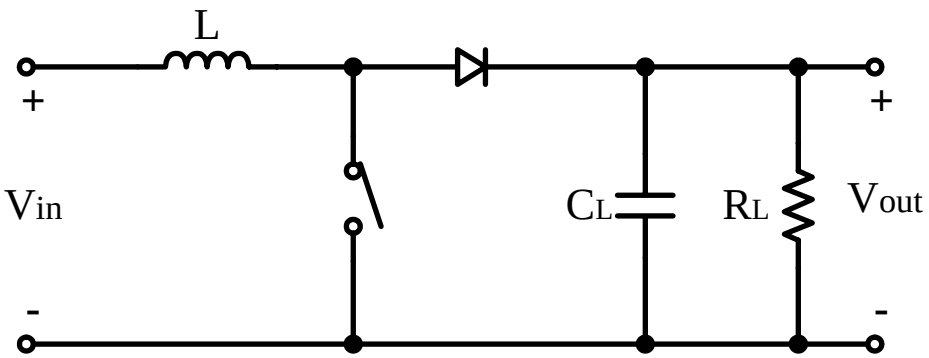


Fig. 5. The boost converter

The boost converter which can generate a voltage level higher than the input voltage is shown in Fig. 5. It is constructed by an inductor, a switch controlled by control block, a diode as a switch, a load capacitor and a load resistor. The function of the boost converter will be mentioned below. First, during the switch is turned ON, the diode is turned of because of the reverse bias, and the supply power Vin will store the power on inductor though the switch as current form. And during the next step when the switch is turned OFF, the energy will be delivered to the output by both input source and the inductor. So the output voltage level is boosted to a higher voltage level than the input voltage level.

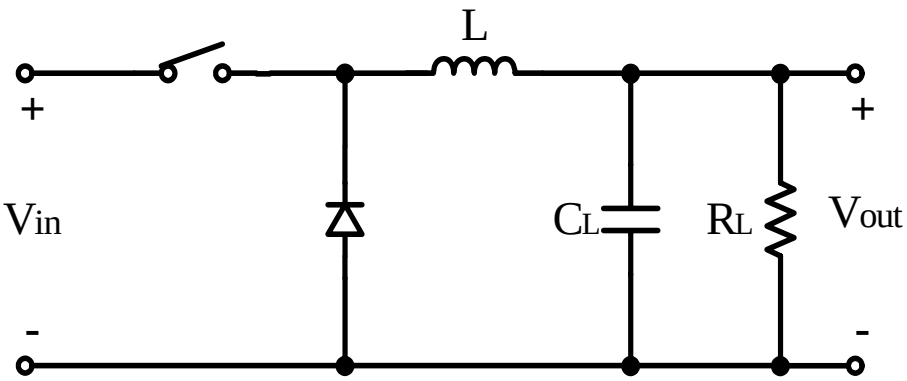


Fig. 6. The buck converter

Fig. 6 shows the architecture of the buck converter. Buck converter can deliver an output voltage lower than the input voltage. Let's see how it works. First, during switch is turned ON, the diode is reverse biased by the input voltage and being turned OFF. Input voltage source than provide energy to the load through inductor. After that, during switch is turned OFF, the diode will be turned ON and the energy in the inductor which stored in previous state will deliver to the output load capacitor through diode. Then the output voltage is a constant voltage level lower than the input voltage if inductor L and capacitor CL form an low-pass filter.

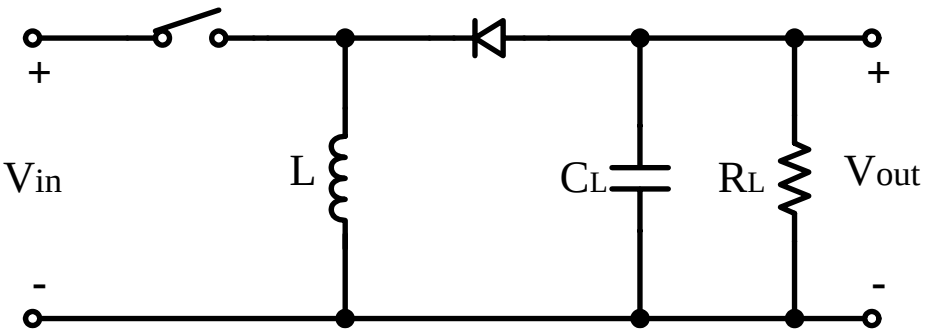


Fig. 7. The buck-boost converter

Fig. 7 is the block diagram of a buck-boost converter. We could cascade a boost converter and a buck converter to be a buck-boost converter. A buck-boost converter can

generate an output voltage higher or lower than the input voltage which depends on the input voltage level. If the input voltage is too high, it will generate a lower output voltage. If the input voltage is too low, it will generate a higher output voltage. Such that we can produce a constant output voltage weather the input voltage is higher or lower than the output voltage we want. During the switch is turned ON, input voltage source delivers energy to the inductor and turned of the diode with reverse biasing. And next during the switch is turned OFF, only the energy stored in the inductor transfer to the output node.

1.2.3 Charge Pumps

The basic concept of the charge pump is to generate a voltage level higher than the input voltage level of the chip's supply voltage. But under specific conditions, charge pump can also be used to produce a voltage lower than the input voltage, even more, produce a negative voltage. The main components in a charge pump are switches, capacitors and a control circuit which provides a two phase control signal.

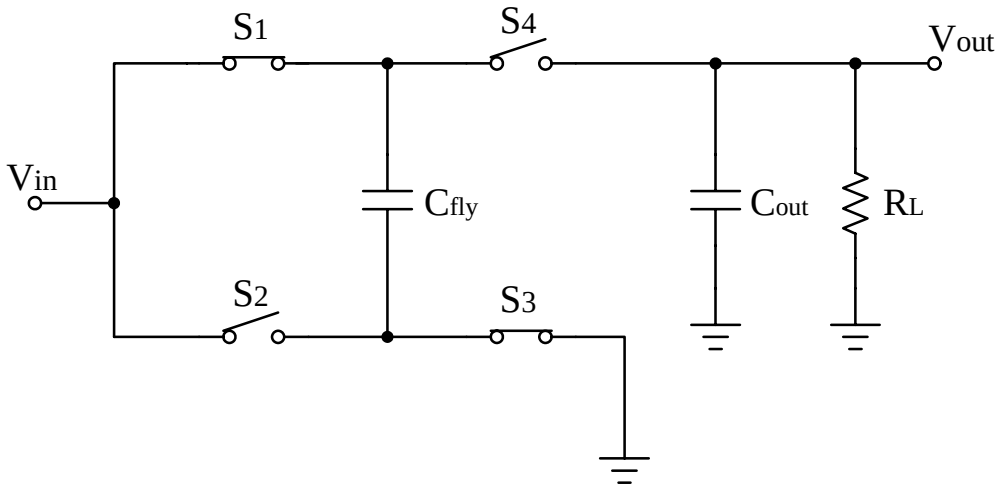


Fig. 8 Phase 1 of the basic charge pump

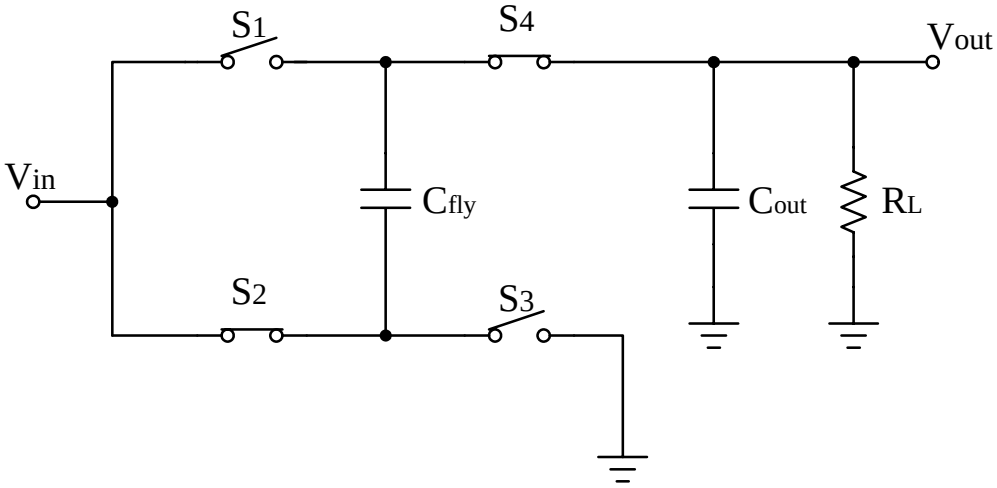


Fig. 9 Phase 2 of the basic charge pump

Fig. 8 and Fig.9 show the two phases of a basic charge pump. During phase 1, as Fig. 8 shows, switches S_1 and S_3 are closed, switches S_2 and S_4 are opened and the fly capacitor C_{fly} is charged by the input voltage to the voltage level, V_{in}. Next, during phase two, as shown in Fig. 9, switches S_2 and S_4 are close, switches S_1 and S_3 are opened. The bottom plate of the fly capacitor C_{fly} is connected to the input voltage V_{in}, and the fly capacitor already reserved the charge in previous phase. So the top plate of the fly capacitor will be pushed to the potential of twice the input voltage, $2V_{in}$. And there is an output capacitor to transfer this generated high voltage, as the presence of the output capacitor, the output voltage will not be 2Vin and will be an ideal output voltage given by

$$V_{out} = \frac{C_{fly}}{C_{fly} + C_{out}} \cdot 2 \cdot V_{in} \qquad (1)$$

When the charge pump has a load resistor, R_L, connected to the output node, a ripple voltage will arise. We can make output capacitor as large as possible to minimize the ripple voltage. But if we enlarge the output capacitor, the output voltage will be reduced. So it is a trade off to choose the proper sizes of output capacitor and the fly capacitor.

1.3 Motivation

LCD panels are going more and more popular. The applications of the LCD panels are widely spread in our daily life. From the small LCD panels on palmtop entertainment machine and cell phone to the large LCD panels on LCD TV or outdoor display screen. Therefore the power supply blocks for LCD panels are more and more important. The needs to integrate the power supply block into the LCD driver circuits are rise in great demands. So we want to reduce the size of the power supply block chip and reduce the use of the external components.

The power sources for LCD panels need different voltage scale to charge and discharge the liquid crystal capacitors. Among the DC-DC power converters, inductive switching converters need external components as inductors and charge pumps need external components as capacitor. Compare these two external components inductors and capacitors, inductors occupy more board area than capacitors. And in the applications, LCDs need a negative voltage to discharge the liquid crystal capacitors. Inductive switching converters can not generate a negative voltage. Therefore, with considering the cost and area, we use charge pumps instead of inductive switching converters. The ripple of the charge pump is reduced by an improved double phase cross-coupled charge pump structure.

This thesis implements a selectable multi output DC-DC converter utilize improved dual phase cross-coupled charge pumps. The input voltage is a high voltage 10V. The circuit can supply 4 different output voltages, 10V, 20V, -10V and 0V. The maximum current load is 50mA.

1.4 Thesis Organization

This thesis presents a new cross-coupled negative charge pump, a cross-coupled charge

pump, a new negative to positive charge pump and their integration. In chapter 2, the reviews of the previous charge pumps and their control scheme will be given. The conventional charge pumps will be discussed in this chapter. And then in chapter 3, the proposed charge pump circuit and their design analysis is described. The switching technique for output the different output voltage is also presents in chapter 3. In Chapter 4 you can find our sub-circuit design and the simulation results. And the conclusion will be given in chapter 5.

Chapter 2

Review of Charge Pumps

2.1 Introduction

Charge pumps are also called switching capacitor DC-DC converters. Because that charge pumps use the switching of capacitors to converter DC levels. We can obtain a higher, lower or an even negative voltage from a charge pump. Charge pumps are finding grown attention in different systems, especially those incorporating nonvolatile memory, such as EEPROM [3] and flash memories, for the programming of the floating-gate devices [4]. The NOR and DINOR Flash memories, require very high positive and negative voltages to do the operations of programming and erasing. If we have only one single power supply voltage, so we need a charge pump to generate such positive and negative voltages on chip. When it comes to NOR Flash memory, the word-line for erasing is set to about -8V and the word-line for programming is set to 12V, respectively. And charge pumps are widely used in low supply voltage devices to generate a higher voltage level to drive the analog circuits, such as switching regulators. And other applications are dynamic random access memory circuits (DRAM) [6] and low dropout voltage regulators [6].

2.1.1 Charge Redistribution

Charge pump circuits use the switching of capacitors to transfer energy and to boost the voltage level. When charge transfers from one capacitor to another capacitor, there is a charge redistribution process. The process will transfer the energy and redistribute the charge on capacitors.

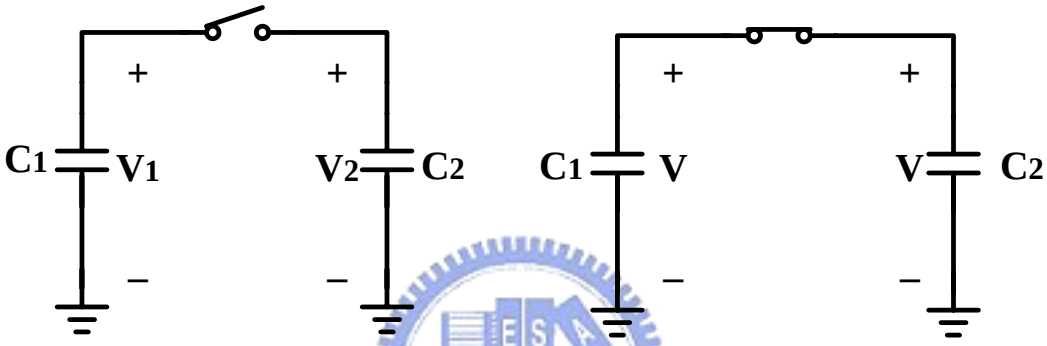


Fig. 10 Charge redistribution

Fig. 10 shows the basic operation of the charge redistribution process. When the switch is opened, the voltage on capacitor C_1 is V_1 and the voltage on capacitor C_2 is V_2. The total charge in the circuit is Q:

$$Q = C_1 \cdot V_1 + C_2 \cdot V_2 \qquad (2)$$

And when it comes to next phase, where the switch is closed. The voltage on both capacitors C_1 and C_2 are the same. And the total charge Q is equal with the previous phase. Then the charge will redistribute on two capacitor and we can get the voltage V with:

$$V = \frac{Q}{C_1 + C_2} \qquad (3)$$

From (2) and (3), we can get the relation between voltages V, V_1 and V_2:

$$V = \frac{C_1}{C_1 + C_2} \cdot V_1 + \frac{C_2}{C_1 + C_2} \cdot V_2 \qquad (4)$$

2.2 Different Charge Pump Circuits

Charge pumps have been proposed for ten years or so. There have been different charge pump types proposed before. In this section, we will describe different types of charge pump. Each one has it own improvement and applications.

2.2.1 Cockcroft-Walton Charge Pump

This type charge pump can be seen as the prototype of charge pumps. The structure was use by John Douglas Cockcroft and Ernest Thomas Sinton Walton to generate voltage potentials of more than 800,000 volts and help them won the Nobel Prize 1951 in Physics. It uses just switches and capacitor to generate higher voltage. And so it was named Cockcroft-Walton charge pump. The new charge pumps proposed nowadays are based on this principle.

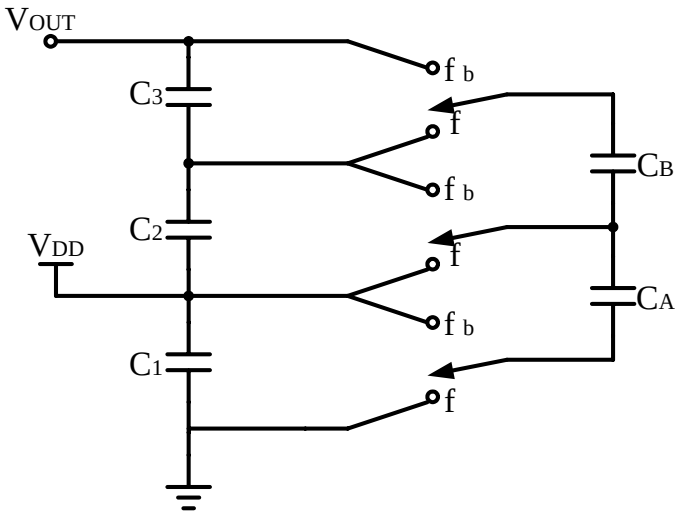


Fig. 11 Cockcroft-Walton charge pump circuit

The Cockcroft-Walton charge pump is shown in Fig. 11. Let's see how it works. When the switches are switched to phase φ, capacitor C_A is connected to the supply voltage V_{DD} and charged to voltage, V_{DD}. And during the next phase, the switches are switched to φ_b, the capacitor C_A will be connected parallel with capacitor C_2. And the charge redistribution will operate and if the C_A and C_2 are in the same size, the voltage o them will be half the supply voltage, $\frac{1}{2}V_{DD}$. And in the next, C_2 will be connected to C_B and redistribute a voltage of $\frac{1}{4}V_{DD}$. The C_A will be charged to V_{DD} again. As the procedure goes, after a few cycles, the C_1, C_2 and C_3 will be charged to the potential V_{DD} and provide a output voltage of $3V_{DD}$.

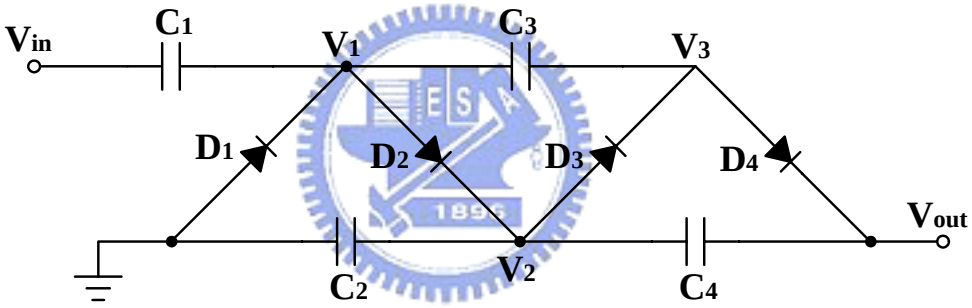


Fig. 12 Cockcroft-Walton charge pump using diode

Fig. 12 shows the circuit of Cockcroft-Walton charge pump using diode to implement. V_{in} is a square wave swing between V_{DD} to ground. During V_{in} is at high, V_1 will be pulled high, D_1 will be turned off and D_2 and D_4 turned on. C_2 will be charged by input voltage through D_2 to voltage, V_{DD}. During next phase, where input voltage is at ground level, there will be charge redistribution occurred between C_1, C_3 and C_2. As C_1 and C_3 is half the size of C_2, the voltage level at V_2 and V_3 pulled to $V_{DD}/2$. After a few cycles, the output voltage, V_{out}, will be twice the input voltage, $2V_{in}$.

2.2.2 Dickson Charge Pump

The Cockcroft and Walton charge pump has its limitations. To overcome the limitations, a new charge pump structure was proposed by John F. Dickson in1976 [7], as shown in Fig. 13. The charge pump then called as “Dickson Charge Pump” because it was proposed by John F. Dickson. Its operation theorem is similar with Cockcroft and Walton charge pump circuit. The diode chain is coupled to the inputs via capacitors in parallel in the Dickson charge pump instead of in series as Cockcroft and Walton charge pump. It needs a pair of clock input clk and clkb with reversion phases to drive the Dickson charge pump. When clk is high and clkb is at low, the diode between the capacitor connected to the clk and the capacitor connected to the clkb will be turned ON and the capacitor connected to clkb will be charged through the diode. Wen clk is at low and clkb at high, the diode mentioned will be turned OFF and the next diode will be turned ON and transfer the charge to the next stage.

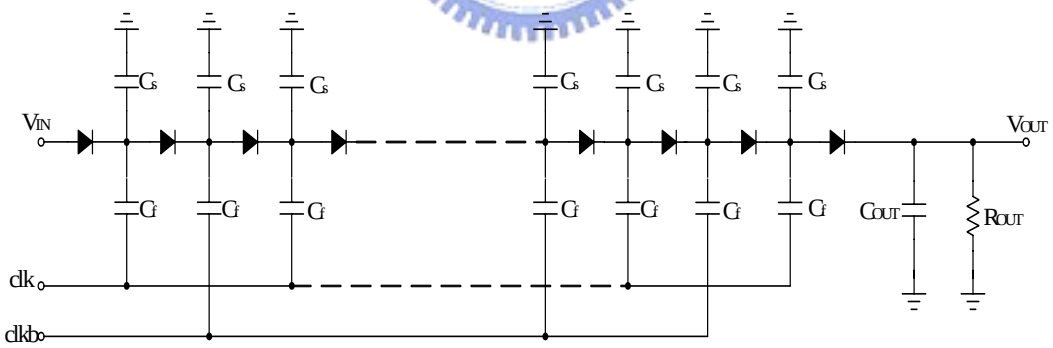


Fig. 13 Dickson charge pump with diode and capacitor implementation

The Dickson charge pump with diode implementation is not sufficient for modern IC industry, it needs too much space. To overcome the size problem, a practical implementation of the Dickson charge pump is proposed as shown in Fig. 14. The diodes used before is replaced by diode-connected MOS transistors. It is more suitable for most of the

semiconductor logic process. As shown in Fig. 14, the diodes are replaced by NMOS transistors, therefore the diode forward voltage, V_D, is replaced by the NMOS threshold voltage, V_t, and the threshold voltage V_t is related to the node voltage of each stage.

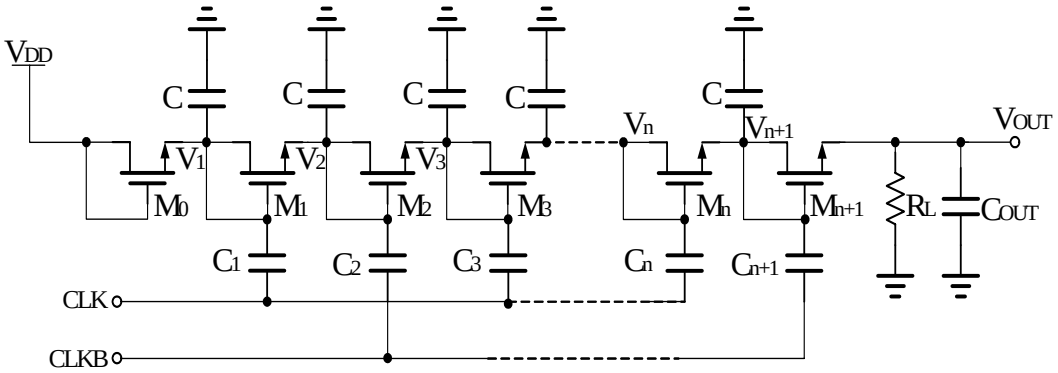


Fig. 14 Dickson charge pump with MOSFET implementation

The operation of the Dickson charge pump circuit is shown in Fig. 14. It is a typical n-stage Dickson charge pump. The input CLK and CLKB are two out-of-phase clocks with amplitude V_{CLK}. These two clocks will increase the potential voltage in capacitors by transferring charges in the capacitor chains through diode-connected MOS transistors. The coupling capacitors will be charged and discharged during each half clock cycle. We first define Cs as the stray capacitance at each node. The coupling capacitances are given as C. The voltage difference between the voltages of the nth stage and (n+1)th nodes is given by:

$$\Delta V = V_{n+1} - V_n = V_{CLK}^{'} + V_t \qquad (5)$$

Where the voltage gain can be express as:

$$V_{CLK}^{'} = \left(\frac{C}{C + Cs} \right) V_{CLK} \qquad (6)$$

For an N stage charge pump, the voltage at the output node is as follow:

$$V_{OUT} = V_{DD} + N\left(V_{CLK}^{'} - V_t\right) - V_t$$
$$= V_{DD} + N\left[\left(\frac{C}{C + C_S}\right)V_{CLK} - V_t\right] - V_t \qquad (7)$$

The equation above is the ideal output voltage when there is no output load and no output current delivered. When the charge pump is connected to an output load, the load current at a clock frequency f , is given by:

$$I_{OUT} = f\left(C + C_S\right)V_L \qquad (8)$$

V_L is the voltage drop per stage for supplying the load current. Therefore, the output voltage will be reduced an N* V_L voltage. So the output voltage with load will be rewrite as follow:

$$V_{OUT} = V_{DD} + N\left[\left(\frac{C}{C + C_S}\right)V_{CLK} - V_t - \frac{I_{OUT}}{\left(C + C_S\right)f}\right] - V_t \qquad (9)$$

Above is the operation and equations for an n-stage Dickson charge pump. Next we are going to see the drawbacks of the Dickson charge pump. The major drawback of the Dickson charge pump is the body effect[8][9]. The threshold voltage of a NMOS transistor is given by:

$$V_t = V_{t0} + \gamma\left(\sqrt{2V_t \ln\frac{N_A}{n_i} + V_{SB}} - \sqrt{2V_t \ln\frac{N_A}{n_i}}\right) \qquad (10)$$

With the increasing stages of the Dickson charge pump, the threshold voltage will be enlarged. It leads to less voltage gain and poor efficiency. The techniques to overcome the drawback have been proposed. Such as floating well MOS transistor [10], the 4 phase charge pump and the boosted pump clock scheme to fully turn on MOS transistor to reduced the body effect [11][12]; a new clocking scheme to control the charge pump [13] and the CTS scheme. In the CTS scheme, an additional transistor is being added to the circuit, and the gate transistor will be controlled by the next stage voltage. We will discuss these solutions in the next section in detail.

2.2.3 4-Phase Charge Pump

The Dickson chare pump mentioned in previous section is suffering the disadvantage and efficiency loss due to the threshold voltage and body effect. The 4-phase charge pump [14][15] is a solution to cancel the effect of the threshold voltage and body effect.

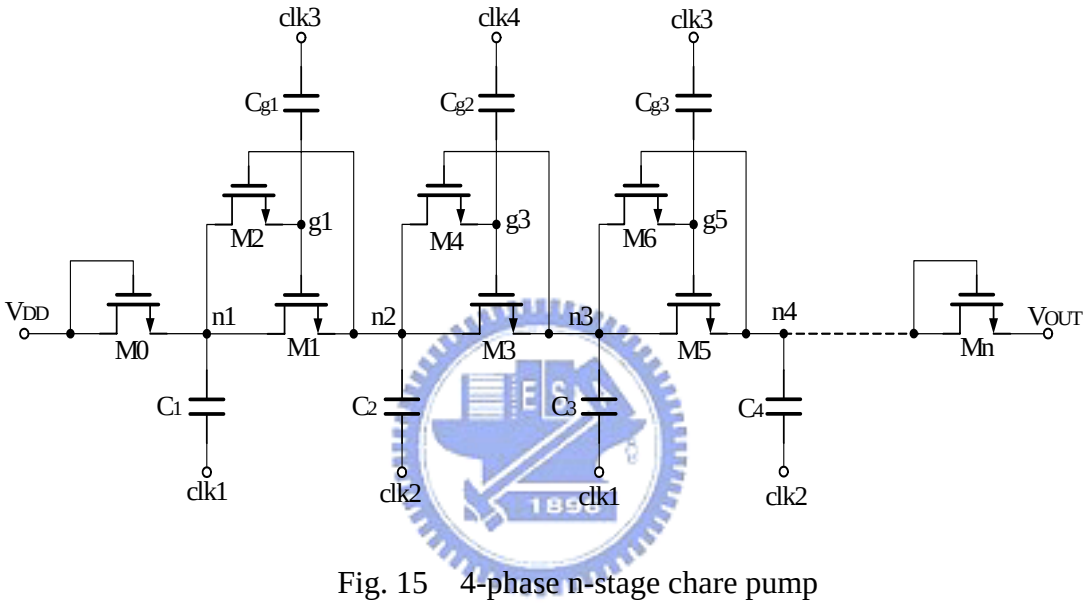


Fig. 15 4-phase n-stage chare pump

The 4-phase n-stage charge pump circuit diagram is shown in Fig. 15. We can see that where the 4-phase charge pump differs from the Dickson charge pump it that the 4-phase charge pump added a MOSFET and a capacitor at each stage. The additional bootstrapping circuits on the gates of NMOS pass transistors are the main contributors to eliminate threshold voltage effect. By added the additional bootstrapping circuits, the gate voltages of NMOS pass transistors are boosted to a higher voltage level than the drain voltage. By doing so, the NMOS pass transistors are fully turned on. Fully turned on NMOS pass transistor allow source and drain terminals to be equalized to the same voltage potential while charge transferring through the pass transistor. The drawback of this design is the extra bootstrapping

circuits needed per pump stage and the extra clocking scheme circuit, it leads to larger chip area. But with the additional circuits, the gain of the 4-phase charge pump can be significant improved. Over the same chip area, the 4-stage charge pump can achieve higher gain and higher charge transfer efficiency.

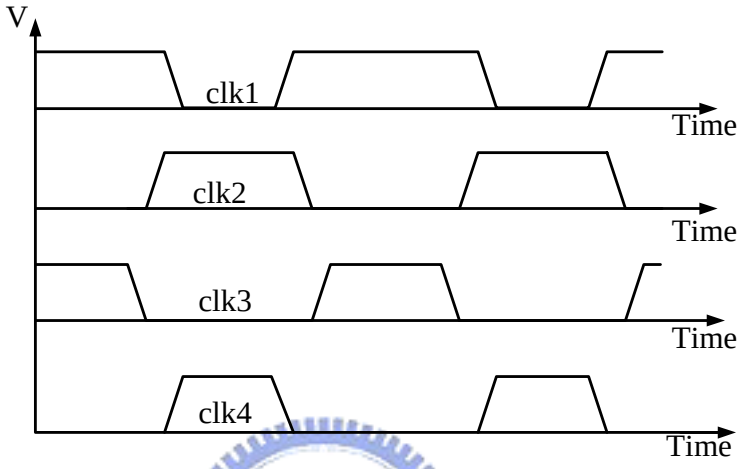


Fig. 16 4-phase chare pump clocking scheme

The operation of the 4-phase charge pump is going to be unfolded. As we can see in the Fig. 15, clk1, clk2, clk3 and clk4 are the non-overlapping clocks. Fig. 16 shows the clocking scheme of these four clocks. In Fig. 15, in the first stage consists of M0 and C_1, when clk1 is low, the diode connected pass transistor M0 is turned on and charges the capacitor C_1 to the voltage level $V_{DD}-V_t$. Once when the voltage of node n1 is lower than $V_{DD}-V_t$, the pass transistor M0 is turned on and charge C_1 to $V_{DD}-V_t$. In the next stage, which is consists of M1, M2, C_1, C_2 and C_{g1}. When clk1 is low, clk2 is high and clk3 is low. Node n2 is pulled high by clk2 through capacitor C_2 and turned on pass transistor M2. Capacitor C_{g1} will be charged and push node g1 to a voltage about $V_{DD}-V_t$. We can see that the gate of pass transistor M1 is not connected direct to the drain as diode connected, it is connected to C_{g1}. And during next phase, clk3 changes from low to high and push the gate of M1 to a higher voltage than its drain terminal. Therefore the pass transistor M1 is fully turned on. The

threshold voltage of M1 is canceled when M1 is fully turned on to conduct. The charge will completely pass through M1 and makes nodes n1 and n2 at the same voltage level. And we analysis the n-stage 4-phase charge pump as we did with Dickson charge pump, the output voltage is given by:

$$V_{OUT} = V_{DD} + n\left[\left(\frac{C}{C+C_S}V_{clk}\right) - \frac{I_{OUT}}{(C+C_S)\,f_{osc}}\right] \qquad (11)$$

The threshold voltage V_t is canceled and the efficiency of the charge pump is improved with the bootstrapping circuit attached.

2.2.4 Static CTS Charge Pump

The charge pump introduced in previous section is a design scheme of canceling threshold voltage V_t effect. In this section we will introduce another design approach of the threshold voltage V_t cancellation scheme. It is a static charge transfer switches charge pump [16][17] as shown in Fig. 17. The difference between circuit in Fig. 17 and the 4-phase charge pump in previous section is that it does not need an extra capacitor an extra clocking scheme. Therefore the chip area can be further reduced and at the same time canceling the threshold voltage effect. The gain of the charge pump with charge transfer switches is being raised.

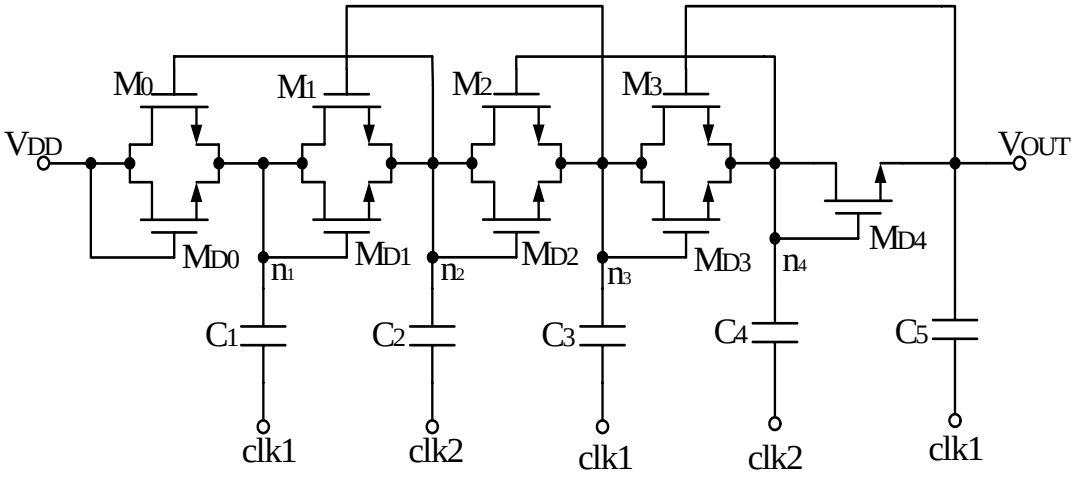


Fig. 17 Static CTS charge pump

As we can see in Fig. 17, every stage of the static charge pump consists of two NMOS transistors and a boosting capacitor. At the first stage, M_{D0} is diode connected as in Dickson charge pump. M_0 is the new circuit added to cancel the threshold voltage of the NMOS. When clk1 is low and clk2 is high, if capacitor C_2 already stored a voltage potential $2V_{DD}$ in the previous phase, node n_2 will be boosted to a higher voltage as $3V_{DD}$ (If the clock high voltage is set to V_{DD}). The node n_2 is connected to the gate of pass transistor M_0, so the gate of M_0 is connected to a higher voltage than its drain voltage and being fully turned on. Therefore the voltages at its drain and source can be equal while conduct. In the first to the fourth stage in the Fig. 17, the effect of the threshold voltage has been canceled. The voltage gain for each stage is given by:

$$V_{GAIN} = \frac{C}{C + C_S} V_{CLK} - \frac{I_{LOAD}}{(C + C_S) f} \qquad (12)$$

Compare with the Dickson charge pump, the voltage gain is increased a threshold voltage V_t. But at the last stage, the voltage gain is the same as Dickson charge pump with threshold voltage V_t. Because the gate of the charge transfer switches is connected to the next stage, therefore the last stage of the CTS charge pump can not have the benefit. So the gain of

an N-stage static CTS charge pump is given below:

$$V_{GAIN} = N\left[\frac{C}{C+C_S}V_{CLK} - \frac{I_{LOAD}}{(C+C_S)\,f}\right] - V_t \qquad (13)$$

There is a critical drawback in this static CTS charge pump. Although the pass transistors can be fully turned on when conduct, is will also be turned on when it is supposed to be turned off. Because when clk1 is high and clk2 is low, pass transistor M_0 is supposed to be turned off, but node n_2 which connected to the gate of M_0 is still higher than the drain terminal. It leads to the reverse leakage current which pass through the pass transistor from node n_1 to V_{DD}.

2.2.5 Dynamic CTS Charge Pump

The above-mentioned static CTS charge pump has a critical drawback, the reverse leakage current. In order to fix the defect, a dynamic CTS charge pump [17] [18] is presented in Fig. 18. Each stage in the dynamic CTS charge pump adds an NMOS transistor and a PMOS transistor to control the gate voltage of the charge transfer transistor. In the first stage, an NMOS M_{N0} transistor and a PMOS M_{P0} transistor are added to control the gate of the charge transfer transistor M_0. The PMOS M_{P0} controls the gate of M_0 connected to a higher voltage potential at node n_2 from the next stage to fully turn on M_0 while transferring the charge to the next stage. And in the next phase where the charge transfer transistor M_0 must be turned off, the NMOS transistor M_{N0} will take the responsibility to control the gate of M_0. The gate of M_0 is connected to a lower voltage potential at node V_{DD} and insure that M_0 is turned off completely to prevent the reverse leakage current. Although the extra NMOS and PMOS will increase the size of the chip, the gain of the charge pump can be raised and the efficiency

can be improved.

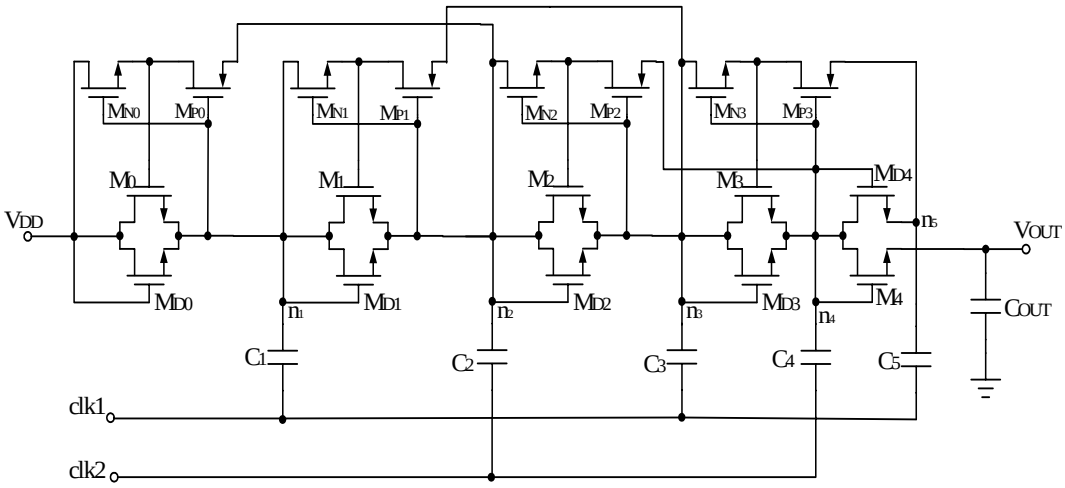


Fig. 18 Dynamic CTS charge pump

Now we consider the final stage of the dynamic CTS charge pump. In Fig. 18, the pass transistor M_3 is turned on by the node n_5 when clk1 is high and n_5 is at the higher voltage potential. But during the previous phase, the gate of M_{D4} is not higher enough to turn on M_{D4} to charge the capacitor C_5 due to the heavy load at the output. The node n_5 will not be higher enough to fully turn on pass transistor M_3. To solve this problem, an ameliorated circuit of the dynamic CTS charge pump is shown in Fig. 19. A bootstrap circuit including two transistors and two capacitors is added to the final stage. This addition circuit is added to ensure that the pass transistor of the final stage can be fully turned on correctly. It uses a pair of cross-coupled NMOS M_{B1} and M_{B2} to charge the capacitors, and ensure that the source of the NMOS M_{B1} is at a higher voltage potential.

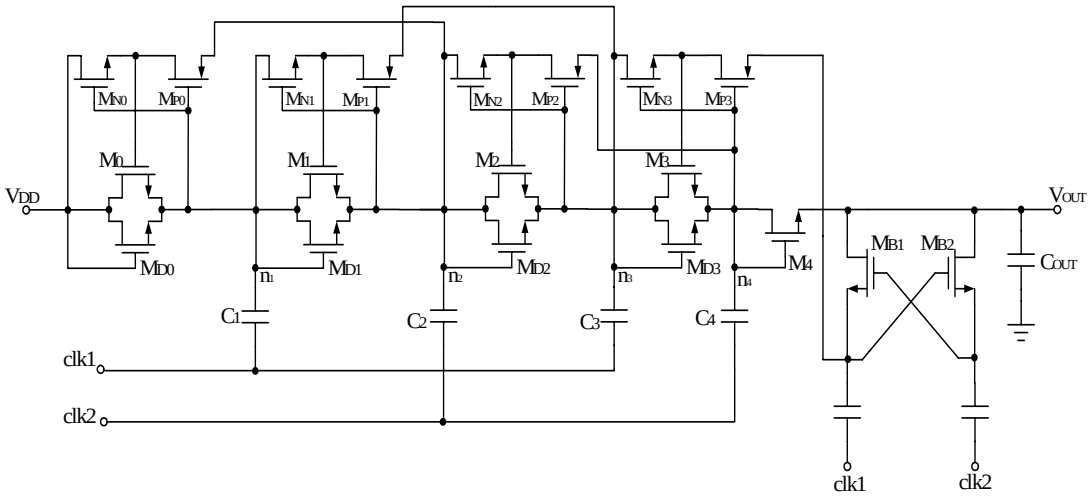


Fig. 19 Dynamic CTS charge pump with an extra level shifter

There are some improvement researches based on above-mentioned circuits. Such as the charge pump implemented by utilizing PMOS transistors [19]. Design and analysis of the output stage to improve the gain and efficiency of the charge pump [20]. Extra branch added to turn on each other [21].

2.2.6 Favrat Charge Pump

The above-mentioned CST charge pumps have improved voltage gain and efficiency. But there is still some deficiencies in the CTS charge pump, such as the gate-oxide reliability for low-voltage operation in CMOS process [21]. Each transistor in the CTS charge pump needs to endure $2V_{DD}$ voltage. When using a low voltage process and $2V_{DD}$ exceeds the process's maximum voltage, the transistors might breakdown and don't function as you want. To solve this problem, a structure called cross-coupled charge pump is proposed.

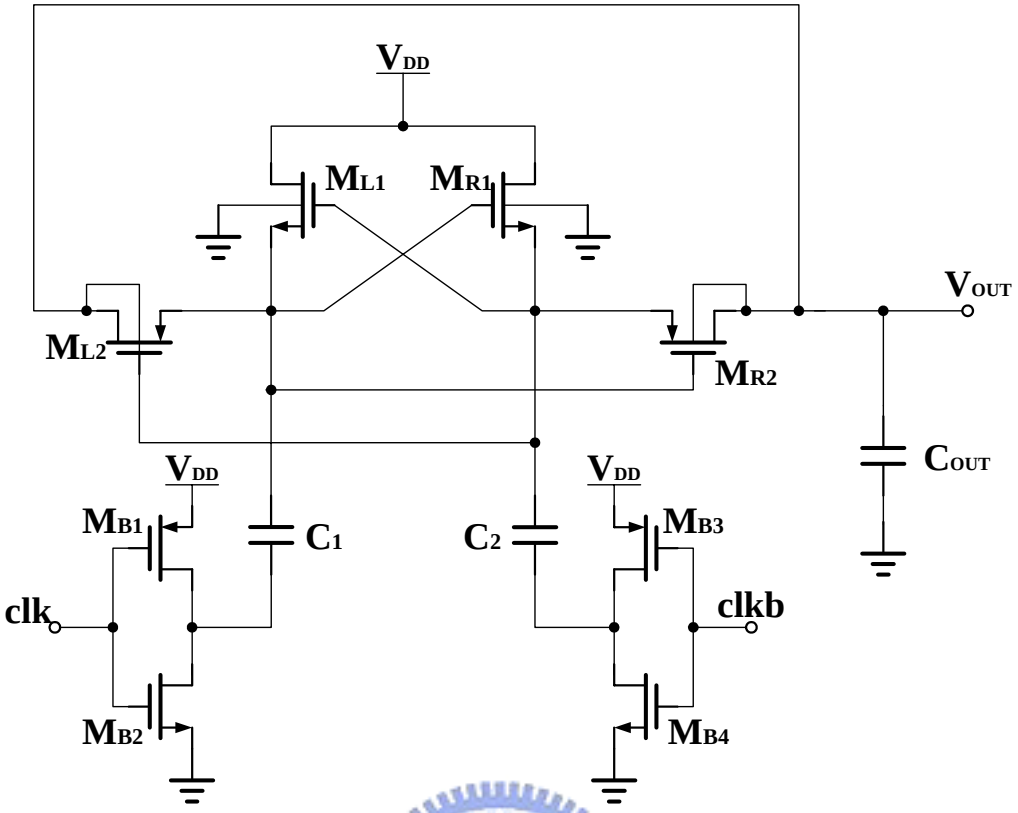


Fig. 20 Cross-coupled charge pump

The cross-coupled charge pump is shown in Fig. 20. The cross-coupled is proposed in the past for DRAM applications [5]. The cross-coupled charge pump uses two different phases charge pumps. The pass transistors of one charge pump are controlled by the other charge pump in the cross-coupled structure. By doing so, the control circuits can be reduced. In the Fig. 20, while the left side charge pump is charging capacitor C_1 through M_{L1} and M_{B2}, the right side charge pump is pumping the output to higher voltage through M_{R2} and M_{B3}. The ripple of the charge pump can be reduced by applying cross-coupled structure. Because of the two charge pumps is connected together and operate at different phase. And there are two transistors sharing the stresses in each stage, therefore each transistor sustains only the voltage ΔV. Hence, it decreases the risks of break through or breakdown in transistors. The output transistors M_{L2} and M_{R2} in the cross-coupled charge pump shown in Fig. 20 run into a problem that the bulk nodes of them are possibly not connected to the highest voltage. To

overcome this problem, a more efficiency cross-coupled charge pump is proposed by Pierre Favrat in 1998 as shown in Fig. 21.

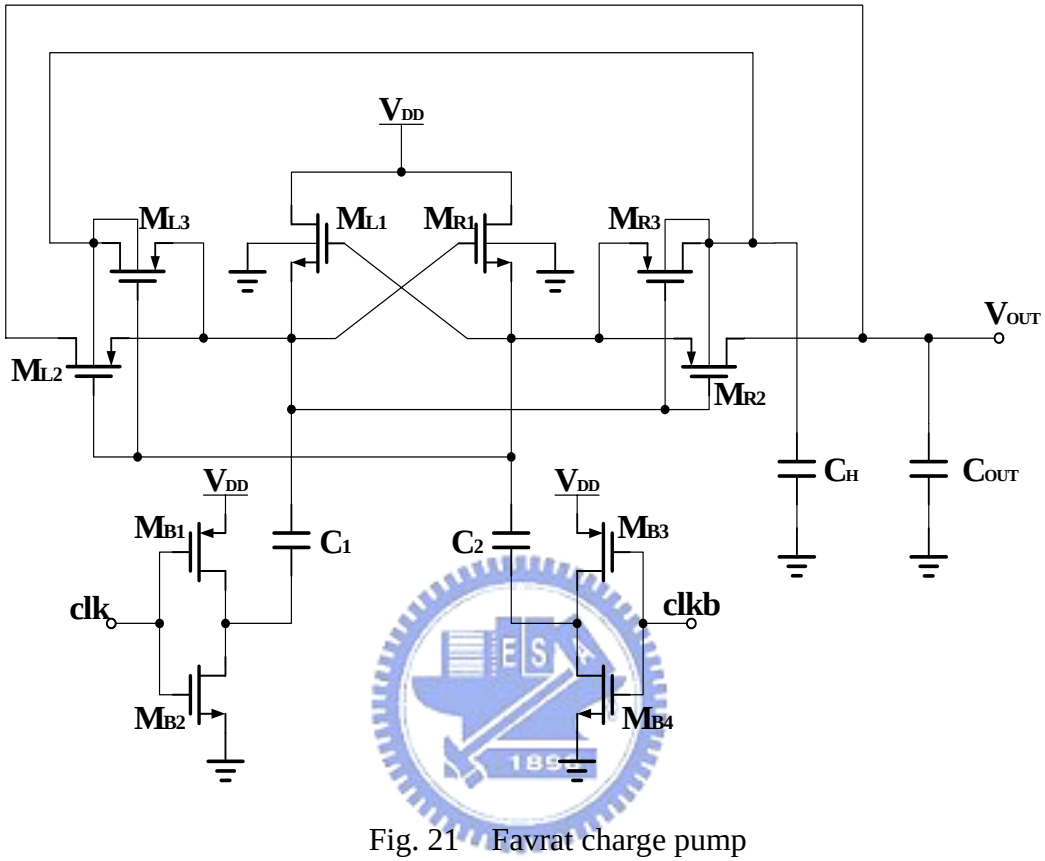


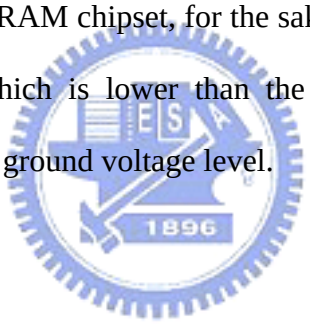
Fig. 21 Favrat charge pump

The Favrat charge pump differs from the conventional cross-coupled charge pump at the output stage. An extra capacitor C_H and extra transistors M_{L3} and M_{R3} are added to the circuit to solve the problem in cross-coupled charge pump. The capacitor C_H will be charged to the highest voltage $2V_{DD}$ through M_{L3} and M_{R3}. The bulk terminals of the PMOS pass transistors are connected to capacitor C_H and push it to the highest voltage $2V_{DD}$. By doing so, the turn on resistors R_{ON} of the PMOS pass transistors will be reduced and the gain and efficiency of the Favrat charge pump can be extended. There are a number of improved charge pumps proposed on the basis of Favarat charge pump. The voltage doubler which is designed to operate at low voltage proposed in [22]. The reduction of the leakage current and conduction

loss in the cross-coupled charge pump and improves the power efficiency [23] [24]. The structure proposed in [25] to reduce the chip area. The body effect eliminating technique utilizing triple-well process [26].

2.3 Negative Charge Pump

The charge pumps mentioned above are all positive charge pumps. The positive charge pumps boost the input voltage to a higher voltage scale which exceeds the source voltage from power supply. If the voltage can be boosted to a higher level, the voltage can be lowered to a lower level too. In modern IC design, the negative voltage which is lower than the ground level is needed. Such as on a DRAM chipset, for the sake of reducing the background leakage current, a negative voltage which is lower than the ground level is utilized to bias the p-substrate instead utilizing the ground voltage level.



2.3.1 Conventional Negative Charge Pump

A conventional negative charge pump is shown in Fig. 22. It is a k-stage 2-phase negative charge pump [27]-[29]. Compare with the positive Dickson charge pump as shown in Fig. 14, the NMOS in the positive Dickson charge pump has been changed to the PMOS in the negative charge pump. The NWELL of the PMOS in the negative charge pump is connected to the most positive voltage per stage. And the source voltage of the first stage in the negative charge pump is connected to ground instead of V_{DD} in the positive charge pump.

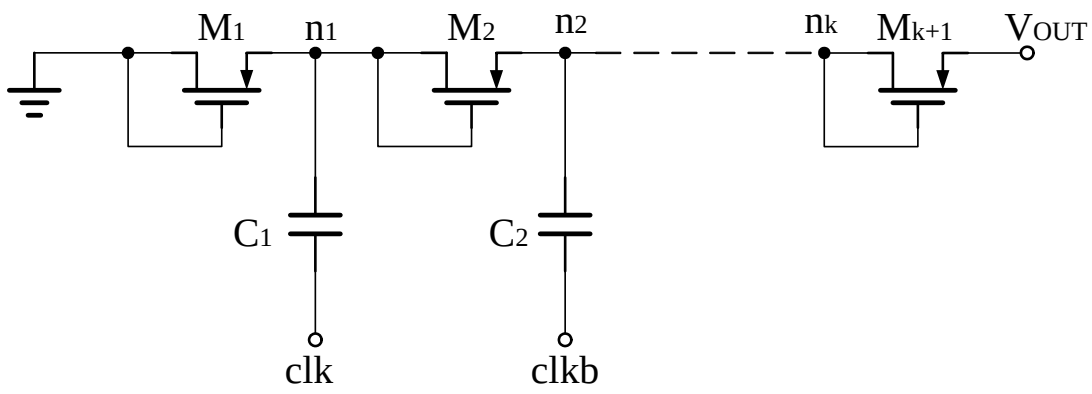


Fig. 22 Conventional k-stage 2-phase negative charge pump

In Fig. 22, the PMOS pass transistors are connected in diode fashion. The operations of the negative charge pump will be given in this paragraph. At the beginning of the pump, the input clock clk is at high as a voltage and the diode connected pass transistor M_1 is turned on and the positive charge from the pump output node n_1 of the first stage will be removed and transfers it to the ground node. And in the next phase, clk is pulled low. Since charge is carried away from node n_1 in the previous phase, the voltage level stored in the capacitor C_1 will make the output node n_1 voltage a negative level. At the same time, the clock clkb is high and turns on the pass transistor M_2 and the positive charge on n_2 will be removed and transfer to n_1. And the next clock phase, clkb is pulled low and node n_2 is boosted to a lower negative voltage. The current direction is going through from output node to the input node just opposite of the positive charge pump. The output voltage of the k-stage negative charge pump as shown in Fig. 22 is give by Equation 14.

$$V_{OUT} = -k\left[\left(\frac{C}{C+C_S}\right)V_{clk} - \left|V_{tp}\right| - \frac{I_{OUT}}{\left(C+C_S\right)}\right] + V_{tp} \qquad (14)$$

2.3.2 Negative Charge Pump Utilize Triple

Well Technology

The above-mentioned negative charge pump has the threshold voltage problem [30]. As shown in the Equation 14, the bigger the threshold voltage is, the lower the output voltage can achieve. Therefore if we want to increase the output voltage and the efficiency of the negative charge pump, the threshold voltage of the pass transistors must be reduced. The above-mentioned conventional negative charge pump utilize PMOS as its pass transistor. The bulk terminal of the PMOS transistor in a standard CMOS process must be connected to the highest voltage of the chip. And when it comes to a negative charge pump, the threshold voltage is due to the voltage V_{SB} across source and bulk. The source voltage of the transistor in a negative charge pump might be a negative voltage lower than the ground level, and the bulk of PMOS transistor is connected to the highest voltage. It makes V_{SB} high and causes the threshold voltage to be large. The large threshold voltage leads to the decrease of the output voltage. So if we want to increase the voltage gain of the negative charge pump, wee need to decrease the threshold voltage V_t. To decrease the threshold voltage, it can be done by reducing the source to bulk voltage V_{SB}.

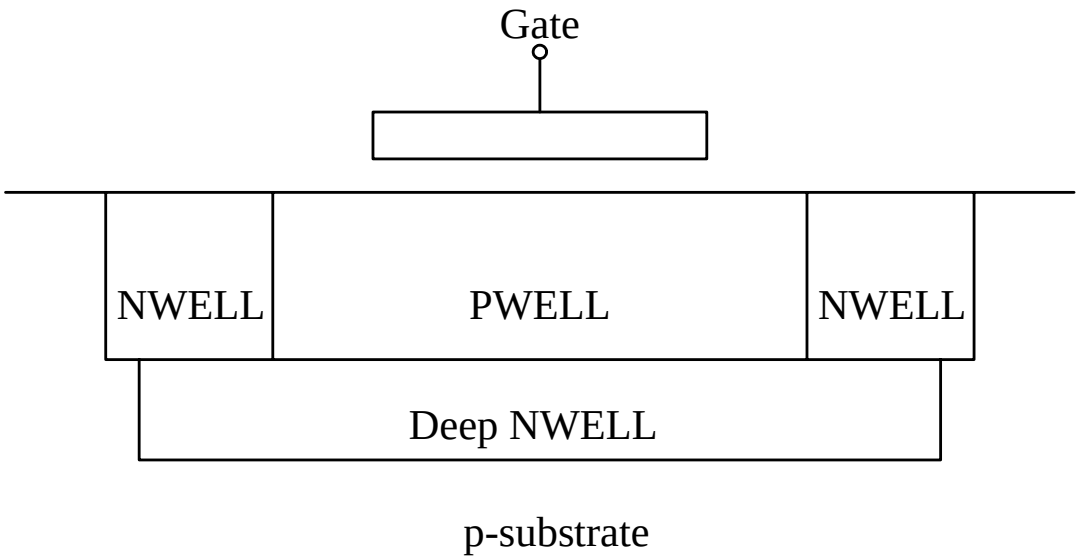


Fig. 23 Deep NWELL n-type transistor profile

The source to bulk voltage V_{SB} must be minimized to reduce the threshold voltage. The NWELL of the PMOS transistor needs to be connected to a higher voltage such as V_{clk} of the input voltage level. But in a negative charge pump, because of the negative output voltage, an approach to reduce V_{SB} is to switch NWELL potential down to the ground level. By doing so, the threshold voltage V_t can be reduced due to the reduction of the source to bulk voltage V_{SB}. Though this approach can reduce V_{SB}, but when the stage increases and the output voltage goes to a more negative voltage, the V_{SB} is still too large. Therefore if we want to further reduce V_{SB}, we need the help from the process technology. A deep NWELL NMOS transistor is introduced in the triple well process technology as shown in Fig. 23. In a normal CMOS process, the NMOS is processed directly on top of p-substrate. If the source of a normal NMOS is boosted to a negative voltage potential, latch-up issues could arise due to the junction forward biasing. A deep NWELL NMOS adds an extra well called deep NWELL as shown in Fig. 23. It will isolate a PWELL from p-substrate. If we connect p-substrate and the extra PWELL together, it is just like a normal NMOS. But with the additional PWELL, the bulk of NMOS can be connected to negative voltage potential. Since the source and bulk of

NMOS can both be connected to negative voltage, source to bulk voltage V_{SB} can be greatly reduced. Therefore the threshold voltage V_t is reduced.

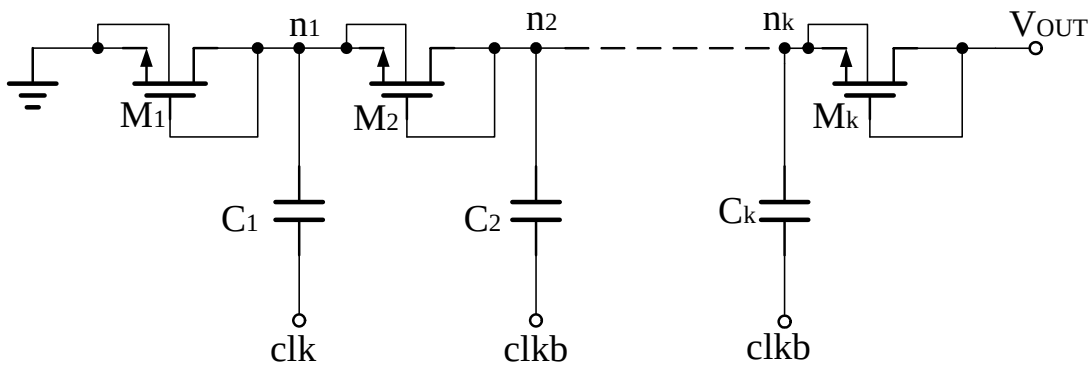


Fig. 24 k-stage 2-phase negative charge pump with a deep NWELL transistor

With the help of the triple well process technology, a negative charge pump utilizing deep NWELL NMOS transistors is shown in Fig. 24. The bulk and source is butted together to eliminate the body effect. The operation of the negative charge pump in Fig. 24 is the same as above-mentioned conventional negative charge pump.

Chapter 3

The Description and Analysis of the Proposed Circuit

3.1 Selectable Multi-Output DC-DC Converters

In some applications, it needs different voltage sources to supply a single node of the chip. Such as the power sources for LCD panels, they need different voltage scale to charge and discharge the liquid crystal capacitors. When we have only one supply voltage scale, we need different DC-DC power converters with different output voltage scales. Among the DC-DC power converters, inductive switching converters need external components as inductors and charge pumps need external components as capacitor. The external component capacitors occupy smaller chip area than the inductors. The amount of external components will increase while we have different DC-DC converters in our chip. Therefore, if we want to reduce the chip area, the external component size must be minimized. The conventional selectable multi-output DC-DC converter utilizes inductive switching converters which occupies larger chip area. The proposed selectable multi-output DC-DC converter utilizes charge pumps as its power converters will reduced the chip area and cost.

3.1.1 Conventional Structure

As mentioned above, the conventional structure of selectable multi-output DC-DC converter uses inductive switching converters as its DC-DC converters. Suppose that the output node needs four voltages, we need four inductive switching converters to supply the different voltage. At least four inductors are needed and they will occupy a large chip area.

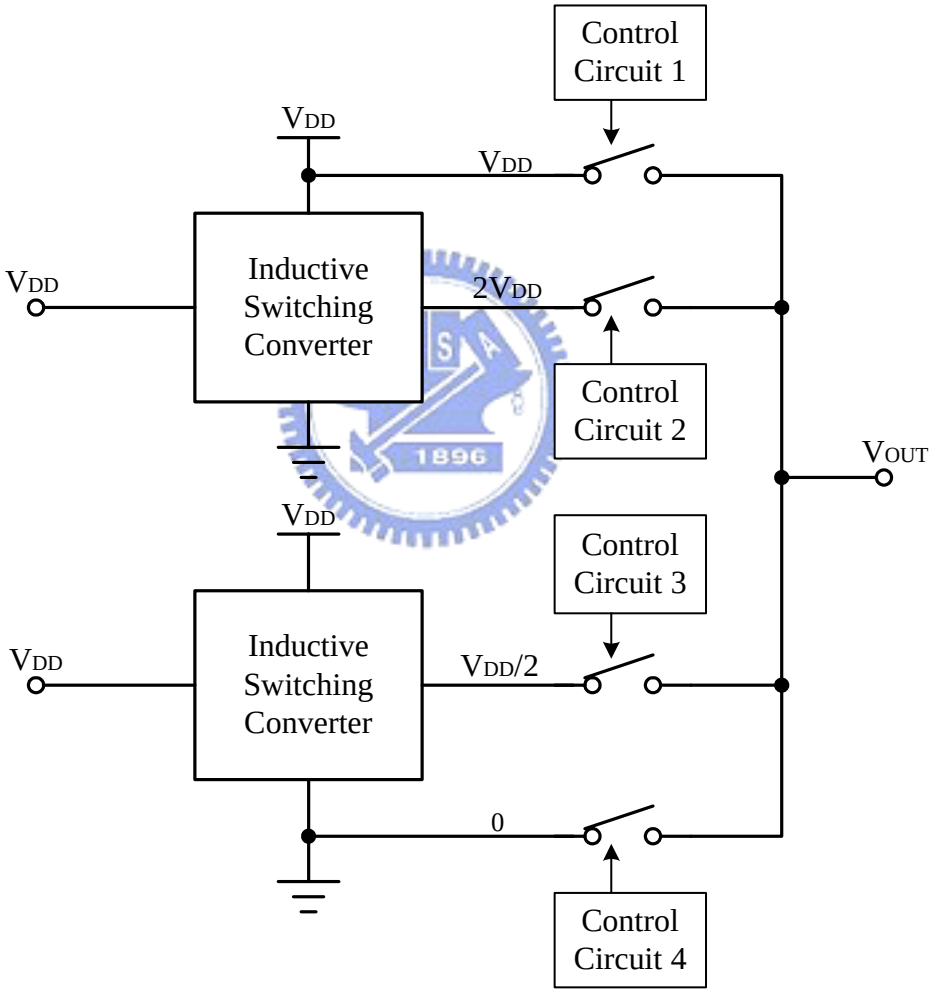


Fig. 25 Conventional structure of a selectable multi-output converter

As shown in Fig. 25, it is the structure of a selectable multi-output converter. It uses inductive switching converters as its DC-DC power converters. In Fig. 25, there are four

voltages for output switching, V_{DD}, $2V_{DD}$, $V_{DD}/2$ and the ground. The voltage potentials V_{DD} and ground are directly supplied by the input power supply, the other two voltage potentials $2V_{DD}$ and $V_{DD}/2$ need two inductive switching converters to generate. The structure can be extended if the output needs more different voltage potentials.

3.1.2 Proposed Structure

The above-mentioned conventional selectable multi-output DC-DC converter which utilizes inductive switching DC-DC converters demands large chip area. The control circuits, feedback loop circuits and compensation circuits of the inductive switching DC-DC converters also enlarge the size of the conventional structure. The applications that need a negative voltage potential lower than the ground level mentioned before can't use the conventional structure. Because the inductive switching DC-DC converter can only generate voltages higher or lower than the input voltage, negative voltage lower than the ground is unavailable. Therefore, we propose a new structure of the selectable multi-output DC-DC converter. The proposed structure is shown in Fig. 26. As you can see in Fig. 26, the DC-DC power converters of the proposed selectable multi-output DC-DC converter is replaced by charge pumps. Charge pumps need no feedback and compensation circuits in the applications that do not need accurate output voltage such as LCD panel gate drivers, charging and discharging of the liquid crystal capacitors and flash memories. The replacement of charge pump can reduce the chip area and the cost. And one of the great contribution is that charge pump can generate negative voltage potential which is lower than the ground level.

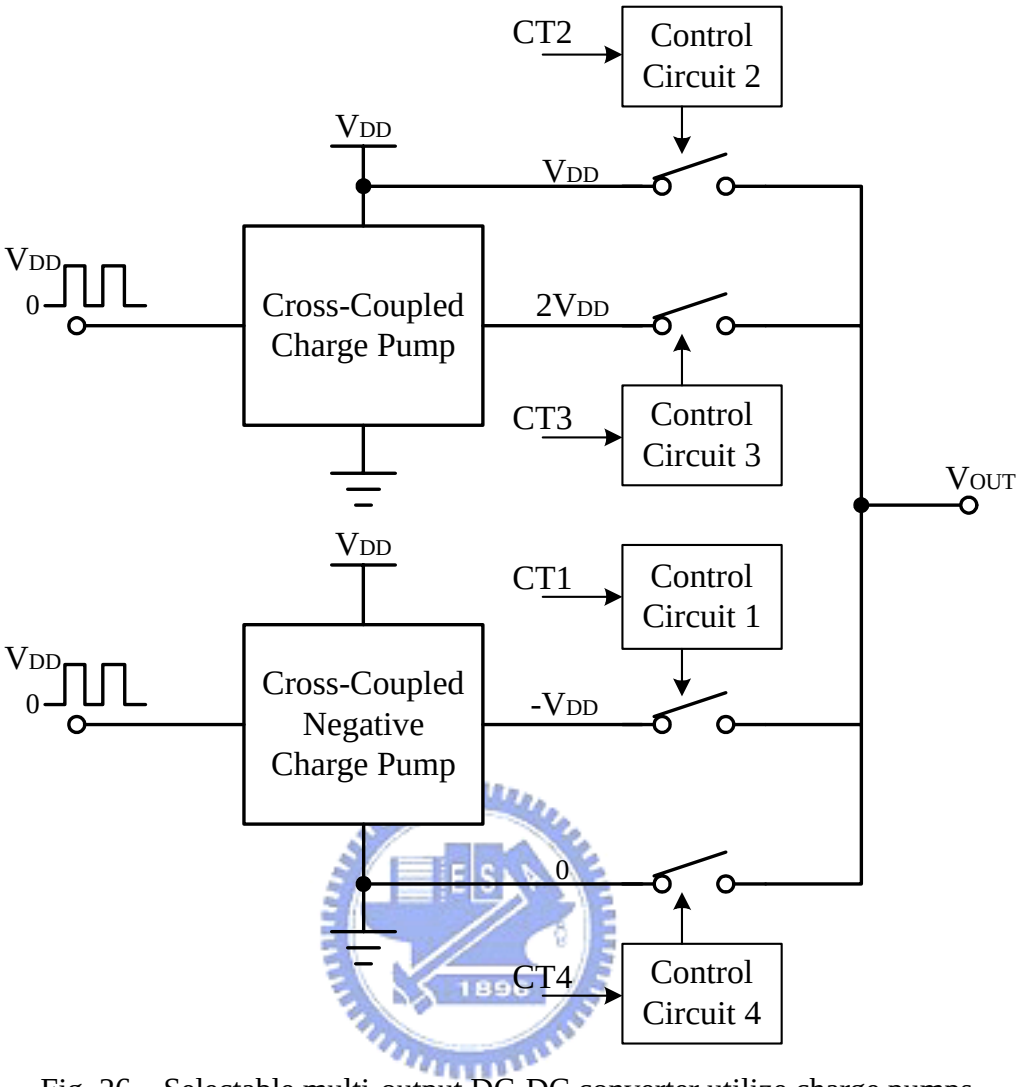


Fig. 26 Selectable multi-output DC-DC converter utilize charge pumps

The proposed structure as shown in Fig. 26 has four voltages $2V_{DD}$, V_{DD}, $-V_{DD}$ and ground for selection. The voltages V_{DD} and ground are directly supplied by the input power source. The voltage $2V_{DD}$ is generated by an improved cross-coupled charge pump which will be introduced in the next section. And the negative voltage $-V_{DD}$ is generated by a cross-coupled negative charge pump which will be discussed in detail in the following sections. As you can see from Fig. 26, there are four switches separately controlled by four control circuits to select the output voltage. There is only one voltage delivered to the output at one time. You can select the voltage arbitrarily as you want to decide which voltage is delivered to the output at the mean time.

3.2 Improved Charge Pump

In this section the cross-coupled charge pump is discussed in detail. The shoot-though current loss may occur in a cross-coupled structure. The shoot-though current will lead to the reduction of voltage gain and efficiency. The shoot-though current here is the current flow from output to input. For a charge pump which boosts the input voltage to a higher level, the current should flow from input supply to output node. Therefore the shoot-though current is a reversion loss which we do not want it to appear. An improve structure of the cross-coupled charge pump will be proposed to reduce the shoot-though current loss. The more the shoot-though current loss can be reduced, the higher gain and efficiency can be achieved.

3.2.1 Shoot-Though Current Loss

In the cross-coupled charge pump such as the Favrat charge pump, there is a loss called shoot-though current loss. It is due to the control of the pass transistors during switching. As shown in Fig. 27, the voltage transition at the node V_1 and V_2 can not be controlled during switching. The shoot-though currents will occur on pass transistors M_{L1}, M_{L2}, M_{R1} and M_{R2} which are controlled by node V_1 and V_2 during switching. The currents I_1 and I_2 are the shoot-through currents which arise in pass transistors M_{L1} and M_{R1}. And the currents I_3 and I_4 are the shoot-through currents which arise in pass transistors M_{L2} and M_{R2}. Because the cross-coupled charge pump is a symmetric structure, therefore the shoot-through current is generated each half cycle in similar way.

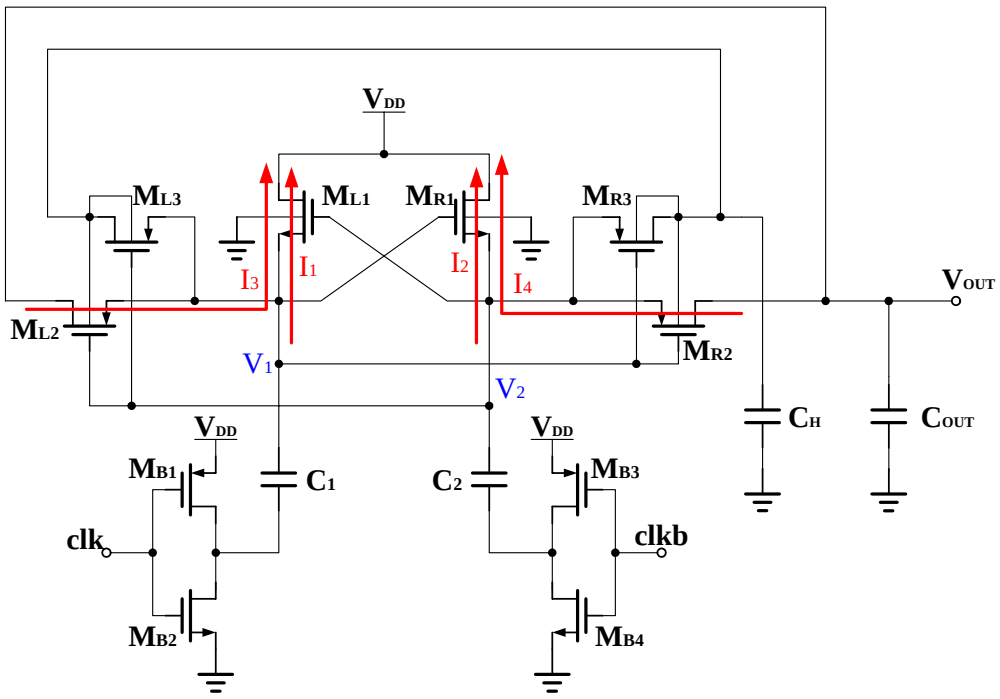


Fig. 27 Shoot-though current generation mechanism in Favrat charge pump

Fig. 27 shows the shoot-through current generation mechanism. The voltages V_1 and V_2 produce shoot-through current in four different ways. Voltages V_1 and V_2 are the control of the pass transistors M_{L1}, M_{L2}, M_{R1} and M_{R2} and they are switched between V_{DD} and $2V_{DD}$. Let's see the generation of the soot-through current I_1, it is due to the leakage from pass transistor M_{L1}. During the switching where V_1 increased from V_{DD} to $2V_{DD}$ and V_2 decreased from $2V_{DD}$ to V_{DD}, at the transition in the initial phase of clock signal where

$$V_2 - V_1 \geq V_{tn} \quad and \quad V_1 > V_{DD} \qquad (14)$$

V_{tn} is the threshold voltage of pass transistors M_{L1} and M_{R1}. Under this condition, the first shoot-through current occurs and flow from node 1 through M_{L1} to the input power supply V_{DD}. The second shoot-through current is generated in a similar way as the symmetry of the cross-coupled structure. Shoot-through current I_2 flows from node 2 through M_{R1} to the input power supply voltage when

$$V_1 - V_2 \geq V_{tn} \quad and \quad V_1 > V_{DD} \qquad (15)$$

AS shown in Fig. 27, the third and fourth shoot-through currents leak from output node the input power supply. This occurs when pass transistor pairs M_{L1} and M_{L2}, M_{R1} and M_{R2} are simultaneously conducted, respectively.

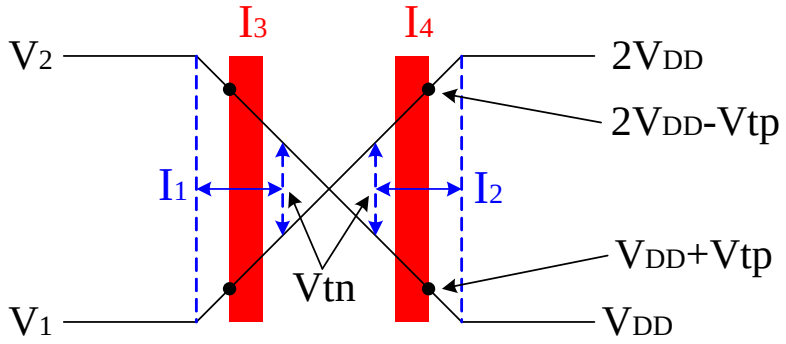


Fig. 28 The occurrence of the shoot-though current during switching

As shown in Fig. 28, The duration of the shoot-through currents I_1 and I_2 are the blue regions. And the red regions are the duration that shoot-through currents I_3 and I_4 occur. I_3 occurs when M_{L1} and M_{L2} are simultaneously conducted. M_{L2} is turned on when

$$V_2 \le 2V_{DD} - \left|V_{tp}\right| \quad and \quad V_{DD} > 2\left|V_{tp}\right| \qquad (16)$$

Based on equation (14), the minimum input power supply voltage V_{DD} to turned on transistor M_{L1} during the turning on of the transistor M_{L2} is given by

$$V_{DD} \ge \max\left(2\left|V_{tp}\right|, 2\left|V_{tp}\right| + V_{tn}\right) = 2\left|V_{tp}\right| + V_{tn} \qquad (17)$$

The red regions where simultaneous conduction occurs in Fig. 28 increases with the input supply voltage V_{DD}. Therefore, the higher the input supply voltage is, the larger the region of simultaneous conduction is. It will lead to larger power loss and poor power efficiency.

3.2.2 Proposed Charge Pump with Loss Reduction Technique

From the discussion in previous section, we want to develop an efficient structure of cross-coupled charge pump to reduce the shoot-through current during switching and the reversion loss. The proposed cross-coupled charge pump circuit is shown in Fig. 29.

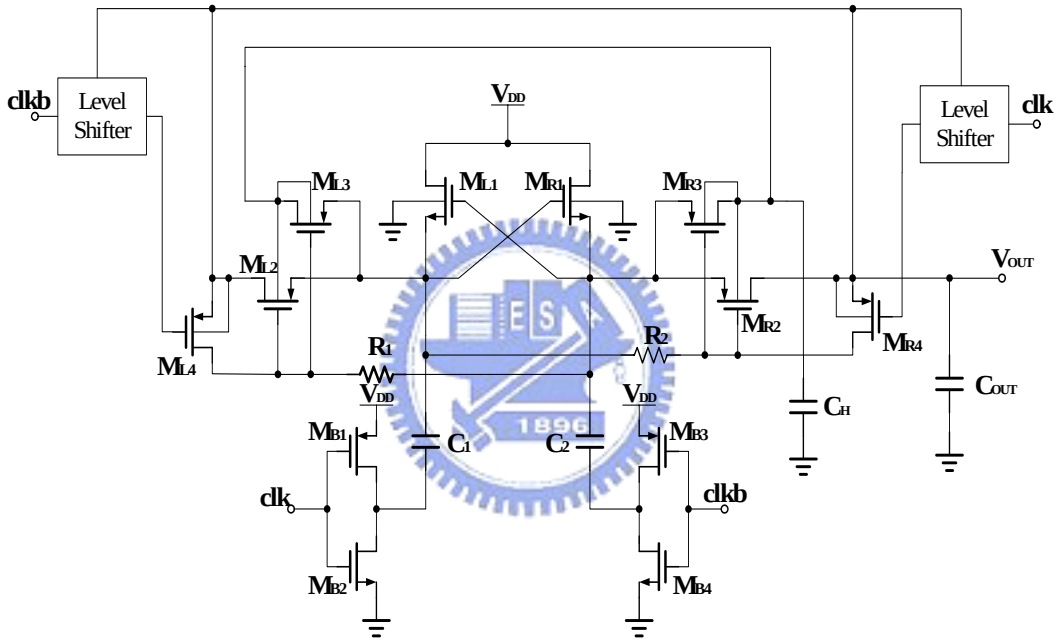


Fig. 29 Proposed cross-coupled charge pump with loss reduction technique

As shown in Fig. 29**,** in the proposed structure, two transistors (M_{L4}, M_{R4}) and two resistors (R_1, R_2) are added into the circuit. Transistors M_{L4} and M_{R4} are controlled by an extra level shifter to ensure the proper turning on and off. The principle of operation of the proposed cross-coupled charge pump is going to be unfolded in this paragraph. In the proposed cross-coupled charge pump, M_{L4} is turned on when M_{L2} is turned off and M_{R4} is turned on when M_{R2} is turned off. The transistors M_{L4} and M_{R4} are used to increase the transition speed of the control signal V_1 and V_2 turning from V_{DD} to $2V_{DD}$. It provides an

additional current path to charge the gate terminals of the power transistors M_{L2} and M_{R2} and makes them turning off much faster. The resistors R_1 and R_2 are added to slower the transition speed of the gate if power transistor M_{L2} and M_{R2}. It makes power transistors to turn on much slower due to the additional RC delay.

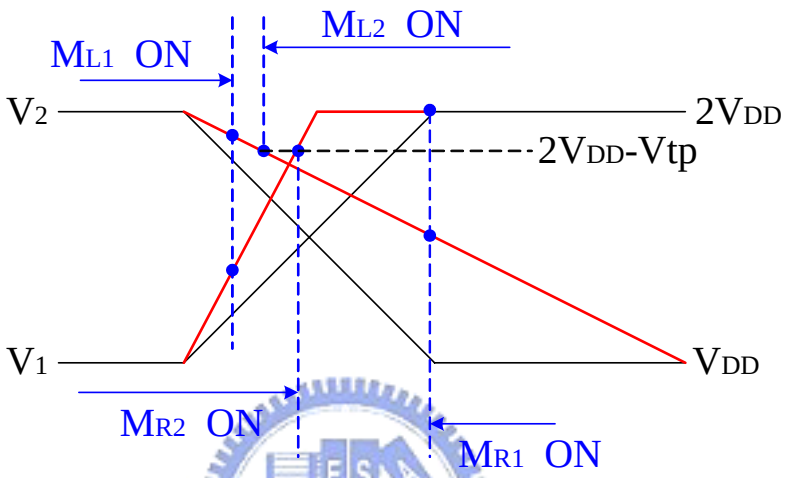


Fig. 30 Simultaneous transitions of control voltages in the proposed structure

The simultaneous transitions of the control clocking signal V1 and V2 is shown in Fig. 30. And the control clocking signal V_1 and V_2 of the proposed cross-coupled charge pump is the blue line in Fig. 30. The gate of M_{L2} is connected to V_2 through R_1. While V2 is changed form $2V_{DD}$ to V_{DD} slower, M_{L2} will be turned on slower. Therefore the M_{L1} on will not overlap to the on time of M_{L2}. This creates a break-before-make mechanism which will prevent the two transistors from simultaneous conduction. The gate of M_{R2} is connected to V_1 through R_2. During the switching of V_1 from V_{DD} to 2 V_{DD}, because the charging assistant current created by M_{R4} will fasten the speed from low to high, power transistor M_{R2} will be turned off quickly. It also creates a break-before-make and prevents M_{R1} and M_{R2} from simultaneous conduction. As mentioned above, the shoot-through current can be reduced. The size value design consideration of the additional transistors and resistors must follow the

following guidelines. The resistors need to be design large enough to let the slower transition from $2V_{DD}$ to V_{DD} of V_2 can make sure that M_{L1} is turned on after M_{L2} is turned off. And the size of the additional transistors are big enough to let the faster transition from V_{DD} to $2V_{DD}$ of V_1 can make sure that M_{R2} is turned off before M_{R1} is turned on.

3.3 Negative Charge Pumps

In this section, we are going to present the negative charge pumps with different structure. As mentioned above, the negative charge pumps presented later all use NMOS transistors as their pass transistors. Therefore we need the help of triple well process technique. In the next sections, we will introduce negative charge pumps utilizing NMOS transistors. Then the proposed cross-coupled negative charge pump will be presented. The negative charge pump structures for symmetric and asymmetric NMOS will be introduced next. The reversion loss is occurred in cross-coupled structure. The reversion loss reduction technique will be given in the end of this section. The considerations and discussion of multi-stage negative charge pump will also be introduced.

3.3.1 Negative Charge Pump Utilize NMOS Transistors

As mentioned in the previous section, the negative charge pump which utilizes NMOS as its switches has higher voltage gain and better efficiency. The reason is that the bulk terminal of PMOS must be connected to the highest voltage of the circuit to prevent P-N junction from forward biasing. When it comes to a negative voltage, the positive bulk biasing will leads to very large threshold voltage V_t. And it will reduce the efficiency of the negative charge pump

greatly. By contraries, the bulk terminal of NMOS can be connected to negative voltage in triple well process [31]. Therefore the threshold voltage can be reduced and the efficiency of the negative charge pumps can be improved.

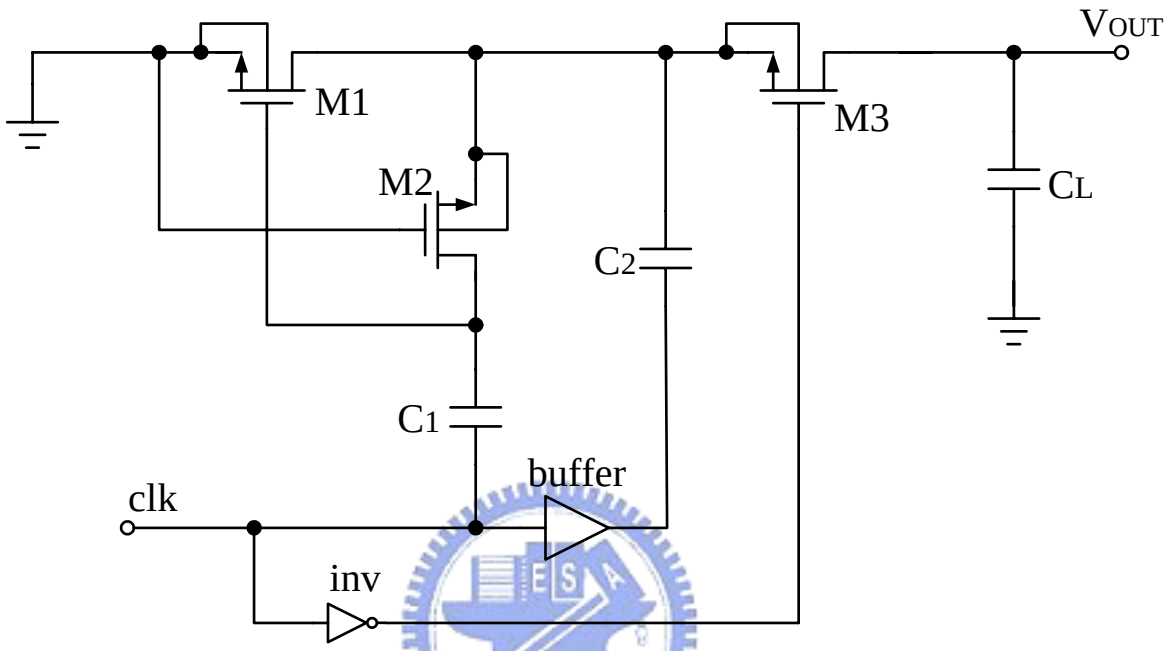


Fig. 31 Negative charge pump circuit utilize NMOS

Fig. 31 is the architecture of a negative charge pump using NMOS as its switches. The circuit is driven by a square wave clk. First, when clk is high (V_{DD}), C_1 and C_2 has no charge on them, the gate and source of transistor M1 will be pulled high and turn on M1. Capacitor C_2 will be charged through M1 and buffer, the source of M1 will be pulled to GND. And C_2 will store a voltage level V_{DD} on it. During next step, when clk is low (GND), the source of M1 will be pulled to a negative voltage $-V_{DD}$ due to the charge stored in capacitor C_2. M2 is turned on and redistribute the charge on C_1 and C_2. C_1 is always set small to store a voltage on it to control the gate of M1.At the mean time, M3 is turned on and the output capacitor C_L will be charged through M3 and pull output voltage V_{OUT} to the negative voltage level $-V_{DD}$.

3.3.2 Cross-Coupled Negative Charge pump

Among different types of charge pumps, the cross-coupled charge pump can reduce the output ripple and deliver more power to the load [24][32][33]. The cross-coupled charge pumps operate at twice the switching frequency of the conventional types. Such that the load capacitor can be halved and the output ripple can be reduced.

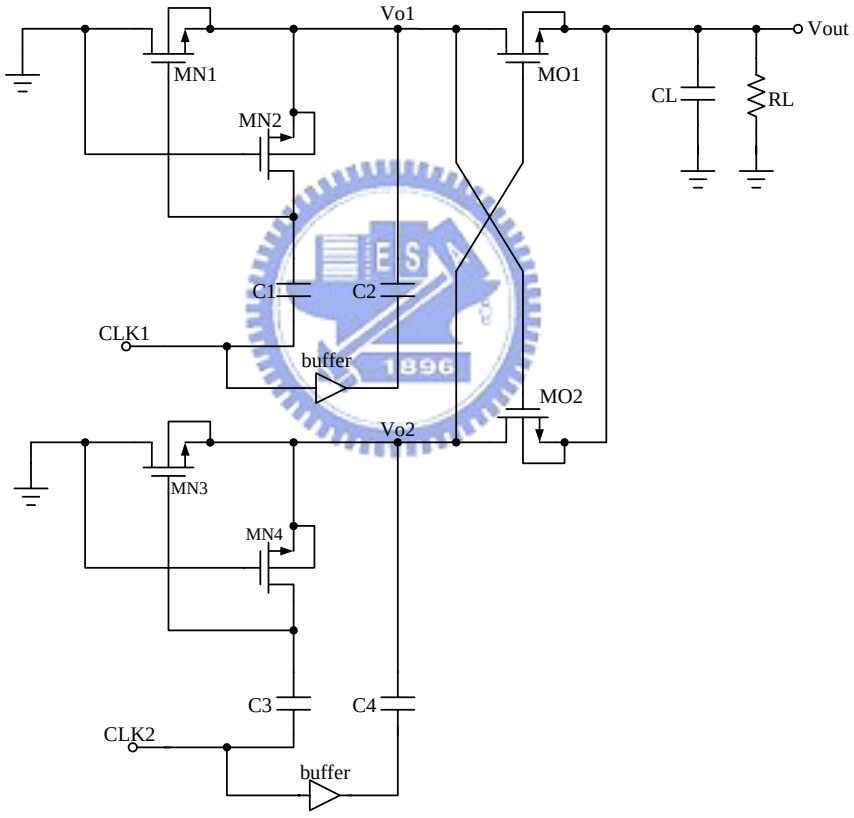


Fig. 32 Cross-coupled negative charge pump circuit

Fig. 32 shows the circuit architecture of the proposed cross-coupled negative charge pump. There is a pair of cross-coupled NMOS transistors (MO1 and MO2) acting as charge transfer devices to provide a negative output voltage. And there are two flying capacitors (C2 and C4) to store the energy through transistors (MN1 and MN3) and buffers to pull nodes (Vo1 and Vo2) to negative voltages. Capacitors C1 and C3 are used to control the charge

transfer transistors MN1 and MN2.

3.3.3 Cross-Coupled Negative Charge Pump with Bulk Biasing

The above-mentioned cross-coupled negative charge pump shown in Fig. 32 utilizes a transistor MN2 and a capacitor C1 to control the gate of the power transistor MN1. The transistor MN2 and the capacitor can be curtailed to reduce the chip area because the gate of MN1 can be controlled directly by node Vo1.

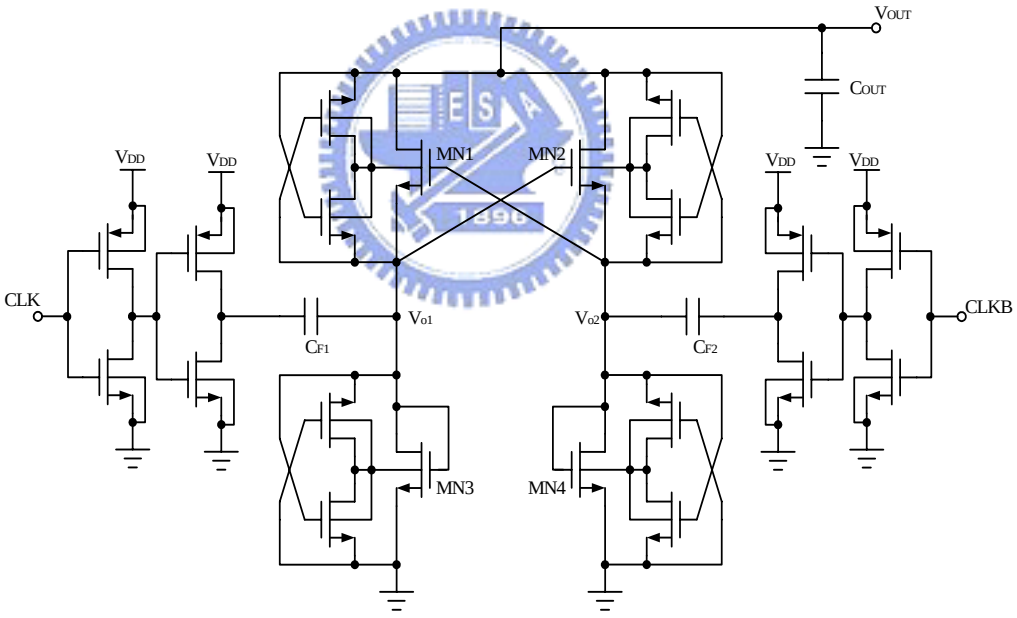


Fig. 33 Negative charge pump using NMOS with isolated bulk and bulk bias

The simplified cross-coupled negative charge pump is shown in Fig. 33. As we can see, the power transistors are all NMOS with bulk biasing circuit. The transistor pair connected on the power transistor's bulk terminal is the bulk biasing circuit. It will switch the bulk of the power transistors to the lower voltage of its drain or source. It can only be done in a triple

well process with symmetric NMOS in it. Only that the bulk of the high voltage transistor NMOS can be separated from source. By switching the bulk of the NMOS transistor to the lowest voltage of the transistor, the threshold voltage can be reduced and the switching noise is also reduced.

3.3.4 Cross-Coupled Negative Charge Pump with Asymmetric NMOS

The above mentioned bulk biasing can only be implemented with the help of the triple well process which has symmetric high voltage transistor in it. But unfortunately most of the high voltage processes do not have the symmetric type high voltage transistor. Instead, they are asymmetric structures as shown in Fig. 34. As we can see, the source and bulk are butted in an asymmetric transistor. The NBL is a deep n-well buried under the high voltage p-well HVPW and high voltage n-well HVNW. Therefore the negative voltage applied on the transistor can be blocked from the p-substrate.

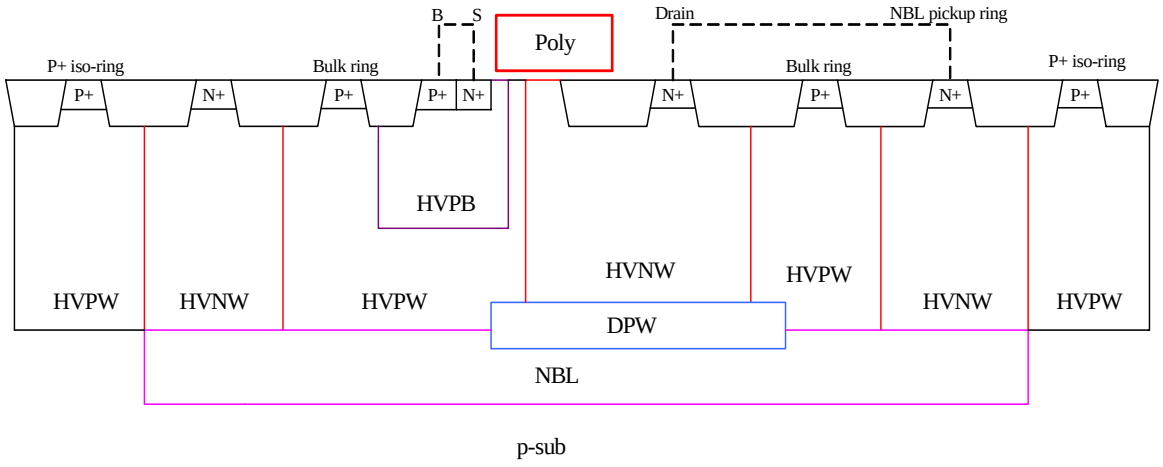


Fig. 34 Asymmetric high voltage 40V NMOS transistor profile

The cross-coupled negative charge pump utilizing asymmetric high voltage transistors is

shown in Fig. 35. The bulk and source of the asymmetric transistors are butted together. The profit of the asymmetric transistor structure is to reduce the latch-up in the transistors. And the DPW layer in the asymmetric high voltage transistor can prevent the deep n-well NBL and the high voltage n-well of the drain terminal from forward biasing.

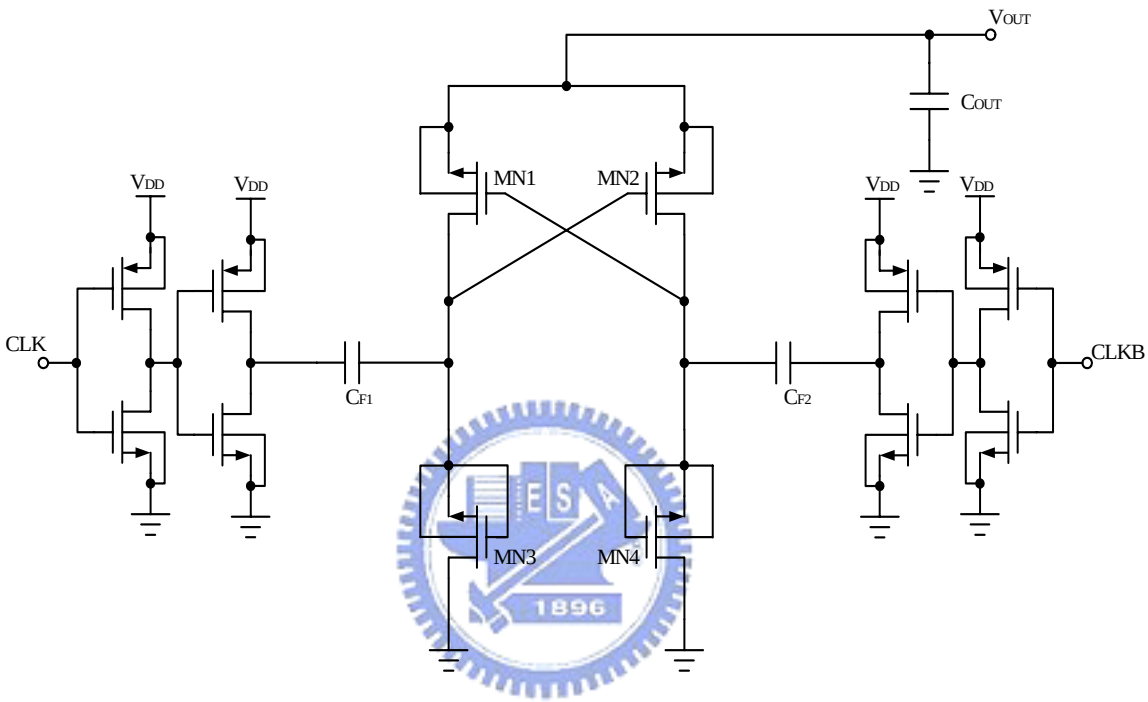


Fig. 35 Negative charge pump using asymmetric high voltage transistors

The operation of the cross-coupled negative charge pump which uses asymmetric high voltage transistor is as same as the type with bulk biasing circuits. Transistors MN3 and MN4 are diode-connected as switches to charge the pumping capacitors C_{F1} and C_{F2}. And the output power transistors MN1 and MN2 are control by the Vo2 and Vo1 respectively as a cross-coupled structure. The reversion loss may occur in the cross-coupled structure. So in later sections, the reversion loss and the technique to reduce it will be presented.

3.3.5 Reversion Loss

The efficiency of a charge pump is related to three energy consumptions [34], [35]. The first one is the energy which supplied by the input voltage (V_{DD} or the square wave signal). The second is the energy consumed by the load. The third is the energy loss of the charge pump. The energy losses include the redistribution loss, conduction loss, switching loss and reversion loss [34]. If we want a high efficiency charge pump, the energy losses must be minimized. Redistribution loss is generated when charge transferring between capacitors [34]. Conduction loss is generated by the finite switch resistance. Switching loss is the charge losses to gate drives and parasitic capacitors. Reversion loss arises from shorting a higher voltage to a lower voltage, and the current will flow from the higher voltage terminal to the lower voltage terminal. It is then defined as the reversion loss because it is due to the reversion charge transfer. In the next we will discuss the reversion loss and the ways to reduce it. A proper gate control schematic can be used to do so.

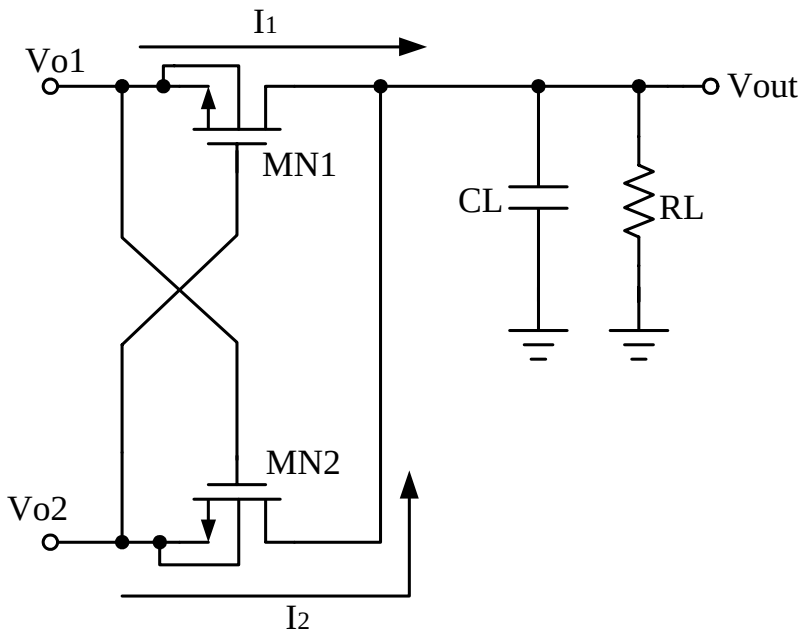


Fig. 36 Reversion loss of the output transistors

Fig. 36 shows the reversion loss occurs in the output transistors of the cross-coupled negative charge pump. As we can see from Fig. 32, nodes Vo1 and Vo2 are connected to the capacitors C2 and C4. The other nodes of capacitors C2 and C4 are connected to the buffers which supply square waves. Therefore nodes Vo1 and Vo2 are going to have square wave signals on them. When output voltage has been pulled to a negative voltage level, transistors MO1 and MO2 are supposed to be turned on while Vo1 and Vo2 are at lower voltages than the output node. Transistors MO1 and MO2 are supposed to be turned off when Vo1 and Vo2 are at higher voltages than the output node. At the same time, because of the cross-coupled structure, Vo1 is connected to the gate of the transistor MO2 and controls the switching; Vo2 is connected to the gate of the transistor MO1 and controls its switching. Vo1 and Vo2 are designed to be two different phase square wave signals. But when Vo1 and Vo2 are at the high voltage V_H at the same time as shown in Fig. 36, MO1 and MO2 will be turned on and the charge will transfer from high voltage nodes Vo1 and Vo2 to the lower voltage output node. This unwanted charge transfer becomes the reversion loss in the cross-coupled negative charge pump.

3.3.6 Reversion Loss Reduction Technique

The reversion loss has been mentioned in the previous section. The appearance of the reversion loss reduces the efficiency of the cross-coupled negative charge pump and leads to larger output voltage ripple. If we want to have a high efficiency cross-coupled negative charge pump, the reversion loss must be canceled or minimized. In this section, we will propose techniques to reduce the reversion loss at the charging stage and the output stage.

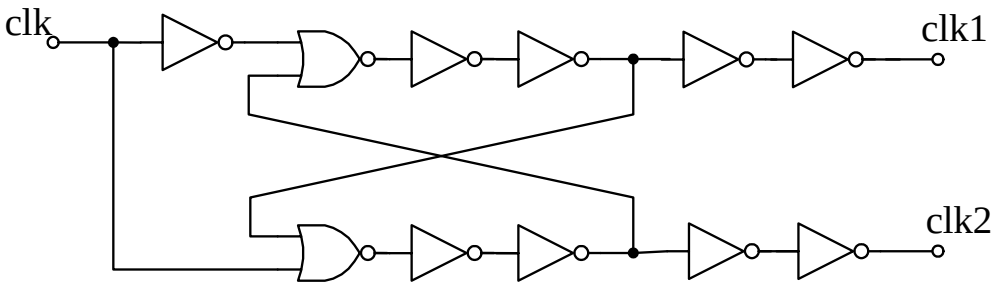


Fig. 37 Non-overlapping square wave control signal generator

The reversion loss at the output stage mentioned above is due to the inverting control signals being high at the same time. As shown in Fig. 37, it is a non-overlapping square wave control signal generator. It can generate two square wave signals with inverting phases and will not be high at the same time. By using the technique, the reversion loss at the output stage can be minimized.

3.3.7 Multi-Stage Negative Charge Pump

The proposed cross-coupled negative charge pump is not limited to generate a negative voltage from the positive voltage. It can also produce a much negative voltage from a negative input voltage. As an example, Fig. 38 shows a 3-stage negative charge pump utilizing cascading 3-stage cross-coupled negative charge pump in series and level shifters to generate the control signal to next stage. As we can see, you can have a $-2V_{DD}$ output voltage from a $-V_{DD}$ input and a square wave swing from $-V_{DD}$ to GND. And you can have a $-3V_{DD}$ output voltage from a $-2V_{DD}$ input and a square wave swing from $-2V_{DD}$ to $-V_{DD}$. Utilizing this structure, you can generate a negative voltage as you want by cascading more stages of cross-coupled negative charge pump to achieve the target negative voltage. When cascading n-stages of the negative charge pump you can get a negative voltage level $-nV_{DD}$ instead of

$-2^{n-1}V_{DD}$ in [24].

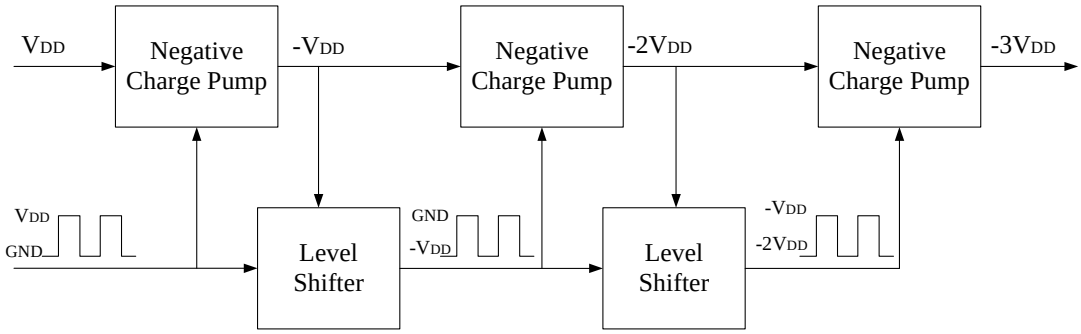


Fig. 38 Schematic of 3-stage negative charge pump

Because the n-stage charge pumps in [24], each stage can boost the output voltage to twice the input voltage. But when using a low voltage process, the structure will course the transistors to suffer high voltage stresses and leads to break down of the transistors. When using the schematic in Fig. 38, each stage only suffers $2V_{DD}$ voltage stresses on the transistors. Therefore, we can generate a high negative voltage in a lower voltage process.

3.4 Negative to Positive Charge Pump

In the previous sections, the positive charge pump which can boost the input positive voltage to a higher positive voltage and the negative charge pump which can generate a negative voltage lower than the ground from positive input voltage are presented. In this section, another charge pump type called negative to positive charge pump is going to be proposed. As implied by the name, the negative to positive charge pump can generate a positive voltage from a negative input voltage. Therefore, the negative voltage generated by the negative charge pump can be used to provide a positive voltage if the output selection is the positive voltage.

3.4.1 Proposed Negative to Positive Charge Pump Circuit

The proposed negative to positive charge pump is shown in fig. 39. The structure is much like the negative charge pump's. The different is that the output power transistors are replaced by PMOS transistors and the input clock signals swing between ground and a negative voltage $-V_{DD}$. The operation of the proposed negative to positive charge pump will be given below. The target of the negative to positive charge pump is to transform the input negative voltage to a positive output voltage. The input of the circuit is a square wave swing from the ground to the negative voltage $-V_{DD}$. The clock is generated by the input clock which is a square wave between the ground and input voltage V_{DD} and a positive to negative level shifter which shifts the clock to the negative level we want.

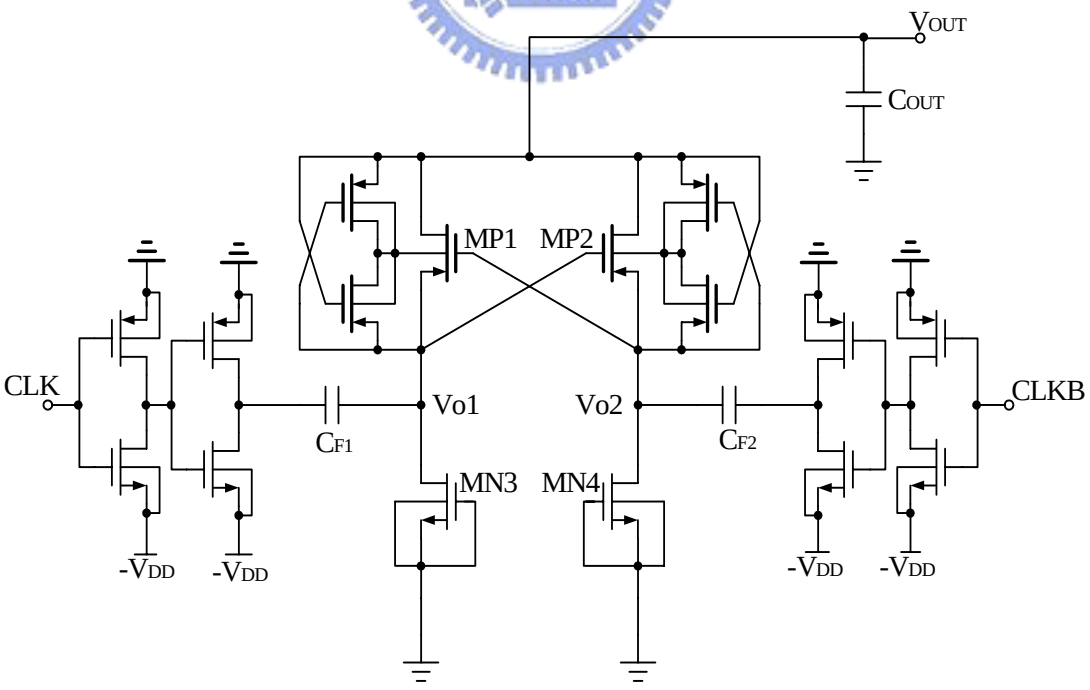


Fig. 39 Negative to positive charge pump schematic

The circuit is also connected as cross-coupled structure to reduce the output ripple and improve the efficiency. The clock signals are two out-of-phase square wave with non-overlapping technique to minimize the reversion current loss. First, when CLK is at low as voltage $-V_{DD}$, pass transistor MN3 will be turned on and charge the flying capacitor C_{F1}. During the next phase, CLK changes from low to high as the ground level, the pass transistos MN3 is turned off and the output transistor MP1 is turned on by the cross-coupled structure node Vo2. And a positive voltage V_{DD} is generated and transfer to the output node. In the another half of the circuit, the operation is same because of the cross-coupled structure.

Chapter 4

Circuits Implementation and Simulation Results

4.1 Output Stages and Control Circuits

The selectable multi-output DC-DC converter utilizing charge pumps needs an output stage to transfer the selected voltage level which is generated by the charge pumps to the output node. As you can see in Fig. 26, there are four output stages with corresponding control circuits. In this section, we are going to present the circuits implementations of the output stages and the control circuits

4.1.1 Output Stages

The output stage is consist of four power transistor switches controlled by four control signals CT1, CT2, CT3 and CT4 as shown in Fig. 26. The control signal CT1 controls the control circuit 1 and the output stage of the negative voltage $-V_{DD}$. The control signals CT2, CT3 and CT4 control the control circuit 2, 3 and 4 and the output stages of the positive voltage 10V, 20V and the ground 0V respectively. The output stages of each output voltages are different because of the difference of the voltages between the output node and the

generated voltages. The output stages are going to be unfolded later in this chapter.

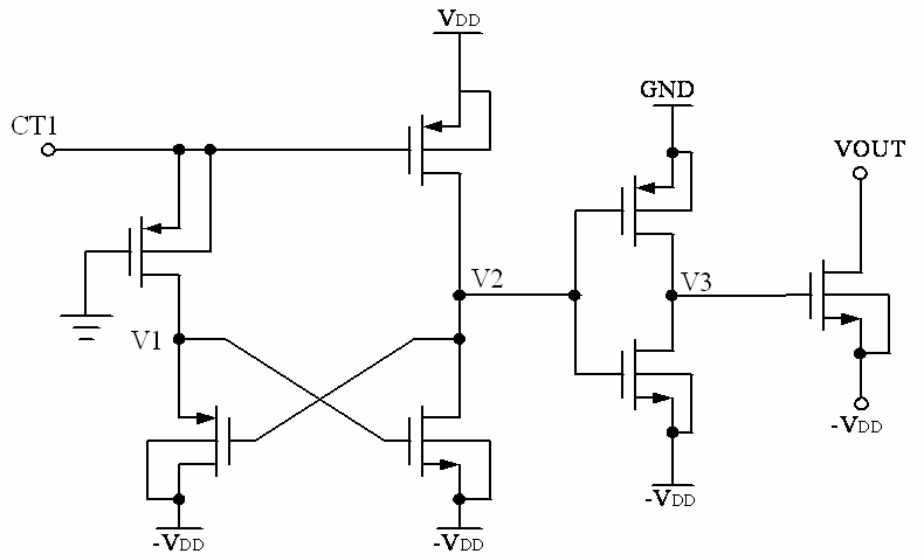


Fig. 40 Output stage of the negative charge pump

Fig. 40 is the circuit schematic of the output stage which outputs the negative voltage from the negative cross-coupled charge pump to the output terminal. CT1 is the control signal as a square wave swings between input voltage V_{DD} and the ground. It transforms to a square wave swings between the ground the negative voltage $-V_{DD}$ by the level shifter circuit in the output stage to control the output power transistor. We name the output stage which is shown in Fig. 40 as output stage 1. The simulation result of the output stage 1 is shown in Fig. 41. The input is control signal CT1 and the output is the delivered output VOUT.

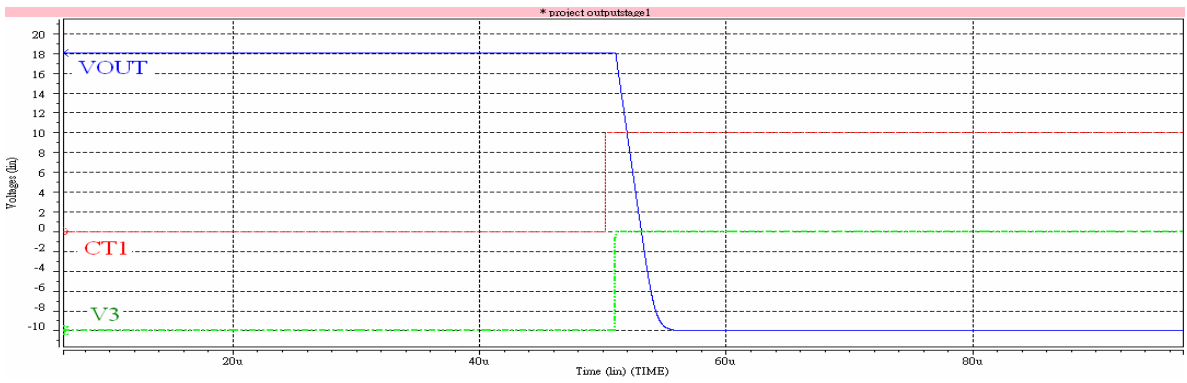


Fig. 41 Simulation of the output stage 1

As shown in Fig. 41, the input control signal CT1 controls the delivering of the negative voltage $-V_{DD}$ to the output node. When CT1 is high, the voltage at node V3 will be pulled high from the negative voltage $-V_{DD}$ to the ground, it will turn on the power transistor M_{O1} and pull the output voltage to the negative voltage $-V_{DD}$ as shown in the figure.

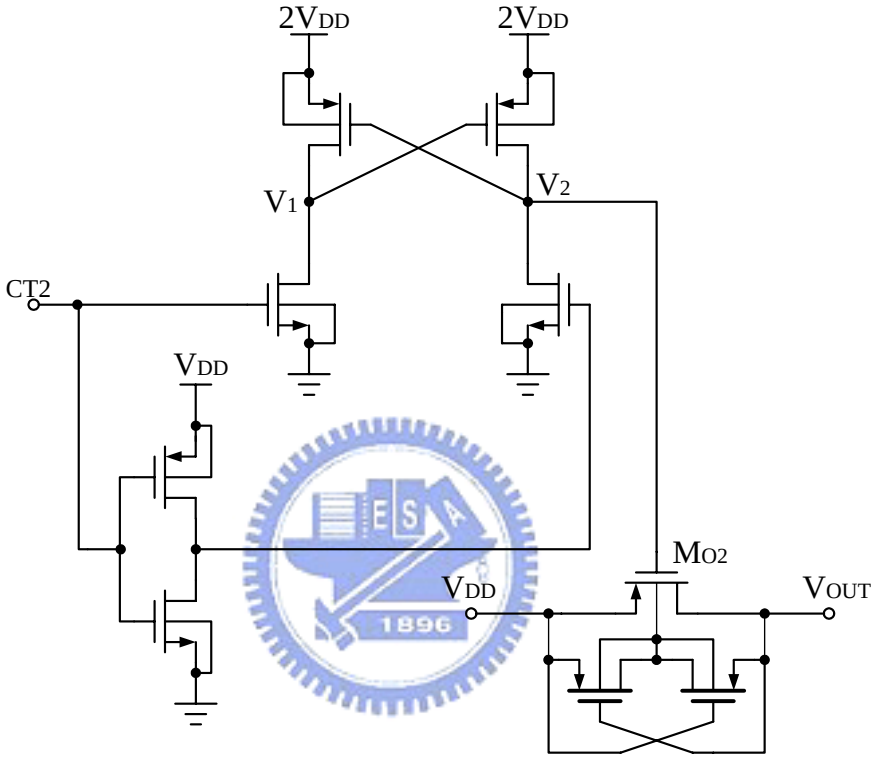


Fig. 42 Output stage of the input voltage V_{DD}

Fig. 42 is the output stage for the input voltage V_{DD} transferring. The control signal CT2 is a square wave swings between the input voltage V_{DD} and the ground. It passes a level shifter and transform to a square wave at node V2 swings between the highest voltage $2V_{DD}$ and the ground. By doing so, the power transistor M_{O2} can be turned off correctly when the output node is at the highest voltage $2V_{DD}$. A pair of PMOS transistor is connected to the bulk of the power transistor M_{O2} to bias the bulk to the highest voltage of the transistor. Fig. 43 shows the simulation results of the above output stage. The output voltage can be pulled from both high to low and low to high as shown in the figure.

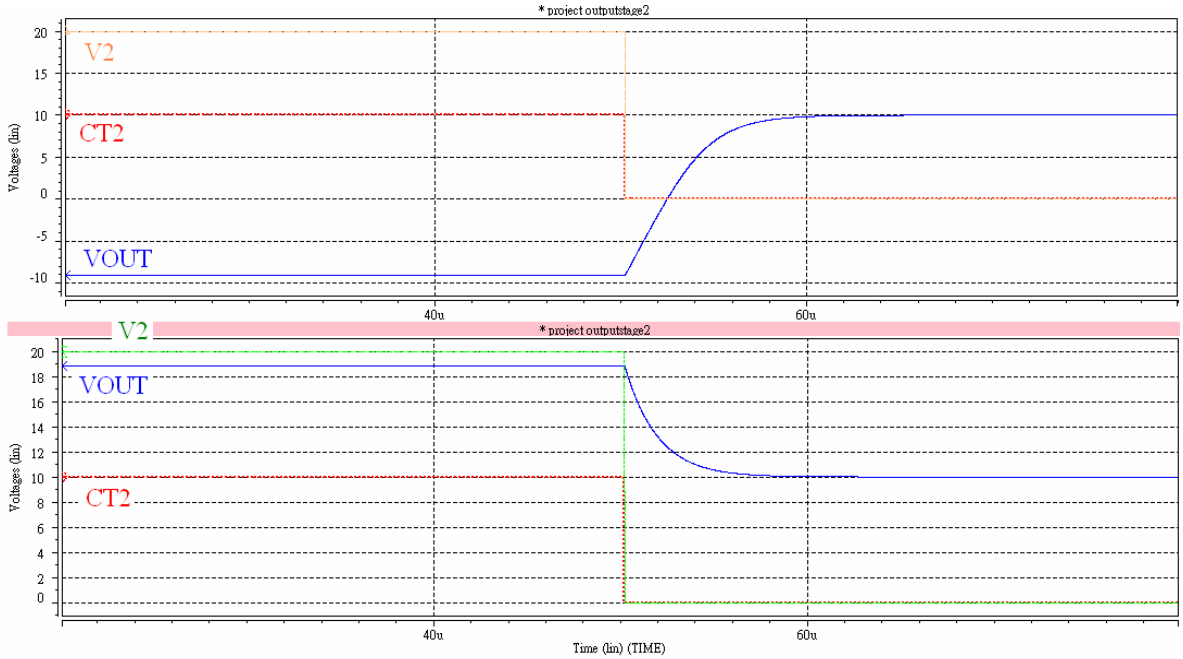


Fig. 43 Simulation of the output stage 2

Fig. 44 is the output stage which delivers the highest voltage $2V_{DD}$ to the output terminal. The structure is much similar as the output stage shown in Fig. 42.

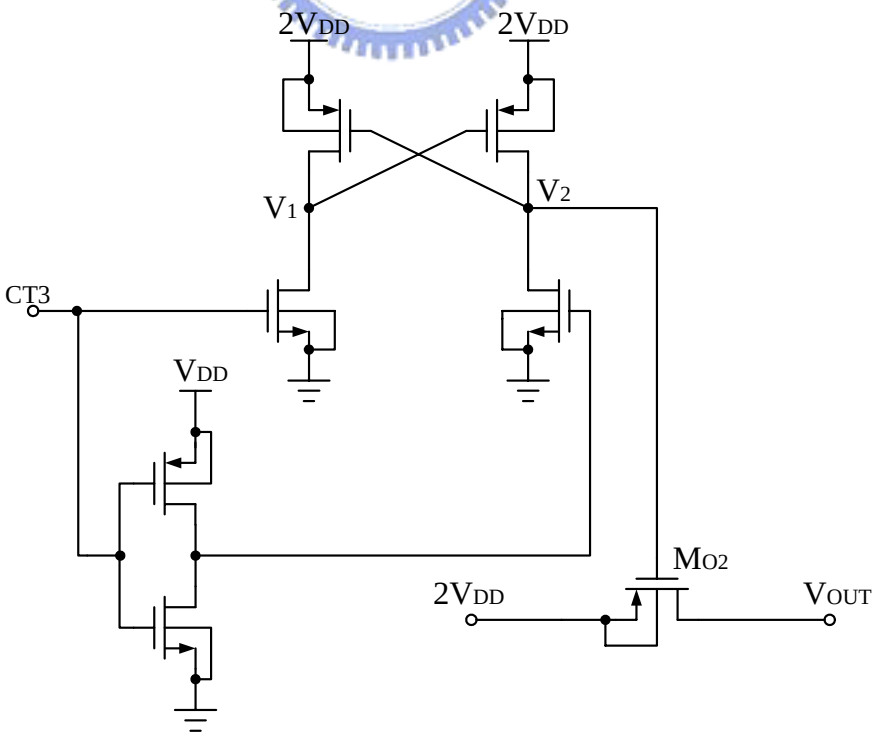


Fig. 44 Output stage of the positive charge pump

The control signal CT3 is a square wave swings between the input voltage V_{DD} and the ground. It passes a level shifter and transform to a square wave at node V2 swings between the highest voltage $2V_{DD}$ and the ground. By doing so, the power transistor M_{O2} can be turned off correctly when the output node is at the highest voltage $2V_{DD}$. The simulation is shown in Fig. 45. The voltage is delivered to the output terminal while CT3 and V2 are low. The output terminal can be pulled to the highest voltage $2V_{DD}$ by the output stage no matter the original voltage of the output terminal is a positive or even a negative voltage.

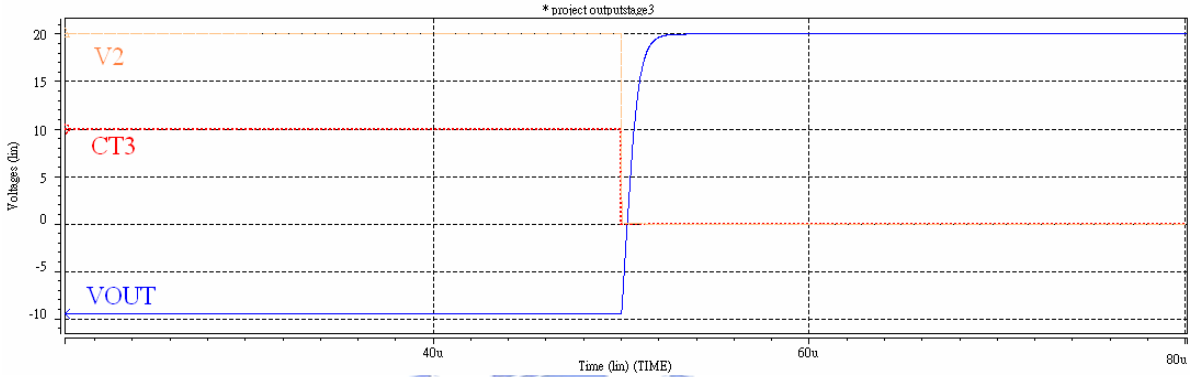


Fig. 45 Simulation of the output stage 3

The last output stage is the output stage which delivers the ground level to the output terminal as shown in Fig. 46. The above-mentioned output stages all need only one power transistor to deliver the voltage. But when it comes to the output stage here, only one power transistor to switch and deliver the ground level to the output terminal will lead to the unwanted leakage current when the transistor supposed to be turned off. Because the original voltage of the output terminal might be higher or lower than the ground level, the output power transistor must be redesign to fit the requirement. If the output power transistor is a PMOS transistor, it can deliver the ground level to the output terminal when it is at negative voltage lower than the ground. And a positive voltage at the output terminal will force the PMOS transistor to leakage a reverse current from output to the ground at the turning off period. Similarly, if the output power transistor is a NMOS transistor, a negative at the output

terminal will force the NMOS transistor to leakage a reverse current from the ground to the output terminal at the turning off period.

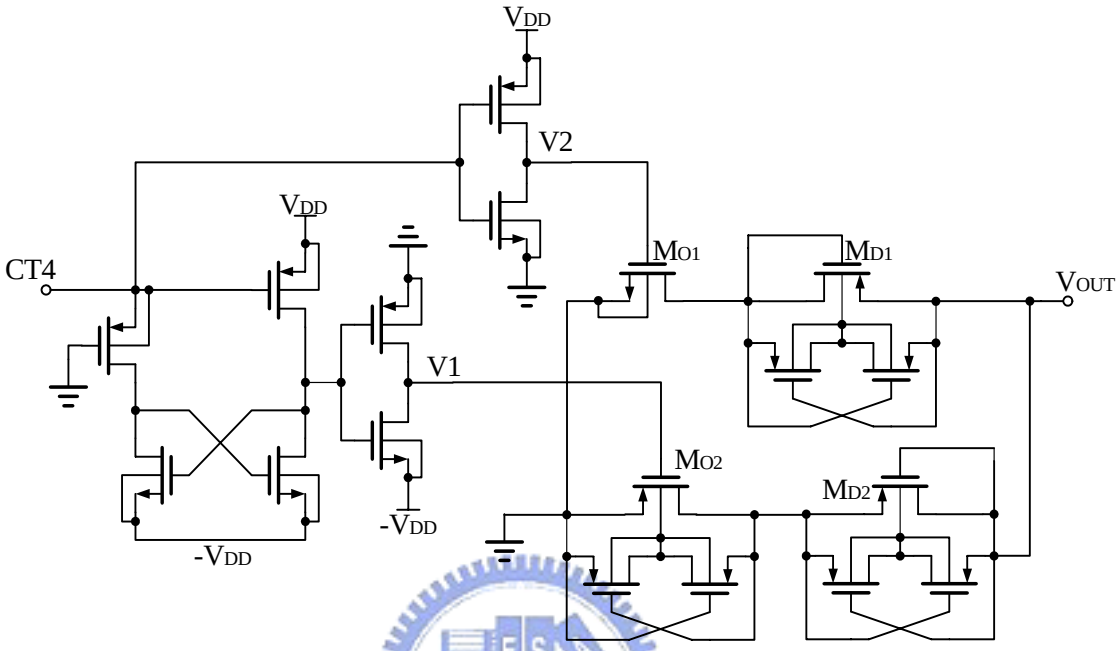


Fig. 46 Output stage of the ground voltage

The output stage of the ground voltage is shown in Fig. 46. It is more complicated than the other above mentioned output stages. It uses two output power transistors to deliver the output voltage level. A PMOS transistor M_{O2} delivers the charge while the output terminal is at a negative voltage lower than the ground and a NMOS transistor M_{O1} delivers the charge while the output terminal is at a positive voltage higher than the ground. Two diode-connected PMOS transistors with bulk biasing circuits M_{D1} and M_{D2} are introduced to prevent the corresponding output power transistors from conducted in the turning off period. The control signal CT4 will transform to a square wave at node V1 which swings from the ground to the negative voltage –VDD to correctly control the output power transistor M_{O2}. And another output power transistor M_{O1} is controlled by CT4 directly.

The simulation result of the output stage 4 is shown in Fig. 47. CT4 is the input control signal. V2 is the reversion of the control signal CT4. V1 is the signal generated by level shifting the control signal C4. As we can see, the output voltage can be pulled to the ground level no matter the original output voltage is higher or lower than the ground. And the output can remain its original voltage when the output stage is turned off without leakage current.

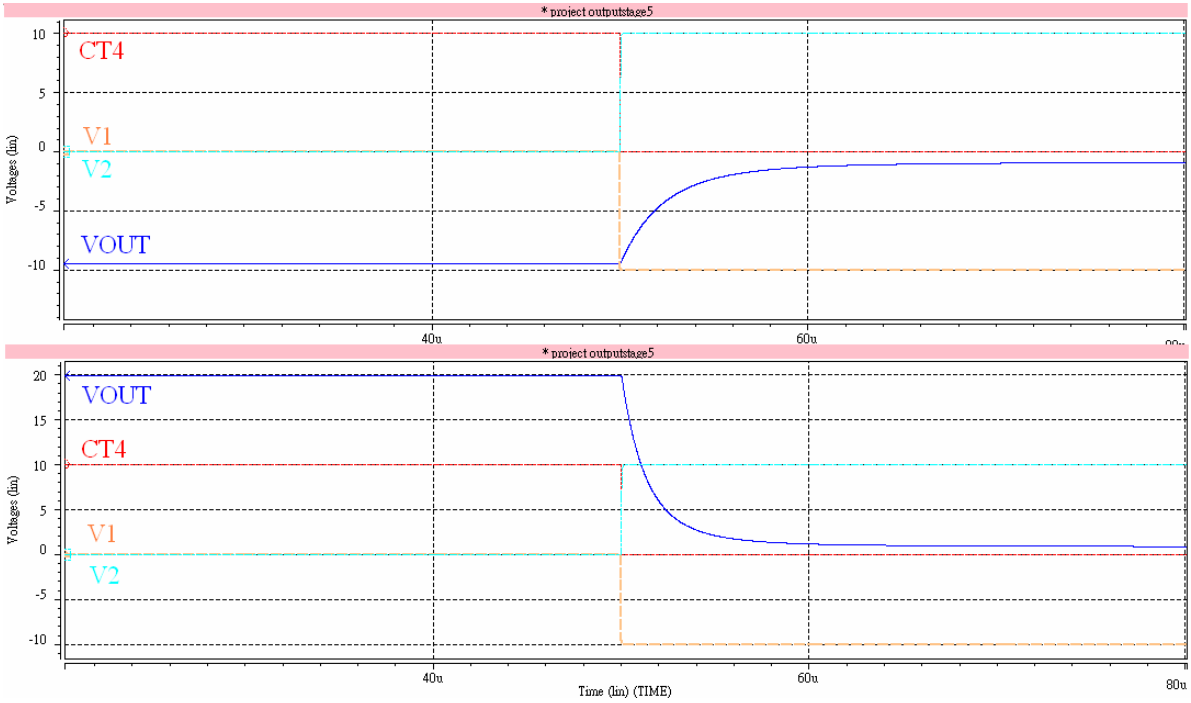


Fig. 47 Simulation of the output stage 4

4.1.2 Control Circuits

The proposed selectable multi-output DC-DC converter can output the desired voltage as you want. By a given control signal, the output stages will be controlled and decide what voltage you want to transfer to the output terminal. There are four different outputs voltages with four output stages. Only one output stage will be turned on at the same time. A pair of control signal X and Y is needed to control the four output stages. The table 1 is the truth table of the signals X, Y, CT1, CT2, CT3, CT4 and the corresponding output voltage V_{OUT}.

X	Y	CT1	CT2	CT3	CT4	V_{OUT}
GND	GND	GND	V_{DD}	V_{DD}	GND	GND
GND	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	$-V_{DD}$
V_{DD}	GND	GND	V_{DD}	GND	V_{DD}	$2V_{DD}$
V_{DD}	V_{DD}	GND	GND	V_{DD}	V_{DD}	V_{DD}

Table 1 Control signal to output reference

The control signal circuit implementation is shown in Fig. 48. It consists of three NAND gates, one NOR gate and four inverters.

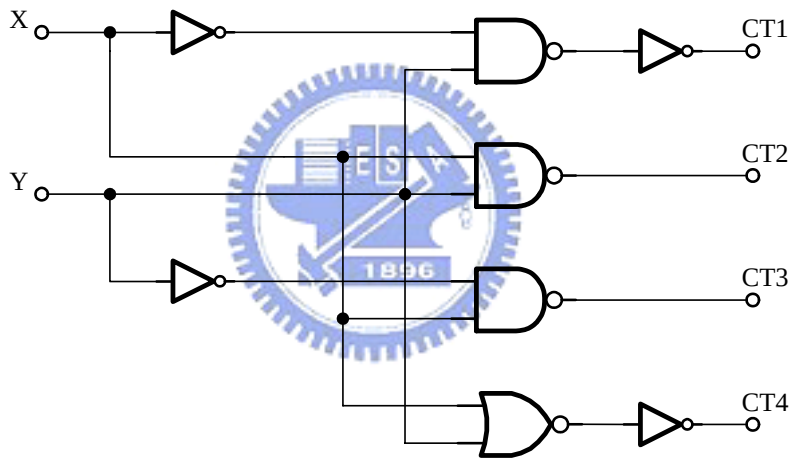


Fig. 48 Control Signal Circuit

The simulation of the control signal circuit is shown in Fig. 49. When X and Y are low, the output stage 4 will be turned on and delivers the ground voltage to the output terminal. When X is low and Y is high, output stage 1 will be turned on and delivers the negative voltage $-V_{DD}$ to the output terminal. When X is high and Y is low, the output stage 3 will be turned on and delivers the most positive voltage $2V_{DD}$ to the output terminal. When X and Y are high, the output stage 2 will be turned on and delivers the input voltage V_{DD} to the output terminal.

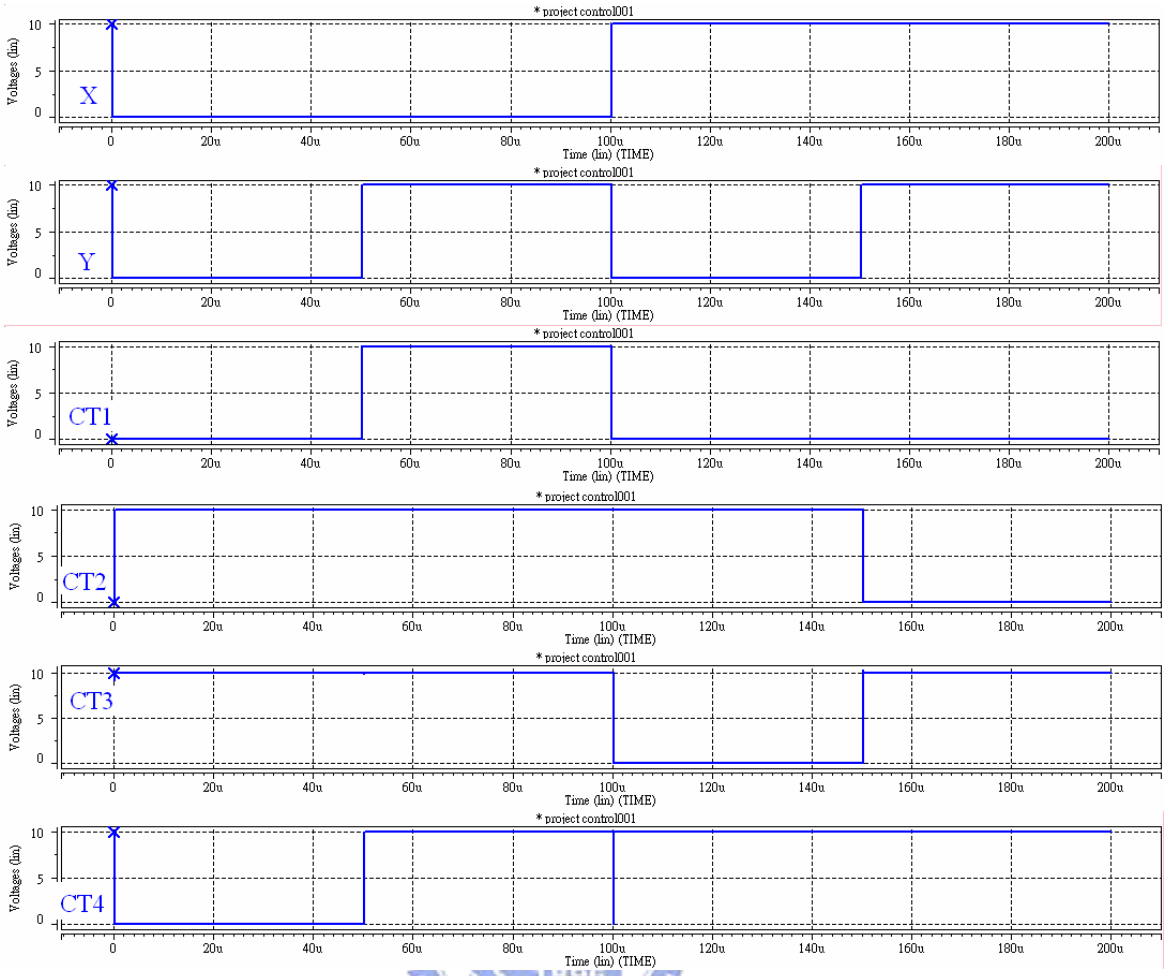


Fig. 49 Simulation result of the control signal circuit

4.2 Simulation Results

In this chapter, the simulation results of the above-mentioned charge pumps and the selectable multi-output DC-DC converter will be presented.

4.2.1 Improved Cross-Coupled Charge Pump

The simulation of the improved cross-coupled charge pump proposed in previous chapter

is shown in Fig. 50. The input voltage is 10V and the output load current is 20mA. It sweeps the temperature from -40℃ to 140℃. The worst case is occurred at the temperature 140℃. The transient is slower when the temperature is higher. The output voltage range is from 19.1V at -40℃ to 19.4V at 140℃.

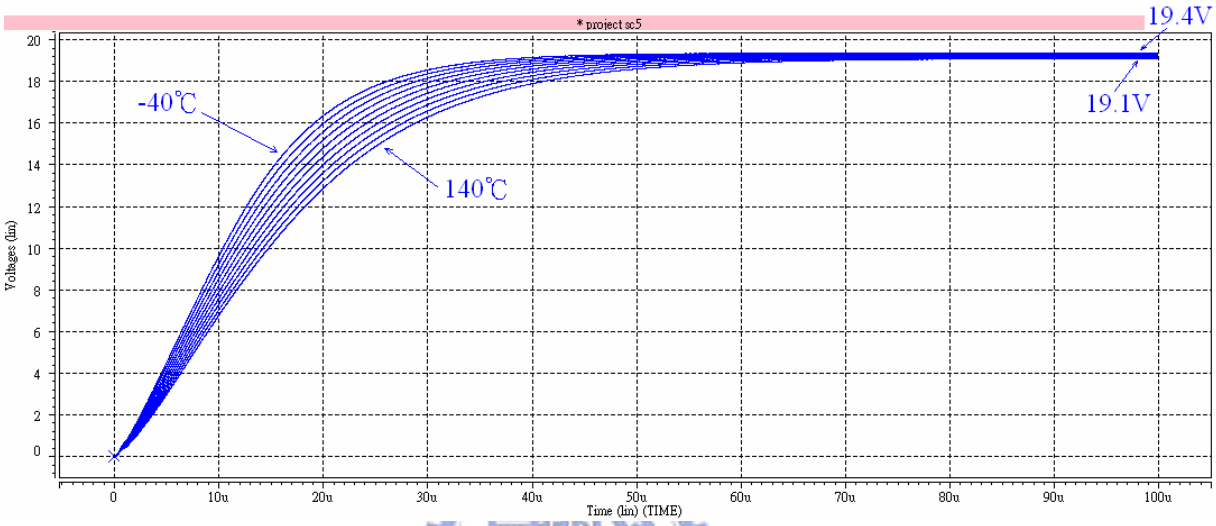


Fig. 50 Output of the improved cross-coupled charge pump under the temperature from -40℃ to 140℃

Fig. 51 is the zoom in simulation result of the above wave form when the temperature is 40℃. The ripple of the proposed improved cross-coupled charge pump is about 8mV.

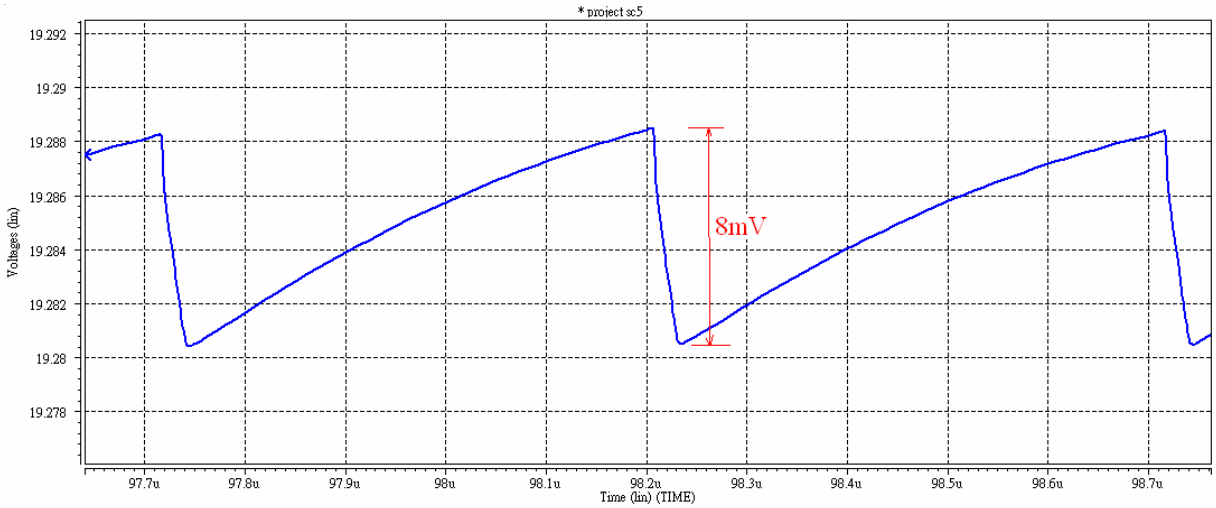


Fig. 51 Output ripple of the improved cross-coupled charge pump

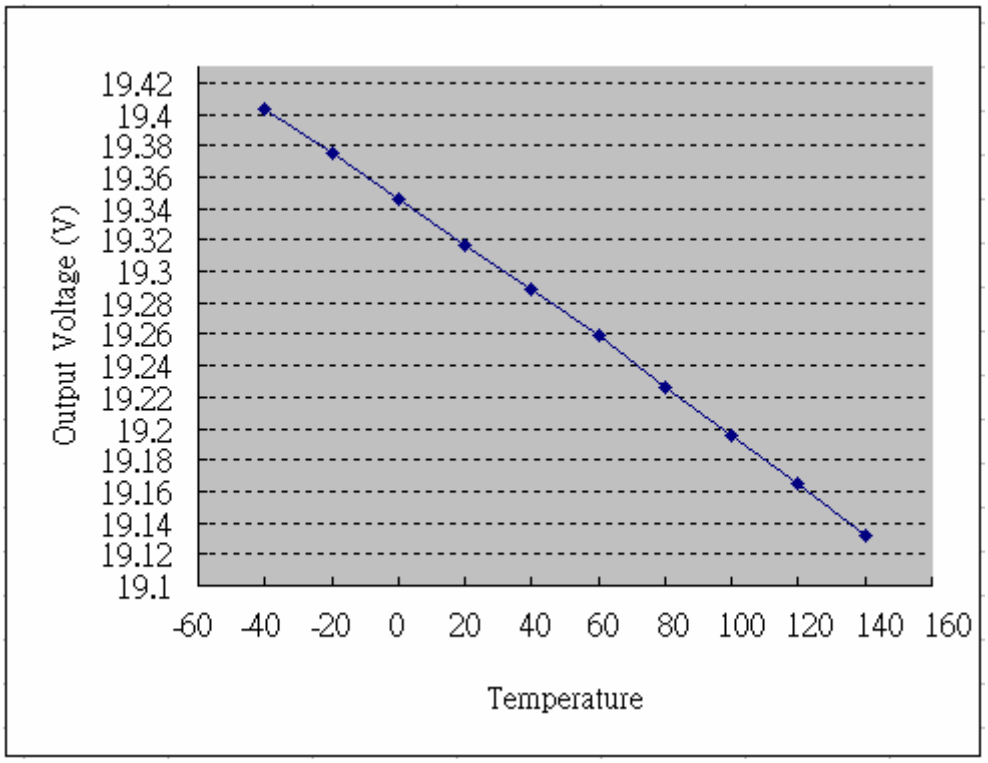
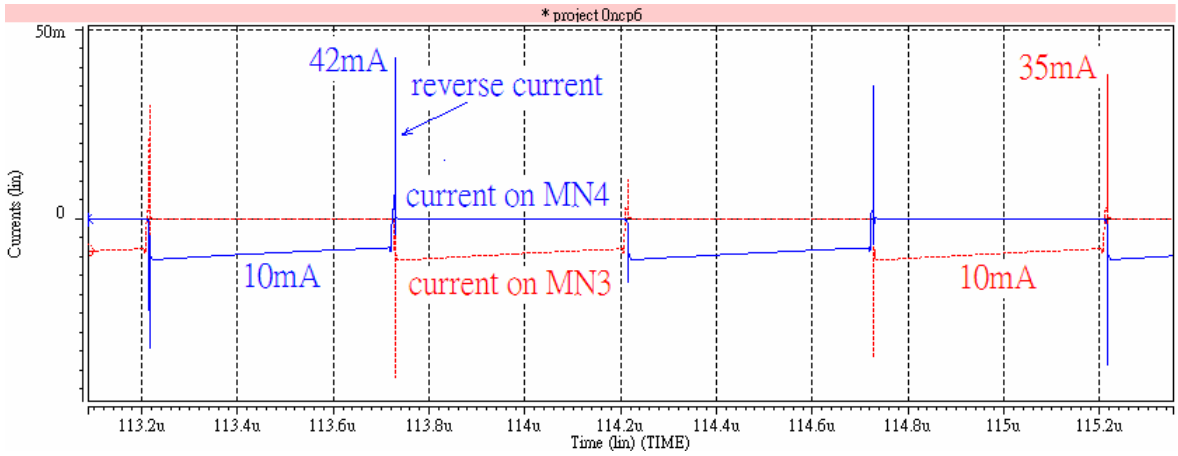


Fig. 52 Temperature to output voltage diagram of the cross-coupled negative charge pump

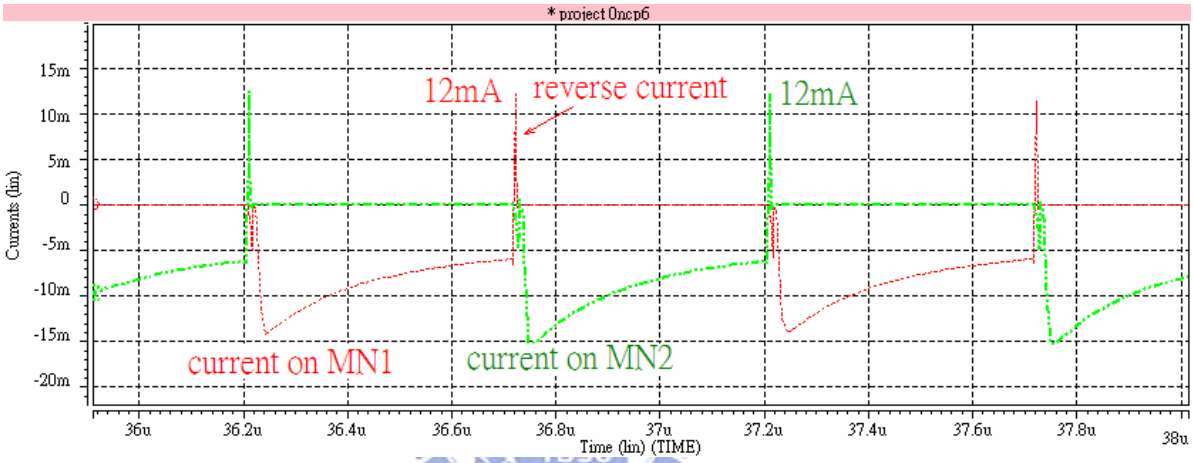
Fig. 52 is the temperature to output voltage diagram of the improved cross-coupled charge pump. The temperature sweeps from -40℃ to 140℃. We can see that the achievable output voltage decreases with the temperature. Higher temperature will leads to higher threshold voltage and decrease the output voltage

4.2.2 Cross-Coupled Negative Charge Pump

The following is the simulation results of the proposed cross-coupled negative charge pump.



(a)



(b)

Fig. 53 Current on (a)MN3, MN4 (b)MN1, MN2 of the proposed cross-coupled negative charge pump

Fig. 53 is the simulation of the current in the pass transistors in the proposed cross-coupled negative charge pump. Fig. 53(a) shows the current on the charging transistors MN3 and MN4. The reverse current which is considered as the reversion loss is reduced to 35mA and 42mA respectively. Fig. 53(b) shows the current on the output cross-coupled transistors MN1 and MN2. The reverse current which is considered as the reversion loss is reduced to 12mA by the reversion loss reduction technique.

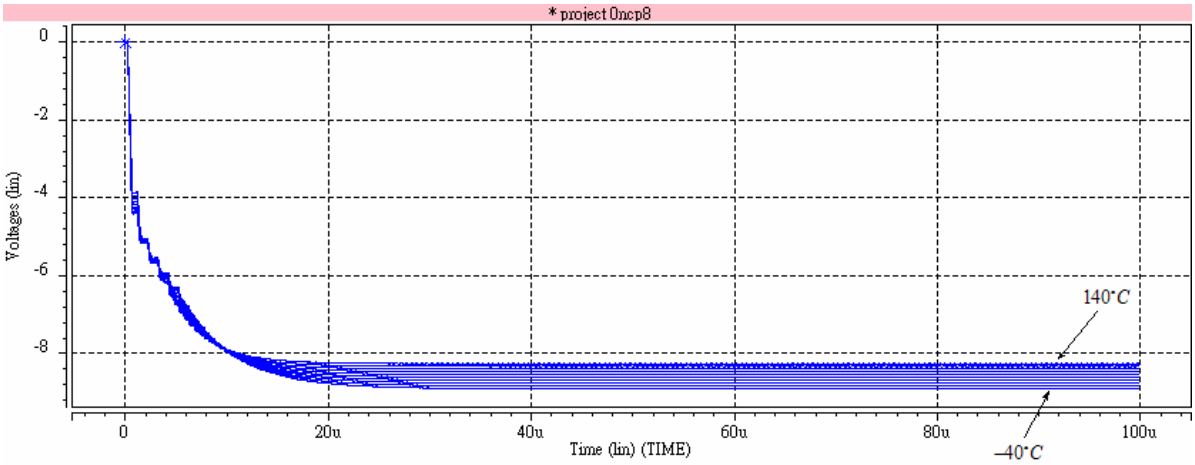


Fig. 54　Output of the cross-coupled negative charge pump with reversion loss reduction under the temperature from -40℃ to 140℃

Fig. 54 is the simulation of the cross-coupled negative charge pump's output sweeps from -40℃ to 140℃. The input voltage is 10V and the load current is about 10mA. The worst case is occurred at the temperature 140℃.

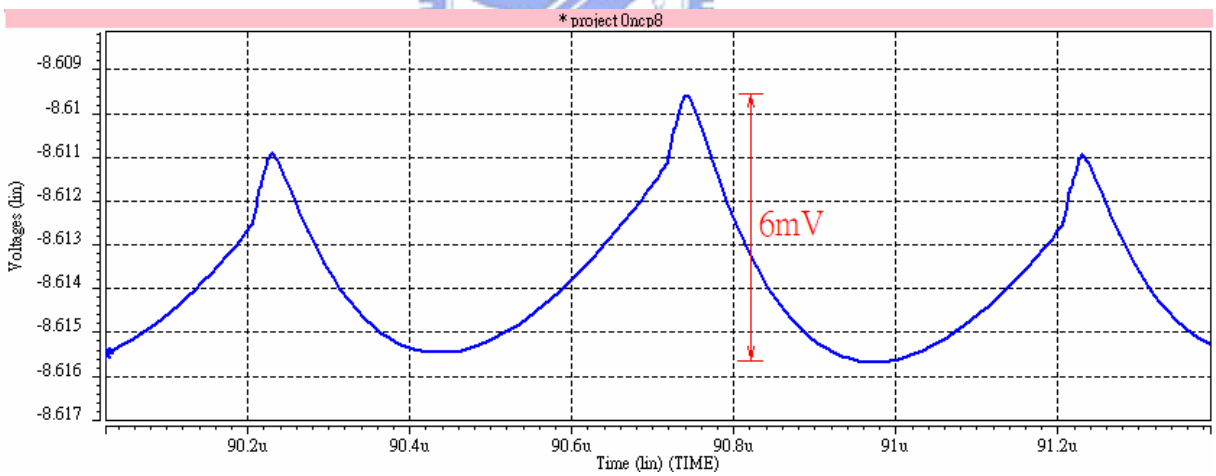


Fig. 55　Output ripple of the cross-coupled negative charge pump

Fig. 55 is the output ripple simulation result of the proposed cross-coupled negative charge pump with reversion loss reduction technique. The input voltage is 10V and the frequency of the control signal is 1MHz. The simulation is under the temperature 40℃. As we can see, the output ripple is about 6mV and the maximum output voltage is -8.6157V.

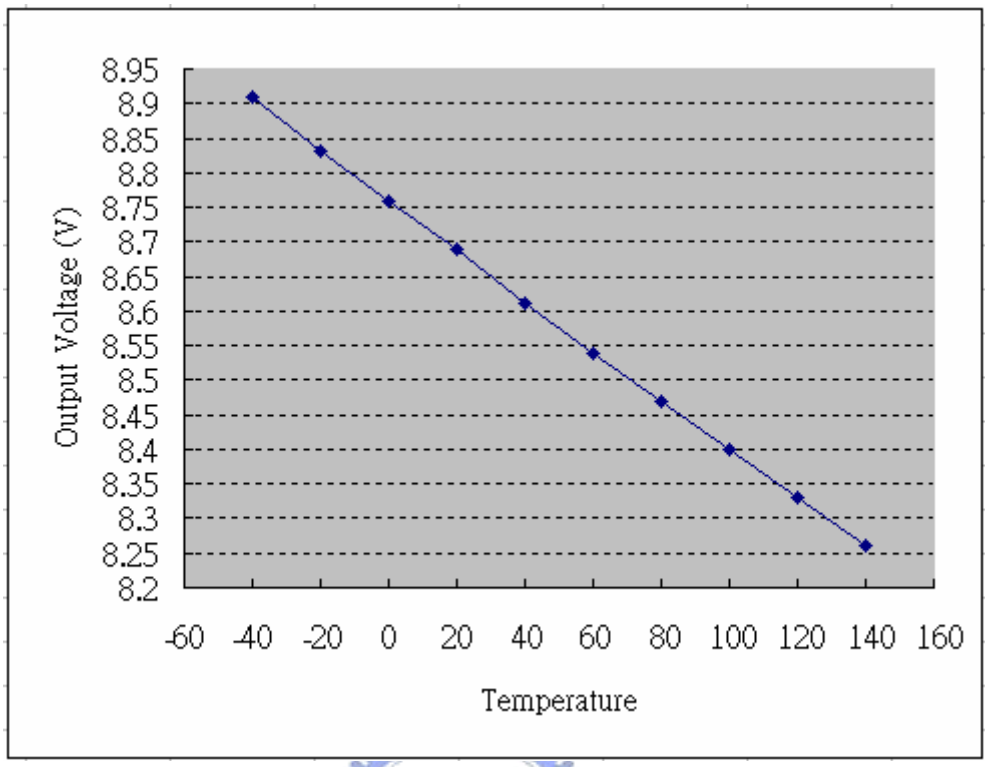


Fig. 56 Temperature to output voltage diagram of the cross-coupled negative charge pump

Fig. 56 is the temperature to output voltage diagram of the cross-coupled negative charge pump. The temperature sweeps from -40℃ to 140℃. We can see that the achievable output voltage decreases with the temperature. Higher temperature will leads to higher threshold voltage and decrease the output voltage.

4.2.3 Load Regulations

Fig. 57 is the load transient response waveform of the proposed cross-coupled charge pump when the supply voltage is 10V. The heavy load transient time is about 0.056ms when the load changes from 10mA to 50mA. The output current steps from 10mA to 50mA and the output voltage variation is 1.183V. The load regulation is 29.57mV/mA.

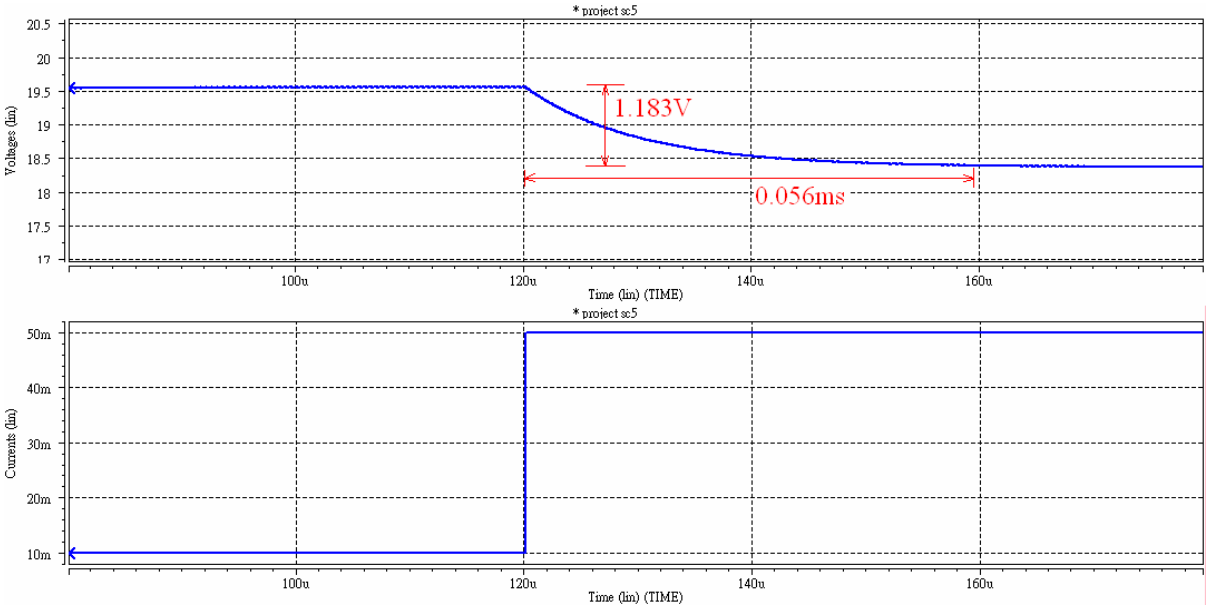


Fig. 57 Load regulation of the proposed cross-coupled charge pump

Fig. 58 is the load transient response waveform of the proposed cross-coupled negative charge pump when the supply voltage is 10V. The heavy load transient time is about 0.0167ms when the load changes from 10mA to 50mA. The output current steps from 10mA to 50mA and the output voltage variation is 0.7121V. The load regulation is 17.803mV/mA.

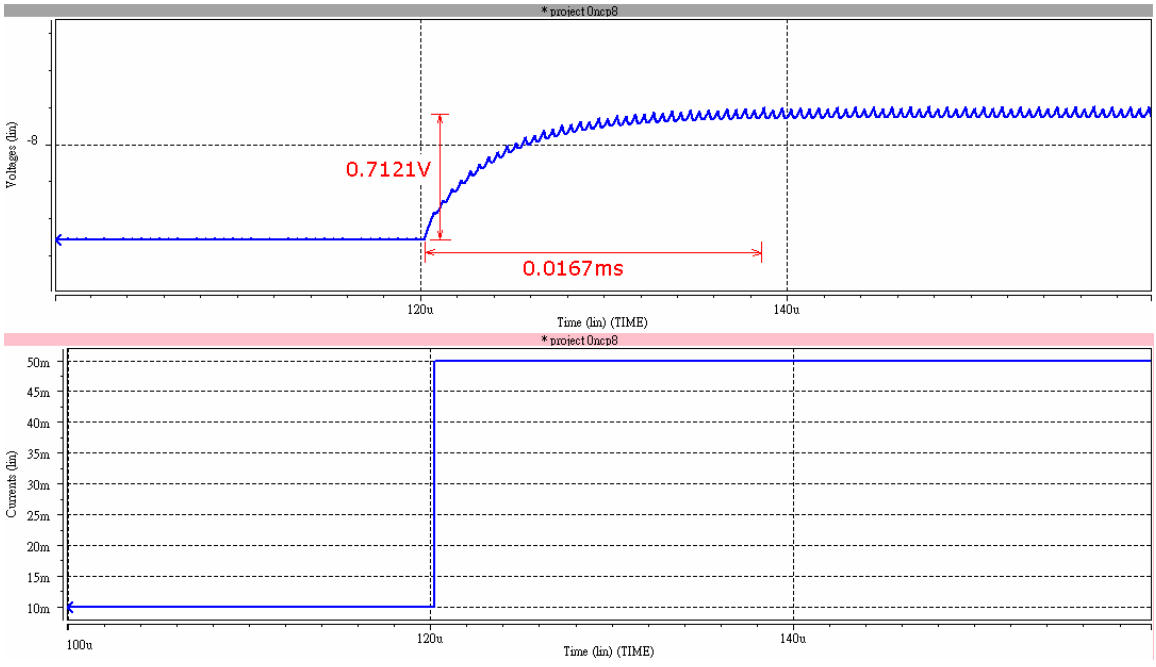


Fig. 58 Load regulation of the proposed cross-coupled negative charge pump

4.2.4 Selectable Multi-Output DC-DC Converter

The overall circuit schematic of the proposed selectable multi-output DC-DC converter is shown in Fig.59. It consists of an improved cross-coupled charge pump, a negative cross-coupled charge pump with reversion loss reduction technique, a control signal circuit and four output stages.

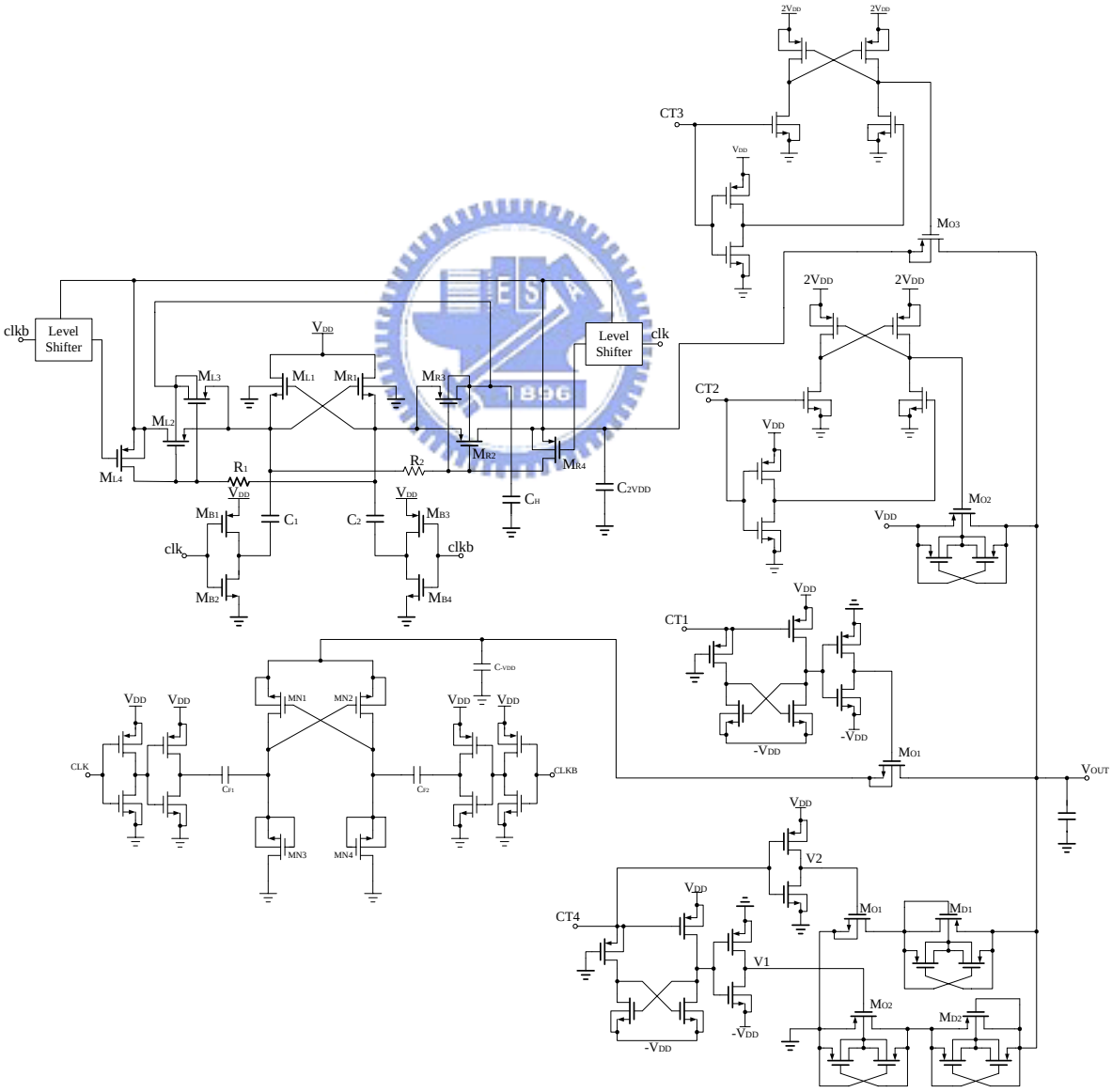


Fig. 59 Overall circuit schematic of the proposed selectable multi-output DC-DC converter

The simulated output of the proposed selectable multi-output DC-DC converter is shown in Fig. 60. The input voltage is 10V and the load current is 20mA. From the figure, we can see that you can switch the output terminal to the desired voltage as you want arbitrarily.

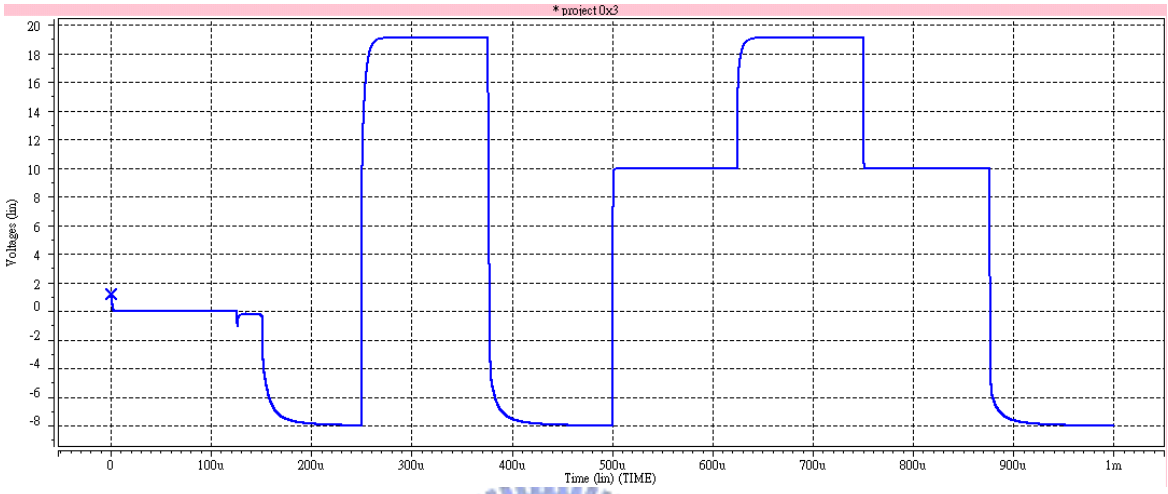


Fig. 60 Output of the selectable multi-output DC-DC converter

4.3 Layout of the Work

The layout [36] of the proposed circuit is shown in Fig. 61. It consists power transistors, output stages and the control circuits. The design was fabricated with the TSMC 0.25um high voltage 1P5M BCD process. The total chip area about 1900 μm *1600 μm

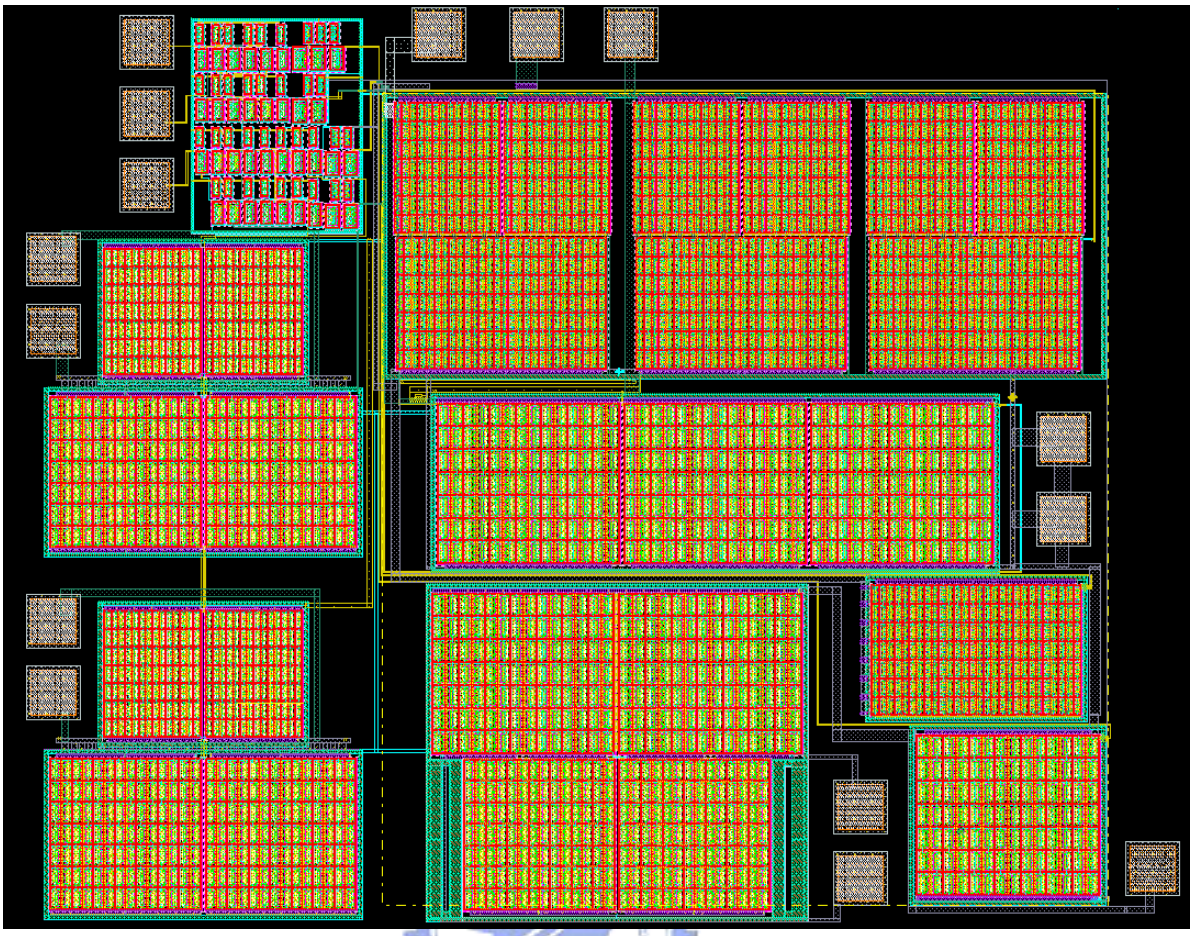


Fig. 61 Layout scheme diagram

Chapter 5

Conclusions and Future Work

5.1 Conclusions

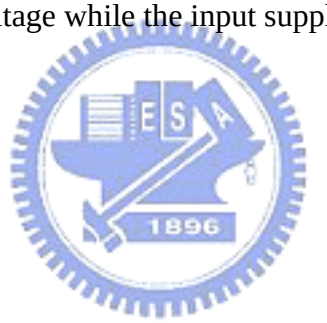
A selectable multi output DC-DC converter utilizing improved dual phase cross-coupled charge pumps is presented in this thesis. The major part of the silicon area is the power transistors. The charge pumps which are used in the circuit are also presented, including the improved cross-coupled positive charge pump, the negative cross-coupled charge pump and the negative to positive charge pump.

The work is for the applications of the LCD panels. The LCD panels need different voltage to charge and discharge the liquid crystal capacitors. In this project, the input voltage is 10V and output voltage 0V, 10V, 20V and -10V. And the output node needs to be selected to the desired voltage arbitrarily. The work is simulated with the help of the high voltage triple well process.

The improved cross-coupled charge pump with shoot-through current loss reduction is proposed and can achieve a higher voltage gain and efficiency. The proposed cross-coupled negative charge pump also achieves a high voltage gain and efficiency by reducing the reversion current loss. And the output ripples of the charge pumps are reduced by the proposed cross-coupled structures.

5.2 Future Works

The proposed selectable multi-output DC-DC converter which utilizes charge pumps in thesis can only be fabricated with the high voltage process to exceed the required voltage level. And the output voltage V_{DD} is directly from the input voltage source. Furthermore, the output voltage is changed with the input voltage without regulation. The future works of the thesis is to design multi-stage charge pumps which can operate under the low voltage process and can exceed high output voltage at the same time. The negative to positive charge pump can be added into the circuits to help the power efficiency when delivering the V_{DD} voltage level to the output terminal. The regulation circuit for the charge pumps can be added in the future to regulate the output voltage while the input supply voltage is changing.



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