國 立 交 通 大 學
電 機 與 控 制 工 程 研 究 所

碩 士 論 文

低功率數位自動增益控制及積分三角調變器應用於音頻前端電路

Low Power Digital AGC and Sigma-Delta Modulator for Audio Front-End Circuit

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中 華 民 國 九十六 年 十 月

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摘要

近年來積體電路製程進步,晶片在單位面積裡面可放進更多電晶體.,使得晶片的應用越來越廣泛.應用在音頻方面的電池裝置產品中,例如助聽器、聽診器...等等,希望所使用的晶片擁有低電壓、低面積、低功率,在這篇論文裡,實現一個應用於音頻前端電路的低電壓、低面積、低功率的數位自動控制器和積分三角調變器。

採用積分三角調變器輸出端直接迴授方式去設計一個數位自動控制器,沒有經過後級抽樣濾波器,進而可以達到節省面積、降低功率和減少自動增益控制器迴路延遲。為了降低三角積分調變器的功率消耗，使用反向器轉導運算放大器和一個全動態式比較器。為了整流積分三角調變器的輸出位元流,在此也提出了一個位元流整流器。數位類比轉換器方面,提出一個低面積循環式數位類比轉換器。

所提出的電路架構將被實現在 TSMC CMOS 0.18μm 的製程，其晶片面積為 0.347μm×0.429μm (不包含 PAD)，設計在音頻頻寬 250Hz~10kHz,操作電壓 1V,擁有 12Bit 的解析度,動態範圍 87dB。此電路系統總共的功率消耗為 42.3 uW。

索引詞彙—三角積分調變器、低電壓、低功率、自動增益控制器、可變增益放大器、數位類比轉換器。

Low Power Digital AGC and Sigma-Delta Modulator for Audio Front-End Circuit

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Abstract

IC processing technologies have a great improvement recently. There are more transistors per unit area. Therefore, applications are more and more extensive. Battery device products for audio applications, such as hearing aids, stethoscope, etc, hope circuits to operate at 1ow voltage, low area, and low power. In this thesis, a low-voltage low-area low-power digital automatic gain control (AGC) with a sigma-delta modulator for audio front-end circuit is realized.

This thesis utilizes a direct feedback at the sigma-delta modulator output to design the digital AGC. It does not go through a decimation filter. Thus it decreases the area, power consumption, and latency of the AGC loop. To decrease the power consumption of the modulator, inverter operational transconductance amplifiers (OTA) are used and a pure dynamic comparator is designed. To rectifier a bit stream of the modulator output, a bit-stream rectifier is presented. In terms of digital to analog converter, a low area recurring DAC is presented.

The proposed circuit is designed in TSMC 1P6M 0.18 μm CMOS process. Its active die area is $0.347\mu m \times 0.429\mu m$. The signal bandwidth is designed in an audio bandwidth from 250Hz to 10 kHz, and the resolution is 12bit. The dynamic range(DR) is 87dB. The supply voltage is 1.0V. The total power consumption of the proposed circuit is 42.3 μW.

Index Terms – sigma-delta modulator, low-voltage, low-power, automatic gain control, variable gain amplifier, digital to analog converter.

誌謝

在此要感謝我的父母，讓我無後顧之憂的完成學業。。不管是在學業上或是其它方面更能專注的學習。

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在此還要感謝一起在實驗室的學長、同學、學弟及助理們。很謝謝煜輝、盈杰、丸子、鴻文、仁乾學長们對事情追根究底的態度以及對自己理想以及興趣付出的神情。以及祥哥、教主、snoopy、忠傑、方董、小馬、賢哥、小潘潘、存遠大家面對人生的選擇、態度都讓我獲益良多。讓我這兩年來，過的相當充實，也學到很多。

王村鑫

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Chapter 1

Introduction

1.1 Motivation

In recent years, IC processing technologies have such a great improvement on dimension scaling down that many applications are realized. In terms of audio applications, rapid expansion of the biomedical-electronic and consumer-product market has necessitated low-power low-voltage low-area systems. Since the battery power is used for these devices, expanding the battery lifetime with low-power dissipation is very crucial. However, the threshold voltage is not scaled down linearly with the dimension. It increases the difficulty of the low voltage design. According to the power consumption law, the power is in proportion to the square of the supply voltage. In order to design low power circuit, the low voltage design is necessary.

The sound is a wide-dynamic-range signal. In order to obtain the input signal with wide-dynamic range, an AGC designed in front-end is necessary. The AGC makes a small input signal be amplified or a large input signal be reduced. Thus, the dynamic range of the AGC output is smaller than the input's. Therefore, the AGC makes next circuits obtain signal easily. In this thesis, a digital AGC is designed. The

digital AGC does not design the loop filter by off-chip capacitors and is programmable. The latter is very important especially for hearing aids. Many hearing loss people have different the dynamic ranges of hearing. So AGC needs to be programmed particularly for different hearing loss people.

Sigma-delta modulators are insensitive to circuit imperfection and less complicated in analog circuits. The modulators are widely used in high-precision low-bandwidth applications, such as audio system. In order to power saving, this thesis uses inverter OTAs and a pure dynamic comparator to design a sigma-delta modulator.

In the thesis, a digital AGC with a sigma-delta modulator for audio front-end circuit is realized. It has a resolution 12 bit and consumes only 42.3 μW .

1.2 Basic Concepts of Audio System

AGC circuits are used in many audio applications, such as hearing aids, stethoscope, record pen, etc. Currently, the AGC circuits are roughly classified as either analog or digital circuits. The conventional analog AGCs are designed with a particular loop bandwidth based on particular audio applications. The Digital AGCs has the most features than the analog ones. Their loop coefficients are redesigned easily by DSP, but the analog AGCs need to use off-chip capacitors. The tuning range of the gain of the digital AGCs is also redesigned easily by DSP. Furthermore, the digital AGCs do not use off-chip capacitors to design filters and integrators. So they have smaller area than the analog ones.

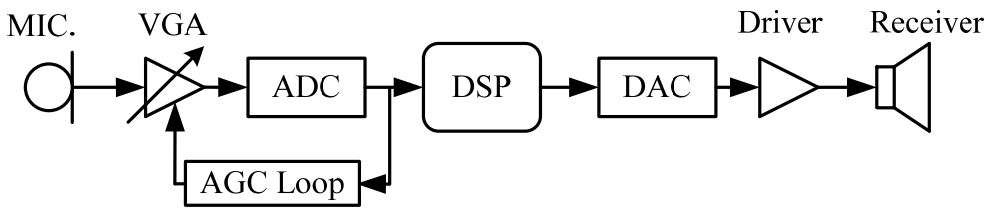


Figure 1-1 Audio system with a digital AGC

Figure 1-1 shows a audio system with a general digital AGC. The VGA is an amplifier which the gain is controlled by the AGC loop. To make the AGC loop bandwidth be independent of the signal levels, an exponential gain control characteristic is required for the VGA. The AGC prevents a large signal from

overloading the A/D converter and generating distortion. The digital signal processor (DSP) receives the output of the A/D converter and performs signal-processing algorithm. The output of DSP is converted to an analog signal by the D/A converter. Finally, the analog signal is transferred to receiver by the driver circuit which usually is a Class-D circuit.

In order to provide a high resolution signal for DSP, the A/D converter is designed by a sigma-delta modulator in the audio system. This thesis presents a low-voltage low-power low-area sigma-delta modulator for the audio system. To be programmable, a digital AGC is designed. The proposed digital AGC architecture has lower area, power, and latency than the traditional digital AGCs.

1.3 Thesis Organization

This thesis is organized into five chapters. In Chapter 1, this thesis and the audio system are briefly introduced. In Chapter 2, the basic concepts of AGC and the fundamentals of a single loop and dual loop AGC are all introduced. The linear model and the equivalent transfer function of AGC are also derived. Finally, the basic architecture and advantages of a digital AGC are introduced.

In Chapter 3, the fundamentals of a sigma-delta modulator are introduced and a single-loop third-order sigma-delta modulator for audio applications is designed. First, the z-domain model of the proposed modulator is derived. Then, the parameters are determined by the z-domain model. In terms of circuit, an inverter OTA with swing improvement, a pure dynamic comparator, and some low voltage techniques are also introduced. Finally, the simulation results of the modulator are presented.

In Chapter 4, the proposed dual loop digital AGC system is introduced. First, the specifications of the AGC are determined. The parameters of the AGC are derived by Matlab. Then, digital circuits, a variable gain amplifier (VGA), and a DAC are designed for the proposed AGC. Finally, the layout and the performances of the AGC are also presented in this chapter.

In Chapter 5, conclusions and future works are described.

Chapter 2

Fundamentals of

Automatic Gain Control

2.1 Introduction

The fundamentals of AGC will be reviewed in this chapter. In Section 2.2, we introduce a single loop AGC system and the definitions of the attack time and the release time for audio systems. The linear model and the equivalent transfer function of the AGC are also introduced. In Section 2.3, a dual loop AGC system is introduced. In Section 2.4, the system architecture and the advantages of a digital AGC are discussed.

2.2 Single loop AGC

Single loop AGC architecture

The traditional single loop AGC architecture is shown in Figure 2-1 [5]. It includes a VGA, a gain and buffer stage, an average detector, and an integrator. The role of the AGC is to amplify a small input signal or decrease a large input signal. It prevents the signals being saturated efficiently especially for signals with high

dynamic range. Therefore, next stage circuits obtain the signals easily. The average detector calculates the average value of the output signal magnitude to represent a signal amplitude. Then it is subtracted from V_{ref}. Finally, the integrator circuit, obtained the difference value, generates a control signal to control the gain of the VGA. The gain and buffer stage offers the ability to drive next circuit. It also amplifies the output signal of the VGA.

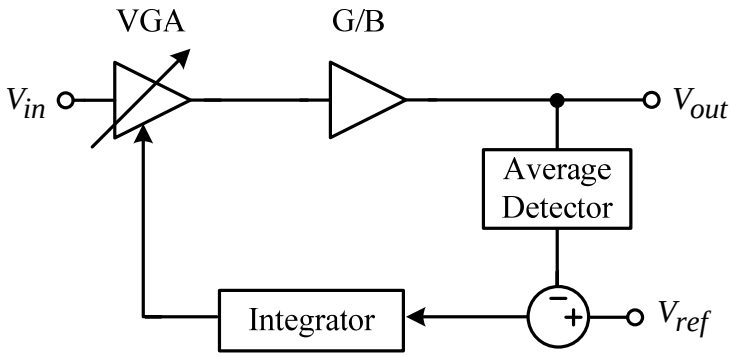


Figure 2-1 Single loop AGC

The static characteristic of the AGC is shown in Figure 2-2 [6]. The input signal is amplified linearly until it exceeds the input threshold level A. Input levels above the threshold are limited to the output level B.

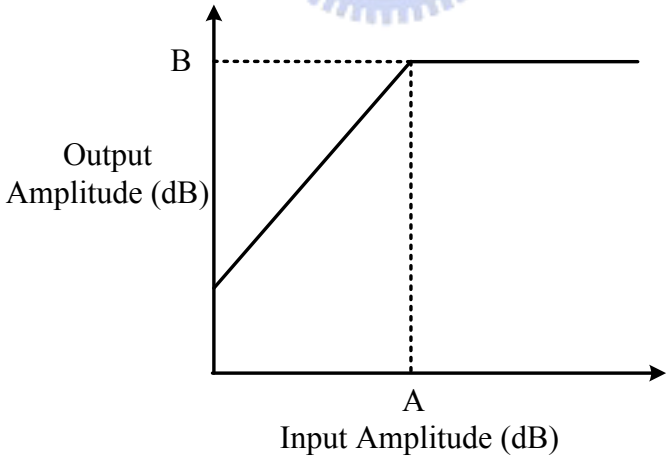


Figure 2-2 AGC static characteristic

Attack time and Release time

When the input signal is changed suddenly, AGC needs to spend some time to settle the output signal. The time is described as the attack time and the release time,

shown in Figure 2-3.

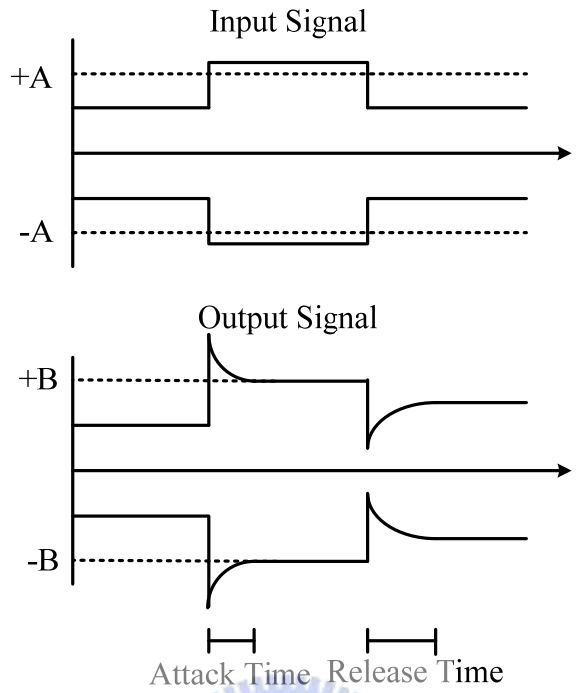


Figure 2-3 AGC dynamic characteristic

The attack time is defined as the time needed to respond to a sudden 25 dB increase of the input signal until the output signal is within 2 dB from its final value. This is in the order of a few milli-seconds. In this way, a sudden loud will not create discomfort for users.

The release time is defined as the time needed to respond to a sudden 25 dB decrease of the input signal until the output signal is within 2 dB from its final value. The release time is much longer so that the gain variations of AGC do not disturb the sound sensation. On the other hand, if release time is too long, a sudden impulse may offset the gain for a long period of time, with consequent loss of speech information.

In order to have better the intelligibility of speech, the attack time and the release time must be carefully controlled. The attack time is usually less than 5ms and the release time is about 50 ms [7].

Linear model of the single loop AGC

VGA

VGA is a block that the gain is controlled by a control voltage. In general, the relationship between the gain and the control voltage is linear or exponential. The function of the linear gain control type is represented as

$$V_O(V_C) = \beta V_C V_{in}. \tag{2.1}$$

The derivative of (2.1) with respect to V_C is rewritten as.

$$K_{VGA} = \frac{dV_O}{dV_C} = \beta V_{in}. \tag{2.2}$$

The function of the exponential gain control type is represented as

$$V_O(V_C) = \beta e^{\alpha V_c} V_{in}. \tag{2.3}$$

The derivative of (2.3) with respect to V_C is rewritten as

$$K_{VGA} = \frac{dV_O}{dV_C} = \alpha\beta e^{\alpha V_c} V_{in} = \alpha V_O. \tag{2.4}$$

Form (2.2) and (2.4), we know that K_{VGA} of (2.4) is independent of the input signal V_{in}. The system bandwidth is not affected by the input signal. So the exponential gain control type has better performance than the linear one.

Average Detector

The average detector includes a rectifier and a low pass filter. It is shown in Figure 2-4. The output signal of the rectifier is an absolute signal of the input signal. The low-pass filter averages the absolute signal at dc. If the input signal is a sine wave, the equivalent gain of the average detector is represented as

$$K_{AD} = \frac{1}{\pi}\int_0^{\pi} \left|\sin(\theta) d\theta\right| = \frac{2}{\pi} \tag{2.5}$$

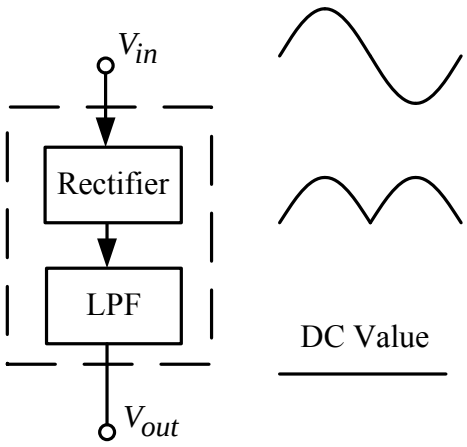


Figure 2-4 Average detector

The liner model of Figure 2-1 is shown in Figure 2-5. K_{VGA} is the small signal

gain of the VGA. The gain is between V_c and V_o. K_{GB} is the gain of the gain and buffer stage. K_{AD} and $p_1/(s+p_1)$ are represented as the average detector gain and the low-pass filter transfer function, respectively. The transfer function of the integrator is ω_u / s where ω_u is a unity gain frequency.

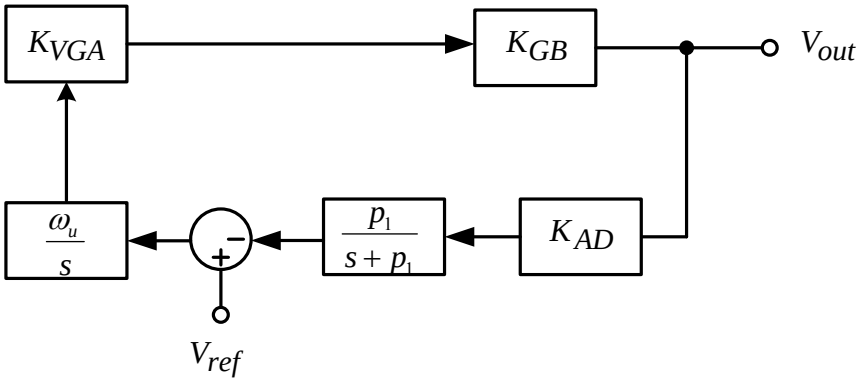


Figure 2-5 Linear model of the single loop AGC

In Figure 2-5, the forward path gain is represented as

$$A = \frac{\omega_u}{s} \times K_{VGA} \times K_{GB} . \tag{2.6}$$

The feedback path gain is represented as

$$f = \frac{p_1 K_{AD}}{s+p_1} . \tag{2.7}$$

From (2.6) and (2.7), the transfer function between V_{ref} and V_{out} is given by

$$\frac{V_{out}}{V_{ref}} = \frac{A}{1+Af} = \frac{K_{VGA}K_{GB}\omega_u(s+p_1)}{s^2 + p_1 s + K_{VGA}K_{GB}\omega_u K_{AD} p_1} \tag{2.8}$$

2.3 Dual loop automatic gain control

Dual loop AGC architecture

The attack time and the release time must be different for many audio applications. A single loop AGC does not achieve this property. Therefore, a dual loop AGC is a better choice for audio applications. It is shown in Figure 2-6 [8]. This architecture includes additionally a comparator, a MUX, and an integrator from the single loop AGC. When an input single becomes large suddenly, the comparator output will obtain zero. The single path will through the integrator (a), which has a larger unity gain frequency. Thus, the gain of the VGA is decreased fast. When an input single

becomes small suddenly, the comparator output will obtain one. The single path will through the integrator(r), which has such a smaller unity gain frequency that the gain of the VGA is amplified slowly. Furthermore, another advantage of the dual loop AGC is that the control voltage of the VGA in steady state changes so slowly that it obtains a noise-less output signal.

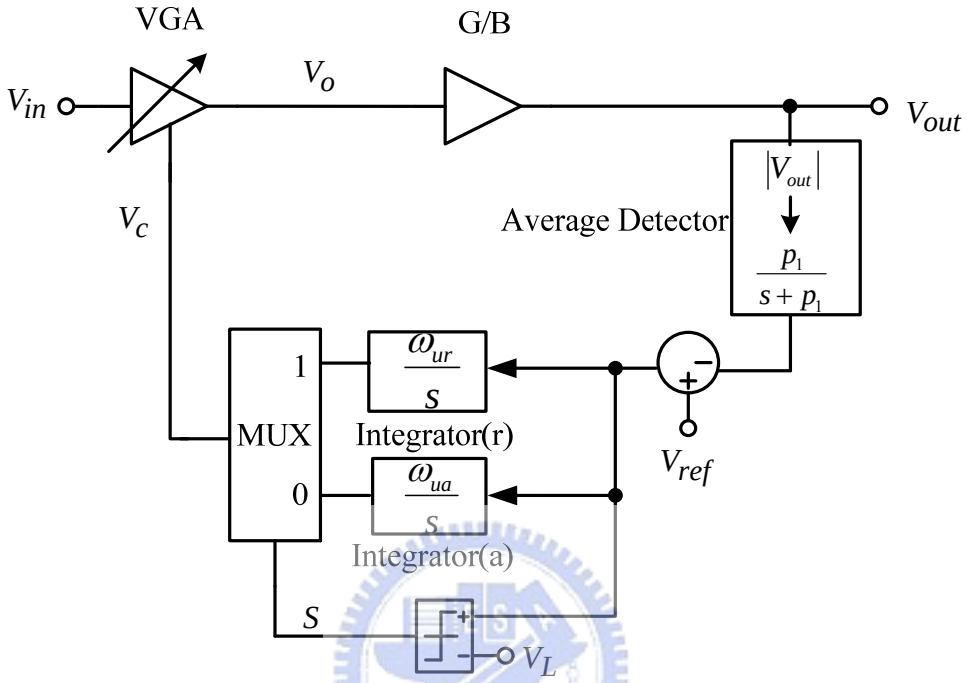


Figure 2-6 Dual loop AGC

Linear model of the dual loop AGC

Figure 2-7 is the linear model of Figure 2-6. It is different from the linear model of the single loop AGC, which is a new integrator linear model. S is the comparator output signal and mainly selects the wide or narrow bandwidth path. The forward path gain is represented as

$$A = (S\omega_{ur} + \bar{S}\omega_{ua}) \times K_{VGA} \times K_{GB} \tag{2.9}$$

and the feedback path gain is represented as

$$f = \frac{p_1 K_{AD}}{s + p_1}. \tag{2.10}$$

Form (2.9) and (2.10), the transfer function between V_{ref} and V_{out} is derived as

$$\frac{V_{out}}{V_{ref}} = \frac{A}{1 + Af} = \frac{K_{VGA}K_{GB}(S\omega_{ur} + \bar{S}\omega_{ua})(s + p_1)}{s^2 + p_1 \times s + K_{VGA}K_{GB}(S\omega_{ur} + \bar{S}\omega_{ua})K_{AD}p_1} \tag{2.11}$$

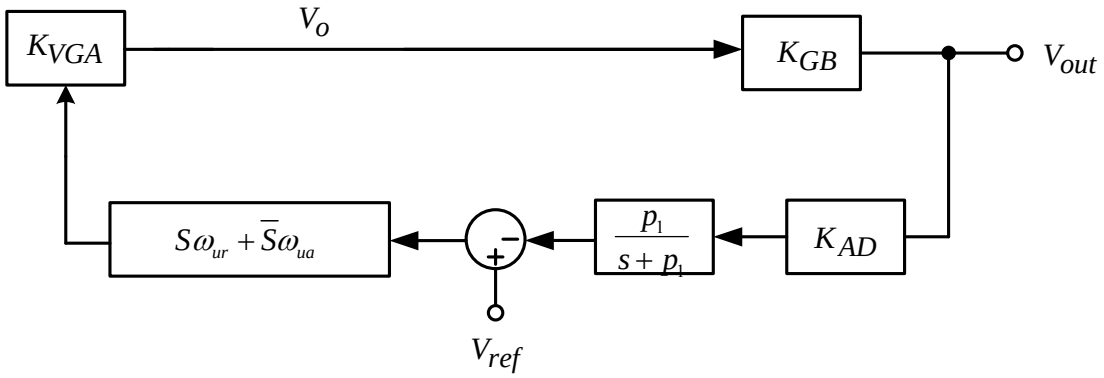


Figure 2-7 Linear model of the dual loop AGC

2.4 Digital automatic gain control

Digital AGC architecture

A digital AGC is shown in Figure 2-8. It is different from analog AGCs. It adds an ADC and a DAC. The average detector and the integrator become digital circuits. The output signal of the gain and buffer stage is converted to a digital code by the ADC. At the output end, the output signal is pulled back into the peak detector to detect the output signal. Then, it goes through the subtractor and the integrator. Finally, the output code of the integrator controls the DAC. The DAC will generate a analog signal. The gain of the VGA is changed by this analog signal. The digital AGC does not design the average detector and the integrator by off-chip capacitors. It is also programmable and its system coefficients are controlled by DSP.

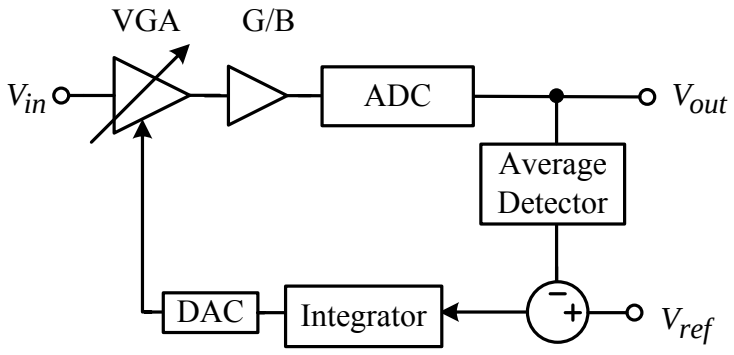


Figure 2-8 Digital AGC architecture

2.5 Summary

AGC is employed in many systems where the input signals have a wide dynamic range. The role of AGC is to provide a relatively constant output amplitude. Thus, circuits following AGC require less dynamic range and obtain singles easily. To have the settling time of AGC independent of the input signal, VGA designed with exponential gain control is necessary. To achieve different settling times, the attack time and the release time, this thesis uses a dual loop AGC architecture. It allows a signal to go through different bandwidth paths. In order to decrease area and have flexibility, a digital AGC is designed in this thesis.

Chapter 3

The Proposed Low-Voltage Low-Power Sigma-Delta Modulator

3.1 Introduction

Form Figure 2-8, we know that an ADC is needed in the design of digital AGC. A sigma-delta modulator ADC is designed for the ADC of the proposed digital AGC. In this chapter, the structure of the proposed 12-bit low-power third-order sigma-delta modulator with 20 kHz bandwidth is presented. The fundamentals of the modulator are introduced in Section 3.2. Section 3.3 introduces an inverter OTA with swing improvement and an integrator with the inverter OTA. In Section 3.4, the system design methods of the modulator are described. In Section 3.5, the circuit design techniques of the modulator are introduced.

3.2 Fundamentals of Sigma-Delta Modulator

Quantization noise and Oversampling technique

A 1-bit quantizer is the heart of single-quantizer sigma-delta modulators. The analysis of the behavior of a sigma-delta modulator must include the behavior of the quantizer. Since the quantizer is a nonlinear element, the analysis is complicated even in a simple system. Before the analysis, the quantizer is modeled as the linear model shown in Figure 3-1. The signal $e(n)$ is the adding quantization error, which is the difference between the input and output signals. The linear model is valid as long as the quantization error, *e(n)*, is an independent white-noise signal[1].

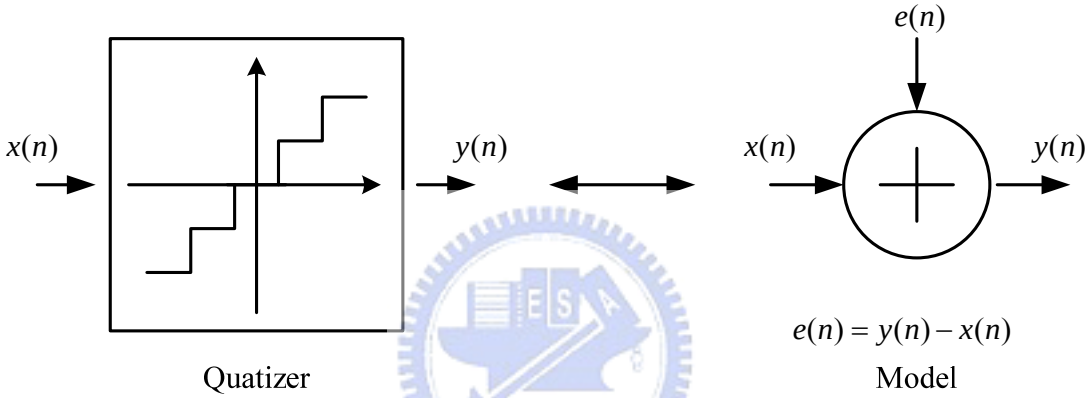


Figure 3-1 Quantizer and its linear model

At the beginning, the quantization error, *e(n)*, is assumed to be an independent random number with a uniform distribution. The signal *e(n)* uniformly distribute between $\pm\Delta/2$, where Δ is the difference between two adjacent quantization levels. Figure 3-2 is the power spectral density (PSD) of the quantization noise, *e(n)*.

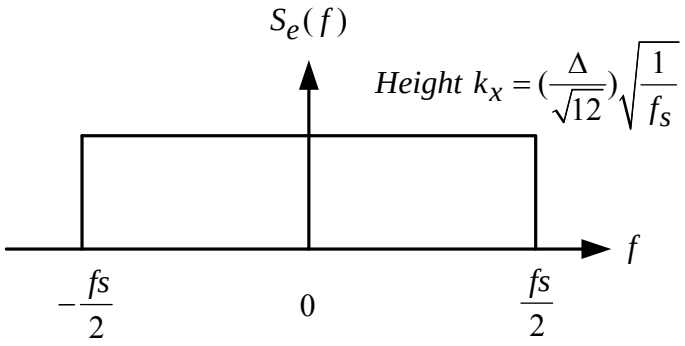


Figure 3-2 PSD of the quantization noise

The total noise power is $\Delta^2/12$ and f_s is the sampling frequency. With a two-sided definition of power, the area under $S_e(f)$ within $\pm\frac{f_s}{2}$ is equal to the total noise power. The total noise power is calculated as

$$\int_{-f_s/2}^{f_s/2} S_e^2(f)df = \int_{-f_s/2}^{f_s/2} k_x^2 df = k_x^2 f_s = \frac{\Delta^2}{12}. \tag{3.1}$$

Solving (3.1), k_x equals $\left(\frac{\Delta}{\sqrt{12}}\right)\sqrt{\frac{1}{f_s}}$ [1].

Oversampling means that the sampling frequency exceeds Nyquist frequency. In other words, the sampling frequency is greater than twice the signal bandwidth. And the oversampling ratio (*OSR*) is defined as

$$OSR = \frac{f_S}{2f_B}. \tag{3.2}$$

For a sinusoidal input signal, the maximum signal power is a square of the RMS voltage ($2^N\left(\Delta/2\sqrt{2}\right)$) and is rewritten as

$$P_S = \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8} \tag{3.3}$$

For an oversampling system, the input signal with a frequency below the bandwidth (f_B) pass through the low-pass filter without any decay. But, the out-of-band quantization noise is filtered out, shown in Figure 3-3. Thus, the quantization noise power is obtained as

$$P_Q = \int_{-f_s/2}^{f_s/2} S_e^2(f)\times|H(f)|^2 df = \int_{-f_B}^{f_B} S_e^2(f)df$$

$$= 2f_B \times \frac{\Delta^2}{12}\frac{1}{f_S} = \frac{\Delta^2}{12}\times\left(\frac{1}{OSR}\right). \tag{3.4}$$

It is found that the quantization noise power is reduced half or equivalently 3dB as the OSR is doubled. The maximum SNR value is calculated as follows by (3.3) and (3.4).

$$SNR = 10\log\left(\frac{P_S}{P_Q}\right) = 10\log\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2}{12}\cdot\left(\frac{1}{OSR}\right)}\right) = 10\log\left(\frac{3\cdot 2^{2N}\cdot OSR}{2}\right)$$

$$= 10\log\left(2^{2N}\right) + 10\log\left(\frac{3}{2}\right) + 10\log\left(OSR\right)$$

$$= 6.02N + 1.76 + 10\log\left(OSR\right) \tag{3.5}$$

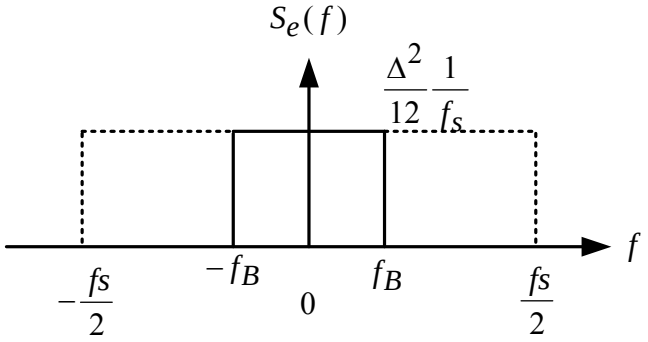


Figure 3-3 Quantization noise PSD after low-pass filter.

The oversampling technique has an improvement of 3dB/octave or 0.5-bit/octave. In other words, if the oversampling ratio is increased by a factor of 4, the resolution is improved by one bit. Thus, increasing the OSR improves the SNR. However, the oversampling is not an attractive way because the higher sampling frequency and the linearity are required severely for high resolution ADCs. Hence, the noise-shaped method will be introduced. It provides a reasonable oversampling frequency to achieve a much higher dynamic range.

First-order Noise shaping

The architecture of a first-order sigma-delta modulator is shown in Figure 3-4. The first-order modulator contains a integrator, a 1-bit quantizer, and a 1-bit DAC used for the feedback. In Figure 3-4(b), the z-domain linear model of the first-order modulator is presented [4]. According to the linear model, the signal transfer function(STF) and the noise transfer function(NTF) are derived as follows.

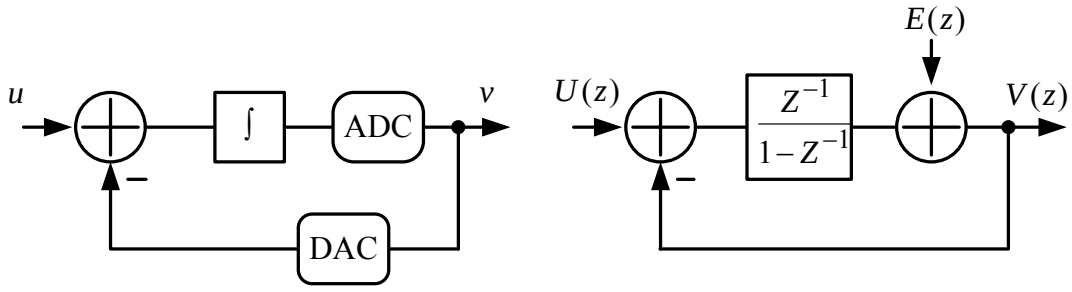
$$V(z) = \frac{Z^{-1}}{1-Z^{-1}}(U(z) - V(z)) + E(z)$$

$$V(z) = Z^{-1}U(z) + (1-Z^{-1})E(z) \tag{3.6}$$

(3.6) is written in the general form as

$$V(z) = STF(z)U(z) + NTF(z)E(z). \tag{3.7}$$

Comparing to (3.6), the first-order modulator has the signal transfer function (STF) of $STF(z)=Z^{-1}$ and the noise transfer function (NTF) of $NTF(z)=1-Z^{-1}$.



(a) (b)

Figure 3-4 (a) Topology of 1st-order sigma-delta modulator, (b) z-domain linear model

Let $Z=e^{j\omega T}=e^{j2\pi f/f_s}$, the noise transfer function is written as

$$NTF(f)=1-e^{-j2\pi f/f_s}=\frac{e^{j\pi f/f_s}-e^{-j\pi f/f_s}}{2j}\times 2j\times e^{-j\pi f/f_s}$$

$$=\sin\left(\frac{\pi f}{f_s}\right)\times 2j\times e^{-j\pi f/f_s}. \tag{3.8}$$

Take the magnitude of the noise transfer function, we have

$$\left|NTF(f)\right|=2\sin\left(\frac{\pi f}{f_s}\right). \tag{3.9}$$

Based on the above assumption, the quantization noise power over the frequency band from $-f_B$ to f_B is given by

$$P_e=\int_{-f_B}^{f_B}S_e^2(f)\left|NTF(f)\right|^2df=\int_{-f_B}^{f_B}\left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2df. \tag{3.10}$$

When $f_B<<f_s$, $\sin\left((\pi f)/f_s\right)$ approximates $(\pi f)/f_s$. (3.10) is recalculated as

$$P_e\approx\left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{f_B}{f_s}\right)^3=\frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3. \tag{3.11}$$

The maximum signal power is the same as that obtained before in (3.3), the maximum SNR for this case is given by

$$SNR = 10\log(\frac{P_S}{P_e}) = 10\log(\frac{3}{2}2^{2N}) + 10\log(\frac{3}{\pi^2}(OSR)^3) \tag{3.12}$$

or, equivalently,

$$SNR = 6.02N + 1.76 - 5.17 + 30\log(OSR). \tag{3.13}$$

From (3.13), it shows that the *SNR* increases by 9 dB for each doubling of the *OSR* [4].

High-order Noise shaping

In a sigma-delta modulator, the order of noise transfer function determines how much the noise is placed outside the signal frequency band. The high-order signal and noise transfer functions are derived by the similar method. Thus, the general form for the output of the Lth-order noise-shaping modulator is given by

$$Y(z) = U(z)\cdot z^{-L} + E(z)\cdot\left(1-z^{-1}\right)^L. \tag{3.14}$$

The quantization noise power in the signal frequency band is derived as

$$P_Q = \int_{-f_B/2}^{f_B/2} S_Q(f)\cdot\left|H(f)\right|^2 df = \int_{-f_B}^{f_B}\left(\frac{\Delta^2}{12}\cdot\frac{1}{f_S}\right)\cdot\left(2\sin\left(\frac{\pi f}{f_S}\right)\right)^{2L} df$$

$$= \frac{2^{2L}\times\Delta^2}{12}\times\frac{1}{f_S}\int_{-f_B}^{f_B}\left(\frac{\pi f}{f_S}\right)df = \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^{2L}}{2L+1}\right)\left(\frac{2f_B}{f_S}\right)^{2L+1}$$

$$= \frac{\Delta^2}{12}\frac{\pi^{2L}}{2n+1}\left(\frac{1}{OSR}\right)^{2L+1}. \tag{3.15}$$

Thus, the maximum SNR for the Lth-order modulator is

$$SNR = 10\log\left(\frac{P_S}{P_Q}\right) = 10\log\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2}{12}\frac{\pi^{2L}}{2n+1}\left(\frac{1}{OSR}\right)^{2L+1}}\right)$$

$$= 10\log\left(2^{2N}\right) + 10\log\left(\frac{3}{2}\right) + 10\log\left(\frac{2L+1}{\pi^{2L}}\right) + 10\log\left(OSR^{2L+1}\right)$$

$$= 6.02N + 1.76 + 10\log\left(\frac{2L+1}{\pi^{2L}}\right) + (20L+10)\log(OSR). \tag{3.16}$$

The above equation shows that an Lth-order noise-shaping modulator improves the SNR by 6L+3 dB as doubling the OSR, or equivalently L+0.5 bits/octave.

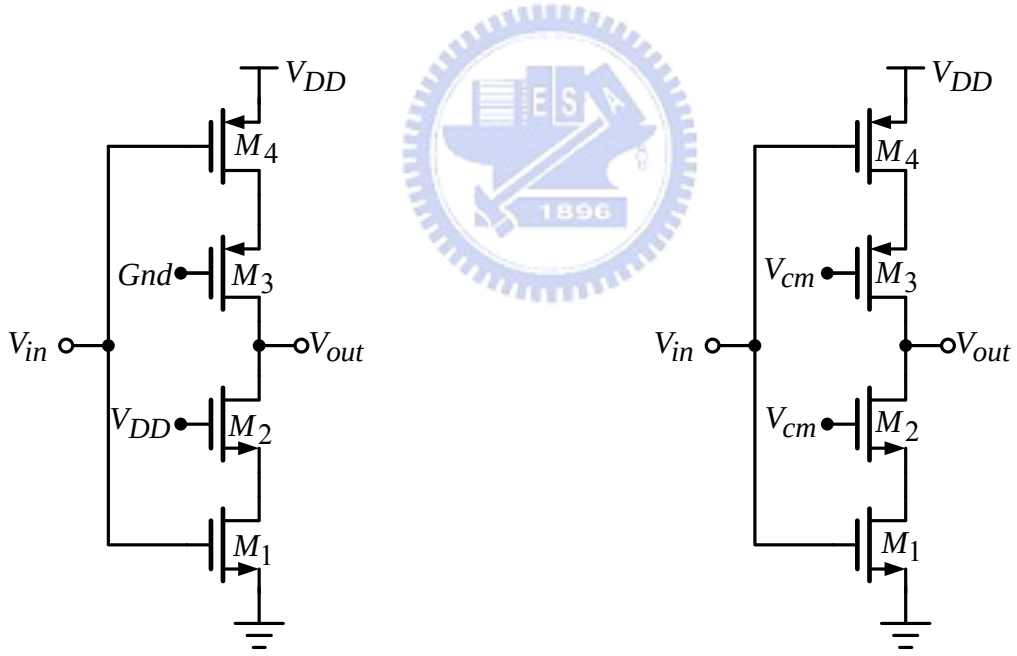
However, the high-order sigma-delta modulator has a system stability issue.

3.3 Integrator with inverter OTA

Inverter OTA

The major building block in switched-capacitor sigma-delta modulator is OTA which forms a negative feedback loop. To decrease the power consumption and the area, the inverter OTA, shown in Figure 3-5, is used in this thesis. Area wise, it is a simple circuit and needs only one current path. So the area is smaller than the traditional OTAs. Power wise, it is a class-AB structure and its g_m is four times as much as the traditional OTAs' at the same current. Thus the inverter OTA has a higher power efficiency. The gain of the inverter OTA is increased by the cascode method. The gain of Figure 3-5 (a) and (b) all are represented as

$$Gain = (g_{m1} + g_{m4})(g_{m2} ro_2 ro_1 \parallel g_{m3} ro_3 ro_4) . \quad (3.17)$$



(a) (b)

Figure 3-5 Inverter OTA (a) Biased in saturation (b) Biased in weak inversion

Figure 3-5 has two different bias methods. In Figure 3-5 (a) [9], transistors M_2 and M_3 are biased in saturation at a supply voltage 1V in TSMC 0.18 μm CMOS technology. Its swing is obtained as

$$(Gnd + V_{thp}) - (V_{DD} - V_{thn}) = V_{thp} + V_{thn} - V_{DD} . \quad (3.18)$$

In Figure 3-5 (b), transistors M_2 and M_3 are biased in weak inversion. Its swing is obtained as

$$(V_{cm}+V_{gs3}-100mV)-(V_{cm}-V_{gs2}+100mV)$$

$$=V_{gs3}+V_{gs2}-200mV\,. \tag{3.19}$$

At the supply voltage of 1V, the former swing is about 100mV and the latter swing is about 500mV. Figure 3-5 (b) has a larger swing. It is very important for switched-capacitor circuits due to have the wide linear range at the output. So it is used in this thesis.

Integrator

Figure 3-6 shows the switched-capacitor integrator with the inverter OTA , which the gain is finite. The threshold voltage of the inverter OTA is easily changed by the process variation. So the switched-capacitor integrator must utilize the correlated double sampling (CDS) [10] technique to decrease this effect.

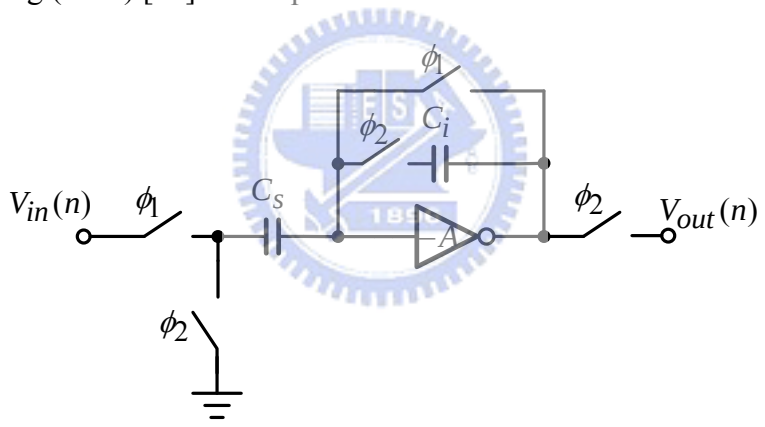


Figure 3-6 Integrator with inverter OTA

The total charge in capacitors C_S and C_i during $\phi_1=1$ is

$$(\mathrm{V_{IN}}(n-\frac{1}{2})-V_{off})C_S+(\mathrm{V_{out}}(n-1)-(V_{off}-\frac{\mathrm{V_{out}}(n-1)}{A}))C_i \tag{3.20}$$

where V_{off} is the offset voltage of the inverter OTA due to that its threshold voltage is not $V_{DD}/2$ and A represents the finite gain of the inverter OTA. The total charge in C_S and C_i during $\phi_2=1$ is

$$-(V_{off}-\frac{\mathrm{V_{out}}(n)}{A})C_S+(\mathrm{V_{out}}(n)-(V_{off}-\frac{\mathrm{V_{out}}(n)}{A}))C_i\,. \tag{3.21}$$

(3.21) and (3.22) have the same charge due to the law of conservation of charge. It is

represented as

$$(V_{IN}(n-\frac{1}{2})-V_{off})C_S+(V_{out}(n-1)-(V_{off}-\frac{V_{out}(n-1)}{A}))C_i$$

$$=-(V_{off}-\frac{V_{out}(n)}{A})C_S+(V_{out}(n)-(V_{off}-\frac{V_{out}(n)}{A}))C_i\,. \qquad (3.22)$$

Finally, (3.22) is simplified as

$$\frac{V_{out}(Z)}{V_{in}(Z)}=\frac{(\frac{A}{A+1})\frac{C_S}{C_i}Z^{-\frac{1}{2}}}{\frac{\frac{C_S}{C_i}}{(A+1)}+1-Z^{-1}}\,. \qquad (3.23)$$

It shows that the finite gain affects the gain and the pole of the integrator. When the gain is large, the finite gain effects will be ignored. So an enough gain of the integrator is very important for circuit designs. The ratio of C_S and C_i is also have the same effects.

3.4 The System Design of Third-Order Sigma-Delta Modulator

Circuit Architecture

In this thesis, a third-order sigma-delta modulator is designed because it has less idle tone. The circuit architecture of the third-order sigma-delta modulator with the inverter OTAs is shown in Figure 3-7. The last stage circuit has a fully-differential output signal. To obtain a larger input dynamic range, the fully-differential input signal is directly sampled by the sampling capacitor C_1. The dynamic range is doubled and the value of C_1 becomes one fourth. The input signal needs to go through a constant gain circuit before the input signal is sampled. The constant gain circuit is realized by C_1. The constant gain circuit does not need to be designed additionally. The gain is 3 in this design.

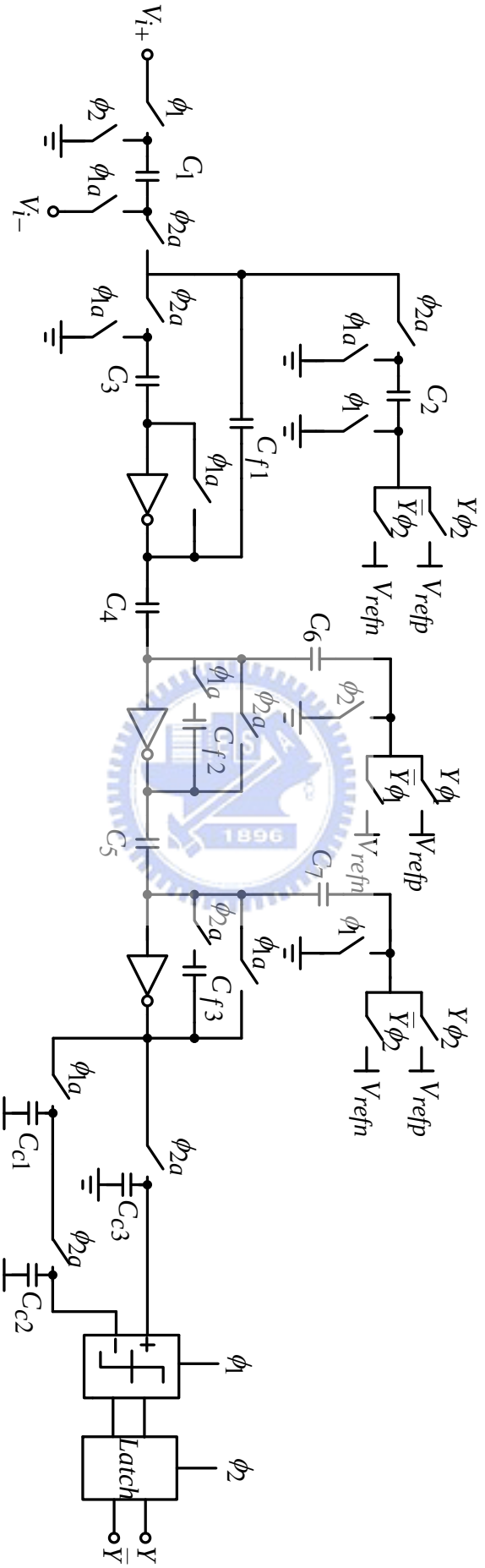


Figure 3-7 The proposed third-order sigma-delta modulator

The z-domain model of the sigma-delta modulator

In order to design coefficients of the sigma-delta modulator, the equivalent z-domain model must be obtained first. The quantizer costs one clock delay and integrators cost one half clock delay, form (3.23),. Using these properties, the circuit of Figure 3-7 is transferred to the z-domain model, shown in Figure 3-8 where Q_e represents the quantization noise and the value 3 is the constant gain. The rearrangement of Figure 3-8 obtains Figure 3-9. It has only one-clock-delay integrators such that it is easier to be simulated by Matlab.

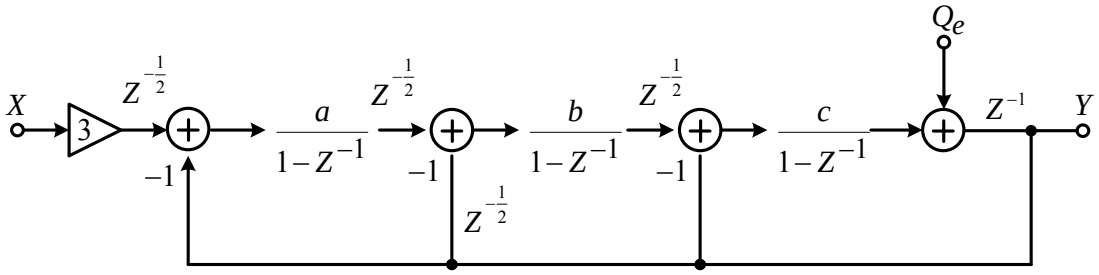


Figure Figure 3-8 Equivalent z-domain model of the sigma-delta modulator

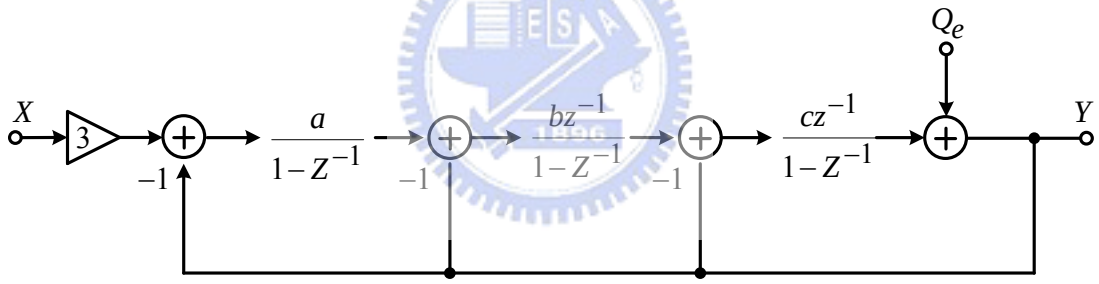


Figure 3-9 Simplification of the z-domain model

Determine OSR

From Figure 3-9, the noise transfer function is derived as

$$\mathrm{NTF(z)}=\frac{\mathrm{Y(z)}}{\mathrm{Q_e(z)}}=\frac{(z-1)^3}{z^3+(c-3)z^2+(abc+bc-2c+3)z-bc+c-1}. \qquad (3.24)$$

Firstly, the NTF, a high-pass filter, needs to be designed. The high-order sigma-delta modulator has a stability problem. So Lee's criterion [4], which means the maximum gain of the NTF must be less than 1.5, is used in this design. The NTF with a pass-band edge at 150 kHz, designed by Butterworth, is represented as

$$\mathrm{NTF(z)}=\frac{\mathrm{Y(z)}}{\mathrm{Q_e(z)}}=\frac{(z-1)^3}{z^3-2.25z^2+1.756z-0.4683}. \qquad (3.25)$$

Its maximum gain is 1.461 which it is less than 1.5. Using (3.25) to calculate the parameters of (3-24), $a = 0.173$, $b = 0.291$, and $c = 0.75$ are obtained. In order to improve the capacitor matching, capacitors must be designed by unit capacitors. So the parameters are redesigned as $a = 1/5$, $b = 2/7$, and $c = 3/4$. The maximum gain of the NTF is 1.462. The poles and zeros plots are shown in Figure 3-10.

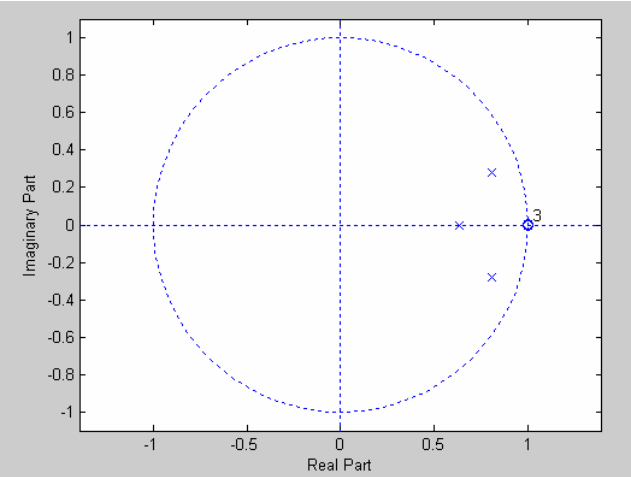


Figure 3-10 Pole-zero plot for the NTF

In order to obtain 12-bit resolution, the OSR must be determined by Matlab. When the OSR is 64, FFT spectrum of the sigma-delta modulator is obtained in Figure 3-11. The signal bandwidth is 20 kHz. When the input frequency and amplitude are 5.625 kHz and 0.1V, respectively, it shows that the sigma-delta modulator has the ENOB of 13.1 bit.

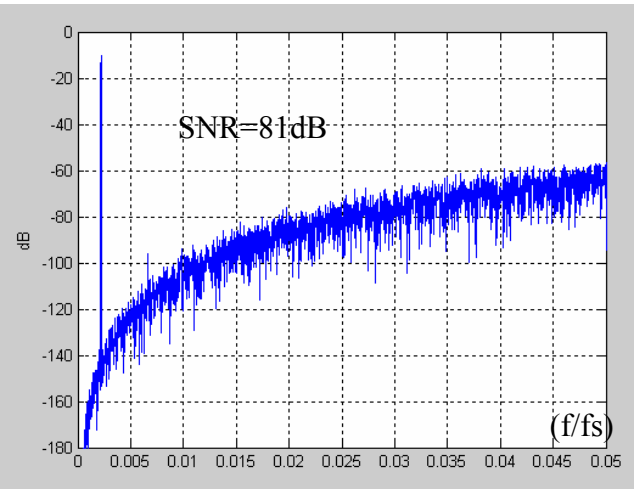


Figure 3-11 FFT spectrum of the sigma-delta modulator

The dynamic range (DR) of the sigma-delta modulator is shown in Figure 3-12. It

shows that the DR is 90dB.The peak SNR of 81dB occurs at the input amplitude of 0.1V.

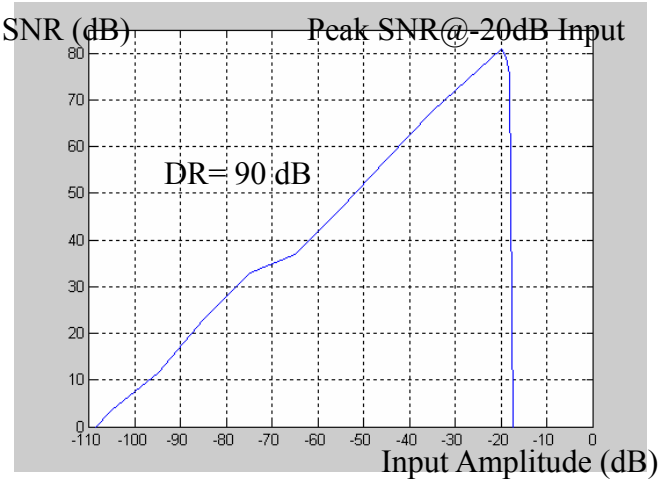


Figure 3-12 Dynamic range of the sigma-delta modulator

Finite gain effect of inverter OTA

The integrators of the sigma-delta modulator shown in Figure 3-9 are modeled by (3.23). The A factor represents the gain of the inverter OTAs. When the gain is only considered, the effect of the finite gain A on the SNR is obtained in Figure 3-13. In order to obtain enough SNR, the gain must be larger than 50 at least.

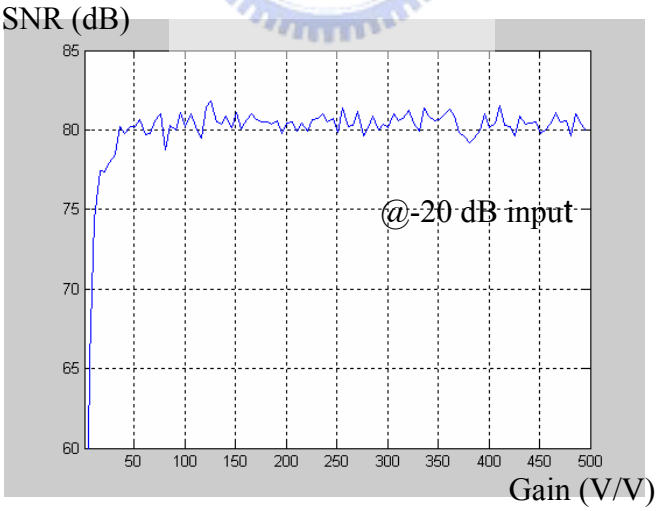


Figure 3-13 Finite gain effect of the sigma-delta modulator

Capacitor mismatch

Capacitor mismatch will affect the gain of integrators. The gain is the value of the capacitor ratio. The capacitor mismatch is represented as

$$gain_{new} = gain_{original}(1-e) \quad . \tag{3.26}$$

where e represents mismatch error. (3.26) is used to model the gain of the integrators of the sigma-delta modulator shown in Figure 3-9. Assume the percent of the mismatch error of the integrators are all the same. The effect of the capacitor mismatch on the SNR is obtained in Figure 3-14. In order to obtain 12-bit resolution, The variation of the mismatch error form +25% to -30% is tolerable. This variation is achieved easily in CMOS processing technologies today.

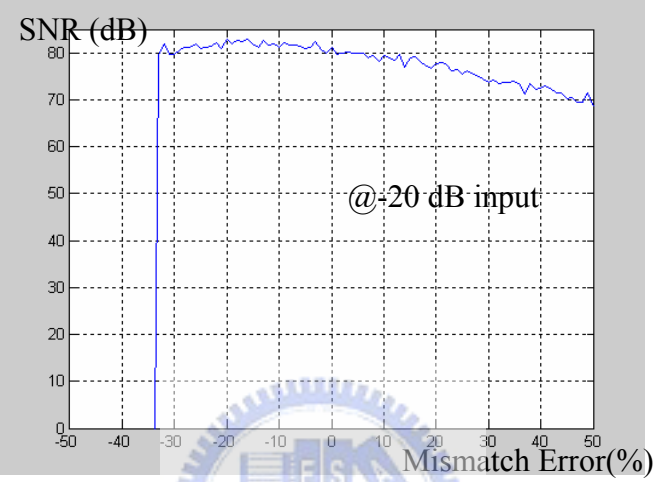


Figure 3-14 Capacitor mismatch effect of the sigma-delta modulator

3.5 The Circuit Design of Third-Order Sigma-Delta Modulator

Quantizer

The one-bit quantizer used in the proposed sigma-delta modulator is shown in Figure 3-15. The one- bit quantizer is composed of a dynamic latch comparator [11] and a latch. It is a modified one- bit quantizer of [9]. The one-bit quantizer is a dynamic structure, and it is suitable for the low power requirement because it consumes only the dynamic power. The Capacitor C_{c2} is charged to V_{off} , and the capacitor C_{c3} is charged to $signal + V_{off}$. The difference of the comparator input is the $signal$. The V_{off} is dependent on process variation. It can be positive or negative value. When it is negative, the response time of the comparator becomes larger. In order to decrease this effect, the comparator output does not directly feedback. The additional latch is designed at the comparator output. It relaxes the response time of

the comparator. So the comparator has a half clock time to compare the signal.

The dynamic latch comparator is shown in Figure 3-16. It is made of two back-to-back inverters with a positive regeneration and a latch. When the phase ϕ_1 is low, the outputs, nodes V_1 and V_2, are charged to V_{DD} by transistors M_9 and M_{10}. When the phase ϕ_1 is high, the nodes V_1 and V_2 are discharged by transistors M_1 and M_2. The voltages of nodes V_1 and V_2 are latched while dropping to the threshold voltage.

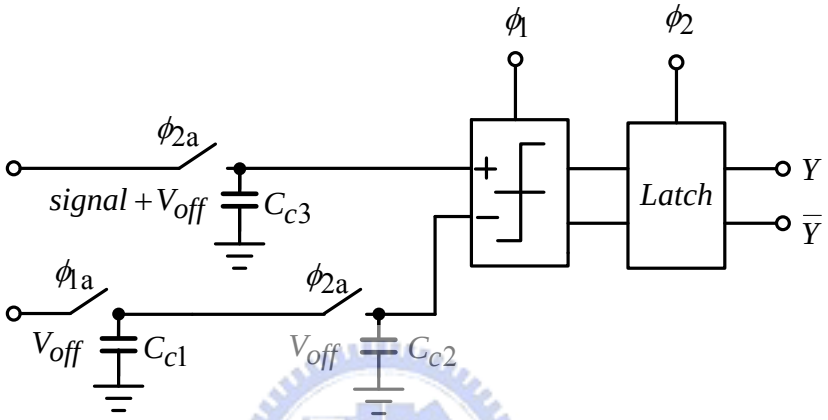


Figure 3-15 One-bit quantizer

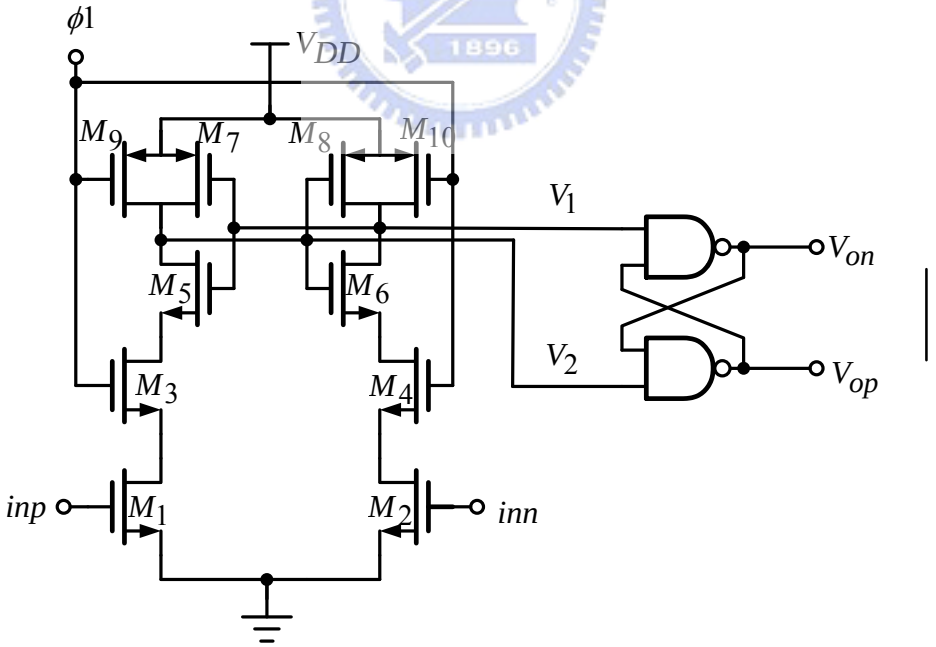


Figure 3-16 Dynamic latch comparator

Non-overlapping clock generator

The structure of the non-overlapping clock generator used in the proposed

sigma-delta modulator is shown in Figure 3-17. The Phases ϕ_1 and ϕ_2 are non-overlapping and generated by NOR gates and inverter chains. The other two phases ϕ_{1a} and ϕ_{2a} are slightly advanced than the phases ϕ_1 and ϕ_2. The delay is achieved by bottom-plate sampling technique [3]. It decreases the signal dependent charge injection. The D Flip-flop isolates such the noise of the external clock that clock generator has clearer clock phases.

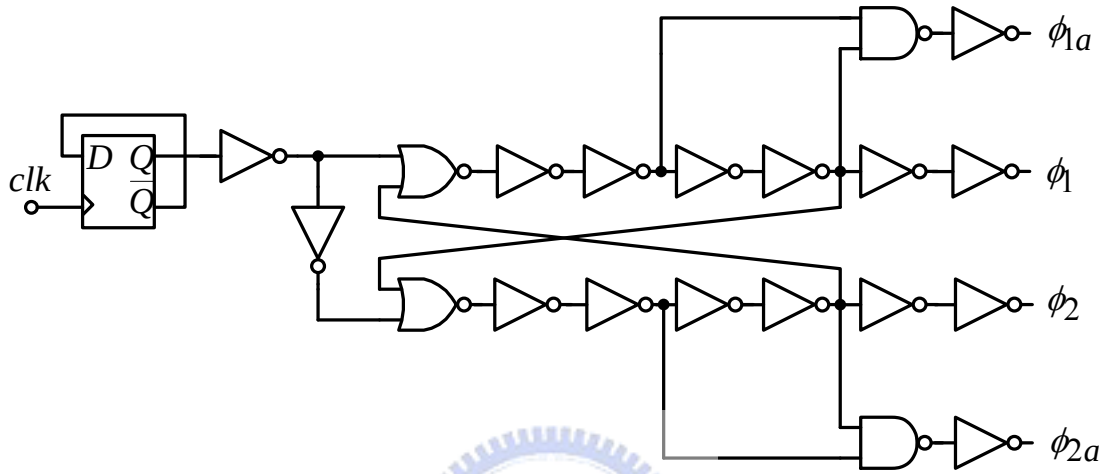


Figure 3-17 Non-overlapping clock generator

Voltage multiplier

Since the power supply of the system is 1V, the four clock phases generated by the non-overlapping clock generator shown in Figure 3-17 are not used to drive switches in the low-voltage switched-capacitor circuits. In order to guarantee an adequately low switch on-resistance in a low voltage environment, the clock voltage, used to drive only NMOS switches, is bootstrapped beyond the supply voltage range. Therefore, the voltage multiplier technique is implemented. It converts available voltage to a higher voltage. Figure 3-18 [12] shows a boosted clock driver. Capacitors C_1 and C_2 are charged to V_{DD} via the cross-coupled transistors M_1 and M_2. When the input clock, clk, is high, the output voltage, clk_{sw}, approaches $2V_{DD}$. The output voltage does not actually reach $2V_{DD}$ due to the charge sharing with the parasitic capacitances of the output. Capacitor C_2 must be large enough to boost the gates of MOS transistors to reduce the effect of charge sharing. To decrease the potential for latch-up, the bulk of the PMOS M_4 is tied to an on-chip voltage doubler. The bulk of the PMOS switch is biased by the circuit shown in Figure 3-19

[12].

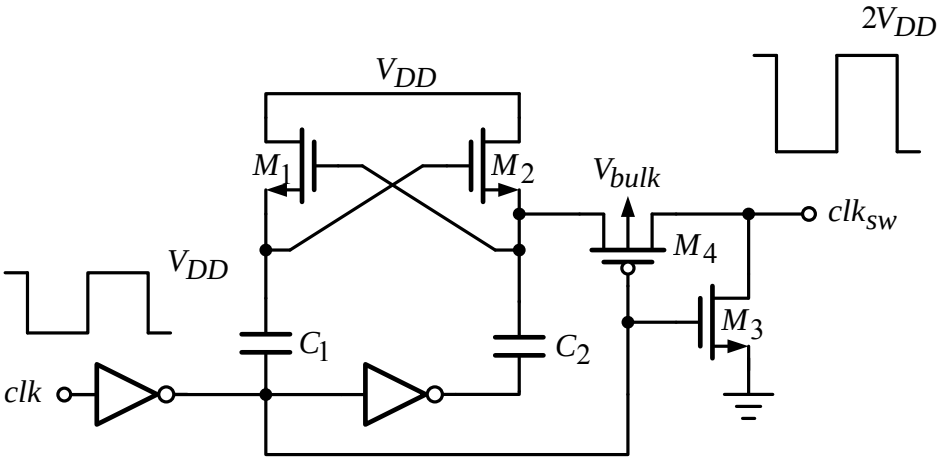


Figure 3-18 Boosted clock driver

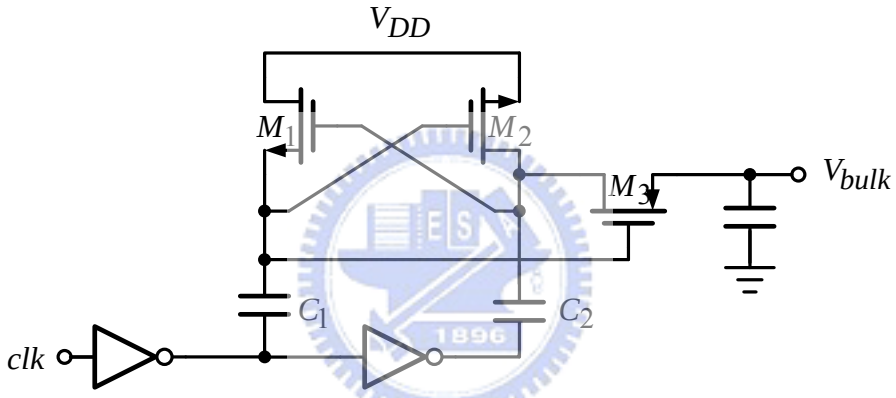


Figure 3-19 Voltage doubler

Noise effects

There are three main noise sources in a sigma-delta modulator. One is the flicker noise which occupies main component of noises at low frequency band. Another is the thermal noise which is white noise in spectrum. For a sigma-delta modulator, the thermal noise power is usually larger than flicker noise power in the signal frequency band. The third one is the quantization noise. It is introduced in Section 3.2. The flicker noise is high-pass filtered by CDS. Hence, thermal noise [4] is only discussed in this section.

The general switched-capacitor integrator is shown in Figure 3-20.

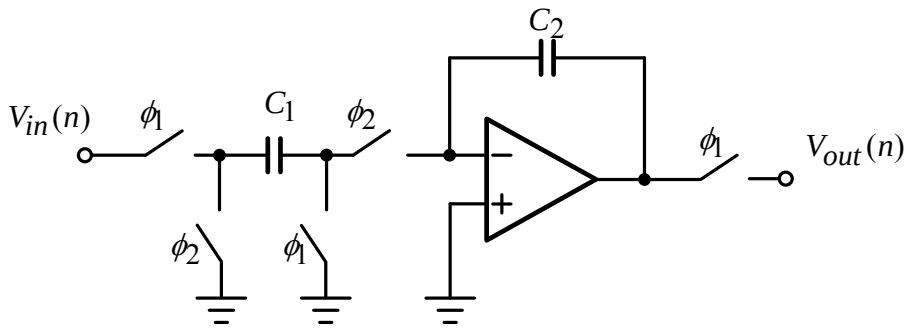


Figure 3-20 General switched-capacitor integrator

When ϕ_1 is high, the noise is shown in Figure 3-21.

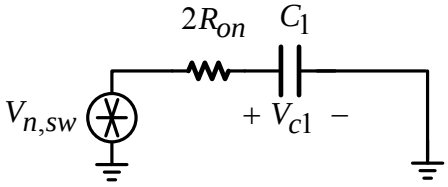


Figure 3-21 Noise model during ϕ_1

Its PSD is obtained as

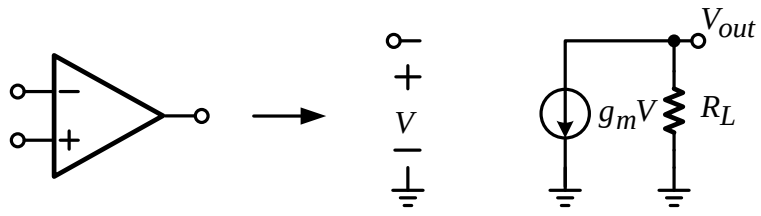
$$S_{n,\phi_1} = 4kT(2R_{on}) = 8kTR_{on}. \tag{3.27}$$

Its transfer function is derived as

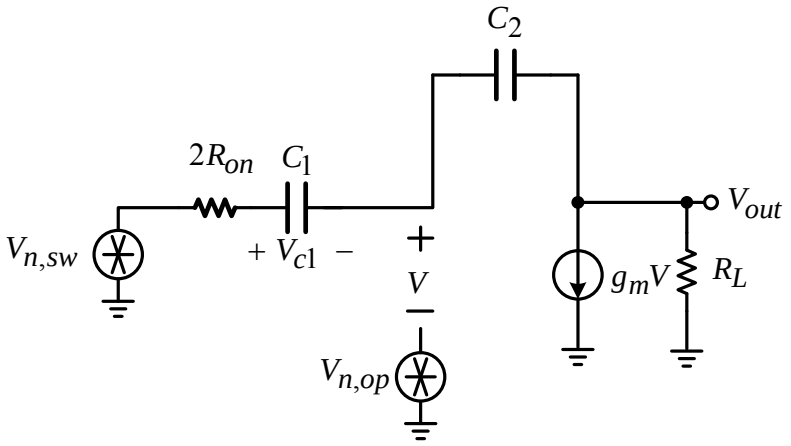
$$H(s) = \frac{V_{c1}(s)}{V_{n,sw}(s)} = \frac{1}{1+s\tau}, \tag{3.28}$$

where $\tau = 2R_{on}C_1$. Hence, the thermal noise in C_1 is calculated as

$$\overline{V_{c1}^2} = \int_0^\infty S_{n,\phi 1}(f)\left|H(j2\pi f)\right|^2 df = \frac{8kTR_{on}}{4\tau} = \frac{kT}{C_1}. \tag{3.29}$$



(a)



(b)

Figure 3-22 (a) Amplifier's small-signal, (b) Noise model in ϕ_2

Figure 3-22 (a) shows the small signal of the amplifier. When ϕ_2 is high, the noise is shown in Figure 3-22 (b). Assume R_L is infinite. The noise voltage across C_1 is represented as

$$V_{C1} = \frac{V_{n,sw}(s) - V_{n,op}(s)}{1 + s\tau} = \frac{V_{n,sw}(s) - V_{n,op}(s)}{1 + s(2R_{on} + 1/g_m)C_1}. \tag{3.30}$$

The transfer function is $H(s) = 1/1 + s\tau$. The total noise power in the switches is calculated as

$$\overline{V^2_{c1,sw}} = \int_0^\infty S_V(f)\left|H(j2\pi f)\right|^2 df = \frac{2kTR_{on}}{(2R_{on} + 1/g_m)C_1}$$

$$= \frac{kT/C_1}{(1 + 1/x)}, \tag{3.31}$$

where $x = 2g_m R_{on}$. The noise power in the amplifier is also considered. Assume the transfer function of the amplifier is $H(s) = 1/1 + s\tau_{op}$ where $\tau_{op} = 2R_{on} + 1/g_m$, and the transistors of the inverter OTA have the same g_m. The thermal noise is calculated as $(16/3)kT/g_m$. Therefore, the noise in the integrator is

$$\overline{V^2_{C1,op}} = \int_0^\infty S_{n,op}\left|H(j2\pi f)\right| df = \frac{S_{n,op}}{4\tau} = \frac{(16/3)kT/g_m}{4(2R_{on} + 1/g_m)C_1} = \frac{4}{3}\frac{kT/C_1}{1 + x}. \tag{3.32}$$

The total noise power includes the switch noise during $\phi_1 = 1$ and the switch and amplifier noises during $\phi_2 = 1$. The three noise sources are uncorrelated. Therefore the total noise power is calculated as

$$\overline{V^2_{c1,total}} = \frac{kT}{C_1}\left(1+\frac{x}{1+x}+\frac{4/3}{1+x}\right) = \frac{kT}{C_1}\left(\frac{7/3+2x}{1+x}\right)$$

$$= \frac{2kT}{C_1}\left(1+\frac{1/6}{1+x}\right), \tag{3.33}$$

where $x = 2g_m R_{on}$. If $x << 1$ the worse total noise power approaches $2.33kT/C_1$.

The total input noise power in Figure 3-7 is calculated as

$$\overline{V'^2_{c1}} = \frac{2.33kT}{C_1 OSR} + \frac{2.33kT}{C_2 OSR}\times\left(\frac{C_2}{C_{f1}}\right)^2 \times\left(\frac{C_{f1}}{C_1}\right)^2$$

$$= \frac{2.33kT}{C_1 OSR} + \frac{2.33kT}{C_1 OSR}\times\frac{C_2}{C_1} \quad \left(\frac{C_2}{C_1}=\frac{1}{3}\right)$$

$$= \frac{3.1kT}{C_1 OSR} \tag{3.34}$$

To calculate the value of the input sampling capacitance, the preamplifier in front of it must be considered. When the preamplifier has an input signal of 63mV, a noise power of $(5.42uV)^2$, and a gain of 4dB, the total input noise must be less than $(8.9uV)^2$ to have a SNR of 74 dB. Therefore, the input noise of the sampling capacitor must be less than

$$((8.9uV)^2 - (5.42uV)^2)\times 1.58^2 = (11.15uV)^2. \tag{3.35}$$

Since (3.34) must be less than (3.35), we obtain

$$\frac{3.1kT}{C_1 OSR} < (11.15u)^2. \tag{3.36}$$

It is rewritten as

$$C_1 > \frac{3.1kT}{(11.15u)^2 OSR} = \frac{3.1\times 1.38\times 10^{-23}\times 300}{(11.15u)^2\times 64} = 1.61\ (pF). \tag{3.37}$$

Simulation Results

Figure 3-23 is the Hspice simulation results of the proposed sigma-delta modulator. It is in the TT corner and has a power consumption of 14μW, a SNDR of 80 dB, a OSR of 64, and a signal bandwidth of 20 kHz. It is simulation at the 0.1V input sinusoid wave with the 5.625 kHz frequency. The total corner simulation results are list in Table 3-1. The simulation results of the power consumption have large variations in TT, SS, and FF corners due to that this architecture does not have a bias circuit.

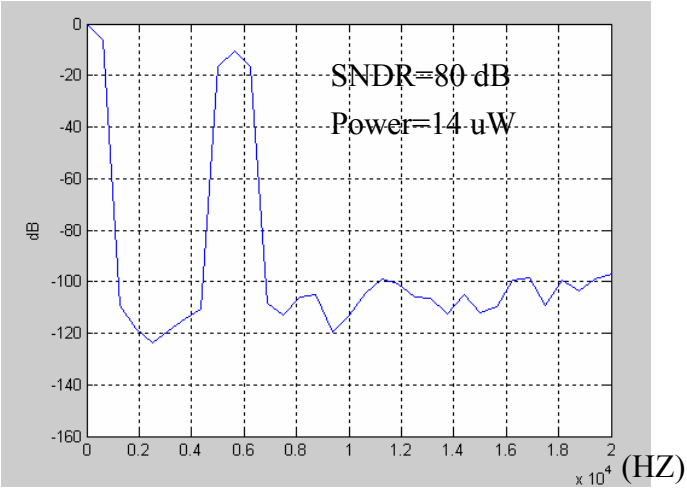


Figure 3-23 SNDR simulation result in TT corner

Table 3-1 Simulation results of the sigma-delta modulator

Corner	TT	SS	FF	FS	SF
SNDR (dB)	80	76.4	75.1	76	77.2
ENOB (Bit)	12.9	12.3	12.1	12.3	12.5
Power (u W)	14	8.7	24.8	14.5	14.2

The dynamic range of the sigma-delta modulator is shown in Figure 3-24. The DR is 82dB. A peak SNR of 80dB occurs at the input signal of -20dBV sinusoid wave.

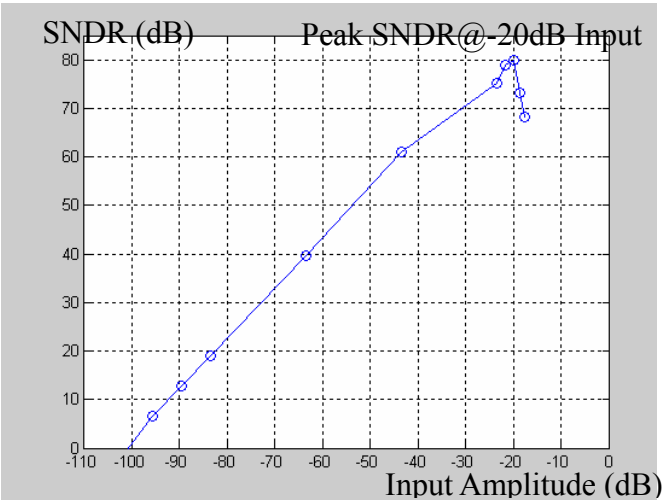


Figure 3-24 SNDR versus input amplitude for the sigma-delta modulator

3.6 Summary

There are many system coefficients which need to be determined in the sigma-delta modulator, such as the OSR, the input sampling capacitance, the sampling clock frequency, and the DC gain of the amplifier. The oversampling ratio is determined to be 64, and sampling capacitance must be larger than 1.61pF. The DC gain of the amplifier must be larger than 50 for the proposed sigma-delta modulator to achieve over 12-bit resolution. In terms of circuit, the inverter OTA, which has a higher power efficient and a lower area, is used instead of the traditional OTAs. The pure dynamic comparator used in the modulator with the inverter OTA is realized. It has a peak SNDR of 80 dB, and a DR of 80 dB at a sampling rate 2.56 MHz, a signal bandwidth of 20 kHz, and a power consumption of 14μW.

Chapter 4

A Low Power Digital Automatic Gain Control for Audio Front-End Circuit

4.1 Introduction

In this chapter, a dual-loop digital AGC is realized. The low-voltage low-power low-area techniques are described in the following sections. The system simulations and specifications of the AGC are introduced in Section 4.2. In Section 4.3, the digital blocks for the AGC loop are designed. They include a rectifier, a sinc filter, a low pass filter, integrators, and a value mapping block. The circuit design of a VGA is discussed in Section 4.4. A recurring DAC is shown in Section 4.5. Finally, the AGC system simulation results, performances, and layout are included in Section 4.6. The comparisons of the sigma-delta modulator and the digital AGC are presented in Section 4.7

4.2 Digital AGC System Design

The Proposed Digital AGC

Figure 4-1 is the proposed dual-loop digital AGC. It includes a VGA, a

sigma-delta modulator, a bit-stream rectifier, a sinc filter, a low-pass filter (LPF), integrators, a value mapping (VM) block, and a DAC. It is different from the traditional digital AGC shown in Figure 2-8. The feedback point is at the output of the modulator rather than the output of ADC. It does not go through a decimation filter. Therefore, this architecture has a lower latency, power, and area than the traditional one. The AGC is programmable and does not design the integrators and the LPF by off-chip capacitors. The circuits of the feedback loop of the AGC are designed easier than the analog AGCs' in low voltage. To achieve requirements of the attack time and the release time, the dual loop architecture is used in this design. The modulator has been introduced in Chapter 3.

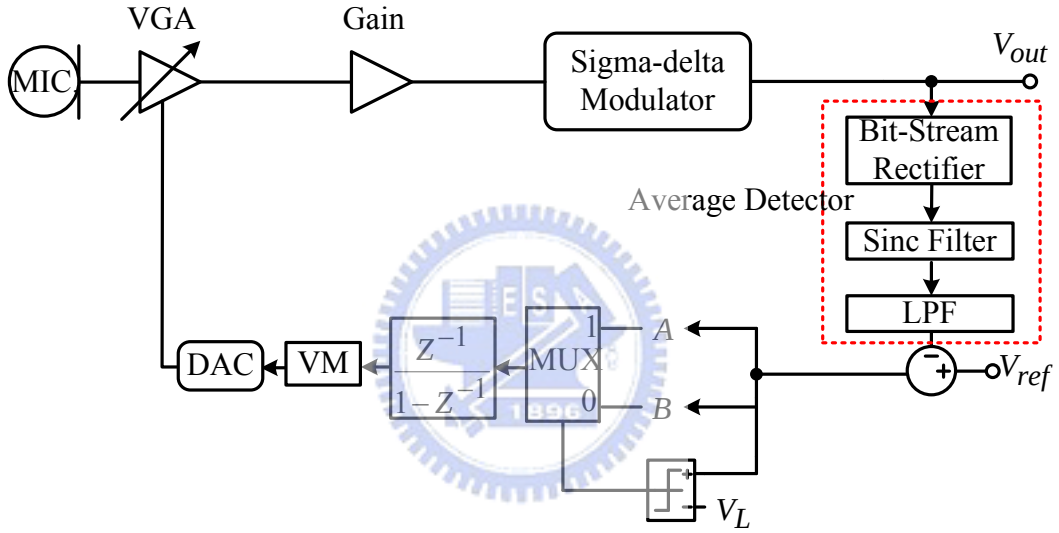


Figure 4-1 The proposed dual-loop digital AGC

Design specifications

The specifications of the AGC are listed in Table 4-1. The input signal bandwidth is designed in audio bandwidth from 250 Hz to 10 kHz. It covers the speech bandwidth. The total harmonic distortion (THD) must be less than 5%. It is enough for the intelligibility of speech signals. The maximum output amplitude of the AGC is designed as 0.3V because the input signal of the modulator at the peak SNR is 0.3V. The AGC also avoid the instability of the modulator. Form (2.5), V_{ref} is designed as 0.191V. The SNR of the AGC is designed as 74dB. The attack time is less than 5ms and the release time is about 50ms. The specifications of the modulator have been introduced in Chapter 3. The microphone sensor is SP0102N of Knowles. The output voltage range of the microphone is form 12.6uV to125mv. It equals the sound

pressure level (SPL) form 35dB to115dB.

Table 4-1 Specifications of the proposed AGC

Spec.		Performance Value	Unit
Audio Frequency Range		250 – 10k	Hz
SNR		> 74	dB
THD		< 5	%
Attack Time		< 5	ms
Release Time		~ 50	ms
Output amplitude		< 0.3	V
Microphone (Knowles SP0102N)	Output Voltage Range	12.6u - 125m	V
	Input Sound Range	35-115	dB

Simulation results of a analog AGC

To design the digital AGC, an analog AGC shown in Figure 2-6 must be designed first. The coefficients are obtained by simulating the analog AGC. Then the digital AGC is designed by the parameters.

There are two nonlinear features in Figure 2-6. One is that V_o will be saturated when the input signal becomes large suddenly. Another is that K_{VGA} is dependent on V_o. The transfer function between V_{ref} and V_{out} of the analog AGC has been derived as (2.11), and it is rewritten as

$$\frac{V_{out}}{V_{ref}} = \frac{K_{VGA}K_{GB}(D\omega_{ur} + \overline{D}\omega_{ua})(s + p_1)}{s^2 + p_1 \times s + K_{VGA}K_{GB}(S\omega_{ur} + \overline{S}\omega_{ua})K_{AD}p_1}$$

$$= \frac{K_{VGA}K_{GB}(D\omega_{ur} + \overline{D}\omega_{ua})(s + p_1)}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad , \tag{4.1}$$

where ω_n is the natural frequency, ξ is the damping ratio, and K_{VGA} is $19.58V_o$ which is obtained from the VGA circuit. The maximum output amplitude of the VGA is 0.1V and the maximum input amplitude of the modulator is 0.3V. Thus K_{GB} is designed as 3. The average detector gain K_{AP} is $2/\pi$ which has been introduced from (2.5). However, the p_1 and ω_u, which represents ω_{ua} or ω_{ur}, factors must be designed. When p_1 is increased, ω_n and ξ will be increased. When ω_u is increased, ω_n and ξ will be increased and decreased, respectively. The analog AGC is designed by these properties. Finally, p_1 is obtained as $1400(rad/s)$, ω_{ua}

is obtained as $180(rad/s)$, ω_{ur} is obtained as $22(rad/s)$, and V_L is derived as

$$0.15\times\left|\frac{1400}{j2\pi\times500+1400}\right|=0.061\ (V)$$

It means that the rectifier output signal with the lowest frequency of 500 Hz and the maximum amplitude of 0.15V will obtain a Voltage of 0.061V at the LPF output. It hopes that the output signal amplitude is not decreased in low frequency. When the input signal changes suddenly between 5.6mV and 100mV at the frequency of 250 Hz, the simulation result is shown in Figure 4-2. The attack time is 3ms and the release time is 51ms.

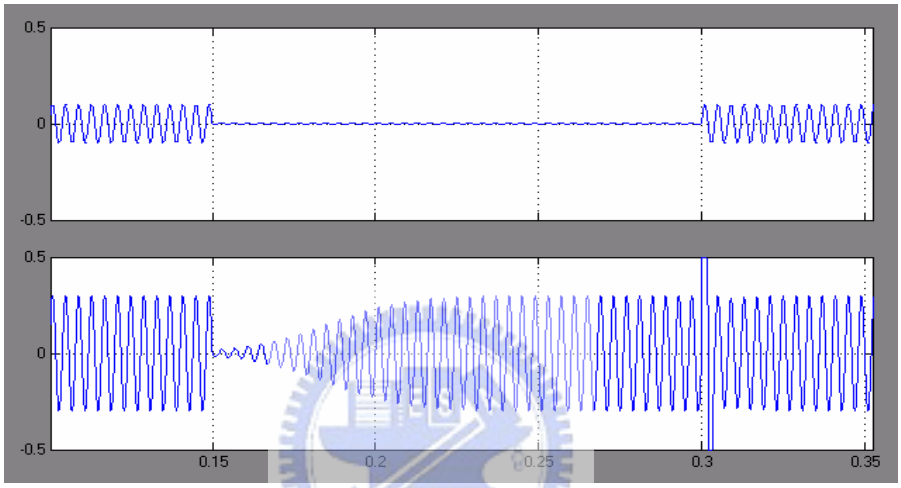


Figure 4-2 The simulation result of the analog AGC at frequency of 250 Hz

When the input signal changes suddenly between 5.6mV and 100mV at the frequency of 10 kHz, the simulation result is shown in Figure 4-3. The attack time is 3ms and the release time is 51ms.

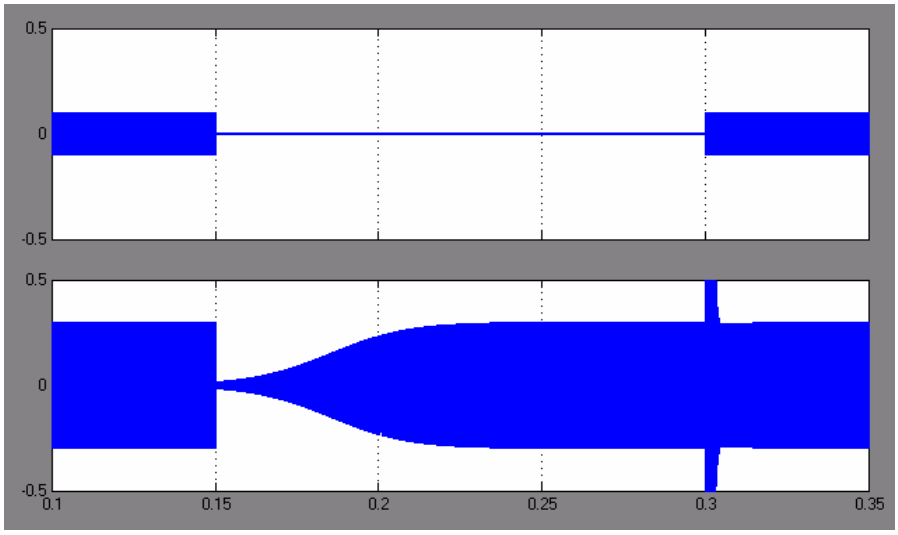


Figure 4-3 The simulation result of the analog AGC at frequency of 10 kHz

Figure 4-4 shows the input SPL versus the output amplitude. When the SPL is more than 88 dB, the AGC output amplitude will be pulled to -10.5dBV. When the SPL is less than 88 dB, the AGC input signal will be linearly amplified by the constant gain of 25dB. The SPL of 115dB represents a voltage of 125mV.

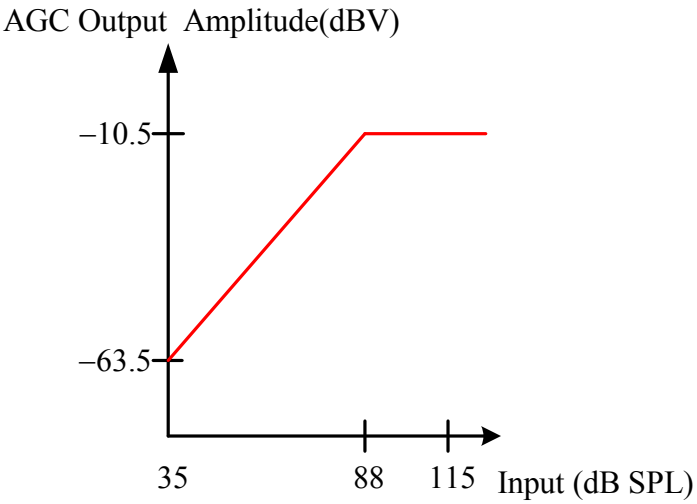


Figure 4-4 Input SPL versus output amplitude for the proposed AGC

4.3 Digital AGC System Design

Bit-stream rectifier design

Figure 4-5 shows the one-order sigma-delta modulator. When the input signal is positive, the pattern of -1-1 will be not occurred. When the input signal is negative, the pattern of 11 will be not occurred. The simulation result is shown in Figure 4-6(a) where the sinusoid wave is the input signal and the pulse wave is the output of the one-order modulator.

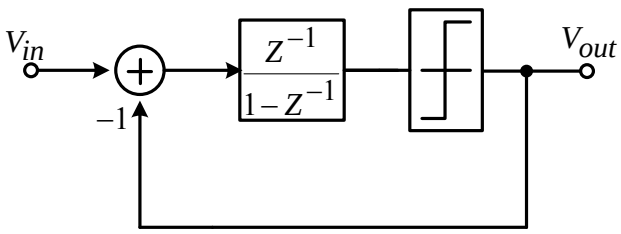


Figure 4-5 One-order sigma-delta modulator

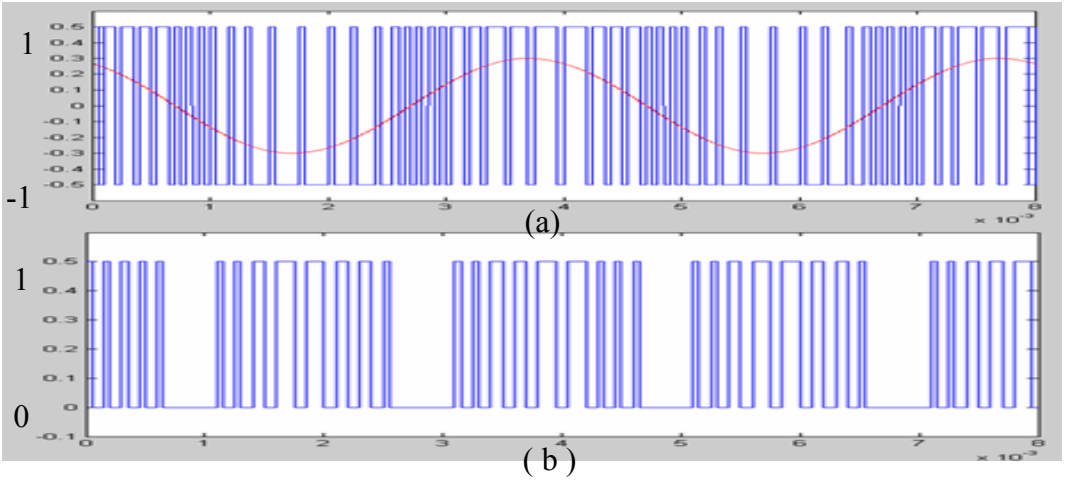


Figure 4-6 (a) The one-order SDM output signal (b) The rectifier output signal

Using these pattern properties, a bit-steam rectifier will be designed by Table 4-2. If the output bit of the one-order modulator represents a zero-average amplitude information, the rectifier output will obtain 0. If the output bit represents an amplitude information, the rectifier output will obtain 1. The simulation result of the rectifier table is shown in Figure 4-6(b). It shows that the original pulse wave signal becomes the positive signal.

Table 4-2 Rectifier table for 1-order SDM

Series (V_{out})		Result
n	n+1	n
1	-1	0
-1	1	0
1	1	1
-1	-1	1

For a high-order sigma-delta modulator, the patterns of -1-111 and 11-1-1 will be occurred when a small input signal is imported. The simulation result of the third-order modulator is shown in Figure 4-7(a). These patterns are occurred in dotted-line circles.

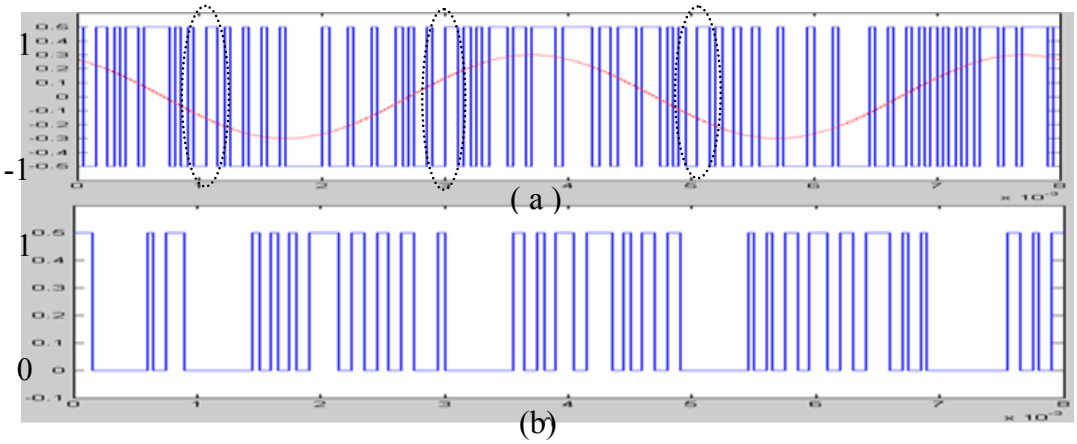


Figure 4-7 (a) Third-order SDM output signal (b) Rectifier output signal

These patterns represent a zero-average amplitude information. When Table 4-2 is used only, it will not obtain the zero-average amplitude information. So an additional table must be used. It is listed in Table 4-3. Using this additional table, the simulation result of the rectifier table with the additional rectifier table is shown in Figure 4-7(b).

Table 4-3 Additional rectifier table for high-order SDM

Series (V_{out})				Result		
n	n+1	n+2	n+3	n	n+1	n+2
1	1	-1	-1	0	0	0
-1	-1	1	1	0	0	0

In Figure 4-9, the transverse axle is the input sinusoid signals with the amplitude from 0V to 0.5 V at the frequency of 1 kHz. The signals are imported to a third-order sigma-delta modulator. Then the rectifier output obtains the output signals of the modulator. The average value of the rectifier output which represents a LPF output signal at DC is multiplied by $\pi/2$, and it represents the detected amplitude. The result shows that the proposed bit-stream rectifier works well.

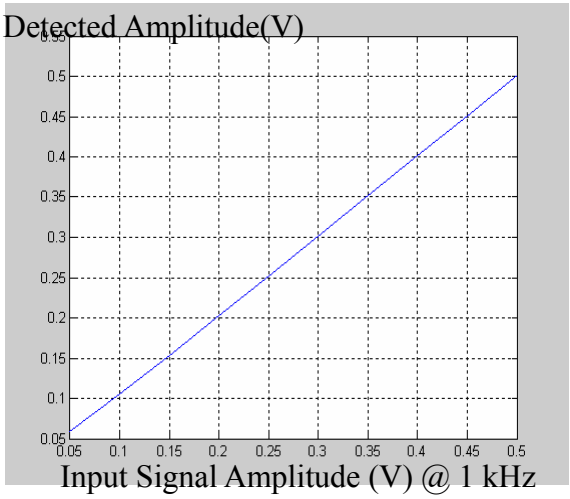


Figure 4-8 Simulation result of the proposed bit-stream rectifier

Low Pass Filter

Figure 4-9 includes a sinc filter and a LPF. The sinc filter filters the input signal roughly. The main purpose is to down the clock frequency. The sinc filter is a simple circuit, and it operates at high frequency. The LPF is a complex circuit, and it operates at low frequency. Thus, the power consumption of this architecture is lower than the architecture of only a low pass filter.

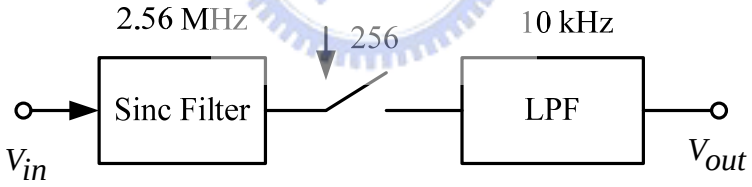


Figure 4-9 The architecture of low pass filter

The transfer function of the sinc filter is represented as

$$\frac{1}{N}\frac{1-Z^{-N}}{1-Z^{-1}}, \tag{4.2}$$

where N is the decimation ratio. Let $Z = e^{j\omega T} = e^{j2\pi f / f_S}$, (4.2) is rewritten as

$$\frac{1}{N}\frac{\sin(\pi N \frac{f}{f_S})}{\sin(\pi \frac{f}{f_S})} e^{-j\pi \frac{f}{f_s}(N-1)}. \tag{4.3}$$

When N is 256, f_S is 2.56 MHz, and f is 233 Hz which is the 3dB bandwidth of the LPF, the gain at 233Hz will be obtained as

$$20\log\left(\frac{1}{256}\frac{\sin\left(\pi 256\frac{223}{2560000}\right)}{\sin\left(\pi\frac{223}{2560000}\right)}\right) = -0.0077(dB) \tag{4.4}$$

It shows that the sinc filter decays a little gain at the 3dB bandwidth. The effect is ignored. The z-domain model of the sinc filter is shown in Figure 4-10. It also shows the bit numbers of the paths. The bit numbers of the input is one, and the bit numbers of the output is eight because that V_{ref} is designed as 8 bit. When a value one is imported only, the output will obtain the maximum value of 0.5.

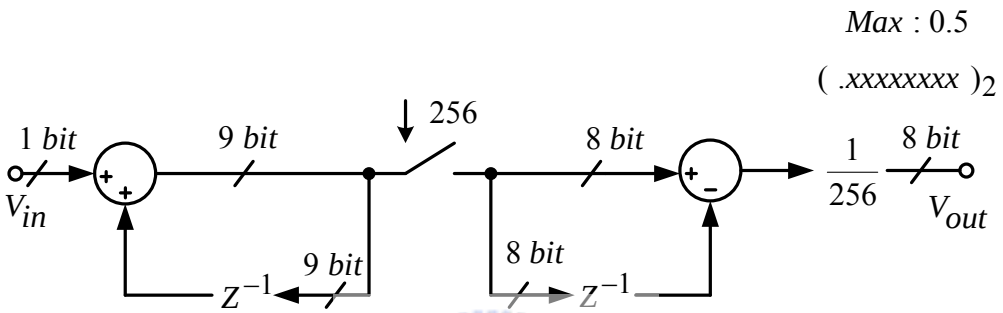


Figure 4-10 Z-domain model of the sinc filter

From Section 4.2, The Z-domain transfer function of the LPF is derived as (4.5) by Foreward Euler and the sampling frequency is10 kHz.

$$\frac{1400}{s+1400} \rightarrow \frac{0.14Z^{-1}}{1-0.86Z^{-1}} \tag{4.5}$$

To design it as a circuit, the parameters need to be quantized. The quantization result is shown in Figure 4-11 where A is a binary value of $(0.001001)_2$. The quantization method is like to Canonic Sign Digit (CSD). It has the minimum number of non-zero digits. So a number of adders are decreased. Figure 4-11 also shows the paths with bit numbers and maximum value.

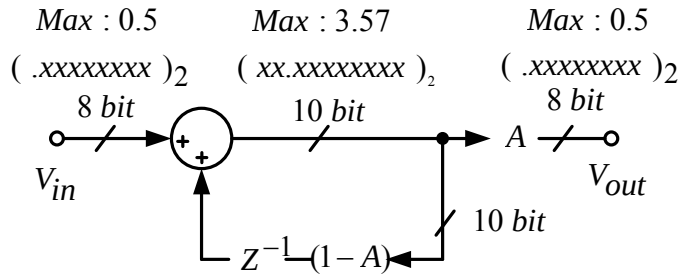


Figure 4-11 Z-domain model of the LPF

The comparison of the non-quantization LPF and the quantization LPF is shown in

Figure 4-12 where the continuous line and the star line represent spectrums of the non-quantization LPF and the quantization LPF, respectively. Test signals at the frequencies of 19.53Hz, 195.3Hz, and 1953Hz are imported. It shows that they match well.

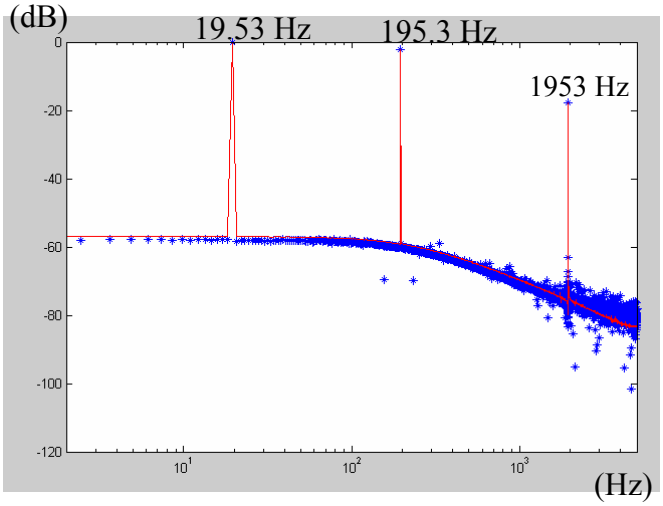


Figure 4-12 Non-quantization LPF versus quantization LPF

Integrator and value mapping

From Section 4.2, the Z-domain transfer functions of the integrators are derived as (4.6) and (4.7) by Foreward Euler and the sampling frequency of 10 kHz.

$$\frac{22}{s} \rightarrow \frac{0.0022Z^{-1}}{1-Z^{-1}} \tag{4.6}$$

$$\frac{180}{s} \rightarrow \frac{0.018Z^{-1}}{1-Z^{-1}} \tag{4.7}$$

From (4.6) and (4.7), A and B, shown in Figure 4-1, are 0.0022 and 0.018, respectively. In terms of value mapping block, the maximum and minimum output values of the integrators are 0.1468 and -0.05, respectively. The value 0.1468 maps to the value 111111 at the DAC input. The value -0.05 maps to the value 000000 at the DAC input. So the mapping equation between the integrator output and the DAC input is derived as

$$(x+0.05)\times\frac{63}{(0.05+0.1468)}=(x+0.05)\times 320=y\,, \tag{4.8}$$

where x is the integrator output value and y is the DAC input value. This equation needs to cost some adders.

When A and B are multiplied by 1.25, a new mapping equation is given by

$$(x+0.05\times1.25)\times\frac{63}{(0.05\times1.25+0.1468\times1.25)}=(x+2^{-4})\times2^{8}=y \qquad (4.9)$$

It needs only two adders to realize it. So the VM area will be decreased. The Z-domain models of the integrators and the VM are shown in Figure 4-13 where S is the selection signal of MUX, V_{in} is the input signal of the integrators, and V_{out} is the output signal of the VM.

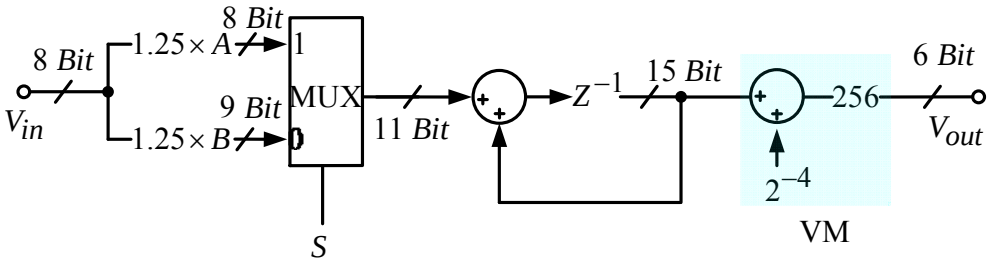


Figure 4-13 Z-domain model of integrators and VM

4.4 Variable Gain Amplifier

Variable Gain Amplifier

In an AGC loop, to maintain its settling time independent of the input signal levels, an exponential gain control characteristic is required. Unlike the exponential characteristic of the bipolar transistors, which is very suitable for dB-linear AGC, CMOS transistors follow a square-law characteristic in strong inversion. Although the transistors present exponential characteristic in weak inversion, their area is large at large current. Thus, some of the reported CMOS dB-linear VGAs are based on a pseudo-exponential function [13] given by

$$(\frac{1+x}{1-x})^{n}\approx e^{2nx} \quad (|x|\ll1) \qquad (4.10)$$

The approximation errors of this pseudo- exponential function to ideal one is within 5% only when $|x|<0.32$.

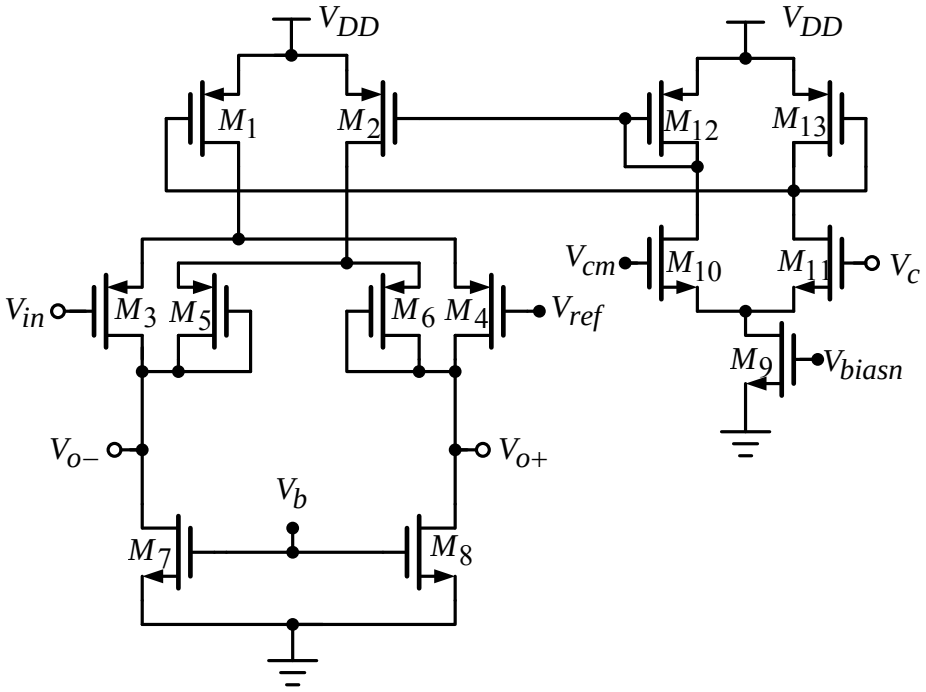


Figure 4-14 Variable gain amplifier

There are two types of VGA, which are current-mode and voltage-mode VGAs. The current mode VGAs are presented in [15] and [16]. But they are hard to be used in reality due to need a current to voltage converter and a voltage to current converter. The offset voltage in the current mode VGAs is also a seriously problem. Figure 4-14 is a voltage-mode VGA circuit [14] where V_c is a gain control signal. The VGA is used in this design due to be designed easily in low voltage. This architecture has a fully-differential output and a single-end input

Using (4.10) to approximate the exponential function, the gain equation for the VGA in Figure 4-14 is derived as

$$Gain = \frac{g_{m3}}{g_{m5}} = \sqrt{\frac{\mu_p C_{ox}(\frac{W}{L})_3 I_{D3}}{\mu_p C_{ox}(\frac{W}{L})_5 I_{D5}}} = \sqrt{\frac{(\frac{W}{L})_3 (I_{bias} + I_{ctrl})}{(\frac{W}{L})_5 (I_{bias} - I_{ctrl})}}$$

$$= \sqrt{\frac{(\frac{W}{L})_3}{(\frac{W}{L})_5}} \sqrt{\frac{\left(1+\frac{I_{ctrl}}{I_{bias}}\right)}{\left(1-\frac{I_{ctrl}}{I_{bias}}\right)}} = m\left(\frac{1+x}{1-x}\right)^{0.5} \approx me^x \quad (|x|<<1), \ (4.11)$$

where x is represented as

$$x=\frac{I_{ctrl}}{I_{bias}}=\frac{V_c\frac{g_{m11}}{2g_{m13}}\times\frac{g_{m1}}{2}}{\frac{I_{D1}}{2}}=\frac{V_c}{V_{gs1}-V_{thp}}\times\frac{g_{m11}}{g_{m13}} \tag{4.12}$$

Common Mode Feedback

There are two types of common-mode feedback (CMFB) [1]. One is a continuous circuit, and another is a switched-capacitor circuit shown in Figure 4-15. In a low voltage environment, the latter is chosen. Because it does not affects the swing of a amplifier and is designed easily in low voltage. In terms of the power consumption, it consumes only the dynamic power and so this circuit has a lower power consumption. The equivalent equation of the switched-capacitor CMFB is derived as

$$V_b=\frac{V_{o+}+V_{o-}}{2}+V_{bias}-V_{refa} \tag{4.13}$$

It shows that the CMFB output generates a common mode voltage. It is fed back to the amplifier. Thus, the output common mode voltage of the amplifier will be controlled by this voltage.

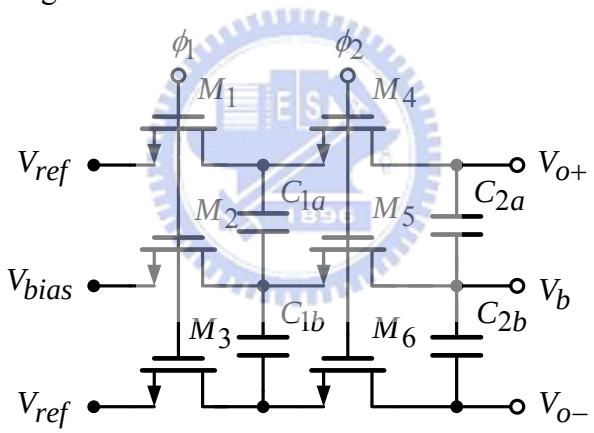


Figure 4-15 Common mode feedback

Output Buffer and Bias Circuit

The driving ability of the VGA is not enough. One main reason is that the VGA drives a next stage circuit by the variations of the drain-to-source voltage of MOSs. To obtain a better driving ability, Figure 4-16 is used. This circuit will decrease the gate voltage of M_3 when the output charges a load capacitor. It will increase the gate voltage of transistor M_3 when the output discharges the capacitor. So it has a higher power efficiency.

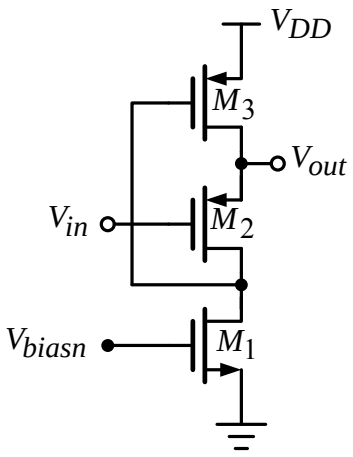


Figure 4-16 Output buffer for the VGA

The bias circuit [3] is shown in Figure 4-17. The resistor is designed between V_{DD} and the drain of PMOS M_4. PMOS M_4 avoids such body effect that this circuit is designed easily in low voltage. The bias circuit has two stable conditions. One is the bias circuit in work state, and another is the all transistors of the bias circuit in off state. So a start-up circuit must be designed. When the power supply is on initially, M_{s3} will be on. The gate voltage of M_{s1} is given by V_{DD}. After transistor M_{s1} is conducted, the bias circuit is revived. Then the gate of M_{s2} obtains a operational voltage such that the drain of M_{s2} obtains a low voltage. Finally, M_{s1} is in off state. So the start-up circuit does not affect the bias circuit at the bias circuit in work state. The channel resistance of M_{s3} must be designed large.

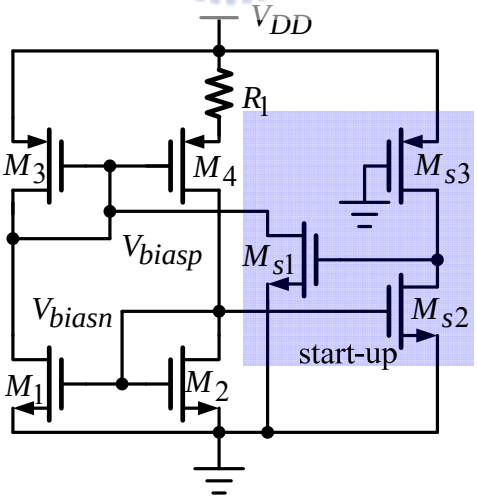


Figure 4-17 Bias circuit

Simulation Results

The gain versus the control voltage of the VGA is shown in Figure 4-18. It shows that the relationship between the control voltage and the gain is exponential. The

tuning range of the gain is 33.5dB. The range of the control voltage is 0.197V. From (2.3) and Figure 4-17, α is calculated as 19.58 and so K_{VGA} is $19.58V_o$.

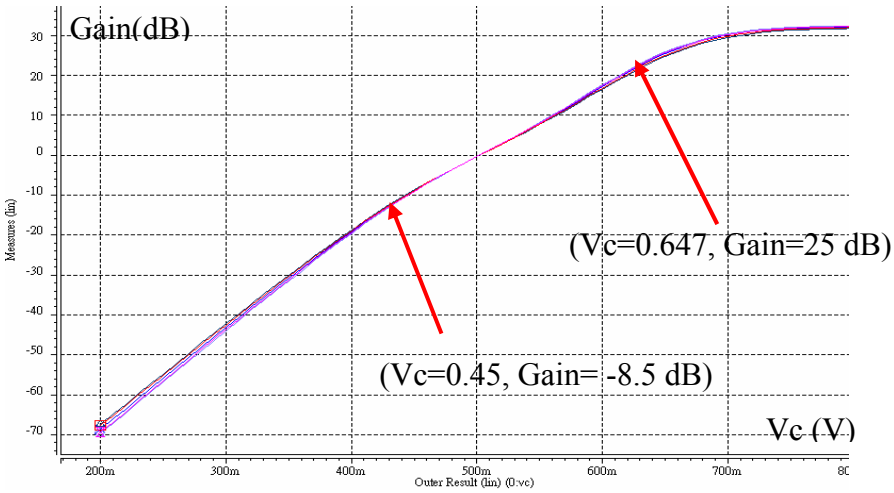


Figure 4-18 Gain versus control voltage

In order to have the enough the intelligibility of speech signals, the THD of sound signals must be less than 5%. The THD versus the sound pressure level (SPL) is shown in Figure 4-19. The THD is less than 4.1% when the SPL is less than 115dB.

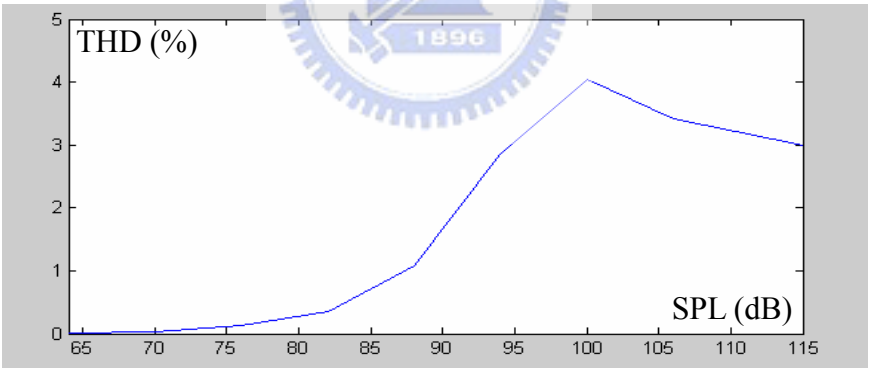


Figure 4-19 THD versus SPL

The microphone Specifications are shown in Table 4-1. When the output voltage is 63mV, the SNR will be 74dB. It represents to have 12-bit resolution. Thus, a test sinusoid wave of 63mV is imported to the VGA input. In this condition, the VGA gain is 4dB because this input signal will be amplified as 100mV, witch is the maximum amplitude of the VGA. In order to obtain a SNR of 74dB for the VGA, the minimum noise power requited is calculated as follow.

$$SNR = 74dB = 10\log(\frac{V_s^2}{V_n^2}) = 20\log(\frac{\frac{63mV}{\sqrt{2}}}{V_n}) \Rightarrow V_n = 8.9(uV) \quad (4.14)$$

Where V_s^2 is the signal power and V_n^2 is the noise power. So the total equivalent input noise power of the VGA must be less than $(8.9uV)^2$. In Figure 4-20, the total input noise power of the VGA from 250Hz to 20 kHz is calculated as

$$V_{inn(rms)} = \sqrt{\int_{250Hz}^{20k} P_{inn}(f)df} = 5.42uV, \quad (4.15)$$

where $P_{inn}(f)$ is the PSD of the input noise power. It shows that the input noise voltage of $5.42uV$ is less than $8.9uV$.

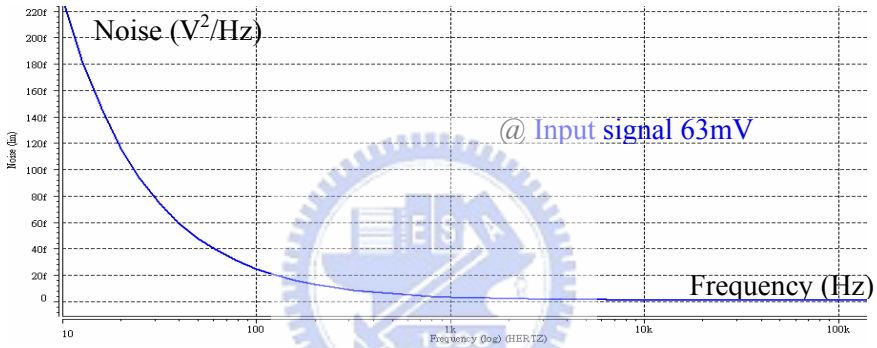


Figure 4-20 Noise power versus input frequency at gain 4dB

When the control voltage is changed, the input noise power of the VGA will be changed. The minimum noise power occurs at the maximum gain which has the maximum input g_m. In this condition, a small signal is imported. In Figure 4-21, the noise RMS voltage is calculated as (4.16) when the gain is maximum.

$$\sqrt{\int_{250Hz}^{20k} P_{inn}(f)df} = 3.75uV. \quad (4.16)$$

The maximum RMS voltage is calculated as 88mV below the THD of 4.1% . So the dynamic range of the VGA is derived as

$$DR = 10\log(\frac{V_{s,\max}^2}{V_{in,\min}^2}) = 10\log(\frac{(88m)^2}{(3.75u)^2}) = 87\ dB, \quad (4.17)$$

where $V_{s,\max}^2$ is the maximum input signal power and $V_{in,\min}^2$ is the maximum input noise power.

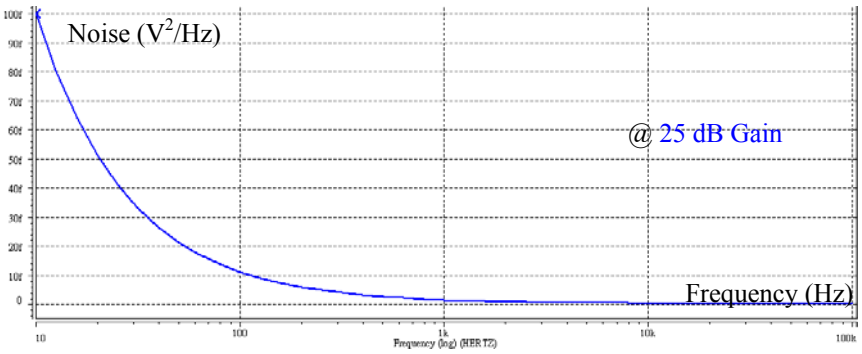


Figure 4-21 Noise power versus input frequency at gain 25dB

4.5 Digital to Analog Converter

The proposed recurring DAC

The 1-dB change of SPL is difficult to distinguish for people. In this thesis, a 6-bit DAC is designed. The VGA has the gain range of 33.5dB. The gain change per bit of the DAC is calculated as (4.18). It is less than 1dB and so it is enough.

$$\frac{33.5}{63} = 0.53(\frac{dB}{bit}) \quad . \tag{4.18}$$

There are three ways [2] of current, voltage, and charge in designing a DAC. Using a current based architecture, it is hard to be designed in low power because the low reference current is difficult to be realized. In voltage based architecture, it has large area in low power design due to be designed by resistors. In order to design a low-area low-power DAC, a charging based architecture is used. It uses capacitors to design circuit and so it consumes mainly dynamic power. To decrease area, a recurring DAC is designed.

The charging based recurring DAC is shown in Figure 4-22 where ϕ_r is a reset signal, ϕ_c is a charging load signal, and S_0, S_1, and S_2 are the selection signals of the multiplexer. Figure 4-23(a) is a multiplexer which selects input bits at different phases. Figure 4-23(b) is a timing diagram. The timing diagram has eight phases. In from one to six phases, the DAC calculates the output value according to the input sequence codes. In seven and eight phases, the result value of the DAC is charged to load capacitor.

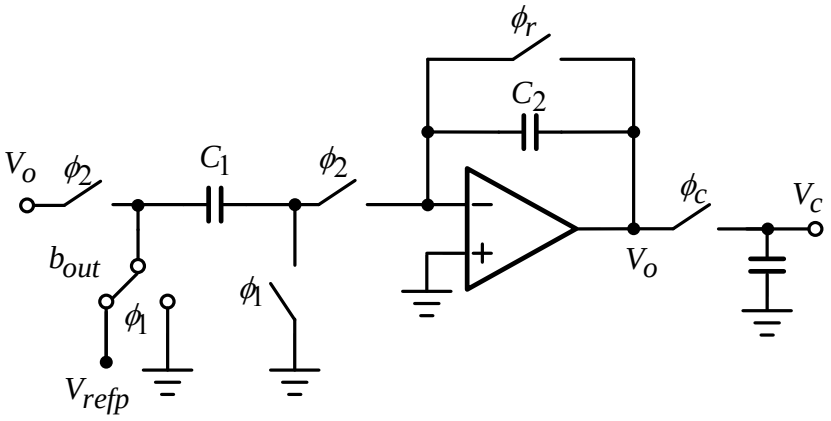
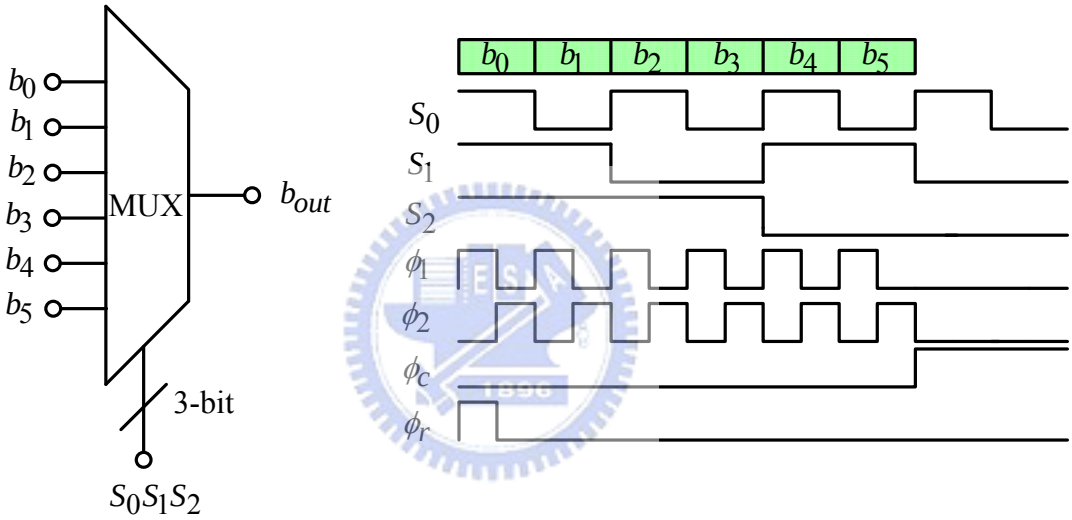


Figure 4-22 Recurring DAC



(a) (b)

Figure 4-23 (a) Multiplexer and (b) timing diagram for recurring DAC

The total charge in capacitors C_1 and C_2 during $\phi_1 = 1$ is represented as

$$V_o(n\text{-}1)C_2 + V_{refp}b_{out}C_1 . \tag{4.19}$$

The total charge in C_1 and C_2 during $\phi_2 = 1$ is represented as

$$V_o(n)C_2 + V_o(n)C_1 . \tag{4.20}$$

(4.19) and (4.20) have the same charge due to the law of conservation of charge, and it is obtained as

$$V_o(n\text{-}1)C_2 + V_{refp}b_{out}C_1 = V_o(n)C_2 + V_o(n)C_1 . \tag{4.21}$$

Simplifying (4.21), it is rewritten as

$$V_o(n) = V_o(n\text{-}1)\frac{C_2}{C_1 + C_2} + V_{refp} b_{out} \frac{C_1}{C_1 + C_2}. \quad (4.22)$$

The ratio of C_1 and C_2 is 1 : 1. From (4.22), (4.23) and (4.24) are obtained by $b_{out} = 1$ and $b_{out} = 0$, respectively.

$$b_{out} = 1 \quad : V_o(n) = \frac{1}{2} V_o(n\text{-}1) + \frac{1}{2} V_{refp} \quad (4.23)$$

$$b_{out} = 0 \quad : V_o(n) = \frac{1}{2} V_o(n\text{-}1) \quad (4.24)$$

Using (4.23) and (4.24), the relationship between the input codes and V_o is derived as follows.

$$m = \frac{C_1}{C_1 + C_2}, \quad k = \frac{C_2}{C_1 + C_2} \quad (4.25)$$

$$V_o = (mb_5 + mkb_4 + mk^2 b_3 + mk^3 b_2 + mk^4 b_1 + mk^5 b_0) \times V_{refp}$$

$$= \left(\frac{b_5}{2} + \frac{b_4}{4} + \frac{b_3}{8} + \frac{b_2}{16} + \frac{b_1}{32} + \frac{b_0}{64}\right) \times V_{refp} \quad (4.26)$$

Current mirror OTA

In terms of low voltage design, two-stage OTA and current-mirror OTA will be chosen due to have less cascode MOSs. The two-stage OTA needs a compensation capacitor and so a current must charge or discharge it. Therefore, the current-mirror OTA has smaller power consumption than the two-stage OTA[11]. The current-mirror OTA is shown in Figure 4.24. Equations of the gain, the bandwidth, the out swing, and the slew rate of the current-mirror OTA are derived as follows.

$$\text{Gain} = g_{m2}(ro_8 \,||\, ro_9) \quad (4.27)$$

$$\text{Bandwidth} = \frac{g_{m2}}{C_L} \quad (4.28)$$

$$\text{Output Swing} = V_{DD} - V_{OD8} - V_{OD9} \quad (4.29)$$

$$\text{Slew rate} = \frac{I_{D1}}{C_L} \quad (4.30)$$

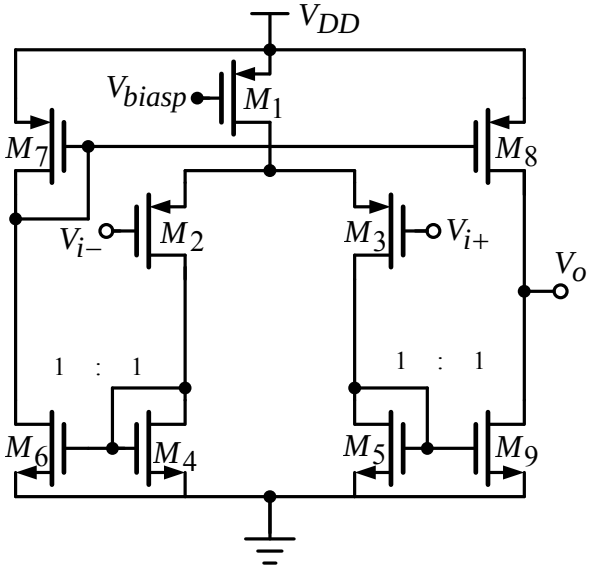


Figure 4-24 Current-mirror OTA

In this thesis, a load capacitor of 0.4p is used as load. The performances of the current-mirror OTA are listed in Table 4-4.

Table 4-4 Performances of the current-mirror OTA

Gain	54 dB
Bandwidth	1.8MHz
Power	0.936uW

Capacitor mismatch

Capacitor matching is very important in switched-capacitor circuits. In reality, a large unit capacitor has a better ability of capacitor matching. If a too large unit capacitor is designed, it will waste the power consumption. So the requirements of the capacitor-matching ability of switched-capacitor circuits must be known. The mismatch effect is obtained by (4.25) and (4.26). When the mismatch error of the ratio of C_2/C_1 is 1%, the INL and DNL effects of the proposed DAC are shown in Figure 4-25. The INL versus the C_2/C_1 mismatch error is shown in Figure 4.26(a). The DNL versus the C_2/C_1 mismatch error is shown in Figure 4.26(b). If the mismatch error is more than 3.5%, it will occur non-monotonic. Thus, the capacitor mismatch error must be less than 3.5%. This requirement is achieved easily in CMOS processing technologies today.

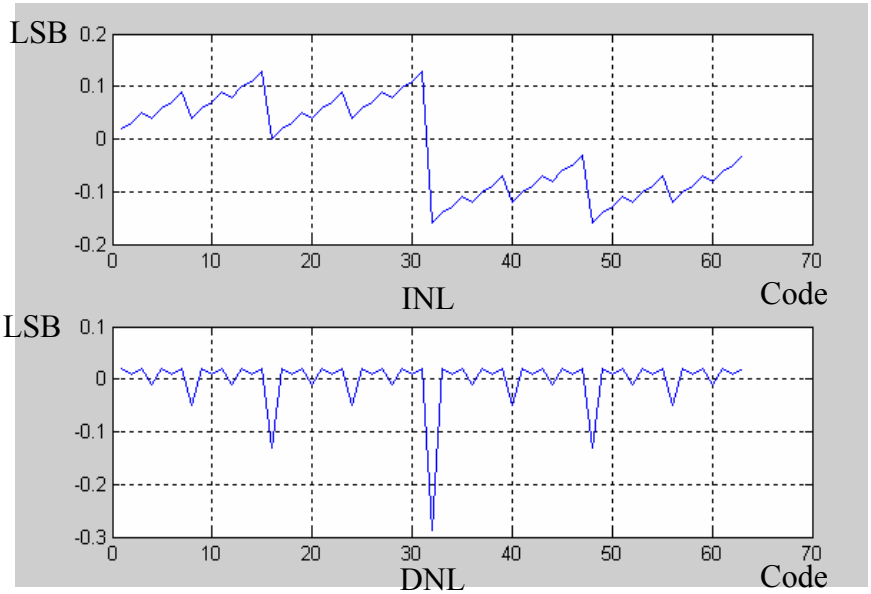


Figure 4-25 (a) INL and (b) DNL effect at 1% mismatch error

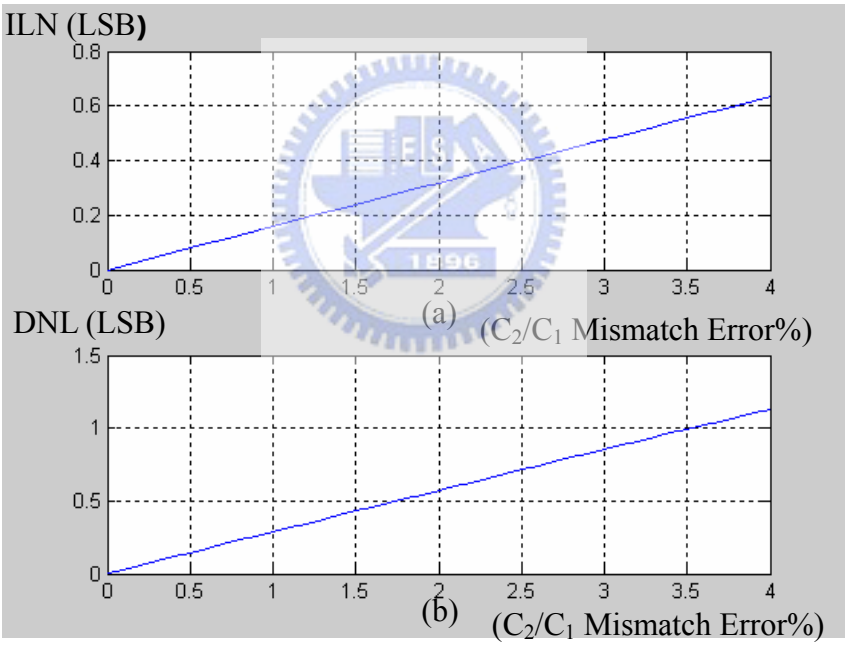


Figure 4-26 (a) INL and (b) DNL effect of capacitor mismatch

Simulation Results

The INL and DNL simulation results of the proposed recurring DAC are shown in Figure 4-27. It is simulated in the TT corner. The simulation results of the total corners are listed in Table 4-5. The INL is less than 0.12LSB and the DNL is less than 0.05LSB.

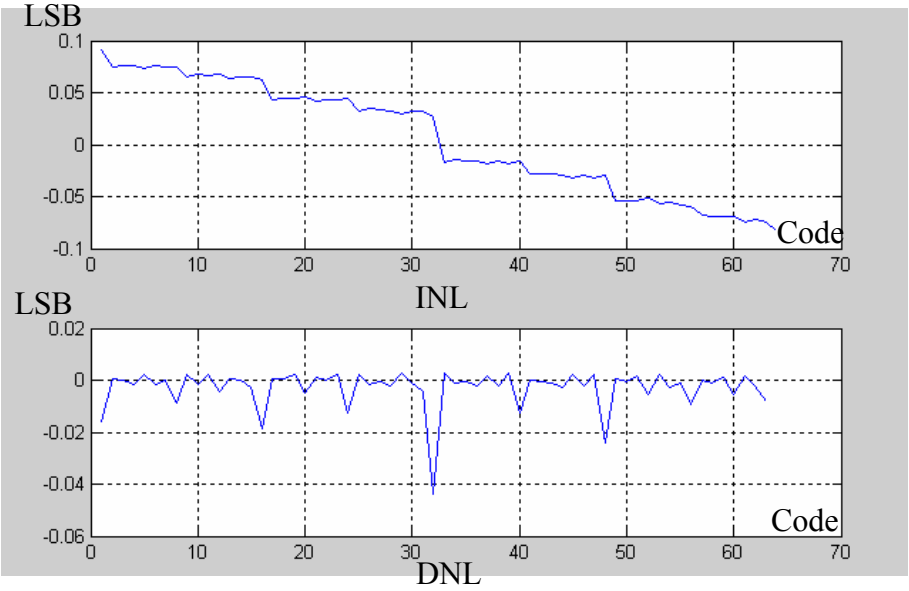


Figure 4-27 INL and DNL in TT corner

Table 4-5 Performances of the recurring DAC

Corner	TT	FF	SS	SF	FS
INL (LSB)	0.09	0.119	0.108	0.095	0.113
DNL(LSB)	0.044	0.048	0.033	0.033	0.03

4.6 Simulation Results and Layout

Figure 4-28 shows the simulation result of the proposed dual loop digital AGC at the input frequency of 250 Hz. The input amplitude is between two amplitude levels with a sudden 25 dB increase. The larger input amplitude is 100mV which represents the 113dB SPL. The smaller input amplitude is 5.6mV which represents the 88dB SPL. The AGC pulls the output voltage of the VGA to 100mV. If the input amplitude is more than 100mV, the amplitude will be decreased. If the input amplitude is less than 100mV, the amplitude will be amplified. The voltage V_C is a control voltage for the VGA. The release time goes through the narrow loop bandwidth. The attack time goes through the width loop bandwidth. When the signal changes suddenly form 100mV to 5.6mV, the release time is obtained as 53.2ms. When the signal changes suddenly form 5.6mV to 100mV, the attack time is obtained as 3.4ms.

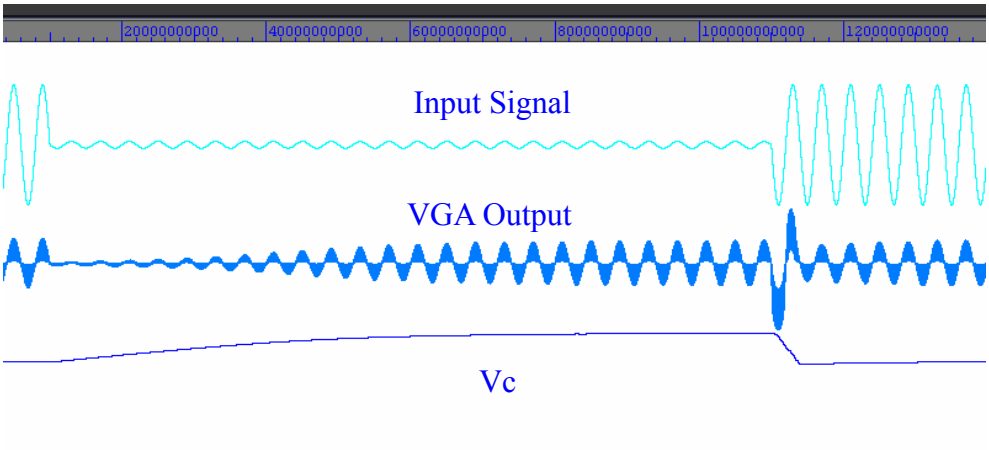


Figure 4-28 Simulation result of the proposed AGC at the input frequency of 250 Hz by Hsim

Figure 4-29 shows that the release time is 53.1ms and the attack time is 3.2ms at the input frequency of 10 kHz. From the two simulation results, the attack times are all less than 5ms. The release times are all about 50ms. They reach the design specifications. The power consumption of the AGC is 42.3μW.

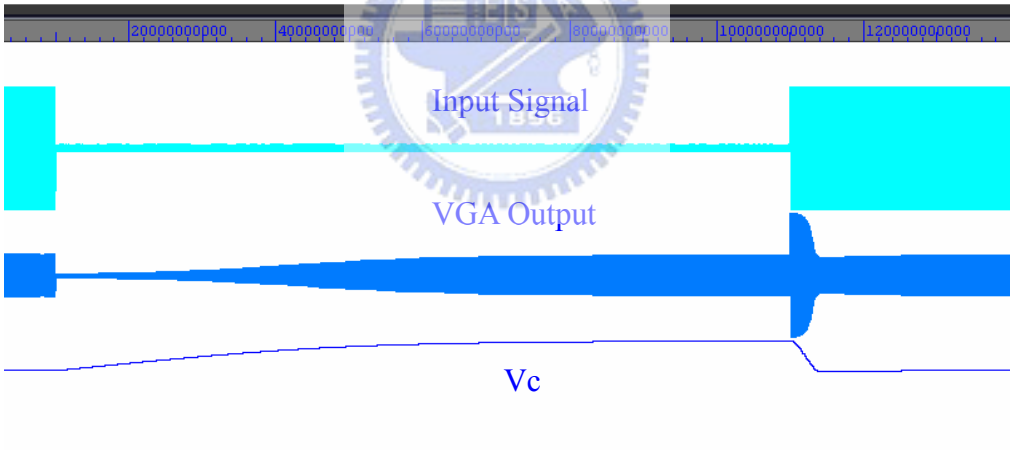


Figure 4-29 Simulation result of the proposed AGC at the input frequency of 10k Hz by Hsim

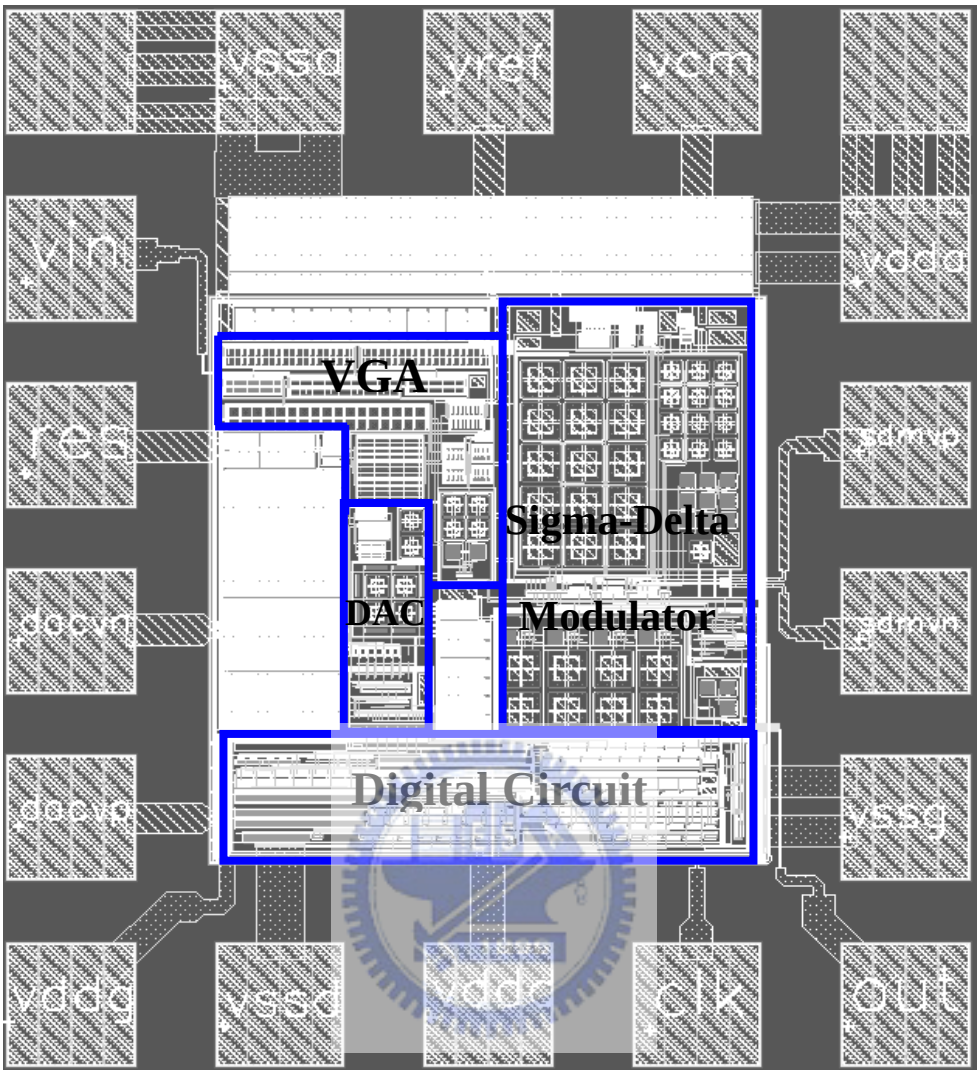


Figure 4-30 Layout of the proposed AGC system

The layout shown in Figure 4-30 is divided into the analog and digital parts. The bottom of the layout is the digital blocks which includes a bit-stream rectifier, a sinc filter, a LPF, integrators, and a value mapping block. The above part is the analog part which contains a VGA, a third-order sigma-delta modulator, and a DAC. The rest area of the layout is filled with PMOS capacitors which are used as decoupling capacitors. The decoupling capacitors are connected to the power plane. The chip area is $0.6\text{x}0.68\,mm^2$. The summary of the performances is listed in Table 4-6

Table 4-6 The summary of the performance

Spec.		Performance Value	Unit
Supply Voltage		1	V
Signal Bandwidth		250 ~ 10k	Hz
Dynamic Range @ THD < 4 .1%		87	dB
THD		< 4.1	%
Attack Time		< 5	ms
Release Time		53	ms
Σ-Δ Modulator	Sampling Frequency	2.56M	Hz
	Signal Bandwidth	20K	Hz
	SNDR	80	dB
	DR	82	dB
	Power	14	uW
Power Consumption		42.3	uW
Chip/core area		0.6x0.68/0.347x0.429	mm^2
Technology		0.18	um (TSMC)

4.7 Comparison

Table 4-7 shows the comparison of the sigma-delta modulators for audio applications. The range of paper survey is below 0.25mW and above SNR of 60dB. It is difficult to compare the power efficiencies. In general, the figure-of-merit (FOM)[11] is a criterion for the power efficiency of sigma-delta modulators. The FOM is defined as

$$FOM = \frac{4kT \cdot f_B \cdot DR}{P}, \tag{5.1}$$

where k is Boltzmann's constant, T is the absolute temperature, f_B is the signal bandwidth, and P is the power consumption. Although the signal bandwidth and the power consumption are considered in FOM, the supply voltage is not taken into account [29]. This thesis has more two times score than the best one. The area is not included into FOM and it is difficult to compare due to different capacitor processes (poly-to-poly, metal-to-metal, and so on) and structures. In general, the area is dominated by the capacitors for switched-capacitor sigma-delta modulators. From Table 4-7, the proposed sigma-delta modulator has best area performance.

Table 4-7 The comparison of sigma-delta modulators for the audio applications

Year	V_{DD}	DR	BW	Power	Area	Process	FOM
JSSC, 2004[11]	1.0V	88Db	20kHz	140uW	0.18 mm^2	90nm CMOS	1493e-6
JSSC, 2003[17]	1.5V	80dB	25kHz	135uW	-	0.5um CMOS	306.8e-6
JSSC, 2002[18]	0.7V	75dB	8kHz	80uW	0.082 mm^2	0.18um CMOS	52.4e-6
DCAS, 2001 [19]	1.2V	75dB	3.4kHz	38uW	-	0.35um CMOS	46.88e-6
DATE, 2001 [20]	1.5V	75dB	25kHz	230uW	1.2 mm^2	0.5 um CMOS	56.95e-6
This work	1.0V	82dB	20kHz	14uW	0.045 mm^2	0.18um CMOS	3749e-6

Table 4-8 shows the comparison of the AGCs for audio applications. The comparison papers are all analog AGC architecture. Only this thesis is a digital AGC architecture. So this thesis does not design integrators and low pass filters by off-chip capacitors. And it is also programmable easily. In terms of power consumption, this thesis has the additional sigma-delta modulator block which is different from the other papers. In other words, the power consumption of this thesis needs to include additionally the power consumption of the modulator. Table 4-8 shows that the power consumption of this thesis is almost the same as the others. The area has best performance than the other papers. The supply voltage 1.0V is lowest than the other voltage-mode AGCs. [22] is a current-mode architecture. In reality, it lacks an analog to current block and a current to analog block for voltage-mode applications. When the THD is less than 4.1%, the DR of this thesis is 87dB. The DR of the other papers is measured in different condition.

Table 4-8 The comparison of AGC for the audio applications

Year	V_{DD}	DR	BW	Power	Area	Process
JSSC,2006[21]	2.8V	78dB	10kHz	36uW	4.41mm^2	1.5um BiCMOS
IP-CDS,2005[22]	1.0V	72dB	100-10kHz	25uW	0.16mm^2	1.2um CMOS
ISCAS,1998[23]	3.0V	69dB	100-10kHz	162uW	-	1.2um CMOS
This work	1.0V.	87dB	250-10kHz	42.3uW	0.148mm^2	0.18um CMOS

Chapter 5

Conclusions

5.1 Conclusions

This thesis presents the low-power low-voltage low-area dual-loop digital AGC and sigma-delta modulator for audio front-end circuit. In terms of the sigma-delta modulator, the single-loop third–order sigma delta modulator used in this thesis has a low-power consumption due to less circuit components and matching requirements. The inverter OTAs with swing improvement and the pure dynamic comparator are used for the sigma-delta modulator. They all have higher power efficiency. The low-voltage design techniques are also used and they solve the switch-driving problem and enhance the gain of the inverter OTA. The CDS technique is used to eliminate the offset voltage and attenuate the noise floor. It has a peak SNDR of 80 dB, a DR of 80 dB at a sampling rate 2.56 MHz, a signal bandwidth of 20 kHz, and a power consumption. of 14μW

Using this low-power sigma-delta modulator to design the digital AGC, it does not go through decimator filter so can decrease area, power, and latency of the AGC loop. The proposed AGC system is implemented at the supply voltage of 1V. It has a DR of 87 dB, a SNR of 74Db, a power consumption of 42.3μW, and a signal

bandwidth of 250 Hz-10 kHz.

5.2 Future works

The high performance architecture of sigma-delta modulator is fully-differential signal due to have better common-mode noise immunity. So decreasing effect of common-mode noise is an object in the future. In low voltage, the linear of a VGA is hard to be designed well because the linear range of circuits is decreased. If it is designed as high linear, the output dynamic range will be small. It causes that the capacitor becomes large in the some SNR. So the power consumption becomes large. How to design more linear circuit of a VGA in low voltage and low power is also very important in the future.

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