國立交通大學

電機與控制工程系

碩士論文

離散時間單迴路積分三角類比數位轉換器之功率損耗模型建立與針對非對稱數位用戶迴路終端機應用之電路設計

Building the power consumption model of discrete time single-loop multi-bit sigma-delta ADC and designing the circuit for ADSL-CO (central office) application

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摘要

在本篇論文中，我們建立了積分三角類比數位轉換器的功率消耗模型，而我們把功率消耗模型分成類比功率消耗模型和數位功率消耗模型兩個部份，類比功率消耗模型包括積分器功率消耗模型、量化器功率消耗模型、數位類比轉換器功率消耗模型；數位功率消耗模型包括時脈產生器功率消耗模型和開關功率消耗模型。

我們針對非對稱數位用戶迴路終端機應用來做電路設計。我們選擇的電路架構為離散時間單迴路單一位元積分三角類比數位轉換器來實現非對稱數位用戶迴路終端機。

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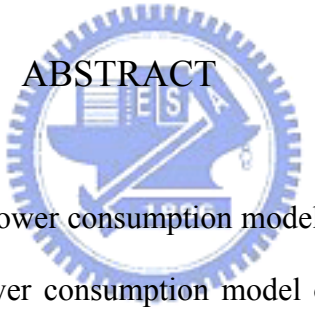

ABSTRACT

In this work, we build the power consumption model of discrete time single-loop multi-bit sigma-delta ADC, and the power consumption model of discrete time single-loop multi-bit sigma-delta ADC can be divided into two parts. The one is the analog power consumption model, and the other is the digital power consumption model. The analog power consumption model includes the integrator power consumption model, the Quantizer power consumption model and the DAC power consumption model. The digital power consumption model includes the clock driver power consumption model and the switch power consumption model.

We design the circuit for ADSL-CO (central office) application. And we used the discrete time single-loop single -bit sigma-delta ADC architecture to simulate.

誌　　謝

首先感謝陳福川老師在我的研究論文方面的指導，使我的論文能夠更完善，並且在 ic 設計的領域建立的一定的基礎；接下來要感謝的是邱俊誠老師在微機電製程、8051 單晶片與 ZigBee 無線感測網路方面的指導，使我能夠在各方面都有一定的基礎，以後能有更完善的能力去應對工作上的需求。

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最後要感謝的是我的父母親與我的家人，有他們在精神及物質方面的支持，我才有半碼這麼無後顧之憂的完成學業，將來的我一定更加的懂事，也會盡一切努力讓你們覺得驕傲。

List of Symbols

Symbols

V_{LSB}	Quantizer step size
OSR	OverSampling Ratio
n	Order of the Sigma-Delta modulator
B	Number of bits in the quantizer
f_S	Sampling Frequency
f_B	Signal Bandwidth
V_{ref}	Reference Voltage of the quantizer
A	Gain of OTA
f_{in}	Frequency of the input signal
ϕ_i	ith phase of a nonoverlap clock
A_{in}	Amplitude of input signal
$\sigma_{jit.}$	standard deviation of clock jitter
C_S	Sampling capacitor
C_I	Integrating capacitor
C_L	Load capacitor of OTA
V_S	Input signal plus feedback DAC signal
τ_1	Time constant of input branch
σ_{VS}	Standard deviation of V_S
τ_2	Time constant of integrator output settling
a_i	gain coefficient of i th integrator
η	percentage of the bottom plate parasitic
T	Absolute temperature
R	Switch ON resistance
N	quantizer levels
gm1	Amplifier transconductance

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Chapter 1

Introduction

1.1 Motivation

Sigma-Delta A/D converters have become popular for high-resolution medium-to-low-speed applications such as digital audio [Bos 88][Nor 89], voice codec, and DSP chip. Recently, ΣΔ ADCs have been applied to higher bandwidth signals, and low power designs are frequently emphasized. For example, in ×DSL [Gag 03][Rio 04] applications, signals up to several MHz must be handled.

The power consumption of the Sigma-Delta A/D converters is very important in all kinds of application. So it is very important that how to design can get the better power consumption. We propose an power consumption model to estimate the power consumption in the discrete time single-loop multi-bit ΣΔ ADCs design.

As illustrated in Fig. 1.1, As illustrated in Fig. 1, in an ADSL modem the downstream data (DS) are transferred at higher frequencies in a wider band as compared to the upstream data (US). Flexible band allocations are standardized, such as frequency division (FDD), frequency overlapping, single upstream (SUS), and double upstream (DUS).1 The developed converter targets a central-office (CO) line-card application. For such transceivers, the analog-to-digital converter (ADC) typically requires 14-bit resolution over an analog signal bandwidth of 276 kHz.

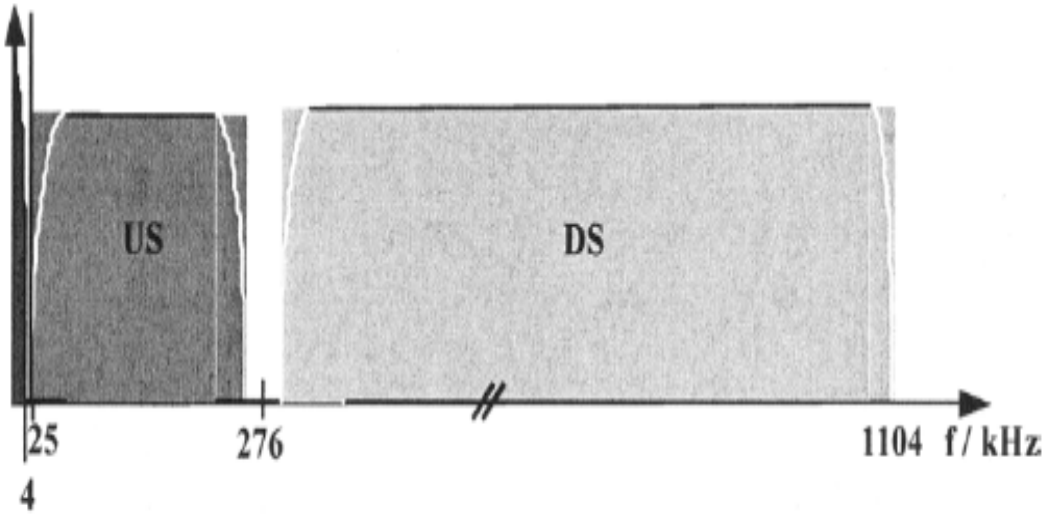


Fig. 1.1 ADSL band allocation (DUS, FDD).

1.2 Organization

This work is organized as follows. In Chapter 2 and Chapter 3, systematic studies of fundamental theory and various architectures of ΣΔ modulator are presented first. In Chapter 4, the power consumption model is derived and verified. In Chapter 5, design the circuit for ADSL-CO application. Conclusions and future works are presented in Chapter 6.

Chapter 2

Fundamental Theorems of Sigma-Delta Modulators

Before we establish the error models of ΣΔ modulators, several important theorems and concepts must be known, such as Nyquist sampling theorem, quantization error and the two most critical techniques in a ΣΔ modulator: oversampling and noise shaping. All topologies of ΣΔ modulators are based on these two techniques. There also have some parameters we must to understand, such as OSR, SNR, and SNDR …etc. This chapter starts from fundamental theorems, and introduces several topologies of ΣΔ modulators.

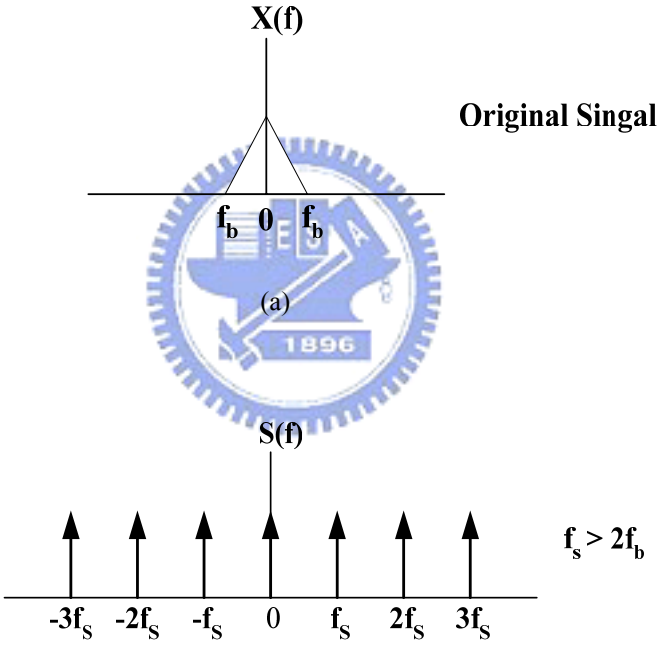
We will illustrate quantization error and analyze quantization noise in an ideal A/D converter and then derives the peak signal-to-noise ratio. The resolution of an A/D converter is determined by signal-to-noise ratio, which is a very important specification in an A/D converter.

2.1 Nyquist Sampling Theorem

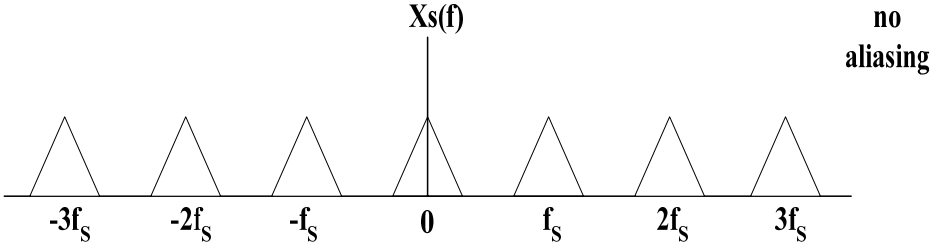
In an analog-to-digital converter, the analog signal from external environment must be converted to discrete-time signal by sampling. However, the sampling rate (fs) and signal bandwidth (f_B) must follow the Nyquist sampling theorem in (2.1):

$$f_S \geqq 2f_B \qquad (2.1)$$

The sampling rate must be higher or equal to twice of signal bandwidth in order to prevent from aliasing. We will illustrate the phenomenon of aliasing by Fig. 2.1. Fig. 2.1(a) and (b) are the spectrums of signal and sample function respectively; from fig. 2.1(c), when sampling rate is twice higher than signal bandwidth, the signal after sampling has no aliasing and it can be perfectly reconstructed by using low pass filters. However, in Fig. 2.1(d), when the sampling rate is lower than twice of signal bandwidth, aliasing will appear in the signal after sampling. The signal having aliasing is difficult to reconstruct to original signal [Mach 96], like Fig. 2.1(e).



(b)



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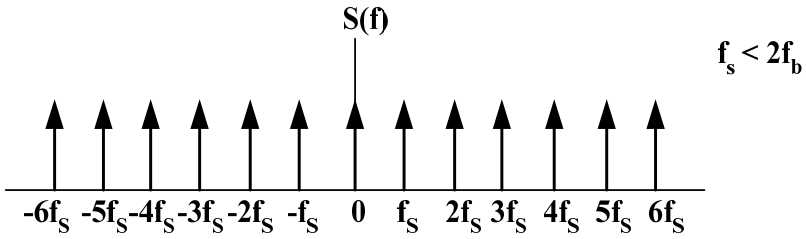

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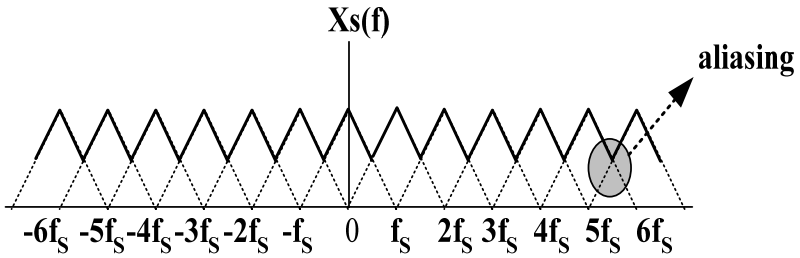


(e)

Fig. 2.1（a）Original signal spectrum（b）Sample function when fs > 2fB（c）Signal spectrum that' sampled by (b)（d）Sample function when fs < 2fB（e）Signal spectrum that sampled by (d).

2.2 Quantization noise and Peak SNR

We can get a discrete-time signal by sampling a continuous-time signal, and this sampled signal can be converted to digital signal. Quantization will appear in this process, the basic concept of quantization is to classify the original signal to different levels according to its level to determine the bit number of this signal, as shown in Fig. 2.2.

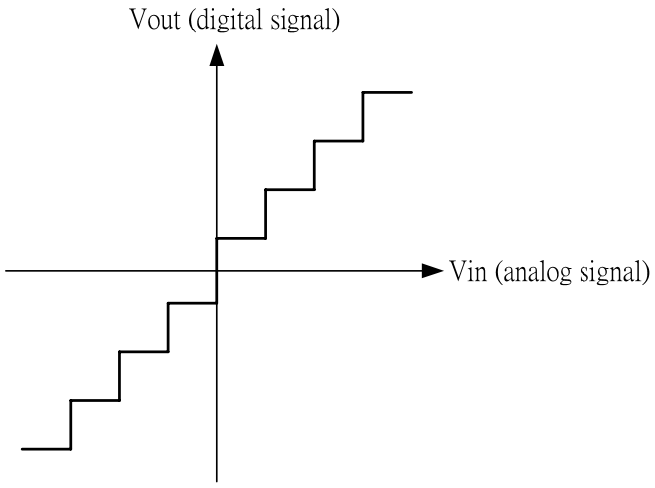


Fig. 2.2 Quantization process

It will have quantization error even in an ideal analog-to-digital converter. As shown in Fig .2.3, we convert the digital signal B to analog signal V_1 by a D/A converter, and then the signal V_1 is subtracted by input signal Vin. The result is the quantization error V_Q, as in (2.2) [Joh 97].

$$V_Q = V_{in} - V_1 \qquad (2.2)$$

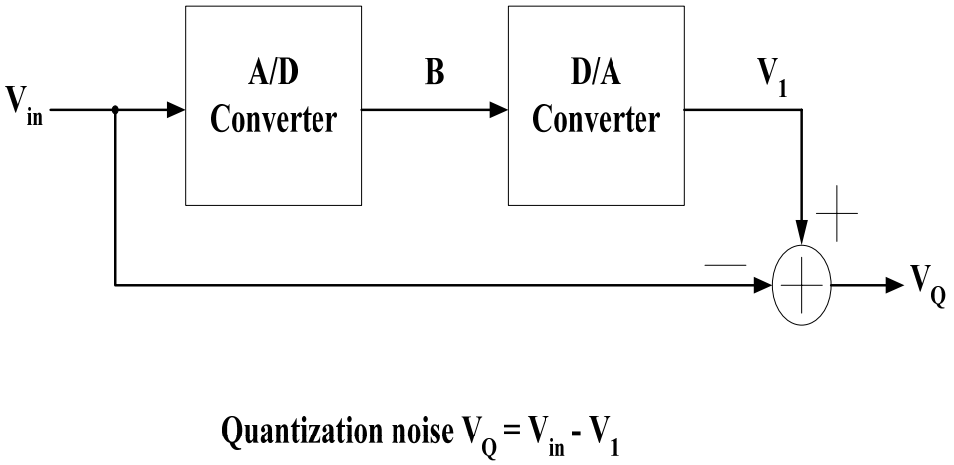


Fig. 2.3 Quantization error caused by A/D converter

The range of quantization error is limited in $\pm V_{LSB}/2$ (as in Fig. 2.4), and we assume the probability density function of quantization error is uniformly distributed between $\pm V_{LSB}/2$ and its mean is zero, as shown in Fig. 2.5. From this assumption, we can easily get the quantization noise power $V_{Q(rms)}^2$ in (2.3).

$$V_{Q(rms)}^2 = \int_{-\infty}^{\infty} x^2 \cdot f_Q(x) \cdot dx = \frac{1}{V_{LSB}} \int_{-VLSB/2}^{VLSB/2} x^2 \cdot dx = \frac{V_{LSB}^2}{12} \qquad (2.3)$$

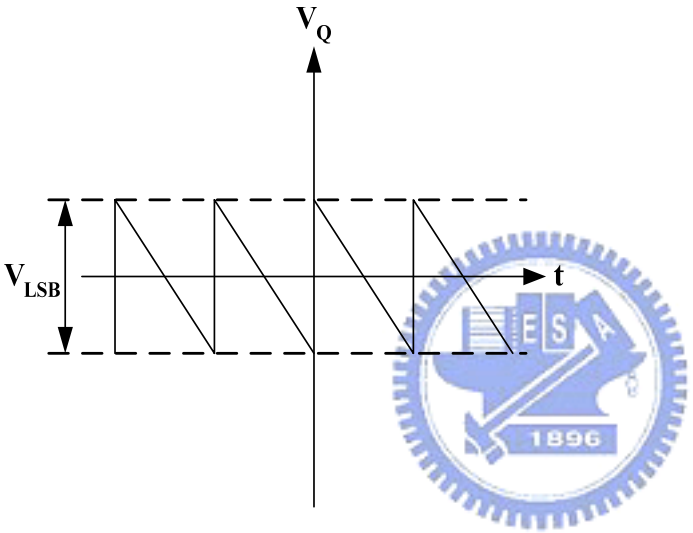


Fig. 2.4 Quantization error range

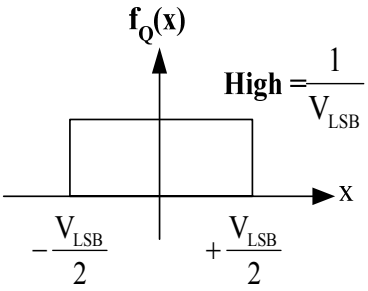


Fig. 2.5 P.D.F of quantization error

From (2.3) we can know the quantization noise power is proportional to square of V_{LSB}, and V_{LSB} can be represented as in (2.4). Therefore, we can say that the quatization noise will reduce by increasing quantization bit number.

$$V_{LSB} = \frac{FS}{2^B} \qquad (2.4)$$

FS=Full scale = $V_{ref+} - V_{ref-}$　　B：Quantization bit number

Assume that input signal is sinusoidal, expressed as $V_{in}(t) = A \sin\omega t$, so the input signal power

$V_{in(rms)}^2$ is as （2.5）. In （2.5）, we define the amplitude of input signal is the full scale of reference voltage, and from (2.3), (2.4) and (2.5), the peak SNR(Peak Signal-to-Noise Ratio) can be derived as in (2.6).

$$V_{in(rms)}^2 = \frac{1}{T}\int_{-T/2}^{T/2}(A\cdot\sin\omega t)^2\cdot dt = \frac{A^2}{2} = \frac{(2A)^2}{8} = \frac{FS^2}{8} \qquad (2.5)$$

$$PSNR = 10\log\left(\frac{V_{in(rms)}^2}{V_{Q(rms)}^2}\right) = 6.02B + 1.76\ dB \qquad (2.6)$$

(2.6) is the result obtained by Nyquist sampling rate. From (2.6), we can know that each additional bit number in quantizer increases 6dB in SNR. In Nyquist A/D converters, increasing the resolution of quantizer (decrease V_{LSB}) while reducing the quantization noise is a general method to reach higher SNR, but this method is sensitive to mismatches of analog device. Therefore, the general Nyquist A/D converter is not easily to implement with high resolution.

2.3 Techniques of Sigma-Delta Modulator

ΣΔ A/D converters are based on oversampling and noise shaping to reach high resolution. Oversampling means the sampling rate is much higher than Nyquist rate, about 8~512 times in general applications. The goal of oversampling is to expand quantization noise to wider range. It can reduce the quantization noise in signal bandwidth and increase the DR (Dynamic range) of input signal. Noise shaping is a technique that moves noise to high frequency, which is done by using discrete time filter and feedback technique. After noise shaping, the noise in high frequency can be filtered out by a digital filter [Nor 97].

2.3.1 Oversampling Technique

First, we made the assumption that quantization noise is a uniform distribution in sampling spectrum so its mean is zero and is a white noise [Raz 01]. The system in Fig. 2.6 just has oversampling function and does not have noise shaping effect. If a A/D converter is sampled in Nyquist rate, then the quantization noise is uniform distributed between $\pm f_B$; if it is sampled by oversampling technique, then quantization noise is uniform distributed between$\pm$ $f_{S2}/2_s$, which is much larger than f_B. As shown in Fig. 2.7, if the signal bandwidth is between $\pm f_B$, then quantization noise in this bandwidth will be reduced by using oversampling technique, which will raise PSNR significantly.

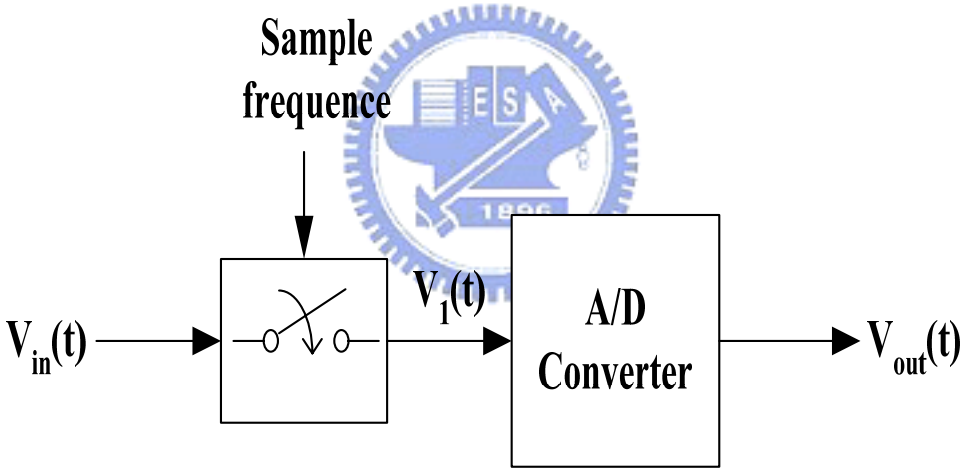


Fig. 2.6 Sampling system

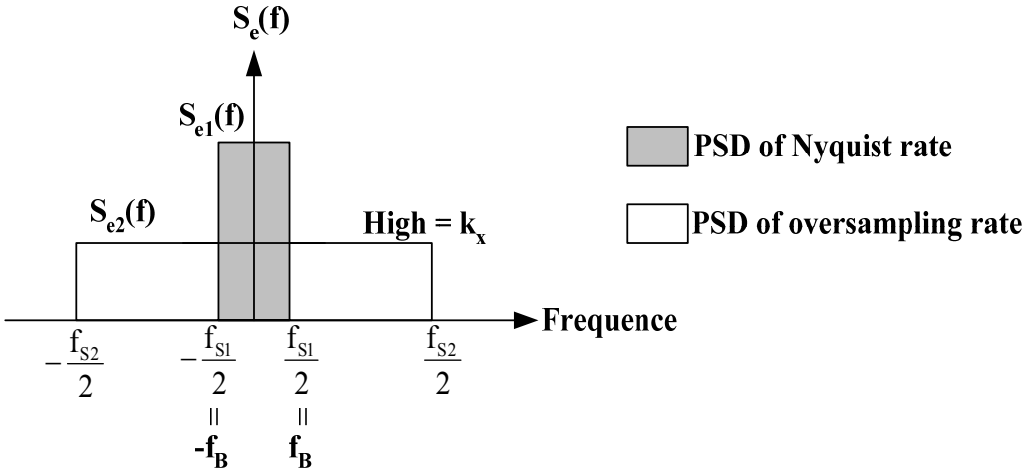


Fig. 2.7 Noise distribution after sampling

In the condition of oversampling, the PSD (Power Spectrum Density) of quantization noise is as $S_{e2}(f)$ in Fig. 2.7 and can be represented as:

$$k_x^2 = \frac{V_{LSB}^2}{12 \cdot f_s} = S_{e2}^2(f) \qquad (2.7)$$

From (2.7) we can estimate the quantization noise in $2f_B$ after oversampling

$$P_Q = \int_{-f_B}^{f_B} k_x^2 \cdot df = \frac{2f_B}{f_s} \cdot \frac{V_{LSB}^2}{12} = \frac{FS^2}{12 \cdot 2^{2B} \cdot OSR} \qquad (2.8)$$

In (2.8), we define a parameter OSR (Oversampling Ratio) as

$$OSR = \frac{f_s}{2f_B} \qquad (2.9)$$

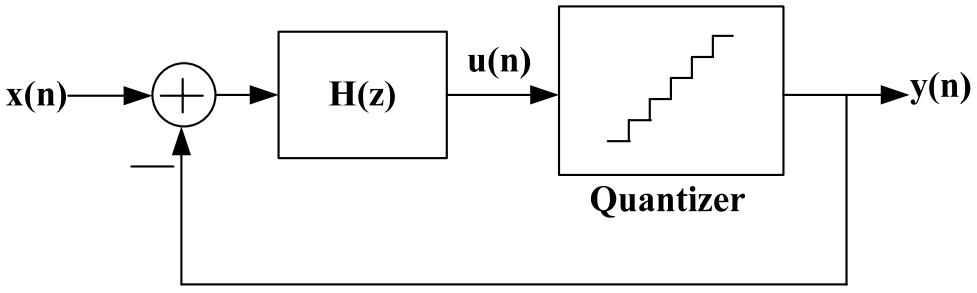
Finally, we can get PSNR from (2.5) and (2.8)

$$PSNR = 10 \log \left(\frac{P_{signal}}{P_Q} \right) = 6.02B + 1.76 + 10 \log (OSR) \qquad (2.10)$$

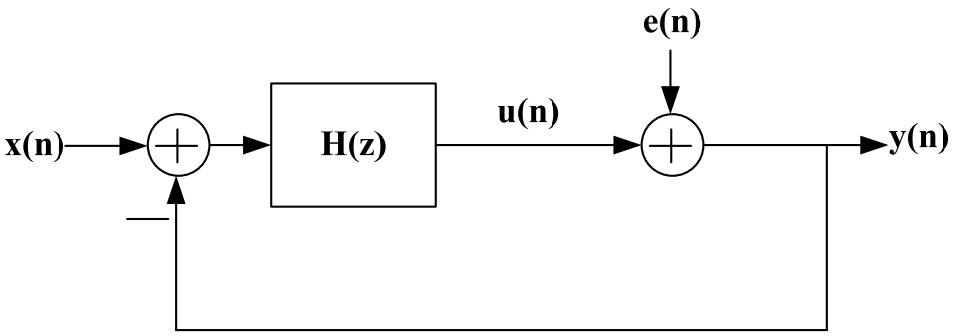
From (2.10), we can find that doubling OSR will increase 3dB in PSNR, which is about 0.5 bit increase in resolution. Although oversampling can reduce quantization noise, it is difficult to reach high SNR when using a low bit quantizer. For example, if we need a 16bit A/D converter, then SNR must be equal to 98dB, if the signal bandwidth is 20KHz, then the sampling rate must equal to $2 \times 10^9 \times 20KHz$, it is impossible to implement. Because at such high frequency, quantization noise is no longer a white noise, it is correlated with input signal. So there is not only oversampling technique, we must add noise shaping technique also, if we want to achieve high resolution.

2.3.2 Noise Shaping

We can model a general ΣΔ modulator and its linear model as shown in Fig. 2.8.



（a）



（b）

Fig. 2.8 (a) General ΣΔ modulator (b) Linear model with quantization noise

From Fig. 2.8(a), we can derive output Y(z) as (2.11)

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z) \qquad (2.11)$$

and define Signal Transfer Function S_{TF} and Noise transfer function N_{TF} as

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \qquad (2.12)$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \qquad (2.13)$$

where H(z) is the transfer function of a discrete time filter. There have two important meanings in (2.12), (2.13). If we want to obtain highest SNR, S_{TF} must be equal to 1, that means the input signal can transfer to output without attenuating; and N_{TF} (z) must be equal to 0, because the quantization noise will not affect output SNR.

In order to make N_{TF} (z) be a high pass filter, so at DC(z = 1), N_{TF} must be 0, and z = 1 is a pole of H(z), so the transfer function H(z) of the discrete filter is as

$$H(z) = \frac{1}{Z-1} = \frac{Z^{-1}}{1-Z^{-1}} \qquad (2.14)$$

Substitute (2.14) into (2.12) and (2.13), we can get

$$S_{TF}(z) = \frac{1}{z} \qquad (2.15)$$

$$N_{TF}(z) = 1-\frac{1}{z} \qquad (2.16)$$

And we substitute z with $e^{j\frac{2\pi f}{fs}}$, then we can plot $|S_{TF}(f)|^2$ and $|N_{TF}(f)|^2$ in frequency domain, as Fig. 2.9. We can find $|N_{TF}(f)|^2$ also increases with frequency, and $|S_{TF}(f)|^2$ is always equal to 1, if we choose signal bandwidth in low frequency, then we can get highest signal power and lowest noise power, from this figure we see that quantization noise is moved to higher frequency significantly, this is the noise shaping effect.

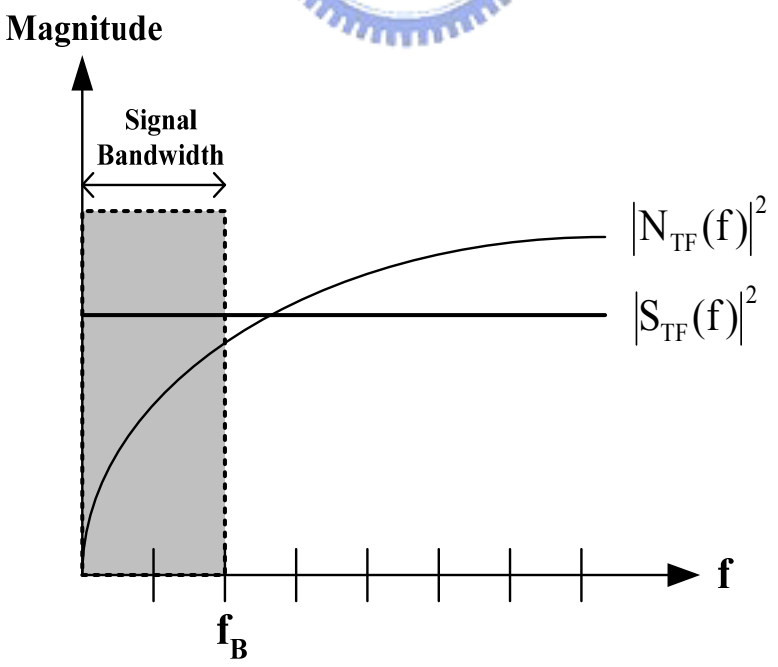


Fig. 2.9 Noise shaping

After noise shaping, we can filter out the noise in high frequency by using digital filter, and we will illustrate its architecture more detail in the next chapter.

Chapter 3

Architectures of Sigma-Delta Modulator

Before we introduce various architectures of ΣΔ modulators, we must to realize the basic architecture of a general ΣΔ A/D converter. Fig. 3.1 is a complete block diagram of a ΣΔ A/D converter [Joh 97], and we can divide it into two different parts. First part is the ΣΔ modulator. The main function of this part is doing oversampling and noise shaping to the input analog signal. Second part is the decimation filter. The main function of this part is to remove noise in high frequency and down sampling the sampling frequency to base band frequency.

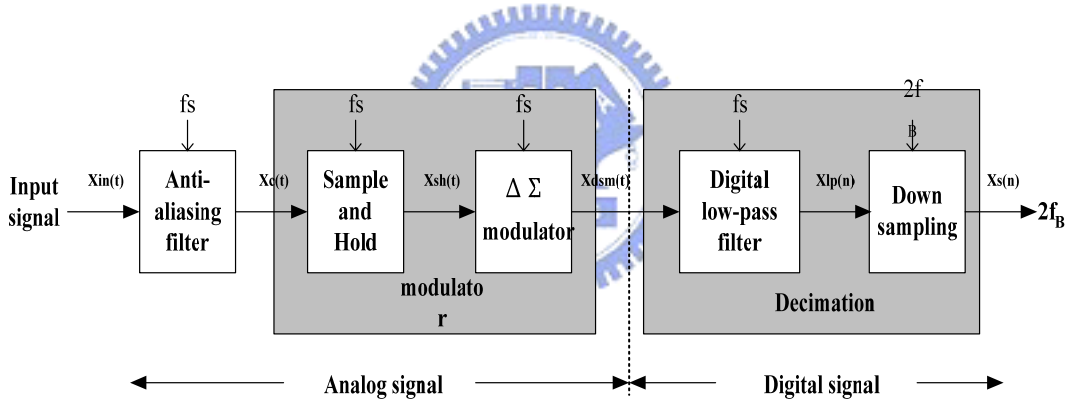


Fig. 3.1 Block diagram of ΣΔ A/D converter

First, the input signal Xin(t) pass an Anti-aliasing filter, the 3dB frequency of this filter is about few times of Nyquist frequency, so signal and noise out of Nyquist frequency is filtered roughly, and this signal goes into the ΣΔ modulator after goes through a S/H circuit. However, in the circuits implement situation, the sample and hold function is included in the circuits of ΣΔ modulator, so the signal Xc(t) will pass this modulator and produces a high speed data code Xdsm(n), because of noise shaping, the quantization noise will appear in high frequency. Finally, we must filter the noise in high frequency and reduce the sampling

frequency to Nyquist frequency by a decimator, and passes the digital signal to the output [Joh 97].

In this chapter, we will focus on the architectures of ΣΔ modulator, because that the noise model and optimal method is focus on this part, we must understand the theorem, benefits and drawbacks of each kinds of ΣΔ modulators. In addition, the implement of decimator is very typical [Ner 02][Mok 94]. In today's technology, DSP processors are also used to replace decimators, so we will introduce this part roughly.

3.1 First-Order Sigma-Delta Modulator

We recall that H(z) in (2.14) is $\frac{Z^{-1}}{1-Z^{-1}}$, substitute it into Fig. 2.8, then we can get a first-order ΣΔ modulator; Analyze transfer function H(z) from time-domain, it indicates that output signal m(t) is obtained by adding the delayed input signal n(t-1) and the delayed output signal m(t-1), so we can express a complete first-order ΣΔ modulator as Fig. 3.2.

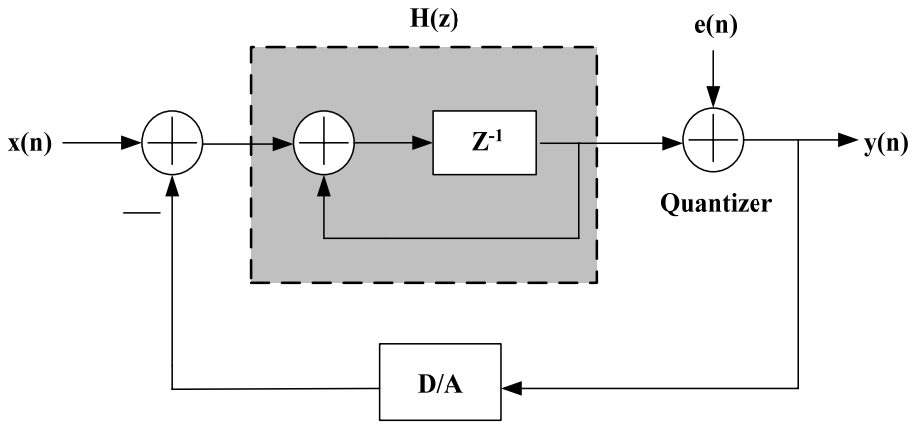


Fig. 3.2 First-order ΣΔ modulator

H(z) in Fig. 3.2 is indicated the effects of delay and accumulation, this is equivalent with an integrator in circuit design, so the three circuits components of ΣΔ modulator are integrator, quantizer and DAC in the feedback path.

A first order ΣΔ modulator's output can represent as

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \qquad (3.1)$$

From (3.1) we can find the signal transfer function is as a delay function, and noise transfer function is as a high pass filter, moves the noise to high frequency. In order to derive PSNR of first order ΣΔ modulator, we must get the magnitude of $N_{TF}(z)$ and $S_{TF}(z)$ in the frequency domain, so we substitute z with $e^{j2\pi \cdot f/f_s}$, and get $|S_{TF}(f)|$ and $|N_{TF}(f)|$ respectively as:

$$|S_{TF}(f)| = |z^{-1}| = |e^{-j2\pi \cdot f/f_s}| = 1 \qquad (3.2)$$

$$N_{TF}(f) = 1 - e^{-j2\pi \cdot f/f_s} = \sin(\frac{\pi f}{f_s}) \times 2j \times e^{-j\pi \cdot f/f_s}$$

$$\Rightarrow \quad |N_{TF}(f)| = 2 \cdot \sin(\frac{\pi f}{f_s}) \qquad (3.3)$$

So the quantization noise in base band $\pm f_B$ can obtain by (2.7) and (3.3)

$$P_Q = \int_{-f_B}^{f_B} S_e^{\,2}(f) \cdot |N_{TF}(f)|^2 df = \int_{-f_B}^{f_B} \frac{V_{LSB}^{\,2}}{12 \cdot f_s} \cdot \left[2\sin\left(\frac{\pi f}{f_s} \right) \right]^2 \cdot df \qquad (3.4)$$

Because that f_B is much lower than f_s, so $\sin(\pi f/f_s)$ is approximate equal to $(\pi f/f_s)$, and P_Q is as

$$P_Q = \frac{V_{LSB}^2 \pi^2}{36} \cdot \left(\frac{1}{OSR}\right)^3 = \frac{FS^2 \cdot \pi^2}{36 \cdot 2^{2B} \cdot OSR^3} \qquad (3.5)$$

From (2.5) and (3.5), if we have the maximum signal power, then PSNR is as (3.6)

$$PSNR = 10 \log\left(\frac{P_{signal}}{P_Q}\right) = 10 \log\left(\frac{3}{2} 2^{2B}\right) + 10 \log\left[\frac{3}{\pi^2}(OSR)^3\right]$$

$$= 6.02B + 1.76 - 5.17 + 30 \log(OSR) \qquad (3.6)$$

From (3.6), we find that each octave of OSR, PSNR will increase 9dB, increase 1.5 bit in resolution. Compare (3.6) with (2.10) that only has oversampling effect; we can find that 1st order noise shaping increases the performance of ΣΔ modulator.

3.2 Single-Loop Second-Order Sigma-Delta Modulator

When the discrete time filter in Fig. 2.8 is replaced by two cascade integrator, then it is a second order ΣΔ modulator, output of the first integrator is only connecting with the input of the second integrator, it is shown in Fig. 3.3

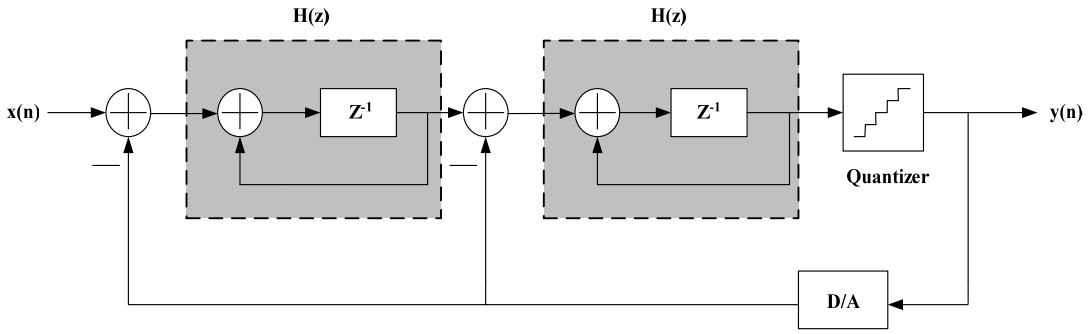


Fig. 3.3 Single loop second order ΣΔ modulator

Then the output of it can easily be derived as

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2E(z) \quad (3.7)$$

where S_{TF} and N_{TF} is as

$$S_{TF}(z) = z^{-2} \quad (3.8)$$

$$N_{TF}(z) = (1- z^{-1})^2 \quad (3.9)$$

Using the same method in (3.3) (3.4), we can obtain

$$|S_{TF}(f)| = 1 \quad (3.10)$$

$$|N_{TF}(f)| = \left[2 \cdot \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \quad (3.11)$$

$$P_Q = \frac{V_{LSB}^{\ 2} \cdot \pi^4}{60 \cdot OSR^5} = \frac{FS^2 \cdot \pi^4}{2^{2B} \cdot 60 \cdot OSR^5} \quad (3.12)$$

So finally, PSNR of the second order ΣΔ modulator is as

$$PSNR = 10 \log(\frac{P_{signal}}{P_Q}) = 10 \log(\frac{3}{2}2^{2B}) + 10 \log[\frac{5}{\pi^4}(OSR)^5]$$

$$= 6.02B + 1.76 - 12.9 + 50 \log(OSR) \quad (3.13)$$

In the single loop second order architecture, each octave of OSR can increase PSNR by 15 dB, it is equivalent to 2.5 bit in resolution. If we compare (3.13), (3.11) with $|NTF(f)|=1$ that without noise shaping, as Fig. 3.4, we can find that in our needed signal bandwidth, the

quantization noise is highest when $|NTF(f)|=1$, and that with second order noise shaping is smallest among this figure [Joh 97].

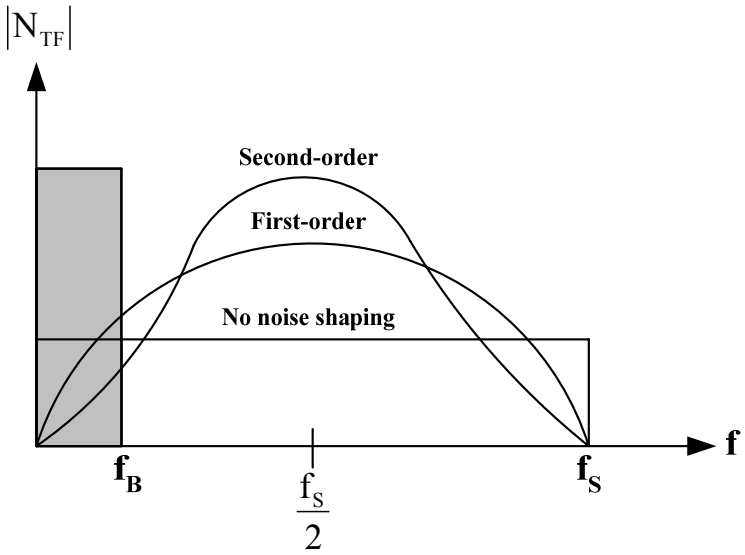


Fig. 3.4 Comparison of noise shaping techniques

3.3 Single-Loop High Order Sigma-Delta Modulator

Fig. 3.5 is a single loop high order ΣΔ modulator, from the derivation in Section 3.1 and Section 3.2, we can get the quantization noise P_Q in signal bandwidth is as

$$P_Q = \frac{V_{LSB}^{\ 2}}{12} \cdot \frac{\pi^{2L}}{2L+1} \cdot \left(\frac{1}{OSR}\right)^{2L+1} \quad , L：\text{order} \qquad (3.14)$$

and its PSNR is

$$PSNR = 6.02B + 1.76 - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \qquad (3.15)$$

In the application of high order ΣΔ modulator, (6L+3)dB increases in SNR when OSR is octave, so PSNR can be raised by increasing the order of the system, especially at large oversampling ratio. But sometimes in high order architecture, the performance will be worsen than result predicted by (3.13), because of the stability problem, it will make less effective noise shaping function, so the quantization noise will not be suppressed completely.

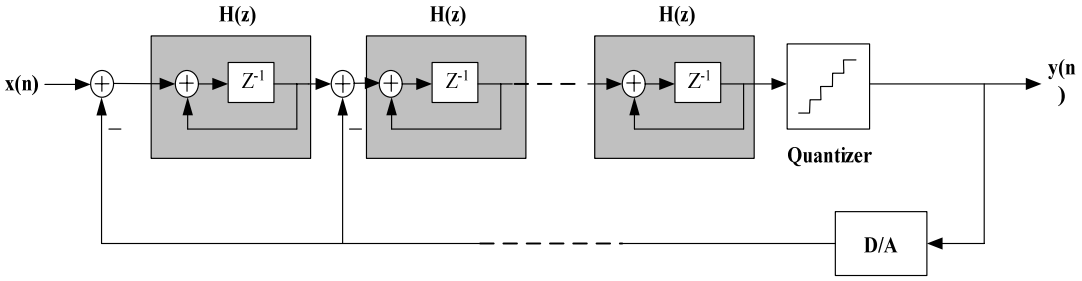


Fig 3.5 Single-loop high order ΣΔ modulator

3.4 Interpolative Sigma-Delta Modulator

Interpolative is a kind of high order ΣΔ modulator, it changes connection of some stages, adds some feedforward paths and feedback paths in order to suppose more aggressive noise shaping effect, Fig. 3.6 is a four-order interpolative architecture ΣΔ modulator [Cha 90].

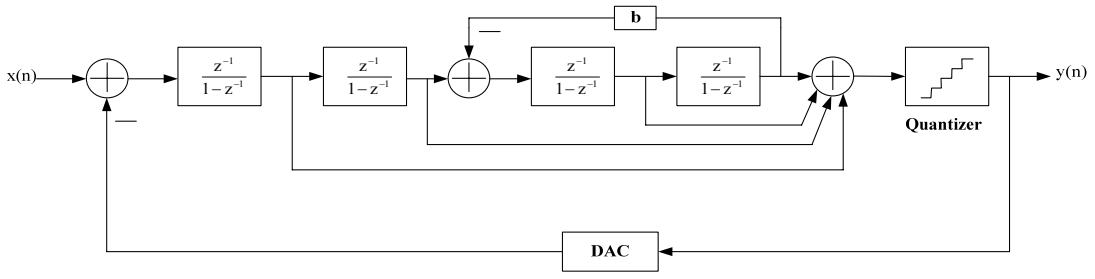


Fig. 3.6 Four-order interpolative architecture

This architecture also has stability problem, when the order L increases, each integrator produces one pole, and when the order is higher, poles of this system will also increase, and it will cause unstable situation, so the range of integrator gain will be limited; if the range of integrator gain is small, oscillation will appear in the circuits. Another is the considerations of clock control, when we use SC (switched-capacitor) to implement the integrator, each integrator needs two clocks to control its operation, and we will need more clock to control the integrator when the order of system increases, it will produce more problems.

3.5 MASH Architecture

MASH (Multi-stage noise shaping) architecture is also called cascade architecture, which is a method that cascades several low order loops modulator in order to get high order noise shaping effect. The fundamental ideal of MASH is delivering quantization noise of front stage to input of next stage, and combining the digital outputs of all the stages with proper transfer function in digital domain, only the quantization noise of last stage will appear at the output, and the orders of N_{TF} is the same with total orders in the cascade $\Sigma\Delta$ modulator. Fig 3.7 is a three-order cascade $\Sigma\Delta$ modulator, its is the combination of a second-order and first-order $\Sigma\Delta$ modulator, so also called 2-1 cascade architecture [Wil 94].

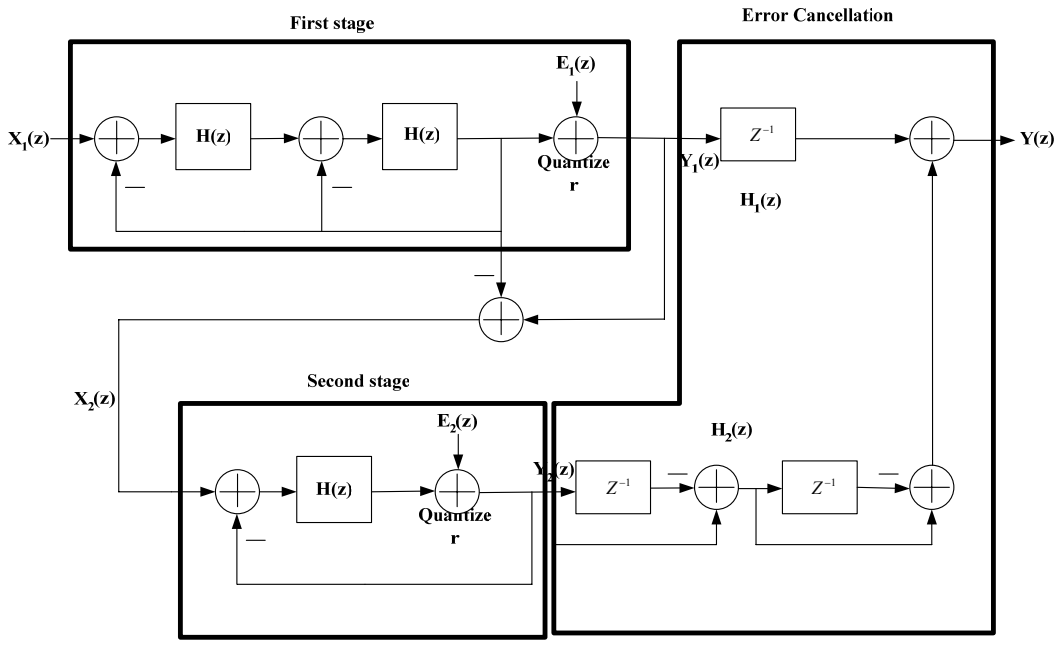


Fig. 3.7 2-1 architecture MASH ΣΔ modulator

From Fig. 3.7, we can derive the first stage output $Y_1(z)$ can be represented as

$$Y_1(z) = z^{-2}X_1(z) + (1-z^{-1})^2E_1(z) \quad (3.16)$$

Output of second stage $Y_2(z)$ is as

$$Y_2(z) = z^{-1}X_2(z) + (1-z^{-1})E_2(z) \quad (3.17)$$

and overall output of MASH Y(z) is as

$$Y(z) = H_1(z)Y_1(z) + H_2(z)Y_2(z) \quad (3.18)$$

and we can say that second stage input $X_2(z)$ is almost the same with $E_1(z)$, in order to eliminate first stage quantization noise $E_1(z)$, from (3.16) ~ (3.18), we can define the error cancellation functions $H_1(z)$ and $H_2(z)$ as

$$H_1(z) = z^{-1} \quad (3.19)$$

$$H_2(z) = (1-z^{-1})^2 \quad (3.20)$$

From (3.16)~(3.20), $E_1(z)$ can be eliminated, and second stage quantization noise $E_2(z)$ is shaped by third-order noise shaping function, and the MASH output Y(z) is as

$$Y(z) = z^{-3}X_1(z) + (1-z^{-1})^3E_2(z) \quad (3.21)$$

The most significant advantage of this architecture is that stability is not an issue, because it is composed by several low-order systems, and the quantization noise will not be amplified stage by stage, so its stability is good. Most important, the noise shaping function is equivalent as high order ΣΔ modulator, so it is popular in recent publications [Rio 04][Vle 01]. However, there also have some drawbacks of this topology; it is sensitive to the circuits' imperfections, such as finite DC gain of OTA, variance of integrator gain due to capacitor mismatch and non-zero switch resistance. These are all practical considerations when we design a MASH architecture ΣΔ modulator [Gag 03].

3.6 Multi-bit Quantizer Sigma-Delta Modulator

The demands of high resolution and high bandwidth ADC are more and more in recent years. In a high signal bandwidth, OSR of ΣΔ ADC can't be too high, and the peak SNR of a ΣΔ modulator with such limited OSR can't satisfy of high resolution applications, if we use higher order architecture, then the performance will degrade due to instability. So the most general method to increase performance is to use multibit quantizer. The most obvious advantage of using multibit quantizer is that the distance between quantizer level V_{LSB} in (2.4)

is much smaller due to increasing of B, and according to (2.3), the power of quantization noise is attenuated. Fig. 3.8 is the results of theoretical peak SNR of ΣΔ modulator versus oversampling ratio, with different order and quantizer bits, it is noted that peak SNR of the same OSR is increase 6 dB with each additional bit number in quantizer, and at low OSR, low order higher bit number architecture has equivalent performance as high order architecture. This result is usable for high bandwidth applications, and the power consumption of digital circuit in ΣΔ modulator is reduced due to lower sampling rate [Pel 99].

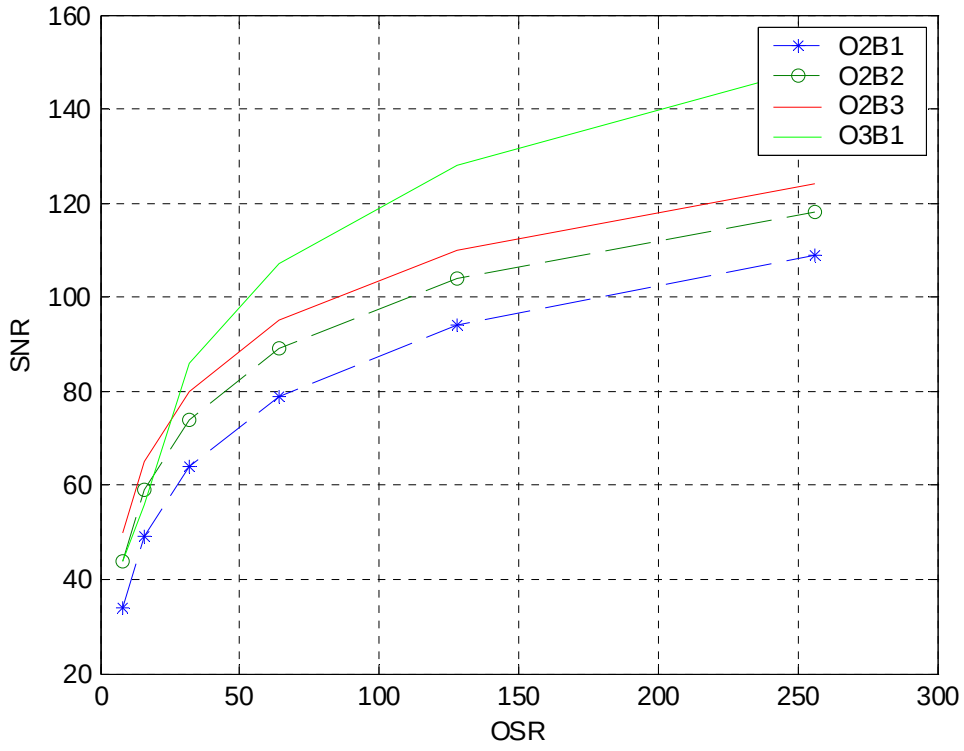


Fig. 3.8 SNR vs. OSR with different quantizer bit number

Because of using multi-bit quantizer, so we also need to use multi-bit DAC(Digital-to Analog Converter) to transfer the digital output to analog signal, and feed it back to integrator. The most significant disadvantage is the non-linearities introduced by multi-bit DAC can degrade the performance of ΣΔ converter, like Fig. 3.9. It is a linear model of multi-bit ΣΔ

modulator, where E(Q) and E(D) represent the quantization noise and feedback DAC noise respectively. The values of these capacitor elements in DAC will not equal to ideal values that we need, it is due to process variation, typical value of mismatch in modern CMOS technology is about 0.05% ~ 0.5%. In recent years, so many researches are make efforts on reduce DAC noise due to mismatch, such as trimming [Nor97], Dynamic element matching(DEM)[Mil 03][Reb 90], although trimming is effective, but it has a expensive production step. So, DEM becomes more and more popular because of its efficiency and cheaper cost.

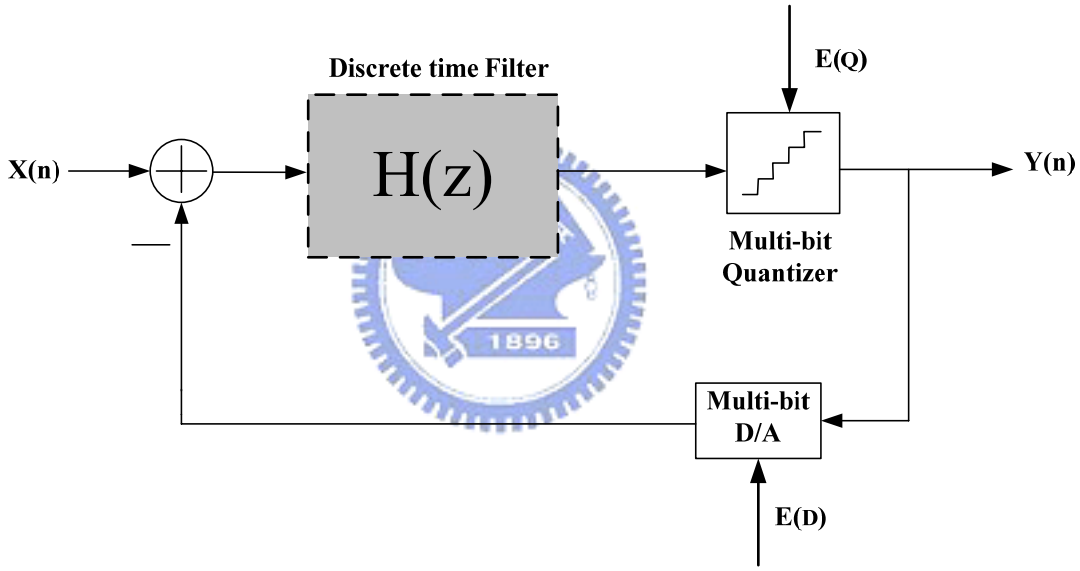


Fig. 3.9 Multi-bit architecture

3.7 Multi-bit Sigma-Delta Modulator use DEM Technique

Dynamic element matching is a different approach to decrease the DAC noise, it is used to improve the linearity of pure DACs [Pla 79], but now it is most used in inner DAC of multi-bit ΣΔ modulator. A DAC with DEM technique is illustrated in Fig. 3.10, 2^B bits

thermometer code is put into the element selection logic block, and the function of element selection logic is try to select DAC elements in such way let the errors introduced by DAC average to zero for several operation periods. Because the DEM block is located in feedback loop, so its delay must be very small prevent to degrade the performance of ΣΔ converter, therefore the algorithm used in the DEM block must be simple. There are several techniques of DEM, such as Randomization [Car 89], Clocked Averaging (CLA) [Pla 79], Individual Level Averaging (ILA) [Che 95], Data Weighted Averaging (DWA) [Bai 95], Randomization is the first approach to use DEM technique in ΣΔ ADC, and DWA offers a good performance to reduce DAC error, in this section, an overview introduction of these two algorithms will be presented, and the operation principle of them will be explained.

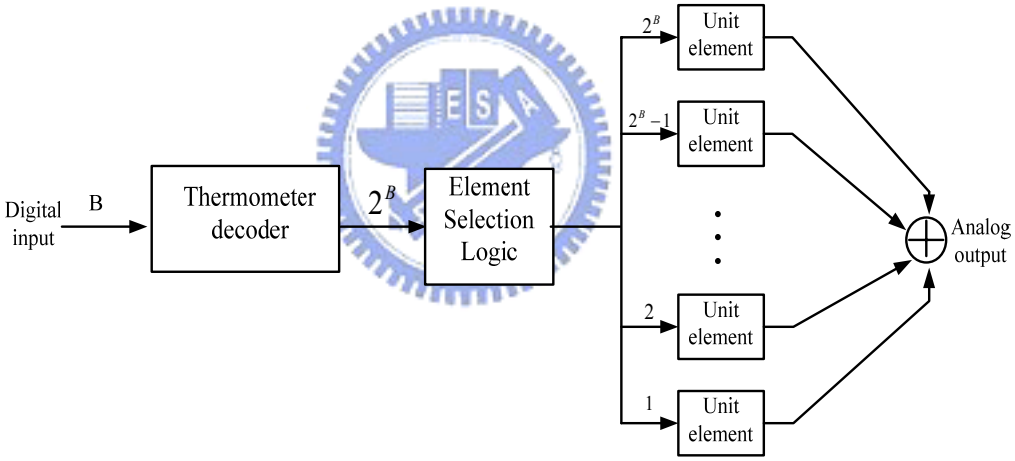


Fig. 3.10 A B-bit DAC with DEM technique

3.7.1 Randomization Technique

The main operation principle of randomization is that the element selection logic performs as a randomizer. In each clock period, the randomizer selects DAC elements randomly to generate the output of DAC. If the randomizer is ideal, then the DAC noise will become uncorrelated with each other. Simulation results show that randomization DEM

technique reduces the noise floor from DAC error by several dB, but it still be a white noise in low frequency. Fig. 3.12 is the output spectrum of a second-order ΣΔ modulator with a 0.1% capacitor mismatch, it is notable that the noise floor of randomization DEM is lower than that without any calibration technique in the feedback DAC.

3.7.2 Data Weighted Averaging (DWA)

DWA is a efficiently method to reduce DAC mismatch noise, it uses one register to remember the capacitor last time used, and always points to the first unused unit capacitor in this clock, so DWA rotates through all the unit capacitors such that all capacitors are used at the maximum possible rate. From this algorithm, each elements is used the same number of times in long interval, this ensures that the errors caused by the DAC average to zero quickly. In Fig. 3.11, it is a 4-bit DAC and the shaded boxes are the number of 1's in the thermometer code. Assumes that the input codes sequence is 8, 8, 10, 9, 10, 10, 11, 11, 12, 11, 14, 11, 14, 13, 12, 15... Fig. 3.12 is the simulation results of a third order ΣΔ modulator, we can see that without DEM has highest noise floor and DWA works as a first order noise shaping function of DAC noise, ideal DAC only with quantization noise has third-order noise shaping.

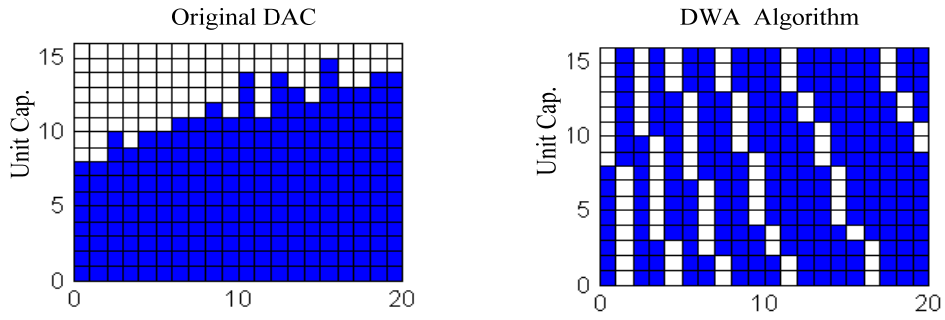


Fig. 3.11 Operation principle of the DWA algorithm

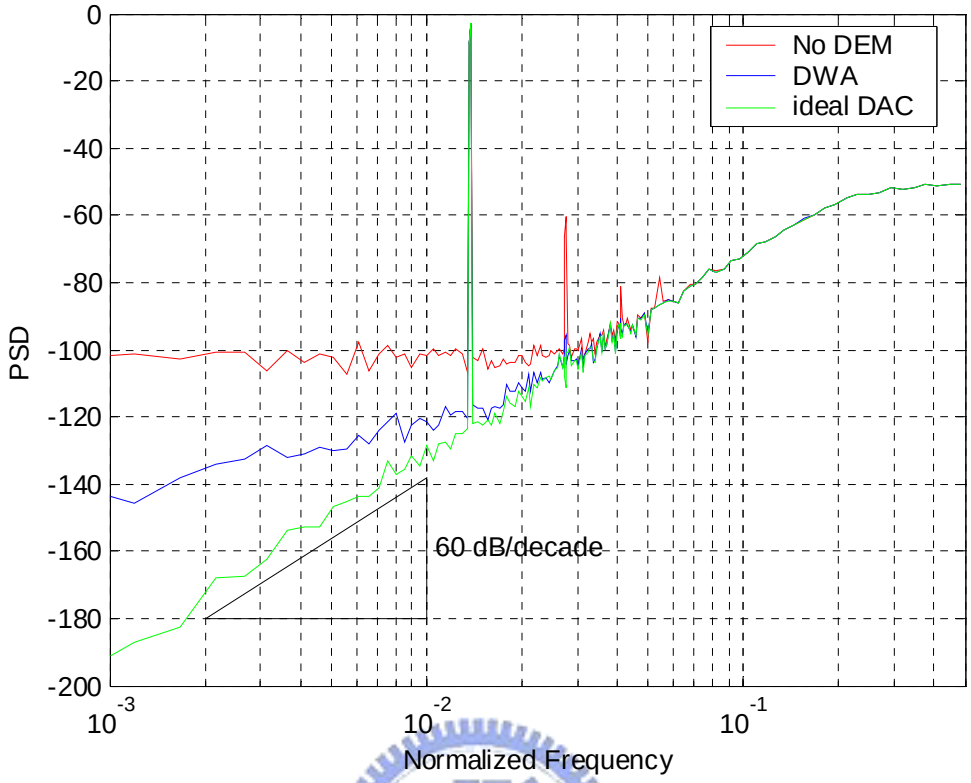


Fig. 3.12 Output spectrum with three kinds of DAC

Another consideration is the sub-ADC(quantizer) of the ΣΔ modulator, we usually use Flash A/D as the multi-bit quantizer because of its high speed, but Flash A/D has a significant disadvantage is that the number of comparators of it is proportional to 2^B. That means a 6 bit quantizer needs 64 comparators, the occupied area of comparator may not much, but in modern SOC applications, the problems of power and area are important, so it becomes one limitation of multi-bit quantization.

ΣΔ A/D converter is attractive for high resolution application, for higher signal bandwidth, we increase system order to raise SNR, but it still have stability problem. So people develop MASH and multi-bit architecture to improve its performance. Finally, we classify they into low order, high order, MASH and multi-bit four kinds of architecture, and compare their advantage and disadvantage as Fig. 3.13 [Med 99]

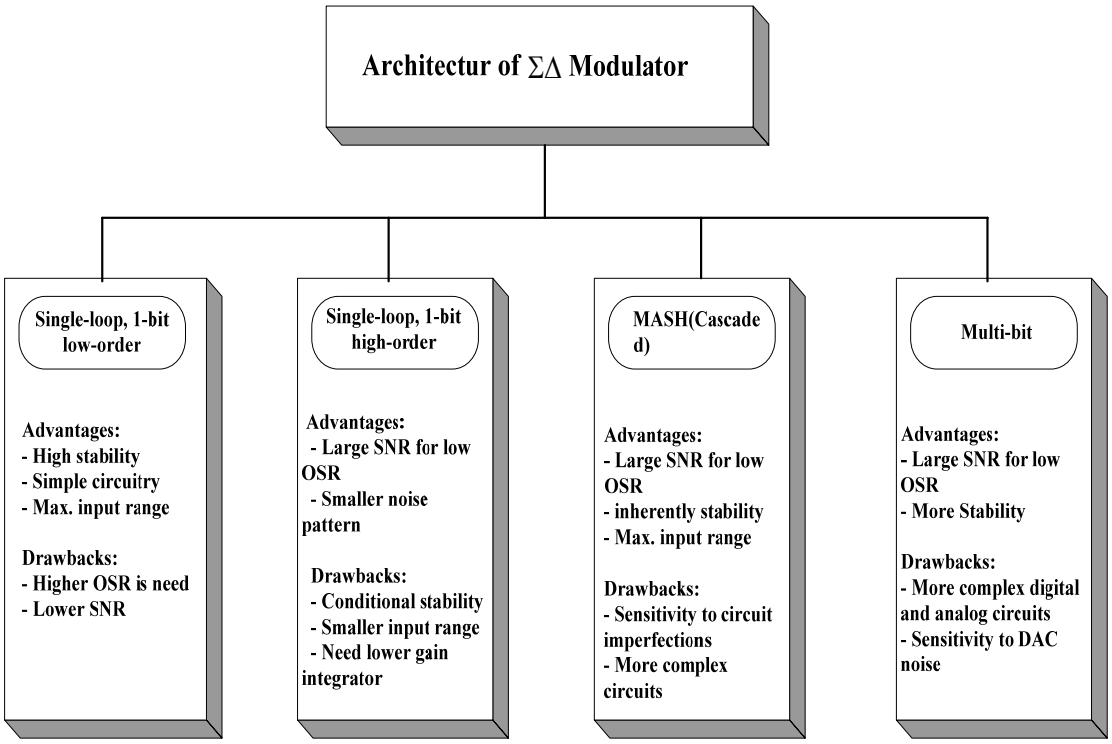


Fig. 3.13 Comparison of ΣΔ modulator architectures

3.8 Decimator

In ΣΔ A/D converter, digital decimator is used to process digital signal of the quantizer output, the high speed data word after oversampling modulation can't be used directly. Because there have original signal and quantization noise among it, so the main function of decimator is to convert the oversampled B-bit output words of the quantizer at a sampling rate of fs to N-bit words at Nyquist rate of input, and removes the noise out of signal band. In order to prevent the noise introduced by other frequency, the decimator filter must have very flat signal pass-band, and sharp transition region and enough signal attenuation in stop band. Two-stage decimator is used in a general situation, because that single stage decimator is difficult to convert sampling rate to Nyquist rate in 1 time and without degrading SNR. In the

first stage, we can down-sample the sample frequency to 2~4 times of Nyquist frequency, and in the second stage, we can use IIR or FIR filter that have high linearity [Nor 97]. For a large OSR, multi-stage decimator is used.

3.9 Performance Metrics for a ΣΔ Modulator

In order to understand the performance merits used to specify the behavior of ΣΔ modulator, several specifications concerning the performance are discussed [Gee 02].

- **Signal to Noise Ratio:** The SNR of a data converter is the ratio of the signal power to the noise power, measured at the output of the converter for a certain input amplitude. The maximum SNR that a converter can achieve is called the peak SNR.

- **Signal to Noise and Distortion Ratio:** The SNDR of a converter is the ratio of the signal power to the power of the noise and the distortion components, measured at the output of the converter for a certain input amplitude. The maximum SNDR that a converter can achieve is called the peak SNDR.

- **Dynamic Range at the input:** The DRi is the ratio between the power of the largest input signal that can be applied without significantly degrading the performance of the converter, and the power of the smallest detectable input signal. The level of significantly degrading the performance is defined as the point where the SNDR is 6 dB bellow the peak SNDR. The smallest detectable input signal is determined by the noise floor of the converter.

- **Dynamic Range at the output:** The dynamic range can also be considered at the output of the converter. The ratio between maximum and minimum output power is the dynamic

range at the output DR_O, which is exactly equal to peak SNR.

- **Effective Number of Bits:** ENOB gives an indication of how many bits would be required in an ideal quantizer to get the same performance as the converter. This numbers also includes the distortion components and can be calculated from (2.6) as

$$\text{ENOB} = \frac{SNR - 1.76}{6.02} \tag{3.22}$$

- **Overload Level:** OL is defined as the relative input amplitude where the SNDR is decreased by 6dB compared to peak SNDR

Typically, these specifications are reported using plots like Fig. 3.14. This figure shows the SNR and SNDR of the ΣΔ converter versus the amplitude of the sinusoidal wave applied to the input of the converter. For small input levels, the distortion components are submerged in the noise floor of the converter. Consequently, the SNDR and SNR curves coincide for small input levels. When the input level increases, the distortion components start to degrade the modulator performance. Therefore, the SNDR will be smaller than the SNR for large input signals. Note that these specifications are dependent on the frequency of the input signal and the clock frequency of the converter. Fig. 3.14 also shows that SNDR curves drop very fast once the overload point is achieved. This is due to the overloading effect of the quantizer which results in instabilities.

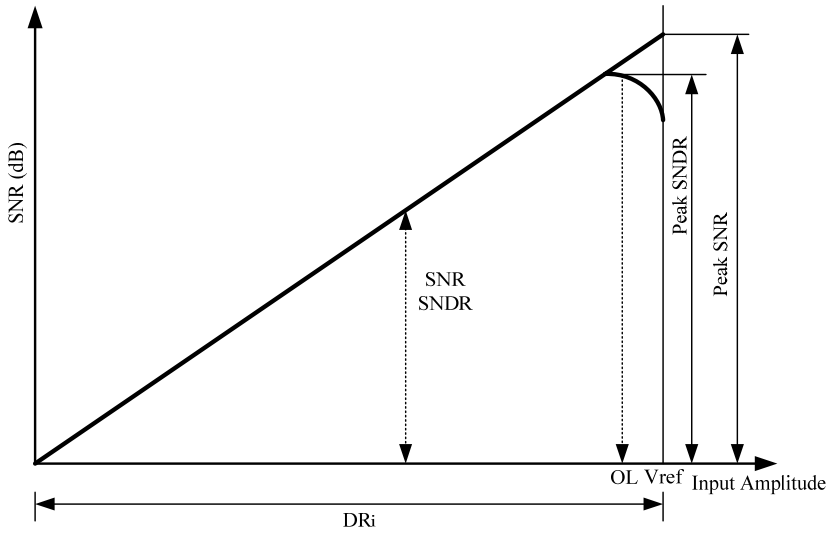


Fig. 3.14 Performance characteristic of a $\Sigma\Delta$ converter

Chapter 4

Models of Multi-Bit Sigma-Delta Modulator Power

The power estimation is presented for a sigma-delta converter with a certain accuracy and bandwidth specification. The influence of several design choices on the power-bandwidth-resolution trade-off will be discussed. This leads to some general design considerations.

The power estimation can be derived into the analog power consumption and the digital power consumption. The analog power consumption mainly includes the OTA of the integrator, the comparator of the quantizer, and the DAC from the quantizer to the integrator. The digital power consumption mainly includes the logic in the quantizer, the dynamic element matching algorithm, the CMOS switch and the clock generator. But in this paper, the digital power consumption only considers the CMOS switch and the clock generator.

4.1 Integrator power

The first considered power consumption is the integrator of the analog power consumption. The most power consumption is the OTA in the integrator. So, the total power consumption of the OTA can be written as

$$P_{OTA} = I_{OTA} \cdot V_{DD}$$

$$= k_{OTA} \cdot I_B \cdot V_{DD} \tag{4.1}$$

where I_{OTA} represents the total current of the OTA, I_B represents the bias current of the OTA, k_{OTA} represents the ratio of the total current of the OTA to this bias current and V_{DD} represents the supply voltage of the OTA. The factor k_{OTA} which depends on the number of current branches and the relative amount of current in each of them.

The ratio of the total current of the OTA to this bias current is represented by

$$I_B = \frac{1}{2} \cdot \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot V_{eff}^{\ 2} \tag{4.2}$$

Where $V_{eff} = V_{GS} - V_{TH}$

For CMOS implementations, the OTA transconductance is related to the transconductance of a MOS transistor used in a differential input pair. The transconductance of the OTA to current relationship for a differential input pair is given by

$$g_m = \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot V_{eff} = \frac{2I_B}{V_{eff}}. \tag{4.3}$$

So I_B can be written as

$$I_B = \frac{1}{2} \cdot g_m \cdot V_{eff} \tag{4.4}$$

where I_B represents the bias current of each transistor of the differential pair and V_{eff} represents the overdrive voltage.

The effective closed-loop load capacitance can be written as

$$C_{eq,cl} = C_S \cdot \left(1 + \frac{C_P}{C_S} + \frac{C_L}{C_S}\left(1 + \frac{C_S}{C_I}\left(1 + \frac{C_P}{C_S}\right)\right)\right)$$

$$= k_{Ceq,cl} \cdot C_S \tag{4.5}$$

where $k_{Ceq,cl}$ represents the ratio between the effective closed-loop load capacitance and the sampling capacitance. It depends on the relative size of C_P and C_L compared to C_S. These sizes can only be determined when the OTA is designed since they depend on parasitic capacitances. The ratio of C_S to C_I is determined by loop-coefficient a_1 of the sigma-delta converter[Gee 02].

The gain-bandwidth product of operational amplifier of the first integrator is a function of the equivalent load capacitor $C_{eq,cl}$ and of the transconductance g_m, according to

$$f_{cl2} = \frac{g_m}{2\pi \bullet C_{eq,cl}} = \frac{g_m}{2\pi \bullet k_{Ceq,cl} \bullet C_S}. \tag{4.6}$$

The bias current of each transistor of the differential pair combined the gain-bandwidth product of operational amplifier with the equivalent load capacitor, so I_B can be written as

$$I_B = \frac{1}{2} g_m \cdot V_{eff}$$

$$= \frac{1}{2} \bullet f_{cl2} \cdot \left(2\pi \cdot k_{Ceq,cl} \cdot C_S\right) \cdot V_{eff}$$

$$= \pi \cdot k_{Ceq,cl} \cdot C_S \cdot V_{eff} \cdot f_{cl2} \tag{4.7}$$

It may be stated from the above results that the total power consumption of first OTA can

be written as

$$P_{OTA} = I_{OTA} \cdot V_{DD}$$

$$= k_{OTA} \cdot I_B \cdot V_{DD}$$

$$= k_{OTA} \cdot \left(\pi \cdot k_{Ceq,cl} \cdot C_S \cdot V_{eff} \cdot f_{cl2} \right) \cdot V_{DD}$$

$$= \pi \cdot k_{OTA} \cdot k_{Ceq,cl} \cdot C_S \cdot f_{cl2} \cdot V_{eff} \cdot V_{DD} \qquad (4.8)$$

The power consumption of the first integrator is almost consumed in the first OTA. So this equation can be extended to the total analog power consumption of all the integrators in a sigma-delta converter by introducing the factor $k_{\Delta\Sigma}$ which represents the ratio between the total current consumption of all the OTAs and the first OTA. The total analog power consumption of the integrators in a sigma-delta converter is given by

$$P_{an} = I_{\Delta\Sigma} \cdot V_{DD}$$

$$= k_{\Delta\Sigma} \cdot I_{OTA} \cdot V_{DD}$$

$$= \pi \cdot k_{\Delta\Sigma} \cdot k_{OTA} \cdot k_{Ceq,cl} \cdot C_S \cdot f_{cl2} \cdot V_{eff} \cdot V_{DD} \qquad (4.9)$$

The analog power consumption is not included the power consumption of the quantizer yet.

k_{OTA} indicates how much current the OTA consumes, relative to the bias current of one transistor of the differential input pair. This depends on the chosen OTA architecture. Three different alternatives are now briefly compared.

A single-stage telescopic OTA is shown in the Figure 1[Kus 98]. It can provide a large gain, has an excellent frequency performance and has only two current branches. This means k_{OTA} is only two. The mean drawback is the small output swing since it has five stacked transistors which have to remain in saturation region. Furthermore, it becomes difficult to employ the same common-mode levels at the input and the output of the OTA.

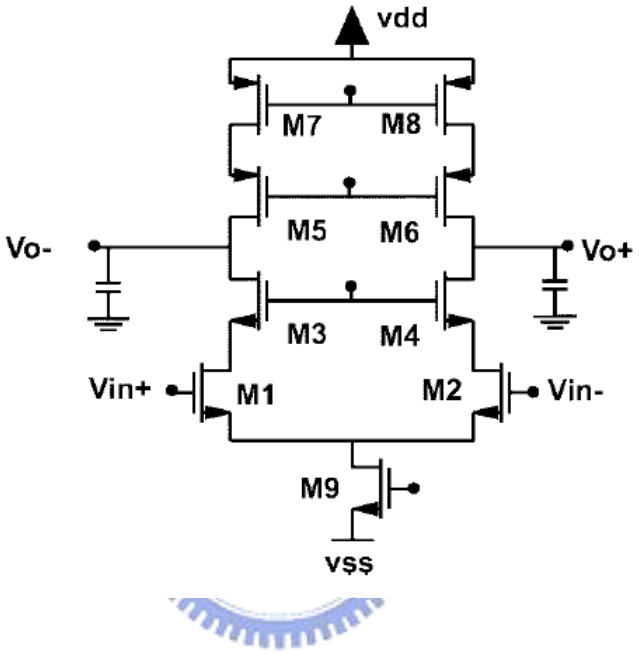


Figure 4.1 A single-stage telescopic OTA

The folded cascode OTA is shown in the Figure 2[Kus 98]. It can provide a large gain, and has an excellent frequency performance. The frequency performance of the folded cascade OTA is worse than the frequency performance of the telescopic OTA because more parasitic capacitances are associated with the non-dominant pole. The folded cascode OTA has two current branches that resulting in a value of four for k_{OTA}.

Compared with the telescopic OTA, the main advantages of the folded cascade OTA are the large output swing and the larger range for the input common-mode level. Because the folded cascode OTA only has four transistors need to remain in saturation.

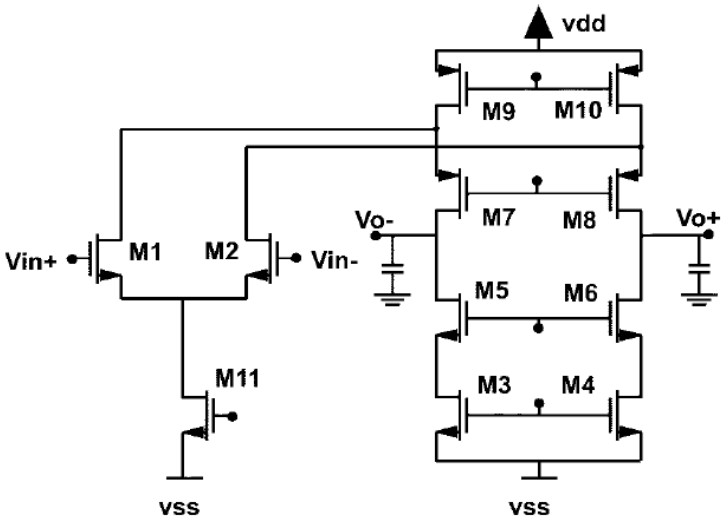


Figure 4,2 The folded cascode OTA

The two-stage Miller-compensated OTA is shown in the Figure 3[Kus 98]. It also can provide a large gain, but the frequency performance is worse. The dominant pole is determined by the compensation capacitance. The non-dominant pole is determined by the ratio of the transconductance of the output stage to the load capacitance. Compared with the telescopic OTA and the folded cascade OTA, the k_{OTA} of the two-stage Miller-compensated OTA is difficult to get it. Because the two-stage Miller-compensated OTA must improve the frequency performance by the compensation capacitance. The transconductance of the two-stage Miller-compensated OTA to current relationship for a differential input pair is

$$g_{m1} = \frac{2I_{B1}}{V_{GS1} - V_T} . \tag{4.10}$$

And, the bandwidth of the two-stage Miller-compensated OTA to transconductance relationship for a differential input pair is

$$\frac{g_{m1}}{C_M} = 2\pi \cdot f_{cl2} \tag{4.11}$$

where C_M is the Miller compensation capacitance.

So, the bandwidth of the two-stage Miller-compensated OTA to current relationship for a differential input pair is

$$I_{B1} = \frac{1}{2} g_{m1} \cdot \left(V_{GS1} - V_T\right)$$

$$= \frac{1}{2} \cdot 2\pi \cdot f_{cl2} \cdot C_M \cdot \left(V_{GS1} - V_T\right)$$

$$= \pi \cdot f_{cl2} \cdot C_M \cdot \left(V_{GS1} - V_T\right). \quad (4.12)$$

The non-dominant pole, which is created by the load capacitance, should be placed beyond the three times of the f_{cl2} [Lib 04]. This criterion is shown as

$$\frac{g_{m3}}{C_M + C_{eq,cl}} = 3 \cdot 2\pi \cdot f_{cl2}$$

$$= 6\pi \cdot f_{cl2}. \quad (4.13)$$

So, the bandwidth of the two-stage Miller-compensated OTA to the branch current relationship is

$$I_{D3} = \frac{1}{2} g_{m3} \cdot \left(V_{GS3} - V_T\right)$$

$$= \frac{1}{2} \cdot 6\pi \cdot f_{cl2} \cdot \left(C_M + C_{eq,cl}\right) \cdot \left(V_{GS3} - V_T\right)$$

$$= \pi \cdot f_{cl2} \cdot \left(3C_M + 3C_{eq,cl}\right) \cdot \left(V_{GS3} - V_T\right). \quad (4.14)$$

In general design of the operational amplifier, the phase margin usually is about 60^0. Assuming that a 60^0 phase margin is required, the following relationships apply[Phi 02]：

$$C_M \geq 0.22C_{eq,cl}\,. \tag{4.15}$$

Let

$$V_{GS3} - V_T = V_{GS1} - V_T\,. \tag{4.16}$$

Therefore, the bandwidth of the two-stage Miller-compensated OTA to current relationship for a differential input pair is also written as

$$\begin{aligned} I_{B1} &= \pi \cdot f_{cl2} \cdot C_M \cdot \left(V_{GS1} - V_T\right) \\ &= 0.22\pi \cdot f_{cl2} \cdot C_{eq,cl} \cdot \left(V_{GS1} - V_T\right). \end{aligned} \tag{4.17}$$

And, the bandwidth of the two-stage Miller-compensated OTA to the branch current relationship is also written as

$$I_{D3} = \pi \cdot f_{cl2} \cdot \left(3C_M + 3C_{eq,cl}\right) \cdot \left(V_{GS3} - V_T\right)$$

$$= \pi \cdot f_{cl2} \cdot \left(3 \cdot 0.22C_{eq,cl} + 3C_{eq,cl}\right) \cdot \left(V_{GS1} - V_T\right)$$

$$= 3.66\pi \cdot f_{cl2} \cdot C_{eq,cl} \cdot \left(V_{GS1} - V_T\right). \tag{4.18}$$

Consequently, the total currents of the two-stage Miller-compensated OTA can be written as

$$I_{Miller} = 2I_{B1} + 2I_{D3}$$

$$= 2 \cdot \left[\pi \cdot f_{cl2} \cdot C_M \cdot \left(V_{GS1} - V_T \right) \right] + 2 \cdot \left[\pi \cdot f_{cl2} \cdot \left(3C_M + 3C_{eq,cl} \right) \cdot \left(V_{GS3} - V_T \right) \right]$$

$$= 2 \cdot \left[0.22\pi \cdot f_{cl2} \cdot C_{eq,cl} \cdot \left(V_{GS1} - V_T \right) \right] + 2 \cdot \left[3.66\pi \cdot f_{cl2} \cdot C_{eq,cl} \cdot \left(V_{GS1} - V_T \right) \right]$$

$$= 7.76\pi \cdot f_{cl2} \cdot C_{eq,cl} \cdot \left(V_{GS1} - V_T \right). \tag{4.19}$$

This means k_{OTA} is only 7.76 for the two-stage Miller-compensated OTA.

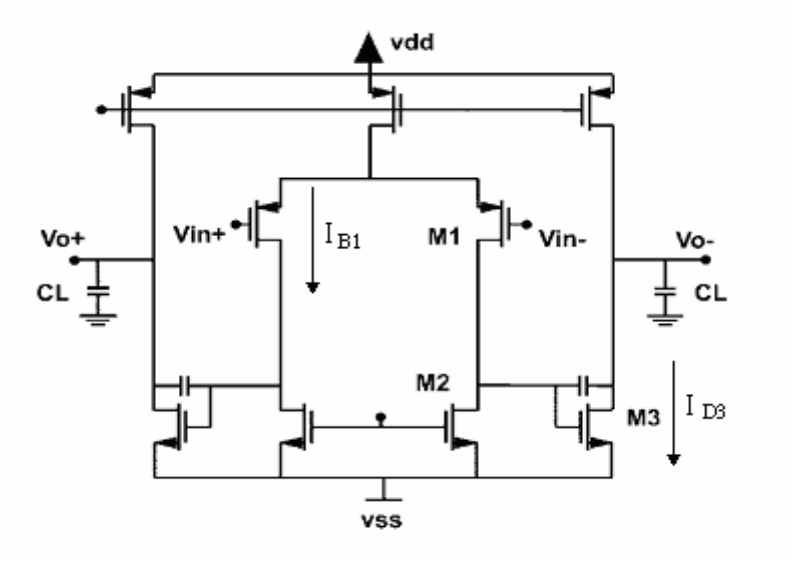


Figure 4.3 The two-stage Miller-compensated OTA

$k_{\Delta\Sigma}$ represents the ratio between the total current consumption of all the OTAs and the first OTA. At first sight, one would expect that it increases significantly as the order of the converter increases since an extra OTA is required.

$k_{Ceq,cl}$ represents the ratio between the effective closed-loop load capacitance and the sampling capacitance.

4.2 Quantizer power

A multi-bit quantizer is used to quantize the analog signal to multi-level digital output signal in the implementation of a multi-bit sigma-delta modulator. The multi-bit quantizer is implemented by Nyquist-rate analog to digital converter. In the multi-bit sigma-delta modulator, the power estimation for the quantizer can be as the power estimation for the Nyquist-rate ADC. There are many parameters to be considered for the quantizer (Nyquist-rate ADC) like the speed and the accuracy.

The power is proportional to the supply voltage, the frequency and a charge. And, the power can be wrote as

$$P = V_{DD} \cdot I = V_{DD} \cdot f \cdot \text{Charge} . \tag{4.20}$$

From the equation (20), we can find a question. The question is what frequency should be considered for the multi-bit quantizer and then which charge is being transferred. The quantizer has two parts, comparators and processing circuitry. The comparator is clocked at frequency of the sample and the processing circuitry varies at the frequency of the input signal. So the equation (1) can be wrote as [Eri 02]

$$P = P_{comparator, fs} + P_{processing\_circuit, fb} . \tag{4.21}$$

and

$$P = V_{DD} \cdot f \cdot \left(Voltage\ swing\right) \cdot C . \tag{4.22}$$

The voltage swing for the comparators is always the full supply voltage. So the equation (22) can be wrote as

$$P = V_{DD}^{\ 2} \cdot C \cdot f \ . \tag{4.23}$$

About the capacitances is not easy to estimate in the quantizer. Therefore, the equality is replaced by a proportionality and the capacitance is taken proportional to the technology's minimal channel length. So the following equation for the total power estimator is [Eri 02]

$$P \propto V_{DD}^{\ 2} \cdot L_{\min} \cdot \left(fs + fb \right). \tag{4.24}$$

The accuracy is expressed as the effective number of bits (ENOB), which is defined as shown in the well-known [Eri 02]

$$ENOB = \frac{20 \cdot \log\left(SNDR \right) - 1.76}{6.02}. \tag{4.25}$$

where SNDR represents the signal-to-noise-and-distortion ratio. The accuracy expressed in (6) is related to the size of the devices and in this way to the power (5): this correlation has been investigated for 75 data points as show in Figure 4 [Eri 02]. From the Figure 4, we can get the following regression relation[Eri 02]

$$\log\left(\frac{V_{DD}^{\ 2} \cdot L_{\min} \cdot \left(fs + fb \right)}{P_Q} \right) = -0.1525 \cdot ENOB + 4.8381 \, . \tag{4.26}$$

So the final power estimator for the complete CMOS Nyquist-rate ADC can be written as [Eri 02]

$$P_Q = \frac{V_{DD}^{\ 2} \cdot L_{\min} \cdot \left(fs + fb \right)}{10^{(-0.1525 \cdot ENOB + 4.8381)}}. \tag{4.27}$$

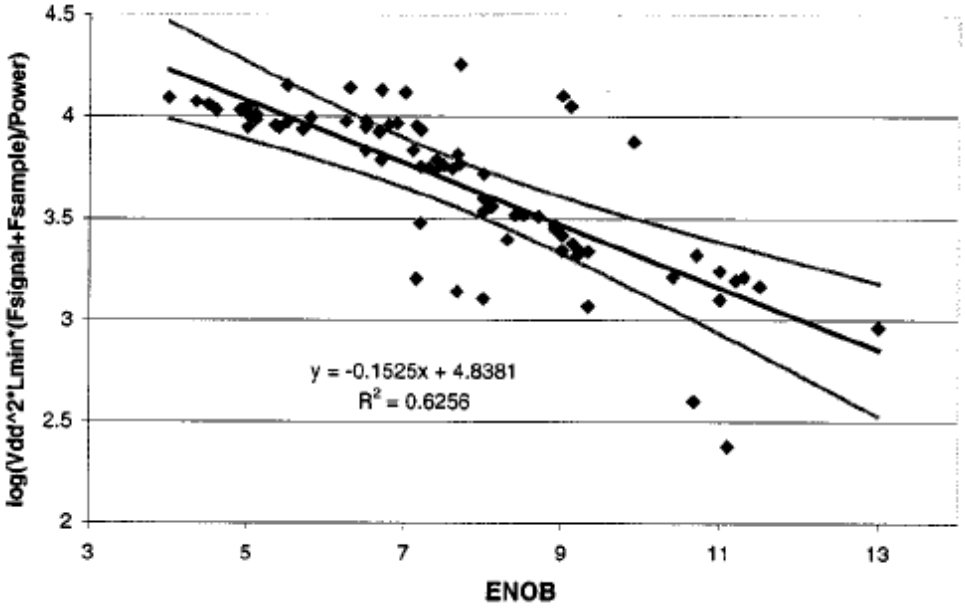


Figure 4.4.An overview of the obtained data points. The ENOB are given as a function of the input signal frequency.

4.3 DAC Power

We estimate the power consumption of multi-bit DAC in the single-loop multi-bit sigma-delta converter. The multi-bit DAC is shown in Figure 5 (a) [Gag 03]. It is composed of switches and unit capacitors. At first, we consider charge and discharge for an unit capacitor in the multi-bit DAC. The operations of a unit capacitor are illustrated in Figure 5 (b) and Figure 5 (c) respectively. We assumed that the periods of charge and discharge both are T/2, the power consumption of a unit capacitor in the multi-bit DAC is

$$P_u = \frac{1}{T}\int_0^{T/2} V_{Cu} \cdot I_u dt + \frac{1}{T}\int_{T/2}^{T} (0 - V_{Cu}) \cdot I_u dt \,. \tag{4.28}$$

To employ charge conservation law, we can obtain (29):

$$I_u = Cu\, dV_{Cu}/dt . \tag{4.29}$$

When (29) substitutes for I_u in (29), (28) can be derived as

$$P_u = \frac{1}{T}\int_0^{T/2} V_{Cu}\cdot Cu\, dV_{Cu}/dt\, dt + \frac{1}{T}\int_{T/2}^{T}(0-V_{Cu})\cdot Cu\, dV_{Cu}/dt\, dt$$

$$= \frac{1}{T}\int_0^{Vref} V_{Cu}\cdot Cu\, dV_{Cu} + \frac{1}{T}\int_{Vref}^{0}(0-V_{Cu})\cdot Cu\, dV_{Cu}$$

$$= \frac{1}{T}\left(1/2\cdot V_{Cu}^{\,2}\cdot Cu\right)\Big|_0^{Vref} + \frac{1}{T}\left(0-1/2\cdot V_{Cu}^{\,2}\cdot Cu\right)\Big|_{Vref}^{0}$$

$$= \frac{1}{T}\left(1/2\cdot \mathrm{Vref}^2\cdot Cu\right) + \frac{1}{T}\left[0-\left(-1/2\cdot \mathrm{Vref}^2\cdot Cu\right)\right]$$

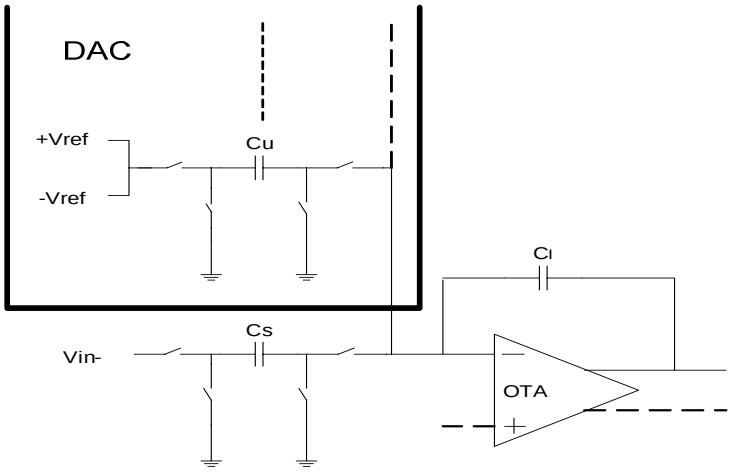
$$= \frac{1}{\mathrm{T}}\mathrm{Vref}^2\cdot Cu = \mathrm{Vref}^2\cdot Cu\cdot \mathrm{f_s} . \tag{4.30}$$

We can get the power estimation of a unit capacitor from (30), so the total power estimation for a multi-bit DAC is

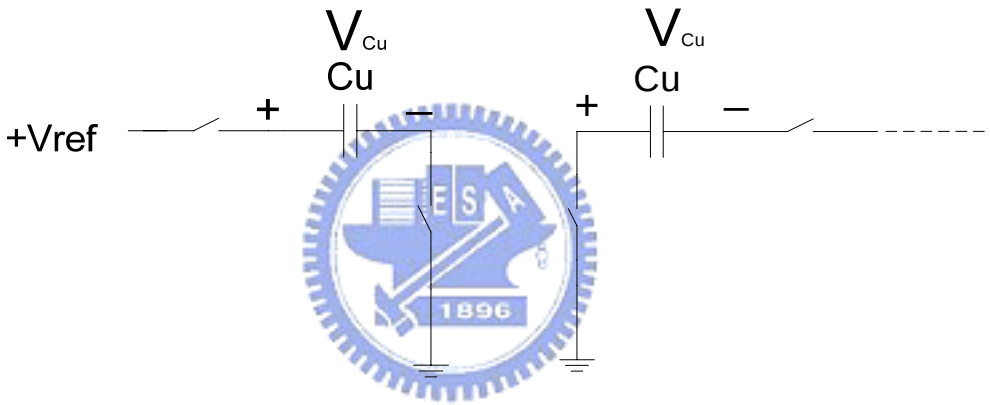
$$P_{DAC} = 2\cdot 2^B\cdot Cu\cdot Vref^2\cdot f_s$$

$$= 2\cdot 2^B\cdot \frac{1}{2^B} Cs\cdot Vref^2\cdot f_s$$

$$= 2\cdot Cs\cdot Vref^2\cdot f_s . \tag{4.31}$$



(a)



(b) (c)

Figure 4.5 (a) Implementation of the integrator and the feedback DAC. (b) To charge the unit capacitance. (c) To discharge the unit capacitance.

4.4 Clock driver power and switch power

Static CMOS logic gates are very power-efficient because they dissipate nearly zero power while idle, so the primary dissipation component is the dynamic dissipation component.

And, the primary dynamic dissipation component is charging and discharging the load capacitance. For much of the history of CMOS design, power was a secondary consideration behind speed and area for many chips. As transistor counts and clock frequencies have increased, power consumption has skyrocketed and now is a primary design constraint.

Begin to review some definitions first. The instantaneous power $P(t)$ drawn from the power supply is proportional to the supply current $i_{DD}(t)$ and the supply voltage V_{DD}

$$P(t) = i_{DD}(t) \cdot V_{DD} . \tag{4.32}$$

The energy consumed over some time interval T is the integral of the instantaneous power. And, the energy can be wrote as

$$E = \int_0^T i_{DD}(t) \cdot V_{DD} dt . \tag{4.33}$$

The average power over this interval is

$$P_{avg} = \frac{E}{T} = \frac{1}{T} \int_0^T i_{DD}(t) \cdot V_{DD} dt . \tag{4.34}$$

Considering an ideal inverter and a CMOS inverter with the load capacitor C_L are shown in Figure 6 (a) and Figure 6 (b) respectively. Giving a periodic square-wave from the input point is shown in Figure 6 (c). The associated NMOS transistor is ON and the PMOS transistor is OFF when the input signal approach high level voltage at $t = 0^-$. At the same time, the output voltage is 0 volts (GND).

Further, the associated NMOS transistor is OFF and the PMOS transistor is ON when the input signal voltage is changed from high level voltage to low level voltage at $t = 0$. At the same time, the charging current pours into the load capacitor through the channel PMOS transistor, and the output voltage is going to approach high level voltage. At first, the energy of computation is E_S provided by the power supply is

$$E_S = \int V_{DD} \cdot i(t)dt = V_{DD} \cdot \int i(t)dt$$

$$= V_{DD} \cdot Q = V_{DD} \cdot (C_L \cdot V_{DD})$$

$$= C_L \cdot V^2{}_{DD} \,. \tag{4.35}$$

However, the energy E_C which stored up on the load capacitor is

$$E_C = \int V_{DD}(t) \cdot i(t)dt = \int V_{DD}(t) \cdot (C_L \cdot \frac{dv}{dt})dt$$

$$= C_L \cdot \int V_{DD}(t)dv = \frac{1}{2} C_L \cdot V^2{}_{DD} \,. \tag{4.36}$$

Therefore, the energy E_P which dissipated on the PMOS transistor should be equal to the energy E_S provided by the power supply to subtract the energy E_C stored up on the load capacitance, also is

$$E_P = E_S - E_C$$

$$= C_L \cdot V_{DD}^2 - \frac{1}{2} C_L \cdot V_{DD}^2 = \frac{1}{2} C_L \cdot V_{DD}^2 \,. \tag{4.37}$$

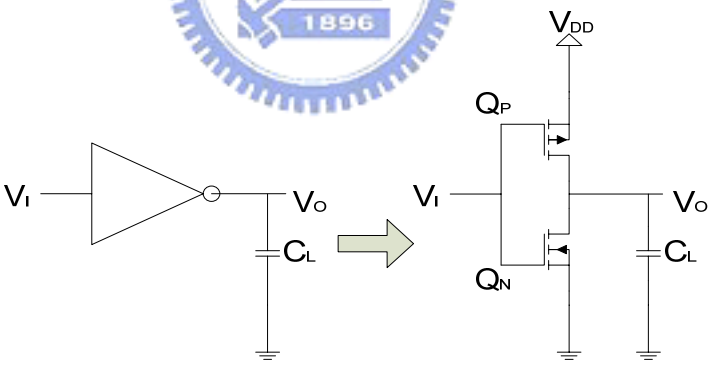
When $t = T_1$, the input signal V_I returns to the higher state once again so that the NMOS

transistor is ON and the PMOS transistor is OFF. After transformation, the load capacitor will be discharged through the channel of NMOS transistor, and leads to the power dissipation on the NMOS transistor. Consequently, the energy E_N which dissipated on the NMOS should be equal to the energy E_C stored up on the load capacitor, also is

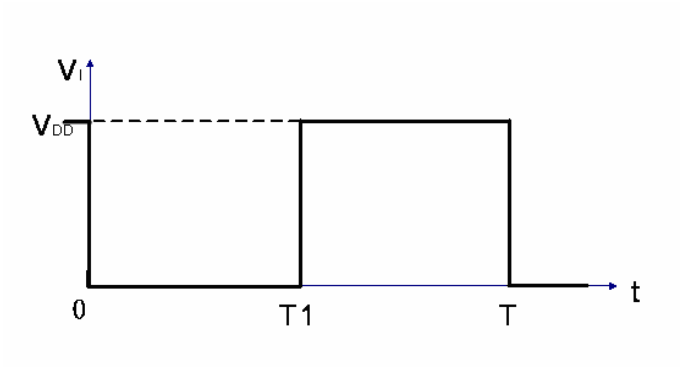
$$E_N = E_C = \frac{1}{2} C_L \cdot V_{DD}^2 . \tag{4.38}$$

For this reason, the total energy consumed by the logic gate in one cycle is $\left(E_P + E_N\right) = C_L \bullet V_{DD}^2$. If the input signal frequency of the CMOS inverter is f ,so the dynamic power dissipation $P_{D(dyn)}$ is

$$P_{D(dyn)} = f \cdot C_L \cdot V_{DD}^2 . \tag{4.39}$$



(a) (b)



(c)

Figure 4.6 (a) an ideal inverter for logic level with a load capacitance (b) an ideal CMOS inverter for transistor level with a load capacitance (c) a periodic square-wave for the input.

The switched-capacitor circuits and quantizers require various clock signals. These signals are generated on chip from one external clock signal. The switched-capacitor circuit requires two non-overlapping clocks for sampling and the integration phase. The clock generator with non-overlapping clocks is shown in Figure 2[Gee 02]. From Figure 7, it shows that the clock generator is composed of the logic gates. The primary logic gates which compose of the clock generator are inverters and the NAND gates. Assuming the clock generator has N_C logic gates, and the capacitance of one capacitor is C_{logic}. Under these assumptions the power dissipation of the clock generator can be wrote as

$$P_{clock} = f \cdot C_{clock} \cdot V_{DD}^2$$

$$= N_C \cdot f \cdot C_{logic} \cdot V_{DD}^2 . \qquad (4.40)$$

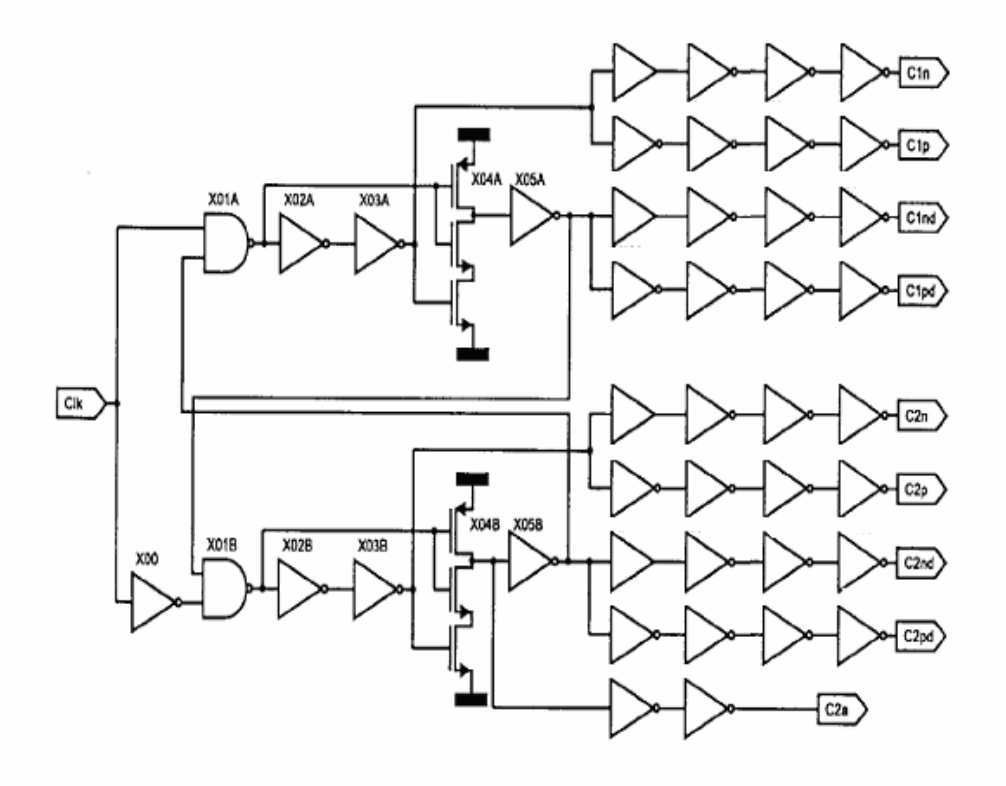


Figure 4.7 the clock generator with non-overlapping clocks.

Another important component for the power dissipation is offered by CMOS transmitters in the switched-capacitor circuits. The output of the clock generator is connected to the gate of the CMOS switches in the switched-capacitor circuits. The CMOS switch is shown in Figure 4.8. Assuming that the number of the CMOS transmission gate in Sigma-Delta modulator is N_S and the gate capacitances of all CMOS transmission gates are C_{gate}. Under these assumptions the power dissipation of the CMOS switch can be wrote as

$$P_{switch} = f \cdot C_{switch} \cdot V_{DD}^2$$

$$= N_S \cdot f \cdot C_{gate} \cdot V_{DD}^2 . \qquad (4.41)$$

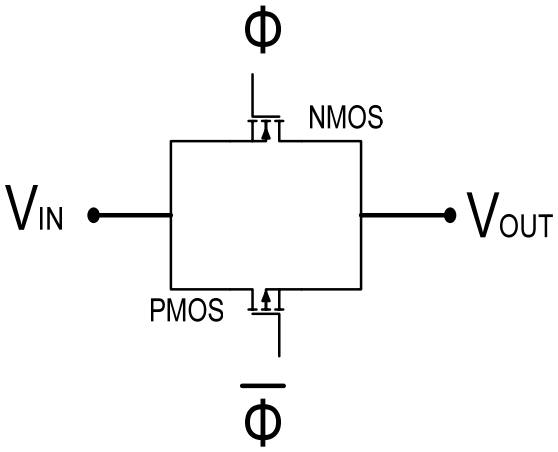


Figure 4.8 the CMOS switch

C_{gate} is the capacitance of the gate capacitor in one CMOS switch. The gate of an MOS transistor is a good capacitor. Indeed, its capacitance is necessary to attract charge to invert the channel of the transistor. The gate capacitor can be viewed as a parallel plate capacitor with the gate on top and channel on bottom with the thin oxide dielectric between. From the Table 1[Nei 05], it is clearly to observe that to get the approximation of intrinsic MOS gate capacitance with the CMOS switch. Because the voltage of the gate varies in V_{DD} and GND, the status of the CMOS switch is either cut-off or linear. Consequently, the value of the gate capacitance C_{gate} can be wrote as

$$C_{gate} = C_0$$

$$= C_{OX} \cdot W \cdot L . \qquad (4.42)$$

where C_{OX} is the capacitance per unit area of the gate oxide, L is length of the gate, and W is width of the gate. C_{OX} can be wrote as

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}} \tag{4.43}$$

where the permittivity $\varepsilon_{OX} = 3.9\varepsilon_0$ for SiO_2 and ε_0 is the permittivity of free space, 8.85×10^{-14} F/cm.

Besides, R_{CMOS} is the parallel resistance with R_N and R_P. Consequently, R_{CMOS} can be wrote as

$$R_{CMOS} = R_N // R_P$$

$$= \frac{1}{\mu_n \cdot C_{OX} \cdot \left(\frac{W}{L}\right)_n \cdot \left(V_{DD} - V_{tn} - \left|V_{tp}\right|\right)}. \tag{4.44}$$

Let R_{CMOS} be remained constant with the input signal level (44) employs the supposition that can be wrote as

$$\mu_n \cdot C_{OX} \cdot \left(\frac{W}{L}\right)_n = \mu_p \cdot C_{OX} \cdot \left(\frac{W}{L}\right)_p. \tag{4.45}$$

After combining the equation (42) with the equation (44), one may derive the results for the gate capacitance C_{gate} so the gate capacitance C_{gate} can be wrote as

$$C_{gate} = \frac{L_{\min}^2}{\mu_n \cdot R_{CMOS} \cdot \left(V_{DD} - V_{tn} - \left|V_{tp}\right|\right)}. \tag{4.46}$$

where $L_{\min}$ represents the minimum manufacturable length because this results in greatest speed and lowest power consumption.

$C_{\log ic}$ is the value of the gate capacitance in one logic gate. Because the voltage of the

gate varies in V_{DD} and GND with the most logic gates, the status of the MOS of the logic gate is either cut-off or linear. Consequently, the value of the gate capacitance $C_{\log ic}$ can be wrote as

$$C_{\log ic} = 2C_0$$

$$= 2C_{OX} \cdot W \cdot L . \qquad (4.47)$$

Table 4.1 Approximation of intrinsic MOS gate capacitance

Approximation of intrinsic MOS gate capacitance $(C_0 = C_{ox} \cdot W \cdot L)$			
Parameter	Cut-off	Linear	Saturation
C_{gb}	C_0	0	0
C_{gs}	0	$C_0/2$	$2C_0/3$
C_{gd}	0	$C_0/2$	0
$C_g = C_{gb} + C_{gs} + C_{gd}$	C_0	C_0	$2C_0/3$

It may be stated from the above result that the digital power consumption P_{dig} can be wrote as

$$P_{dig} = P_{clock} + P_{switch}$$

$$= N_C \cdot f \cdot C_{\log ic} \cdot V_{DD}^2 + N_S \cdot f \cdot C_{gate} \cdot V_{DD}^2$$

$$= N_C \cdot f \cdot \left(2C_{OX} \cdot W_{avg} \cdot L_{avg}\right) \cdot V_{DD}^2$$

$$+ N_S \cdot f \cdot \left[\frac{L_{\min}^2}{\mu_n \cdot R_{CMOS} \cdot \left(V_{DD} - V_{tn} - \left|V_{tp}\right|\right)}\right] \cdot V_{DD}^2 . \qquad (4.48)$$

where L_{avg} is average length and W_{avg} is average width of the logic gates in the clock generator.

The digital power consumption P_{dig} doesn't include the logic gates in the quantizer, and the dynamic element matching algorithm.

4.5 Verification for the power consumption model

By adding up all the contribution, the power dissipation of the sigma-delta modulator can be estimated as

$$Power \cong P_{an} + P_Q + P_{DAC} + P_{clock} + P_{switch}$$

$$= \pi \cdot k_{\Delta\Sigma} \cdot k_{OTA} \cdot k_{Ceq,cl} \cdot C_S \cdot f_{cl2} \cdot V_{eff} \cdot V_{DD}$$

$$+ \frac{V_{DD}{}^2 \cdot L_{\min} \cdot \left(fs + fb\right)}{10^{(-0.1525 \cdot ENOB + 4.8381)}}$$

$$+ 2 \cdot Cs \cdot Vref^2 \cdot f_s + N_C \cdot f_s \cdot \left(2C_{OX} \cdot W_{avg} \cdot L_{avg}\right) \cdot V_{DD}^2$$

$$+N_S \cdot f_s \cdot \left[\frac{L_{\min}^2}{\mu_n \cdot R_{CMOS} \cdot \left(V_{DD} - V_{tn} - \left| V_{tp} \right| \right)} \right] \cdot V_{DD}^2 \qquad (4.49)$$

We used the second-order single-bit sigma-delta modulator of the Chapter 5 to verify the power consumption model. The total power consumption of the circuit is 16.96mW. The power consumption of the OTA is 7.95mW. So we know that the $P_Q + P_{clock} + P_{switch}$ of the circuit is 1.06mW and the P_{an} of the circuit is 15.9mW.

The power consumption P_{an} of our power consumption model is 12.2mW and the power consumption $P_Q + P_{clock} + P_{switch}$ of our power consumption model is 1.11mW. So we know that the power consumption of our power consumption model is 13.31mW.

The accuracy of our power consumption model is about 78.5%. So we have 21.5% inaccuracy for the power consumption model because the power consumption of the gain-boosting technique and bias circuit for OTA is not consider in our power consumption model.

Now we know that the gain-boosting technique for OTA can increase 25% power consumption of the OTA by Hspice simulation. So we can get the power consumption of the OTA is $6.1 \times 1.25 = 7.625mW$. The total power consumption of our power consumption model is 16.36mW. The accuracy of our power consumption model is about 96.5%.

Chapter 5

Circuit Implementation for Second-order One-bit Sigma-Delta Modulators

This chapter describes the detail circuit design for Second-order sigma-delta modulators. These circuit components include switched-capacitor integrators, operational transconductance amplifiers, bias network, comparators, quantizers, and digital networks.

Fully differential architectures are usually used in the analog circuits for the following reasons. First, a fully differential topology provides for high rejection of common-mode disturbance such as supply and substrate noise. It has the additional advantage that that if each single-ended signal is distorted symmetrically around the common-mode voltage, the differential signal will have only odd-order distortion terms. Second, a fully differential signal has twice amplitude as single-ended signal. Thus there is a net increase in dynamic range of 3dB for fully differential circuits.

5.1 Switched-Capacitor Integrator Design

Sigma-delta Modulators can be implemented by using either the discrete-time architectures, e.g. switched-capacitor (SC) and switched-current (SI) circuits, or continuous-time architectures, e.g. active-RC and transconductance-C (Gm-C) circuits. In general, most integrated circuits (IC) of sigma-delta A/D converters are implemented using SC circuits, because of easily simulation and compatible with VLSI CMOS process. Additionally, SC circuits provide better immunity to clock jitter than continuous-time circuits

and more preferable accuracy than SI circuits. Therefore, the SC circuit is a better choice for high-resolution applications. In our design, the integrator is implemented in a fully differential configuration. This improves the signal to thermal noise ratio $SNR_{KT/C}$ by 3dB compared with the single-ended structure. If considering the same $SNR_{KT/C}$, the total values of sampling capacitors can be reduced by a factor of two and the capacitive load of the op-amp also can be decreased by reducing the sampling capacitance. This means the power dissipation of the amplifier is also reduced.

The timing phases used in the switched-capacitor integrator are two-phase non-overlapping clocks, ϕ_1 and ϕ_2, and delayed clock phases, ϕ_{1d} and ϕ_{2d}. Fig. 5.1 shows the first integrator and timing diagram in the cascaded modulators. The input signal is sampled during phase 1 (ϕ_1 and ϕ_{1d}). During phase 2, the charge is transferred from sampling capacitor (C_S) to the integrating capacitor (C_I). At the same time, depending on the output value, the appropriate DAC reference voltage is applied to the sampling capacitor by the switches labeled ϕ_{1yd} and ϕ_{2yd}. The integrator employs the bottom-plate sampling technique to minimize the parasitic capacitance to the substrate [Fel 98]. The capacitors should be connected such that the bottom plate is driven either directly or through a switch by a voltage source or the output of the op-amp. This arrangement causes the parasitic capacitances to have the least effect on the operation of circuit, and the substrate noise coupling is also reduced by this arrangement.

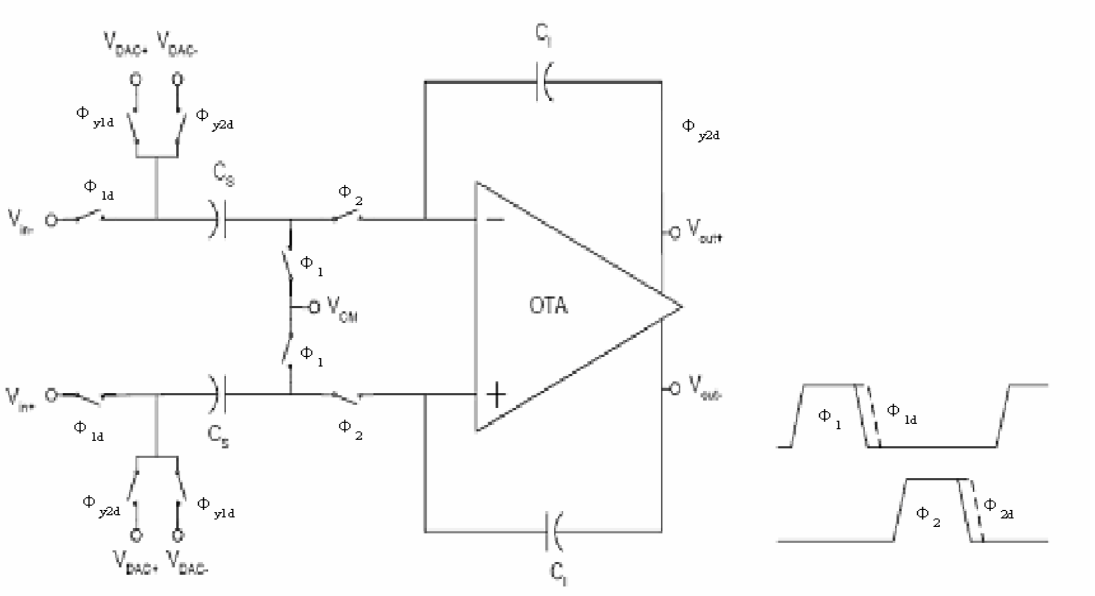


Fig. 5.1： Fully differential switched-capacitor integrator and timing diagram.

In Fig. 5.1, the summing junction switches (labeled ϕ_1 and ϕ_2) are implemented by nMOS and the other switches are implemented by CMOS transmission gates. The summing junction switches are clocked by ϕ_1 and ϕ_2 and the other switches that operate over the signal range are clocked by ϕ_{1d}, ϕ_{1yd}, and ϕ_{2yd}. This will cause the switches coupled to the summing junction to turn off slightly before the signal conducting switches. Once the summing junction switches have turned off, there is no conductive path to the top plate of the switched capacitance. The total charge on this node cannot change when the summing switches are open. With this clocking arrangement, the charge injection from the summing junction switches will be signal independent, since both the source and drain of a summing junction will always be at analog ground when the switches are turned off.

5.2 Operational Transconductance Amplifier

The operational amplifier is widely used in many types of analog circuits. Especially in switched-capacitor circuits, the operational amplifier is the most critical block. The operational amplifier of the integrator usually determines the resolution and speed of the sigma-delta modulators. In general, the amplifier open loop DC-gain limits the settling accuracy of the amplifier output, while the bandwidth and slew rate of the amplifier determine the maximal clock frequency. To maximize the signal-to-noise ratio, the operational amplifier should also utilize a large signal swing at the output.

5.2.1 Folded Cascode OTA

The folded cascade op-amp, shown in Fig. 5.2, is probably the most commonly used op-amp architecture in switched-capacitor circuits. This op-amp provides a large output swing and input common-mode range than the cascoding OTA with the same DC gain and without major loss of speed. The maximum output voltage swing of the folded cascode op-amp shown in Fig. 5.2 can be calculated. With the proper choice of biasing voltages, the lower bound of the swing is given by $V_{ds,sat8}+V_{ds,sat10}$ and the upper bound by $V_{DD}-\left(\left|V_{ds,sat4}\right|+\left|V_{ds,sat6}\right|\right)$. If all of the overdrive voltage is approximate $V_{ds,sat}$, the peak-to-peak swing on each side is equal to $V_{DD}-4V_{ds,sat}$.

From Figure 5.2, we can easily derive some small-signal parameters of the op-amp. The output impedance is given by

$$r_o=\left[g_{m7}\cdot r_{o7}\cdot\left(r_{o2}\,//\,r_{o5}\right)\right]//\left(g_{m9}\cdot r_{o9}\cdot r_{o11}\right) \tag{5.1}$$

The open-loop dc voltage gain is given by

$$A = -g_{m1} \cdot r_o \tag{5.2}$$

If the second pole is at the behind of the unity-gain frequency, then the unity-gain bandwidth of the amplifier is derived by

$$\left|A(s)\right| = \left|g_{m1}\left(r_o \,//\, \frac{1}{sC_L}\right)\right| \approx \left|\frac{g_{m1}}{sC_L}\right| = 1 \tag{5.3}$$

$$\Rightarrow \qquad w_t = \frac{g_{m1}}{C_L} \tag{5.4}$$

The dominant pole of the cascode op-amp is determined by the capacitance at the output. So the cascode op-amp could be compensated by its output load capacitance. The load capacitance will create a dominant pole at a frequency

$$w_t = \frac{g_{m1}}{C_L} = g_{m1} \cdot r_o \cdot w_{p1} \tag{5.5}$$

$$\Rightarrow \qquad w_{p1} = \frac{1}{r_o \cdot C_L} \tag{5.6}$$

M_6, M_7, M_8 and M_9 are common-gate devices. A common-gate connected device has input impedance that is a factor $(g_m \cdot r_o)$ lower than its output impedance. This can still be fairly high input impedance if the output impedance of the common-gate device is high enough. At frequencies above the dominant-pole frequency, the output impedance is reduced by the load capacitor C_L. At dc, the output impedance is expressed by Equation (5.8). The dc gain from the gate of the M_1 to the source of the M_7 is given by

$$A_1 = -g_{m1}\left[\left(r_{o2} \,//\, r_{o5}\right)//\left(\frac{r_{o7} \,//\, g_{m9} r_{o9} r_{o11}}{g_{m7} r_{o7}}\right)\right] \tag{5.7}$$

The gain from the source of the M_8 to the output is

$$A_2 \approx g_{m7} \cdot r_{o7} \tag{5.8}$$

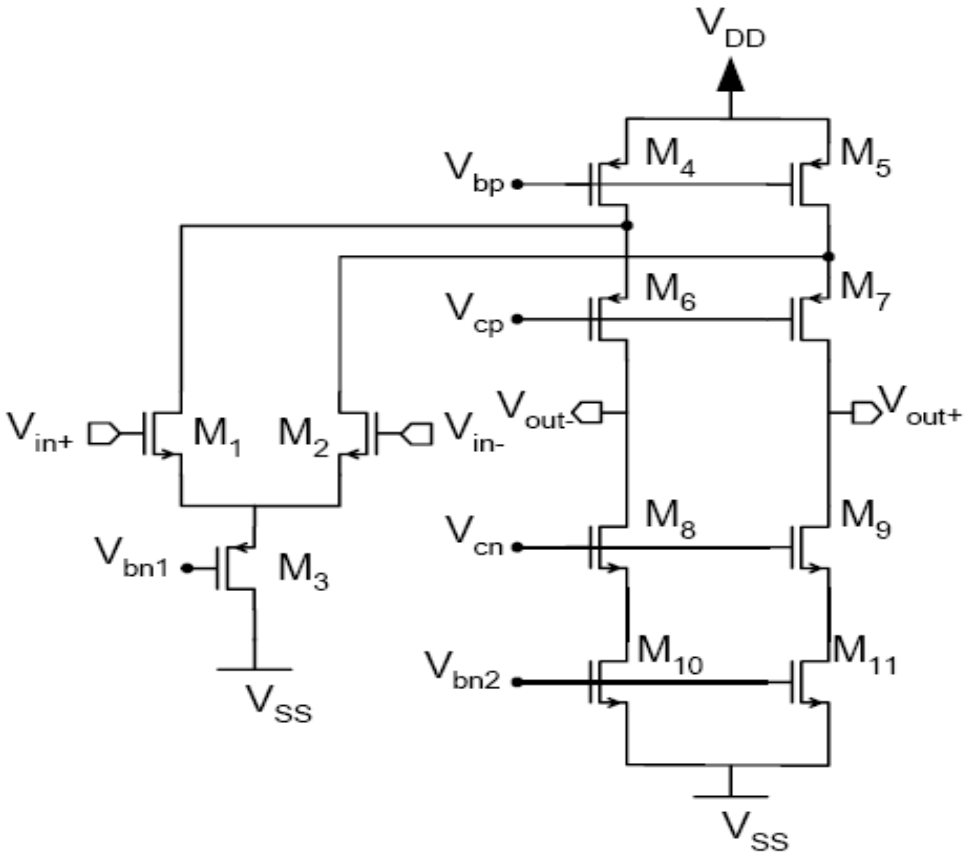


Fig. 5.2: Folded cascode op-amp.

The choice between an nMOS and pMOS input pair has to be made on the basis of the required phase margin. When using the nMOS input pair, the unit-gain bandwidth $\left(GBW = g_{m1}/C_L\right)$ can be increased due to the nMOS input transistors, but the nondominant pole $\left(g_{m6}/C_P\right)$ will be decreased due to the low pMOS transconductance of M_6 and large

parasitic capacitance, C_P, from transistors M_1, M_4, and M_6. On the other hand, utilizing a pMOS input pair gives lower GBW, but the non-dominant pole is higher due to the nMOS cascode devices. The frequency response of this amplifier is deteriorated from that of the cascode transistor because of a smaller transconductance of the p-channel device and a larger parasitic capacitance. However, compared to the two-stage Miller compensated amplifier, a larger bandwidth can be achieved.

5.2.2 Gain Enhancement Technique

In many applications, the op-amp DC gain requirement is higher than what is achievable in a folded cascode op-amp. Therefore, several techniques are developed to enhance the output impedance so as to obtain a high voltage gain. The idea behind gain enhancement is to further increase the output impedance without adding more cascode devices. The open-loop DC-gain of amplifier with cascode transistors can be boosted by regulating the gate voltage of the cascode transistors [Bul 90]. The regulation is realized by adding an extra gain stage as shown in Fig. 5.3. This stage reduces the feedback from the output to the drain of the input transistors. Therefore, the output impedance of the circuit is increased by the gain of the additional amplifier stage with a gain of A_f :

$$r_{out} = g_{m2} \cdot r_{ds1} \cdot r_{ds2} \cdot (A_f + 1) + r_{ds1} + r_{ds2}$$

$$\approx g_{m2} \cdot r_{ds1} \cdot r_{ds2} \cdot A_f \qquad (5.9)$$

where g_{m2} is the transconductance of M_2, and r_{ds1} and r_{ds2} are the output resistances of M_1 and M_2, respectively. In this way, the DC-gain of the amplifier can be increased by

several orders of magnitude. The dependency of the stability of the whole amplifier on the feedback amplifier bandwidth deserves great attention. If the parasitic pole introduced by the feedback amplifier can be kept at high frequencies, a single-pole roll-off and settling behavior can be obtained. Furthermore, the increasing in power and chip area can be kept very small with an appropriate feedback amplifier architecture [Bul 90].

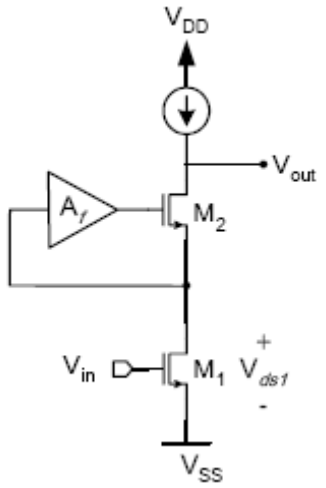


Fig. 5.3: Regulated cascaded gain stage

Three different implementations of the regulation amplifier are shown in Fig. 5.3. The first one shown in Fig .5.4 (a) [Hos 79] [Säc 90] is very simple, but it sets the voltage on the cascode node unnecessarily high. The circuit shown in Fig. 5.4 (b) [Gat 90] utilizes a level shifter, and the third one shown in Fig. 5.4 (c) [Zar 94] is a common gate amplifier, which allows the biasing of the cascode node to a lower voltage. Using a more complicated regulation amplifier, e.g. a folded cascode OTA, is also possible. In fully differential circuits the regulation amplifier can also be fully differential.

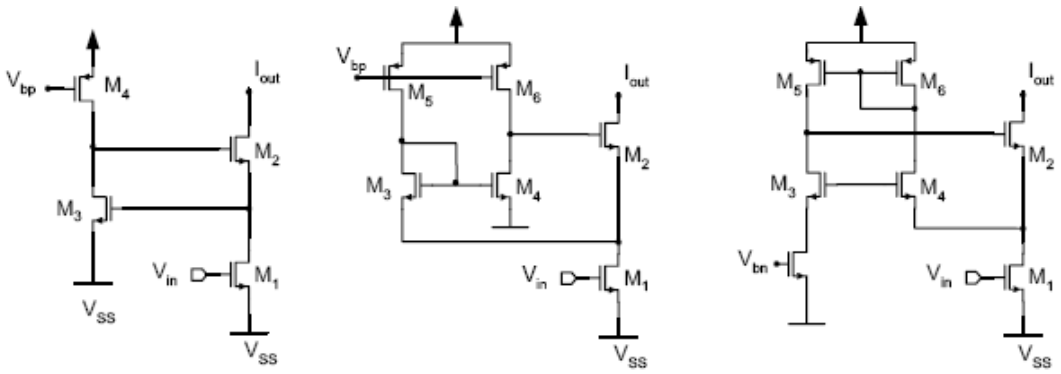


Fig. 5.4：Gain boosting in cascode stage (a) simply amplifier, (b) level shifter amplifier, (c) common gate amplifier

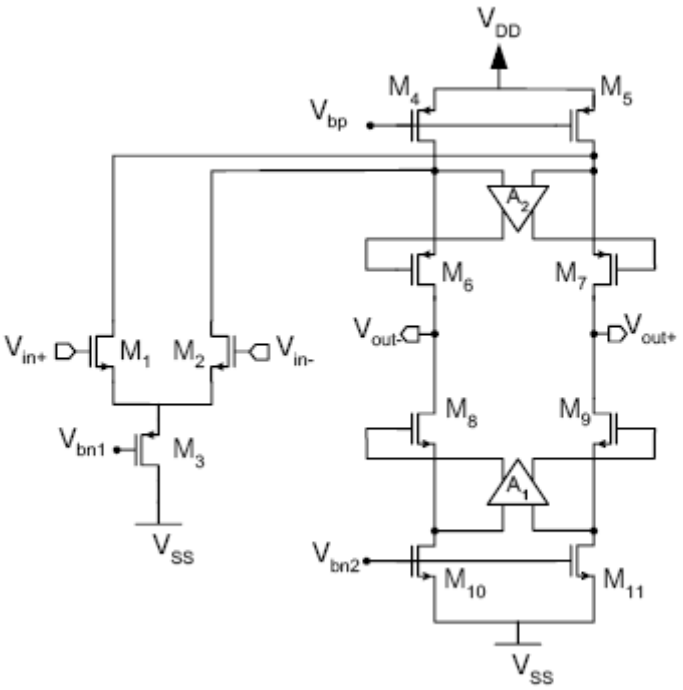


Fig. 5.5：Gain boosting folded cascode op-amp

Regulated cascodes can be utilized in the load current sources of a cascode op-amp. Shown in Fig. 5.5, such a topology boosts the output impedance of the pMOS current sources as well, thereby achieving a high voltage gain more than 80dB. To allow maximum swings at the output, amplifier A_2 must employ an nMOS input differential pair and amplifier A_1 must

employ pMOS ones.

5.2.3 Bias circuit

The bias circuit of the operational amplifier is implemented by incorporating wide-swing current mirrors into the constant-transconductance bias. This architecture greatly minimizes most of the detrimental second-order imperfection caused by the finite output impedance of the transistors, without greatly restricting signal swings. The wide-swing constant-transconductance bias circuit is shown in Fig. 5.6. The circuit includes wide-swing cascode current mirrors, stable transconductance (i.e., constant g_m) bias circuits, and a start-up circuit [Mar 97]. It should be mentioned that bias circuit is presently becoming the most popular CMOS bias circuit and is therefore very important in many analog designs besides op-amp.

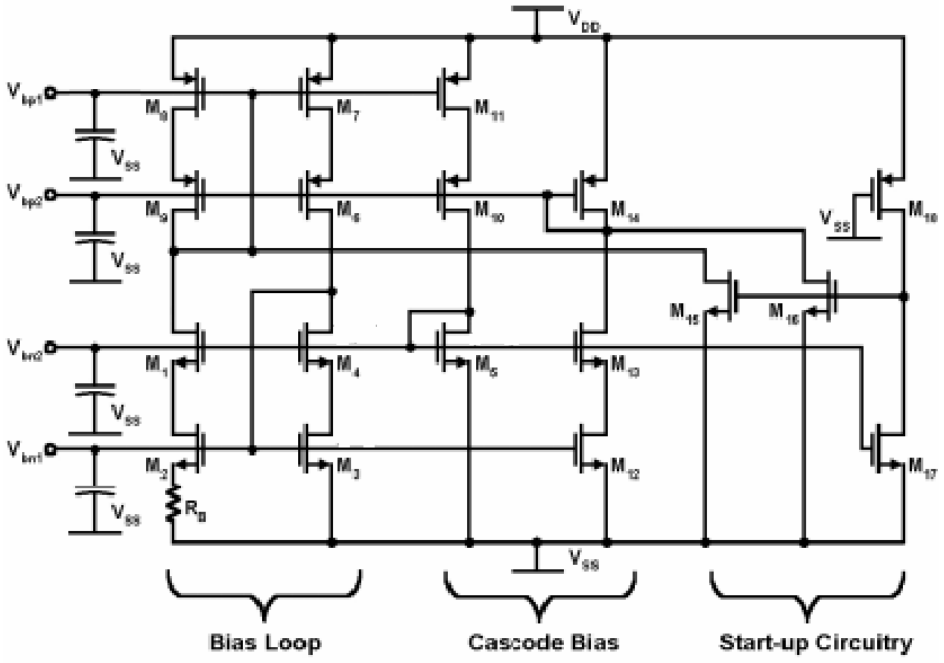


Fig. 5.6：A wide-swing constant-transconductance bias circuit

The stable transconductance bias is provided by the resistor R_B and transistors M_2, M_3 in the bias loop shown in Fig. 5.6 [Ste 90]. We assumed that $(W/L)_8 = (W/L)_7$. This equality results M_1 and M_3 of the circuit having the same current due to the current-mirror pair M_8, M_7. Now, around the loop consisting of M_3, M_2 and R_B, we obtain

$$V_{GS3} = V_{GS2} + I_{D2}R_B \tag{5.10}$$

Recalling that $V_{eff} = V_{GS} - V_t$, we can subtract the threshold voltage, V_t, from both sides, resulting in

$$V_{GS3} - V_{tn} = V_{GS2} - V_{tn} + I_{D2}R_B \tag{5.11}$$

$$\Rightarrow V_{eff3} = V_{eff2} + I_{D2}R_B \tag{5.12}$$

This equation can be rewritten as

$$\sqrt{\frac{2I_{D3}}{\mu_n C_{OX}\left(W/L\right)_3}} = \sqrt{\frac{2I_{D2}}{\mu_n C_{OX}\left(W/L\right)_2}} + I_{D2}R_B \tag{5.13}$$

Since $I_{D3} = I_{D2}$, Equation (5.13) can also be written as

$$\sqrt{\frac{2I_{D3}}{\mu_n C_{OX}\left(W/L\right)_3}} = \sqrt{\frac{2I_{D3}}{\mu_n C_{OX}\left(W/L\right)_2}} + I_{D3}R_B \tag{5.14}$$

Rearranging Equation (5.14), we obtain

$$\frac{2}{\sqrt{2\mu_n C_{OX}\left(W/L\right)_3 I_{D3}}}\left(1 - \sqrt{\frac{\left(W/L\right)_3}{\left(W/L\right)_2}}\right) = R_B \tag{5.15}$$

We also know that

$$g_{m3} = \sqrt{2\mu_n C_{OX} \left(W/L\right)_3 I_{D3}} \tag{5.16}$$

From Equation (5.15) and (5.16), we can obtain and important relationship

$$g_{m3} = \frac{2}{R_B}\left(1 - \sqrt{\frac{\left(W/L\right)_3}{\left(W/L\right)_2}}\right) \tag{5.17}$$

It is obvious that the transconductances of the M_3 could only be determined by the geometric ratio between M_3 and M_2. Thus, it is nothing to do with power-supply voltage, process parameter, temperature, or any other parameters with large variability. But it should put emphasis on the fact that

$$\frac{\left(W/L\right)_3}{\left(W/L\right)_2} < 1 \tag{5.18}$$

should be true for any case. Otherwise, it may cause this circuit unstable.

For special case of $(W/L)_2 = 4(W/L)_3$, we can simplified equation (5.17) as

$$g_{m3} = \frac{1}{R_B} \tag{5.19}$$

From equation (5.19), not only is g_{m3} is stabilized, but all other transconductances are also stabilized since all transistors currents are derived from the same biasing network, and, therefore, ratios of the currents are mainly dependent on geometry. We thus have, for all N-channel transistors,

$$g_{mi} = \sqrt{\frac{\left(W/L\right)_i \cdot I_{Di}}{\left(W/L\right)_3 \cdot I_{D3}}} \cdot g_{m3} \tag{5.20}$$

And for all P-channel transistors,

$$g_{mi} = \sqrt{\frac{\mu_p}{\mu_n} \cdot \frac{\left(W/L\right)_i \cdot I_{Di}}{\left(W/L\right)_3 \cdot I_{D3}}} \cdot g_{m3} \tag{5.21}$$

The N-channel wide-swing cascode current mirror shown in Figure 1 consists of transistors $M_1 \sim M_4$, along with the diode-connected biasing transistors M_5 to provide the bias current. The pair M_3, M_4 acts similarly to a diode-connected transistor at the input side of the mirror. The output current comes from M_1. The diode-connected transistor M_5 derives the gate voltages of cascode transistors M_1 and M_4. The current for this biasing transistor is actually derived from the bias loop via M_{10} and M_{11} [Mar 97].

Similarly, the P-channel wide-swing cascode current mirror is realized by $M_6 \sim M_9$. Transistors M_8 and M_9 operate as a diode-connected transistor at the input side of the P-channel current mirror. The current mirror output current is the drain current of M_6. The cascode transistors M_6 and M_9 have gate voltages derived from diode-connected M_{14}, which has a bias current derived from the cascode bias loop via M_{12} and M_{13}. It should be noted that the P-channel wide-swing current mirror has the same characteristic as the N-channel wide-swing current mirror, so we ignore the explanation of the P-channel device in bias loop and cascode bias as shown in Fig. 5.6.

However, this circuit unfortunately can have a second stable state where all the currents are zero, and the circuit will remain in this stable state forever. To guarantee this condition

doesn't happen, it is necessary to add a start-up circuit that only affects the operation if all the currents are zero at start up. The start-up circuit consisting of transistors M_{15}, M_{16}, M_{17} and M_{18} is also shown in Fig. 5.6. In the state that all currents in the bias loop and cascode bias are zero, the gate voltage of M_{17} (i.e., V_{bn1}) would close to V_{SS}. Thus M_{17} would be turn off. In general, we assume the $(W/L)_{18}$ very small, so the output impedance of M_{18} would very large. Since the M_{18} operates as a high-impedance load that is always on. The gates of M_{15} and M_{16} would be pulled high. So M_{15} and M_{16} then will inject currents into M_9 and M_{14}, respectively, which will start-up the bias loop. Once the loop starts up, output bias voltages, V_{bn1}, V_{bn2}, V_{bp1} and V_{bp2}, would settle to a stable state, then M_{17} would be turn on and sinking all of the current from M_{18}. Since I_{D18} equals I_{D17} and the $(W/L)_{17}$ is much larger then $(W/L)_{18}$, the drain-source voltage of M_{17} would be small than the source-drain voltage of M_{18}. In other words, M_{18} operates in the saturation region and M_{17} operates in the triode region. This pulls the gate voltages of M_{15} and M_{16} low and thereby turns them off so they no longer affect the bias loop. Sometimes the P-channel transistor is replaced by an actual resistor. Since M_{18} operates as high-impedance load, the value of actual resistor should be very large without high accuracy. Basically, the resistor is realized by well resistor in CMOS process.

According to the discussion above, the transient response of the bias circuit is shown in Fig. 5.7

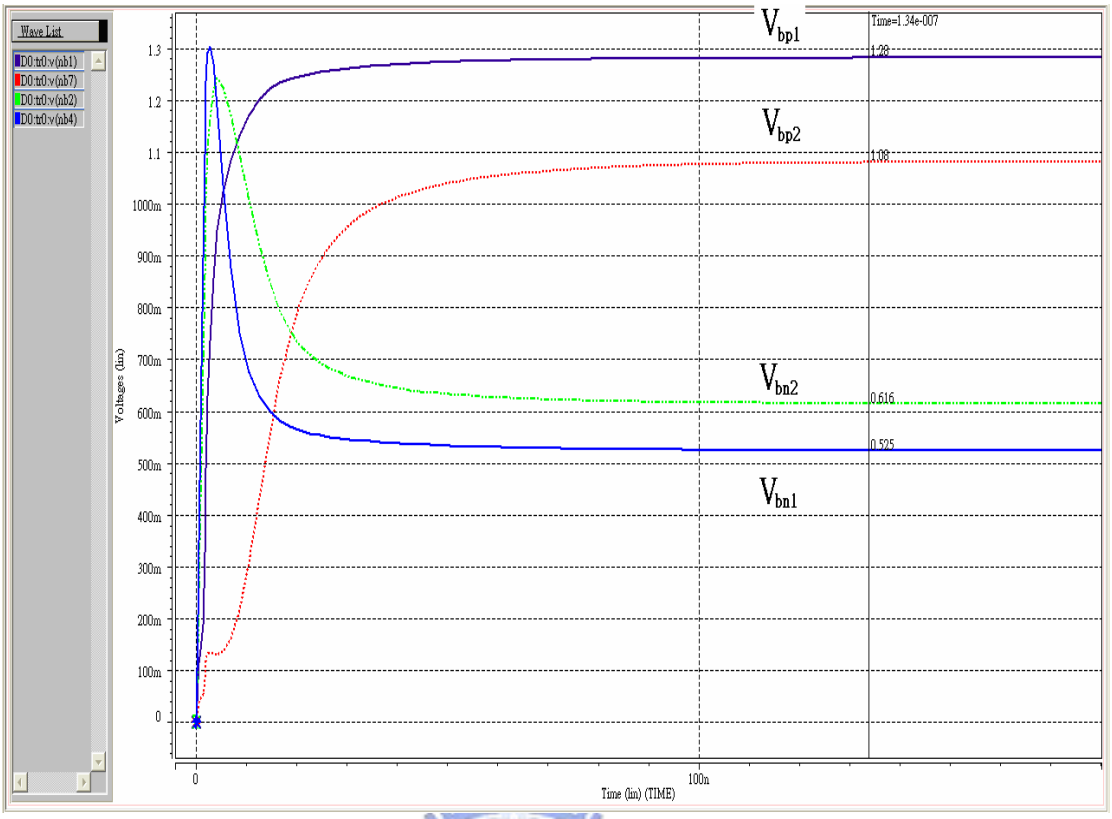


Fig. 5.7：Simulated bias output voltages

5.2.4 Common-Mode Feedback

Common-mode feedback (CMFB) circuit is required in a fully differential amplifier to define the high-impedance output nodes. The desired op-amp output common-mode voltage is usually equal to half of the supply voltage for maximizing the output swing. When signals are processing differential, the CMFB hence tries to keep the common mode of the output signal in the middle of the available output swing. In general, two kinds of CMFB can be chosen in the fully differential op-amp, which are continuous-time approach and switched-capacitor approach. In order to minimize the power consumption, the switched-capacitor CMFB circuit is a better choice in switched-capacitor applications.

The common mode output level of the amplifier is maintained by the switched-capacitor feedback shown in Fig. 5.8. The common-mode feedback (CMFB) circuit is based on the use of switched-capacitor circuits. In this approach, capacitors labeled C_2 generate the average of the output voltages, which is used to create control voltages for the op-amp output current sources, M_5 and M_6. The dc voltage across C_2 is determined by capacitors C_1, which are switched between bias voltages and between being in parallel with C_2. This circuit acts much like a simple switched-capacitor low-pass filter having a dc input signal. The bias voltage are designed to be equal to the difference between the desired common-mode voltage (V_{cm}) and the desire control voltage (V_{bn1}) used for the op-amp current sources.

The capacitor C_2 equals 1pF and form a voltage divider to drive node V_{CMFB}, the gates of the NMOS current source transistors in the output stage. Only changing in the common-mode voltage of the amplifier output are coupled to node Vctrl, which returns the common-mode output voltage to the desired level through negative feedback. During phase φ1, corrective charges are transferred onto C2 from refresh capacitor C1 to prevent drift in the common-mode output voltage [Mar 97].

The capacitors being switched, C_1, might be between one-quarter and one-tenth the sizes of the non-switched capacitors, C_2. Using larger capacitance values overloads the op-amp more than is necessary during the phase ϕ_1, and their size is not critical to circuit performance. Reducing the capacitors too much causes common-mode offset voltages due to charge injection of the switches. Normally, all of switches would be realized by minimum length N-channel transistors only, except for the switches connected to the outputs, which are realized by transmission gates to accommodate a wider signal swing.

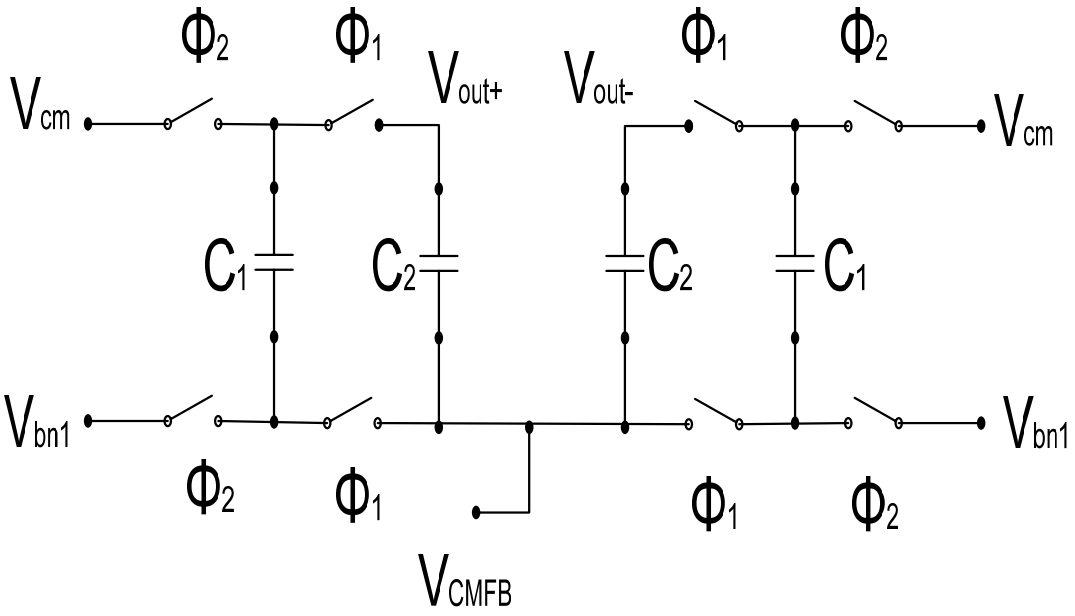


Fig. 5.8：A switched-capacitor CMFB circuit

5.2.5 Design of the Gain boosting folded cascode op-amp

The amplifier topology choice plays a critical role in the low-voltage, high speed, and low-power integrator design. A fully differential folded-cascode OTA with gain-boosted technique is applied to the proposed modulator and is shown in Fig. 5.9. Due to the fully differential architecture of the op-amp, the common mode feedback circuit (CMFB) must be added. The key performance parameters for the op-amp are summarized in Table 5.1.

The frequency response of the fully differential folded-cascode operational amplifier simulated by HSPICE is shown in Fig. 5.10.

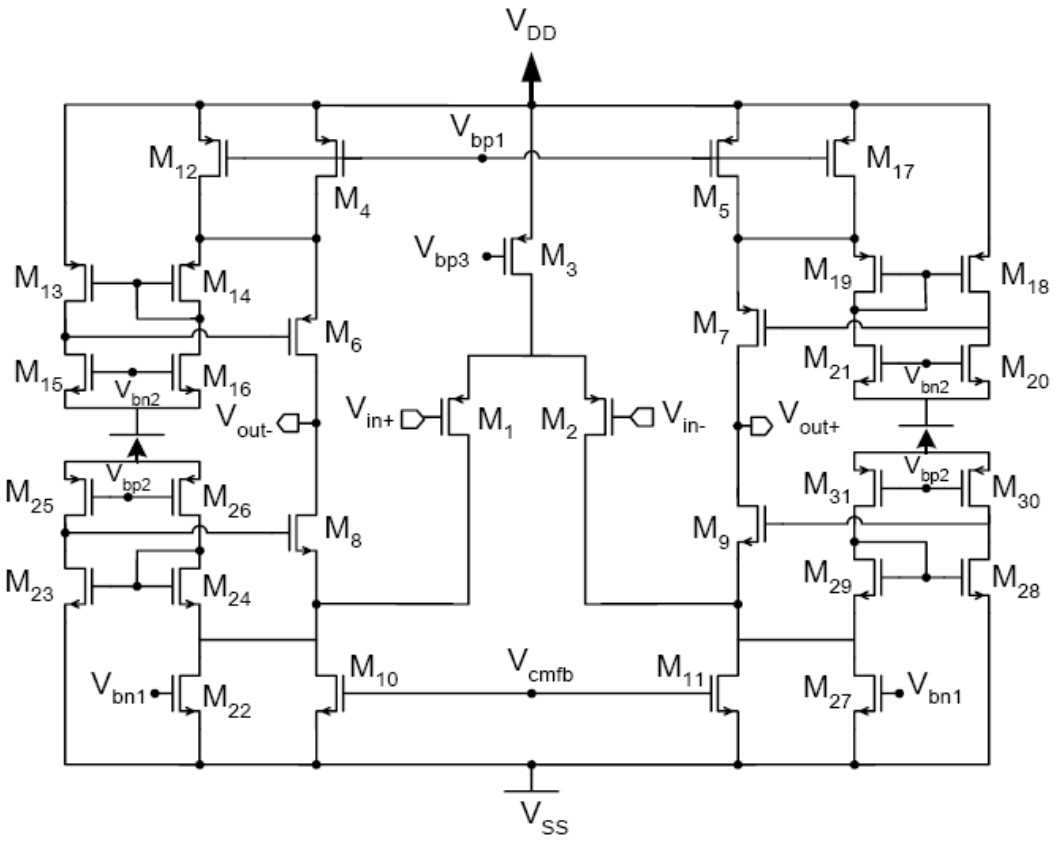
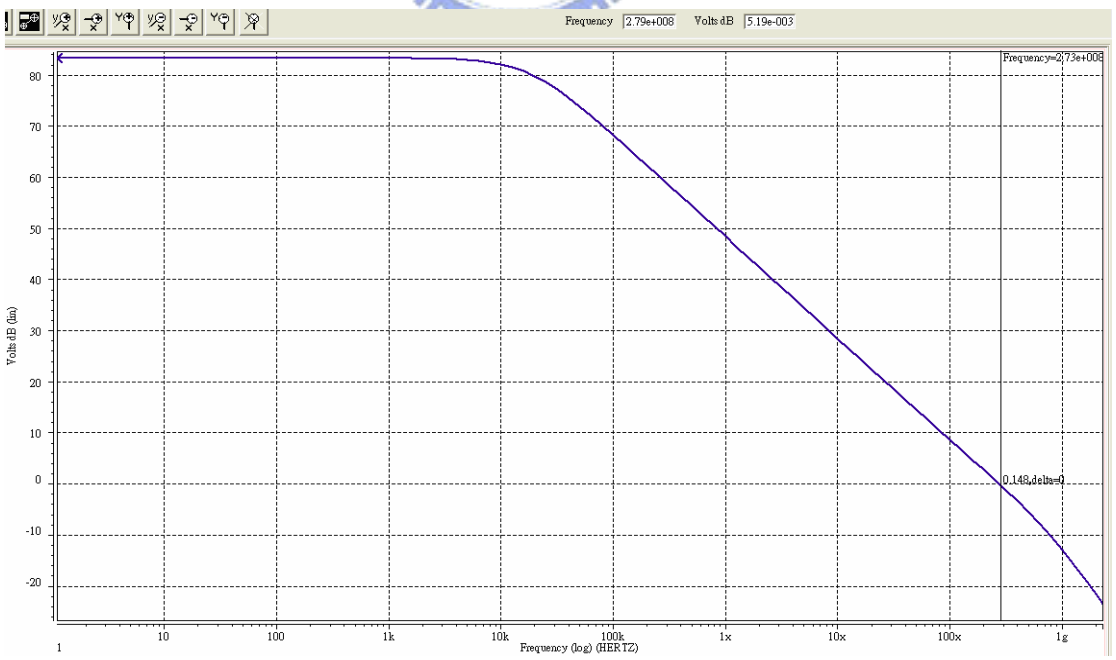
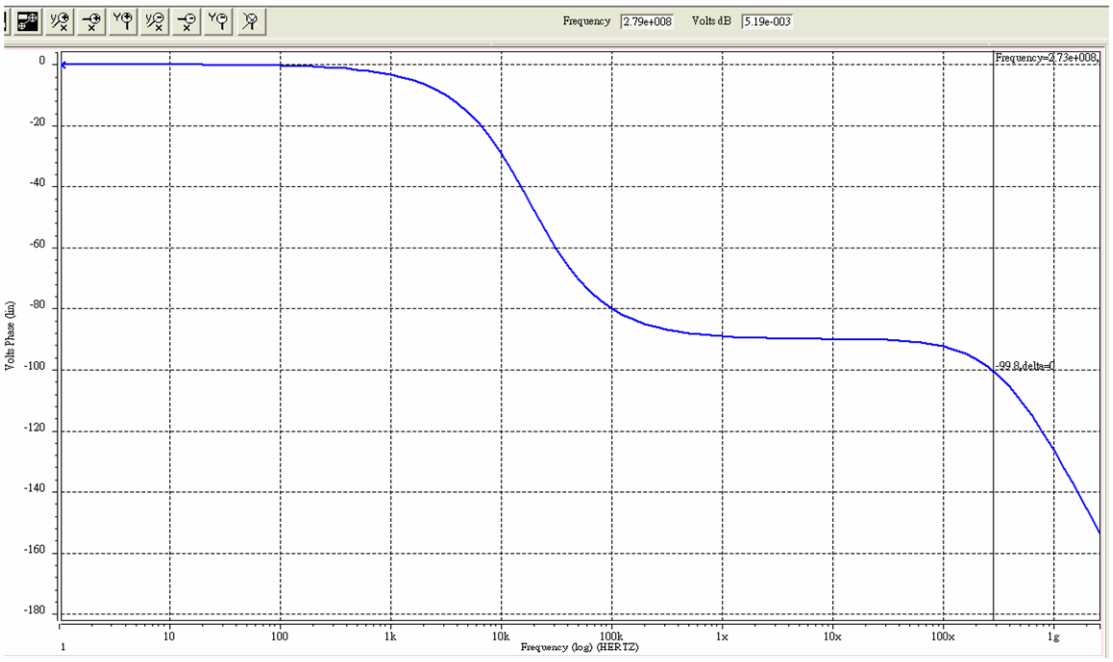


Fig. 5.9：The gain-boosting folded-cascode OTA



(a)



(b)

Fig. 5.10：Simulated frequency response of the amplifier:(a) output gain (b) output phase.

Table 5.1 Simulated summary of the amplifier.

Op-amp Specification	Value
DC Gain	84 dB
Load	6 pF
GBW	273 MHz
Phase Marge	80 degree
Slew Rate	281 V/μs
Power Dissipation	7.95 mW
Technology	0.18μm COMS

5.3 Comparator

The purpose of the comparator in a sigma-delta modulator is to quantize a signal in the loop and provide the output of the modulator. Since the comparator locates after the loop gain block and before the output terminal, the nonidealities associated with it can be shaped by the loop in the same manner as the quantization noise. This means that, at the frequencies of interest, the comparator nonidealities of a SDM can be reduced significantly.

In general, two kinds of comparator are widely used in the SDM design, which are the regenerated latching comparator and dynamic comparator with a pre-amplifier input stage, respectively.

A simple regenerative latch comparator is shown in Fig. 5.11. The comparator consists of a dynamic latch followed by a simple static S-R latch. When the control signal ϕ_1 is low, the nodes n_1 and n_2 are pulled high and nodes S and R, which are the inputs to an S-R latch, are consequently both pulled low. According to the S-R exciting table, when S=0 and R=0, the outputs Q and Qb are maintained to the previous states. When the control signal ϕ_1 goes high, nodes n_1 and n_2 are released and the regenerative feedback is produced by the cross-coupling of transistors $M_{2A}-M_{2B}$ and $M_{5A}-M_{5B}$.

The differential pull-down currents developed by the input transistors $M_{1A}-M_{1B}$ latch the comparator in one direction to drive S=1, R=0 (or S=0, R=1). Therefore, the outputs are set to Q=1, Qb=0 (or Q=0, Qb=1). In the comparator the cross-coupled devices, $M_{2A}-M_{2B}$ and $M_{5A}-M_{5B}$, are stored at their drains, rather than at the sources, to eliminate the offset and speed up the regeneration process.

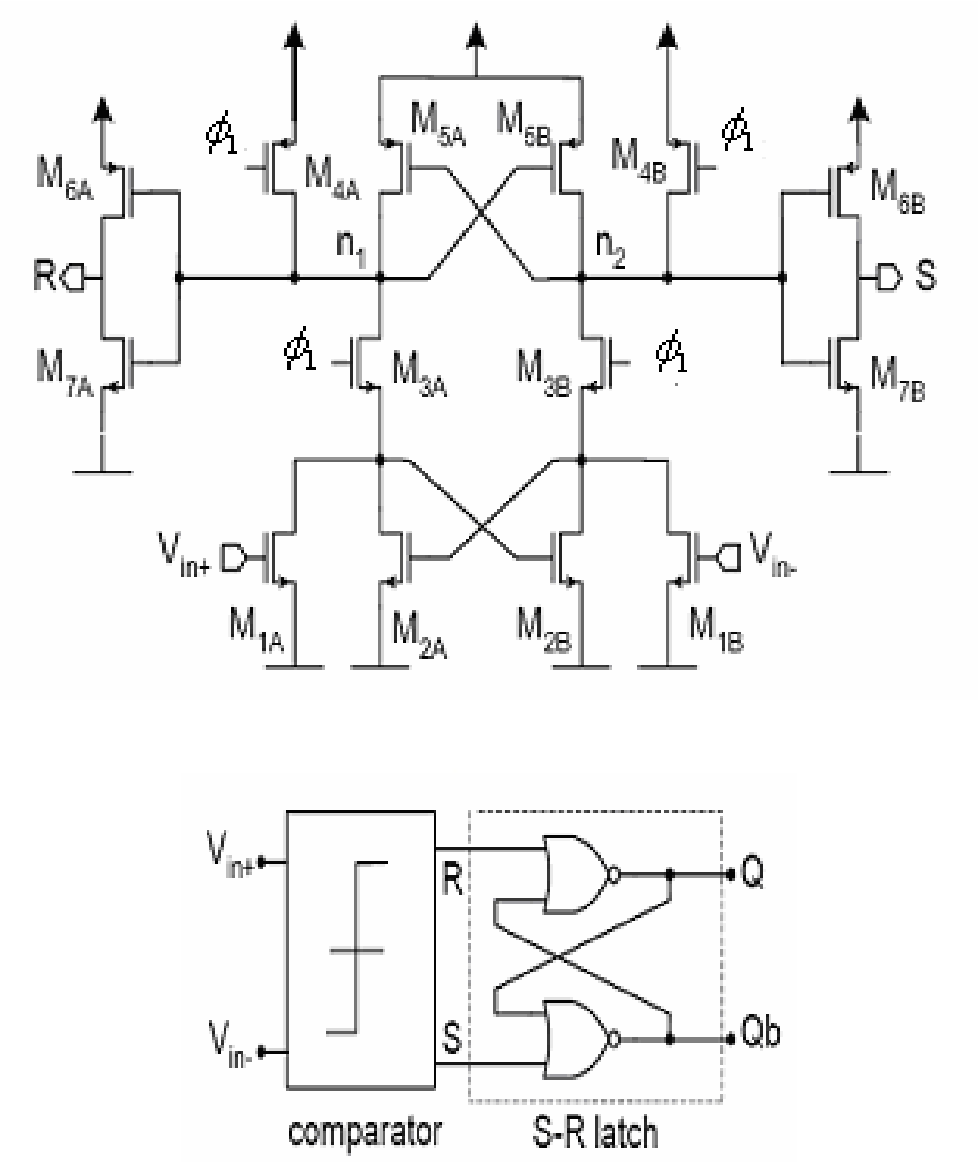


Fig. 5.11：Regenerative latch comparator

A fully differential comparator can be also realized by employing a pre-amplifier in the input stage, as Fig. 5.12 shows in a simplified form for a CMOS implementation. The rationale behind this architecture is as follows: the pre-amplifier is used to obtain higher resolution and to minimize the effects of kickback [Yin 90]. The output of the pre-amplifier, although it is lager than the comparator input, is still much smaller than the voltage levels needed to drive the digital circuitry. The track-and-latch stage then amplifies this signal further during the track phase, and then amplifies it again during the latch-phase, when the

positive feedback is enabled. The positive feedback regenerates the analog signal into a full-scale digital signal.

A very important consideration for comparators is to ensure that no memory is transferred from one decision cycle to the next. For example, if a comparator toggles in one direction, it might have a tendency to stay in that direction. This tendency is called hysteresis. In order to eliminate it, one can reset the different stages before it enters the track mode. This might be achieved by connecting differential nodes together using switch M_T before it enters the track mode.

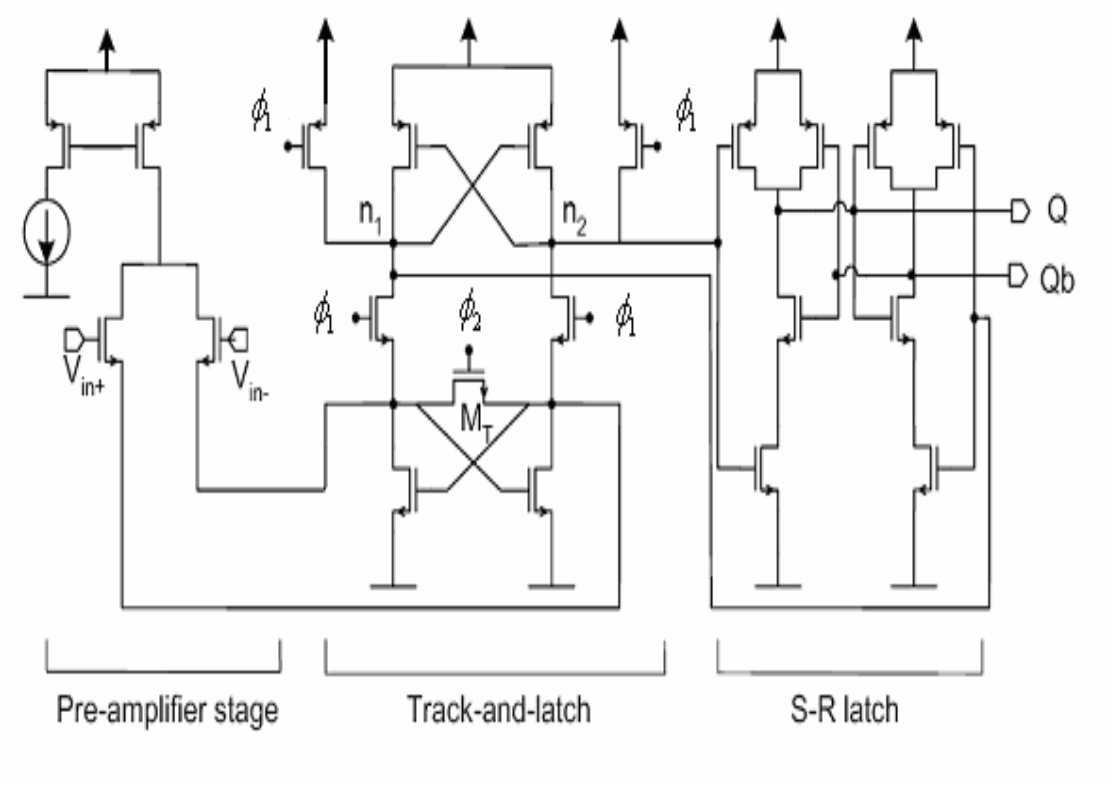


Fig. 5.12：The dynamic comparator with a pre-amplifier input stage

The dynamic comparator with a pre-amplifier input stage has been used to implement the quantizer. Fig. 5.13 shows the output voltage as a function of the input voltage, and the hysteresis region is depend on the clock rate (ϕ_1) and input signal frequency. Fig. 5.14 shows

the output waveform of the comparator for a rail-to-rail sinusoidal input.

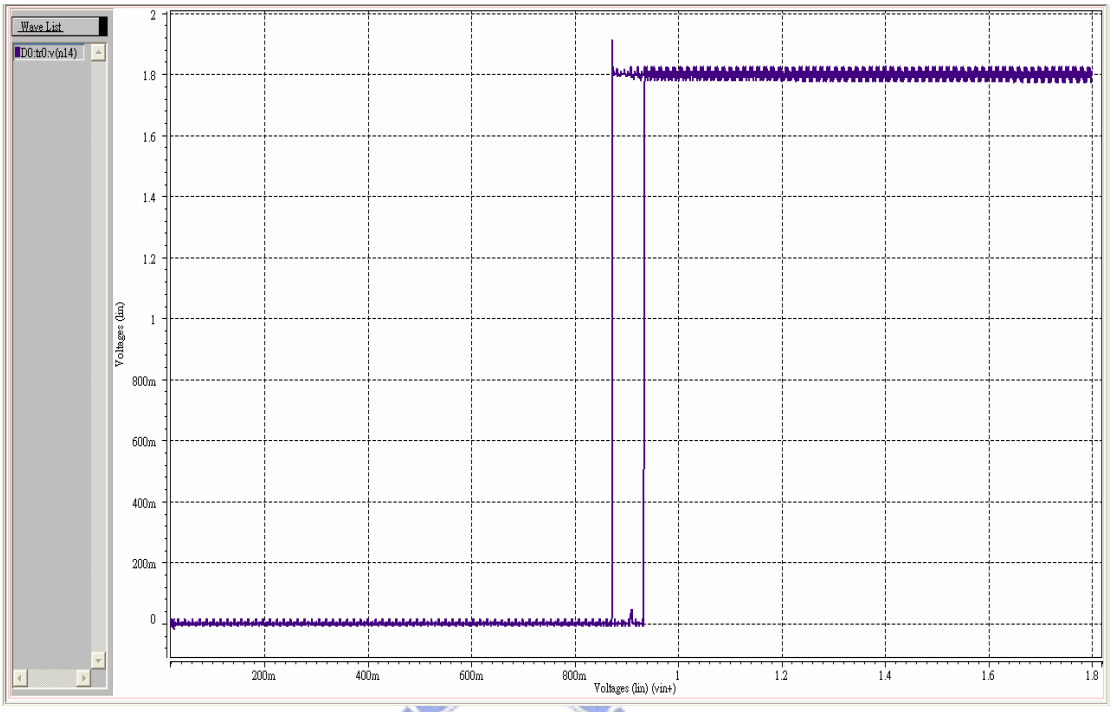


Fig. 5.13：Simulated output vs. input voltage of the comparator

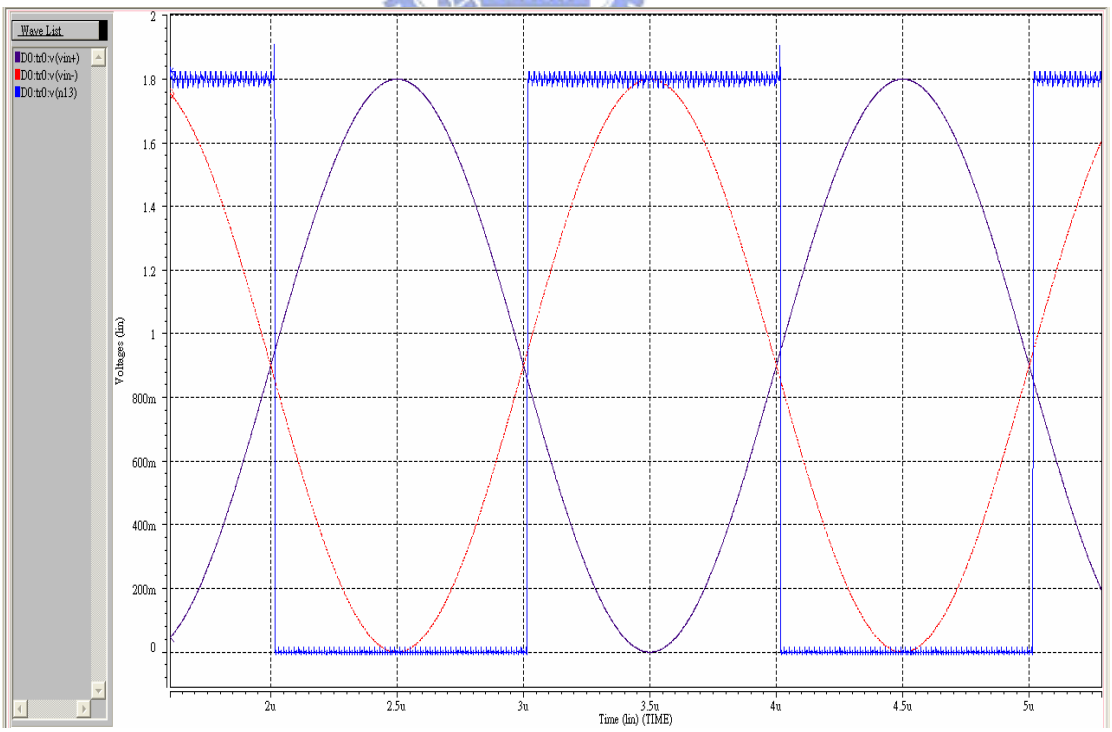


Fig. 5.14：Input and output waveform of the comparator

5.4 Clock generator

In this prototype, we may at least need two pairs of non-overlapping clocks. These clocks determine when charge transfers occur or not. For the non-overlapping property, they guarantee charge won't be inadvertently lost.

The clock generation circuit used in the experimental prototype is shown in Fig.5.15. The clock phase requirements of the second-order multi-bit delta-sigma modulator are ϕ_{1n}, ϕ_{1p}, ϕ_{1nd}, ϕ_{1pd}, ϕ_{2n}, ϕ_{2p}, ϕ_{2nd} and ϕ_{2pd}. ϕ_{1n} and ϕ_{2n} are non-overlapping clocks and ϕ_{1nd} and ϕ_{2nd} are slighter delayed than ϕ_{1n} and ϕ_{2n}, respectively.

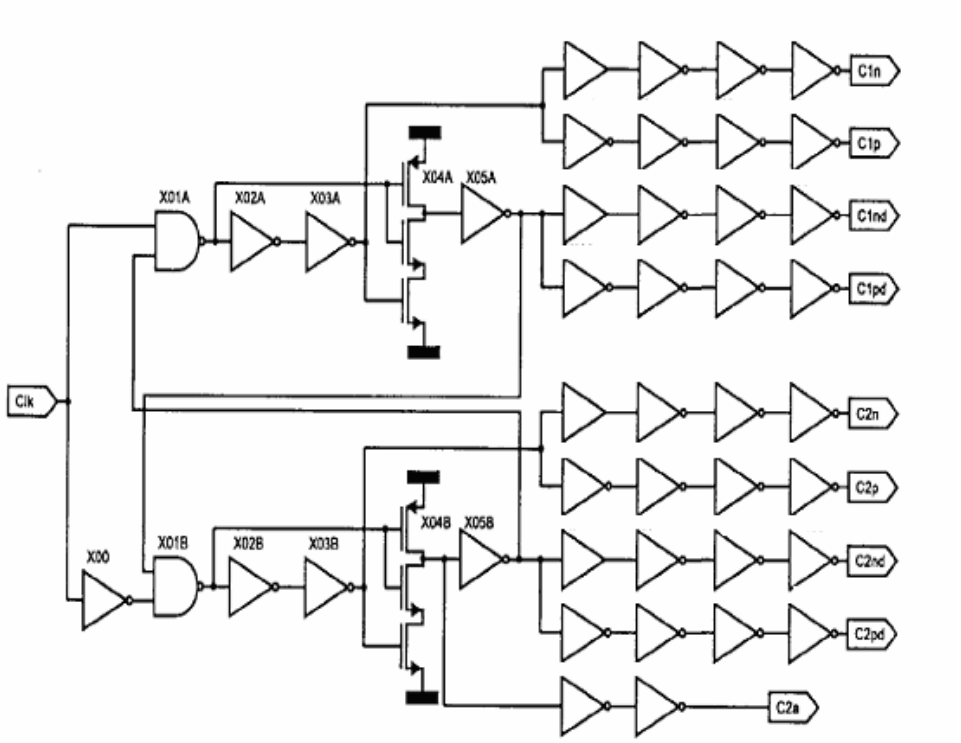
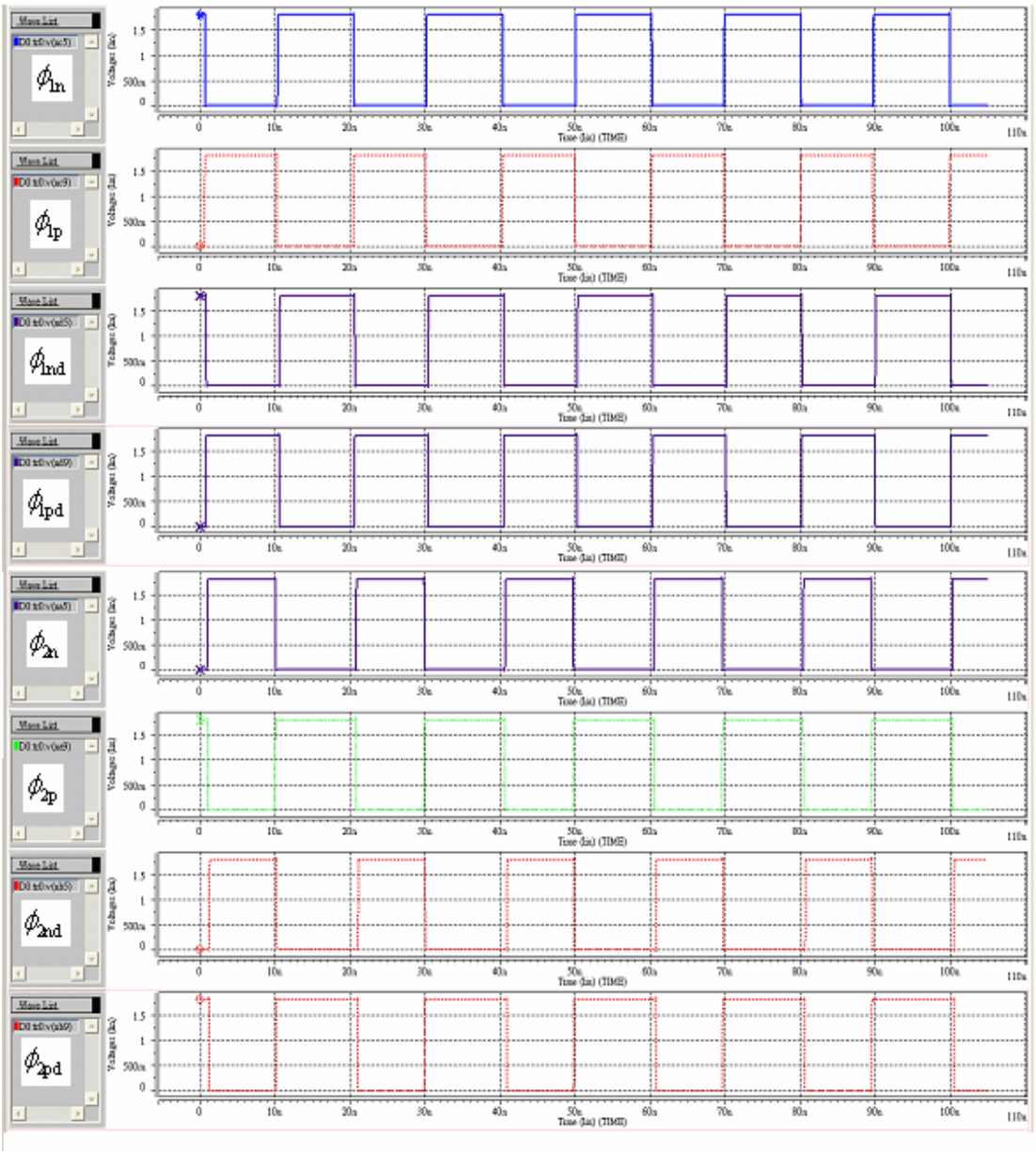
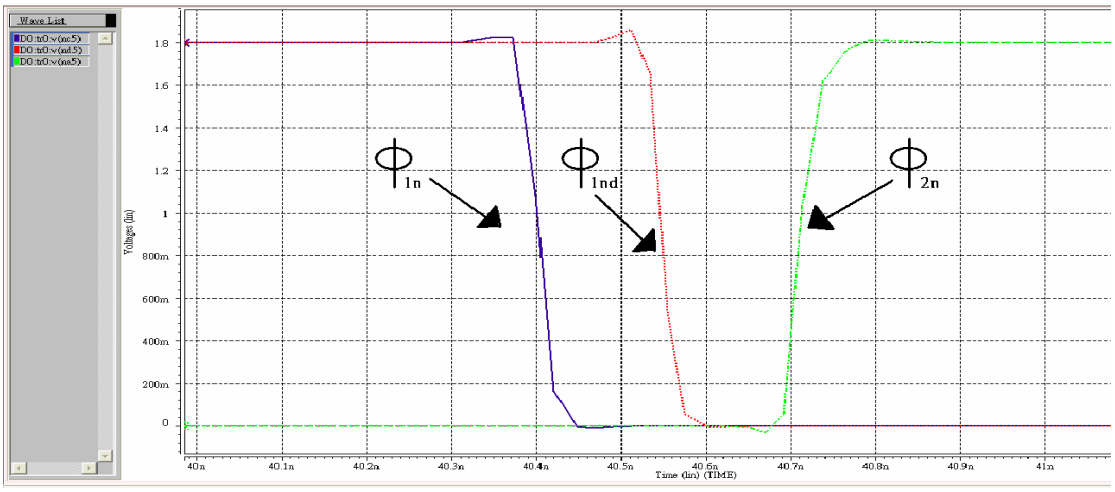


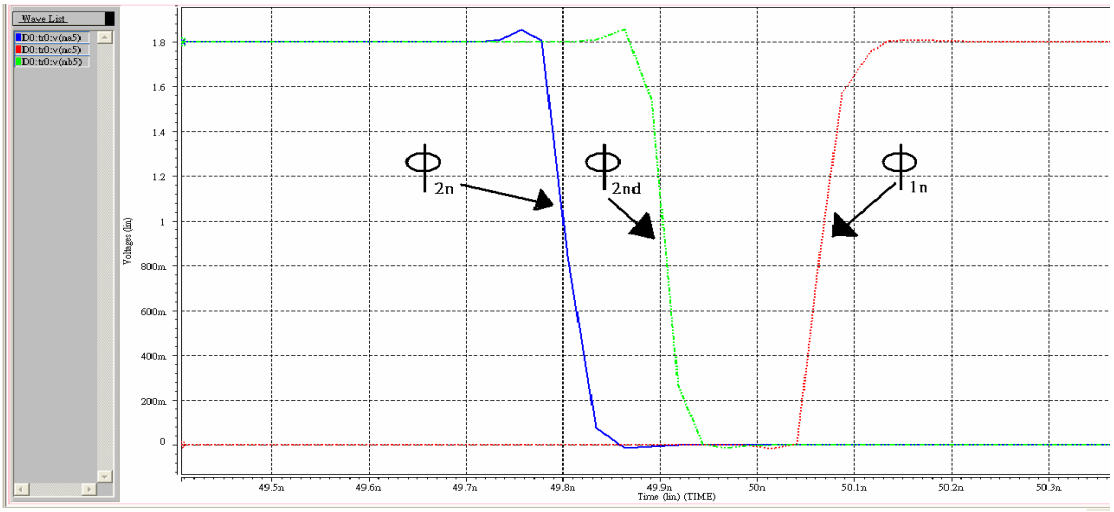
Fig. 5.15：Two-phase non-overlapping clock generator


ϕ_{1n}
ϕ_{1p}
ϕ_{1nd}
ϕ_{1pd}
ϕ_{2n}
ϕ_{2p}
ϕ_{2nd}
ϕ_{2pd}
Time (lin) (TIME)

(a)



(b)



(c)

Fig. 5.16：Relationship of the simulated clock signals

5.5 Switch

Now we can consider the switch by the integrator operating in sampling mode as show in Fig. 5.17 (a) for understand the characteristic of the switch. The switches and sampling capacitor are shown in Fig. 5.17 (b). Because S3 connects C_S to common voltage, the effect of S3 can be combined into S1. Consequently, the sampling circuit can be simplified to a switch S1 and sampling capacitor C_S as show in Fig. 5.17 (c).

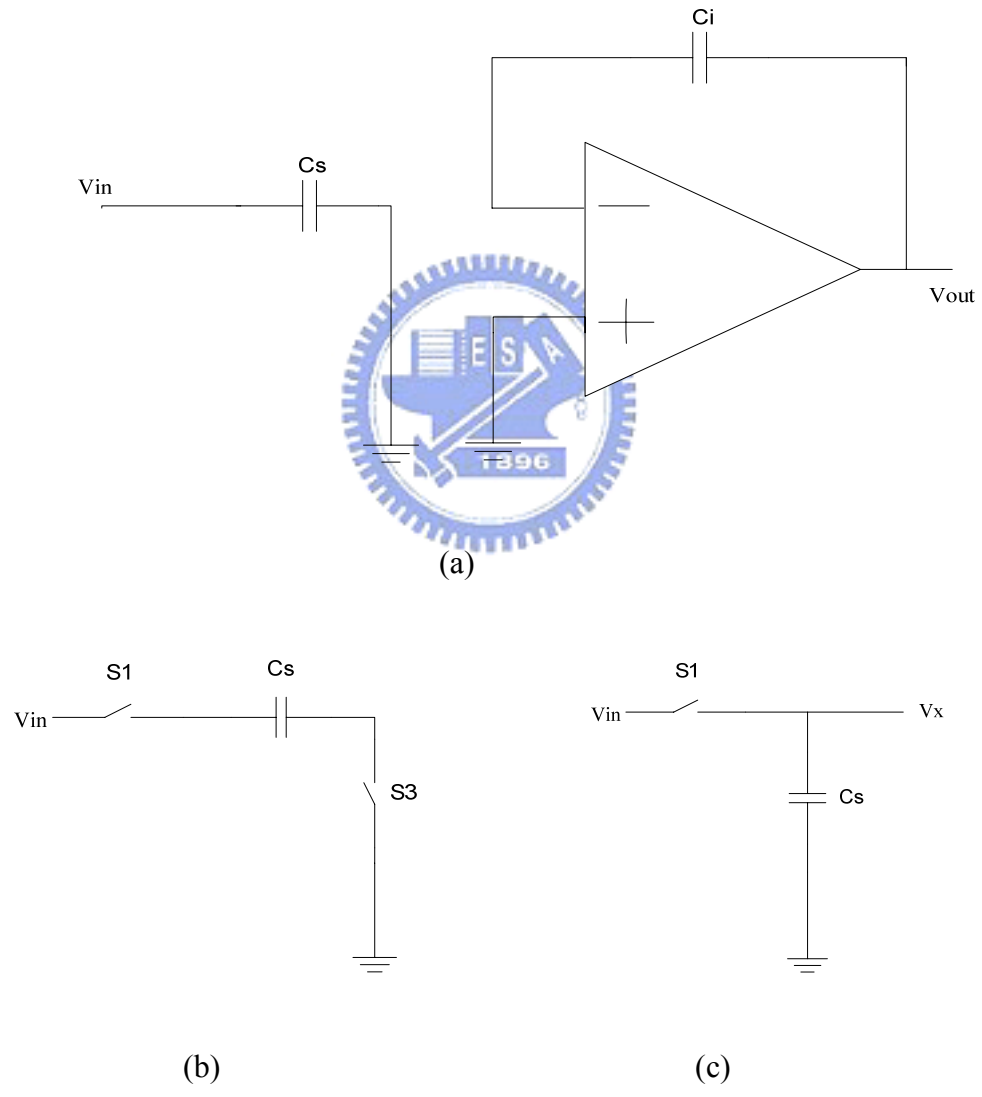


Fig. 5.17：(a) sampling mode for a switch-capacitors integrator (b) a sampling circuit, and (c) a simplified sampling circuit

The sampling circuit speed is an important factor to influence the harmonic distortions of the integrator. Usually, the definition of sampling circuit speed is the time required for the output voltage to go to from common-mode voltage to the maximum input level after the switch turn on. Since the output voltage of the sampling circuit would take infinite time to become equal V_{in}, we consider the output (V_X) settled when it is within a certain error band, △V, around the final value. Thus, the speed specification must be accompanied by an accuracy specification as well. It should be noted that after switch turns on t_S seconds, we could consider the source and drain voltages to be approximately equal. From the sampling circuit in Fig. 5.18, we surmise that the sampling capacitor. Thus, a large (W/L) and a small capacitor must be used to achieve a higher speed sampling circuit.

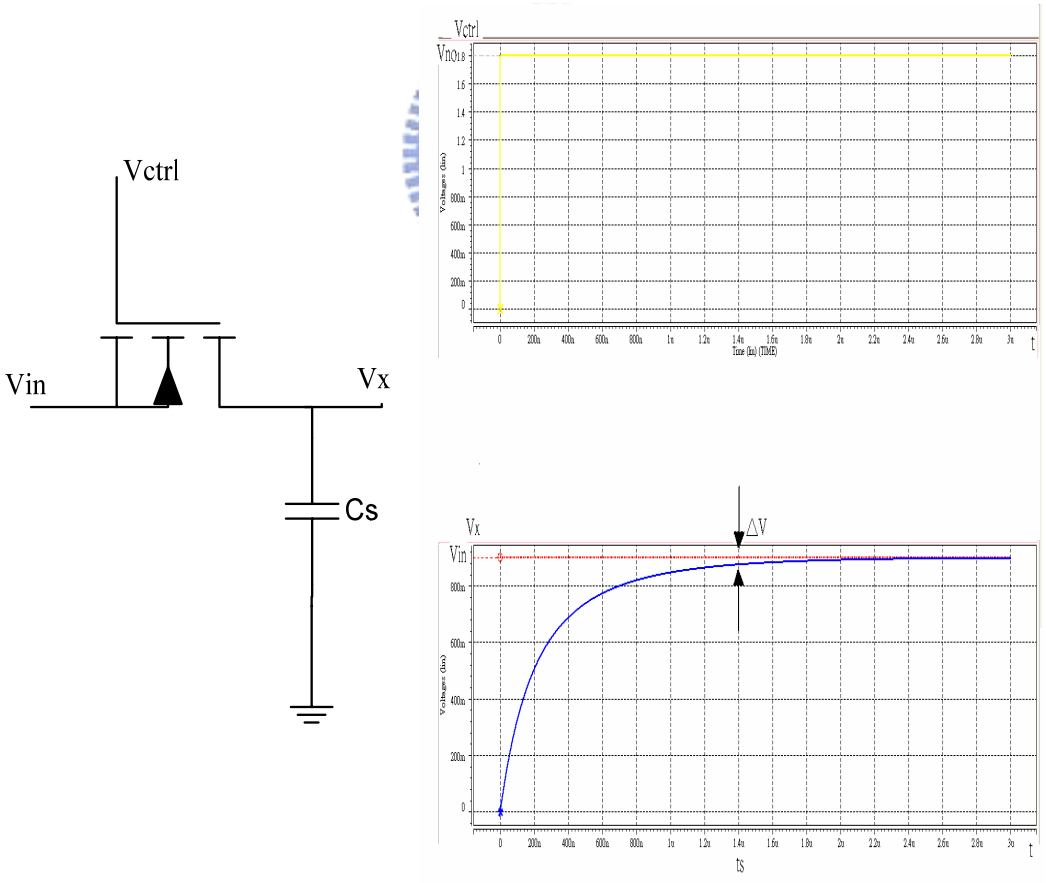


Fig. 5.18：Definition of speed in a sampling circuit

The analysis has mainly focused on four main types of sampling switches: a single NMOS transistor switch, a single PMOS transistor switch, the CMOS transmission gate, and the bootstrapped MOS switch, in Fig. 5.19. It is well known that the "on" resistance, R_{on}, for a transistor is nonlinear and introduces distortion to the performance of the switch.

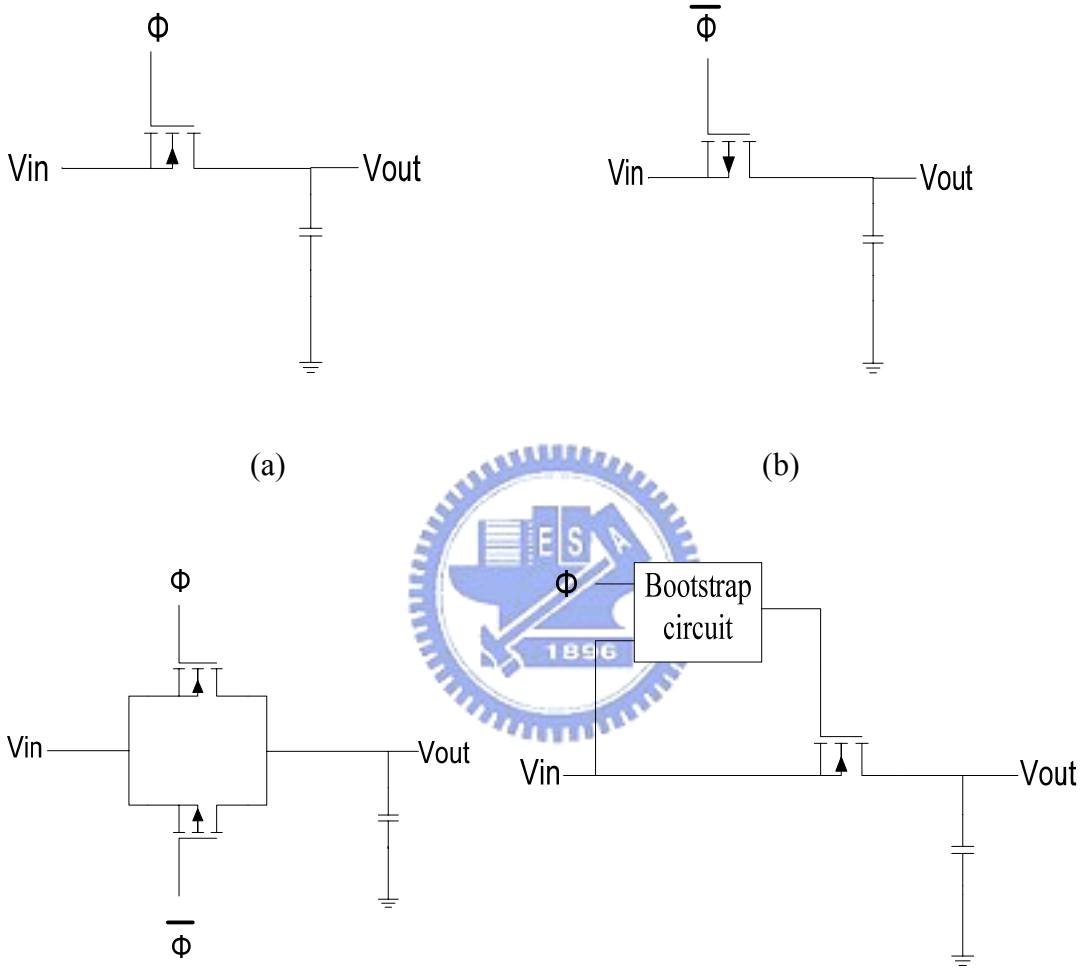


Fig. 5.19：Types of sampling switches (a) NMOS, (b) PMOS, (c) transmission gate, and (d) bootstrap NMOS

The "on" resistance for a single NMOS sampling switch, Fig. 5.19(a), can be written as

$$R_{onN} = \frac{1}{\mu_N C_{OX} (\frac{W}{L})_N (V_{GS} - V_{tN})} = \frac{1}{\mu_N C_{OX} (\frac{W}{L})_N (V_{DD} - V_{in} - V_{tN})} \tag{5.22}$$

Where W_N and L_N are the width and length, C_{OX} the oxide capacitance, and μ_N the mobility, of NMOS transistor. In the manner, the "on" resistance for a single PMOS sampling switch, Fig. 5.19 (b), can be written as

$$R_{onP} = \frac{1}{\mu_P C_{OX} (\frac{W}{L})_P (V_{SG} - |V_{tP}|)} = \frac{1}{\mu_P C_{OX} (\frac{W}{L})_P (V_{in} - V_G - |V_{tP}|)} \tag{5.23}$$

These equations show two important effects. First, a reduction of the supply voltage immediately increases the switch resistance since the overdrive voltage of transistor decrease. Second, the switch resistance is dependent on the source and drain voltages, or, in the case of switch, on the input signal. This generates harmonic. Both these effects can be reduced by employing transmission gates. The transmission gates, Fig. 5.19 (c), are comprised by a NMOS and PMOS transistor in parallel, an improved linearity for the resistance over the entire input voltage range is achieved. The equivalent resistance for the complementary NMOS and PMOS pair is defined (5.24).

$$\begin{aligned} R_{onC} &= R_{onN} \,||\, R_{onP} \\ &= \frac{1}{k_N (V_{DD} - V_{in} - V_{tN})} \,||\, \frac{1}{k_P (V_{in} - |V_{tP}|)} \\ &= \frac{1}{k_N (V_{DD} - V_{tN}) - (k_N - k_P) V_{in} - k_P |V_{t_P}|} \end{aligned} \tag{5.24}$$

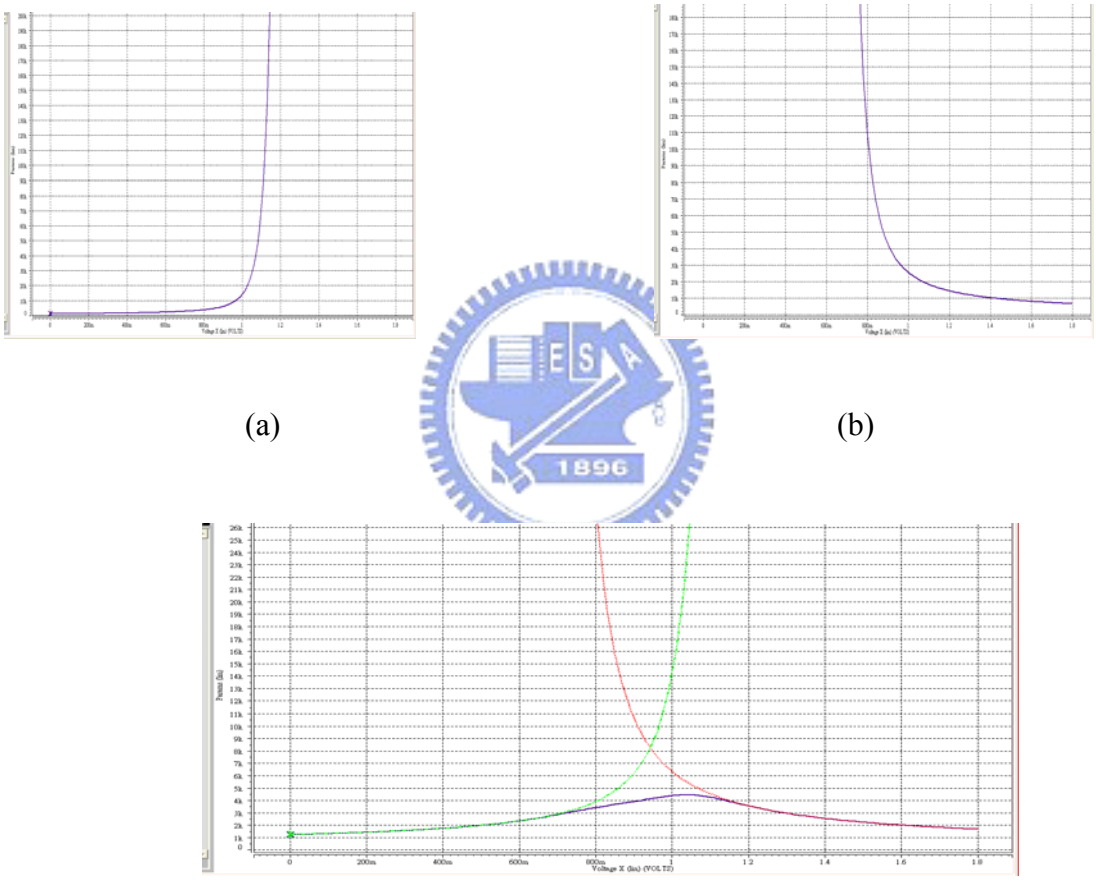
where

$$k_N = \mu_N C_{OX} (\frac{W}{L})_N \quad \text{and} \quad k_P = \mu_P C_{OX} (\frac{W}{L})_P \tag{5.25}$$

Here, the PMOS is scaled so that the width and length is equal to the NMOS transistor. However, if the PMOS transistor is scaled so that

$$\left(W/L\right)_P = \left(\mu_N/\mu_P\right)\left(W/L\right)_N \tag{5.26}$$

Then (5.24) will be independent of the input voltage level, if the small dependence of V_{in} on the threshold voltages, V_{tP} and V_{tN}, is neglected.



(a) (b)

(c)

Fig. 5.20：Simulated on-resistance of (a) NMOS, (b) PMOS, and (c) transmission gate devices

5.6 Simulation of System Circuit

After behavior simulation with MATLAB, we must try to implement the circuit of this modulator as shown in Fig.5.21. The pre-simulation results using HSPICE are provided in this session. After FFT analysis in MATLAB, the output spectrum is shown in Fig. 5.22 reveals peak SNDR about 74dB with the input signal of –7dB. The SNDR diagram of simulation is shown in Fig. 5.23, and the dynamic range of this modulator is about 82dB, satisfying a resolution 13-bit. The overall performances are shown in Table 5.2.

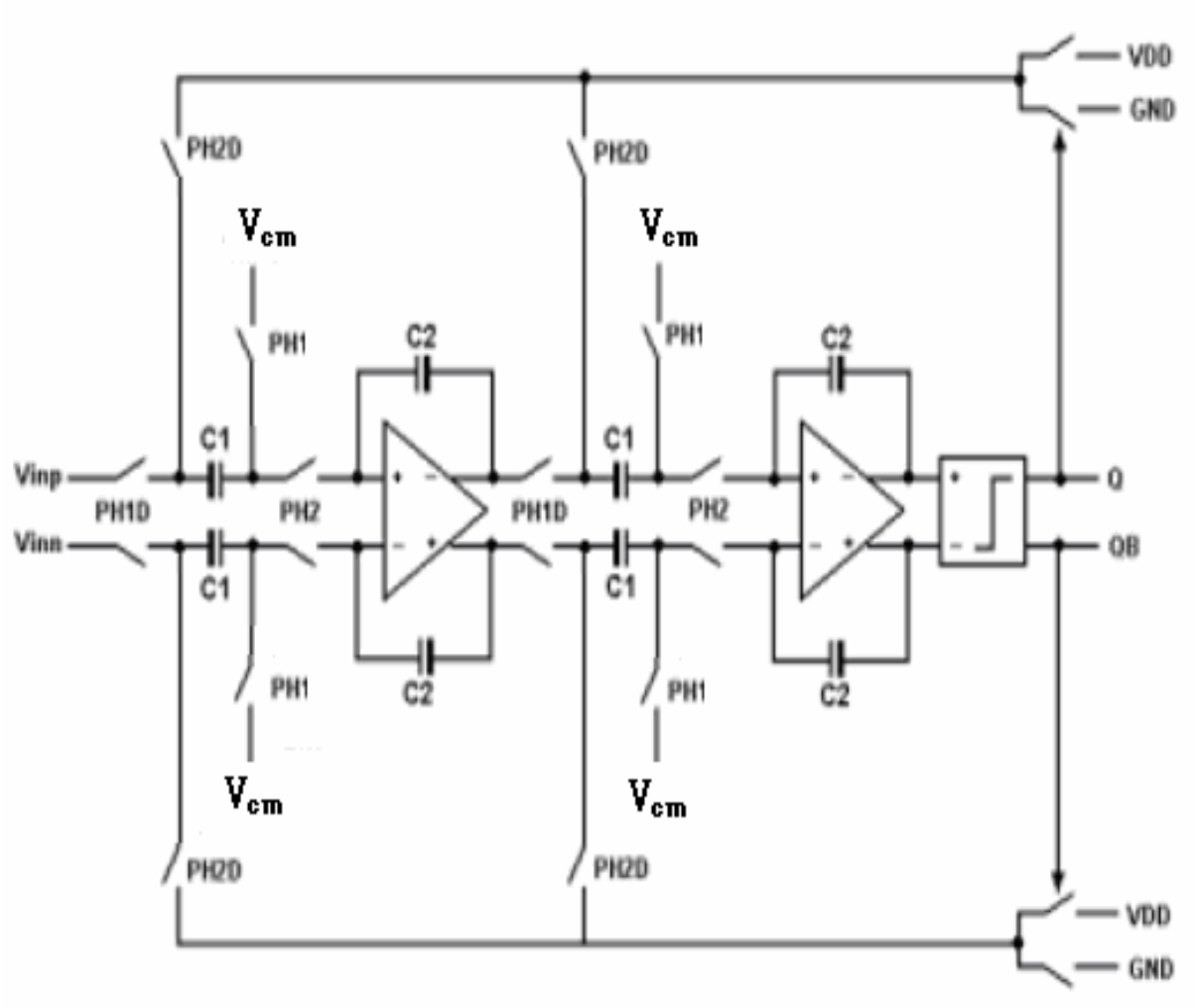


Fig. 5.21 Schematic of modulator circuit

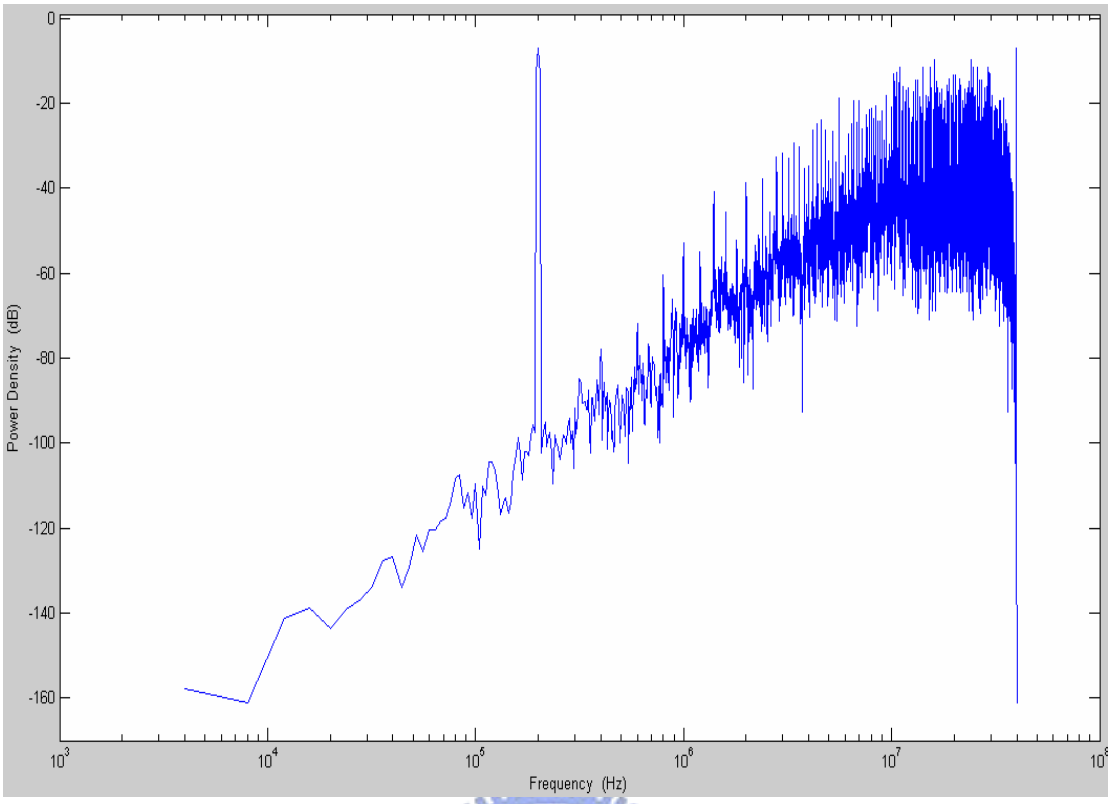


Fig. 5.22 The output spectrum of –7dB input

Table. 5.2 The performance summary table

Parameter	Pre-simulation
Order	2
Power supply	1.8V
Power dissipation	16.96mW
$SNDR_{peak}$	74dB
Resolution	12-bit
Signal Bandwidth	276KHz
OSR	72
Technology	0.18um CMOS Process

Chapter 6

Conclusions and Future Works

The power estimation is presented for a sigma-delta converter with a certain accuracy and bandwidth specification. The power estimation can be derived into the analog power consumption and the digital power consumption. The digital power consumption is not included the DEM for the DAC. So the model is not faultless for the digital power consumption for the Multi-bit sigma-delta converter. This point can be improved in the future.

The discrete-time second-order one-bit Sigma-Delta Modulator is designed for the ADSL-CO. The 14-bits would be required in the ADC for the ADSL-CO. But the dynamic range of this modulator is about 82dB, satisfying a resolution 13-bit. We can increase the bits of the quantizer to get the better performance.

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