硬體規格描述語言的觀察度分析
以達成有效率的功能驗證和錯誤診斷

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摘要

以模擬為基礎的功能驗證依然是驗證硬體規格描述語言所描述之硬體電路的主要方法之一。在這個以模擬為基礎的功能驗證的框架中，電路模擬的結果必須在某些特定的點(我們叫它們觀察點)上面和我們所期望該點該有的正確值做比對來判斷電路行為的正確性。電路裡的設計錯誤只有在模擬值的錯誤出現在觀察點上時，才能夠被發現。然而，大部分的功能涵蓋量度都沒有直接地去考慮到偵測內部設計錯誤的所需要的觀察度需求。以觀察度為基礎的程式碼涵蓋量度是

第一個考慮到偵測內部設計錯誤的所必須的觀察度需求之程式碼涵蓋量度。然而，這個方法裡面所使用的標籤只能夠表達兩種結果，標籤有出現在觀察點跟沒出現在觀察點兩種。僅能提供兩級的觀察度評估。這個不準確性可能造成高估了驗證的完成度，使得設計錯誤有機會隱藏而沒被發現。鑒於此，在這篇論文哩，我們發展了一套新的機率式的觀察度量度以及其有效的計算演算法。我們的機率式的觀察度量度可以當成一個新的以觀察度為基礎的程式碼涵蓋量度。因為是機率式的量度所以可以提供零到壹任何一個數值，比起兩級的量度結果，相信可以準確不少。也可以用來指出在上一階段驗證中電路內部觀察度較低的點，讓驗證的資源可以正確被導到這些上階段驗證的弱點上。

如果模擬的時候發現了設計錯誤在電路裡面，我們就必須對這個以硬體規格描述語言寫成的電路程式碼進行設計錯誤診斷。針對這個問題，已存在的研究大多都試著去抽取出一個較小的錯誤候選者集合來加速找到真正設計錯誤的過程。然而，給一個錯誤候選者集合後，在內部找到真正的設計錯誤依然需要花上不少時間。有一個叫做除錯優先序的方法被發展除來加速這個在候選者集合內找到真正錯誤的過程。這個方法的概念是把每個錯誤候選者都依照它為錯誤的可能性依序條列呈現下來。但是，用以量度錯誤候選者為錯誤可能性的量度

(信心分數)卻因為缺少考慮錯誤有可能被遮掩而有了瑕疵。因此，我們修改了針對硬體規格描述語言的觀察度分析，發展出新的「機率性信心分數」來提供更準確、更可靠的除錯優先序。這個新的除錯優先序理論上可以和任何種抽取錯誤候選者集合的方法做搭配。如此可以加速在除錯候選者及合理找到真正設計錯誤的過程。

Observability Analysis on HDL Descriptions for Efficient Functional Validation and HDL Source Code Debugging

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Abstract

Simulation-based *functional validation* is still one of the primary approaches for verifying Design Under Validation (DUV) described in a Hardware Description Languages (HDL). In simulation-based functional validation framework, the simulation results should be compared with the expected values on some signals of interest (called Observation Points (OPs) in this thesis) to check for the correctness of certain behaviors on the implementation. Design errors are uncovered only if the erroneous effects of the design errors cause incorrect simulation values on the OPs.

Most of functional coverage or code coverage metrics for HDL designs do not explicitly consider this observability requirement for revealing internal design errors. Observability-based Code COverate Metric (OCCOM) [18] is the first code coverage metric considering the essential observability issue. However, the applied *tags* can only be observed or unobserved, providing only two levels of measurement (1 and 0). This inaccuracy may overestimate completeness of verification and let internal design errors remain hidden. Therefore, in this dissertation, we develop a new probabilistic observability measure and its efficient computation algorithm. The probabilistic observability measures that can provide any intermediate values between 0 and 1 can be used as a new and more accurate observability-based code coverage metric. In addition, it also can be used to point out hard-to-observe points, leading verification resources to these weak portions of the verification process.

If simulation finds that some simulation values are different from the expected values on the OPs, design error diagnosis for the DUV that is modeled in a HDL is needed. Existing approaches for this HDL debugging problem attempt to extract a reduced error candidate set to accelerate the HDL debugging process. However, locating true design errors in the derived candidate set may still consume much valuable time. A *debugging priority* method [46] was thus proposed to speed up the error searching process in the derived error candidate set. This idea is to display error

candidates in an order that corresponds to an individual's degree of suspicion such that design errors can be displayed in the front of the candidate list. However, the applied Confidence Score (CS) has some flaws in estimating the likelihood of correctness for error candidates due to error masking. This reduces the degree of accuracy in establishing a *debugging priority*. Therefore, we modify the probabilistic observability measure for HDL descriptions to form a new Probabilistic Confidence Score (PCS) with the consideration of error masking in order to provide more reliable and accurate *debugging priority*. This new PCS-based *debugging priority* method can cooperate with almost any kinds of approaches that extract a reduced set of error candidates to further accelerate the error searching process in the extracted error candidate set.

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