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Electrical Properties of Metal–Silicon Nitride–Hydrogenated Amorphous Silicon Capacitor Elucidated Using Admittance Spectroscopy

Ming-Ta HSIEH*, Jenn-Fang CHEN, Kuo-Hsi YEN[1], Hsiao-Wen ZAN[1], Chan-Ching CHANG[2], Chih-Hsien CHEN[2], Ching-Chieh SHIH[2], and Yeong-Shyang LEE[2]

Department of Electrophysics, National Chiao Tung University, Hsinchu, Taiwan 30050, Republic of China
[1]*Department of Photonics and Institute of Electro-Optical Engineering and Department of Photonics and Display Institute, National Chiao Tung University, Hsinchu, Taiwan 300, Republic of China*
[2]*AU Optronics Corporation, Technology Center, Hsinchu, Taiwan 300, Republic of China*

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Detailed admittance spectroscopy was performed on a metal–silicon nitride–hydrogenated amorphous silicon (MIAS) structure. On the basis of the properties of hydrogenated amorphous silicon (a-Si:H), three simplified equivalent circuit models under various operating conditions (accumulation, depletion and full depletion) are presented along with an alternative direct measurement method at room temperature. Admittance spectroscopy shows that the interface states density between silicon nitride (SiN_x) and a-Si:H can be determined from the depletion equivalent circuit model. The resisivity and activation energy of a-Si:H can also be obtained using the accumulation and depletion equivalent circuit models. These models can be employed easily to monitor the fabrication parameters of thin-films transistors (TFTs) and to accurately and directly obtain the capacitance model parameters of TFTs. [DOI: 10.1143/JJAP.47.8714]

KEYWORDS: amorphous silicon, interface state density, admittance spectroscopy, capacitance, equivalent circuit model

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) is applied in numerous applications, particularly in thin-film transistors (TFTs).[1,2] The performance of a-Si:H TFTs is well known to depend strongly on the fabrication process such as gas dilution, and on the substrate temperature, pressure and RF power during film deposition.[3–5] A method of monitoring the fabrication process must be developed to elucidate the effects of these process conditions. Over the past years, capacitance–voltage (*C*–*V*) measurements have been a powerful diagnostic tool in studying the electrical properties and in monitoring the fabrication processes of metal–oxide–semiconductor (MOS) structures.[6] However, the *C*–*V* measurements of metal–insulator–a-Si:H (MIAS) are limited because of the high density of defect states and the low electron and hole mobilities of the a-Si:H layer.[7,8] Directly obtaining information by *C*–*V* measurements at various frequencies and temperatures is difficult, particularly under a depletion operating condition, because numerous factors simultaneously govern the frequency response of capacitance; these factors include the interface states, deep buck trap state, lateral current flow.[9] Accordingly, admittance spectroscopy is an exact method that uses an accurate equivalent circuit model to investigate the MIAS structure along with an alternative direct measurement method. Several works have entailed *C*–*V* measurements on MIAS, a-Si:H Schottky diode, and TFTs structures.[9–14] However, systematic studies involving capacitance–frequency (*C*–*F*) and conduction/frequency–frequency (*G*/*F*–*F*) measurements of an MIAS structure are few. In this study, temperature-dependent admittance spectroscopy was employed to investigate the interface states and properties of a-Si:H films. Careful and detailed *C*–*F* and *G*/*F*–*F* measurements of the MIAS configuration were performed.

*E-mail address: mthsieh.ep94g@nctu.edu.tw

2. Equivalent Circuit Model

An equivalent circuit model must initially be developed for admittance spectroscopy. Figure 1 shows enlarged cross sections of the MAIS structure. (Details of the fabrication process will be introduced later.) The areas of each layer in the MIAS structure are all the same, except for the bottom gate contact, to prevent lateral current flow from affecting the experimental measurements.[12] The schematic band diagram of the MIAS capacitor in Fig. 2(a) for a slightly doped n-type a-Si:H under an electron depletion condition elucidates the physics of the MIAS capacitor. In the MIAS capacitor, a highly resistive intrinsic a-Si:H is used. Therefore, a-Si:H bulk capacitance and resistance have to be considered in the equivalent circuit model. On the basis of the properties of a-Si:H and the operating conditions, three equivalent circuit models were developed and are shown in Figs. 2(b)–2(d) for accumulation, depletion, and full depletion, respectively. C_{SiN} represents the geometric capacitance of the insulator layer (SiN_x), and $C_{a\text{-}Si}$ and $R_{a\text{-}Si}$ are the geometric capacitance and resistance of a-Si:H, respectively. C_D and R_D represent the capacitance and resistance of depletion, respectively. C_S and R_S are the interface state capacitance and the specific emission time constant of charge trapped in the interface state, respectively. In Fig. 2(b), the model is described only by the series-connected C_{SiN} and $C_{a\text{-}Si}$ because a large number of carriers were injected from the electrode and accumulated at the interface. Therefore, the number of charges that are trapped in the interface state or buck trap state is neglected in comparison to the number of injected carriers under the accumulation operating condition. Hence, *C*–*F* measurements under accumulation operating conditions are expected to reveal only C_{SiN} in the low-frequency region and a series combination of C_{SiN} and $C_{a\text{-}Si}$ in the high-frequency region owing to the resistance–capacitance (*RC*) time constant of a-Si:H. Furthermore, the properties of a-Si:H in accumulation with various biases can be determined by admittance spectroscopy using an equivalent circuit model. Figure 2(c)

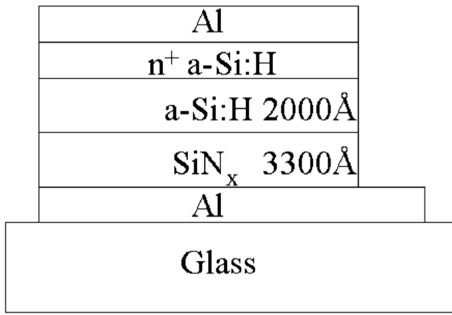


Fig. 1. Cross section of MIAS structure.

shows an equivalent circuit model under a depletion condition. In the model, $C_{\text{a-Si}}$ and C_D are introduced. $C_{\text{a-Si}}$ and C_D are determined from the width of the space charge region. Under the depletion condition, $R_{\text{a-Si}}$ should be linearly dependent on the difference between the total a-Si:H film thickness and the width of the space charge region. In the depletion condition, therefore, the equations for $C_{\text{a-Si}}$, $R_{\text{a-Si}}$, and C_D are

$$C_{\text{a-Si}} = \varepsilon_r\varepsilon_0 A/(D-W), \tag{1}$$

$$R_{\text{a-Si}} = \rho(D-W)/A, \tag{2}$$

$$C_D = \varepsilon_r\varepsilon_0 A/W, \tag{3}$$

where D is the total a-Si:H film thickness, W represents the width of the space charge region, ε_r and ε_0 represent the dielectric constant of a-Si:H and the permittivity of free space, respectively, ρ is the resistivity of the a-Si:H film, and A is the active area of the MIAS device. In the depletion condition, C_S should be considered in the equivalent circuit model because the number of interface trapped charges is comparable to the number of mobile charges in the a-Si:H film. However, the effect of deep-level trapped charges or generation–recombination charges can be ignored herein because its response frequency is approximately 0.1 Hz at room temperature, which significantly exceeds the limit of the equipment.[14] Hence, C_S is in parallel with C_D, and can be determined in the depletion condition by C–F measurements using the equivalent circuit model. In the MIAS structure for a TFT, the a-Si:H layer can be fully depleted in a strong reverse bias because the film is very thin. Accordingly, $C_{\text{a-Si}}$ is expected to be absent when the a-Si:H layer is fully depleted.[15] In Fig. 2(d), C_S is also neglected because there is no carrier that can be injected from the electrode.[14,15] R_D can be treated as an open circuit due to the very high resistance. Consequently, the ac parallel equivalent capacitance of each equivalent circuit model in Fig. 2 is given by the following:

(a) Accumulation

$$C(\omega) = \frac{C_{\text{a-Si}}C_{\text{SiN}}}{C_{\text{a-Si}}+C_{\text{SiN}}}\left[1+\frac{C_{\text{SiN}}/C_{\text{a-Si}}}{1+\omega^2R_{\text{a-Si}}^2(C_{\text{a-Si}}+C_{\text{SiN}})^2}\right]. \tag{4}$$

(b) Depletion

$$C(\omega) = \frac{C_{\text{a-Si}}C_1}{C_{\text{a-Si}}+C_1}\left[1+\frac{C_1/C_{\text{a-Si}}}{1+\omega^2R_{\text{a-Si}}^2(C_{\text{a-Si}}+C_1)^2}\right], \tag{5}$$

where

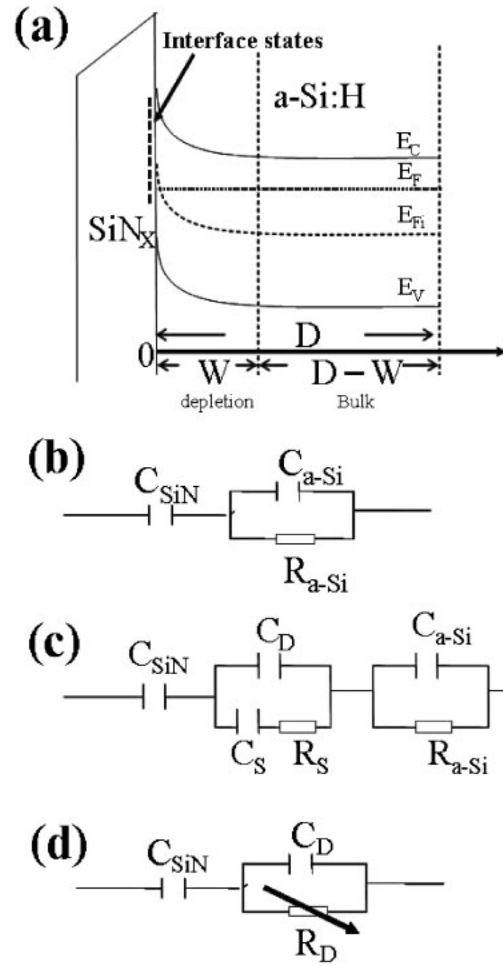


Fig. 2. Band diagram and equivalent circuit models of MIAS structure: (a) schematic band diagram of metal/SiN$_x$/a-Si:H capacitor under depletion operating condition. (b), (c), and (d) Equivalent circuit models for accumulation, depletion, and full depletion operating conditions, respectively.

$$C_1 = \frac{C_{\text{SiN}}C_P}{C_{\text{SiN}}+C_P}, \tag{6}$$

$$C_P = C_D + \frac{C_S}{1+\omega^2R_S^2C_S^2}, \tag{7}$$

$$C_S = qN_S. \tag{8}$$

(c) Full depletion

$$C = \frac{C_{\text{SiN}}C_D}{C_{\text{SiN}}+C_D}. \tag{9}$$

(Details of the theory of admittance spectroscopy can be found elsewhere.[16]) where q is the electronic charge and N_S is the density of interface states. The above equations indicate that capacitance depends strongly on frequency under the accumulation and depletion operating conditions, a fact that can be used to study the properties of a-Si:H and the density of interface states by admittance spectroscopy.

3. Experiments

In this study, two conventional inverted-staggered MIAS capacitors were fabricated and studied by admittance spectroscopy. The SiN$_x$ layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) with a mixture of H_2, NH_3, N_2, and SiH_4 gases at 1.2 Torr at a substrate temper-

Table I. Extracted parameters of a-Si:H TFTs for devices A and B under $V_{DS} = 5$ V.

	Swing (V/dec)	Mobility ($cm^2 V^{-1} s^{-1}$)	I_{ON}/I_{OFF}	I_{ON} (A) ($V_g = 20$ V)
Device A	0.8	0.81	4.81×10^5	3.30×10^{-6}
Device B	0.7	1.04	5.68×10^5	3.86×10^{-6}

ature of 380 °C and an RF power density of 1700 mW/cm^2. A SiN_x film, serving as the gate dielectric, was deposited at a flow rate ratio of 1200/240 of NH_3 to SiH_4 gases for devices A and B. The a-Si:H layer was deposited on top of the SiN_x film from a glow discharge of pure SiH_4 at 0.7 Torr at a substrate temperature of 270 °C and an RF power density of 70 mW/cm^2. The a-Si:H film was slightly of the n-type with different H_2 dilutions of SiH_4. The H_2/SiH_4 ratios of device A and B were 1250/250 and 2500/250, respectively. Another phosphorus-doped (n^+) a-Si:H layer was deposited on top of the a-Si:H layer to ensure an ohmic source or a drain contact. The thicknesses of the SiN_x, a-Si:H, and n^+ contact layers were 330, 200, and 50 nm respectively. The areas of the MIAS capacitors were both $500 \times 1000\,\mu m^2$. Aluminum was used as both gate and source/drain metals. Two a-Si:H TFTs devices with a W/L ratio of 15 μm/3 μm were also fabricated, in which all of the thin films were deposited under the same process conditions as those for devices A and B. The MIAS and TFTs were fabricated using standard photolithographic techniques. The electrical and stability characteristics of the completed TFTs were determined using an HP4145B semiconductor parameter analyzer. Table I shows the extracted parameters of both devices at $V_{DS} = 5$ V. Admittance spectroscopy was performed using an HP4194A gain phase analyzer at an oscillation level of 0.1 V to study the equivalent circuit model of the devices.

4. Results and Discussion

Figure 3 displays a frequency-dependent *C–V* spectrum of device A measured at room temperature (RT). When gate bias (V_g) is increased beyond −1 V, capacitance depends strongly on frequency, suggesting the presence of a geometric *RC* time constant that results from the presence of R_s and $R_{a\text{-}Si}$. However, the capacitance is almost constant below −1 V. Excellent agreement exists between the above equations and the frequency-dependent *C–V* spectrum of the MIAS device. Figures 4(a) and 4(b) show the *RT C–F* and *G/F–F* spectra, respectively, for different gate biases applied to the MIAS capacitor. In Fig. 4(a), the capacitance below −1 V is almost constant, whose value is comparable to that determined from the thicknesses of SiN_x and *W* according to a parallel-capacitor model. (Notably, in this region, *W* equals the thickness of a-Si:H.) As gate bias is increased beyond −1 V, the operating condition enters the depletion region and capacitance increases rapidly in the low-frequency region owing to a decrease in *W*. During the depletion (−1 to 2 V), the *C–F* spectra show two drops at inflexion frequencies of 10 and 200 kHz equal to the inverse *RC* time constant of the interface states and a-Si:H film, respectively. As gate bias is further increased beyond 2 V, the capacitance in the low-frequency region reaches a saturated value of 82.5 pF, which is comparable to C_{SiN}. In

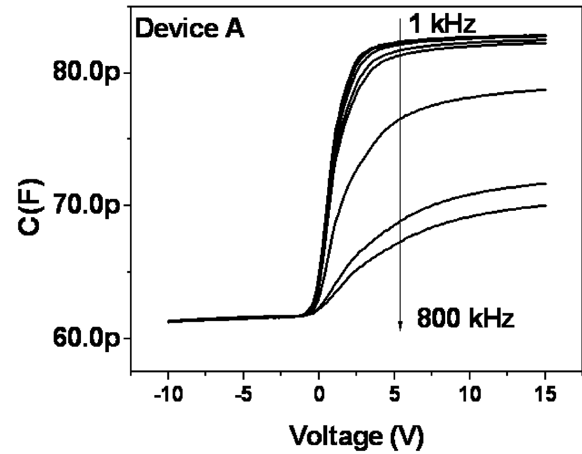


Fig. 3. A frequency-dependent *C–V* spectrum of device A of MIAS structure at room temperature.

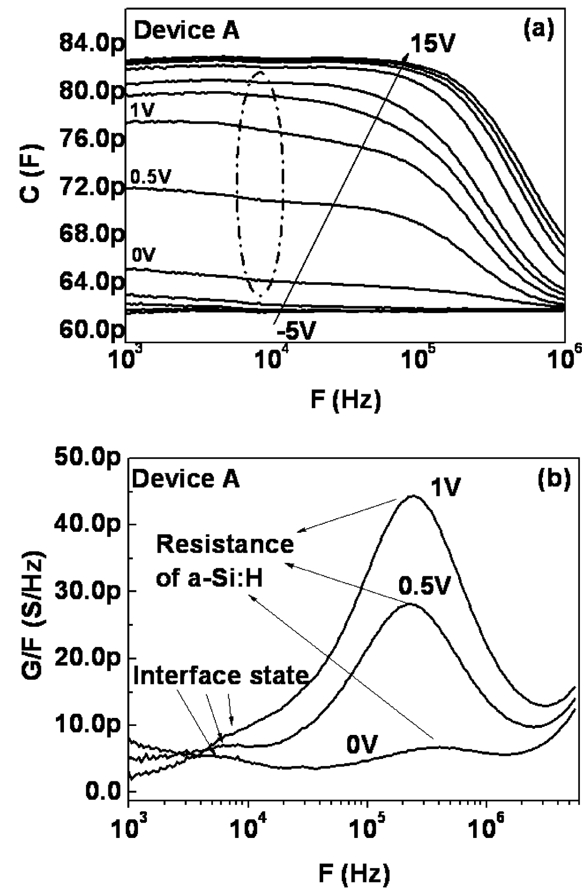


Fig. 4. Admittance spectra of MIAS structure for device A. (a) Bias-dependent *C–F* curves. (b) *G/F–F* curves measured in depletion region.

conductance measurement, the ac parallel equivalent conductance of each equivalent circuit model in Fig. 2 is given by

$$\frac{G(\omega)}{\omega} = \frac{\omega R_S C(\omega)^2}{1 + [C(\omega) R_S \omega]^2}, \qquad (10)$$

where $C(\omega)$ is determined using the eqs. (4), (5), and (9) depending on the various operation conditions. According to eq. (10), the peak in the *G/F–F* spectra is observed as the *C–F* spectra that are observed at the inflexion frequency.

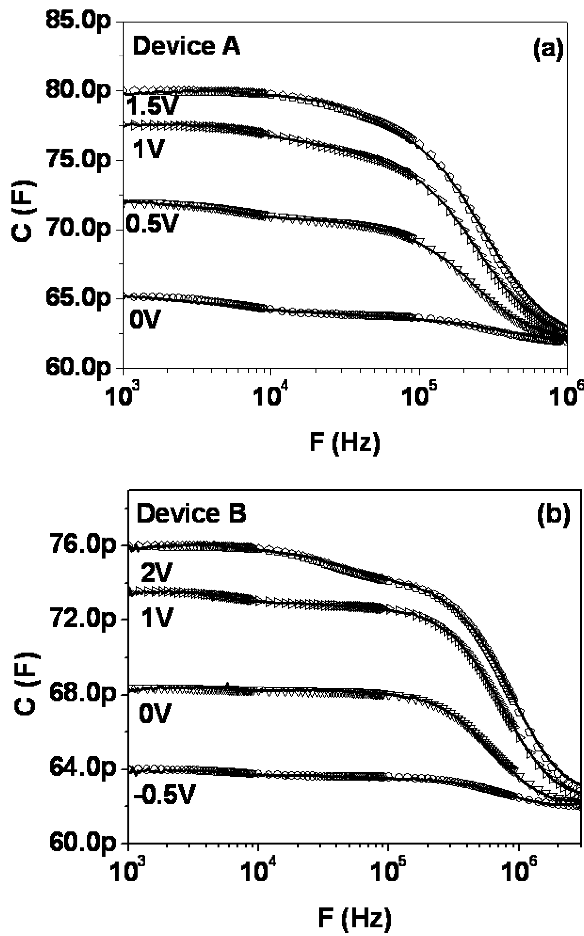


Fig. 5. Simulations (open squares) and experiments (solid curve) of C–F curves in depletion region: (a) device A and (b) device B.

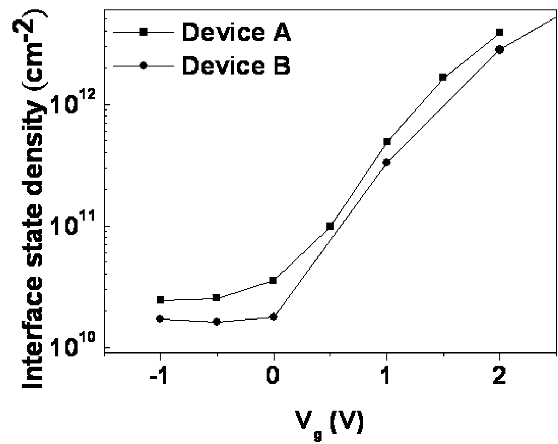
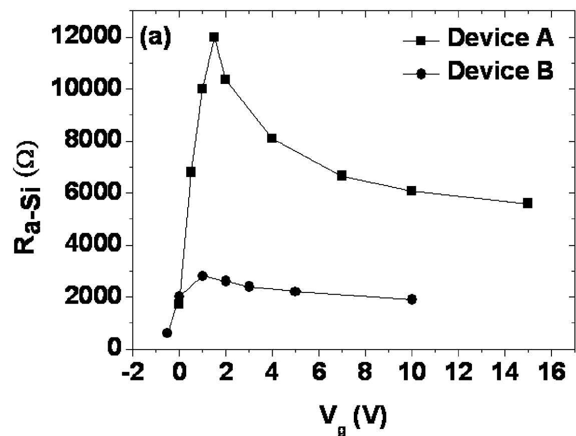


Fig. 6. Comparison of density of interface states at various gate biases between devices A and B.



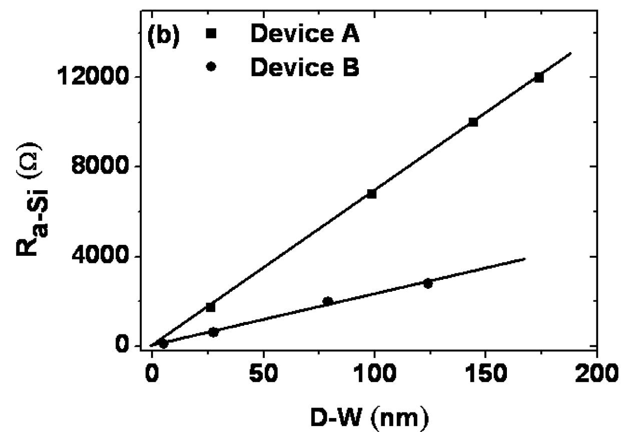


Fig. 7. (a) Comparison of resistance at various gate biases between devices A and B. (b) $R_{\text{a-Si}}$ as function of thickness of a-Si:H in depletion region for devices A and B. The resistances and depleted widths are derived from fitted data using the equations of ac parallel equivalent capacitance of each equivalent circuit model in Fig. 2.

Therefore, the inflexion frequency can also be observed from the peaks in the G/F–F spectra. In Fig. 4(b), the spectra show two peaks at around 10 and 200 kHz, which correspond to those in Fig. 4(a) and represent the interface state and resistance of a-Si:H, respectively. Furthermore, the inflexion frequency can be obtained more easily from the G/F–F spectra. Figures 5(a) and 5(b) show plots of the simulated ac parallel equivalent capacitance under the depletion operating condition obtained using the above equations, for devices A and B, respectively. Figures 5(a) and 5(b) show excellent agreement between the simulated (open squares) and experimental (solid curve) C–F spectra for devices A and B, respectively. The density of interface states and the resistance of a-Si:H at various V_g can be determined from the fitted data in Figs. 5(a) and 5(b), respectively. Figure 6 plot of interface state density as a function of V_g for devices A and B under the depletion condition. The densities of interface states for both devices obtained from Fig. 5 are comparable to those obtained by others using other methods.[9,17,18] Under the same gate bias, the density of interface states of device A always exceeds that of device B which explains the lower swing observed in device B. Figure 7(a) plot of $R_{\text{a-Si}}$ vs V_g for devices A and B. As V_g increases, $R_{\text{a-Si}}$ increases in the depletion region ($0-2$ V) because depletion width decreases. When V_g is increased beyond 2 V, $R_{\text{a-Si}}$ is decreased owing to the carrier injection from the electrode. Figure 7(b) shows a plot of $R_{\text{a-Si}}$ as a function of the thickness of the a-Si:H layer in the depletion region. From Fig. 7(b), $R_{\text{a-Si}}$ is proportional to the difference between D and W, indicating the correctness of the equivalent circuit model. Furthermore, the resistivity of a-Si:H can also be determined. The resistivities of devices A and B are 3.48×10^6 and 1.16×10^6 Ω cm, respectively.

The performance of a-Si:H TFT also strongly depends on the quality of the a-Si:H film. In previous works, the quality

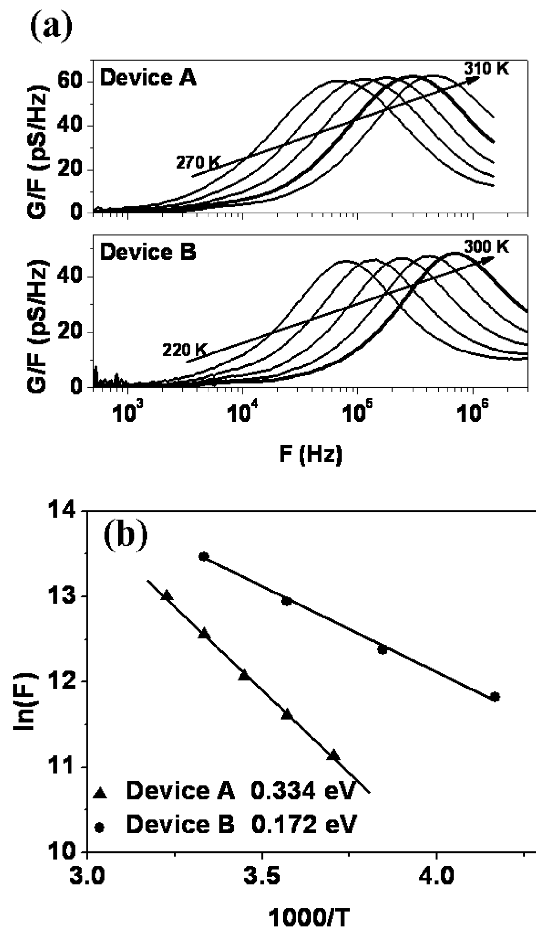


Fig. 8. (a) Temperature-dependent G/F–F spectra at $V_g = 10\,V$ for devices A and B. (b) Plots of $-\ln F$ vs $1000/T$. F is derived from the peak in G/F–F spectra in (a).

of a-Si:H can be determined by evaluating the activation energy of a-Si:H. From depletion to accumulation, the activation energy of a-Si:H decreases and gradually approaches a constant in the strong-accumulation region.[19) Figure 8(a) shows a plot of the temperature-dependent G/F–F spectra of devices A and B measured at $V_g = 10\,V$ (corresponding to strong electron accumulation). For both devices A and B, the curves show a significant temperature dependence. For comparison, the curve obtained at 300 K is plotted in boldface. The peak shifts toward a high frequency from device A to device B, indicating a decrease in the resistance of a-Si:H which indicates an improvement in the quality of a-Si:H film. Furthermore, the characteristic G/F–F peak, corresponding to temperature, increases as a function of the ac modulation frequency F for both devices A and B:[19)]

$$F = F^0 \exp(-E_a/KT), \tag{11}$$

where F^0 is the pre-exponential factor, E_a is the activation energy that represents the energy separation between the edge of the Fermi level and the a-Si:H conduction band near the SiN_x/a-Si:H interface. K is the Boltzmann's constant, and T is the temperature. Figure 8(b) shows a plot of $\ln F$ as a function of $1000/T$. As shown, increasing the H_2/SiH_4 gas flow rate ratio from 1250/250 to 2500/250 reduces the activation energy from 0.334 to 0.174 eV, the resistance and activation energy of a-Si:H in device B were better than those in device A. Accordingly, device B is expected to exhibit improved output characteristics. Table I shows that the I_{ON} current and mobility of device B are indeed better than those of device A. The better output characteristics of device B are explained as being associated with the lower resistance (or resistivity) and lower activation energy of the device.

5. Conclusions

In summary, a method of investigating an MIAS capacitor and monitoring the performance of an a-Si:H TFTs device using admittance spectroscopy was presented. On the basis of the properties of a-Si:H, three equivalent circuit models were developed and simplified for various operating conditions. Excellent agreement between the experimental data and the proposed equivalent circuit models was found. The simulation C–F measurement using equivalent circuit models easily yielded the interface density of states at room temperature. The resistance and activation energy of a-Si:H film was also determined to evaluate the quality of the a-Si:H film. Experimental data concerning the MIAS structure agreed excellently with the output characteristics of TFTs. Consequently, admittance spectroscopy based on the equivalent circuit models can be used as a powerful and efficient tool for the process monitoring of TFTs.

Acknowledgements

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