國立交通大學

電子工程學系電子研究所

博士論文

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# 用於管線式類比數位轉換器之數位背景校正技術

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## 摘要

隨著先進製程的進步， MOS 電晶體的通道長度越來越短，電晶體的寄生效應也因此隨之變小，這樣可以大大提升其操作速度以及節省功率消耗。但是因為通道長度的縮短，也使得電晶體的輸出阻抗降低；另外因為越來越薄的 oxide 厚度，為了元件的可靠度，工作電壓也隨之下降。因為輸出阻抗變小與工作電壓的降低，使得類比電路設計難以得到高增益以及大動態範圍的要求。這些因素都使得類比電路設計的難度越來越高，讓類比電路的效能面臨嚴峻的考驗。

電壓式的切換電容管線式類比數位轉換器目前被廣泛的使用，因為其在運作時將一個高增益的運算放大器操作在負迴授的狀態，使得其轉換特性可以達到高線性度以及高準確度的要求，但是因為的電容不匹配或者是有限增益的運算放大器會在類比數位轉換器的輸出造成非線性的失真。以目前 CMOS 的製程技術，電容的匹配可以讓類比數位轉換器達到 10-12Bit 左右的解析度；但是先進製程卻使得要設計一個高增益放大器的難度變得相當的高，既使達到增益的設計要求，但是卻往往會犧牲運算放大器的操作速度。所以如何利用一個高速低增益的運算放大

器，設計出一個高效能的類比數位轉換器，是本篇論文的重點。

本篇論文描述一個應用於管線式類比數位轉換器之強健背景校正技術。對於一個切換電容式的管線式類比數位轉換器，我們可以切割他的輸入取樣電容，並且將亂數序列利用切割的電容混入主要的訊號之中。輸入的亂數序列可以利用類比數位轉換器的輸出加以萃取出來，如此便可以不影響到類比數位轉換器的正常工作達到校正的目的。利用與數入相關的亂數產生序列，就可以使得類比數位轉換器的工作不需要額外的輸出擺幅。

我們實現了一個 65 奈米金氧半場效電晶體製程的 12-Bit 、 80 MHz 、 32mW 之管線式類比數位轉換器，它利用新的背景校正技術，將類比數位轉換器所造成的非線性加以校正，其中除了將增益以及次數位類比轉換器加以校正之外，更進一步將運算放大器之非線性增益所造成之非線性失真加以修正。我們所提出的技術是強健而且不會受到元件不匹配的影響，另外也不需額外的輸出擺幅。因為我們減輕類比電路所需要的準確度與線性度要求，所以可以利用比較簡單並且省電的方式來實現類比電路。我們實現的類比數位轉換器在輸入為 2 MHz 的弦波，並且工作在 80MS/s 時可以達到 67 dB 的 SNDR 與 81 dB 的 SFDR 。

另外我們還提出一個切割通道的類比數位轉換器架構來減少校正所需要的時間。這個切割通道類比數位轉換器，由兩個一樣的類比數位轉換器所組成，它們接收相同的輸入訊號，但是利用不同的亂數序列來進行校正。我們在校正資料萃取前將兩個類比數位轉換器的輸出加以比較並且將雜訊先加以消除，如此便可以大幅降低所需要的校正時間。在此篇論文之中我們將所提出的架構利用理論分析與系統模擬加以驗證。

# Digital Background Calibration of Pipelined ADCs

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## Abstract

Following the progress of advanced technology, the channel length of MOS transistor is smaller and the parasitic is also reduced. These characteristics make the transistor be able to be operated in higher frequency and lower power dissipation. However, the output impedance of MOS transistor reduces with the channel length. In addition to the output impedance, the thickness of gate oxide also becomes thinner than a long channel device. For device reliability issue, supply voltage scales down with channel length. The reduced output impedance and supply voltage make analog circuits can not be designed with high gain and large dynamic range. These features make the design of high performance analog circuits more difficult.

Voltage-mode switched-capacitor (SC) pipelined ADC is widely used. This circuit is operated with high gain operation amp (opamp) and configures in negative feedback. The negative feedback circuit can achieve high linearity and high accuracy at the same time.

However, with capacitor mismatch and finite opamp's dc gain, the output of a pipelined ADC may contain servere nonlinearity. The capacitor matching with present CMOS technology can be used to design a pipelined ADC with 10-12 bit resolution. But it's hard to design a high gain opamp with high unit-gain frequency in deep-submicron technology. The main purpose of this thesis is to design a high performance pipelined ADC in deep-submicron technology.

This thesis presents a background calibration scheme for pipelined analog-to-digital converters (ADCs) that is robust. For a SC pipeline stage, by splitting its input sampling capacitor, a random sequence can be injected into the ADC's signal path, and then calibration data can be extracted from the ADC's digital output without interrupting its normal conversion operation. Using an input-dependent scheme to generate the calibration random sequence, no additional signal range is required to accommodate the extra calibration signal.

A 32-mW 12-bit 80-MS/s pipelined ADC was fabricated using a 65 nm CMOS technology. The ADC demonstrates a new digital background technique, which corrects pipeline stage nonlinearity as well as gain and sub-DAC errors. The proposed technique is robust and immune to device mismatches, and does not need extra signal range. Since the accuracy and linearity requirements are mitigated, analog circuits with less complexity and power can be used. The ADC achieves 67 dB SNDR and 81 dB SFDR at 80 MS/s sampling rate with a 2 MHz sinewave input.

In addition, a split-channel ADC architecture is proposed to reduce the calibration time. The split-channel ADC consists of two A/D channels that receive the same analog input but employ different random sequences for calibration. The calibration time can be greatly reduced by comparing the digital outputs from both channels and then removing the embedded perturbations before extracting the calibration data. The proposed calibration techniques are analyzed by using both theoretical formulation and system-level simulation.

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JEN-LIN FAN

*National Chiao-Tung University*

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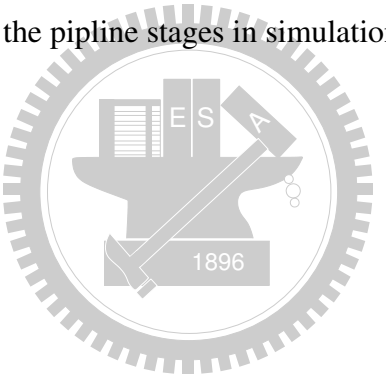

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# Chapter 1

# Introduction

## 1.1 Motivation

The role of analog-to-digital converter (ADC) is the interface between the analog signal and the digital signal processing system as shown in Figure 1.1. Various ADCs have been designed for the same purpose. Pipelined ADC is a popular structure in nowadays because of the compromise between high speed and high resolution. Other structures are hard to achieve high speed and high resolution requirements at the same time. Although several design configurations are used for pipelined ADC, switched-capacitor (SC) structure is particularly popular due to its capability of high-precision sampling and charge transfer. The resolution of the SC pipeline ADC is mainly limited by the matching of the capacitors and the finite gain of the operational amplifier. The nature matching of the capacitors in

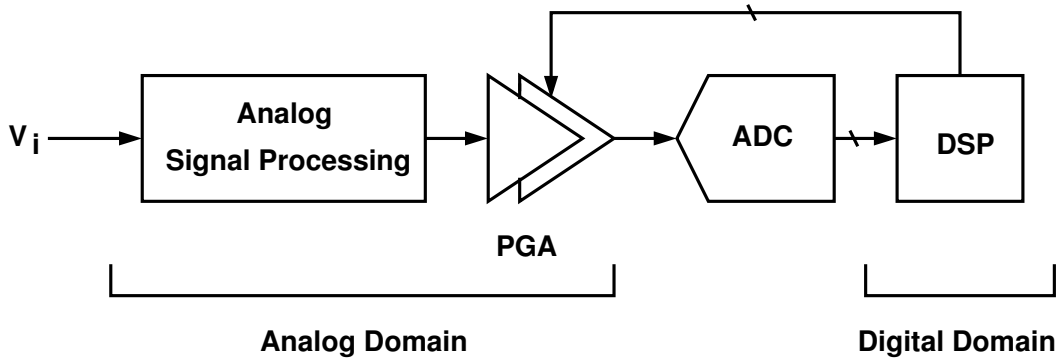


Figure 1.1: Block disgram of DSP-based system.

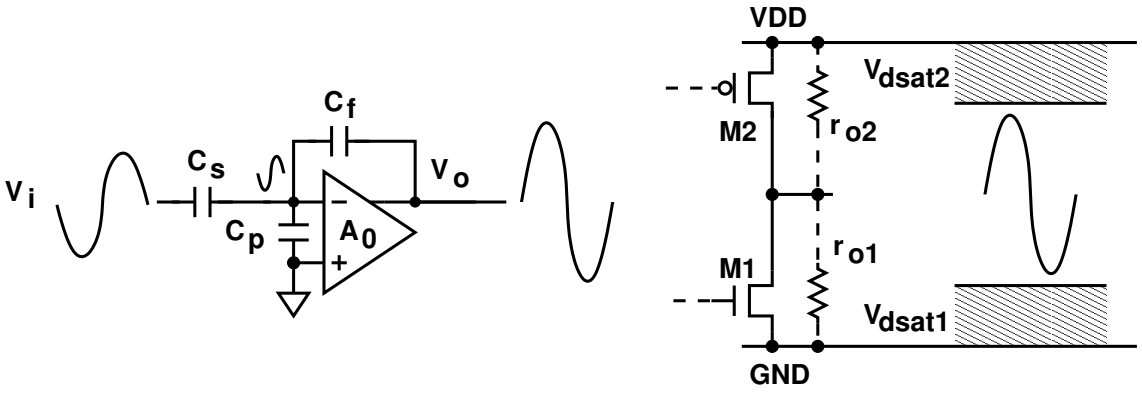


Figure 1.2: Impact of deep-submicron technology.

modern technology limited the resolution of pipelined ADC to 10-12bit. Moreover, it is more difficult to design a high gain operational amplifier for high resolution ADC because of the shrinks of the channel length and supply voltage.

In deep-submicron technology, the parasitic of MOS transistor is smaller than its long channel counterpart and reduced parasitic makes the device be able to be operated in higher frequency. This feature also means the circuit can be implemented with lower power dissipation and smaller area. However, short channel device has low output impedance and this limits the achievable gain of an amplifier. A closed-loop amplifier is shown in Figure 1.2 and its output is

$$\frac{V_o}{V_i} = \frac{C_s}{C_f} \times \frac{1}{1 + \frac{1}{A_0} \cdot \frac{C_s + C_f + C_p}{C_f}} \tag{1.1}$$

The accuracy of the amplifier output is affected by the gain of the opamp. Furthermore, low gain opamp means the signal swing at the opamp's input node is increased. This also increases nonlinear distortion of the amplifier [5]. Besides, the thickness of the gate oxide is also reduced and that means the supply voltage must be reduced for reliability issue. Reducing the supply voltage also reduces the dynamic range of the analog circuits, as shown in Figure 1.2. These properties make analog circuit design have more challenges especially for the circuits that need high gain amplifier and large dynamic range. In order to design a high performance analog circuit in such a suffering condition, these drawbacks must be overcome by other techniques. In this thesis, the analog circuit imperfection is remedied by digital calibration.

In a SC pipelined ADC, capacitor mismatch and finite opamp dc gain make the residue gain and sub-DAC output deviate from its nominal value. In order to overcome these natural limitations, various calibration techniques are proposed to enhance the ADC resolution. By using these techniques, the matching and gain requirements can be greatly loosened and the analog circuit can be implemented with less complexity. This means that the ADC can be fabricated with less power dissipation and smaller area. ADC calibration can be classified into analog calibration and digital calibration. Analog calibration means that the ADC imperfection is corrected in analog domain. However, this technique usually makes the analog circuitry more complex and usually needs larger area. This is undesirable because it may deteriorate the circuit performance. In contrast, digital calibration usually corrects the ADC imperfection in digital domain. This technique may need more complex digital signal process. However, this overhead is inapparent in advanced technology. For these reasons, digital calibration technique is more popular and is widely used at present.

In pipelined analog-to-digital converter (ADC) designs, digital calibration enables a trade-off between analog circuitry and digital circuitry. Various correlation-based digital background calibration schemes have been proposed [2, 5, 6, 7, 8, 9, 10]. They share the same basic principle which involves randomly varying the configuration of a pipeline stage, digitizing its analog output by using its back-end stages, and then extracting the slow-varying stage parameters in the digital domain by employing correlation. They differ in (1) how a pipeline stage is reconfigured; (2) what and how stage parameters are extracted; (3) how the overall A/D conversion is corrected. Criteria to evaluate a calibration scheme include:

1. Hardware overhead. What analog and digital circuits are added? Are circuit performances, such as speed and power, deteriorated by the circuit modification?

2. Signal range overhead. How much extra signal range does the calibration require? This is crucial for circuits already under low-voltage supplies.

3. Component matching requirement. Does the calibration scheme hint any matching requirement for circuit components? Is the calibration sensitive to offset or other effects due to mismatches?

4. Robustness. Can the background calibration be effective under any input condition? Is the calibration still functional if the input is a dc signal?

5. Calibration time. How long does it take for the calibration process to converge? Can the calibration track the variations of the stage parameters?

A generic pipeline stage comprises a sub-ADC, a sub-DAC, and a subtracting amplifier. Calibrating a pipeline stage is extracting the parameters related to the characteristics of its sub-DAC and amplifier. The extracted data are then used to correct the digital output so that the overall analog-to-digital (A/D) conversion becomes linear. To enable background calibration, a pipeline stage is randomly reconfigured by either switching the sub-ADC's thresholds [5, 6] or adding a digital test signal to the sub-DAC's input [2, 7, 8]. However, the above stage reconfiguration techniques increase the stage's output signal range. The original signal range can be restored by adding redundant sub-ADC thresholds and extra sub-DAC output levels [5, 10].

Some calibration schemes assume certain matching requirements. The [6] scheme requires a precise sub-ADC threshold shift. The [5, 7] schemes assume the sub-DAC has an uniform output step size. On the other hand, the [8, 9] schemes employ a separate calibration procedure to correct the sub-DAC error, thus eliminating the matching requirement. The [2] scheme calibrates both gain and sub-DAC at the same time; thus, no need to have any component matching.

Correlation-based calibration schemes usually require a large number of samples to extract accurate data, thus resulting in long calibration time. There are techniques to reduce the calibration time [6, 10, 11, 12].

To further improve A/D conversion linearity, there are schemes which also calibrate amplifier's nonlinearity [5, 7, 9]. However, the schemes of [5, 7] cannot function under certain input conditions, such as a dc input. The [9] scheme requires extra signal range, which in turn degrades stage linearity. Unlike simple gain/sub-DAC calibration, amplifier's offset can affect nonlinearity calibration. Nevertheless, it was neglected or was not corrected in the aforementioned schemes.

In this thesis, a 12-bit pipelined ADC was designed to demonstrate a new digital background calibration scheme that can calibrate stage gain, sub-DAC, and stage nonlinear-

ity simultaneously. To enable background calibration, multiple uncorrelated random sequences are injected into a split-capacitor pipeline stage. By employing input-dependent generation of the random sequences, no extra signal range is required. Calibration data are extracted by correlation-based integration-and-dump. Nonlinearity is detected by solving simple linear equations. The proposed calibration scheme needs no matching requirement and is flexible to include multiple harmonics calibration. The offset effect can be simply treated as even-order harmonics and be removed by calibration.

## 1.2 Organization

The organization of the thesis is described as follow:

Chapter 2 is the overview of pipelined ADC. Mathematics description and analysis are presented in this chapter. The design considerations of a pipelined ADC, including opamp dc gain, capacitor matching and thermal noise requirement etc., are introduced by mathematics analyses.

Chapter 3 describes the error sources of a pipelined ADC. The opamp's finite dc gain and capacitor mismatch make the residue gain and sub-DAC output deviate from their nominal values and also result in nonlinear conversion of a pipelined ADC. To correct these errors, a new split-capacitor digital background calibration configuration is proposed. With calibration, the analog circuit imperfection is corrected. An input-dependent random sequence generator is also proposed to remedy the defects of prior arts.

Chapter 4 analyzes the effect of the stage nonlinearity. In deep-submicron technology, high gain and high swing opamp is hard to obtain and the pipelined ADC may still have significant distortion even with gain and DAC calibration. To further enhance the resolution of the ADC, the pipeline stage nonlinearity must be corrected. Split-capacitor calibration technique is extended and used to correct the stage nonlinearity.

To verify the digital background calibration configuration described in Chapter 3 and Chapter 4, a 65nm 12-bit 80MS/s pipelined ADC was demonstrated in Chapter 5. A low gain and low power dissipation opamp is also proposed in this chapter.

Chapter 6 describes the convergence issue of a correlation-based calibration technique. The main source that limits the calibration data extraction time is mentioned in the chapter.

A new split-channel ADC configuration is proposed to remedy this drawback. With this technique, the calibration convergent speed is improved by more than 1000 times.

Finally, conclusions and recommendations for future works will be given in Chapter 7.

# Chapter 2

# Overview of Pipelined ADC

## 2.1 Introduction

Analog-to-digital converters (ADCs) are used to convert an analog signal into a corresponding digital output. Various different ADCs are designed to achieve the same purpose. Pipelined ADC is the most popular structure in nowadays because of the compromise between high speed and high resolution. Other structures are hard to achieve high speed and high resolution requirements at the same time. Although several design styles are used for pipelined ADC, switched-capacitor (SC) structure is particularly popular due to its capability of high- precision sampling and charge transfer. The resolution of the SC pipelined ADC is mainly limited by the matching of the capacitors and the finite gain of the operational amplifier (opamp). In this chapter, we will introduce the concept and the error sources of pipelined ADCs by mathematic analysis. The operation of a 2.5-bit pipeline stage is also described in this chapter. Moreover, the design considerations of a pipelined ADC are also analyzed.

## 2.2 Quantization Feedforward Architecture

Analog-to-digital converters (ADCs) are used to quantize an analog signal $V_i$ to a digital signal $D_o$ which is a linear representation of $V_i$. To achieve this goal, a signal approximation concept can be used to estimate the analog signal. As shown in Figure 2.1, the input

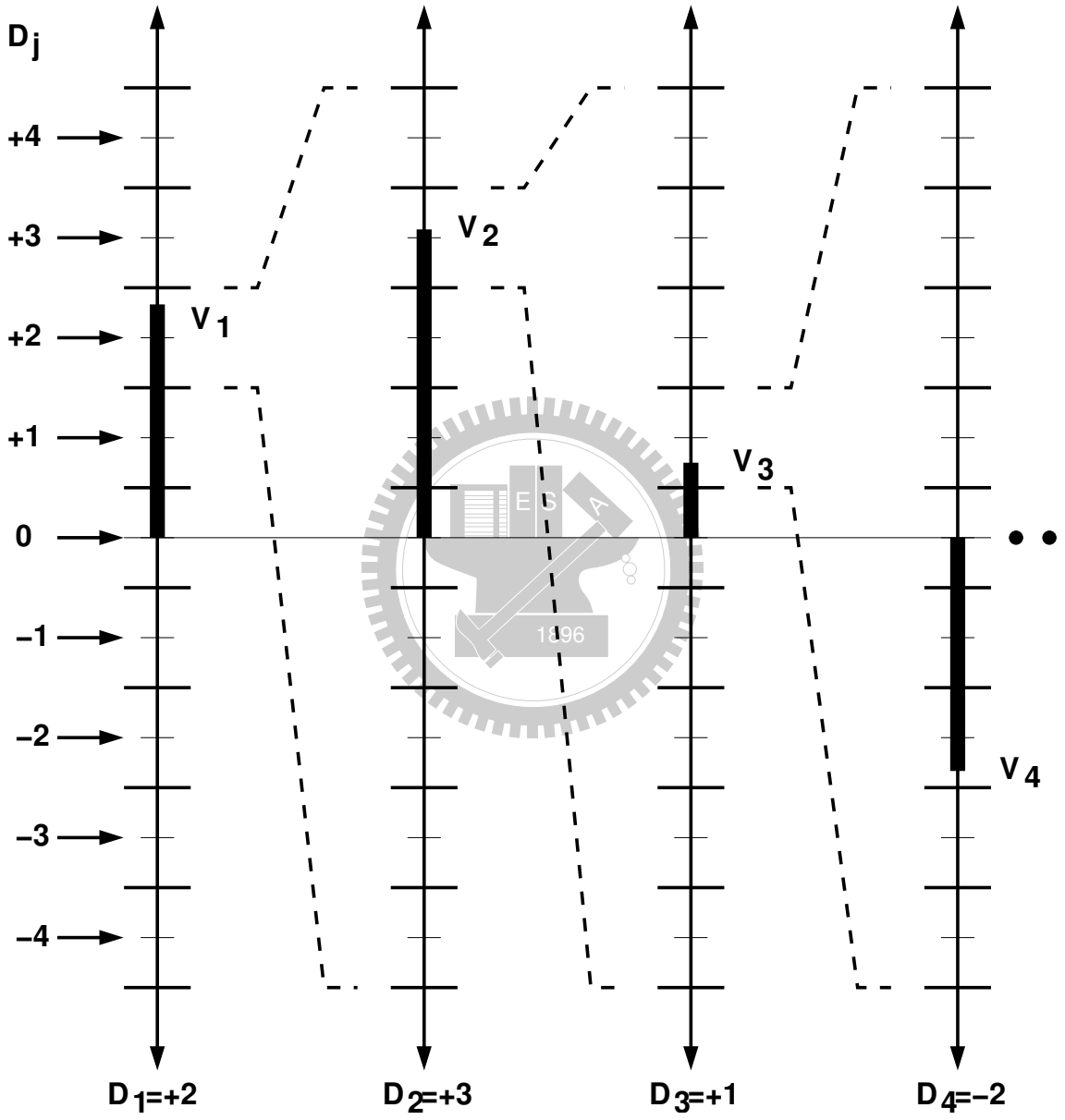


Figure 2.1: Analog signal approximation concept.

$V_1$ is first compared with a scaler and is coarsely quantized, the output $D_1$ is 2. $D_1$ is the rough estimation of the signal $V_1$. The coarsely quantized output $D_1$ is then subtracted from $V_1$. The resulting residue value is multiplied with $G_1 = 9$ and amplified to the full scale. In the next step, $V_2$ is quantized again with the same scaler and $D_2 = 3$. Then $D_2$ is subtracted from $V_2$ and the residue is amplified again to the full scale. These processes repeat in each comparison. With the residue gain, the input signal can be quantized more accurately with the same scaler, as shown in Figure 2.1. If $G_j = 1$ for each comparison, we will need a more accurate scaler for the later conversion. By combining the output $D_j$ for each conversion, we can estimate and linear represent the input $V_i$. As illustrated in this figure, the input $V_1$ can be expressed as:

$$V_1 = 2 + \frac{3}{9} + \frac{1}{9^2} + \frac{-2}{9^3} + \cdots + \frac{V_{P+1}}{9^P} \tag{2.1}$$

where $P$ is the total conversion number. The denominator in Equation (2.1) is because the residue of each conversion is amplified by the gain factor and is referred back to the input.

A pipelined ADC is used to realize this signal approximation processing. The general form of a pipelined ADC is shown in Figure 2.2, which consists of $P$ identical pipeline stage. Each pipeline stage includes both an analog processor (AP) and an encoder. A AP comprises sample and hold amplifier (SH), sub-ADC, sub-DAC and residue amplifier. For the $j$-th AP, its analog input $V_j$ is quantized by an internal sub-ADC and generates a digital output $D_j$. Its digital output $D_j$ drives an internal sub-DAC to generate a corresponding analog signal $V_j^{\mathrm{da}}$. The digital signal $D_j$ is a rough estimate of $V_j$ in digital domain. $V_j^{\mathrm{da}}$ is the analog expression of $D_j$ and is an rough estimate of $V_j$ in analog domain. The $j$-th stage's analog output $V_{j+1}$ can be expressed as:

$$V_{j+1} = G_j \times \left(V_j - V_j^{\mathrm{da}}\right) \tag{2.2}$$

The output $V_{j+1}$ is the residue voltage that is obtained by amplifying the quantization error by the gain factor $G_j$, the $V_j$-$V_{j+1}$ transfer function is shown in Figure 2.3. The detail operation and the analog signal flow of the pipeline stage is shown in Figure 2.4.

To obtain a linear representation of the input signal, Equation (2.2) can be re-written

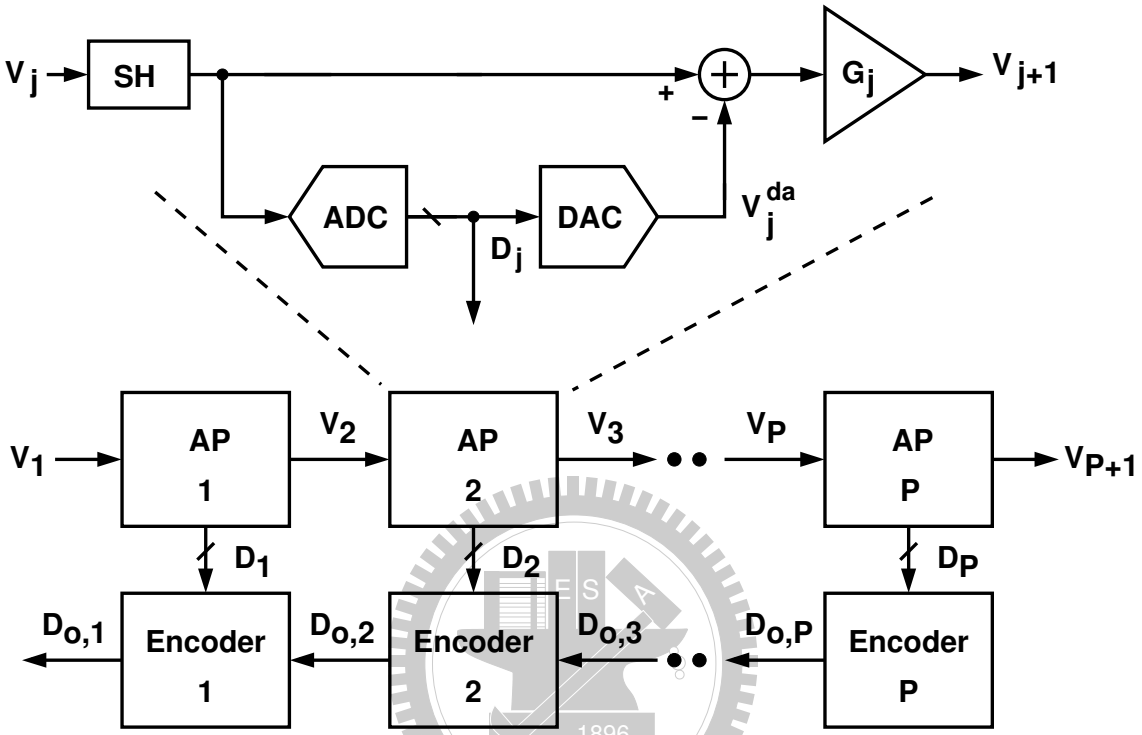


Figure 2.2: Pipelined ADC block diagram.

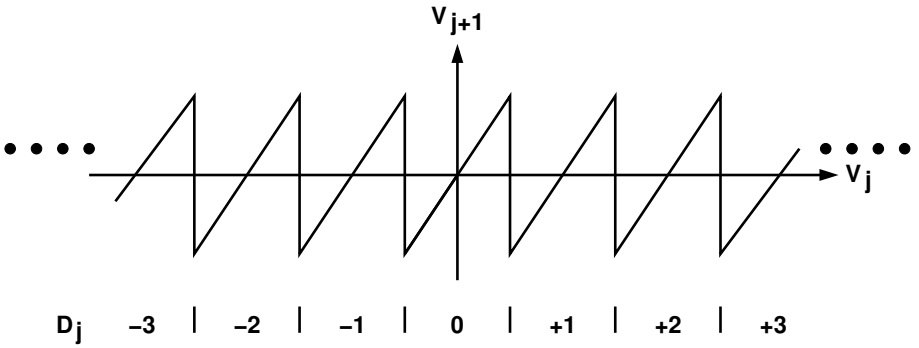


Figure 2.3: Transfer characteristic of a pipelined ADC.

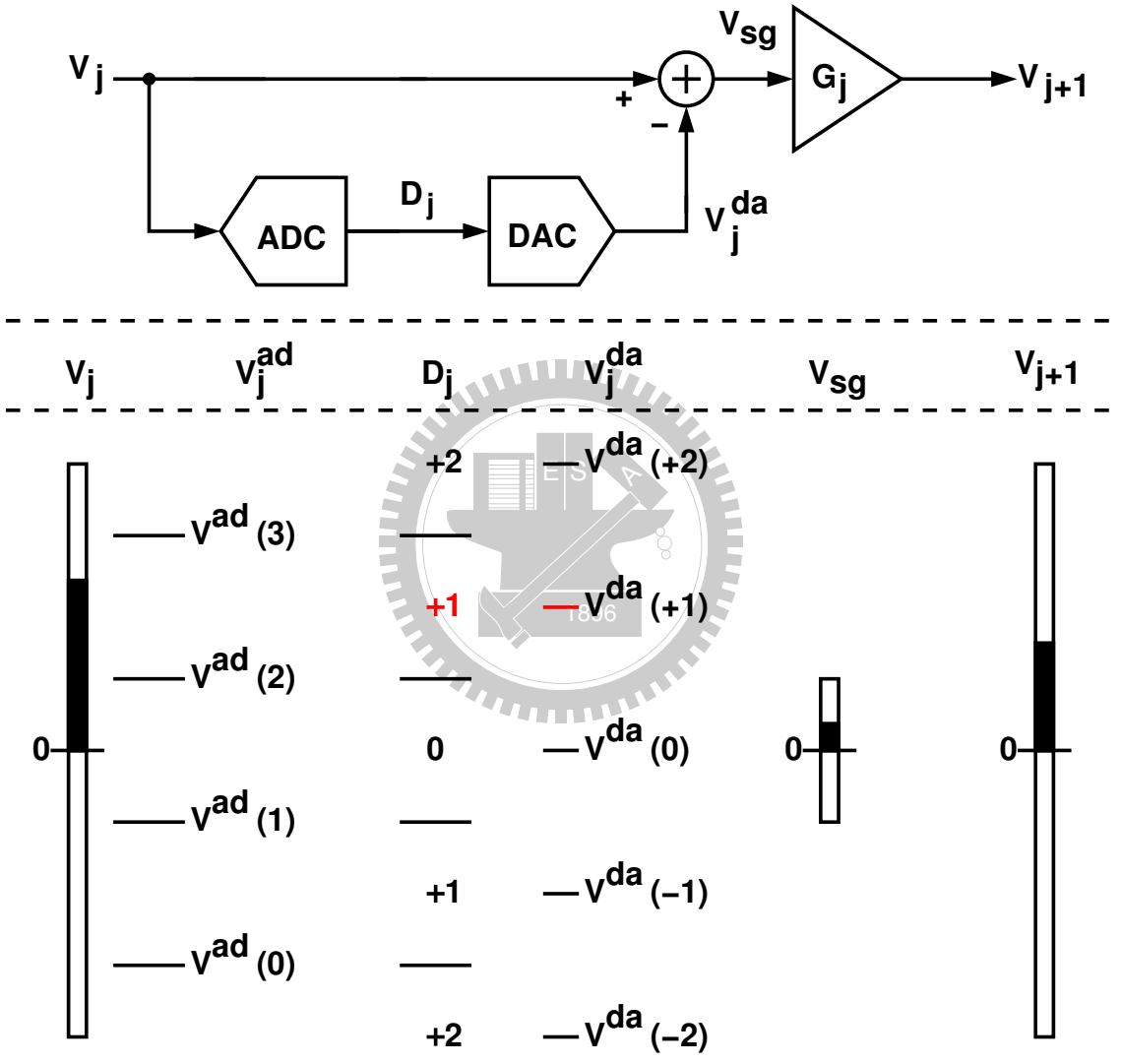


Figure 2.4: Signal flow of an analog processor.

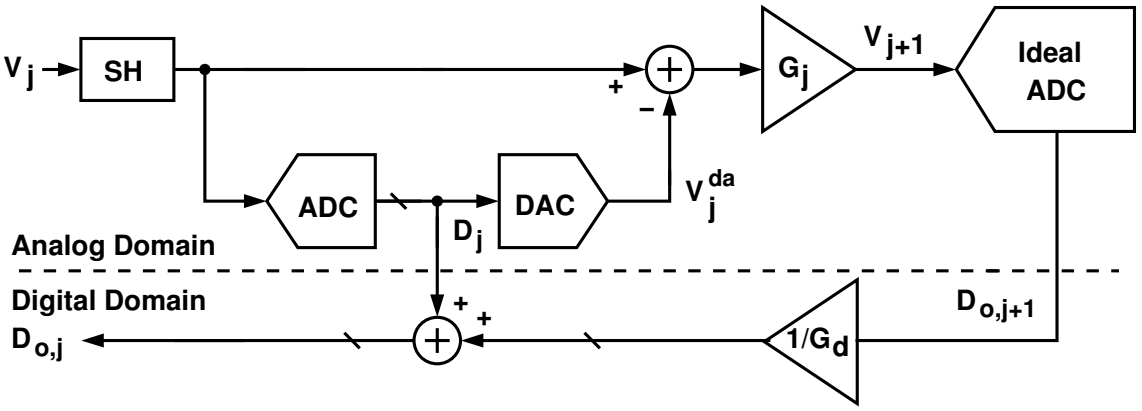


Figure 2.5: Input-referred signal reconstruction in digital domain.

as:

$$V_j = \frac{1}{G_j} \times V_{j+1} + V_j^{\mathrm{da}} \tag{2.3}$$

The signal processing of Equation (2.3) is usually implemented in digital domain and can also be depicted in Figure 2.5. $V_j^{\mathrm{da}}$ in Equation (2.3) is replaced with $D_j$ in this figure and $G_j$ is replaced with $G_d$, because they represent the same signal in different signal domain. The ideal ADC in Figure 2.5 linearly transfers its input signal to a corresponding digital output, that means $D_{o,j+1} = V_{j+1}$. According to Equation (2.3), the input analog signal $V_1$ in Figure 2.2 can be approximated as a digital output $D_{o,1}$ and can be expressed as:

$$D_{o,1} = V_1^{\mathrm{da}} + \frac{V_2^{\mathrm{da}}}{G_1} + \frac{V_3^{\mathrm{da}}}{G_1G_2} + \frac{V_4^{\mathrm{da}}}{G_1G_2G_3} + \cdots + \frac{V_P^{\mathrm{da}}}{G_1G_2\cdots G_{P-1}} + \frac{V_{P+1}}{G_1G_2\cdots G_P} \tag{2.4}$$

$$= D_1 + \frac{D_2}{G_1} + \frac{D_3}{G_1G_2} + \frac{D_4}{G_1G_2G_3} + \cdots + \frac{D_P}{G_1G_2G_3\cdots G_{P-1}} + Q_n \tag{2.5}$$

$$= W_1 + W_2 + W_3 + W_4 + \cdots + W_P + Q_n \tag{2.6}$$

where $Q_n$ is the quantization error and its value is

$$Q_n = \frac{V_{P+1}}{G_1G_2\cdots G_P} \tag{2.7}$$

and

$$W_j = \frac{D_j}{G_1G_2\cdots G_{j-1}} \tag{2.8}$$

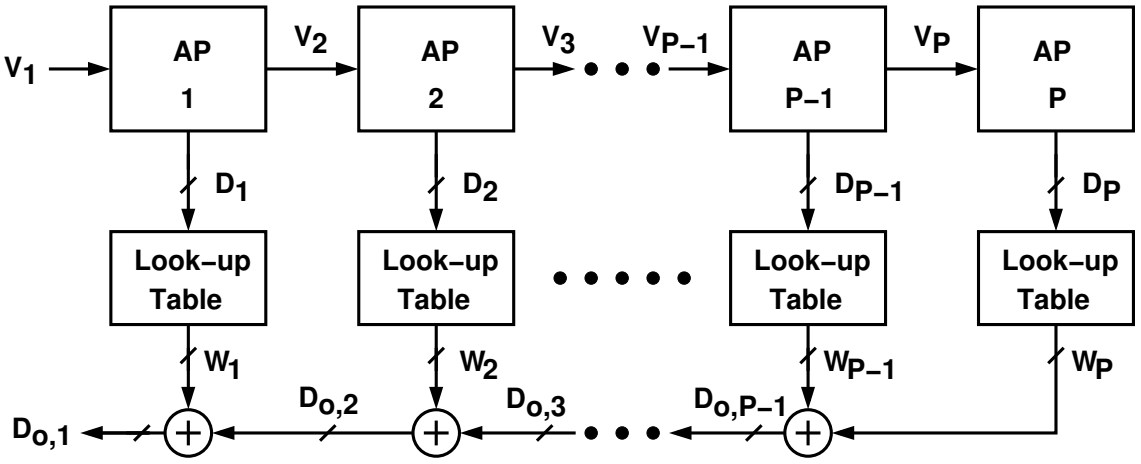


Figure 2.6: Encoding of the pipelind ADC.

The result is consistent with the result mentioned in Equation (2.1). The input signal can be correctly estimated by combing the $W_j$ of each stage. Consequently, as long as the $D_j$ and $G_j$ are known for each conversion, the input signal can be approximated.

Based on Equation (2.6), the complete block diagram of the pipelined ADC is shown in Figure 2.6, where $D_{o,1}$ is simplified as $D_o$ and $Q_n$ is ignored. An ideal ADC is used to convert the input signal to a corresponding output and the output should be a linear representation of the input. Pipelined ADC can achieve this goal by simply repeating the same signal processing in analog domain and combining the output in digital domain.

Now we consider the effect of quantization error. The quantization error $Q_n$ of a ADC and its probability-density function (PDF) is shown in Figure 2.7 [13], $\Delta$ is the least-significant bit (LSB) of the ADC and its value is

$$\Delta = \frac{V_{FS}}{2^N} \tag{2.9}$$

where $V_{FS}$ is the full-scale input range of the ADC and $N$ is the resolution of the ADC. Assuming that the quantization error uniform distributes between $+\Delta/2$ and $-\Delta/2$ and

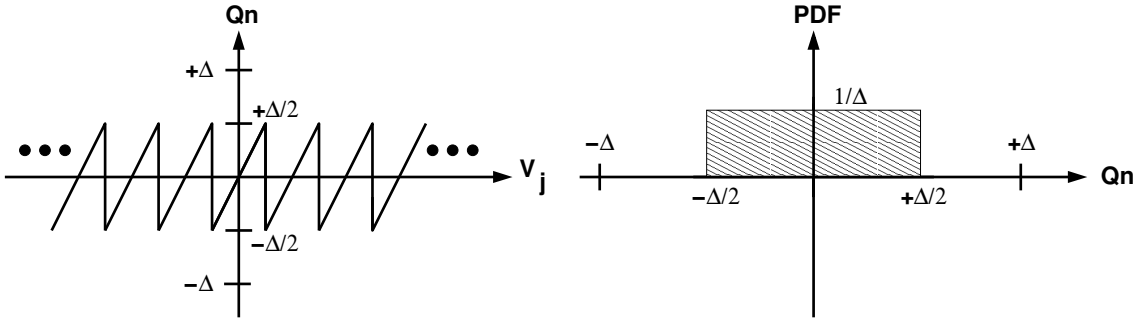


Figure 2.7: Quantization error and its probability-density function.

its PDF is $1/\Delta$. The quantization noise power, $P_{Qn}$, is

$$P_{Qn} = \int_{-\Delta/2}^{+\Delta/2} (Q_n)^2 \times pdf(Q_n)\, d(Q_n) \tag{2.10}$$

$$= \int_{-\Delta/2}^{+\Delta/2} (Q_n)^2 \times \frac{1}{\Delta}\, d(Q_n) \tag{2.11}$$

$$= \frac{\Delta^2}{12} \tag{2.12}$$

For an ideal ADC which contains only the quantization noise, the SNR is

$$SNR = \frac{P_{in}}{P_{Qn}} = \frac{V_{FS}^2/8}{\Delta^2/12} = \frac{2^{2N} \cdot 3}{2} \tag{2.13}$$

$$= 6.02 \cdot N + 1.76\ (dB) \tag{2.14}$$

where $P_{in}$ is the input signal power. We assume the input signal is sine-wave and its amplitude is $V_{FS}/2$. This value is the natural limitation for a ADC design.

## 2.3 A 2.5-bit Pipeline Stage

Multi-bit switched-capacitor (SC) pipelined ADC is widely used in recent years because it can achieve the same resolution with fewer opamps. Multi-bit pipeline stage usually suffers from the low feedback factor and that usually means low operating frequency. However, this drawback can be mitigated by using deep-submicron technology which has higher unit-gain frequency. This architecture also loosens the opamp's dc gain requirement. Consequently, multi-bit pipeline stage becomes a popular choice in nowadays.

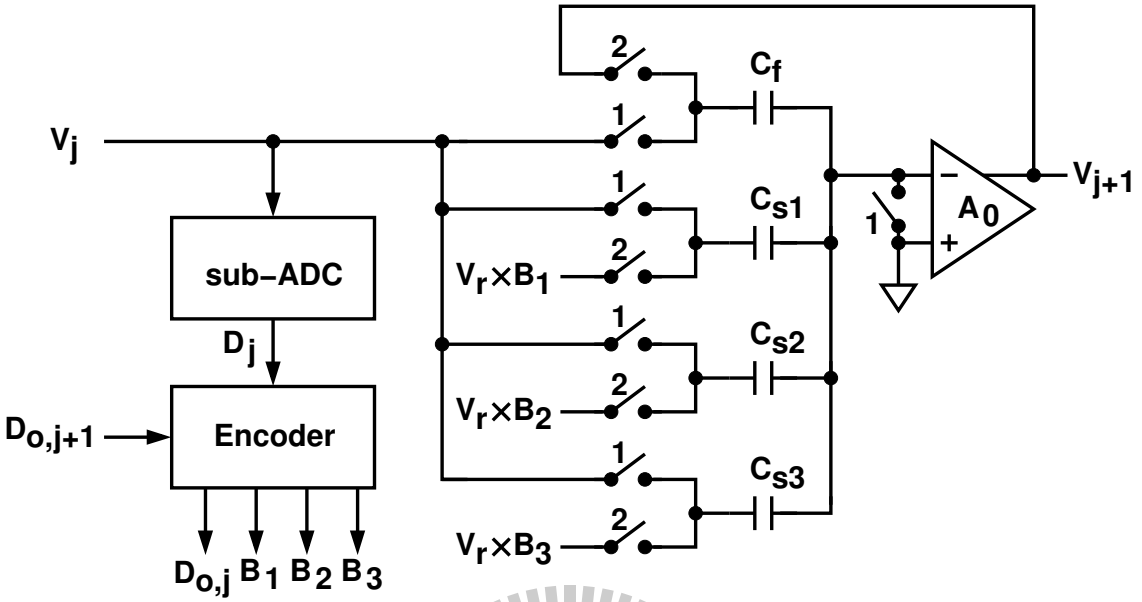


Figure 2.8: Schematic of a tranditional 2.5-bit switched-capacitor pipeline stage.

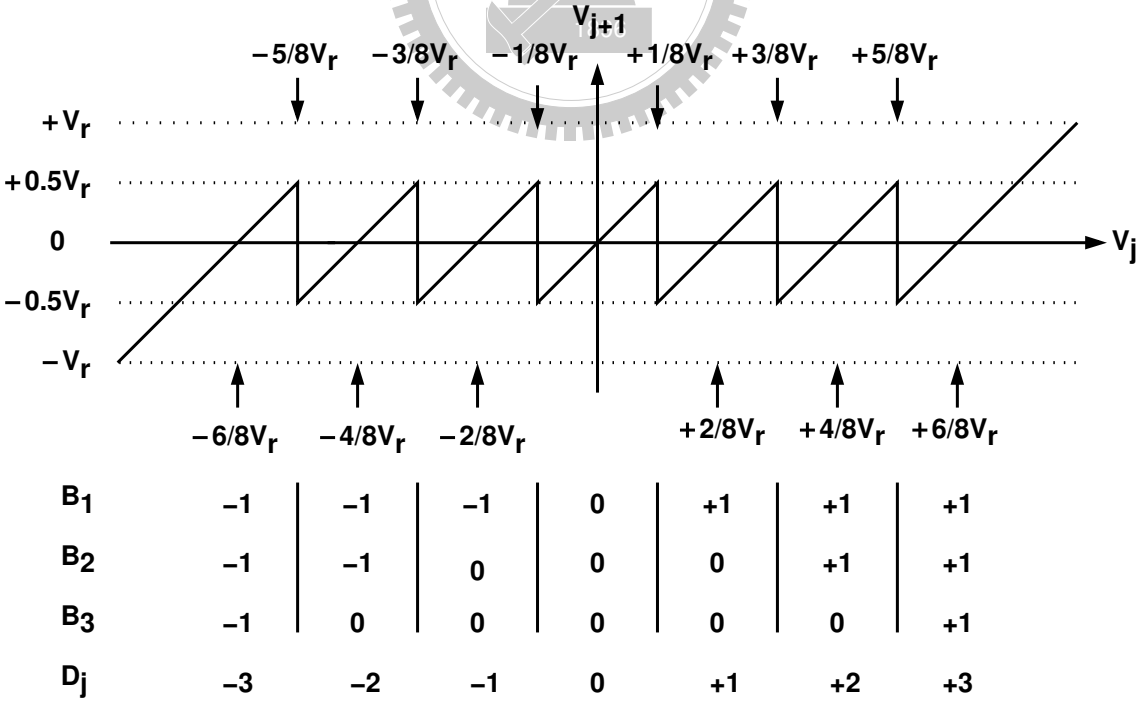


Figure 2.9: Transfer function of Figure 2.8.

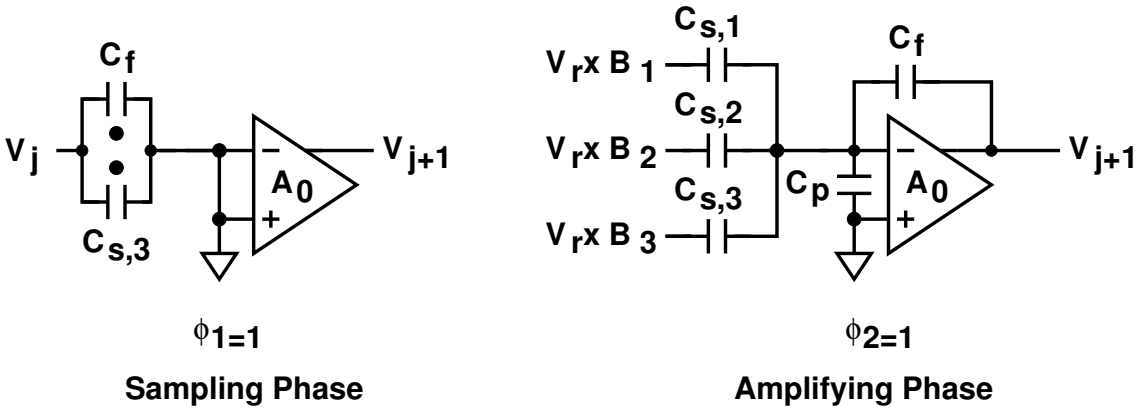


Figure 2.10: The configurtion of the SC circuit in sampling phase and amplifying phase.

In this thesis, instead a 1.5-bit pipeline stage, a 2.5-bit pipeline stage is introduced and implemented. Figure 2.8 is a 2.5-bit SC pipeline stage and the corresponding conversion characteristic of the pipeline stage is shown in Figure 2.9. The SC pipeline stage can provide the gain of four and also have the sample-and-hold function. The switches in Figure 2.8 are controlled by two non-overlapping clocks, $\phi_1$ and $\phi_2$. During $\phi_1 = 1$, also called sampling phase, the voltage $V_j$ is sampled on capacitors $C_f$, $C_{s,1}$, $C_{s,2}$, and $C_{s,3}$. During $\phi_2 = 1$, also called amplifying phase, $C_f$ becomes a feedback capacitor, and each $C_{s,i}$, where $i = 1, 2, 3$, is connected to a $V_r \times B_i$ reference. The value of $B_i$ is among $\{-1, 0, +1\}$. The $C_{s,i}$ capacitors form the sub-DAC, whose output is controlled by the signals $B_i$. The pipeline stage in sampling phase and amplifying phase are shown in Figure 2.10.

The sub-ADC comprises 6 comparators with thresholds at $\pm V_r/8$, $\pm 3V_r/8$ and $\pm 5V_r/8$ respectively. Its digital output $D_j$ is an estimate of the input $V_j$. The relationship between $D_j$ and $V_j$ is shown in Figure 2.9. The value of $D_j$ is among $\{0, \pm 1, \pm 2, \pm 3\}$. Assume the opamp in Figure 2.8 is linear and has a finite dc gain of $A_0$. Then, its output during $\phi_2 = 1$ can be written as:

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}} - V_j^{\mathrm{os}}\right] \tag{2.15}$$

where

$$\hat{G}_j = \frac{C_s + C_f}{C_f} \times \frac{1}{1 + \frac{1}{A_0} \cdot \frac{C_s + C_f + C_p}{C_f}} \tag{2.16}$$

$$\hat{V}_j^{\text{da}} = V_r \sum_{i=1}^{3} \frac{C_{s,i} \times B_i}{C_s + C_f} \tag{2.17}$$

$$C_s = C_{s,1} + C_{s,2} + C_{s,3} \tag{2.18}$$

Comparing Equation (2.15) with Equation (2.2), $\hat{G}_j$ and $\hat{V}_j^{\text{da}}$ represent the actual value which contain the capacitor mismatch and opamp's finite dc gain. In Equation (2.16), $A_0$ is the opamp's dc voltage gain and $C_p$ is the capacitance associated with the opamp's negative input node. The $V_j^{\text{os}}$ term represents the offset of the $j$-th stage, which summarizes the offset effect due to the input-referred offset voltage of the opamp, the charge injection from the analog switches, and the offset of the sub-DAC. If $C_f = C_{s,1} = C_{s,2} = C_{s,3}$ and opamp's dc gain is infinite, the nominal value of $\hat{G}_j = 4$ and $\hat{V}_j^{\text{da}} = 0, \pm 2V_r/8, \pm 4V_r/8$ and $\pm 6V_r/8$ respectively. The SC circuit in Figure 2.8 can perform the sample-and-hold (SH), sub-DAC and multiplication function, and is also called multiply-DAC (MDAC).

## 2.4 Opamp Gain and Capacitor Matching

Equation (2.16) and Equation (2.17) show that $\hat{G}_j$ and $\hat{V}_j^{\text{da}}$ are affected by opamp's dc gain and capacitor mismatching. To achieve desired ADC resolution, large enough dc gain is required to reduce the error in $G_j$. In addition to opamp's dc gain, capacitor matching in the SC circuit must be good enough to reduce the error in $\hat{G}_j$ and $\hat{V}_j^{\text{da}}$. In this section, we will determine gain and matching requirements of pipelined ADCs.

According to Equation (2.16), gain error of a $M$ bit pipeline stage in Figure 2.11 can be written as:

$$\text{Gain error} = \frac{\Delta V_{j+1}}{V_{j+1}} = \frac{1}{A_0} \times \frac{C_s + C_f + C_p}{C_f} \tag{2.19}$$

where $C_f = C$ and $C_S = (2^{M-1} - 1) \cdot C$. The output $V_{j+1}$ of the pipeline stage is sampled by the backend ADC. Usually we want

$$\frac{1}{A_0} \times \frac{C_s + C_f + C_p}{C_f} \leq \frac{1}{2^{Z+1}} \tag{2.20}$$

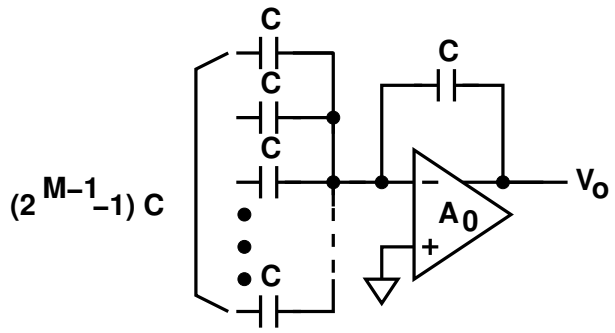


Figure 2.11: MDAC with M bit/stage in amplifying phase.

where $Z$ is the resolution of the backend ADC. If the resolution of the entire pipelined ADC is $N$ and $N = M + Z - 1$. Then Equation (2.20) can be re-written as:

$$A_0 \geq 2^{Z+1} \times \left(2^{M-1} + \frac{C_p}{C}\right) \tag{2.21}$$

$$= 2^{N+1} \times \left(1 + \frac{C_p}{2^{M-1} \cdot C}\right) \tag{2.22}$$

Equation (2.22) shows that for high resolution application, large dc gain is required to make the error neglected. In deep-submicron technology, large dc gain is obtained by cascading several gain stages. However, this topology usually needs frequency compensation that will decrease the unit-gain frequency of the opamp. Equation (2.22) also reveals that increasing bit/stage loosens the gain requirement, because the second term in Equation (2.22) is insignificant for large $M$.

As mentioned in previous section, for a $M$ bit pipeline stage, $2^{M-1}$ capacitors are used to sample and amplify the signal. Assuming that each capacitor has $\Delta C/C$ mismatch, generally the capacitor matching requirement can be expressed as:

$$\frac{\Delta C}{C} \leq \frac{1}{2^{Z+1}} \times \frac{1}{\sqrt{2^{M-1}}} \tag{2.23}$$

Increasing bit/stage will relax the matching requirement of the capacitor. For current CMOS technology, 0.1% capacitor matching can be obtained easily and achieve more than 10-bit resolution. For high resolution application, we can use large capacitor to improve the matching requirement. However, this approach increases the power dissipation of the amplifier. Generally calibration can be applied to relax the requirement and enhance the resolution.

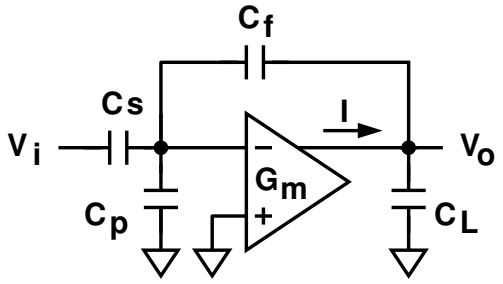


Figure 2.12: An Opamp in closed loop configuration.

## 2.5 Opamp Speed Requirement

For the SC circuit mentioned above, the opamp is configured as a closed loop amplifier in amplifying phase. Figure 2.12 is an opamp in closed loop configuration. The input-output transfer function of the closed loop amplifier can be calculated as:

$$\frac{V_o}{V_i} = \frac{-C_s}{C_f} \times \frac{1 - s \cdot \frac{C_f}{G_m}}{1 + s\tau} \tag{2.24}$$

$G_m$ is the transconductance of the opamp. The 3-dB bandwidth is

$$\omega_{3dB} = \frac{1}{\tau} = f \times \frac{G_m}{C_{load}} = f \times \omega_u \tag{2.25}$$

where

$$f = \frac{C_f}{C_s + C_f + C_p} \tag{2.26}$$

$$C_{load} = C_L + \frac{C_f \cdot (C_s + C_p)}{C_s + C_f + C_p} \tag{2.27}$$

The 3-dB bandwidth of the closed loop amplifier is determined by the opamp's unit-gain bandwidth $\omega_u$ and the feedback factor $f$.

Assuming the amplifier is a single pole system. The step response of a single-pole system is

$$V_o(t) = V_{step} \cdot \left(1 - e^{\frac{-t}{\tau}}\right) \tag{2.28}$$

To achieve N-bit ADC, we usually want

$$\frac{\Delta V_o}{V_o} = e^{\frac{-t_{settle}}{\tau}} \leq \frac{1}{2^{Z+1}} \tag{2.29}$$

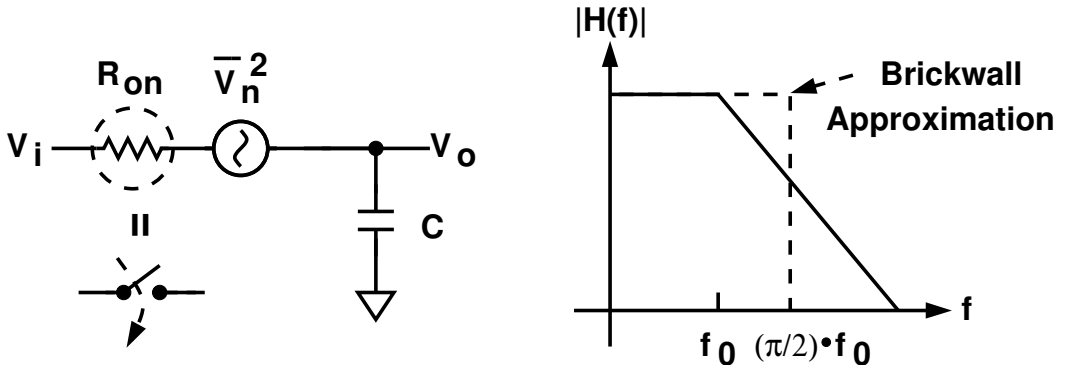


Figure 2.13: RC sampling network and its low-pass characterestics.

where $t_{settle}$ is the required settling time. Assuming that the clock period of the SC circuit is $T$ and $t_{settle}$ is half of the clock period. Equation (2.29) can be simplified as:

$$\frac{T}{2} \geq ln2 \cdot (Z+1) \cdot \tau \tag{2.30}$$

Equation (2.30) can be used to roughly estimate the required time constant. In general, $t_{settle}$ is usually smaller than $T/2$ due to the output slewing and the nonoverlapping period for different clock phases. In general, increasing bit/stage in a pipelined ADC design will reduce the $f$ and higher $\omega_u$ is required for the same operating speed.

## 2.6 Thermal Noise

Noise is an important concern in high resolution ADC design. To achieve desired signal-to-noise ration (SNR), the noise should be as low as possible. The main noise source of the SC pipeline stage is thermal noise. Thermal noise comes from the turn-on resistance of the switches and the opamp. In this section, we will analyze and calculate the output noise of a pipeline stage.

### 2.6.1 Sampling Thermal Noise

At first, we consider the noise generated during the sample duration. For a SC pipeline stage, the input is sampled by switches and capacitors. The thermal noise comes from the turn-on resistance of the switch and occurs at the sampling period, this can be realized in

Figure 2.13. The thermal noise of the turn-on resistance $R_{on}$ is

$$\bar{V}_n^2 = 4KTR_{on} \tag{2.31}$$

The $V_i$-to-$V_o$ transfer function $H(s)$ of the $R_{on}$ and C sampling network is a low-pass function and can be expressed as:

$$H(s) = \frac{V_o}{V_i} = \frac{1}{1 + sR_{on}C} \tag{2.32}$$

its frequency response is shown in Figure 2.13 and is calculated as:

$$|H(f)|^2 = \frac{1}{1 + (\frac{f}{f_0})^2} \tag{2.33}$$

where

$$f_0 = \frac{1}{2\pi R_{on}C} \tag{2.34}$$

The noise bandwidth of the single-pole low-pass system can be approximated to $f_0\pi/2$. Hence, the noise sampled by the capacitor is

$$\bar{V}_{thn}^2 = 4KTR_{on} \times \frac{\pi}{2} f_0 = \frac{kT}{C} \tag{2.35}$$

The sampled thermal noise is inverse proportion to the sampling capacitor and independent of the turn-on resistance of the switch. Larger $C$ may reduce the sampling noise but also reduce the operating bandwidth. A compromise should be made between the noise and the bandwidth requirement.

Consider the sampling thermal noise of a $M$ bit pipeline stage and there are $2^{M-1}$ identical capacitors used to sample and amplify the input signal, as shown in Figure 2.14. In sampling phase, $V_i$ is sampled by the $2^{M-1}$ capacitors and according to Equation (2.35), the noise in each capacitor is $kT/C$. In amplifying phase, the noise in each capacitor transfers to the feedback capacitor. The total noise $\bar{V}_{o1}^2$ at the output can be expressed as:

$$\bar{V}_{o1}^2 = \frac{kT}{C} \times 2^{M-1} \tag{2.36}$$

The total noise at the output depends on capacitor value and bit/stage.

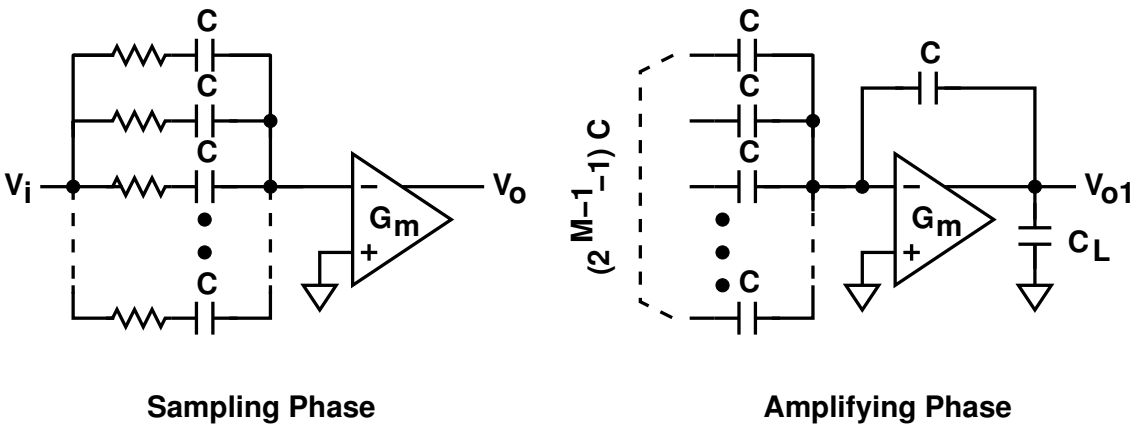


Figure 2.14: Sampling thermal noise of a M bit SC pipeline stage.

### 2.6.2 Thermal Noise of Opamp

For a MOS transistor operating in saturation and strong inversion region, the channel thermal noise can be modeled by a current source connected between the drain and source terminals. The noise current power spectral density (PSD) can be expressed as:

$$\bar{I}_n^2 = 4kT\gamma g_m \tag{2.37}$$

where $g_m$ is the transcondutance of the transistor and $\gamma$ is the noise factor which is about $2/3$ for a long channel transistor. To represent the thermal noise of an opamp, a simple CMOS fully differential opamp is shown in Figure 2.15. The input-referred noise of the opamp is

$$\bar{V}_{n,op}^2 = \bar{V}_{n,on}^2 = 4kT\frac{\gamma}{g_{m1}} \times n_f \tag{2.38}$$

where $n_f = 1 + g_{m3}/g_{m1}$ is the input-referred factor of the input differential pair and the active load.

The simple model used to calculate the output-referred noise of the pipeline stage is shown in Figure 2.15. The noise transfer function can be expressed as

$$\frac{V_{o2}}{V_{n,op}} = \left(1 + \frac{C_s}{C_f}\right) \times \frac{1}{1 + s\tau} \tag{2.39}$$

where $\tau$ is the same as Equation (2.25) and $C_f = C$, $C_S = (2^{M-1} - 1)C$. Assuming the opamp is a single pole system and the total output noise $\bar{V}_{o2}^2$ which is due to the opamp

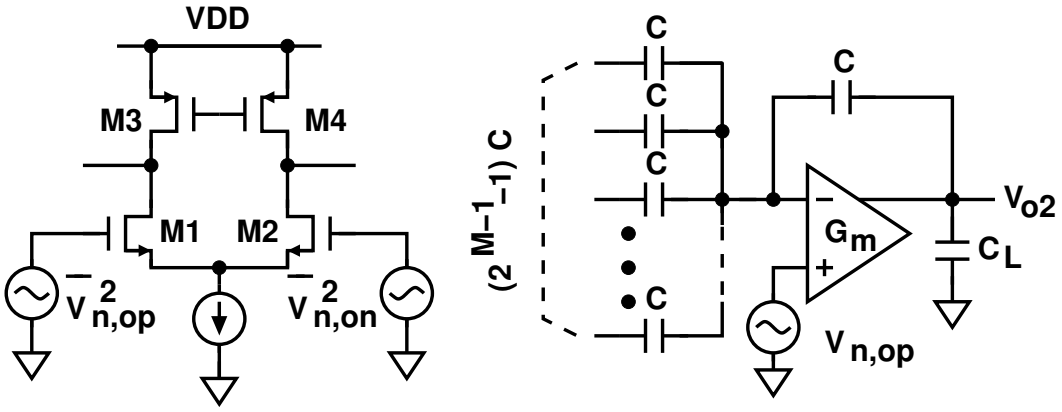


Figure 2.15: Opamp input-referred noise and the model used to calculate the opamp thermal noise of the pipeline stage in amplifying phase.

thermal noise is

$$\bar{V}_{o2}^2 = \bar{V}_{n,op}^2 \times \frac{1}{4\tau} \times \left(1 + \frac{C_s}{C_f}\right)^2 \tag{2.40}$$

$$= \frac{kT}{C_{load}} \times n_f \times \gamma \times 2^{M-1} \tag{2.41}$$

Where the transcondutance $G_m$ of the opamp is equal to $g_{m1}$. $C_{load}$ is the same as Equation (2.27). Similar to the sampling thermal noise as it is, the noise at the output of the pipeline stage is independent of the transconductance of the opamp. The opamp induced noise at the output of the pipeline stage is inverse proportional to the total capacitance loading at the output node.

### 2.6.3 Thermal Noise of $R_s$

In the next step, we consider the thermal noise comes from the turn-on resistance $R_s$. The switches are used to connect to the reference voltage in amplifying phase. First, we calculate the noise effect of one of the switches. The simple model is shown in Figure 2.16. The noise transfer function of this circuit can be approximated to

$$\frac{V_{o3}}{V_{n,s}} \approx \frac{1 - s \cdot \frac{C_f}{G_m}}{1 + s\tau} \tag{2.42}$$

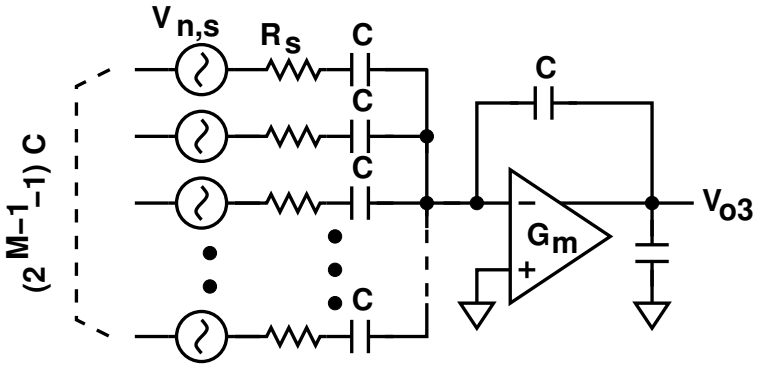


Figure 2.16: Simple model used to represent the noise of the turn-on resistance $R_s$.

In amplifying phase, there are $(2^{M-1}-1)$ different noise sources and all of them are uncorrelated to each other. According to superposition theory, the total output noise $\bar{V}_{o3}^2$ is

$$\bar{V}_{o3}^2 = \bar{V}_{n,s}^2 \times \frac{1}{4\tau} \times \left(2^{M-1}-1\right) \tag{2.43}$$

$$= \frac{kT}{C_{load}} \times \left(2^{M-1}-1\right) \times g_{m1} R_s \tag{2.44}$$

where the turn-on thermal noise $\bar{V}_{n,s}^2$ is $4kTR_s$. Similar to the opamp induced noise as it is, the noise contributed by $R_s$ is also inverse proportional to the total capacitance loading at the output node. Besides, the noise is also proportional to $g_{m1}R_s$.

### 2.6.4 Thermal Noise of $R_f$

Finally we consider the thermal noise coming from the turn-on resistance $R_f$. In amplifying phase, the feedback capacitor connects between the input and output of the opamp. The turn-on resistance $R_f$ also contributes noise to the output. The simplified model is shown in Figure 2.17 and the transfer function of $V_{n,f}$ can be approximated to

$$\frac{V_{o4}}{V_{n,f}} \approx \frac{1 + s \cdot \dfrac{C_s}{G_m}}{1 + s\tau} \tag{2.45}$$

The output noise $\bar{V}_{o4}^2$ introduced by $R_f$ is

$$\bar{V}_{o4}^2 = \bar{V}_{n,s}^2 \times \frac{1}{4\tau} \tag{2.46}$$

$$= \frac{kT}{C_{load}} \times g_{m1} R_f \tag{2.47}$$

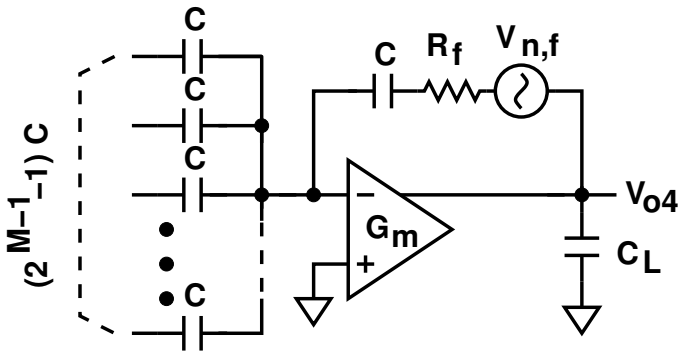


Figure 2.17: Simple model used to represent the noise of the turn-on resistance $R_f$.

where the turn-on thermal noise $\bar{V}_{n,f}^2$ is $4kTR_f$. Similar to Equation (2.44), the noise is inverse proportional to the total loading capacitors at the output node and is proportional to $g_{m1}R_f$.

### 2.6.5 Total Noise of Pipelined ADC

The output noise coming from individual noise source has been calculated. By combining Equation (2.36), Equation (2.41), Equation (2.44) and Equation (2.47), we can estimate the total output noise $\bar{V}_{n,out}^2$ of the M-bit pipeline stage is

$$\bar{V}_{n,out}^2 = \bar{V}_{o1}^2 + \bar{V}_{o2}^2 + \bar{V}_{o3}^2 + \bar{V}_{o4}^2 \tag{2.48}$$

$$= \frac{kT}{C} \times 2^{M-1} + \frac{kT}{C_{load}} \times 2^{M-1} \times \left(\gamma n_f + g_m R_s\right) \tag{2.49}$$

where we assume $R_s = R_f$ for simplification. To further simplify Equation (2.48) and to calculate the input-referred noise of the pipeline stage, we assume $C_{load} = 2C$, $\gamma = 2/3$, $n_f = 2$ and neglect the parasitic capacitor $C_p$. Next, assuming that the time constant $\tau_{RC}$ of the $R_s$ and $C$ is $\tau/8$. That means

$$R_s C = \frac{1}{8} \times \frac{C_{load}}{f \times g_{m1}} \Rightarrow g_{m1} R_s = 2^{M-3} \tag{2.50}$$

According to Equation (2.49) and Equation (2.50), the input referred-noise of the pipeline stage is

$$\bar{V}_{n,in}^2 = \frac{kT}{C_t} \times \left(\frac{5}{3} + 2^{M-4}\right) \tag{2.51}$$

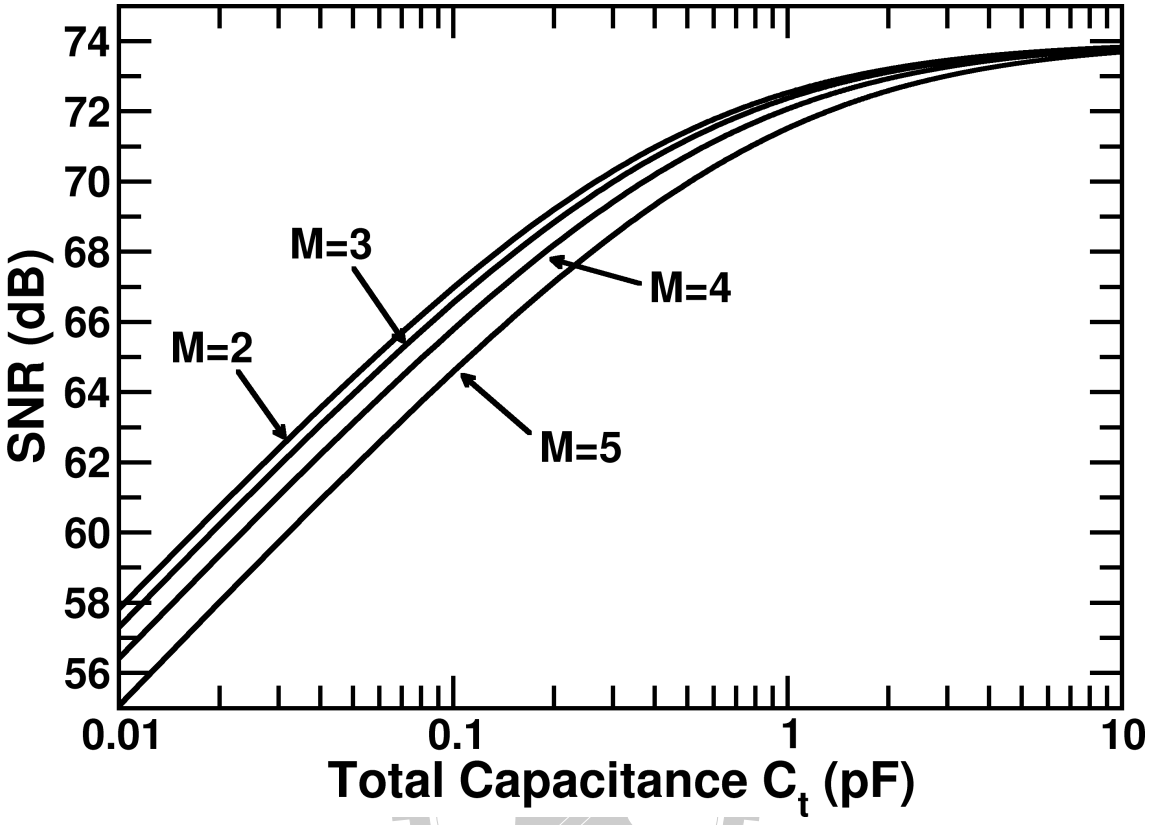


Figure 2.18: A 12-bit ADC SNR versus total capacitance $C_t$ for different stage resolution.

where $C_t = 2^{M-1}C$ is the total capacitance of the pipeline stage. The first term in Equation (2.51) is introduced by opamp and sampling switch. The second term is introduced by switches in amplifying phase. If $C_t$ is keep constant for different $M$, increasing bit/stage will increase the value of second term. This is because when bit/stage increases, the feedback factor reduces and larger $g_{m1}$ is required for the same operating speed. Furthermore, increasing bit/stage means the unit capacitance $C$ decreases and the turn-on resistance increases for the same time constant $\tau_{RC}$.

In reality, both quantization noise and thermal noise present in the pipelined ADC. Equation (2.12) and Equation (2.51) are used to represent the total noise in a pipelined ADC, the SNR of the ADC is

$$SNR = \frac{(\frac{V_{FS}}{2\sqrt{2}})^2}{\alpha \times \frac{kT}{C_t} \times \left(\frac{5}{3} + 2^{M-4}\right) + \frac{\Delta^2}{12}} \tag{2.52}$$

$\alpha$ is a scaling factor which is used to estimate the capacitor scale down effect and is usually larger than 1. Figure 2.18 is the SNR of a 12-bit ADC versus capacitor size for different stage resolution. Where $V_{FS}$ is 2 and $\alpha$ is 1 in this figure. For small capacitor size, the SNR is dominated by the thermal noise and increasing capacitor size will improve the SNR performance. For large capacitor size, the SNR is dominated by the quantization noise and further increasing the capacitor size has negligible effect.

Another important issue is about the front-end sample and hold amplifier (SHA). In a conventional pipelined ADC design, a front-end SHA is usually adopted to ease the design requirement of the first pipeline stage. However, SHA do not provide signal amplification but induce additional noise source. Besides, to meet the resolution and speed requirements, SHA usually needs large capacitor and consumes large power. For these reasons, SHA is usually omitted to save area and power dissipation of the ADC in nowadays. The omission of SHA needs careful design of the first pipeline stage and its sub-ADC.

## 2.7 Summary

In this chapter, the operation principle and the mathematical analysis of the pipelined ADC are introduced. Pipelined ADC is usually implemented in voltage mode SC circuit. The design considerations of a SC pipeline ADC are noise, amplifier gain and amplifier operation speed. With the mathematic analysis, we can get a general idea of designing a pipelined ADC. However, in real implementation, the circuits may suffer from some process variation such as capacitor mismatch or dc gain drift, etc.. These imperfections result in the nonlinear conversion of the pipelined ADC. In the following chapters, we will explain the nonlinearity induced by imperfection and see how to remedy these errors.

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# Chapter 3

# Gain/DAC Calibration

## 3.1 Introduction

Pipelined analog-to-digital converters (ADCs) consist of comparators and switched capacitor (SC) multiplying digital-to-analog converter (MDAC). Individual MDAC is linearized by employing high-gain capacitive feedback. However, it is mainly the accuracy of conversion gain of each MDAC along the pipeline stage that determines the overall resolution of an ADC. For a SC MDAC, the uncertainty of its conversion gain is caused by capacitor mismatch and finite gain of the opamp. For high-resolution applications, several background calibration techniques have been developed to constantly monitor MDACs's conversion gains against variations in temperature and supply voltage without interrupting normal analog-to-digital (A/D) conversion operation [5, 14, 15, 16, 17, 18]. In this chapter, the nonlinearity induced by capacitor mismatch and finite opamp dc gain will be analyzed. we will detail background calibration principle and propose a new configuration for background calibration.

## 3.2 Gain and DAC Errors

As shown in Equation (2.15)-Equation (2.17), the transfer characteristic of a 2.5-bit pipeline stage is affected by capacitor mismatch and opamp's finite gain. Due to component mismatches and variations in fabrication process, supply voltage, and tempera-

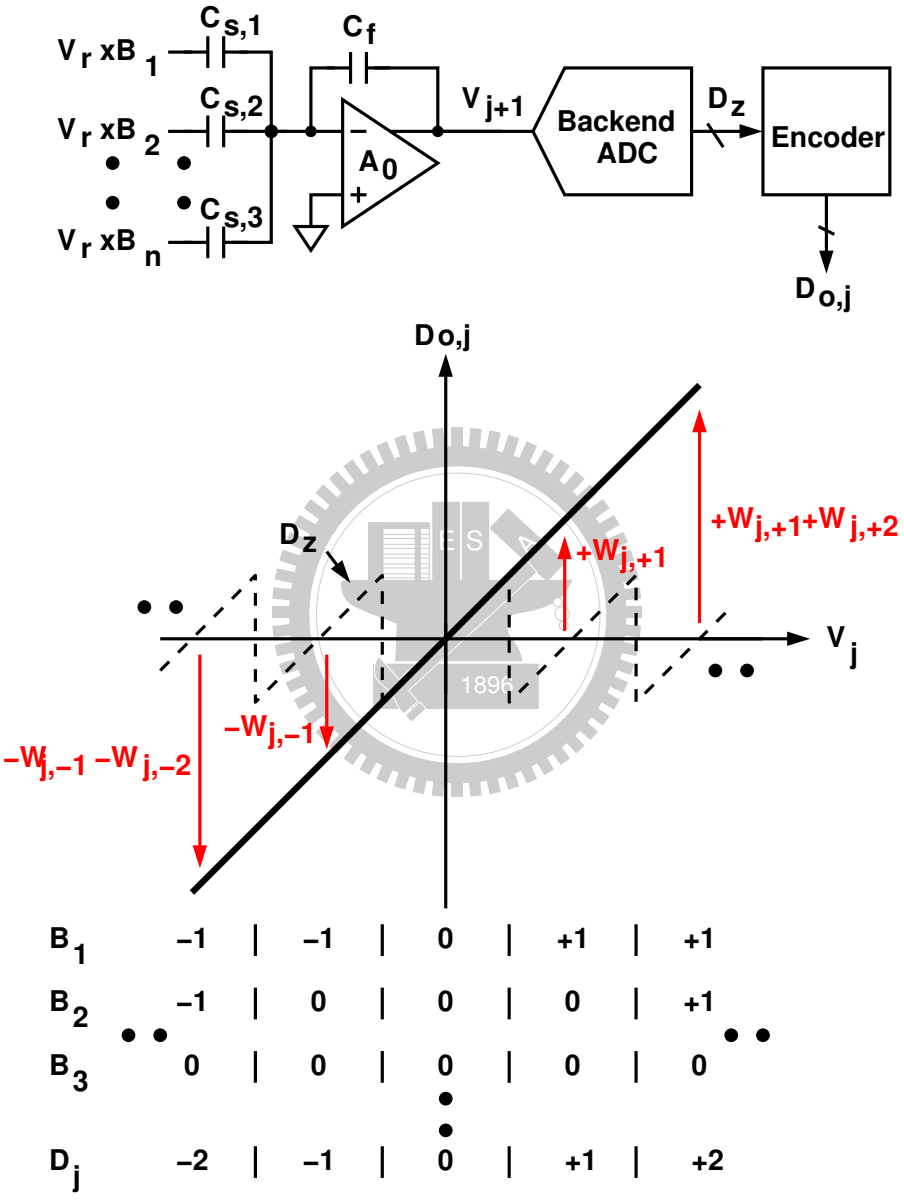



Figure 3.1: $V_j$-to-$D_{o,j}$ transfer characteristic of a pipelined ADC.

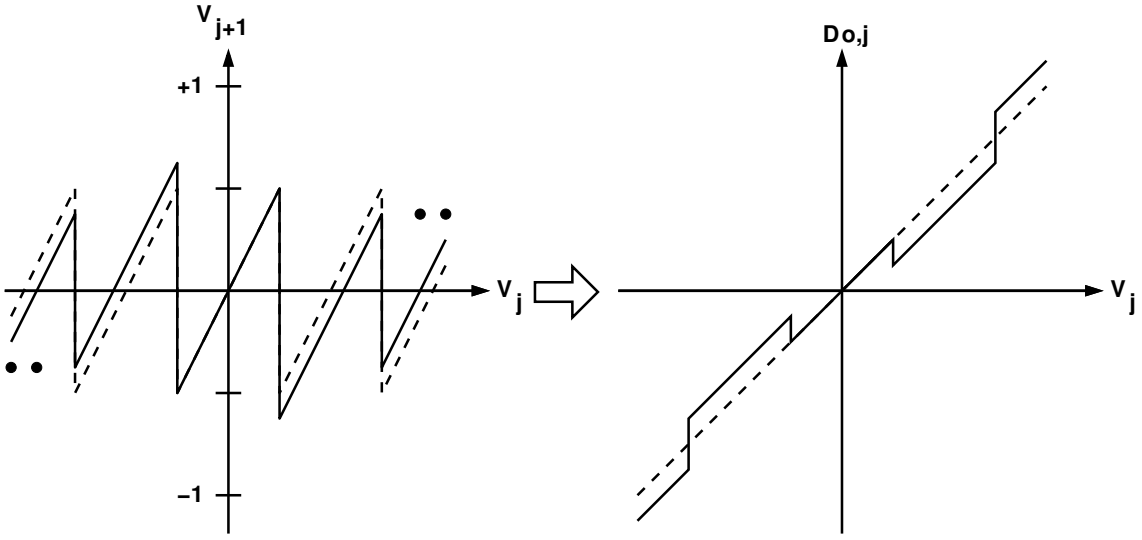



Figure 3.2: $V_j$-to-$D_{o,j}$ transfer charasteristics of pipeline stage with $V_j^{\mathrm{da}}$ mismatch.

ture, both $\hat{G}_j$ and $\hat{V}_j^{\mathrm{da}}(D_j)$ may also deviate from their nominal values respectively. These undesired deviations lead into nonlinearity for the overall A/D conversion [19, 20, 21, 22].

A multi-bit pipeline stage in amplifying phase is shown in Figure 3.1. The output $V_{j+1}$ is quantized by the backend ADC which comprises of (j+1)-th to P-th pipeline stages and the result is $D_{o,j+1}$. In the following section, we use $D_z$ to denote the backend ADC output for simplification. Assuming that the backend ADC is an ideal ADC and linear converts its input $V_{j+1}$ to a corresponding output $D_z$, that means

$$D_z = V_{j+1} \tag{3.1}$$

To encode a pipelined ADC output is to generate a digital output which is the linear representation of its input signal, that means $V_j$-to-$D_{o,j}$ is a linear transformation. As shown in Figure 3.1, $D_{o,j}$ can be expressed as:

$$D_{o,j} = D_z + \sum_{i=1}^{n} B_i \times W_{j,i} \tag{3.2}$$

The $D_z$ is shifted up or down by $W_{j,i}$ according to the value of $B_i$. The digital value $W_{j,i}$ represents the transition height when $D_i$ is changed by one. If the transfer characteristic of the pipeline stage is ideal , which means the transition height is equal to the nominal value, then after encoding, the ADC output $D_{o,j}$ is a linear representation of its analog input $V_j$, as shown in Figure 3.1.

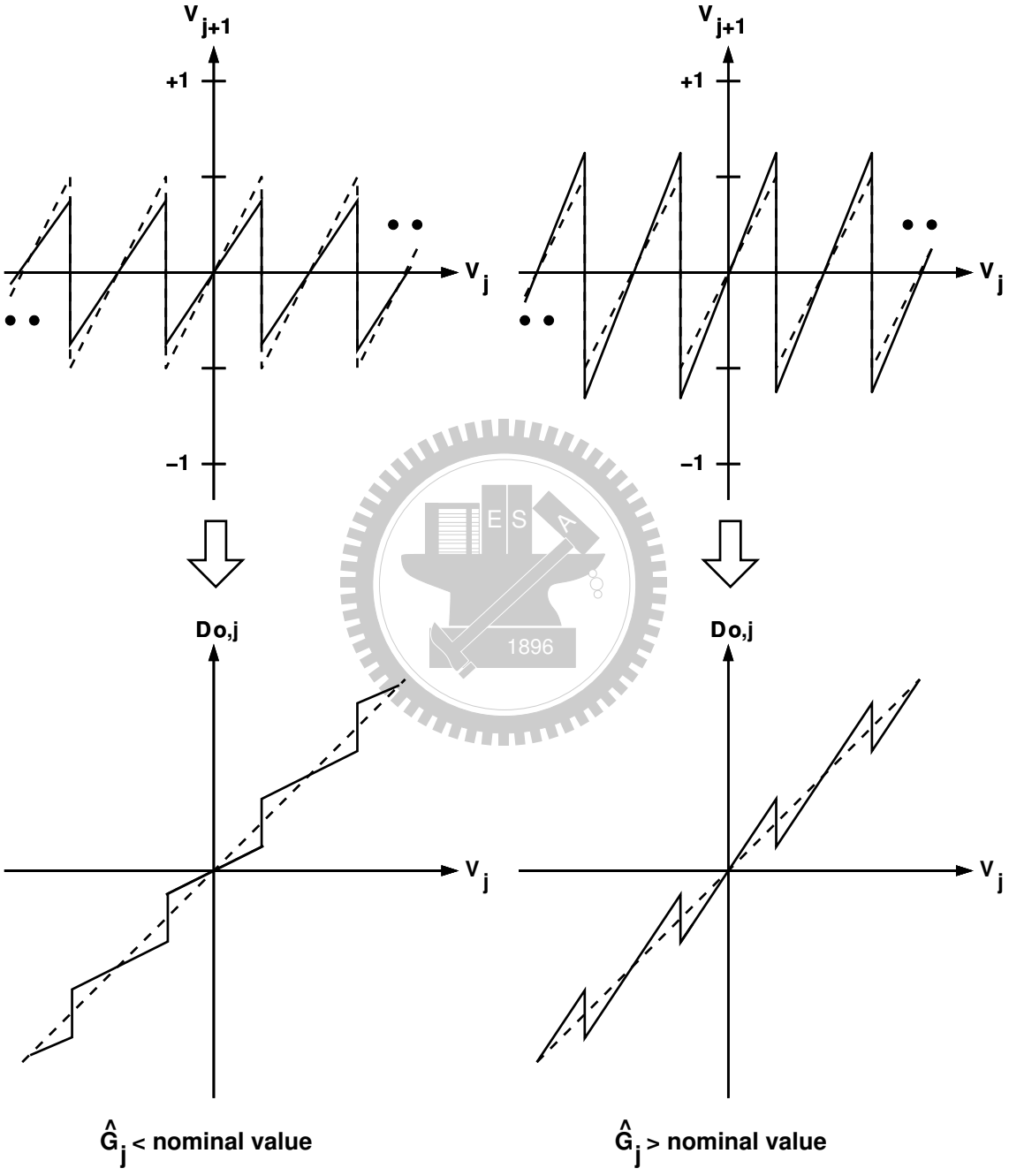



Figure 3.3: $V_j$-to-$D_{o,j}$ transfer charasteristics pipeline stage only with $\hat{G}_j$ mismatch.

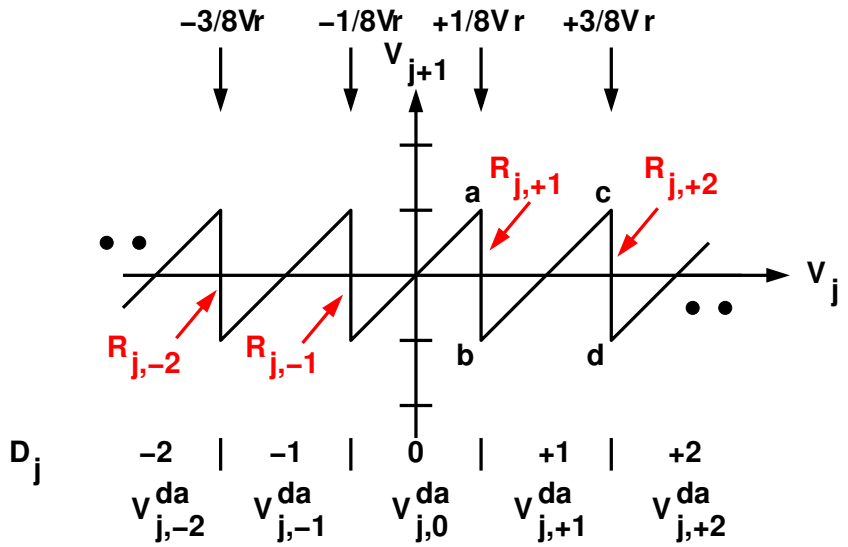



Figure 3.4: Output transfer curve of a pipeline stage.

However, in actual condition, the transfer characteristic deviates from the ideal case and the transition height is different from the ideal value, as shown in Figure 3.2 and Figure 3.3. Where the dash line is the ideal case and the solid line is the case with mismatch. Figure 3.2 is the pipeline stage that contains only $\hat{V}_j^{\mathrm{da}}$ mismatch and Figure 3.3 contains only $\hat{G}_j$ mismatch. $\hat{V}_j^{\mathrm{da}}$ and $\hat{G}_j$ make the transition height larger or smaller than the nominal value. According to Equation (3.2), the deviation of the transition height makes $V_j$-to-$D_{o,j}$ conversion not a linear relationship and have a discontinuous jump. These discontinuity means nonlinear distortion occurs in A/D conversion. This results can also be realized in Figure 3.2 and Figure 3.3. Imperfections introduce missing code and missing decision level in A/D conversion. In order to linearize the output of the ADC, the pipeline stage must be calibrated to eliminate these errors. We will introduce calibration techniques in the following section.

## 3.3 Digital Foreground Calibration

As mentioned above, to linearize the $V_j$-to-$D_{o,j}$ transfer characteristic of the ADC, the transition height of the pipeline stage must be calculated and corrected, and then used to encode the ADC's output. The calibration of the $j$-th pipeline stage involves measuring the

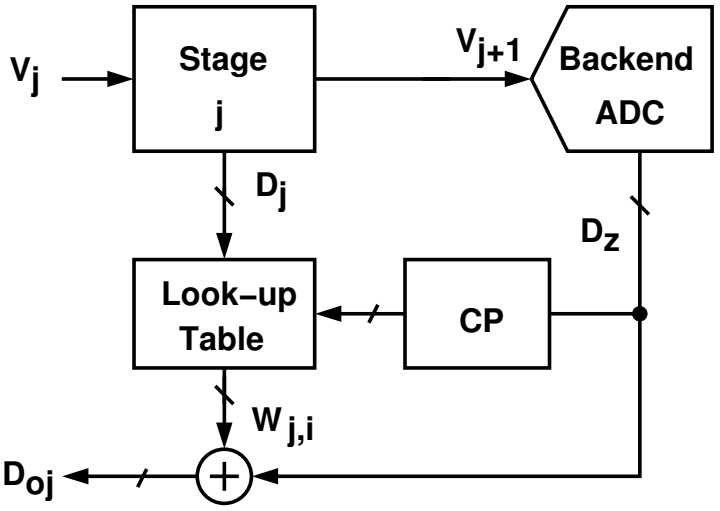



Figure 3.5: Digital calibration concept.

magnitude of the transition height and updating the value of $W_{j,i}$. According to Figure 3.4 and Equation (2.15), the transition height can be calculated as:

$$R_{j,+1} = V_{j+1,a} - V_{j+1,b} = +G_j \cdot V_{j,+1}^{da} - G_j \cdot V_{j,0}^{da} \tag{3.3}$$

$$R_{j,+2} = V_{j+1,c} - V_{j+1,d} = +G_j \cdot V_{j,+2}^{da} - G_j \cdot V_{j,+1}^{da} \tag{3.4}$$

$$\vdots$$

The transition height of the $V_j$-to-$V_{j+1}$ transfer function in Figure 3.4 is the value of $R_{j,i}$ when the $D_j$ digital code is changed by one. During calibration, $R_{j,i}$ is measured and digitized by a backend pipelined ADC, and the result is $W_{j,i}$. $W_{j,i}$ is the digital expression of $R_{j,i}$. The backend ADC quantizes the output $V_{j+1}$ of the $j$-th stage and generates a corresponding digital code $D_z$. If the backend ADC has a linear A/D characteristic, then its input $V_{j+1}$ can be denoted as:

$$V_{j+1} = \frac{1}{\hat{G}_z} \times D_z + O_z + Q_z \tag{3.5}$$

This $V_{j+1}$-to-$D_z$ conversion contains a conversion gain of $1/\hat{G}_z$, an offset of $O_z$, and a quantization error of $Q_z$.

According to Equation (3.3)-Equation (3.5), the calibration processor (CP) can yield calibration data $W_{j,i}$ that is related to $R_{j,i}$ as:

$$W_{j,i} = \hat{G}_z \times R_{j,i} \tag{3.6}$$

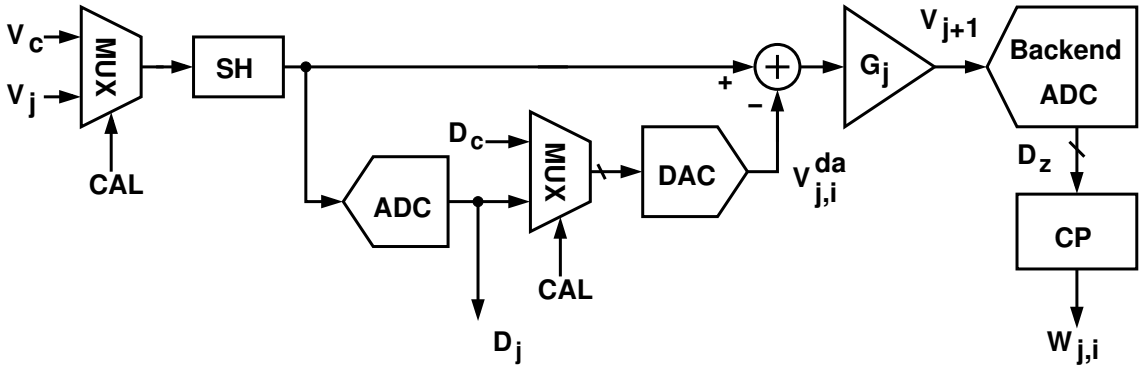



Figure 3.6: Calibration scheme of foreground calibration.

$W_{j,i}$ is the linear representation of $R_{j,i}$ and contains the actual gain of the backend ADC. During normal A/D conversion operation, the $W_{j,i}$ data become a look-up table, as shown in Figure 3.5.

In order to linearize the ADC, digital foreground calibration technique is used to calibrate the ADC [22, 23, 24, 25]. Foreground calibration, also called off-line calibration, is to calibrate the ADC with a deterministic testing analog input signal. During calibration period, the actual analog input is disabled and the calibration signal is applied to the ADC. Based on this reason, foreground calibration is usually performed in the power-on condition or the idle duration. By using a deterministic input signal, the calibration can be accomplished with less clock cycles compared with a background calibration technique.

Figure 3.6 is one of the scheme used to perform the foreground calibration. The concept of the foreground calibration is based on Equation (3.3) and Equation (3.4). To measure the transition height in foreground, the analog testing input $V_c$ is applied to the pipeline stage and the analog input $V_j$ is disabled in samplng phase, as shown in Figure 3.6. In amplifying phase, the sub-DAC input connects to $D_c$. To calculate $R_{j,1}$, $V_c = +V_r/8$ and $D_c$ changes from 0 to +1, that will alternate the output of the pipeline stage from $a$ to $b$ in Figure 3.4. $W_{j,1}$ can be estimated by calculating the difference of $D_z$ when $D_c$ changes from 0 to +1. The $W_{j,i}$ data in look-up table is then updated by the estimated $W_{j,1}$. To calculate $R_{j,2}$, $V_c = +3V_r/8$ and $D_c$ changes from +1 to +2, that will alternate the output of the pipeline stage from $c$ to $d$ in Figure 3.4. $W_{j,2}$ can then be obtained in the same way. The calibration procedure is repeated and is completed when all the transition

heights $W_{j,i}$ are obtained.

By calculating the difference of $D_z$, the transition height can be obtained easily. However, foreground calibration can not trace the change of temperature, supply voltage and other environment variation. Moreover, when the calibration is performed, the interruption of the input signal may not be suitable of some actual applications. These reasons make background calibration more attractive.

## 3.4 Correlation-Based Technique

Correlation-based technique is the most popular technique in digital background calibration. This technique is developed based on spread-spectrum modulation theory and used in background calibration. Spread-spectrum modulation technique is widely used in communication system [26]. With spread-spectrum modulation, the modulated signal can be transmitted to the receiver with high suppression of the interference. In this technique the desired input signal is spread by a pseudo-random number (PN) sequence and transmitted to the receiver. The desired signal passes through the channel with wideband interference that comes from the other channels. In the receiver, the received signal is despread by the same PN sequence and the interference is spread. Finally, a filter is used to extract the desired input signal.

Now, this theory is used to calibrate the pipelined ADC. The desired signal, which is mentioned in spread-spectrum theory, is the calibration data which is the value contains the capacitor mismatch and finite opamp's dc gain ,and is usually a dc signal. The ADC is like the channel in communication. The wideband interference is the ADC input analog signal and the ADC's quantization noise. In this technique, the calibration data is modulated by a PN sequence and mixed with the input signal, as shown in Figure 3.7. It's not necessary to interrupt the ADC's input signal and makes background calibration possible. In calibration duration, the calibration data can be extracted from ADC output in background without interrupting the normal operation of the ADC. The ADC's output $D_o$ can be written as:

$$D_o = V_i + R_{j,i} \times q \tag{3.7}$$

where $R_{j,i}$ is the randomized calibration data that we want to extract from the output and

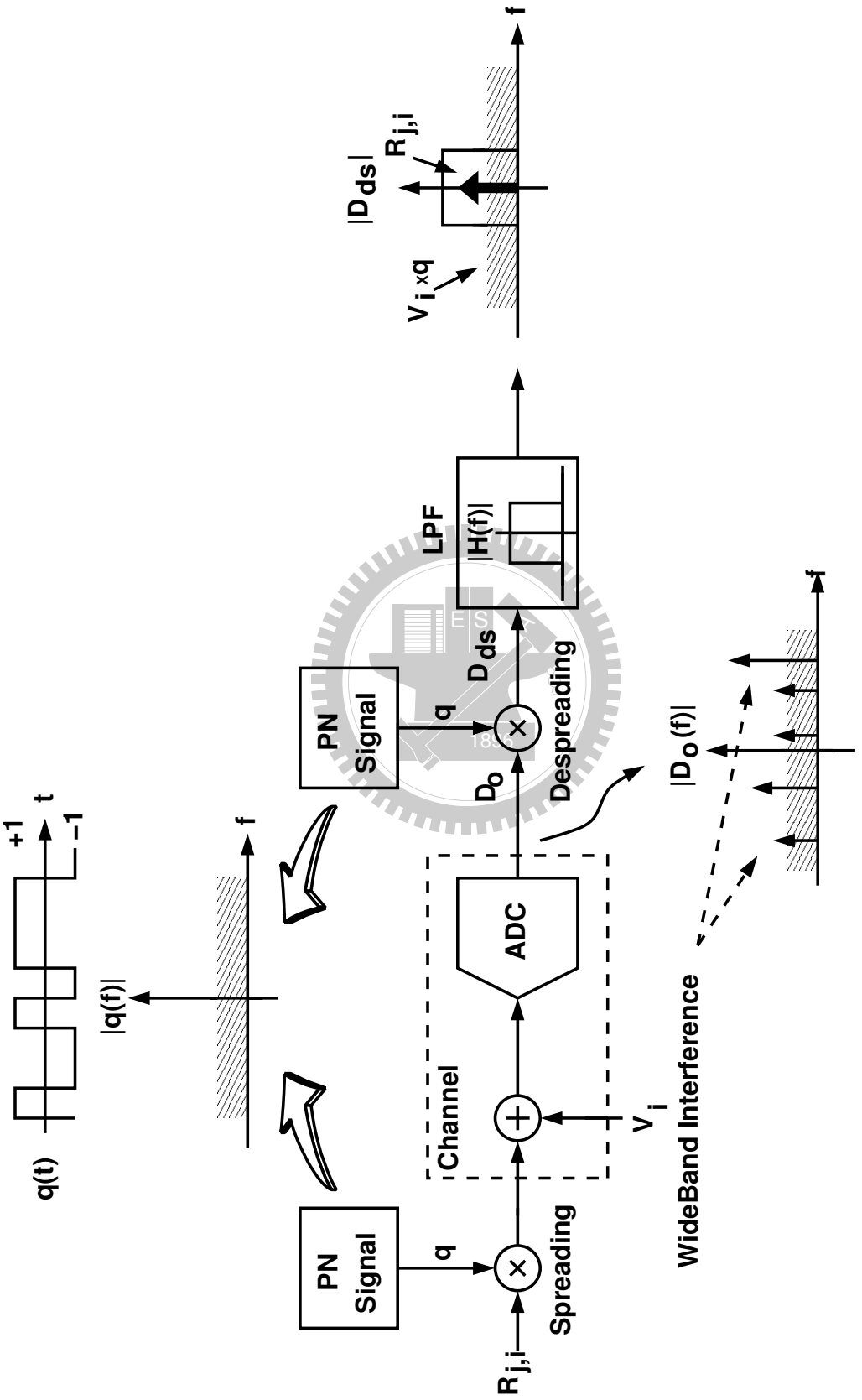



Figure 3.7: Spread-spectrum modulation in correlation data extraction.

$V_i$ is the ADC's input signal. The PN signal $q$ is white noise and uncorrelated $V_i$, as shown in Figure 3.7. The PN sequence $q$ alternates between $-1$ and $+1$ and its mean is zero.

To despread $D_o$, we multiply the output $D_o$ with $q$ and the result is

$$D_{ds} = D_o \times q = V_i \times q + R_{j,i} \times q^2 \tag{3.8}$$

$V_i$ is uncorrelated with $q$ and will be spread in frequency domain. The expected value $E[V_i \times q] = E[V_i] \times E[q] = 0$ and $E[R_{j,i} \times q^2] = E[R_{j,i}] \times E[q^2] = R_{j,k}$. Because $R_{j,i}$ is almost a dc signal, we can process $D_{ds}$ with a low-pass filter and the result is

$$E[D_{ds}] = E[V_i \times q] + R_{j,i} \times E[q^2] = R_{j,i} \tag{3.9}$$

The despread signal $V_i \times q$ is white in frequency domain and $R_{j,i}$ is a dc value. To achieve desired SNR, the low-pass filter must have sufficient low bandwidth to filter out the out-of-band noise that results from $V_i$. The bandwidth requirement is an important issue in background calibration, we will discuss this later. To perform a background calibration in pipelined ADC, we must try to modulate the calibration data and mix it with the input signal. This goal can be achieved in various ways, we will introduce these techniques in next section.

## 3.5 Prior Arts

Various calibration techniques have been demonstrated in pipelined ADCs to enhance their linearity [5, 6, 7, 8, 9, 2, 10, 27, 28]. These calibration techniques can be perform in analog domain or digital domain. But in our discussion, we focus on correlation-based digital background calibration technique. Background calibration techniques usually need to modify the analog circuit or change the operation configuration, that usually make the analog circuit more complex. How to modify the analog circuits without degrading the operating speed is an important issue in background calibration. In this section, we will learn about these techniques.

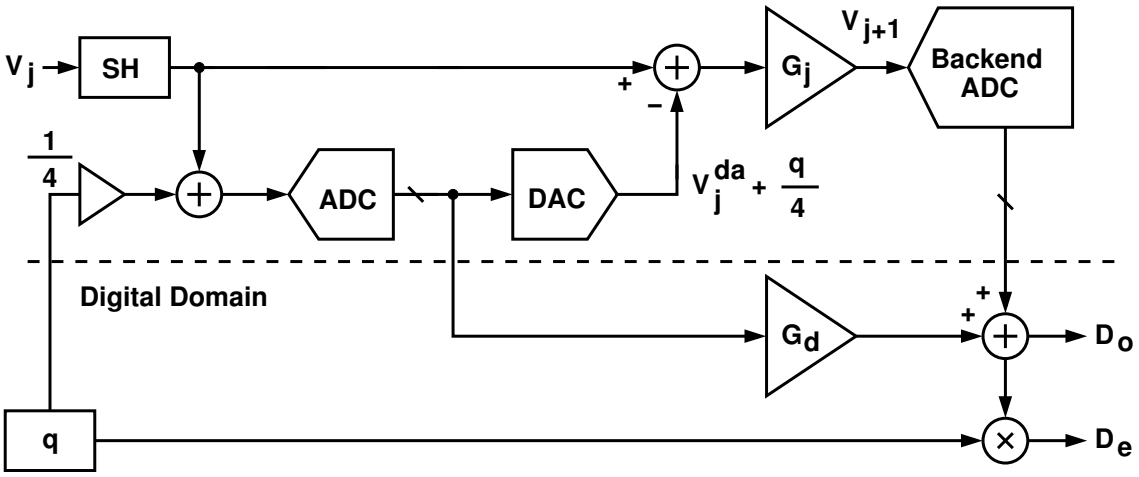



Figure 3.8: PN signal injects into the pipeline stage before the sub-ADC.

### 3.5.1 Randomization of sub-ADC and sub-DAC

As mentioned in Section 2.2, the pipelined ADC can generate linear output as long as the residue gains for each stage are known. One approach is to adjust the residue gain in digital domain to make sure that it is equal to the residue gain in analog domain. In order to calculate the residue gain, a PN signal is injected before the residue gain amplifier. One can inject the PN signal $q$ into the pipeline stage through the sub-ADC, as shown in Figure 3.8 [6, 4]. Where $G_j$ is the analog residue gain and $G_d$ is the residue gain in digital domain. This PN signal injection can be achieved by randomly scrambling the reference of the sub-ADC. The injected PN signal increases the output swing of the amplifier and reduces the input dynamic range of the ADC, so that the injected signal is scaled by a factor of $1/4$ to reduce the required extra output range. The output of the pipeline stage in Figure 3.8 is

$$V_{j+1} = G_j \times \left( V_j - V_j^{\mathrm{da}} - q \cdot \frac{1}{4} \right) \tag{3.10}$$

The output $D_o$ is

$$D_o = G_j \cdot V_j + V_j^{\mathrm{da}} \cdot (G_d - G_j) + q \cdot \frac{1}{4} \cdot (G_d - G_j) \tag{3.11}$$

The third term of Equation (3.11) is correlated with the PN signal and is also proportion to the residue gain mismatch. After passing $q \times D_o$ through a LPF, the output will be

$$D_e = \frac{1}{4} \cdot (G_d - G_j) \tag{3.12}$$

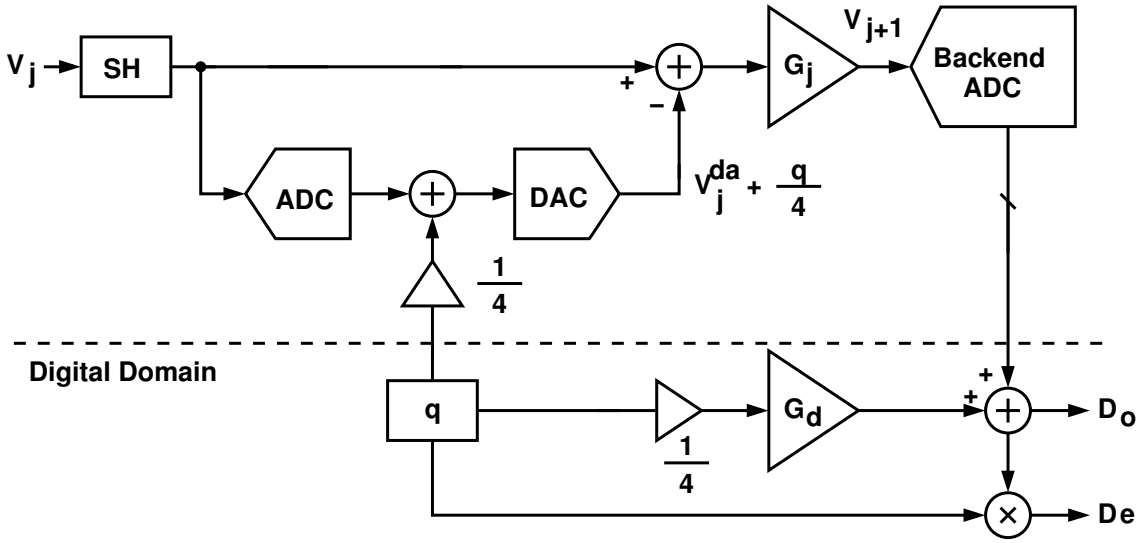



Figure 3.9: PN signal injects into the pipeline stage before the sub-DAC.

So that we can adjust the $G_d$ in digital domain to force the error term $D_e$ is zero. With $G_j = G_d$, the output $D_o$ is equal to $G_j \cdot V_j$ and the $V_j$-to-$D_o$ conversion is a linear A/D conversion.

As similar to Figure 3.8, the PN signal can also be injected into the signal path of the pipelined ADC through the sub-DAC, as shown in Figure 3.9 [6, 29]. The injected signal is also scaled to reduce the extra output signal range. The output of the pipeline stage is the same as Equation (3.10). The digital output $D_o$ is

$$D_o = G_j \times \left(V_j - V_j^{\mathrm{da}}\right) + q \cdot \frac{1}{4} \cdot (G_d - G_j) \tag{3.13}$$

After passing $q \times D_o$ through with a LPF, the error is the same as Equation (3.12) and can be used to correct the gain mismatch in digital domain.

However, this technique demands sufficient matching requirement of the PN signal between analog domain and digital domain. The PN signal injection technique usually expands the output signal swing of the residue amplifier. This drawback also reduces the dynamic range of the ADC. These requirements limit the practical application of these techniques.

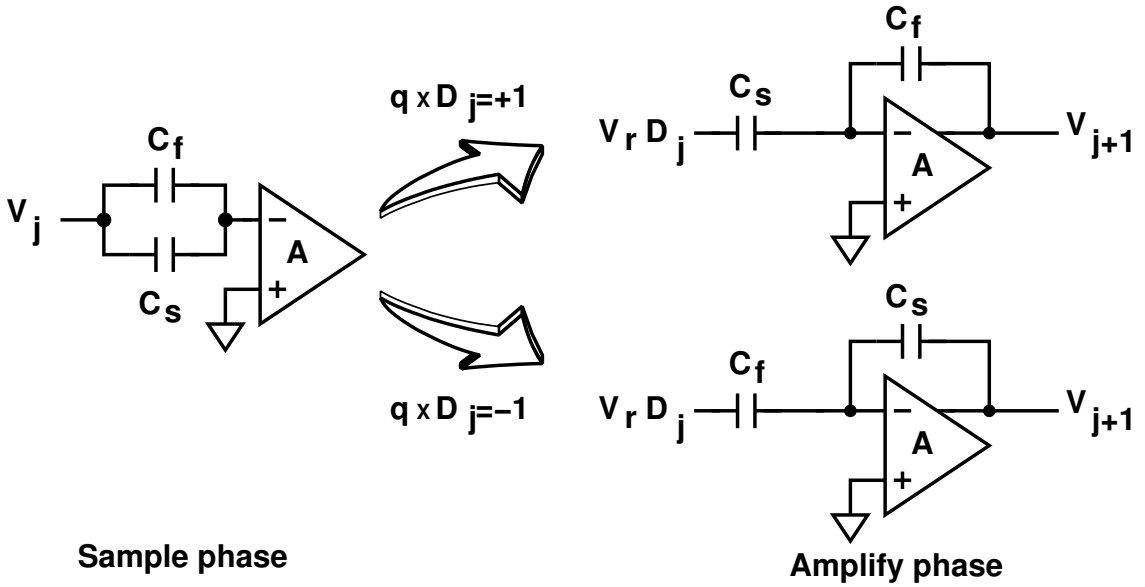



Figure 3.10: A 1.5-bit pipeline stage with capacitor swapping using PN signal.

### 3.5.2 Capacitor-Swapping Technique

The PN signal injection techniques described above may reduce the dynamic range of the ADC that is undesired in low-voltage technology. A capacitor-swapping technique is introduced in [30, 31, 32, 33]. This technique changes the operation configuration and requires no extra signal range. Now we introduce the technique published in [32] for example. Consider a 1.5-bit pipeline stage, its output can be written as:

$$V_{j+1} = \frac{C_s + C_f}{C_f} \cdot V_j - \frac{C_s}{C_f} \cdot V_r \cdot D_j \tag{3.14}$$

where we neglect the opamp finite dc gain and its input parasitic. Now we can change the role of $C_s$ and $C_f$ randomly according to PN signal $q$ and sub-DAC output $D_j$, as shown in Figure 3.10. The different configuration can be expressed by re-writing Equation (3.14) as:

$$V_{j+1} = (2 + \Delta_c \cdot q \cdot D_j) \cdot V_j - (1 + \Delta_c \cdot q \cdot D_j) \cdot V_r \cdot D_j \tag{3.15}$$

where $C_s = C(1 + \Delta_c)$ and $C_f = C$. Multiply $V_{j+1}$ with $q$ and pass through a LPF, then the residue term, which is uncorrelated with q and contains the capacitor mismatch information, is:

$$V_e = \Delta_c \times (D_j \cdot V_j - V_r) \tag{3.16}$$

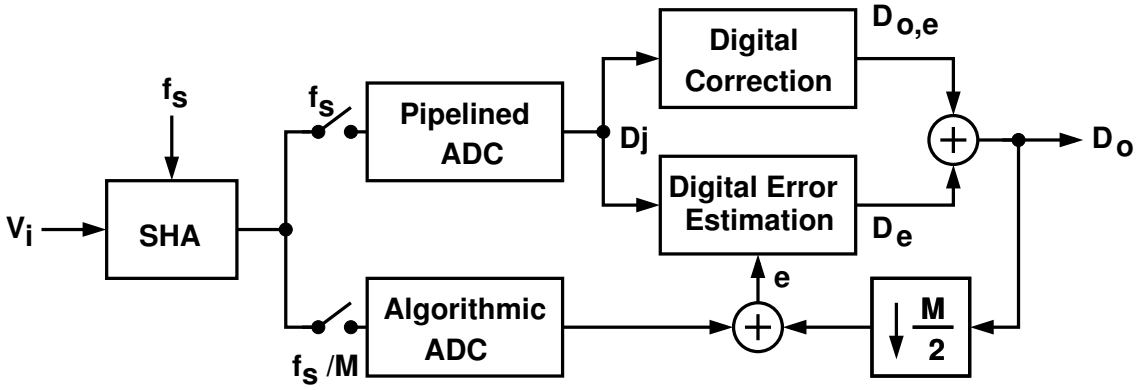



Figure 3.11: The calibration scheme published in [1].

Because $(D_j \cdot V_j - V_r) \leq 0$, the polarity of $V_e$ always depends on the polarity of $\Delta_c$. The polarity of $V_e$ can be used to trim the capacitor in analog domain or adaptive adjust the residue gain in digital domain to make a more linear A/D conversion. However, the opamp's finite dc gain will not be randomized by the PN signal, so that sufficient large dc gain is required to make the error caused by the finite dc gain neglected.

### 3.5.3 Calibration with Reference ADC

To achieve a high speed and high resolution ADC, the main ADC can be calibrated by a slow-speed but high-accuracy ADC [1, 34, 35]. The slow-speed ADC is used as a reference ADC and used to estimate the error of the main ADC, as shown in Figure 3.11. With a high accuracy ADC, the error between the main ADC and the reference ADC is minimized to achieve a high resolution ADC.

The calibration scheme is shown in Figure 3.11 [1], the reference ADC is used to calibrate the main ADC. The output difference $e$ is processed by a digital error estimation (DEE) block to estimation the error of each pipeline stage. The output $D_{o,e}$ of the digital correction block is the output with error and $D_e$ is the estimated error of the pipelined ADC output. Combining $D_{o,e}$ and $D_e$ will generate the correct output $D_o$.

However, to make sure the reference ADC is accurate enough, self-calibration may be applied to the reference ADC. In addition, the reference ADC needs extra area, power and results in larger area and power dissipation.

### 3.5.4 Split-Capacitor Technique

As described in Section 3.3, to calibrate a pipeline stage, foreground technique can be used to estimate the transition height of the transfer characteristics. In radix-2 1.5-bit architecture, the transition height is the output difference when the sub-DAC value $D_j$ swaps between $\{0, +1\}$ or $\{0, -1\}$, as shown in Figure 3.6. However, the input signal is disabled so that the $D_j$ swapping can be performed in foreground calibration. To make the foreground approach can be used in background configuration, a split-capacitor technique is proposed to make it possible.

Split-capacitor technique was first introduced in [2]. For a radix-2 1.5-bit pipeline stage, the sampling capacitor $C_s$ is split into $N$ equal capacitors and $C_s = C_{s,1} + C_{s,2} + \cdots + C_{s,N}$. In samplng phase, all of the capacitors are used to sample the input signal. In amplifying phase, one of the sampling capacitors is used to inject a PN signal, its value is $\{0, +1\}$ or $\{0, -1\}$, and the others are under the normal operation. The modified configuration makes the normal operation of the MDAC reserved and also enables the swapping of the $D_j$ for the capacitor. The modified pipeline stage and its transfer characteristics are shown in Figure 3.12 and Figure 3.13.

The detail operation of the modefied pipeline stage in calibration is described below. When $\phi_1 = 1$ its operation is the same as the traditional pipeline stage, the input $V_j$ is connected and sampled by all the capacitors. When $\phi_2 = 1$, the $q \cdot V_r$ voltage is connected to one of the $C_s$ fragments, $C_{s,i}$, where $i \in \{1, 2, \cdots, N\}$, while the $D_j \cdot V_r$ voltage is connected to the other $C_s$ fragment. The signal $q$ is a digital binary-valued sequence generated from a PN generator. With this modified operation, a PN sequence with a magnitude of $R_{j,i}$ is injected into the signal path of the pipeline stage. The output of the pipeline stage can be expressed as:

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}} - V_j^{\mathrm{os}}\right] + R_{j,i} \times \left(D_j - q\right) \tag{3.17}$$

$$= \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}} - V_j^{\mathrm{os}}\right] + R_{j,i} \times D_j - R_{j,i} \times q \tag{3.18}$$

where

$$R_{j,i} = \hat{G}_j \times \frac{C_{s,i}}{C_s + C_f} \tag{3.19}$$

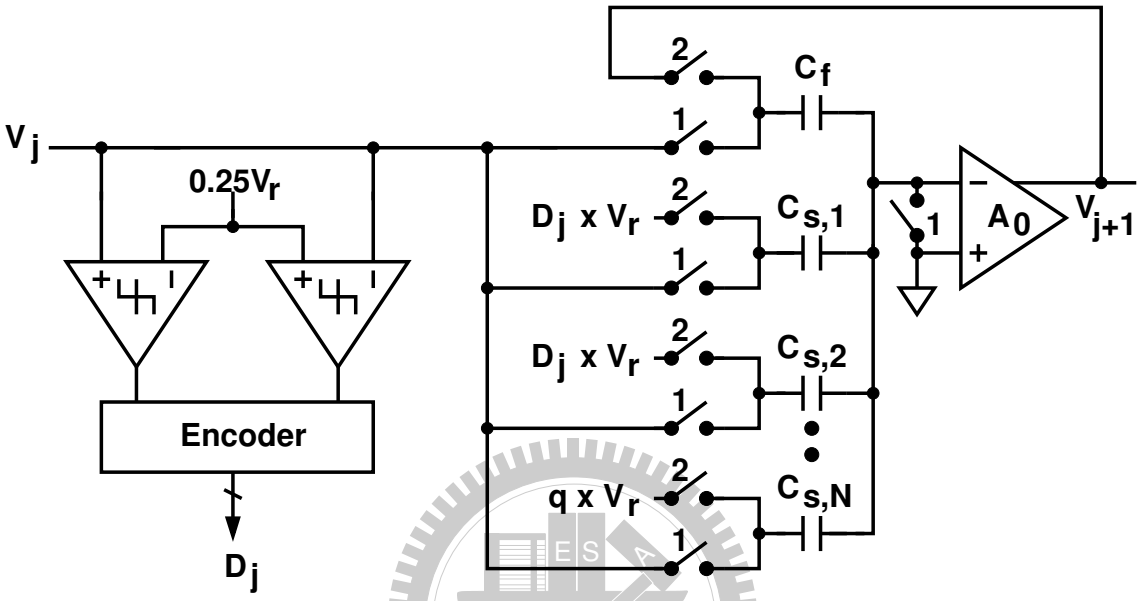



Figure 3.12: The split-capacitor radix-2 1.5-bit pipeline stage in [2].

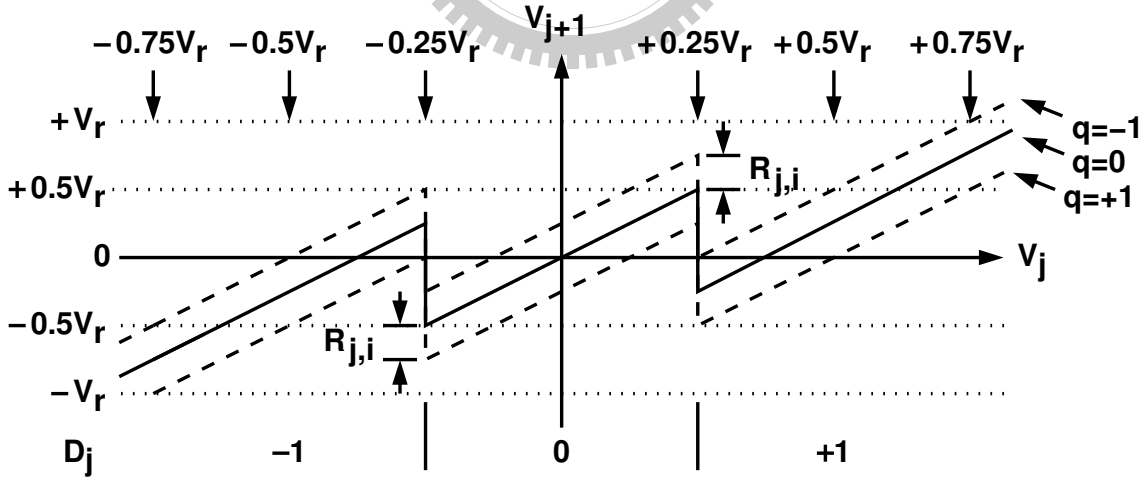



Figure 3.13: Figure 3.12's conversion characteristic with "q" injection.

The transition height $R_j$ is

$$R_j = \sum_{i=1}^{N} R_{j,i} \tag{3.20}$$

To measure $R_{j,i}$, $q$ alternates between $\{+1, 0\}$ and $\{-1, 0\}$. As mentioned in Section 3.4, by using a low-pass filter, the magnitude of $R_{j,i}$ can be extracted in the digital domain and the its value is $W_{j,i}$.

In beginning, $C_{s,1}$, i.e. $i = 1$, is being calibrated and is used to inject the PN signal. After $R_{j,1}$ is obtained, capacitor $C_{s,1}$ is connected to $D_j \cdot V_r$ and capacitor $C_{s,2}$ is connected to $q \cdot V_r$. After $R_{j,2}$ is obtained, capacitor $C_{s,2}$ is connected to $D_j \cdot V_r$ and capacitor $C_{s,3}$ is connected to $q \cdot V_r$ and so on. The calibration is sequentially from $i = 1$ to $i = N$. After the $R_{j,1}$ is calculated for $i = 1, 2, \cdots, N$, the magnitude of $R_j$ can be obtained by using Equation (3.20).

As shown in Figure 3.13 and Equation (3.17), the q injection increases the required range of the output signal swing. The extra signal range is

$$\Delta V_{j+1} = \hat{G}_j \times V_r \times \frac{C_{s,i}}{C_s + C_f} \approx V_r \times \frac{C_{s,i}}{C_f} \approx \frac{V_r}{N} \tag{3.21}$$

For the same opamp output swing, the $q$ injection decreases the dynamic range of the ADC. The impact can be mitigated by splitting the capacitor into more capacitors, i.e., increasing $N$ and resulting in smaller $C_{s,i}$.

According to [2], the calculated $W_{j,i}$ contains error term $\Delta W_{j,i}$. The error is caused by the nominal A/D residual signal in $V_{j+1}$. One can assume this residual signal is uniformly distributed between $+0.5V_r$ and $-0.5V_r$. Then, the variance of $\Delta W_j$ can be expressed as:

$$\sigma^2 \left(\Delta W_j\right) = \frac{N}{M} \times \frac{V_r^2}{12} \tag{3.22}$$

This result shows that the variance is proportioned to $N$ but larger $N$ also results in long calibration time.

From the discussion above we can conclude that for calculation variance and calibration time consideration, smaller $N$ is desirable. For dynamic range consideration, larger $N$ is desirable. A compromise should be made between the variance and the dynamic range.

## 3.6 Proposed Split-Capacitor Configuration

As mentioned in previous section, the split-capacitor number $N$ should be as small as possible, but this also leads to large output swing. A 1.5-bit pipeline stage with $N = 2$ and its transfer characteristic are shown in Figure 3.14 and Figure 3.15. The transfer function of the pipeline stage now depends on the state of $q$. Introducing the $q$ sequence increases the required voltage range of $V_{j+1}$. If the input $V_j$ is confined between $\pm 0.5V_r$, then the output $V_{j+1}$ expands between $\pm V_r$, comparing with the $\pm 0.5V_r$ span of the origin design. This situation is worsened for multi-bit pipeline stage. In order to make the calibration technique be feasible with $N = 2$, the operation configuration must be modified and the extra output range in the split-capacitor calibration scheme can be eliminated by more intelligent control of the $q$ sequence.

Now we propose a new split-capacitor configuration and apply it to a 2.5-bit pipeline stage. For the $j$-th pipeline stage, its analog processor (AP) receives the analog signal $V_j$ from the $(j-1)$-th stage and generates the analog output $V_{j+1}$. The pipeline stage also includes a digital calibration processor (CP) and an encoder. The digital signal $D_j$ from the AP and the digital signal $D_{o,j+1}$ from the $(j+1)$-th stage are combined to produce the digital output $D_{o,j}$. Their function is to ensure that $D_{o,j}$ is an accurate digital representation of $V_j$. The AP includes a sub-ADC and a voltage-mode switched-capacitor circuit that implements the functions of a sub-DAC and a subtracting amplifier. The modified 2.5-bit pipeline stage and its transfer characteristics are shown in Figure 3.16 and Figure 3.17. The switches in Figure 3.16 are controlled by two non-overlapping clocks, $\phi_1$ and $\phi_2$. During $\phi_1 = 1$, the voltage $V_j$ is sampled on capacitors $C_f$, $C_{s,1}$, $C_{s,2}$, ..., $C_{s,6}$. During $\phi_2 = 1$, $C_f$ becomes a feedback capacitor, and each $C_{s,i}$, where $i = 1, 2, \cdots, 6$, is connected to a reference $V_r \times B_i$. The value of $B_i$ is among $\{-1, 0, +1\}$. The $C_{s,i}$ capacitors form the sub-DAC, whose output is controlled by the signals $B_i$.

The sub-ADC comprises 13 comparators with thresholds at 0, $\pm(1/8)V_r$, $\pm(2/8)V_r$, ..., $\pm(6/8)V_r$ respectively. Its digital output $D_j$ is an estimate of the input $V_j$. The relationship between $D_j$ and $V_j$ is shown in Figure 3.17. The value of $D_j$ is among $\{\pm 0, \pm 1, \pm 2, \cdots, \pm 6\}$. The two zeros, $-0$ and $+0$, are used to distinguish the polarity of $V_j$.

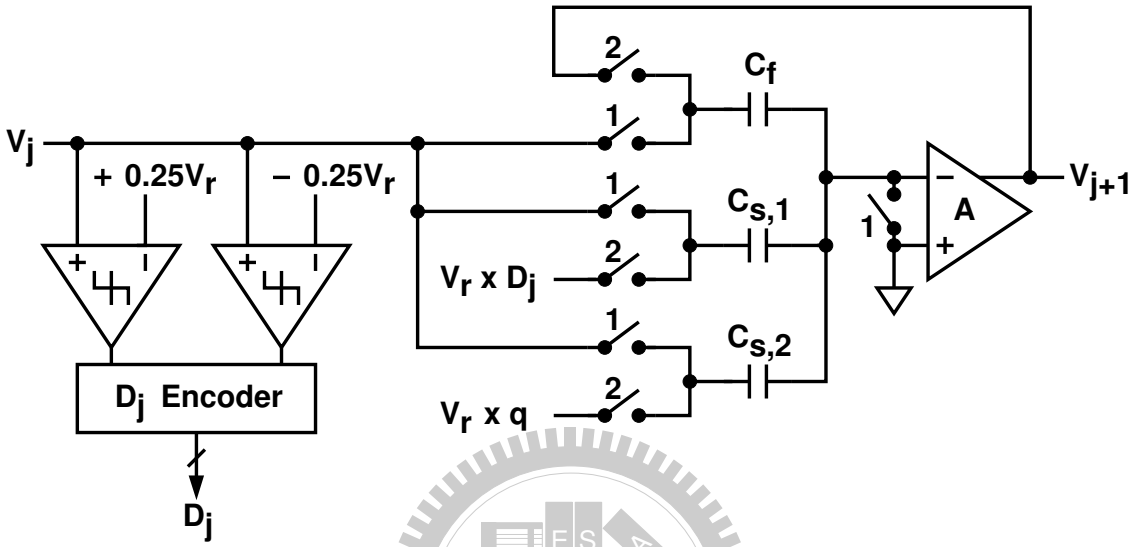



Figure 3.14: A split-capacitor SC pipeline stage with $N = 2$.

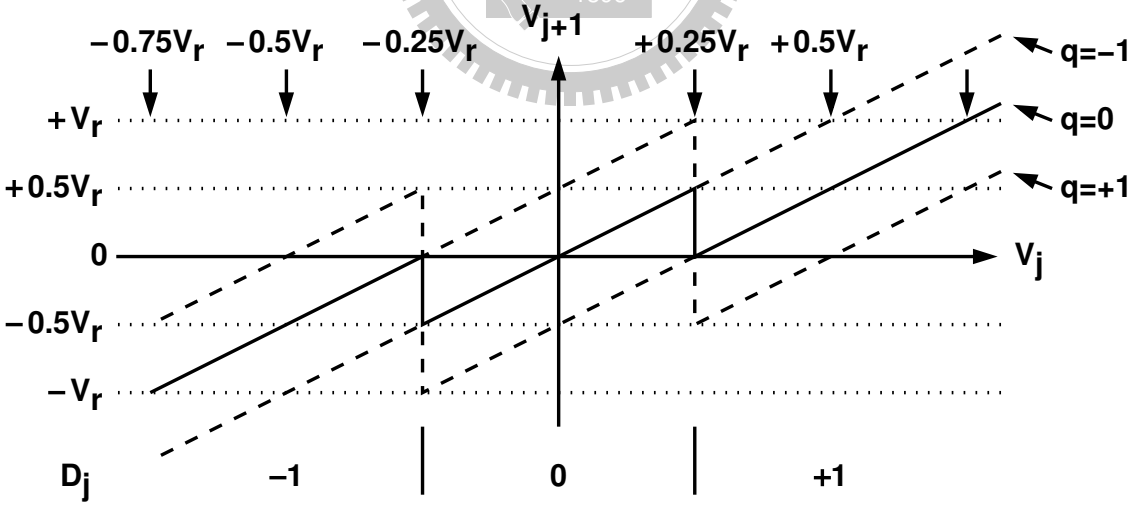



Figure 3.15: Transfer characteristic of Figure 3.14's pipeline stage.

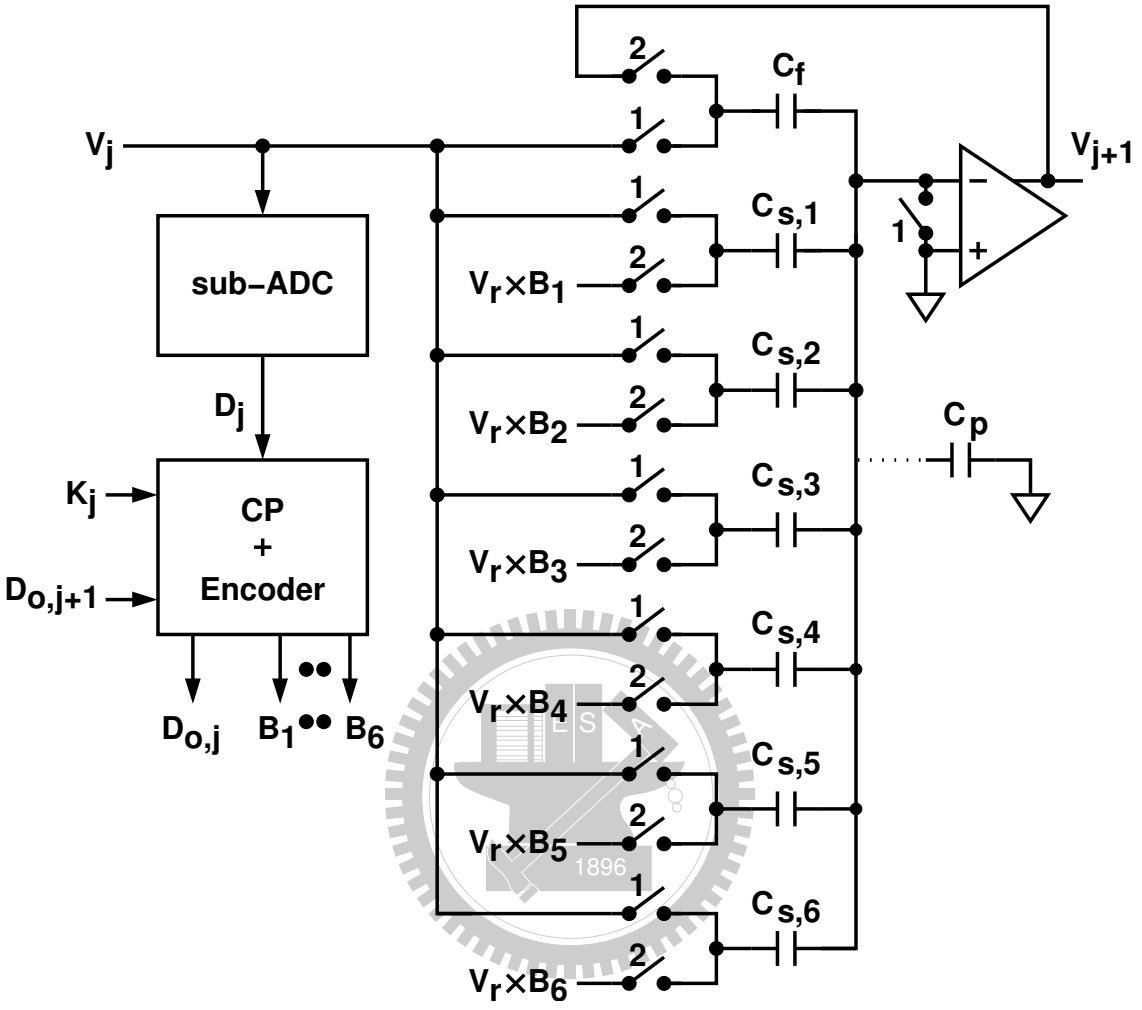



Figure 3.16: A split-capacitor SC pipeline stage with redundant comparators.

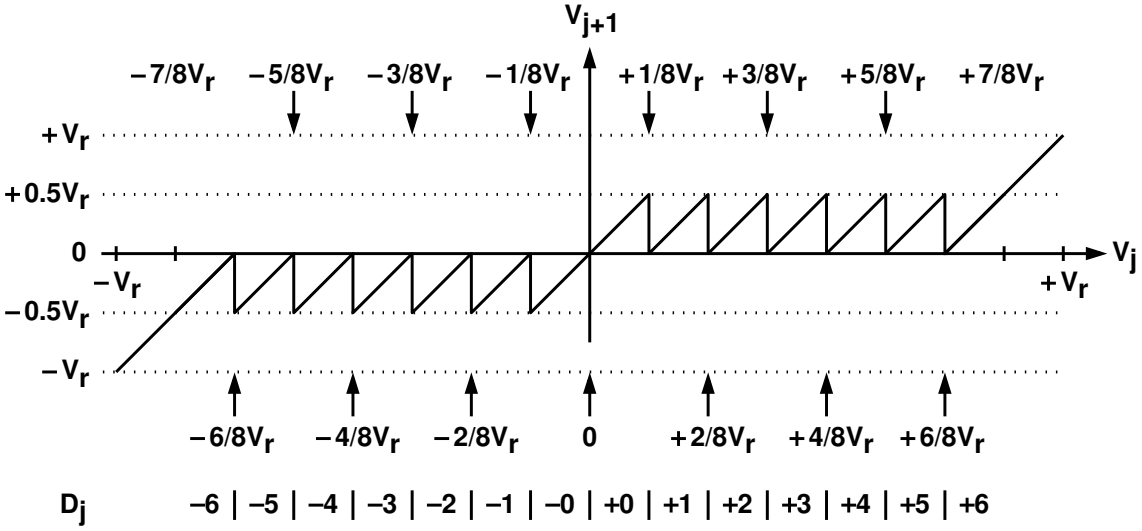



Figure 3.17: Transfer characteristic of Figure 3.16's pipeline stage.

The pipeline stage includes a CP and an encoder that generates the digital output $D_{o,j}$ and the sub-DAC control signals $B_i$, where $i = 1, 2, \cdots, 6$. When $K_j = 0$, the calibration operation for the $j$-th stage is disabled. The $\boldsymbol{B} = [B_1, B_2, \cdots, B_6]$ signal set forms a thermometer code of $D_j$. For example, if $D_j = +2$, then $\boldsymbol{B} = [+1, +1, +0, +0, +0, +0]$. If $D_j = -4$, then $\boldsymbol{B} = [-1, -1, -1, -1, -0, -0]$.

Assume the opamp in Figure 3.16 is linear and has a finite dc gain of $A_0$. Then, its output during $\phi_2 = 1$ can be written as:

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}} - V_j^{\mathrm{os}}\right] \tag{3.23}$$

where

$$\hat{G}_j = \frac{C_s + C_f}{C_f} \times \frac{1}{1 + \frac{1}{A_0} \cdot \frac{C_s + C_f + C_p}{C_f}} \tag{3.24}$$

$$\hat{V}_j^{\mathrm{da}} = V_r \sum_{i=1}^{6} \frac{C_{s,i} \times B_i}{C_s + C_f} \tag{3.25}$$

$$C_s = C_{s,1} + C_{s,2} + \cdots + C_{s,6} \tag{3.26}$$

In the above equations, $\hat{G}_j$ is the realized stage gain. $\hat{V}_j^{\mathrm{da}}$ is the output of the sub-DAC. $C_p$ is the total parasitic capacitance at the opamp's input. $V_j^{\mathrm{os}}$ represents the offset of this pipeline stage.

In an ideal case, $A_0 = \infty$ and $C_{s,i} = C_f/2$ for all $i$. Then, the stage gain is $G_j = 4$. The sub-DAC's output is $V_j^{\mathrm{da}} = D_j \times V_r/8$. The ideal $V_j$-to-$V_{j+1}$ transfer function is shown in Figure 3.17. In reality, the opamp gain $A_0$ is finite and the capacitance $C_{s,i}$ randomly deviates from the $C_f/2$ nominal value.

The $V_j$-to-$V_{j+1}$ transfer function shown in Figure 3.17 indicates that the stage output range is between $\pm V_r/2$ if the input is confined between $\pm 7V_r/8$. In our design, the overall ADC input range is $\pm 7V_r/8$. The maximum output range of the opamp is also closed to $\pm 7V_r/8$. The $\pm 3V_r/8$ design margin for the opamp's output range is served to accommodate device variations.

The complexity of both sub-ADC and sub-DAC in the design of Figure 3.16 is twice as much as that in a conventional pipeline stage with a stage gain of 4. Those are the overhead for enabling digital background calibration without increasing the stage's output range. However, the total capacitance $C_s + C_f$ in Figure 3.16 remains the same value as

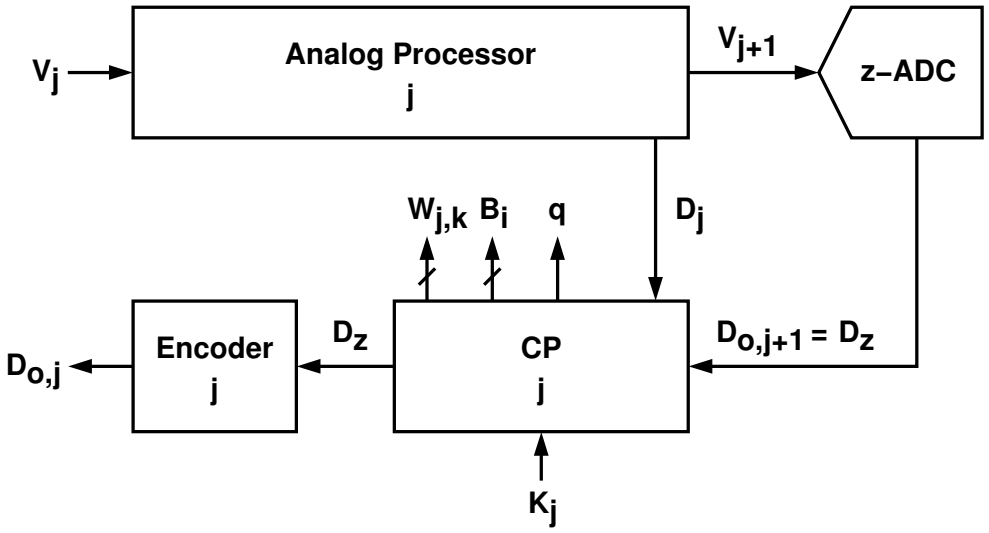



Figure 3.18: Configuration for gain/sub-DAC calibration.

that of a conventional design. Thus, the speed of the analog signal path is only degraded slightly by the increased input capacitance of the sub-ADC.

## 3.7 Principle of Gain/DAC Calibration

The operation of the $j$-th pipeline stage is summarized in Figure 3.18. The sub-ADC in the AP quantizes the analog input $V_j$ and generates the corresponding $D_j$. The sub-DAC in the AP is controlled by the CP through the control signals $B_i$. The AP generates the analog signal $V_{j+1}$ which is expressed in Equation (3.23). The $V_{j+1}$ is then digitized by a back-end ADC, called z-ADC, which comprises the succeeding stages starting from the $(j+1)$-th pipeline stage to the final flash ADC. The digital output from the z-ADC is $D_{o,j+1}$. The $j$-th encoder combines this $D_{o,j+1}$ with information from the CP to generate the $D_{o,j}$ digital output. To simplify denotation, instead of $D_{o,j+1}$, $D_z$ is used as the z-ADC's digital output for the rest of this paper.

Let the A/D conversion of the z-ADC be linear and expressed as:

$$V_{j+1} = \frac{1}{\hat{G}_z} \times D_z + O_z + Q_z \tag{3.27}$$

This $V_{j+1}$-to-$D_z$ conversion contains a conversion gain of $1/\hat{G}_z$, an offset of $O_z$, and a quantization error of $Q_z$.

For a specific $i$, where $i = 1, 2, \cdots, 6$, define $R_{j,i}$ as the $V_{j+1}$ variation when the signal $B_i$ in Figure 3.16 is changed by 1, i.e.,

$$R_{j,i} = \hat{G}_j \times V_r \times \frac{C_{s,i}}{C_s + C_f} \tag{3.28}$$

Also define $W_{j,i}$ as the digital value of $R_{j,i}$ when it is digitized by the z-ADC, i.e,

$$W_{j,i} = \hat{G}_z \times R_{j,i} \tag{3.29}$$

Then the digital output $D_{o,j}$ can be encoded as:

$$D_{o,j} = \sum_{i=1}^{6} \left( B_i \times W_{j,i} \right) + D_z \tag{3.30}$$

The relationship between $V_j$ and $D_{o,j}$ is

$$V_j = \frac{1}{\hat{G}_j \hat{G}_z} \times D_{o,j} + \left[ V_j^{\text{os}} + \frac{O_z}{\hat{G}_j} \right] + \frac{Q_z}{\hat{G}_j} \tag{3.31}$$

Note that Equation (3.31) is arranged in a form similar to Equation (3.27). The $V_j$-to-$D_j$ A/D conversion is also linear, but has a new conversion gain of $1/(\hat{G}_j \hat{G}_z)$, a new offset of $V_j^{\text{os}} + O_z/\hat{G}_j$, and a quantization error of $Q_z/\hat{G}_j$. The quantization error is reduced by the stage gain $\hat{G}_j$. The unknown $\hat{G}_j$ gain and $R_{j,i}$ sub-DAC step sizes do not affect the linearity of Equation (3.31).

The $D_{o,j}$ encoding defined in Equation (3.30) requires the $W_{j,i}$ data. Thus, calibrating the $j$-th stage involves acquiring $W_{j,i}$ for $i = 1, 2, \cdots, 6$. For a pipelined ADC, there is no need to calibrate all the pipeline stages. In practice, only the first $K$ stages are subjected to calibration. Accuracy of the remaining pipeline stages are ensured by circuit components' inherent characteristics. Assuming that PN sequence $q$ with an identical length of $M$ is employed to calibrate each pipeline stage. A total of $6KM$ samples are required to complete one calibration cycle. In reality, smaller $M$ can be used for the later stage because of the reduced resolution requirement.

For a pipelined ADC calibration, the entire pipelined ADC is calibrated backward and sequentially. A calibration cycle begins with calibrating the $K$-th stage with the backend ADC as the z-ADC, i.e., $D_z = D_{o,K+1}$. The acquired $W_{K,i}$ data are stored and used in the $D_{o,K}$ encoding. Once the calibration of the $K$-th stage is completed, the calibration

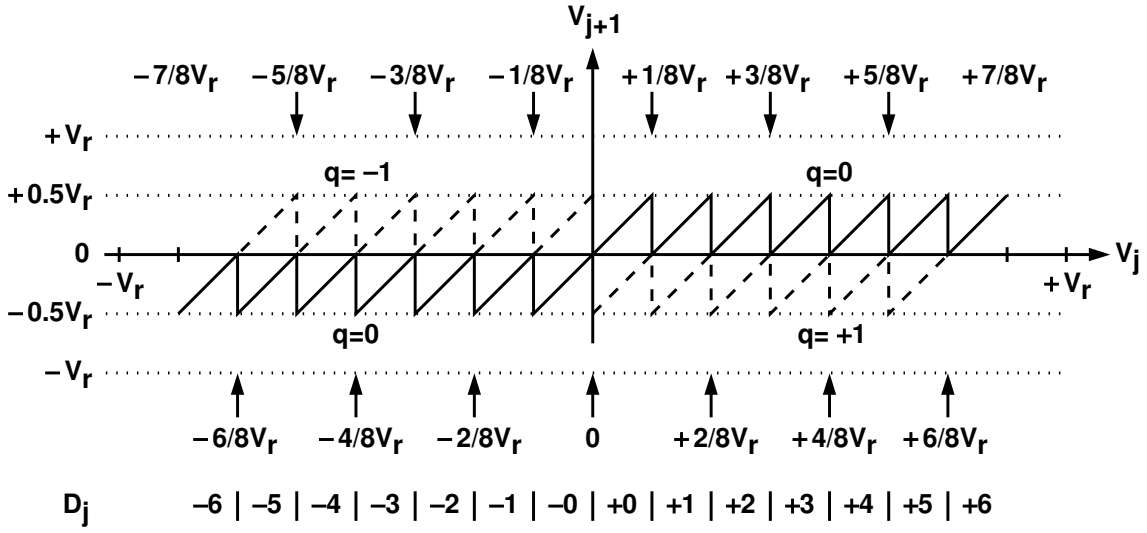



Figure 3.19: Transfer characteristic of Figure 3.16's pipeline stage when PN sequence is injected in it.

of the $(K-1)$-th stage is started, and then, the backend ADC from the $K$-th stage serves as the z-ADC, i.e., $D_z = D_{o,K}$. One calibration cycle is completed when the calibration procedure of the first stage is finished.

## 3.8 Input-dependent $q$ Generation

In Figure 3.18 and Figure 3.16, if $K_j = k \neq 0$, then the $j$-th stage is under calibration. The CP isolates the $C_{s,k}$ capacitor and makes the remaining $C_{s,i}$ capacitors provide the $D_j$-to-$\hat{V}_j^{\mathrm{da}}$ conversion. For example, if $k = 2$, then, the signal set $\boldsymbol{B} = [B_1, B_3, B_4, B_5, B_6]$ forms a thermometer code of $D_j$ with $B_2$ excluded. This $D_j$-to-$\hat{V}_j^{\mathrm{da}}$ conversion has an input range of $|D_j| \leq 5$. When $D_j = +6$, all $B_i$ signals are set to $+1$. When $D_j = -6$, all $B_i$ signals are set to $-1$.

In the $K_j = k$ calibration mode, the control signal $B_k$ for the $C_{s,k}$ capacitor adopts the value of a PN sequence, $q$, whose value is among $\{-1, 0, +1\}$. The sequence $q$ changes its value every clock cycle. But the change depends on $D_j$. When $+0 \leq D_j \leq +5$, the sequence $q$ switches randomly between $+1$ and 0. When $-5 \leq D_j \leq -0$, the sequence $q$ switches randomly between $-1$ and 0. However, when $D_j = +6$, $q$ is frozen as $q = +1$. When $D_j = -6$, $q = -1$.

To avoid a correlation between $q$ and $V_j$, two separate PN sequences generators are used, which are $q_1$ and $q_2$. The value of $q_1$ is among $\{0, +1\}$, and the value of $q_2$ is among $\{0, -1\}$. When $+0 \leq D_j \leq +5$, $q_1$ is activated and $q = q_1$. When $-5 \leq D_j \leq -0$, $q_2$ is activated and $q = q_2$.

The $V_j$-to-$V_{j+1}$ transfer function now becomes:

$$V_{j+1} = \underbrace{\hat{G}_j \times \left[V_j - \hat{V}_j^{\text{da}} - V_j^{\text{os}}\right]}_{Y'} - R_{j,k} \times q \tag{3.32}$$

where $R_{j,k}$ is defined in Equation (3.28) with $i$ replaced by $k$. Compared to Equation (3.23), a $R_{j,k} \times q$ random sequence is added to the output $V_{j+1}$. The $Y'$ in Equation (3.32) is defined as the $V_j$-dependent component in $V_{j+1}$. The resulting $V_j$-to-$V_{j+1}$ transfer function is shown in Figure 3.19. The sequence $q$ dynamically changes the transfer function while confining the $V_{j+1}$ output between $\pm 0.5 V_r$. When $q = 0$, the solid line is the transfer function, which is also the $V_j$-to-$Y'$ transfer function. When $D_j \geq +0$ and $q = +1$, the dash line is the transfer function, which is shifted downward from the solid line by an amount of $R_{j,k}$. When $D_j \leq -0$ and $q = -1$, the dash line is the transfer function, which is shifted upward from the solid line by an amount of $R_{j,k}$.

## 3.9 Correlation-Based Calibration Data Extraction

In Figure 3.16 and Figure 3.18, if $K_j = k \neq 0$, the CP controls the behavior of the AP so that it can extract the $W_{j,k}$ parameter from $D_z$. In Figure 3.19, under the $+0 \leq D_j \leq +5$ input condition, the average value of $V_{j+1}$ for the $q = +1$ dash line is less than the average value of $V_{j+1}$ for the $q = 0$ solid line by an exact amount of $R_{j,k}$.

The parameter $W_{j,k}$ is a digitized value of $R_{j,k}$. It can be extracted from $D_z$ using the $W_{j,k}$ extractor shown in Figure 3.20. The extractor collects only those $D_z$ samples when $+0 \leq D_j \leq +5$. To complete one extraction, $M$ samples of $D_z$ are needed. The samples are sorted according to the value of $q$, and then accumulated on two accumulators (ACCs). It is assumed that half of the samples are associated with $q = 0$ and the other halves are associated with $q = +1$. The accumulation-and-dump operation depicted in Figure 3.20 acquires an average of the sorted samples. The results are $E\left[D_z\right]_q$, where $q \in \{0, +1\}$.

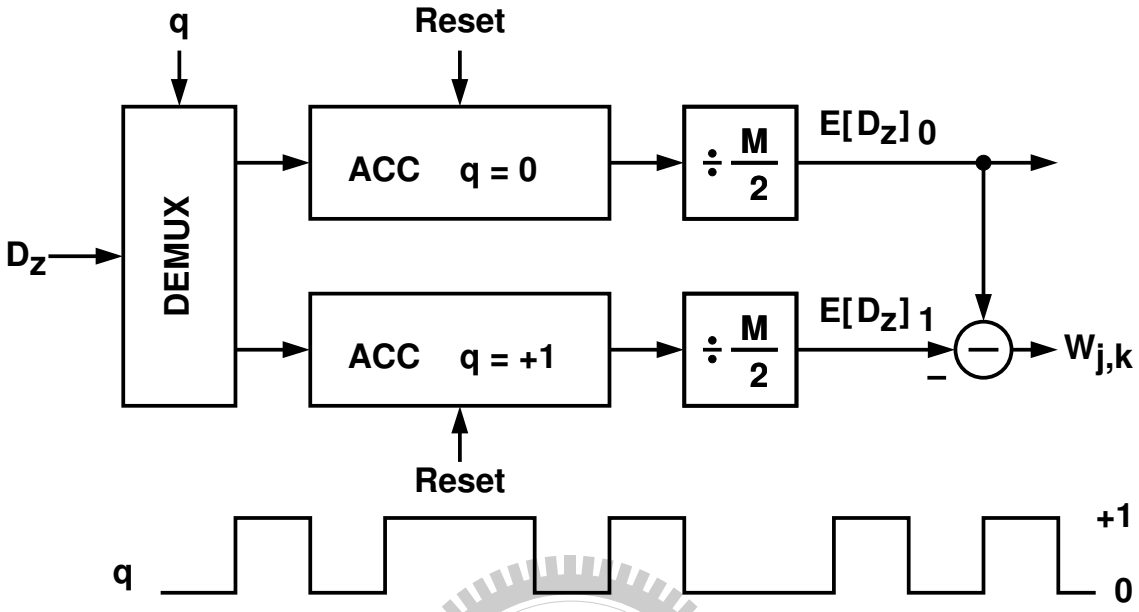



Figure 3.20: A correlation-based $W_{j,k}$ extractor.

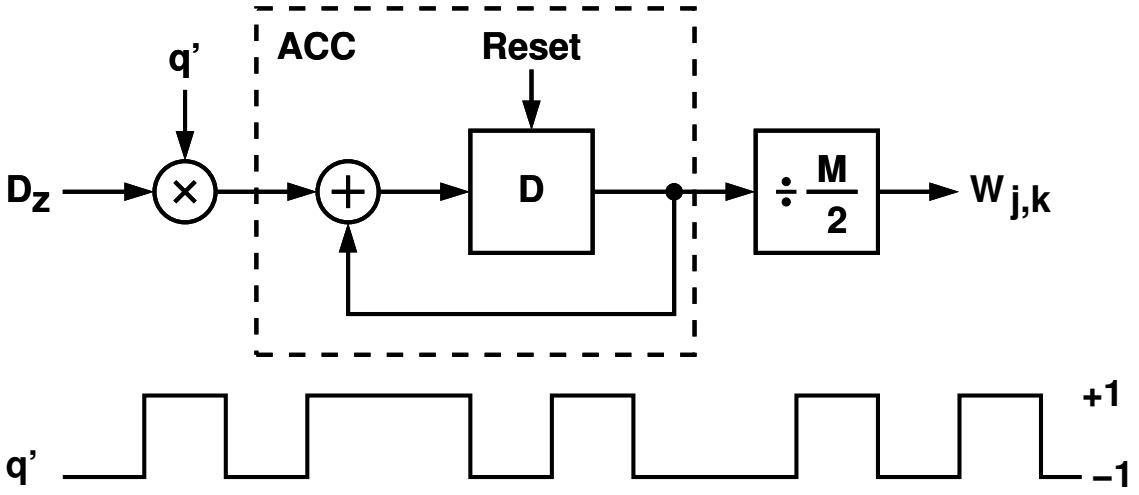



Figure 3.21: An alternative form of $W_{j,k}$ extractor.

From Equation (3.32) and Equation (3.27), they can be expressed as:

$$(1/\hat{G}_z) \times E\left[D_z\right]_0 + O_z = E[Y'] \tag{3.33}$$

$$(1/\hat{G}_z) \times E\left[D_z\right]_{+1} + O_z = E[Y'] - R_{j,k} \tag{3.34}$$

Thus, the difference between $E\left[D_z\right]_0$ and $E\left[D_z\right]_{+1}$ is $W_{j,k} = \hat{G}_z R_{j,k}$.

It is assumed that the PN sequence $q$ is not correlated with $V_j$, so that $E[Y']$ under $q = 0$ is identical to $E[Y']$ under $q = +1$. Note that the quantization error $Q_z$ in Equation (3.27) is eliminated due to averaging, and the offset $O_z$ is eliminated by the subtraction shown in Figure 3.20.

The subtractor and DEMUX in Figure 3.20 can be combined, resulting in an alternative form of $W_{j,k}$ extractor shown in Figure 3.21 [2]. The $D_z$ samples are multiplied with an $q'$ sequence before being averaged, where $q' \in \{-1, +1\}$ has the same sequence pattern as $q$. The hardware cost for Figure 3.21 is less than that for Figure 3.20.

The $W_{j,k}$ extractor shown in Figure 3.20 collects only the $D_z$ samples when $+0 \leq D_j \leq +5$. The other $W_{j,k}$ extractor is needed when $-5 \leq D_j \leq -0$. Both extractors acquire the same $W_{j,k}$ parameter. Using two extractors can avoid the situation in which $V_j$ is always positive or always negative. If $V_j$ is always negative, although the $W_{j,k}$ extractor for $D_j > 0$ cannot collect enough valid $D_z$ samples to extract $W_{j,k}$, the extractor for $D_j < 0$ can produce the same $W_{j,k}$ at the same time.

To complete the $j$-th stage calibration, the $K_j$ calibration control is varied from 1 to 6 sequentially, so that all $W_{j,k}$ data are acquired, where $i = 1, 2, \cdots, 6$. When a stage is under calibration, it can still perform its nominal A/D conversion, i.e., converting $V_j$ to $D_{o,j}$. The digital output $D_{o,j}$ is generated by employing Equation (3.30) with previously acquired $W_{j,k}$ data.

As similar to Section 3.5.4, the output of $W_{j,k}$ extractor contains a $W_{j,k}$ term and a variation term $\Delta W_{j,k}$. The variation is caused by the nominal A/D residual signal in $V_{j+1}$. One can assume this residual signal is uniformly distributed between $+0.25V_r$ and $-0.25V_r$. Then, the $\Delta W_j$ variation can be expressed as:

$$\sigma^2\left(\Delta W_j\right) = \frac{2}{M} \times \frac{V_r^2}{48} \tag{3.35}$$

Equation (3.22) and Equation (3.35) show that the $M$ requirement is relaxed com-

pared to the original design in Figure 3.12, this is because the input-dependent $q$ generation technique reduces the signal swing, i.e. reduce the variance of $\Delta W_{j,k}$.

## 3.10 Summary

The nonlinearity caused by capacitor mismatch and finite opamp gain is described in this chapter. The calibration concept is presented with mathematics analysis. This chapter describes a robust background calibration scheme for switched-capacitor pipelined ADCs. A new split-capacitor calibration configuration is proposed to remedy the drawback of prior arts. By splitting the input sampling capacitor $C_s$ of a MDAC, random noise containing calibration data can be injected into the signal path and then extracted from the ADC's digital output. By adding redundant comparators and applying input-dependent generation of the PN sequence $q$, the $C_s$ capacitor needs only to be split to two equal parts, while requiring no extra signal range for accommodating the random term in the signal path. Another benefit of this technique is the reduced length requirement of the PN signal. With minimum modification, the split-capacitor pipeline stage can operate in the same speed compared to the original 2.5-bit pipeline stage.

This technique described in this chapter is used to correct the gain/DAC error of the pipeline stage. However, in deep-submicron technology, the stage gain may contain nonlinearity. This means the gain/DAC calibration is insufficient in this condition. In next chapter, we will discuss about the nonlinearity of the pipeline stage.

# Chapter 4

# Stage Nonlinearity Calibration

## 4.1 Introduction

The calibration technique we described above is used to correct the residue gain and sub-DAC error of the pipeline stage. In deep-submicron technology, low supply voltage and low intrinsic gain make the nonlinearity of pipeline stage become an important issue. Even with the calibration techniques we have learned, the ADC output may contain servere nonlinearity that limits the resolution. For the pipeline stage of Figure 2.8, if the opamp's gain is low and depends on its signal swing, then the stage's analog transfer function can no longer be treated as a jagged straight line, as shown in Figure 4.1. Stage's nonlinearity worsened if the supply voltage is reduced while the $V_{j+1}$ signal range is kept unchanged. So that the nonlinearity of the pipeline stage should be calibrated to enhance the resolution of ADC. To further improve A/D conversion linearity, there are schemes which also calibrate amplifier's nonlinearity [5, 7, 9, 36, 37, 38]. However, these schemes have their limilations. In this chapter, we will explain the nonlinearity of the pipeline stage and describe the limitations of prior arts. Finally, split-capacitor calibration technique is extended to correct the stage's nonlinearity.

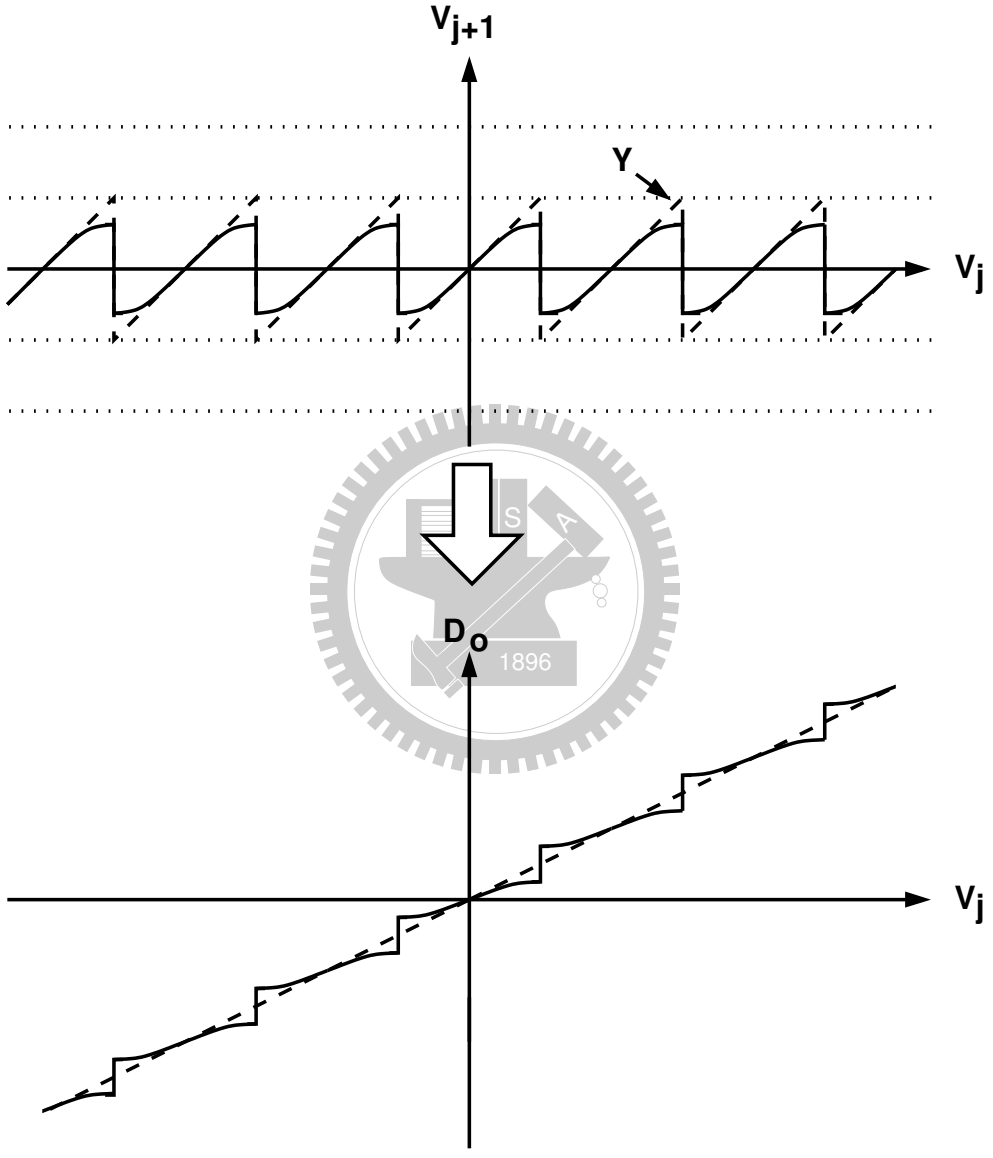



Figure 4.1: Multi-bit pipelined ADC transfer charateristics with stage nonlinearity.

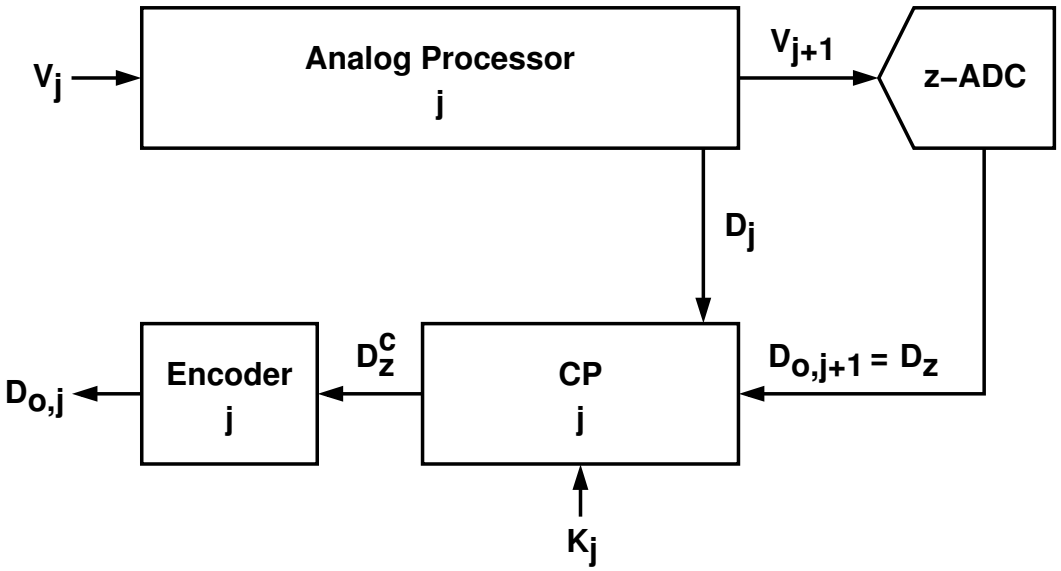



Figure 4.2: Basic nonlinearity correction scheme.

## 4.2 Nonlinearity Modeling and Correction

To linearize the pipelined ADC, the distortion error must be compensated to enhance the resolution of the ADC. Now consider a pipeline stage with nonlinear distortion. The basic calibration scheme is shown in Figure 4.2. The pipeline stage output $V_{j+1}$, which contains the distortion error, is quantized by the backend ADC and the output is $D_z$. The output $D_z$ is processed by the calibration processor (CP) which is used to correct the nonlinearity of the j-th pipeline stage and its output is $D_z^c$. The generated output $D_z^c$ is a linear representation of $Y$ which is the linear output described in Equation (2.15). The encoder combines $D_j$ and $D_z^c$ and generates the linear output $D_{o,j}$ which is the linear representation of analog input $V_j$.

Now consider a 2.5-bit pipeline stage with only odd-order nonlinearity, then the output $V_{j+1}$ is

$$V_{j+1} = Y - a_3 \cdot Y^3 - a_5 \cdot Y^5 + \cdots \tag{4.1}$$

where $Y$ is the linear output expressed in Equation (2.15). This equation is usually used to model the nonlinear distortion or used in system level simulation. As described in previous chapter, assuming that $D_z$ is a linear expression of $V_{j+1}$ and according to Equa-

tion (4.1), $D_z$ can be written as:

$$D_z = V_{j+1} = Y - a_3 \cdot Y^3 - a_5 \cdot Y^5 + \cdots \tag{4.2}$$

The output $D_z^c$ is generated by the following approximation:

$$Y = D_z^c = D_z + b_3 \cdot D_z^3 + b_5 \cdot D_z^5 + \cdots \tag{4.3}$$

In order to generate a linear output $D_z^c$, we have to estimate the distortion coefficients, $b_3$, $b_5$, etc., and use to correct the nonlinear distortion. If the distortion coefficients can be estimated in advance, then the distortion can be corrected in digital domain regardless of the distortion generated in analog domain. Equation (4.3) is used to compensate the distortion error in the following section.

## 4.3 Prior Arts

In order to enhance the resolution of the pipelined ADC and correct the distortion error of the opamp, several digital background calibration techniques have been demonstrated in various publications. Here, we will introduce these techniques and their limitations.

### 4.3.1 Statistic-based Distance Estimation

[5] is the first article trying to correct the nonlinear distortion of the residue amplifier in pipelined ADC. The calibration concept is illustrated in Figure 4.3. A PN sequence is used to switch the operation mode of the pipeline stage. The output alternates randomly between the solid line and dash line according to the random-nimber generator (RNG) output. This can be accomplished easily by using different comparator decision levels. The slope of the input and output transfer characteristic is determined by the capacitor ratio and the gain of the amplifier. If the amplifier's gain is a constant value for different output swing, the slope will be the same for the two operation configurations. The calibration processor estimates the distance between the dash line and the solid line for different input distributions, and the distances for the two input distributions are $h_1$ and $h_2$. For a linear opamp, the distances $h_1$ and $h_2$ are equal. For a nonlinear opamp, large

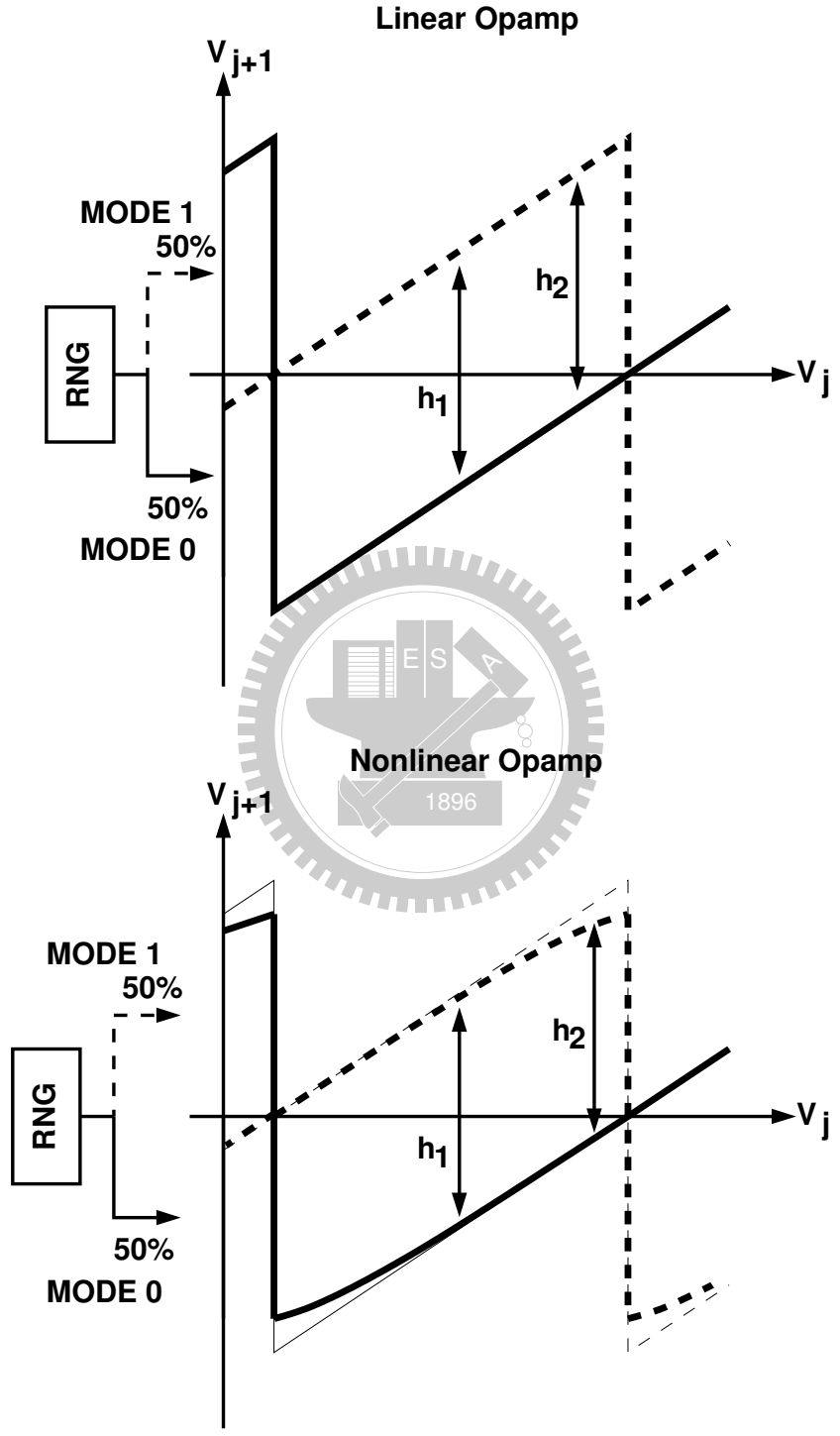



Figure 4.3: Input-output transfer curve for linear and nonlinear opamp.

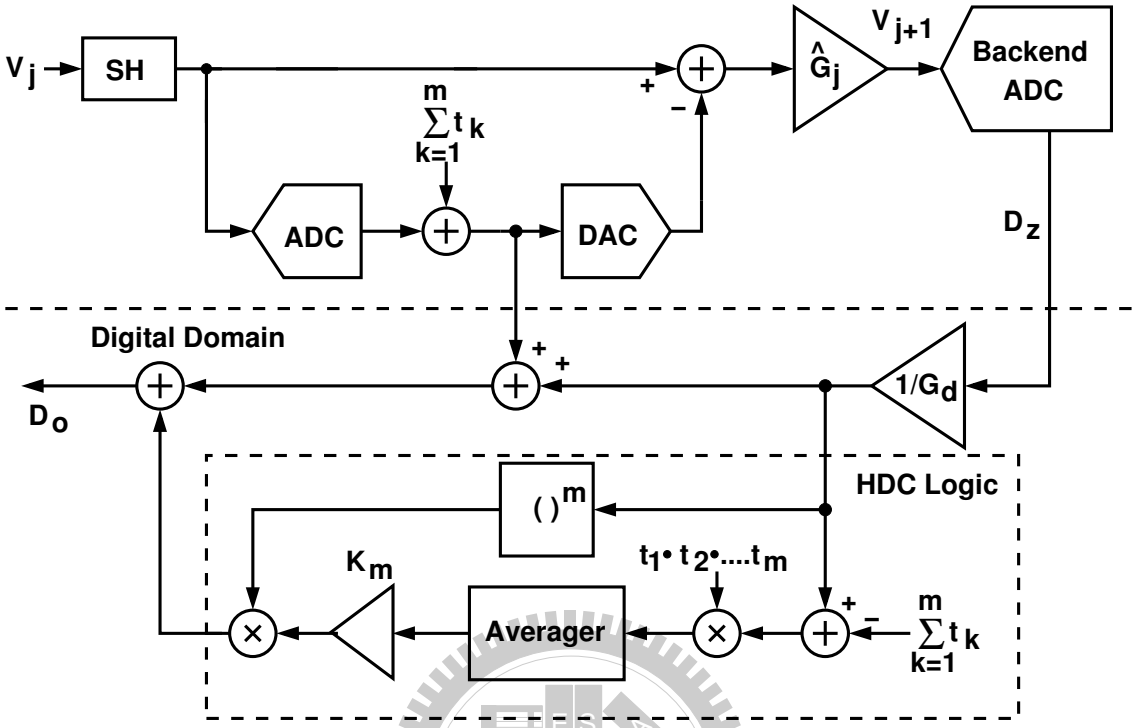



Figure 4.4: Correlation-based nonlieanr detection technique.

output may suffer from large output distortion and the distances $h_1$ and $h_2$ are unequal. By estimating the distances $h_1$ and $h_2$, and comparing the difference of them, the distortion coefficients can be detected. However, this technique can't operate properly under a static signal, because there are not have enough information to generate different $h_1$ and $h_2$.

### 4.3.2 Harmonic Distortion Correction

A correlation-based technique is proposed to extract the harmonic distortion coefficients[9, 39]. $k$ different PN signals, $t_1$, $t_2$, $\cdots$, $t_k$, are injected before the sub-DAC and each of them has a magnitude of $\Delta A$, as shown in Figure 4.4. The PN signals are uncorrelated with each other. Assume that the residue gain is linear and the output $V_{j+1}$ of the residue amplifier is

$$V_{j+1} = Y = \hat{G}_j \cdot \left( V_j - \hat{V}_j^{\mathrm{da}} - \sum_{k=1}^{m} t_k \right) \tag{4.4}$$

The nonlinear output of the pipeline stage is described by Equation (4.2) and assume the residue amplifier contains third order distortion only for simplicity. The distortion can

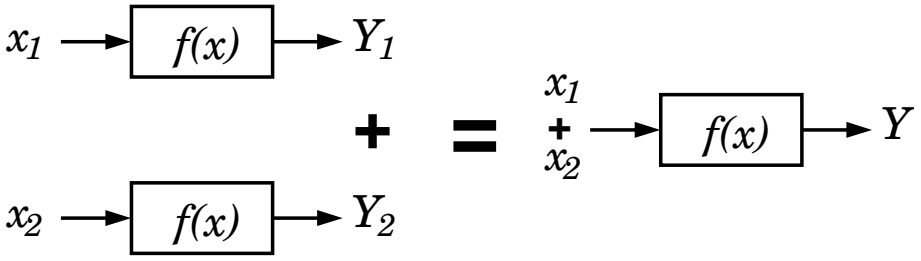



Figure 4.5: Linear system definition.

be calculated by combining Equation (4.2) and Equation (4.4) , and then multiplying $D_z$ with $t_1 \times t_2 \times \cdots \times t_m$. Since the random sequences are zero mean, uncorrelated with each other and independent of the ADC's input signal, then $t_1 \times t_2 \times \cdots \times t_m$ is uncorrelated with other terms in $V_{j+1}$ except the error term $\epsilon$

$$\epsilon = a_3 \times m! \times t_1 \times t_2 \times \cdots \times t_m \tag{4.5}$$

which comes from the harmonic distortion of the residue amplifier. The averager acts as a LPF to filter out the terms that are uncorrelated with $t_1 \times t_2 \times \cdots \times t_m$. The coefficient $k_m$ is used to normalize the error term $\epsilon$ and its value is

$$k_m = \frac{(\Delta A)^{2m}}{m!} \tag{4.6}$$

The nonlinear coefficients $a_3$ is extracted by using Equation (4.5) and Equation (4.6), and for a linear residue amplifier, the error $\epsilon = 0$.

To calibrate k-th order distortion, k random signals should be injected into the pipeline stage. However, the injection signals increase the output swing and also reduce the dynamic range of the pipelined ADC. To calibrate high order distortion, the magnitude $\Delta A$ should be reduced to maintain the dynamic range of the ADC. However, with reduced magnitude, the efficiency of the data extraction is affected. The increasing output swing also worsens the nonlinear distortion and may make the high order distortion in Equation (4.3) un-neglected. This situation is more significant for low voltage technology.

## 4.4 Definition of Linear System

As described in [40], to check a linear system we can apply different signals into the system under detection. By applying different input $x_1$ and $x_2$ into a linear system $f(x)$,

the system generates output $Y_1$ and $Y_2$ respectively, as shown in Figure 4.5. If we apply $x_1 + x_2$ into the system, the linear system should generate a output $Y$, which is the sum of $Y_1$ and $Y_2$. If the output $Y \neq Y_1 + Y_2$, the system is a nonlinear system. Based on the linear system theory, we can determine whether a system is linear or not by simply applying different signal and checking the output of the system.

It's very simple to inject different signals in split-capacitor technique. Random sequences can be injected by using two different capacitors and the two capacitors can also be combined to inject the same random sequence. The can be illustrated in Figure 4.6. The corresponding results are used to detect the nonlinear coefficients. In this figure, we take the extreme case to make this theory more realizable. The distances, $R_{j,ka}$, $R_{j,kb}$ and $R_{j,k}$, between the solid line and the dash line is the magnitude of the injected random sequence. For a linear pipeline stage, $R_{j,ka} + R_{j,kb}$ is equal to $R_{j,k}$. However, for a nonlinear pipeline stage, $R_{j,ka} + R_{j,kb}$ is unequal to $R_{j,k}$. In the following section, we will detail the operation of this calibration technique.

## 4.5 Split-Capacitor SC Stage with Dual $q$

To enable nonlinearity calibration, the pipeline stage of Figure 3.16 is modified and becomes the one shown in Figure 4.7. The only modification done to the AP is that the original $C_{s,6}$ capacitor is split into $C_{s,6a}$ and $C_{s,6b}$. The CP has to generate additional $B_{6a}$ and $B_{6b}$ control signals. When $0 \leq K_j \leq 5$, the CP sets $B_{6a} = B_{6b} = B_6$. The combination of $C_{s,6a}$ and $C_{s,6b}$ is treated as a single $C_{s,6}$ capacitor. The stage acts as a pipeline stage with operation described in Chapter 3. When $K_j = 6$, the stage is configured for nonlinearity calibration. the CP sets $B_{6a} = q_a$ and $B_{6b} = q_b$, while the signal set $\boldsymbol{B} = [B_1, B_2, B_3, B_4, B_5]$ forms a thermometer code of $D_j$. The signals $q_a$ and $q_b$ are two orthogonal random sequences. Their possible values are among $\{-1, 0, +1\}$.

The algorithm which is used to generate the two input-dependent random sequences for $q_a$ and $q_b$ is identical to that described in Section 3.8. Figure 4.8 shows the resulting $V_j$-to-$V_{j+1}$ transfer function. There are 4 different curves for different combination of $q_a$ and $q_b$. The $V_{j+1}$ voltage range is confined between $\pm 0.5V_r$ as long as $V_j$ is within $\pm 7V_r/8$. Maintaining the signal range is crucial for nonlinearity calibration. If a calibration scheme

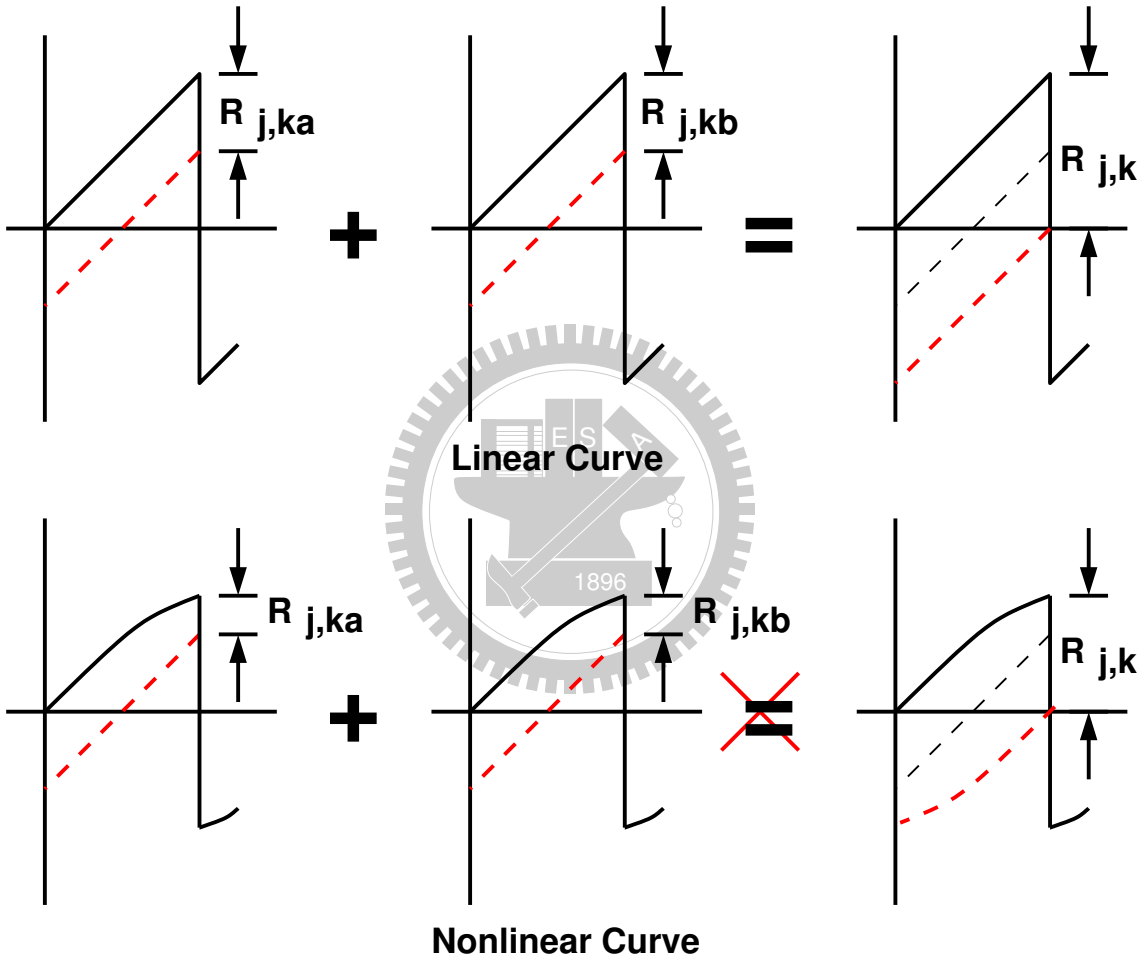



Figure 4.6: Pipeline stage transfer curve with random sequence injection for linear and nonlinear amplifier.

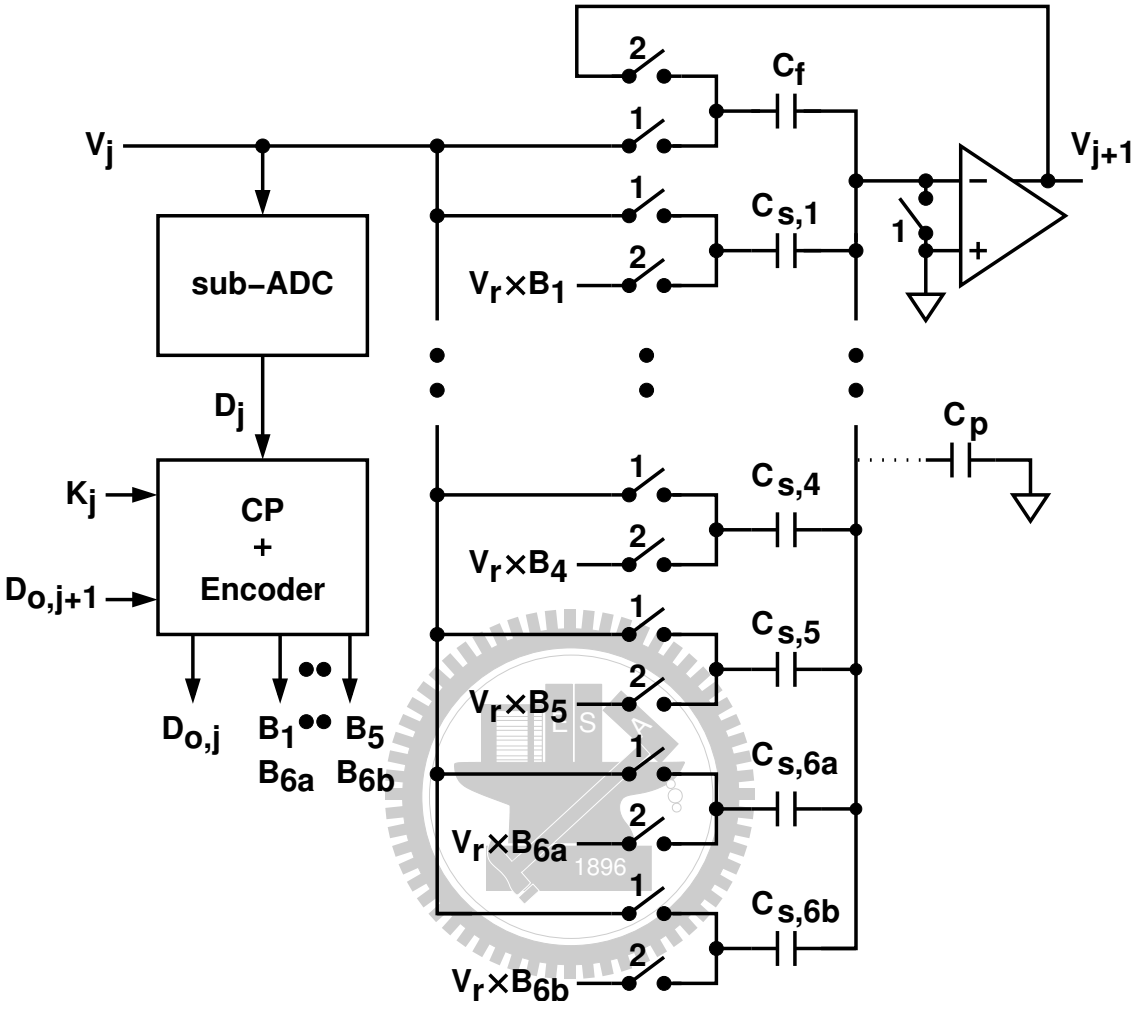



Figure 4.7: A pipeline stage for $b_3$ nonlinearity calibration.

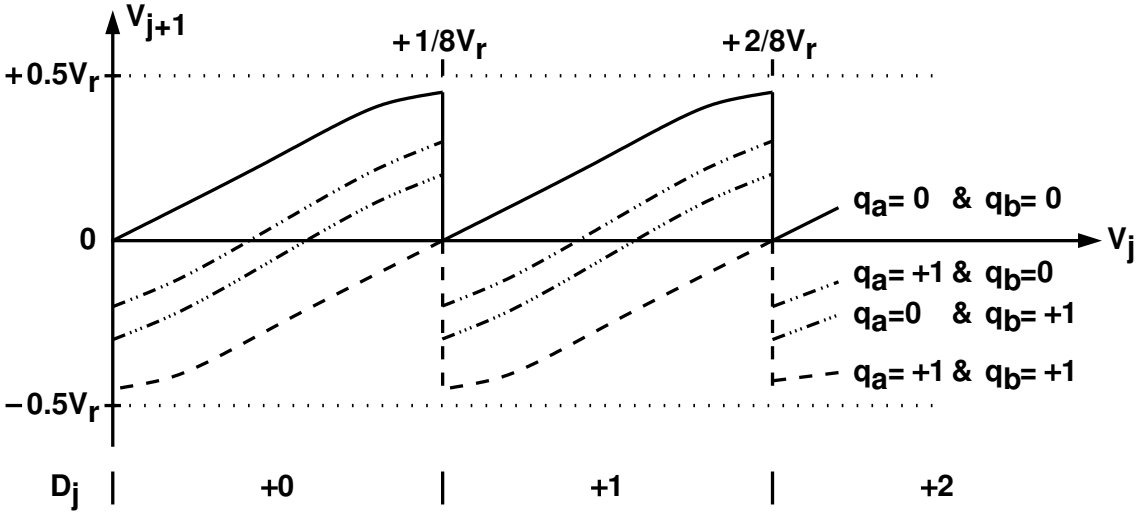



Figure 4.8: Analog transfer fynction of a nonlinear pipeline stage.

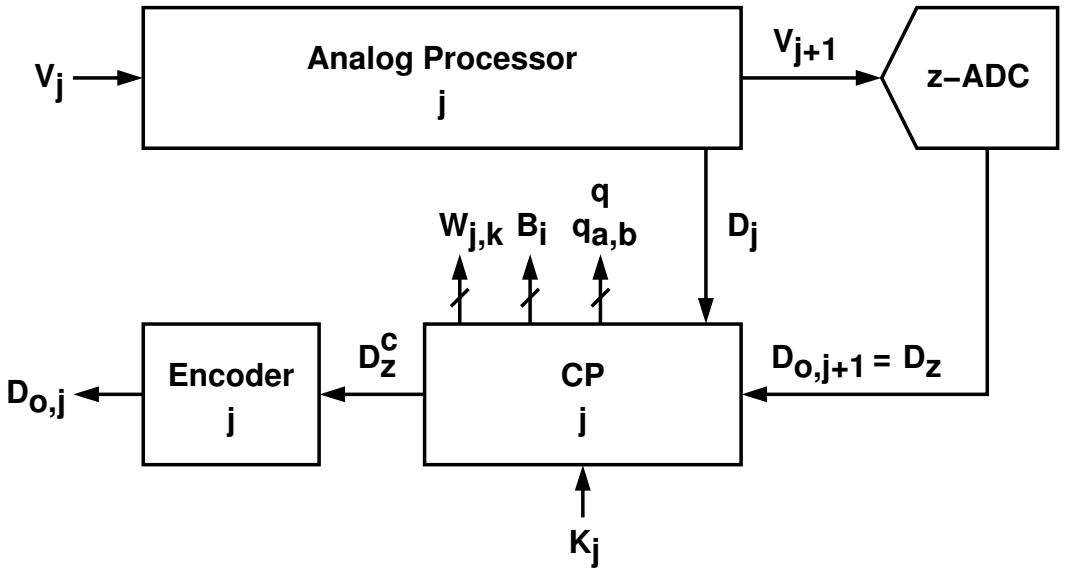



Figure 4.9: Configuration for nonlinearity calibration.

requires an extra signal range, the worsened stage nonlinearity may upset the improvement by the calibration.

If the opamp is linear, then the analog output $V_{j+1}$ can be modified from Equation (3.32) and becomes

$$V_{j+1} = Y \equiv Y' - R_{j,6a} \times q_a - R_{j,6b} \times q_b \tag{4.7}$$

where

$$R_{j,6a} = R_{j,6} \times \frac{C_{s,6a}}{C_{s,6}} \qquad R_{j,6b} = R_{j,6} \times \frac{C_{s,6b}}{C_{s,6}} \tag{4.8}$$

and $Y$ denotes the stage's linear output response. Since $C_{s,6a} + C_{s,6b} = C_{s,6}$, we have

$$R_{j,6a} + R_{j,6b} - R_{j,6} = 0 \tag{4.9}$$

Note that Equation (4.9) is always true and is the criterion for linearity check. Matching between $C_{s,6a}$ and $C_{s,6b}$ is not required.

## 4.6 Calibration Configuration

Figure 4.9 shows the configuration to calibrate and correct the nonlinearity of the $j$-th stage. The nonlinearity of the AP is described by Equation (4.3). Succeeding the $j$-th

stage is a z-ADC. It digitizes $V_{j+1}$ and yields $D_z$. The $V_{j+1}$-to-$D_z$ conversion is assumed to be linear and is simplified as:

$$V_{j+1} = D_z \tag{4.10}$$

Compared with Equation (3.27), the offset $O_z$ of the z-ADC is neglected for the time being. The $1/\hat{G}_z$ conversion gain variation is ignored since it does not affect the calibration procedures as well as the following analyses. The quantization error $Q_z$ is also ignored since it is eliminated during calibration data extraction.

In Figure 4.9, the CP extracts calibration data from $D_z$. The required calibration data include $W_{j,i}$ for $i = 1, 2, \cdots, 6$, as well as $W_{j,6a}$ and $W_{j,6b}$. They stand for the values of $R_{j,i}$, $R_{j,6a}$, and $R_{j,6b}$ digitized by the z-ADC respectively. The CP also corrects the harmonics in $D_z$, yielding a $D_z^c$ such as $D_z^c = Y$. Finally, similar to Equation (3.30), the encoder combines $D_z^c$ and calibration data to calculate $D_{o,j}$ using

$$D_{o,j} = \sum_{i=1}^{5} \left( B_i \times W_{j,i} \right) + B_{6a} \times W_{j,6a} + B_{6b} \times W_{j,6b} + D_z^c \tag{4.11}$$

Note that Equation (4.11) also corrects both stage gain and sub-DAC errors.

## 4.7 Harmonic Correction

Let's assume the $j$-th pipeline stage exhibit a 3rd-order harmonic and, similar to [7, 5], is modeled as:

$$V_{j+1} + b_3 \times V_{j+1}^3 = Y \tag{4.12}$$

The output $V_{j+1}$ is digitized by the z-ADC whose conversion function is Equation (4.10). Figure 4.10 shows the proposed CP. A $b_3$ estimator generates a $\check{b}_3$ output, which approximates the coefficient $b_3$. The $\check{b}_3$ is used to correct $D_z$. The correction is expressed as:

$$D_z^c = D_z + \check{b}_3 \times (D_z)^3 \tag{4.13}$$

By letting $V_{j+1} = D_z^c - \check{b}_3 (D_z)^3$ and $V_{j+1}^3 = (D_z)^3$, Equation (4.12) can be rewritten as:

$$D_z^c + \Delta b_3 \times (D_z)^3 = Y \tag{4.14}$$

where $\Delta b_3 = b_3 - \check{b}_3$.

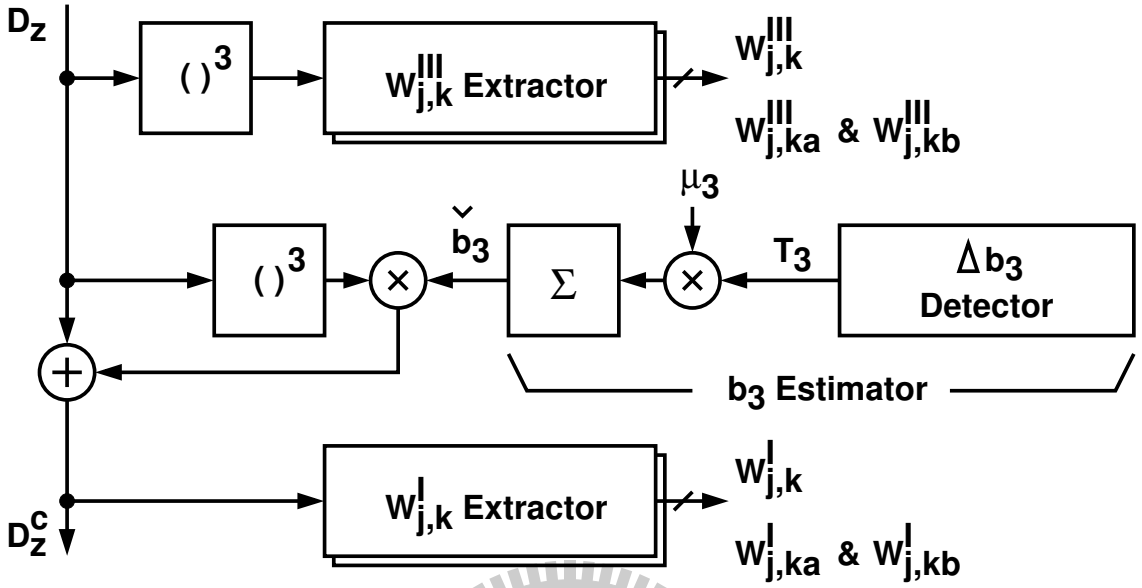



Figure 4.10: Calibration processor for $b_3$ calibration.

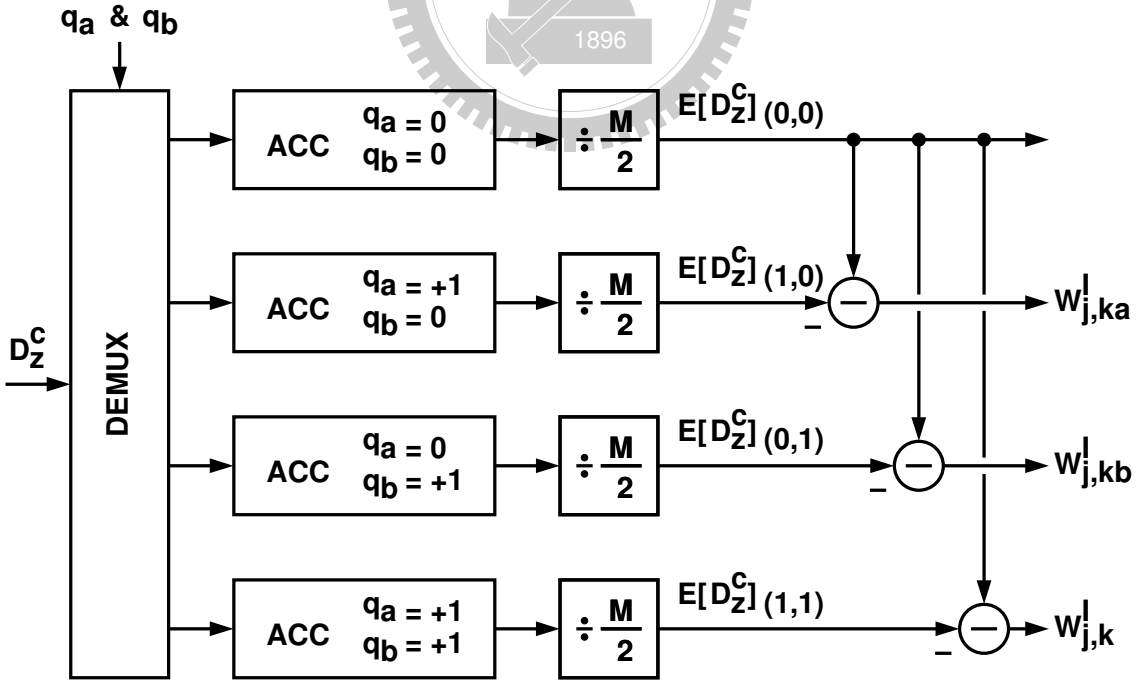
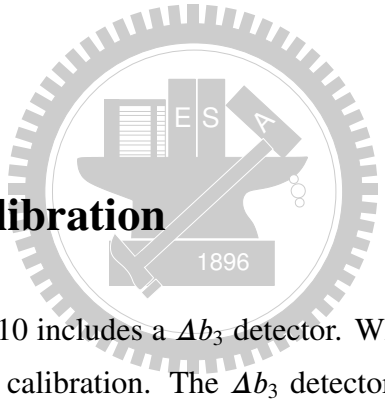



Figure 4.11: A correlation-based dual-$q$ $W^{\mathrm{I}}_{j,k}$ extractor.

If the $b_3$ estimator can generate a $\check{b}_3$ such as $\check{b}_3 = b_3$, then $D_z^c = Y$. The $W_{j,k}^{\mathrm{I}}$ extractor in Figure 4.11 is used to extract the calibration data when $+0 \le D_j \le +5$. This $W_{j,k}^{\mathrm{I}}$ extractor is similar to the one shown in Figure 3.20, except that it collects the $D_z^c$ samples, and sorts the samples according to both $q_a$ and $q_b$ values. It can be easily verified that $W_{j,ka}^{\mathrm{I}}$, $W_{j,kb}^{\mathrm{I}}$, and $W_{j,k}^{\mathrm{I}}$ represent the digitized values of $R_{j,ka}$, $R_{j,kb}$, and $R_{j,k}$ respectively. In our design case, $k = 6$. A similar $W_{j,k}^{\mathrm{I}}$ extractor is used to collect the $D_z^c$ samples when $-5 \le D_j \le -0$. The $W_{j,k}^{\mathrm{I}}$ calibration data are used in the $D_{o,j}$ encoding by applying Equation (4.11) and replacing $W_{j,i}$, $W_{j,6a}$ and $W_{j,6b}$ with $W_{j,i}^{\mathrm{I}}$, $W_{j,6a}^{\mathrm{I}}$ and $W_{j,6b}^{\mathrm{I}}$.

When $K_j = k \le 5$, the pipeline stage is not configured for nonlinearity calibration. However, the harmonic correction continues to operate. The $D_{o,j}$ is encoded using Equation (3.30) with $D_z^c$ replacing $D_z$. The extractor of Figure 3.20 is used to extract $W_{j,k}$ by collecting the $D_z^c$ samples.



## 4.8 Harmonic Calibration

The $b_3$ estimator in Figure 4.10 includes a $\Delta b_3$ detector. When $K_j = k = 6$, the pipeline stage undergoes nonlinearity calibration. The $\Delta b_3$ detector produces a $T_3$ that approximates $\Delta b_3$. The estimator output, $\check{b}_3$, is updated by adding the $\mu_3 \times T_3$ product, where $\mu_3 \le 1$ is a constant. This $b_3$ calibration loop is to minimize $|\Delta b_3|$.

The theory of harmonic detection is described as follows. Consider the $j$-th pipeline stage of Figure 4.7. Its output is modeled as Equation (4.12). When $K_j = k = 6$, The two capacitors, $C_{s,ka}$ and $C_{s,kb}$, are controlled by the random sequences $q_a$ and $q_b$ respectively. The $b_3$ estimator in the CP of Figure 4.10 needs to detect $\Delta b_3 = b_3 - \check{b}_3$.

Combining Equation (4.14) and Equation (4.7), we have

$$D_z^c + \Delta b_3 \times D_z^3 = Y' - R_{j,ka} \times q_a - R_{j,kb} \times q_b \tag{4.15}$$

Averaging Equation (4.15) under different $(q_a, q_b)$ conditions, i.e., $(q_a, q_b) = (0, 0), (1, 0),$

(0, 1), and (1, 1), we obtain the following 4 equations:

$$E\left[D_z^c\right]_{(0,0)} + \Delta b_3 \times E\left[(D_z)^3\right]_{(0,0)} = E[Y'] \tag{4.16}$$

$$E\left[D_z^c\right]_{(1,0)} + \Delta b_3 \times E\left[(D_z)^3\right]_{(1,0)} = E[Y'] - R_{j,ka} \tag{4.17}$$

$$E\left[D_z^c\right]_{(0,1)} + \Delta b_3 \times E\left[(D_z)^3\right]_{(0,1)} = E[Y'] - R_{j,kb} \tag{4.18}$$

$$E\left[D_z^c\right]_{(1,1)} + \Delta b_3 \times E\left[(D_z)^3\right]_{(1,1)} = E[Y'] - R_{j,k} \tag{4.19}$$

where $E\left[D_z^c\right]_{(q_a,q_b)}$ denotes the average of the $D_z^c$ samples under different $(q_a, q_b)$ conditions, and $E\left[(D_z)^3\right]_{(q_a,q_b)}$ denotes the average of the $(D_z)^3$ samples under different $(q_a, q_b)$ conditions. Applying Equation (4.16) −Equation (4.17), Equation (4.16) −Equation (4.18), Equation (4.16) −Equation (4.19), we can write the following equations:

$$W_{j,ka}^{\mathrm{I}} + \Delta b_3 \times W_{j,ka}^{\mathrm{III}} = R_{j,ka} \tag{4.20}$$

$$W_{j,kb}^{\mathrm{I}} + \Delta b_3 \times W_{j,kb}^{\mathrm{III}} = R_{j,kb} \tag{4.21}$$

$$W_{j,k}^{\mathrm{I}} + \Delta b_3 \times W_{j,k}^{\mathrm{III}} = R_{j,k} \tag{4.22}$$

with

$$W_{j,ka}^{\mathrm{I}} \equiv E\left[D_z^c\right]_{(0,0)} - E\left[D_z^c\right]_{(1,0)} \tag{4.23}$$

$$W_{j,kb}^{\mathrm{I}} \equiv E\left[D_z^c\right]_{(0,0)} - E\left[D_z^c\right]_{(0,1)} \tag{4.24}$$

$$W_{j,k}^{\mathrm{I}} \equiv E\left[D_z^c\right]_{(0,0)} - E\left[D_z^c\right]_{(1,1)} \tag{4.25}$$

$$W_{j,ka}^{\mathrm{IIII}} \equiv E\left[(D_z)^3\right]_{(0,0)} - E\left[(D_z)^3\right]_{(1,0)} \tag{4.26}$$

$$W_{j,kb}^{\mathrm{IIII}} \equiv E\left[(D_z)^3\right]_{(0,0)} - E\left[(D_z)^3\right]_{(0,1)} \tag{4.27}$$

$$W_{j,k}^{\mathrm{IIII}} \equiv E\left[(D_z)^3\right]_{(0,0)} - E\left[(D_z)^3\right]_{(1,1)} \tag{4.28}$$

Finally, applying Equation (4.20) +Equation (4.21) −Equation (4.22) and Equation (4.9) gives

$$\mathcal{H}_k^{\mathrm{I}} + \Delta b_3 \times \mathcal{H}_k^{\mathrm{III}} = 0 \tag{4.29}$$

The $\mathcal{H}_k^{\mathrm{x}}$ function, where $x \in \{\mathrm{I}, \mathrm{II}, \mathrm{III}, \cdots\}$, is defined as:

$$\mathcal{H}_k^{\mathrm{x}} \equiv W_{j,ka}^{x} + W_{j,kb}^{x} - W_{j,k}^{x} \tag{4.30}$$

As shown in Figure 4.10, the CP requires an additional $W^{\mathrm{III}}_{j,k}$ extractor. This $W^{\mathrm{III}}_{j,k}$ extractor is identical to the $W^{\mathrm{I}}_{j,k}$ extractor shown in Figure 4.11, except it collects the $(D_z)^3$ samples instead of the $D^c_z$ samples. In the CP of Figure 4.10, the $W^{\mathrm{I}}_{j,k}$ extractor collects the $D^c_z$ samples and yields $W_{j,ka}$, $W_{j,kb}$, and $W_{j,k}$ calibration data. The $W^{\mathrm{III}}_{j,i}$ extractor collects the $(D_z)^3$ samples and yields $W^{\mathrm{III}}_{j,ka}$, $W^{\mathrm{III}}_{j,kb}$, and $W^{\mathrm{III}}_{j,k}$ calibration data. Once all calibration data are acquired, the $\Delta b_3$ detector collects the extracted data from both $W^{\mathrm{I}}_{j,k}$ extractor and $W^{\mathrm{III}}_{j,k}$ extractor, then Equation (4.30) is applied to find $\mathcal{H}^{\mathrm{I}}_k$ and $\mathcal{H}^{\mathrm{III}}_k$. Finally, the detector calculates its output $T_3$by using

$$T_3 = -\frac{\mathcal{H}^{\mathrm{I}}_k}{\mathcal{H}^{\mathrm{III}}_k} \tag{4.31}$$

From Equation (4.29), $T_3$ is an estimate of $\Delta b_3$.

To avoid the division operation, Equation (4.31) can be simplified by replacing $\mathcal{H}^{\mathrm{III}}_k$ with the polarity of $\mathcal{H}^{\mathrm{III}}_k$. The $\mu_3$ scaling factor must be small enough so that the resulting $b_3$ calibration loop can converge. However, smaller $\mu_3$ leads to longer converging time.

A practical nonlinear pipeline stage contains higher-order harmonics, such as the $b_5$ term in Equation (4.3). Then Equation (4.29) becomes

$$\mathcal{H}^{\mathrm{I}}_k + \Delta b_3 \times \mathcal{H}^{\mathrm{III}}_k + n = 0 \tag{4.32}$$

where $n$ is a disturbance caused by higher-order harmonics. If Equation (4.31) is used for $T_3$, then the $b_3$ calibration loop still automatically adjusts $\check{b}_3$ to force $\mathcal{H}^{\mathrm{I}}_k = 0$, but $\Delta b_3$ is converged toward $-E[n]/\mathcal{H}^{\mathrm{III}}_k$.

Note that this calibration scheme employs the criterion of Equation (4.9) for linearity test. From this criterion, the $\mathcal{H}^{\mathrm{x}}_k$ functions are defined as Equation (4.30). The entire calibration scheme does not require any component matching.

## 4.9 Multiple Harmonics Calibration

The calibration theory described in Section 4.8 considers only 3rd harmonic distortion only. However, this technique can also be applied to pipeline stage with higher order harmonic distortion. Now, consider a pipeline stage with 3rd and 5th order harmonic

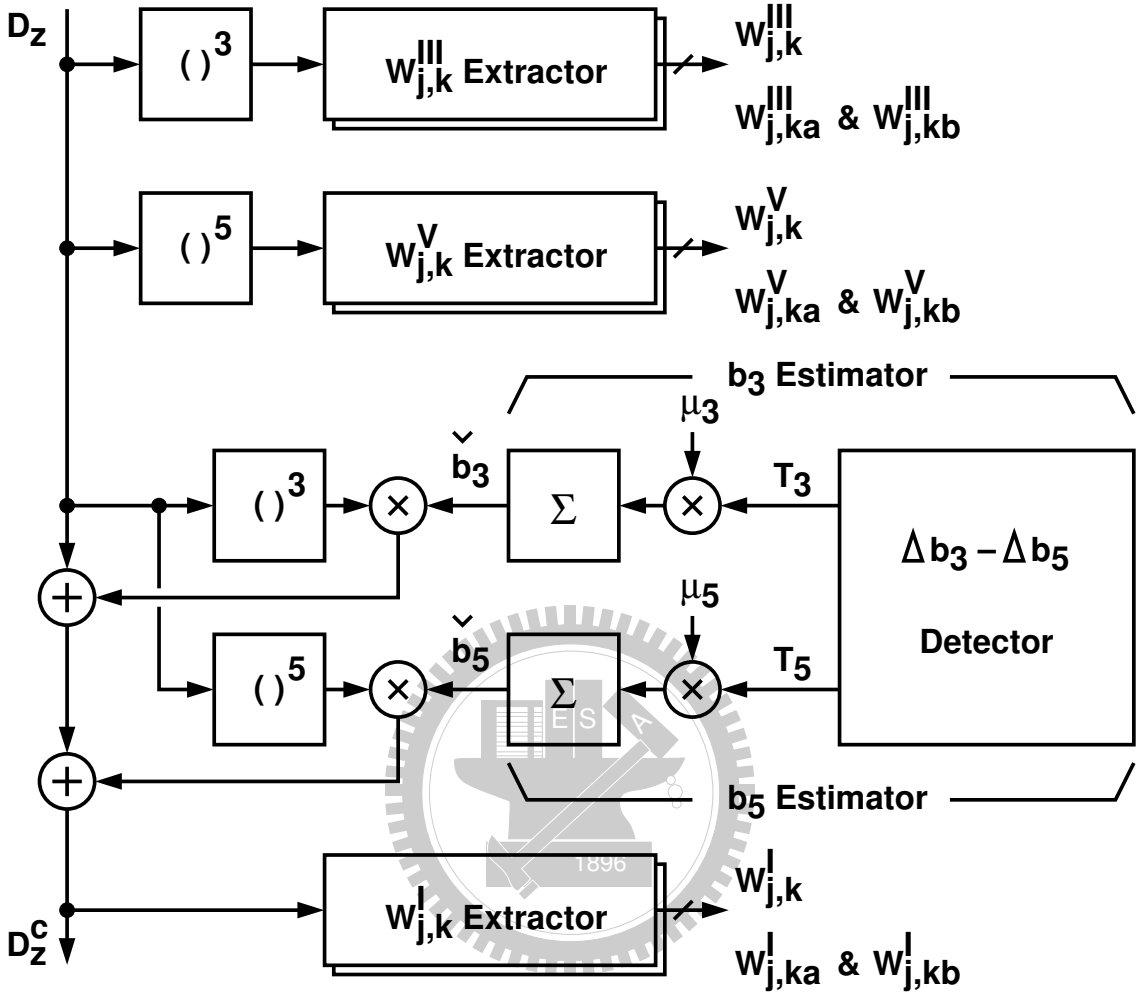



Figure 4.12: Calibration processor for $b_3$ and $b_5$ calibration.

distortion which can be modeled as:

$$V_{j+1} + b_3 \times V_{j+1}^3 + b_5 \times V_{j+1}^5 = Y \tag{4.33}$$

The CP shown in Figure 4.12 can be used to correct both $b_3$ and $b_5$ harmonics. It includes both $b_3$ and $b_5$ estimators, whose outputs are $\check{b}_3$ and $\check{b}_5$ respectively. The corrected $D_z^c$ is calculated by using $D_z^c = D_z + \check{b}_3 (D_z)^3 + \check{b}_5 (D_z)^5$. Following the procedures described in Section 4.7, Equation (4.33) leads to:

$$D_z^c + \Delta b_3 \times (D_z)^3 + \Delta b_5 \times (D_z)^5 = Y \tag{4.34}$$

where $\Delta b_3 = b_3 - \check{b}_3$ and $\Delta b_5 = b_5 - \check{b}_5$. To calibrate $b_5$, the CP adds a $W_{j,i}^{\mathrm{V}}$ extractor, which is also similar to the one shown in Figure 4.11. It collects the $(D_z)^5$ samples and

acquires $W^{\mathrm{V}}_{j,i}$, $W^{\mathrm{V}}_{j,ia}$, and $W^{\mathrm{V}}_{j,ib}$ calibration data.

Consider the pipeline stage of Figure 4.7, in which the $C_{s,6}$ capacitor is split into $C_{s,6a}$ and $C_{s,6b}$. When $K_j = 6$, following the procedures described in Section 4.8, we have

$$\mathcal{H}^{\mathrm{I}}_6 + \Delta b_3 \times \mathcal{H}^{\mathrm{III}}_6 + \Delta b_5 \times \mathcal{H}^{\mathrm{V}}_6 = 0 \tag{4.35}$$

However, one equation is not sufficient to solve for both $\Delta b_3$ and $\Delta b_5$. To obtain another equation, the capacitor $C_{s,5}$ in Figure 4.7 is also split into $C_{s,5a}$ and $C_{s,5b}$. When $K_j = 5$, the two split capacitors are controlled by the sequences $q_a$ and $q_b$. Following the same procedures described in Section 4.8, we have

$$\mathcal{H}^{\mathrm{I}}_5 + \Delta b_3 \times \mathcal{H}^{\mathrm{III}}_5 + \Delta b_5 \times \mathcal{H}^{\mathrm{V}}_5 = 0 \tag{4.36}$$

The two equations, Equation (4.35) and Equation (4.36), are sufficient to solve both $\Delta b_3$ and $\Delta b_5$ unknown parameters.

$$\begin{bmatrix} T_3 \\ T_5 \end{bmatrix} = \begin{bmatrix} \mathcal{H}^{\mathrm{III}}_5 & \mathcal{H}^{\mathrm{V}}_5 \\ \mathcal{H}^{\mathrm{III}}_6 & \mathcal{H}^{\mathrm{V}}_6 \end{bmatrix}^{-1} \times \begin{bmatrix} -\mathcal{H}^{\mathrm{I}}_5 \\ -\mathcal{H}^{\mathrm{I}}_6 \end{bmatrix} \tag{4.37}$$

According to Equation (4.39), when both $b_3$ and $b_5$ loops converge, the relationship between $D^c_z$ and $Y$ is linear.

## 4.10 Calibration under z-ADC Offset

Consider a pipeline stage modeled as Equation (4.12), which includes only a $b_3$ harmonic. Now let the z-ADC exhibit an offset and be modeled as:

$$V_{j+1} = D_z + O_z \tag{4.38}$$

Combining Equation (4.12) and Equation (4.38) gives

$$\frac{O_z + b_3 O_z^3}{1 + 3b_3 O_z^2} + D_z + b'_2 \times (D_z)^2 + b'_3 \times (D_z)^3 = \frac{Y}{1 + 3b_3 O_z^2} \tag{4.39}$$

where

$$b'_2 = \frac{3b_3 O_z}{1 + 3b_3 O_z^2} \qquad b'_3 = \frac{b_3}{1 + 3b_3 O_z^2} \tag{4.40}$$

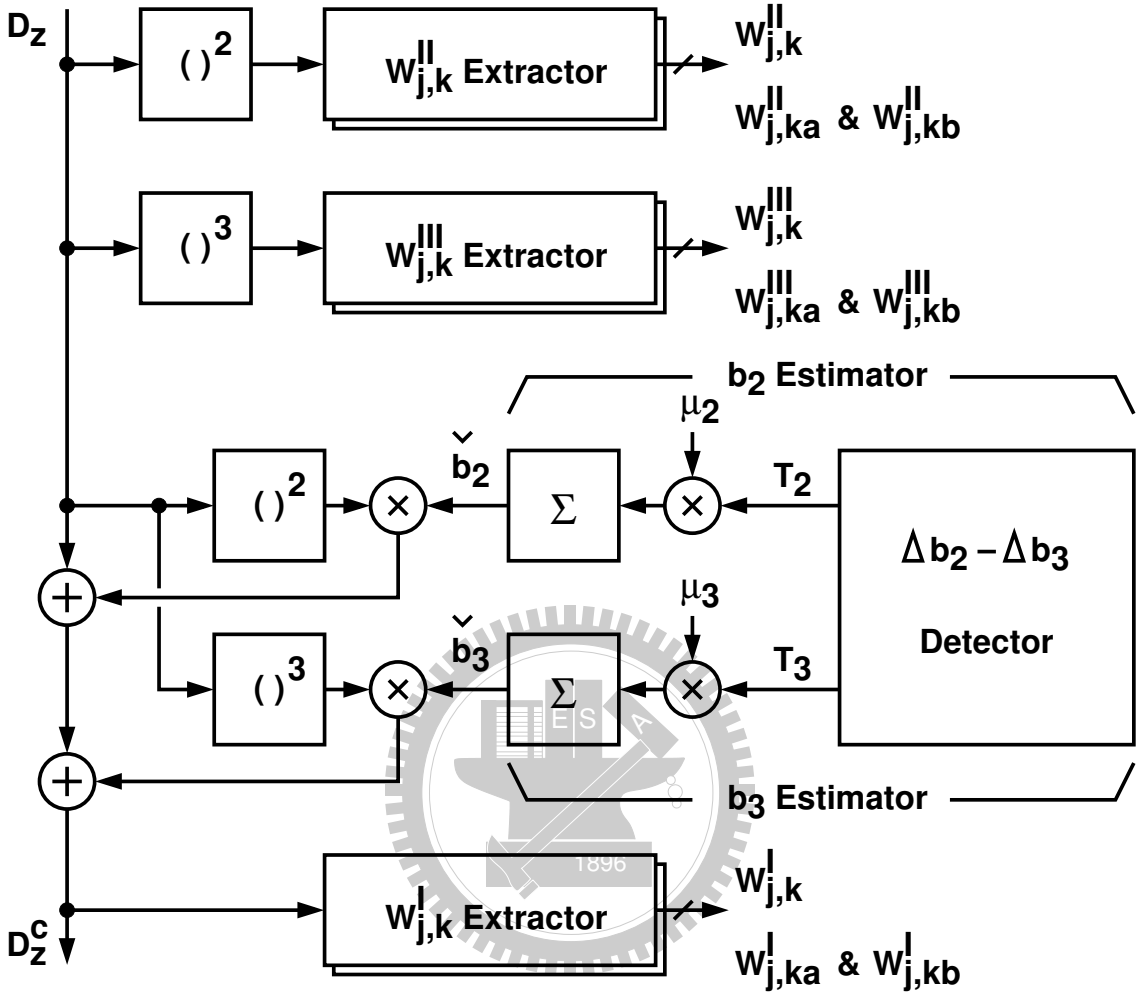



Figure 4.13: Calibration processor for $b_2$ and $b_3$ calibration.

Equation (4.39) shows the effects of $O_z$ with the $j$-th stage nonlinearity. It introduces a 2nd-order harmonic, i.e., the $b_2'$ term. It also changes the gain factor between $D_z$ and $Y$. There are calibration techniques to reduce $O_z$ [10, 41]. But the techniques are required to place a random chopper between the $j$-th stage and the z-ADC.

An alternative is to remove both $b_2'$ and $b_3'$ harmonics in Equation (4.39). The principle of multiple harmonics calibration is detailed in Section 4.9. It requires splitting the capacitors $C_{s,5}$ in Figure 3.16 into $C_{s,5a}$ and $C_{s,5b}$ and splitting the capacitor $C_{s,6}$ into $C_{s,6a}$ and $C_{s,6b}$. The control signals $B_5$ and $B_6$ are replaced by $B_{5a}$, $B_{5b}$, $B_{6a}$, and $B_{6b}$. Similar to the operation described in Section 4.8, when $K_j = 5$, $B_{5a}$ and $B_{5b}$ adopt the values of $q_a$ and $q_b$ respectively, and $B_{6a} = B_{6b} = B_6$. When $K_j = 6$, $B_{6a}$ and $B_{6b}$ adopt the values

of $q_a$ and $q_b$ respectively, and $B_{5a} = B_{5b} = B_5$.

The required CP is shown in Figure 4.13. It includes a $b_2$ estimator and a $b_3$ estimator, whose outputs are $\check{b}_2$ and $\check{b}_3$ respectively. The corrected $D_z^c$ is calculated by using $D_z^c = D_z + \check{b}_2 (D_z)^2 + \check{b}_3 (D_z)^3$. In addition to a $W_{j,k}^{\mathrm{I}}$ extractor and a $W_{j,k}^{\mathrm{III}}$ extractor, the CP also includes a $W_{j,k}^{\mathrm{II}}$ extractor, which collects the $(D_z)^2$ samples and generates $W_{j,ka}^{\mathrm{II}}$, $W_{j,kb}^{\mathrm{II}}$, and $W_{j,k}^{\mathrm{II}}$.

Following the procedures outlined in Section 4.9, when $K_j = 5$, both $\mathcal{H}_5^{\mathrm{II}}$ and $\mathcal{H}_5^{\mathrm{III}}$, as defined in Equation (4.30), are acquired. When $K_j = 6$, both $\mathcal{H}_6^{\mathrm{II}}$ and $\mathcal{H}_6^{\mathrm{III}}$ are acquired. It can be shown as below

$$\begin{aligned} \mathcal{H}_5^{\mathrm{I}} + \Delta b_2' \times \mathcal{H}_5^{\mathrm{II}} + \Delta b_3' \times \mathcal{H}_5^{\mathrm{III}} = 0 \\ \mathcal{H}_6^{\mathrm{I}} + \Delta b_2' \times \mathcal{H}_6^{\mathrm{II}} + \Delta b_3' \times \mathcal{H}_6^{\mathrm{III}} = 0 \end{aligned} \tag{4.41}$$

where $\Delta b_2' = b_2' - \check{b}_2$ and $\Delta b_3' = b_3' - \check{b}_3$ with $\check{b}_2$ and $\check{b}_3$ being the outputs of the $b_2$ and $b_3$ estimators respectively. The $\Delta b_2$-$\Delta b_3$ detector in Figure 4.13 calculates its $T_2$ and $T_3$ outputs by solving the unknown parameters $\Delta b_2'$ and $\Delta b_3'$ in the above equation set, i.e.,

$$\begin{bmatrix} T_2 \\ T_3 \end{bmatrix} = \begin{bmatrix} \mathcal{H}_5^{\mathrm{II}} & \mathcal{H}_5^{\mathrm{III}} \\ \mathcal{H}_6^{\mathrm{II}} & \mathcal{H}_6^{\mathrm{III}} \end{bmatrix}^{-1} \times \begin{bmatrix} -\mathcal{H}_5^{\mathrm{I}} \\ -\mathcal{H}_6^{\mathrm{I}} \end{bmatrix} \tag{4.42}$$

According to Equation (4.39), when both $b_2$ and $b_3$ loops converge, the relationship between $D_z^c$ and $Y$ is linear, but with an unknown offset and an unknown conversion gain factor. The unknowns have no effect on the overall A/D linearity if $D_{o,j}$ is encoded by using Equation (4.11).

If $\mathcal{H}_5^{\mathrm{I}} = \mathcal{H}_6^{\mathrm{I}}$, $\mathcal{H}_5^{\mathrm{II}} = \mathcal{H}_6^{\mathrm{II}}$, and $\mathcal{H}_5^{\mathrm{III}} = \mathcal{H}_6^{\mathrm{IIII}}$, then the equation set of Equation (4.41) is degenerated and cannot be used to solve both $\Delta b_2'$ and $\Delta b_3'$. The above situation can be avoided by making $C_{s,5a}/C_{s,5b} \neq C_{s,6a}/C_{s,6b}$. For example, we can choose $C_{s,5a}/C_{s,5b} = 1/1$ and $C_{s,6a}/C_{s,6b} = 1/3$.

## 4.11 $C_s$ Partition Consideration

The nonlinearity calibration is the most effective if the stage's output randomly spans the entire output range. The proposed calibration scheme can still function for constant stage input. The technique described in the section is to make the calibration more robust.

Consider the calibration processor of Figure 4.13, which calibrates both $b_2$ and $b_3$ harmonic terms. To simplify analysis, consider a pipeline stage with negligible nonlinear terms. It can be modeled as Equation (4.7) with $V_{j+1} = D_z = D_z^c$. Its analog transfer function is shown in Figure 4.8. Let's observe only those $W_{j,k}^x$ extractors that collect samples with corresponding $+0 \le D_j \le +5$. In Equation (4.7), $Y'$ is the stage's output if both $q_a = 0$ and $q_b = 0$. Its value is between 0 and 0.5 if $+0 \le D_j \le +5$, assuming $V_r = 1$. If $Y'$ remains constant during the entire $W_{j,k}^x$ extraction cycle, i.e., a dc $V_j$ stage input, then the corresponding $\mathcal{H}^{\rm II}$ and $\mathcal{H}^{\rm III}$ are:

$$\mathcal{H}^{\rm II} = -\left[R_{j,ia}^2 + R_{j,ib}^2 - R_{j,i}^2\right] \tag{4.43}$$

$$\mathcal{H}^{\rm III} = 3\mathcal{H}^{\rm II} \times Y' - \left[R_{j,ia}^3 + R_{j,ib}^3 - R_{j,i}^3\right] \tag{4.44}$$

Figure 4.14 shows the $\mathcal{H}^{\rm III}/\mathcal{H}^{\rm II}$ ratio versus $Y'$ at various $C_{s,i}$ values, where $C_{s,i} = C_{s,ia} + C_{s,ib}$. It can be shown that the $\mathcal{H}^{\rm III}/\mathcal{H}^{\rm II}$ ratio does not vary with the $C_{s,ia}/C_{s,ib}$ ratio as long as $C_{s,i}$ remains unchanged. In addition, $\mathcal{H}^{\rm III} = 0$ at $Y' = (C_{s,i}/C_s)(V_r/2)$.

Thus, under dc input condition, the calibration scheme described in Section 4.10 will fail if the $C_{s,i}$ values for all $i$ are equal. Equal $C_{s,i}$ leads to identical $\mathcal{H}^{\rm III}/\mathcal{H}^{\rm II}$ ratio, thus degenerating Equation (4.41). Furthermore, all proposed calibration configurations fail if $\mathcal{H}^{\rm III} = 0$.

One solution to avoid the above scenario is to randomly select different value of $C_{s,i}$ for different $W_{j,k}^x$ extraction cycle, thus randomly changing the null $Y'$ position at which $\mathcal{H}^{\rm III} = 0$. For example, let $C_{s,6a} = C_{s,6}/2$ and $C_{s,6b} = C_{s,6c} = C_{s,6}/4$. To complete one stage calibration, all $C_{s,i}$ with $i \in \{1, 2, 3\}$ must be selected separately to do $W_{j,i}^x$ extraction. By randomizing the $i$ sequence, the null $Y'$ position can be randomly switched between $V_r/4$ and $V_r/8$. After one $W_{j,k}^x$ extraction, the acquired calibration data are discarded if the corresponding $\mathcal{H}^{\rm III}/\mathcal{H}^{\rm II}$ is too small. It is advised to make $C_{s,i} \le C_s/2$ for all $i$, to avoid increasing the signal range of the stage's output.

## 4.12 Summary

A digital background calibration for pipelined ADCs is presented. The calibration can correct pipeline stage nonlinearity in addition to gain and sub-DAC inaccuracy. The cal-

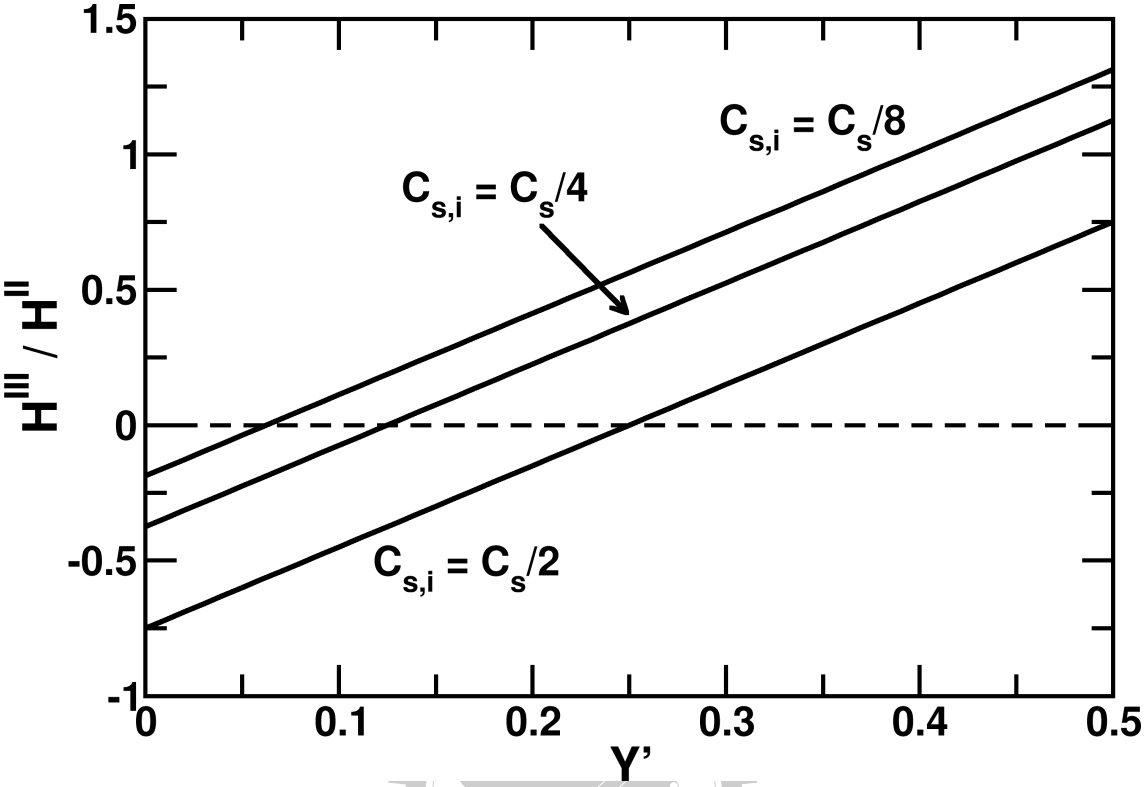



Figure 4.14: $\mathcal{H}^{\mathrm{III}}/\mathcal{H}^{\mathrm{II}}$ versus $Y'$ at various $C_{s,i}$.

ibration can mitigate the accuracy and linearity requirements for pipeline stages, thus reducing analog circuitry's power consumption. Most of the calibration overhead is digital circuitry, whose power consumption and area are scaled along with technology scaling. The calibration requires neither stringent device matching nor extra signal range. The latter is crucial for circuits to operate under low-voltage supply.

Although only a 2.5-bit switched-capacitor pipeline stage is included in the discussions, the proposed technique can be extended and applied to 1.5-bit or multi-bit pipeline stages as well as pipeline stages other than switched-capacitor configuration.

# Chapter 5

# A 12-Bit 80 MS/s Pipelined ADC

## 5.1 Introduction

A 65nm 32-mW 12-bit 80-MS/s pipelined ADC was presented in this chapter. The ADC adopts the techniques described in previous chapters. The circuit architecture and the measurement results are demonstrated. A low power and high speed opamp is also proposed to reduce the power dissipation of the ADC. With proposed calibration technique, the ADC achieves 67 dB SNDR and 81 dB SFDR at 80 MS/s sampling rate with a 2 MHz sinewave input.

## 5.2 Pipelined ADC Architecture

Figure 5.1 shows the architecture of the pipelined ADC. There are five pipeline stages followed by a 4-bit flash ADC. For the $j$-th pipeline stage where $j = 1, \cdots, 5$, its analog processor (AP) receives the analog signal $V_j$ from the $(j-1)$-th stage and generates the analog output $V_{j+1}$. The pipeline stage also includes a digital calibration processor (CP) and an encoder. The digital signal $D_j$ from the AP and the digital signal $D_{o,j+1}$ from the $(j+1)$-th stage are combined to produce the digital output $D_{o,j}$. Their function is to ensure that $D_{o,j}$ is an accurate digital representation of $V_j$.

Figure 5.2 shows the detailed schematic of the pipeline stage for gaib/DAC calibration. The transfer characteristic is shown in Figure 5.3. The AP includes a sub-ADC and

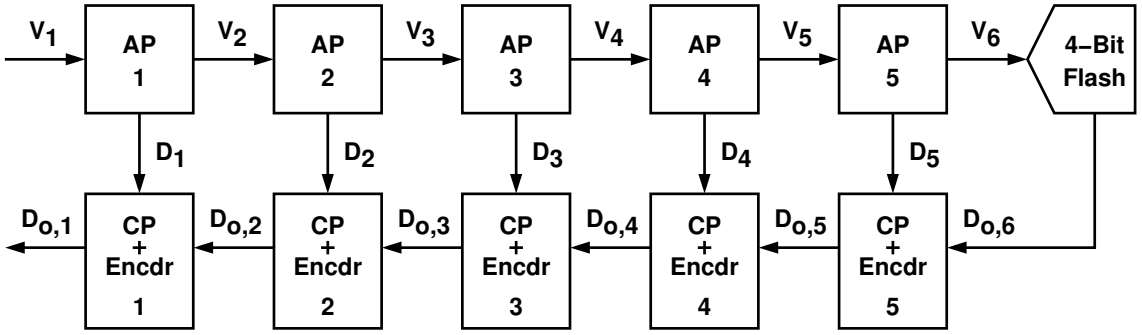



Figure 5.1: Pipelined ADC architecture.

a voltage-mode switched-capacitor circuit that implements the functions of a sub-DAC and a subtracting amplifier. The operation of the pipeline stage is described in Chapter 3. The sub-ADC comprises 13 comparators with thresholds at 0, $\pm V_r/8$, $\pm 2V_r/8V_r$, ..., $\pm 6V_r/8V_r$ respectively. Its digital output, $D_j$, is an estimate of the $V_j$ input. The relationship between $D_j$ and $V_j$ is shown in Figure 5.3. The value of $D_j$ is among $\{\pm 0, \pm 1, \pm 2, \cdots, \pm 6\}$. The two zeros, $-0$ and $+0$, are used to distinguish the polarity of $V_j$. To enable nonlinearity calibration, the pipeline stage of Figure 5.2 is modified and becomes the one shown in Figure 5.4. The original $C_{s,5}$ capacitor is split into $C_{s,5a}$ and $C_{s,5b}$ and the original $C_{s,6}$ capacitor is split into $C_{s,6a}$ and $C_{s,6b}$. The transfer characteristic when dual $q$ are injected into the pipeline stage is shown in Figure 5.5. The operation of the pipeline stage is described in Chapter 4.

An ADC prototype was fabricated using a 65nm 1P6M CMOS technology. The first two pipeline stages employ nonlinearity calibration. They employ the pipeline stage of Figure 5.4 and the CP of Figure 4.13. The next 3 pipeline stages employ only gain and sub-DAC calibration. They employ the pipeline stage of Figure 5.2. When calibration is disabled, the pipeline stage is configured as a conventional 2.5-bit pipeline stage. The last stage is a 4-bit flash ADC with an input range of $\pm V_r$. For the first stage, the total capacitance is $C_s + C_f = 1$ pF. For the second stage, $C_s + C_f = 0.5$ pF. For the next 3 stages, $C_s + C_f = 0.2$ pF. The length of the pseudo-random sequence is $M = 2^{24}$. The updating factors $\mu_2$ and $\mu_3$ shown in Figure 4.13 are adjustable. When they are set to 1, the time required to complete one calibration cycle is about 8 sec at 80 MS/s sampling rate.

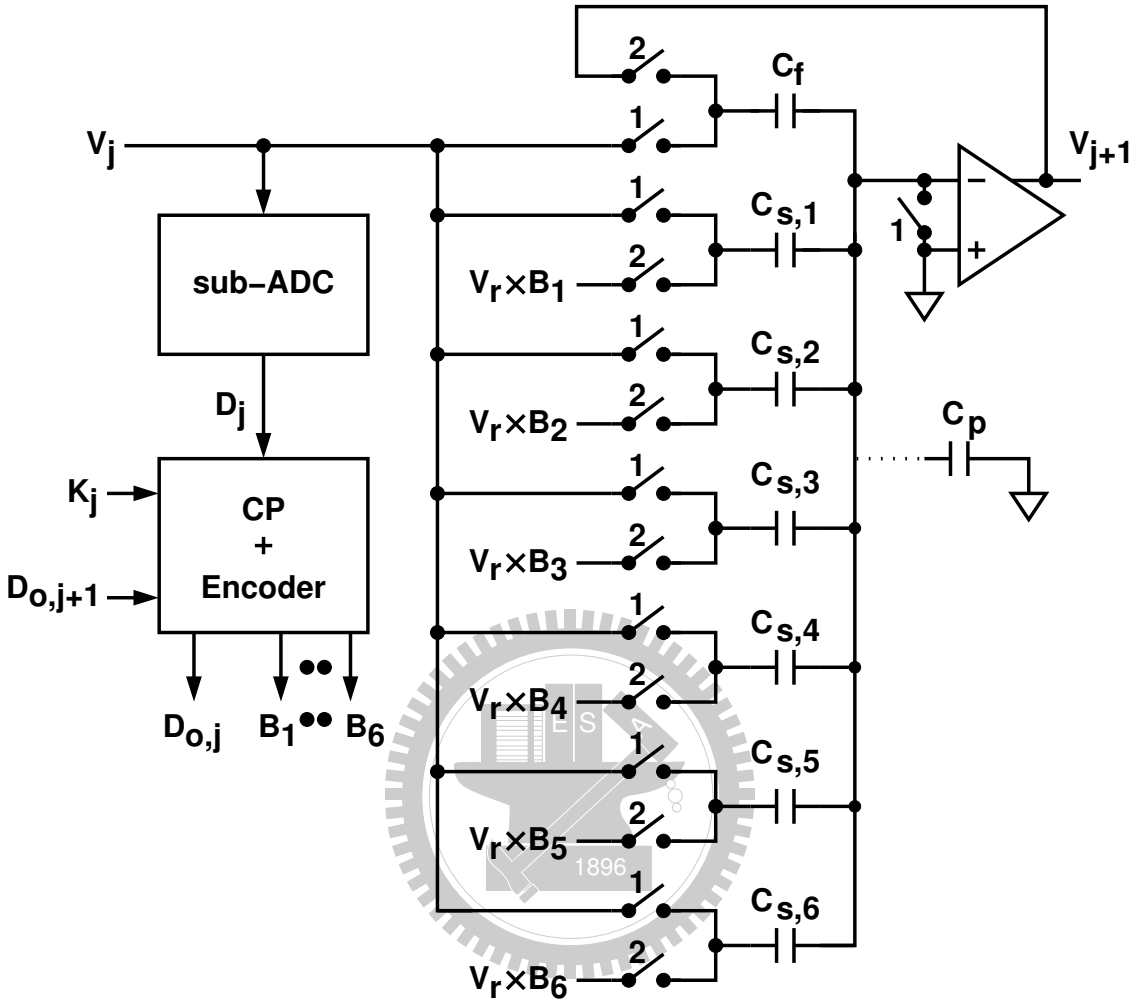



Figure 5.2: Schematic of the pipeline stage for gain/DAC calibration.

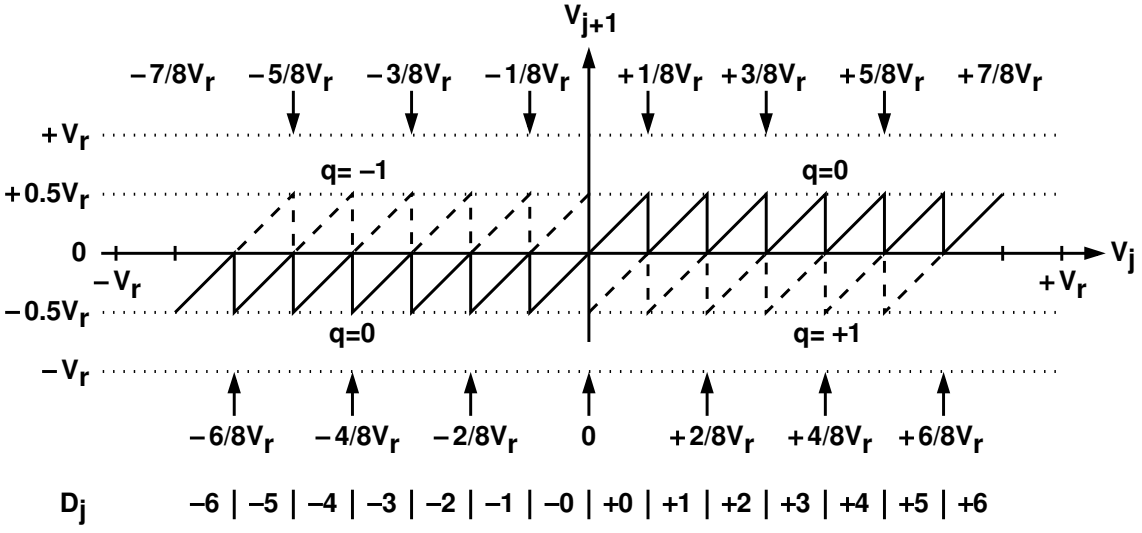



Figure 5.3: Transfer function of Figure 5.2 when random sequence is injected in it.

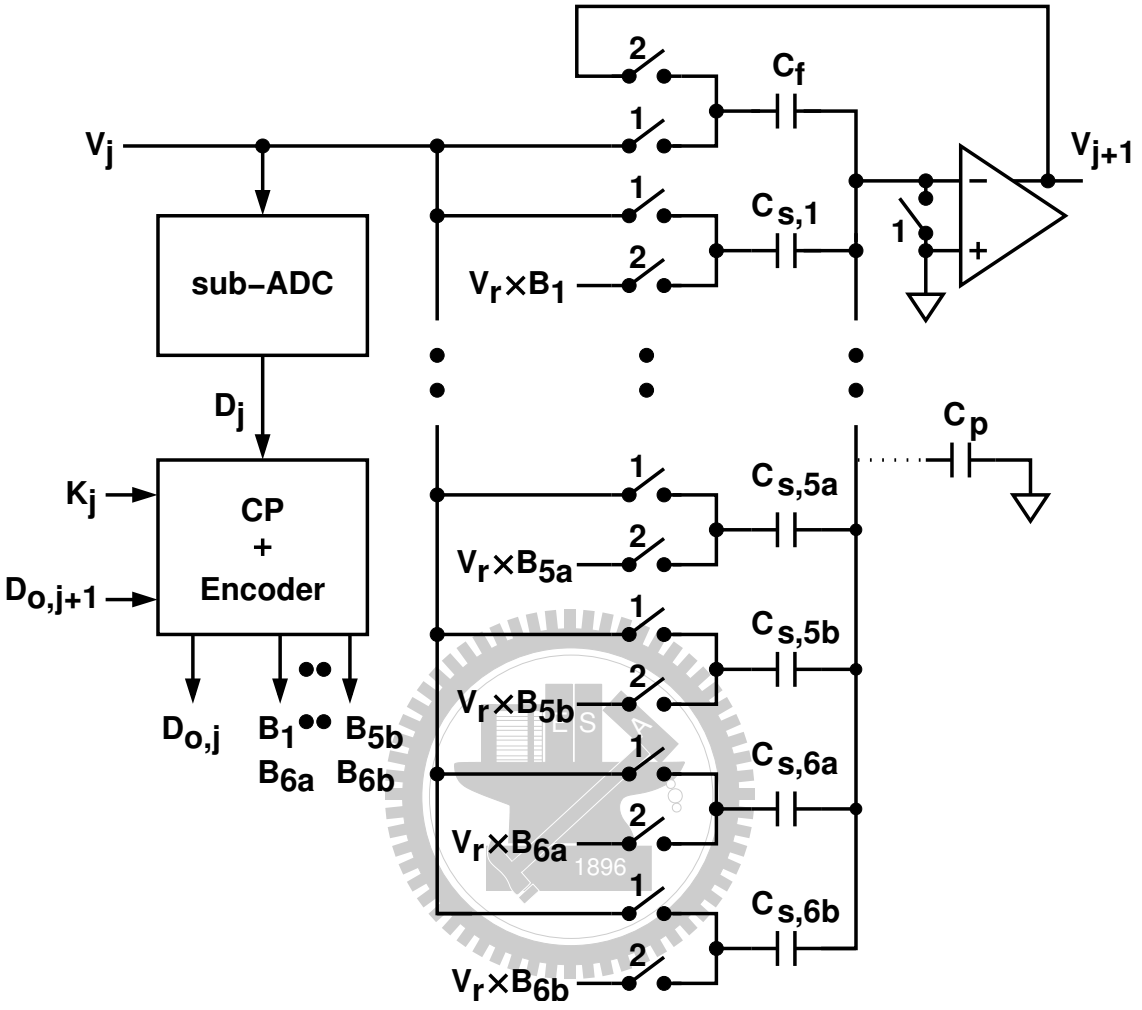



Figure 5.4: Schematic of the pipeline stage for nonlinearity calibration.

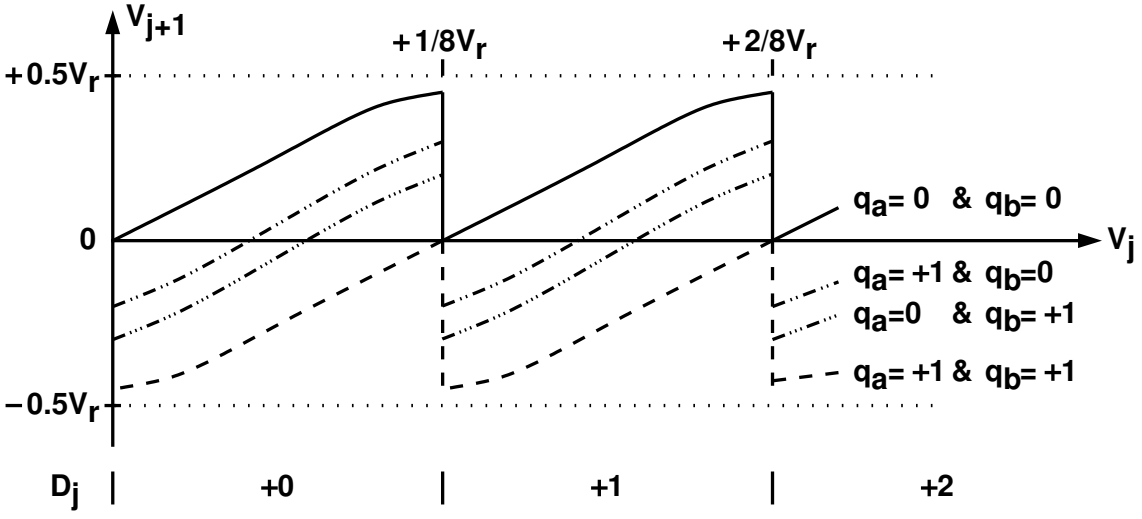



Figure 5.5: Analog transfer function of a nonlinear pipeline stage when $q_a$ and $q_b$ are injected in it.

## 5.3 Circuit Implementation

The main building blocks of a pipelined ADC are input sampling network, operational amplifier and comparator. We will detail the implementation of those circuits in the following section.

### 5.3.1 Bootstrapped Switch

The $R_{on}$ and $C$ sampling network may limit the operation speed of the ADC. For deep-submicron technology, the supply voltage shrinks faster than the threshold voltage. The lower supply voltage increases the turn on resistance and also makes the switch have poor linearity. To achieve a high resolution and high speed ADC, a bootstrapped switch is usually used in the input sampling network to lower the turn on resistance and for better linearity[3, 42]. Figure 5.6 is the bootstrapped circuit used in our design. The circuit provides a constant voltage of $V_{dd}$ across the gate and source of the switch Ms. The boosted voltage $V_A$ at the gate of Ms is

$$V_A = V_i + \frac{C_b}{C_b + C_p} V_{dd} \tag{5.1}$$

where $C_p$ is the parasitic capacitor in node A. Equation (5.1) shows that $C_p$ limits the efficiency of the bootstrapped circuit and $C_b$ must be large enough to reduce effect of the parasitic.

### 5.3.2 Operational Amplifier

According to Section 2.4, high opamp's dc gain is required to achieve a high resolution ADC. However in deep-submicron technology, low supply voltage and low intrinsic gain make high gain opamp not a easy task. Figure 5.7 is the folded opamp which is usually used in low voltage technology. To achieve high gain opamp, cascade amplifiers and frequency compensation technique are used in this architecture. However, these techniques usually increase the power consumption and lower the unit-gain frequency.

Figure 5.8 shows the schematic of the opamp used in the pipeline stage. It is a simple two-stage cascaded amplifier without frequency compensation. It has a dc gain of 35 dB.

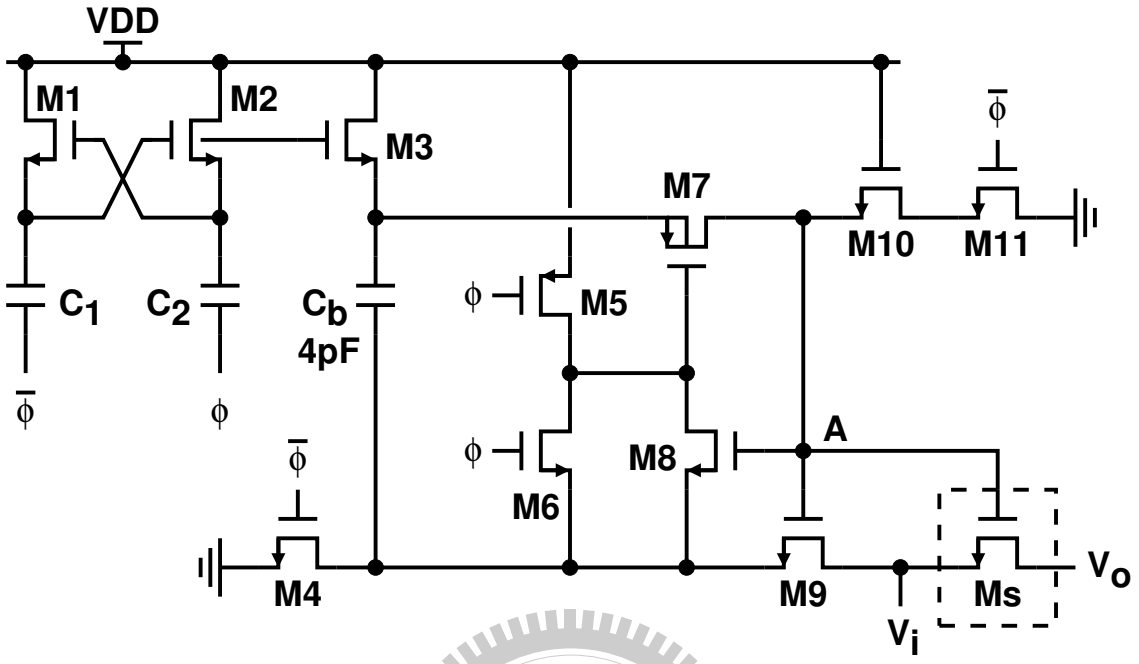



Figure 5.6: Bootstrapped analog switch proposed in [3].

The dominant poles are at the outputs $V_{o,p}$ and $V_{o,n}$. The poles at the drains of M1 and M2 can be pushed away from the unity-gain frequency due to the availability of short-channel MOSFETs. Post-layout simulation shows that the frequency of the non-dominant poles is larger than 2 GHz. The common-mode feedback of the first stage is provided by the R1 and R2 resistors. The second stage employs conventional switched-capacitor common-mode feedback. The unit-gain frequency of this opamp can be approximated to:

$$\omega_u = g_{m1} R_{o,1} \frac{g_{m5}}{C'_{load}} \tag{5.2}$$

Where $R_{o,1} = r_{o,1}//r_{o,3}//R_1$ and $C'_{load}$ is the same as Equation (2.27). $r_{o,1}$ and $r_{o,3}$ are the output impedance of M2 and M3. Identical opamps are deployed in the first four pipeline stages and each consumes 2.9 mW. Using a low-gain opamp introduces gain error and degrades linearity of a pipeline stage. They are corrected by digital calibration. The opamps performance of the pipelined ADC are summaried in Table 5.1.

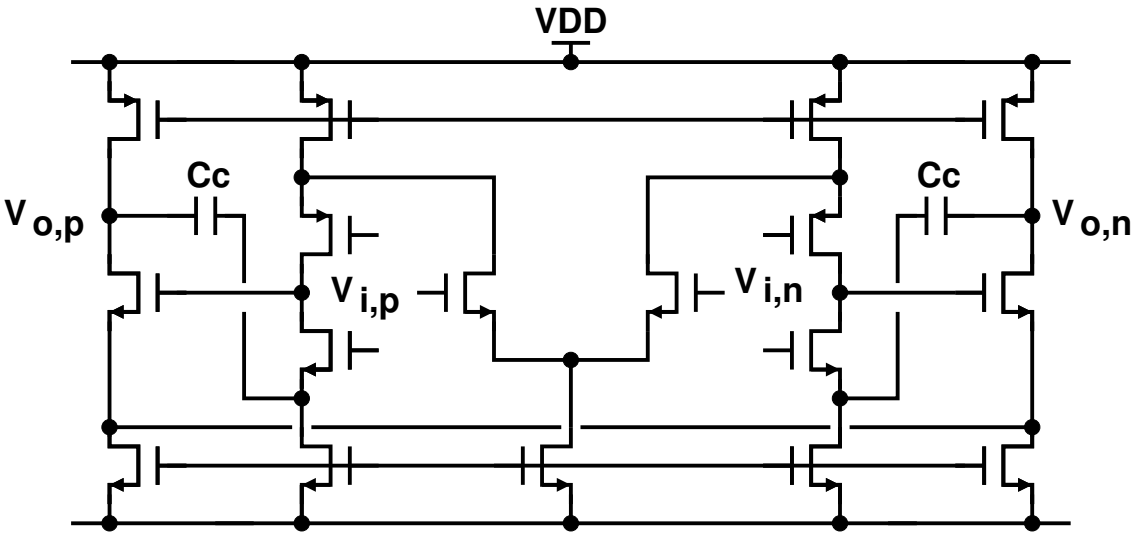



Figure 5.7: Traditional folded-cascode two stage opamp.

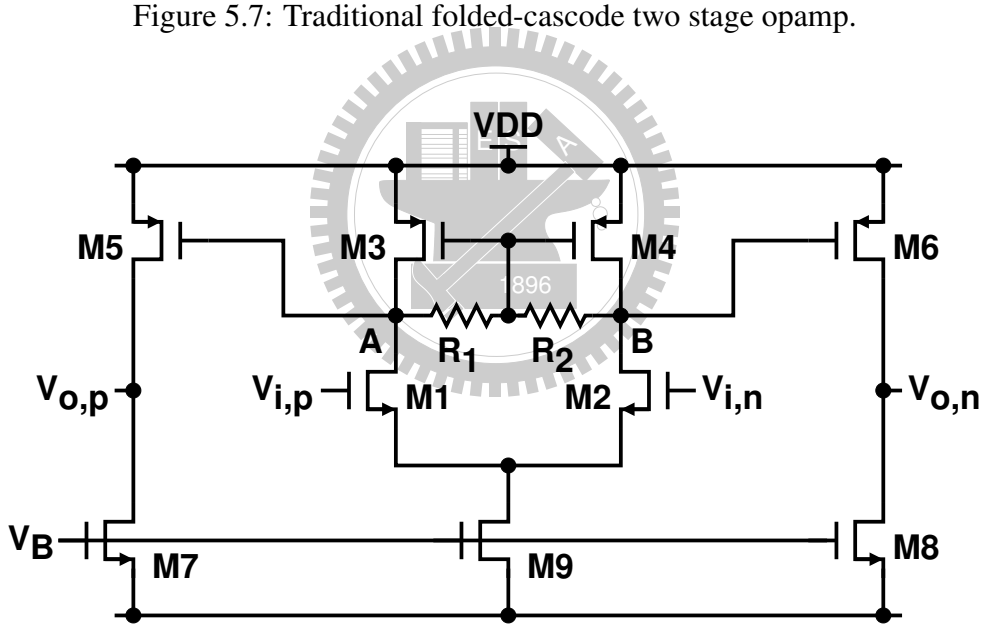



Figure 5.8: Proposed two stage opamp circuit.

Table 5.1: Opamp Performance Summary

| Post Layout Simulation | | | | | |
|---|---|---|---|---|---|
| STG | Power (mW) | $f_u$ (GHz) | $A_v$ dB | $C_s + C_f$ (pF) | $C_L$ (pF) |
| 1 | 2.9 | 1.02 | 35 | 1.0 | 0.5 |
| 2 | 2.9 | 0.99 | 35 | 0.5 | 0.2 |
| 3-4 | 2.9 | 0.97 | 35 | 0.2 | 0.2 |
| 5 | 2.2 | 0.90 | 35 | 0.2 | - |

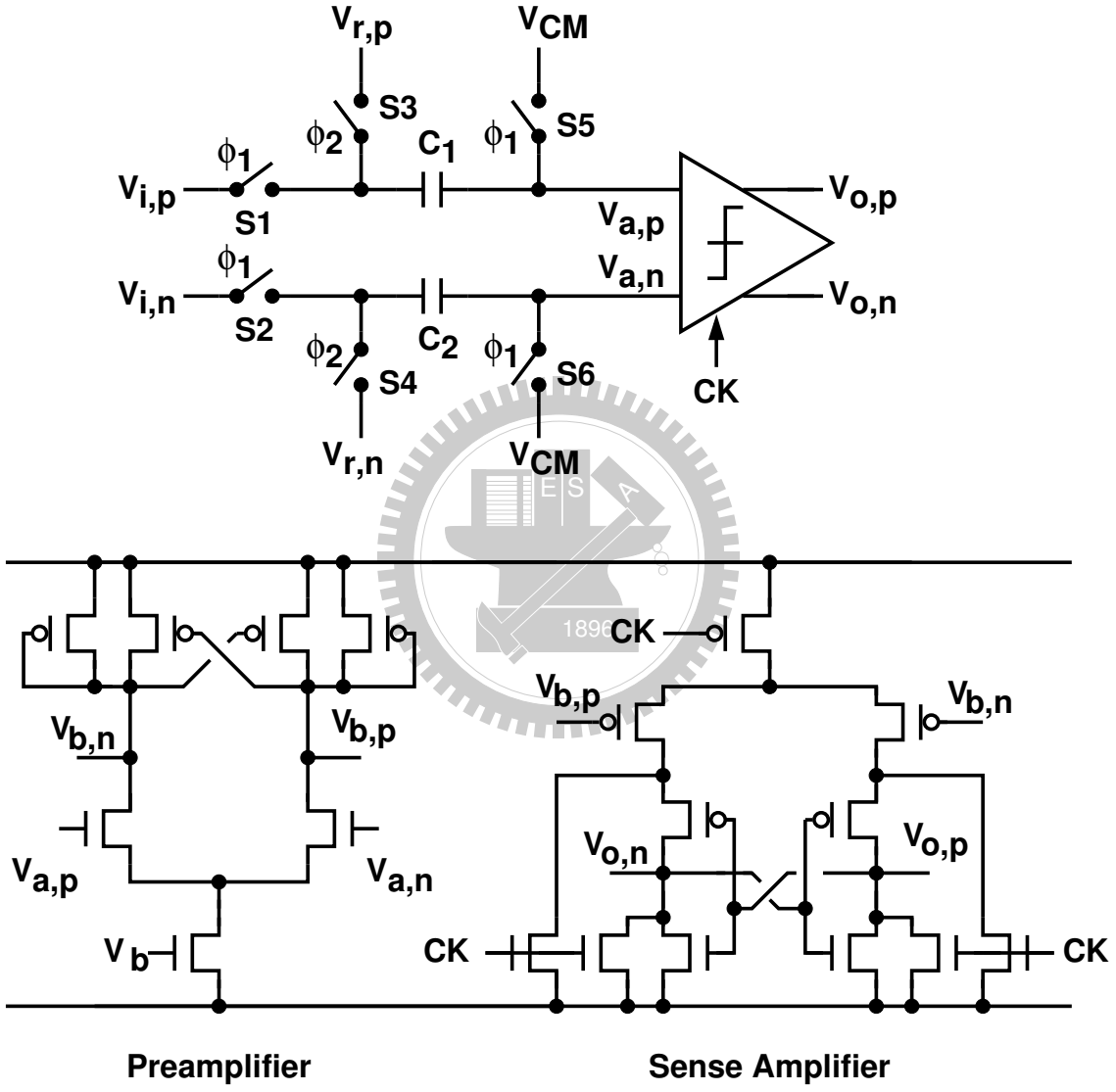



Figure 5.9: Switched-capacitor comparator circuit schematic.

### 5.3.3 Switched-Capacitor Comparator

Figure 5.9 shows the schematic of the comparators of the sub-ADC in the first pipeline stage. The comparator comprises a switched-capacitor input network, a low-gain preamplifier, and a regenerative sense amplifier. The capacitance of both $C_1$ and $C_2$ are 25 fF. For the other pipeline stages, i.e., $j = 2, 3, 4, 5$, the S5 and S6 switches in Figure 5.9 are driven by the clock $\phi_2$. This arrangement can reduce the total input capacitance of a sub-ADC.

The analog input of this ADC is sampled directly by the first pipeline stage. No additional sample-and-hold amplifier is used. because SHA provides no gain but induces additional noise. The sample-and-hold operation of the capacitors $C_s$ and $C_f$ in Figure 4.7 and that of the capacitors $C_1$ and $C_2$ in Figure 5.9 are synchronized. All the $\phi_1$ switches in Figure 4.7 and the S1 and S2 switches in Figure 5.9 are bootstrapped switches. The sub-ADC's total input capacitance in the first pipeline stage is 0.35 pF. The sub-ADC's input capacitance in other pipeline stage is less than 50 fF. Because of the lack of SHA, the matching of the input sampling network between 1st pipeline stage and the comparators is critical. Mismatch of the sampling network degrades the performance at high input frequency [43, 44].

## 5.4 Measurement Results

The testing setup is shown in Figure 5.10. The Analog input is generated by HP 8648C and the clk source is generated by Agilent E4438C. To ensure the signal quality of the analog source, the output of 8648C is filtered by a BPF and then passes through a transformer to achieve single-to-differential conversion. The clk source generates sinesoide waveform and its frequency is $2f_s$.

Figure 5.11 shows the ADC chip micrograph. The core area is $0.92 \times 0.75$ mm$^2$. Digital circuits occupy about 30% of the total area. The digital block and the analog block use separate power lines. The supply voltage is 1.2 V. Operating at 80 MS/s sampling rate, the analog block consumes 26 mW, while the digital block consumes 6 mW. All the voltage references are externally applied.

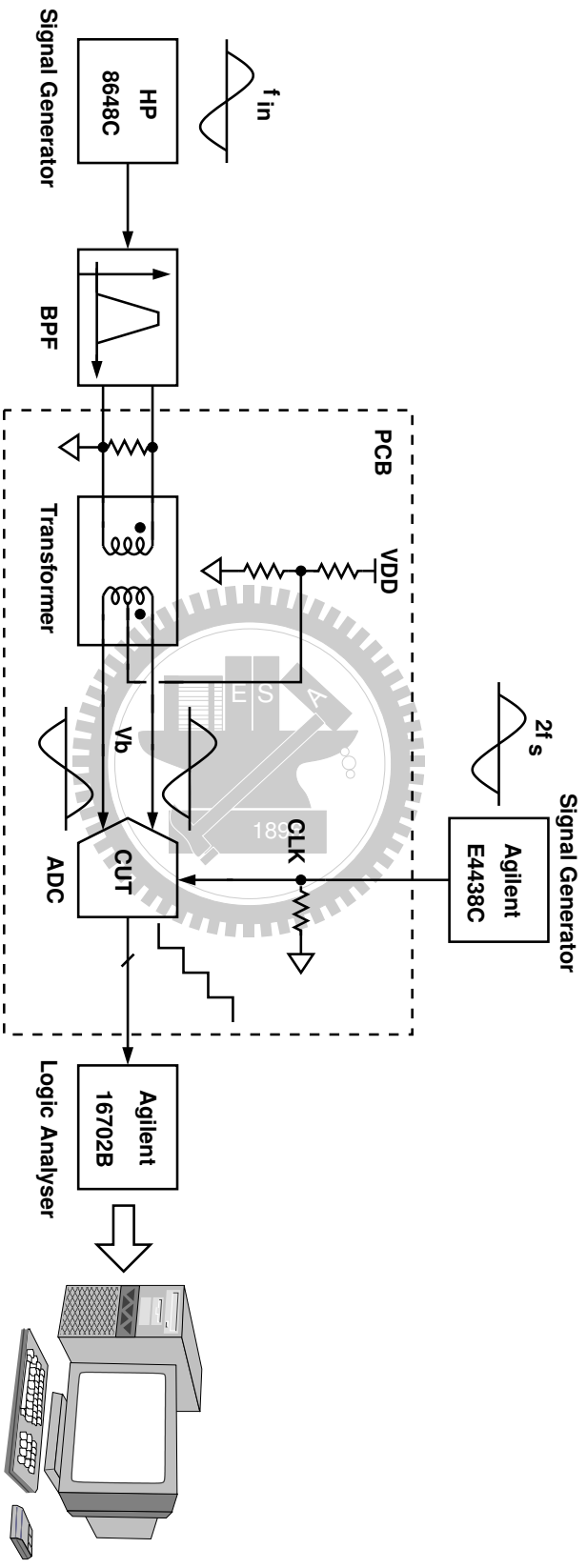



Figure 5.10: Testing enviroment setup.

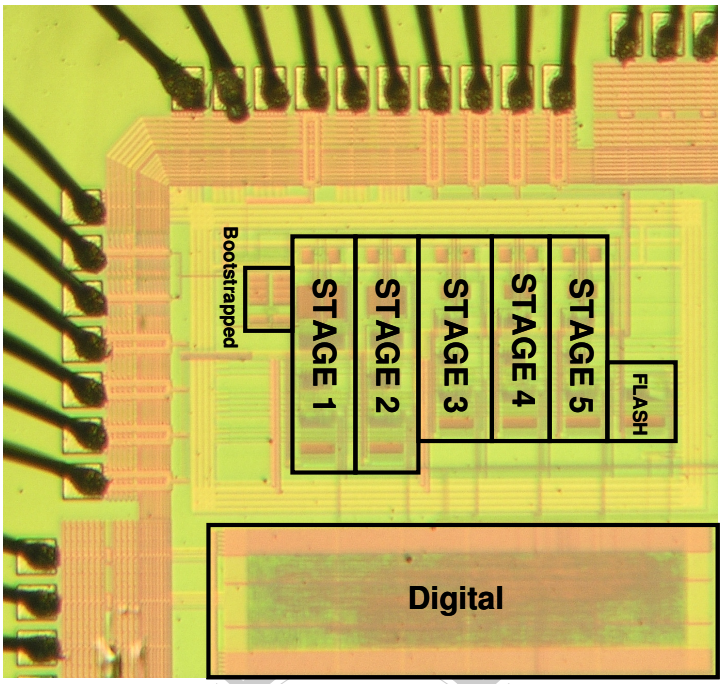



Figure 5.11: Micrograph of the ADC prototype.

Figure 5.12 and Figure 5.13 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC operating at 80 MS/s sample rate with a 2 MHz sinewave input. Before activating the calibration processor, the native DNL is $+1.1/-1.0$ LSB and the INL is $+21.0/-22.2$ LSB. There are missing codes in the digital output. When the Gain/DAC calibration is activated for all pipeline stages, the DNL is reduced to $+0.8/-0.8$ LSB and the INL is reduced to $+7.0/-5.7$ LSB. After the nonlinearity calibration is also enabled for the first two pipeline stages, the DNL is reduced to $+0.7/-0.7$ LSB and the INL is reduced to $+2.4/-1.7$ LSB.

Figure 5.14 shows the ADC's output FFT spectrum at 80 MS/s sampling rate. The input is a 2 MHz differential sinewave with an peak-to-peak amplitude of 2.0 V. Before calibration, the signal to distortion plus noise ratio (SNDR) is 45 dB and the spurious-free dynamic range (SFDR) is 52 dB. After the Gain/DAC calibration is activated for all pipeline stages, the SNDR is improved by 17 dB to 62 dB and the SFDR is improved by 20 dB to 72 dB. After the nonlinearity calibration is also enabled for the first two pipeline stages, the SNDR is further improved to 67 dB and the SFDR is improved to 81 dB. Figure 5.15 shows the ADC's measured SNDR and SFDR versus input frequen-

Table 5.2: Performance Summary

| | |
|---|---|
| Technology | 65nm 1P6M CMOS |
| Supply Voltage ($V_{AA}/V_{DD}$) | 1.2 V / 1.2 V |
| Resolution (bit) | 12 |
| Max. Sampling Rate (MHz) | 80 |
| Input Range ($V_{pp}$) | 2.0 |
| DNL (LSB) | +0.7 / −0.7 |
| INL (LSB) | +2.4 / −1.7 |
| SNDR (dB) @ 2MHz | 67 |
| SFDR (dB) @ 2MHz | 81 |
| THD (dB) @ 2MHz | −71 |
| Power Consumption (mW) | 32 |
| Chip Area ($mm^2$) | 0.92 × 0.75 |

cies at 80 MS/s sampling rate. The calibration can improve the SNDR by more than 20 dB and the SFDR by 30 dB. Figure 5.16 shows the ADC's measured total harmonic distortion (THD) versus input frequencies at 80 MS/s sampling rate. The calibration can improve the THD by more than 20 dB.

Table 5.2 summarizes the measured specifications of this ADC chip. Table 5.3 compares the ADC with the published works that claim to have 12-bit resolution. The figure-of-merit (FOM) is calculated by

$$FOM = \frac{\text{Power}}{2 \cdot ERBW \times 2^{ENOB}} \tag{5.3}$$

ERBW is the effective resolution bandwidth and ENOB is effective number of bits at ERBW.

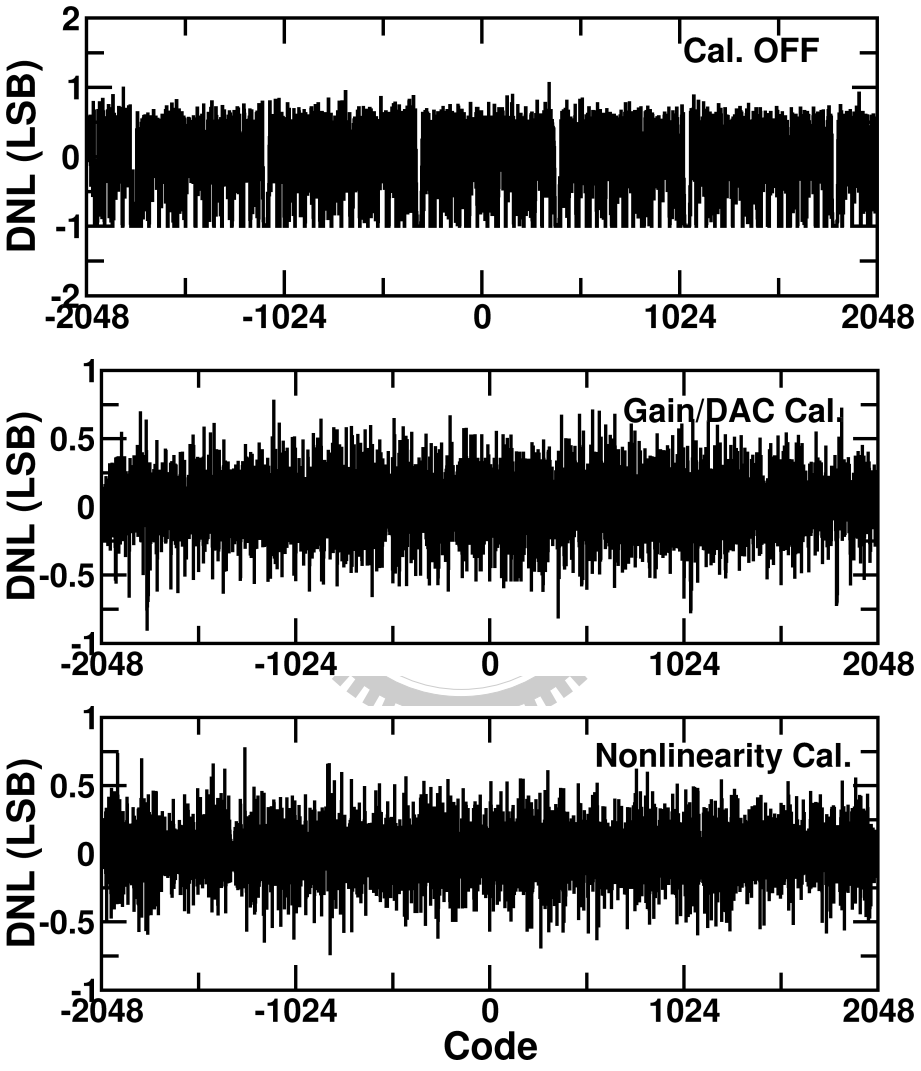



Figure 5.12: Measured DNL performance at 12-bit resolution.

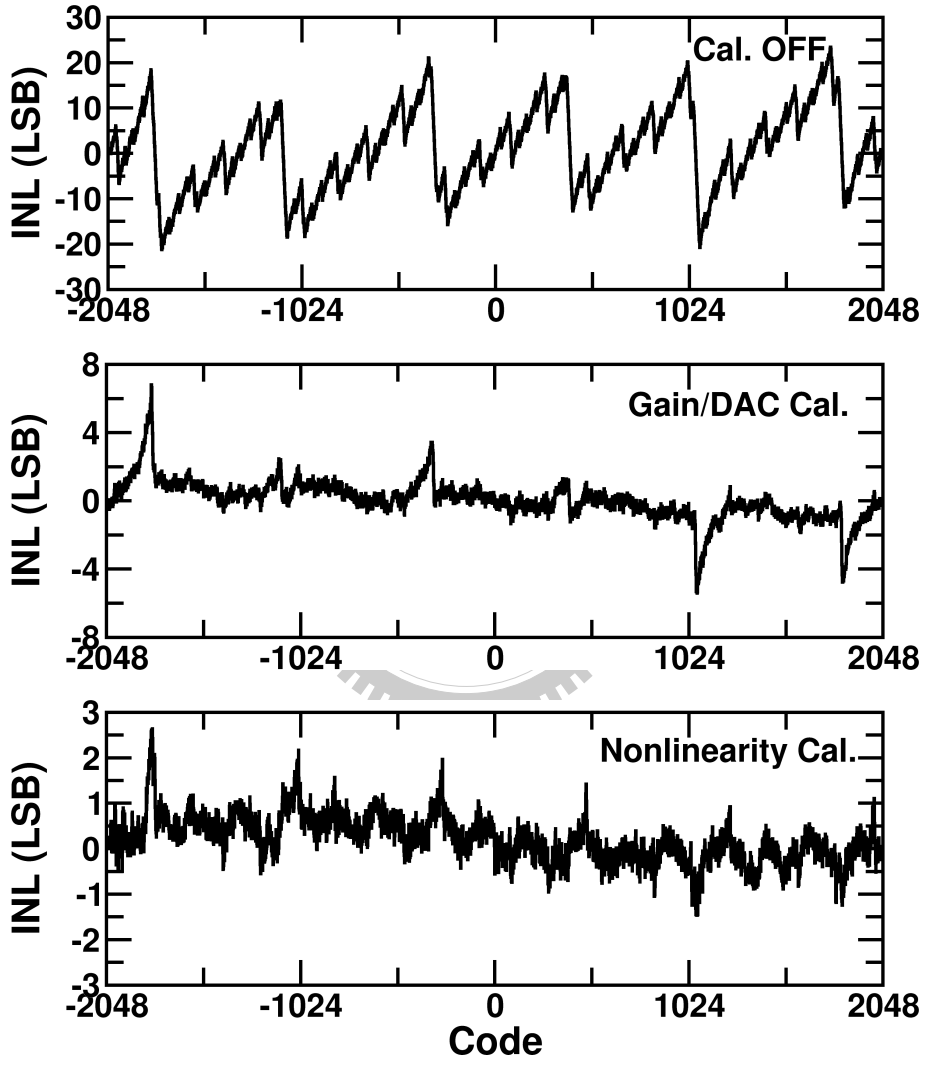



Figure 5.13: Measured INL performance at 12-bit resolution.

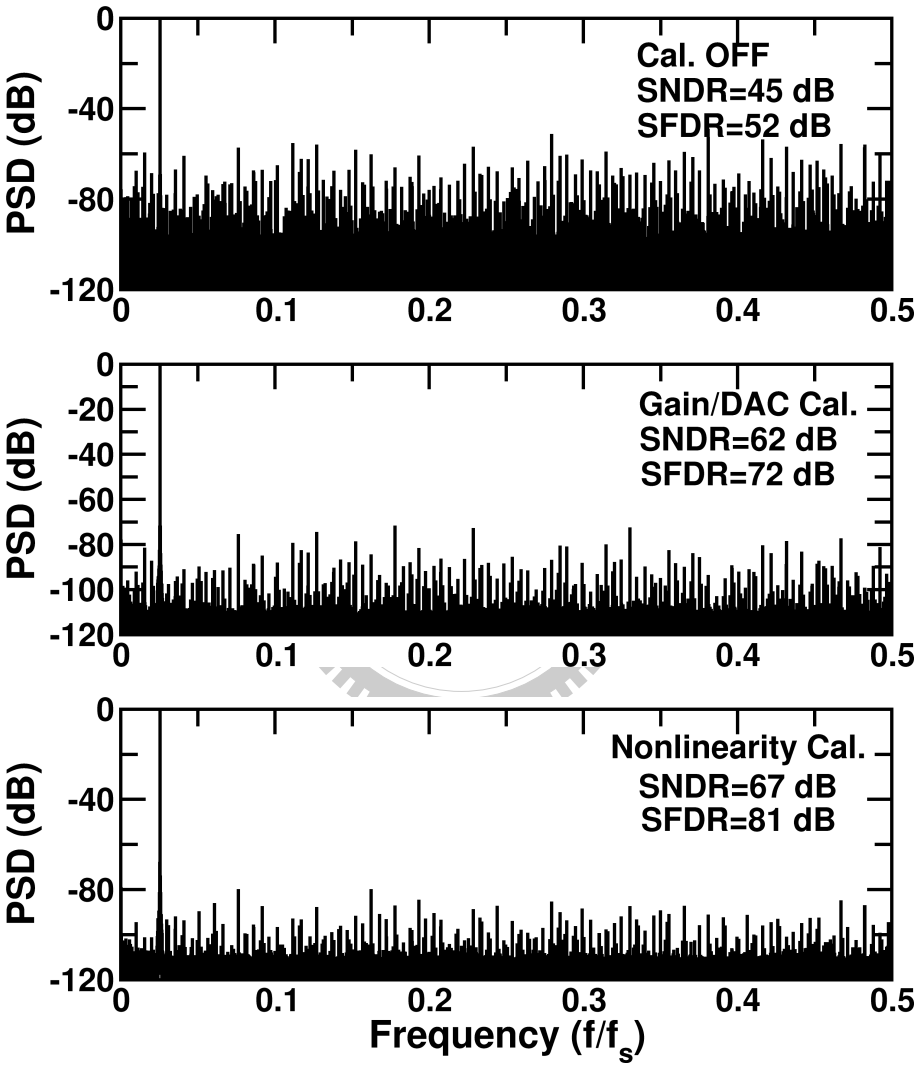



Figure 5.14: Measured FFT spectrum.

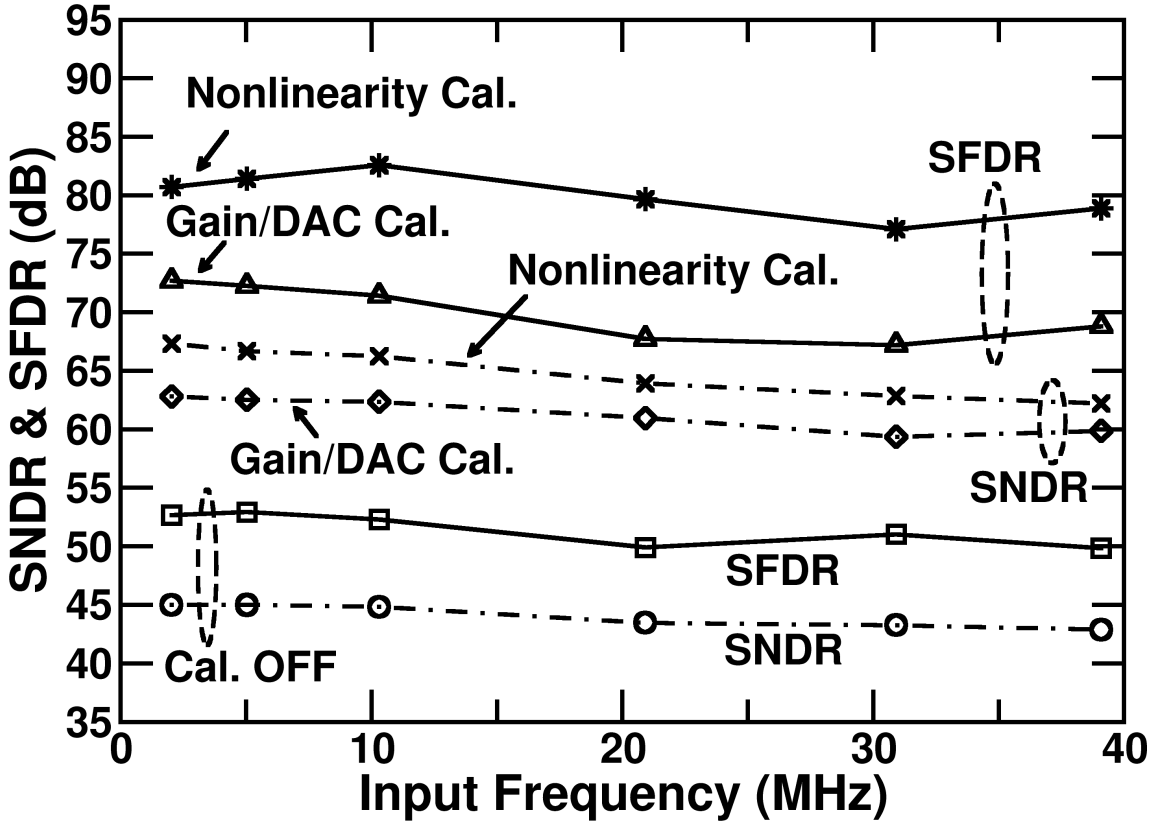



Figure 5.15: Measured SNR and SFDR versus input frequencies with 80MS/s.

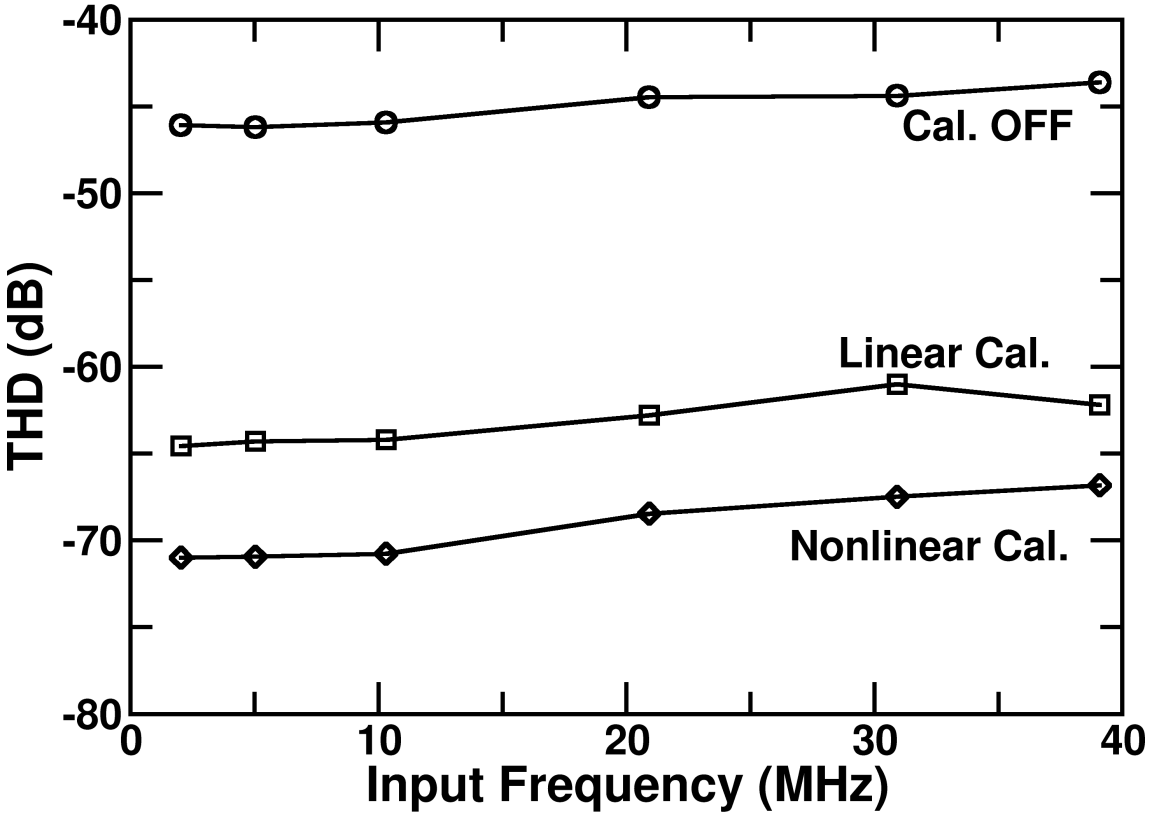



Figure 5.16: Measured THD versus input frequencies with 80MS/s.

## 5.5 Summary

A 32-mW 12-bit 80-MS/s pipelined ADC was fabricated using 65 nm CMOS technology. The ADC demonstrates a new digital background technique, which corrects pipeline stage nonlinearity as well as gain and sub-DAC errors. The calibration technique is robust and immune to device mismatches. The calibration requires neither stringent device matching nor extra signal range. Since the accuracy and linearity requirements are mitigated, analog circuits with less complexity and power can be used. The ADC achieves 67 dB SNDR and 81 dB SFDR at 80 MS/s sampling rate with a 2 MHz sinewave input.

Table 5.3: 12-bit Nyquist-rate ADC

| Year | This Work | [39] | [45] | [46] | [47] | [48] | [49] | [50] | [5] | [51] |
|---|---|---|---|---|---|---|---|---|---|---|
| CMOS Technology (nm) | 65 | 90 | 90 | 180 | 90 | 90 | 250 | 180 | 350 | 180 |
| Supply Voltage (V) | 1.2 | 1.2 | 1.2 | 1.8 | 1.0 | 1.2 | 2.5 | 1.8 | 3.0 | 3.0 |
| Power (mW) | 32 | 130 | 4.5 | 18.4 | 16.0 | 55.0 | 755 | 97 | 290 | 259 |
| Input Range (V) | 2.0 | 1.5 | 2.0 | 2.4 | 0.8 | 0.8 | 1.0 | 2.0 | 2.0 | 2.0 |
| Sampling Rate (MHz) | 80 | 100 | 50 | 50 | 40 | 100 | 80 | 110 | 75 | 80 |
| ERBW (MHz) | 20.0 | 50.0 | 25.0 | 25.0 | | 50.0 | 40.0 | 10.0 | 37.5 | 30.0 |
| SNDR (dB) | 64.0 | 69.8 | 62.0 | 64.0 | 62.0 | 59.7 | 72.6 | 64.2 | 67.0 | 64.0 |
| SFDR (dB) | 81.0 | 85.0 | 68.0 | 76.6 | 73.0 | 69.9 | 84.5 | 69.4 | 76 | 75.0 |
| ENOB (bit) | 10.3 | 11.3 | 10.0 | 10.3 | 10.0 | 9.6 | 11.8 | 10.4 | 10.8 | 10.3 |
| FOM (pJ/Step) | 0.62 | 0.52 | 0.09 | 0.29 | | 0.70 | 2.71 | 3.66 | 2.11 | 3.33 |

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# Chapter 6

# Split-Channel ADC

## 6.1 Introduction

Correlation-based techniques described in previous chapters usually need lots of samples to filter out the interference which is usually the ADC's input signal. For a $N$-bit ADC, we usually need $2^{2N}$ samples to achieve desired resolution [2]. This feature makes background calibration usually need long time to test and limit its practical application, especially in mass production. To make the background calibration more applicable, the calibration cycles reduction becomes an important issue in recent years.

As depicted in Figure 3.7, a narrow band filter is used to filter out the out-of-band noise and to extract the calibration data with desired SNR. In general, the filter is implemented by an accumulator (ACC). A low bandwidth LPF means that the ACC needs to accumulate lots of samples and to eliminate the effect of interference. In order to reduce the required huge samples during the data extraction duration, we have to eliminate the interference before passing the despreading signal through the filter. In this chapter, we will introduce several techniques that are used to speed up the convergent time. A new split-ADC configuration is proposed to shorten the calibration time of the ADC and this technique will be explained in the following sections.

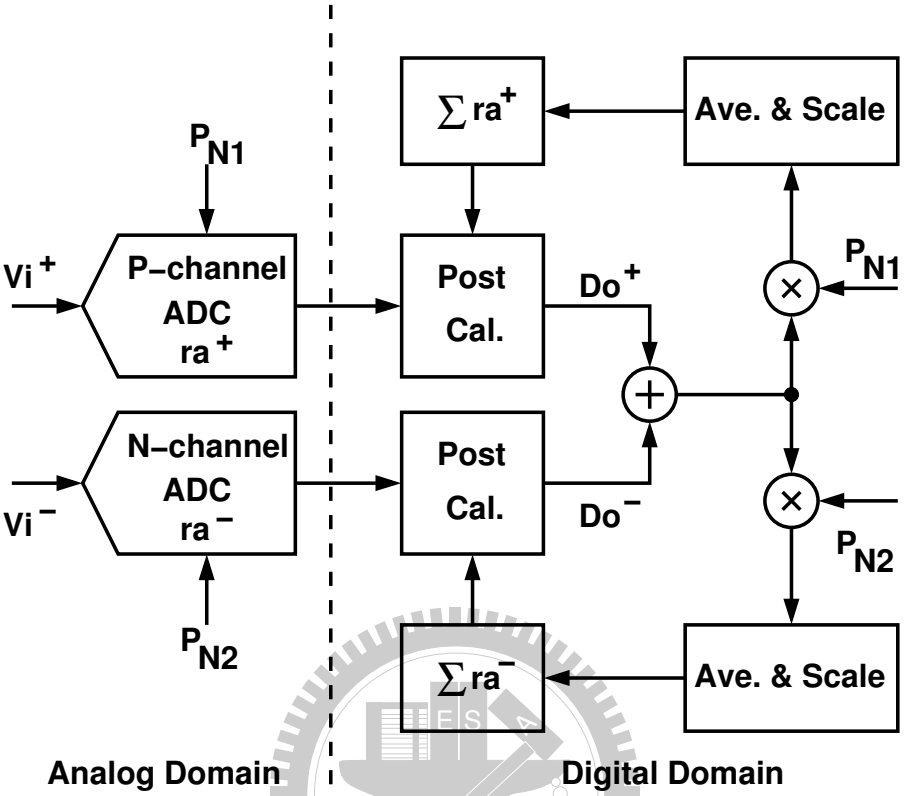


Figure 6.1: Two-channel ADC architecture proposed in [4].

## 6.2 Prior Arts

Correlation-based technique usually suffers from its long calibration time. Various techniques have been proposed to speed up the calibration convergence [11, 12, 4, 52]. These techniques share the same concept which predicts the input signal and eliminates it before data extraction. We will introduce these techniques in this section.

### 6.2.1 Two-Channel ADCs

A two-channel ADC is proposed to eliminate the interference during the data extraction duration [4]. The proposed ADC is a pseudo-differential architecture, as shown in Figure 6.1. For a fully differential input, the positive input signal and the negative input signal have the same magnitude but with 180° phase difference. If the positive input $V_i^+$ and negative input $V_i^-$ are quantized by two different ADCs and the ADC output is the

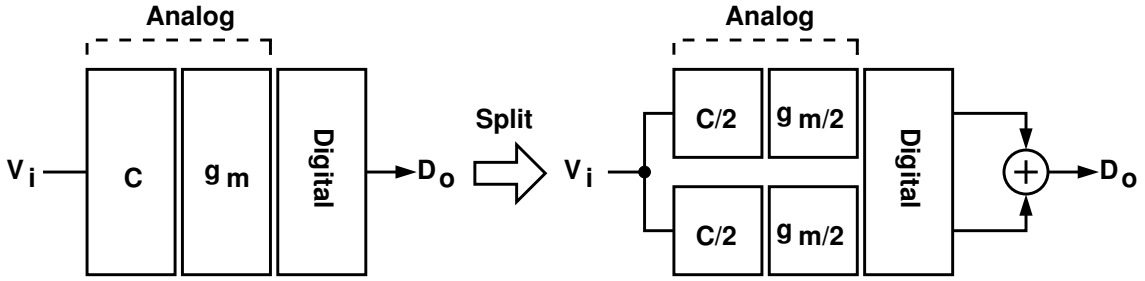


Figure 6.2: Basic concept of split-channel ADC architecture.

difference of the two ADCs' output $D_o^+$ and $D_o^-$.

$$D_o = D_o^+ - D_o^- \tag{6.1}$$

To calibrate the ADCs, two uncorrelated calibration signals $P_{N1}$ and $P_{N2}$ are injected into the two ADCs respectively. The output of the two ADCs are combined to eliminate the input signal, because the output of the two ADCs are 180° out of phase. To calibrate the two ADCs, the gain can be adjusted as:

$$ra^+[n+1] = ra^+[n] + \Delta \times (D_o^+ + D_o^-) \times P_{N1} \tag{6.2}$$

$$ra^-[n+1] = ra^-[n] + \Delta \times (D_o^+ + D_o^-) \times P_{N2} \tag{6.3}$$

where $\Delta$ is the adjusted step. Due to the elimination of the interference, the convergent speed can be improved. However, the efficiency of this technique is limited by the mismatch between the two ADCs.

### 6.2.2 Split-ADC

As similar to two-channel ADC, a split-ADC architecture is proposed to speed-up the calibration procedure [11, 52]. The power dissipation, chip area and noise performance of a ADC are mainly determined by the $g_m$ of the opamp and the capacitor size $C$, as shown in Figure 6.2. If we split the ADC into two separate ADCs and each of them has $g_m/2$ and $C/2$, then the power dissipation, chip area and noise performance will be the same theoretically. The output of the entire ADC is generated by combining the outputs of the two separate ADCs. The SNR of the split-ADC is 3dB better than the original one, this is because the signal power is four times larger and the noise power is only 2 times larger.

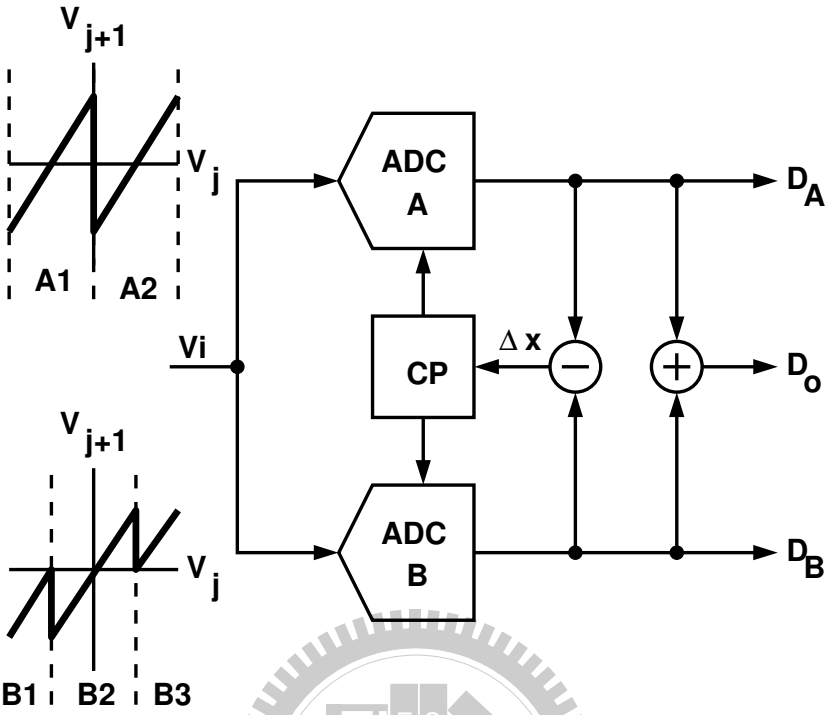


Figure 6.3: Split-channel ADC architecture for background calibration.

A split-ADC is illustrated in Figure 6.3. The two ADCs operate in different configurations, as shown in Figure 6.3. The different configurations can be achieved easily by simply changing the sub-ADC and sub-DAC values. During the calibration period, each ADC is the reference ADC of the other. For example, if the input $V_i$ locates in the $A1$ region, then ADC-A is used as the reference of ADC-B. Because there is no transition jump in ADC-A and its output can be used to predict the input without transition height error. In other words, if the input $V_i$ locates in the $B2$ region, then ADC-B is used as the reference of ADC-A. In calibration duration, the difference of the two ADCs is the error estimation. Any difference between the two ADCs is being processed by the CP and used to adjust the residue gain in digital domain. However, the efficiency is also limited by the mismatch between the two ADCs.

### 6.2.3 Prediction Using a FIR Filter

In order to predict the ADC input signal when the calibration data is injected into the ADC, a FIR filter is adopted [12]. The calibration signal is injected once into the ADC

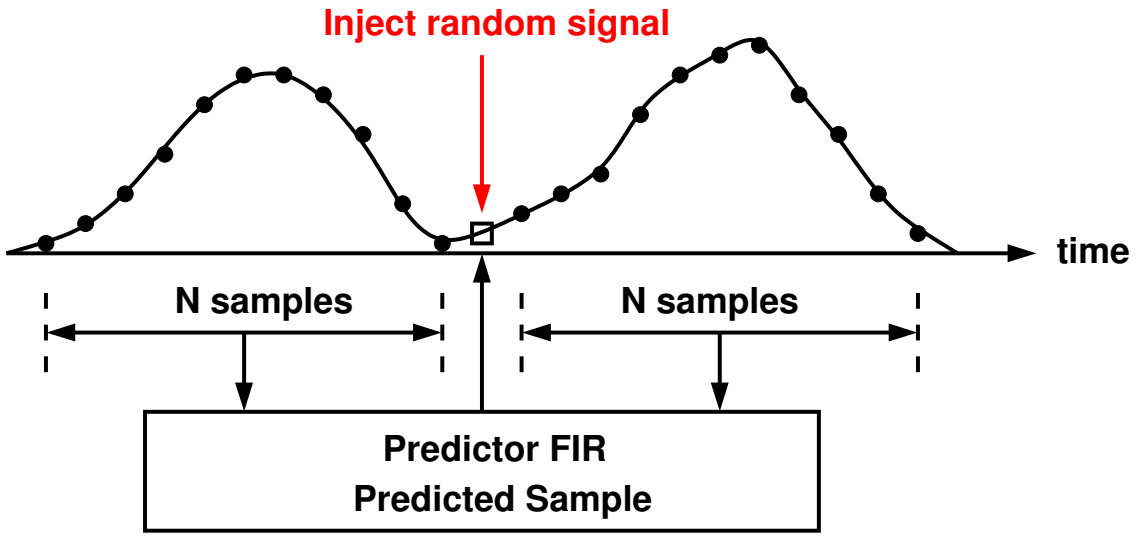


Figure 6.4: Predict the input signal using a FIR filter.

every $N$ clock cycles and the $N$ samples are processed by a FIR filter, as illustrated in Figure 6.4. The FIR filter is used to predict the ADC's input when the calibration signal is injected into the ADC. As long as the ADC's input signal is approximated, the input signal can be subtracted from the despreading signal and the calibration cycle can be reduced dramatically. However, the efficiency of this technique is reduced for the input near naquist rate. This is because the FIR filter can not predict the input signal well for high input frequency.

## 6.3 Split-Channel Configuration

The correlation-based calibration schemes usually suffer from long calibration time when applied to high-resolution ADCs. Referring to split-capacitor technique mentioned in Section 3.5.4, the $V_{j+1}$ stage output contains both the $R_{j,k}$ calibration term and the nominal A/D residue term. To extract $W_{j,k}$ from the $D_z$ digital codes, a large number of samples are required for the correlator to attenuate the perturbation caused by the $V_j$ stage input, as expressed by Equation (3.35). To decrease calibration time, i.e., decrease the $M$ in Equation (3.35), all signals other than the $q \times R_{j,k}$ term must be reduced at the inputs of the $W_{j,k}$ extractors. In the following section, the split-ADC technique is presented with

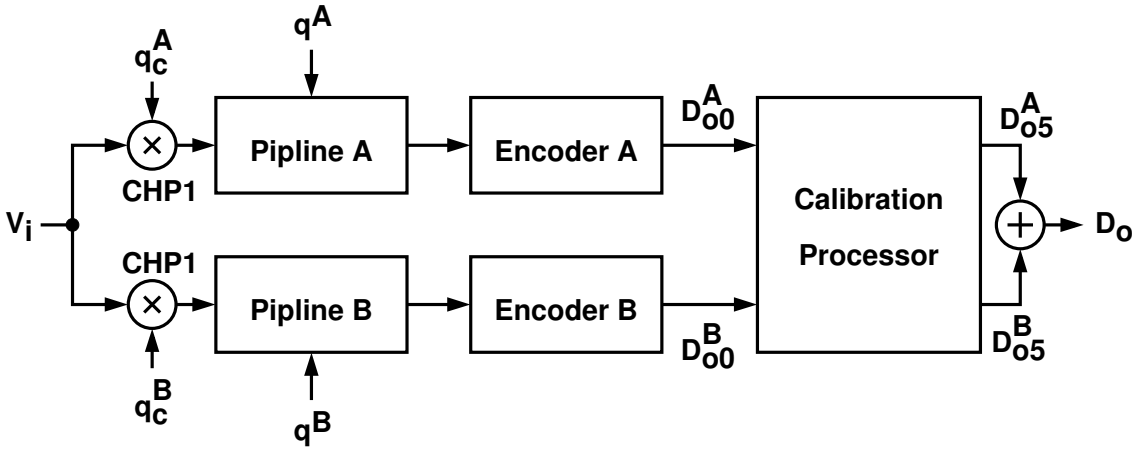


Figure 6.5: Split-channel ADC architecture for background calibration.

the split-capacitor calibration technique describes in [10].

### 6.3.1 Split-Channel ADC Architecture

Figure 6.5 shows the proposed split-channel ADC architecture that can be used to reduce the calibration time. The ADC is formed by splitting the original single-channel ADC into two identical parallel A/D channels. Both the A channel and the B channel quantize the same analog input, $V_i$. Their separate outputs are then combined to produce the final $D_o$ digital output. Each split channel has the same circuit topology as the single-channel ADC but with devices half of the original size. Compared with the original single-channel ADC, the operating speed and total power dissipation are preserved in the split-channel ADC. Considering only the effect of $kT/C$ thermal noises, each split path contains thermal noises with average powers twice as large as those in the original design. But since both split paths convert the same analog input, the combined digital output has the same signal-to-noise ratio as the output of a single-channel ADC [11, 4].

The two CHP1 random choppers in Figure 6.5 are controlled by two mutually uncorrelated binary random sequences, $q_c^A$ and $q_c^B$, which alternate between $+1$ and $-1$. The choppers are added to scramble the $V_i$ input and to make sure that the data extraction is efficient for any input condition [10]. The input scrambling is also useful in extracting the input offsets of the two A/D channels. The offset extraction is described in Section 6.4.

The other two random sequences, $q^A$ and $q^B$, are injected into the respective pipeline stages for $R_{j,k}$ calibration. The $q^A$ and $q^B$ sequences are designed to be statistically uncorrelated, and their generation is described in Section 3.8. The two A/D channels are calibrated concurrently.

### 6.3.2 ADC Output Encoding

The raw digital output of the overall ADC, $D_{o0}$, can be encoded by using the following equation:

$$D_{o0} = \sum_{j=1}^{P} \frac{W_j}{G_1 G_2 \cdots G_j} \tag{6.4}$$

Neglecting quantization error, the relationship between the $D_{o0}$ digital output and the $V_1$ analog input is:

$$D_{o0} = g \cdot V_1 + r_{j,k} \cdot \left(D_j - q\right) + o \tag{6.5}$$

where

$$g = \frac{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_P}{G_1 G_2 \cdots G_P} \tag{6.6}$$

$$r_{j,k} = \frac{g}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_j} \times R_{j,k} \tag{6.7}$$

$$o = -g \times \sum_{j=1}^{P} \frac{V_j^{\text{os}}}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_{j-1}} \tag{6.8}$$

In Equation (6.5), $g$ is the overall A/D conversion gain, $o$ is the overall offset, and $r_{j,k}$ is the magnitude of the pseudo-random noise injected into the pipeline signal path for calibration. The relationship between $W_{j,k}$ and $r_{j,k}$ is

$$\frac{W_{j,k}}{G_1 G_2 \cdots G_j} = \check{r}_{j,k} = r_{j,k} - \Delta r_{j,k} \tag{6.9}$$

where $\check{r}_{j,k}$ is an estimation of $r_{j,k}$ calculated from $W_{j,k}$. Let $r_j = r_{j,1} + r_{j,2}$, we also have

$$\frac{W_j}{G_1 G_2 \cdots G_j} = \check{r}_j = r_j - \Delta r_j \tag{6.10}$$

The final digital output of the ADC is generated by subtracting $[W_{j,k}/(G_1G_2\cdots G_j)]\cdot\left(D_j-q\right)$ from $D_{o0}$. From Equation (6.5) and Equation (6.9), the $D_o$ final output can be expressed as:

$$D_o = g\cdot V_1 + o + \underbrace{\Delta r_{j,k}\cdot\left(D_j-q\right)}_{n_{cal}} + n_{enc} \tag{6.11}$$

where the calibration noise, $n_{cal}$, is the residue introduced by the calibration process. From Equation (6.7), the average power of $n_{cal}$ can be found to be:

$$N_{cal} = \sigma^2\left(\Delta r_{j,k}\right) = \sigma^2\left(\Delta R_{j,k}\right)\times\frac{g^2}{\left(\hat{G}_1\hat{G}_2\cdots\hat{G}_j\right)^2} \tag{6.12}$$

In Equation (6.11), the encoding noise, $n_{enc}$, is added to represent the introduced error when using $W_j/(G_1G_2\cdots G_j)=\check{r}_j$ to encode $D_{o0}$. Since the $\check{r}_j$ data, for all $j$, are slow-varying variables compared with a normal $V_1$ input, the $n_{enc}$ encoding noise in Equation (6.11) is input-dependent and difficult to be modeled. To simplify the analysis, it is assumed that the $\Delta r_j$ variables, for all $j$, are random and mutually uncorrelated. Then, the average power of $n_{enc}$ can be approximated to:

$$N_{enc}\approx\sum_{j=1}^{K}\sigma^2\left(\Delta r_j\right)\approx 2\sigma^2\left(\Delta R_{j,k}\right)\times\sum_{j=1}^{k}\frac{1}{2^{2j}}\approx\frac{2}{3}\cdot\sigma^2\left(\Delta R_{j,k}\right) \tag{6.13}$$

The total noise power due to both calibration and encoding is $N_{cal}+N_{enc}=(11/12)\sigma^2(\Delta R_{j,k})$. It is assumed that the first pipeline stage is calibrated for worst-case condition, in which $N_{cal}=\sigma^2(\Delta r_{j,k})=0.25\sigma^2(\Delta R_{j,k})$ with $j=1$. To estimate the required value of $M$, let $N_{cal}+N_{enc}$ be less than the average power of the ADC's quantization noise, $N_{qn}$. For an ideal $N$-bit ADC with an input range of $\pm 0.5V_r$, its $N_{qn}$ is $(1/12)(V_r/2^N)^2$. Thus, the required value for $M$ is:

$$M\geq\frac{11}{12}\times 2^{2N-2}\approx 2^{2N-2} \tag{6.14}$$

Large $M$ is necessary to achieve high A/D resolution, but also results in long calibration time. If the input is a full-range sine wave, i.e., $V_1(t)=0.5V_r\sin(\omega_i t)$, the signal-to-distortion-plus-noise (SNDR) of the $D_o$ of Equation (6.11) is:

$$\mathrm{SNDR}_o\approx\frac{g^2\cdot E\left[V_1^2\right]}{N_{cal}+N_{enc}}\approx\frac{72}{11}\times M \tag{6.15}$$

The equation assumes $g=1$ and neglects the quantization noise.

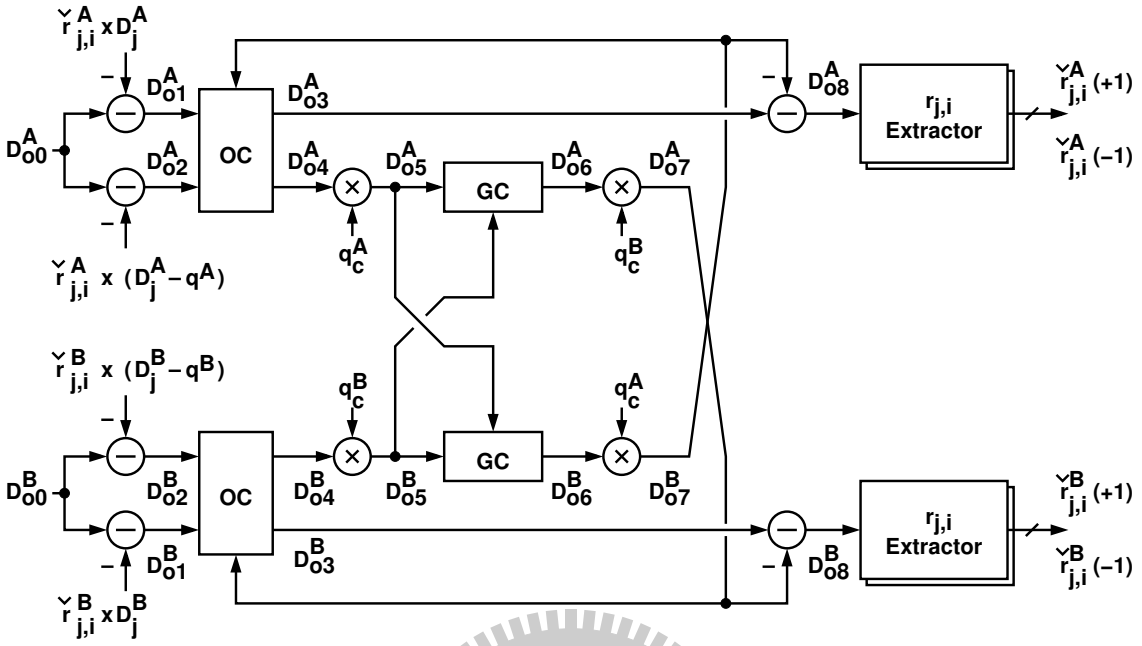


Figure 6.6: Calibration processor for the split-channel ADC.

### 6.3.3 Calibration Principle

Unlike the calibration procedures described in Section 3.8 in which the $R_{j,k}$ is extracted from the output of the backend z-ADC, the calibration scheme described in this section extracts $R_{j,k}$ from the overall ADC digital output. From Equation (6.4), Equation (6.5) and Equation (6.11), the raw digital outputs of the two A/D channels can be expressed as:

$$D_{o0}^{A} = q_c^A \cdot g^A \cdot V_i + r_{j,k}^A \cdot \left(D_j^A - q^A\right) + o^A + n_{enc}^A \tag{6.16}$$

$$D_{o0}^{B} = q_c^B \cdot g^B \cdot V_i + r_{j,k}^B \cdot \left(D_j^B - q^B\right) + o^B + n_{enc}^B \tag{6.17}$$

The definitions of $g^A$, $g^B$, $o^A$, and $o^B$ are the same as those of Equation (6.5). The $r_{j,k}^A$ and $r_{j,k}^B$ symbols are simplified notations for $r_{j,k}^A$ and $r_{j,k}^B$ respectively. Both $n_{enc}^A$ and $n_{enc}^B$ are encoding noises due to the errors in $r_{j,k}^A$ and $r_{j,k}^B$ estimations, as defined in Equation (6.11). In the equations mentioned above and for the following analysis, a variable with a superscript of $A$ or $B$ is denoted as a variable in one of the A/D channel. A variable without the $A$ or $B$ superscript implies it can be applied to both channels.

Figure 6.6 shows the block diagram of the calibration processor in Figure 6.5. The $D_{o0}^A$ and $D_{o0}^B$ raw digital outputs from the encoders are subjected to identical signal process-

ing procedures in the calibration processor. Instead of sending $D_{o0}$ to the $r_{j,k}$ extractors directly, the offset in $D_{o0}$, i.e., the $o$ term in Equation (6.16), is eliminated by using the offset correction (OC) functional block. The resulting $D_{o3}$ is subtracted by $D_{o7}$ generated from the other channel to eliminate the $q_c g V_i$ term in Equation (6.16). If both $o$ and $q_c g V_i$ can be removed effectively in the resulting $D_{o8}$ signal, the required number of samples for $r_{j,k}$ extraction can then be decreased to reduce calibration time. The output of the $r_{j,k}$ extractor is an estimation of $r_{j,k}$, i.e., the $\check{r}_{j,k}$ defined in Equation (6.9).

It will become clear later that the $D_{o6}$ signal in either channel is a $V_i$ duplicate of the other channel. They can be expressed as:

$$\begin{aligned} D_{o6}^{A} &= g_c^{A} g^{A} \cdot V_i + g_c^{A} q_c^{A} \cdot \left[ \Delta r_{j,k}^{A} \left( D_j^{A} - q^{A} \right) - \Delta o^{A} + n_{enc}^{A} \right] \\ D_{o6}^{B} &= g_c^{B} g^{B} \cdot V_i + g_c^{B} q_c^{B} \cdot \left[ \Delta r_{j,k}^{B} \left( D_j^{B} - q^{B} \right) - \Delta o^{B} + n_{enc}^{B} \right] \end{aligned} \tag{6.18}$$

The $g_c$ is a gain correction factor generated from the gain correction (GC) functional block. Both $\Delta r_{j,k}$ and $\Delta o$ are residues due to non-ideal $r_{j,k}$ extraction and offset cancellation. Their values will be reduced to a level as low as the ADC's LSB. Neglecting $\Delta r_{j,k}$, $\Delta o$, and $n_{enc}$, if $g_c^{A} g^{A} = g^{B}$, the $q_c^{B} g^{B} V_i$ term in $D_{o0}^{B}$ of Equation (6.16) can be eliminated by subtracting $D_{o7}^{A} = q_c^{B} D_{o6}^{A}$ from $D_{o0}^{B}$. The GC block adaptively adjusts the $g_c^{A}$ GC factor so that $g_c^{A} \times g^{A} \approx g^{B}$. The gain mismatches are defined as:

$$\begin{aligned} \Delta g^{A} &= g^{A} - g_c^{B} \times g^{B} \\ \Delta g^{B} &= g^{B} - g_c^{A} \times g^{A} \end{aligned} \tag{6.19}$$

The detailed signal processing procedures of the calibration processor are described in the following sections.

### 6.3.4 Calibration Noise Reduction

As shown in Figure 6.6, the $r_{j,k}$ random term in Equation (6.16) is first subtracted from $D_{o0}$ to yield $D_{o1}$ and $D_{o2}$ respectively. The $\check{r}_{j,k}$ value used in the subtraction is an estimation of $r_{j,k}$ obtained in the previous calibration cycle using the $r_{j,k}$ extractor. The difference between $r_{j,k}$ and $\check{r}_{j,k}$ is $\Delta r_{j,k}$, as defined in Equation (6.9).

The $r_{j,k} q$ term is kept in $D_{o1}$. The calibration processor extracts $r_{j,k} q$ from $D_{o1}$ to obtain a new $\check{r}_{j,k}$.

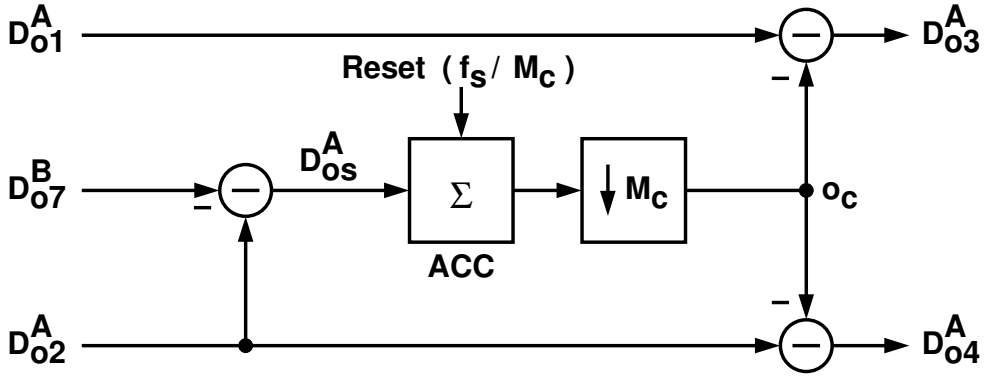


Figure 6.7: OC block diagram.

## 6.4 Offset Correction

Due to the use of the CHP1 random choppers shown in Figure 6.5, the only dc components in the $D_{o1}$ and $D_{o2}$ signals are the input-referred offsets of the A/D channels [41], i.e., the $o$ terms in Equation (6.16). Figure 6.7 shows the block diagram of the OC block for the A channel. The OC block uses the integration and dump technique to estimate the channel offset from $D^A_{o2}$. The $D^A_{o2}$ signal is first subtracted by $D^B_{o7}$, and the result, $D^A_{os}$, is then integrated on an accumulator (ACC). The $o_c$ offset estimation is taken out only after $M_c$ cycles of integration, where $M_c$ is the period of the $q^A_c$ random sequence shown in Figure 6.5. The difference between $o$ and $o_c$ is defined as:

$$\Delta o = o - o_c \tag{6.20}$$

The OC block's outputs, $D^A_{o3}$ and $D^A_{o4}$, are generated by subtracting $o_c$ from $D^A_{o1}$ and $D^A_{o2}$ respectively.

In Figure 6.7, the reason to undertake $D^A_{os} = D^A_{o2} - D^B_{0o7}$ before the integration is to reduce the perturbation of the $q^A_c g^A V_i$ term in Equation (6.16) and decrease the required integration time for offset estimation. When the calibration process converges, $\Delta o$, $\Delta r_{j,k}$, and $n_{enc}$ are reduced to a level close to the ADC's LSB, the only significant perturbation remaining in $D^A_{os}$ is the $\Delta g^A V_i$ term. Thus, the variance of $\Delta o$ can be approximated to:

$$\sigma^2(\Delta o) \approx \frac{1}{M_c} \times \left\{ \sigma^2(\Delta g) \cdot E\left[V_i^2\right] \right\} \tag{6.21}$$

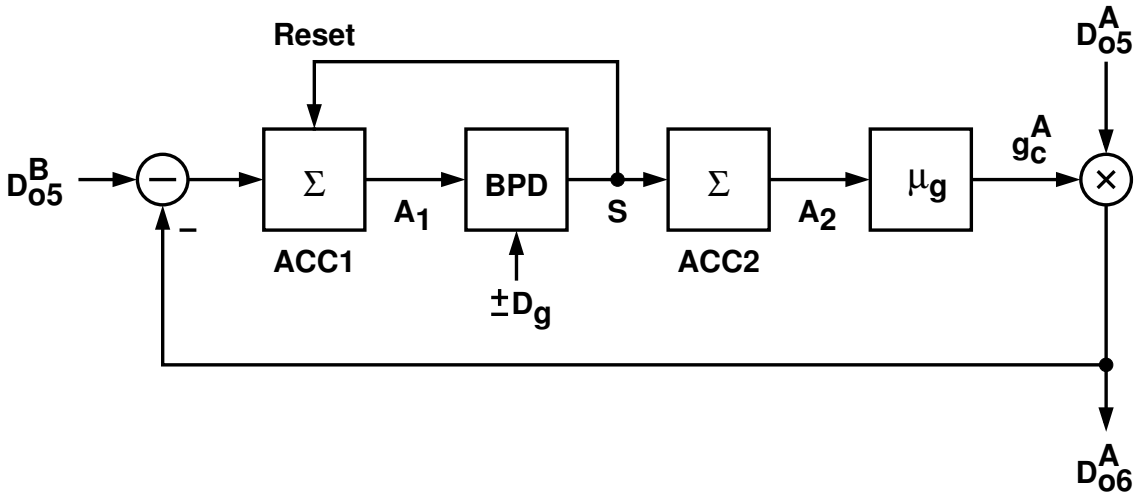


Figure 6.8: GC block diagram.

## 6.5 Gain Correction

As shown in Figure 6.6, $D_{o5} = q_c \cdot D_{o4}$, thus $D_{o5}$ contains the unscrambled $g \cdot V_i$ term. In the GC blocks, $D_{o5}$ is multiplied by a GC factor, $g_c$, to generate $D_{o6}$. The $D_{o7}$ is generated by scrambling the $D_{o6}$ of Equation (6.18) with the $q_c$ random sequence of the other channel. The GC blocks are used to generate the $g_c$ gain factors so that the $\Delta g^A$ and $\Delta g^B$ of Equation (6.19) can be minimized.

Figure 6.8 is the GC's block diagram in the A-channel signal path, which is similar to the adaptation scheme of [53], and is a variation of least-mean-square (LMS) algorithm [54]. The GC block adaptively adjusts the $g_c^A$ GC factor to minimize the difference between $D_{o6}^A$ and $D_{o5}^B$. The converged $g_c^A$ yields $g_c^A \times g^A \approx g^B$. In Figure 6.8, the difference between $D_{o6}^A$ and $D_{o5}^B$ is integrated on the ACC1 accumulator. The bilateral peak detector (BPD) monitors the ACC1's output, $A_1$, and generates a corresponding triple-valued output, $S \in \{+1, 0, -1\}$. The BPD has two thresholds, $+D_g$ and $-D_g$. When $A_1 > +D_g$, $S = +1$. When $A_1 < -D_g$, $S = -1$. Otherwise, $S = 0$. In addition, if $S = +1$ or $S = -1$, the ACC1 accumulator will be reset in the following clock cycle. Thus, $-(D_g + 1) \le A_1 \le +(D_g + 1)$, and $S$ can only remain $+1$ or $-1$ for one clock cycle. The $S$ sequence is integrated on the ACC2 accumulator, yielding $A_2$. The $g_c^A$ GC factor is $\mu_g \times A_2$.

This automatic gain-control loop has two design parameters, i.e., $D_g$ and $\mu_g$. Small

$D_g$ and large $\mu_g$ result in fast converging speed but larger fluctuation in $g^A$. On the other hand, large $D_g$ and small $\mu_g$ result in slow converging speed but smaller fluctuation in $g^A$.

If the $V_i$ input is stable such as $E[|V_i|]$ is a constant, then the gain-control feedback loop can be modeled as a single-pole system with a $\tau_g$ time constant expressed as:

$$\tau_g \approx \frac{1}{\mu_g} \times \frac{D_g}{E\,[|V_i|]} \tag{6.22}$$

The $\tau_g$ must be much shorter than $M$, the period of the $q^A$ and $q^B$ random sequences. This ensures that the GC adaptation process has little effect on the overall calibration result.

This GC adaptation loop adjusts the $g_c^A$ gain factor according to the difference between $D_{o5}^B$ and $g_c^A D_{o5}^A$. As what will be explained later, both $D_{o5}^A$ and $D_{o5}^B$ contain encoding noise, $n_{enc}$, and calibration noise, $n_{cal}$. Those noises cause $g_c$ to fluctuate. The behavior of the loop can be analyzed by using stochastic signal processing technique [53]. It is desirable to make $D_g$ larger than $\sqrt{N_{enc} + N_{cal}}$ so that both $n_{enc}$ and $n_{cal}$ noises have little effect on the BPD's output, where $N_{enc}$ and $N_{cal}$ are the average powers of $n_{enc}$ and $n_{cal}$ respectively. A semi-empirical expression for the variance of $\Delta g$ is:

$$\sigma^2(\Delta g) = \frac{\mu_g^2}{6} + \frac{\mu_g^2}{3} \times \frac{E[|V_i|]}{D_g} \times \frac{\sqrt{N_{enc} + N_{cal}}}{V_{\text{LSB}}} \tag{6.23}$$

where $V_{\text{LSB}}$ is the ADC's LSB voltage. If $D_g$ is large enough, the $\Delta g$ of Equation (6.19) has a mean of zero and fluctuates between $[P,\, P - \mu_g]$, where $P \in [0,\, \mu_g]$. The probability density function of $\Delta g$ is $1 - |\Delta g|/\mu_g$. In such case the variance of $\Delta g$ approximates to $\mu_g^2/6$, which is the first term on the right-hand side of Equation (6.23). The second term on the right-hand side of Equation (6.23) arises from the perturbation of $n_{enc}$ and $n_{cal}$. Both noises are increased if smaller $M$ is used, then large $D_g$ is required. A compromise should be made between the $\sigma^2(\Delta g)$ and the convergent speed of the GC loop.

## 6.6 Correlation Data Extraction

As shown in Figure 6.6, the input of the $r_{j,k}$ extractor, $D_{o8}$, is generated by subtracting $D_{o7}$ coming from the other channel from $D_{o3}$. The $r_{j,k}$ extractors in Figure 6.6 are identical to the $W_{j,k}$ extractor shown in Figure 3.21. The $D_{o8}$ signal contains the $r_{j,k}q$ term which

the $r_{j,k}$ extractors are in need of, and other terms which can be regarded as perturbations and cause variation in the $r_{j,k}$ extraction. Among the perturbations, the $\Delta g V_i$ term is much larger than other ones that contain the residual $\Delta r_{j,k}$ or $\Delta o$ terms. As the calibration process converges, both $\Delta r_{j,k}$ and $\Delta o$ are reduced to a level close to the ADC's LSB. The variance of the $r_{j,k}$ estimation can be approximated to:

$$\sigma^2(\Delta r_{j,k}) \approx \frac{1}{M} \times \left\{ \sigma^2(\Delta g) \cdot E\left[V_i^2\right] \right\} \tag{6.24}$$

Comparing Equation (6.24) with Equation (3.35), the required $M$ for the split-channel architecture can be decreased by a factor comparable to $\sigma^2(\Delta g)$. Since much smaller $M$ can be used, it is critical to ensure that the $q$ random sequence has equal number of zeros and ones for consecutive $M$ samples in each $r_{j,k}$ extraction cycle.

## 6.7 ADC Outputs

In Figure 6.6, $D_{o5}^A$ and $D_{o5}^B$ are the final digital outputs for the two A/D channels. Both can be expressed as:

$$D_{o5} = g \cdot V_i + q_c \cdot \Big[ \underbrace{\Delta r_{j,k} \cdot \left(D_j - q\right) - \Delta o}_{n_{cal}} + n_{enc} \Big] \tag{6.25}$$

The $n_{cal}$ calibration noise is introduced by the calibration process. The $n_{enc}$ encoding noise occurs when using the $\check{r}_{j,k}$ estimation to encode $D_{o0}$. The average power of $n_{cal}$ can be expressed as:

$$N_{cal} = 2\sigma^2\left(\Delta r_{j,k}\right) + \sigma^2\left(\Delta o\right) \approx \left( \frac{1}{M} + \frac{1}{M_c} \right) \times \sigma^2(\Delta g) \cdot E\left[V_i^2\right] \tag{6.26}$$

The average power of $n_{enc}$ can be approximated to:

$$N_{enc} \approx 2K \times \sigma^2(\Delta r_{j,k}) \approx \frac{2K}{M} \times \sigma^2(\Delta g) \cdot E\left[V_i^2\right] \tag{6.27}$$

Neglecting quantization noise, the SNDR of the $D_{o5}$ digital output can be expressed as:

$$\mathrm{SNDR}_{o5} = \frac{g^2 \cdot E\left[V_i^2\right]}{N_{cal} + N_{enc}} \approx \frac{g^2}{\sigma^2(\Delta g)} \times \frac{1}{\frac{2K+1}{M} + \frac{1}{M_c}} \tag{6.28}$$

The required $M$ and $M_c$ can be estimated by letting $N_{cal} + N_{enc}$ approximate the average power of ADC's quantization noise.

In Figure 6.5, the final ADC output $D_o$ is $D_{o5}^A + D_{o5}^B$. Assuming that the calibration noises and the encoding noises are uncorrelated, the SNDR of the $D_o$ digital output is 3 dB better than the one predicted by Equation (6.28).

Referring to Figure 6.5, a CHP1 random chopper is placed in front of each A/D channel. It should be pointed out that mismatches among analog switches within the CHP1 chopper can superimpose a $q_c$-like noise at A/D channel's input. If this $q_c$-like noise has a non-zero mean value, it can cause offset estimation error in the OC block, and its mean value is added to the $\Delta o$. In practical cases, a minuscule increasing in $|\Delta o|$ has little effect on the succeeding GC and $r_{j,k}$ extraction operations. However, it can degrade the SNDR of ADC's final digital output, as manifested by Equation (6.25).

## 6.8 A 15-Bit ADC Design Example

A 15-bit pipelined split-channel ADC was simulated by using a C program to verify the proposed calibration techniques. The ADC employs the architecture of Figure 6.5, which consists of two separate A/D channels. Each channel comprises 15 radix-2 1.5-bit pipeline stages. Each pipeline stage has a transfer characteristic of Equation (2.15), and its nominal stage gain is $G_j = 2$. Let $V_r = 1$, then the ADC's input range is $\pm 0.5$. For 15-bit resolution, the ADC's LSB step size is $V_{\text{LSB}} = 2^{-15}$. Assuming the ADC's input is a full-range sine wave, i.e., $V_i(t) = 0.5\sin(\omega_i t)$, we have $E[|V_i|] = 1/\pi$ and $E\left[V_i^2\right] = 1/8$. The quantization noise power is $N_{qn} = (1/12) \times 2^{-30}$.

For each A/D channel, only the first five pipeline stages, i.e., from the 1st to the 5th stage ($K = 5$), are subjected to calibration. The gains and offsets of the pipeline stages in each channel are assigned the values in TABLE 6.1. The last 10 stages in each A/D channel, i.e., from the 6th to the 15th stage, are summarized as a single 11-bit ADC with its own conversion gain and offset and an input range of $\pm 1$. Similar to Equation (3.5),

Table 6.1: Gains and offsets of the pipline stages in simulations.

| Gain | | | | | | |
|---|---|---|---|---|---|---|
| Channel | $\hat{G}_1$ | $\hat{G}_2$ | $\hat{G}_3$ | $\hat{G}_4$ | $\hat{G}_5$ | $G_{z6}/\hat{G}_{z6}$ |
| A | 1.90 | 1.90 | 1.90 | 1.90 | 1.90 | 0.95 |
| B | 2.10 | 2.10 | 2.10 | 2.10 | 2.10 | 1.05 |
| **Offset** | | | | | | |
| Channel | $V_1^{os}$ | $V_2^{os}$ | $V_3^{os}$ | $V_4^{os}$ | $V_5^{os}$ | $O_{z6}$ |
| A | +0.05 | +0.05 | +0.05 | +0.05 | +0.05 | +0.05 |
| B | −0.005 | −0.05 | −0.05 | −0.05 | −0.05 | −0.05 |

their functions are expressed as:

$$\begin{aligned} V_6^A &= \frac{G_{z6}^A}{\hat{G}_{z6}^A} \cdot D_{z6}^A + O_{z6}^A + Q_{z6}^A \\ V_6^B &= \frac{G_{z6}^B}{\hat{G}_{z6}^B} \cdot D_{z6}^B + O_{z6}^B + Q_{z6}^B \end{aligned} \tag{6.29}$$

Both $Q_{z6}^A$ and $Q_{z6}^B$ are quantization errors. For 10-bit resolution over ±0.5 input range, we have $\left|Q_{z6}^A\right| < 2^{-11}$ and $\left|Q_{z6}^B\right| < 2^{-11}$.

The ADC follows the calibration procedures described in Section 3.5.4. For a split-channel ADC, its $r_j$ is getting updated by calibration. A total of $5 \times 4M$ samples are required to calibrate 5 pipeline stages in one $r_j$ calibration cycle.

In addition to the $r_j$ calibration, the OC block and GC block shown in Figure 6.6 operate concurrently. For both GC blocks, we choose $D_g = 2^{-6}$ and $\mu_g = 2^{-11}$. From Equation (6.22), the time constant of the GC system is $\tau_g = 2^6$. From Equation (6.23), Equation (6.26), and Equation (6.27), by letting $N_{cal} + N_{enc}$ equals the $N_{qn}$ quantization noise power for 15-bit resolution, one can choose $M_c = 2^{11}$ and $M = 2^{14}$, resulting in $\sigma^2(\Delta g) = 8.5 \times 10^{-7}$, $N_{cal} \approx N_{enc} \approx 5.8 \times 10^{-11}$. However, simulations show that a system with $M_c = 2^{12}$ and $M = 2^{13}$ can also achieve 15-bit resolution and has a shorter calibration time.

Unless otherwise specified, the following simulations and discussions assume that $M_c = 2^{12}$, $D_g = 2^{-6}$, $\mu_g = 2^{-11}$, and $M = 2^{13}$. The $V_i$ input is a sine wave with an amplitude of 0.5 and a frequency close to $1/10$ of the ADC's sample rate.

Figure 6.9 shows the transient behaviors of the $g_c$ and $o_c$ variables. The variables are shown against the progress of calibration cycle. Each calibration cycle spans $20M$ clock

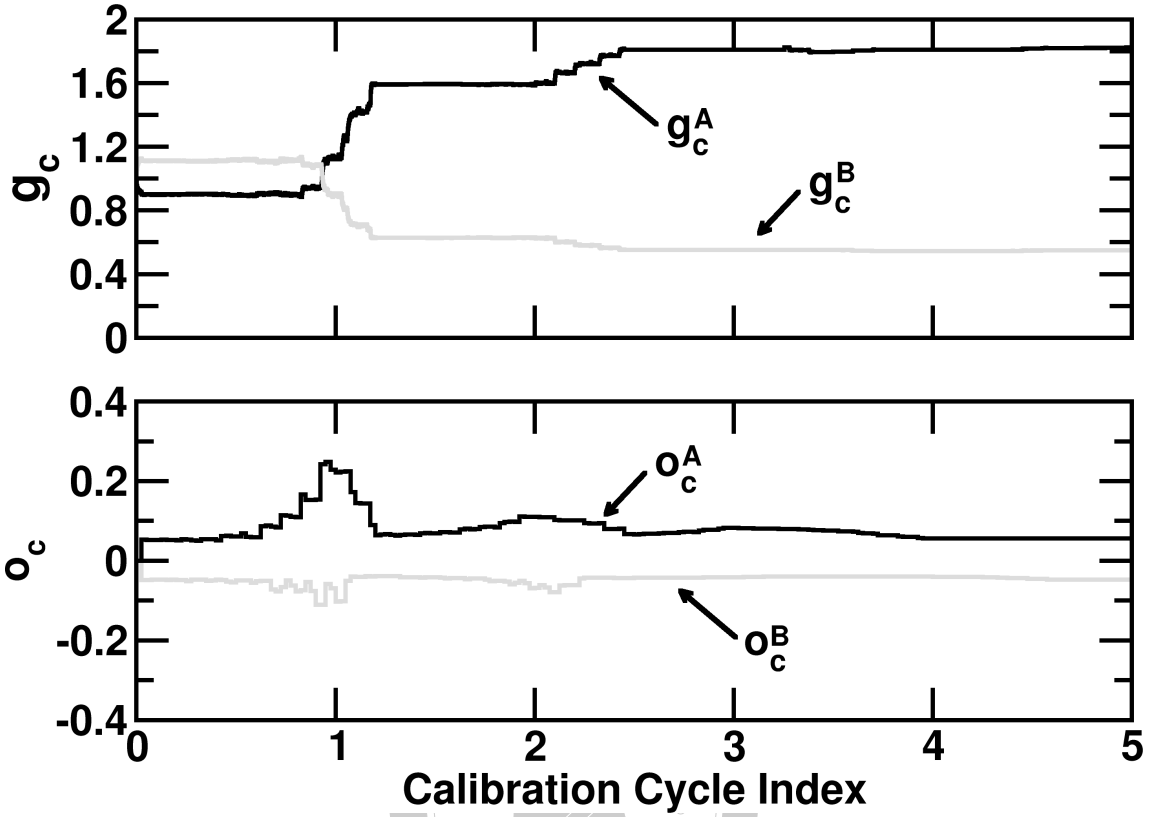


Figure 6.9: Simulated $g_c$ and $o_c$ versus calibration cycle.

cycles. Both $o_c^A$ and $o_c^A$ are updated once every $M_c$ clock cycles. Although both $g_c^A$ and $g_c^B$ are continuously adjusted, there are visible abrupt changes during initial calibration cycles. The abrupt changes occur whenever ADC's $W_j$ variables are updated.

Figure 6.10 shows the initial converging behavior of the calibration process in the split-channel ADC as well as the behavior in the single-channel ADC. Each calibration cycle spans $20M$ clock cycles, where $M = 2^{13}$ for the split-channel ADC and $M = 2^{25}$ for the single-channel ADC. The SNDR of the split-channel ADC is stabilized after five calibration cycles, while the SNDR of the single-channel ADC approximates its final value after only one calibration cycle. In a split-channel ADC, the effectiveness of $r_{j,k}$ extraction, OC, and GC, depends on each other. The coupling effect slows down the calibration progress. For this split-channel ADC with other design parameters unchanged, the calibration cannot converge if $M$ is smaller than $2^9$.

Figure 6.11 shows the SNDR performance of the split-channel ADC with different

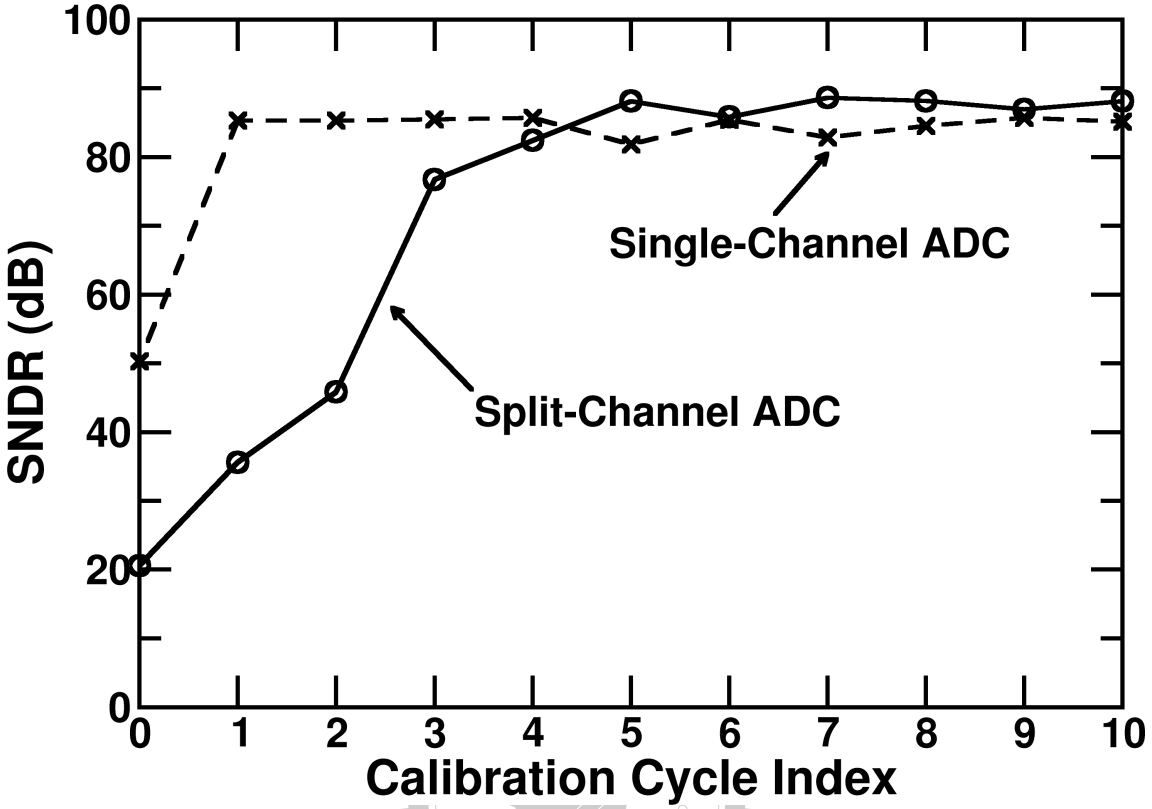


Figure 6.10: Simulated ADC's SNDR versus calibration cycle.

$M$. It also compares the split-channel ADC with a single-channel ADC that consists of pipeline stages identical to those in the split-channel ADC. The SNDR of the split-channel ADC is calculated from the digital output of the A channel only. For the combined output of the split-channel ADC, its SNDR is 3 dB better than those shown in Figure 6.11. The SNDR values predicted by Equation (6.15) and Equation (6.28) are more pessimistic than those obtained from simulations. Nevertheless, the equations are useful in the initial performance estimations. From both theoretical calculations and simulations, the required $M$ for a split-channel ADC is significantly smaller than that for a single-channel ADC of similar design.

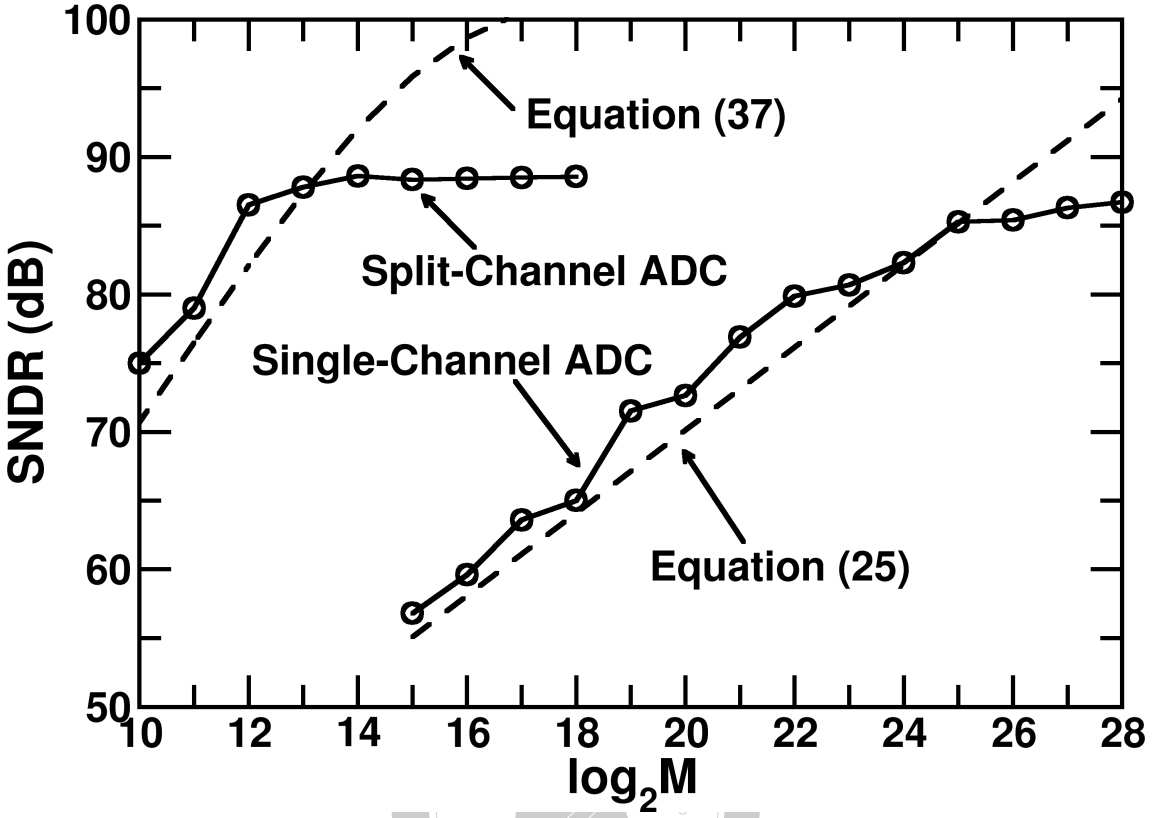


Figure 6.11: Simulated SNDR performance with different values of $M$.

## 6.9 Summary

This thesis describes a robust and fast background calibration scheme for SC pipelined ADCs. The split-channel ADC architecture consists of two identical A/D channels that receive the same $V_i$ input but employ different random sequences for calibration. The calibration time can be greatly reduced by comparing the digital output streams from both channels and then removing the $V_i$-related term at the inputs of $r_{j,k}$ extractors and offset estimators. OC block and GC block are employed to equalize the transfer characteristics of the two A/D channels.

The proposed calibration scheme is most suitable for high-resolution ADCs realized in nano-scaled CMOS technologies. Most of the calibration overhead is digital circuitry, whose power consumption and area are scaled down with technology scaling. The proposed scheme eliminates the concern for long calibration time, which may become unacceptable in high-resolution ADC designs. The scheme is robust since it can function

under any input condition as long as it does not exceed the specified ADC's input range. Although only radix-2 1.5-bit SC pipeline stages are included in the discussions, the techniques described in this paper can be extended and applied to multi-bit pipeline stages as well as pipeline stages with circuit configuration not in the SC form.

# Chapter 7

# Conclusions and Future Works

## 7.1 Conclusions

The performance of a pipelined ADC is limited by the accuracy of residue gain and sub-DAC output. These two analog design parameters are affected by the capacitors mismatch and finit opamp dc gain. This situation is worsened in advanced technology. In order to achieve desired ADC performance, the pipelined ADC is needed to be calibrated. In this thesis, a new digital background calibration technique for pipelined ADCs is presented. The calibration can correct pipeline stage nonlinearity as well as stage gain and sub-DAC errors. Since the accuracy and linearity requirements are mitigated, analog circuits of less complexity and power can be used. Simpler analog circuits are easier to transfer to different fabrication technologies. Most of the calibration overhead is digital circuitry, whose area and power consumption is minuscule in nano-scale CMOS technologies. The proposed calibration technique requires neither stringent device matching nor extra signal range. The latter is crucial for circuits to be operated under low-voltage supplies. Finally, a 32-mW 12-bit 80-MS/s pipelined ADC was presented. This ADC adopts the proposed calibration technique and achieve 67dB SNDR. A simple operational amplifier is also proposed to save the power and the chip area.

A new split-ADC architecture is proposed to reduce the calibration time for a correlation-based digital background calibration technique. By eliminating the interference of the extractor, the required calibration samples are dramatically reduced. Long calibration time

limits the practical application of the background calibration, especially in mass production. This technique makes the background more attractive to the industry.

## 7.2 Recommendations for Future Investigation

This section presents several suggestions for future investigations in high performance ADC design.

- The correlation-based nonlinearity calibration technique proposed in this thesis still needs long calibration time to converge. The split-ADC technique proposed in this thesis can be used to mitigate this requirement, especially for high resolution ADCs. By combining these two techniques, the nonlinear calibration can be accomplished by much less samples and make this technique more feasible in industry application.
- Besides the thermal noise, clock jitter also limits the achievable ADC performance. In recent years, the acievable SNDR of CMOS pipelined ADC presented in recent years is about 70dB. It's an important object to find out the other noise sources that limit the ADC performance.
- Another important aspect is the impact of deep sub-micron technology. In deep sub-micron technology, lower supply voltage is used to prevent the high-voltage stress on the thin gate oxide. This feature increases the turn-on resistance of the switch especially for the switch used to conduct a voltage of $V_{dd}/2$. This property may limit the operating speed of a SC circuit. Furthermore, the MOS gate leakage for the channel-length less than 65nm may not be negelected. The gate leakege may induce additional nonlineaity and limit the performance of high resolution ADCs.

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# Publication List

- Journal Paper:
  - **J.-L. Fan**, C.-Y. Wang, and J.-T. Wu, "A Robust and Fast Digital Background Calibration Technique for Pipelined ADCs," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 6, pp. 1213–1223, June 2007.
  - **J.-L. Fan** and J.-T. Wu, 'A 32-mW 12-Bit 80-MS/s Pipelined ADC with Digital Background Calibration," submitted to *IEEE Journal of Solid-State Circuits*.
- Conference Paper:
  - **J.-L. Fan** and J.-T. Wu, "A Robust Background Calibration Technique for Switched-Capacitor Pipelined ADCs," in *IEEE International Symposium on Circuits and Systems Digest of Technical Papers*, May 2005, pp. 1374–1377.
- Patent:
  - **J.-L. Fan** and J-T Wu, "Digital Background Calibration Technique for Amplifier Nonlinearity in ADCs," US/TW patent pending.