國 立 交 通 大 學

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可調式頻寬/增益之四通道生理訊號擷取晶片設計

Tunable BW/Gain Circuit Design of Four-Channel Bio-Signal Acquisition

研 究 生：戴毓廷

指導教授：林進燈 博士

中華民國 九十七 年 六 月

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研 究 生：戴毓廷　　Student：Yu-Ting Tai

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中文摘要

在人體所有的生理訊號中，其訊號振幅皆非常微弱，亦容易被受測者本身、量測環境及設備等因素所影響，故本論文提出適用於各種電生理訊號擷取之晶片設計。除了一般著重的低功率、低雜訊之外，同時提高共模訊號拒斥比(CMRR)與電源漣波拒斥比(PSRR)，並將整體多通道前端電路整合實現在單一晶片上，不需要任何外接元件，除了兼具成本與晶片面積效益，亦可降低因複雜的接線對生理訊號在量測時所造成的干擾，使後端處理及分析的訊號品質能夠更為精確。另外，在系統加入了數位控制介面，根據不同生理訊號的需求，利用數位訊號去控制選擇所要的訊號放大倍率與系統頻寬。

本論文所設計的生理訊號擷取晶片包含：電流平衡式儀表放大器(CBIA)、類比多工器、切換式電容低通濾波器(SCLPF)、非重疊時脈產生器(Non-Overlapping Clock Generator)及可程式增益放大器(PGA)等電路。整個電路設計使用 TSMC 0.18μm CMOS 1P6M 製程技術來實現，而整體晶片面積為 $0.823\times0.953\ mm^2$。由模擬結果顯示，在頻率 150Hz 下，可獲得 CMRR 135dB、PSRR+ 105dB，和 PSRR- 112dB 的效能。在操作電壓±0.75V 下，總消耗功率約 112.68μA，平均每一通道消耗功率約 28.17μA。

關鍵字：生理訊號，腦電圖，電流平衡式儀表放大器，切換式電容低通濾波器，可程式化增益放大器。

Tunable BW/Gain Circuit Design of Four-channel Bio-Signal Acquisition System

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Abstract

Due to properties of low-amplitude and non-stationary, most of biomedical signals are easily influenced by examined persons, measured environment, and electronic devices. A novel analog circuit design is proposed in this thesis, which is suitable for various biomedical signal acquisitions. In addition to the consideration of low power and low noise, the multi-channel analog front-end integrated circuit (AFEIC) is designed with high common-mode rejection ratio (CMRR) and high power supply ratio (PSRR). This circuit is realized into a single chip without any external component. It can not only reduce the number of outer components, but also enhance a better signal-to-noise ratio enormously. In addition, to select system gain and bandwidth corresponding to different amplitude and frequency of biomedical signals, the controllable digital interface was also designed and integrated into AFEIC.

In this thesis, AFEIC design is composed of four current-balancing instrumentation amplifiers (CBIA), one analog multiplexer, one switched-capacitor low-pass filter (SCLPF), one non-overlapping clock generator, and one programmable gain amplifier (PGA). These circuits have been integrated into a single chip of the total area of $0.823\times0.953mm^2$ by using TSMC 0.18μm COMS Mixed-Signal RF General purpose MiM Al 1P6M 1.8&3.3V process. For the simulation results, the proposed chip can achieve 135dB of CMRR, 105dB of PSRR+, and 112dB of PSRR- at 50Hz. The total power consumption is about 112.68μW under ±0.75V supply, and the power consumption is about 28.17μW per channel.

Keyword: Biomedical signal, electroencephalogram (EEG), current-balancing instrumentation amplifier (CBIA), switched-capacitor low-pass filter (SCLPF), programmable gain amplifier (PGA).

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Chapter 1
Introduction

1.1 Background

The medical application of science and microelectronic technology recently has made significantly advances, thus improving human quality of life. Biomedical instruments are crucial in modern life. The biomedical signal acquisition instrument has already developed years ago. However, the amplitude of the biomedical signals is all very weak. Biomedical signals are very easy to be influenced by testing environment and biomedical signals of the person who examined. These effects make recording biomedical signals become more and more difficult. Among them, the interferences of the testing environment are including the temperature and humidity of the electronic components, capacity effect of the pads, power supply variation, electromagnetic wave, digital noise, etc. The interferences of the biomedical signals are including electroencephalogram (EEG), electro-oculogram (EOG), electromyography (EMG), electrocardiogram (ECG), respiration, perspiration, etc. Therefore, we should amplify measured biomedical signals effectively and restrain noise by an analog front-end (AFE) circuit.

After an AFE circuit, the processed biomedical signals input an analog-to-digital converter (ADC), and then make further analysis via a computer or an embedded system. Amplifying the measured signals and restraining noise play important parts of the biomedical signal acquisition system. Fig. 1-1 shows the typical setup for an EEG recording system which comprises the instrumentation amplifier (IA) as analog front-end (AFE), the programmable gain amplifier (PGA) for boosting the acquired

EEG signal to levels for further analog signal processing [1]. Hence, the specification of analog front-end circuit affects the performance of the system directly.

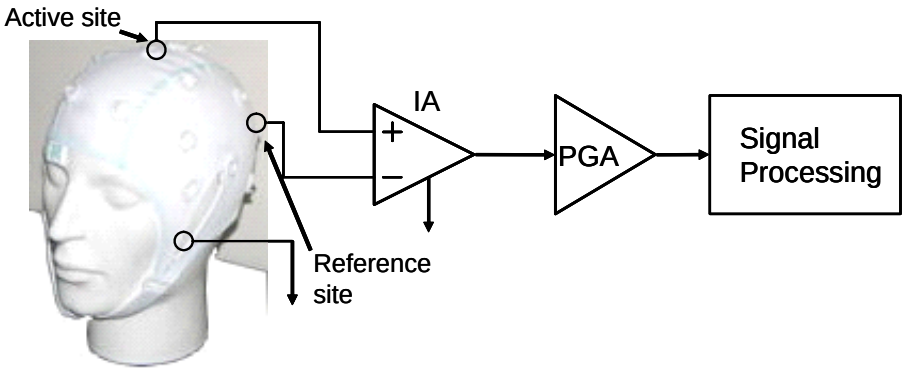

Fig. 1-1 Typical setup for EEG recording.

The instrumentation amplifier [2][3][4][5] has already used in the analog front-end circuit of the biomedical signals recording system widely. The greatest advantages are effective restraining noise such factors as the measuring environment, electrical electrode, etc. and amplifying the weak biomedical signals to observable signals. Therefore, noise interference cannot lead to the signals distortion. Since all biomedical signals are low frequency signals, and the frequency of the noise is usually higher than the biomedical signals, the circuit in this study has a low-pass filter after an instrumentation amplifier. The low-pass filter goes one step future to get rid of noise [5][6][7] to assure the quality of the signals.

This research is the first stage in the biomedical signal acquisition and analysis system, so the performance of gain and restraining noise is extremely important. Its result will influence the efficiency of the whole system. The first generation analog front-end circuit of the biomedical signal recording system has been developed in our laboratory, and has already been accepted by 2008 IEEE International Symposium on Circuits and Systems [8]. This research direction and achievement are received the

affirmation by the international academia. We will be devoted to this future development of the research base on the research results.

1.2 Motivation

Medical treatment progresses more and more in recent years. Besides improving the medical technology that has already had, gradually paying attention to the important representative information of biomedical signals is sent out from our body each position. Examine and analyze these biomedical signals can go a step future to find out about the state of the body.

Giving an example of EEG, analyzing the potential signal of human brain is researched from Berger, etc. proposed in 1920 time. EEG is produced by many accumulated current of nerve cells under cerebral cortex. Through the research of decades, we can learn the state of mind of the persons who are examined EEG from the measured results [9][10]. Nevertheless, complicated EEG signals can be few processed to study. Computer operation is faster and faster in speed and the algorithms are progressing excellently in recent years, so processing measured EEG signals is enough for real-time. People pay attention to the discussion of human spiritual information gradually. The traditional EEG recording system is shown in Fig. 1-2. This system is composed of an international 10-20 electrode placement system as Fig. 1-3, a biomedical signal amplifier, an analog-to-digital converter (ADC), and a computer. Because the instrument of recording and analyzing is very bulky, it is very inconvenient to use. The difficult problems of reducing systematic volume and simplifying difficulty use of the system should be overcome.

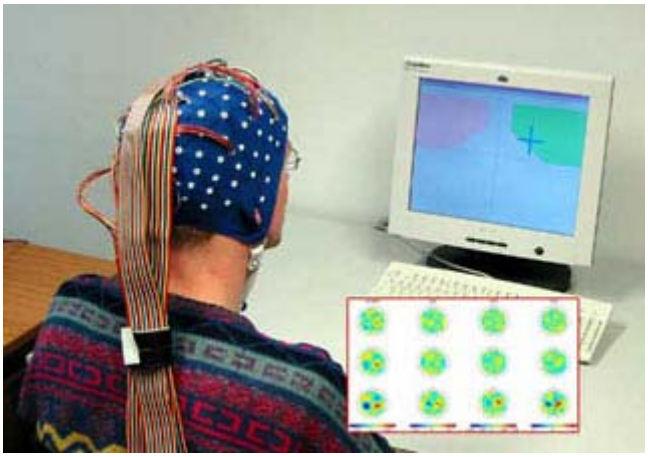

Fig. 1-2 Traditional EEG recording system.

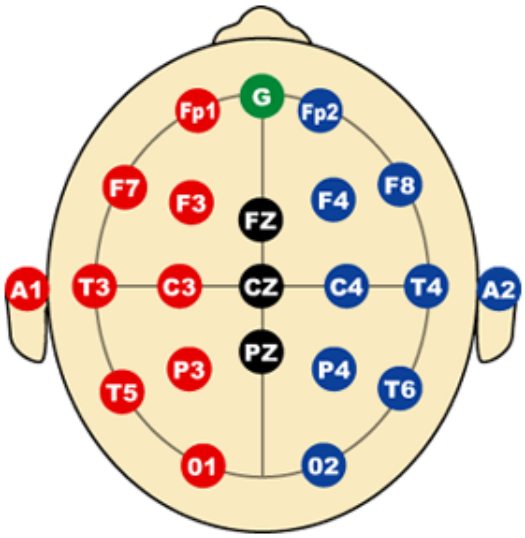

Fig. 1-3 International 10-20 electrode placement system.

Generally, the commonly used biomedical signals of body have the characteristics illustrated in Table 1, including EEG, EOG, EMG, ECG. Biomedical signals are all distributed over ultra-low amplitude and ultra-low frequency, so they are hard to process. For this reason, how to receive and amplify the real biomedical signals that are not distortion is an important issue in this study. Its frequency or amplitude is not a constant value even if it is the same kind of biomedical signals. So

the signals must have different bandwidth and different voltage gain.

Table 1 The characteristics of biomedical signals.

Biomedical signal	Amplitude distribution	Frequency distribution
EEG	1μV~100μV	DC~150Hz
ECG	100μV~10mV	0.01Hz~250Hz
EOG	10μV~10mV	DC~100Hz
EMG	10μV~10mV	20Hz~1kHz

Furthermore, the use of very large scale integrated circuits (VLSI) dominates medical electronics applications, which range from small, battery-powered electronic implants to room-filling diagnostic imaging systems [11]. As in other VLSI applications, the design and processing of the technology chosen for medical devices depends on the specific applications involved. Product complexity, size, sales volume, cost objectives, and available power source all play significant roles in the specific process [12]. The fabrication of VLSI may be based on the bipolar, CMOS or BiCMOS technologies. However, portable instruments and implantable products, where low power consumption is a necessity, primarily use CMOS devices. CMOS technology has become popular in the last few years for implementing complex circuits and systems. The integration of the AFE circuit and other processing units on the same chip has brought a new era in biomedical systems [13][14][15]. The cost of electronic instruments is proportional to their size, the number of devices and interconnections they contain. VLSI circuits have done a great deal to reduce size, components, and interconnections, and thus the cost of the products that contain them.

This study realized an AFE circuit design which is suitable for a portable

biomedical signals recording system [2][16][17][18]. It combines the system on a chip (SoC) and needs no external components. It reduced the area and cost of the circuit effectively, in order to combine with ADC and embedded system in the future. This study expanded the applications of the circuit. In addition, it has joined the digital controlling interface in the circuit. The user can choose the proper gain and bandwidth according to different characteristics of biomedical signals. The AFE circuit can amplify biomedical signals to the range that can be observed and filter out the noise besides the bandwidth of biomedical signals. Consequently, the systematic structure could measure many kinds of biomedical signals. Additionally, the circuit reduces the supply voltage to +/- 0.75 Volt. For this reason, the AFEIC reduces power consumption and increases the measured time of the system.

1.3 Thesis Organization

The thesis is organized as follows. Chapter 2 describes the development of analog front end circuit for biomedical signal acquisition. Descriptions of AFEIC design are in Chapter 3. Then the circuit performance and testing platform are presented in Chapter 4. Finally, a summary of this thesis research and future work is briefly concluded by Chapter 5.

Chapter 2
Development and Critical Issue of Analog Front-End Integrated Circuit

The chapter introduced critical issues concerning the design of a high performance analog circuit and the development of the analog front-end circuit in a biomedical signals acquisition system.

2.1 Current-Balancing Instrumentation Amplifier (CBIA)

Rui Martins et al. proposed a CMOS IC for portable EEG acquisition systems in 1998 [2].Besides low power, the key design points are high common mode rejection ratio (CMRR) and very low noise. Minimum component count is also important to reduce system weight and volume. The system includes 16 instrumentation amplifiers, one 16-to-1 analog multiplexer, a microprocessor compatible digital interface, and an internal current/voltage reference source as shown in the block diagram of Fig. 2-1.

The basic functional block diagram of current feedback amplifiers is presented in Fig. 2-2. Analyzing the input branch of this figure, we conclude that high input impedance is guaranteed by two unity gain buffers. Utilizing the current feedback, by the ratio of input impedance and output impedance to determine voltage gain, and reach high CMRR.

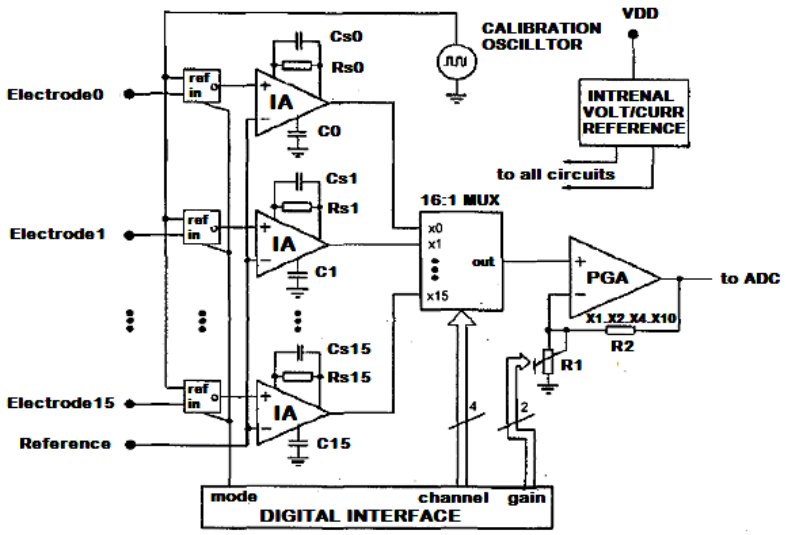

Fig. 2-1 IC block diagram [2].

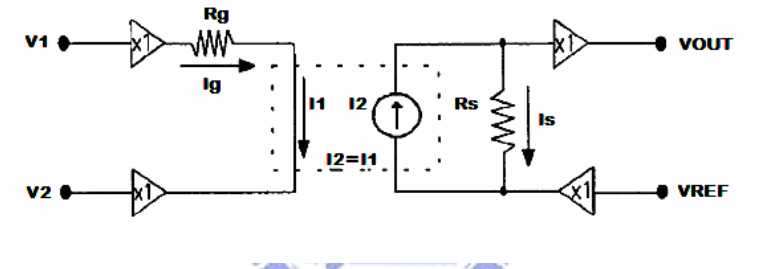

Fig. 2-2 Block diagram of an IA with current feedback [2].

Design the concept as the following Eqs. (2-1)(2-2)(2-3)(2-4)(2-5)(2-6).

$$i_g = \frac{1}{R_s} \cdot (v_1 - v_2) \tag{2-1}$$

$$i_1 = i_g = i_2 = i_s \tag{2-2}$$

$$v_{out} = R_s \cdot i_s + v_{ref} \tag{2-3}$$

$$i_{Rg} = \frac{v_1 - v_2}{R_g} \tag{2-4}$$

$$i_{Rs} = \frac{v_{out} - v_{ref}}{R_s} \tag{2-5}$$

$$v_{out} = \frac{R_s}{R_g} \cdot (v_1 - v_2) + v_{ref} \tag{2-6}$$

But it is important to note that, contrary to the classical configuration with three operational amplifiers, there is no global feedback (from the output to the input) and that there is only one high impedance node, which simplifies the frequency compensation. Another advantage is the CMRR do not depend on any matching of resistor values. The resistor count is also reduced, saving chip area.

They implemented a CMOS variation of [19], as with this configuration only a reduced number of stacked transistors is necessary (improving dc behavior at low voltage power supply) and only two transistors at input are needed. Also, as PMOS transistors exhibit low flicker noise for the same area, we chose them to the input as shown in Fig. 2-3.

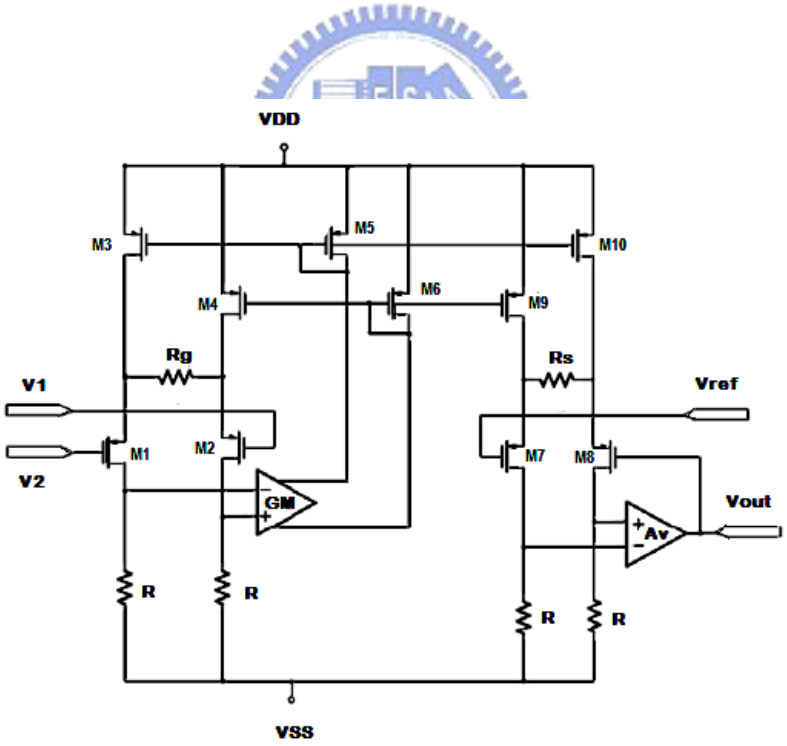

Fig. 2-3 Simplified IA circuit [2].

In order to realize high pass filter function, it was implemented using another feedback loop around the output circuit, as shown in Fig. 2-4. The complete circuit of

the IA is shown in Fig. 2-5.

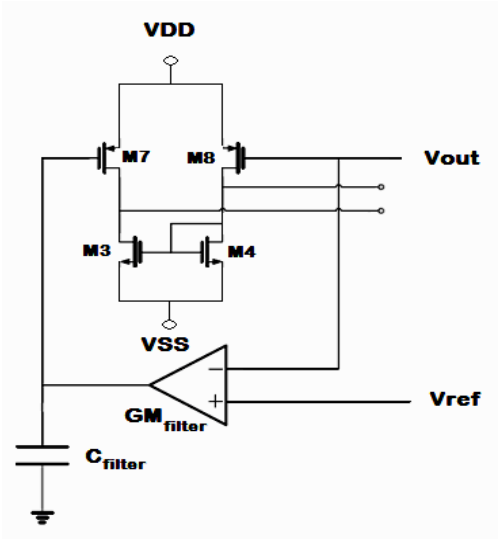

Fig. 2-4 Feedback look realizing the high pass filter function [2].

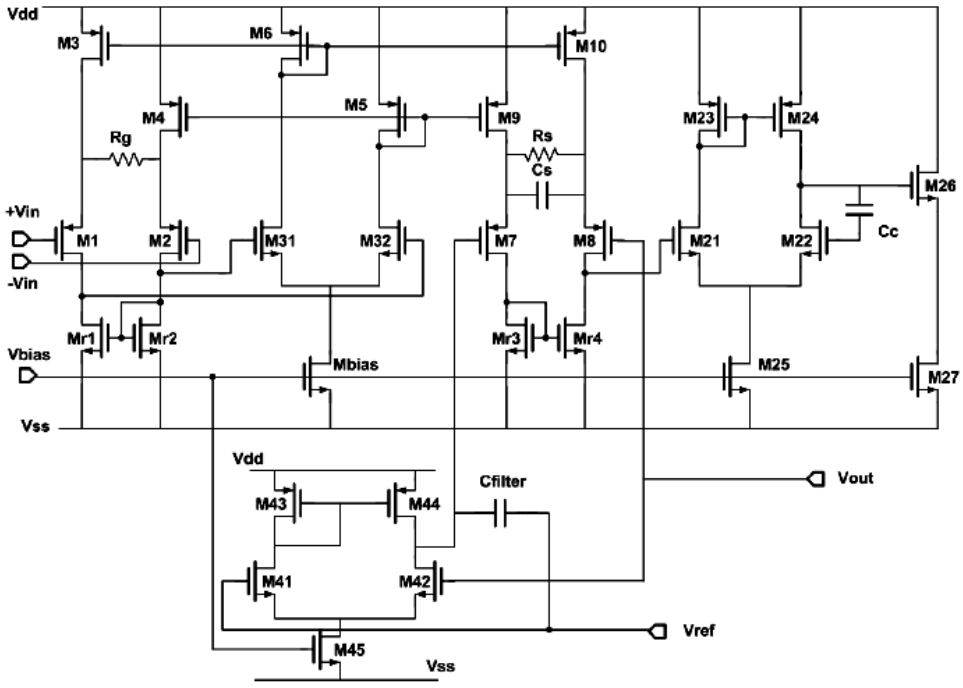

Fig. 2-5 Complete circuit of the IA [2].

2.2 Rail-to-Rail Instrumentation Amplifier

K. A. Ng and P. K. Chan proposed a CMOS analog front-end (AFE) IC for portable EEG/ECG monitoring applications in 2005[20]. The proposed AFE system chip is shown in Fig. 2-6. A promising approach is the differential difference amplifier (DDA) based non-inverting IA [21][22], which has favorable properties such as simplicity and acceptable low power dissipation. Fig. 2-7 shows the basic DDA non-inverting amplifier.

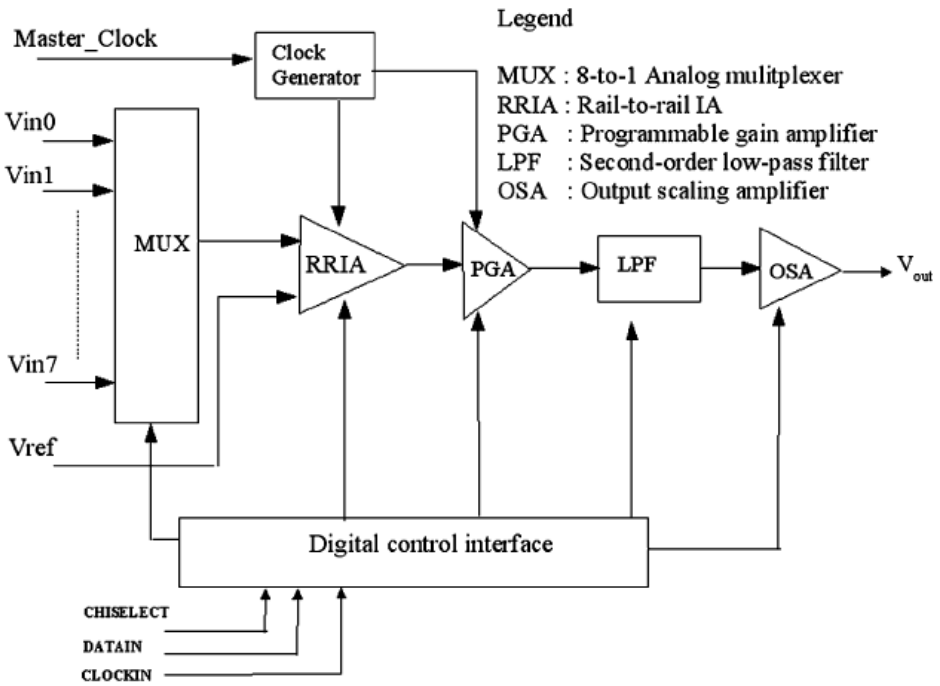

Fig. 2-6 System block diagram of the proposed AFE IC [20].

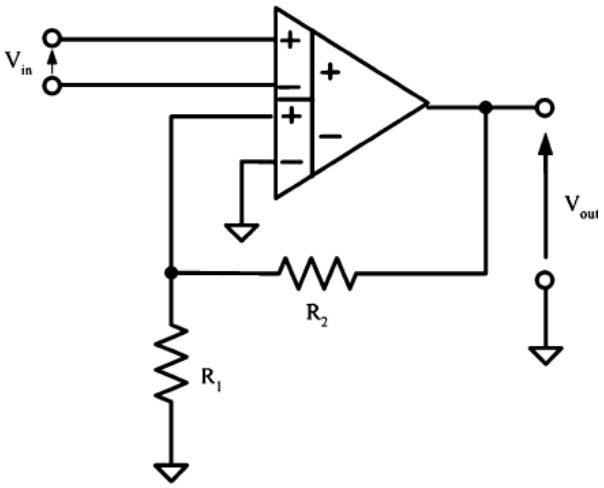

Fig. 2-7 Non-inverting DDA for use an IA [20].

The input and output relation of non-inverting DDA is defined as (2-7). The major advantage of the DDA non-inverting amplifier over the typical IA is it requires an active amplifier and two resistors to set the instrumentation gain. In this DDA-based design, the CMRR is related to the mismatch of the input ports. Mismatch between resistors R_1 and R_2 only affects the gain factor, but it does not degrade the CMRR of the amplifier.

$$V_{out} = V_{in} \times \left(\frac{R_2}{R_1} + 1 \right) \tag{2-7}$$

Fig.2-8 is a circuit schematic of the PMOS differential-input chopper-stabilized differential difference amplifier (CHSDDA). It joined a chopper-stabilized skill in the circuit to reduce flicker noise and DC offset voltage.

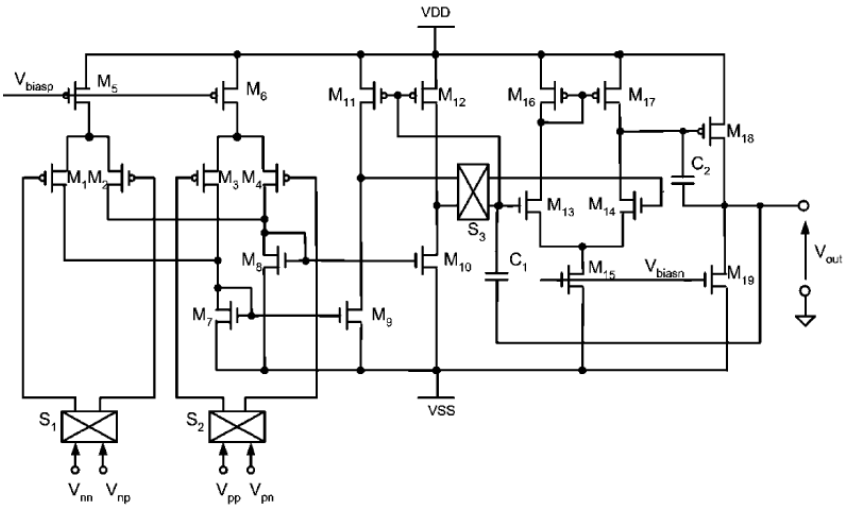

Fig. 2-8 Circuit schematic of the PMOS CHSDDA [20].

A new rail-to-rail input IA is proposed in Fig. 2-9, which shows the filtering circuits added to the basic chopper-stabilized DDA non-inverting amplifier for suppressing this input DC offset voltage. In this realization, two CHSDDAs are arranged in parallel configuration. Input pairs are NMOS and PMOS separately, guarantee to normal running of the circuit in any input common mode voltage. In addition, the circuit added an external RC band pass filter to eliminate noise outside the frequency bandwidth of biomedical signals.

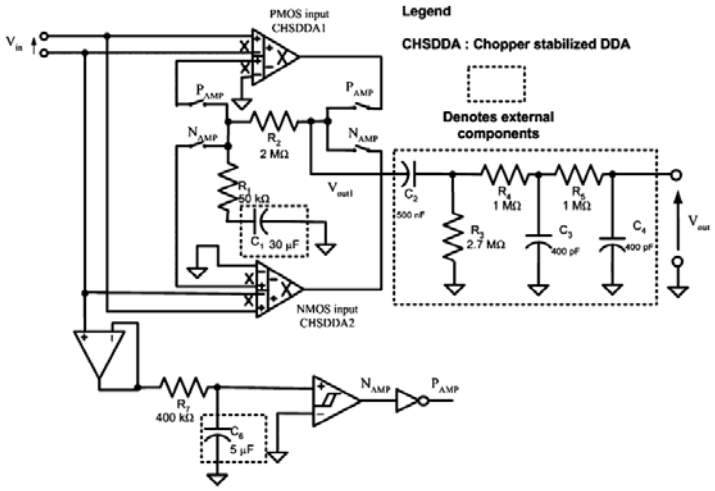

Fig. 2-9 Proposed rail-to-rail IA [20].

Fig. 2-10 shows the conceptual circuit block diagram of the chopper-stabilized DDA circuit. The two pairs of input differential voltage signals are modulated concurrently and translated to the current signals via the trans-conductance cells having identical trans-conductance gain of *Gm*.

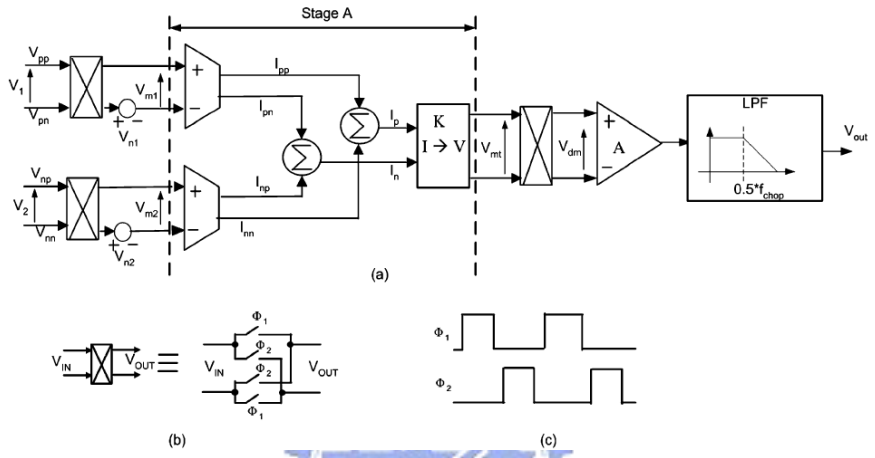

Fig. 2-10 CHSDDA and its associated clock for the chopping switches [20].

Because the chopper-stabilized circuit utilizes clock to control the switches, it could produce the high frequency noise. In order to reduce the influence, it must join a low pass filter used to except the switch noise.

The programmable gain amplifier (PGA) provides further amplification with respect to the output of the rail-to-rail IA. To prevent the input impedance of the amplifier from loading the band pass filter output of the rail-to-rail IA, a non-inverting configuration is used. Note that the first chopper-stabilized stage inside the PGA is derived from the CHSDDA by just removing one input differential port. By digitally connecting the resistors via CMOS switches, the amplifier provides programmable voltage gain

2.3 AC Coupled Chopped Instrumentation Amplifier

Refet Firat Yazicioglu et al. proposed low-power low-noise 8-channel EEG front-end ASIC for ambulatory acquisition systems in 2006 [16]. Fig. 2-11 shows the architecture of the implemented 8-channel EEG readout front-end ASIC. Each channel of the ASIC consists of an instrumentation amplifier (IA), a spike filter (SF), a fixed gain stage, a variable gain amplifier (VGA) stage, and a channel buffer.

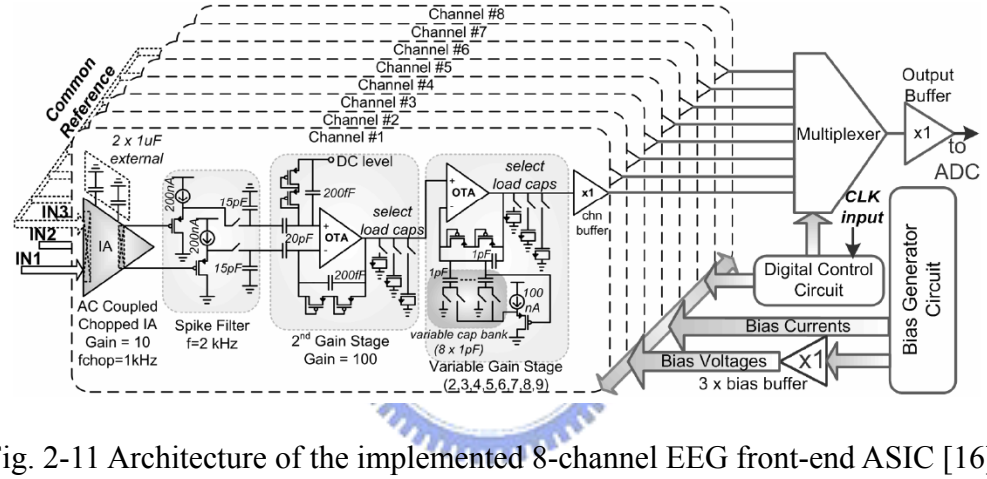

Fig. 2-11 Architecture of the implemented 8-channel EEG front-end ASIC [16].

The IA defines the noise level and CMRR of the channel, and filters the electrode offset. The second gain stage further amplifies the output of the IA and also serves as a differential to single-ended converter. The VGA is used to adjust the gain of the channels for different applications. A multiplexer, time multiplexes the output of each channel. Moreover, a bias generator and a digital control circuit generate the bias currents and digital signals for the ASIC, respectively.

Fig. 2-12 shows the implemented current feedback instrumentation amplifier (CFIA) architecture. The presented CFIA consists of only 4 main parallel branches to minimize the power dissipation, and the ratio of two resistors defines the gain (R2/R1).

On the other hand, flicker noise and process related mismatches still put a limit on the minimum achievable power dissipation and CMMR. A commonly used technique to eliminate flicker noise and to achieve high CMRR is called chopping [23]. However, conventional chopping amplifiers are inherently DC coupled devices. Fig. 2-12 shows the architecture of the implemented AC coupled chopped IA.

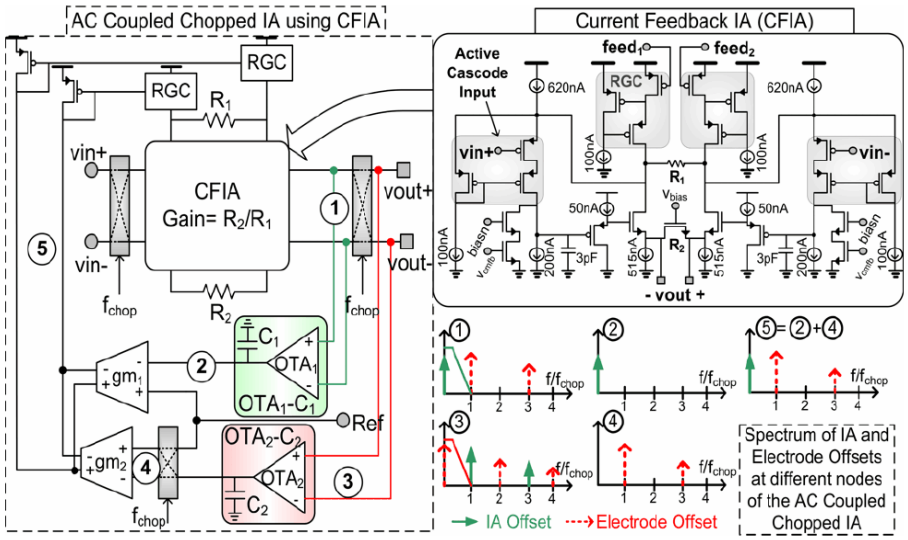

Fig. 2-12 CFIA architecture and the AC coupled chopped IA topology [16].

Fig. 2-13 shows the block diagram of the digital control circuit. It generates the necessary clock signals for the AC coupled chopped IA, the spike filter and the output multiplexer from a single clock input. Additionally, this block generates a sync-signal that can be used to synchronize the ASIC with an ADC. A non-overlapping clock generator supplies the chopping signal for the chopping switches of the AC coupled chopped IA.

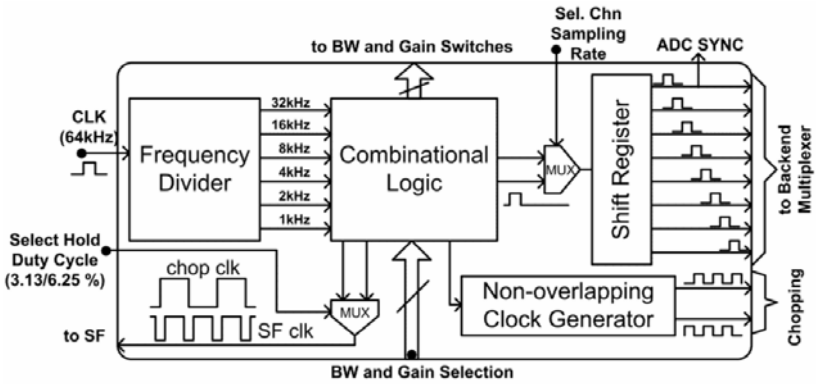

Fig. 2-13 Block diagram of the digital control circuit [16].

Refet Firat Yazicioglu et al. proposed a 60 uW 60 nV/$\sqrt{Hz}$ readout front-end for portable bio-potential acquisition systems in 2007 [6]. The architecture of the front-end acquisition system is shown as Fig. 2-14. The readout channel of the system consists of the AC coupled chopped instrumentation amplifier (ACCIA), a chopping spike filter (CSF) stage, a digitally programmable gain stage and an output buffer.

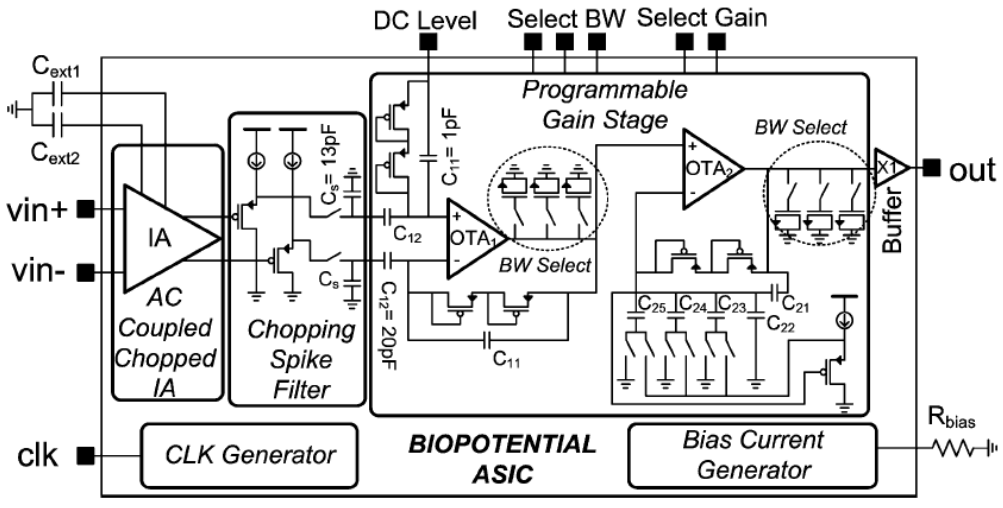

Fig. 2-14 Architecture of the bio-potential readout front-end for the acquisition of EEG, ECG, and EMG signals [6].

The concept of the ACCIA is shown in Fig. 2-15. DC input voltage which is the

offset voltage is modulated by the input chopper and copied to the terminals of R_1. The voltage creates a current through R_1 which is copied to R_2 and defines the output voltage after demodulation by the output chopper. A trans-conductance stage *GM* with trans-conductance and low pass cut-off frequency f_p filters the DC component of the output and converts it into current. The transfer function of the architecture is as (2-8), assuming low pass cut-off frequency of the ACCIA $f_{LP,IA}$ is much larger than f_{chop} and $gmR_2>>1$.

$$\frac{V_{out}}{V_{in}}(s)=\frac{R_2}{R_1}\frac{s+2\pi f_p}{s+gmR_2(2\pi f_p)} \tag{2-8}$$

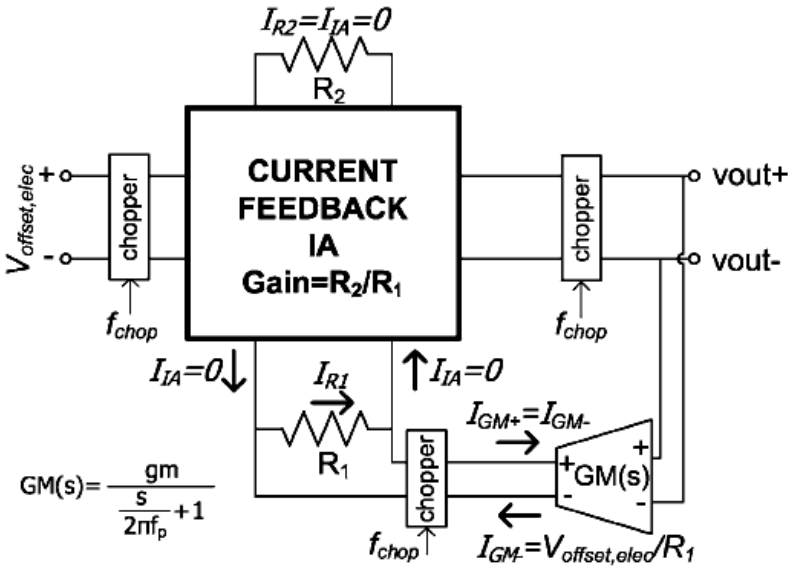

Fig. 2-15 Concept of the ACCIA [6].

On the other hand, the noise of the IA is only modulated by the output chopper. Therefore, the output noise power spectral density of ACCIA, S_{ACCIA}, can be expressed in terms of the output noise power spectral density of the IA, S_{IA}, as (2-9).

$$S_{ACCIA}(f)=\left(\frac{2}{\pi}\right)^2\sum_{\substack{n=-\infty\\ n=odd}}^{+\infty}\frac{1}{n^2}S_{IA}(f-nf_{chop})$$
$$\cong S_{IA,white}(f) \tag{2-9}$$

If $f_{LP,IA}>>f_{chop}$ and the flicker noise corner frequency of the current feedback IA is smaller than $f_{chop}/2$, $S_{IA,white}$ [23]. As a result, while flicker noise of the current feedback IA is eliminated by chopping, the electrode offset is filtered by the feedback loop implemented by *GM*. Fig. 2-16 shows the implementation of the concept presented Fig. 2-15. This architecture can eliminate flicker noise, and external circuit reduces the offset voltage is presented by electrode and IA. The GM is implemented by the OTA_2-C_{ext2} filter and the trans-conductance stage, gm_2. This results in an equivalent trans-conductance of A_v gm_2, where A_v is the voltage gain of OTA_2. By replacing gm of (2-8) with $A_v gm_2$ and f_p with $gm_{OTA2}/(A_v C_{ext2})$, high-pass cut-off frequency of the ACCIA, $f_{HP,ACCIA}$, is shown as (2-10).

$$f_{HP,ACCIA}=\frac{1}{2\pi}R_2 gm_2\left(\frac{gm_{OTA2}}{C_{ext2}}\right) \tag{2-10}$$

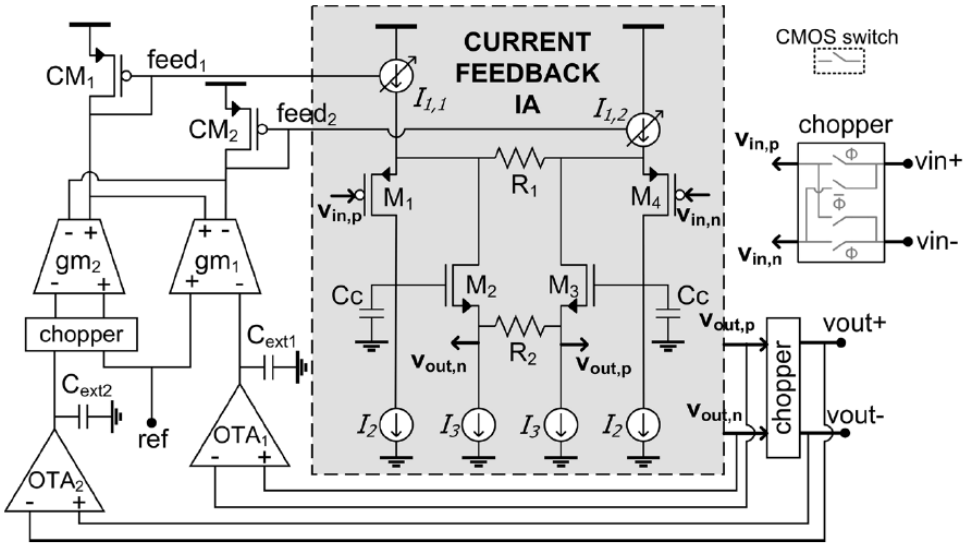

Fig. 2-16 ACCIA implemented circuit [6].

OTA_2 is implemented as a current mirror OTA as Fig. 2-17(a), where is reduced using a series parallel division of current [24]. The gm2 stage is implemented as a basic differential stage as Fig. 2-17(b), which acts as a voltage to current converter. The combination of the two feedback loops cancels both different electrode offset (DEO) and the IA offset.

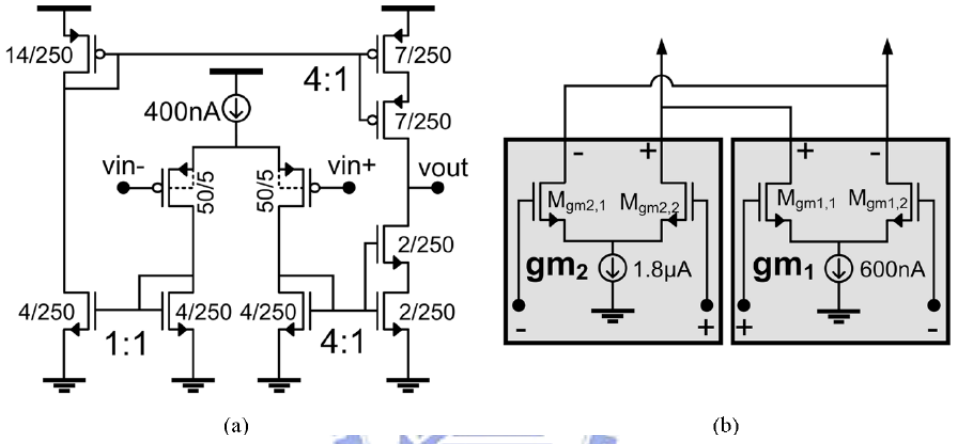

Fig. 2-17 Schematic of OTA [6].

(a) OTA_1-$C_{ext1}$and OTA_2-C_{ext2} implemented circuit

(b) gm_1 and gm_2 implemented circuit

Fig. 2-18 shows the complete schematic of the implemented current feedback IA. All the current sources are implemented by paralleling the unit cascode current source, M_{SN1}, M_{SN2} for NMOS current sources and M_{SP1}, M_{SP2} for PMOS current sources. Current sources $I_{1,1}$ and $I_{1,2}$ are implemented by combining a fixed current source and a regulated cascade current mirror. R2 is implemented with a NMOS transistor so that the gain of the IA can be continuously adjusted. The source follower stages, which consist of transistors and act as level shifters in order to maximize the input-output voltage swing of the IA

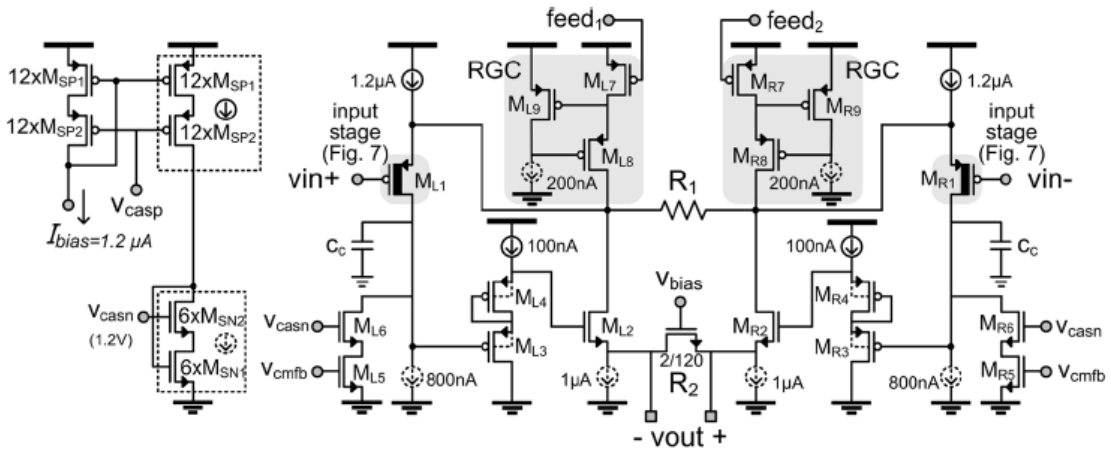

Fig. 2-18 Schematic of current feedback IA is used in ACCIC implementation [6].

Fig. 2-19 shows the implemented chopping spike filter (CSF) stage. Before the appearance of the chopping spike, output is sampled to the capacitor and during the presence of a chopping spike, switch S is opened and output is held on the capacitor.

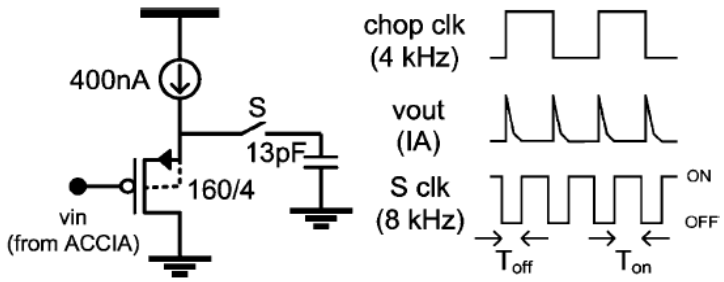

Fig. 2-19 Schematic of CSF and operation principle [6].

A continuous-time variable gain amplifier (VGA) stage with digitally controllable gain is shown as Fig.2-20. Pseudo-resistors are used in order to set the DC level at the inverting node of the OTA. The VGA transfer function of the VGA is shown as (2-11).

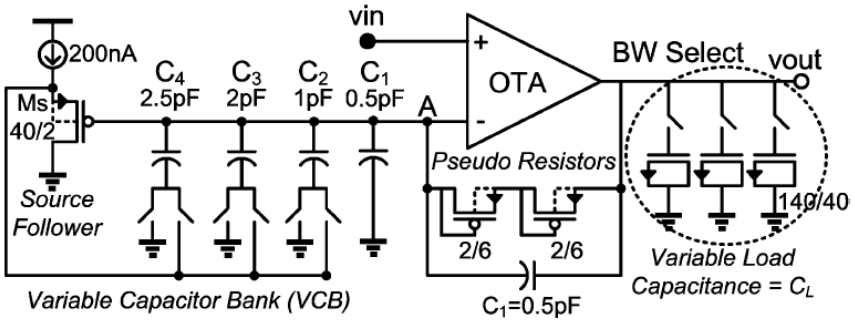

Fig. 2-20 Schematic of the VGA [6].

$$A_v(s) = \frac{\left\{1 + \frac{C_T}{C_1}\left[\frac{\left(s + \frac{1}{C_T R_{par}}\right)}{\left(s + \frac{1}{C_1 R_{eq}}\right)}\right]\right\}}{\left[s\left(\frac{C_T}{C_1}\frac{C_L}{gm_{OTA}}\right) + 1\right]} \tag{2-11}$$

2.4 Critical Issues Concerning the Design of a High Performance Analog Circuit

Biomedical signals have very low voltage amplitude from 1μV to 10mV and very low frequency range of DC~1kHz, so noise is a very important issue in the analog circuit design. The power consumption is the other significant aspect for a portable system, because it governs the lifetime of a battery.

2.4.1 Noise

Noise is an important consideration in the analog circuit design, since it needs lots of design trade-off. Noise performance is a critical concern when biomedical

signals must be amplified. The optimization of noise performance is complex and involves many parameters. Parameters that can be manipulated to optimize the noise performance are including the size of the device, bias current, the type of the device, circuit impedance and circuit topologies. Noise arises because electric charge is not continuous but is carried in discrete amounts equal to the charge of an electron. In electronic circuits, noise is reduced the voltage limit below which electrical signals cannot be amplified without substantially degrading the signal.

Noise represents a fundamental limit on the performance of the analog circuit. For example, EEG signals contain information of interest over a bandwidth of DC~150 Hz, and they have a dynamic range from 1 μV to 100 μV. Although the EEG carries useful information outside this bandwidth, the signal-to-noise ratio (SNR) declines abruptly there. Principle noise sources below 0.05 Hz include the electrode offset drift and the respiration-induced muscle artifact. Above 150 Hz, muscle tremor and thermal noise are problems. Unfortunately, the bandwidth of the EEG spans around DC~150Hz, so some means of power noise rejection is essential.

(1) Thermal Noise

Thermal noise [25][26][27][28] is generated by a completely different mechanism from shot noise. In conventional resistor it is due to the random thermal motion of the electrons and is unaffected by the presence or absence of direct current, since typical electron drift velocities in a conductor are much less than electron thermal velocities. Since the source of noise is due to the thermal motion of electrons, we expect that it is related to absolute temperature *T*. In fact, thermal noise is directly proportional to *T* and as approaches zero, thermal noise also approaches zero.

In a resistor R, thermal noise can be shown to be represented by a series voltage

generator $\overline{v^2}$ as shown in Fig. 2-21. These representations are equivalent as (2-12).

$$\overline{v^2} = 4kTR\Delta f \tag{2-12}$$

Where k is Boltzmann's constant. Equation (2-12) shows that the noise spectral density is again independent of frequency. Thermal noise is a fundamental physical phenomenon and is present in any linear passive resistor.

Fig. 2-21 Alternative representation of thermal noise.

(2) Flicker Noise (1/f Noise)

This is a type of noise in all active devices, as well as in some discrete passive elements such as a resistor. The origins of flicker noise [25][29][30][31] are varied, but it is caused mainly by traps associated with contamination and crystal defects. These traps capture and release carriers in a random fashion and the time constants associated with the process give rise to a noise signal with energy concentrated at low frequencies.

Flicker noise, which is always associated with a flow of direct current, displays a spectral density of the form (2-13).

$$\overline{i^2} = K_1 \frac{I^a}{f^b} \Delta f \tag{2-13}$$

where

Δf =small bandwidth at frequency *f*,

I=direct current,

K_1=constant for a particular device,

a=constant in the range 0.5 to 2,

b=constant of about unity.

If *b*=1 in (2-13), the noise spectral density has a 1/f frequency dependence as shown in Fig. 2-22. It is apparent that flicker noise is most significant at low frequencies, although in devices exhibiting high flicker noise levels. This noise source may dominate the device noise at frequencies well into the megahertz range.

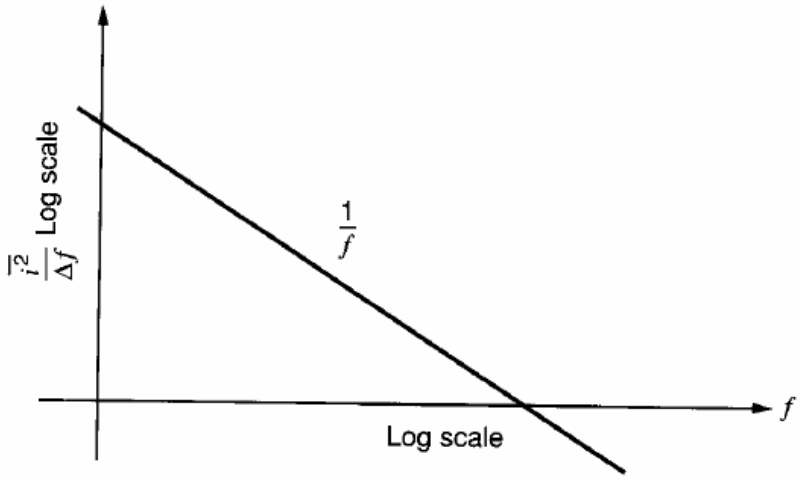

Fig. 2-22 Flicker noise spectral density versus frequency.

(3) Charge Injection

Charge injection [32] occurs by channel charge when MOS switches turn off. From Fig. 2-23 we can see the channel charge flow out from the channel region of the

transistor to the drain and source junctions. The channel charge of a transistor had zero drain-source voltage is given by (2-14).

$$Q_{ch} = WLC_{ox}V_{eff} = WLC_{ox}(V_{gs} - V_t) \tag{2-14}$$

And we derive voltage error due to charge injection is given by (2-15).

$$\Delta V = -\frac{1}{2}Q_{ch} \cdot \frac{1}{C_l + C_{ov}} \approx -\frac{WLC_{ox}(V_{gs} - V_t)}{2C_l} \tag{2-15}$$

Switches connected to analog ground and virtual ground will cause signal-independent error because its turn-on voltage is constant. Besides these, switches connected to the signal will cause signal-dependent error which is changed with signal. Signal-dependent error is important because it truly affects resolution of the circuit. Therefore, How to reduce this kind of errors is the critical issue when we design switches of switch capacitor filter.

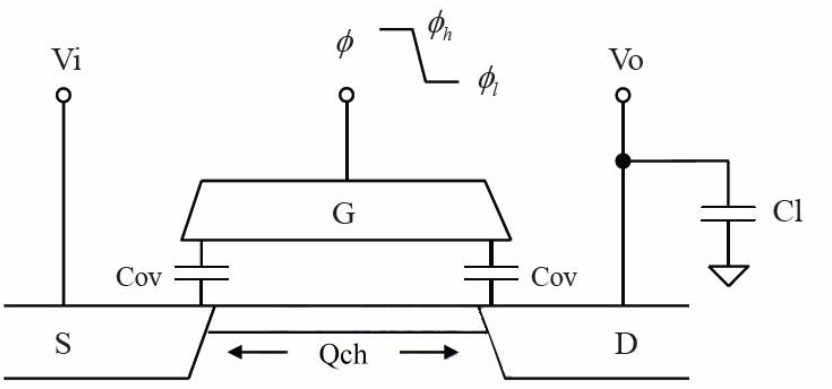

Fig. 2-23 Non-ideal effects of MOS switch.

2.4.2 Power Consumption

Power consumption in the analog circuit affects performance and price. High power consumption is bad for a system since it requires the use of more advanced packaging and heat removal technology. A portable electronic device is limited by

battery life. For the reason, power consumption is an essential issue in the analog circuit design.

An analog circuit that operates at high supply voltage commonly has more power consumption. We should implement the circuit that is operated at low supply voltage. Operation amplifiers dissipate most of the power of the analog circuit. Accordingly, a low supply voltage and low power consumption operation amplifier must be developed for use in the analog circuit.

Chapter 3
Tunable Bandwidth and Gain Circuit Design of Four-channel Bio-Signal Acquisition

This chapter introduces the design and consideration of the complete analog front-end integrated circuit (AFEIC) from every stage circuit design, simulation, and verification.

3.1 System Architecture

This study aims to develop a bandwidth/gain tunable, low noise, low power and multi-channel analog front-end integrated circuit (AFEIC) for patient's biomedical signals monitoring. It amplifies the measured signals and filters other noise and makes these signals become to the meaningful information. Because the biomedical signals distribute over the very weak amplitude and very low frequency, they must be processed by AFEIC before input the analog-to-digital converter (ADC) and input the computer or embedded system to analyze. AFEIC is divided into three parts, that including instrumentation amplifier (IA), low-pass filter (LPF), and operation amplifier (OP). The general AFEIC for biomedical signals also includes the three parts.

However, the measured node of the biomedical signals is not only one node, so the AFEIC is a multi-channel design to cooperate to measure conditions practically. The structure of the AFEIC is shown as Fig. 3-1. It is composed of four IAs, a four-to-one analog multiplexer, one switched-capacitor low-pass filter (SCLPF), one

programmable gain amplifier (PGA), and a digital controlling interface with a clock generator, and a two-to-four decoder.

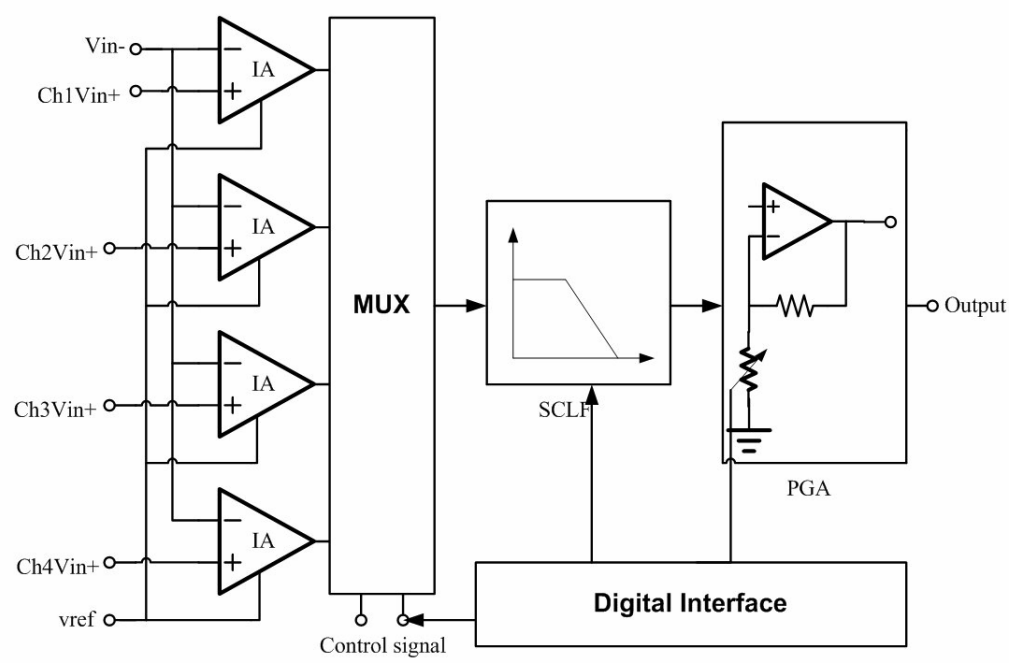

Fig. 3-1 The structure of the AFEIC.

In this structure of AFEIC, the first stage IA initially amplifies the weak biomedical signals which are received by electrodes. Moreover, it can eliminate common mode noise and increase signal-to-noise ratio (SNR) by the characters of high input impendence and high common mode rejection ratio (CMRR). The area of the IA in this AFEIC is much smaller than a typical voltage mode IA [33]. Four IAs share one resistor of IA, and four channels share one SCLPF and a PGA to save more area and cost based on a portable system.

After the biomedical signals input the first stage IA to amplify initially and eliminate common mode noise, they input the second stage SCLPF in order to filter the high frequency noise over the biomedical signals bandwidth to assure accuracy of the weak biomedical signals. The general biomedical signals bandwidth is all within

1kHz. If the AFEIC uses an active filter, the equivalent resistor and capacitor are very large, and it is not suitable for IC fabrication. If it uses external resistors and capacitors, the AFEIC cannot realize the system on chip (SoC). Using external components increases size of the circuit, and it is not proper for a portable system. For the reason, the AFEIC used a SCLPF, and it utilized the property of switch and capacitor to simulate an equivalent resistor. If the AFEIC needs to acquire different biomedical signals, it only adjusts switch clock to different bandwidth for the filter. Therefore, it makes the applications of AFEIC more elastic.

Due to the amplitude of all biomedical signals are very weak and not a constant value, it is changed by different patients, electrodes, measured environment, etc. so AFEIC is not adequate for the same voltage gain. Consequentially, in the AFEIC we used a PGA, which utilized a digital controlling interface to tune a property voltage gain, in order to assure the output signals from the ADC correctly. If input signals of the ADC are too small, the errors of output signals are very large. If input signals are too large, they will lead the output signals of the ADC to saturation.

In addition to low noise, high common mode rejection ratio (CMRR), high power supply rejection ratio (PSRR) and SoC in the first generation AFEIC, this generation AFEIC has lower power consumption, multi-channel, shared a resistor in the four IAs, lower area, and lower cost. Furthermore, we considered the influence of the high frequency noise, which is produced by switched-capacitor filter, and avoided the digital noise affecting the operation of the AFEIC.

3.2 Circuit Design

The structure of AFEIC is divided into three parts mainly. The first stage is a

current balancing instrumentation amplifier (CBIA), the second stage is a switched-capacitor low-pass filter (SCLPF), and the third stage is a programmable gain amplifier (PGA). In addition, the circuit has a four-to-one analog multiplexer to select each channel for this four-channel AFEIC, a clock generator to change switch frequency in the second stage, and a two-to-four decoder to choose different voltage gain in the third stage.

3.2.1 Current-Balancing Instrumentation Amplifier (CBIA)

The common instrumentation amplifier (IA) is mainly divided into a voltage mode IA and a current mode IA. The voltage mode IA reaches high CMRR by the resistors matching among them. The voltage mode IA is not a good choice, owing to the bulky area of passive elements (resistor or capacitor) on the chip and sensitive CMRR to resistors matching. The current mode IA is better than the voltage mode IA because voltage gain of the current mode IA is decided by only two resistors and the current mode IA attains to high CMRR at the same time. The resistor matching affects few CMRR in the current mode IA.

After considering the circuit area, manufacture variation, circuit characteristics, and reference papers, the structure of CBIA is the best choice in IA structure. In addition, in order to improve CMRR further, we utilized the high-swing cascode current mirror [34], which is shown as Fig. 3-2, to replace the common simple current mirror in the current transmission part. The function of the high-swing cascode current mirror is increasing the current mirror output impendence to reach high CMRR [35][36]. Furthermore, to reduce the area of the AFEIC, we put two switches, S1 and S2, in the resistor R_g both end. They make four CBIAs share the larger resistor R_g which decides the gain. And the controlling circuit of the switches, S1 and S2, is

shared the decoder in the multiplexer, it gains two advantages by a single move. The architecture of the CBIA is shown as Fig. 3-3.

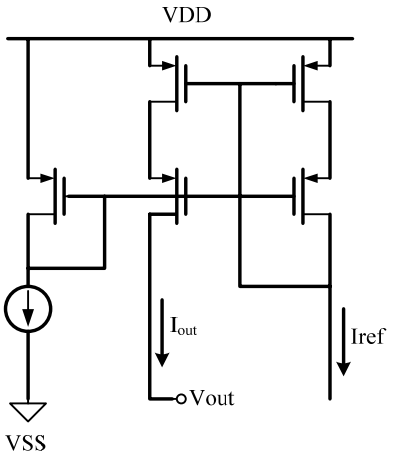

Fig. 3-2 The structure of the high-swing cascode current mirror.

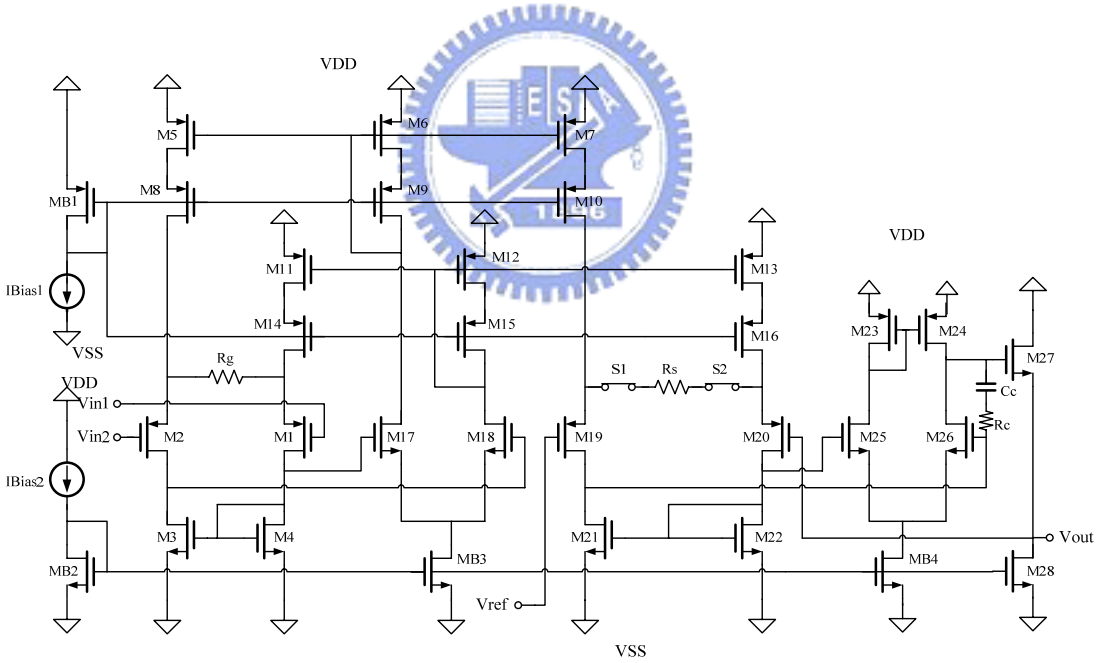

Fig. 3-3 The architecture of the CBIA.

In order to reach a high linearity of input pair, M1 and M2, and output pair, M19 and M20, in the CBIA design, the feedback between input and output must have enough voltage gain. The voltage gain of the CBIA approximates the ratio of two

resistors in (3-1).

$$A_V = \frac{R_g}{R_s} \tag{3-1}$$

The supply voltage of CBIA is +/-0.75V. Under the extremely small supply voltage condition, the thermal noise and flicker noise greatly affects upon performance of the circuit. The noise becomes more important relatively. A simple noise analysis of the input referred thermal noise and input referred flicker noise of the CBIA is shown in (3-2) and (3-3) [37], respectively.

$$\overline{V_{n,themal}^2} \approx 4kT\Delta f\left[\frac{1}{3}\left(\frac{2}{gm_1}+R_g\right)^2\cdot\left(gm_6+gm_{b3}\right)+\frac{4}{3gm_1}+\frac{2gm_3+gm_{23}}{3}\cdot R_g^2+R_g+\frac{R_g^2}{R_s}\right] \tag{3-2}$$

$$\overline{V_{n,flicker}^2} \approx \frac{1}{2}\left(\frac{2}{gm_1}+R_g\right)^2\cdot\left(gm_6^2\cdot\overline{V_{nfb3}^2}\right)+2\cdot\overline{V_{nf1}^2}+\left(gm_3^2\cdot\overline{V_{rf3}^2}+gm_{23}^2\cdot\overline{V_{rf23}^2}\right)\cdot R_g^2 \tag{3-3}$$

where $\overline{V_{n,fi}^2}$ denotes the flicker noise of transistor M_i and is given by $\overline{v_{nfi}^2} = \frac{K_i}{(W\cdot L)_i f}\cdot\Delta f$

According to (3-2) and (3-3), in order to reduce the noise, gm_1 should be high and the *gm* of other transistors should be low. This can be achieved by choosing appropriate ratios for these transistors to reduce the input referred noise. Small R_g should be used for low input referred noise. However, the input range is directly proportional to R_g for a fixed bias current. Large R_g should be used for low effect of the electrode offset voltage [38]. Thus, there is a trade-off among noise, input range and power consumption. PMOS transistor exhibits lower flicker noise than NMOS transistor, and thus CBIA should be used PMOS input pair to reach low noise performance.

The pre-layout simulation of the CBIA is shown as Fig. 3-4. The differential gain of the CBIA is 43dB and phase margin (PM) is about 90 degrees. Common mode rejection ratio (CMRR) is 139dB@150Hz as Fig. 3-5 (EEG signals distribute from

DC to 150Hz) and the lower frequency is, the higher CMRR is. The corner simulation of CMRR is shown in Table 2. Furthermore, the CBIA also increases power supply rejection ratio (PSRR). The PSRR+ is about 100dB@150Hz and the simulation is shown as Fig. 3-6. The corner simulation of PSRR+ is shown in Table 3. The PSRR- is about 114dB@150Hz and the simulation is shown as Fig. 3-7. The corner simulation of PSRR- is shown in Table 4.

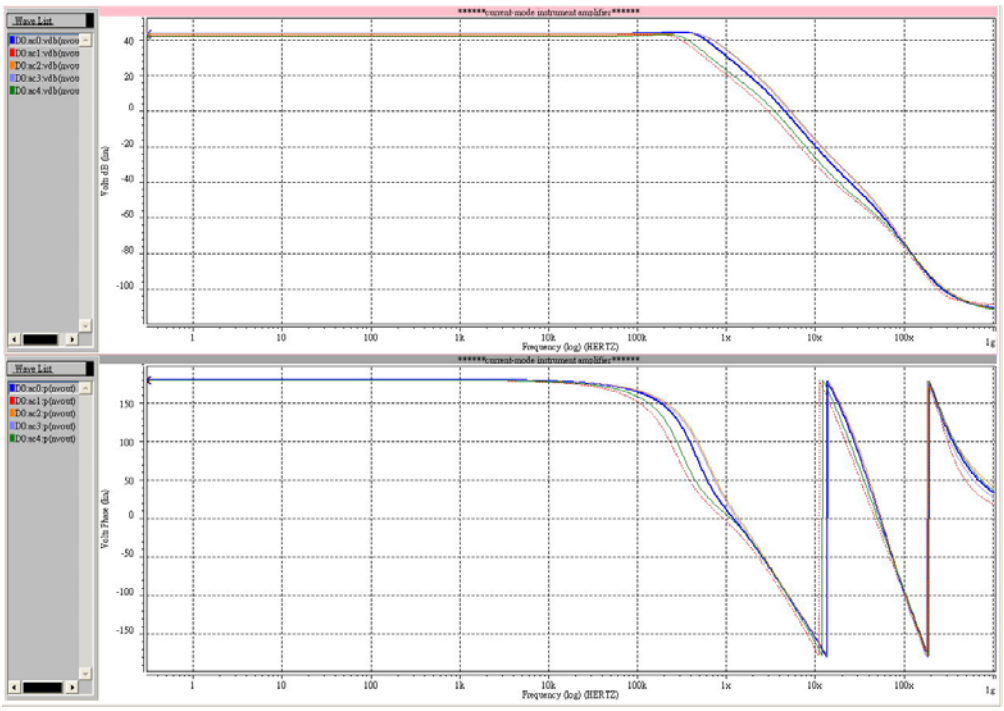

Fig. 3-4 The pre-layout frequency response simulation of the CBIA.

Gain=43dB PM=90degrees

(Pre- layout simulation with 5 corners：TT、SS、FF、FS、SF)

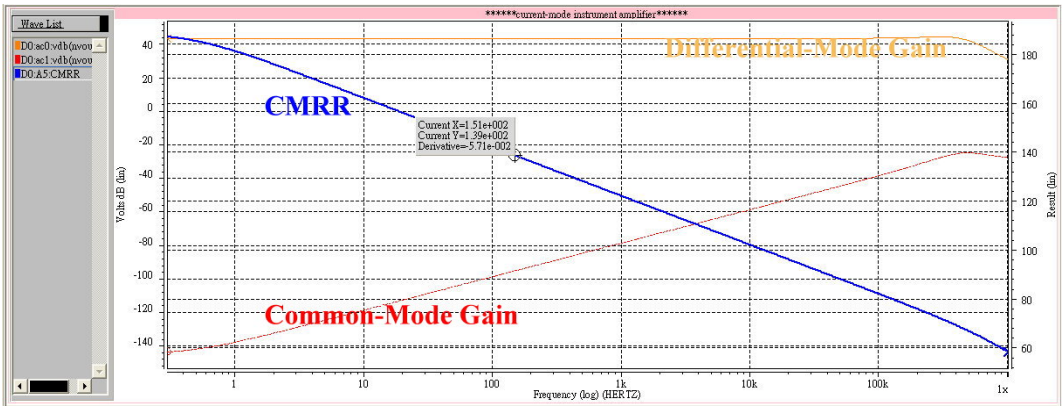

Fig. 3-5 CMRR of the CBIA (139dB@150Hz, 148dB@50Hz).

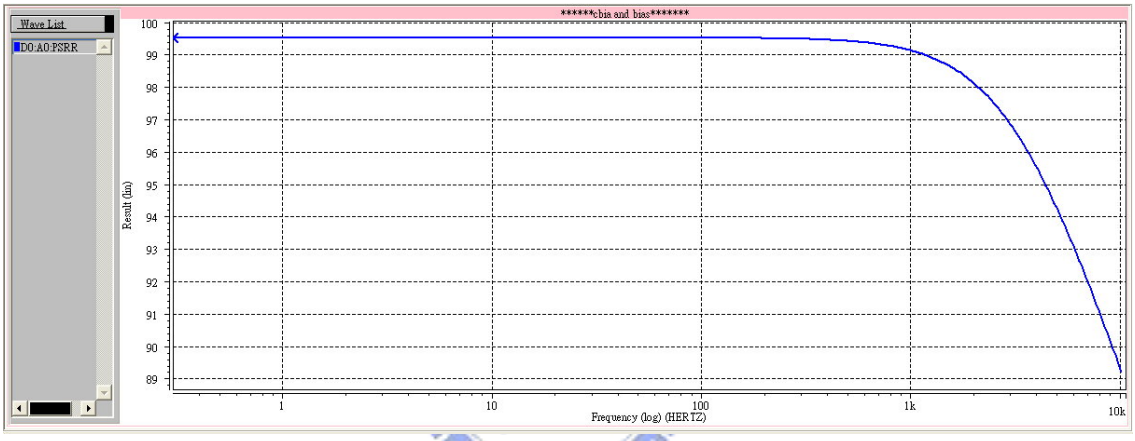

Fig. 3-6 PSRR+ of the CBIA (99.5dB @ DC~150Hz).

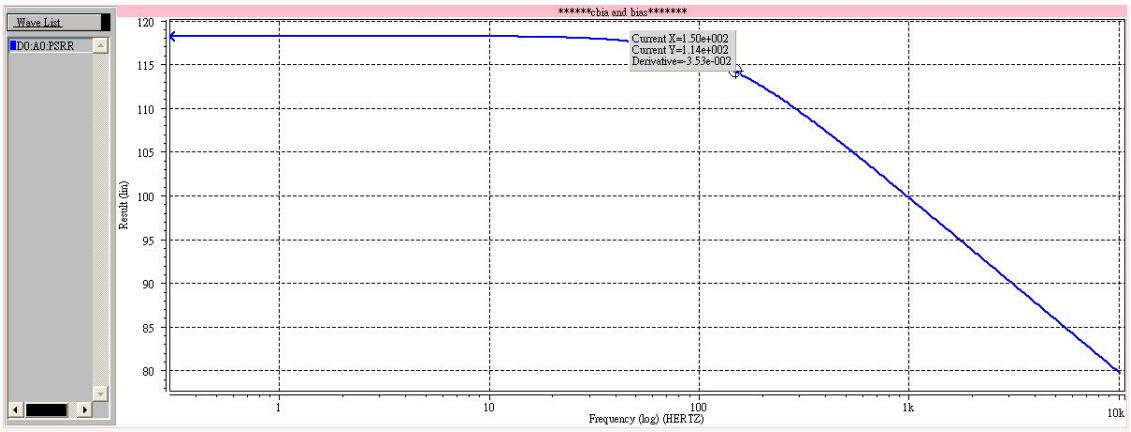

Fig. 3-7 PSRR- of the CBIA (114dB@150Hz, 118dB@50Hz).

Table 2 The corner simulation of CMRR.

CMRR	@50Hz	@150Hz
tt	148 dB	139 dB
ss	133 dB	124 dB
ff	158 dB	148 dB
fs	149 dB	139 dB
sf	146 dB	138 dB

Table 3 The corner simulation of PSRR+.

PSRR+	@50Hz	@150Hz
tt	99.5 dB	99.5 dB
ss	75.7 dB	75.7 dB
ff	114 dB	114 dB
fs	115 dB	115 dB
sf	75 dB	75 dB

Table 4 The corner simulation of PSRR-.

PSRR-	@50Hz	@150Hz
tt	118 dB	114 dB
ss	100 dB	100 dB
ff	125 dB	115 dB
fs	125 dB	116 dB
sf	100 dB	101 dB

The supply voltage is +/- 0.75V and the static current is about 8.95uA in the

CBIA design. Under the low current operation, we supposed the over-drive voltage of a transistor is from 0.05V to 0.1V and adjusted the W/L ratio. And simulated the CBIA operation in the 5 corners of manufacture variation (TT、SS、FF、FS、SF) as Fig.3-4. This result shows the error, which is produced by manufacture variation, has few effect on the CBIA architecture.

3.2.2 Analog Multiplexer

The analog multiplexer [39] is used to select which channel we want to analyze in the AFEIC. The four-to-one analog multiplexer is composed of a two-to-four decoder and four switches in Fig. 3-8. A and B nodes are the input ends of the decoder and then can select a switch (MCH). For example, if AB=00, MCH1 is on, it can transmit signals from CBIA1 to OUT. In addition, utilize the two-to-four decoder (SCH1, SCH2, SCH3, SCH4) to select which R_s of CBIA is on. That is to say, the resistor R_s determines which channel of the CBIA is on at the same time.

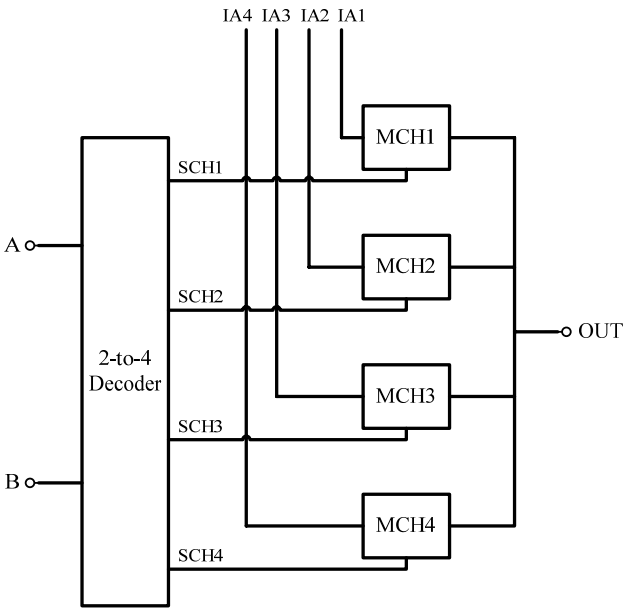

Fig. 3-8 A four-to-one analog multiplexer.

3.2.3 Switched-Capacitor Low-Pass Filter (SCLPF)

Typical passive filter and active filter are very bulky and not suitable for IC fabrication. The biomedical signals distribute over very low bandwidth such as EEG signals distributed from DC to 150Hz. We regarded the EEG bandwidth as the filter bandwidth, must filter the high frequency noise above 150Hz. If adopt the general active filter to set up 150Hz in 3dB frequency, certainly the filter will use the large resistor and capacitor to produce low poles. It is hard to realize the large resistor and capacitor in the CMOS fabrication because they occupy bulky area and they are also low accuracy and sensitive to temperature. Therefore, AFEIC used the switched-capacitor low-pass filter to realize a low-pass filter. It used some switches and capacitors to approximate a large resistor. They replace bulky resistors in traditional filter, so SCLPF can be integrated the system into a chip. First, set up switch frequency that is sampling frequency. Second, set up the sampling capacitor value. The frequency of EEG signals ranges from DC to 150Hz, so the lowest sampling frequency is 300Hz. However, other biomedical signals opposite to EEG should blend into the input-end and they can regard as noise. Most biomedical signals are within 1kHz so the sampling frequency is set up in 5kHz properly.

The switched-capacitor filter mentioned in documents can be divided into the following several structures: switched-capacitor ladder filter, switched-capacitor differentiator biquad filter, and switched-capacitor integrator biquad filter. AFEIC used the switched-capacitor integrator biquad second order filter. This structure can be divided into two kinds of high-Q and low-Q filter, and that is suitable for application of high frequency and low frequency separately. Due to the biomedical signals are all low frequency signals, so we used the low-Q biquad filter and added the

switched-sharing to realize the filter. Switched-sharing can not only reduce the layout area but also save the dynamic power consumption. The architecture of the SCLPF is shown as Fig. 3-9 and the operation amplifier is shown as Fig. 3-10.

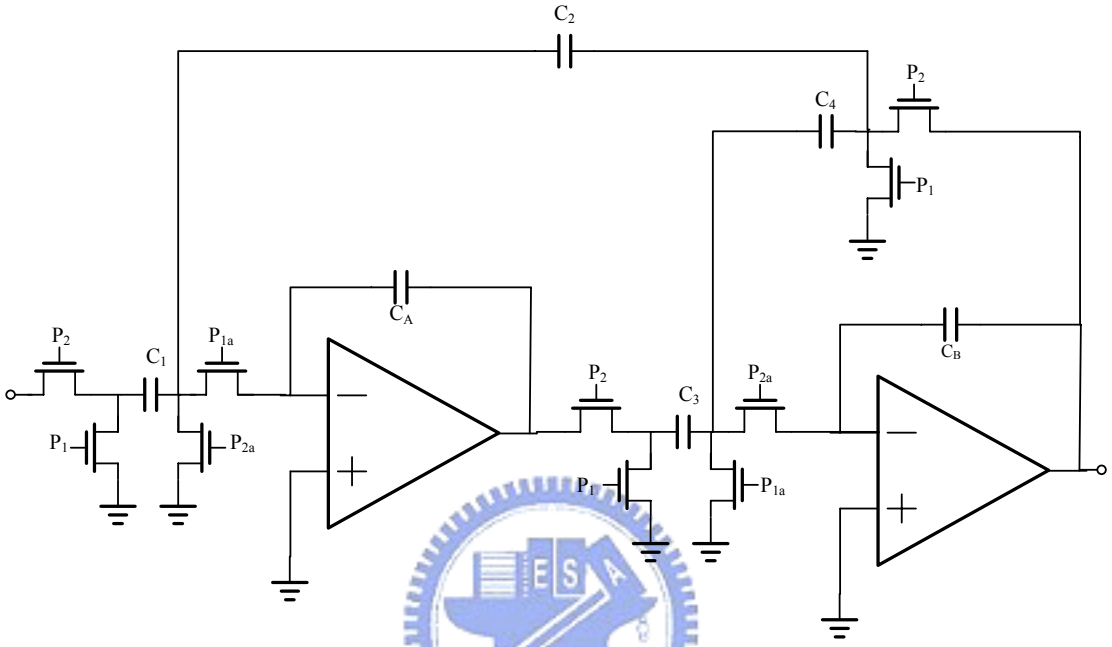

Fig. 3-9 The architecture of the SCLPF.

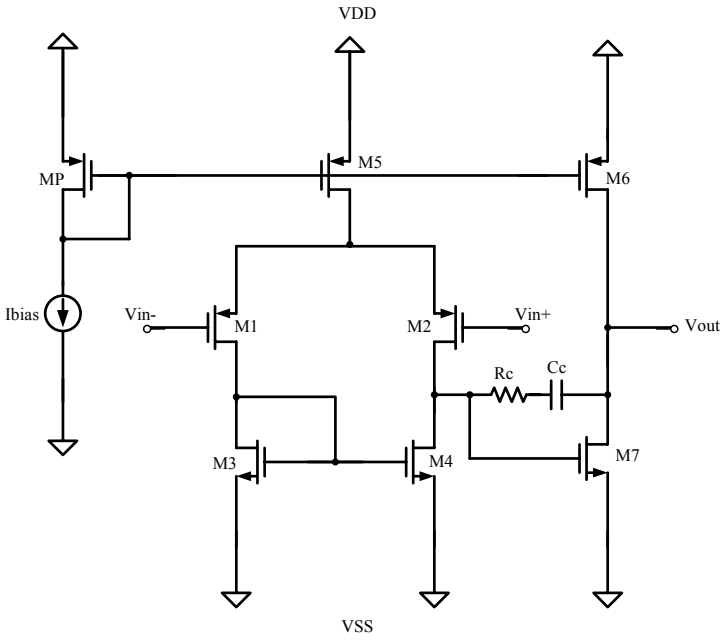

Fig. 3-10 An operation amplifier of the SCLPF.

We adjusted the clock in the SCLPF as Fig. 3-9 opposite to the first generation AFEIC. The reason is when the transistor state changed from on (1) to off (0), charge injection occurs. Charge injection [26][40] occurs by channel charge when MOS switches turn off. From Fig. 3-11, we can see the channel charge flow out from the channel region of the transistor to the drain and source junctions. High frequency switch produces a lot of digital noise by charge injection and affects the performance of the AFEIC.

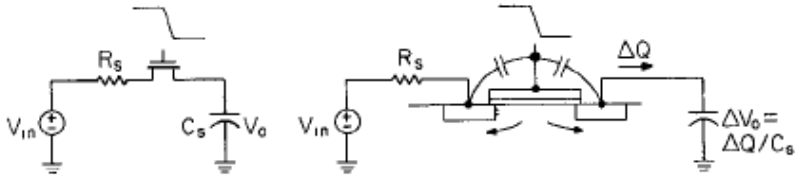

Fig. 3-11 A concept of charge injection [40].

To avoid the above-mentioned, we should select a proper clock frequency in the Fig. 3-9. The first generation AFEIC has only two clock and this generation AFEIC utilizes four clock to switch [41] in this AFEIC design in order to reduce the digital noise of charge injection. Fig. 3-12 analyzes the influence of utilizing switch clock to reduce charge injection. Assume the phase of M1 and M2 are the same (P1=P1a) and the phase of M3 and M4 are the same (P2=P2a), and analyze the charge injection of each transistor.

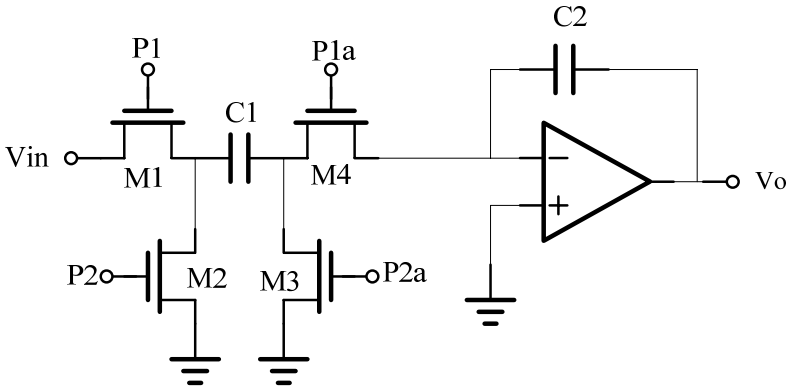

Fig. 3-12 Analysis of charge injection.

(1) M1: When M1 state is from on to off, charge in the channel will flow to the capacitor C1. Different charge will flow to the capacitor C1 by different Vin. This is a distorted source.

(2) M2: When M2 state is from on to off, charge in the channel will flow to the GND and Vin. Assume Vin is an ideal voltage source and the impendence of M1 is very small, so it has no influence to the circuit.

(3) M3: When M3 state is from on to off, charge in the channel will flow to the capacitor C1 and GND. It will affect the sampling voltage of C1, but it is a DC offset voltage that can be predicted. Therefore, it has few influences to the circuit.

(4) M4: When M4 state is from on to off, charge in the channel will flow to the capacitors C1 and C2. However, two ends are both DC offset voltage, so it has few effects to the circuit.

We adjusted the clock by the analysis drawbacks of the above. Let P1a turn off little earlier than P1, and P2a turn off little earlier than P2. Thus, right-end of the capacitor C1 becomes floating, and the charge in the channel of M1 and M3 can not move forward to C1. Consequently, it can not become a loop, so can reduce the effect

of charge injection.

From the analysis of the above, mutual matching of four clocks can effectively reduce the influences of charge injection. Therefore, the non-overlapping clock generator in a SCLPF is shown as Fig. 3-13. In order to assure the output of the clock generator correctly, we adjusted appropriate transistor size in the output inverter.

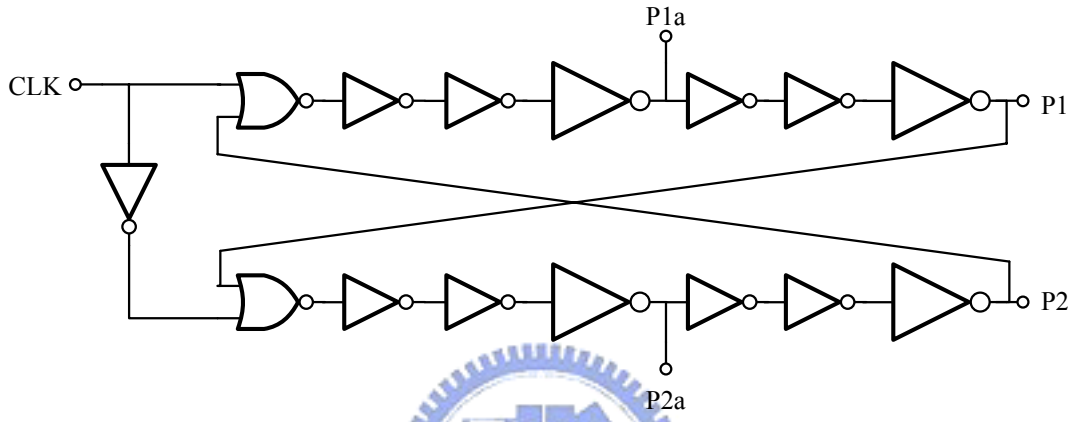

Fig. 3-13 Non-overlapping clock generator.

The pre-layout simulation of the operation amplifier in the SCLPF is shown as Fig. 3-14. The differential gain of the OP is about 80dB and the phase margin is about 75 degrees.

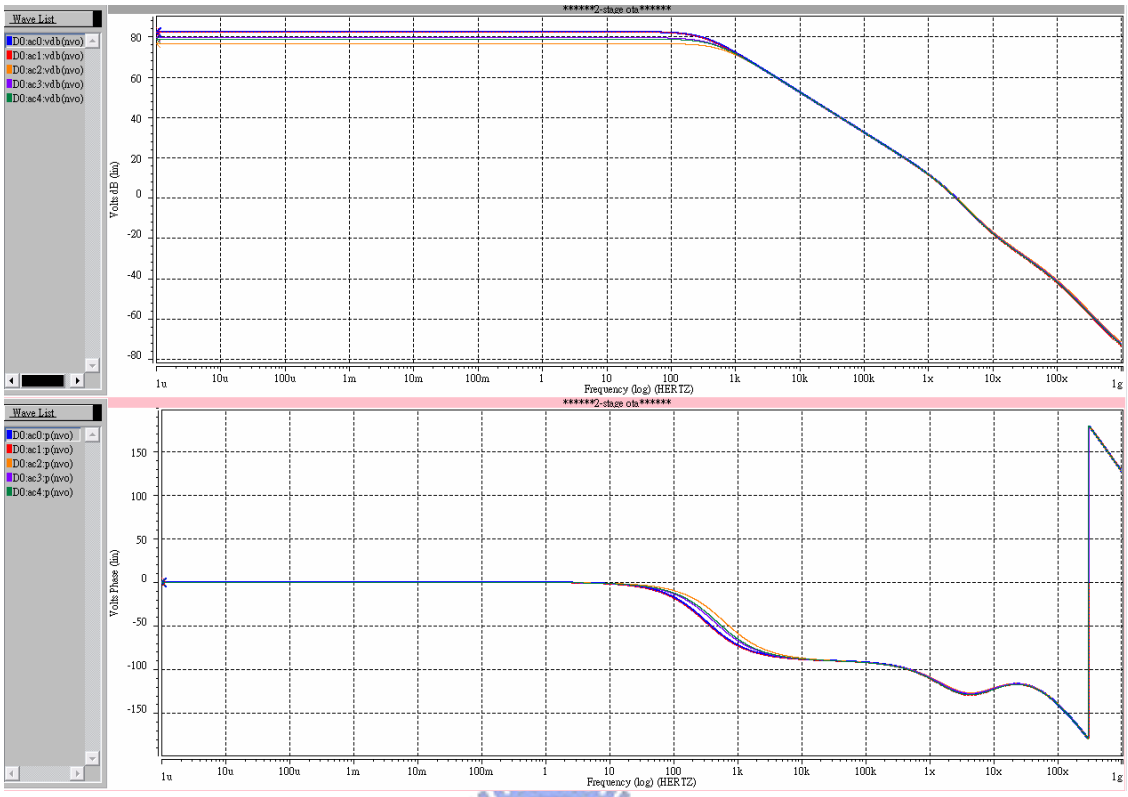

Fig. 3-14 The pre-layout frequency response simulation of the OP in the SCLPF. Gain=80dB PM=75degree

Additionally, the non-overlapping clock generator provided four non-overlapping phases to switch controlling switch, and the clock transient response simulation is shown as Fig. 3-15. The top signal is input clock among the figure, and output signals that are produced by the clock generator are P1, P1a, P2, and P2a in order. The pre-layout simulation of the SCLPF is shown as Fig. 3-16, Fig. 3-17, and Fig. 3-18. The amplitude of input testing signal is 15mV (Take the largest EEG amplitude 100uV as an example, EEG signals via the CBIA and its output amplitude is about 14.125mV, so decide the testing signal is 15mV.) to test SCLPF with different frequency. The different frequency distributes over 10Hz (pass band), 150Hz (3dB band), and 1kHz (stop band) separately. The SCLPF really has the function of low pass filter from the input/output signals transient response simulation.

Fig. 3-15 The pre-layout transient response simulation of the clock generator.

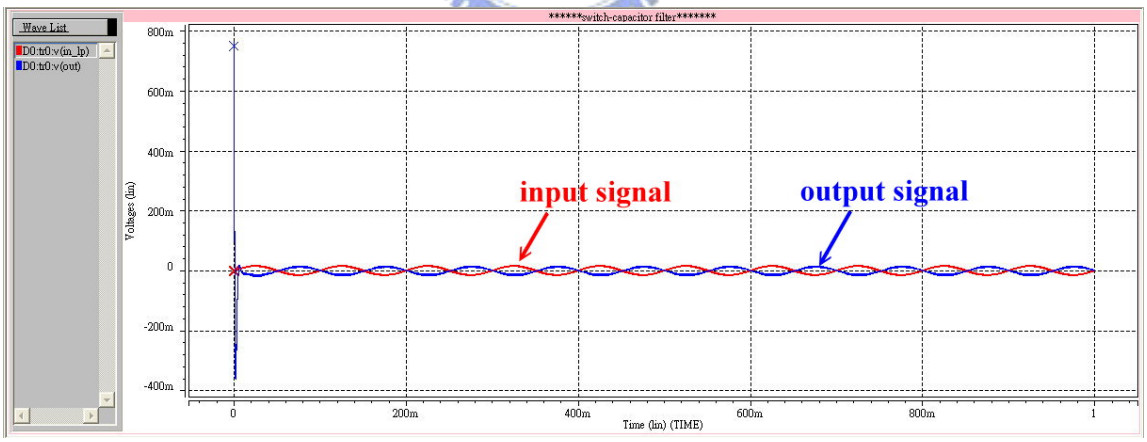

Fig. 3-16 The pre-layout transient response simulation of SCLPF (pass band).

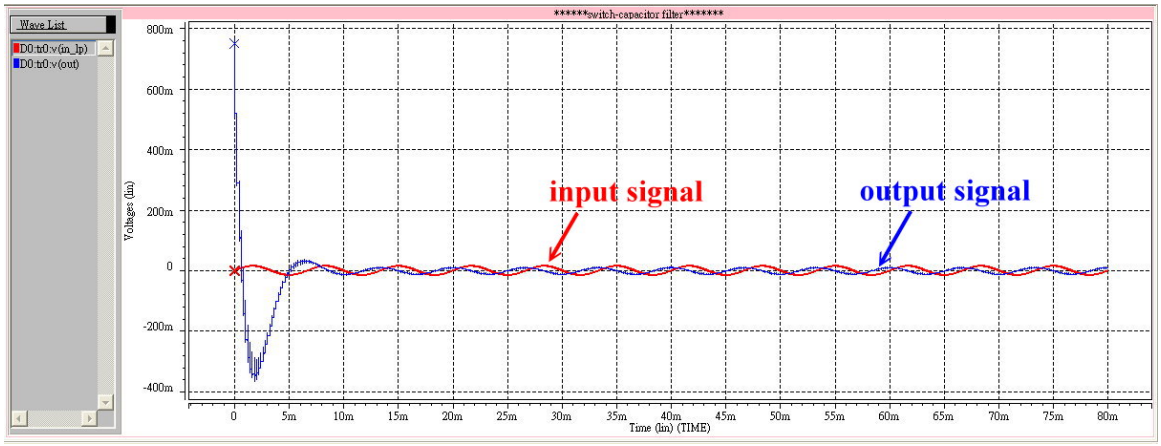

Fig. 3-17 The pre-layout transient response simulation of SCLPF (3dB band).

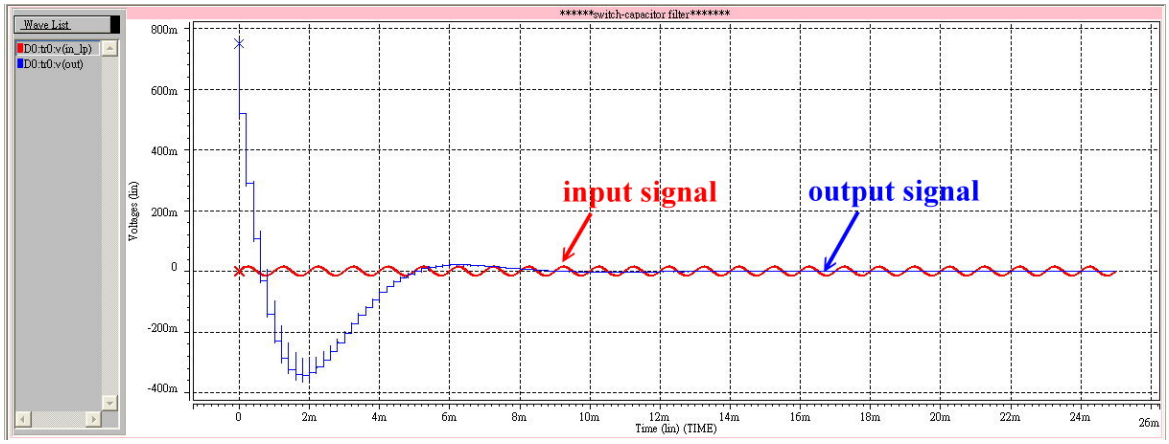

Fig. 3-18 The pre-layout transient response simulation of SCLPF (stop band).

3.2.4 Programmable Gain Amplifier (PGA)

The architecture of the programmable gain amplifier is shown as Fig. 3-19. PGA is the second gain stage besides the CBIA. With the measured environment and signal amplitude at that time, PGA amplifies the biomedical signals to the range easy to analyze. According to the different amplitudes of the biomedical signals, we utilized tunable digital interface to choose proper voltage gain. The two-to-four decoder is used to control the switches, S0, S1, S2, S3, in the Fig. 3-19, and its structure is

shown as Fig. 3-20. The pre-layout simulation of the two-to-four decoder is shown as Fig. 3-21 and the decoder provides two input bits to choose four switch nodes of the resistor array.

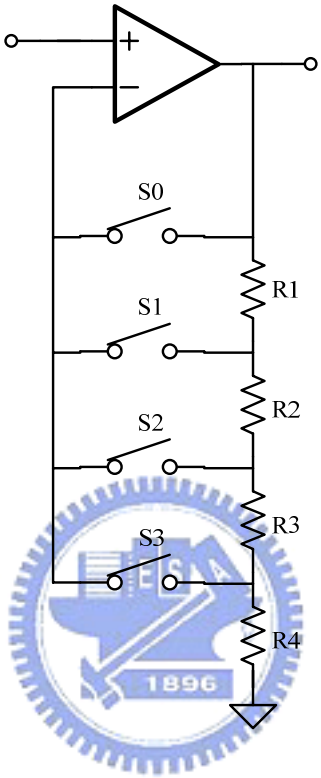

Fig. 3-19 The architecture of the PGA.

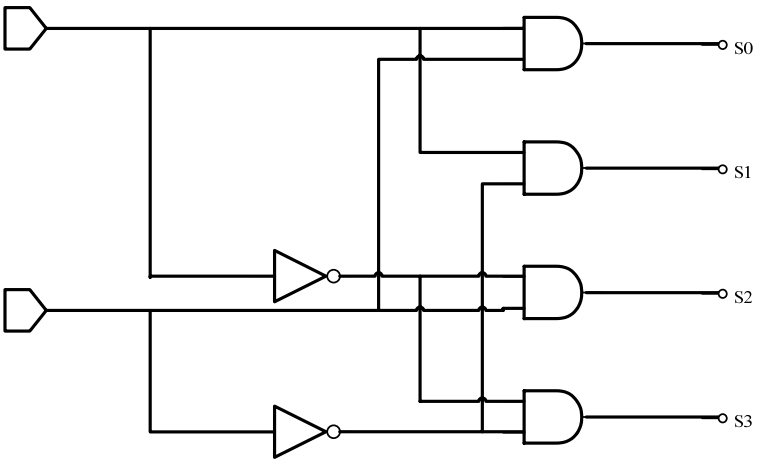

Fig. 3-20 The structure of the two-to-four decoder.

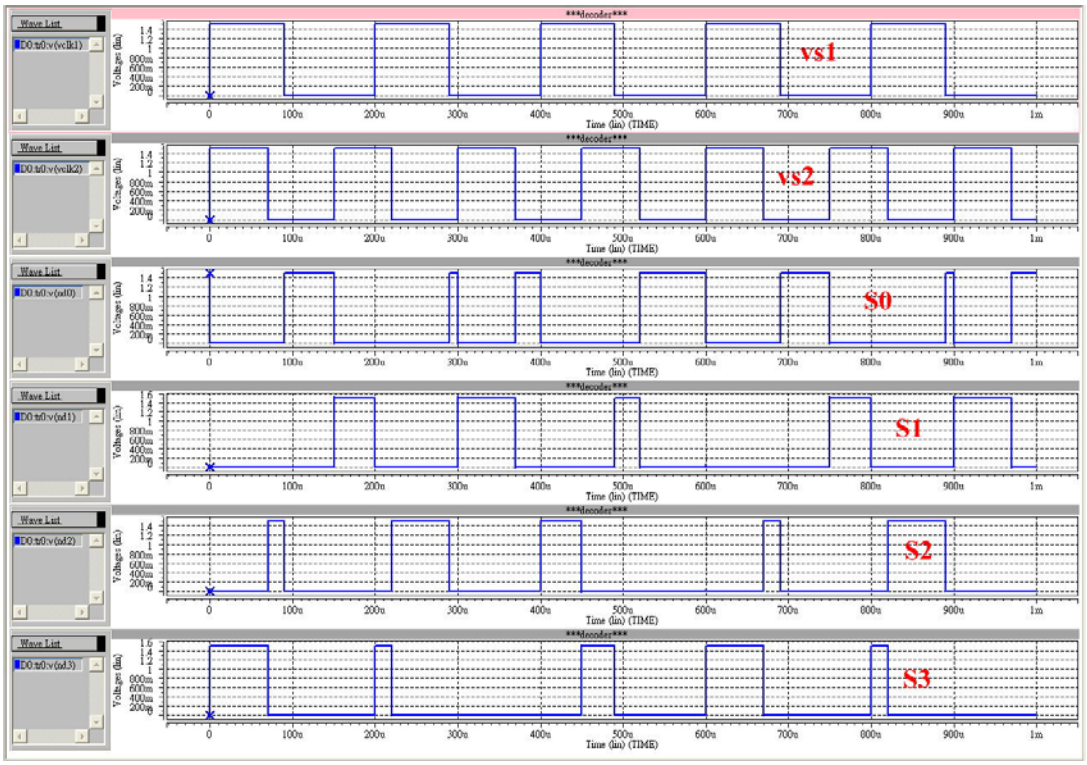

Fig. 3-21 The pre-layout simulation of the two-to-four decoder.

The decoder cooperated with the principle of the amplifier [42] in the PGA, and then it produced four kinds of gain, 0dB, 9.93dB, 17.3dB, and 26.7dB as Fig. 3-22. The architecture of the operational amplifier in the PGA is shown as Fig. 3-10. The pre-layout simulation of the OP in the PGA is shown as Fig. 3-14. The differential gain of the OP is about 80dB and the phase margin is about 75 degrees.

Fig. 3-22 The pre-layout simulation of PGA.

3.2.5 Wide-Swing Constant-Gm Cascode Biasing Circuit

The architecture of the wide-swing constant-Gm cascade biasing circuit is shown as Fig. 3-23. It can be divided into three parts: The first part is a bias loop which is composed of high-swing cascode current mirror [43] to provide a stable current source. On the presupposition of low power consumption, the current mirror used about 1uA to drive the core circuit. The second part is a cascode bias which utilizes the current mirror to copy the current of bias loop and utilizes the cascode structure to bias voltage. The third part is a start-up circuit. Because this structure adopts the wide-swing and constant-Gm, the biasing circuit must add a start-up circuit to maintain the circuit in a correct state at any time. The concepts of the start-up circuit are low consumption and no effects on the biasing circuit. The start-up circuit will revise the voltage in order to maintain the biasing circuit in a normal operational state following the feedback during the biasing circuit only when the biasing circuit is operated abnormally.

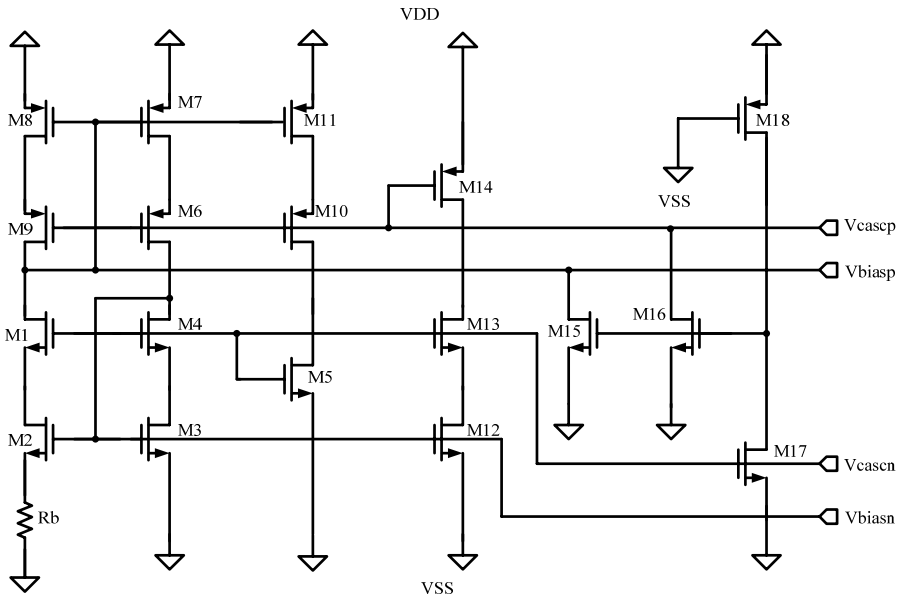

Fig. 3-23 The architecture of the biasing circuit.

3.3 AFEIC Pre-Layout Simulation

After simulations of each circuit separately, we connected every stage circuit as Fig. 3-1 to simulate the whole AFEIC. The input signals are common biomedical signals, which have different magnitude and different frequency. Then, we set the input of the multiplexer to select the channel which we want to observe, and set the input of the decoder in the PGA to choose different voltage gain. AFEIC offered more tunable choices to different characteristics of the biomedical signals. The pre-layout simulation of AFEIC is shown as Fig. 3-24, Fig. 3-25, Fig. 3-26, and Fig. 3-27. The input simulated biomedical signals separately are EEG, ECG, EOG, and EMG among of these figures. In the figures are input signals, the output of CBIA, the output of four-to-one multiplexer, the output of SCLPF, and the output of PGA in order from top to bottom.

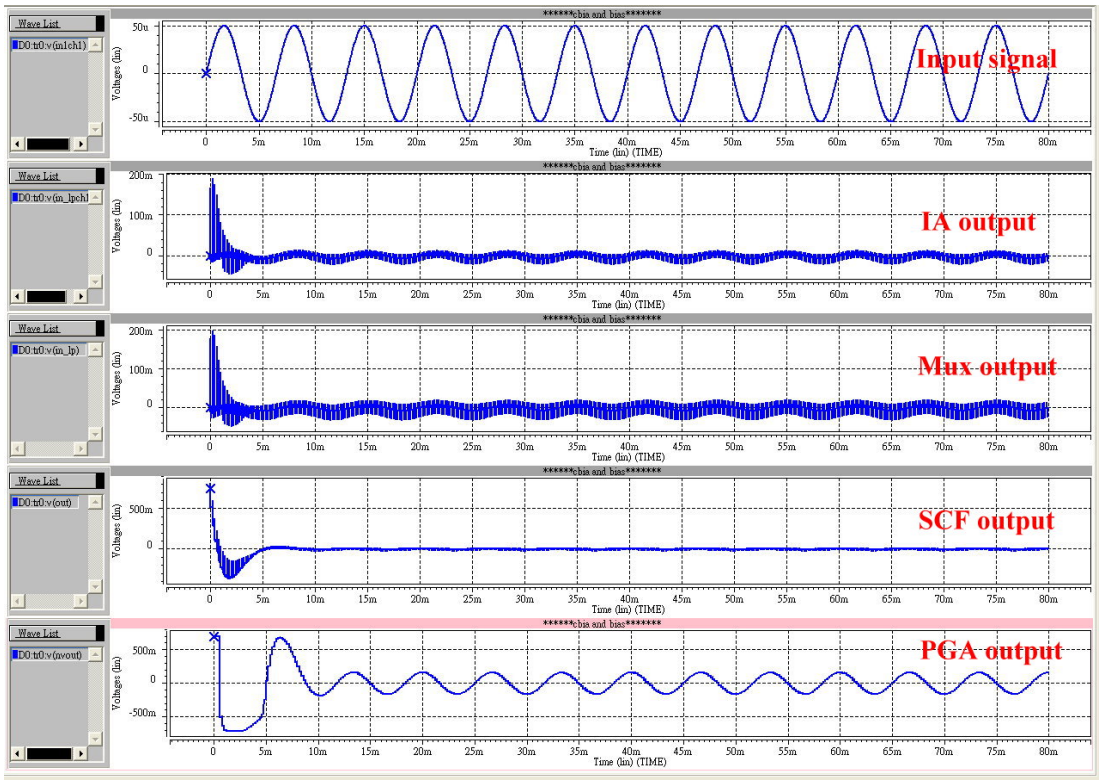

Fig. 3-24 The pre-layout transient response simulation of AFEIC (EEG). [Input signals: amplitude=50uV, frequency=150Hz, channel 1 mux(0 0), sampling frequency of SCLPF=5kHz (equivalent frequency is 150Hz), gain of PGA=26.7dB, decoder (1 1)]

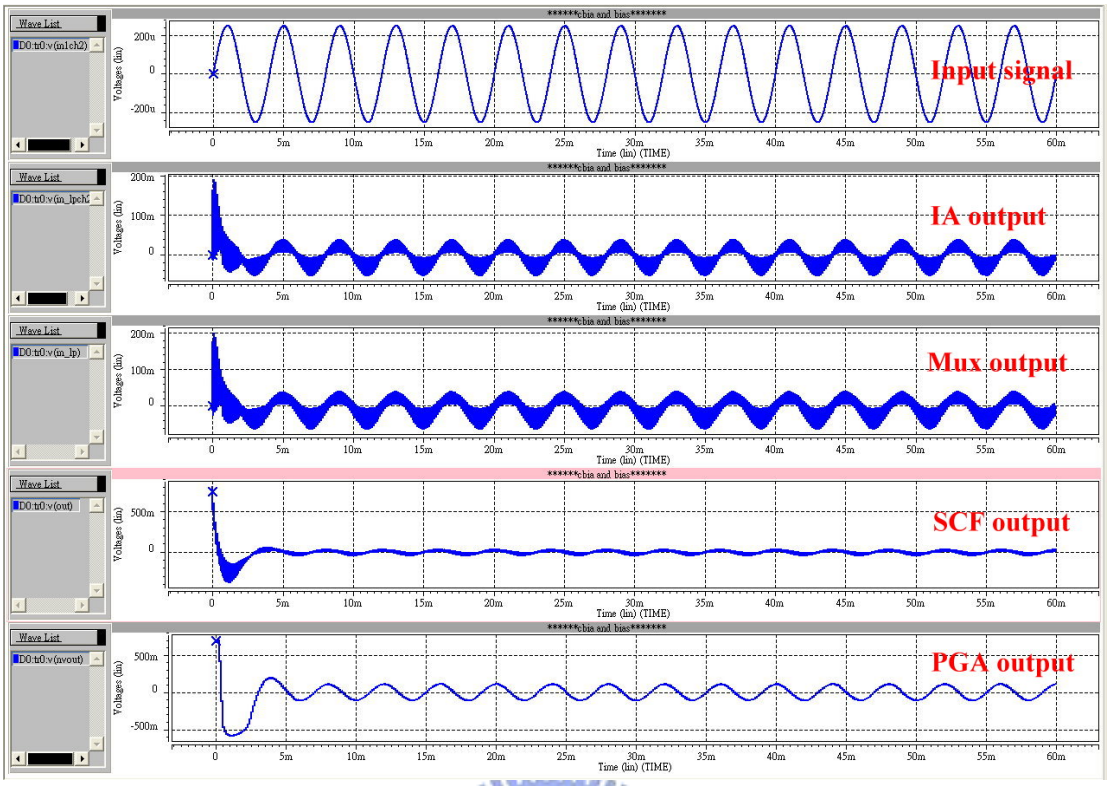

Fig. 3-25 The pre-layout transient response simulation of AFEIC (ECG).

[Input signals: amplitude=250uV, frequency=250Hz, channel 2 mux(0 1), sampling frequency of SCLPF=8.33kHz (equivalent frequency is 250Hz), gain of PGA=9.93dB, decoder (0 1)]

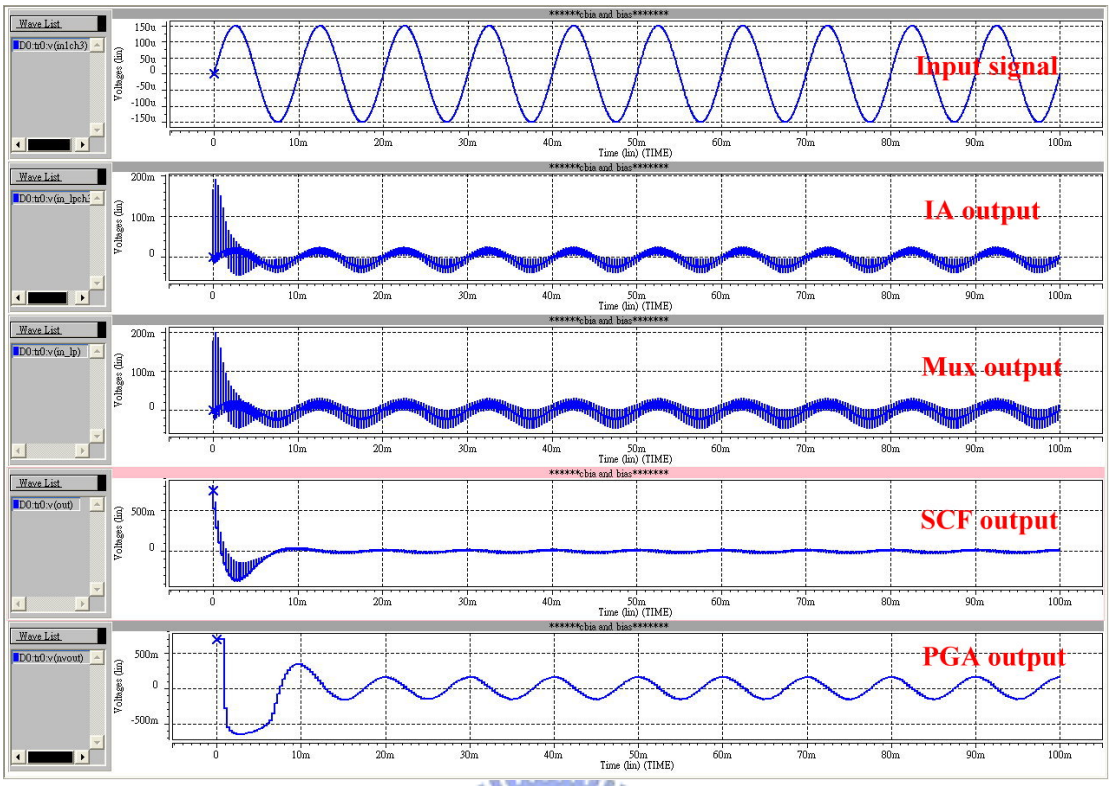

Fig. 3-26 The pre-layout transient response simulation of AFEIC (EOG). [Input signals: amplitude=150uV, frequency=100Hz, channel 3 mux(1 0), sampling frequency of SCLPF=3.33kHz (equivalent frequency is 100Hz), gain of PGA=17. 3dB, decoder (1 0)]

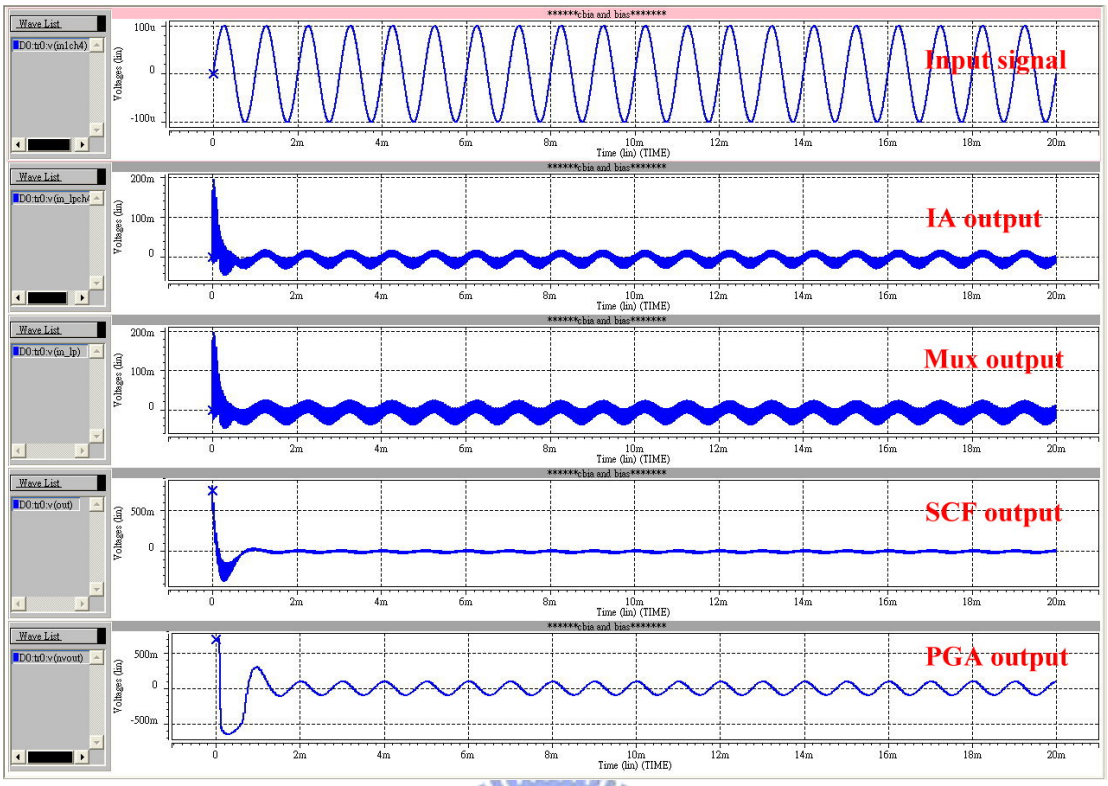

Fig. 3-27 The pre-layout transient response simulation of AFEIC (EMG). [Input signals: amplitude=100uV, frequency=1kHz, channel 4 mux(1 1), sampling frequency of SCLPF=33.3kHz (equivalent frequency is 1kHz), gain of PGA=26.7dB, decoder (1 1)]

According to the results of the AFEIC pre-layout simulation as Fig. 3-24, Fig. 3-25, Fig. 3-26, and Fig. 3-27, they showed the AFEIC really conform to the specification that various kinds of biomedical signals measured. Consequently, we can proceed to simulate post-layout simulation to assure feasibility of CMOS realization in this structure.

Chapter 4
Chip Implementation, Verification and Test Platform

4.1 Design Flow

While design the suitable AFEIC for acquiring biomedical signals, we observed the characteristics of the biomedical signals first, for example, different biomedical signals have different amplitude and frequency. Then we consulted other structures of the circuit proposed by other laboratories and the first generation AFEIC design to think that the drawbacks of design and practical applications. Revise and improve the drawbacks, and design more complete structure. And then we utilized HSPICE to design the circuit with transistor level and simulate the pre-layout simulation. After AFEIC passed the pre-layout simulation, we utilized Laker tools to layout the circuits, verified the layout (Calibre DRC、LVS、PEX), and simulated the post-layout simulation. We checked the specification with conformability to improve the practicability of the AFEIC. After the chip is manufactured, we will test the characteristic and analyze the different between the simulation and the result of testing. The design flow is shown as Fig. 4-1.

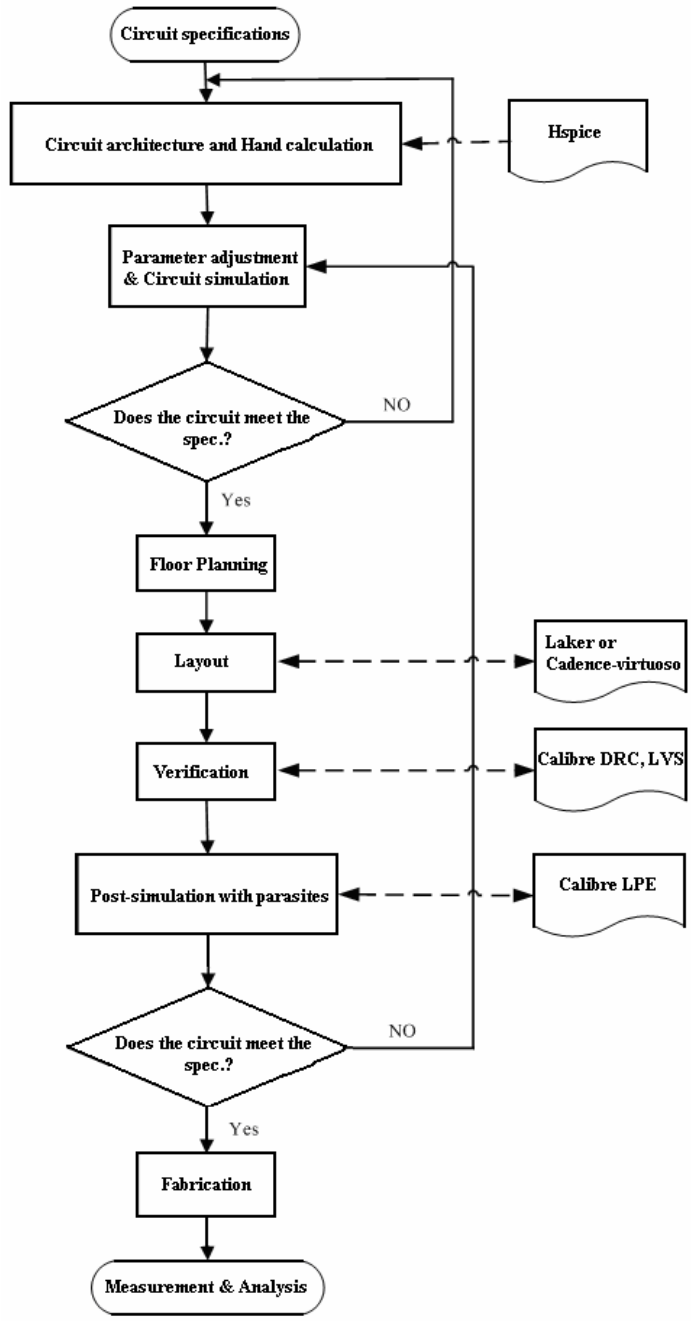

Fig. 4-1 Design flow.

4.2 Layout Consideration and Implementation

Analog circuits have low noise resistance and high processing sensitivity, so we must consider the place when layout the circuit. The fundamental consideration of

analog circuit layout is matching, so it should add dummy cells to protect the elements in order to reduce errors in the processing. In the core circuit parts, we used a guard ring to isolate the passive elements and to avoid the surrounding noise affecting the performance of the core circuit. Therefore, we used a double-layer guard ring in the layout to isolate the core analog circuit, digital controlling circuit, and passive elements (resistors and capacitors array).

The unit capacitor is 100fF and is cut the angle of 45 degrees neatly in this design. It is composed of two metal boards (M5, M6) as Fig. 4-2. We utilized the unit capacitor to arrange into a necessary capacitor array, and added dummy cells, and surrounded a guard ring with six contacts. The unit P+ poly resistor with RPO is 1kΩ as Fig. 4-3. We utilized the unit resistor to arrange into a necessary resistor array, and added dummy cells, and surrounded a guard ring with six contacts.

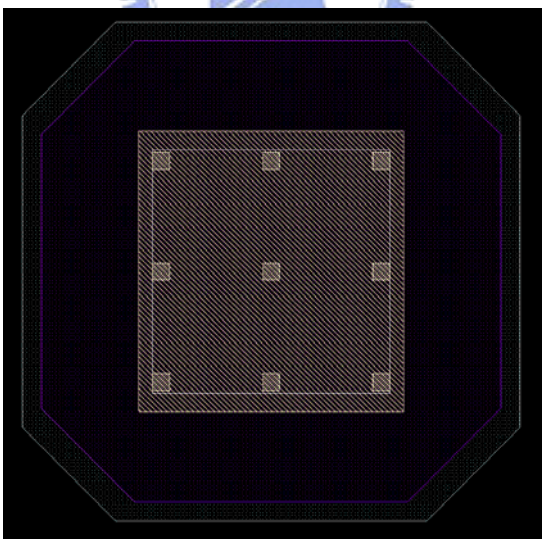

Fig. 4-2 Unit capacitor layout.

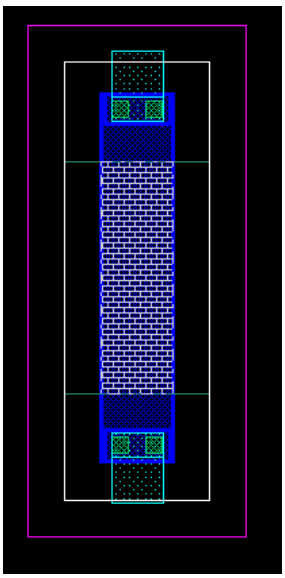

Fig. 4-3 Unit resistor layout.

Fig. 4-4 is the complete AFEIC layout containing electrostatic discharge (ESD) pads. Fig. 4-5 is a diagram of AFEIC layout and area of the core circuit is 0.517×0.364 mm^2. Due to the chip is composed of analog signals and digital signals circuit, layout needs to pay attention to the following notices.

(1) In order to avoid noise by the high frequency signals coupling to the analog circuit, we utilized resistors and capacitors to isolate the analog circuits and digital circuits.

(2) Separate the analog power supply and digital power supply and be distant from each other. The power supplies are used different pads to connect with outside to increase PSRR of the analog circuit.

(3) In the sensitive circuit, add one or more guard ring layers to protect the circuit from noise effects.

(4) If accuracy of resistors or capacitors is expected much, capacitors must use common centroid layout and resistors must use intersection layout.

(5) The differential input pairs, for example the differential input pair of OP, are

possible symmetry in the layout.

(6) Choose the pads with ESD protection to reduce the effects of latch up.

(7) Add dummy cells around the passive elements to avoid the imperfect etching.

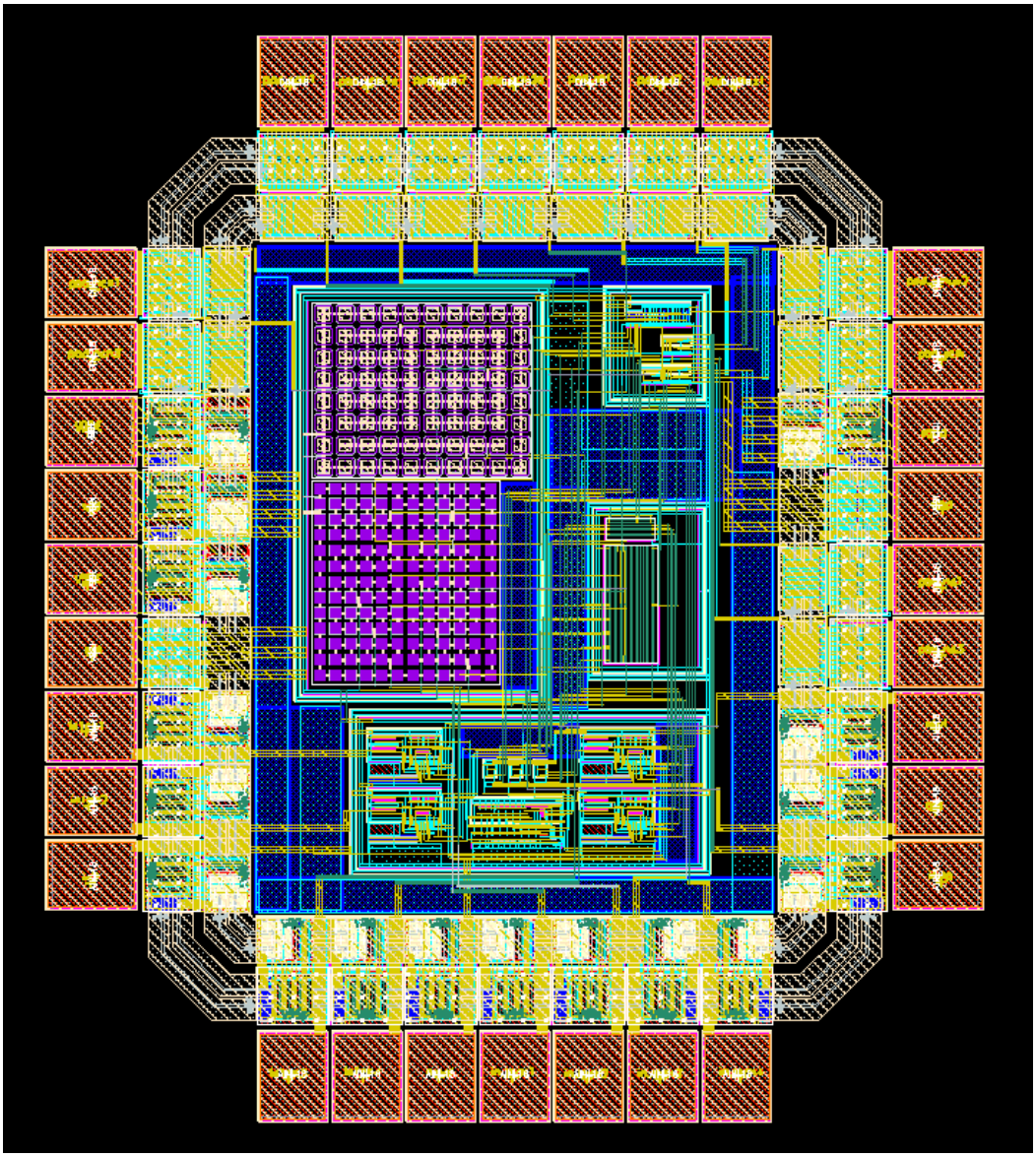

Fig. 4-4 Complete AFEIC layout.

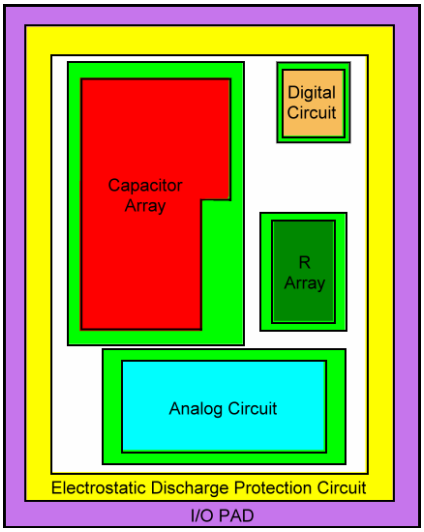

Fig. 4-5 A diagram of AFEIC layout.

The details are enlarged from the AFEIC layout in Fig. 4-4. Fig. 4-6 is the core CBIA layout, Fig. 4-7 is the biasing circuit layout, Fig. 4-8 is the digital controlling circuit layout, and Fig. 4-9 is the core analog circuit layout.

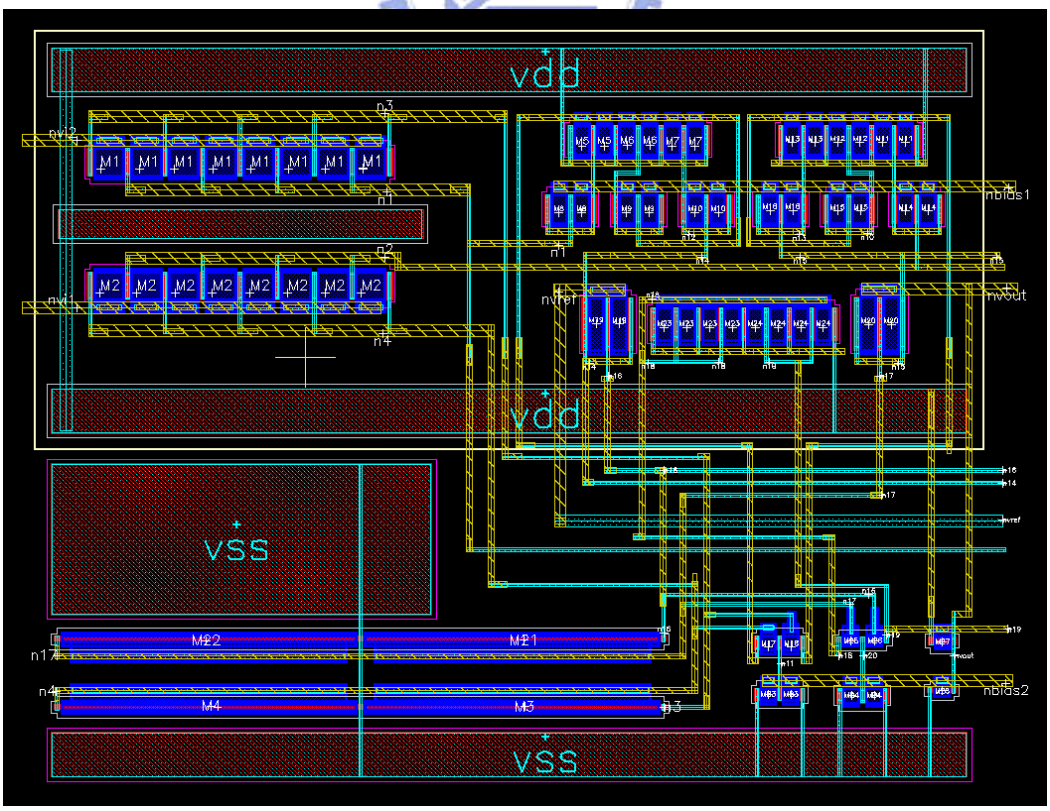

Fig. 4-6 The core CBIA layout.

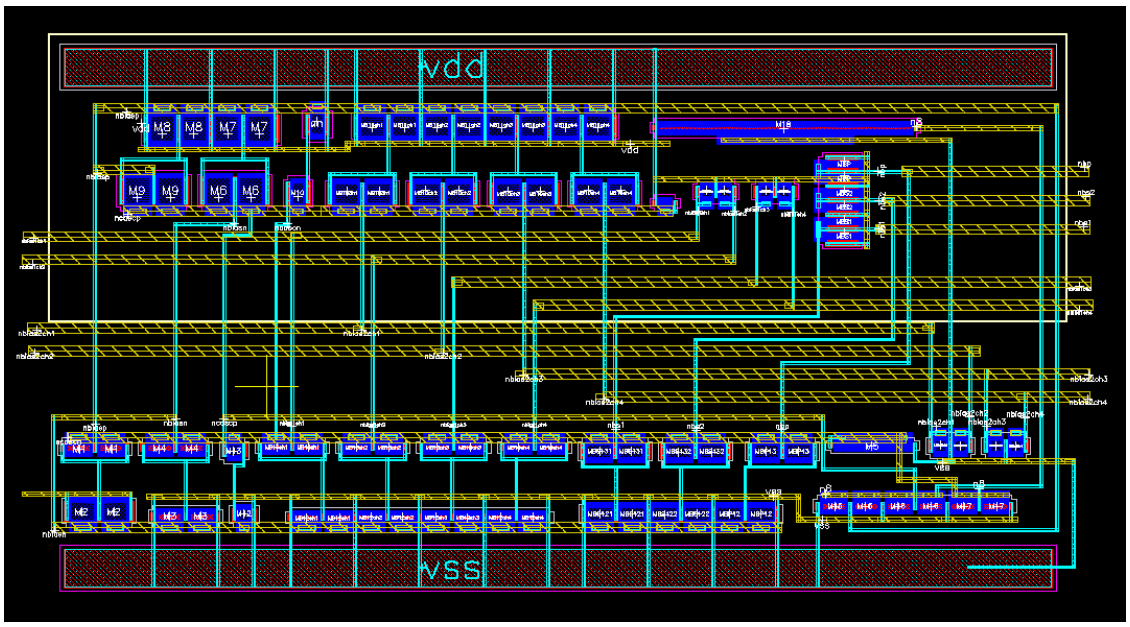

Fig. 4-7 The biasing circuit layout.

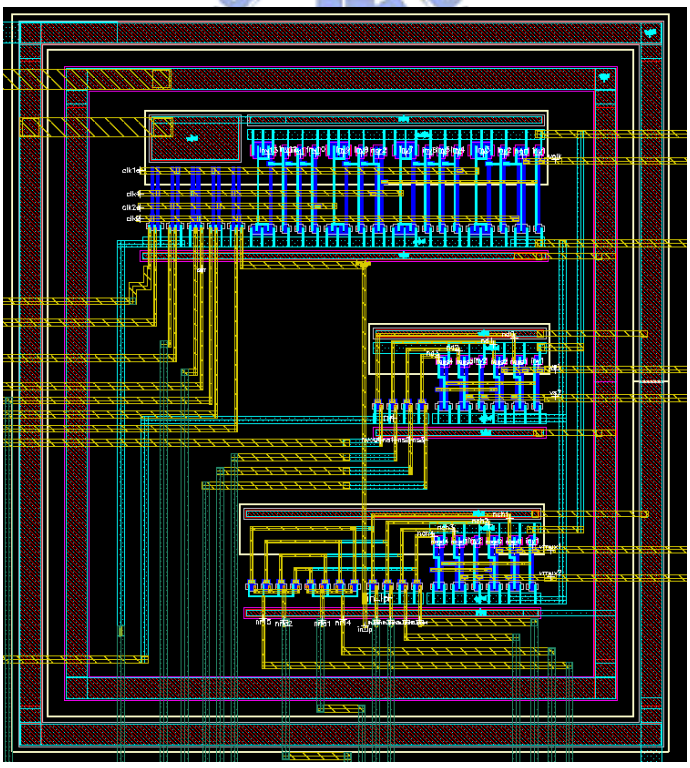

Fig. 4-8 The digital controlling circuit layout.

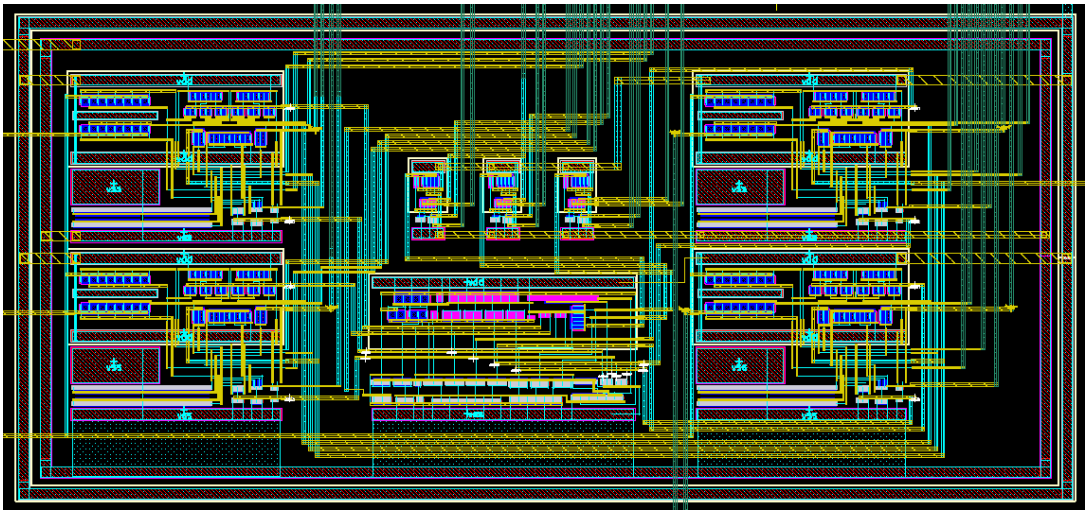

Fig. 4-9 The core analog circuit layout.

4.3 Post-Layout Simulation

In order to assure the performance of the tape-out chip, we must make a post-layout simulation of the AFEIC and absorb equivalent RC effects on this circuit. And then simulate the AFEIC post-layout simulation in the structure of Fig. 3-1 and layout of Fig. 4-2. In order to guarantee practicability and application of the circuit, besides the manufacture variation simulation (5 corners: TT、FF、FS、SF、SS), we acceded to the temperature variation simulation and supply voltage variation simulation. Finally, we compared this post-layout simulation with relevant papers and the first generation circuit and found out the benefits in this AFEIC.

4.3.1 Chip Post-Layout Simulation

To assure the correct AFEIC, which is suitable for any biomedical signals recording systems, we made the post-layout simulation of the whole circuit. The input signals are common biomedical signals, which have different magnitude and different

frequency. Then, we set the input of the multiplexer to select the channel which we want to observe, and set the input of the decoder in the PGA to choose different gain ratio. AFEIC offered more tunable choices to different characteristics of the biomedical signals. The post-layout simulation of AFEIC is shown as Fig. 4-10, Fig. 4-11, Fig. 4-12, and Fig. 4-13. The input simulated biomedical signals separately are EEG, ECG, EOG, and EMG among of these figures. In the figures are input signals, the output of CBIA, the output of four-to-one multiplexer, the output of SCLPF, and the output of PGA in order from top to bottom. The post-layout simulation of AFEIC with ECG characteristic input signal is shown as Fig. 4-14.

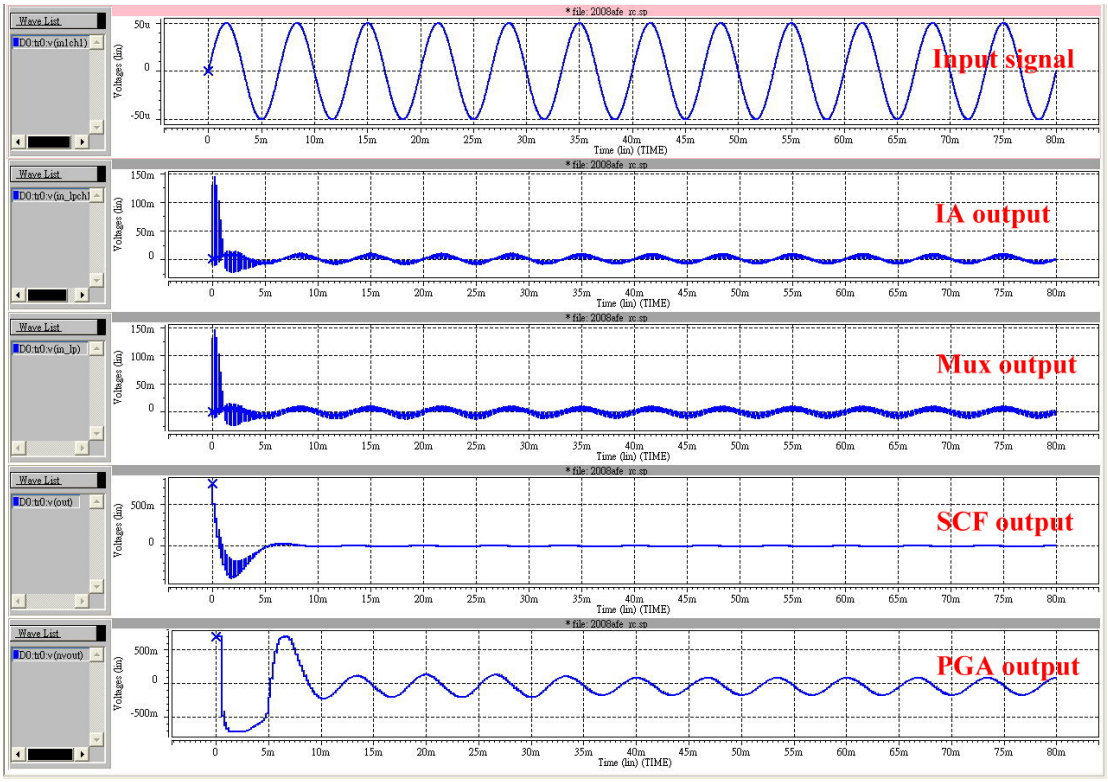

Fig. 4-10 The post-layout transient response simulation of AFEIC (EEG). [Input signals: amplitude=50uV, frequency=150Hz, channel 1 mux(0 0), sampling frequency of SCLPF=5kHz (equivalent frequency is 150Hz), gain of PGA=26.7dB, decoder (1 1)]

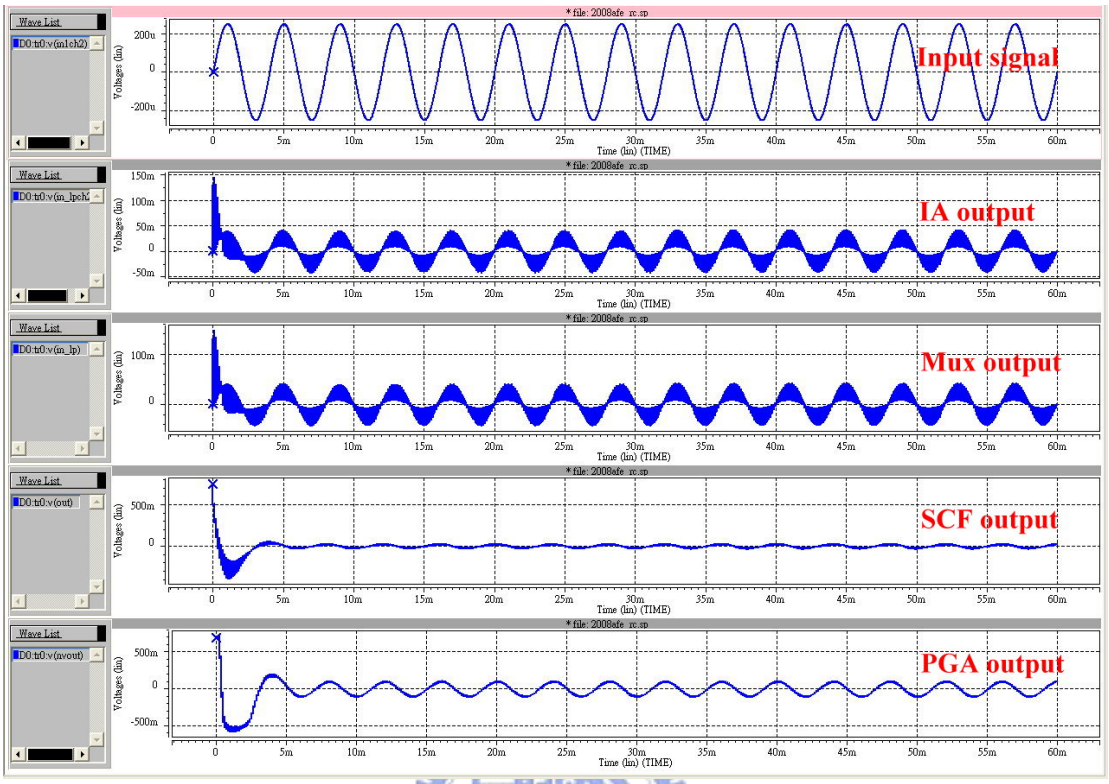

Fig. 4-11 The post -layout transient response simulation of AFEIC (ECG). [Input signals: amplitude=250uV, frequency=250Hz, channel 2 mux(0 1), sampling frequency of SCLPF=8.33kHz (equivalent frequency is 250Hz), gain of PGA=9.93dB, decoder (0 1)]

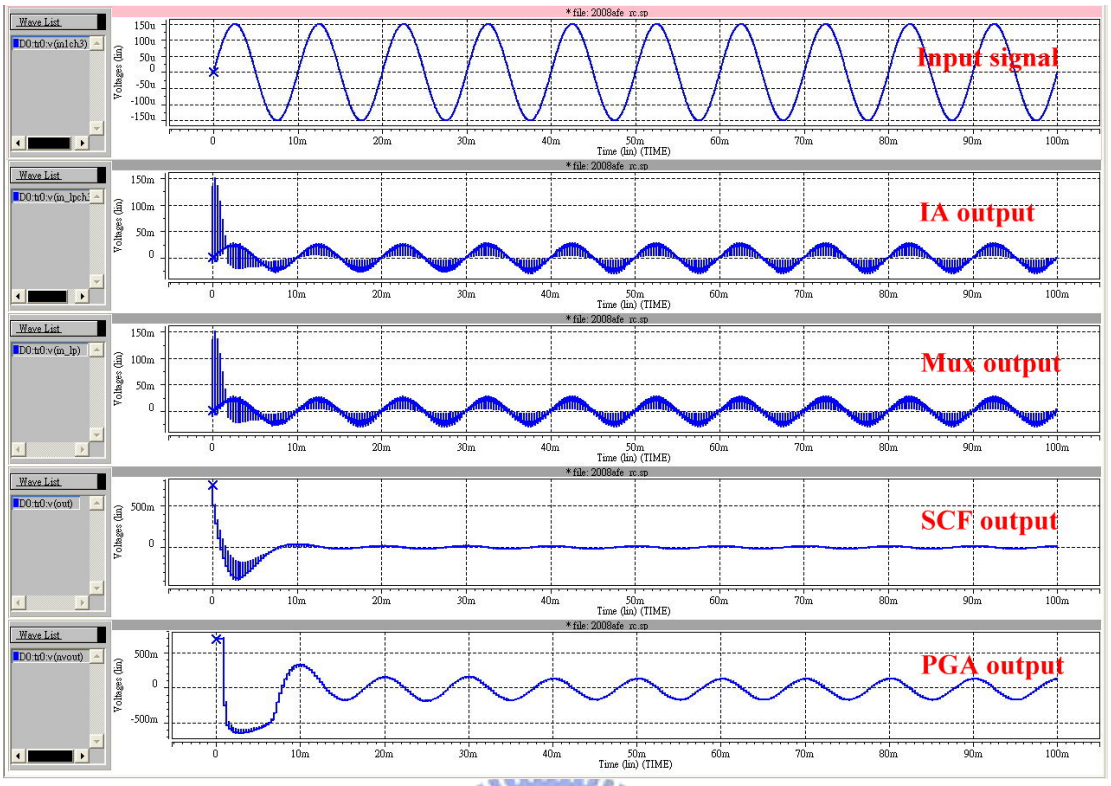

Fig. 4-12 The post -layout transient response simulation of AFEIC (EOG). [Input signals: amplitude=150uV, frequency=100Hz, channel 3 mux(1 0), sampling frequency of SCLPF=3.33kHz (equivalent frequency is 100Hz), gain of PGA=17. 3dB, decoder (1 0)]

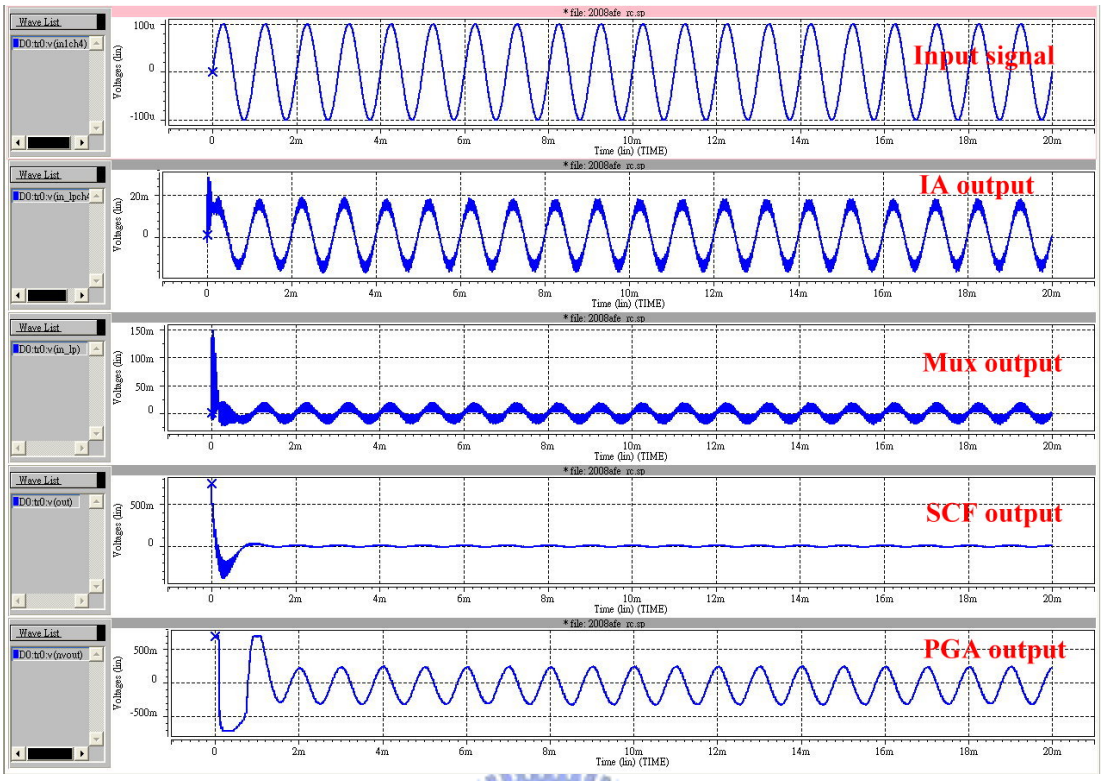

Fig. 4-13 The post -layout transient response simulation of AFEIC (EMG).

[Input signals: amplitude=100uV, frequency=1kHz, channel 4 mux(1 1), sampling frequency of SCLPF=33.3kHz (equivalent frequency is 1kHz), gain of PGA=26.7dB, decoder (1 1)]

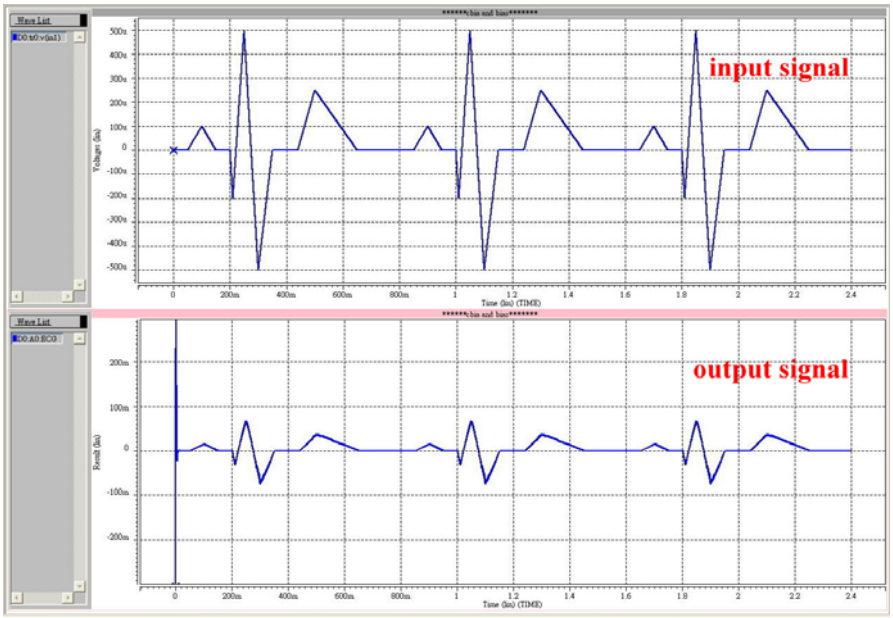

Fig. 4-14 The post -layout transient response simulation of AFEIC (ECG).

[Input signals: signal with ECG characteristic]

4.3.2 Manufacture Variation Post-Layout Simulation

According to the result of the post-layout simulation in the five manufacture variations, the AFEIC design can tolerate the manufacture variation. The simulation is shown as Fig. 4-14. The input signal is simulated EEG signal, which amplitude is 50uV and frequency is 150Hz, and the temperature is at 25℃.

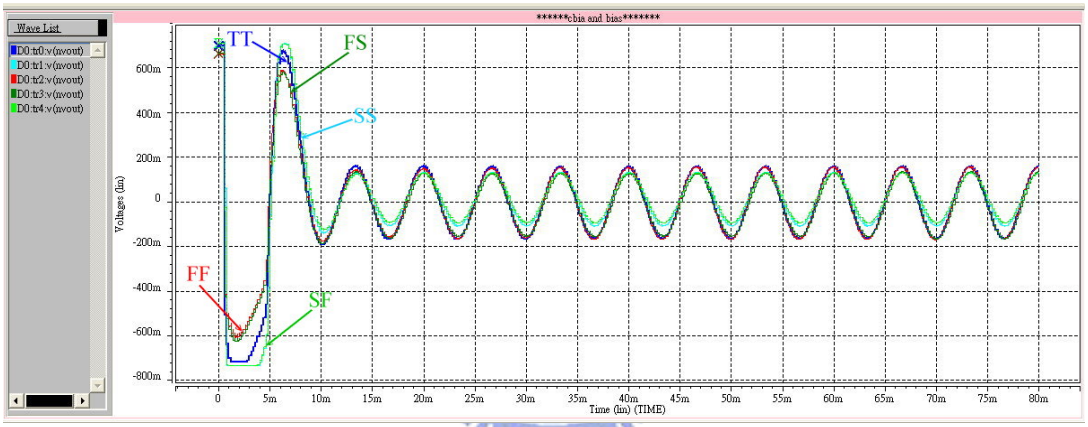

Fig. 4-14 The manufacture variation post -layout simulation of AFEIC (EEG).

[Input signals: amplitude=50uV, frequency=150Hz, channel 1 mux (0 0), sampling frequency of SCLPF=5kHz (equivalent frequency is 150Hz), gain of PGA=26.7dB, decoder (1 1)]

4.3.3 Temperature Variation Post-Layout Simulation

We simulated the effects of temperature variation on the chip, and the temperature range is from -25℃ to 95℃. AFEIC tested temperatures are at the -25℃, 0℃, 25℃, 60℃, 85℃, 90℃, and 95℃ separately. The simulation is shown as Fig. 4-15. From the result of simulation, the temperature variation has few effects on the chip under 95℃.

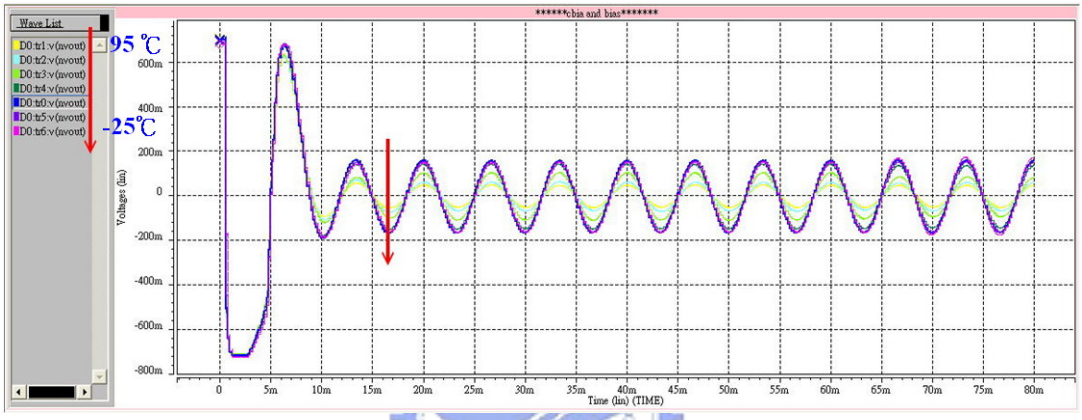

Fig. 4-15 The temperature variation post -layout simulation of AFEIC (EEG).

[Input signals: amplitude=50uV, frequency=150Hz, channel 1 mux (0 0), sampling frequency of SCLPF=5kHz (equivalent frequency is 150Hz), gain of PGA=26.7dB, decoder (1 1)]

4.3.4 Power Supply Variation Post-Simulation

The stable supply voltage on the chip is +/-0.75V. We simulated the supply voltage variation on the chip, and the supply voltage variations are +50%, +40%, +30%, +25%, +20%, +10%, 0%, and -10% separately. The simulation is shown as Fig. 4-16. From the result of simulation, the AFEIC can tolerate the supply voltage variation.

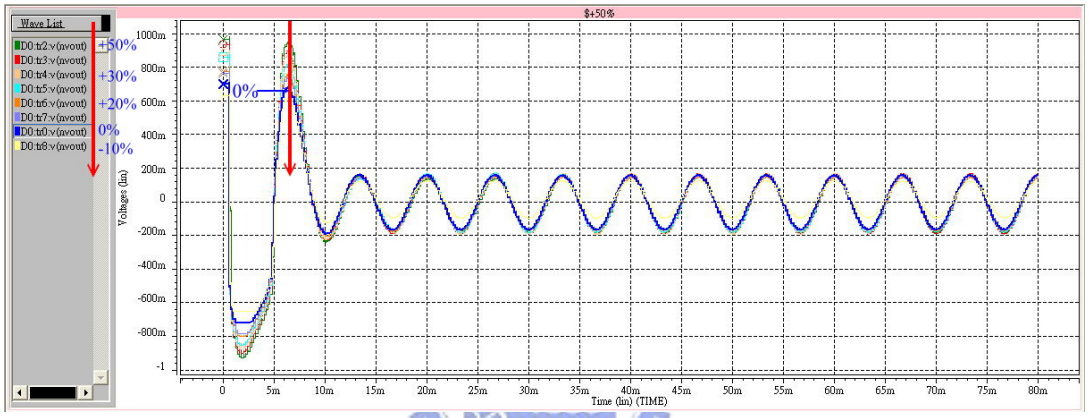

Fig. 4-16 The supply voltage variation post -layout simulation of AFEIC (EEG).

[Input signals: amplitude=50uV, frequency=150Hz, channel 1 mux (0 0), sampling frequency of SCLPF=5kHz (equivalent frequency is 150Hz), gain of PGA=26.7dB, decoder (1 1)]

4.4 Specification Comparison

The specification of AFEIC design in this thesis is shown as Table 5. Table 6 summarizes the comparison results among the proposed AFEIC and the conventional designs. It can be seen that the proposed AFEIC offers reasonable low power, high CMRR, PSRR+ and PSRR- performance. In terms of area size, the proposed

four-channel AFEIC is fully implemented with relative small size. Importantly, by integrating digital interface, the AFEIC has the selectable system gain and bandwidth.

Table 5 The specification of AFEIC.

Process Technology	**TSMC 0.18um 1P6M**	
	Pre-Simulation	**Post-Simulation**
Supply voltage	±0.75V	±0.75V
DC Gain (Max.)	69.7dB	68.9dB
CMRR (DC~150Hz)	> 139dB	> 135dB
PSRR+ (DC~150Hz)	> 99.5dB	> 105dB
PSRR- (DC~150Hz)	> 114dB	> 112dB
Bandwidth	Selectable	Selectable
Input referred noise (DC~150Hz)	1.565uVrms	1.713uVrms
Input Resistance	1.000e+20 Ω	1.000e+20Ω
Temperature range	0 ~ 95 ℃	0 ~ 95 ℃
Phase margin	> 80 degree	> 80 degree
Power consumption	104.5945uW	112.6837uW

Table 6 The comparison AFEIC with relevant papers.

Parameter	Ref [2]	Ref [16]	Ref [6]	The 1st circuit[8]	This Work
Technology	2.4um CMOS	0. 5um CMOS	0.5um CMOS	0.35um CMOS	0.18um CMOS
Supply Voltage (V)	+/- 4.5	3	3	+/- 1.5	+/- 0.75
No. of Channel	16	8	1	1	4
Core Area (mm^2)	24	12	1.95	0.268	0.188
Mid-Band Gain (dB)	Up to 74	66-79	51.82 - 67.96	52.66 - 80.45	43-68.9
Current Consumption per Channel (uA)	520	92.6	20	47.468	18.8
Power Consumption per Channel (uW)	292.5	100	60	150.7682	28.1709
Bandwidth (Hz)	0.3 - 150	Selectable	Selectable	Selectable	Selectable
Input Common Mode Range (V)	-3.8 to 1.5	N/A	1.05 to 1.7	-1.4 to 0.33	-0.45to 0.35
Input Referred Noise (uVrms) (0.3Hz<BW<150Hz)	1.39	0.93	< 0.7	2.417	1.713
CMRR @ 50Hz (dB)	99	130	> 120	145	148
PSRR+ (dB)	40 @10Hz	N/A	80 @50Hz	131 @50Hz	105 @50Hz
PSRR- (dB)	N/A	N/A	78 @50Hz	118 @50Hz	116 @50Hz

Ref [2]："A CMOS IC for portable EEG acquisition systems," *Instrumentation and Measurement, IEEE Transactions on* , vol.47, no.5, pp.1191-1196, Oct 1998

Ref [16]："Low-Power Low-Noise 8-Channel EEG Front-End ASIC for Ambulatory Acquisition Systems," *Solid-State Circuits Conference, 2006. ESSCIRC 2006. Proceedings of the 32nd European* , vol., no., pp.247-250, Sept. 2006

Ref [6]：“A 60 uW 60 nV/ $\sqrt{Hz}$ Readout Front-End for Portable Biopotential Acquisition Systems”, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. 5, MAY 2007.

4.5 Test Platform Design

In testing, consider testing all the specifications of AFEIC in detail, and set many testing nodes. Inputs and outputs of every analog stage circuit are set testing nodes to verify the operation of each core analog circuit. Inputs and outputs of digital circuits are also set testing nodes to prevent from if digital circuits are failure, cause unable to test the core analog circuit. If the digital circuit is failure unfortunately, clocks can be input the circuit to test the analog circuit. Fig. 4-17 is the bonding diagram of AFEIC, which is used SB32 package and has 32 testing pins.

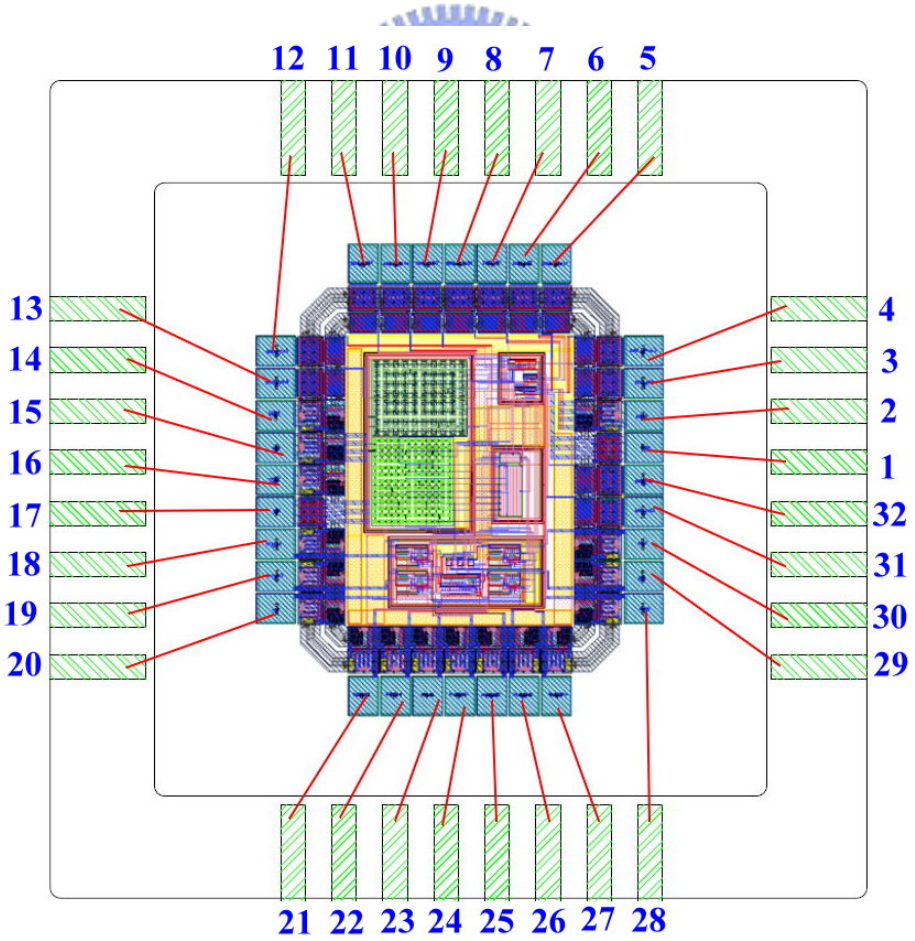

Fig. 4-17 The bonding diagram of AFEIC.

4.5.1 Chip Pins Instructions and Signal Illustration

Table 7 is the illustration of the testing pins and signal explanations in AFEIC.

Table 7 The illustration of the testing pins.

Pin No.	Signal name	I/O direction	Signal explanation
1	GND	I	Core voltage source
2	VDDA	I	Core voltage source
3	vclk	I	Input of non-overlapping clock generator
4	vmux2	I	2nd input of multiplexer
5	vmux1	I	1st input of multiplexer
6	vs2	I	2nd input of 2-to-4decoder
7	vs1	I	1st input of 2-to-4decoder
8	vclk2a	I/O	Output of non-overlapping clock generator, P2a
9	vclk2	I/O	Output of non-overlapping clock generator, P2
10	vclk1a	I/O	Output of non-overlapping clock generator, P1a
11	vclk1	I/O	Output of non-overlapping clock generator, P1
12	nch1	I/O	1st output of decoder in the multiplexer
13	nch3	I/O	2nd output of decoder in the multiplexer
14	VDDE	I	ESD voltage source
15	VDD	I	Core voltage source
16	VSSE	I	ESD voltage source
17	VSS	I	Core voltage source
18	in1ch1	I	Positive input of channel1 CBIA
19	in1ch2	I	Positive input of channel2 CBIA
20	in2	I	Negative input of CBIA
21	in1ch3	I	Positive input of channel3 CBIA
22	in1ch4	I	Positive input of channel4 CBIA
23	nvref	I	Input of CBIA reference voltage
24	in_lpch1	I/O	Output of channel1 CBIA
25	in_lpch2	I/O	Output of channel2 CBIA
26	in_lpch3	I/O	Output of channel3 CBIA
27	in_lpch4	I/O	Output of channel4 CBIA
28	in_lp	I/O	Output of multiplexer
29	out	I/O	Output of SCLPF
30	nvout	O	Output of PGA
31	ns3	I/O	2nd output of 2-to-4decoder
32	ns1	I/O	1st output of 2-to-4decoder

4.5.2 Test Platform Architecture

The architecture of testing the chip is shown as Fig. 4-18. Its purpose confirms that whether the chip can operate correctly or not. Test the performances of amplification, filter, and eliminating noise in the AFEIC. The equipments of testing the chip include function generators, an oscilloscope, power supplies, etc. The testing step is as following.

(1) Adjust the power supply to proper voltage supply, and connect to the analog voltage supply (+/-0.75V), digital voltage supply (0/1.5V), and ESD voltage supply (0/1.5V). In order to avoid 60Hz noise with power supply, we must add a capacitor and a resistor to filter the noise.

(2) Input the simulated biomedical signal sine wave, which is produced by the function generator, to the CBIA.

(3) Input voltage to digital selected input of the multiplexer to pass a channel which we want to analyze.

(4) Set the sampling frequency of SCLPF by the function generator producing a suitable clock.

(5) Input voltage to digital selected input of the decoder to choose appropriate voltage gain by passing the resistor switch.

(6) Connect the output of PGA to an oscilloscope to observe the output wave of the AFEIC. If the AFEIC is function work, and the result of testing is similar to the figures as Fig. 3-24~Fig. 3-27.

(7) Outputs of the multiplexer and decoder have pins. If the multiplexer or decoder is failure, input the signals to the output of the multiplexer or decoder to test other analog circuits.

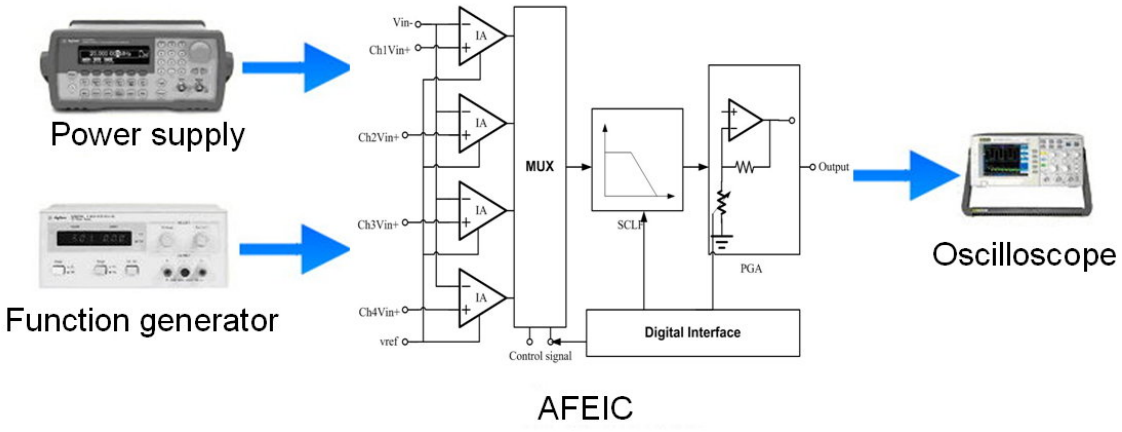

Fig. 4-18 The architecture of testing the chip.

Chapter 5
Conclusions

5.1 Conclusion

The study realized a tunable bandwidth/gain circuit design of multi-channel biomedical signals acquisition. Besides low power consumption and low noise, it increased the characteristics of CMRR and PSRR. The AFEIC is integrated on a chip, that is SoC, and it has advantages of low cost and size. It is conducive to integrate the embedded biomedical system. The feature of AFEIC is that utilized the characteristic of self-circuit to reduce additional circuit design and area. For example, the four CBIAs shared a large resistor, R_s, by the decoder in the multiplexer to control, multi-channel design shared a SCFLP and a PGA to reduce the area of the circuit, SCFLP utilized different clock frequency to select different bandwidth of the system, and PGA utilized different MOS switches in one series resistor to select different gain ratio. The way of using a series resistor is save more resistors than using a parallel resistor and reduces layout area directly.

5.2 Future Work

The thesis has had superiority in the biomedical signals recording system according to the result of the AFEIC post-layout simulation. However, the AFEIC is still worth improving further in the future. For example, reduce the phase delay in the SCLPF, consume lower power, use battery to supply the power of AFEIC, integrate with digital circuit, ADC and embedded system, has fewer noise, etc.

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Appendix

A. DRC Verification

Whole Chip DRC

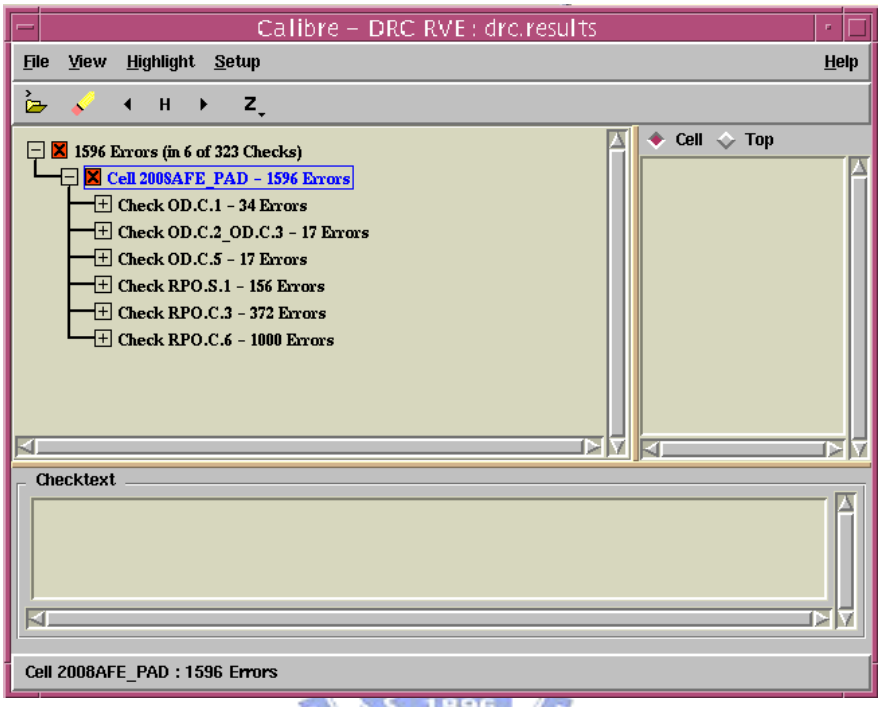

圖 I 全系統晶片之 DRC 驗證

其中DRC ERROR 為I/O PAD內部錯誤，錯誤訊息皆在PAD，為可忽略的錯，如圖II所示。

常見command file判斷錯誤

原因	適用	座標標示
STC I/O PAD ERROR	STC18io_18T	N/A
批註用編號		
OD.C.1 OD.C.2_OD.C.3 OD.C.5 RPO.S.1 RPO.C.3 RPO.C.6		

圖II 可允許DRC錯誤說明

B. LVS Verification

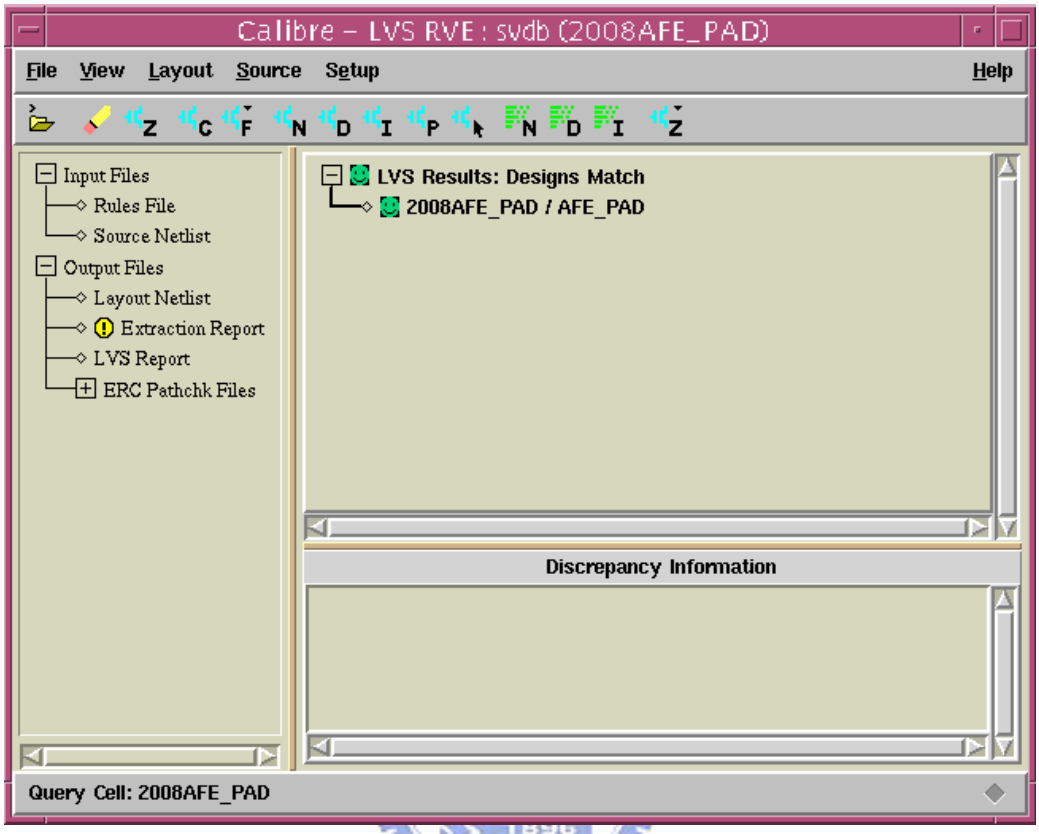

圖 III 全系統晶片之 LVS 驗證無誤

```
                    CELL COMPARISON RESULTS  ( TOP LEVEL )


                         #       ###################
                       #         #                 #       ∓   ∓
                     #   #       #     CORRECT     #         |
                      # #        #                 #       \___/
                       #         ###################


  Warning:  Ambiguity points were found and resolved arbitrarily.

LAYOUT CELL NAME:          2008AFE_PAD_v1
SOURCE CELL NAME:          AFE_PAD_1
```

INITIAL NUMBERS OF OBJECTS

	Layout	Source		Component Type
Ports:	32	32		
Nets:	1211	274	*	
Instances:	850	210	*	MN (4 pins)
	538	187	*	MP (4 pins)
	236	13	*	C (2 pins)
	1014	75	*	R (2 pins)
Total Inst:	2638	485		

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	32	32	
Nets:	223	223	
Instances:	190	190	MN (4 pins)
	105	105	MP (4 pins)
	13	13	C (2 pins)
	75	75	R (2 pins)
	9	9	SDW2 (3 pins)
	31	31	SUP2 (3 pins)
	1	1	SMN2 (4 pins)
	10	10	SMP2 (4 pins)
Total Inst:	434	434	

* = Number of objects in layout different from number in source.

****

INFORMATION AND WARNINGS

****

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Ports:	32	32	0	0	
Nets:	223	223	0	0	
Instances:	190	190	0	0	MN(N)
	105	105	0	0	MP(P)
	13	13	0	0	C(M5)
	30	30	0	0	R(PR)
	45	45	0	0	R(WR)
	9	9	0	0	SDW2
	31	31	0	0	SUP2
	1	1	0	0	SMN2
	10	10	0	0	SMP2
Total Inst:	434	434	0	0	

C. Tapeout Review Form

Tapeout review form 的用意在提醒設計者在設計、模擬、佈局、佈局驗證及 tapeout 時具備設計理念及了解應注意事項,希望能藉此提昇晶片設計的成功率及達到完整的學習效果。因此,請指導教授及設計者確實檢查該晶片設計過程是否已注意本表格之要求,並在填寫確定後簽名,若審查時發現設計內容與 Tapeout Review Form 之填寫不符,很可能遭取消該晶片下線製作資格。可參考本表後所附範例確實填寫。

1 電路概述

專題名稱: 可調式頻寬/增益之四通道生理訊號擷取晶片設計

1-1. Top Cell 名稱: 2008AFE_PAD_v1

1-2. 製程名稱: TSMC 0.18um CMOS Mixed Signal RF General Purpose MiM Al 1P6M 1.8&3.3V

1-3. 工作電壓: +/- 0.75V

1-4. 工作頻率: 2MegaHz(Max)

1-5. 功率消耗: 112.6837uW

1-6. 是否使用 CIC 提供之 ARM CPU IP？ 否

使用 CPU 之種類爲何？(ARM7TDMI or ARM926EJ)

1-7. 此電路架構於貴實驗室是否第一次設計?是(接 2-1)___否(接 1-6-1) V

1-7-1. 此電路之前不 work 或 performance 不好的原因爲何?

(1) 部分 work：其數位部分的 CLK Generator 不能夠正常動作，使其影響整體電路之運作，推測當初沒有加上足夠的負載去設計。

(2) Performance：(a)之前電路架構爲單一通道的電路

(b)工作電壓爲+/-1.5V，略顯過高

(c)切換電容式低通濾波器無考慮到 charge injection 之效應

1-7-2. 對之前的錯誤作何種修改?

(1) CLK Generator 有加入足夠的負載去模擬，使其能正常運作。

(2) 將電路改爲四通道之架構，且有許多共用電路，更節省面積。

(3) 將工作電壓降爲+/-0.75V。

(4) 利用不同的數位時脈切換，降低 charge injection 的效應。

2 電路模擬考量

2-1． 已用 SS,SF,TT,FS,FF 中哪些不同狀態之 spice model 模擬? 五種皆有模擬

2-2． 已模擬過電壓變動+/-10%中哪些情況對電路工作之影響? 是

2-3． 如何考量溫度變異之影響? 已從-25℃~95℃ 測試過前端電路增益與濾波的影響

2-4． 如何考量電阻、電容製程變異之影響? 加入 Dummy 及使用受製程變異較小的架構

2-5． 模擬時是否加入 IO PAD、Bonding wire 的效應及考量測試儀器之負載等影響? 是

2-6． 是否作 LPE 及 post layout simulation? 是 使用的軟體爲 Laker, Calibre, Hspice

3 Power Line 佈局考量

3-1. Power Line 畫多寬? ＞5um

3-2. 是否考量 power line current density? 是

3-3. 是否考量 Metal Line 之寄生電阻、電容? 是

4 DRC,LVS

4-1. 是否有作 whole chip 的 DRC 及 LVS? 是，whole chip DRC&LVS 驗證正確

4-2. 除了 PAD 上 DRC 的錯誤之外,內部電路及與 PAD 連接的線路是否有錯?_否__錯誤原因爲何?_____

4-3. 在作 LVS 的過程中,PIN 腳及元件是否 match?__是___ 不 match 的原因爲何?_____

4-4. 檢查 PAD 與 PAD 間是否有移位、短路或斷路的現象? 否，DRC&LVS 驗證正確

5 類比-混合訊號電路佈局考量(類比-混合訊號電路設計者填寫)

5-1 佈局對稱性及一致性考量

5-1-1 OP(Comparator) Input Stage 是否對稱? 是

5-1-2 OP(Comparator) Input Stage 是否對稱? 是

5-1-3 佈局中對稱元件是否使用 dummy cell 技巧? 是

5-1-4 對稱電容是否採用同心圓佈局? 是

5-1-5 對稱單位電容四周是否切成 45 度斜角? 是

5-1-6 對稱電容的單位面積是否一致? 是

單位電容面積多大? 10.66 um x 10.66 um

單位電容值多大? 0.1 pF

5-1-7 電阻採用哪一材質製作? P+ poly resistor with RPO

單位電阻值多大? 1kΩ

5-2 電路雜訊佈局考量

5-2-1 是否將 Analog 及 Digital 的 power line 分開? 是

5-2-2 Analog area 是否用 guard ring 隔絕? 是

5-2-3 Digital area 是否用 guard ring 隔絕? 是

5-2-4 對於 sensitive line 是否使用 shield 的技巧? 是

5-2-5 Analog guard ring 及 shield 是否接至乾淨之電位? 是

5-2-6 是否將 sensitive line 儘量縮短及避免跨越 noise(clock)line? 是

5-2-7 電容的上下極板是否接對? 是

6 MEMS 設計考量(MEMS 設計者填寫)

6-1 請簡述所進行之後製程：_____

6-2 後製程操作地點：_____

6-3 下線者目前是否有操作該製程設備之合法授權?_____若目前無操作該製程設備之合法授權，是否可在晶片取回前得到合法授權?_____

6-4 下線者是否有使用該製程設備之經驗?_____

6-5 是否有該後製程之製程參數（壓力、溫度、流量、……）?_____

6-6 之前是否有成功實現過該後製程?_____

6-7 Layout 違反 design rule 的部分是否會影響微結構本身或元件操作？___

6-8 Layout 之蝕刻孔尺寸是否足以讓結構懸浮?_____

6-9 元件驅動電壓範圍?_____

7 RF Circuit 電路佈局考量 (RF 操作頻段設計者填寫)：

7-1 電路規格適用何種系統? _____

7-2 說明被動元件模型的來源 _____

7-3 模擬軟體 (可不只一種)? _____

7-4 系統整合 chip 裡之各個 block 是否曾下過線且量測符合預期規格 (chip 爲系統整合者回答,並說明製程梯次代號)?_____

7-5 佈局考量：

7-5-1 元件佈局方式是否與模型提供者所提供的佈局一致? _____

7-5-2 接地與電壓源是否均勻? _____

7-5-3 元件與拉線的電流承載能力考量? _____

7-5-4 拉線是否過長過細? _____

7-5-5 PAD 的佈局是否配合量測上之考量? _____

7-5-6 PAD 與 Bond-wire 的效應是否考量? _____

7-6 DRC 驗證過程中, 部分錯誤若爲特殊考量, 請說明_____

_____

_____

7-7 LVS 驗證過程中, 電感電容或其他特殊元件的比對是否做過處理, 請說明_____

_____

_____

7-8 量測方式爲 on wafer, on PCB or in package? 並說明量測時應該注意事項與量測地點

_____

_____

8 PAD Replacement 考量(使用 TSMC I/O PAD 設計者填寫)

8-1 已於申請表勾選申請使用 TSMC I/O PAD

8-2 個人設計的 Cell 名稱(cell-name)未與 TSMC 所提供之任一 Pad Cell 名稱相同__是____

8-3 採用 Create Instance 方式加入 I/O Pad，未用 Copy 或 Flatten 破壞 Instance 的結構 是

8-4 由 IC Core 部份拉線到 Pad 只拉到最邊緣部分，未過於覆蓋 Pad__是__

9. 使用 ARM926EJ or ARM7TDMI CPU IP

9-1. 若有使用 ARM926EJ /ARM7TDMI CPU IP，請提供以下訊息以便向 ARM 原廠申請 Design ID。

使用的 CPU 種類 (ARM926EJ or ARM7TDMI) :_____

使用的 metal layers 的層數:_____

佈局中 ARM926EJ /ARM7TDMI Macro 的 cell name:_____

這個晶片是否爲修訂版本(revision,也就是之前曾下線過相同晶片)？_____

若是修訂版本，前一次下線的晶片編號:_____

修訂版本的原因是？(例如修正 bug) _____

10 其他考量

10-1 是否考量測試時的輸出量測點?__是_____

10-2 是否考量電路之可修改性(如用 laser cut 設備)__是_____

設計者簽名:___戴毓廷_____ 指導教授簽名:___林進燈____