國立交通大學

電子工程學系 電子研究所

博士論文

互補式金氧半積體電路之系統層級靜電放電防護設計

SYSTEM-LEVEL ESD PROTECTION DESIGN IN CMOS ICS WITH TRANSIENT DETECTION CIRCUITS

研 究 生：顏承正(Cheng-Cheng Yen)

指導教授：柯明道(Ming-Dou Ker)

中華民國九十八年四月

互補式金氧半積體電路之系統層級靜電放電防護設計

SYSTEM-LEVEL ESD PROTECTION DESIGN IN CMOS ICS WITH TRANSIENT DETECTION CIRCUITS

研究生：顏承正　　Student: Cheng-Cheng Yen
指導教授：柯明道　　Advisor: Ming-Dou Ker

國立交通大學
電子工程學系電子研究所
博士論文

A Dissertation
Submitted to Department of Electronics Engineering &
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy
in
Electronics Engineering

April 2009
Hsinchu, Taiwan, Republic of China

中華民國九十八年四月

互補式金氧半積體電路之系統層級靜電放電防護設計

研究生：顏承正　　　　　　　　　　指導教授：柯明道 博士

國立交通大學電子工程學系電子研究所

摘要

在互補式金氧半積體電路中，系統層級靜電放電測試(System-Level ESD Test)已成為一個重要的可靠度問題。由於日益複雜的積體電路功能，如混合式信號(Mix-Signal)電路、多重電源供應系統(Multiple Power Supplies)、射頻(Radio Frequency, RF)電路、系統單晶片(System on Chip)等等，使得積體電路元件所處的環境會受到來自元件內部或外部的雜訊干擾，因此這些雜訊會隨機地出現在積體電路產品的電源、接地、輸入/輸出腳位(Pin)上，使積體電路產品較以往更容易受到雜訊干擾的威脅。隨著半導體元件尺寸的微縮，過去的研究已經證實在系統層級靜電放電測試以及快速暫態脈衝測試(Electrical Fast Transient Test)之下，暫態的干擾訊號會使寄生在互補式金氧半導體積體電路中的矽控整流器(Silicon ControlledRectifier, SCR)產生閂鎖效應。由系統層級靜電放電測試所引起的可靠度問題來自於多功能整合型的積體電路設計，以及嚴格的法規要求。在系統層級靜電放電測試的規格中(IEC 61000-4-2)，一個擁有積體電路的電子設備在接觸放電(Contact-Discharge)及空氣放電(Air-Discharge)測試模式中如欲達到“等級四”的標準需求，則此待測設備(Equipment Under Test, EUT)必須通過高達±8kV(接觸放電模式)及±15kV(空氣放電模式)的靜電放電等級需求。

在傳統的解決方法中，會在電子產品的印刷電路板上增加離散元件(Discrete Component)抑制暫態雜訊的干擾，包括利用反耦合電容(Decoupling Capacitor)、Ferrite

Choke、暫態突波抑制器(Transient Voltage Suppressor)、限流電阻(Current-Limiting Resistance)、防護板(Shielding Plate)等，皆能在印刷電路板抑制對積體電路產品所產生的暫態雜訊干擾，但是這些額外增加的離散元件會大幅增加電子產品的成本。因此在以積體電路方式提出相關的解決方案，設計出符合高階系統層級靜電放電測試規格以及減少離散元件使用的電子產品，將會為工業界所急切需求。

有鑒於此，本論文將針對用於系統層級靜電放電防護所需的暫態偵測電路積體電路設計進行研究分析。主要的研究方向包括：(1) 評估不同電源匯流排之間的靜電放電箝制電路(Power-Rail ESD Clamp Circuit)結構對於系統層級靜電放電測試的耐受度，(2) 在快速脈衝測試時暫態觸發閂鎖效應的物理機制，(3) 評估各種面板層級(Board-Level)雜訊濾波器對抑制暫態觸發閂鎖效應的效用，(4) 暫態偵測電路積體電路設計方法(IC Design Methodology)，以及(5) 暫態數位轉換器積體電路設計方法。

本論文第二章首先評估不同電源匯流排之間的靜電放電箝制電路(Power-Rail ESD Clamp Circuit)結構對於系統層級靜電放電測試以及快速暫態脈衝測試的耐受度。在本論文中，發現在電源匯流排之間的靜電放電箝制電路結構中具有鎖存迴授迴路以及串接PMOS 迴授迴路電路架構容易產生似閉鎖效應(Latchup-Like Failure)之故障出現，在系統層級靜電放電以及快速暫態脈衝測試過後，在電源(V_{DD})與地端(V_{SS})之間導致巨大電流通過，容易使積體電路產品因過大電流而損毀。相較於以三級反相器為主的靜電放電箝制電路架構，該具有鎖存迴授迴路以及串接 PMOS 迴授迴路的電源匯流排之間的靜電放電箝制電路架構較易發生類似閂鎖效應(Latchup-Like Failure)之故障狀況。本論文中提出一個結合鎖存迴授迴路以及利用 NMOS 產生回復功能的新電源匯流排之間的靜電放電箝制電路結構，經實驗晶片驗證，本研究所提出的電源匯流排間靜電放電箝制電路結構可成功避免類似閂鎖效應的觸發，以及具有高箝制能力且能節省佈局面積，可應用在全晶片之靜電放電防護設計上。

本論文第三章針對在快速暫態脈衝測試時造成暫態觸發閂鎖效應的物理機制加以探討分析。經由相關的實驗量測驗証，本論文發現快速暫態脈衝測試將導致一種電壓振幅會隨時間遞減的脈衝震盪電壓產生於積體電路的電源腳位上。此種電壓會使儲存於積體電路內的少數載子(Minority Carrier)快速移動，進一步形成“掃回電流(Sweep-Back Current)”而引發暫態觸發閂鎖效應。本論文所提出的實驗驗證提供實用的研究分析工具，以期能進一步發展出能有效防止暫態觸發閂鎖效應的電路設計技巧、佈局(Layout)準則、以及半導體製程技術。為了能更進一步地提升積體電路對暫態觸發閂鎖效應的防

護能力，本論文更評估了不同面板層級雜訊濾波器對抑制暫態觸發閂鎖效應的實際效用。這些雜訊濾波元件包括電容濾波器、電容−電感濾波器(LC-Like)、π形濾波器、亞鐵鹽珠(Ferrite Bead)、暫態突波抑制器(Transient Voltage Suppressor, TVS)、及混合式濾波器等。藉由這些雜訊濾波元件反耦合(Decouple)或吸收因快速暫態脈衝測試在積體電路電源(地)端造成的瞬間雜訊，則積體電路對抑制暫態觸發閂鎖效應的防護能力將可有效提升。所得到的實驗結果可提供印刷電路板(Printed Circuit Board, PCB)設計者一個有用的參考準則，以期能利用適當的雜訊濾波器來有效提升積體電路對暫態觸發閂鎖效應的防護能力。

本論文第四章是在 0.18-µm 3.3-V CMOS 製程技術中，所實現的暫態偵測電路(Transient detection Circuit)。此偵測電路是利用閉鎖電路的架構來設計，利用 HSPICE 軟體所提供的正弦波以及阻尼因子(Damping Factor)的參數設定，可成功模擬並量化暫態偵測電路在系統層級靜電放電以及快速暫態脈衝測試時的工作情形。電路系統的模擬狀態包括了在電源線與地線上的同步干擾，或因為電路板繞線差異或待測元件擺放位置不同而造成在電源線與地線之間的非同步干擾情形，以及在各種不同製程參數下對於暫態偵測電路的影響。此暫態偵測電路在系統層級靜電放電或是快速暫態脈衝發生時，可偵測出發生在電源線上的暫態干擾訊號並紀錄之，並配合韌體或軟體設定，使電路在受到電磁干擾而故障時，能送出重新啟動訊號(Reset)使系統自動作回復的動作。此暫態偵測電路可整合至 CMOS 晶片中，並可結合韌體的使用，以提升待測電子產品對系統層級靜電放電以及快速暫態脈衝測試的防護能力。

本論文第五章是在 0.18-µm 1.8-V CMOS 製程技術中，所實現的暫態偵測電路。此偵測電路是利用反相器電路架構以及電阻電容延遲效應來設計，利用 HSPICE 軟體所提供的正弦波以及阻尼因子(Damping Factor)的參數設定，可成功模擬並量化此暫態偵測電路在系統層級靜電放電以及快速暫態脈衝測試時的工作情形。此暫態偵測電路在系統層級靜電放電或是快速暫態脈衝發生時，已成功驗證可偵測出發生在電源線上的暫態干擾訊號並紀錄之，使電子產品在受到電磁干擾而故障時，可配合韌體或軟體設定送出重新啟動訊號(Reset)使系統自動作回復的動作。

本論文第六章是結合暫態偵測電路以及積體電路濾波電路(On-Chip Noise Filter Network)，發展完全整合於積體電路上(Full Integrated Circuit)能輸出數位編碼訊號的暫態數位轉換器(Transient-to-Digital Converter)。在系統層級靜電放電測試時，暫態數位轉換器所輸出的數位編碼訊號會對應不同電壓準位的暫態突波。在整體系統的設計上，利

用結合韌體(Firmware)的系統設計，制定出具有執行自動恢復功能的整體系統規劃。當有快速變化且具有低電壓準位的暫態突波發生時，暫態數位轉換器會送出低位元數位編碼訊號，可做為韌體執行部分系統自動重新恢復(Partial System Auto-Recovery)的指標(Index)，指標訊號可暫存於韌體中，並經由回授程式的不斷檢測，直至暫態突波的影響消失為止。當有快速變化且具有低電壓準位的暫態突波發生時，暫態數位轉換器會送出高位元數位編碼訊號，可做為韌體執行全部系統自動重新恢復(Total System Auto-Recovery)的指標。因此，利用結合暫態數位轉換器以及韌體的系統規劃的設計方式，以期增進顯示電子產品對系統規格靜電放電的全晶片防護能力。

以上針對用於系統層級靜電放電測試的積體電路設計方法，快速暫態脈衝測試造成的暫態閂鎖效應特性，以及暫態偵測電路晶片設計，本論文所進行的相關研究皆有實際晶片量測，並有相對應的國際會議及期刊論文發表。

SYSTEM-LEVEL ESD PROTECTION DESIGN IN CMOS ICS WITH TRANSIENT DETECTION CIRCUITS

Student: Cheng-Cheng Yen **Advisor: Dr. Ming-Dou Ker**

Department of Electronics Engineering and Institute of Electronics
National Chiao-Tung University

Abstract

System-level electrostatic discharge (ESD) events have become a primary reliability issue in CMOS integrated circuit (IC) products. With more and more complicated design of integrated circuits, such as mixed-signal, mixed-voltage, system-on-chip (SOC), etc, CMOS devices will suffer more electrical transient noises coming from environment and the interior of CMOS ICs. With advanced semiconductor technology of scaled clearance between PMOS and NMOS devices, it has been proven that such electrical transient noises can cause transient-induced latchup (TLU) failure on the inevitable parasitic silicon controlled rectifier (SCR) in CMOS ICs under system-level ESD and electrical fast transient (EFT) tests. The reliability issue of system-level ESD events results from not only the progress of more integrated functions into a single chip but also from the strict requirements of reliability test standards, such as the system-level ESD test standard of IEC 61000-4-2. The microelectronic products must sustain the ESD level of ±8kV (±15kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4" in the IEC 61000-4-2 test standard.

The additional noise filter networks, such as the magnetic core, capacitor filter, ferrite bead (FB), transient voltage suppressor (TVS), RC filters, are often used to improve the system-level ESD immunity of microelectronic products. The system-level ESD immunity of CMOS ICs under system-level ESD test can be significantly enhanced by choosing proper

noise filter networks. However, the additional discrete noise-bypassing components substantially increase the total cost of microelectronic products. Therefore, the chip-level solutions to meet high system-level ESD specification for microelectronic products without additional discrete noise-decoupling components on the microelectronic products are highly desired by IC industry.

This dissertation focuses on the chip-level solutions for the system-level ESD protection design. Several major topics including: (1) investigation on the latchup-like failure of power-rail ESD clamp circuits under system-level ESD tests, (2) clarification of TLU physical mechanism under EFT tests, (3) evaluations of board-level noise filters to suppress TLU, (3) proposed on-chip transient detection circuits, and (5) proposed transient-to-digital converters.

In chapter 2, four power-rail ESD clamp circuits with different ESD-transient detection circuits were fabricated in a 0.18-µm CMOS process and tested to compare their system-level ESD and EFT susceptibility, which are named as power-rail ESD clamp circuits with typical RC-based detection, PMOS feedback, NMOS+PMOS feedback, and cascaded PMOS feedback in this work. During the system-level ESD and EFT tests, where the ICs in a system have been powered up, the feedback loop used in the power-rail ESD clamp circuits provides the lock function to keep the ESD-clamping NMOS in a “latch-on” state. The latch-on ESD-clamping NMOS, which is often drawn with a larger device dimension to sustain high ESD level, conducts a huge current between the power lines to perform a latchup-like failure after the system-level ESD and EFT tests. A modified power-rail ESD clamp circuit is proposed to solve this problem. The proposed power-rail ESD clamp circuit can provide high enough chip-level ESD robustness, and without suffering the latchup-like failure during the system-level ESD and EFT tests.

In chapter 3, the occurrence of TLU in CMOS ICs under the EFT tests is studied. The test chip with the parasitic SCR structure fabricated by a 0.18-µm CMOS process was used in the EFT tests. For physical mechanism characterization, the specific “sweep-back” current caused by the minority carriers stored within the parasitic PNPN structure of CMOS ICs is the major cause of TLU under EFT tests. Different types of board-level noise filter networks are evaluated to find their effectiveness for improving the immunity of CMOS ICs against TLU under EFT tests. By choosing proper components in each noise filter network, the TLU immunity of CMOS ICs against EFT tests can be greatly improved.

In chapter 4, a novel RC-based on-chip transient detection circuit for system-level ESD and EFT protection are proposed in this work. The circuit performance to detect positive and negative electrical transients under system-level ESD and EFT testing conditions has been investigated by the HSPICE simulation and verified in silicon chip. The experimental results have confirmed that the proposed on-chip transient detection circuit can successfully memorize the occurrence of the system-level ESD and EFT events. The detection output of proposed on-chip transient detection circuits can be used as the firmware index to execute system recovery procedure to provide a hardware/firmware co-design to improve the immunity of CMOS IC products against electrical transient disturbance.

In chapter 5, a new on-chip transient detection circuit for electrical fast disturbance protection design is proposed in this work. The circuit performance to detect different positive and negative ESD-induced or EFT-induced transient disturbance has been investigated by the HSPICE simulation and verified in silicon chip. The EFT generator combined with attenuation network and capacitive coupling clamp has been used as the evaluation method to verify the detection function of the proposed on-chip transient detection circuit under EFT tests. The test chip in a 0.18-μm CMOS process with 1.8-V devices has confirmed that the proposed on-chip transient detection circuit can successfully detect and memorize the occurrence of the transient disturbance under system-level ESD or EFT tests.

In chapter 6, a novel on-chip transient-to-digital converter composed of four RC-based transient detection circuits and four different RC filter networks has been successfully designed and verified in a 0.18-μm CMOS process with 3.3-V devices. The output digital thermometer codes of the proposed on-chip transient-to-digital converter correspond to different ESD voltages under system-level ESD tests. These output digital codes can be used as the firmware index to execute different auto-recovery procedures in microelectronic systems. Thus, the proposed on-chip transient-to-digital converter can be further combined with firmware design to provide an effective solution to solve the system-level ESD and EFT protection issue in microelectronic systems equipped with CMOS ICs.

Chapter 7 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in this chapter.

Acknowledgment

感謝柯明道教授的指導與專業領域上的訓練。感謝交通大學吳重雨校長、晶焱科技姜信欽博士、奇景光電陳東暘博士、中山大學王朝欽教授、交通大學吳介琮教授、交通大學蘇朝琴教授在百忙之中抽空擔任我的口試委員，並給予珍貴的指導與建議，讓此博士論文更加完整。

感謝任職於奇景光電的蔡志忠技術長、陳東暘博士鼎力協助實驗晶片下線與研究工作進行，使本論文的研究成果得以成功驗證，並順利發表於國際期刊與國際研討會。

感謝實驗室的陳世倫博士、許勝福博士、陳榮昇博士、張瑋仁博士、蕭淵文博士、陳世宏博士、徐振洲學長、羅文裕學長、黃鈞正學長、阿傑、祖德、豪哥、瑋明、羅怡凱、台祐、二師兄、邱大人、范振麟、霸子、金毛、智閔、與陳穩義、賴泰翔、王資閔、林群祐、邱柏硯、蔡惠雯、弼嘉、莊介堯、俊哥、蒙神、鯉魚、世範、小州哥、佳琪、翁怡歆、林宛彥等同學與學弟妹們在研究與生活上的協助與扶持，尤其在我心情低落時，很多人給我許多鼓勵。感謝任職於晶焱科技的賢哥、阿貴、志豪哥、小李、小黑、阿方、蔡耀城學長、子平學長給我的許多幫助與支持。特別感謝學弟廖期聖在晶片設計與製作上的用心與努力，可以使相關的研究順利進行。爸爸開刀期間，謝謝蕭淵文博士常常幫我處理投稿的論文。口試前一個月來回新竹台北加護病房，謝謝陳穩義、小胖、小州哥、佳琪幫我處理口試準備的事情，我很珍惜大家幫助過我的一切，謝謝你們。此外，感謝實驗室助理卓慧貞小姐在行政事務上的許多協助。

謝謝新竹馬偕醫院洗腎室的醫師與護士照料長期洗腎的父親。謝謝淡水馬偕的羅鈺華護理師，台北振興醫院開刀房的小英，慈濟大林醫院的嬋芳，高雄榮總的雅婷，在爸爸各地看診期間給予的幫助跟關懷。我要特別感謝新竹東區扶輪社以及耳鼻喉科林安復醫師，在生活上以及醫療上給予我們的幫助，在面對許多洗腎的併發病症以及被診斷出鼻咽腫瘤時，林醫師細心幫爸爸看診並給予我們建議與協助，許多畫面至今令我感動以及難忘。

由衷感謝敬愛的父親顏色先生、母親黎柑妹女士、姊姊顏承真小姐、姊夫曾明育先生、兩位可愛的外甥女圓元跟詣琁。感謝親人的支持、陪伴與照顧，讓我順利完成學業。感謝所有幫助我、陪伴我一同成長的師長、長輩、朋友、學長姊、同學、學弟妹們，願大家平安喜樂。

顏承正
誌於竹塹交大
九十八年 春

Contents

Table Captions

Chapter 1

Chapter 2

Chapter 6

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

Chapter 1

Introduction

In this chapter, the background and the organization of this dissertation are discussed. First, the background of transient disturbance events is introduced. Secondly, the system design solutions are discussed. Finally, the organization of this dissertation is well described.

1.1. Background

Electrical transient disturbance events have become an important reliability issue to integrated circuits (ICs). To meet the component-level ESD reliability, on-chip ESD protection circuits have been added to the I/O cells and power (V_{DD} and V_{SS}) cells of CMOS ICs [1]-[8]. Besides the component-level ESD stress, electrical transient disturbance is an increasingly significant reliability issue in CMOS integrated circuit (IC) products. This tendency results from the strict requirements of reliability test standards, such as system-level ESD test for electromagnetic compatibility (EMC) regulation. In the system-level electrostatic discharge (ESD) test standard of IEC 61000-4-2 [9], the electrical/electronic product must sustain the ESD level of ±8 kV (±15 kV) under contact-discharge (air-discharge) test mode to meet the immunity requirement of “level 4.” Such high-energy ESD-induced noises often cause damage or malfunction of CMOS ICs inside the equipment under test (EUT). It has been reported that some CMOS ICs are very susceptible to electrical transient disturbance [10]-[18], even though they have passed the component-level ESD specifications such as human-body-model (HBM) of ±2 kV [19], [20], machine-model (MM) of ±200 V [21], [22], and charged-device-model (CDM) of ±1 kV [23]-[25].

1.2. Issue of Transient Disturbance Events

1.2.1. System-Level ESD Tests

The equivalent circuit of ESD gun used in the system-level ESD test is shown in Fig. 1.1 The ESD gun has the charging (energy-storage) capacitor of 150 pF and discharge resistor of 330 Ω. The equivalent circuit of human body model (HBM) in the component-level ESD test is shown in Fig. 1.2 In the HBM component-level ESD test, however, the charging capacitor (discharge resistor) is a smaller (larger) value of 100pF (1.5 kΩ). Thus, compared with the ESD current in component-level ESD test, ESD current in system-level ESD test has a much larger peak current and a shorter rise time, leading to more severe damages for electronic products or their interior ICs. The ESD-induced energy can be zapped out of the mechanism with ESD gun in faster speed.

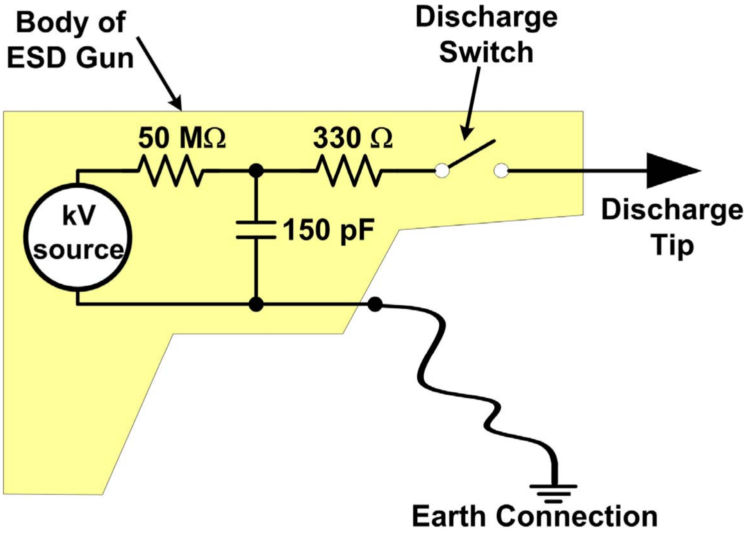


Fig. 1.1 Equivalent circuit of ESD gun used in the system-level ESD test. The ESD gun has the charging (energy-storage) capacitor of 150 pF and discharge resistor of 330 Ω.

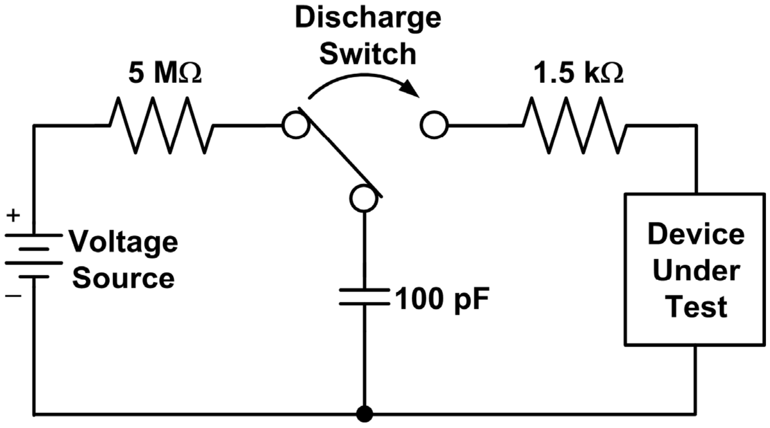


Fig. 1.2 Equivalent circuit of human body model (HBM) in the component-level ESD test. The charging capacitor (discharge resistor) is a smaller (larger) value of 100 pF (1.5 kΩ).

Fig. 1.3 shows the typical waveforms of the discharge current under system-level ESD test (IEC 61000-4-2) and component-level ESD test (MIL-STD 883). Under 8-kV ESD zapping, the peak current in system-level ESD test is about five times larger than that in component-level ESD test. Additionally, ESD protection designs for system- and component-level ESD tests are quite different. It has been proven [10] that a robust CMOS IC product with high component-level ESD levels could be very susceptible to the system-level ESD test. Thus, efficient ESD protection methodologies against system-level ESD events are very significant for electronic products.

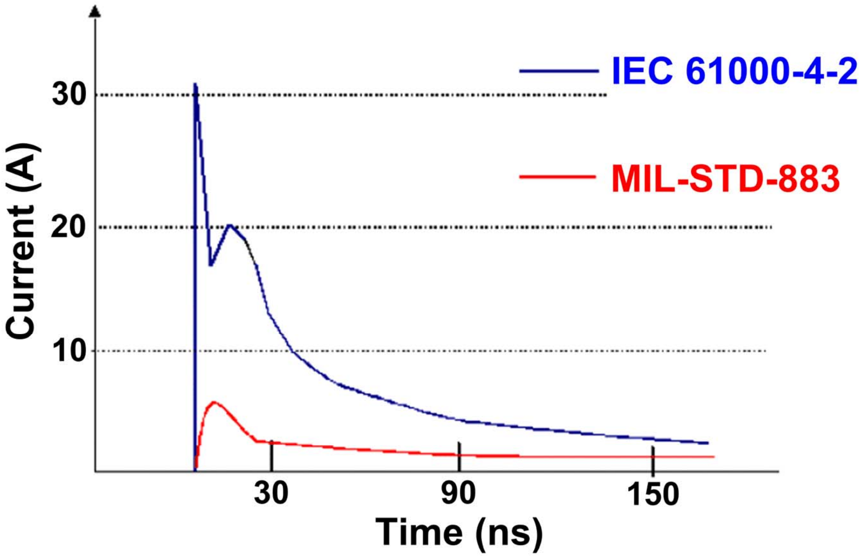


Fig. 1.3 Under 8-kV ESD zapping, the peak current in system-level ESD test is about five times larger than that in component-level ESD test.

In the IEC 61000-4-2 standard [9], two test modes have been specified, which are the air-discharge test mode and the contact-discharge test mode. Contact discharge is further divided into direct discharge to the system under test, and indirect discharge to horizontal or vertical coupling planes. Fig. 1.4 shows the standard measurement setup of the system-level ESD test in the indirect contact-discharge test mode. As shown in Fig. 1.5, in the air discharge test mode, the round discharge head of ESD gun is brought close to the EUT. In the contact discharge test mode, the sharp discharge head of ESD gun is held in contact with the EUT. The measurement setup for system-level ESD test consists of a wooden table on the grounded reference plane (GRP). In addition, an insulation plane is used to separate the EUT from the horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470 kΩ resistors in series. When the ESD gun zaps the HCP, the electromagnetic interference (EMI) coming from ESD will be coupled into all CMOS ICs inside EUT. The power lines of CMOS ICs inside EUT will be disturbed by the ESD-coupled energy.

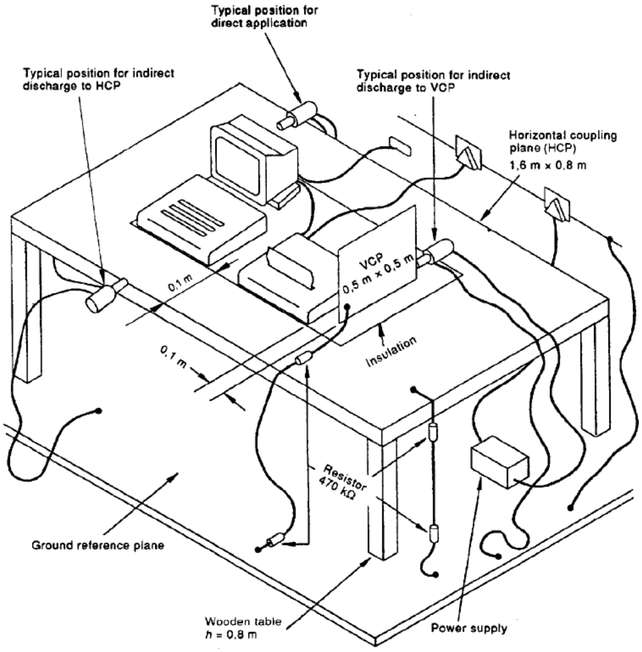


Fig. 1.4 Measurement instruments of system-level ESD test [9].

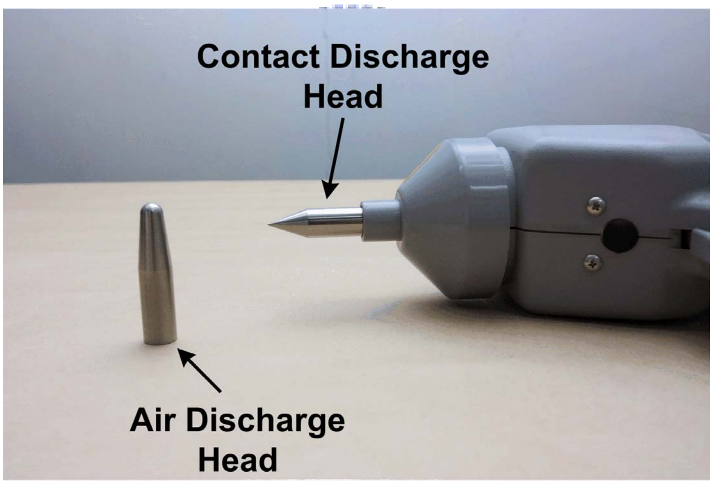


Fig. 1.5 Discharge electrodes of ESD gun which is used under system-level ESD test with contact discharge mode and air discharge mode.

The object of the standard, IEC 61000-4-2 is to establish a common and reproducible basis for evaluating the performance of CMOS ICs inside the electrical/electronic microelectronic products. This standard specifies typical waveform of the discharge current, test levels, test equipment, test set-up, and test procedure. In order to verity the disturbance under system-level ESD test, the ESD gun is used to zap the ESD-induced energy into the equipment under test. In order to compare the test results in system-level ESD and component-level ESD standards, the characteristics of the waveform of discharge current are shown in Table 1.1. Table 1.2 shows the test level (test voltage) of component-level ESD test such as human body model (HBM), machine model (MM), and charge device model (CDM) in usual condition. The system-level ESD test level with contact discharge and air discharge is shown in Table 1.3. Contact discharge is the preferred test method, and air discharge shall be used where contact discharge can't be applied. It is not intended to imply that the test severity is equivalent between contact discharge and air discharge test methods. To compare Table 1.3 with Table 1.2, the test voltage of system-level ESD is lager than component-level ESD, no matter with contact discharge or air discharge. Noteworthiness, the voltages shown are different for each method due to the different methods of test. According to those phenomena, system-level ESD is more significant to influence the microelectronic products than component-level ESD in some situations. Table 1.4 shows the evaluation of test results, the test results shall be classified in terms of loss function or degradation of performance of the equipment under test. Generally speaking, the microelectronic product should reset itself automatically after system-level ESD test to pass the "Class B" specification at least. The equipment under test shall be operated within the specified climatic conditions to avoid unnecessary electromagnetic environment of the laboratory influencing the test results.

Table 1.1
Waveform Parameters of System-Level ESD Discharge Current

Level	Indicated Voltage (kV)	First Peak Current ±10% (A)	Rise Time (ns)	Current (±30%) at 30ns (A)	Current (±30%) at 60ns (A)
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

Table 1.2
Component-Level ESD Specifications

Model Name	Test Voltage
Human Body Mode	> 2000V
Machine Mode	> 200V
Charge Device Mode	> 1000V

Table 1.3
Levels of System-Level ESD Test

Contact Discharge		Air Discharge	
Level	**Test Voltage (kV)**	**Level**	**Test Voltage (kV)**
1	**± 2**	**1**	**± 2**
2	**± 4**	**2**	**± 4**
3	**± 6**	**3**	**± 8**
4	**± 8**	**4**	**± 15**
X	**Specified by Customer**	**X**	**Specified by Customer**

Table 1.4
Recommended Classifications of System-Level ESD Test Results

Criterion	Recommended Classification
Class A	**Normal performance within limits specified by the manufacturer, requestor or purchaser.**
Class B	**Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention. (Automatic Recovery)**
Class C	**Temporary loss of function or degradation of performance, the correction of which requires operator intervention. (Manual Recovery)**
Class D	**Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.**

To evaluate the performance of electrical/electronic equipments subjected to electromagnetic compatibility (EMC) regulation, performing the system-level ESD tests for the electrical/electronic equipments is necessary. The inset figure in Fig. 1.6 shows an EUT (keyboard) which was stressed by an ESD gun with a charged voltage of +1 kV zapping on the horizontal coupling plane (HCP). During the system-level ESD test, the power and ground lines of the microcontroller IC in the keyboard no longer maintain their normal voltage levels, but an underdamped sinusoidal voltage with the amplitude of several hundred volts occurred, as shown in Fig. 1.6 This ESD-generated transient is quite large and fast, which can randomly couple to the power, ground, or I/O pins of microelectronics system. Such a high-voltage-level fast transient causes the keyboard to be upset or frozen after the system-level ESD zapping. Such fast electrical transients can also cause transient-induced latchup events in CMOS ICs [26]-[28].

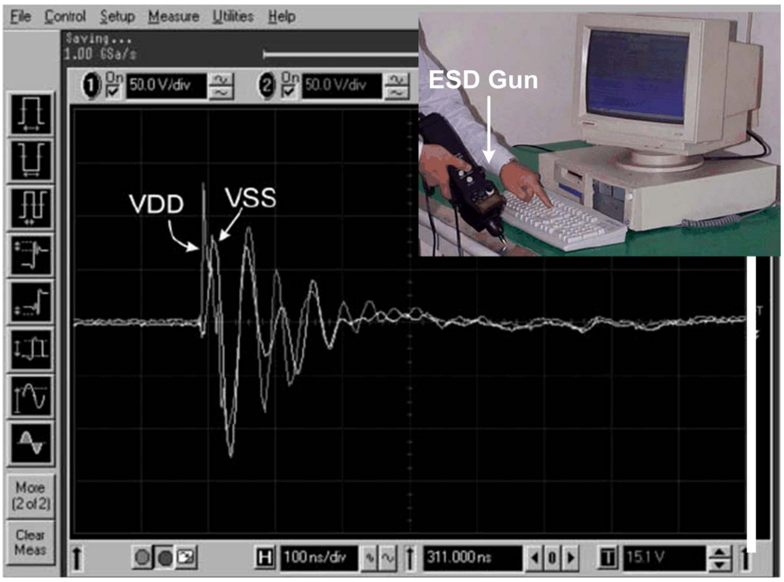


Fig. 1.6 Measured V_{DD} and V_{SS} waveforms of the microcontroller ICs inside the keyboard with ESD voltage of +1 kV zapping on the HCP under system-level ESD test [10].

This ESD-generated transient voltage is quite large (with the amplitude of several tens to hundreds volts) and fast (with the period of several tens nanoseconds) and randomly exists on power, ground, or I/O pins of the ICs inside the microelectronic system. Such a high-voltage-level ESD-induced fast transients often cause the CMOS ICs inside the EUT to be upset or frozen after the system-level ESD zapping. It has been reported that, for a capacitive fingerprint sensor circuit, the MOSFET devices can be melted from device surface into silicon substrate under system-level ESD test with air discharge mode. It has been also observed that, under system-level ESD tests, the underdamped sinusoidal voltage waveforms coupled on V_{DD} and V_{SS} pins of a super twisted nematic (STN) LCD driver circuit can cause abnormal display function of LCD panel. Such a high-energy ESD-induced fast transients can cause serious reliability events on CMOS ICs inside the microelectronic products. Therefore, the CMOS ICs inside the microelectronic products are very susceptible to system-level ESD stress, even though they have passed the component-level ESD specifications such as human-body-model (HBM) of ±2 kV, machine-model (MM) of ±200 V, and charged-device-model (CDM) of ±1 kV.

1.2.2. Electrical Fast Transient (EFT) Tests

The standard of IEC 61000-4-4 defines immunity requirements and test methods for electronic equipment to repetitive fast transients [29]. The EFT is a test with repetitive burst string consisting of a number of fast pulses, coupled into power supply, control, signal, and ground ports of microelectronic products. The characteristics of EFT are high amplitude, short rise time, and high repetition rate of the transients. The EFT test is intended to demonstrate the immunity of microelectronic products to transient disturbances such as those originating from switching transients (interruption of inductive loads, relay contact bounce, etc.).

According to the standard of IEC 61000-4-4, the simplified circuit diagram of EFT generator is shown in Fig. 1.7 with the impedance matching resistor R_m of 50 Ω and the dc blocking capacitor C_d of 10 nF. The charging capacitor C_c is used to store the charging energy and R_c is the charging resistor. The resistor R_s is used to shape the pulse duration. The parameters of EFT generator is summarized in Table 1.5.

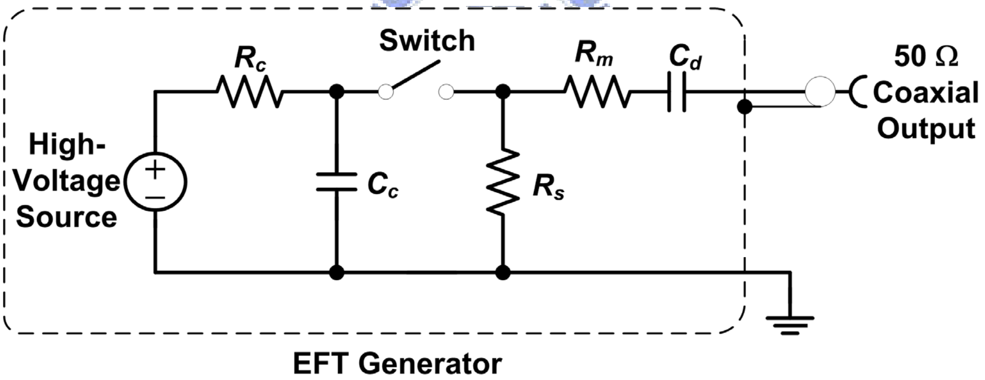


Fig. 1.7 The equivalent circuit of EFT generator.

Table 1.5
Characteristics of the EFT Generator

Parameter	**Definition**
R_c	**Charge Resistor**
C_c	**Energy Storage Capacitor**
R_s	**Duration Shaping Resistor**
R_m	**Impedance Matching Resistor**
C_d	**DC Blocking Capacitor**

The standard of IEC 61000-4-4 defines the test voltage waveforms of these fast transients with the repetition frequency of 5 kHz and 100 kHz. The use of 5 kHz repetition rate is the traditional EFT test and 100 kHz is closer to reality. For EFT pulse with the repetition frequency of 5 kHz, there are totally 75 pulses in each burst string and the burst duration time is 15ms. For EFT pulse with the repetition frequency of 100 kHz, there are 75 pulses in each burst string and the burst duration time is only 0.75 ms. For both repetition rates, the burst string repeats every 300 ms. The characteristics of EFT burst are summarized in Table 1.6.

For EFT pulses with the repetition frequency of 5 kHz, the measured +200-V and -200-V voltage waveforms on the 1-kΩ load are shown in Figs. 1.8(a) and 1.8(b), respectively. Because the output loading (1 kΩ) is larger than the impedance matching resistor R_m (50 Ω), the measured output pulse peak is close to the input EFT voltage pulse. As shown in Figs. 1.8(a) and 1.8(b), the measured output pulse peaks on the 1-kΩ load are approximately +200 V and -200 V, respectively. For EFT repetition frequency of 5 kHz, the time interval between each pulse is 0.2ms. Under EFT tests, the application time should not be less than 1 minute and both polarities have to be tested. With the 1 kΩ load, the voltage waveforms of a single pulse with EFT voltage of +200 V and -200 V are shown in Figs. 1.9(a) and 1.9(b), respectively. In Figs. 1.9(a) and 1.9(b), the waveforms of a single pulse have a rise time of ~5ns and the pulse duration (time interval at half of peak EFT voltage) of ~50 ns. The characteristics of a single EFT pulse are summarized in Table 1.7.

Table 1.6

Characteristics of the Fast Transient/Burst

Repetition Rate (kHz)	Repetition Period (ms)	Pulse Number	Burst Duration (ms)	Burst Period (ms)
5	0.2	75	15	300
100	0.01	75	0.75	300

Table 1.7

Characteristics of a Single EFT Voltage Pulse

Parameter	Value
Frequency	5 or 100 kHz
Rise Time	5ns ± 30%
Duration	50ns ± 30%

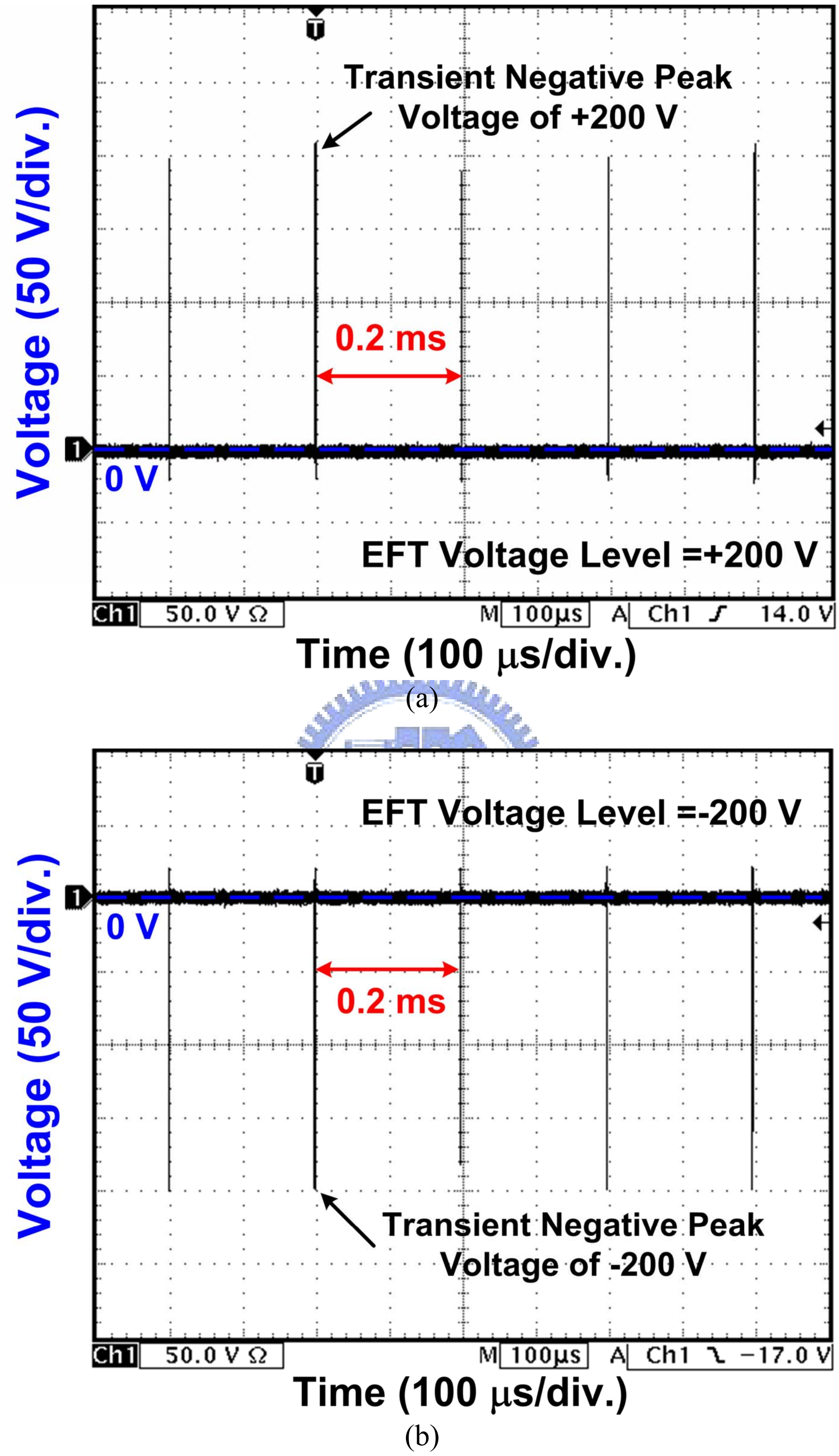
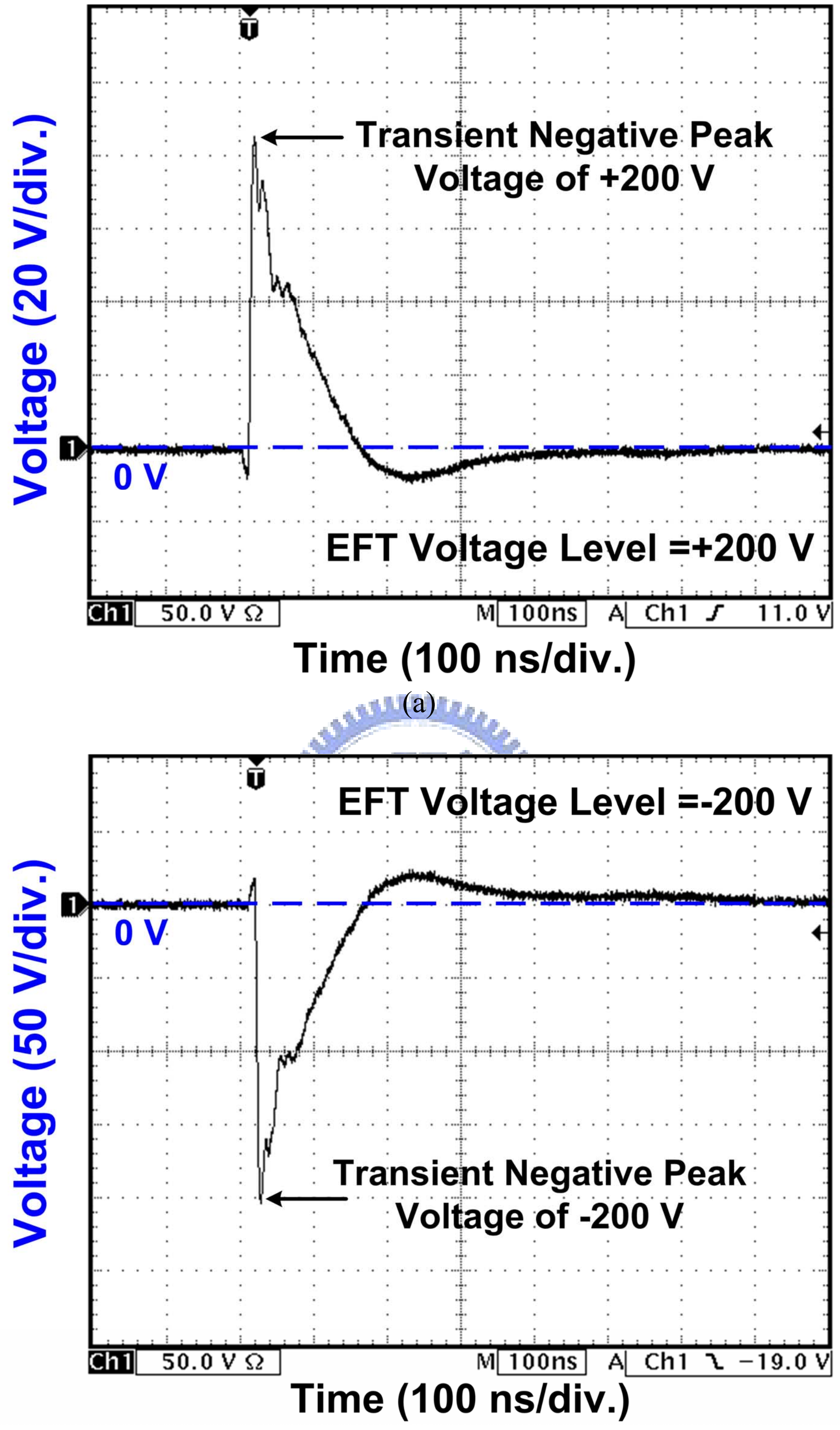


Fig. 1.8 Measured voltage waveforms under EFT tests with EFT voltage of (a) +200 V, and (b) -200 V, on 1-kΩ load with a repetition rate of 5 kHz.



(a)

(b)

Fig. 1.9 Measured voltage waveforms of a single pulse with EFT voltage of (a) +200 V, and (b) -200 V, on 1-kΩ load under EFT test.

The EFT levels for testing power supply ports and for testing I/O, data, and control ports of the equipment are listed in Table 1.8. The voltage peak for testing I/O, data, and control ports is half of the voltage peak for testing power supply ports. The repetition rate is determined by specific products or product types. Level "X" is an open level, which is specified in the dedicated equipment specification by customers. The output voltage peaks of EFT test are listed in Table 1.9. With output load of 50 Ω, the measured output voltage is 0.5 times the value of open-circuit load due to impedance matching.

Table 1.8
Levels of EFT Test

Level	On Power and PE (Protective Earth) Ports		On I/O (Input/Output) Signal, Data, and Control Ports	
	Voltage Peak (kV)	Repetition Rate (kHz)	Voltage Peak (kV)	Repetition Rate (kHz)
1	0.5	5 or 100	0.25	5 or 100
2	1	5 or 100	0.5	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
X	Specified by Customer	Specified by Customer	Specified by Customer	Specified by Customer

Table 1.9
Output Voltage Peak (V_P) Values and Repetition Rates under EFT Test

Set Voltage (kV)	V_P (Open) (kV)	V_P (1000 Ω) (kV)	V_P (50 Ω) (kV)	Repetition Rate (kHz)
0.25	0.25	0.24	0.125	5 or 100
0.5	0.5	0.48	0.25	5 or 100
1	1	0.95	0.5	5 or 100
2	2	1.9	1	5 or 100
4	4	3.8	2	5 or 100

1.3. Solutions to Overcome Electrical Transient Disturbance

1.3.1. Traditional Board-Level Solution

In order to meet the system-level ESD specifications, two useful methods have been reported and investigated [30]-[34]. One effective method is to add some discrete noise-bypassing components or board-level noise filters into the CMOS IC products to decouple, bypass, or absorb the electrical transient voltage (energy) under system-level ESD test. The system-level ESD immunity of CMOS ICs under system-level ESD test can be significantly enhanced by choosing proper noise filter networks. As shown in Fig. 1.10, some discrete components (such as the magnetic core, ferrite bead (FB), and RC low-pass filters) are added into printed circuit board (PCB) of a keyboard product to restrain the electrical transients from the system-level ESD tests. The system-level ESD immunity of CMOS ICs under system-level ESD test can be significantly enhanced by choosing proper noise filter networks. The other method to improve the system-level ESD immunity of CMOS ICs is to regularly check the system abnormal conditions by using an external hardware timer, such as watch dog timer. The external hardware timer is often consisted of registers or flip flops to reset the operation system if the main program is locked or frozen due to some fault conditions. However, during system-level ESD tests, the logic states stored in the registers or flip flops may be destroyed or changed to cause malfunction or frozen state on the main operation program. The additional discrete noise-bypassing components also substantially increase the total cost of microelectronic products. Therefore, the chip-level solutions to meet high transient disturbance immunity specification for microelectronic products without additional discrete noise-decoupling components are highly desired by IC industry [35]-[39].

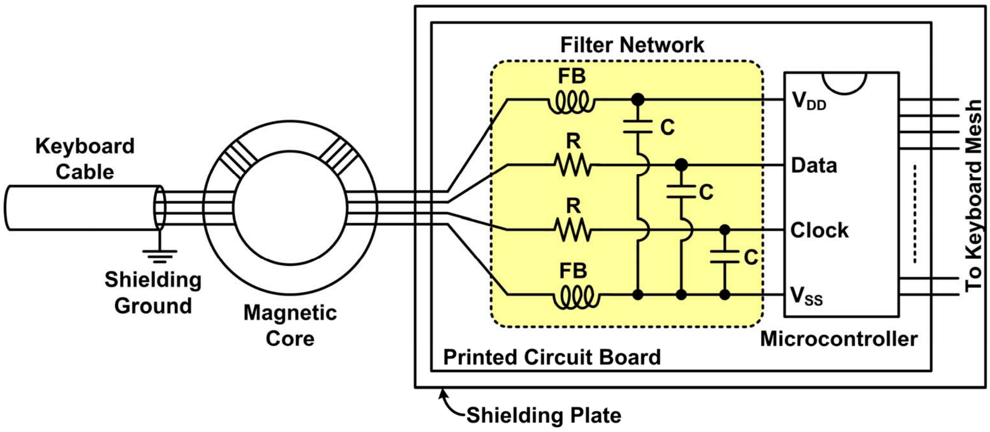


Fig. 1.10 A traditional solution to overcome the electrical transient disturbance in a keyboard product by adding extra discrete components to absorb or bypass the electrical transients.

1.3.2. Hardware/Firmware System Co-Design Solution

It had been reported that the hardware/firmware co-design can effectively improve the system-level ESD susceptibility of the CMOS IC products [10]. In this work, a new on-chip transient detection circuit is proposed to detect the fast electrical transient under system-level ESD or EFT tests. By using a longer time delay in the RC circuit under system-level ESD tests, the proposed new on-chip transient detection circuit can memorize the occurrence of electrical transient disturbance events. As shown in the hardware/firmware system co-design in the Fig. 1.11, the detection results (V_{OUT}) from the proposed on-chip transient detection circuit can be temporarily stored as a system recovery index for firmware check.

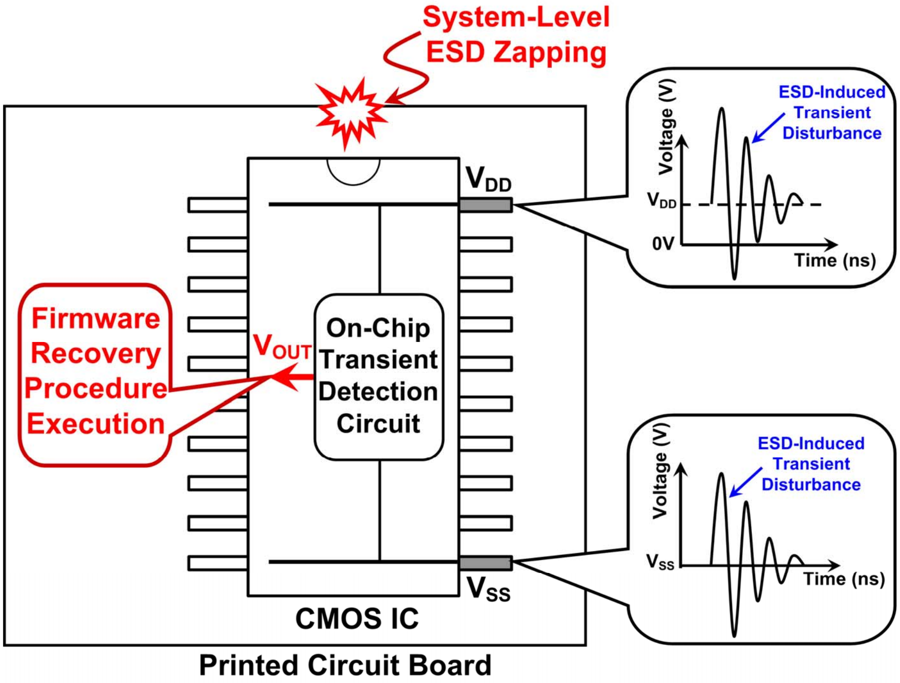


Fig. 1.11. Hardware/firmware co-design for system recovery by using the output of the on-chip transient detection circuit.

For example, the output (V_{OUT}) states in the proposed on-chip transient detection circuit and the firmware index are initially cleared to logic "0." When the fast electrical transient happens, the proposed on-chip transient detection circuit can detect the fast electrical transients to transit the output state (V_{OUT}) from logic "0" to logic "1." At this time, the system recovery index is stored at logic "1" and the firmware executes the recovery procedure to recover all system functions to a stable state as soon as possible. After the recovery procedures, the output state of the proposed on-chip transient detection circuit and the firmware index are re-set to logic "0" again for detecting the next system-level ESD events. A novel on-chip transient-to-digital converter composed of transient detection circuits was proposed to detect the fast electrical transients and convert them to digital thermometer codes under system-level ESD or EFT tests. The proposed on-chip transient-to-digital converter can be also coordinated with firmware to provide a hardware/firmware co-design solution for protection design against electrical transient disturbance.

1.4. Organization of This Dissertation

This dissertation is composed of seven chapters. This dissertation (chapter 2 ~ chapter 6) focuses on the system-level ESD issues and the design of on-chip transient detection circuits and transient-to-digital converter. Several major topics including: (1) investigation and design of on-chip power-rail ESD clamp circuits without suffering latchup-like failure during system-level ESD and EFT tests (chapter 2), (2) transient-induced latchup in CMOS integrated circuits under EFT tests (chapter 3), (3) on-chip transient detection circuit design (scheme I) (chapter 4), (4) on-chip transient detection circuit design (scheme I) (chapter 5) , and (5) transient-to-digital converters (chapter 6). Chapter 7 gives the conclusions and future works of this dissertation. The outlines of each chapter are summarized below.

In chapter 2, on-chip power-rail electrostatic discharge (ESD) protection circuit designed with active ESD detection function is the key role to significantly improve ESD robustness of CMOS ICs. Four power-rail ESD clamp circuits with different ESD-transient detection circuits were fabricated in a 0.18-μm CMOS process and tested to compare their system-level ESD and EFT susceptibility, which are named as power-rail ESD clamp circuits with typical RC-based detection, PMOS feedback, NMOS+PMOS feedback, and cascaded PMOS feedback in this work. During the system-level ESD and EFT tests, where the ICs in a system have been powered up, the feedback loop used in the power-rail ESD clamp circuits provides the lock function to keep the ESD-clamping NMOS in a “latch-on” state. The latch-on ESD-clamping NMOS, which is often drawn with a larger device dimension to sustain high ESD and EFT testing levels, conducts a huge current between the power lines to perform a latchup-like failure after the system-level ESD and EFT tests. A modified power-rail ESD clamp circuit is proposed to solve this problem. The proposed power-rail ESD clamp circuit can provide high enough chip-level ESD robustness, and without suffering the latchup-like failure during the system-level ESD and EFT tests.

In chapter 3, the occurrence of transient-induced latchup (TLU) in CMOS ICs under the EFT tests is studied. The test chip with the parasitic silicon-controlled rectifier (SCR) structure fabricated by a 0.18-μm CMOS process was used in the EFT tests. For physical mechanism characterization, the specific “sweep-back” current caused by the minority carriers stored within the parasitic PNPN structure of CMOS ICs is the major cause of TLU under EFT tests. Different types of board-level noise filter networks are evaluated to find their effectiveness for improving the immunity of CMOS ICs against TLU under EFT tests. By choosing proper components in each noise filter network, the TLU immunity of CMOS ICs against EFT tests can be greatly improved.

In chapter 4, a novel on-chip RC-based transient detection circuits for system-level ESD)and EFT protection are proposed in this work. The circuit performance to detect positive and negative electrical transients under system-level ESD and EFT testing conditions has been investigated by the HSPICE simulation and verified in silicon chip. The experimental results have confirmed that the proposed on-chip RC-based transient detection circuit I can successfully memorize the occurrence of the system-level ESD and EFT events. The detection output of proposed on-chip RC-based transient detection circuit I can be used as the firmware index to execute system recovery procedure to provide a hardware/firmware co-design to improve the immunity of CMOS IC products against electrical transient disturbance.

In chapter 5, a new on-chip transient detection circuit II for electrical fast disturbance protection design is proposed in this work. The circuit performance to detect different positive and negative ESD-induced or EFT-induced transient disturbance has been investigated by the HSPICE simulation and verified in silicon chip. The EFT generator combined with attenuation network and capacitive coupling clamp has been used as the evaluation method to verify the detection function of the proposed on-chip transient detection circuit II under EFT tests. The test chip in a 0.18-µm CMOS process with 1.8-V devices has confirmed that the proposed on-chip transient detection circuit II can successfully detect and memorize the occurrence of the transient disturbance under system-level ESD or EFT tests.

In chapter 6, a novel on-chip transient-to-digital converter composed of four RC-based transient detection circuits and four different RC filter networks has been successfully designed and verified in a 0.18-µm CMOS process with 3.3-V devices. The output digital thermometer codes of the proposed on-chip transient-to-digital converter correspond to different electrical transient voltages under system-level ESD and EFT tests. These output digital codes can be used as the firmware index to execute different auto-recovery procedures in microelectronic systems. Thus, the proposed on-chip transient-to-digital converter can be further combined with firmware design to provide an effective solution to solve the system-level ESD and EFT protection issue in microelectronic systems equipped with CMOS ICs.

Chapter 7 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in this chapter.

Chapter 2

Investigation and Design of On-Chip Power-Rail ESD Clamp Circuits Without Suffering Latchup-Like Failure During System-Level ESD and EFT Tests

On-chip power-rail electrostatic discharge (ESD) protection circuit designed with active ESD detection function is the key role to significantly improve ESD robustness of CMOS integrated circuits (ICs). Four power-rail ESD clamp circuits with different ESD-transient detection circuits were fabricated in a 0.18-μm CMOS process and tested to compare their system-level ESD susceptibility, which are named as power-rail ESD clamp circuits with typical RC-based detection, PMOS feedback, NMOS+PMOS feedback, and cascaded PMOS feedback in this work. During the system-level ESD and EFT tests, where the ICs in a system have been powered up, the feedback loop used in the power-rail ESD clamp circuits provides the lock function to keep the ESD-clamping NMOS in a "latch-on" state. The latch-on ESD-clamping NMOS, which is often drawn with a larger device dimension to sustain high ESD level, conducts a huge current between the power lines to perform a latchup-like failure after the system-level ESD test. A modified power-rail ESD clamp circuit is proposed to resolve this problem. The proposed power-rail ESD clamp circuit can provide high enough chip-level ESD robustness, and without suffering the latchup-like failure during the system-level ESD and EFT tests.

2.1. Background

ESD protection has been one of the most important reliability issues in CMOS IC products. ESD failures caused by thermal breakdown due to high current transient, or dielectric breakdown in gate oxide due to high voltage overstress, often result in immediate malfunction of IC chips. In order to obtain high ESD robustness, CMOS ICs must be designed with on-chip ESD protection circuits at the input/output (I/O) pins and across the power lines. With the reduced breakdown voltage of the thinner gate oxide in advanced deep-submicron CMOS processes, turn-on-efficient ESD protection circuit is required to clamp the overstress across the gate oxide of internal circuits. Since the stored electrostatic charges could be either positive or negative, there are four different ESD-testing modes at input-output (I/O) pins with respect to the grounded V_{DD} or V_{SS} pins [2]. Besides, for a comprehensive ESD verification, two additional pin combinations under ESD test, which are the pin-to-pin ESD stress and the V_{DD}-to-V_{SS} ESD stress, are performed to verify the ESD reliability of IC chip [8]. These two additional ESD testing modes often lead to some unexpected ESD current through I/O pins and power lines into the internal circuits and result in ESD damage in the internal circuits. Therefore, effective power-rail ESD clamp circuit between V_{DD} and V_{SS} power lines is necessary for whole-chip ESD protection. The typical on-chip ESD protection design with active power-rail ESD clamp circuit in CMOS ICs is shown in Fig. 2.1. When the input (or output) pin is zapped under the positive-to-V_{SS} (PS-mode) or negative-to-V_{DD} (ND-mode) ESD stresses, the power-rail ESD clamp circuit can provide a low impedance path between V_{DD} and V_{SS} power lines to efficiently discharge ESD current. To avoid unexpected ESD damages in the internal circuits under pin-to-pin and V_{DD}-to-V_{SS} ESD stresses, the power-rail ESD clamp circuit must be designed with high turn-on efficiency and fast turn-on speed.

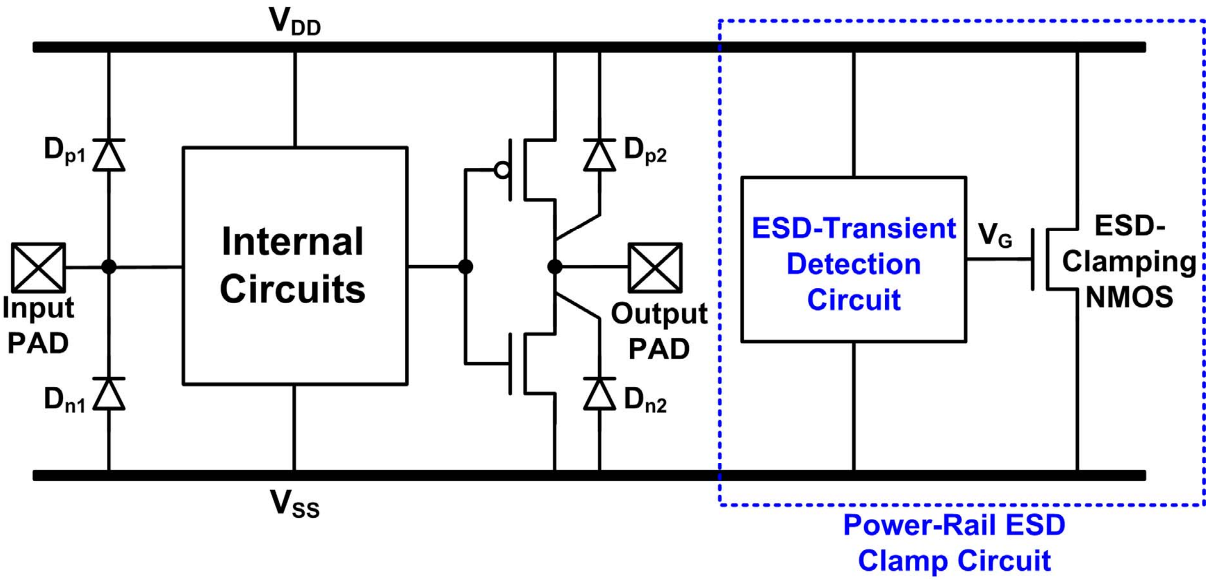


Fig. 2.1 Typical on-chip ESD protection design with active power-rail ESD clamp circuit.

In the active power-rail ESD clamp circuit, the ESD-transient detection circuit is designed to detect ESD event and sends a control voltage to the gate of ESD-clamping NMOS. Since the ESD-clamping NMOS is turned on by a positive gate voltage rather than by snapback breakdown, the ESD-clamping NMOS can be turned on quickly to discharge

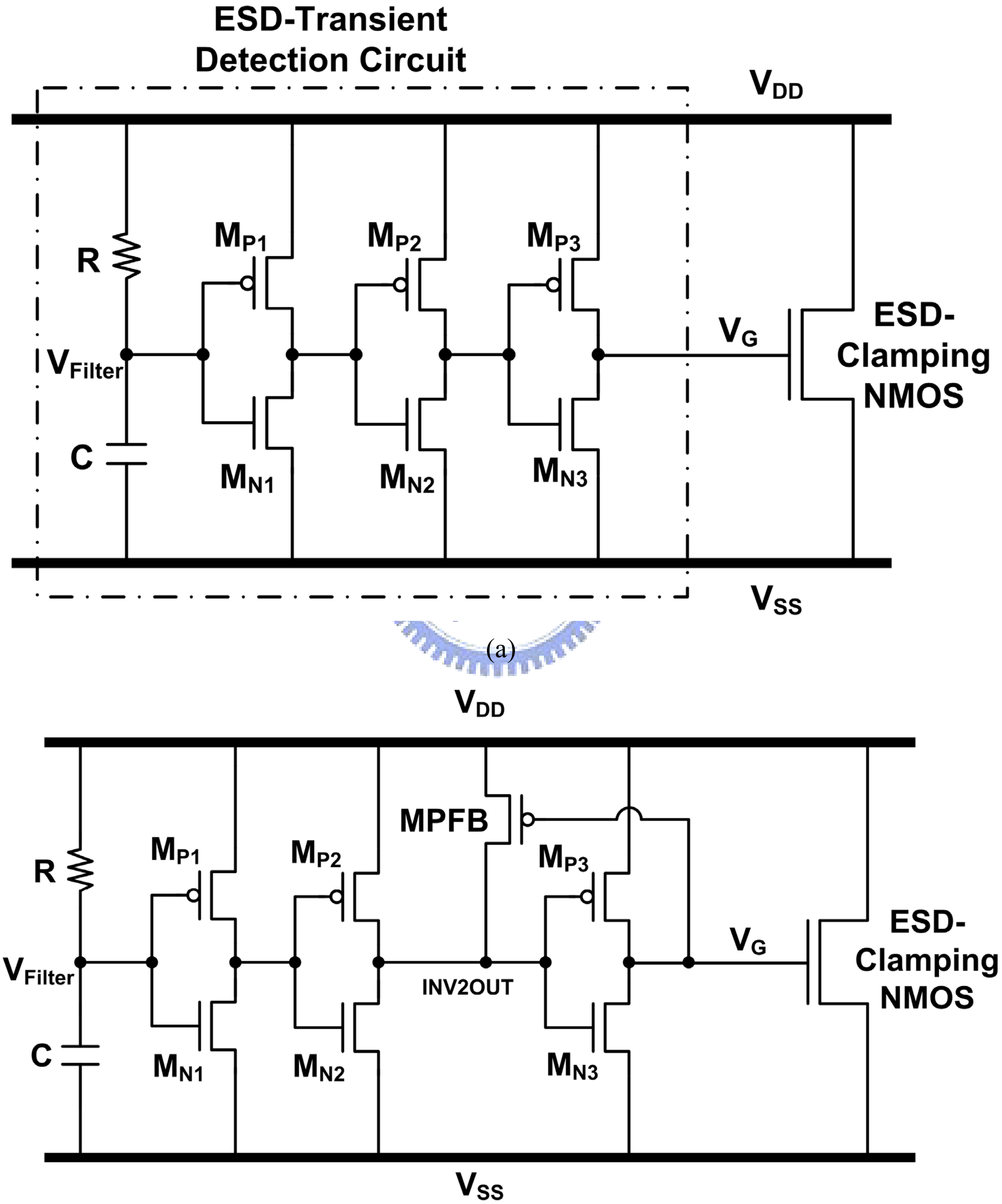
ESD current before the internal circuits are damaged. Thus, the effective power-rail ESD clamp circuit is necessary for protecting the internal circuits against ESD damage. Some modified designs on the ESD-transient detection circuits had been reported to enhance the performance of power-rail ESD clamp circuits [40]-[45].

Recently, system-level ESD and EFT reliability has attracted more attentions than before in microelectronics products. This tendency results from not only the integration of more functional circuits in a single chip, but also the strict requirement of reliability regulation, such as the system-level ESD test for electromagnetic compatibility (EMC). During the system-level ESD test, the microelectronics products must sustain the ESD stress of ±8 kV (±15 kV) under the contact-discharge (air-discharge) test mode to meet the immunity requirement of “level 4.” During such a high-energy ESD event, some of ESD-induced overshooting/undershooting pulses may be coupled into the microelectronics products to cause damage or malfunction on the CMOS ICs inside the device under test (DUT). Some CMOS ICs are very susceptible to electrical transient disturbance, even though they have passed the component-level ESD specifications of human-body-model (HBM) of ±2 kV, machine-model (MM) of ±200 V, and charged-device- model (CDM) of ±1 kV.

In this work, the malfunction or wrong triggering behavior among different on-chip power-rail ESD clamp circuits under system-level ESD and EFT tests are investigated [46]. Some ESD-transient detection circuits designed with feedback loop in the power-rail ESD clamp circuits continually keep the ESD-clamping NMOS in the latch-on state after the system-level ESD test. The latch-on ESD-clamping NMOS between V_{DD} and V_{SS} power lines in the powered-up microelectronic system causes a serious latchup-like failure in CMOS ICs. The system-level ESD gun [47], the transient-induced latchup (TLU) measurement method [48], and EFT generator [49] are used to evaluate the susceptibility among four different power-rail ESD clamp circuits to system-level ESD and EFT tests. Furthermore, a modified power-rail ESD clamp circuit is proposed to avoid such latchup-like failure. The proposed power-rail ESD clamp circuit can provide high enough chip-level ESD robustness without suffering the latchup-like failure during the system-level ESD and EFT tests.

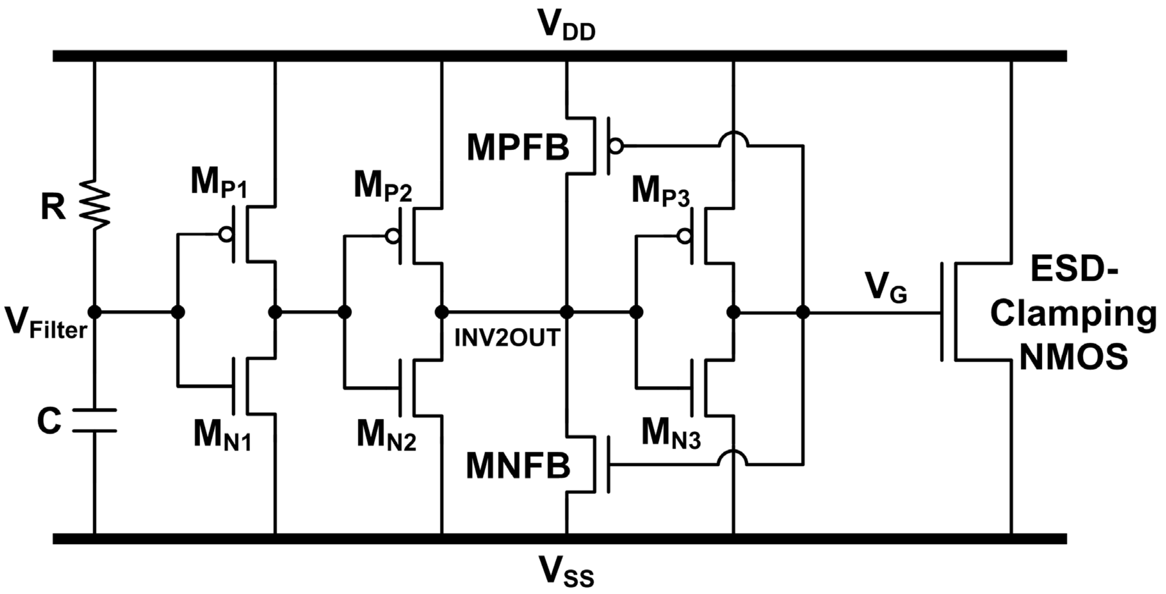
2.2. Power-Rail ESD Clamp Circuits

To provide effective on-chip ESD protection, four different power-rail ESD clamp circuits had been reported [40]-[45], which are re-drawn in Figs. 2.2(a)-2.2(d) with the names of (1) power-rail ESD clamp circuit with typical RC-based detection, (2) power-rail ESD clamp circuit with PMOS feedback, (3) power-rail ESD clamp circuit with NMOS+PMOS feedback, and (4) power-rail ESD clamp circuit with cascaded PMOS feedback, in this work. Those power-rail ESD clamp circuits have been designed and fabricated in a 0.18-μm CMOS process to investigate their susceptibility to system-level ESD test.

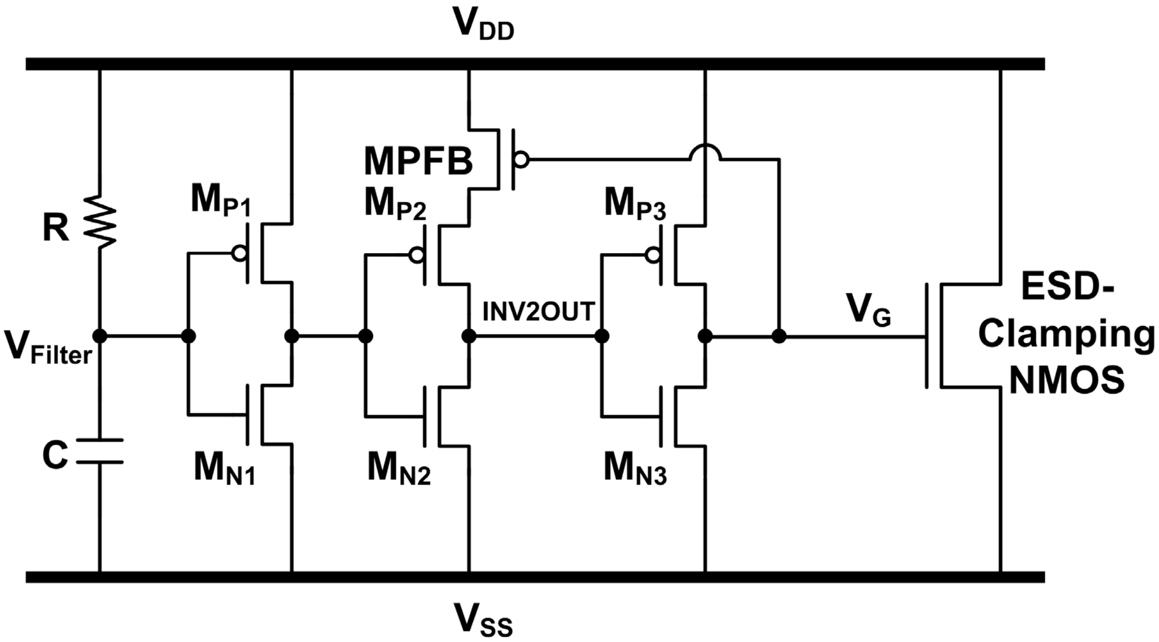


(a)

(b)



(c)



(d)

Fig. 2.2 Four different power-rail ESD clamp circuits designed with (a) typical RC-based detection, (b) PMOS feedback, (c) NMOS+PMOS feedback, and (d) cascaded PMOS feedback.

2.2.1. Power-Rail ESD Clamp Circuit With Typical RC-Based Detection

The typical RC-based power-rail ESD clamp circuit is illustrated in Fig. 2.2(a) with a three-stage buffer between the RC circuit and the ESD-clamping NMOS [40]. The ESD-clamping NMOS is used to provide a low impedance path between V_{DD} and V_{SS} to discharge ESD current. The ESD-transient detection circuit detects ESD pulses with the rise time of ~10ns and sends a control voltage to the gate of ESD-clamping NMOS. Under the ESD stress condition, the voltage level at the V_{Filter} node is increased much slower than that on V_{DD} power line, because the RC circuit has a time constant in the order of microsecond (µs). Due to the delay of the voltage increase at the V_{Filter} node, the three-stage buffer is powered by the ESD energy and conduct a voltage to the V_G node to turn on the ESD-clamping NMOS. The turned-on ESD-clamping NMOS, which provides a low-impedance path between V_{DD} and V_{SS} power lines, clamps the overstress ESD voltage to effectively protect the internal circuits against ESD damage.

The turn-on time of ESD-clamping NMOS during ESD transition can be adjusted by designing the RC time constant in the ESD transient detection circuit. The turn-on time is usually designed around ~100 ns to meet the half-energy discharging time of HBM ESD current. Under normal circuit operating conditions, the power-rail ESD clamp circuit must be kept off to avoid power loss from V_{DD} to V_{SS}. The rise time of V_{DD} powered up is around ~1ms or even longer in the most of microelectronics systems. To meet such a timing requirement, the RC time constant in the RC-based ESD-transient detection circuit is typically designed with 0.1~1 µs to achieve the design constrains.

2.2.2. Power-Rail ESD Clamp Circuit With PMOS Feedback

Another design consideration for power-rail ESD clamp circuit is the circuit immunity to false triggering during power-up condition. The power-rail ESD clamp circuit should be turned on when the ESD voltage appears across V_{DD} and V_{SS} power lines, but kept off when the IC is under normal power-on condition. To meet these requirements, the RC time constant was usually designed with 0.1~1 µs to achieve the design constraints. However, the large RC time constant used in the power-rail ESD clamp circuit may cause false triggering during a fast power-up condition with a rise time of less than 10µs. The modified power-rail ESD clamp circuit incorporated with PMOS feedback, as shown in Fig. 2.2(b), was used to mitigate such a mis-trigger problem [41]. The transistor MPFB can help to keep the gate voltage of ESD-clamping NMOS below its threshold voltage and further reduce the current drawn during the power-up condition.

2.2.3. Power-Rail ESD Clamp Circuit With NMOS+PMOS Feedback

In the advanced CMOS technology with thinner gate oxide, the power-rail ESD clamp circuit with a large MOS capacitance in the RC timer was reported to cause significant stand-by power consumption due to gate oxide leakage current [42]. Thus, the modified power-rail ESD clamp circuits with small MOS capacitance are desired to combat the gate leakage. It was reported that the power-rail ESD clamp circuit incorporated with a regenerative feedback network can be used to significantly reduce the RC time constant, as illustrated in Fig. 2.2(c) [43].

The transistors MPFB and MNFB provide a feedback loop, which can latch the ESD-clamping NMOS in the conductive state during ESD-stress condition. When a fast positive going ESD transient across the power rails, the MNFB can further pull the potential of INV2OUT node towards ground to latch the ESD-clamping NMOS in the conductive state until the voltage on V_{DD} drops below the threshold voltage of ESD-clamping NMOS. With this feedback loop in the power-rail ESD clamp circuit, the dynamic currents of M_{P2}, M_{N2}, MPFB, and MNFB determine the critical voltage to trigger on the ESD-clamping NMOS. After the timing out of the RC time constant in ESD transient detection circuit, the transistor MP2 begins to conduct and increase the potential of INVOUT2 node. The settling potential of INVOUT2 node is set by the current balance between M_{P2} and MNFB. Thus, the device ratios of M_{P2} and MNFB in the power-rail ESD clamp circuit with NMOS+PMOS feedback should be appropriately selected.

2.2.4. Power-Rail ESD Clamp Circuit With Cascaded PMOS Feedback

Another RC-based power-rail ESD clamp circuit with cascaded PMOS feedback has been proposed to reduce the RC time constant and to solve false trigger issue during fast power-up constrains, as shown in Fig. 2.2(d) [44]. The PMOS transistor MPFB is connected to form the cascaded feedback loop, which is a dynamic feedback design.

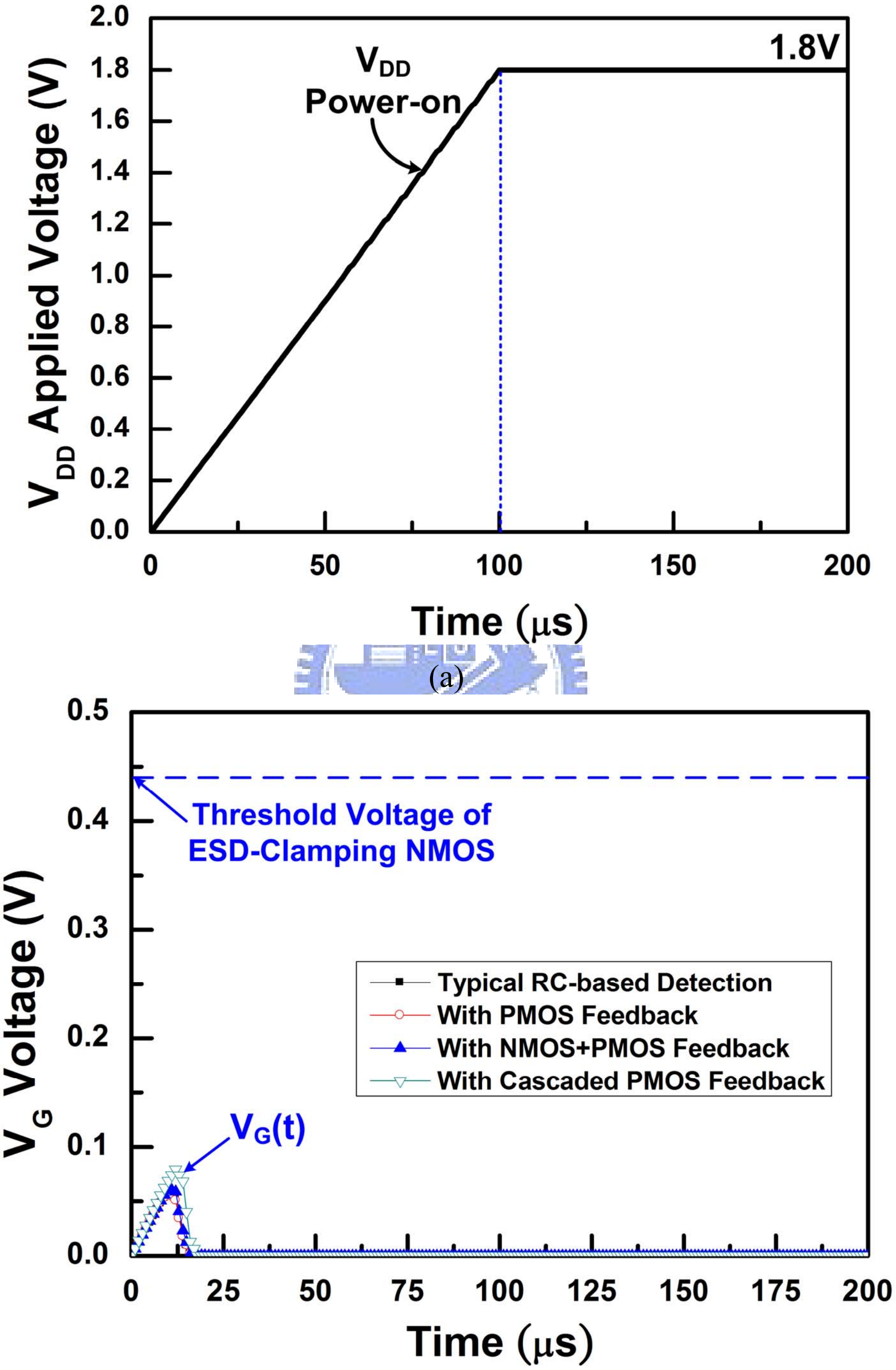
During the ESD-stress condition, the transistor MPFB was turned off and the voltage on the INV2OUT node can be remained in a low state. Thus, the turn-on time of the ESD-clamping NMOS can be longer than that of the typical RC-based power-rail ESD clamp circuit. If the ESD-clamping NMOS is mis-triggered during fast power-up condition or by an overvoltage under normal operating conditions, the voltage on the INV2OUT node can be charged up toward V_{DD} by the subthreshold current of MPFB. Therefore, the ESD-clamping NMOS will not stay at latch-on state and turn itself off after the fast power-up condition. Compared with the feedback designs with direct PMOS feedback in Fig. 2.2(b), the power-rail ESD clamp circuit with cascaded PMOS feedback has the advantage of capacitance reduction.

2.2.5. Realization in Silicon Chip

For the four power-rail ESD clamp circuits in this work, the ESD-clamping NMOS is designed to turn on under the ESD-stress condition to efficiently discharge the ESD current between V_{DD} and V_{SS} power lines. The turn-on time of the ESD-clamping NMOS is designed to meet the half-energy discharging time of HBM ESD event. In the normal operating condition and V_{DD} power-up condition, the ESD-clamping NMOS is designed to keep off to avoid power loss or false triggering. The four power-rail ESD clamp circuits in this work are designed with such design concepts to evaluate their susceptibility to system-level ESD tests.

To verify such a design, some simulations are provided in the following text. In Fig. 2.3(a), a V_{DD} power-on voltage waveform with a rise time of 0.1ms and a voltage height of 1.8 V is applied to the V_{DD} line of the power-rail ESD clamp circuits. During such a V_{DD} power-on condition, among the four different power-rail ESD clamp circuits, the voltage waveforms on the node V_G are shown in Fig. 2.3(b), where the V_G peak voltage during the power-on transition are all below the threshold voltage (~0.44 V) of the ESD-clamping NMOS. With a very small V_G voltage in Fig. 2.3(b), the ESD-clamping NMOS in the four different power-rail ESD clamp circuits was expected to be always kept off when the IC is in normal operating conditions.

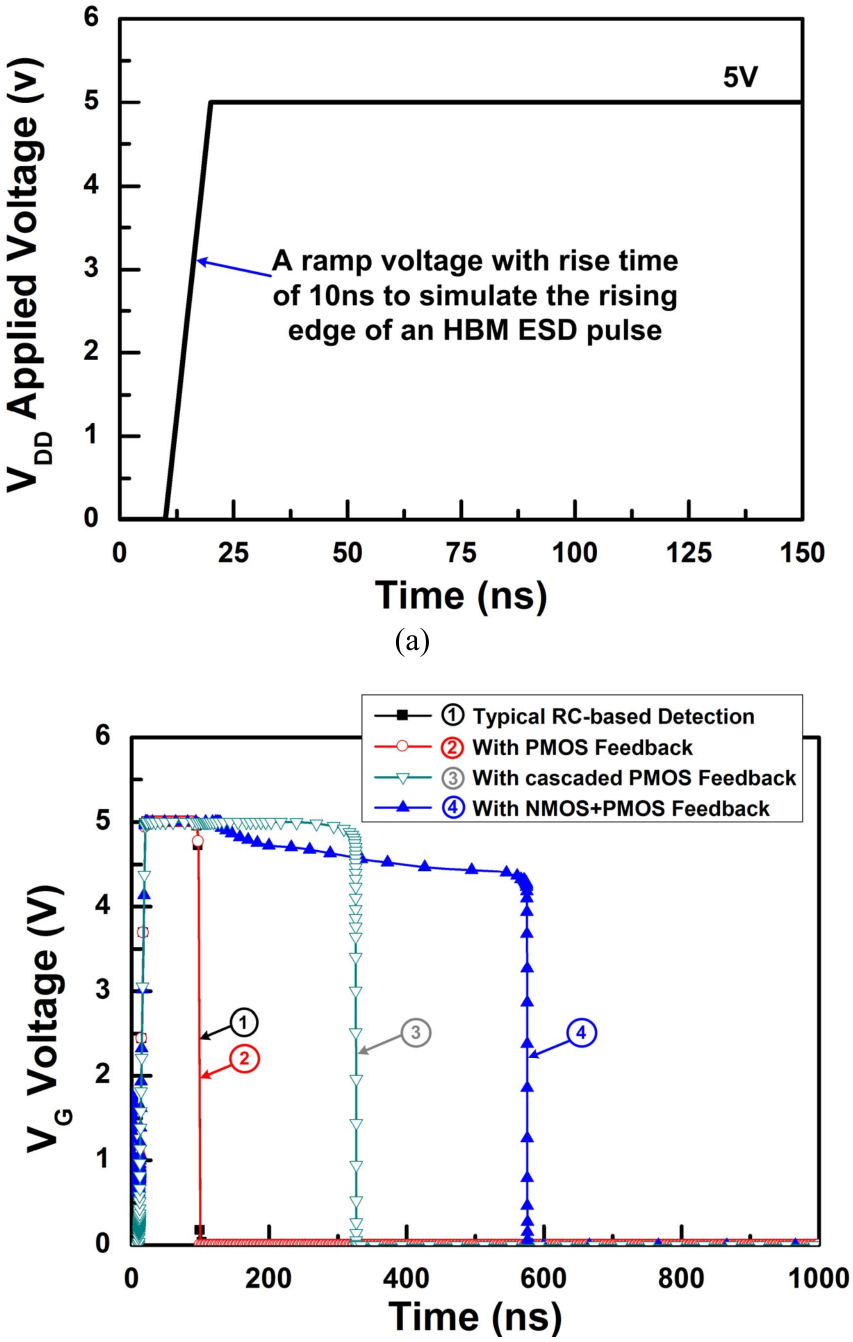
In Fig. 2.4(a), a fast ramp voltage with a rise time of 10ns is used to simulate the rising edge of HBM ESD pulse. The pulse height of the fast ramp voltage set as 5 V is used to monitor the voltage on the node V_G before the drain breakdown of ESD-clamping NMOS. As shown in Fig. 2.4(b), among the four different power-rail ESD clamp circuits, the voltage waveforms on the node V_G are simultaneously increased when the fast ramp voltage is applied to V_{DD}, whereas the V_{SS} is grounded. The four power-rail ESD clamp circuits are designed to provide a low impedance path between V_{DD} and V_{SS} power lines to efficiently discharge ESD current under ESD stress conditions. Combing with feedback circuit structure in the ESD-transient detection circuits, the turn-on time of the ESD-clamping NMOS can be increased by static or dynamic latches. For the power-rail ESD clamp circuits with NMOS+PMOS feedback and cascaded PMOS feedback, the turn-on time of the ESD-clamping NMOS can be longer than that of power-rail ESD clamp circuits with typical RC-based detection and PMOS feedback. The turn-on time of power-rail ESD clamp circuits with NMOS+PMOS feedback or cascaded PMOS feedback can be designed around 100ns, if the RC time constant in the corresponding ESD-transient detection circuit is further reduced. To simply the comparison for transient-induced latchup-like failure in this work, the RC values in the ESD-transient detection circuits among four power-rail ESD clamp circuits are set the same of R=50 kΩ and C=2 pF in silicon fabrication.



(a)

(b)

Fig. 2.3 HSPICE simulated voltage waveforms among the four different power-rail ESD clamp circuits under the V_{DD} power-on condition. (a) A slow ramp voltage waveform with rise time of 0.1 ms is used to simulate the rising edge of the V_{DD} power-on voltage. (b) The simulated voltage waveforms on the node V_G when the power-on voltage is applied to V_{DD}.



(a)

(b)

Fig. 2.4 HSPICE simulated voltage waveforms among the four different power-rail ESD clamp circuits under HBM ESD stress condition. (a) A fast ramp voltage waveform with rise time of 10 ns is used to simulate the rising edge of an HBM ESD pulse. (b) The simulated voltage waveforms on the node V_G when the fast ramp voltage is applied to V_{DD}.

2.3. Experimental Results and Discussion

Four different power-rail ESD clamp circuits, which are re-drawn in Figs. 2.2(a)-2.2(d) with the names of (1) power-rail ESD clamp circuit with typical RC-based detection, (2) power-rail ESD clamp circuit with PMOS feedback, (3) power-rail ESD clamp circuit with NMOS+PMOS feedback, and (4) power-rail ESD clamp circuit with cascaded PMOS feedback, are used as the test structures in this work. Those power-rail ESD clamp circuits have been designed and fabricated in a 0.18-μm CMOS process to investigate their susceptibility to system-level ESD and EFT tests. The system-level ESD gun [47], the transient-induced latchup (TLU) measurement method [48], and EFT generator [49] are used to evaluate the susceptibility among four different power-rail ESD clamp circuits to system-level ESD and EFT tests. The latchup-like failure caused by latch-on ESD-clamping NMOS between V_{DD} and V_{SS} power lines can be observed in some power-rail ESD clamp circuits due to increased I_{DD} current and pulled down V_{DD} voltage level.

2.3.1. Transient-Induced Latchup (TLU) Test

Transient-induced latchup (TLU) test has been used to investigate the susceptibility of DUT to the noise transient or glitch on the power lines under normal circuit operating condition. The component-level TLU measurement setup with bipolar trigger voltage can accurately simulate the ESD-induced noises on the power lines of CMOS ICs under system-level ESD test. The measurement setup for TLU test is shown in Fig. 2.5. The charging voltage V_{Charge} has two different polarities, which are positive ($V_{Charge}>0$) or negative ($V_{Charge}<0$). The positive (negative) V_{Charge} can generate the positive-going (negative-going) bipolar trigger noises on the power pins of DUT.

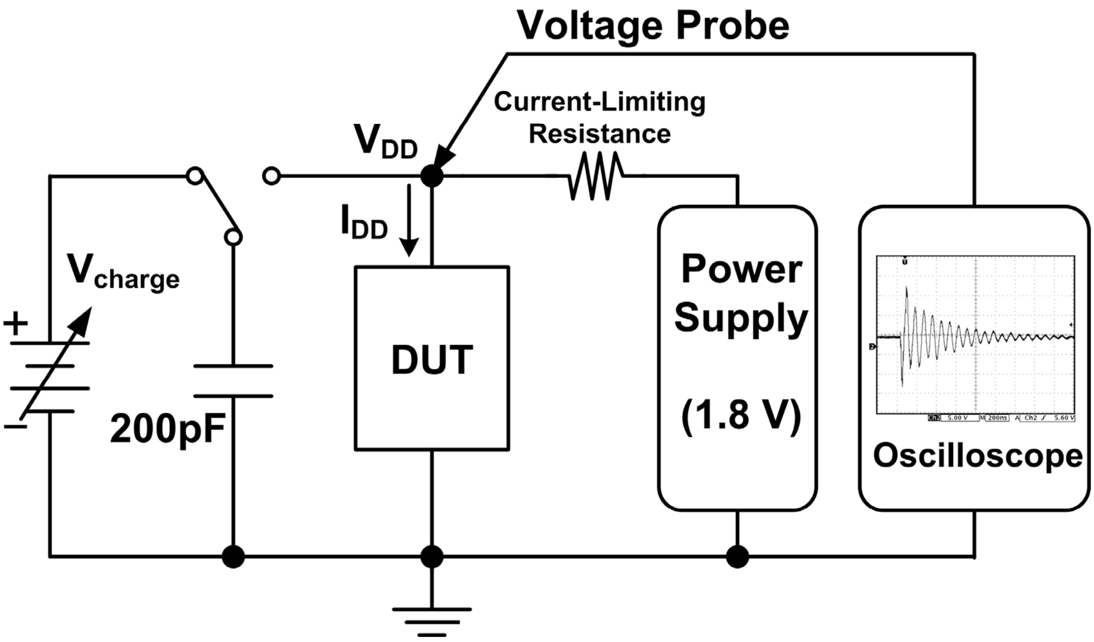
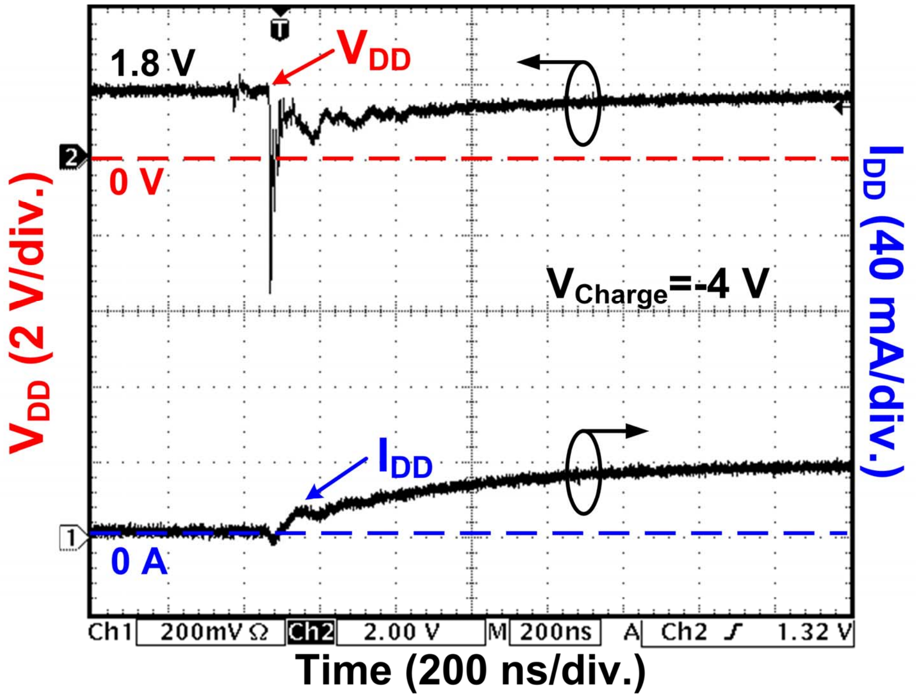


Fig. 2.5 Measurement setup for transient-induced latchup (TLU).

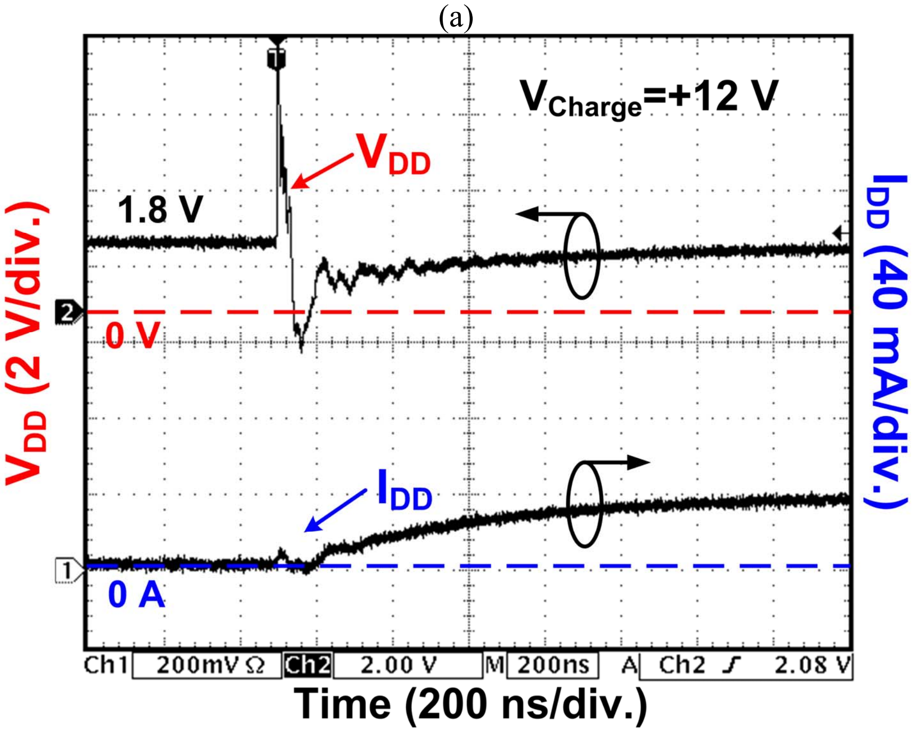
For the system-level ESD test, it can only judge whether the EUT passes the required criterion through its abnormal function (e.g. EUT shuts down). Nevertheless, it is hard to directly evaluate the TLU immunity of single IC inside the EUT. To solve this problem, a component-level TLU measurement setup with the following two advantages is used. First, it can easily evaluate the TLU immunity of single IC by the related measured voltage/current waveforms through oscilloscope. Second, with the ability of generating an underdamped sinusoidal voltage, it can accurately simulate how an IC inside the EUT will be disturbed by the ESD-generated noise under the system-level ESD test. Moreover, a small current-limiting resistance (5Ω) is recommended to protect the DUT from electrical-over-stress (EOS) damage during a high-current (low-impedance) latchup state.

A 200-pF capacitor used in the machine model (MM) ESD test is employed as the charging capacitor. The power-rail ESD clamp circuits shown in Figs. 2.2(a)-2.2(d) are placed as DUT. The supply voltage of 1.8V is used as V_{DD} and the noise trigger source is directly connected to DUT through the relay in the measurement setup. The I_{DD} current waveform is measured by a separated current probe. The current-limiting resistance is used to avoid electrical-over-stress (EOS) damage in DUT under a high-current latch-up state. The voltage and current waveforms on DUT (at V_{DD} node) after TLU test are monitored by the oscilloscope.

With the TLU measurement setup in Fig. 2.5, the V_{DD} and I_{DD} transient responses can be recorded by the oscilloscope, which can clearly indicate whether TLU occurs (I_{DD} significantly increases) or not. Figs. 2.6(a) and 2.6(b) show the measured V_{DD} and I_{DD} transient waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback under the stresses with V_{Charge} of -4 V and +12 V, respectively. After the TLU test with an initial V_{Charge} of -4 V, the latchup-like failure occurs in this power-rail ESD clamp circuit, because I_{DD} significantly increases and V_{DD} is pulled down, as shown in Fig. 2.6(a). After the TLU test with an initial V_{Charge} of +12 V, latchup-like failure occurs in Fig. 2.6(b). All the PMOS and NMOS devices in the ESD-transient detection circuits are surrounded with double guard rings to guarantee no latchup issue in this part [50]. This implies that the feedback loop in the ESD-transient detection circuit is locked after TLU test and continually keeps the ESD-clamping NMOS in the latch-on state. From the observed voltage and current waveforms, large I_{DD} current is caused by the latch-on state of ESD-clamping NMOS after TLU test.



(a)

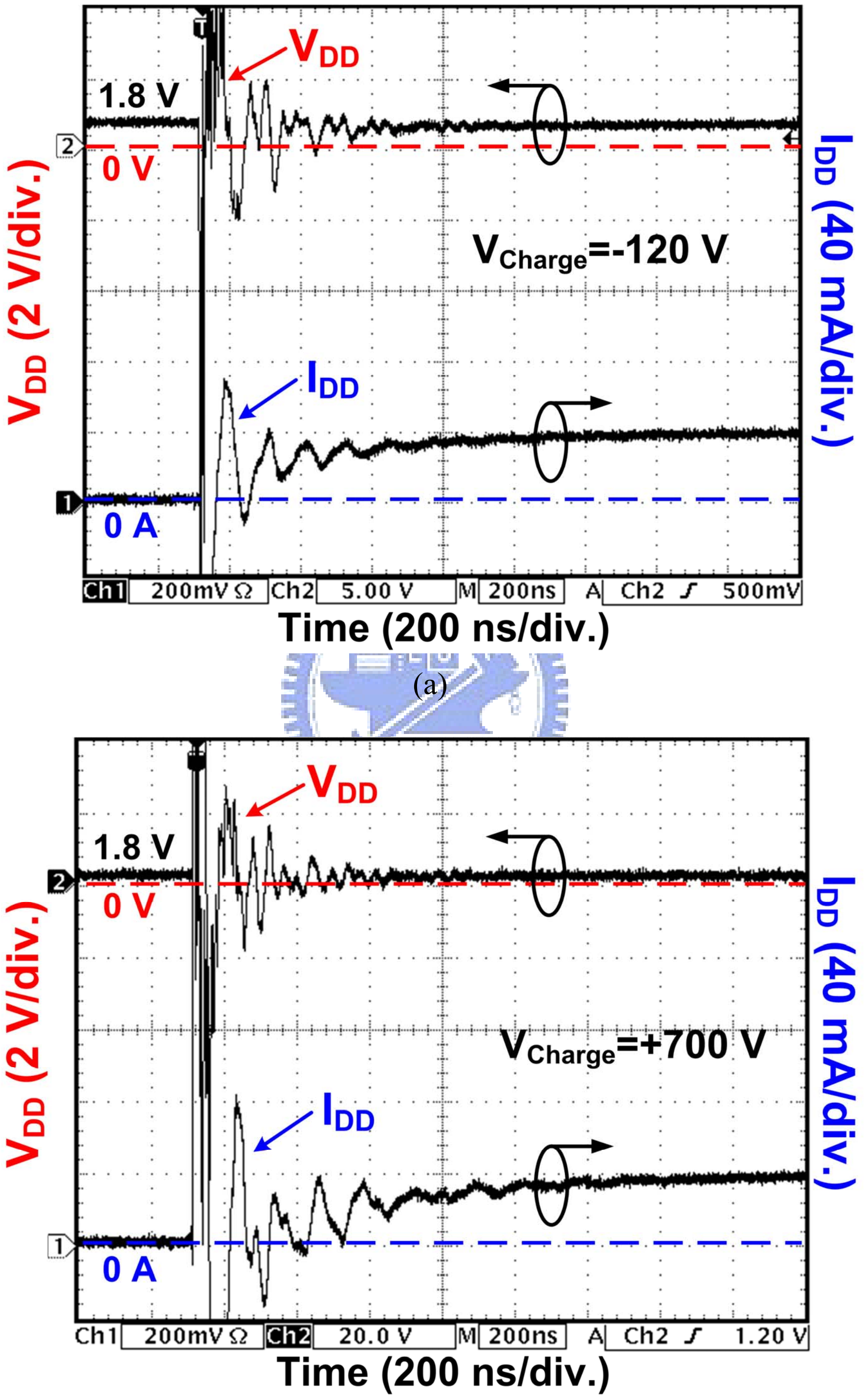


(b)

Fig. 2.6 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with NMOS+ PMOS feedback under TLU test with V_{Charge} of (a) -4 V, and (b) +12 V.

For the power-rail ESD clamp circuit with cascaded PMOS feedback, the measured V_{DD} and I_{DD} transient responses are shown in Figs. 2.7(a) and 2.7(b) under the TLU test with the initial V_{Charge} of -120 V and +700 V, respectively. The similar latchup-like failure also occurs in this power-rail ESD clamp circuit due to the latch-on state of ESD-clamping NMOS after

TLU test. The TLU levels (the minimum voltage of V_{Charge} to induce the latchup-like failure on V_{DD}) among the aforementioned four different power-rail ESD clamp circuits are listed in Table 2.1.



(a)

(b)

Fig. 2.7 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with cascaded PMOS feedback under TLU test with V_{Charge} of (a) -120 V, and (b) +700 V.

Table 2.1

Comparison on TLU Levels among Four Power-Rail ESD Clamp Circuits Under TLU Test

Power-Rail ESD Clamp Circuits	Positive TLU Level	Negative TLU Level
Typical RC-Based Detection	Over +1 kV	Over -1 kV
With PMOS Feedback	Over +1 kV	Over -1 kV
With NMOS+PMOS Feedback	+12 V	-4 V
With Cascaded PMOS Feedback	+700 V	-120 V

2.3.2. System-Level ESD Test

In the standard of IEC 61000-4-2, two test modes have been specified, which are air-discharge test mode and contact-discharge test mode. Fig. 2.8 shows the standard measurement setup of the system-level ESD test with indirect contact-discharge test mode. The measurement setup of system-level ESD test consists of a wooden table on the grounded reference plane (GRP). In addition, an insulation plane is used to separate the equipment under test (EUT) from the horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470 kΩ resistors in series. When the ESD gun zaps the HCP, the electromagnetic interference (EMI) coming from the ESD will be coupled into all CMOS ICs inside EUT. The power lines of CMOS ICs inside EUT will be disturbed by such high ESD-coupled energy.

Compared with the component-level HBM ESD tests, where the objects under test are ICs, the system-level ESD test aims to evaluate the robustness of electronic products. The equivalent circuit of ESD gun used in the system-level ESD test. The ESD gun has the charging (energy-storage) capacitor of 150pF and discharge resistor of 330Ω. In the HBM component-level ESD test, however, the charging capacitor (discharge resistor) is a smaller (larger) value of 100pF (1.5kΩ). Thus, compared with the ESD current in component-level ESD test, ESD current in system-level ESD test has much larger peak current and shorter rise time, leading to more severe damages for electronic products or their interior ICs. It has also been proven that a robust CMOS IC product with high component-level ESD levels could be very susceptible to the system-level ESD test. Thus, efficient ESD protection methodologies against system-level ESD events are very significant for electronic products.

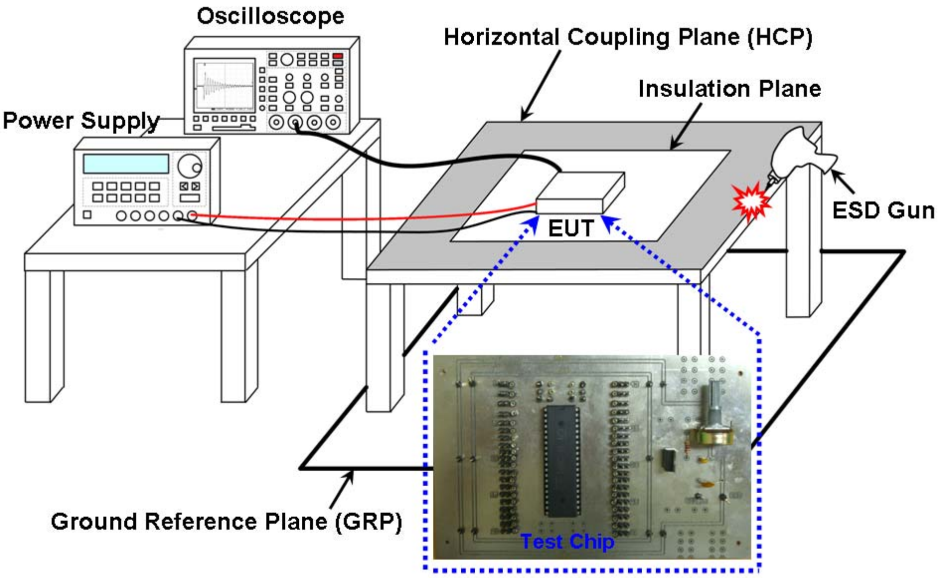
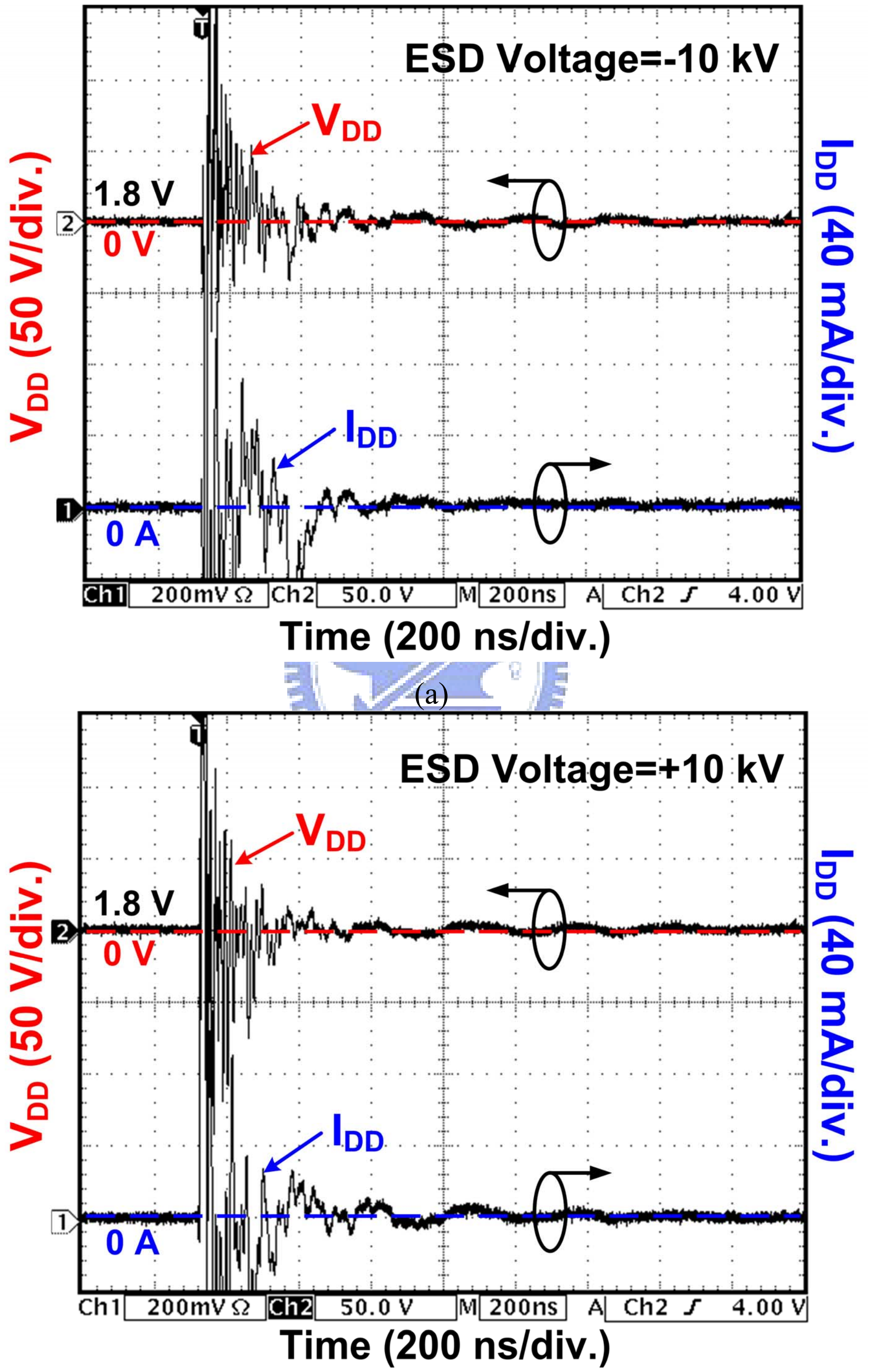


Fig. 2.8 Measurement setup for system-level ESD test with indirect contact-discharge mode.

With such a standard measurement setup, the susceptibility of different power-rail ESD clamp circuits against the system-level ESD stresses can be evaluated. The stand alone power-rail ESD clamp circuit in IC package is powered up with power supply of 1.8 V. Before any ESD zapping, the initial V_{DD} voltage level on the IC is measured to make sure the correct bias of 1.8 V. After every ESD zapping, the voltage level on V_{DD} node of IC is measured again to watch whether latchup-like failure occurs after the system-level ESD test, or not. If the latchup-like failure occurs, the potential on V_{DD} node will be pulled down to a much lower level due to the latch-on state of ESD-clamping NMOS in the power-rail ESD clamp circuits, and I_{DD} will be significantly increased.

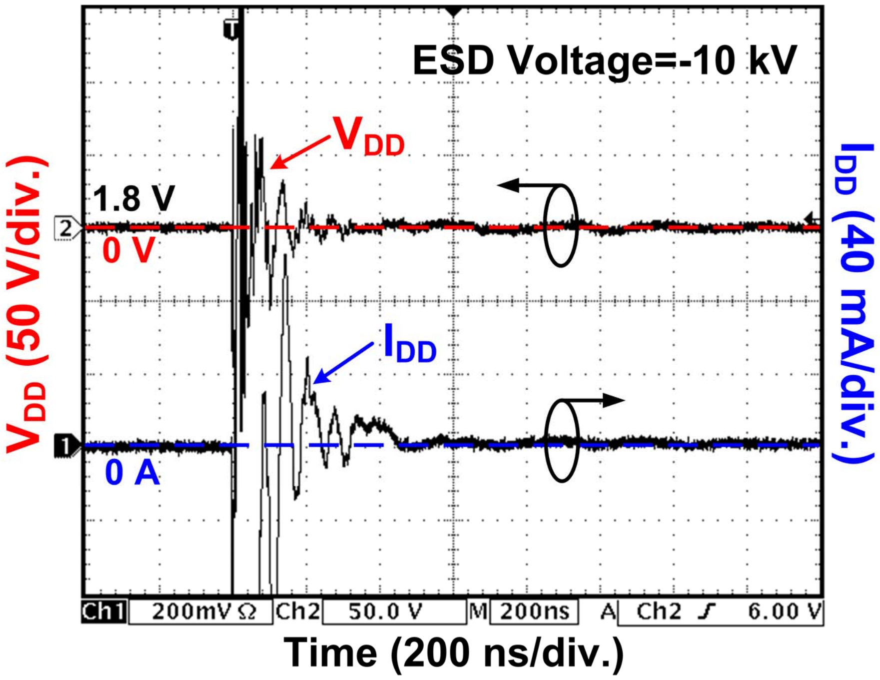
With the system-level ESD measurement setup in Fig. 2.8, the V_{DD} and I_{DD} transient responses can be recorded by the oscilloscope, which can clearly indicate whether the latchup-like failure occurs or not. Figs. 2.9(a) and 2.9(b) show the measured V_{DD} and I_{DD} transient responses on the power-rail ESD clamp circuit with typical RC-based detection when ESD gun with ESD voltage of -10 kV and +10 kV zapping on the HCP, respectively. After the system-level ESD test with an ESD voltage of -10 kV, latchup-like failure is not initiated in this power-rail ESD clamp circuit, because I_{DD} is still kept at zero, as shown in Fig. 2.9(a). After the system-level ESD test with an ESD voltage of +10 kV, latchup-like failure is not observed in Fig. 2.9(b). Under system-level ESD test with ESD voltage of -10 kV and +10 kV, the measured V_{DD} and I_{DD} transient waveforms on the power-rail ESD clamp circuit with PMOS feedback are shown in Figs. 10(a) and 10(b), respectively. Under system-level ESD test with an ESD voltage of -10 kV (+10 kV), V_{DD} acts with the intended bipolar trigger. Meanwhile, latchup-like failure does not occur because I_{DD} is not increased, as shown in Fig. 2.10(a) (Fig. 2.10(b)). For the power-rail ESD clamp circuits with typical RC-based detection or PMOS feedback, latchup-like failure does not occur even though the ESD voltage is as high as -10 kV or +10 kV in the system-level ESD test.



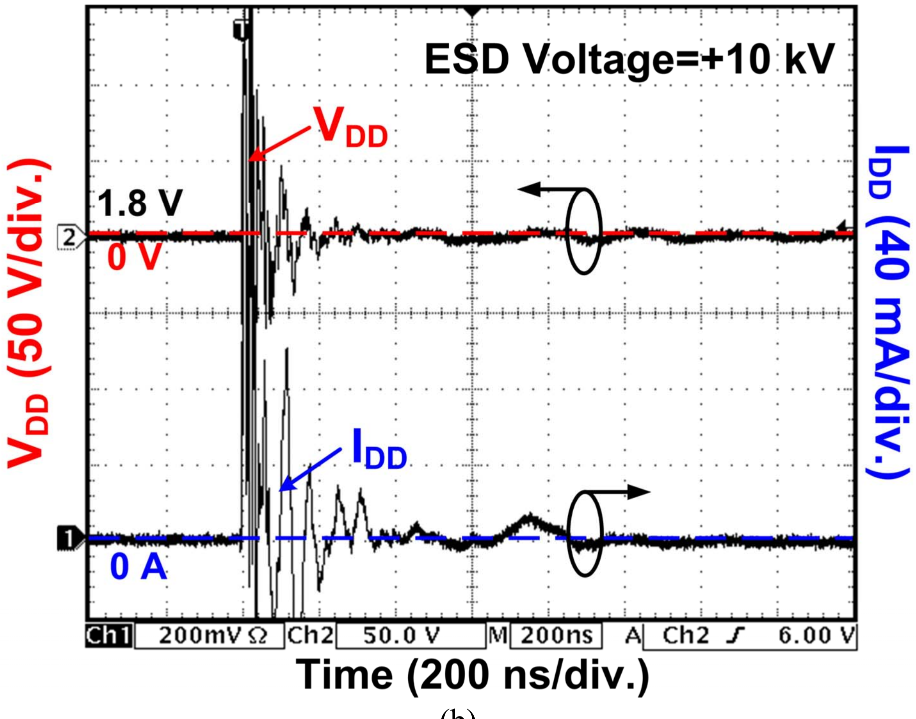
(a)

(b)

Fig. 2.9 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with typical RC-based detection under system-level ESD test with ESD voltage of (a) -10 kV, and (b) +10 kV.



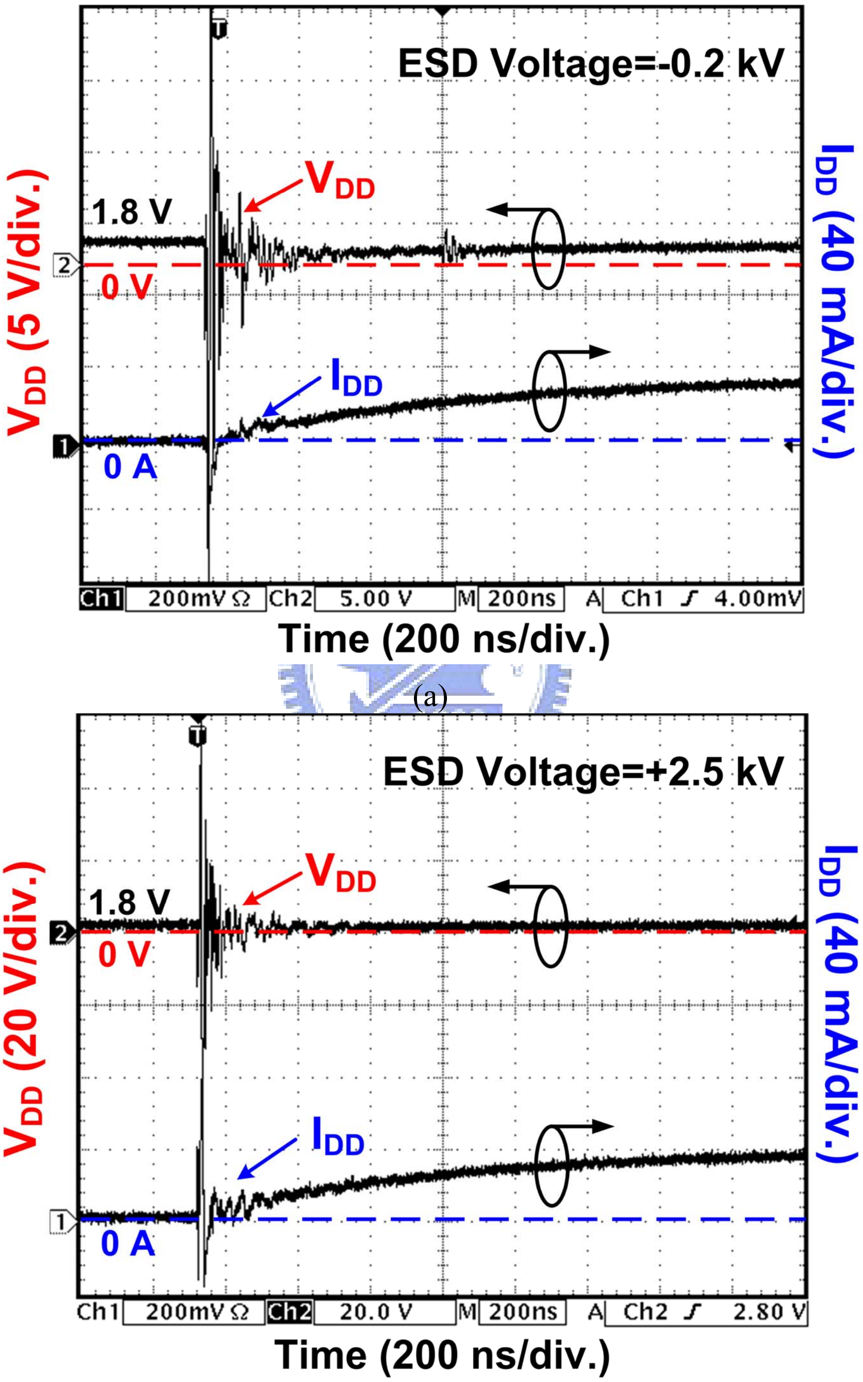
(a)



(b)

Fig. 2.10 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with PMOS feedback under system-level ESD test with ESD voltage of (a) -10 kV, and (b) +10 kV.

Figs. 2.11(a) and 2.11(b) show the measured V_{DD} and I_{DD} transient responses on the power-rail ESD clamp circuit with NMOS+PMOS feedback under the system-level ESD test with ESD voltages of -0.2 kV and +2.5 kV, respectively. After the system-level ESD test with an ESD voltage of -0.2 kV, latchup-like failure can be initiated in this power-rail ESD clamp circuit, because I_{DD} is significantly increased and V_{DD} is pulled down as shown in Fig. 2.11(a). After the system-level ESD test with an ESD voltage of +2.5 kV, the latchup-like failure can be also found in Fig. 2.11(b).

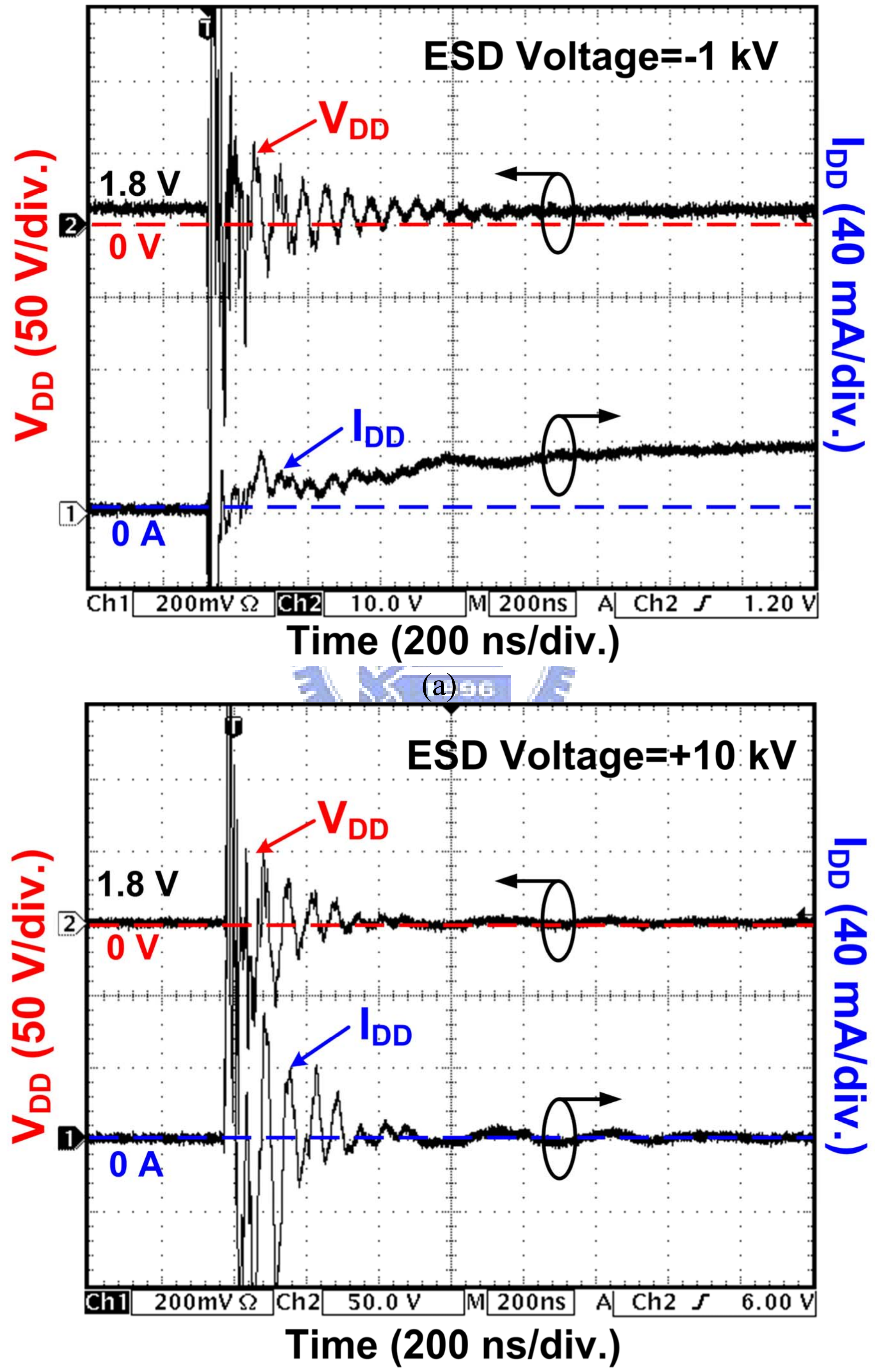


(a)

(b)

Fig. 2.11 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback under system-level ESD test with ESD voltage of (a) -0.2 kV, and (b) +2.5 kV.

For the power-rail ESD clamp circuit with cascaded PMOS feedback, the measured V_{DD} and I_{DD} transient responses are shown in Figs. 2.12(a) and 2.12(b) under the system-level ESD test with ESD voltages of -1 kV and +10 kV, respectively. The similar latchup-like failure also occurs due to the latch-on state of ESD-clamping NMOS under the system-level ESD test with an ESD voltage of -1 kV, as shown in Fig. 2.12(a).



(a)

(b)

Fig. 2.12 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with cascaded PMOS feedback under system-level ESD test with ESD voltage of (a) -1 kV, and (b) +10 kV.

The susceptibility among the aforementioned four different power-rail ESD clamp circuits against system-level ESD test are listed in Table 2.2. The power-rail ESD clamp circuits with NMOS+PMOS feedback or with cascaded PMOS feedback have lower ESD voltages to cause latchup-like failure after system-level ESD test. Such measured results by ESD gun test are consistent with those of TLU shown in Table 2.1. From the experimental results, the power-rail ESD clamp circuit designed with NMOS+PMOS feedback is highly sensitive to transient-induced latchup-like failure. The typical power-rail ESD clamp circuits with RC-based detection and with PMOS feedback are free to such a latchup-like failure.

Table 2.2
Comparison on the Susceptibility among Four Different Power-Rail ESD Clamp Circuits Under System-Level ESD Test

Power-Rail ESD Clamp Circuits	Positive ESD Stress	Negative ESD Stress
Typical RC-Based Detection	Over +10 kV	Over -10 kV
With PMOS Feedback	Over +10 kV	Over -10 kV
With NMOS+PMOS Feedback	+2.5 kV	-0.2 kV
With Cascaded PMOS Feedback	Over +10 kV	-1 kV

The failure location after system-level ESD test has been inspected, as shown in Fig. 2.13. The failure location is located at the V_{DD} metal line from the V_{DD} pad to the power-rail ESD clamp circuit, which was drawn with a metal width of 30 μm in the test chip.

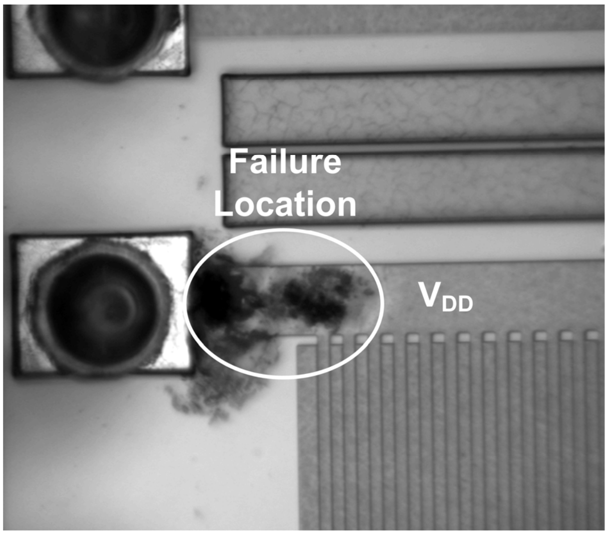


Fig. 2.13 Failure location of power-rail ESD clamp circuit after system-level ESD stress.

2.3.3. Electrical Fast Transient (EFT) Test

The measurement setup for EFT test is shown in Fig. 2.14. The supply voltage of 1.8 V is used as V_{DD} and the EFT generator is connected directly to the device under test (DUT) through the cable in this work. The voltage and current waveforms on the DUT (at V_{DD} node) after EFT test are monitored by the digital oscilloscope. With such a standard measurement setup, the susceptibility of different power-rail ESD clamp circuits against the EFT tests can be evaluated. The stand alone power-rail ESD clamp circuit in IC package is powered up with power supply of 1.8 V. Before any EFT zapping, the initial V_{DD} voltage level on the IC is measured to make sure the correct bias of 1.8 V. After every EFT voltage zapping, the voltage level on V_{DD} node of IC is measured again to watch whether latchup-like failure occurs after the EFT test, or not. If the latchup-like failure occurs, the potential on V_{DD} node will be pulled down to a much lower level due to the latch-on state of ESD-clamping NMOS in the power-rail ESD clamp circuits, and I_{DD} will be significantly increased.

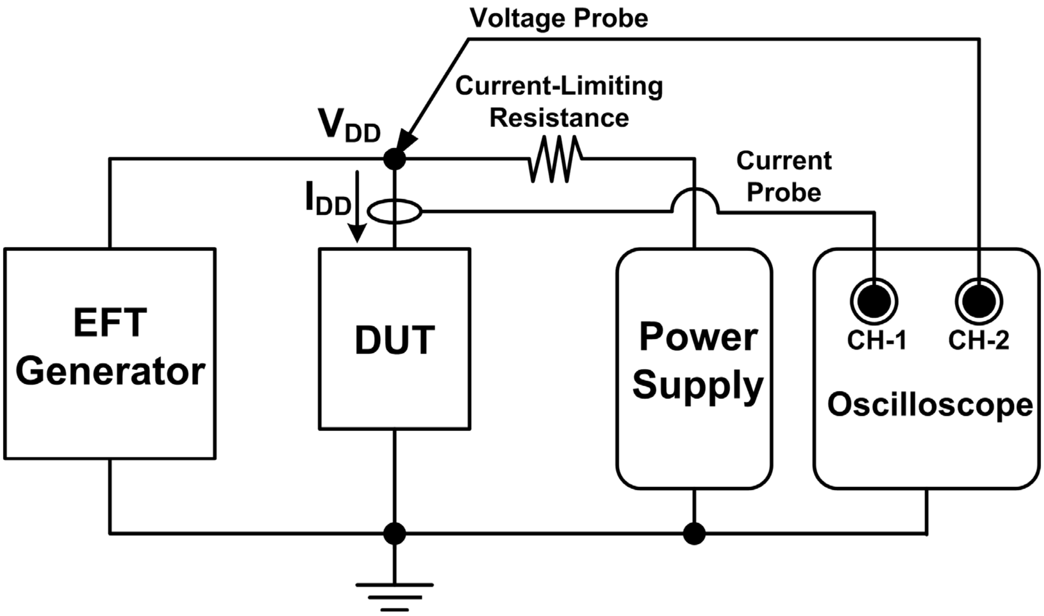
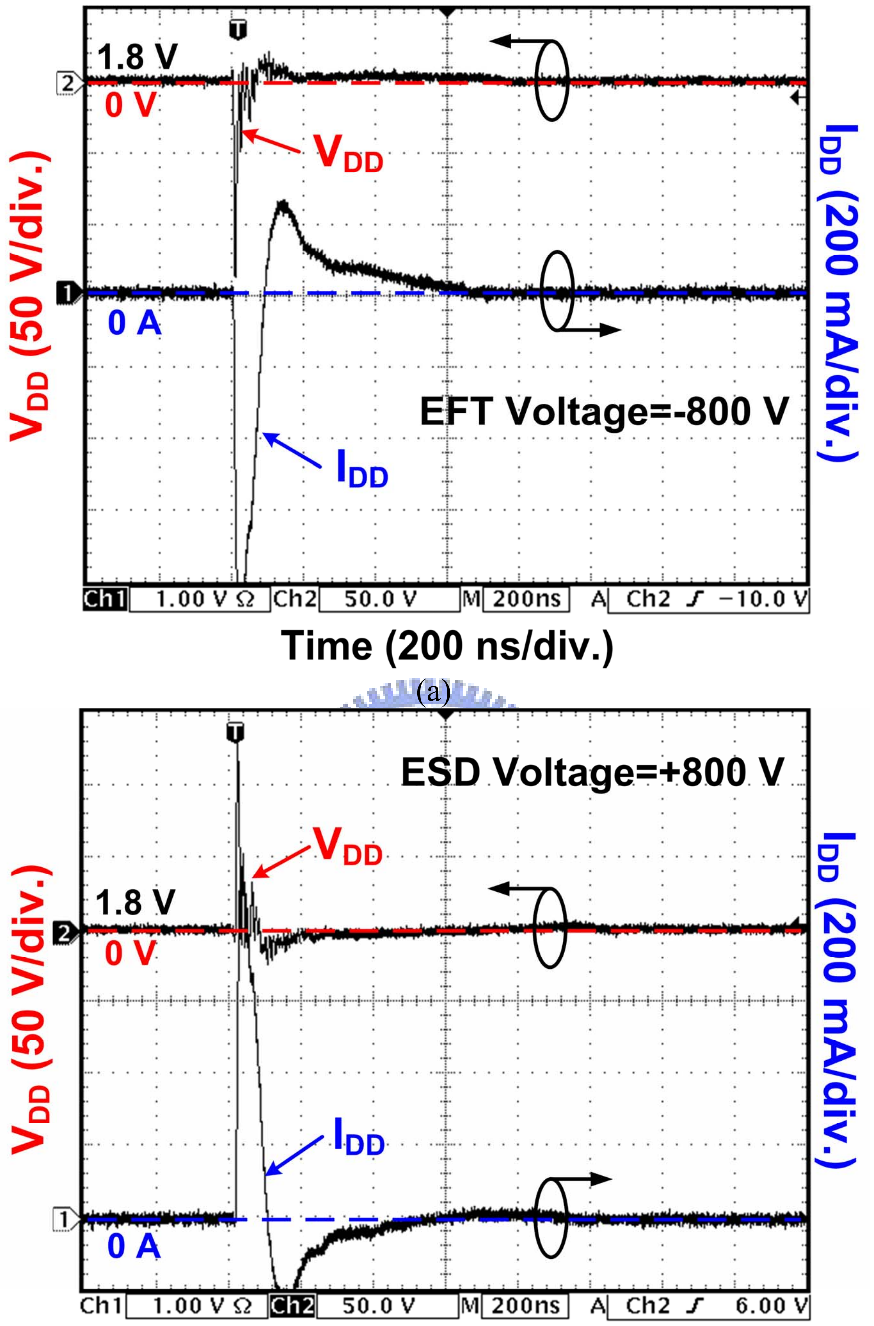


Fig. 2.14 Measurement setup for EFT test with IC power supply of 1.8 V.

With the EFT measurement setup shown in Fig. 2.14, the V_{DD} and I_{DD} transient responses can be recorded by the oscilloscope, which can clearly indicate whether the latchup-like failure occurs or not. Figs. 2.15(a) and 2.15(b) show the measured V_{DD} and I_{DD} transient responses on the power-rail ESD clamp circuit with typical RC-based detection when EFT generator with EFT voltage of -800 V and +800 V zapping, respectively. After the EFT test with an EFT voltage of -800 V, latchup-like failure is not initiated in this power-rail ESD clamp circuit, because I_{DD} is still kept at zero, as shown in Fig. 2.15(a). After the EFT test with an EFT voltage of +800 V, latchup-like failure is not observed in Fig. 2.15(b).



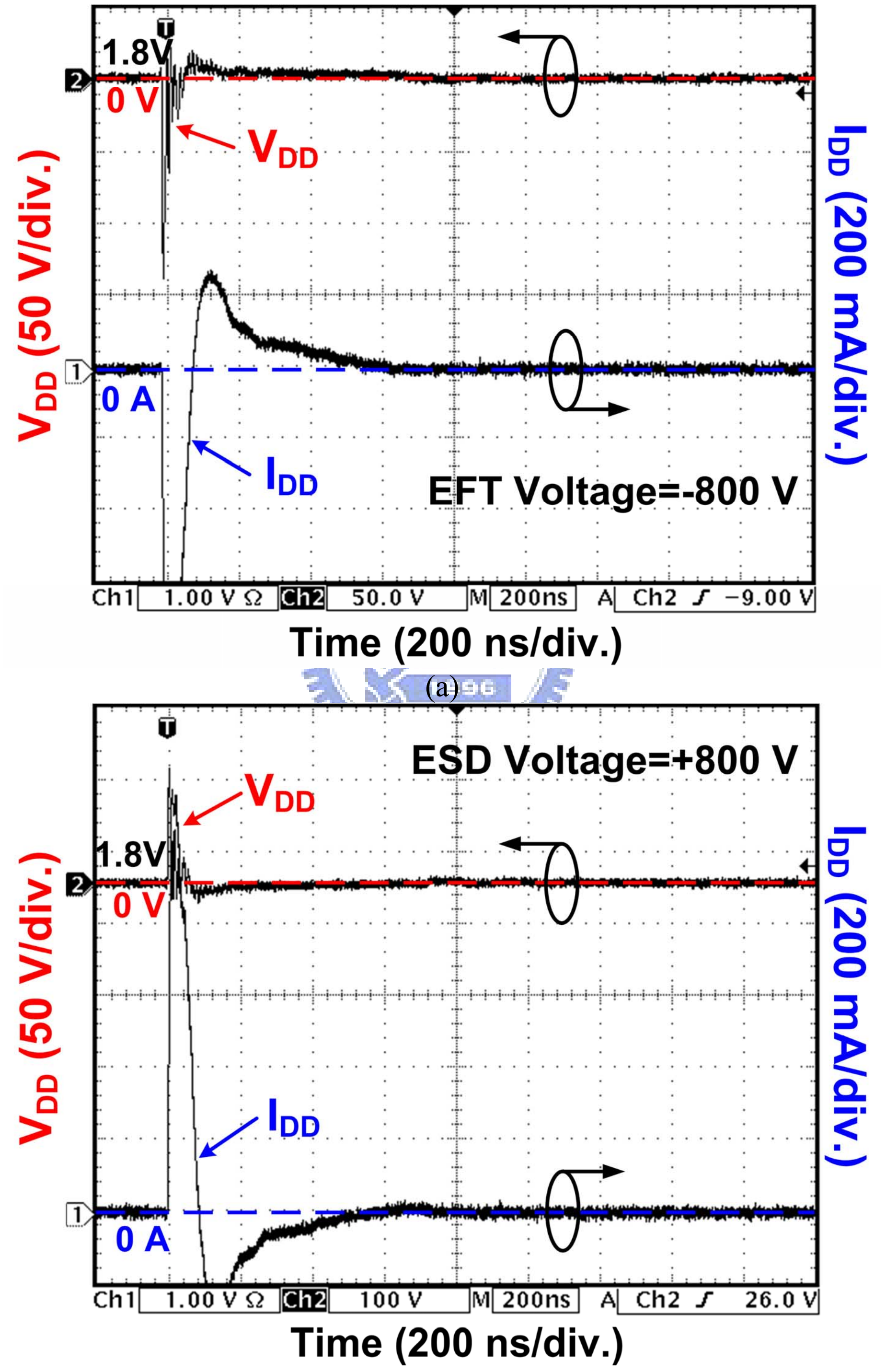
(a)

(b)

Fig. 2.15 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with typical RC-based detection under EFT test with EFT voltage of (a) -800 V, and (b) +800 V.

Under EFT test with EFT voltage of -800 V and +800 V, the measured V_{DD} and I_{DD} transient waveforms on the power-rail ESD clamp circuit with PMOS feedback are shown in Figs. 2.16(a) and 2.16(b), respectively. Under EFT test with an EFT voltage of -800 V (+800

V), V_{DD} acts with the EFT-induced trigger. Meanwhile, latchup-like failure does not occur because I_{DD} is not increased, as shown in Fig. 2.16(a) (Fig. 2.16(b)). For the power-rail ESD clamp circuits with typical RC-based detection or PMOS feedback, latchup-like failure does not occur even though the EFT voltage is as high as -800 V or +800 V in the EFT test.

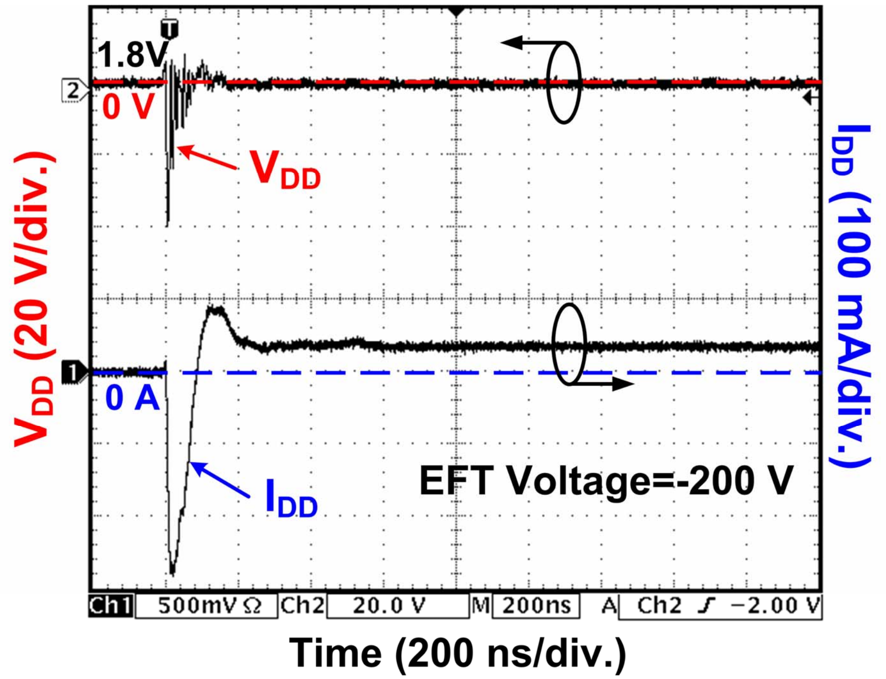


(a)

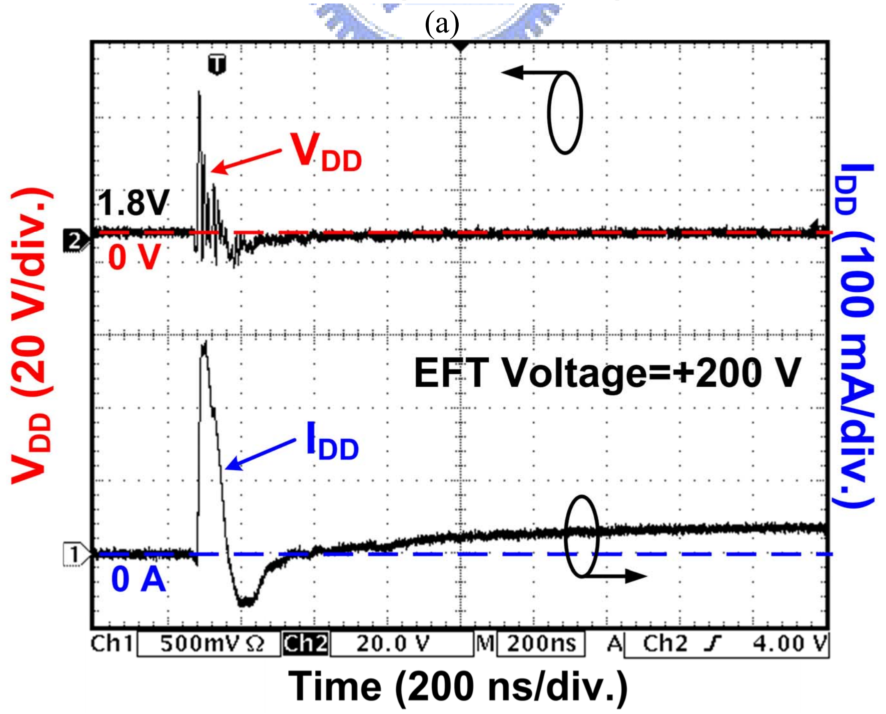
(b)

Fig. 2.16 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with PMOS feedback under EFT test with EFT voltage of (a) -800 V, and (b) +800 V.

Figs. 2.17(a) and 2.17(b) show the measured V_{DD} and I_{DD} transient responses on the power-rail ESD clamp circuit with NMOS+PMOS feedback under the EFT test with EFT voltages of -200 V and +200 V, respectively. After the EFT test with an EFT voltage of -200 V, latchup-like failure can be initiated in this power-rail ESD clamp circuit, because I_{DD} is significantly increased and V_{DD} is pulled down as shown in Fig. 2.17(a). After the EFT test with an EFT voltage of +200 V, the latchup-like failure can be also found in Fig. 2.17(b).



(a)



(b)

Fig. 2.17 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback under EFT test with EFT voltage of (a) -200 V, and (b) +200 V.

All the PMOS and NMOS devices in the ESD-transient detection circuits are surrounded with double guard rings to guarantee no latchup issue in this part. This implies that the feedback loop in the ESD-transient detection circuit is locked after EFT test and continually keeps the ESD-clamping NMOS in the latch-on state. From the observed voltage and current waveforms, large I_{DD} current is caused by the latch-on state of ESD-clamping NMOS after EFT tests.

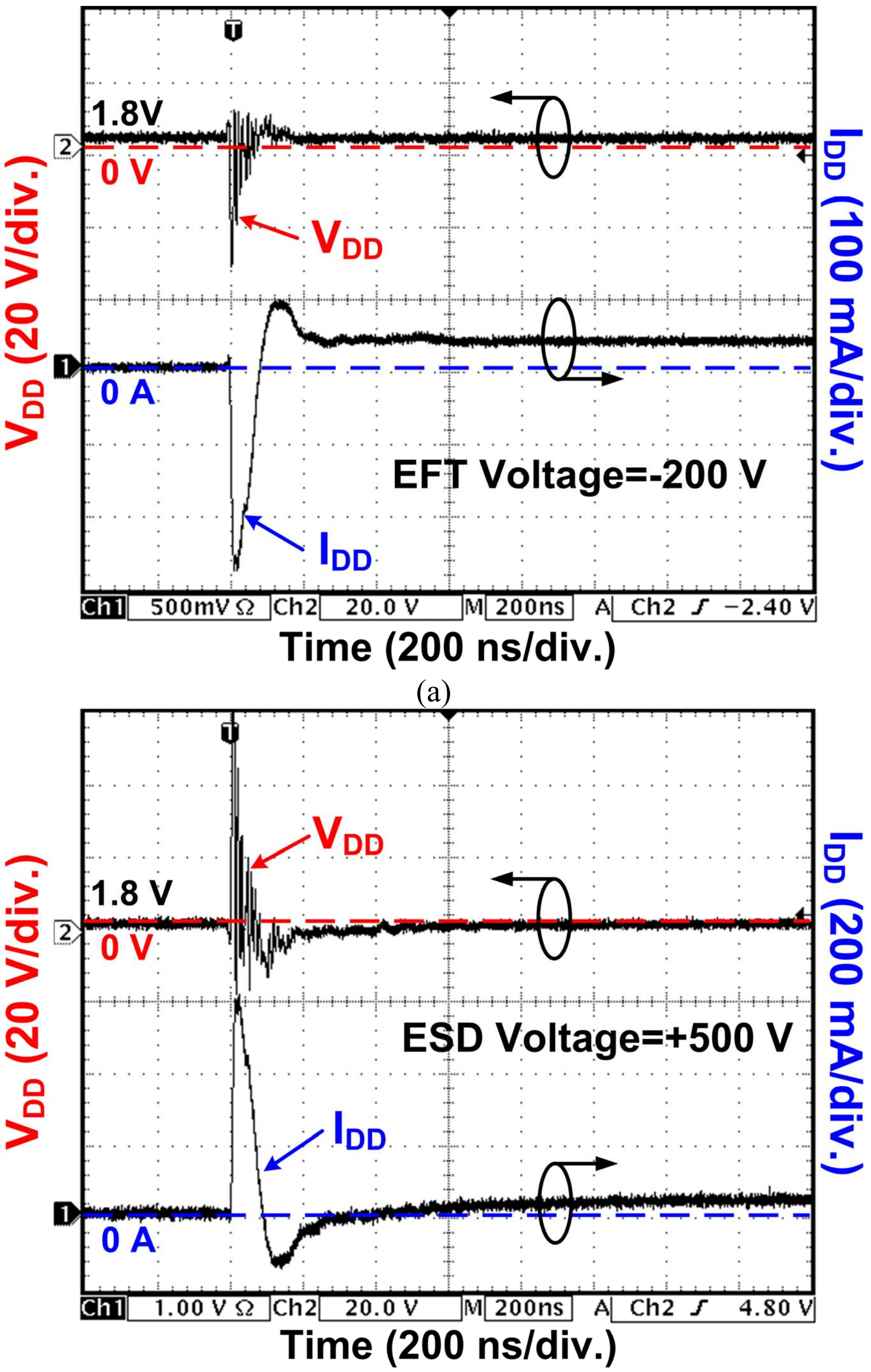
For the power-rail ESD clamp circuit with cascaded PMOS feedback, the measured V_{DD} and I_{DD} transient responses are shown in Figs. 2.18(a) and 2.18(b) under the EFT test with EFT voltages of -200 V and +500 V, respectively. The similar latchup-like failure also occurs in this power-rail ESD clamp circuit due to the latch-on state of ESD-clamping NMOS under the EFT test with an EFT voltage of -200 V, as shown in Fig. 2.18(a).

The susceptibility among the aforementioned four different power-rail ESD clamp circuits against EFT tests are listed in Table 2.3. The power-rail ESD clamp circuits with NMOS+PMOS feedback or with cascaded PMOS feedback have lower EFT voltages to cause latchup-like failure after EFT test. From the experimental results, the power-rail ESD clamp circuit designed with NMOS+PMOS feedback is highly sensitive to transient-induced latchup-like failure. The typical power-rail ESD clamp circuits with RC-based detection and with PMOS feedback are free to such a latchup-like failure.

Table 2.3

Comparison on Susceptibility among Four Different Power-Rail ESD Clamp Circuits Against EFT Tests

Power-Rail ESD Clamp Circuits	Positive EFT Voltage	Negative EFT Voltage
Typical RC-Based Detection	**Over +800 V**	**Over -800 V**
With PMOS Feedback	**Over +800 V**	**Over -800 V**
With NMOS+PMOS Feedback	**Under +200 V**	**Under -200 V**
With Cascaded PMOS Feedback	**+500 V**	**Under -200 V**



(a)

(b)

Fig. 2.18 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with cascaded PMOS feedback under EFT test with EFT voltage of (a) -200 V, and (b) +500 V. Latchup-like failure in this EFT test.

The failure location after EFT test has been inspected, as shown in Fig. 2.19. The failure location is located at the V_{DD} metal line from the V_{DD} pad to the power-rail ESD clamp circuit, which was drawn with a metal width of 30 μm in the test chip.

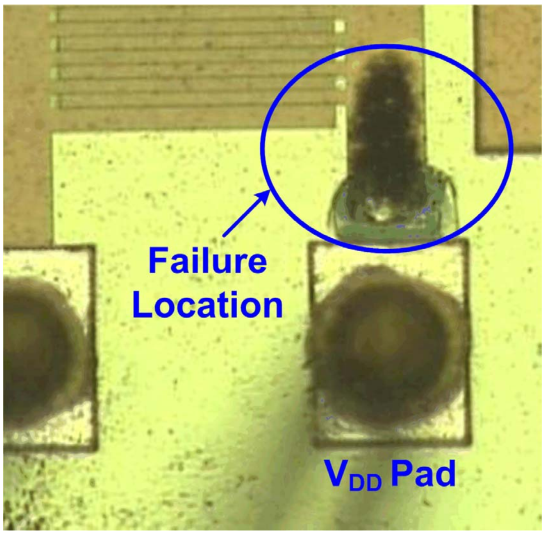


Fig. 2.19 Failure location of power-rail ESD clamp circuit after EFT tests.

2.4. Modified Power-Rail ESD Clamp Circuit

From the above measurement results, some ESD-transient detection circuits designed with feedback loop in the power-rail ESD clamp circuits continually keep the ESD-clamping NMOS in the latch-on state after the system-level ESD test. The latch-on ESD-clamping NMOS between V_{DD} and VSS power lines in the powered-up microelectronic system causes a serious latchup-like failure in CMOS ICs. In order to meet electromagnetic compatibility regulation under system-level ESD test, modified power-rail ESD clamp circuits without suffering the latchup-like failure are highly desirable. It has been reported that the power-rail ESD clamp circuit with conventional rise time detector and a separated on-time control circuit can reduce the RC area and improve the immunity to false triggering [19]. The separated on-time control circuit can keep the ESD-clamping NMOS turned on for the expected maximum duration of an ESD event. From the measured results under the system-level ESD test, two ESD-transient detection circuits designed with feedback loop in the power-rail ESD clamp circuits had been found suffering latchup-like failure. In order to avoid such a latchup-like failure, it could be useful to reduce the latch strength of the feedback loop in the ESD-transient detection circuit by suitable device dimension sizing. In this work, another modified power-rail ESD clamp circuit is proposed to avoid such a latchup-like failure. The proposed power-rail ESD clamp circuit can provide high enough chip-level ESD robustness without suffering the latchup-like failure during the system-level ESD test.

2.4.1. Power-Rail ESD Clamp Circuit With NMOS Reset Function

Fig. 2.20 shows the proposed power-rail ESD clamp circuit with NMOS reset function to overcome the latchup-like failure, which is realized with NMOS+PMOS feedback and an additional NMOS device (M_{NR1}) to provide the reset function after system-level ESD stresses. When the ESD-clamping NMOS is latched-on, the NMOS device (M_{NR1}) will be turned on after the time out of RC time constant. Thus, the gate potential of the ESD-clamping NMOS will be pulled down toward 0V to release the "latch-on" state.

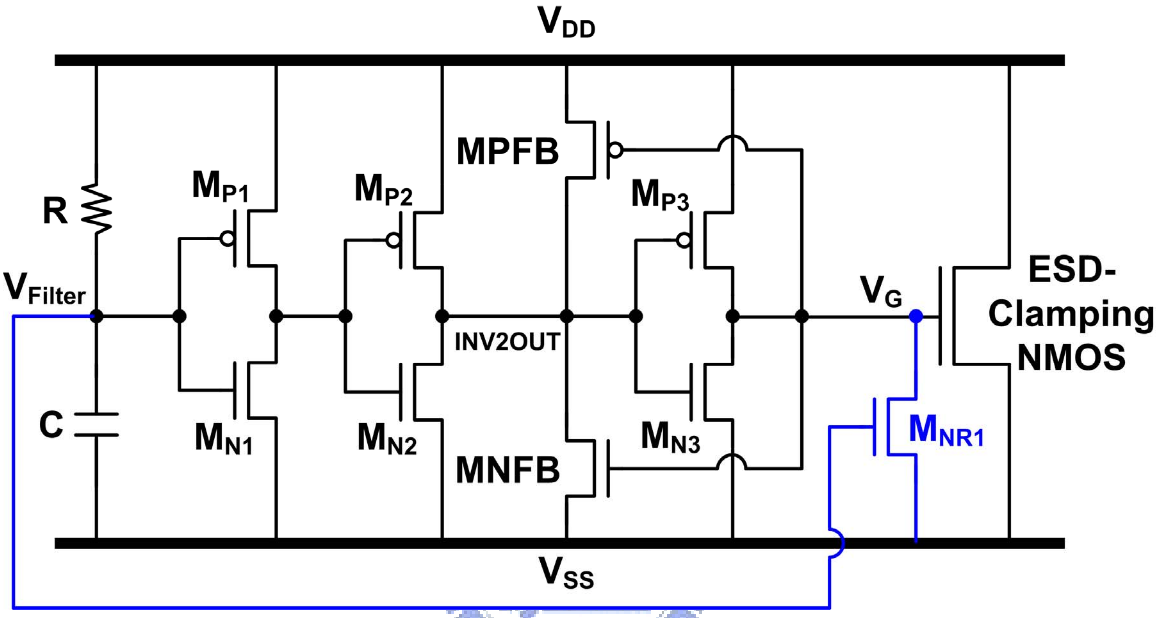


Fig. 2.20 The proposed power-rail ESD clamp circuit with NMOS reset function to overcome latchup-like failure.

2.4.2. Simulation Results

The NMOS device M_{NR1} is used to release the "latch-on" state of the ESD-clamping NMOS. After system-level ESD tests, the potential on the V_{Filter} node is charged toward the voltage potential on V_{DD}. When the potential at the V_{Filter} node is greater than the threshold voltage of M_{NR1}, M_{NR1} can be turned on to pull down any potential at V_G. Thus, the "latch-on" state of the ESD-clamping NMOS caused by system-level ESD test can be released. With the NMOS+PMOS feedback in the power-rail ESD clamp circuit, the dynamic currents of M_{P2}, M_{N2}, MPFB, and MNFB determine the critical voltage to trigger on the ESD-clamping NMOS. The dimensions of M_{NR1} and M_{P3} should be appropriately designed with consideration of the NMOS+PMOS feedback loop. By increasing the device size of M_{NR1}, the latch-on time of ESD-clamping NMOS can be reduced. Therefore, the proposed power-rail ESD clamp circuit with NMOS reset function can avoid the latchup-like failure after system-level ESD tests. Compared with power-rail ESD clamp circuits with NMOS+PMOS feedback, the proposed power-rail ESD clamp circuit with NMOS reset function has a shorter turn-on time of around 380ns.

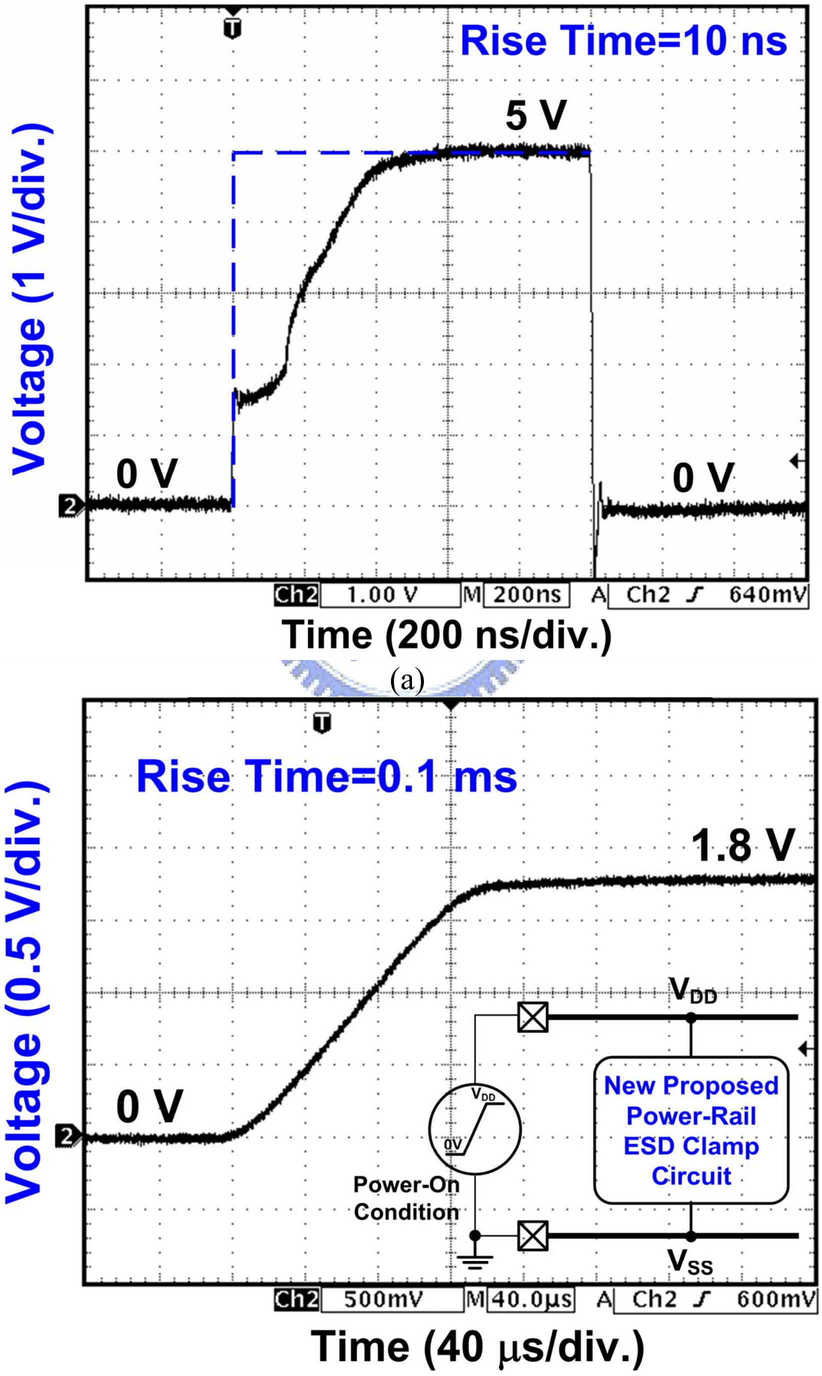
2.4.3. Experimental Results

The proposed power-rail ESD clamp circuit with NMOS reset function has been designed and fabricated in a 0.18-μm CMOS process. Measurements were performed to compare the system-level ESD robustness between this proposed and the original power-rail ESD clamp circuits.

2.4.3.1. Turn-On Verification

To verify the ESD-transient detection function of the proposed power-rail ESD clamp circuit with NMOS reset function, a voltage pulse generated from a pulse generator is used to simulate the rising edge of HBM ESD pulse, which has a square-type voltage waveform with a rise time about 10 ns. When the voltage pulse is applied to V_{DD} power line with V_{SS} grounded, the sharp-rising edge of the ESD-like voltage pulse will trigger on the ESD-clamping NMOS to provide a low-impedance path between V_{DD} and V_{SS} power lines. Due to the limited driving current of the pulse generator, the voltage on V_{DD} power line will be degraded by the turned-on ESD-clamping NMOS. The voltage waveform on V_{DD} power line of the proposed power-rail ESD clamp circuit with NMOS reset function is shown in Fig. 2.21(a), where a voltage pulse with a pulse height of 5 V and a pulse width of 1000 ns is applied to V_{DD} power line. The voltage waveform is degraded at the rising edge because the ESD-clamping NMOS is simultaneously turned-on when the ESD-like voltage pulse is applied to V_{DD} power line. The voltage degradation is dependent on the turned-on resistance of the ESD-clamping NMOS and the output resistance (typically, 50 ohm) of the pulse generator. A larger device dimension of the ESD-clamping NMOS leads to a more serious degradation on the voltage waveform. When the V_{Filter} node is charged up to the threshold voltage of the inverter1 formed by M_{P1} and M_{N1}, the ESD-clamping NMOS will be turned off and the voltage waveform will be restored to the original voltage level. In Fig. 2.21(a), the applied 5-V voltage pulse has a recovery time of about 400 ns, which is corresponding to the turn-on time of the ESD-clamping NMOS.

To verify the action of the proposed power-rail ESD clamp circuit with NMOS reset function under normal power-on conditions, an experimental setup is shown in the inset figure of Fig. 2.21(b). A ramp voltage with a rise time of 0.1 ms and a magnitude of 1.8 V is applied to V_{DD} power line with V_{SS} power line grounded to simulate the power-on condition. The measured voltage waveform on V_{DD} power line is shown in Fig. 2.21(b), where the voltage waveform is still remained as a ramp voltage without degradation. Thus, the ESD-clamping NMOS in the proposed power-rail ESD clamp circuit with NMOS reset function has been verified to keep off while the IC is in the power-on condition.



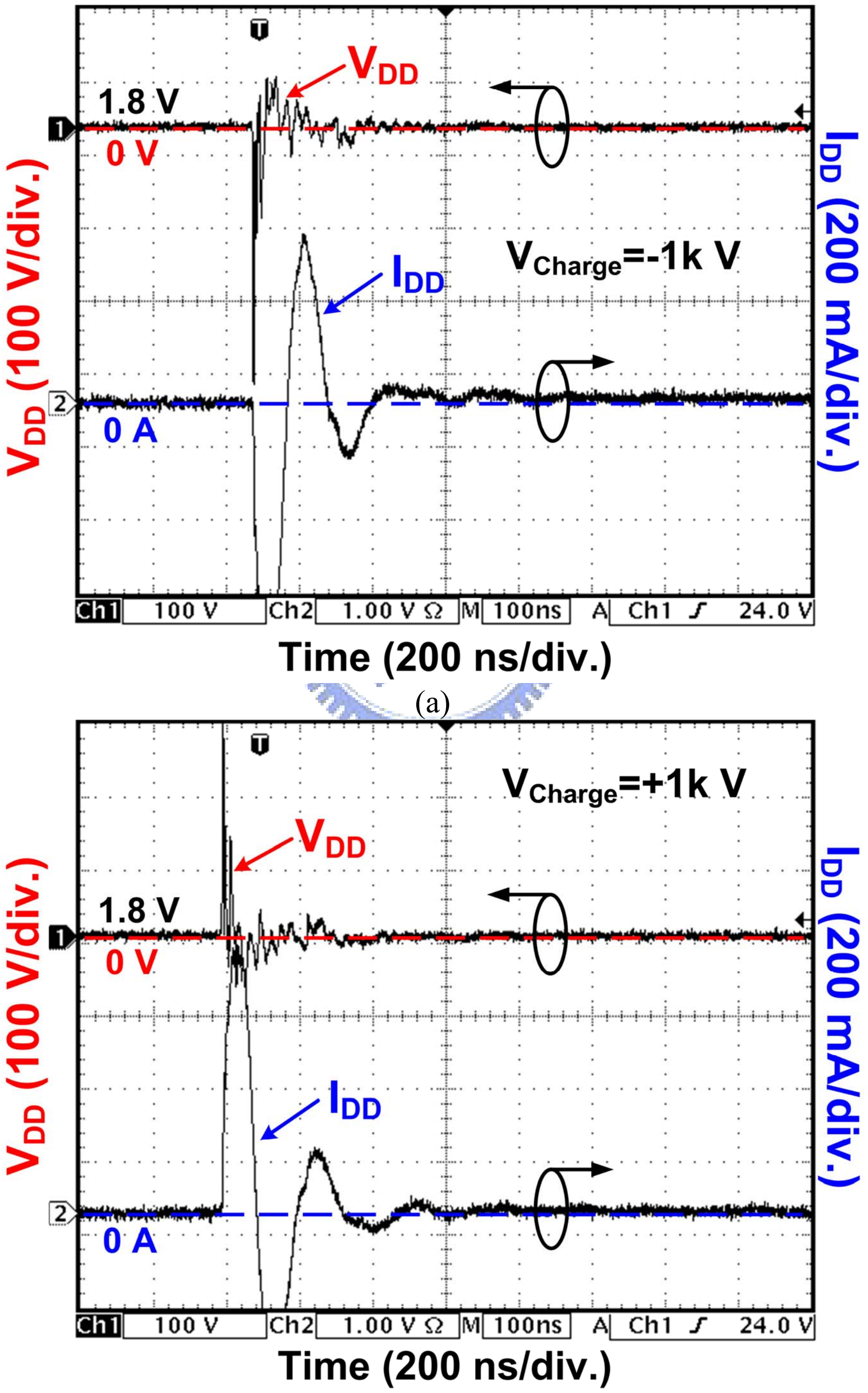
(a)

(b)

Fig. 2.21 Measured voltage waveforms on the proposed power-rail ESD clamp circuit with NMOS reset function in (a) ESD-stress condition, and (b) power-on condition.

2.4.3.2. TLU Immunity

With the TLU measurement setup in Fig. 2.5, the measured V_{DD} and I_{DD} responses on the proposed power-rail ESD clamp circuit with V_{Charge} of -1 kV and +1 kV are shown in Figs. 2.22(a) and 2.22(b), respectively. With a negative (positive) V_{Charge} of -1 kV (+1 kV), latchup-like failure does not occur in Fig. 2.22(a) (Fig. 2.22(b)) because I_{DD} is not significantly increased and V_{DD} is not pulled down.



(a)

(b)

Fig. 2.22 Measured V_{DD} and I_{DD} waveforms on the proposed power-rail ESD clamp circuit under TLU test with V_{Charge} of (a) -1 kV, and (b) +1 kV.

The TLU level of the proposed power-rail ESD clamp circuit with NMOS reset function and the original power-rail ESD clamp circuit with NMOS+PMOS feedback against system-level ESD test are listed in Table 2.4. Moreover, latchup-like failure does not occur in the proposed power-rail ESD clamp circuit after TLU tests with ESD voltage of up to -1 kV and +1 kV.

Table 2.4

Comparison on TLU Levels Between Proposed Power-Rail ESD Clamp Circuit with NMOS Reset Function and the Original ESD Clamp Circuit With NMOS+PMOS Feedback Under TLU Test

Power-Rail ESD Clamp Circuits	Positive TLU Level	Negative TLU Level
With NMOS+PMOS Feedback and NMOS Reset Function	Over +1 kV	Over -1 kV
With NMOS+PMOS Feedback	+12 V	-4 V

2.4.3.3. System-Level ESD Susceptibility

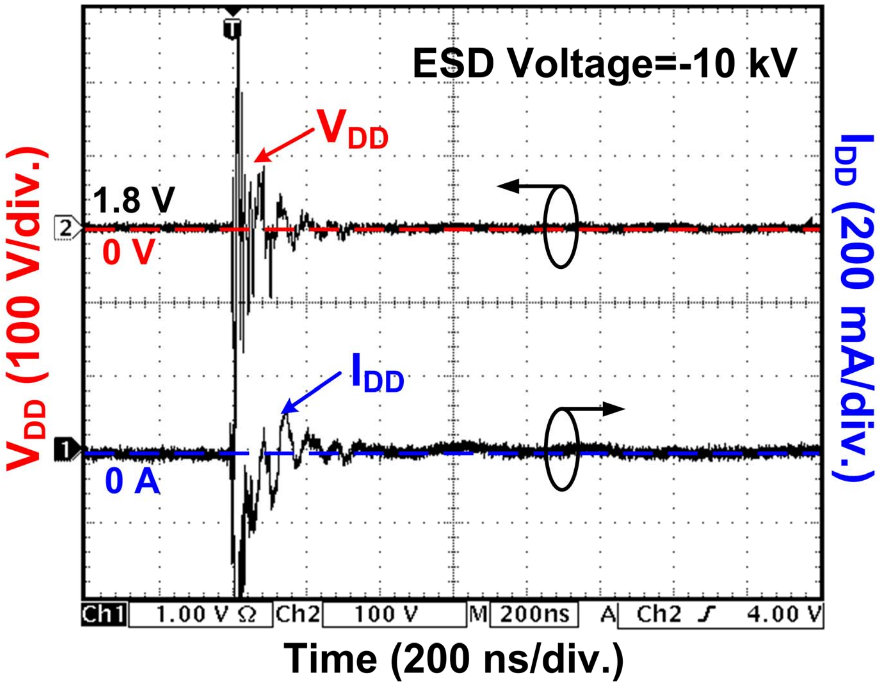
The measured V_{DD} and I_{DD} responses on the proposed power-rail ESD clamp circuit under system-level ESD tests with ESD voltages of -10 kV and +10 kV are shown in Figs. 2.23(a) and 2.23(b), respectively. With a negative (positive) ESD voltage of -10 kV (+10 kV), the latchup-like failure does not occur in Fig. 2.23(a) (Fig. 2.23(b)) because the I_{DD} is not significantly increased and V_{DD} is not pulled down.

The susceptibility of the proposed power-rail ESD clamp circuit with NMOS reset function and the original power-rail ESD clamp circuit with NMOS+PMOS feedback against system-level ESD test are compared in Table 2.5. For the proposed power-rail ESD clamp circuit, latchup-like failure does not occur.

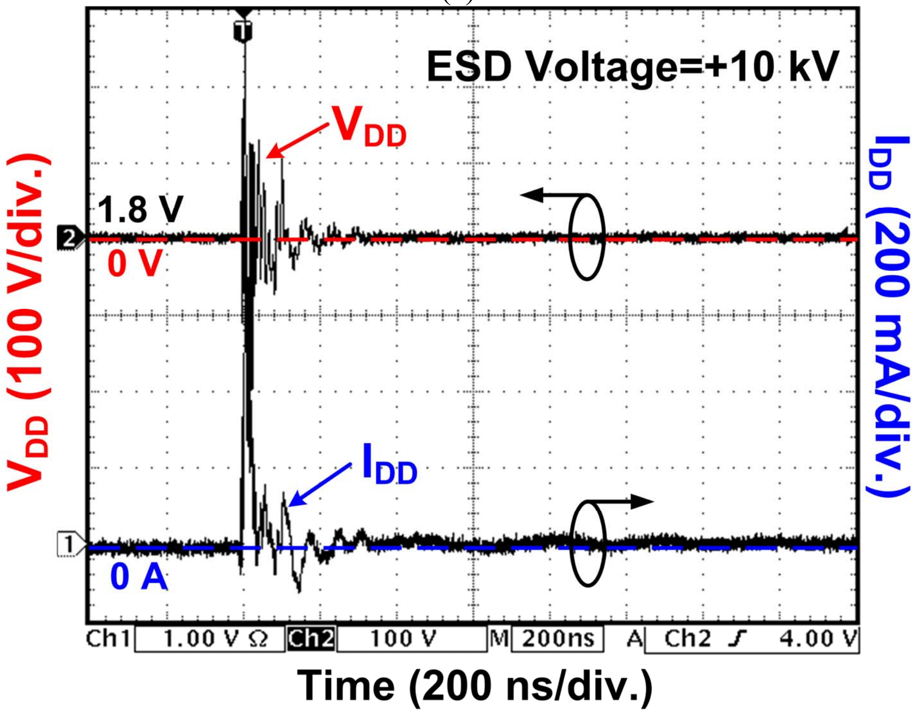
Table 2.5

Comparison on the Susceptibility Between Proposed Power-Rail ESD Clamp Circuit with NMOS Reset Function and the Original Power-Rail ESD Clamp Circuit With NMOS+PMOS Feedback Under System-Level ESD Test

Power-Rail ESD Clamp Circuits	Positive ESD Stress	Negative ESD Stress
With NMOS+PMOS Feedback and NMOS Reset Function	Over +10 kV	Over -10 kV
With NMOS+PMOS Feedback	+2.5 kV	-0.2 kV



(a)



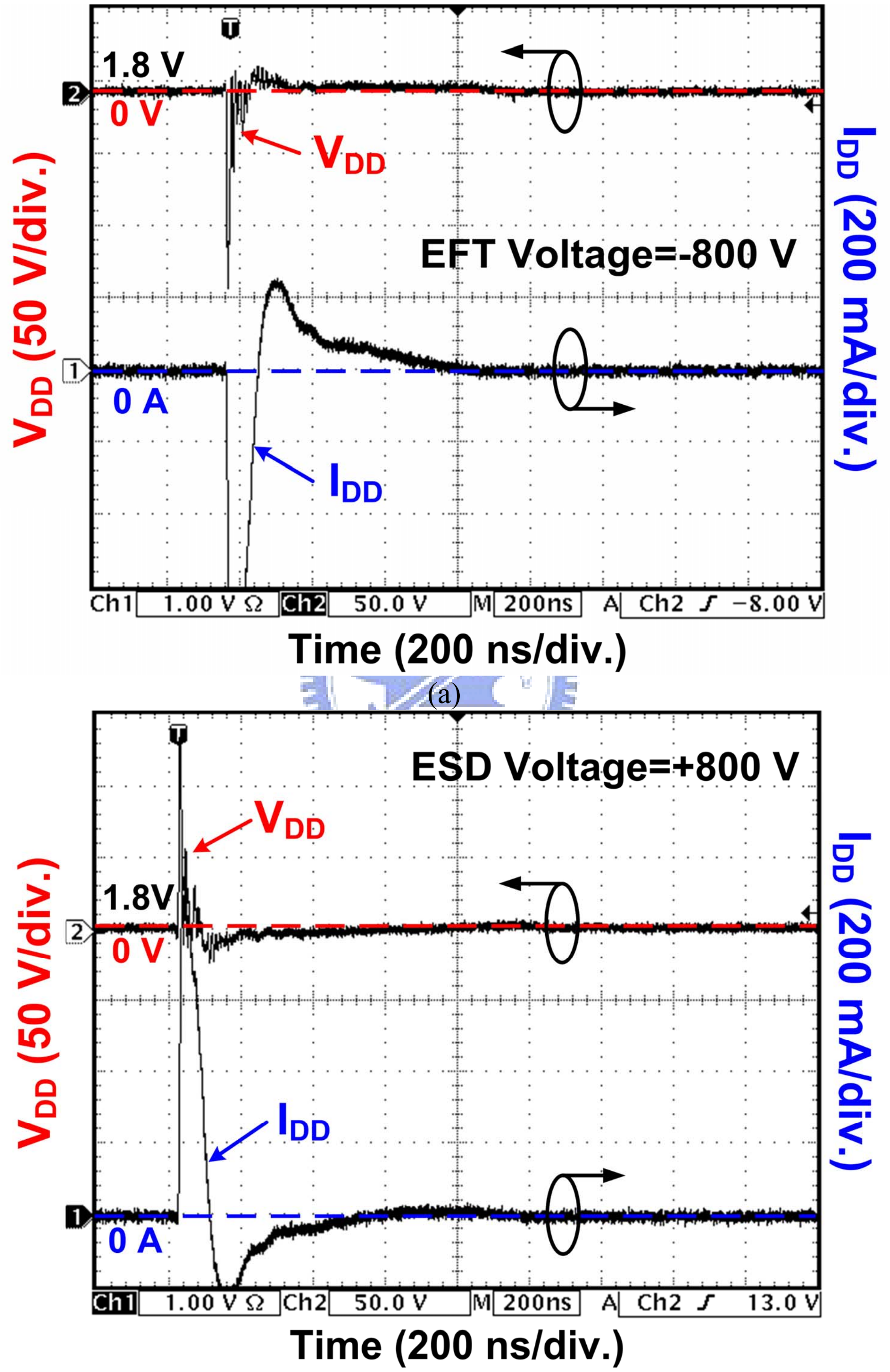
(b)

Fig. 2.23 Measured V_{DD} and I_{DD} waveforms on the proposed power-rail ESD clamp circuit with NMOS reset function under system-level ESD test with ESD voltage of (a) -10 kV, and (b) +10 kV. No latchup-like failure occurs in this system-level ESD test.

2.4.3.4. EFT Tests

The measured V_{DD} and I_{DD} responses on the proposed power-rail ESD clamp circuit under EFT tests with EFT voltages of -800 V and +800 V are shown in Figs. 2.24(a) and 2.24

(b), respectively. With a negative (positive) EFT voltage of -800 V (+800 V), the latchup-like failure does not occur in Fig. 2.24 (a) (Fig. 2.24 (b)) because the I_{DD} is not significantly increased and V_{DD} is not pulled down.



(a)

(b)

Fig. 2.24 Measured V_{DD} and I_{DD} waveforms on the proposed power-rail ESD clamp circuit under EFT test with EFT voltage of (a) -800 V, and (b) +800 V. No latchup-like failure occurs in this EFT test.

The susceptibility of the proposed power-rail ESD clamp circuit with NMOS reset function and the original power-rail ESD clamp circuit with NMOS+PMOS feedback against EFT test is compared in Table 2.6. For the proposed power-rail ESD clamp circuit, latchup-like failure does not occur.

Table 2.6
Comparison on Susceptibility Between Proposed Power-Rail ESD Clamp Circuit with NMOS Reset Function and the Original Power-Rail ESD Clamp Circuit With NMOS+PMOS Feedback Against EFT Tests

Power-Rail ESD Clamp Circuits	**Positive EFT Voltage**	**Negative EFT Voltage**
With NMOS+PMOS Feedback and NMOS Reset Function	**Under +200 V**	**Under -200 V**
With NMOS+PMOS Feedback	**Over +800 V**	**Over -800 V**

2.4.3.5. Chip-Level ESD Robustness

The chip-level ESD robustness (HBM and CDM) and layout area of the five different power-rail ESD clamp circuits integrated in this work are listed in Table 2.7. In order to provide a low impedance path between V_{DD} and V_{SS} power lines to efficiently discharge ESD current under chip-level ESD stresses conditions, the ESD-clamping NMOS has been drawn with a large device dimension (W/L=2000 μm/0.18 μm). Therefore, the layout area of five different power-rail ESD clamp circuits is dominated by the ESD-clamping NMOS. ESD-transient detection circuits only occupy smaller part in the whole layout area, as compared with the layout area of ESD-clamping NMOS. The proposed power-rail ESD clamp circuit with NMOS reset function and the aforementioned four different power-rail ESD clamp circuits can pass HBM ESD stress of over ±8 kV and CDM ESD stress of over ±1 kV.

CDM test in this work was carried out according to ESDA CDM test standard and the package type of test chip is 40-pin side braze package. Five different power-rail ESD clamp circuits are all included in a test chip with separated V_{DD} and V_{SS} pins, where the die size of test chip is 1500 × 1500 μm^2. During CDM ESD test on the test chip with different power-rail ESD clamp circuits, the direct charging method in the ESDA CDM test standard was used. The ±1 kV ESD voltages are directly charged into the V_{SS} pin that is connected with the p-type substrate of the test chip, and then the corresponding separated V_{DD} pin of the selected power-rail ESD clamp circuit is touched by external ground. After CDM test with ESD voltage of ±1 kV, the leakage current of power-rail ESD clamp circuits under 1.8-V bias was re-checked to be within 20% variation of its initial value. CDM ESD characterization is highly dependent on the package type, die size, and the adopted ESD test method. A chip with large parasitic capacitance from the package or from the large die size often has a lower CDM ESD robustness.

Table 2.7
Comparison on HBM Level, CDM Level, and Layout Area among Five Different Power-Rail ESD Clamp Circuits in a 0.18-μm CMOS Process

Power-Rail ESD Clamp Circuits	HBM ESD Level	CDM ESD Level	Layout Area	
			ESD-Clamping NMOS	ESD-Transient Detection Circuit
Typical RC-Based Detection	Over ±8 kV	Over ±1 kV	95 μm x 80 μm	35 μm x 80 μm
With PMOS Feedback	Over ±8 kV	Over ±1 kV	95 μm x 80 μm	40 μm x 80 μm
With NMOS+PMOS Feedback	Over ±8 kV	Over ±1 kV	95 μm x 80 μm	40 μm x 80 μm
With Cascaded PMOS Feedback	Over ±8 kV	Over ±1 kV	95 μm x 80 μm	40 μm x 80 μm
With NMOS+PMOS Feedback and NMOS Reset Function	Over ±8 kV	Over ±1 kV	95 μm x 80 μm	40 μm x 80 μm

CDM test in this work was carried out according to ESDA CDM test standard and the package type of test chip is 40-pin side braze package. Five different power-rail ESD clamp circuits are all included in a test chip with separated V_{DD} and V_{SS} pins, where the die size of test chip is 1500 × 1500 μm^2. During CDM ESD test on the test chip with different power-rail ESD clamp circuits, the direct charging method in the ESDA CDM test standard was used. The ±1 kV ESD voltages are directly charged into the V_{SS} pin that is connected with the p-type substrate of the test chip, and then the corresponding separated V_{DD} pin of the selected power-rail ESD clamp circuit is touched by external ground. After CDM test with ESD voltage of ±1 kV, the leakage current of power-rail ESD clamp circuits under 1.8-V bias was re-checked to be within 20% variation of its initial value. CDM ESD characterization is highly dependent on the package type, die size, and the adopted ESD test method. A chip with large parasitic capacitance from the package or from the large die size often has a lower CDM ESD robustness.

2.5. Conclusion

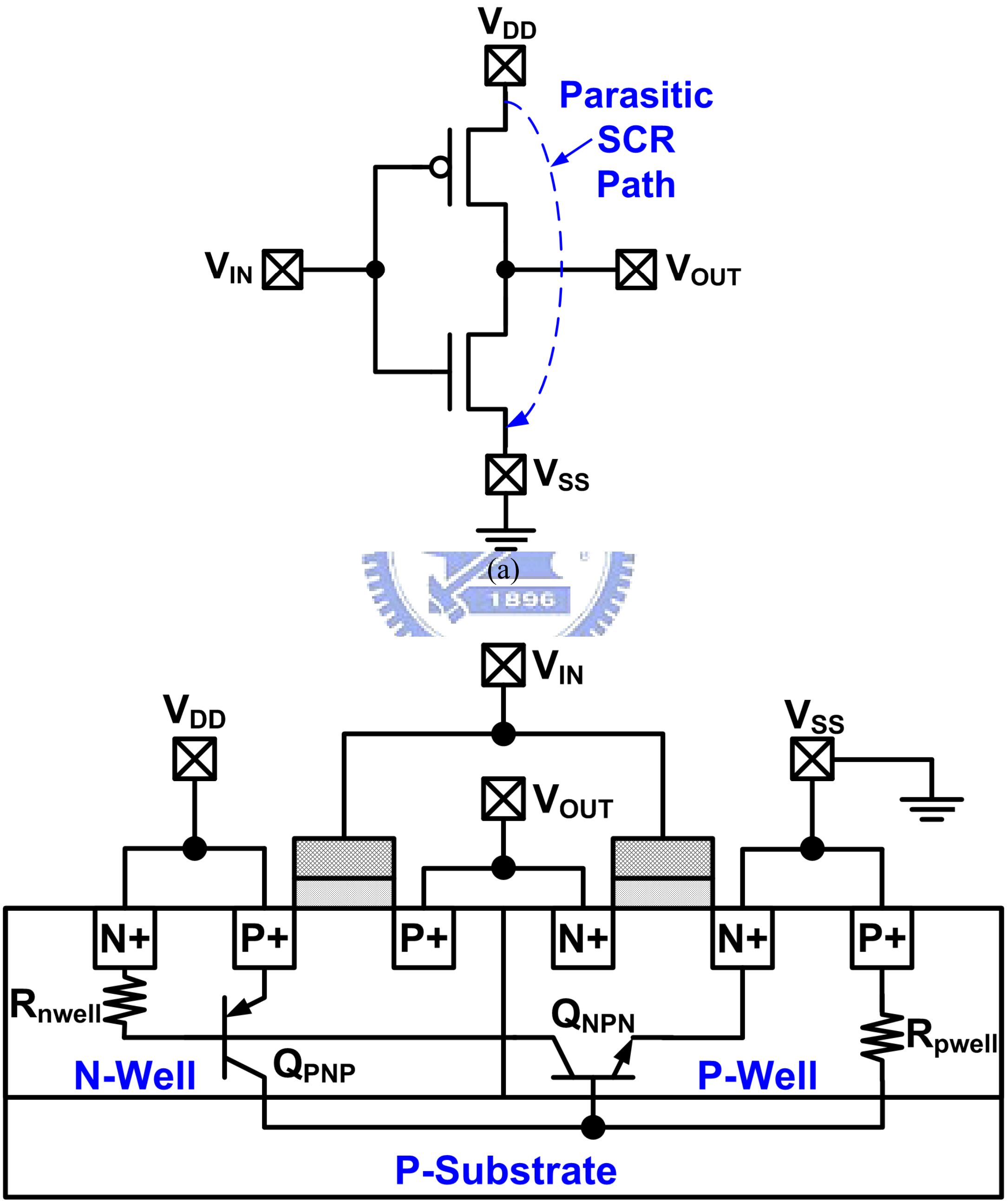
Some of advanced on-chip power-rail ESD clamp circuits with feedback loop have been found to suffer the latchup-like failure after system-level ESD tests. A modified design on the power-rail ESD clamp circuit with NMOS+PMOS feedback, by using NMOS reset function to turn off the ESD-clamping NMOS after system-level ESD tests, has been successfully verified in a 0.18-µm CMOS process. The proposed power-rail ESD clamp circuit with NMOS reset function can sustain the system-level ESD stress of over ±10 kV without causing latchup-like failure after system-level ESD tests. The proposed power-rail ESD clamp circuit has the advantages of smaller RC area, high ESD robustness, and no latchup-like failure, which is much suitable for CMOS ICs in system applications.

Chapter 3

Transient-Induced Latchup in CMOS Integrated Circuits under EFT Tests

3.1. Background

Transient-induced latchup (TLU) has been a primary reliability issue in complementary-metal-oxide-semiconductor (CMOS) integrated circuit (IC) products [51]-[77]. This TLU tendency is caused by several factors. First, aggressive scaling of both device feature size, as well as the reduced clearance between p-channel metal-oxide-semiconductor (PMOS) and n-channel metal-oxide-semiconductor (NMOS) transistors, leads the inevitable parasitic silicon controlled rectifier (SCR) in CMOS ICs to exhibit poor latchup immunity. The typical circuit structure and the device cross-sectional view of a CMOS inverter in digital ICs are shown in Figs. 3.1(a) and Fig. 3.1(b), respectively. The SCR structure in the inverter is formed by the parasitic PNPN (P+/N-well/P-well/N+) structure between V_{DD} and V_{SS} of CMOS circuits. The equivalent circuit of the SCR structure is formed by a vertical PNP bipolar junction transistor (BJT) (Q_{PNP}) coupled with a lateral NPN BJT (Q_{NPN}). When one of the BJTs is turned on, the mechanism of positive feedback regeneration in the SCR structure will be initiated [52]. If the product of beta gains of these two BJTs can be kept greater than one, the SCR structure will hold in a stable latching state. When the parasitic SCR in CMOS ICs is triggered to cause latchup, it generates a low-impedance path from V_{DD} to V_{SS} with a high current that often burns out the chip. It has been also reported that the latchup triggering current does not significantly increase with the scaling rule of CMOS processes while the power supply voltage keeps decreasing. Second, there are much more complicated implementations of CMOS ICs, such as mixed-signal, multiple power supplies, radio frequency (RF), system-on-chip (SOC), etc. The environment where these CMOS devices are located will suffer from considerable electrical transient disturbances coming from both interior and exterior of CMOS ICs. Thus, such electrical transients often unpredictably exist on power, ground, or input/output (I/O) pins of CMOS ICs, which induces TLU much more often than before. Third, more and more ICs are rather susceptible to TLU under the strict requirements of reliability test standards, such as the electrical fast transient (EFT) test standard of IEC 61000-4-4 [78]-[80]. The I/O, data, and control ports of electronic products must sustain the EFT peak voltage of ±2 kV to achieve the immunity requirement of “level 4” in the IEC 61000-4-4 test standard. It has been reported that some CMOS ICs are very susceptible to electrical transients, even though they have passed the component-level ESD specifications such as human-body-model (HBM) of ±2 kV, machine-model (MM) of ±200 V, and charged-device-model (CDM) of ±1 kV.



(a)

(b)

Fig. 3.1 (a) Circuit structure, and (b) device cross-sectional view of a CMOS inverter.

Figs. 3.2(a) and 3.2(b) show the emission microscope (EMMI) photographs of EFT-induced TLU failure in a 0.5-µm CMOS IC product with the power-supply voltage of 5V. The EMMI is a widely used technique for wafer level reliability and yield analysis for semiconductor devices. In general, this analysis is performed by collecting the recombination radiation emitted by recombination of electrons and holes. For NMOS transistors under high electric fields and currents, the radiative intraband transitions of photons are the predominant emission mechanism in EMMI analysis. Fig. 3.2(a) shows the hot spots of latchup locations in the test chip after EFT test, and Fig. 3.2(b) show the corresponding zoomed-in latchup location, which is located across the boundary between NMOS and PMOS transistors in a digital logic block. From the test results shown in Figs. 3.2(a) and 3.2(b), under EFT tests, the parasitic SCR structure located across the boundary between NMOS and PMOS transistors can be initiated to cause latchup event. Due to mechanism of positive feedback regeneration, the SCR structure can provide a low-impedance path to conduct high current from V_{DD} to ground to burn out the IC. This result has demonstrated that the EFT test can trigger on the parasitic SCR structure to cause TLU event in real IC products. In this work, an SCR structure is designed to clarify the TLU event and to investigate the mechanism under EFT tests with positive and or negative EFT voltages.

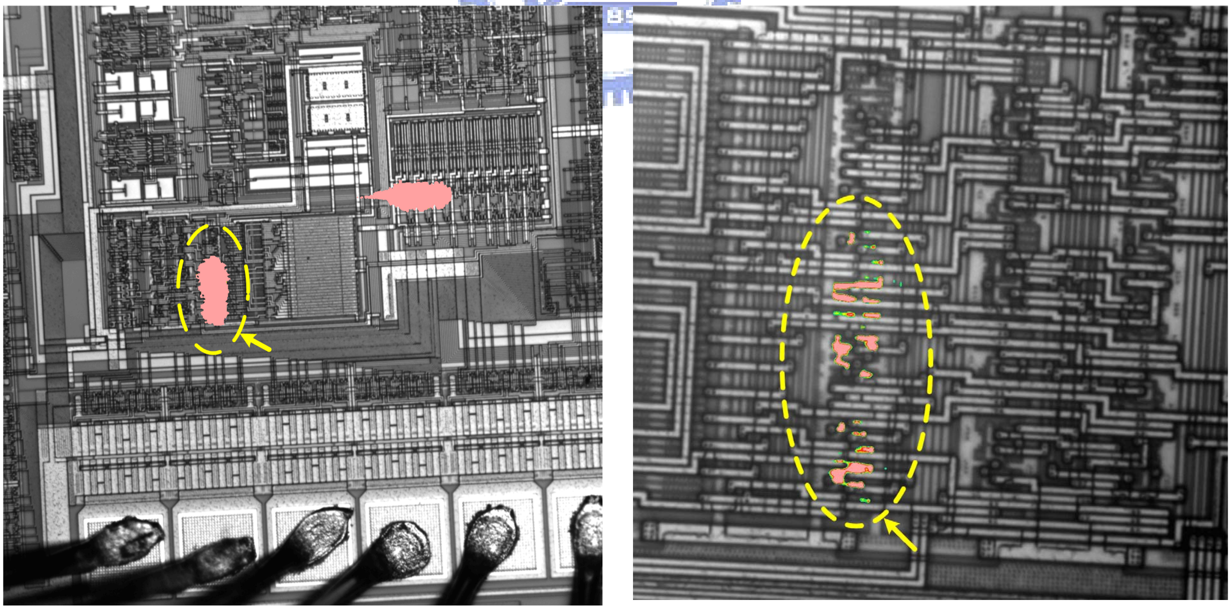

(a) (b)

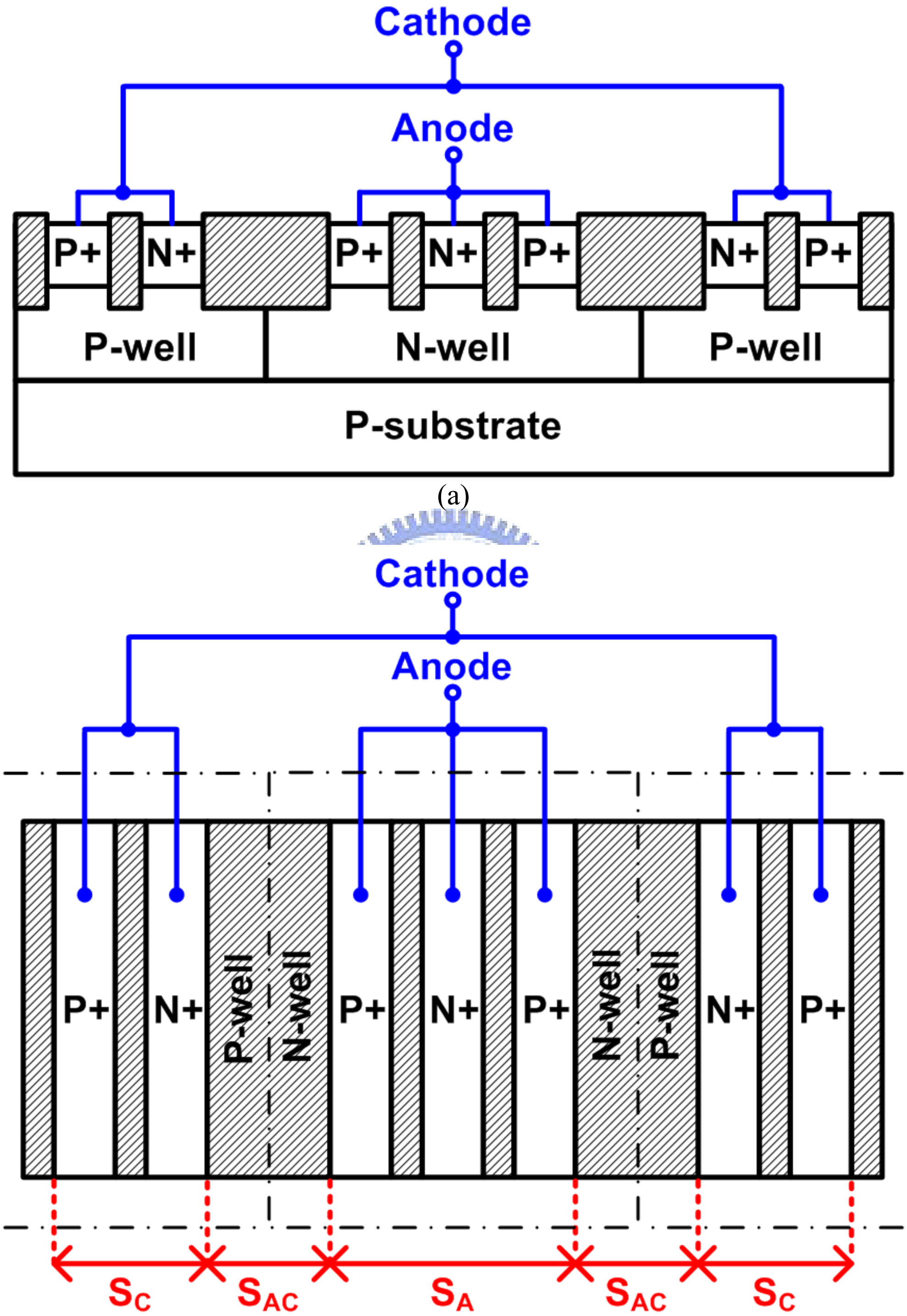
Fig. 3.2. Emission microscope (EMMI) photographs of EFT-induced TLU event in a 0.5-µm CMOS IC product with power-supply voltage of 5V. (a) Hot spots of latchup locations in the chip after EFT test, and (b) the corresponding zoomed-in latchup location, which is located across the boundary between NMOS and PMOS transistors in a digital logic block.

It has been clarified that the “sweep-back current” [26] caused by the electrical transients on power (ground) pins of CMOS ICs is the major cause of TLU. TLU can be initiated by the sweep-back current when an electrical transient on V_{DD} increases from its negative peak voltage to a positive voltage. Such a sweep-back current is strongly dependent on the parameters of the electrical transient voltage waveform, such as transient peak voltage, damping frequency, and duration time [27]. In real situations, however, all these parameters depend on the set voltage of EFT generator, metal traces of board-level (chip-level) layout, board-level noise filter network, etc. To suppress the occurrence of TLU, a board-level noise filter could be a solution to enhance the TLU immunity of CMOS ICs, because the board-level noise filter network between the noise sources and CMOS ICs can decouple, bypass, or absorb noise voltage (energy) [30]. Thus, the TLU immunity of CMOS ICs strongly depends on the board-level noise filter network. However, how the board-level noise filter network can enhance the TLU immunity of CMOS ICs against the EFT tests was not investigated so far.

In this work, TLU induced in CMOS ICs by EFT tests is clearly studied [81]. Another purpose of this work is to investigate a high efficiency board-level noise filter network for TLU prevention under EFT tests. Different types of noise filter networks are evaluated to find their improvements to TLU immunity, including capacitor filter, ferrite bead, transient voltage suppressor (TVS), and several high-order noise filters such as LC-like (2nd-order) and π-section (3rd-order) filters. All the experimental results have been verified with the SCR test structure fabricated in a 0.18-μm CMOS process.

3.2. SCR Test Structure

The SCR structure is used as the test structure for TLU measurements under EFT tests because the occurrence of latchup is due to the inherent SCR in bulk CMOS ICs. The device cross-sectional view and layout top view of the SCR structure are sketched in Figs. 3.3(a) and 3.3(b), respectively. The anode of the SCR is connected to the N+ and P+ diffusions in N-well, whereas the cathode of the SCR is connected to the N+ and P+ diffusions in P-well. The geometrical parameters such as S_A, S_C, and S_{AC} represent the distances between the P+ diffusions in N-well, P+ and N+ diffusions in P-well, and P+ diffusion in N-well and N+ diffusion in P-well, respectively. In the SCR structure, the N+ and P+ diffusions in N-well are connected to V_{DD}, whereas the N+ and P+ diffusions in P-well are connected to ground. Once latchup occurs through the SCR structure, a huge current will be generated by the mechanism of positive-feedback regeneration [6]. As a result, the huge current will conduct through the low-impedance path from V_{DD} to ground, and further probably burn out the chip due to excess heat.



(a)

(b)

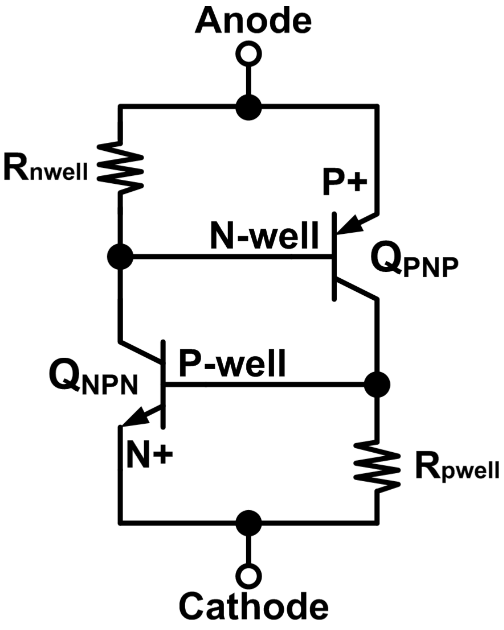
Fig. 3.3 (a) Device cross-sectional view, and (b) layout top view, of the SCR test structure for TLU measurements.

In this work, to investigate the occurrence of TLU under EFT tests, the SCR structure with the layout parameters of S_A=29.12 μm, S_C=14.25 μm, and S_{AC}=4 μm in a 0.18-μm CMOS process with 3.3-V devices is used for the TLU measurements.

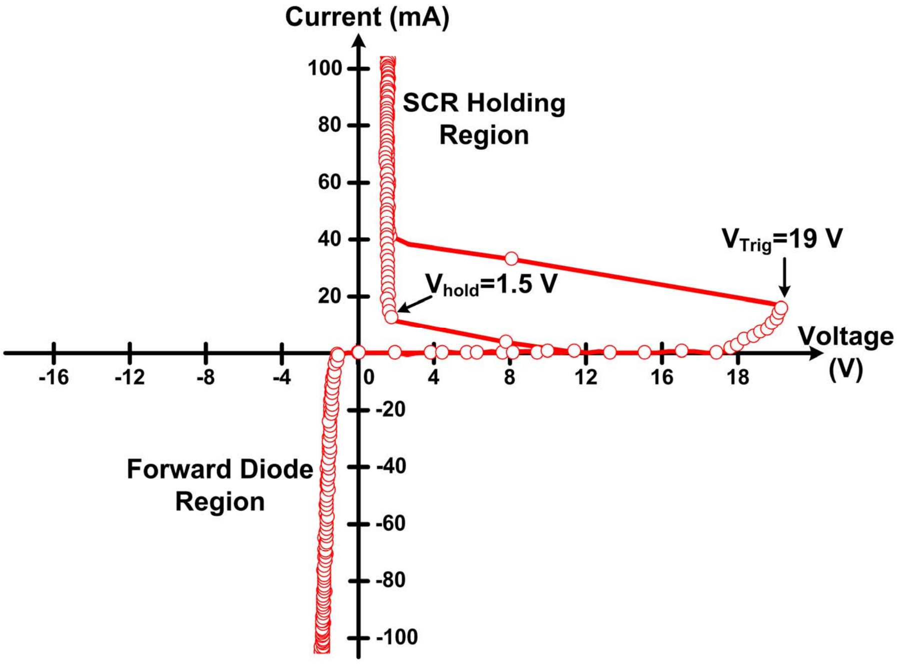
The equivalent circuit schematic of the SCR structure is shown in Fig. 3.4(a). The SCR structure consists of a lateral NPN BJT (Q_{NPN}) and a vertical PNP BJT (Q_{PNP}) to form a 2-terminal/4-layer PNPN (P+/N-well/P-well/N+) structure. The switching voltage of the SCR device is dominated by the avalanche breakdown voltage of the N-well/P-well junction, which could be as high as ~19 V in a 0.18-μm CMOS process. When the positive voltage applied to the anode of the SCR is greater than the breakdown voltage of the N-well/P-well junction with its cathode relatively grounded, the hole and electron currents will be generated through the avalanche breakdown mechanism. The hole current will flow through the P-well to the grounded P+ diffusion, whereas the electron current will flow through the N-well to N+ diffusion connected to the anode of SCR. As long as the voltage drop across the P-well resistor (R_{pwell}) (N-well resistor (R_{nwell})) is greater than the cut-in voltage of the PN junction, the Q_{NPN} (Q_{PNP}) transistor will be turned on to inject the electron (hole) current to further bias the Q_{PNP} (Q_{NPN}) transistor, which initiates the SCR latching action. Finally, the SCR will be fully triggered into its latching state with the positive-feedback regenerative mechanism.

In CMOS ICs, the P+ anode (source of PMOS) and the N+ well contact are connected to V_{DD}, whereas the N+ cathode (source of NMOS) and the P+ well contact are connected to ground. Once latchup occurs inside the SCR structure, huge current will be generated through a mechanism of positive-feedback regeneration. As a result, the huge current will conduct through a low-impedance path from V_{DD} to ground, and further probably burn out the chip due to excess heat.

The dc I-V characteristic of the fabricated SCR device is shown in Fig. 3.4(b). Once the SCR is triggered on, the required holding current to keep the NPN and PNP transistor on can be generated through the positive-feedback latchup mechanism without involving the avalanche breakdown again. Therefore, the SCR has a lower holding voltage (V_{hold}) of typically ~1.5 V in this 0.18-μm CMOS process. If the negative voltage is applied on the anode terminal of the SCR, the parasitic diode (N-well/P-well junction) inherent in the SCR structure will be forward biased to clamp the negative voltage at the cut-in voltage of diode. Whatever, the energy is, positive and negative, so the SCR device can sustain the highest ESD robustness within a smaller layout area in CMOS ICs.



(a)



(b)

Fig. 3.4 (a) Equivalent circuit schematic of SCR device. (b) I-V characteristics of SCR device under positive and negative biases.

3.3. Experimental Measurements

The TLU measurement setup under EFT tests is sketched in Fig. 3.5. The EFT generator can generate the positive and negative transient EFT pulses on power pins of the device under test (DUT). The SCR device shown in Figs. 3.3(a) and 3.3(b) is used as the DUT where the anode (cathode) of SCR is connected to V_{DD} (ground). I_{DD} is the total current flowing into the anode of SCR. The I_{DD} current waveform is monitored by a separated current probe. The current-limiting resistance (5 Ω) is used to protect the DUT from electrical-over-stress (EOS) damage during a high-current (low-impedance) latchup state. With both positive and negative EFT voltages, the measured V_{DD} (I_{DD}) transient response is recorded through the voltage (current) probe on the oscilloscope. This clearly indicates whether TLU occurs (I_{DD} significantly increases) during the TLU tests with EFT pulses.

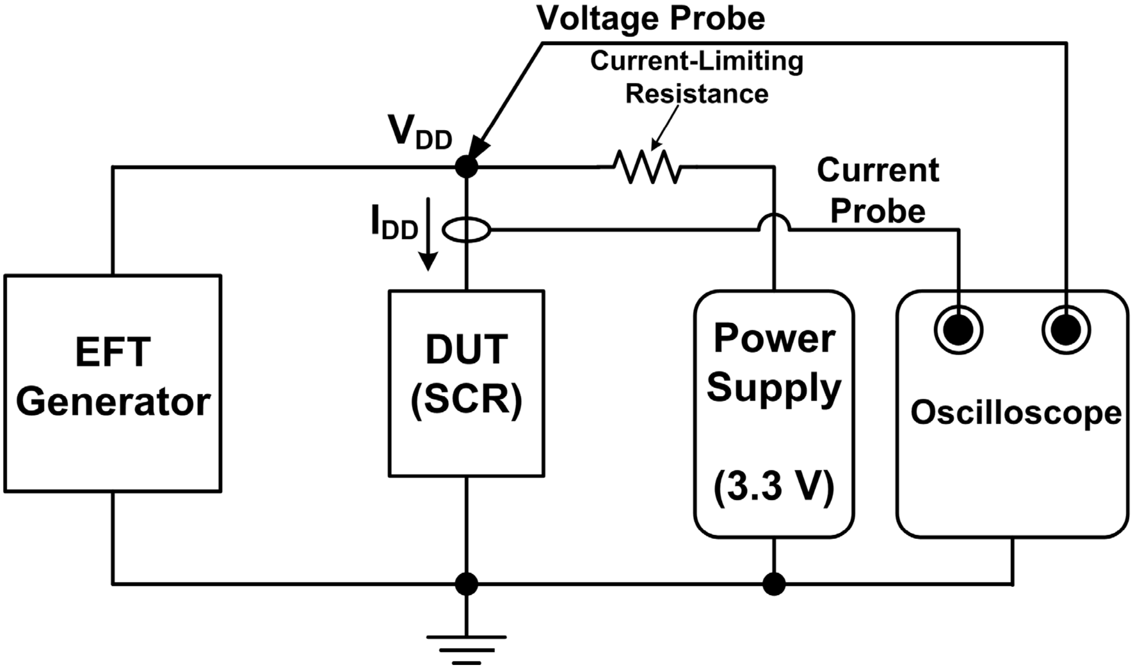


Fig. 3.5 Measurement setup for TLU under EFT tests.

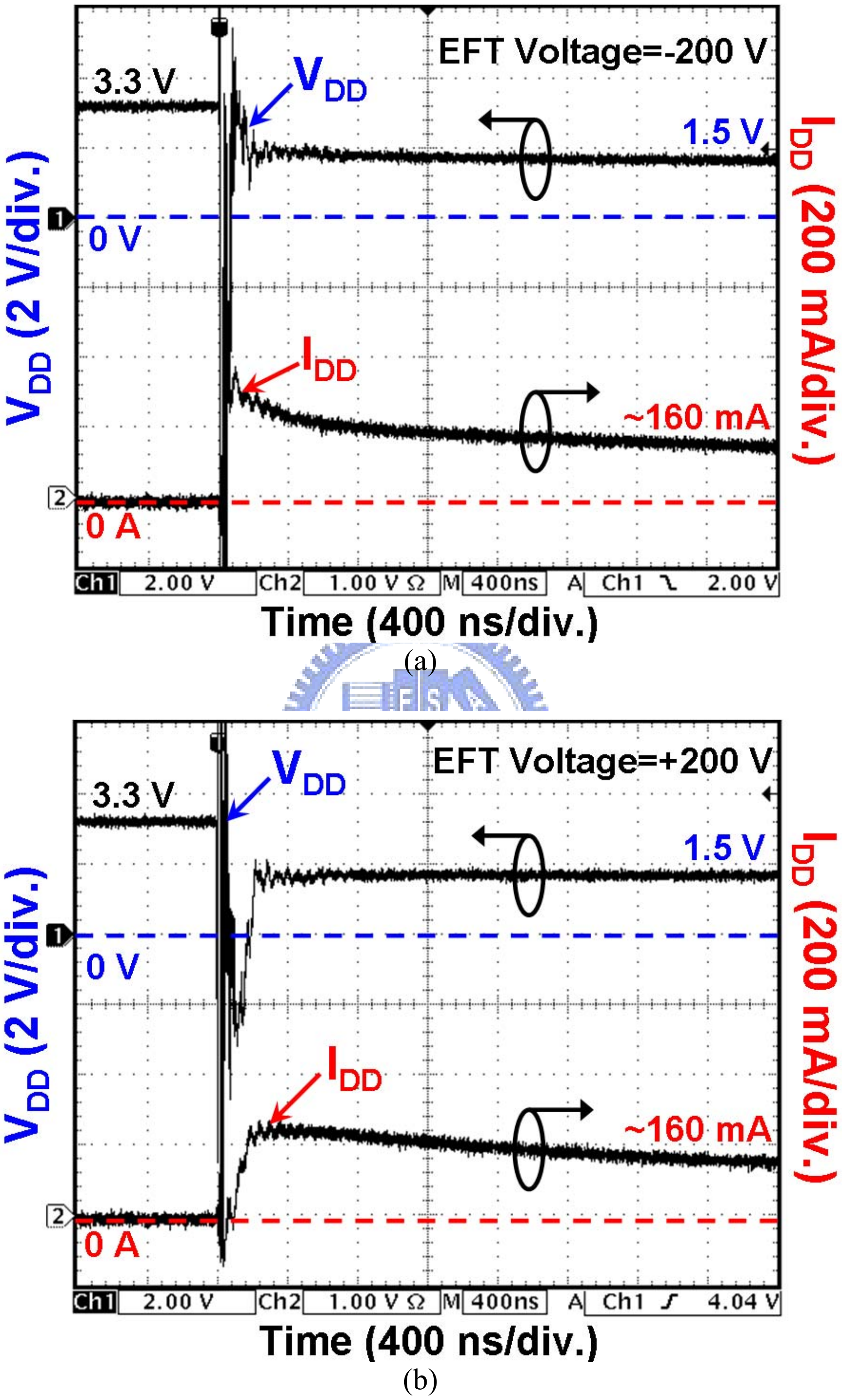
3.3.1. TLU Tests with EFT Generator

With a negative EFT voltage of -200 V, the measured V_{DD} and I_{DD} transient responses on the SCR structure are shown in Fig. 3.6(a). In the beginning with normal power supply (V_{DD}=3.3 V, V_{SS}=0 V), the SCR operates in the off state and V_{DD} is kept at the normal operating voltage (+3.3 V). Within this duration before EFT pulse applied, the N-well/P-well junction is in a normal reverse-biased state, and I_{DD} only comes from the negligible leakage current in the reverse junction. When the EFT pulse is applied with a negative EFT voltage, V_{DD} begins to decrease rapidly from +3.3 V and will eventually reach the negative peak voltage. Within this duration, the N-well/P-well junction becomes forward biased when V_{DD}

drops below 0V. Thus, the forward-biased N-well/P-well junction can generate the forward current. When V_{DD} increases from the negative peak voltage back to its normal operating voltage (+3.3 V), the N-well/P-well junction will rapidly change from the forward-biased state to the reverse-biased state. Meanwhile, inside the N-well (P-well) region, a large number of stored minority holes (electrons) offered by the forward peak current will be instantaneously “swept-back” to the P-well (N-well) region where they originally come from. Therefore, such “sweep-back” current, I_{Sb}, will produce a localized voltage drop and flow through the parasitic P-well or N-well resistance. Once this localized voltage drop approaches the cut-in voltage of the PN junction, the emitter-base junction of either the vertical PNP or the lateral NPN BJT in the SCR structure will be forward biased to further trigger on latchup. Afterwards, I_{DD} will greatly increase while V_{DD} returns to above 0V, which indicates the occurrence of latchup. After EFT tests, V_{DD} will eventually be pulled down to the latchup holding voltage (+1.5 V), as shown in Fig. 3.6(a). Finally, the V_{DD} (I_{DD}) waveform is locked at a low voltage (high current) latchup state after this transition induced by the EFT pulse. From the measured results in Fig. 3.6(a), the occurrence TLU in SCR under EFT test had been observed because the huge I_{DD} of ~160 mA can be found and V_{DD} finally pulls down to the holding voltage (+1.5 V). TLU will be triggered on due to large enough I_{Sb} while V_{DD} returns from negative peak voltage to the positive voltage.

With a positive EFT voltage of +200 V, the measured V_{DD} and I_{DD} transient responses on the SCR structure are shown in Fig. 3.6(b). Unlike the V_{DD} waveform with a negative EFT voltage shown in Fig. 3.6(a), where V_{DD} begins decreasing rapidly, V_{DD} starts to increase and reaches a positive peak voltage. Within this duration, the N-well/P-well junction is always reverse biased within the SCR. Afterwards, V_{DD} decreases from the positive peak voltage to the negative peak voltage. Within this duration, the N-well/P-well junction gradually changes from the reverse-biased state to the forward-biased state, while more minority electrons (holes) are injected into the P-well (N-well) region. When V_{DD} returns from the negative peak voltage to the positive voltage, these minority electrons (holes) are subsequently swept back to the N-well (P-well) regions where they originally come from and finally TLU is triggered on. As a result, I_{DD} will considerably increase when V_{DD} returns from the negative peak voltage to the positive voltage. After the EFT test, TLU occurs because the huge I_{DD} of ~160 mA can be found and V_{DD} eventually pulls down to its latchup holding voltage of +1.5 V, as shown in Fig. 3.6(b).

The SCR structure in bulk CMOS processes is very susceptible to TLU under an EFT pulse as low as ±200 V. Due to such weak immunity against TLU under EFT tests, some latchup prevention methods should be provided to improve TLU immunity of CMOS ICs.



(a)

(b)

Fig. 3.6 Measured V_{DD} and I_{DD} transient waveforms on SCR test structure under EFT tests with EFT voltage of (a) -200 V, and (b) +200 V.

3.3.2. Physical Mechanism

Under the EFT test with the negative voltage pulse, it has been proved that the swept-back current, I_{Sb}, caused by the minority carrier stored within the parasitic PNPN structure of CMOS ICs is the major cause of the TLU. For the sake of simplicity, two reasonable assumptions are made. First, the N-well/P-well junction is treated as an ideal 1-D diode with step junction profile, as in the inset figure shown in Fig. 3.7. Second, the storage time of minority carriers is assumed to be negligible because I_{DD} can rapidly follow the polarity variation of V_{DD}. Therefore, from the assumptions, the stored minority holes (Q_{Stored}) inside the N-well region can be expressed as

$$Q_{Stored} = \int_{X_n}^{X_{n'}} \left[P_n(x,t)\Big|_{t=t_B} - P_n(x,t)\Big|_{t=t_A} \right] dx\,, \qquad (1)$$

where $P_{n(x,t)}$ is the hole concentration in the N-well region and t_A (t_B) is the initial (final) timing point of a specific duration when I_{Sb} exists. Q_{Stored} represents the total stored minority carriers (holes) causing I_{Sb} ($t_A \le t \le t_B$) inside the N-well region. Compared with the quasi-static latchup test, the specific duration ($t_A \le t \le t_B$) in the EFT test is much shorter than that in the quasi-static latchup test because the EFT pulse duration is only several tens of nanoseconds [19]. The rise time (fall) time for the quasi-static latchup test is much longer (~μs) than that for the EFT test. Thus, once these Q_{Stored} are swept back to the regions where they come from, the averaged I_{Sb} can be expressed as

$$I_{Ave} \equiv \frac{Q_{Stored}}{t_B - t_A}. \qquad (2)$$

In both TLU and quasi-static latchup conditions, if the initial ($t=t_A$) and the final ($t=t_B$) voltages during $t_A \le t \le t_B$ are equal (i.e., with the same amount Q_{Stored}), the averaged I_{Sb} in the TLU case will be about $10^3 \sim 10^6$ times larger than that in the quasi-static latchup case. The averaged I_{Sb} is rather small and hard to trigger on latchup in the quasi-static latchup test. Therefore, the averaged I_{Sb} is large enough to easily trigger on latchup in the SCR structure under the EFT test.

The physical mechanism of TLU under the EFT tests can be well proved by comparing the experimental results. As shown in Figs. 3.6(a) and 3.6(b), large enough I_{Sb} caused by the instantaneously forward-biased N-well/P-substrate junction can easily trigger on TLU under EFT tests with positive and negative EFT voltages.

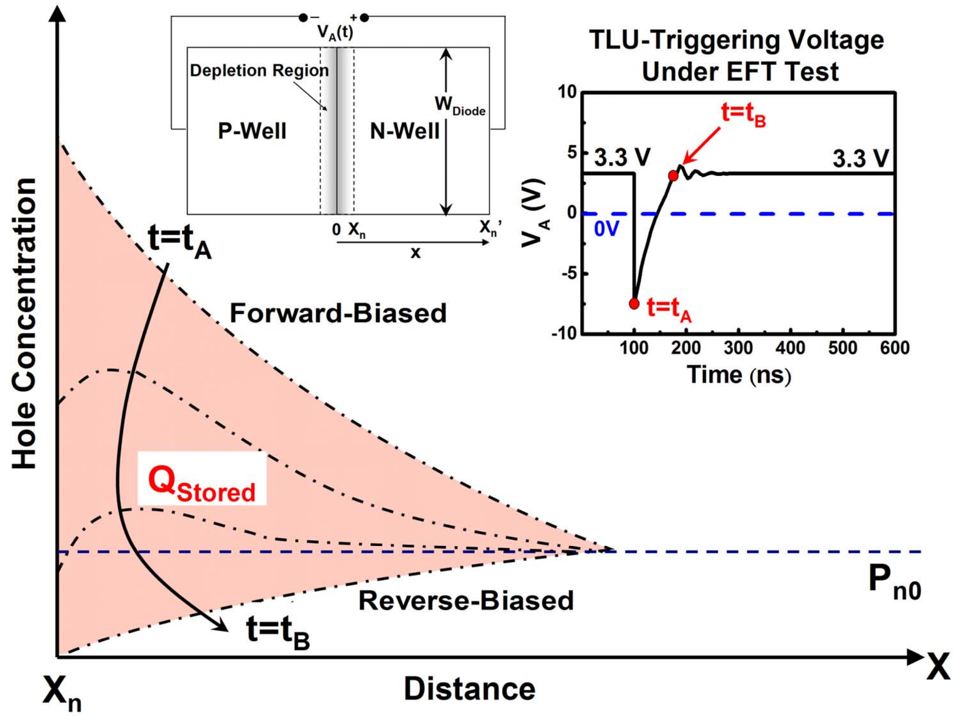


Fig. 3.7 The total stored minority carriers, Q_{Stored}, causing ISb ($t_A \leq t \leq t_B$) inside the N-well region. The inset figure is an ideal 1-D diode used for deriving the 1-D analytical model of the averaged I_{Sb} ($\equiv I_{Ave}$).

3.4. Evaluation on Board-Level Noise Filters to Suppress Latchup under EFT Tests

Different types of noise filter networks are investigated to find their effectiveness for improving the TLU immunity of an SCR structure against EFT tests, including: (1) capacitor filter, (2) LC-like filter, (3) π-section filter, (4) ferrite bead, (5) transient voltage suppressor (TVS), and (6) hybrid type filters based on the combinations with TVS and ferrite bead. In this measurement, the SCR structure for all test cases has the same layout parameters of S_A=29.12 μm, S_C=14.25 μm, and S_{AC}=4 μm.

The modified TLU measurement setup under EFT tests with noise filter network is sketched in Fig. 3.8. Noise filter networks between the EFT generator and the DUT are used to decouple, bypass, or absorb electrical transient voltage (energy) produced by the EFT generator. The DUT in this work is the SCR structure shown in Figs. 3.6(a) and 3.6(b). The anode of the SCR is connected together to V_{DD}, whereas the cathode of the SCR is connected together to ground. I_{DD} is the total current flowing into the anode of the SCR.

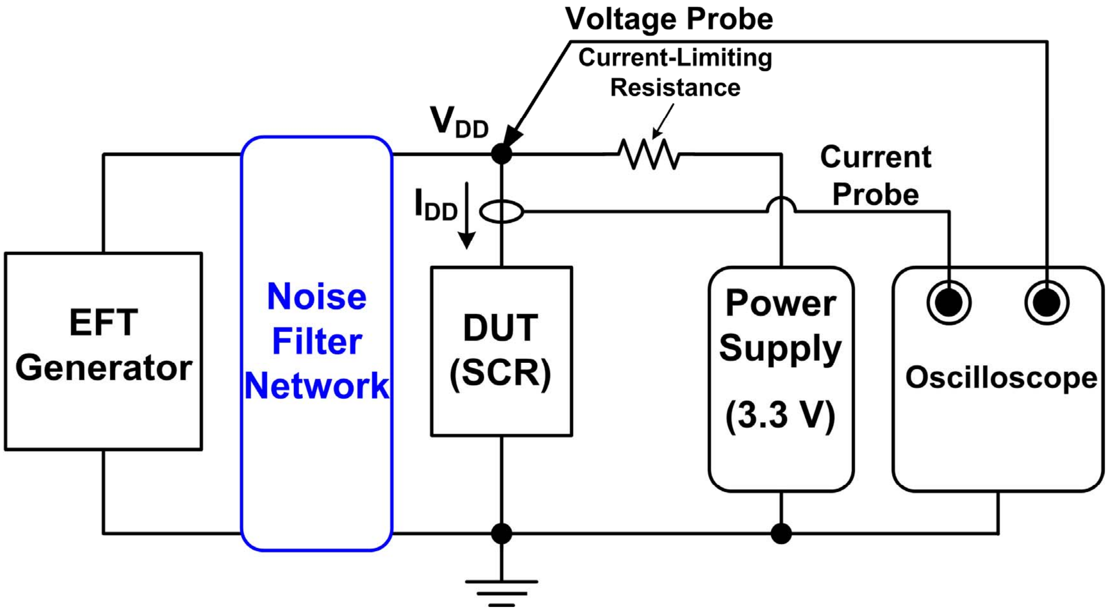


Fig. 3.8 Measurement setup for TLU combined with noise filter network under EFT tests.

3.4.1. Capacitor Filter, LC-Like Filter, and π-Section Filter

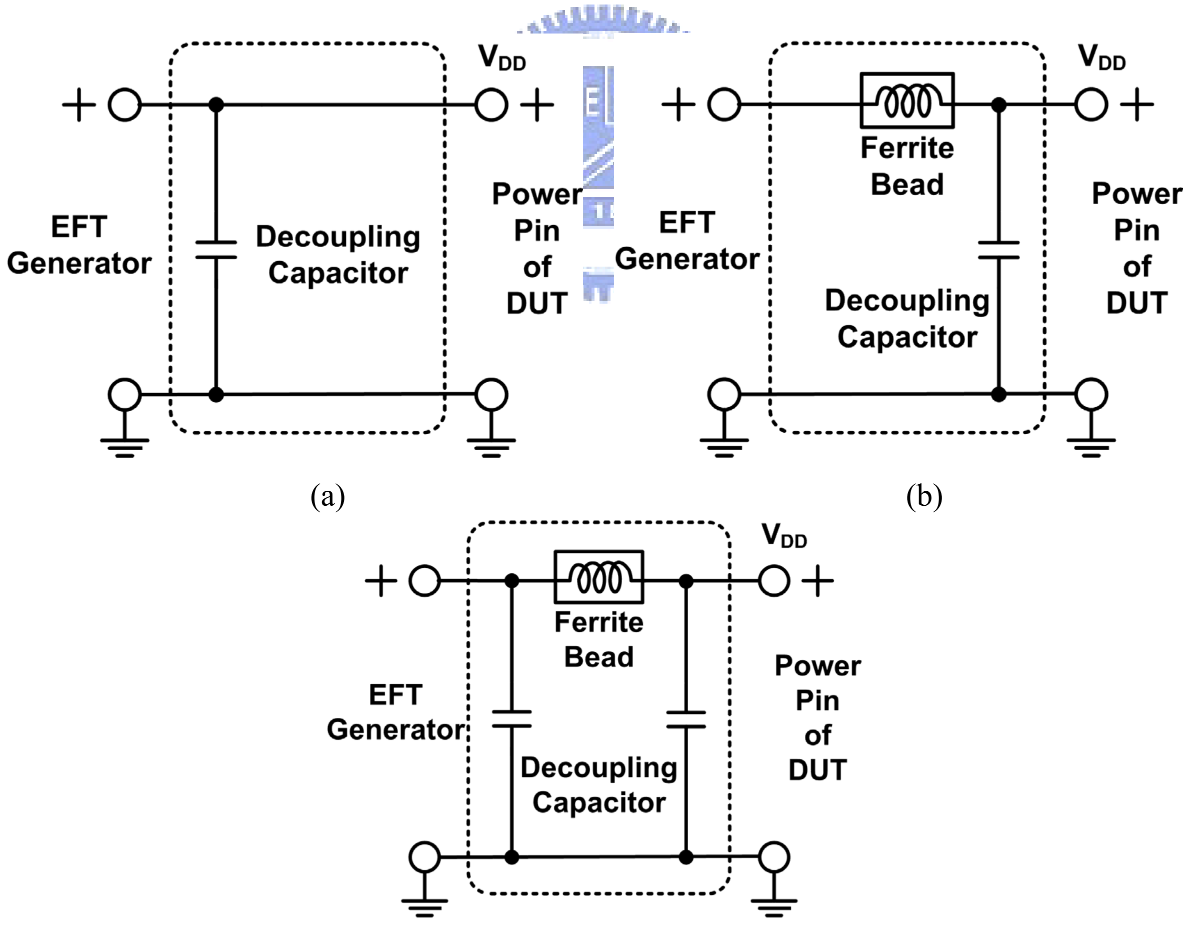
Three types of noise filter networks: capacitor filter, LC-like filter, and π-section filter are depicted in Figs. 3.9(a), 3.9(b), and 3.9(c), respectively. Fig. 3.10 shows their improvements on both positive and negative TLU levels of the SCR structure.

The ceramic disc capacitor with advantages such as high rated working voltage (1 kV), good thermal stability, and low loss over a wide range of frequency is employed as the decoupling capacitor in the noise filter of Fig. 3.9(a). Decoupling capacitances ranging from 1 nF to 0.1 μF are used to investigate their improvements on the TLU level of the SCR structure. With the aid of the capacitor filter to reduce the electrical transient voltage on V_{DD}, the positive TLU level can be significantly enhanced from +200 V (without decoupling capacitor) to over +1000 V (with a decoupling capacitance of 0.1 μF), as shown in Fig. 3.10. Similarly, the negative TLU level can be also greatly enhanced from -200 V (without decoupling capacitor) to -800 V (with a decoupling capacitance of 0.1 μF). Thus, by choosing a decoupling capacitor with proper capacitance value, a simple 1st-order decoupling capacitor placed between V_{DD} and V_{SS} (ground) of CMOS ICs can be used to appropriately improve the TLU immunity of DUT under the EFT tests.

The ferrite bead, which is commonly used for absorbing RF energy, substitutes for an inductor as a 2nd-order LC-like filter component, as shown in Fig. 3.9(b). A resistor-type ferrite bead (part number: RH 3.5x9x0.8 with minimum impedance of 80 Ω (120 Ω) at 25 MHz (100 MHz)) is employed. Due to a higher insertion loss (2nd-order filter), such an

LC-like filter has more TLU level enhancements than the capacitor filter (1^{st}-order filter) in Fig. 3.9(a). For example, the negative TLU level can also be greatly enhanced from -200 V (without decoupling capacitor) to over -1000 V (with a decoupling capacitance of 0.1 μF). Thus, the LC-like filter can be used to achieve a higher negative TLU level.

A 3rd-order π-section filter is used to further enhance the TLU level of the SCR, as shown in Fig. 3.9(c). This π-section filter consists of a ferrite bead (the same one in Fig. 3.9(b)) and two decoupling capacitors with equal decoupling capacitance. With the highest insertion loss among the noise filter networks in Figs. 3.9(a), 3.9(b), and 3.9(c), the TLU level of the SCR can be most improved. For example, the positive TLU level can be significantly enhanced to over +1000 V (with a decoupling capacitance of 47 nF), as shown in Fig. 3.10. Similarly, the negative TLU level can also be significantly enhanced to over -1000 V (with decoupling capacitance of 47 nF). From the comprehensive measured results in Fig. 3.10, the decoupling capacitance can be optimized according to the desired TLU level and the type of board-level noise filter chosen.



(a) (b)

(c)

Fig. 3.9 Three types of noise filter network investigated for their improvements on the TLU level of the SCR. (a) Capacitor filter, (b) LC-like filter, and (c) π-section filter.

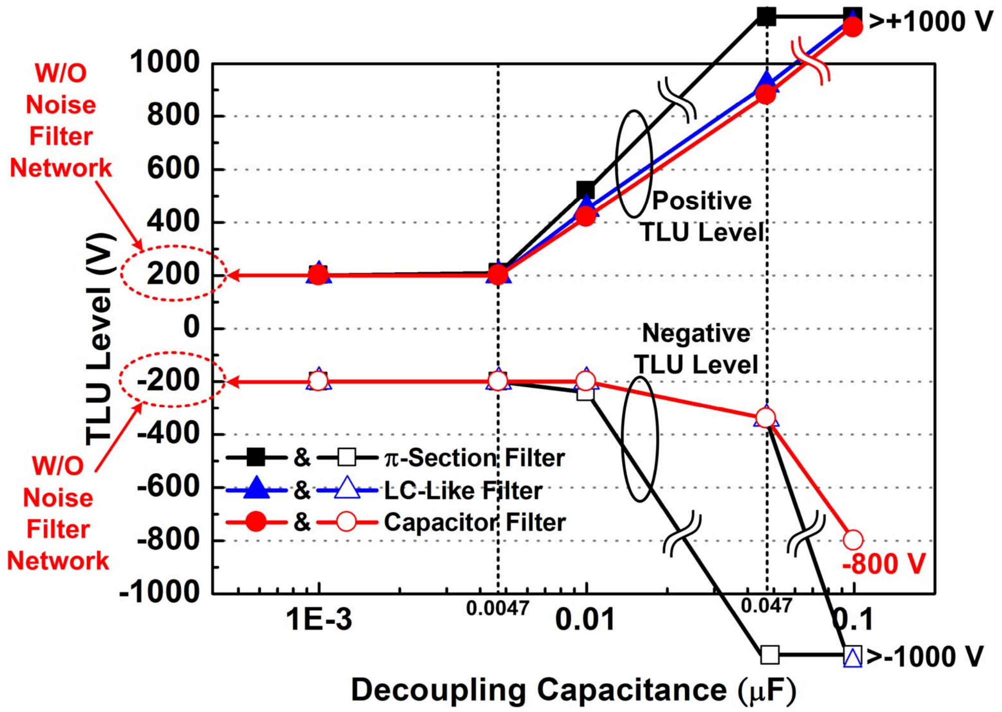


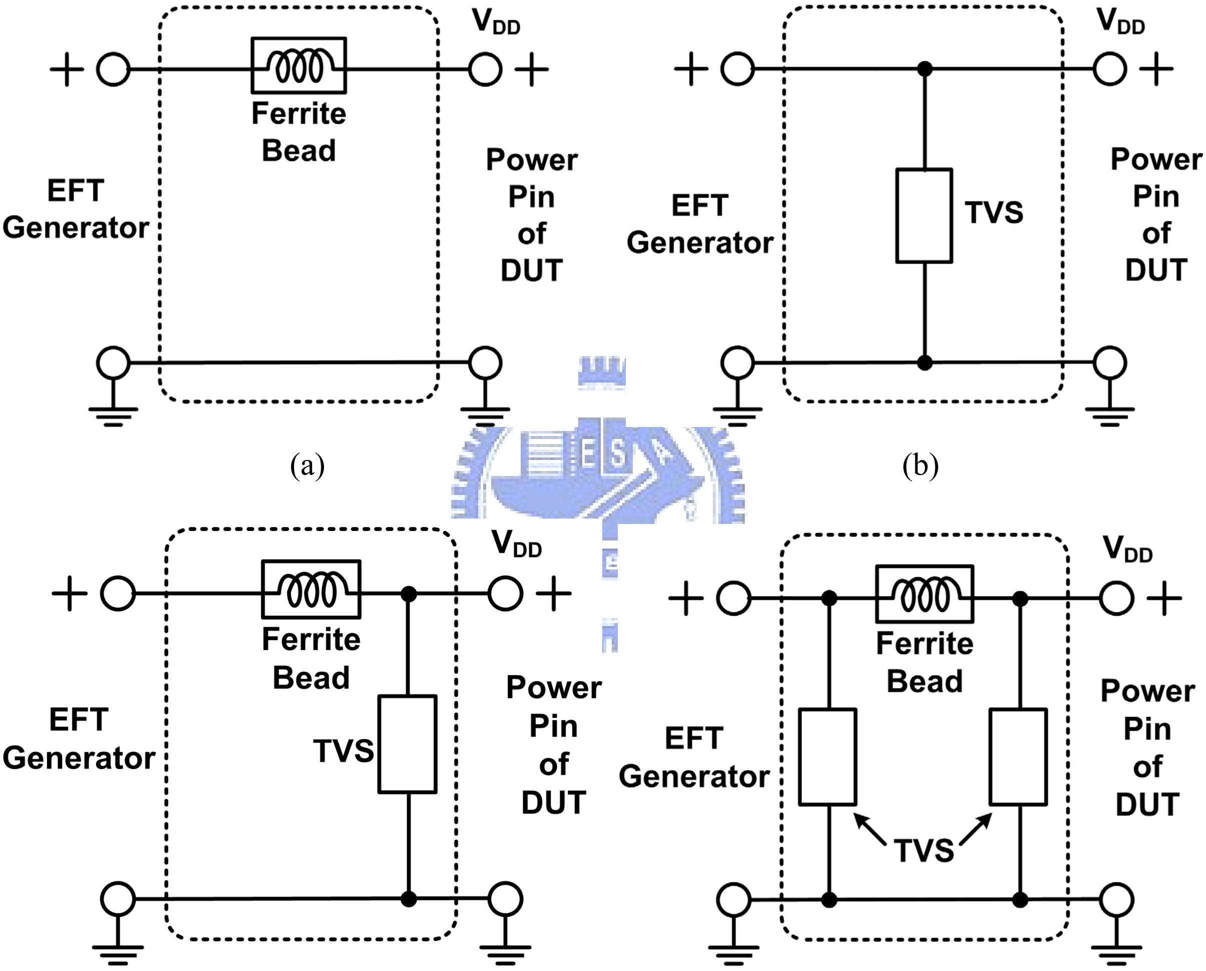
Fig. 3.10 Relations between the decoupling capacitance and the TLU level of the SCR with three types of noise filter networks: capacitor filter, LC-like filter, and π-section filter.

3.4.2. Ferrite Bead, TVS, and Hybrid Type Filters

Four other types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II are depicted in Figs. 3.11(a), 3.11(b), 3.11(c), and 3.11(d), respectively. Fig. 3.12 shows their improvements on both positive and negative TLU levels of the SCR test structure.

The ferrite bead can absorb RF energy while the noise-induced transient current flows through it. The resistor-type ferrite beads with three different minimum impedances at 25 MHz are employed in this work: 35 Ω, 50 Ω, and 80 Ω. However, a noise filter network with only ferrite bead alone does not have an improvement on the TLU level due to a lesser energy-absorbing ability at frequencies lower than 10 MHz. As shown in Fig. 3.12, the TLU level of the SCR structure will not be efficiently improved (the magnitudes of both positive and negative TLU levels are all equal to 200 V), even though the minimum impedance of the ferrite bead at 25 MHz is as high as 80 Ω.

TVS, which is commonly used to bypass/decouple the high-frequency transient noises, is also considered for its improvement on the TLU immunity of the SCR. The bidirectional-type TVS components (part number: P6KE series) with three different breakdown voltages, V_{BR}, (±13 V, ±82 V, and ±200 V) are employed. As shown in Fig. 3.12, the TVS components with breakdown voltage of ±82 V and ±200 V fail to efficiently improve the TLU level of the SCR (the magnitudes of both positive and negative TLU levels are all equal to 200 V), because TLU occurs prior to the breakdown of the high-V_{BR} TVS. Only the TVS with a low V_{BR} can effectively enhance the TLU level. For example, the positive TLU level can be enhanced to +520 V for TVS with breakdown voltage of ±13 V. Thus, to optimize the efficiency of TVS for TLU prevention, the correlations between V_{BR} of TVS and the intrinsic TLU level of DUT should be clarified in advance.



(a) (b)

(c) (d)

Fig. 3.11 Four types of noise filter networks investigated for their improvements on the TLU level of the SCR. (a) Ferrite bead, (b) TVS, (c) hybeid type I, and (d) hybeid type II.

Hybrid type filters consisting of both ferrite bead (minimum impedance of 80 Ω at 25 MHz) and TVS (with different V_{BR}) are also evaluated for their improvements on the TLU level of the SCR, as shown in Figs. 3.11(c) and 3.11(d). Hybrid types I and II are the counterparts of the LC-like and π-section filters where the TVS substitutes for the decoupling capacitor as a low-pass component. Because such higher-order hybrid type filters provide higher insertion loss, they enhance the TLU level of SCR more significantly than ferrite bead or TVS alone, as shown in Fig. 3. 12. For example, hybrid type I with a low-V_{BR} (±13 V) TVS can enhance the positive TLU level up to +550 V. For hybrid type II with a low-V_{BR} (±13 V) TVS, the positive (negative) TLU level can be enhanced to over +1000 V (-780 V).

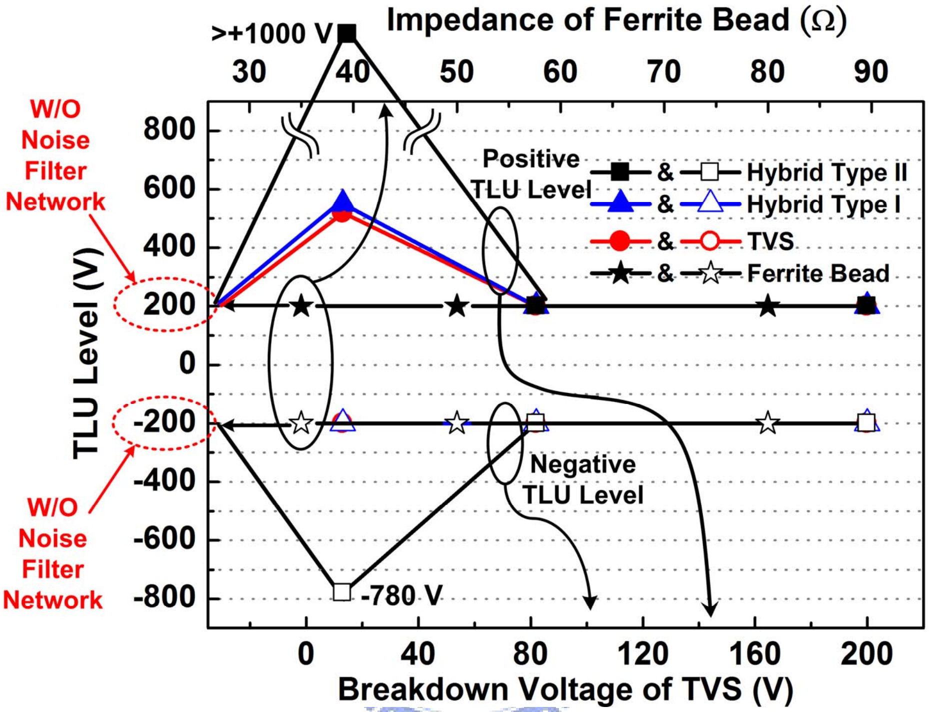


Fig. 3.12 Relations among the TLU level of SCR, minimum impedance of ferrite bead at 25MHz, and the breakdown voltage of TVS with four types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II.

3.4.3. Discussion

Through investigating different types of noise filter networks to find their improvements on TLU levels in Figs. 3.10 and 3.12, it is found that TVS (hybrid type II) does not improve the negative TLU level as greatly as the 1st-order capacitor filter (LC-like filter) does. For example, the negative TLU level can be significantly enhanced to over -1000 V using an LC-like filter with a decoupling capacitance of 0.1μF, while the TLU level is -780 V using the hybrid type II with a low V_{BR} (±13 V) TVS. Thus, the decoupling capacitor is better than TVS for being a noise-bypassing component in the noise filter networks, because it not only can enhance the negative TLU level more efficiently, but also is compatible to CMOS technology for integrating the noise filter into the CMOS chips. Especially for some TVS components, the fabrication is made by modified processes with special materials. Therefore, it may be difficult to integrate the TVS into the silicon chip due to complex process integration. To further improve the TLU immunity of electronic products, chip-level solutions should be adopted to meet the applications with high EFT specification and reduce the cost of electronic products. For example, an on-chip power-rail ESD clamp circuit between V_{DD} and V_{SS} power lines can provide a low impedance path to efficiently discharge ESD current during ESD stress conditions. For CMOS ICs under EFT tests, it may be a solution to apply an on-chip power-rail ESD clamp circuit to suppress electrical transients and avoid unexpected current into the internal circuits. In the on-chip circuit design techniques, some circuits have been also proposed to avoid latchup or to detect the electrical fast transients under ESD stress conditions The chip-level solutions have the advantages of single chip integration in nanoscale CMOS technology and substantially reduce the total cost of microelectronic products. Therefore, the chip-level solutions to meet high EFT specification for microelectronic products are highly requested by the IC industry.

3.5. Conclusion

The positive and negative EFT voltage pulses have been identified as the realistic TLU-triggering source under EFT tests. From experimental measurements, the specific "swept-back" current caused by the minority carriers stored within the parasitic PNPN structure of CMOS ICs has been proven to be the cause of TLU. Thus, TLU reliability may still exist in qualified CMOS IC products through the quasi-static latchup test. With understanding of the physical mechanism and experimental verification on TLU, circuit design and layout techniques in CMOS ICs can be developed against TLU events under EFT tests.

By choosing proper components in each noise filter network, the TLU immunity of CMOS ICs under the EFT tests can be greatly improved. From the experimental results, the decoupling capacitor is better than TVS as a noise-bypassing component in noise filter networks, because it not only can enhance the negative TLU level more efficiently, but is also compatible to CMOS technology for integrating the noise filter into chips. The optimal design for enhancements of TLU immunity can be achieved through a clear characterization of TLU prevention from different kinds of board-level noise filters. In addition, chip-level solutions should be further developed to meet high EFT immunity requirement for microelectronic products.

Chapter 4

On-Chip Transient Detection Circuit Design for Electrical Transient Disturbance Protection (Scheme I)

A novel on-chip transient detection circuit I for system-level electrostatic discharge (ESD) protection is proposed in this work. The circuit performance to detect positive and negative electrical transients under system-level ESD and EFT zapping conditions has been investigated by the HSPICE simulation and verified on silicon. The experimental results have confirmed that the proposed on-chip transient detection circuit I can successfully memorize the occurrence of the system-level ESD and EFT events. The detection output of proposed on-chip transient detection circuit I can be used as the firmware index to execute system recovery procedure to provide a hardware/firmware co-design to improve the immunity of CMOS IC products against system-level ESD and EFT stress.

4.1. Background

In order to solve the electrical transient disturbance events, one effective method is to add some discrete noise-bypassing components or board-level noise filters into the CMOS IC products to decouple, bypass, or absorb the electrical transient voltage (energy) under system-level ESD test. The system-level ESD immunity of CMOS ICs under system-level ESD test can be significantly enhanced by choosing proper noise filter networks. As shown in Fig. 4.1, some discrete components (such as the ferrite bead (FB), and RC low-pass filters) are added into printed circuit board (PCB) of a keyboard product to restrain the electrical transients from the system-level ESD and EFT tests. The electrical transient disturbance immunity of CMOS ICs under system-level ESD and EFT tests can be significantly enhanced by choosing proper noise filter networks. However, the additional discrete noise-bypassing components also substantially increase the total cost of microelectronic products. Therefore, the chip-level solutions to meet high electrical transient disturbance immunity specification for microelectronic products without additional discrete noise-decoupling components added on PCB are highly desired by IC industry.

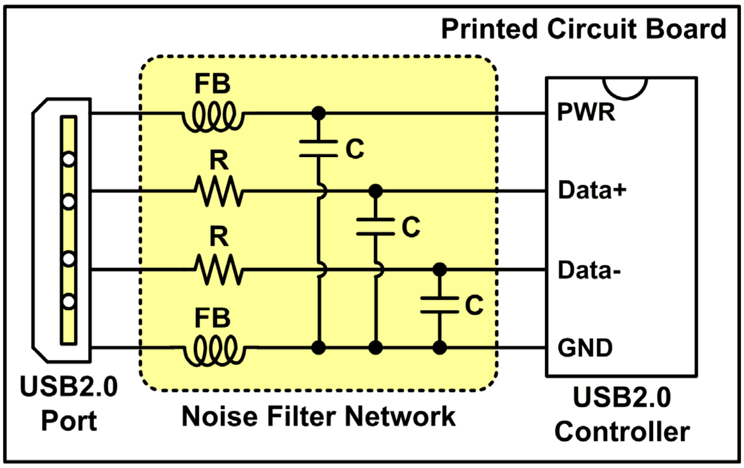


Fig. 4.1 The board-level solution for microelectronic products against electrical transient disturbance.

4.2. On-Chip Transient Detection Scheme I Designed with 3.3-V Devices

The proposed on-chip transient detection circuit I is designed to detect the positive and negative fast electrical transients under the system-level ESD and EFT tests. Under the normal power supply condition, the output state (V_{OUT}) of the proposed on-chip transient detection circuit is designed to keep at initial logic state. Under the system-level ESD and EFT tests, the output state (V_{OUT}) of the proposed on-chip transient detection circuit I is designed to transit from initial logic state to conjugate logic state. Therefore the proposed on-chip transient detection circuit I can be designed to memorize the occurrence of system-level ESD and EFT events.

Fig. 4.2 shows the proposed on-chip RC-based transient detection circuit I. The RC-based circuit structure is designed to realize the transient detection function. The two-inverter latch (INV_2 and INV_3) is designed to memorize the logic state before and after system-level ESD stress. The NMOS (M_{nr}) is used to provide the initial reset function to set the initial output voltage (V_{OUT}) level to 0 V. In Fig. 4.2, the node V_X is biased at V_{DD} and the node V_G is biased at V_{SS} during the normal operation condition. Under the system-level ESD and EFT stresses, the electrical transient voltage has a fast rise time, on the order of a nanosecond (ns). The voltage level of V_X has a much slower voltage response than the voltage level at V_{DD} because the RC circuit has a time constant, on the order of a microsecond (μs). Due to the longer delay of the voltage increase at the node V_X, the PMOS device in the inverter1 (INV_1) can be turned on by the overshooting ESD voltage and conducts a voltage to the node V_G to further turn on the M_{n1} device. The turned-on M_{n1}

device can pull down the output voltage level at the node V_A. Therefore, the logic level stored in the two-inverter latch can be changed to detect the system-level ESD and EFT events. The output voltage (V_{OUT}) of the proposed on-chip RC-based transient detection circuit I is finally changed from 0V to 3.3 V to memorize the occurrence of system-level ESD and EFT events.

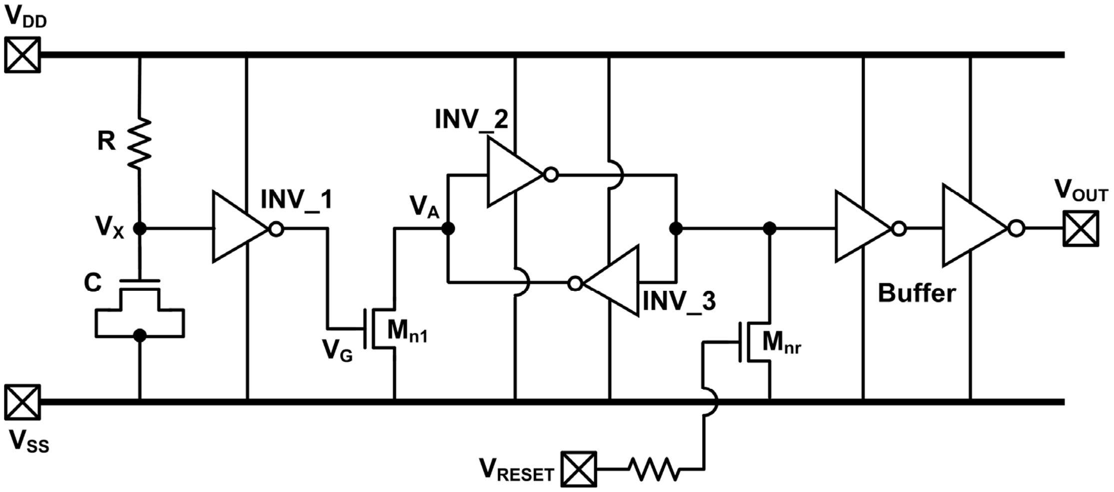


Fig. 4.2 Schematic diagram of the proposed novel transient detection circuit I.

4.3. HSPICE Simulation Results

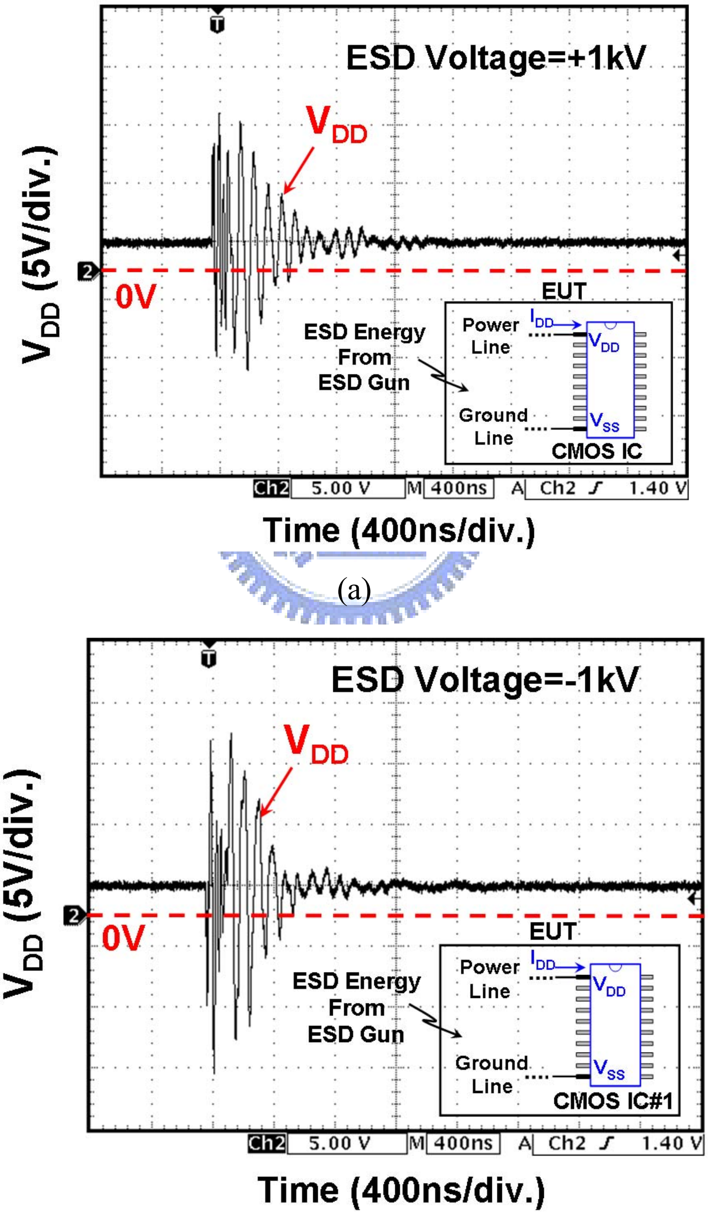
4.3.1. System-Level ESD Zapping Conditions

Figs. 4.3(a) and 4.3(b) show the measured transient voltage waveform on the power line of CMOS ICs inside the EUT with ESD voltages of +1 kV and -1 kV, respectively. The power lines (pins) of the CMOS ICs no longer maintain their normal voltage levels, but acts as an underdamped sinusoidal voltage instead.

From the measured electrical transient waveform shown in Figs. 4.3(a) and 4.3(b), the underdamped sinusoidal voltage waveform on power line of CMOS IC during the system-level ESD stress has been observed. There, a sinusoidal time-dependent voltage source with damping factor parameter is given by

$$V(t) = V_0 + V_a \cdot \sin(2\pi f(t-t_d)) \cdot \exp(-(t-t_d)D_a). \tag{1}$$

It is used to simulate an underdamped sinusoidal voltage on the V_{DD} and V_{SS} lines of the proposed on-chip transient detection circuit I, as shown in Fig. 4.4. With the proper parameters such as the applied voltage amplitude V_a, initial dc voltage V_0, damping factor D_a, damping frequency f ($=D_{Freq}$), and time delay t_d, the underdamped sinusoidal voltage can be used to simulate the electrical transient waveforms under system-level ESD tests. In the HSPICE simulation with positive-going or negative-going underdamped sinusoidal waveforms, the same parameters of D_a= 2x10^7 s^{-1}, f= 50 MHz, and t_d= 500 ns are used (which is corresponding to the measured transient waveform in Figs. 4.3(a) and 4.3(b)). For the positive-going underdamped sinusoidal waveform, the polarity of V_a parameter is positive. For the negative-going underdamped sinusoidal waveform, the polarity of V_a parameter is negative. In addition, V_0 is 3.3 V (0 V) as the initial dc voltage on the V_{DD} (V_{SS}) line of the proposed on-chip transient detection circuit I.



(a)

(b)

Fig. 4.3 Measured voltage waveforms with ESD voltage of (a) +1 kV, and (b) -1 kV

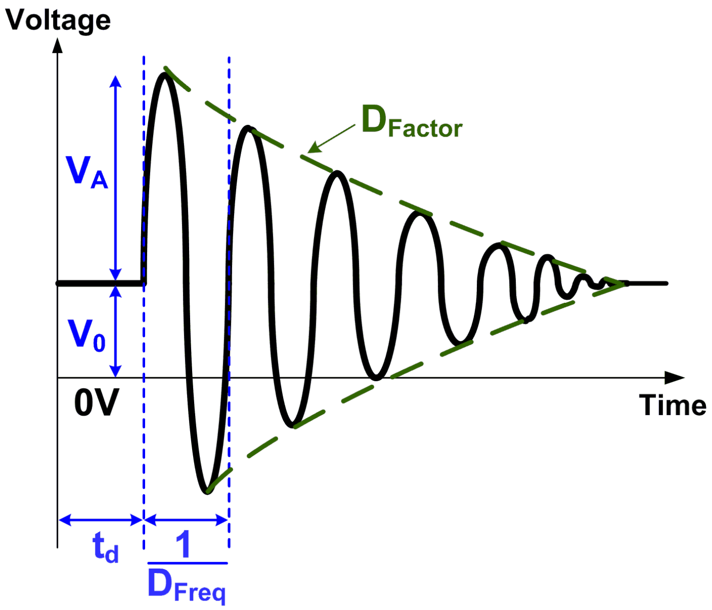
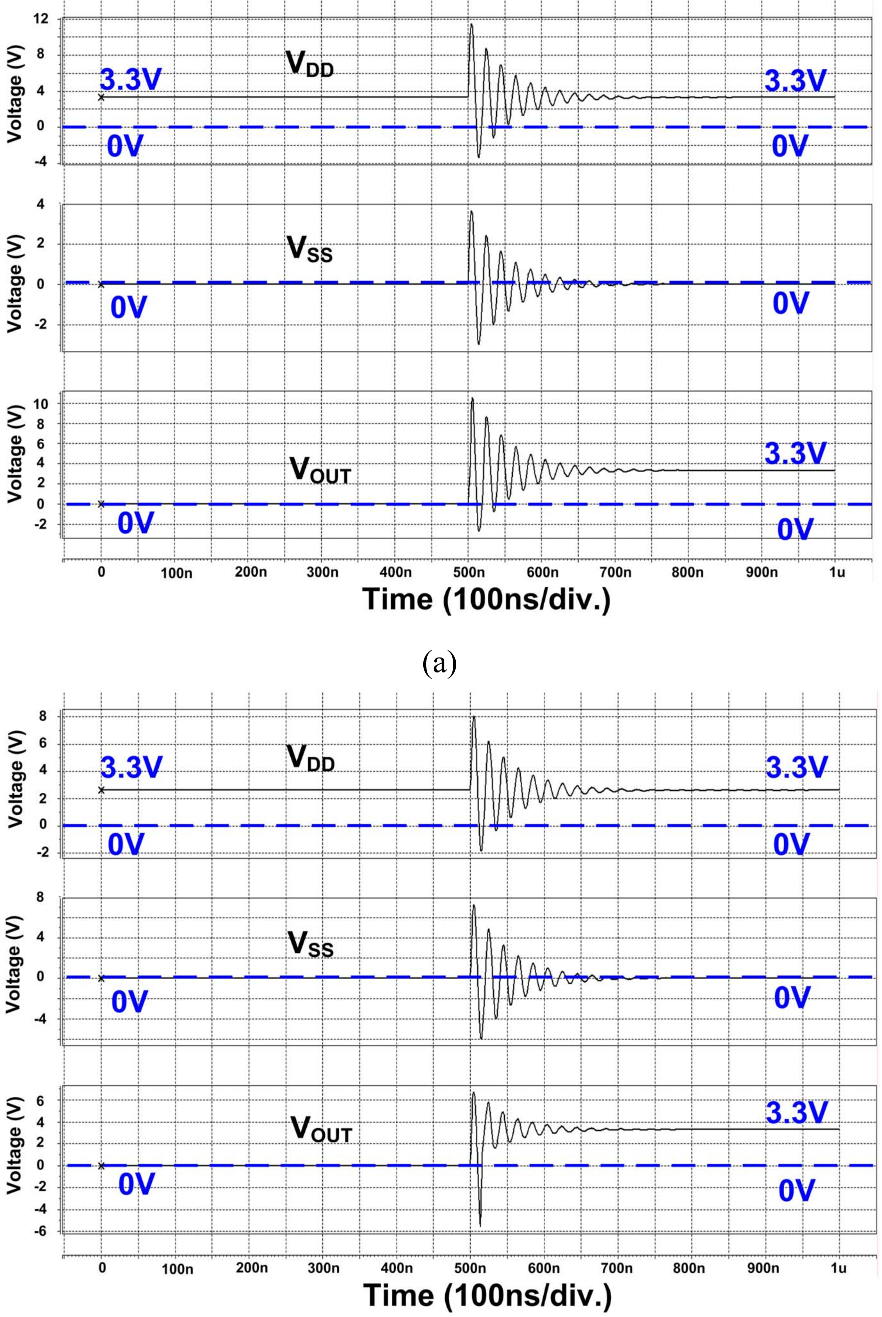


Fig. 4.4 The specific time-dependent underdamped sinusoidal waveforms applied on the power and ground lines to simulate the transient disturbance under system-level ESD zapping.

The simulated V_{DD}, V_{SS}, and V_{OUT} waveforms of the proposed on-chip transient detection circuit I with a positive-going underdamped sinusoidal voltage on both V_{DD} and V_{SS} are shown in Fig. 4.5(a). The positive-going underdamped sinusoidal voltage with V_a of +8 V on V_{DD} and with V_a of +4 V on V_{SS} are used to simulate the larger overshooting voltage coupled on V_{DD} under the system-level ESD test, as shown in Fig. 4.5(a). Under ESD stress, V_{DD} (V_{SS}) begins to increase rapidly from 3.3 V (0 V) to 11 V (4 V). V_{OUT} is disturbed simultaneously during the V_{DD} and V_{SS} disturbance. During this period, the proposed on-chip RC-based transient detection circuit I can detect the occurrence of disturbances on V_{DD} and V_{SS}. As a result, after V_{DD} finally returns to its normal voltage level of 3.3 V, V_{OUT} will be changed from 0 V to 3.3 V, as shown in Fig. 4.5(a).

The simulated V_{DD}, V_{SS}, and V_{OUT} waveforms of the proposed on-chip transient detection circuit I with a positive-going underdamped sinusoidal voltage on both V_{DD} and V_{SS} are shown in Fig. 4.5(b). The positive-going underdamped sinusoidal voltage with V_a of +4 V on V_{DD} and with V_a of +8 V on V_{SS} are used to simulate the larger overshooting voltage coupled on V_{SS} under the system-level ESD test, as shown in Fig. 4.5(b). The V_{OUT} is influenced by the V_{DD} and V_{SS} disturbance through the coupling paths. Finally, the output (V_{OUT}) of the proposed on-chip transient detection circuit is changed from 0 V to 3.3 V.



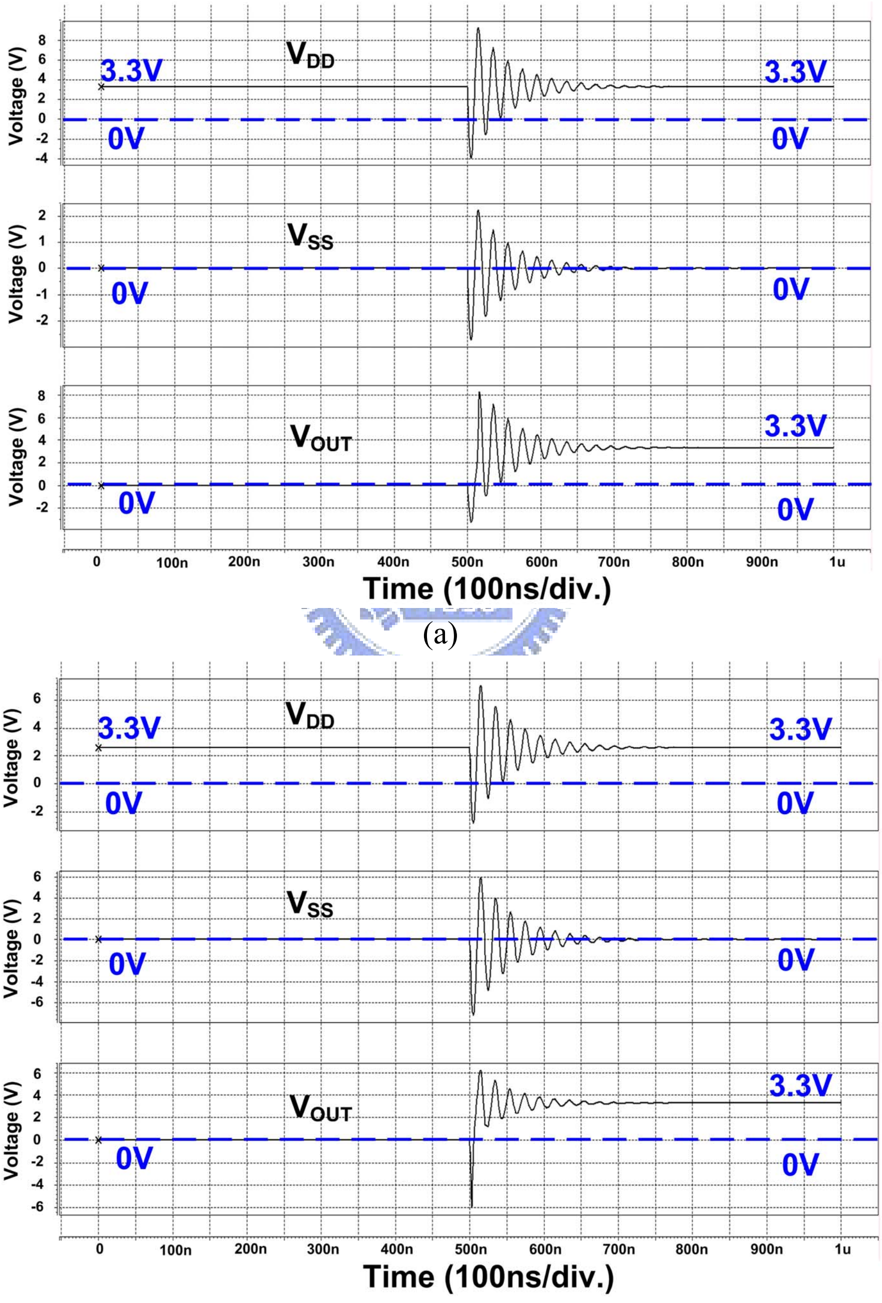
(a)

(b)

Fig. 4.5 Simulated V_{DD}, V_{SS}, and V_{OUT} waveforms of the proposed transient detection circuit I under system-level ESD test with larger overshooting voltage coupled on (a) V_{DD}, and (b) V_{SS}.

Under the negative system-level ESD zapping condition, the simulated V_{DD}, V_{SS}, V_{OUT1}, and V_{OUT2} waveforms of the proposed transient detection circuit with a negative-going underdamped sinusoidal voltage on V_{DD} and V_{SS} are shown in Figs. 4.6(a) and 4.6(b). The negative-going underdamped sinusoidal voltages with V_a of -8 V on V_{DD} and with V_a of -4 V on V_{SS} are used to simulate the larger undershooting voltage coupled on V_{DD} under the system-level

ESD test, as shown in Fig. 4.6(a). The negative-going underdamped sinusoidal voltages with V_a of -4 V on V_{DD} and with V_a of -8 V on V_{SS} are used to simulate the larger undershooting voltage coupled on V_{SS} under the system-level ESD test, as shown in Fig. 4.6(b). In Figs. 4.6(a) and 4.6(b), the output voltage of the transient detection circuit I begins to decrease rapidly. The V_{OUT1} and V_{OUT2} are influenced by the V_{DD}/V_{SS} disturbance. Finally, the output voltages (V_{OUT1} and V_{OUT2}) of the transient detection circuit I are changed from 0V to 3.3 V, as shown in Figs. 4.6(a) and 4.6(b).

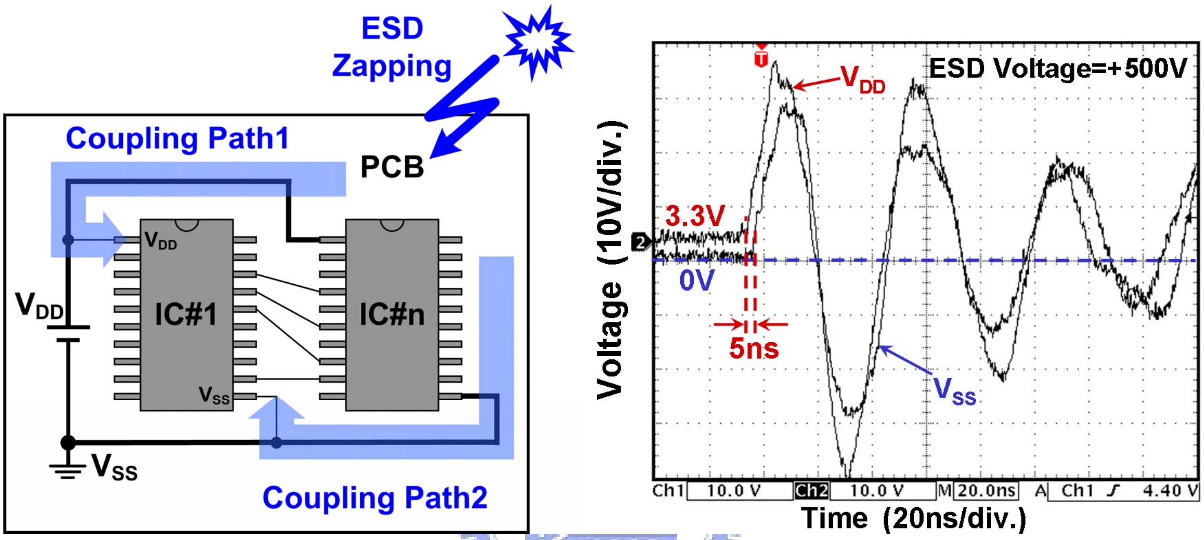


(a)

(b)

Fig. 4.6 Simulated V_{DD}, V_{SS}, and V_{OUT} waveforms of the proposed transient detection circuit I under system-level ESD test with larger undershooting voltage coupled on (a) V_{DD}, and (b) V_{SS}.

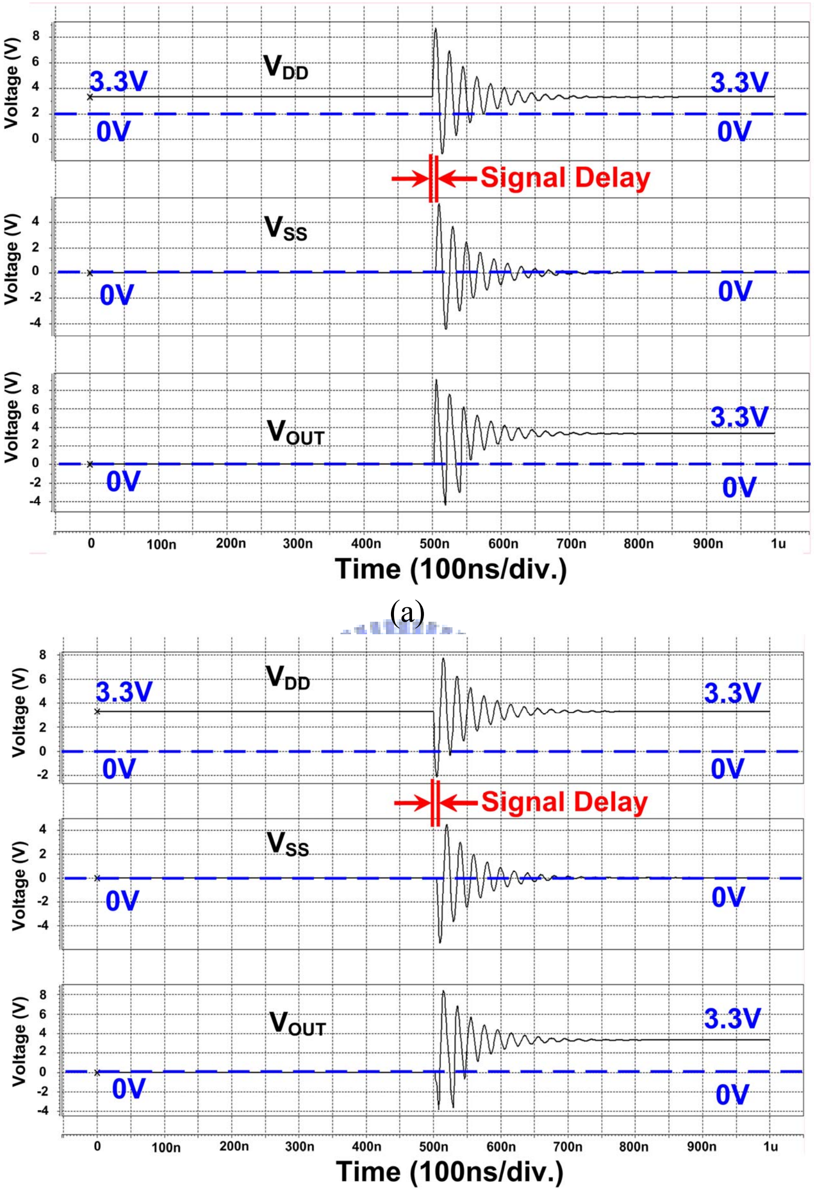
On the PCB design with CMOS IC products, the trace routing placements may be different for power (V_{DD}) lines and ground (V_{SS}) lines. This will cause different signal paths from ESD source to V_{DD} and V_{SS} pins of the chip, as shown in Fig. 4.7(a). The different signal paths may result in different signal delays between V_{DD} and V_{SS} waveforms. As shown in Fig. 4.7(b), 5-ns signal delay has been observed between V_{DD} and V_{SS} pins of the chip. Therefore, the different signal delays in the transient waveforms between V_{DD} and V_{SS} should be taken into consideration in the design of the proposed on-chip transient detection circuit



(a) (b)

Fig. 4.7 (a) Different signal coupling path from the ESD zapping source to V_{DD} and V_{SS} pins of CMOS IC on the PCB. (b) Time delay between the measured V_{DD} and V_{SS} waveforms is due to the different coupling path.

The simulated V_{DD}, V_{SS}, and V_{OUT} waveforms of the proposed transient detection circuit I with signal delay between V_{DD} and V_{SS} waveforms are shown in Figs. 4.8(a) and 4.8(b). In order to simulate the signal delay condition that V_{DD} signal leads the V_{SS} signal, different t_d parameters are used on V_{DD} (t_d =500 ns) and V_{SS} (t_d =505 ns) voltage sources. The positive V_a on V_{DD} and V_{SS} waveforms is used in this simulation for signal delay condition, as shown in Fig. 4.8(a). The negative V_a on V_{DD} and V_{SS} waveforms is used in this simulation for another signal delay condition, as shown in Fig. 4.8(b). During the period with electrical transient disturbance, V_{OUT} is influenced with the V_{DD}/V_{SS} waveforms and acts as underdamped sinusoidal voltage waveform. After the simulated electrical transient disturbance, V_{OUT} is pulled up to the voltage level of 3.3 V. With a signal delay between V_{DD} and V_{SS}, the proposed on-chip transient detection circuit I can still memorize the occurrence of electrical transients on V_{DD} and V_{SS} lines.



(a)

(b)

Fig. 4.8 Simulated V_{DD}, V_{SS}, and V_{OUT} waveforms of the proposed transient detection circuit I under (a) positive, and (b) negative underdamped sinusoidal voltage on V_{DD}/V_{SS} power lines with signal delay condition.

4.3.2. EFT Zapping Conditions

For microelectronic products, the shielding plate is often designed into microelectronic products to bypass or reduce the EFT-induced electrical transient disturbance. Therefore, the electrical transients injected into CMOS ICs inside the microelectronic products can be degraded with smaller amplitude compared with the original testing voltage. Therefore, the EFT-induced transients with different degraded amplitudes are taken into considerations in HSPICE simulation on the novel proposed on-chip transient detection circuit I.

From the measured electrical transient waveforms shown in Figs. 1.9(a) and 1.9(b), the approximated exponential voltage pulse waveforms during the EFT tests have been observed. There, an exponential pulse time-dependent voltage source with rise/fall time constant parameters is used to simulate EFT-induced transient disturbance on the novel proposed on-chip transient detection circuit I. The rising edge of this exponential time-dependent voltage pulse is expressed as

$$V_{p(rising\ edge)}(t) = V_1 + \left(V_2 - V_1\right) \times \left[1 - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right)\right], \text{ when } t_{d1} \le t \le t_{d2}. \quad (2)$$

The falling edge of this exponential time-dependent voltage pulse is expressed as

$$V_{p(fall)}(t) = V_1 + \left(V_2 - V_1\right) \times \left[1 - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right)\right] + \left(V_1 - V_2\right)\left[1 - \exp\left(-\frac{t - t_{d2}}{\tau_2}\right)\right], \text{ when } t \ge t_{d2}. \quad (3)$$

With the proper parameters (including the rise time constant τ_1, fall time constant τ_2, rise time delay t_{d1}, fall time delay t_{d2}, initial dc voltage value V_1, and exponential pulse voltage value V_2), the exponential voltage pulse can be constructed to simulate the EFT-induced disturbance under EFT tests as shown in Fig. 4.9. In HSPICE simulation with positive or negative exponential voltage pulse waveforms, the same parameters of $\tau_1 = 3$ ns, $\tau_2 = 25$ ns, and $t_{d2} - t_{d1} = 10$ ns are used (which is corresponding to the measured transient waveforms in Figs. 1.9(a) and 1.9(b)). For the positive exponential voltage pulse, the value of V_2 parameter is larger than the value of V_1 parameter. For the negative exponential voltage pulse, the polarity of $V_2 - V_1$ parameter is negative. In addition, V_1 is 3.3 V as the initial dc voltage on the V_{DD} line of the novel proposed on-chip transient detection circuit I.

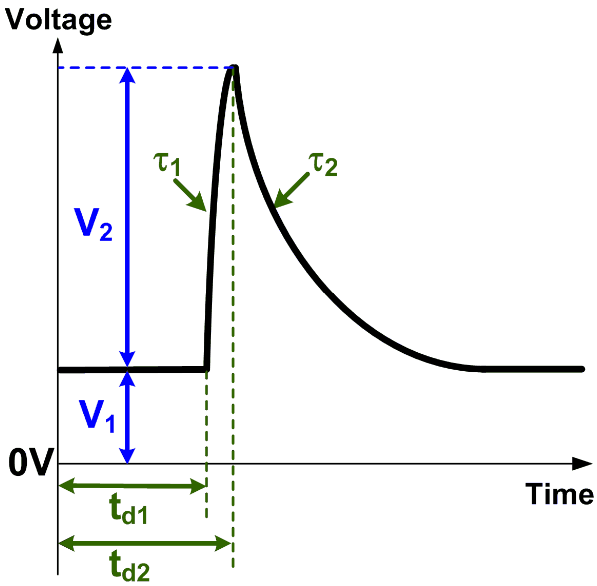


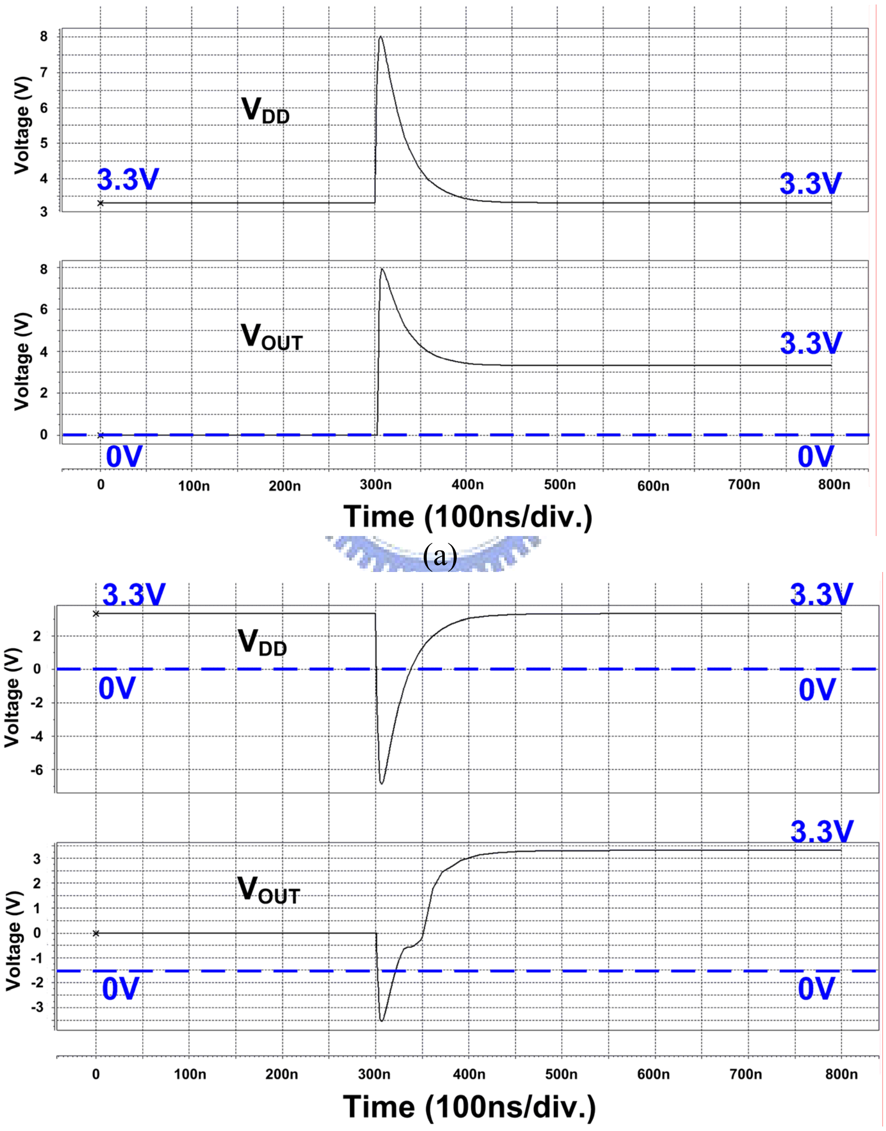
Fig. 4.9 The specific time-dependent exponential pulse waveform applied on the power lines to simulate the disturbance under EFT zapping.

The simulated V_{DD} and V_{OUT} waveforms of the novel proposed on-chip transient detection circuit I with a positive exponential pulse transient disturbance on V_{DD} line are shown in Fig. 4.10(a). The exponential voltage pulse with amplitude of +10 V is used to simulate the coupling positive transient disturbance under the EFT test. From the simulated waveforms, V_{DD} begins to increase rapidly from 3.3 V and V_{OUT} also acts with a positive exponential voltage pulse waveform during the simulated transient disturbance on V_{DD} line. After the transient disturbance duration, V_{DD} returns to its normal voltage level of 3.3 V and the output state (V_{OUT}) of the novel proposed on-chip transient detection circuit I transits from 0V to 3.3 V, as shown in Fig. 4.10(a). As a result, the novel proposed on-chip transient detection circuit I can detect the occurrence of positive EFT-induced exponential pulse transient disturbance.

The simulated V_{DD} and V_{OUT} waveforms of the novel proposed on-chip transient detection circuit I with a negative exponential pulse transient disturbance on V_{DD} line are shown in Fig. 4.10(b). The exponential voltage pulse with amplitude of -10 V is used to simulate the coupling negative transient disturbance under the EFT test. From the simulated waveforms, V_{DD} begins to decrease rapidly from 3.3 V and V_{OUT} also acts with a negative exponential voltage pulse during the simulated transient disturbance on V_{DD} line. After the transient disturbance duration, V_{DD} returns to its normal voltage level of 3.3 V and the output state (V_{OUT}) of the novel proposed on-chip transient detection circuit I transits from 0 V to

3.3 V, as shown in Fig. 4.10(b). As a result, the novel proposed on-chip transient detection circuit I can detect the occurrence of negative EFT-induced exponential pulse transient disturbance.

From the aforementioned simulation results in Figs. 4.10(a) and 4.10(b), after the positive or negative EFT-induced transient disturbance on V_{DD} line, the output state of the novel proposed on-chip transient detection circuit I can be changed from 0 V and kept at 3.3 V. Therefore, the novel proposed on-chip transient detection circuit I can successfully memorize the occurrence of positive or negative EFT-induced exponential pulse transient disturbance.



(a)

(b)

Fig. 4.10 Simulated V_{DD} and V_{OUT} waveforms of the proposed on-chip transient detection circuit I under EFT tests with (a) positive, and (b) negative exponential pulse voltage waveforms coupled on V_{DD}.

The novel proposed on-chip transient detection circuit I has been designed and fabricated in a 0.18-µm 1P5M CMOS process with 3.3-V devices. The fabricated chip for transient disturbance tests is shown in Fig. 4.11. The TLU measurement method, the system-level ESD gun, and the EFT generator are used to evaluate the detection function of the novel proposed on-chip transient detection circuit I after ESD-induced or EFT-induced electrical transient disturbance.

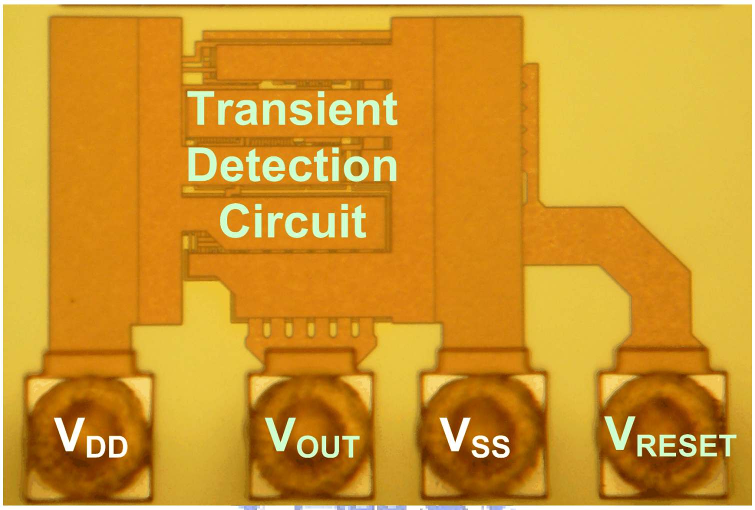


Fig. 4.11 Die photo of the proposed on-chip transient detection circuit I.

4.4. Experimental Results

4.4.1. TLU Tests

A Transient-induced latchup (TLU) test has been used to investigate the susceptibility of device under test (DUT) to the noise transient or glitch on the power lines under normal circuit operating condition. The component-level TLU measurement setup with bipolar trigger waveform can accurately simulate the ESD-induced noises on the power lines of CMOS ICs under system-level ESD test. The measurement setup for TLU test is shown in Fig. 4.12. The charging voltage V_{Charge} has two different polarities, which are positive ($V_{Charge}>0$) and negative ($V_{Charge}<0$). The positive (negative) V_{Charge} can generate the positive-going (negative-going) bipolar trigger noise on the power pins of the DUT. A 200-pF capacitor used in the machine model (MM) ESD test is employed as the charging capacitor. The proposed on-chip RC-based transient detection circuit is placed as the DUT in Fig. 4.12. The supply voltage of 3.3 V is used as V_{DD} and the noise trigger source is directly connected to DUT through the relay in the measurement setup. The current-limiting resistance is used to avoid electrical-over-stress (EOS) damage in the DUT under a high-current latch-up state. The voltage and current waveforms on the DUT (at V_{DD} node) after the TLU test are monitored by the oscilloscope.

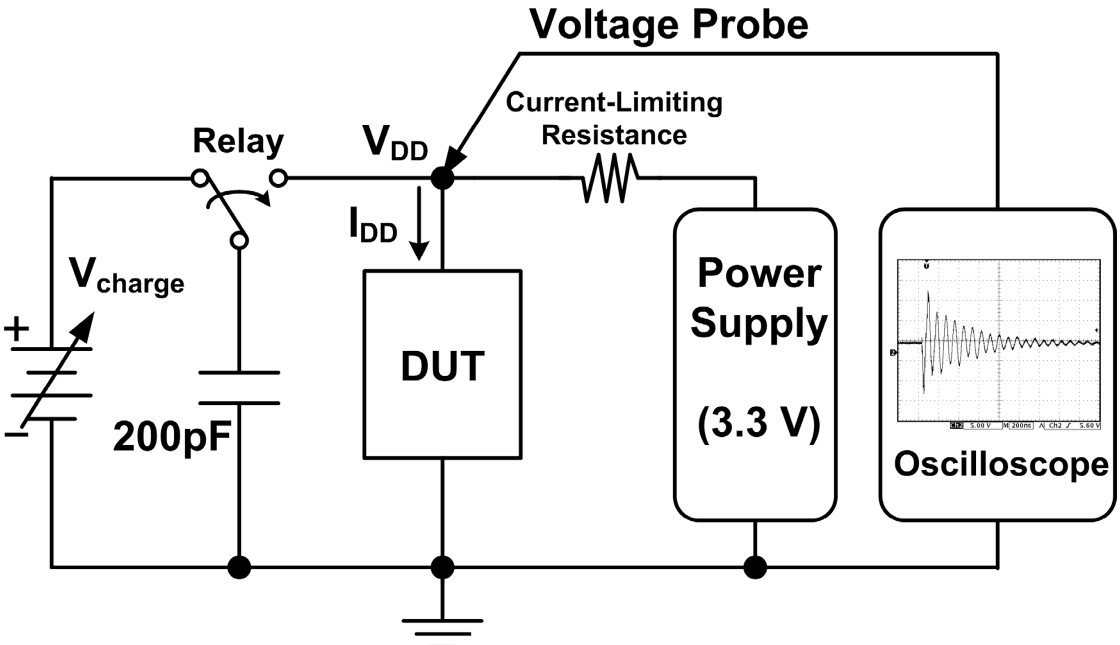
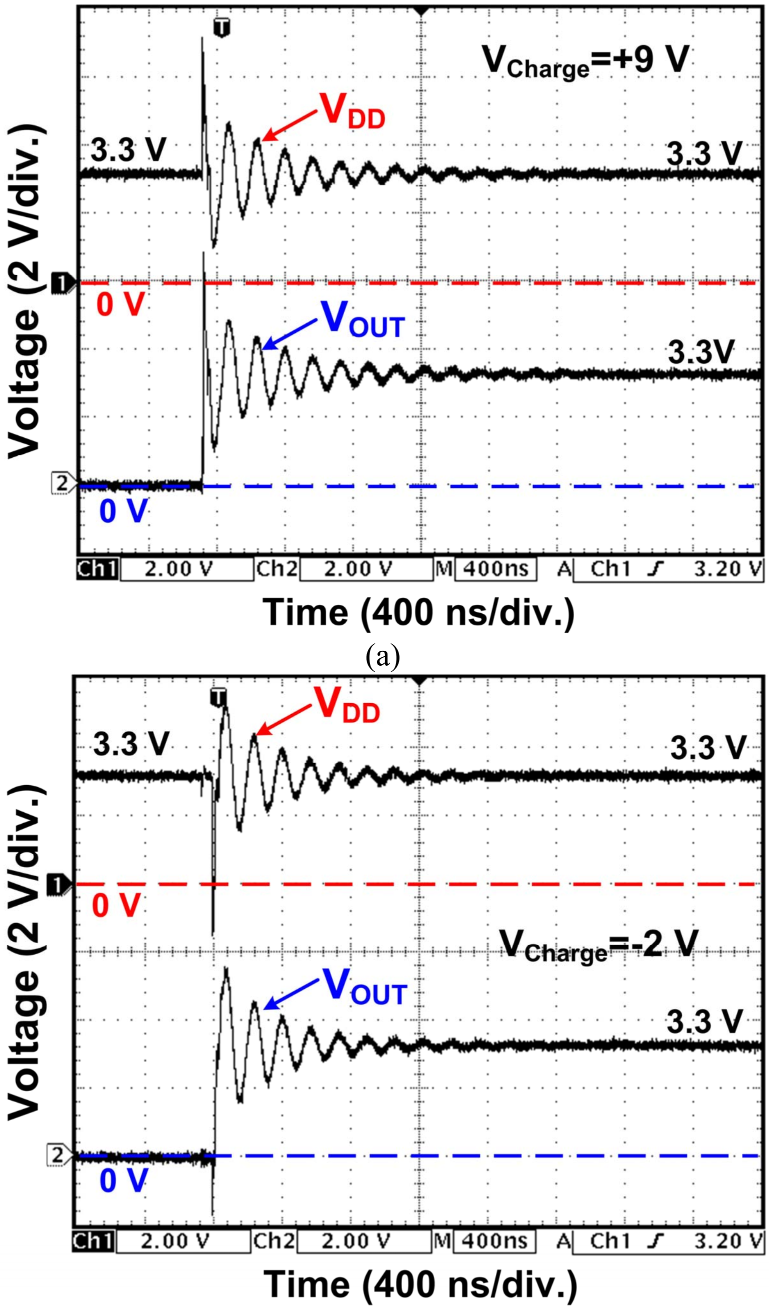


Fig. 4.12 Measurement setup for transient-induced latchup (TLU).

Figs. 4.13(a) and 4.13(b) show the measured V_{DD} and V_{OUT} transient responses of the proposed on-chip RC-based transient detection circuit I under the TLU test with V_{Charge} of +9 V and -2 V, respectively. As shown in Fig. 4.13(a), under the TLU test with V_{Charge} of +9 V, V_{DD} begins to increase rapidly from 3.3 V. V_{OUT} is disturbed simultaneously with positive underdamped sinusoidal voltages on the V_{DD} power line. After the TLU test with an initial V_{Charge} of +9 V, the output (V_{OUT}) of the proposed on-chip RC-based transient detection circuit I is changed from 0 V to 3.3 V. As shown in Fig. 4.13(b), under the TLU test with V_{Charge} of -2 V, V_{DD} begins to decrease rapidly from 3.3 V. V_{OUT} is disturbed simultaneously with negative underdamped sinusoidal voltages on V_{DD} power line. After the TLU test with an initial V_{Charge} of -2 V, the output voltage (V_{OUT}) of the proposed on-chip RC-based transient detection circuit I is increased from 0 V to a stable voltage of 3.3 V.



(a)

(b)

Fig. 4.13 Measured V_{DD} and V_{OUT} waveforms on the proposed on-chip transient detection circuit I under TLU test with V_{Charge} of (a) +9 V, and (b) -2 V.

4.4.2. System-level ESD Tests

In the IEC 61000-4-2 standard, two test modes have been specified, which are the air-discharge test mode and the contact-discharge test mode. Contact discharge is further divided into direct discharge to the system under test, and indirect discharge to horizontal or vertical coupling planes. Fig. 4.14 shows the standard measurement setup of the system-level ESD test in the indirect contact-discharge test mode. The measurement setup for system-level

ESD test consists of a wooden table on the grounded reference plane (GRP). In addition, an insulation plane is used to separate the EUT from the horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470 kΩ resistors in series. When the ESD gun zaps the HCP, the EMI coming from ESD will be coupled into all CMOS ICs inside EUT. The power lines of CMOS ICs inside EUT will be disturbed by the ESD-coupled energy.

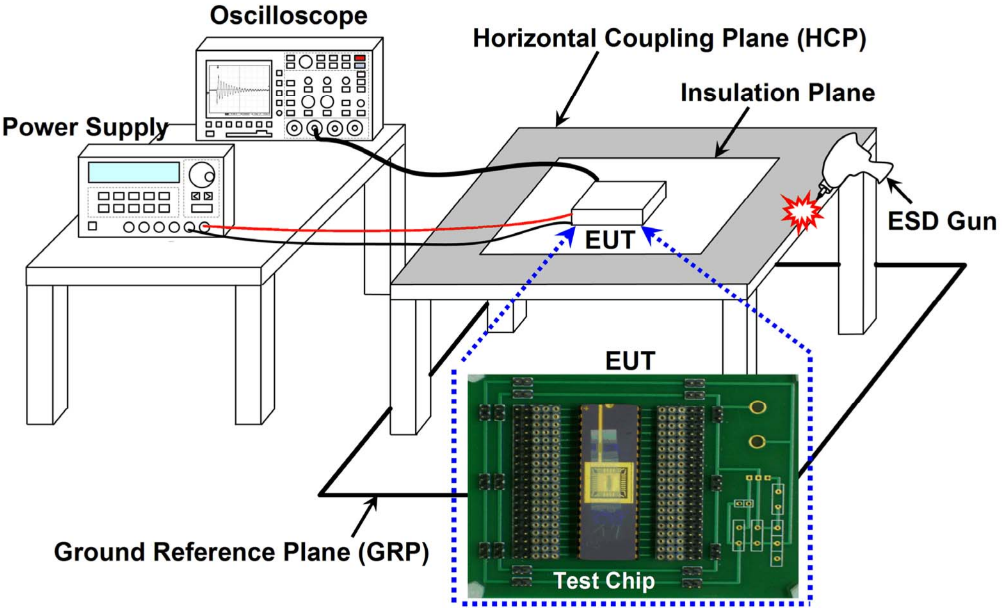
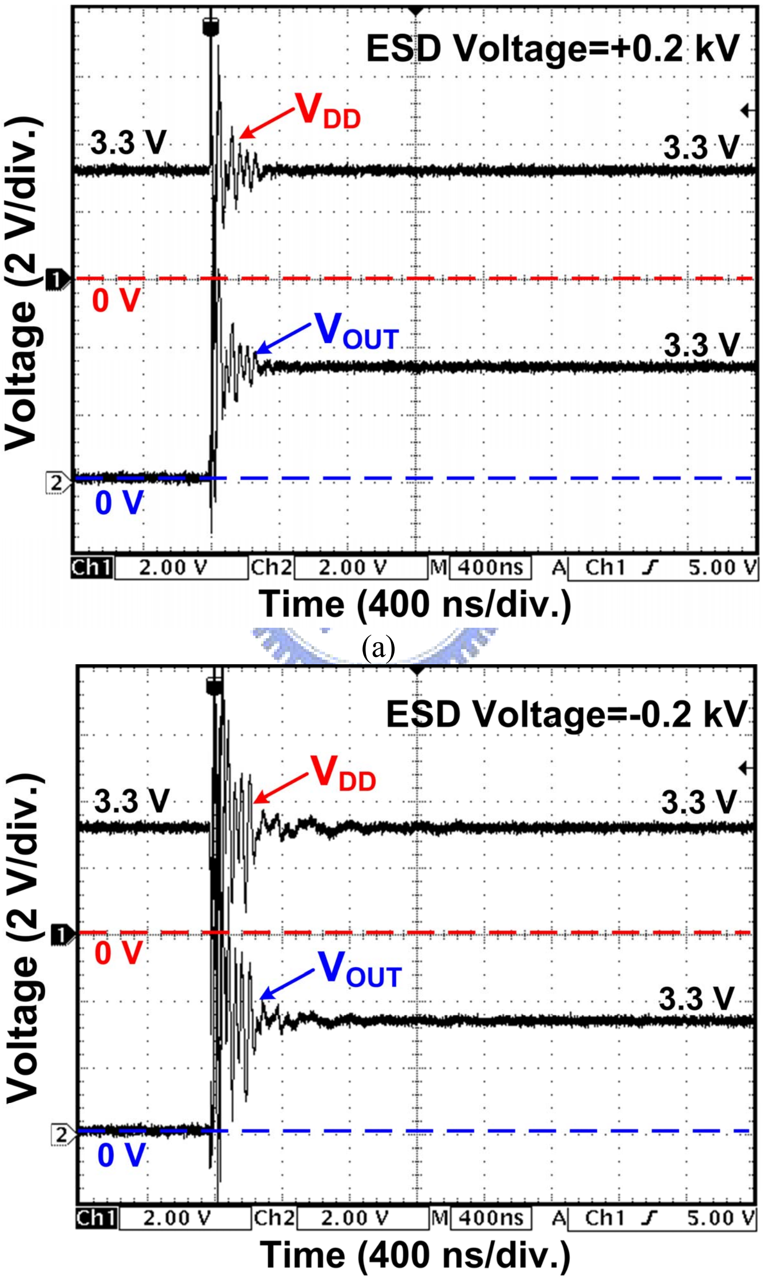


Fig. 4.14 Measurement setup of system-level ESD test with indirect contact discharge mode.

With such a standard measurement setup, the circuit performance of the proposed on-chip RC-based transient detection circuit I under system-level ESD tests can be evaluated. By using the digital oscilloscope, the transient responses on power lines of CMOS IC products can be recorded and analyzed. Before each system-level ESD zapping, the initial output voltage (V_{OUT}) of the proposed on-chip RC-based transient detection circuit I is reset to 0 V. After each system-level ESD zapping, the output voltage (V_{OUT}) level is measured to check the final voltage level and to verify the detection function. Thus, the circuit performance of the proposed on-chip RC-based transient detection circuit I can be directly evaluated with this measurement setup.

The measured V_{DD} and V_{OUT} waveforms of the proposed on-chip RC-based transient detection circuit I under a system-level ESD test with the ESD voltage of +0.2 kV zapping on the HCP is shown in Fig. 4.15(a). V_{DD} begins to increase rapidly from the normal voltage (+3.3 V). Meanwhile, V_{OUT} begins to change under such a high-energy ESD stress. During the fast transient disturbance, V_{DD} and V_{OUT} are influenced simultaneously. Finally, the output voltage of the proposed on-chip RC-based transient detection circuit I has been changed from 0 V to 3.3 V.

The measured V_{DD} and V_{OUT} transient waveforms of the proposed on-chip RC-based transient detection circuit with an ESD voltage of -0.2 kV zapping on the HCP under system-level ESD test are shown in Fig. 4.15(b). During the V_{DD} disturbance, V_{OUT} is disturbed simultaneously. V_{OUT} is finally pulled up to 3.3 V after the system-level ESD test. Therefore, the proposed on-chip RC-based transient detection circuit I can sense the fast electrical transient on the power lines and memorize the occurrence of system-level ESD events.



(a)

(b)

Fig. 4.15 Measured V_{DD} and V_{OUT} transient responses of the proposed transient detection circuit I under system-level ESD test with ESD voltage of (a) +0.2 kV, and (b) -0.2 kV zapping on the HCP.

4.4.3. EFT Tests

4.4.3.1. With Attenuation Network

In order to simulate the EFT-induced transient disturbance on CMOS ICs inside the microelectronic products, the attenuation network with 200 dB degradation is used in this work. The amplitude of EFT-induced transients can be adjusted through the attenuation network.

The measurement setup for EFT test combined with attenuation network is shown in Fig. 4. 16. A supply voltage of 3.3 V is used as V_{DD} and EFT generator is connected to the DUT through the attenuation network. The V_{DD} and V_{OUT} transient responses of the novel proposed on-chip transient detection circuit I are monitored by the digital oscilloscope. With such a measurement setup, the circuit function of the novel proposed on-chip transient detection circuit I after EFT tests can be evaluated. Before each EFT testing, the initial output voltage (V_{OUT}) of the novel proposed on-chip transient detection circuit I is reset to 0 V. After each EFT testing, the output voltage (V_{OUT}) level is measured to check the final voltage level and to verify the detection function. Thus, the detection function of the novel proposed on-chip transient detection circuit I can be directly evaluated with the measurement setup of EFT tests combined with attenuation network.

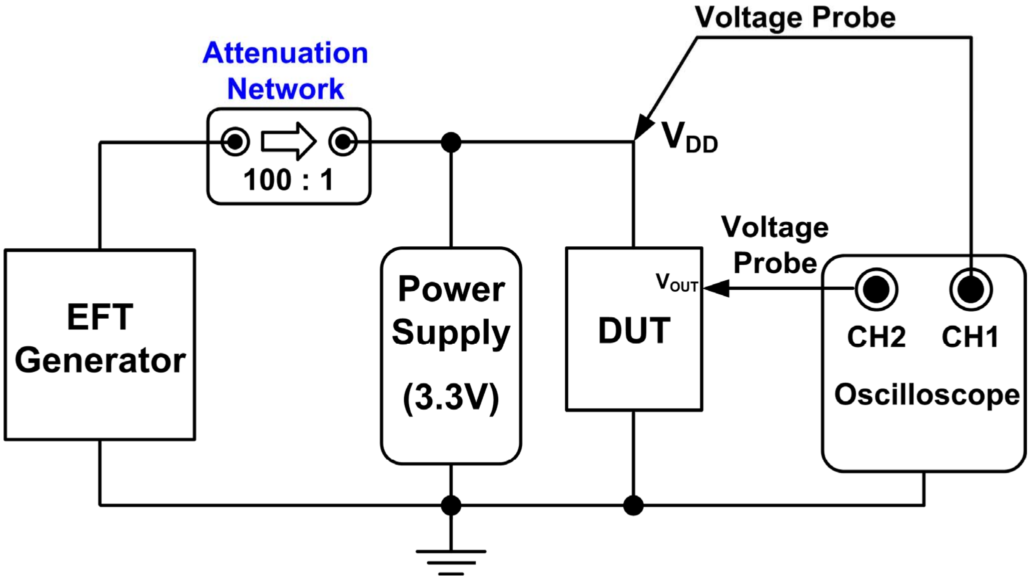
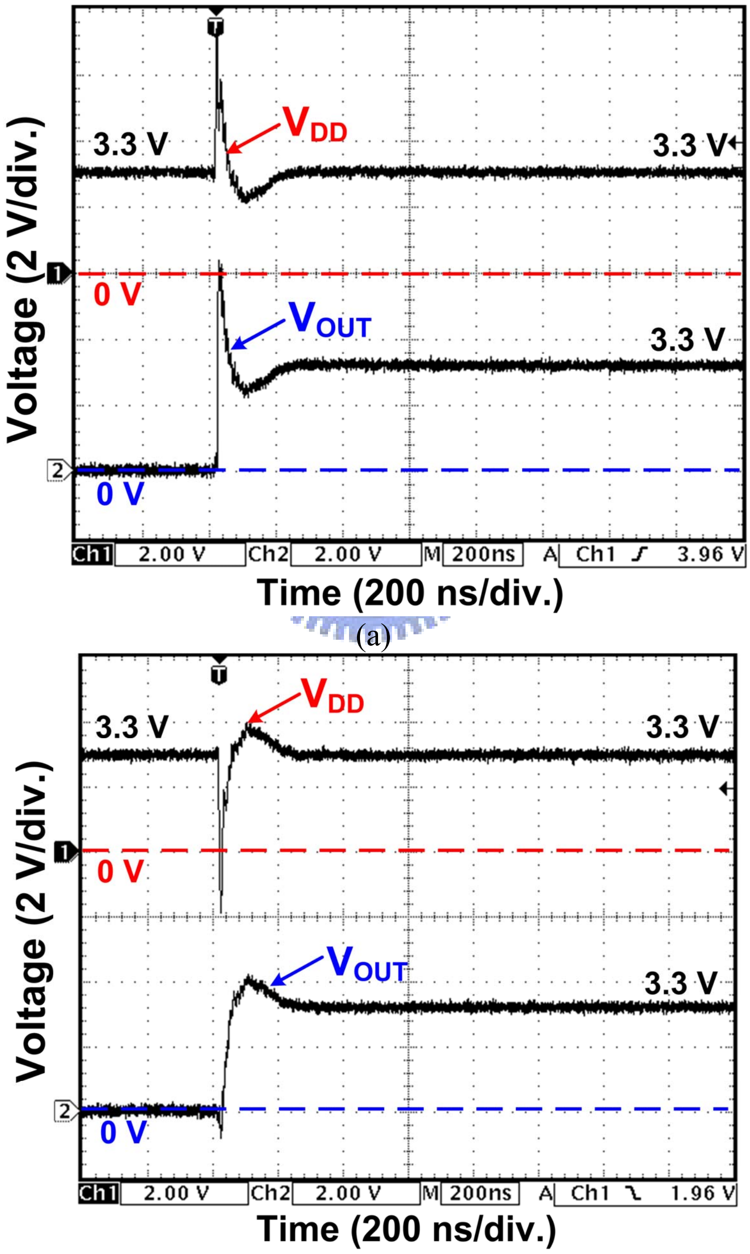


Fig. 4.16 Measurement setup for EFT test combined with attenuation network.

As shown in Fig. 4.17(a), under the EFT test with input EFT voltage of +500 V, V_{DD} begins to increase rapidly from 3.3 V and acts like positive exponential voltage pulse. During the EFT test, V_{OUT} is influenced simultaneously with positive exponential voltage pulse coupled to V_{DD} power line. After the EFT test with the input EFT voltage of +500 V, the output voltage (V_{OUT}) of the novel proposed on-chip transient detection circuit I transits from 0 V to 3.3 V. As shown in Fig. 4.17(b), under the EFT test with input EFT voltage of -500 V, V_{DD} begins to decrease rapidly from 3.3 V and acts like negative exponential voltage pulse. During the EFT test, V_{OUT} is influenced simultaneously with negative exponential voltage pulse coupled to V_{DD} power line. After the EFT test with the input EFT voltage of -500 V, the output voltage (V_{OUT}) of the novel proposed on-chip transient detection circuit I transits from 0 V to 3.3 V.



(a)

(b)

Fig. 4.17 Measured V_{DD} and V_{OUT} waveforms on the proposed on-chip transient detection circuit I under EFT tests with (a) positive, and (b) negative EFT voltages.

4.4.3.2. With Capacitance Coupling Clamp

In standard of IEC 61000-4-4, the capacitive coupling clamp has been recommended as another measurement setup to couple the EFT testing voltages into the EUT.

The capacitive coupling clamp provides the ability of coupling the fast transients and bursts to the circuit under test without any galvanic connection to the terminals of the EUT, shielding of the cables or any other part of the EUT. The coupling capacitance of the clamp depends on the diameter, material of the cables, and shielding. The typical coupling capacitance between the cable and clamp ranges from 50 pF to 200 pF. The capacitive coupling clamp is composed of a clamp unit (made of galvanizes steel, brass, copper, or aluminium) for housing the cables (flat or round) connected to the circuit under test and should be placed on the ground plane with minimum area of 1 m^2. The line should be provided at both ends with a high-voltage coaxial connector for the connection of EFT generator at either end. EFT generator is connected to the end of the clamp which is nearest to the EUT. The capacitive coupling clamp itself should be closed as much as possible to provide maximum coupling capacitance between the cable and the clamp.

The measurement setup for EFT test combined with capacitive coupling clamp is shown in Fig. 4.18. A supply voltage of 3.3 V is used as V_{DD} and the capacitive coupling clamp is connected with EFT generator to directly couple the EFT testing voltages into the V_{DD} cable line. The V_{DD} and V_{OUT} voltage waveforms of the novel proposed on-chip transient detection circuit I are monitored by the digital oscilloscope during the EFT tests. With such a measurement setup, the circuit function of the novel proposed on-chip transient detection circuit I under EFT tests combined with capacitive coupling clamp can be evaluated.

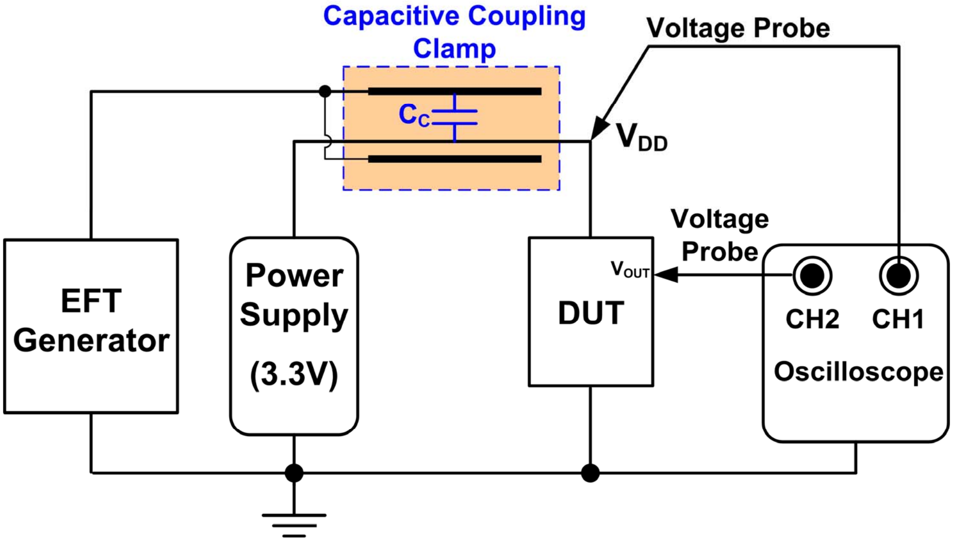
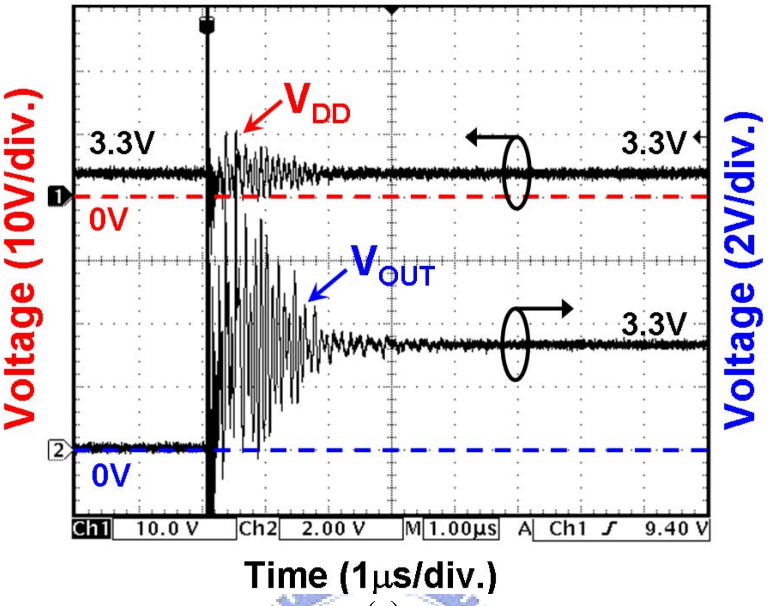
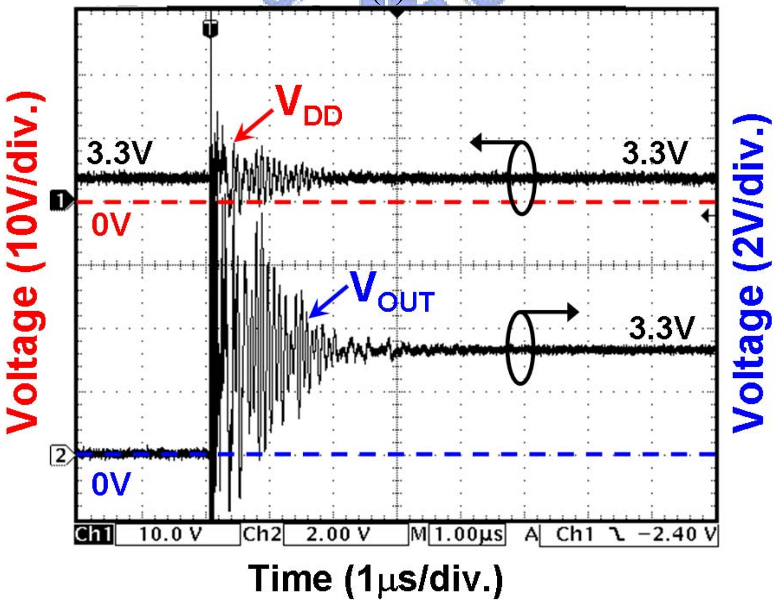


Fig. 4.18 Measurement setup for EFT test combined with capacitive coupling clamp.

Figs. 4.19(a) and 4.19(b) show the measured V_{DD} and V_{OUT} transient responses of the novel proposed on-chip transient detection circuit I under the EFT test with input EFT voltages of +200 V and -200 V, respectively.



(a)



(b)

Fig. 4.19 Measured V_{DD} and V_{OUT} transient voltage waveforms of the proposed on-chip transient detection circuit I under EFT tests with EFT voltage of (a) +200 V, and (b) -200 V by combining with capacitive coupling clamp.

As shown in Fig. 4.19(a), under the EFT tests with input EFT voltage of +200 V, V_{DD} begins to increase rapidly from 3.3 V and acts like positive-going underdamped sinusoidal voltage waveform. During the EFT test, V_{OUT} is influenced simultaneously with positive-going underdamped sinusoidal voltage coupled to V_{DD} power line. After the EFT test with the input EFT voltage of +200 V, the output voltage (V_{OUT}) of the novel proposed on-chip transient detection circuit I transits from 0 V to 3.3 V.

As shown in Fig. 4.19(b), under the EFT test with EFT voltage of -200 V, V_{DD} begins to decrease rapidly from 3.3 V and acts like negative-going underdamped sinusoidal voltage waveform. During the EFT test, V_{OUT} is influenced simultaneously with negative-going underdamped sinusoidal voltage coupled to V_{DD} power line. After the EFT test with the input EFT voltage of -200 V, the output voltage (V_{OUT}) of the novel proposed on-chip transient detection circuit I transits from 0 V to 3.3 V.

From the EFT test results shown in Fig. 4.19(a) and 4.19(b), with positive-going or negative-going underdamped sinusoidal voltage waveforms coupled to V_{DD} power line, the output voltages (V_{OUT}) of the novel proposed on-chip transient detection circuit I can be changed from 0V to the voltage level of 3.3 V. Therefore, the novel proposed on-chip transient detection circuit I can successfully memorize the occurrence of positive-going or negative-going EFT-induced underdamped sinusoidal transient disturbance.

4.5. Hardware/Firmware Co-design Application

The proposed transient detection circuit can be co-designed with firmware to provide a system solution to solve the system-level ESD issue of microelectronic products realized with CMOS ICs. It has been proven that the hardware/firmware can be co-designed can be used to effectively improve the system-level ESD robustness of the CMOS IC products.

As shown in the flowchart in the Fig. 4.20, the detection results (V_{OUT}) from the on-chip transient detection circuits can be temporarily stored as a firmware index for system check. The output states of the transient detection circuit I and the firmware index are initially cleared to logic 0 by the power-on reset circuit. The reset procedure is executed through the normal firmware reset procedure when the firmware index has a state of logic 0. When the fast electrical transient happens, the on-chip transient detection circuit can detect the fast electrical transient to change the output states from logic 0 to logic 1. At the same time, the firmware index is re-stored at logic 1, and the system executes the recover procedure to recover all system functions to a stable state as soon as possible. After recover procedures, the output state of the proposed on-chip transient detection circuit I and the firmware index are re-set to logic 0 again for detecting the next ESD and EFT events.

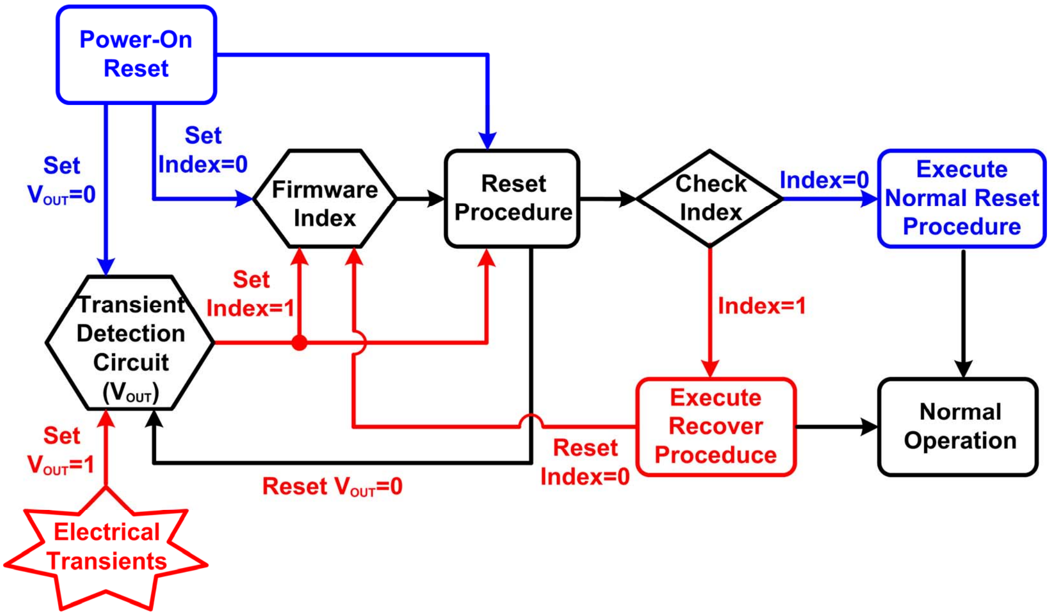
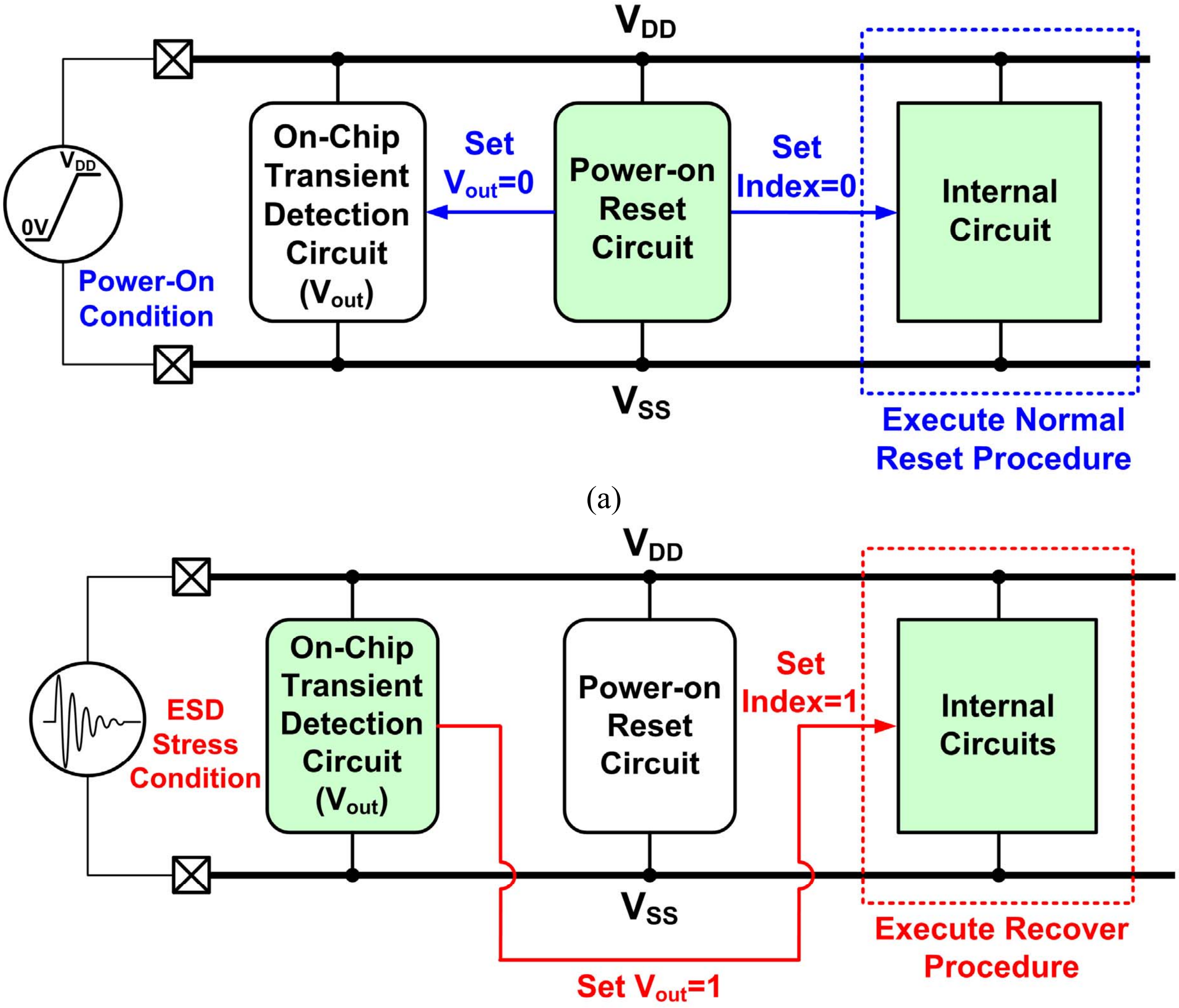


Fig. 4.20 The hardware/firmware co-design flowchart to execute reset or recover procedures.

For example, to realize system-level ESD protection function, a hardware/firmware co-design solution combined with the transient detection circuit and the power-on reset circuit has been analyzed. Under the normal power-on condition, the V_{DD} power-on voltage waveform has a rise time in the order of millisecond (ms). As there is no input signal except V_{DD} power-on voltage waveform, the power on reset circuit should be designed with the same internal delay as the order of millisecond. Thus, the output signal of power-on reset circuit can set the firmware index to logic 0, as shown in Fig. 4.21(a). However, there are some mis-triggered conditions in power-on reset circuit. For example, fast power-up time (in the range of microsecond) may create difficult situations for the power-on reset circuit to work properly. Therefore a transient detection circuit is designed to sense fast electrical transients on power lines and combined with the power-on reset circuit in order to provide hardware/firmware co-design solution for system-level ESD issues.

Due to the difference in the rise times between the ESD voltage and the V_{DD} power-on voltage, the on–chip transient detection circuit is designed to sense fast electrical transients and set the flag signal to logic 1, as shown in Fig. 4.21(b). Then, the firmware can execute the recover procedure to recover all the electrical functions to a stable state as soon as possible. After the reset and recover procedures, the firmware index is reset to logic 0 again for detecting next electrical transient disturbance events.

By including the on-chip transient detection circuit and an additional firmware index into the chip, the firmware flowchart shown in Fig. 4.20 can be used to improve the system-level ESD and EFT robustness of microelectronic products. Such hardware/firmware co-design method can provide an effective system solution to solve the system-level ESD and EFT issues in microelectronics system realized with CMOS ICs.



(a)

(b)

Fig. 4.21 Hardware/firmware operation during (a) power-on reset condition, and (b) system-level ESD stress.

4.6. Conclusion

A novel RC-based on-chip transient detection circuit I have been proposed and verified on silicon. The detection performance under different positive and negative electrical transients had been investigated by HSPICE. The experimental results have verified that the proposed on-chip transient detection circuit I can detect and memorize the occurrence of electrical transients due to system-level ESD and EFT zapping. In the system applications, the proposed on-chip transient detection circuit I can be further used as firmware recover index and combined with firmware design to provide an effective solution against the malfunction caused by system-level ESD or EFT zapping on microelectronic products.

Chapter 5

On-Chip Transient Detection Circuit Design for Electrical Transient Disturbance Protection (Scheme II)

A new on-chip transient detection circuit II is proposed to detect the electrical transient under the system-level ESD or EFT tests. It had been reported that the hardware/firmware co-design can effectively improve the transient disturbance susceptibility of CMOS ICs in microelectronic products. As the conceptual hardware/firmware co-design, when the electrical transient disturbance happens, the detection results from the on-chip transient detection circuit II can be stored as a firmware index to start the system recovery procedure after the disturbance. The circuit function to detect different positive or negative electrical transients has been investigated by HSPICE simulation and verified by silicon chip. The transient-induced latchup (TLU) measurement method, the system-level ESD gun, and the EFT generator are used to evaluate the detection function of the new proposed on-chip transient detection circuit. The experimental results in a 0.18-μm CMOS process have verified that the new proposed on-chip transient detection circuit II can successfully detect and memorize the occurrence of electrical transients during system-level ESD or EFT testing conditions.

5.1. Background

In order to protect microelectronic system against transient disturbance events, the traditional solution used in microelectronic products is to add some discrete noise-bypassing components or board-level noise filters into the printed circuit board (PCB) to decouple, bypass, or absorb the electrical transient energy under system-level electrical transient disturbance conditions. However, the additional discrete noise-bypassing components substantially increase the total cost of microelectronic products. Therefore, the chip-level solutions to meet high transient disturbance immunity specification for microelectronic products without additional discrete noise-decoupling components added on PCB are highly desired by IC industry.

5.2. On-Chip Transient Detection Scheme II Designed with 1.8-V Devices

The new on-chip transient detection circuit II is designed to detect the positive or negative fast electrical transients after the system-level ESD or EFT tests. Under the normal power supply condition (V_{DD}=1.8 V), the output state (V_{OUT}) of the new proposed on-chip transient detection circuit II is kept at 0V as logic “0.” After the transient disturbance, the output state (V_{OUT}) of the new proposed on-chip transient detection circuit II will transit from 0 V to 1.8 V as logic “1.” Therefore, the new proposed on-chip transient detection circuit II can memorize the occurrence of transient disturbance events.

Fig. 5.1 shows the new proposed on-chip transient detection circuit II. The NMOS (M_{nr}) is used to provide the initial reset function to set the initial voltage level to 0 V at the node V_1 and the output node (V_{OUT}). In Fig. 5.1, the node V_X is biased at V_{DD} during the normal operating condition. Under the system-level ESD or EFT tests, the transient voltage coupled to V_{DD} line has a fast rise time in the order of nanosecond (ns). The voltage level of V_X has much slower voltage response than the voltage level at V_{DD} because the RC circuit has a time constant in the order of microsecond (μs). Due to the longer delay of the voltage increase at the node V_X, the PMOS device (M_{P1}) can be turned on by the overshooting transient voltage at V_{DD} to pull up the voltage level at the node V_1. Therefore, the logic level stored at the node V_1 can be changed during transient disturbance events. Finally, the output voltage of the new proposed on-chip transient detection circuit II can transit from 0 V to 1.8 V to memorize the occurrence of electrical transient disturbance after system-level ESD or EFT tests.

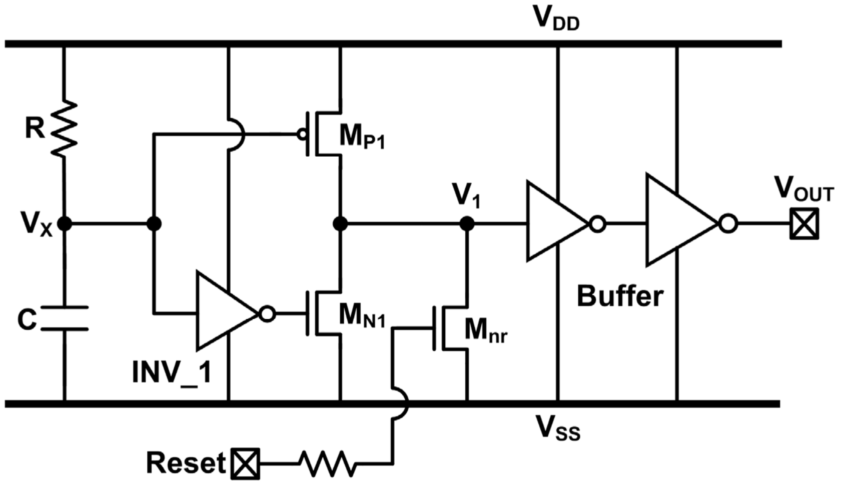


Fig. 5.1 The new proposed on-chip transient detection circuit II.

5.3. HSPICE Simulation Results

5.3.1. System-Level ESD Zapping Conditions

From the measured electrical transient waveforms shown in Fig. 1.6, the underdamped sinusoidal voltage waveform on power line of CMOS IC during the system-level ESD stress has been observed. There, a sinusoidal time-dependent voltage source with damping factor parameter given by

$$V(t) = V_0 + V_a \cdot \sin(2\pi f(t - t_d)) \cdot \exp(-(t - t_d)D_a) \tag{1}$$

is used to simulate an underdamped sinusoidal voltage on the power lines of the new proposed on-chip transient detection circuit II. With the proper parameters (including the applied voltage amplitude V_a, initial dc voltage V_0, damping factor D_a, frequency f, and time delay t_d), the underdamped sinusoidal voltage can be used to simulate the electrical transient waveforms under system-level ESD tests. In HSPICE simulation with positive-going or negative-going underdamped sinusoidal waveforms, the same parameters of $D_a = 2\text{x}10^7\ \text{s}^{-1}$, f = 50 MHz, and t_d = 300 ns are used (which is corresponding to the measured transient waveforms in Fig. 1.6). For the positive-going (negative-going) underdamped sinusoidal waveform, the polarity of V_a parameter is positive (negative). In addition, V_0 is 1.8 V as the initial dc voltage on the V_{DD} line of the new proposed on-chip transient detection circuit II this work, which is fabricated in a 0.18-μm CMOS process.

The simulated V_{DD} and V_{OUT} waveforms of the new proposed on-chip transient detection circuit II with a positive-going underdamped sinusoidal voltage on V_{DD} line are shown in Fig. 5.2(a). The positive-going underdamped sinusoidal voltage with amplitude of +10 V is used to simulate the coupling ESD transient noise under the system-level ESD test. From the simulated waveforms, V_{DD} begins to increase rapidly from 1.8 V and V_{OUT} also acts with a positive-going underdamped sinusoidal voltage waveform during the simulated transient disturbance on V_{DD} line. After this disturbance duration, V_{DD} returns to its normal voltage level of 1.8 V and the output state (V_{OUT}) of the new proposed on-chip transient detection circuit II is changed from 0 V to 1.8 V, as shown in Fig. 5.2(a). As a result, the new proposed on-chip transient detection circuit II can detect the occurrence of positive-going ESD-induced underdamped sinusoidal transient disturbance on V_{DD} line.

The simulated V_{DD} and V_{OUT} waveforms of the new proposed on-chip transient detection circuit II with a negative-going underdamped sinusoidal voltage on V_{DD} are shown in Fig.

5.2(b). The negative-going underdamped sinusoidal voltage with amplitude of -10 V is used to simulate the coupling ESD transient noise under the system-level ESD test with negative voltage. From the simulated waveforms, V_{DD} begins to decrease rapidly from 1.8 V and V_{OUT} also acts with a negative-going underdamped sinusoidal voltage waveform during the simulated transient disturbance on V_{DD} line. After this disturbance duration, V_{DD} returns to its normal voltage level of 1.8 V and the output state (V_{OUT}) of the new proposed on-chip transient detection circuit II is changed from 0 V to 1.8 V, as shown in Fig. 5.2(b). Therefore, the new proposed on-chip transient detection circuit II can detect the occurrence of negative-going ESD-induced underdamped sinusoidal transient disturbance on V_{DD} line.

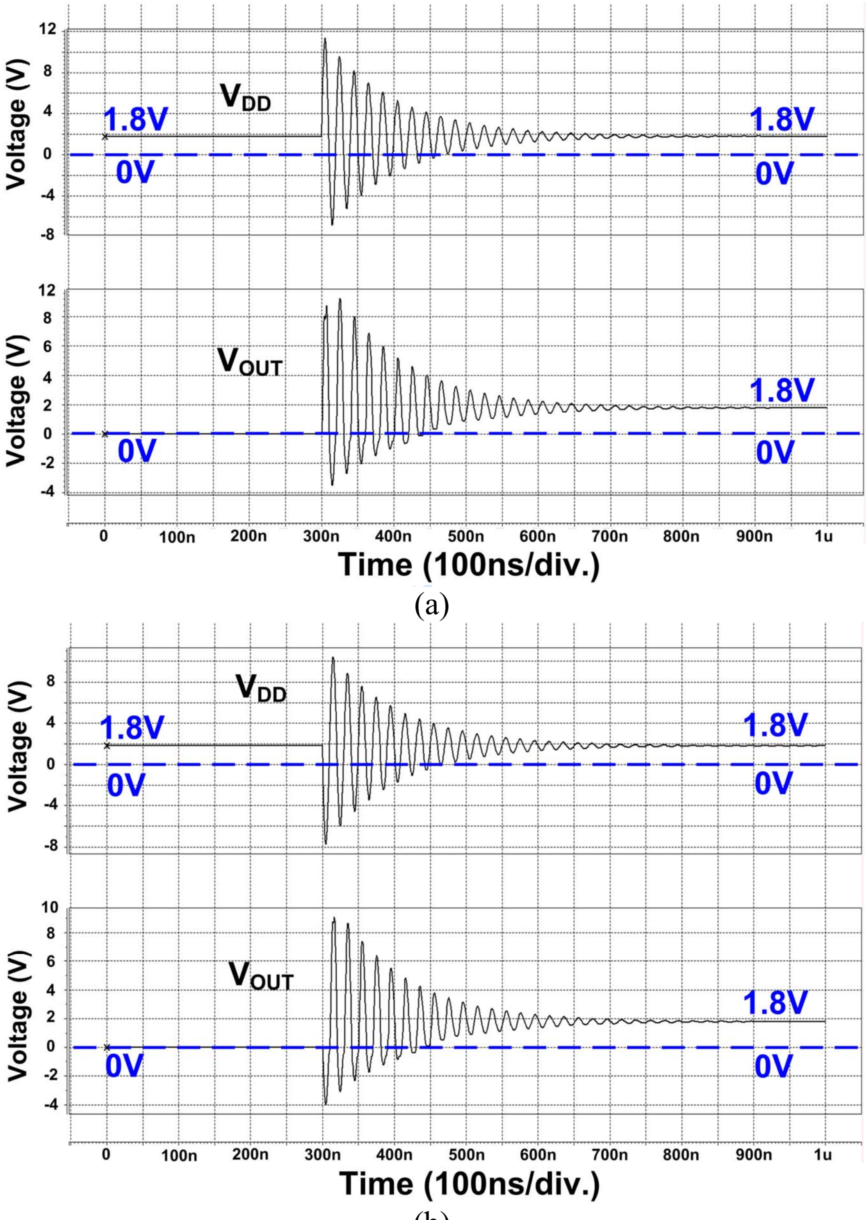


Fig. 5.2 Simulated V_{DD} and V_{OUT} waveforms of the transient detection circuit II under system-level ESD test with (a) positive, and (b) negative underdamped sinusoidal voltages.

From aforementioned simulation results, the output state of the new proposed on-chip transient detection circuit II can be changed and kept at 1.8 V after the system-level ESD events. Therefore, the new proposed transient detection circuit can memorize the occurrence of system-level ESD events.

5.3.2. EFT Zapping Conditions

For microelectronic products, the shielding plate is often designed into microelectronic products to bypass or reduce the EFT-induced electrical transient disturbance. Therefore, the electrical transients injected into CMOS ICs inside the microelectronic products can be degraded with smaller amplitude compared with the original testing voltage. Therefore, the EFT-induced transients with different degraded amplitudes are taken into considerations in HSPICE simulation on the new proposed on-chip transient detection circuit II.

From the measured electrical transient waveforms shown in Figs. 5.3(a) and 5.3(b), the approximated exponential voltage pulse waveforms during the EFT tests have been observed. There, an exponential pulse time-dependent voltage source with rise/fall time constant parameters is used to simulate EFT-induced transient disturbance on the new proposed on-chip transient detection circuit II. The rising edge of this exponential time-dependent voltage pulse is expressed as

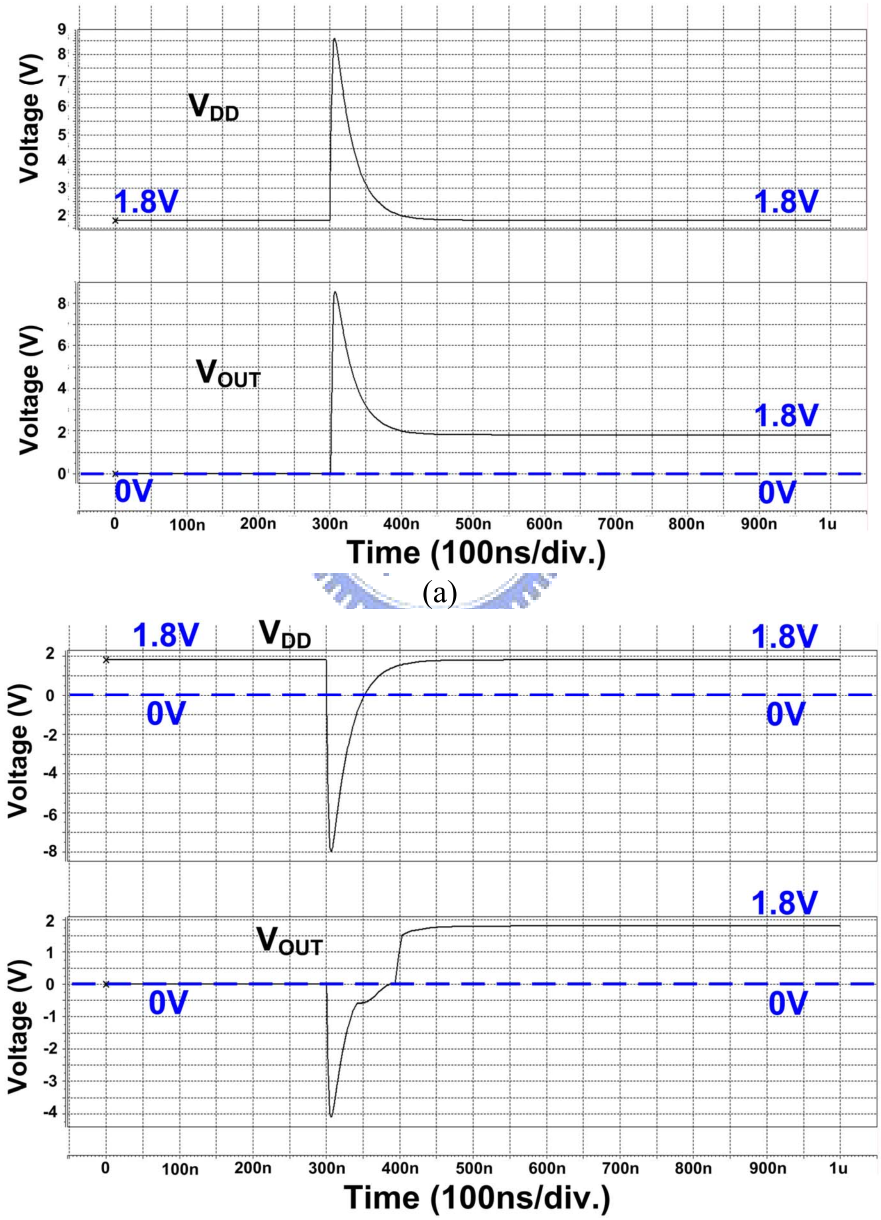
$$V_{p(rise)}(t) = V_1 + \left(V_2 - V_1\right) \times \left[1 - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right)\right], \text{ when } t_{d1} \le t \le t_{d2}. \qquad (2)$$

The falling edge of this exponential time-dependent voltage pulse is expressed as

$$V_{p(fall)}(t) = V_1 + \left(V_2 - V_1\right) \times \left[1 - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right)\right] + \left(V_1 - V_2\right)\left[1 - \exp\left(-\frac{t - t_{d2}}{\tau_2}\right)\right], \text{ when } t \ge t_{d2}. \qquad (3)$$

With the proper parameters (including the rise time constant τ_1, fall time constant τ_2, rise time delay t_{d1}, fall time delay t_{d2}, initial dc voltage value V_1, and exponential pulse voltage value V_2), the exponential voltage pulse can be constructed to simulate the EFT-induced disturbance under EFT tests. In HSPICE simulation with positive or negative exponential voltage pulse waveforms, the same parameters of $\tau_1 = 3$ ns, $\tau_2 = 25$ ns, and $t_{d2} - t_{d1} = 10$ ns are used (which is corresponding to the measured transient waveforms in Figs. 1.9(a) and 1.9(b)). For the positive exponential voltage pulse, the value of V_2 parameter is larger than the value of V_1 parameter. For the negative exponential voltage pulse, the polarity of V_2 - V_1 parameter is negative. In addition, V_1 is 1.8 V as the initial dc voltage on the V_{DD} line of the new proposed on-chip transient detection circuit II.

The simulated V_{DD} and V_{OUT} waveforms of the new proposed on-chip transient detection circuit II with a positive and negative exponential pulse transient disturbance on V_{DD} line are shown in Fig. 5.3(a) and 5.3(b), respectively.



(a)

(b)

Fig. 5.3 Simulated V_{DD} and V_{OUT} waveforms of the new proposed on-chip transient detection circuit II under EFT tests with (a) positive, and (b) negative exponential voltage pulse waveforms coupled to V_{DD}.

The simulated V_{DD} and V_{OUT} waveforms of the new proposed on-chip transient detection circuit II with a positive exponential pulse transient disturbance on V_{DD} line are shown in Fig. 5.3(a). The exponential voltage pulse with amplitude of +10 V is used to simulate the coupling positive transient disturbance under the EFT test. From the simulated waveforms, V_{DD} begins to increase rapidly from 1.8 V and V_{OUT} also acts with a positive exponential voltage pulse waveform during the simulated transient disturbance on V_{DD} line. After the transient disturbance duration, V_{DD} returns to its normal voltage level of 1.8 V and the output state (V_{OUT}) of the new proposed on-chip transient detection circuit II transits from 0 V to 1.8 V, as shown in Fig. 5.3(a). As a result, the new proposed on-chip transient detection circuit II can detect the occurrence of simulated positive EFT-induced exponential pulse transient disturbance.

The simulated V_{DD} and V_{OUT} waveforms of the new proposed on-chip transient detection circuit II with a negative exponential pulse transient disturbance on V_{DD} line are shown in Fig. 5.3(b). The exponential voltage pulse with amplitude of -10 V is used to simulate the coupling negative transient disturbance under the EFT test. From the simulated waveforms, V_{DD} begins to decrease rapidly from 1.8 V and V_{OUT} also acts with a negative exponential voltage pulse during the simulated transient disturbance on V_{DD} line. After the transient disturbance duration, V_{DD} returns to its normal voltage level of 1.8 V and the output state (V_{OUT}) of the new proposed on-chip transient detection circuit II transits from 0 V to 1.8 V, as shown in Fig. 5.3(b). As a result, the new proposed on-chip transient detection circuit II can detect the occurrence of simulated negative EFT-induced exponential pulse transient disturbance.

From the aforementioned simulation results, after the positive or negative EFT-induced transient disturbance on V_{DD} line, the output state of the new proposed on-chip transient detection circuit II can be changed from 0 V and kept at 1.8 V. Therefore, the new proposed on-chip transient detection circuit II can successfully memorize the occurrence of simulated positive or negative EFT-induced exponential pulse transient disturbance.

The new proposed on-chip transient detection circuit II has been designed and fabricated in a 0.18-μm 1P5M CMOS process. The fabricated chip for transient disturbance tests is shown in Fig. 5.4. The TLU measurement method, the system-level ESD gun, and the EFT generator are used to evaluate the detection function of the new proposed on-chip transient detection circuit II after EFT-induced electrical transient disturbance.

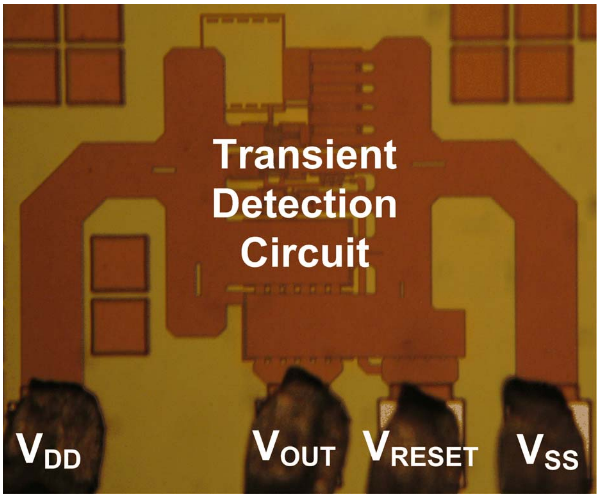


Fig. 5.4 Die photo of the new proposed on-chip transient detection circuit II.

5.4. Experimental Results

5.4.1. TLU Tests

In the TLU measurement setup shown in Fig. 5.5, a charging capacitance of 200pF is used to store charges offered by the TLU-triggering source, V_{Charge}, and then these stored charges are discharged to the device under test (DUT) through the relay. The intended underdamped sinusoidal voltage can be produced to simulate the transient voltage on the power pins of CMOS ICs under the system-level ESD test, no matter which polarity (positive or negative) the ESD voltage is. Moreover, a small current-limiting resistance of 5Ω is recommended to protect the DUT from electrical-over-stress (EOS) damage during a high-current (low-impedance) latchup state. The supply voltage of 1.8 V is used as V_{DD} and the trigger source is directly connected to DUT through the relay in the measurement setup.

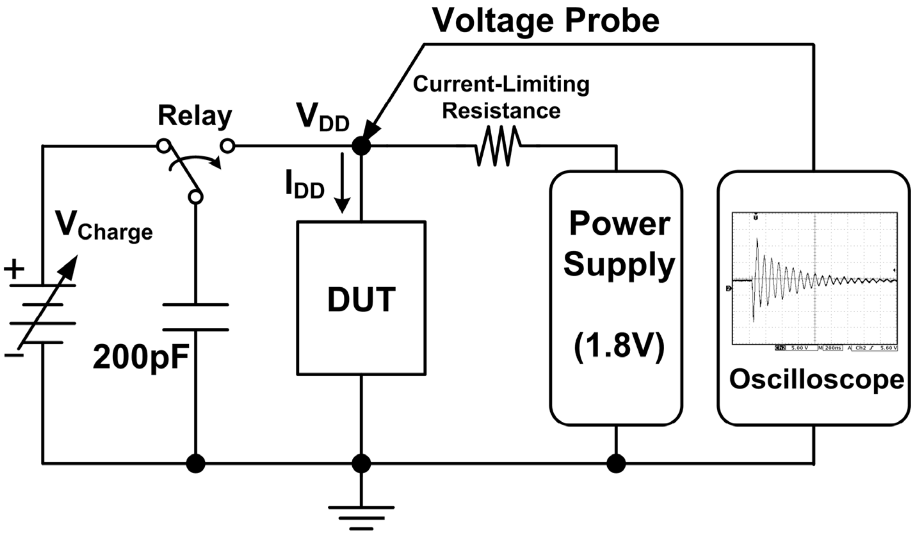
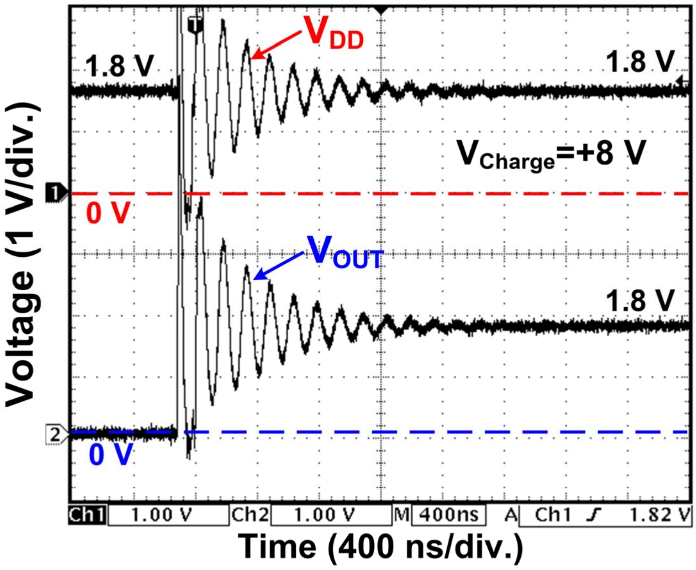
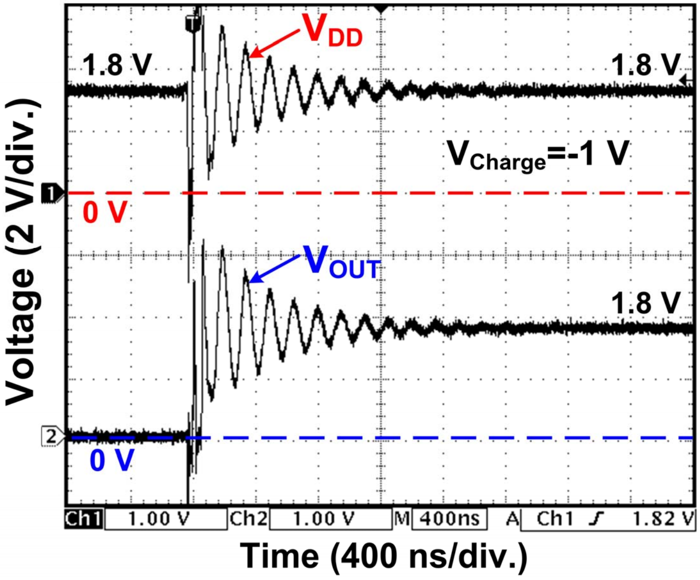


Fig. 5.5 Measurement setup for transient-induced latchup (TLU).

Figs. 5.6(a) and 5.6(b) show the measured V_{DD} and V_{OUT} transient responses of the new proposed on-chip transient detection circuit II under the TLU test with V_{Charge} of +8 V and -1 V, respectively.



(a)



(b)

Fig. 5.6 Measured V_{DD} and V_{OUT} waveforms on the new proposed on-chip transient detection circuit II under TLU tests with V_{Charge} of (a) +8 V, and (b) -1 V.

As shown in Fig. 5.6(a), under the TLU test with V_{Charge} of +8 V, V_{DD} begins to increase rapidly from 1.8 V and acts like positive-going underdamped sinusoidal voltage waveform. During the TLU test, V_{OUT} is influenced simultaneously with positive-going underdamped sinusoidal voltage coupled to V_{DD} power line. After the TLU test with the V_{Charge} of +8 V, the output voltage (V_{OUT}) of the new proposed on-chip transient detection circuit II can transit from 0 V to 1.8 V. As shown in Fig. 5.6(b), under the TLU test with V_{Charge} of -1 V, V_{DD} begins to decrease rapidly from 1.8V and acts like negative-going underdamped sinusoidal voltage waveform. During the TLU test, V_{OUT} is influenced simultaneously with negative-going underdamped sinusoidal voltage coupled to V_{DD} power line. After the TLU test with the V_{Charge} of -1 V, the output voltage (V_{OUT}) of the new proposed on-chip transient detection circuit II can transit from 0 V to 1.8 V.

From the TLU test results, the new proposed on-chip transient detection circuit II can successfully memorize the occurrence of electrical transients. With positive or negative underdamped sinusoidal voltages coupled to V_{DD} power line, the output voltages (V_{OUT}) of the new proposed on-chip transient detection circuit II can be changed from 0V to 1.8V after TLU tests.

5.4.2. System-level ESD Tests

Fig. 5.7 shows the standard measurement setup of the system-level ESD test with indirect contact-discharge test mode. The measurement setup of system-level ESD test consists of a wooden table on the grounded reference plane (GRP). In addition, an insulation plane is used to separate the EUT from the horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470 kΩ resistors in series. When the ESD gun zaps the HCP, the electromagnetic interference (EMI) coming from ESD gun will be coupled into all CMOS ICs inside EUT. The power lines of CMOS ICs inside EUT will be disturbed by the ESD-coupled energy.

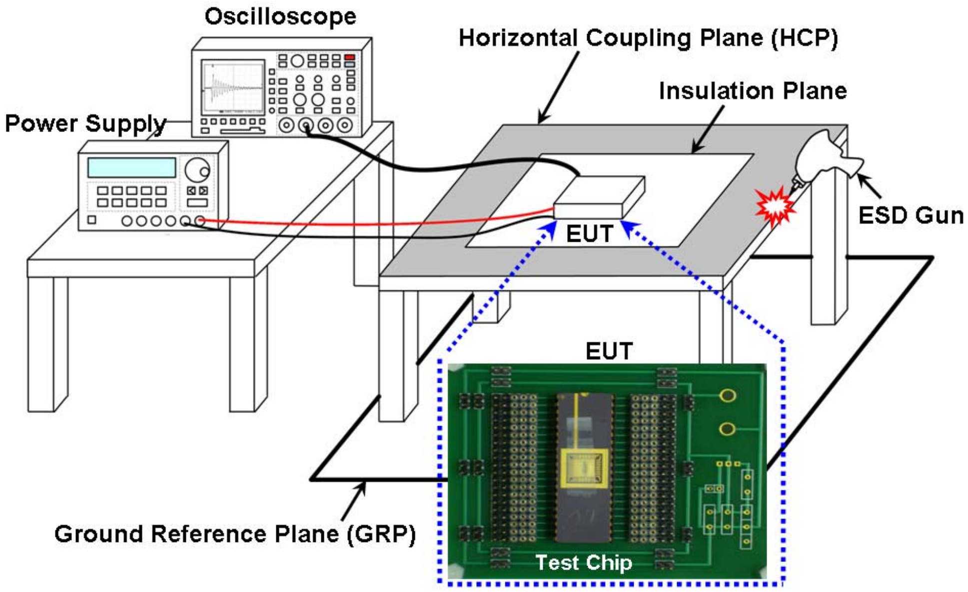
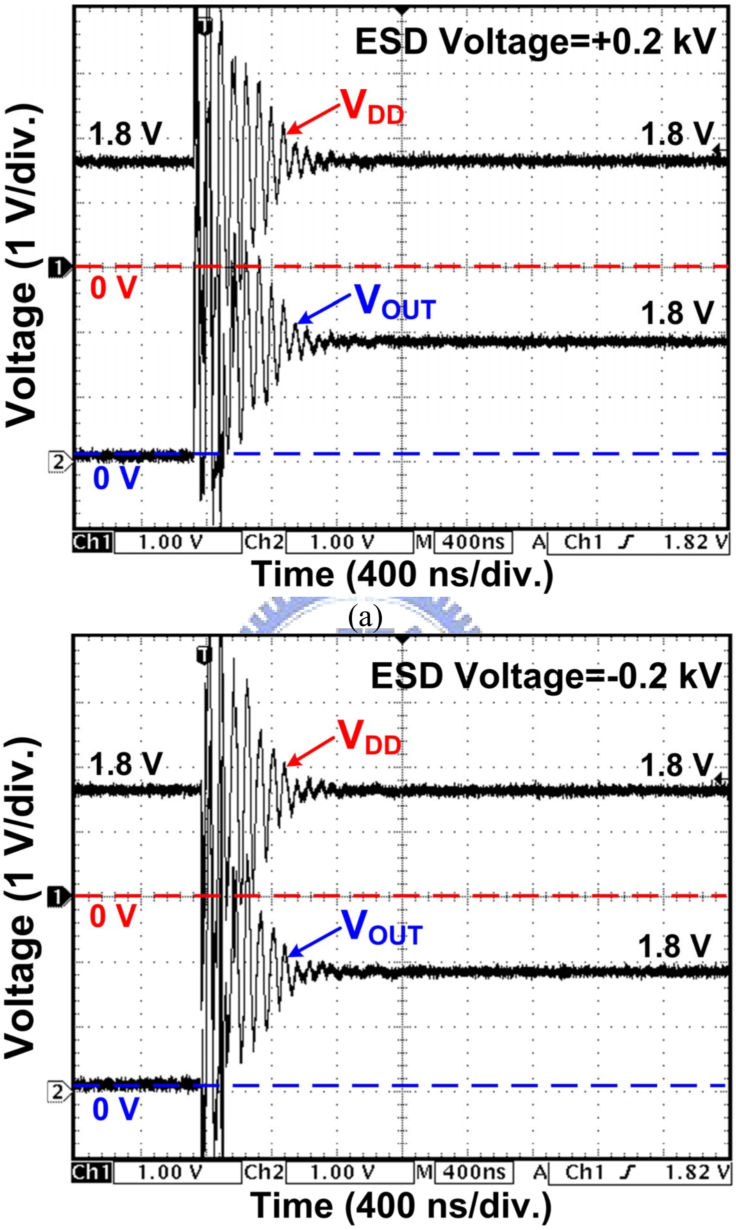


Fig. 5.7 Measurement setup for system-level ESD test with indirect contact-discharge test mode to evaluate the detection function of the fabricated on-chip transient detection circuit II.

Figs. 5.8(a) and 5.8(b) show the measured V_{DD} and V_{OUT} transient responses of the new proposed on-chip transient detection circuit II under system-level ESD test with the ESD voltage of +0.2 kV and -0.2 kV zapping on the HCP, respectively.



(a)

(b)

Fig. 5.8 Measured V_{DD} and V_{OUT} transient voltage waveforms of the new proposed on-chip transient detection circuit II under system-level ESD tests with ESD voltage of (a) +0.2 kV, and (b) -0.2 kV.

The measured V_{DD} and V_{OUT} waveforms of the new proposed on-chip transient detection circuit II under system-level ESD test with the ESD voltage of +0.2 kV zapping on the HCP are shown in Fig. 5.8(a). V_{DD} begins to increase rapidly from the normal voltage of +1.8 V.

Meanwhile, V_{OUT} is disturbed under such a high-energy ESD stress. During the period with positive-going ESD-induced electrical transient disturbance, V_{DD} and V_{OUT} are influenced simultaneously. Finally, the output voltage (V_{OUT}) of the new proposed on-chip transient detection circuit II transits from 0 V to 1.8 V. Therefore, the new proposed on-chip transient detection circuit II can sense the positive-going electrical transient on the power line and memorize the occurrence of system-level ESD event.

The measured V_{DD} and V_{OUT} transient voltage waveforms of the new proposed on-chip transient detection circuit II with the ESD voltage of -0.2 kV zapping on the HCP under system-level ESD test are shown in Fig. 5.8(b). During the negative-going ESD-induced electrical transient disturbance on V_{DD} power line, V_{OUT} is disturbed simultaneously. After the system-level ESD test with the ESD voltage of -0.2 kV, V_{OUT} transits from 0 V to 1.8 V.

From the experimental results, the new proposed on-chip transient detection circuit II can indeed detect and memorize the occurrence of positive or negative electrical transients after system-level ESD tests.

5.4.3. EFT Tests

5.4.3.1. With Attenuation Network

The measurement setup for EFT test combined with attenuation network is shown in Fig. 5.9. A supply voltage of 1.8 V is used as V_{DD} and EFT generator is connected to the DUT through the attenuation network. The V_{DD} and V_{OUT} transient responses of the new proposed on-chip transient detection circuit II are monitored by the digital oscilloscope.

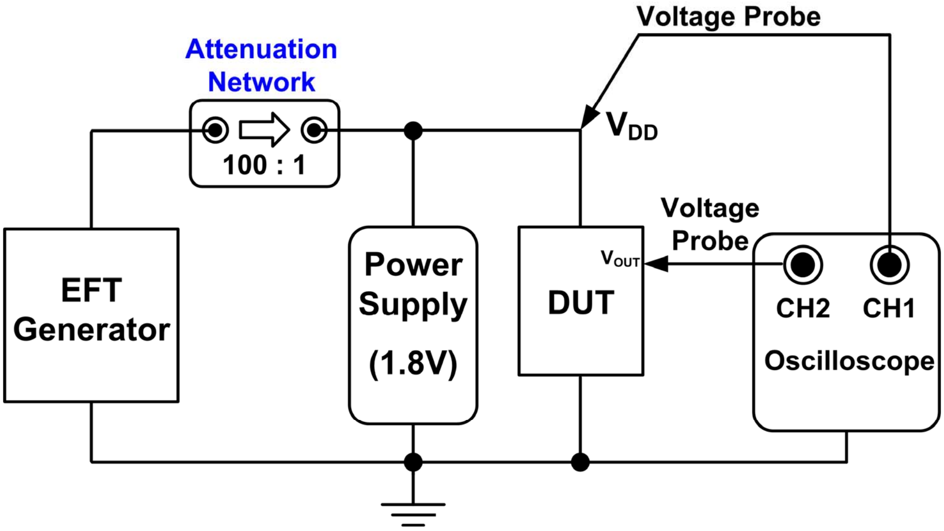
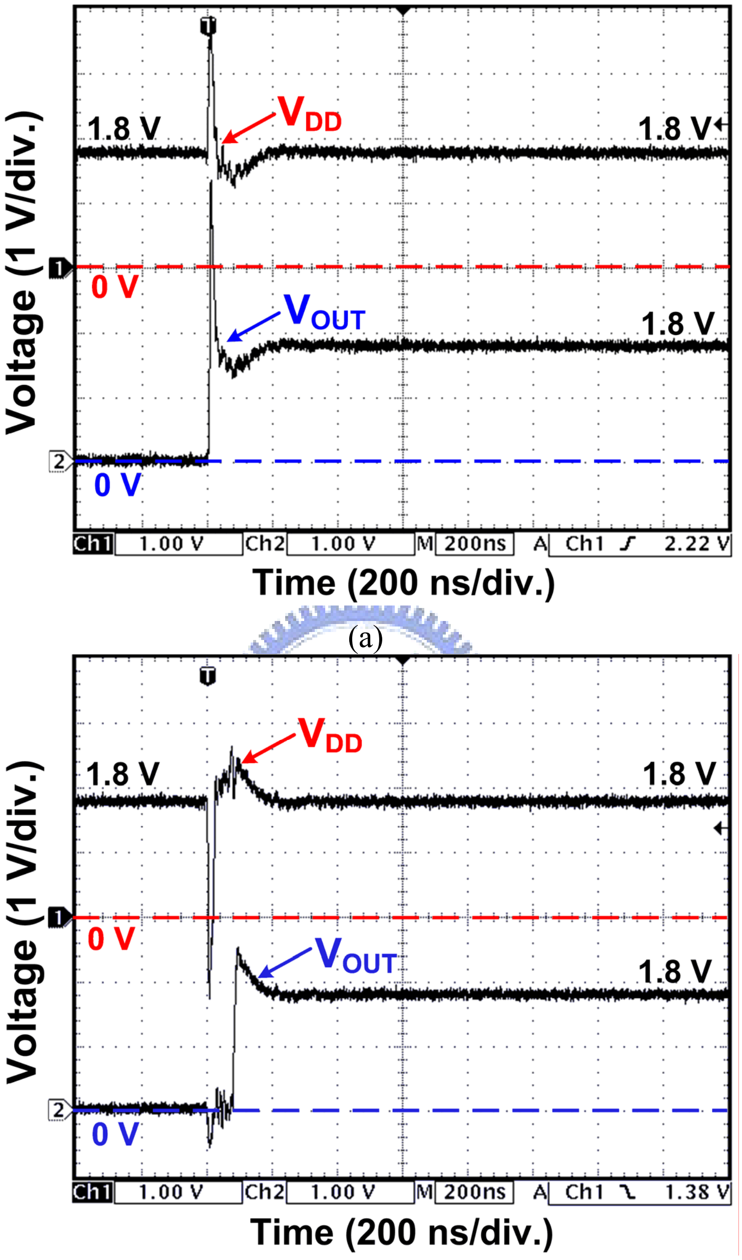


Fig. 5.9 Measurement setup for EFT test combined with attenuation network.

Figs. 5.10(a) and 5.10(b) show the measured V_{DD} and V_{OUT} transient responses of the new proposed on-chip transient detection circuit II under the EFT tests with input EFT voltages of +200 V and -300 V, respectively.



(a)

(b)

Fig. 5.10 Measured V_{DD} and V_{OUT} waveforms on the new proposed on-chip transient detection circuit II under EFT tests with (a) positive, and (b) negative EFT voltages combined with attenuation network.

As shown in Fig. 5.10(a), under the EFT test with input EFT voltage of +200 V, V_{DD} begins to increase rapidly from 1.8 V and acts like positive exponential voltage pulse. During the EFT test, V_{OUT} is influenced simultaneously with positive exponential voltage pulse coupled to V_{DD} power line. After the EFT test with the input EFT voltage of +200 V, the output voltage (V_{OUT}) of the new proposed on-chip transient detection circuit II transits from 0 V to 1.8 V. As shown in Fig. 5.10(b), under the EFT test with input EFT voltage of -300 V, V_{DD} begins to decrease rapidly from 1.8 V and acts like negative exponential voltage pulse. During the EFT test, V_{OUT} is influenced simultaneously with negative exponential voltage pulse coupled to V_{DD} power line. After the EFT test with the input EFT voltage of -300 V, the output voltage (V_{OUT}) of the new proposed on-chip transient detection circuit II transits from 0 V to 1.8 V.

From the EFT test results shown in Figs. 5.10(a) and 5.10(b), with positive or negative exponential voltage pulses coupled to V_{DD} power line, the output voltages (V_{OUT}) of the new proposed on-chip transient detection circuit can be changed from 0 V to 1.8 V. Therefore, the new proposed on-chip transient detection circuit II can successfully memorize the occurrence of EFT-induced exponential pulse transient disturbance.

5.4.3.2. With Capacitance Coupling Clamp

The measurement setup for EFT test combined with capacitive coupling clamp is shown in Fig. 5.11. A supply voltage of 1.8V is used as V_{DD} and the capacitive coupling clamp is connected with EFT generator to directly couple the EFT testing voltages into the V_{DD} cable line. The V_{DD} and V_{OUT} voltage waveforms of the new proposed on-chip transient detection circuit II are monitored by the digital oscilloscope during the EFT tests. With such a measurement setup, the circuit function of the new proposed on-chip transient detection circuit II under EFT tests combined with capacitive coupling clamp can be evaluated.

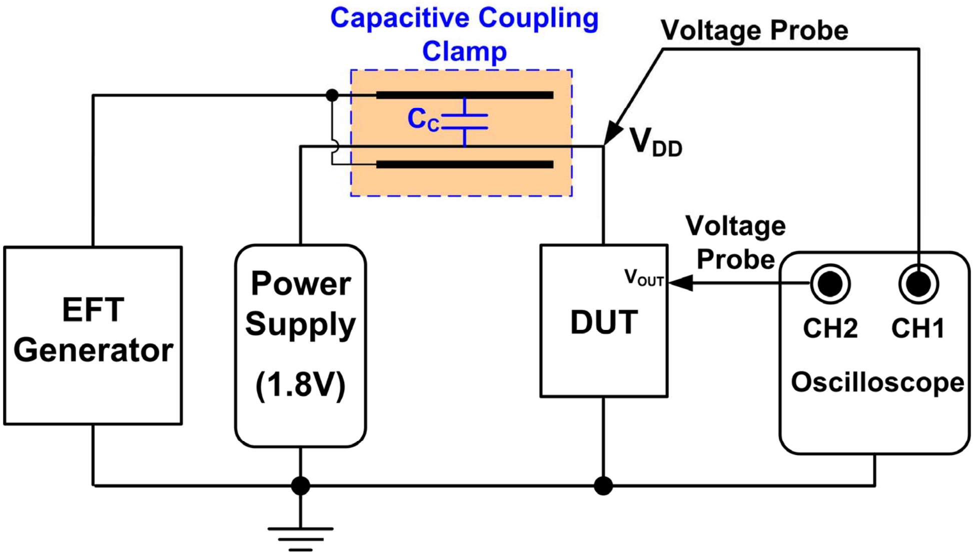
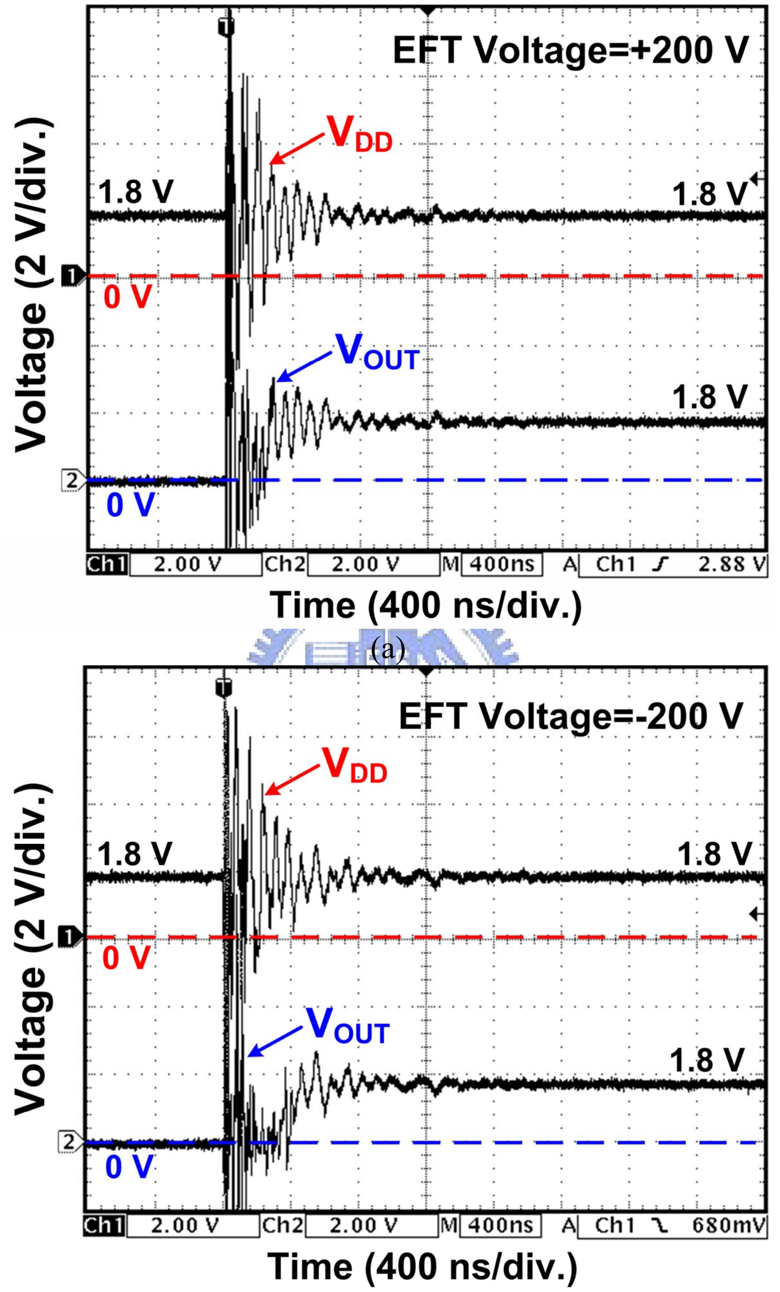


Fig. 5.11 Measurement setup for EFT test combined with capacitive coupling clamp.

Figs. 5.12(a) and 5.12(b) show the measured V_{DD} and V_{OUT} transient responses of the new proposed on-chip transient detection circuit II under the EFT test with input EFT voltages of +200 V and -200 V, respectively.



(a)

(b)

Fig. 5.12 Measured V_{DD} and V_{OUT} transient voltage waveforms of the new proposed on-chip transient detection circuit II under EFT tests with EFT voltage of (a) +200 V, and (b) -200 V combined with capacitive coupling clamp.

As shown in Fig. 5.12(a), under the EFT tests with input EFT voltage of +200 V, V_{DD} begins to increase rapidly from 1.8V and acts like positive-going underdamped sinusoidal voltage waveform. During the EFT test, V_{OUT} is influenced simultaneously with positive-going underdamped sinusoidal voltage coupled to V_{DD} power line. After the EFT test with the input EFT voltage of +200 V, the output voltage (V_{OUT}) of the new proposed on-chip transient detection circuit II transits from 0 V to 1.8 V. As shown in Fig. 5.12(b), under the EFT test with EFT voltage of -200 V, V_{DD} begins to decrease rapidly from 1.8 V and acts like negative-going underdamped sinusoidal voltage waveform. During the EFT test, V_{OUT} is influenced simultaneously with negative-going underdamped sinusoidal voltage coupled to V_{DD} power line. After the EFT test with the input EFT voltage of -200 V, the output voltage (V_{OUT}) of the new proposed on-chip transient detection circuit II transits from 0 V to 1.8 V.

From the EFT test results shown in Fig. 5.12(a) and 5.12(b), with positive-going or negative-going underdamped sinusoidal voltage waveforms coupled to V_{DD} power line, the output voltages (V_{OUT}) of the new proposed on-chip transient detection circuit II can be changed from 0 V to the voltage level of 1.8 V. Therefore, the new proposed on-chip transient detection circuit II can successfully memorize the occurrence of positive-going or negative-going EFT-induced underdamped sinusoidal transient disturbance.

5.5. Conclusion

A new on-chip transient detection circuit II has been proposed and successfully verified in a 0.18-μm CMOS process. The detection function under different positive or negative ESD-induced and EFT-induced electrical transient disturbance has been investigated by HSPICE simulation. The experimental results have verified that the new proposed on-chip transient detection circuit II can detect and memorize the occurrence of electrical transients under system-level ESD or EFT testing conditions. With hardware/firmware co-design, the new proposed on-chip transient detection circuit II can be further used as firmware index to provide an effective solution against the malfunction in microelectronic products caused by ESD-induced and EFT-induced electrical transient disturbance.

Chapter 6

On-Chip Transient-to-Digital Converter

A novel on-chip transient-to-digital converter composed of four transient detection circuits and four different RC filter networks has been successfully designed and verified in a 0.18-μm complementary-metal-oxide-semiconductor (CMOS) process with 3.3-V devices. The output digital thermometer codes of the proposed on-chip transient-to-digital converter correspond to different electrical transient voltages under system-level ESD and EFT tests. These output digital codes can be used as the firmware index to execute different auto-recovery procedures in microelectronic systems. Thus, the proposed on-chip transient-to-digital converter can be further combined with firmware design to provide an effective solution to solve the system-level ESD and EFT protection issue in microelectronic systems equipped with CMOS integrated circuits (ICs).

6.1. Background

In order to solve the locked or frozen states caused by system-level ESD and EFT zapping conditions, microelectronic products system functions can be manually reset with operator intervention, which meets “class C” criterion defined in the standard. However, most microelectronic products are required at least to automatically recover the system functions without operator intervention to meet “class B” criterion. Therefore, to meet high system-level ESD or EFT specifications for microelectronic system products, the chip-level solutions which can help the microelectronic system to execute auto-recovery procedure without using additional discrete noise-decoupling components on the printed circuit board (PCB) are highly desired by the IC industry.

In this work, a novel on-chip transient-to-digital converter composed of on-chip RC-based transient detection circuits has been proposed to detect the fast electrical transients and convert them to digital thermometer codes under system-level ESD and EFT stresses. The proposed on-chip transient-to-digital converter can be coordinated with firmware to provide a hardware/firmware co-design solution for system-level ESD and EFT protection. The experimental results in a 0.18-μm CMOS process with 3.3-V devices have verified that the proposed on-chip transient-to-digital converter can successfully convert the fast electrical transients with different electrical transient voltage levels into digital codes during system-level ESD and EFT zapping conditions.

6.2. Evaluation on Board-Level Noise Filter Networks

During system-level ESD tests, the bi-polar transient voltages (underdamped sinusoidal waveforms) disturbed on the V_{DD}/V_{SS} lines of CMOS ICs inside the EUT often cause malfunction or hardware damage of microelectronic products. It has been reported that the different types of board-level noise filter network can impact the dominant parameters of bi-polar transient voltage, such as transient peak voltage, frequency and damping factor, by suppress the ESD-induced voltage efficiently. Therefore, four types of board-level noise filters have been investigated in this section and the experimental measurement results are shown below. The measurement setup combined noise filter network with TLU test measurement instruments is shown in Fig. 6.1.

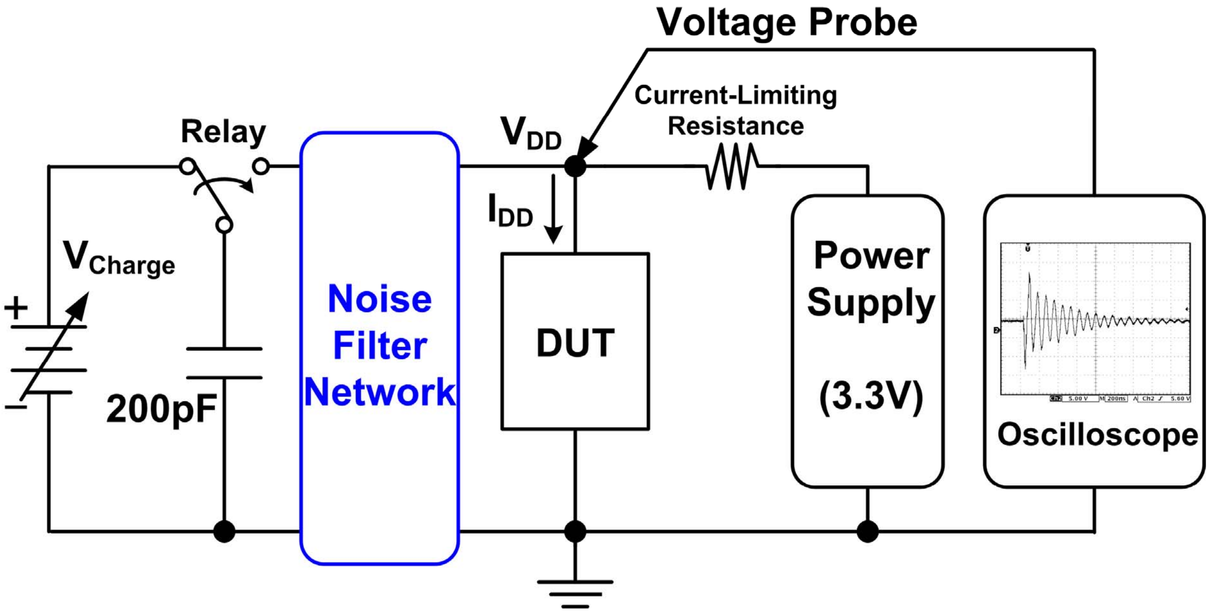
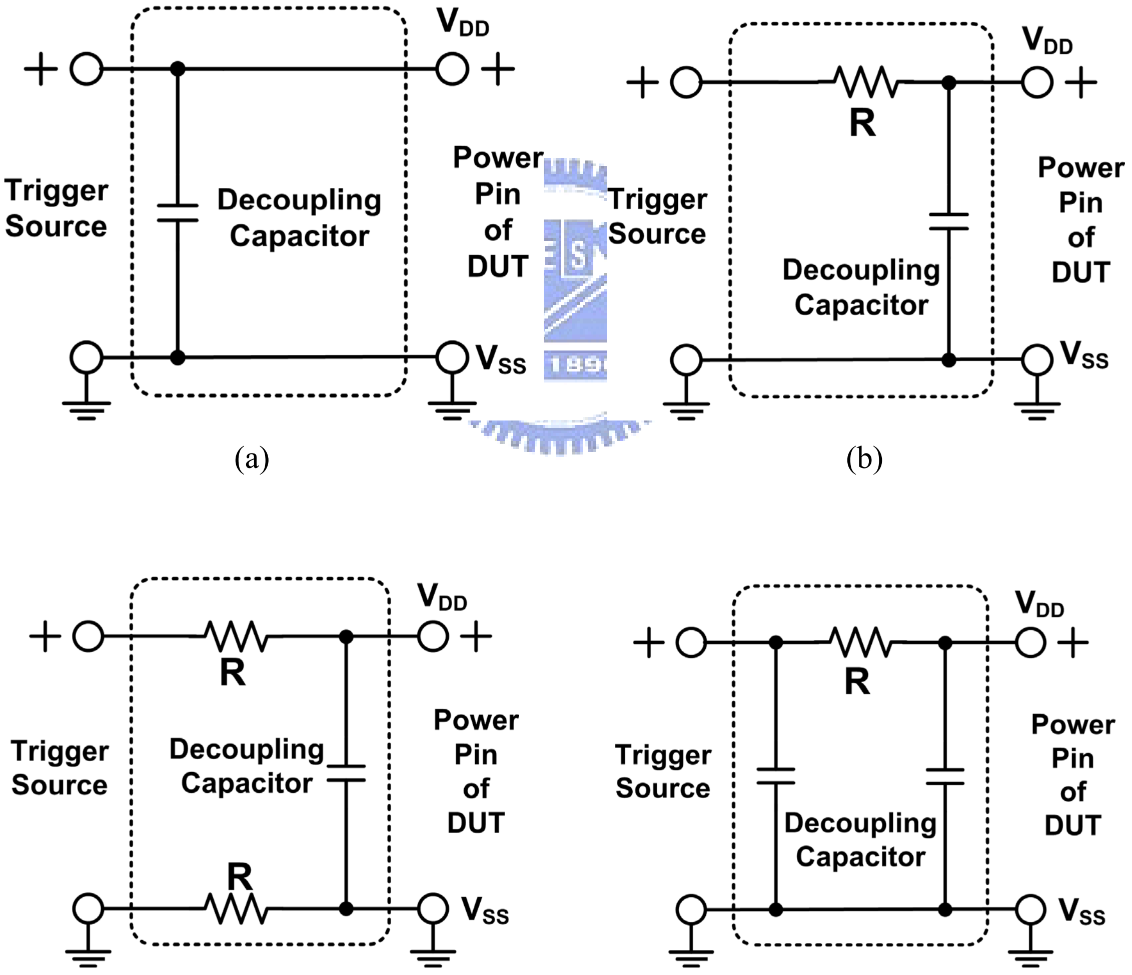


Fig. 6.1 Measurement setup for TLU test combined with noise filter network.

Different types of noise filter networks are investigated to find their effectiveness for improving the detection range of proposed transient detection circuit I under TLU tests, including: (1) capacitor filter, (2) type-I RC filter, (3) type-II RC filter, and (4) π-section filters based on the combinations with TVS and ferrite bead.

6.2.1. *Board-Level Noise Filter Networks*

It has been shown that noise filter networks can enhance immunity of CMOS ICs to system-level ESD test by decoupling, bypassing, or absorbing ESD-induced noise voltage (energy). It has also been reported that the noise filter networks have strong impact to the parameters of the underdamped sinusoidal voltage such as transient peak voltage, damping frequency, and damping factor. Four types of noise filter networks: capacitor filter, type-I RC filter, type-II RC filter, and π-section filter are depicted in Figs. 6.2(a), 6.2(b), 6.2(c), and 6.2(d), respectively. Figs. 6.3, 6.4, 6.5, and 6.6 shows their improvements on both positive and negative detection range enhancement of the proposed on-chip RC-based transient detection circuit I.



(a) (b)

(c) (d)

Fig. 6.2 Four types of noise filter network investigated for their improvements on the detection range of the proposed on-chip RC-based transient detection circuit I. (a) Capacitor filter, (b) Type-I RC filter, (c) Type-II RC filter, and (d) π-section filter.

6.2.2. Experimental Results of System-Level ESD Tests

The ceramic disc capacitor with advantages such as high rated working voltage (1 kV), good thermal stability, and low loss over a wide range of frequency is employed as the decoupling capacitor in the noise filter of Fig. 6.2(a). Decoupling capacitances ranging from 1 nF to 0.1 µF are used to investigate their improvements on the detection range of proposed on-chip RC-based transient detection circuit I. With the aid of the capacitor filter to reduce the electrical transient voltage on V_{DD}, the positive detection range can be significantly enhanced from +9 V (without decoupling capacitor) to over +28 V (with a decoupling capacitance of 0.1 µF), as shown in Fig. 6.3 Similarly, the negative detection level can be also greatly enhanced from -2 V (without decoupling capacitor) to -37 V (with a decoupling capacitance of 0.1µF). Thus, by choosing a decoupling capacitor with proper capacitance value, a simple 1st-order decoupling capacitor placed between V_{DD} and V_{SS} (ground) of CMOS ICs can be used to appropriately improve the detection range of proposed on-chip RC-based transient detection circuit I under the TLU tests.

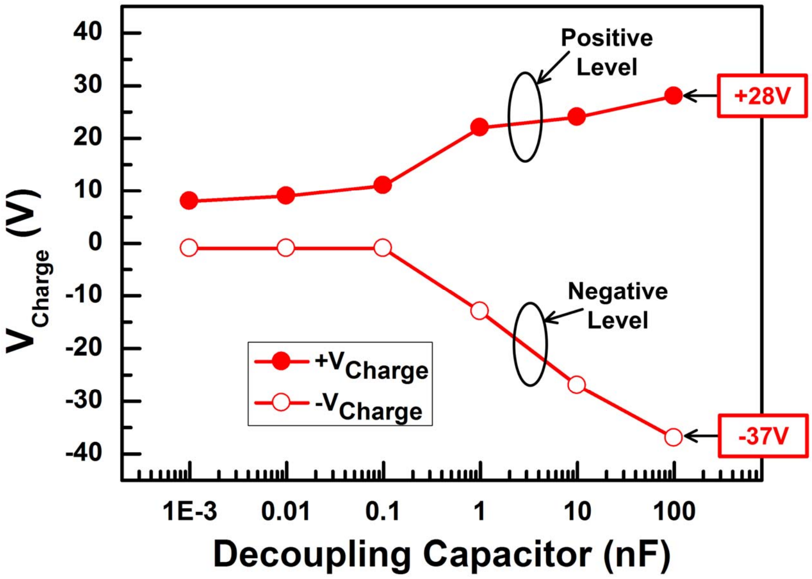


Fig. 6.3 Relations between the decoupling capacitance and the detection range of the proposed on-chip RC-based transient detection circuit I with capacitor filter.

The resistor, which is commonly used for degrading transient disturbance energy, sometimes substitutes for inductor as a 2nd-order type-I RC filter component, as shown in Fig. 6.2(b). Due to a higher insertion loss (2nd-order filter), such type-I RC filter has better detection range enhancements than capacitor filter (1st-order filter) in Fig. 6.2(a). For example, with 5-Ω resistor on the type-I RC filter, the positive detection range can be significantly enhanced from +9 V (without decoupling capacitor) up to +25 V (with decoupling capacitance of 0.1 μF) , as shown in Fig. 6.4. Similarly, the negative detection range can be also greatly enhanced from -2 V (without decoupling capacitor) to -32 V (with decoupling capacitance of 0.1 μF). Thus, in order to achieve higher detection range, the type-I RC filter can be used to avoid an excessively or unreasonably large decoupling capacitance in a simple 1st-order capacitor filter.

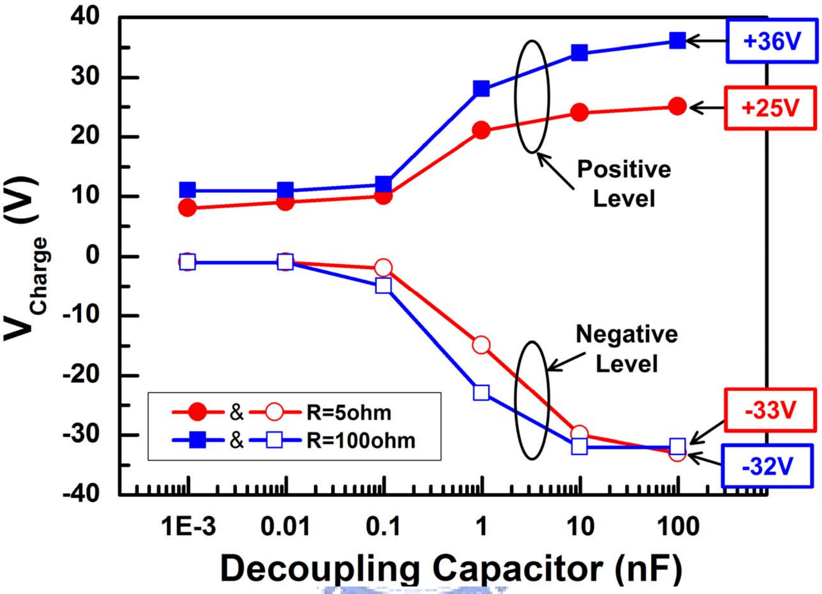


Fig. 6.4 Relations between the decoupling capacitance and the detection range of the proposed on-chip RC-based transient detection circuit I with Type-I RC filter.

The resistor, which is commonly used for degrading transient disturbance energy, sometimes substitutes for inductor as a 2nd-order type-II RC filter component, as shown in Fig. 6.2(c). Due to a higher insertion loss (2nd-order filter), such type-II RC filter has better detection range enhancements than capacitor filter (1st-order filter) in Fig. 6.2(a). For example, the positive detection range can be significantly enhanced from +5 V (with resistor of 5 Ω) up to +13 V (with resistor of 150 Ω), as shown in Fig. 6.5. Similarly, the negative detection range can be also greatly enhanced from -2 V (with resistor of 5 Ω) to -4 V (with resistor of 150 Ω).

A 3rd-order π-section filter is used to further enhance the detection range of the proposed on-chip RC-based transient detection circuit I, as shown in Fig. 6.2(d). This π-section filter consists of a resistor and two decoupling capacitors with equal decoupling capacitance. With the highest insertion loss among the noise filter networks in Figs. 6.2(a), 6.2(b), 6.2(c), and 6.2(d), the detection range of the proposed on-chip RC-based transient detection circuit I can be most improved. For example, the positive detection level can be significantly enhanced to over +400 V (with a decoupling capacitance of 0.1 μF), as shown in Fig. 6.6. Similarly, the negative detection range can also be significantly enhanced to over -63V (with decoupling capacitance of 0.1 μF). From the comprehensive measured results in Fig. 6.6, the decoupling capacitance can be optimized according to the desired detection level and the type of board-level noise filter chosen.

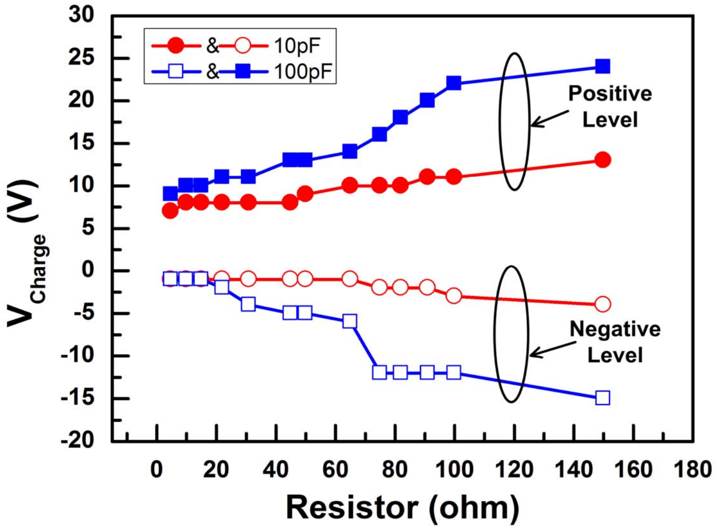


Fig. 6.5 Relations between the decoupling capacitance and the detection range of the proposed on-chip RC-based transient detection circuit I with Type-II RC filter.

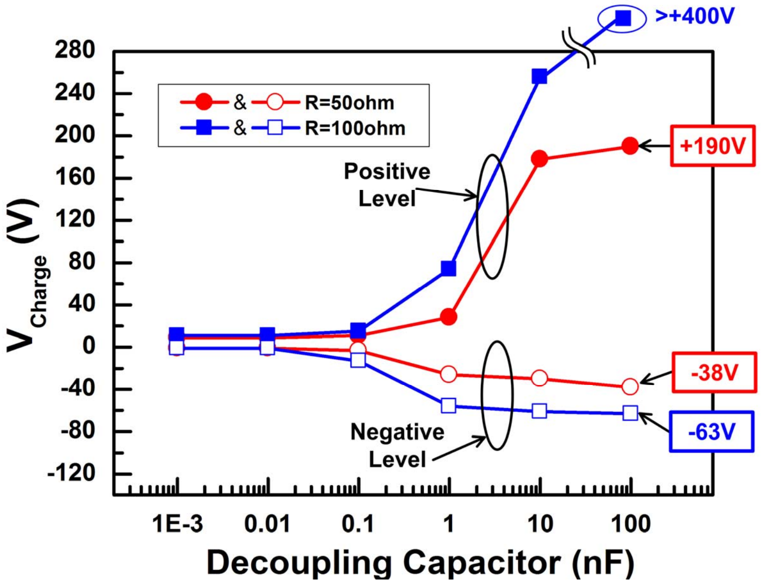


Fig. 6.6 Relations between the decoupling capacitance and the detection range of the proposed on-chip RC-based transient detection circuit I with π-section filter.

6.3. Transient detection Circuit Designed with Noise Filter Network

6.3.1. On-Chip Noise Filter Network

Fig. 6.7 shows the proposed on-chip RC-based transient detection circuit I combined with on-chip RC filter network, which is realized with one decoupling capacitor and two resistors with equal value to provide the noise filter function during system-level ESD stresses. The RC noise filter network can suppress the transient peak voltages on V_{DD} and V_{SS}, which influences positive and negative system-level ESD voltages to cause transition at the output (V_{OUT}) of the proposed on-chip RC-based transient detection circuit I. Therefore, in combination with different on-chip RC noise filter networks, the proposed on-chip RC-based transient detection circuit I can be designed to detect different voltage levels under system-level ESD tests.

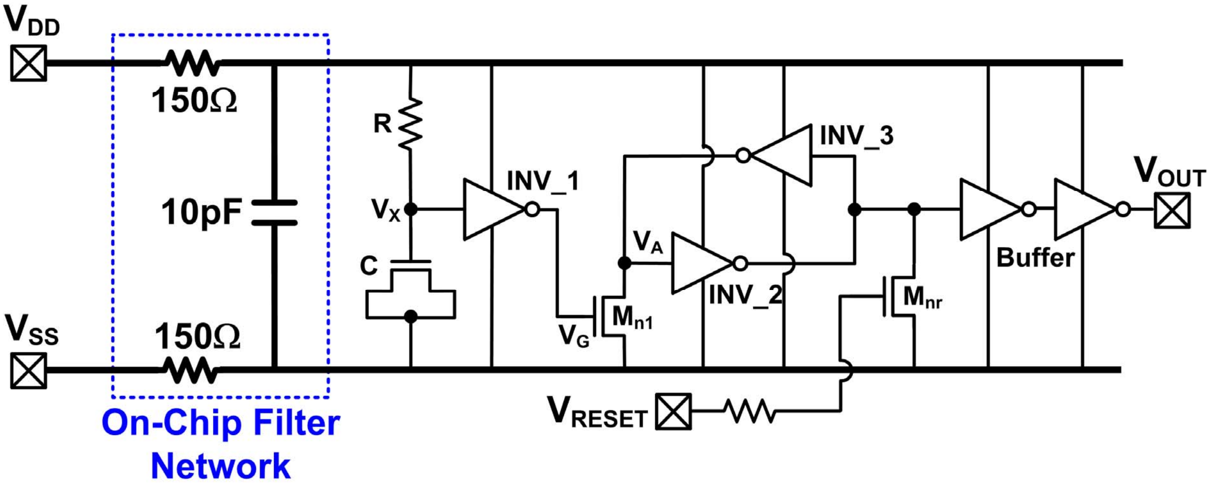


Fig. 6.7 The proposed on-chip RC-based transient detection circuit I combined with on-chip noise filter network.

6.3.2. Experimental Results of System-Level ESD Tests

The proposed on-chip RC-based transient detection circuit I combined with a RC filter network has been designed and fabricated in a 0.18-μm 1P5M CMOS process with 3.3-V devices. The fabricated chip in a package for system-level ESD test is shown in Fig. 6.8. The silicon area of the proposed on-chip RC-based transient detection circuit combined with a noise filter network is 266 μm x 254 μm.

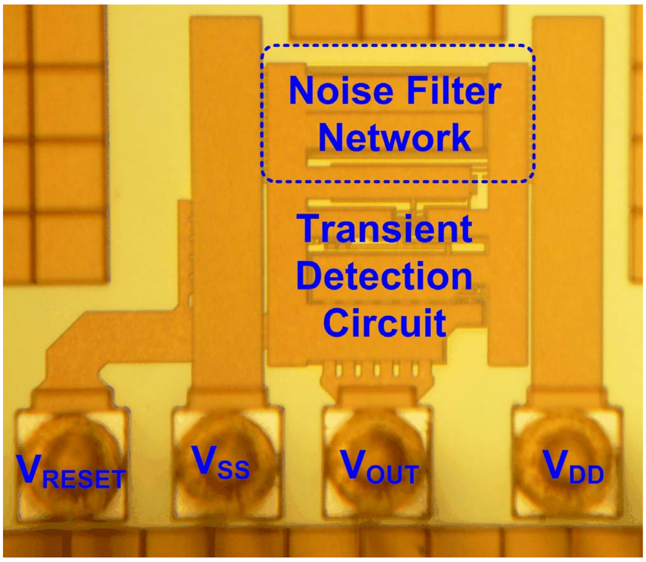
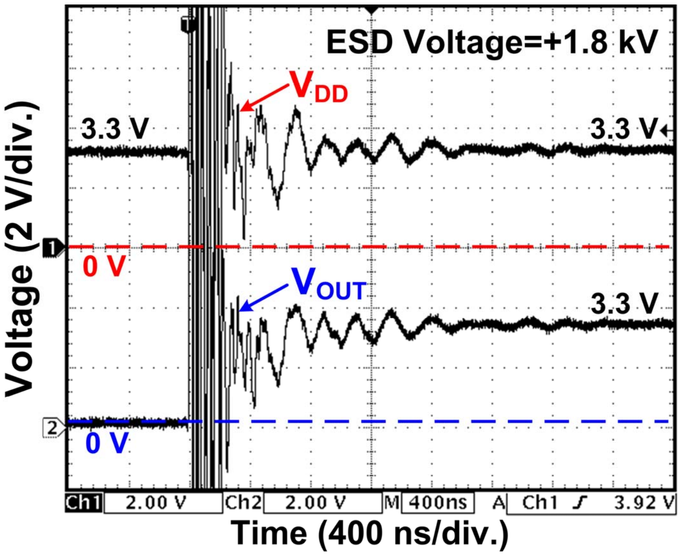
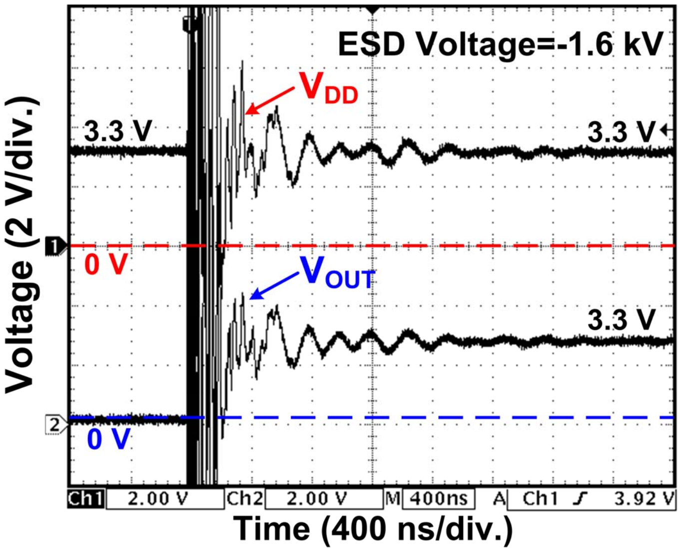


Fig. 6.8 Die photo of the proposed on-chip RC-based transient detection circuit I combined with on-chip noise filter network.

With the aid of the on-chip filter network to reduce the noise voltage on power lines, the minimum positive system-level ESD voltage to cause transition at the output (V_{OUT}) of the proposed on-chip RC-based transient detection circuit I can be significantly enhanced from +0.2 kV (without on-chip filter network) to +1.8 kV (with on-chip filter network), as shown in Fig. 6.9(a). Similarly, the minimum negative system-level ESD voltage to cause transition at the output (V_{OUT}) of the proposed on-chip RC-based transient detection circuit I can be also enhanced from -0.2 kV (without on-chip filter network) to -1.6 kV (with on-chip filter network), as shown in Fig. 6.9(b). Thus, by choosing proper capacitance and resistance, the on-chip filter network placed between V_{DD} and V_{SS} can be used to appropriately adjust the detection voltage level of the proposed on-chip RC-based transient detection circuit I under system-level ESD test, both for the positive or the negative electrical fast transients. With different system-level ESD voltage zapping, the proposed on-chip RC-based transient detection circuit I can be designed to detect different the strength of system-level ESD stress. Therefore, a novel transient-to-digital converter can be built up by using the proposed on-chip RC-based transient detection circuit I with different RC filter networks.



(a)



(b)

Fig. 6.9 Measured V_{DD} and V_{OUT} transient voltage waveforms of the proposed on-chip RC-based transient detection circuit I combined with on-chip noise filter network under a system-level ESD test with an ESD voltage of (a) +1.8 kV, and (b) -1.6 kV.

6.4. On-Chip Transient-to-Digital Converter

A novel on-chip 4-bit transient-to-digital converter composed of four transient detection circuits and four different on-chip RC filter networks have been designed and verified in a 0.18-μm CMOS process with 3.3-V devices. The output digital thermometer codes correspond to different electrical transient voltages under system-level ESD and EFT tests.

6.4.1. Circuit Structure

Fig. 6.10 shows the proposed on-chip 4-bit transient-to-digital converter. The 4-bit on-chip 4-bit transient-to-digital converter consists of four transient detection circuit I with four different on-chip RC filter networks. With different resistance and capacitance values in the filter networks, different ESD-induced and EFT-induced energy on V_{DD} and V_{SS} will reach each transient detection circuit. Therefore, under the system-level ESD and EFT zapping conditions with different electrical transient voltages, the four transient detection circuits will have different output responses.

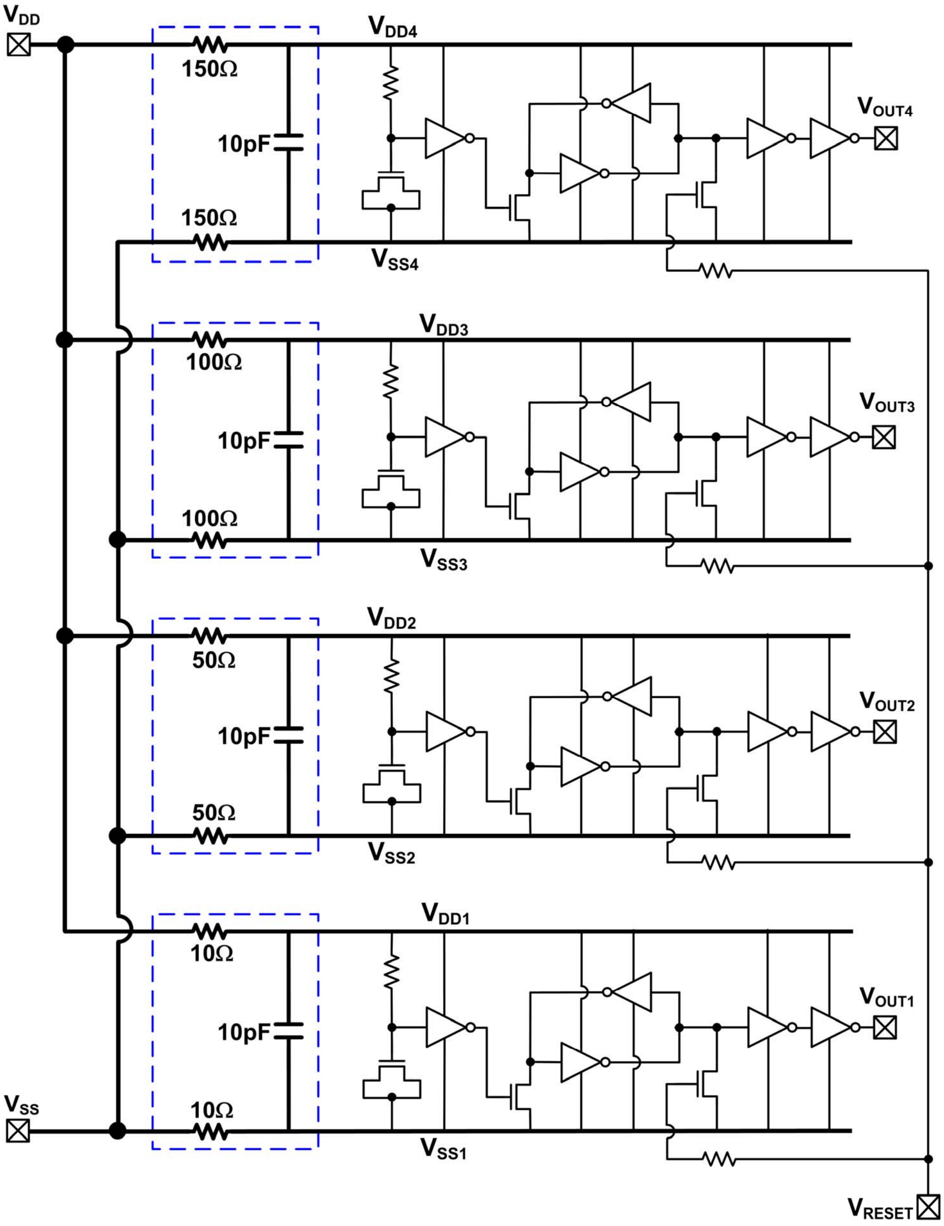


Fig. 6.10 Proposed on-chip 4-bit transient-to-digital converter.

6.4.2. System-Level ESD Tests

The proposed on-chip 4-bit transient-to-digital converter has been designed and fabricated in a 0.18-μm 1P5M CMOS process with 3.3-V devices. The fabricated chip in a package for system-level ESD test is shown in Fig. 6.11. The silicon area of proposed on-chip 4-bit transient-to-digital converter is 1030 μm x 188.5 μm.

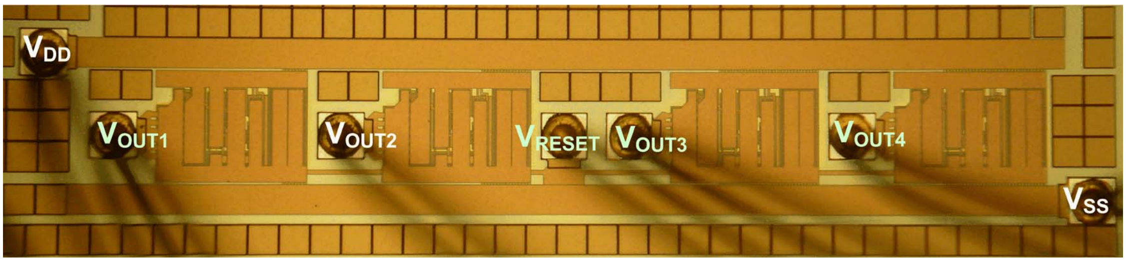


Fig. 6.11 Die photo of the proposed on-chip 4-bit transient-to-digital converter.

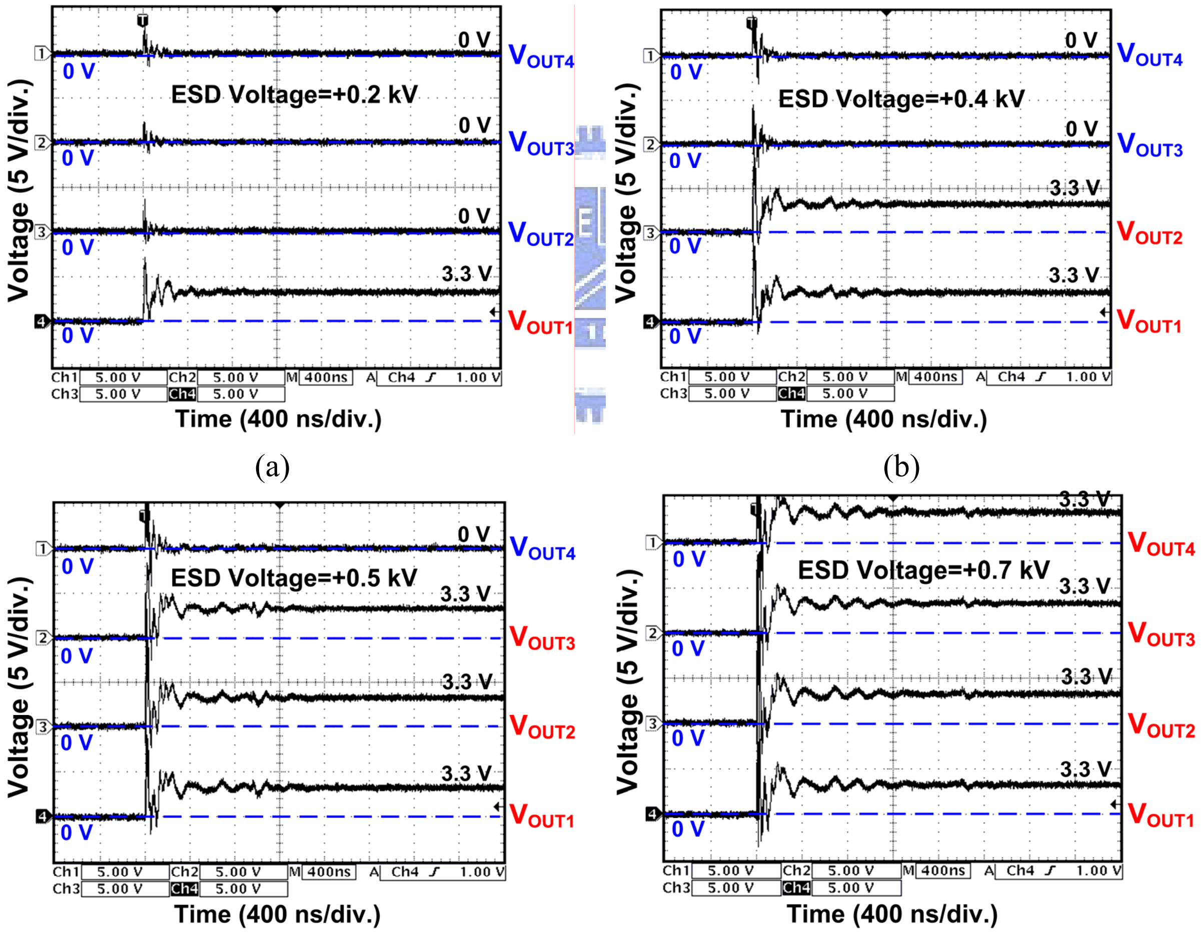
The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed on-chip 4-bit transient-to-digital converter under system-level ESD test with ESD voltage of +0.2 kV zapping on the HCP are shown in Fig. 6.12(a). During the fast transient of ESD stress, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are disturbed simultaneously during V_{DD} and V_{SS} disturbance. Finally, V_{OUT1} will be changed from 0 V to 3.3 V with V_{OUT2}, V_{OUT3}, and V_{OUT4} are still kept at 0V. Therefore, under system-level ESD test with ESD voltage of +0.2 kV zapping, the output voltages of the proposed on-chip 4-bit transient-to-digital converter can be transferred into a thermometer digital code of "0001."

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed on-chip 4-bit transient-to-digital converter under system-level ESD test with ESD voltage of +0.4 kV zapping on the HCP are shown in Fig. 6.12(b). During the fast transient of ESD stress, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are disturbed simultaneously during V_{DD} and V_{SS} disturbance. Finally, V_{OUT1} and V_{OUT2} will be changed from 0 V to 3.3 V, with V_{OUT3} and V_{OUT4} are still kept at 0V. Therefore, under system-level ESD test with ESD voltage of +0.4 kV zapping, the output voltages of the proposed on-chip 4-bit transient-to-digital converter can be transferred into a thermometer digital code of "0011."

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed on-chip 4-bit transient-to-digital converter under system-level ESD test with ESD voltage of +0.5 kV zapping on the HCP are shown in Fig. 6.12(c). During the fast transient of ESD stress, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are disturbed simultaneously during V_{DD} and V_{SS} disturbance. Finally, V_{OUT1}, V_{OUT2}, and V_{OUT3} will be changed from 0 V to 3.3 V with V_{OUT4} is still kept at

0V. Therefore, under system-level ESD test with ESD voltage of +0.5 kV zapping, the output voltages of the proposed on-chip 4-bit transient-to-digital converter can be transferred into a thermometer digital code of “0111.”

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed on-chip 4-bit transient-to-digital converter under system-level ESD test with ESD voltage of +0.7 kV zapping are measured in Fig. 6.12(d). During the high-energy fast transient of ESD stress, all transient detection circuits can detect the occurrence of disturbance on V_{DD} and VSS. Finally, when V_{DD} finally returns to its normal stable voltage level, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} have been changed from 0 V to 3.3 V. Therefore, under system-level ESD test with ESD voltage of +0.7 kV zapping, the output voltages of the proposed on-chip 4-bit transient-to-digital converter can be transferred into a thermometer digital code of “1111.”



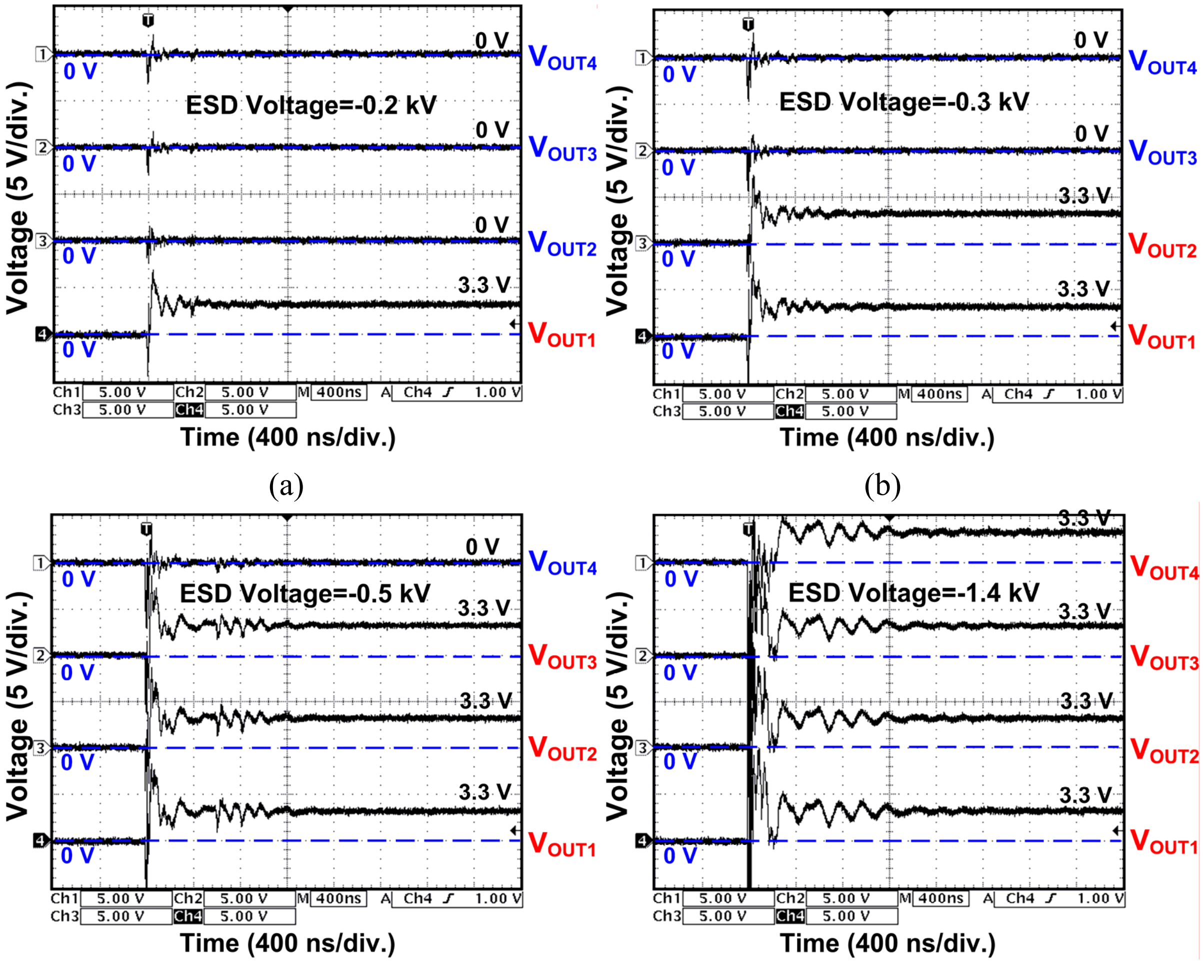
(a) (b)

(c) (d)

Fig. 6.12 Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient voltage waveforms of the proposed on-chip 4-bit transient-to-digital converter under a system-level ESD test with an ESD voltage of (a) +0.2 kV, (b) +0.4 kV, (c) +0.5 kV, and (d) +0.7 kV, zapping on the HCP.

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed on-chip 4-bit transient-to-digital converter under system-level ESD test with ESD voltage of -0.2 kV zapping on the HCP are shown in Fig. 6.13(a). During the fast transient of ESD stress, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are disturbed simultaneously during V_{DD} and V_{SS} disturbance. Finally, V_{OUT1} will be changed from 0 V to 3.3 V with V_{OUT2}, V_{OUT3}, and V_{OUT4} are still kept at 0V. Therefore, under system-level ESD test with ESD voltage of -0.2 kV zapping, the output voltages of the proposed on-chip 4-bit transient-to-digital converter can be transferred into a thermometer digital code of “0001.”

Similarly, Figs. 6.13(b), 6.13(c), and 6.13(d) show the measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed on-chip 4-bit transient-to-digital converter under EFT tests with ESD voltages of -0.3 kV, -0.5 kV, and -1.4 kV zapping, and transferred into digital thermometer codes of “0011,” “0111,” and “1111,” respectively.



(a) (b) (c) (d)

Fig. 6.13 Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient voltage waveforms of the proposed on-chip 4-bit transient-to-digital converter under a system-level ESD test with an ESD voltage of (a) -0.2 kV, (b) -0.3 kV, (c) -0.5 kV, and (d) -1.4 kV, zapping on the HCP.

Fig. 6.14 depicts the characteristic between ESD zapping voltages and the converted codes. With the proposed on-chip 4-bit transient-to-digital converter, different ESD voltages under system-level ESD tests can be detected and transferred into different thermometer digital codes. With larger ESD voltage level, the thermometer digital code goes higher, as listed in Table 6.1.

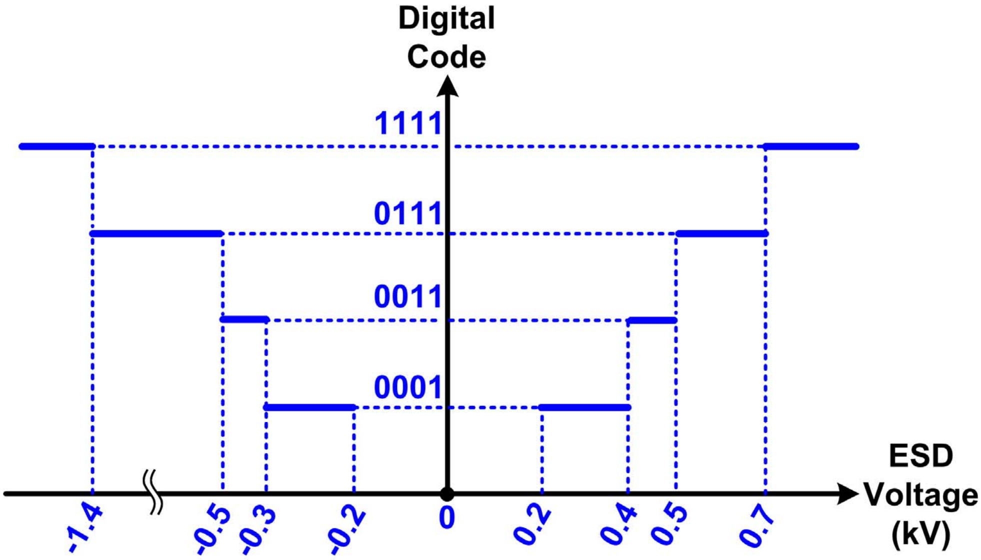


Fig. 6.14 The relationship between the ESD zapping voltage and the digital code in the proposed on-chip 4-bit transient-to-digital converter.

Table 6.1
ESD Voltage to Digital Code Characteristic of Proposed On-Chip 4-Bit transient-to-digital Converter

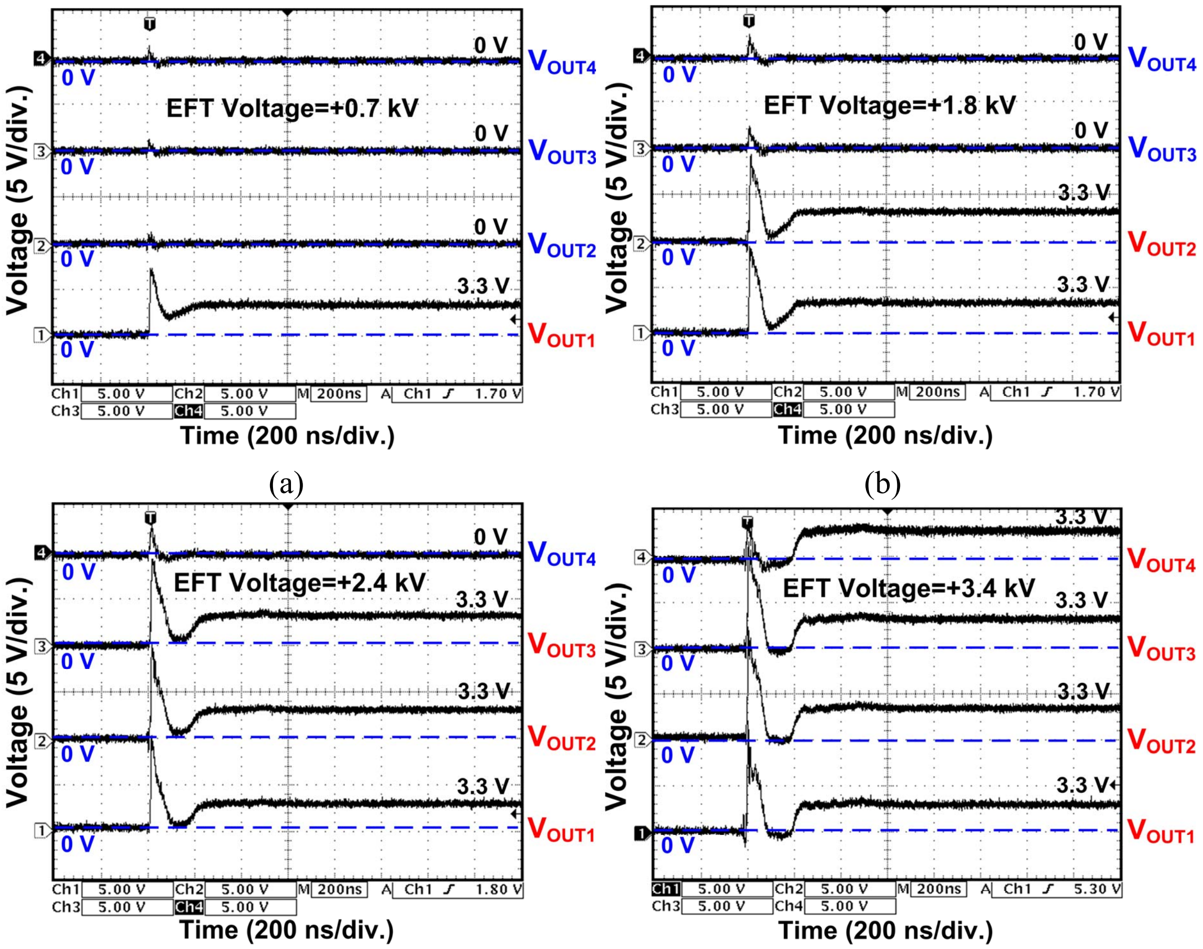
ESD Voltage (kV)	ESD Voltage (kV)	Digital Codes
< +0.2	> -0.2	0000
+0.2 ~ +0.4	-0.2 ~ -0.3	0001
+0.4 ~ +0.5	-0.3 ~ -0.5	0011
+0.5 ~ +0.7	-0.5 ~ -1.4	0111
> +0.7	< -1.4	1111

6.4.3. EFT Tests

The EFT generator combined with attenuation network shown in Fig. 4.16 is used to evaluate the detection function of the transient-to-digital converter under EFT tests.

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed on-chip 4-bit transient-to-digital converter under EFT test with an EFT voltage of +0.7 kV are shown in Fig. 6.15(a). During the EFT-induced fast transient, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are disturbed simultaneously during the V_{DD} and V_{SS} disturbance. Finally, V_{OUT1} will be changed from 0V to 3.3V while V_{OUT2}, V_{OUT3}, and V_{OUT4} remain 0V. Therefore, under EFT test with an EFT voltage of +700V zapping, the output voltages of the proposed on-chip 4-bit transient-to-digital converter can be transferred into a digital thermometer code of "0001."

Similarly, Figs. 6.15(b), 6.15(c), and 6.15(d) show the measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed on-chip 4-bit transient-to-digital converter under EFT tests with EFT voltages of +1.8 kV, +2.4 kV, and +3.4 kV, and transferred into digital thermometer codes of "0011," "0111," and "1111," respectively.



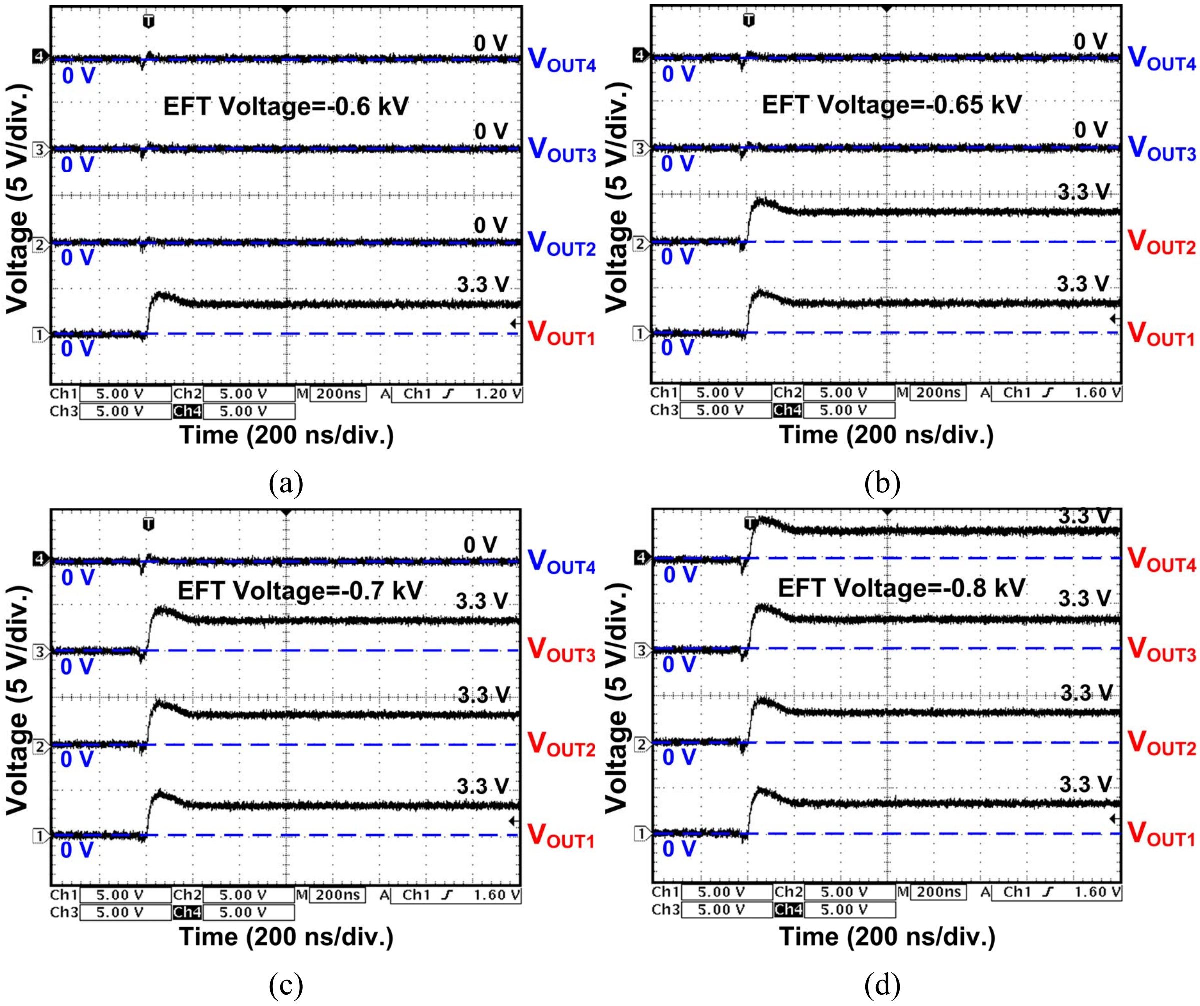
(a) (b)

(c) (d)

Fig. 6.15. Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient voltage waveforms of the proposed on-chip 4-bit transient-to-digital converter under EFT test with EFT voltage of (a) +0.7 kV, (b) +1.8 kV, (c) +2.4 kV, and (d) +3.4 kV.

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed on-chip 4-bit transient-to-digital converter under EFT test with an EFT voltage of -0.6 kV are shown in Fig. 6.16(a). During the EFT-induced fast transient, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are disturbed simultaneously during the V_{DD} and V_{SS} disturbance. Finally, V_{OUT1} will be changed from 0 V to 3.3 V while V_{OUT2}, V_{OUT3}, and V_{OUT4} remain 0 V. Therefore, under EFT test with EFT voltage of -600 V zapping, the output voltages of the proposed on-chip 4-bit transient-to-digital converter can be transferred into a digital thermometer code of “0001.”

Similarly, Figs. 6.16(b), 6.16(c), and 6.16(d) show the measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed on-chip 4-bit transient-to-digital converter under EFT test with EFT voltages of -0.65 kV, -0.7 kV, and -0.8 kV, and transferred into digital thermometer codes of “0011,” “0111,” and “1111,” respectively.



(a) (b)

(c) (d)

Fig. 6.16. Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient voltage waveforms of the proposed on-chip 4-bit transient-to-digital converter under EFT test with EFT voltage of (a) -0.6 kV, (b) -0.65 kV, (c) -0.7 kV, and (d) -0.8 kV.

Fig. 6.17 depicts the relationship between the EFT zapping voltages and the converted codes. With the proposed on-chip 4-bit transient-to-digital converter, different EFT voltages under EFT tests can be detected and transferred into different digital thermometer codes. With a larger EFT voltage level, the digital thermometer code goes higher, as listed in Table 6.2.

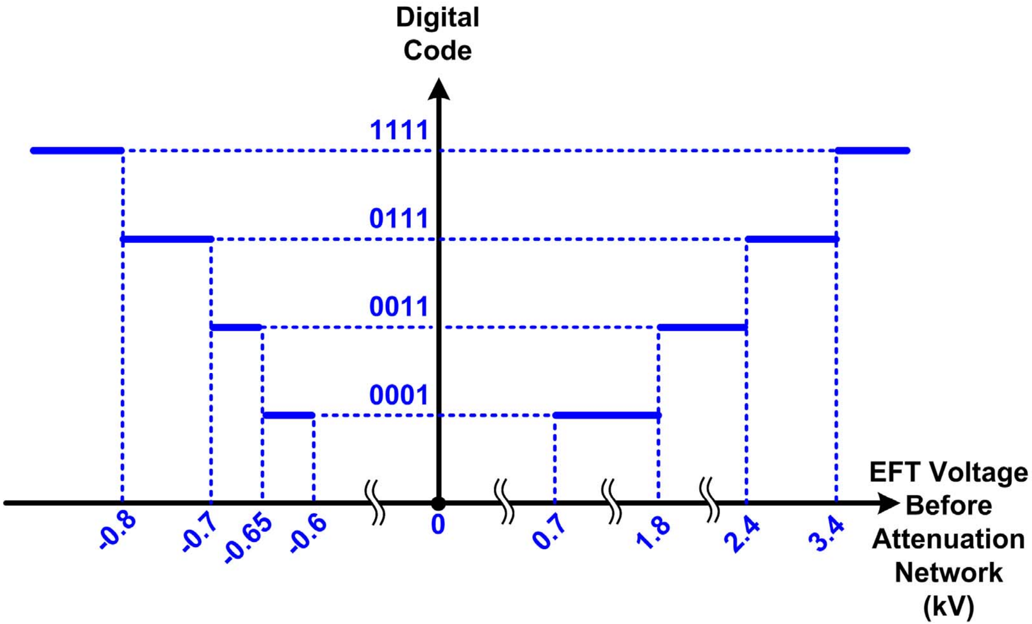


Fig. 6.17. The relationship between the EFT voltage level and the digital code in the proposed on-chip 4-bit transient-to-digital converter.

Table 6.2
EFT Voltage to Digital Code Characteristic of Proposed On-Chip 4-Bit transient-to-digital Converter

Positive EFT Voltage (kV)	Negative EFT Voltage (kV)	Digital Codes
< +0.7	> -0.6	0000
+0.7 ~ +1.8	-0.6 ~ -0.65	0001
+1.8 ~ +2.4	-0.65 ~ -0.7	0011
+2.4 ~ +3.4	-0.7 ~ -0.8	0111
> +3.4	< -0.8	1111

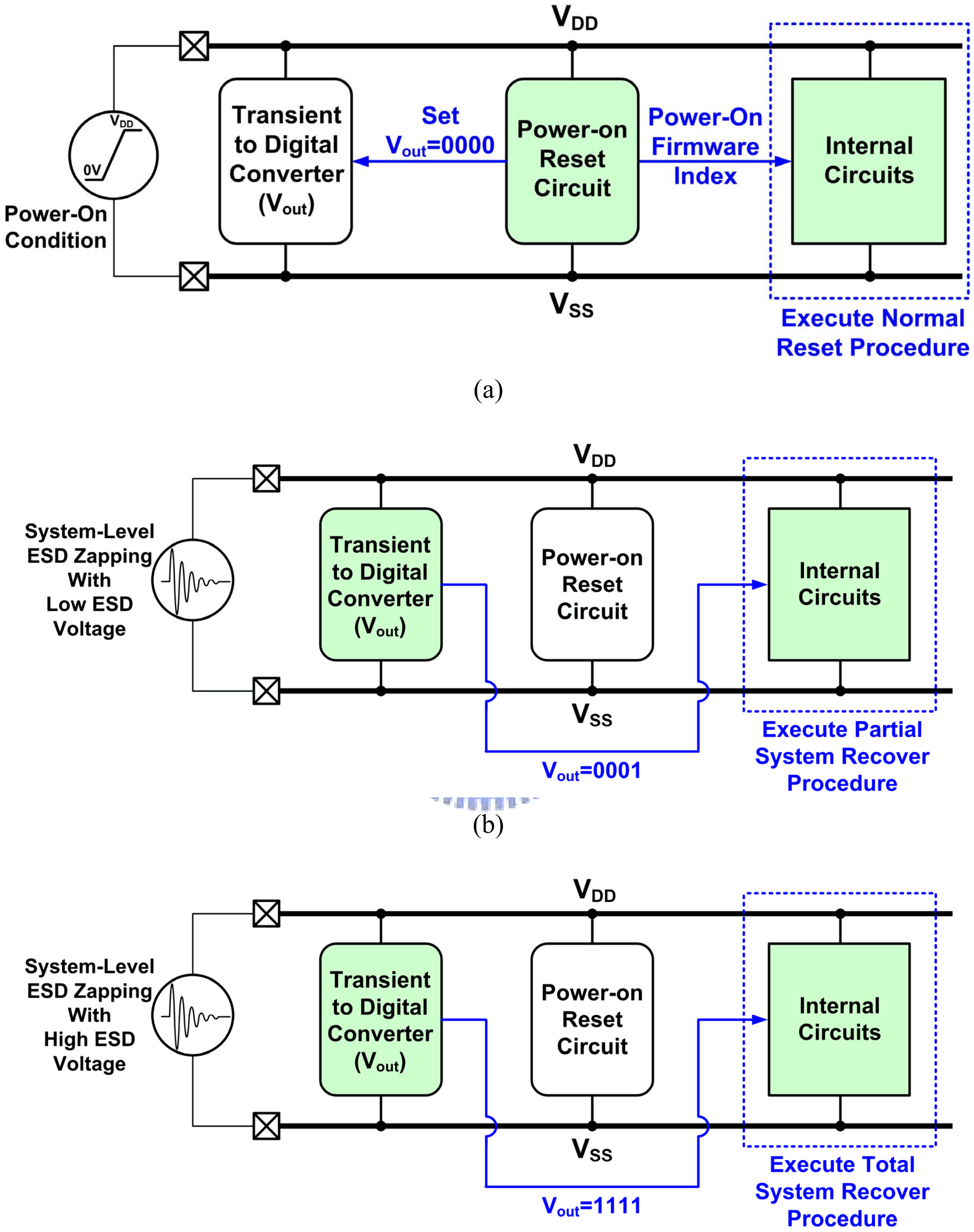
6.5. Applications in CMOS ICs with Firmware Co-Design

It had been reported that the hardware/firmware can be co-designed to effectively improve the system-level ESD and EFT robustness of CMOS IC products. The proposed on-chip 4-bit transient-to-digital converter can be co-designed with firmware to provide a system solution to solve the system-level ESD and EFT events to microelectronic products equipped with CMOS ICs.

For example, to realize a system-level ESD protection of a function against upset or freeze after transition, a hardware/firmware co-design solution combined with the proposed on-chip 4-bit transient-to-digital converter and the power-on reset circuit can be built up. Under the normal power-on condition, the V_{DD} power-on voltage waveform has a rise time on the order of a millisecond (ms). The power on reset circuit should be designed with the longer rise time on the order of millisecond. Thus, the output signal of the power-on reset circuit can send the power-on firmware index for a microelectronic system to execute a normal reset procedure, as shown in Fig. 6.18(a).

Due to the difference in the rise times between the ESD zapping voltage and the V_{DD} power-on voltage, the proposed on-chip transient-to-digital converter is designed to sense fast electrical transients and send different output digital codes under the system-level ESD zapping conditions with different ESD voltages, as shown in Figs. 6.18(b) and 6.18(c). For example, under the system-level ESD zapping with a low ESD voltage, the output digital code of the proposed on-chip 4-bit transient-to-digital converter becomes “0001.” Then, the firmware can execute the partial system recover procedure to check and to recover partial electrical functions of microelectronic system. Under the system-level ESD zapping with high enough ESD voltage, the output digital code of the proposed on-chip 4-bit transient-to-digital converter becomes “1111.” Then, the firmware can execute the recover procedure to recover all the electrical functions to a desired stable state as soon as possible. The firmware can be designed to execute different recover procedures with different output digital codes of the proposed on-chip 4-bit transient-to-digital converter. After the reset and recover procedures, the output digital code of the proposed on-chip 4-bit transient-to-digital converter is again reset to “0000” for detecting the next transient ESD events.

By including the proposed on-chip transient-to-digital converter and an additional firmware index into the chip, the firmware flowchart shown in Figs. 6.18(a)-(c) can be used to improve the system-level ESD and EFT robustness of microelectronic products. Such a hardware/firmware co-design method can provide an effective system solution against system-level ESD and EFT events in microelectronic systems.



(a)

(b)

(c)

Fig. 6.18. Hardware/firmware operation during (a) power-on reset condition, (b) low system-level ESD zapping, and (c) high system-level ESD zapping.

6.6. Conclusion

A novel on-chip 4-bit transient-to-digital converter composed of four transient detection circuits and four different RC filter networks has been successfully designed and verified. The output digital thermometer codes of the proposed on-chip 4-bit transient-to-digital converter correspond to different electrical transient voltages under system-level ESD and EFT tests. These output digital codes can be used as the firmware index to execute different auto-recovery procedures in microelectronic products. Thus, the new proposed on-chip 4-bit transient-to-digital converter can be further combined with firmware design to provide an effective solution against upset or freeze malfunctions after system-level ESD and EFT zapping on microelectronic systems.

Chapter 7

Conclusions and Future Works

This chapter summarizes the specific new results of this dissertation. Future works for system-level ESD topics are also addressed in this chapter.

7.1. Specific New Results of This Dissertation

The specific new results of this dissertation are summarized below:

(1) This dissertation investigates the latchup-like failure of power-rail ESD clamp circuits under system-level ESD and EFT tests. Furthermore, a novel power-rail ESD clamp combined with NMOS reset function is proposed to solve such latchup-like failure and provide high enough chip-level ESD robustness.

(2) This dissertation clarifies the TLU physical mechanism under EFT tests by experimental verification. Furthermore, this dissertation evaluates different board-level noise filter networks to find their effectiveness for TLU prevention under the system-level ESD test. The related technical know-how can provide the printed circuit board (PCB) designers useful references to optimize PCB designs for TLU prevention.

(3) This dissertation proposes two on-chip transient detection circuits. The detection performance of the proposed on-chip transient detection circuits has been evaluated under the system-level ESD or EFT tests. The detection results can be used as system recover index and provide the IC industry a hardware/firmware solution for improving the system-level ESD immunity of CMOS ICs.

(4) This dissertation proposes on-chip transient-to-digital converter. The output digital thermometer codes correspond to different system recover procedures and provide another efficient hardware/firmware solution.

The proposed inventions in this dissertation, such as on-chip transient detection circuits and transient-to-digital converters, can inspire system or IC designers to develop novel techniques for system-level ESD prevention.

7.2. Future Works

In addition to using the on-chip transient detection circuits and transient-to-digital converters proposed in this dissertation, some other techniques could be the useful candidates to further improve the susceptibility of the CMOS ICs against the system-level ESD or EFT tests. These future works are listed below.

(1) Linear Relationship between the ESD/EFT Zapping Voltages and Digital Codes
(2) Hardware and Firmware Co-Design with System-Auto-Reset Function
(3) Latchup Auto-Detection, Self-Stop, and Auto-Reset Circuit
(4) Layout Optimization
(5) Other Specific Advanced Process Technologies

With the developments of future system-level ESD and EFT prevention techniques, it is anticipated that electrical transient disturbance events can be efficiently suppressed in the continual-scaling CMOS technologies.

References

[1] S. Voldman, *ESD: Circuits and Devices*, John Wiley & Sons, 2006.

[2] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd Edition, John Wiley & Sons, Ltd., England, 2002.

[3] A. Amerasekera and C. Duvvury, "The impact of technology scaling on ESD robustness and protection circuit design," in *Proc. EOS/ESD Symp.*, 1994, pp. 237-245.

[4] C. Diaz, T. Kopley, and P. Marcoux, "Building-in ESD/EOS reliability for sub-half-micron CMOS processes," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 1995, pp. 276-283.

[5] S. Daniel and G. Krieger, "Process and design optimization for advanced CMOS I/O ESD protection devices," in *Proc. EOS/ESD Symp.*, 1990, pp. 206-213.

[6] R. Rountree, "ESD protection for submicron CMOS circuits: Issues and solutions," in *IEDM Tech. Dig.*, 1988, pp. 580-583.

[7] C. Jiang, E. Nowak, and M. Manley, "Process and design for ESD robustness in deep submicron CMOS technology," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 1996, pp. 233-236.

[8] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.

[9] *EMC – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test*, IEC 61000-4-2 International Standard, 2001.

[10] M.-D. Ker and Y.-Y. Sung, "Hardware/firmware co-design in an 8-bits microcontroller to solve the system-level ESD issue on keyboard," in *Proc. EOS/ESD Symp.*, 1999, pp. 352–360.

[11] G. Muchaidze, J. Koo, Q. Cai, T. Li, L. Han, A. Martwick, K. Wang, J. Min, J. Drewniak, and D. Pommerenke, "Susceptibility scanning as a failure analysis tool for system-level electrostatic discharge (ESD) problems," *IEEE Trans. Electromagn. Compat.*, vol. 50, no. 2, pp. 268–276, May 2008.

[12] J. Koo, Q. Cai, D. Pommerenke, K. Wang, J. Mass, M. Hirata, and A. Martwick, "The repeatability of system-level ESD test and relevant ESD generator parameters," in *Proc. IEEE Int. Symp. on Electromagn. Compat. (EMC)*, 2008.

[13] D. Smith, and A. Wallash, "Electromagnetic interference (EMI) inside a hard disk driver

due to external ESD," in *Proc. EOS/ESD Symp.*, 2002, pp. 32–36.

[14] D. Smith, l. Henry, M. Hogsett, and J. Nuebel, "Sources of impulsive EMI in large server farms," in *Proc. EOS/ESD Symp.*, 2002, pp. 26–31.

[15] N. Shimoyama, M. Tanno, S. Shigematsu, H. Morimura, Y. Okazaki, and K. Machida, "Evaluation of ESD hardness for fingerprint sensor LSIs," in *Proc. EOS/ESD Symp.*, 2004, pp. 75–81.

[16] T.-H. Wang, W.-H. Ho, and L.-C. Chen, "On-chip system ESD protection design for STN LCD drivers," in *Proc. EOS/ESD Symp.*, 2005, pp. 316–322.

[17] W. Stadler, S. Bargstadt-Franke, T. Brodbeck, R. Gaertner, M. Goroll, H. Goβner, N. Jensen, and Chr. Muller, "From the ESD robustness of products to the system-level ESD robustness," in *Proc. EOS/ESD Symp.*, 2004, pp. 67–74.

[18] T. Smedes, J. Zwol, G. Raad, T. Brodbeck, and H. Wolf, "Relations between system level ESD and (vf-) TLP," in *Proc. EOS/ESD Symp.*, 2006, pp. 136–143.

[19] *ESD Association Standard Test Method ESD STM5.1-2001, for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level*, ESD Association, 2001.

[20] *Electrostatic Discharge (ESD) Sensitivity Testing—Human Body Model (HBM)*, EIA/JEDEC Standard Test Method A114-D, 2006.

[21] *ESD Association Standard Test Method ESD STM5.2-1999, for Electrostatic Discharge Sensitivity Testing – Machine Model – Component Level*, ESD Association, 1999.

[22] *Electrostatic Discharge (ESD) Sensitivity Testing—Machine Model (MM)*, EIA/JEDEC Standard Test Method A115-A, 1997.

[23] *ESD Association Standard Test Method ESD STM5.3.1-1999, for Electrostatic Discharge Sensitivity Testing – Charge Device Model – Component Level*, ESD Association, 1999.

[24] *Electrostatic Discharge (ESD) Sensitivity Testing—Charge Device Model (CDM)*, EIA/JEDEC Standard Test Method C101-C, 2004.

[25] Y.-W. Hsiao and M.-D. Ker, "Investigation on discharge current waveforms in board-level CDM ESD events with different board sizes," in *Presentations of the 2nd International ESD Workshop*, Port D'Albret, France, May 12-15, 2008, pp. 284-296.

[26] M.-D. Ker and S.-F. Hsu, "Physical mechanism and device simulation on transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1821–1831, Aug. 2005.

[27] S.-F. Hsu and M.-D. Ker, "Transient-induced latchup dependences on power-pin

damping frequency and damping factor in CMOS integrated circuits," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 2002–2010, Aug. 2007.

[28] S. -F. Hsu and M. -D. Ker, "Dependences of damping frequency and damping factor of bi-polar trigger waveforms on transient-induced latchup," in *Proc. EOS/ESD Symp.*, 2005, pp. 118–125.

[29] *EMC – Part 4-4: Testing and Measurement Techniques – Electrical Fast Transient/Burst Immunity Test*, 2004. IEC 61000-4-4 International Standard.

[30] M.-D. Ker and S.-F. Hsu, "Evaluation on board-level noise filter networks to suppress transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 1, pp. 161–171, Feb. 2006.

[31] M.-D. Ker and S.-F. Hsu, "Evaluations on board-level noise filter networks to suppress transient-induced latchup under system-level ESD test," in *Proc. EOS/ESD Symp.*, 2005, pp. 262–269.

[32] H. Ott, *Noise Reduction Techniques in Electronic Systems*, 2nd Edition, John Wiley & Sons, 1988.

[33] M. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance*, IEEE Press, 2000.

[34] V. Kodali, *Engineering Electromagnetic Compatibility: Principles, Measurements, and Technologies*, IEEE Press, 1996.

[35] M.-D. Ker, C.-C. Yen, and P.-C. Shin, "On-chip transient detection circuit for system-level ESD protection in CMOS integrated circuits to meet electromagnetic compatibility regulation," *IEEE Trans. Electromagn. Compat.*, vol. 50, no. 1, pp. 13–21, Feb. 2008.

[36] M.-D. Ker, C.-C. Yen, C.-S. Liao, T.-Y. Chen, and C.-C. Tsai, "Transient-to-digital converter for ESD protection design in microelectronic systems," in *Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC)*, 2008, pp. 409-412.

[37] M.-D. Ker, C.-S. Liao, and C.-C. Yen, "Transient detection circuit for system-level ESD protection and its on-board behavior with EMI/EMC filters," in *Proc. IEEE Int. Symp. on Electromagn. Compat. (EMC)*, 2008, in press.

[38] C.-C. Yen, C.-S. Liao, and M.-D. Ker, "New transient detection circuit for system-level ESD protection," in *Proc. IEEE Int. Symp. on VLSI Design, Automation and Test (VLSI-DAT)*, 2008, pp. 180-183.

[39] J.-J. Peng, M.-D. Ker, and H.-C. Jiang, "Latchup current self-stop circuit for whole-chip latchup prevention in bulk CMOS integrated circuits," in *Proc. IEEE Int. Symp. Circuits

Syst. (ISCAS), 2002, vol. 5, pp. 537–540.

[40] R. Merrill and E. Issaq, “ESD design methodology,” in *Proc. EOS/ESD Symp.*, 1993, pp. 233-237.

[41] P. Tong, W. Chen, R. Jiang, J. Hui, P. Xu, and P. Liu, “Active ESD shunt with transistor feedback to reduce latchup susceptibility or false triggering,” in *Proc. IEEE Int. Phys. Failure Anal. Integr. Circuits Symp. (IPFA)*, 2004, pp. 89-92.

[42] S. Poon and T. Maloney, “New considerations for MOSFET power clamps,” in *Proc. EOS/ESD Symp.*, 2002, pp. 1-5.

[43] J. Smith and G. Boselli, “A MOSFET power supply clamp with feedback enhanced triggering for ESD protection in advanced CMOS technologies,” in *Proc. EOS/ESD Symp.*, 2003, pp. 8-16.

[44] J. Li, R. Gauthier, and E. Rosenbaum, “A compact, timed-shutoff, MOSFET-based power clamp for on-chip ESD protection,” in *Proc. EOS/ESD Symp.*, 2004, pp. 273-279.

[45] M. Stockinger, J. Miller, M. Khazhinsky, C. Torres, J. Weldon, B. Preble, M. Bayer, M. Akers, and V. Kamat, “Boosted and distributed rail clamp networks for ESD protection in advanced CMOS technologies,” in *Proc. EOS/ESD Symp.*, 2003, pp. 17-26.

[46] C.-C. Yen and M.-D. Ker, “Failure of on-chip power-rail ESD clamp circuits during system-level ESD test,” in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2007, pp. 598-599.

[47] M.-D. Ker and S.-F. Hsu, “Component-level measurement for transient-induced latch-up in CMOS ICs under system-level ESD considerations,” *IEEE Trans. Device Mat. Rel.*, vol. 6, no. 3, pp. 461-472, Sep. 2006.

[48] *Electrostatic Discharge Simulator*, NoiseKen ESS-2002 & TC-825R, Noise Laboratory Co., LTD., Japan.

[49] *Technical Specification*, EMCPro Plus EMC Test system, Thermo Fisher Scientific Inc., U.S.A.

[50] M.-D. Ker and W.-Y. Lo, “Methodology on extracting compact layout rules for latchup prevention in deep-submicron bulk CMOS technology,” *IEEE Trans. on Semiconductor Manufacturing*, vol. 16, no. 2, pp. 319-334, 2003.

[51] S. Voldman, *Latchup*, John Wiley & Sons, 2008.

[52] M.-D. Ker and C.-Y. Wu, “Modeling the positive-feedback regenerative process of CMOS latchup by a positive transient pole method – part I: theoretical derivation,” *IEEE Trans. Electron Devices*, vol. 42, pp. 1141–1148, Jun. 1995.

[53] S. Bargstätd-Franke, W. Stadler, K. Esmark, M. Streibl, K. Domanski, H. Gieser, H. Wolf, and W. Bala, “Transient latch-up: experimental analysis and device simulation,” in *Proc.*

EOS/ESD Symp., 2003, pp. 80–87.

[54] G. Weiss and D. Young, "Transient-induced latchup testing of CMOS integrated circuits," in *Proc. EOS/ESD Symp.*, 1995, pp. 194–198.

[55] R. Troutman and H. Zappe, "A transient analysis of latchup in bulk CMOS," *IEEE Trans. Electron Devices*, vol. 30, pp. 170–179, Feb. 1983.

[56] E. Hamdy and A. Mohsen, "Characterization and modeling of transient latchup in CMOS technology," in *IEDM Tech. Dig.*, 1983, pp. 172–175.

[57] W. Morris, "Latchup in CMOS," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2003, pp. 76–84.

[58] D. Estreich, A. Ochoa Jr., and R. Dutton, "An analysis of latch-up prevention in CMOS IC's using an epitaxial-buried layer process," in *IEDM Tech. Dig.*, 1978, pp. 230–234.

[59] R. Troutman, "Epitaxial layer enhancement of n-well guard rings for CMOS circuits," *IEEE Electron Device Lett.*, vol. 4, no. 12, pp. 438–440, Dec. 1983.

[60] K. Fu, "Transient latchup in bulk CMOS with a voltage-dependent well-substrate junction capacitance," *IEEE Trans. Electron Devices*, vol. 32, pp. 717–720, Mar. 1985.

[61] G. Goto, H. Takahashi, and T. Nakamura, "Latchup immunity against noise pulses in a CMOS double well structure," in *IEDM Tech. Dig.*, 1983, pp. 168–171.

[62] R. Troutman and H. P. Zappe, "Layout and bias considerations for preventing transiently triggered latchup in CMOS," *IEEE Trans. Electron Devices*, vol. 31, pp. 315–321, Mar. 1984.

[63] R. Troutman and H. Zappe, "Layout and bias considerations for preventing transiently triggered latchup in CMOS," *IEEE Trans. Electron Devices*, vol. 31, pp. 315–321, Mar. 1984.

[64] S. Voldman, E. Gebreselasic, L. Lanzerotti, T. Larsen, N. Feilchenfeld, S. Onge, A. Joseph, and J. Dunn, "The influence of a silicon dioxide-filled trench isolation structure and implanted sub-collector on latchup robustness," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2005, pp. 112–120.

[65] S. Voldman, E. Gebreselasic, M. Zierak, D. Hershberger, D. Collins, N. Feilchenfeld, S. St. Onge, and J. Dunn, "Latchup in merged triple well structure," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2005, pp. 129–136.

[66] C. Duvvury and G. Boselli, "ESD and latch-up reliability for nanometer CMOS technologies," in *IEDM Tech. Dig.*, 2004, pp. 933–936.

[67] G. Boselli, V. Reddy, and C. Duvvury, "Latch-up in 65nm CMOS technology: a scaling perspective," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2005, pp. 137–144.

[68] S. Voldman, “Latchup and the domino effect,” in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2005, pp. 145–156.

[69] R. Troutman, *Latchup in CMOS Technology: The Problem and the Cure*, Kluwer Publications, New York, 1986.

[70] Semiconductor Industry Association (SIA), *International Technology Roadmap for Semiconductors (ITRS)*, 2005.

[71] M. Mahanpour and I. Morgan, “The correlation between latch-up phenomenon and other failure mechanisms,” in *Proc. EOS/ESD Symp.*, 1995, pp. 289–294.

[72] S. Voldman, “Latch-up – it’s back,” in *Threshold Newsletter*, ESD Association, Sep./Oct., 2003.

[73] S. Bargstätd-Franke, W. Stadler, K. Esmark, M. Streibl, K. Domanski, H. Gieser, H. Wolf, and W. Bala, “Transient latch-up: experimental analysis and device simulation,” in *Proc. EOS/ESD Symp.*, 2003, pp. 70-78.

[74] EIA/JEDEC Standard No. 78, “*IC Latch-up Test*,” Electronic Industries Association, 1997.

[75] *ANSI/ESD SP5.4-2004: Transient Latch-up Testing—Component Level Supply Transient Stimulation*, 2004. ESD Association Standard Practice.

[76] M. Kelly, L. Henry, J. Barth, G. Weiss, M. Chaine, H. Gieser, D. Bonfert, T. Meuse, V. Gross, C. Hatchard, and I. Morgan, “Developing a transient induced latch-up standard for testing integrated circuits,” in *Proc. EOS/ESD Symp.*, 1999, pp. 178–189.

[77] C. Brennan, K. Chatty, J. Sloan, P. Dunn, M. Muhammad, and R. Gauthier, “Design automation to suppress cable discharge event (CDE) induced latchup in 90nm CMOS ASICs,” in *Proc. EOS/ESD Symp.*, 2005, pp. 126-130.

[78] G. Cerri, R. Leo, and V. Primiani, “Investigation of radiated susceptibility during EFT tests,” *IEEE Trans. Electromagn. Compat.*, vol. 39, no. 4, pp. 298–303, Nov. 1997.

[79] G. Cerri, R. Leo, and V. Primiani, “Electrical fast-transient: conducted and radiated disturbance determination by a complete source modeling,” *IEEE Trans. Electromagn. Compat.*, vol. 43, no. 1, pp. 37–44, Feb. 2001.

[80] D. Smith, “An investigation into the performance of the IEC 100-4-4 capacitive clamp,” in *Proc. EOS/ESD Symp.*, 1996, pp. 223–226.

[81] C.-C. Yen and M.-D. Ker, “Transient-induced latchup in CMOS integrated circuits due to electrical fast transient (EFT) test,” in *Proc. IEEE Int. Phys. Failure Anal. Integr. Circuits Symp. (IPFA)*, 2007, pp. 11–13.

VITA

姓　　名：顏承正 (Cheng-Cheng Yen)

性　　別：男

出生日期：民國 65 年 5 月 13 日

出 生 地：新竹市

住　　址：新竹市光復路 2 段 10 巷 15 號

學　　歷：國立交通大學電機與控制工程系畢業 (83 年 9 月 - 87 年 6 月)

國立交通大學電子研究所碩士班 (87 年 9 月 - 89 年 6 月)

國立交通大學電子研究所博士班 (89 年 9 月入學)

論文名稱：互補式金氧半積體電路之系統層級靜電放電防護設計

System-Level ESD Protection Design in CMOS ICs with Transient Detection Circuits

Publication List

(A) Referred Journal Papers:

[1]. M.-D. Ker, **C.-C. Yen**, and P.-C. Shin, “On-chip transient detection circuit for system-level ESD protection to meet electromagnetic compatibility regulation,” *IEEE Trans. Electromagn. Compat.*, vol. 50, no. 1, pp. 13–21, Feb. 2008.

[2]. M.-D. Ker and **C.-C. Yen**, “Investigation and design of on-chip power-rail ESD clamp circuits without suffering latchup-like failure during system-level ESD test,” *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2533–2545, Nov. 2008.

[3]. **C.-C. Yen**, M.-D. Ker, and T.-Y. Chen, “Transient-induced latchup in complementary-metal-oxide-semiconductor integrated circuits under electrical fast transient test,” *IEEE Trans. Device Mater. Reliab.*, vol. 9, no. 2, *in press*, 2009.

[4]. **C.-C. Yen** and M.-D. Ker, “Electrical fast transient (EFT) induced latchup failure on power-rail ESD clamp circuits in CMOS integrated circuits,” *IEEE Trans. Electron Devices*, vol. 56, no. 6, *in press*, 2009.

[5]. M.-D. Ker, **C.-C. Yen**, and C.-S. Liao, “Transient-to-digital converter for system-level ESD protection in CMOS integrated circuits,” *IEEE Trans. Electromagn. Compat.*, *in press*, 2009.

[6]. M.-D. Ker and **C.-C. Yen**, “New transient detection circuit for on-chip protection design against system-level electrical transient disturbance,” submitted to *IEEE Trans. Ind. Electron.*.

[7]. M.-D. Ker, **C.-C. Yen**, and C.-S. Liao, “On-chip transient-to-digital converter for electrical fast transient (EFT) protection in CMOS integrated circuits with firmware co-operation,” submitted to *IEEE J. Solid-State Circuits*.

(B) International Conference Papers:

[1]. M.-D. Ker, **C.-C. Yen**, and P.-C. Shin, “On-chip transient detection circuit for system-level ESD protection in CMOS ICs,” in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2006, pp. 361–364.

[2]. **C.-C. Yen**, M.-D. Ker, and P.-C. Shin, “System-level ESD protection design with on-chip transient detection circuit,” in *Proc. IEEE Int. Conference on Electronics, Circuits and Systems (ICECS)*, 2006, pp. 616-619.

[3]. **C.-C. Yen** and M.-D. Ker, “Failure of on-chip power-rail ESD clamp circuits during system-level ESD test,” in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2007, pp. 598-599.

[4]. M.-D. Ker and **C.-C. Yen**, “Latchup-like failure of power-rail ESD clamp circuits in CMOS integrated circuits under system-level ESD test,” in *Proc. IEEE Int. Symp. Electromagn. Compat. (EMC)*, 2007.

[5]. **C.-C. Yen** and M.-D. Ker, “Transient-induced latchup in CMOS integrated circuits due to electrical fast transient (EFT) test,” in *Proc. IEEE Int. Phys. Failure Anal. Integr. Circuits Symp. (IPFA)*, 2007, pp. 11-13.

[6]. M.-D. Ker and **C.-C. Yen**, “Unexpected failure in power-rail ESD clamp circuits of CMOS integrated circuits in microelectronics systems during electrical fast transient (EFT) test and the re-design solution,” in *Proc. IEEE Int. Zurich Symp. Electromagn. Compat.*, 2007, pp. 69-72.

[7]. **C.-C. Yen**, C.-S. Liao, and M.-D. Ker, “New transient detection circuit for system-level ESD protection,” in *Proc. IEEE Int. Symp. VLSI Design, Automation and Test (VLSI-DAT)*, 2008, pp. 180-183.

[8]. M.-D. Ker, C.-S. Liao, and **C.-C. Yen**, “Transient detection circuit for system-level ESD protection and its on-board behavior with EMI/EMC filters,” in *Proc. IEEE Int. Symp. Electromagn. Compat. (EMC)*, 2008.

[9]. M.-D. Ker, **C.-C. Yen**, C.-S. Liao, T.-Y. Chen, and C.-C. Tsai, “Transient-to-digital converter for ESD protection design in microelectronic systems,” in *Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC)*, 2008, pp. 409-412.

[10]. **C.-C. Yen**, M.-D. Ker, C.-S. Liao, T.-Y. Chen, and C.-C. Tsai, “Transient-to-digital converter for protection design in CMOS integrated circuits against electrical fast transient,” in *Proc. IEEE Int. Symp. Electromagn. Compat. (EMC)*, 2009, *in press*.

(C) Local Conference Papers:

[1]. **C.-C. Yen**, M.-D. Ker, and P.-C. Shin, “Design of transient detection circuit for on-chip system-level ESD protection,” in *VLSI Design/CAD Symposium*, 2006.

[2]. **C.-C. Yen** and M.-D. Ker, “On-chip transient detection circuit for system-level ESD protection,” in *Proc. Taiwan ESD Conference*, 2006, pp. 94–99.

[3]. 顏承正 and 柯明道, “應用於系統層級靜電放電防護設計之暫態對數位轉換器,” in *Proc. Taiwan ESD Conference*, 2008, pp. 44–47.

(D) Patents:

[1]. M.-D. Ker, **C.-C. Yen**, and T.-Y. Chen, “On-chip power-rail ESD clamp circuits with reset function against system-level ESD failure,” U.S. and R.O.C. patent pending.

[2]. M.-D. Ker, **C.-C. Yen**, and T.-Y. Chen, “On-chip transient detection circuit for ESD protection,” U.S. and R.O.C. patent pending.

[3]. M.-D. Ker, **C.-C. Yen**, C.-S. Liao, and T.-Y. Chen, “Transient-to-digital converters for system-level ESD protection,” U.S. and R.O.C. patent pending.

[4]. M.-D. Ker, **C.-C. Yen**, C.-S. Liao, and T.-Y. Chen, “On-chip transient detection circuit for ESD protection,” U.S. and R.O.C. patent pending.