國 立 交 通 大 學

電信工程學系

碩 士 論 文

應用電容誤差校正技術之 CMOS 導管式類比數位轉換器

A CMOS Pipelined Analog-to-Digital Converter With Capacitor-Mismatch Calibration Technique

研究生：邱建豪

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中 華 民 國 九十六 年 十 月

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摘要

在無限通訊系統以及影像或音訊應用中，類比數位轉換器扮演了一個重要的角色。當今，對於低功率、高速及高解析度之類比數位轉換電路有著不可或缺的需求。在許多種類之互補式金氧半類比數位轉器的架構當中，導管式類比數位轉換器幾乎可以同時達到以上所述之三項效能。

在此次研究當中，一個十位元每秒取樣 100 百萬次操作電壓為 1.8 伏特的導管式類比數位轉換器，從設計、佈局到製造均使用台積電標準 0.18 微米互補式金氧半製程來完成，最後並完整地測試晶片。此類比數位轉換器主要包含前端的取樣保持電路、相同 8 級串接的轉換器，和最後一級的 2 位元的快閃式轉換器。所有的類比電路皆以全差動輸入設計，輸入峰對峰 1.2V 的輸入訊號並且供應電源為 1.8 伏特。採用每級 1.5 位元解析度的架構是為了更高之類比數位轉換器之轉換率。同時結合數位錯誤校正技術，可容忍比較器的偏移電壓到某個程度，使比較器不需要前置放大器，進而減少整體的功率消耗。最後，因為製程漂移讓電容發生不匹配而導致的增益錯誤，對於導管式類比數位轉換器來說是無法避免的非線性效應。與過去的傳統架構來比較，此研究應用了”隨機切換電容”的技術來抵抗電容不匹配之錯誤並維持線性度。當類比數位轉換器操作在保持相位時，此方法讓位於一級之內的迴授電容可與取樣電容做隨機的切換，換句話說，這兩種電容角色可以隨機互換。所以在此機制下，每一級發生的電容不匹配錯誤可被平均出來並提昇整體類比數位轉換器之線性度。

此原型設計的類比數位轉換器之模擬表現出在頻率 100 萬赫茲的輸入弦波訊號下,無寄生動態範圍(SFDR)達到 69.43dB，訊號對雜訊加上失真比(SNDR)約為 59.15dB 且有效位元數將近 10 位元。最大的微分型非線性誤差為 0.55 最小位元單位,積分型非線性誤差則是 0.7 最小位元單位。當我們假設有 3%的電容不匹配存在時，實驗結果顯示線性度依然維持住，足以證明此技術之有效性。當輸入 80 百萬赫茲取樣頻率及 100 萬赫茲輸入訊號的情形，操作在隨機切換電容模式下，量測到的 SNDR 為 42.73dB、ENOB 約為 6.81 位元;當操作在關閉隨機電容切換模式下，所量測到的 SNDR 降低為 33.57dB、ENOB 約為 5.28 位元。此類比數位轉換器晶片面積約 1.87mm^2，並在最大取樣頻率 100 百萬赫茲及 1.8 伏特電源供應下,共消耗功率 88 毫瓦。

A CMOS Pipelined Analog-to-Digital Converter With Capacitor-Mismatch Calibration Technique

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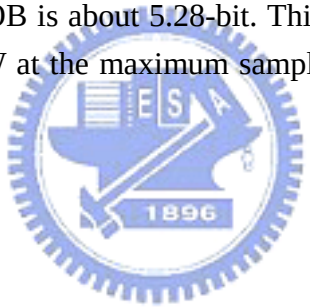
Abstract

The analog-to-digital converter (ADC) plays a critical role in wireless communication systems and video/audio applications. Nowadays, the demand for low-power, high-speed, and high-resolution ADC circuit is indispensable. Among many types of CMOS ADC architectures, the Pipelined architecture can almost achieve above three performances at the same time.

In this work, a 10-bit 100MS/s Pipelined A/D converter operated at 1.8V power supply had been designed, laid out, and fabricated with standard TSMC 0.18μm CMOS 1P6M process, and this chip was also measured completely. This ADC mainly consists of one front-end S/H, eight cascaded MDAC stages, and a 2-bit flash converter in the last stage. All analog circuits are fully differential with a 1.2Vpp input signal and 1.8V power supply. A 1.5-bit/stage architecture is adopted for higher conversion rate. Furthermore, incorporating digital error correction technique, which is a successful algorithm of the redundant signed digit (RSD), tolerates comparators offset to some extent and thus no preamplifier is required. Therefore, total power consumption is reduced. Gain error resulted from capacitor-mismatch which is due to process variation, is an inevitable non-linear effect for the Pipelined ADC. As

compared with the conventional architecture, this research implements a “random capacitor-swapping” technique against the capacitor-mismatch error and maintains the linearity. This technique makes the feedback capacitor randomly swapped with the sampling capacitor in one stage during the hold cycle of the ADC operation, that is, their roles can randomly interchange. Therefore, the capacitor-mismatch error in each stage can be averaged out, and thus overall Pipelined ADC linearity is improved.

The prototype design of ADC simulation exhibits a peak spurious-free dynamic range (SFDR) of 69.43dB, a signal-to-noise-plus-distortion ratio (SNDR) of 59.15dB and the effective number of bits (ENOB) is about 10-bit with a 1MHz sinusoidal input. The maximum differential non-linearity (DNL) is 0.55 least significant bits (LSB) and the integral non-linearity is 0.7LSB. When we assume that there exists a 3% capacitor mismatch, experimental result shows the linearity still sustain to demonstrate the effectiveness of this technique. At 80MHz sampling rate with 1MHz sinusoidal input, the measured peak SNDR is 42.73dB and ENOB is about 6.81-bit when the capacitor-swapping is on; when the capacitor-swapping is off, the measured SNDR degrades to 33.57dB and ENOB is about 5.28-bit. This A/D chip occupies an area of 1.87mm^2 and dissipates 88mW at the maximum sampling rate of 100MHz with 1.8V supply voltage.



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Chapter 1

Introduction

1.1 Motivation

With the rapid evolution of CMOS fabrication technology, more and more signal-processing functions are implemented in the digital domain for lower cost, lower power consumption, and higher yield requirements. As compared with analog circuits, digital circuits are not easily influenced by noise, operating voltage, and process variation. Nowadays, many applications utilize the digital signal processing (DSP) to resolve the transmitted information. Even though digital circuits have so many advantages, they must eventually communicate with the nature environment which abounds with analog signal. Therefore, an analog-to-digital interface between the received analog signal and the DSP system is required and critical. This interface achieves the digitization of the received waveform subject to a sampling rate requirement of the system. In order to make the transmission system more accurate, reliable, storable, faster, and higher yields, the interface of ADC is a critical component and plays an important role in the system.

Furthermore, the trend of increasing integration level for integrated circuits leads to systems with fewer numbers of chips, lower power dissipation, and process integration. The ultimate goal is to be a single chip solution, the system on a chip (SoC). This trend has forced the ADC to reside on the same silicon with a large amount of DSP and digital circuits. By operating at the same supply voltage on the same die, it reduces the overall system cost to save the requirement of generating

multiple supply voltages with DC-DC converters. Therefore, an ADC operating at the same voltage with digital circuits is desirable, and it makes low voltage operation to be a relevant issue. Besides, there is also a tendency for boosting the transmitted data rates, which is based on wider signal bandwidth and higher signal-to-noise ratio in the wireless communication or image processing systems, so, the increasing conversion rate and higher resolution of ADCs are urgently required.

However, the design of data converter accompanying the scaling of CMOS technology has more challenges to confront. Such as thinner gate-oxide in MOS devices, which bring about the problem of reliability and hot carrier effect; and the short channel effect, which is the cause of punch-through. Besides, the lower operating voltage following scaling CMOS technology also makes analog (mixed signal) circuits that emphasize transistors work region to face enormous difficulties in design. As a result, how to overcome these difficulties and choose an appropriate structure in Mixed-Mode ADC design are the research points.

The applications of analog-to-digital converters are widespread, such as wireless communication systems, cellar phones, digital video (audio) systems, etc…, as illustrated in Figure 1.1 [1].

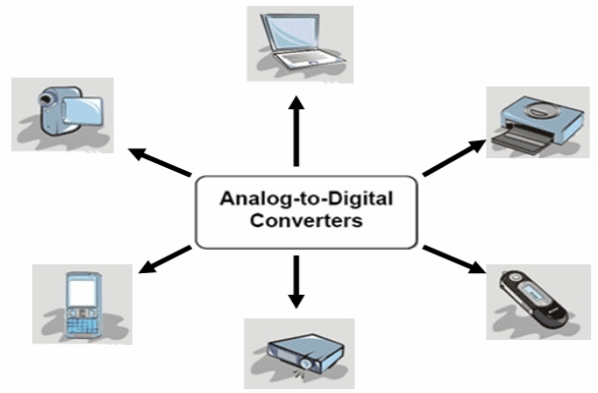


Figure 1.1 Applications of analog-to-digital converters

There are different applications for different architectures of analog-to-digital converters. Various commercial applications demand different ADCs resolution and speed they claim, as illustrated in Figure 1.2. Also, many kinds of ADCs having their own characteristics are chosen for the best suitable applications, as illustrated in Figure 1.3 [2].

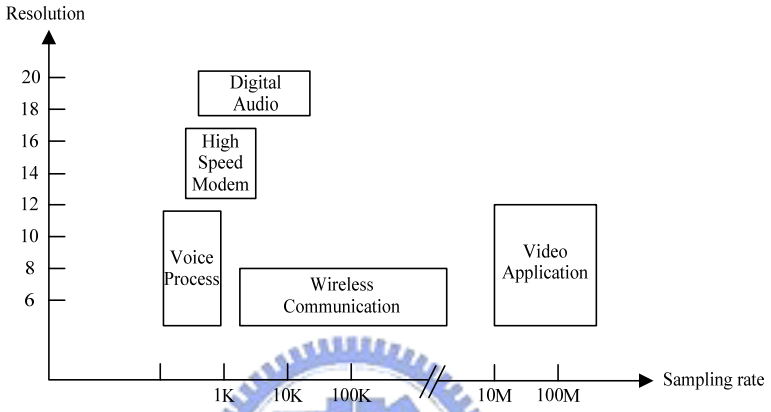


Figure 1.2 ADC spec. v.s applications

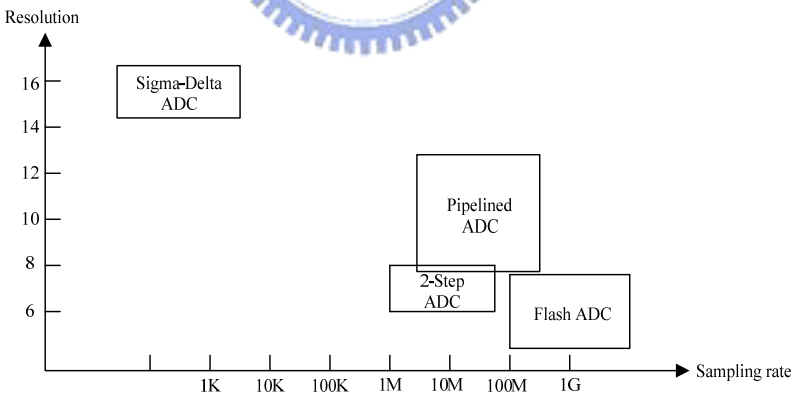
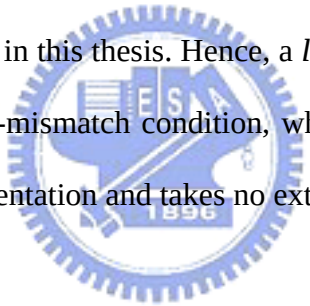


Figure 1.3 ADC architectures v.s sampling rate and resolution

Among many types of CMOS ADC architectures, the Pipelined ADC has many attractive merits in conversion speed, input bandwidth, power consumption, and chip area, that is, the Pipelined architecture offers good trade-off among speed, resolution, and power for Nyquist-ADC [3] when compared to other architectures.

This work, a 10-bit 100MS/s Pipelined A/D converter with a 1.8V supply voltage had been designed and implemented with standard TSMC 0.18μm CMOS 1P6M process, and no special process or multiplied voltage is required. Here the front-end "pre-charged" S/H, which is adopted to achieve high sampling rate, is easily designed to sample more precisely and settle more quickly than the conventional "flip-around" architecture. A 1.5-bit/stage architecture of digital error correction is adopted to make each Pipelined stage capable of correcting comparator offset errors from previous stages, relaxing the comparator accuracy for lower power requirement. Finally, a switched-capacitor (SC) implementation in the Pipelined ADC is sensitive to mismatch of capacitors, and the capacitor ratio determines the inter-stage gain. Therefore, a precision inter-stage gain is required to achieve the desired overall ADC linearity and we concentrate it in this thesis. Hence, a *linearity-improving* technique is employed under the capacitor-mismatch condition, which shows good linearity. It is not complex in circuit implementation and takes no extra clock cycle for calibration.



1.2 Thesis Organization

This thesis is organized into six chapters and is described as following.

Chapter 1 briefly introduces the analog-to-digital converters and this thesis.

Chapter 2 begins with the concepts of analog-to-digital conversion and performance metrics used to characterize ADCs. Then, several high-speed ADC architectures are introduced and the evolution of them is described. Finally, the Pipelined architecture is chosen and we focus on it in summary.

Chapter 3 concentrates on the characteristics of the Pipelined ADC, which is described in detail from its operation principle to the actual implementation of each stage including 1.5-bit/stage architecture with digital error correction. Furthermore, the behavioral models simulations of a Pipelined ADC are built to obtain the requirement of design, and we analyze the effects of circuit components non-idealities. Finally, the proposed technique of capacitor-mismatch calibration is introduced, and it was applied in our design to prevent overall resolution from degrading due to the capacitor-mismatch effect.

Chapter 4 illustrates the design and implementation of the Pipelined ADC with capacitor-mismatch calibration technique, where key circuit components will be introduced in detail. Among them are the operational amplifier, the bootstrapped switch, the comparator, the input stage sample-and-hold circuit (S/H), the 1.5-bit/stage circuit, the 2-bit flash ADC, and digital circuits including clock generator. The transistor level simulation results of each circuit are presented, and the simulation

of whole Pipelined ADC, as well as its layout and floor plan are also shown at the end of this chapter.

Chapter 5 presents the measurement environment, including component circuits on the DUT (device under test) board and the required instruments. Finally, the measured results of the prototype chip described in Chapter 3 and Chapter 4 are shown and summarized.

Finally, Chapter 6 is the conclusion for this work. Some suggestions and improved recommendations are proposed for the future work.

Chapter 2

Fundamentals and Architectures of Analog-to-Digital Converters

2.1 Introduction

In this chapter, we first introduce the concepts of analog-to-digital conversions and discuss some fundamental issues in the design of data converters, which are the performance metrics to characterize ADCs. Second, some of the prominent ADC architectures for high-speed applications are the surveyed subjects and each of them has different trade-off among speed, resolution, power and area. At the end of this chapter, we summarize and focus on the most appropriate architecture to meet our target specification.

2.2 The Concept and Performance Limitations of A/D Converters

In signal transmission systems linking between the nature world and the digital processors, data converters including ADC and DAC are the devices translating the analog signals into digital codes or performing the reverse operation.

Figure 2.1 shows an overall signal transmission system [4]. The original analog signal (a) is filtered by an anti-aliasing filter (b) to remove any high-frequency components that may cause an effect known as aliasing. Then, the signal is converted into a digital form (d) by the analog-to-digital conversion (c) separated into two operations: sampling and quantization. Sampling operation transforms the continuous

and infinite valued signal into a corresponding discrete time signal, while quantization operation quantizes the discrete time signal to have a certain digital code level for each discrete period, which is generally expressed as conversion period. However, some ADC architectures, such as Flash ADC, can execute sampling and quantization simultaneously to achieve very high throughput rates.

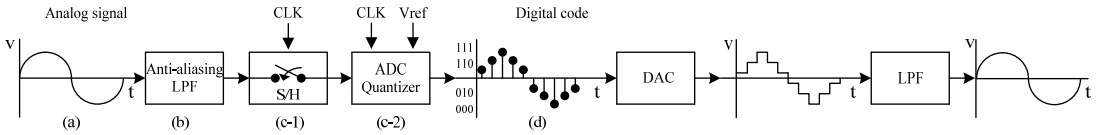


Figure 2.1 Signal characteristics caused by data conversion

2.2.1 Quantization and Error

The analog-to-digital conversion tends to quantize the sampled input analog signal into an N-bit digital word, which is known as the total resolution. That is, the full range of analog signal defining as V_{FS} is divided into several smaller sub-ranges (segments) according to the numbers of quantization steps 2^N, and these sub-ranges are uniform in size ideally. Figure 2.2 illustrates the ideal conversion transfer curve of an N-bit ADC. During the conversion process, the value of signal in which segment range is decided and sends a set of corresponding output digital word representing the sampled input signal [5]. Furthermore, the quantization step size of each sub-range are also referred to as one least significant bit (LSB), and V_{LSB} is the difference of two transition voltages defined as

$$V_{LSB} = \frac{V_{FS}}{2^N} \tag{2.1}$$

, and the transition voltages can be written as

$$V_{tn} = \frac{V_{FS}}{2^N} \cdot n, \quad n \in \{0,1,2,...,2^N\} \tag{2.2}$$

By the way, if the circuit is operated in fully differential, then $V_{FS}=2V_{REF}$, where V_{REF} is the analog reference signal applied to ADCs.

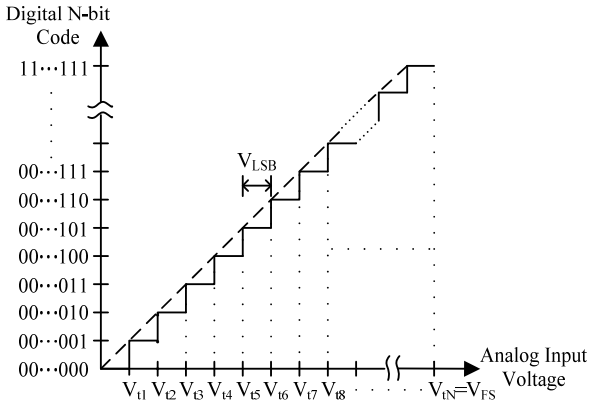


Figure 2.2 Ideal conversion characteristic of a N-bit ADC

Since the analog input signal is continuous-valued and the digital output is discrete-valued, this signal ambiguity produces what is known as quantization error, Q_e, is defined as the difference between the actual analog input and the value of the quantized staircase given in voltage. In Figure 2.3(a), we take an ideal 3-bit ADC conversion for example and shift the transfer curve like Figure 2.2 to the left by 1/2 LSB [4], showing in Figure 2.3(b). The midpoints of the staircase curve defining $V_{staircase}$ can be calculated by

$$V_{staircase} = D \cdot \frac{V_{FS}}{2^N} = D \cdot V_{LSB} \tag{2.3}$$

, where the quantization error can be generated by subtracting the value of the staircase from the dashed line, and Q_e is represented as

$$Q_e = V_{IN} - V_{staircase} \tag{2.4}$$

The result can be seen in Figure 2.3 (c), where a sawtooth waveform is centered about zero.

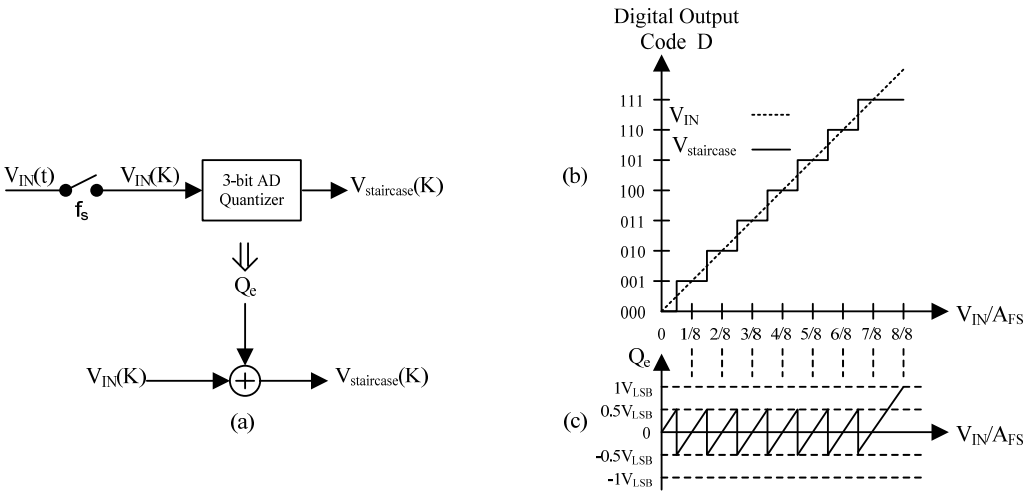


Figure 2.3 (a) An Ideal 3-bit AD quantizer (b) Transfer curve

(c) Quantization error centered about zero

As mentioned in Figure 2.3, quantization errors even occur in ideal A/D converters. Clearly, the average of Q_e is zero and is limited to $\pm 0.5V_{LSB}$, therefore, we can model these errors as being equivalent to an additive noise source and find its power. We assume that the quantization error Q_e is a random variable uniformly distributed between $\pm 0.5V_{LSB}$. The probability density function (PDF) for such an error signal will be a constant value, as shown in Figure 2.4. Hence, the quantization noise power (variance) P_Q can be calculated by

$$P_Q = \int_{-\infty}^{\infty} q^2 f_Q(q) dq = \frac{1}{V_{LSB}} \int_{-0.5V_{LSB}}^{0.5V_{LSB}} q^2 dq = \frac{{V_{LSB}}^2}{12} \qquad (2.5)$$

, and the R.M.S value of the quantization noise equals $V_{LSB} / \sqrt{12}$.

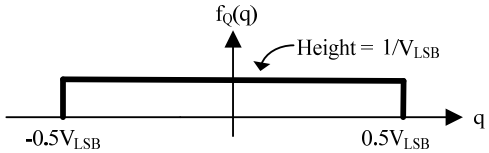


Figure 2.4 Assumed probability density function of the quantization error Q_e

Finally, we can conclude that the quantization noise power is independent of the sampling frequency, f_s; on the contrary, it is proportional to the size of V_{LSB}. The size of V_{LSB} is halved and the noise power decreases by 6 dB for each additional bit-resolution in the A/D converter.

2.2.2 ADC Performance Metrics

In this section, some commonly used definition indicating the performance of the analog-to-digital converters are introduced as below, which can be separated into dynamic characteristics and static characteristics [4][6][7].

Dynamic Characteristics:

Resolution

The "ideal" resolution of ADCs is defined as the numbers of distinct analog input sub-ranges corresponding to the different output digital words. For a fixed full-scale analog input range, an N-bit resolution implies that the converter can resolve 2^N distinct input segments, and the high resolution can resolve smaller sub-ranges of signals than the low resolution. Nevertheless, the "actual" resolution is generally degraded by either noise or non-linearity in ADCs, so it is also treated as effective number of bits (ENOB) of the ADC output digital bits.

Signal-to-Noise Ratio (SNR)

A sinusoidal input signal is usually used to characterize a data converter. The signal to noise ratio (SNR) means the ratio of the signal power to the noise-floor power at ADCs output, and the relationship is expressed as

$$SNR = 20log_{10}\left(\frac{V_{IN\_signal(RMS)}}{V_{Total\_noise(RMS)}}\right) \text{ dB} \tag{2.6}$$

We assume that the sampled sinusoidal input has the form as

$$V_{IN}(k) = A\sin\left(2p\ f_i \cdot kT_s\right) \tag{2.7}$$

, and its R.M.S value is $A/\sqrt{2}$. The noise power here is only referred to the quantization noise and its R.M.S value had been described as $V_{LSB}/\sqrt{12}$. Therefore, when the input amplitude equals $A = A_{FS}/2$, the maximum SNR of an N-bit ADC is

$$\begin{aligned} SNR &= 20log_{10}\left(\frac{V_{IN\_signal(RMS)}}{V_{Q(RMS)}}\right) = 20log_{10}\left(\frac{A/\sqrt{2}}{V_{LSB}/\sqrt{12}}\right) = 20log_{10}\left(\sqrt{\frac{3}{2}}2^N\right) \\ &= 6.02 \cdot N + 1.76\text{dB} \end{aligned} \tag{2.8}$$

, and it decreases from this best value for reduced input signal levels [8].

Signal-to-Noise＋Distortion Ratio (SNDR)

The signal to noise plus distortion ratio (SNDR) is often used to measure the performance of an ADC. When a single frequency sinusoidal signal is applied to the ADC system, the fast Fourier transform (FFT) of the system output generally contains a tone at the fundamental (input) frequency. Due to distortion, the output also contains signal tone including aliasing at all harmonics of the input frequency. As a result, the SNDR of the ADC is defined as the ratio of the signal power at the fundamental frequency to the total power of non-ideal effects, including all harmonic distortions (HD) and all of the noise sources presented at the output, which is expressed as below

$$SNDR = 20log_{10}\left(\frac{V_{IN\_signal(RMS)}}{V_{Total\_noise(RMS)} + V_{Total\_HD(RMS)}}\right) \text{ dB} \tag{2.9}$$

Furthermore, we can derive the effect number of bits (ENOB) to observe how the actual resolution influenced by the combined non-ideal effects to what extent, which

is calculated by the value of SNDR

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{2.10}$$

Spurious-Free Dynamic Range (SFDR)

The spurious free dynamic range is defined as the ratio of the fundamental signal component to the largest distortion component being usually at 3rd harmonic in a specified frequency range and expressed as

$$SFDR = 20log_{10}\left(\frac{V_{IN\_signal(RMS)}}{V_{Max\_HD(RMS)}}\right) \text{ dB} \tag{2.11}$$

Finally, we can easily get much more understanding among SNR, SNDR, and SFDR by the FFT spectrum plot illustrated in Figure 2.5, where S is the fundamental frequency of the input signal, D are the harmonic distortion components, and N is the noise floor.

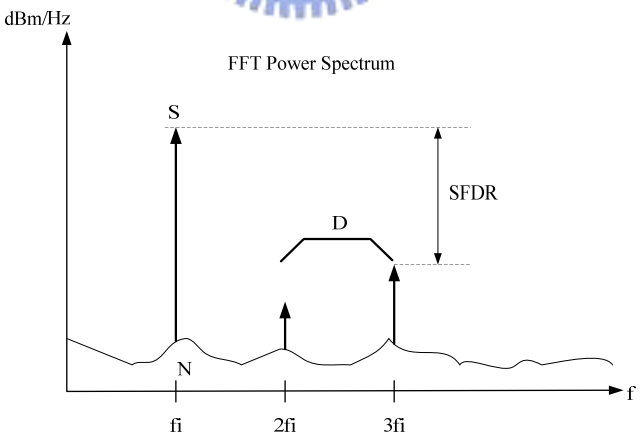


Figure 2.5 The power spectrum with the signal, distortions and noise

Furthermore, SNR and SNDR in Figure 2.5 are respectively depicted as

$$SNR = \frac{S}{N} \qquad SNDR = \frac{S}{N + D} \tag{2.12}$$

Dynamic Range (DR) and Effective Resolution Bandwidth (ERB)

Dynamic range (DR) is a measure of the range of input sinusoidal signal amplitudes, which is also a useful performance benchmark. We apply a single frequency signal to the ADC and vary its amplitude, the definition of dynamic range is the ratio of the input signal level with maximum SNR to the input signal with 0dB SNR, as shown in Figure 2.6(a). SNR with 0dB means that the input signal is too indistinct to be recognized and is the minimum detectable power. If the noise power is independent of the signal level, the dynamic range is equal to the SNR at full scale. Nevertheless, in most conditions, the noise power increases as the signal level increases. In general, the actual maximum SNR is less than the defined dynamic range [5][8]. Figure 2.6(a) also indicates that the harmonic distortions increases as the increasing signal level, and then the value of SNR is severely degraded by distortions.

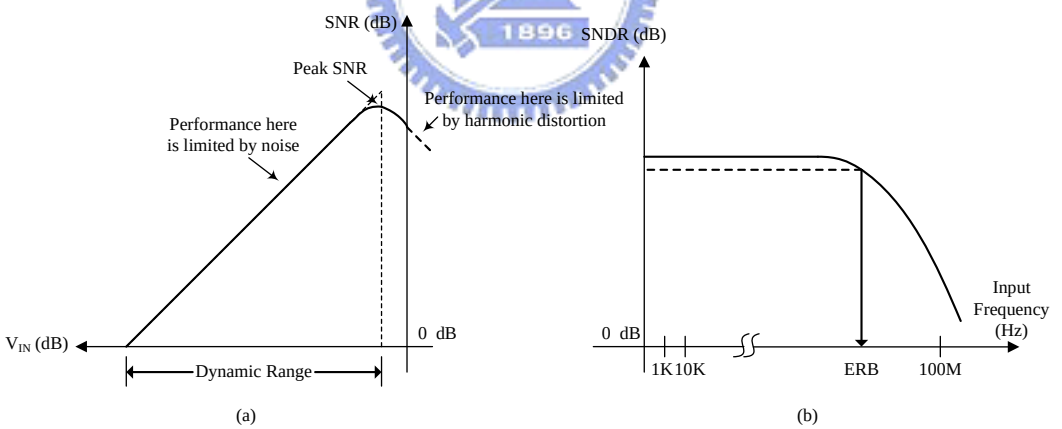


Figure 2.6 (a) Dynamic range (b) Effective resolution bandwidth

Figure 2.6(b) shows that SNDR gradually decreases as the input signal frequency increases. The maximum input frequency that can sustain efficient SNDR dropping about 3dB is called the effective resolution bandwidth (ERB). This bandwidth is limited by Nyquist Sampling Theorem to avoid aliasing.

Static Characteristics:

Offset Error

ADCs have an Input-Output transfer characteristic of quantization that approximates a straight line, and it progresses from low-to-high in uniform steps ideally. However, the practical transfer steps might be not uniform ideally. The imperfections cause errors or non-linearity performance in ADCs. In Figure 2.7, an error which causes the actual steps to shift horizontally from their ideal positions by a constant amount is called the offset error.

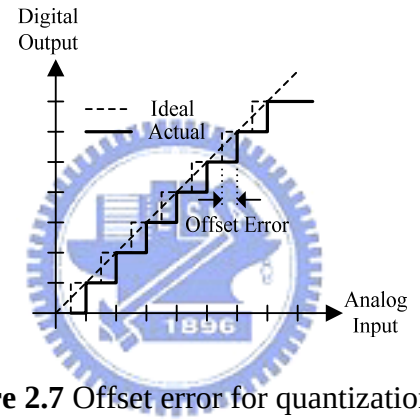


Figure 2.7 Offset error for quantization

Gain Error

Gain error or scale factor error, seen in Figure 2.8, is the difference between the slope of a straight line drawn through the midpoints of the actual transfer steps and the ideal slope of 1 [9].

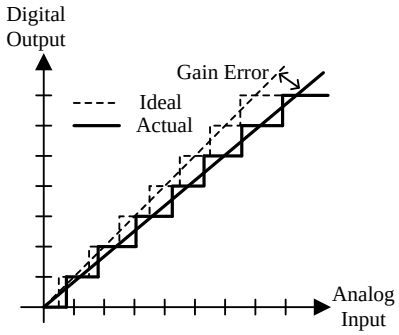


Figure 2.8 Gain error for quantization

Differential Non-Linearity (DNL) and Missing Code

Each width of quantization steps may not equal to one LSB (1LSB = $A_{FS}/2^N$) due to the non-idealities in ADCs. Then, the differential non-linearity (DNL) is defined as the value of each step width deviating from the ideal step width as Figure 2.9

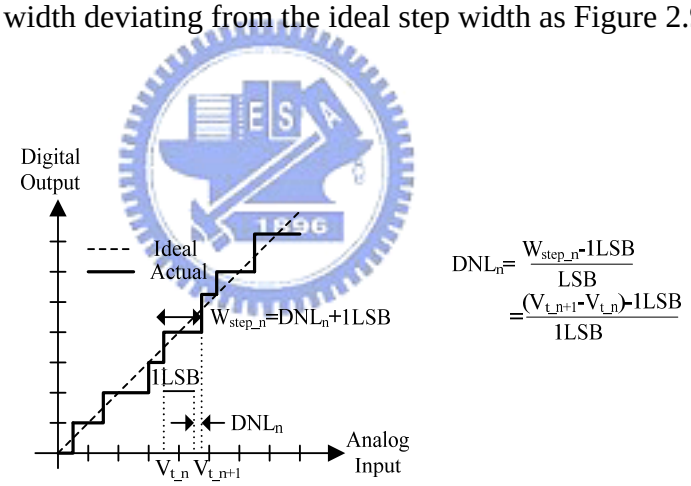


Figure 2.9 DNL for quantization

ADCs possessing a DNL that is equal to -1LSB are guaranteed to have a missing code, as illustrated in Figure 2.10. The step width corresponding to $Code_k$ is completely missing; thus, the value of DNL_k is -1LSB.

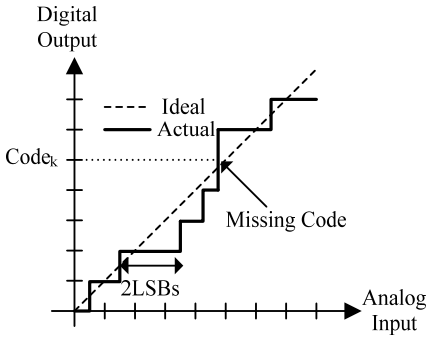
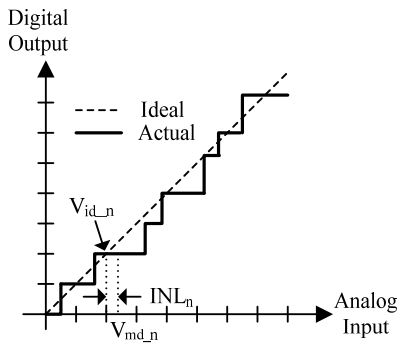


Figure 2.10 Missing code for quantization

On the contrary, DNL larger than +1LSB is not guaranteed to have a missing code, though in all probability a missing code will occur.

Integral Non-Linearity (INL)

The integral non-linearity (INL) is defined as the total deviation of the middle point of step from the ideal value that ADCs tend to approximate. Unlike the DNL, INL can be any values and can be expressed in Figure 2.11, where V_{md_n} is the middle point of the n-th step, and V_{id_k} is the ideal middle point value of this step. From another view-point, INL_n equals to the summation of DNL_0 to DNL_n.



$$INL_n = \sum_{i=0}^{n} DNL_i = \frac{V_{md\_n} - V_{id\_n}}{1LSB}$$

Figure 2.11 INL for quantization

Finally, DNL and INL are expressed in the unit of least significant bits (LSBs),

and ADCs main non-linear effects including DNL, INL as well as Missing Code will cause the non-monotonic characteristic and enhance distortions.

2.3 ADC Architectures Overview

A/D converters can be classified into two types of Nyquist-rate and Over-sampling. According to the speed and accuracy for different applications, the architectures of Nyquist-rate ADCs can be roughly divided into three categories: low-to-medium speed, medium speed, and high speed, as shown in Table 2.1. Choosing each of them has different trade-off among speed, resolution, power and area for the best solution [10][11]. Generally, the Over-Sampling architecture of the ADC is adopted for high resolution (16-bit above) design [10]. In this section, the architectures of Flash, Two-Step and Pipelined will be discussed for their close relationship.

Spec.	*Architecture*
Low-to-Medium Speed, High Resolution	Integrating ADC Over-Sampling (Delta-Sigma) ADC
Medium Speed, Medium Resolution	Successive Approximation ADC Algorithmic ADC
High Speed, Low-to-Medium Resolution	Flash ADC Two-Step ADC Interpolating ADC Folding ADC Pipelined ADC Time-Interleaved ADC

Table 2.1 A/D Converter Architectures

2.3.1 Flash ADC

The Flash ADC [12][13] is the standard approach for realizing very-high-speed

converters. For N-bit resolution, the input signal of a Flash ADC is simultaneously fed to 2^N comparators in parallel, each of the comparators samples the input signal and compares the signal to its corresponding reference value, as shown in Figure 2.12. The series of reference voltages are generated equally spaced by dividing a resistor string connected between $+V_{REF}$ and $-V_{REF}$ and are applied to one input of each comparator. Any comparator connected to a resistor string node where the reference of each comparator is larger than the input signal will have outputs of 1, while those connected to nodes with reference voltages less than the input will have outputs of 0, and the level of the interface between 0s and 1s would indicate the value of the signal. The set of 2^N comparator outputs is commonly referred to as a thermometer code since it looks quite similar to the mercury bar in a thermometer and is encoded to N-bit binary code word with an encoding circuit. Besides, the NAND gates called as the pre-encoder are also designed to remove the bubble error usually occurring near the transition point of the thermometer code. As seen from the Figure 2.12, the process of the input sampling and quantizing are operation in parallel. Thus, the Flash ADC can be capable of very high speed (high throughput and small latency) and its conversion time is only limited by the speed of the comparators.

The most main drawback to the Flash ADC is the huge requirement of hardware which grows exponentially with the increasing resolution, especially the comparators mentioned earlier. For high resolution, the large amounts of comparators take up a large area and consume much power, while the Interpolating and Folding technique can overcome them. Besides, such many comparators have large input capacitive loading limiting the conversion speed and are sensitive to offsets affecting the accuracy. For these reasons, ADCs with resolution higher than 8-bit we rarely adopt the Flash architecture.

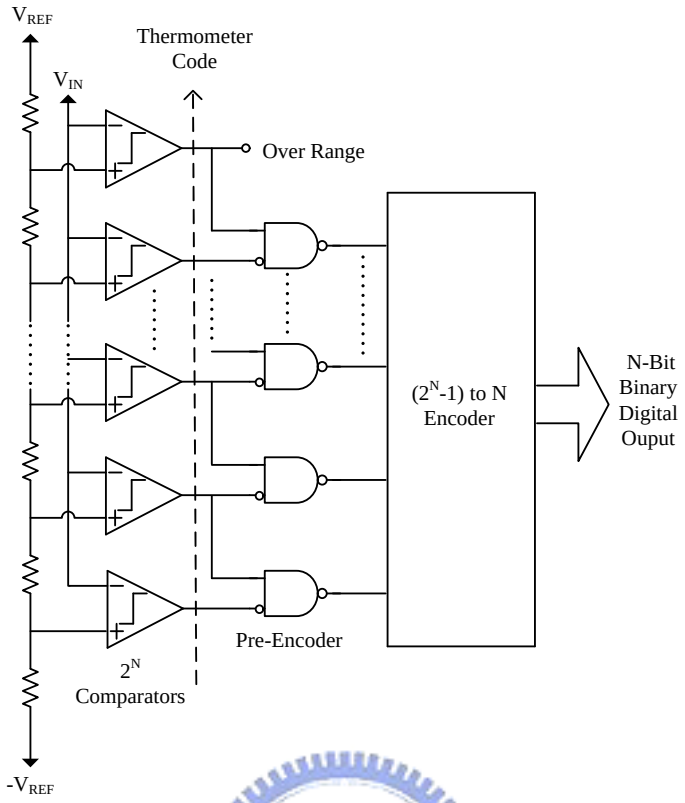


Figure 2.12 N-bit Flash ADC

2.3.2 Two-Step ADC

In order to solve the problems of chip area and power making Flash architectures impractical for higher resolution, the Two-Step (or Sub-Ranging) architecture [14][15] is adopted adequately and its block diagram is shown in Figure 2.13(a). It consists of a front-end S/H, a coarse MSB Sub-ADC of Flash type, a Digital-to-Analog converter (DAC), a Subtractor, and a fine LSB Sub-ADC of Flash type. As implied by the name, the conversion of this ADC architecture takes two steps for total N-bit resolution.

First, the S/H circuit samples the input signal and the first (N/2)-bit most significant bits (MSBs) are generated through the coarse Flash ADC. Subsequently, the DAC converts the first (N/2)-bit digital code back to an analog signal subtracted from the sampled input signal and is known as the residue. This residue is then

amplified by $2^{N/2}$ and is fed to the fine Flash ADC, so the last (N/2)-bit least significant bits (LSBs) are also determined. Therefore, final total N-bit resolution is achieved by combining (N/2)-bit MSBs and (N/2)-bit LSBs, and the conversion process is shown in Figure 2.13(b).

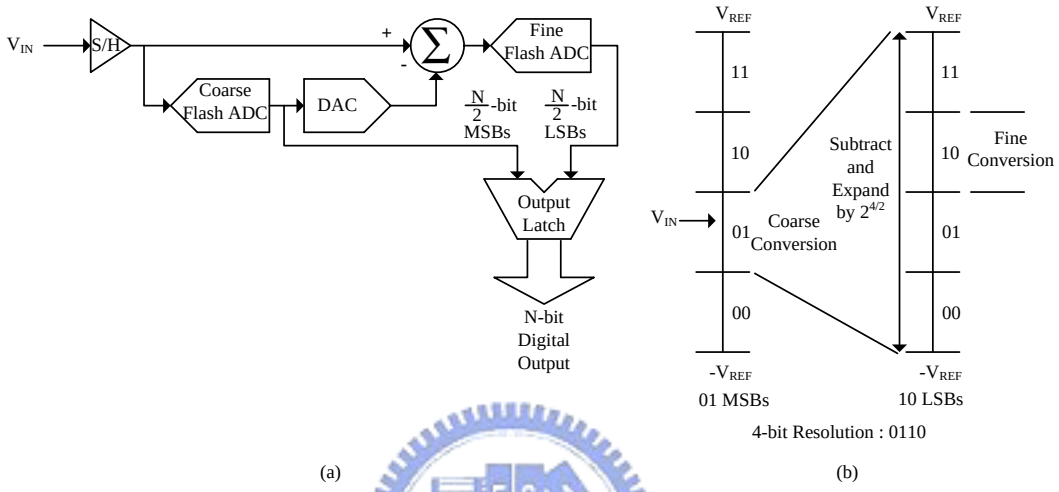


Figure 2.13 (a) N-bit Two-Step ADC (b) Coarse and Fine Conversions

When compared with the Flash ADC, the Two-Step ADC has more potential for high resolution due to fewer numbers of the comparators. For total N-bit resolution, the Two-Step ADC only requires $2 \cdot 2^{N/2}$ comparators, therefore, the chip area and power consumption are greatly saved than the Flash ADC. However, the speed of the Two-Step ADC is slower than the Flash ADC due to the larger latency delay, although the throughput rate approaches that of the Flash ADC.

2.3.3 Pipelined ADC

Pipelined architecture combines the characteristics of Flash and Two-Step architectures. In actuality, the Pipelined ADC could divide the number of conversions

into many steps relative to the Flash and Two-Step ADCs, and the quantization is distributed along a Pipelined signal chain resulting in an effective architecture for high-resolution and high-speed applications. By the idea of the Two-Step architecture, it is spread to a multi-stage architecture to construct the Pipelined ADC that has features of improving the throughput rate and tolerating the comparator offsets [16][17][18]. The block diagram of the Pipelined ADC is shown in Figure 2.14.

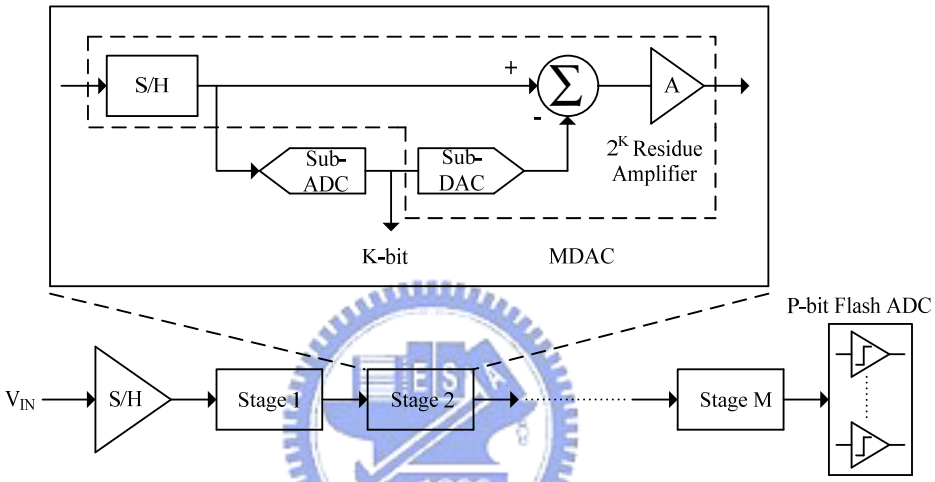


Figure 2.14 N-bit Pipelined ADC with multi-stage

Figure 2.14 consists of a cascade of M low-resolution stages and the operation of each stage generating K-bit output codes is similar to the Two-Step ADC. The last Pipelined stage is followed by a Flash ADC providing P-bit. The input signal is first sampled by the front-end S/H circuit and then the held output is fed to stage 1. For the subsequent stages, their input signal is the amplified output residue from the previous stage and it repeats the same of above operations until all stages have executed completely. The S/H circuit in each stage allows each of the stages to operate concurrently; that is, at any time, in odd or even stages of the Pipelined ADC begin processing a new sample as soon as its residue is sampled by the following stage. Thus, the throughput rate is independent of the number of stages in the Pipelined

ADC. On the contrary, the conversion time for any given sample is proportional to the number of stages. This is because the signal must work its way through all of the stages before the complete output word is generated; that is, the total N-bit (M*K+P) digital code is finally obtained by adding the output code of each stage during some period of latency. Another feature of the Pipelined ADC is that the requirements of comparators in each stage can be relaxed by using inter-stage gain amplifiers and digital error correction. If the requirement of resolution is increased, the circuit complexity grows approximately linear compared with exponential growth in Flash and Two-Step ADCs. Furthermore, the effect of the mismatches being a limitation to resolution can be eliminated by calibration techniques. Therefore, the architecture of Pipelined ADC has good compromise between resolution and speed.

2.3.4 Key Circuit Components of Pipelined ADC

The block diagram of a typical Pipelined ADC has been shown in Figure 2.14. In this architecture, the core of circuit components is the operational amplifier (Op-amp). The front-end S/H mainly composed of the op-amp relaxes the timing requirements of next stage, which can accurately sample high- frequency input signals. The inter-stage gains from these amplifiers diminish the effects of non-idealities in all stages following the first stage. Because the accuracy requirement will lessen stage by stage, the dependency of accuracy on the most significant stage is stringent, even though a slight error in the first stage will propagate through the converter and result in a much larger error at the end of the conversion; that is, the op-amps in the first several stages primarily dominate the accuracy and the conversion speed of the Pipelined ADC. Besides, the S/H and MDAC circuits which equally require the components such as comparators, switches, or passive devices like capacitors also dominate the speed and

accuracy of the whole ADC.

2.4 Summary

The basic concepts of the analog-to-digital conversion and the performance metrics characterizing ADCs were introduced in this chapter. Then, three types of high speed ADC architectures were described explicitly and the Pipelined ADC was chosen in summary for better compromise among resolution, speed, chip area and power consumption than other ADCs. In general, the multi-bit /stage and multi-stage architecture can reduce non-ideal effects from the back-end Pipelined stages by deciding more bits in the front-end stages, but the stage gain amplifiers are the primary source of power consumption and the significant limitation to signal processing speed.

Chapter 3

System Analysis of The Pipelined Analog-to-Digital Converter

3.1 Introduction

In this chapter, we will concentrate more detail on the Pipelined ADC. The basic principle including mathematical description and circuit structure are described. As mentioned earlier, the Pipelined ADC has the capability of tolerance to comparator offset due to the digital error correction, and the redundancy algorithm of 1.5-bit/stage structure is introduced as well. We also build the behavior model to analyze the characteristics of the Pipelined ADC. Furthermore, error sources which are classified into two causes of offset and non-linearity in each section of the Pipelined ADC are pointed out, where the capacitor-mismatch effect belonging to the non-linear error is avoidless and causes the most damage to the accuracy of Pipelined ADC. Therefore, a linearity-improving technique of capacitor-mismatch calibration is proposed to enhance the accuracy of the capacitor-ratio, reducing the distortion due to non-linearity effects.

3.2 Signal Processing of the Pipelined Stage

A prototype of Pipelined ADC introduced in section 2.3.3 consists of M similar cascaded stages and each stage resolves K bits. To develop a general view, we first concern a single stage. Figure 3.1(a) shows a conversion stage representing the i-th stage and it consists of an S/H circuit, a sub-ADC, a sub-DAC and a residue amplifier.

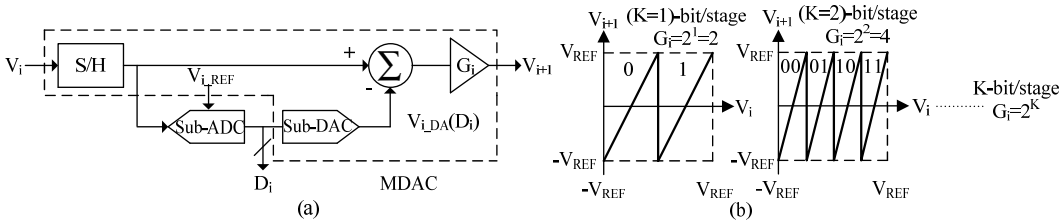


Figure 3.1 (a) A single K-bit Pipelined stage (b) V_i to V_{i+1} residue plot

The analog input V_i is sampled and is compared with the reference voltages V_{i_REF} of the Sub-ADC, then a rough digital code D_i representing input level presents. The sub-ADC with Y comparators generates Y+1 possible codes and it is followed by a reconstructing sub-DAC, which recovers code D_i to a level of analog value V_{i_DA}. The analog level of V_{i_DA} depending on the value of D_i can be one of (Y+1) possible voltages and is then subtracted from the sampled input value V_i. That is, the (Y+1) possible digital words for D_i are the function of V_i and can be represented as integers: 0 for (00..0), 1 for (00..1),……up to Y for (11..1) [19]:

$$D_i = \begin{cases} 0, \ for \quad V_i < V_{i\_REF}[0]_i \\ 1, \ for \quad V_{i\_REF}[0] \le V_i < V_{i\_REF}[1] \\ . \\ . \\ Y, \ for \quad V_{i\_REF}[Y-1] < V_i \end{cases} \tag{3.1}$$

The residue signal (V_i-$V_{i\_DA}(D_i)$) is then amplified by the residue amplifier with a gain of G_i and the output is noted as V_{i+1}:

$$V_{i+1} = G_i \times [V_i - V_{i\_DA}(D_i)] \tag{3.2}$$

This amplification enables the residue signal to recover the full-scale range for next stage conversion. Furthermore, inverting of (3.2) gives V_i as the function of V_{i+1}:

$$V_i = V_{i\_DA}(D_i) + \frac{V_{i+1}}{G_i} \tag{3.3}$$

Thus, the input signal of stage_i can then be expressed as

$$V_i = V_{i\_DA}(D_i) + \frac{V_{(i+1)\_DA}(D_{i+1})}{G_i} + \frac{V_{i+2}}{G_i G_{i+1}} \qquad (3.4)$$

Assuming there are total P stages, then (3.4) can be expanded to

$$V_i = V_{i\_DA}(D_i) + \frac{V_{(i+1)\_DA}(D_{i+1})}{G_i} + \frac{V_{(i+2)\_DA}(D_{i+2})}{G_i G_{i+1}} + \cdots\cdots + \frac{V_{P\_DA}(D_P)}{G_i G_{i+1} \cdots G_{P-1}} + Q \qquad (3.5)$$

, where $Q=V_{P+1}/(G_iG_{i+1}\ldots G_P)$ represents the quantization error and it degrades as the number of converter stages (P) or the gain of the inter-stage amplifiers (G_i) increase.

Figure 3.1(b) illustrates how the residue value of each stage generates in the corresponding input range and the slopes of transfer curves equal the gain of G_i. This residue plot implies that the input signal is folded after quantization and amplified 2^K for the same conversion range of the next stage. Figure 3.2 takes 4 stages with 1-bit/stage architecture for example and it is similar for the K-bit/stage utilization.

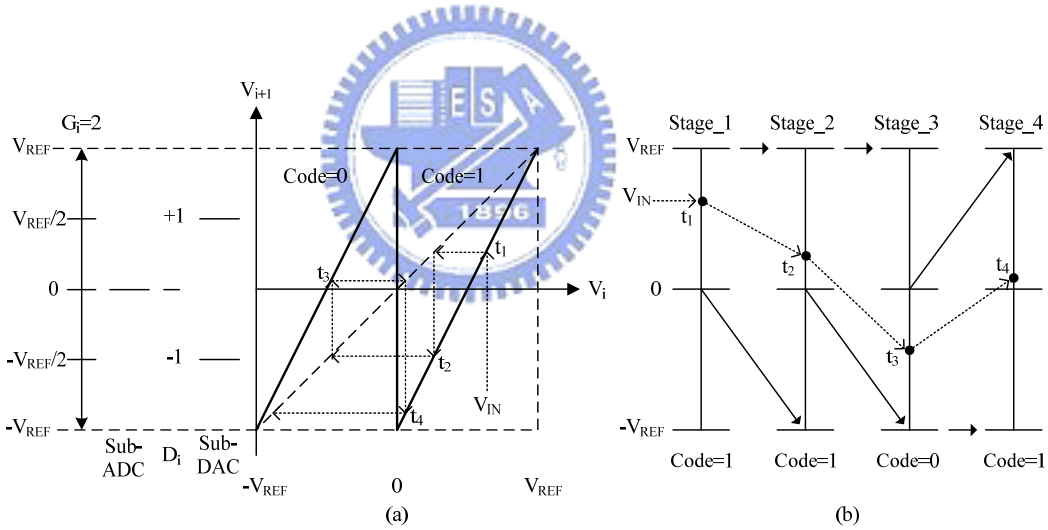


Figure 3.2 The 1-bit/stage example (a) transfer curve (b) trace diagram

First, the sampled signal V_{IN} of stage_1 is located at node t_1 in Figure 3.2(a), and the y-axis value of t_1 is known as the output of stage_1, which is also the input of stage_2. Furthermore, the node t_2 to t_4 can be observed in the same principle recursively. When the input of each stage is larger than reference of 0, the resolved output code is 1; on the other hand, the resolved output code is 0. The trace diagram

of Figure 3.2(b) shows the signal processing stage by stage. The scale-up action for the residue signal can answer the conversion of next stage and can reduce the required number of reference voltages [20]. After the scale-up, the subtraction is required to prevent the scaling signal from exceeding the maximum range of references, which would cause the miss of decision levels. Generally, the transfer function corresponding to different input range of each stage can be expressed as

$$V_{OUT} = 2^k \cdot V_{IN} - D \cdot V_{REF} \tag{3.6}$$

, where D = 0 or 1 depends on the input range in this 1-bit/stage example; if k equals 4, then D = 0 or 1,…, or 15. Note that the Sub_DAC executes the amplification and the subtraction described in (3.6). Therefore, a circuit combining functions of the D/A, the subtraction, and the amplification is called the Multiplying-DAC (MDAC) and will be discussed in detail later.

The Pipelined ADC mainly operates in two phase of non-overlapping clock for conversion. One of two phase is operated for sampling the input signal, and the other is employed for holding and amplifying the residue voltage at the output. MDACs of consecutive stages operate concurrently in opposite phase to obtain high throughput rate, as illustrated in Figure 3.3.

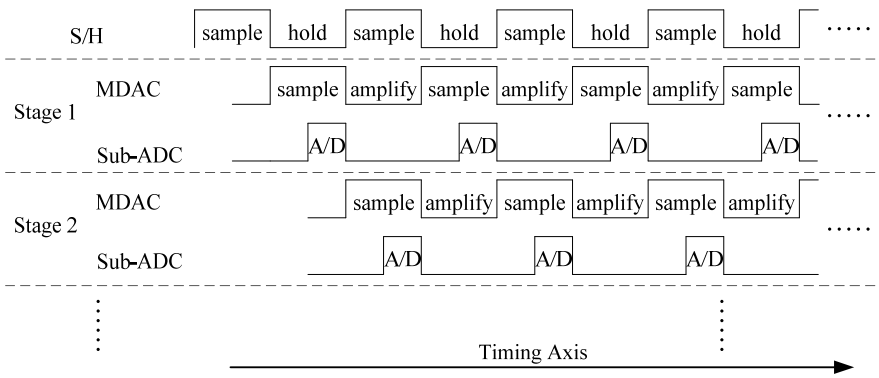


Figure 3.3 Timing analysis of Pipelined ADC

The A/D phase shown at the latter half of sampling cycle is for the quantization of the Sub-ADC in each stage, and the quantized code of each stage is produced at different time. For a complete prototype of M-stage Pipelined ADC where the last stage only consists of comparators is shown in Figure 3.4. Since the K-bit codes resolved from each stage are not simultaneous, output buffers with different delay for each stage are required to synchronously merge K-bit/stage into a complete N-bit word at the ADC output. If there are more stages, the latency period before completely merging K-bit digital codes from different stages is longer. Therefore, the Pipelined ADC may be inappropriate for applications where the larger latency is not tolerated. Finally, the logic for digital error correction is usually employed to relax the requirements of each stage and it will be introduced explicitly in the section of 3.4.

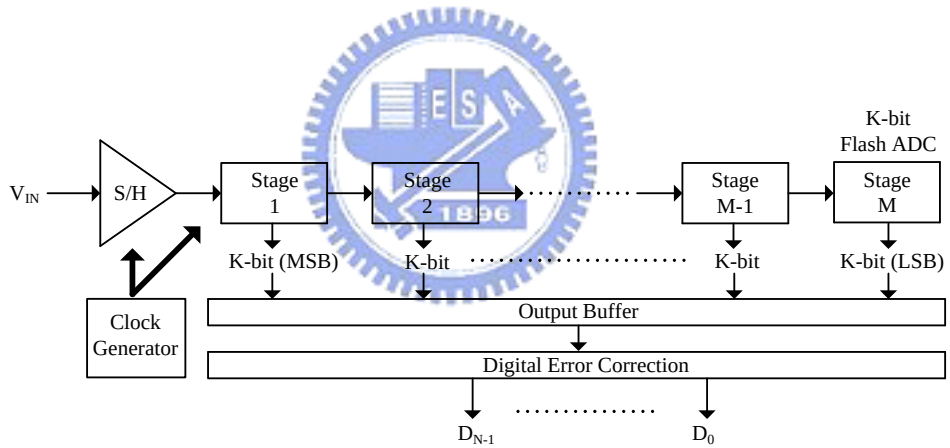


Figure 3.4 M-stage Pipelined ADC with K-bit/stage architecture

3.3 Error Sources Consideration in One Stage

T he 2-bit/stage residue transfer curve and conversion characteristic of the Pipelined ADC are shown in Figure 3.5. Ideally, the transition voltages are located at $-1/2V_{REF}$, 0, and $1/2V_{REF}$, where $2V_{REF}$ represents the full-range of the signal. The plot shown in Figure 3.5 is linear [21] without errors consideration, however, there

exists imperfections in actual circuit implementation.

The primary error sources in a Pipelined ADC are presented by the non-idealities of the Sub-ADC and Sub-DAC, as well as that of the S/H. These non-idealities limiting ADCs performance mainly include offset errors and gain errors in S/H circuits or residue amplifiers, the non-linearity of Sub-ADC and Sub-DAC, and op-amp settling-time errors.

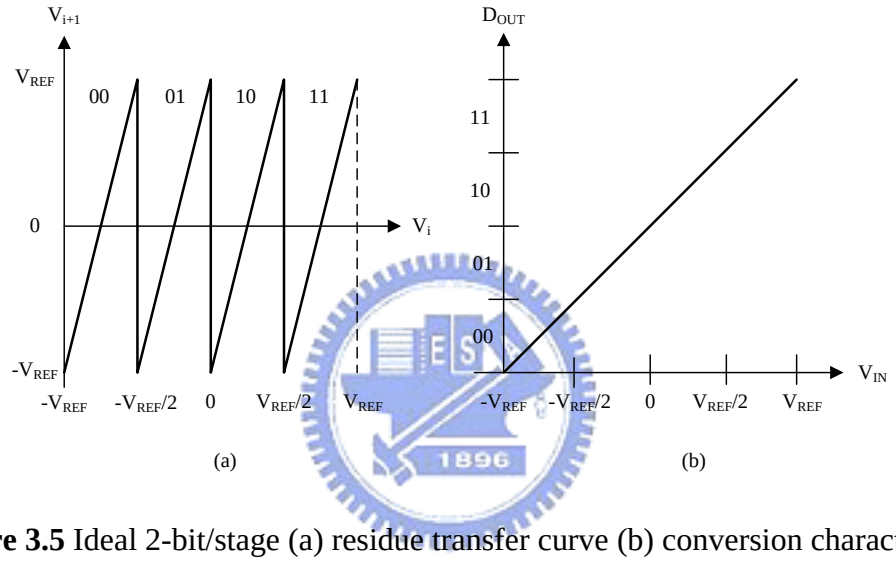


Figure 3.5 Ideal 2-bit/stage (a) residue transfer curve (b) conversion characteristic

3.3.1 Non-idealities in the Sub-ADC

The non-idealities in the Sub-ADC are mainly the comparators offsets, which leads to a decision-level shift of the Sub-ADC. When the close values of two inputs are compared, the comparators may make a wrong decision and a wrong reference voltage will be subtracted from the input if the offset errors exist, which result in the threshold level of the Sub-ADC to shift. For the 2-bit/stage example, this effect of threshold-level shift is shown in Figure 3.6 and can be tolerated to a certain extent by adopting digital error correction technique which will be discussed in detail later. The

offsets are sometimes caused by the residue amplifier and can reflect on the transfer function (3.2) as follows:

$$V_{i+1} = G_i \times [V_i - V_{i\_DA}(D_i) - V_{i\_os}] \quad => \quad V_i = V_{i\_DA}(D_i) + \frac{V_{i+1}}{G_i} + V_{i\_os} \tag{3.7}$$

The input V_1 of the first stage can be expressed as

$$V_1 = V_{1\_DA}(D_1) + \frac{V_{2\_DA}(D_2)}{G_1} + \frac{V_{3\_DA}(D_3)}{G_1 G_2} + \cdots\cdots + \frac{V_{P\_DA}(D_P)}{G_1 G_2 \cdots G_{P-1}} + Q + O \tag{3.8}$$

Therefore, the entire ADC system has a dc offset of

$$O = V_{1\_os} + \frac{V_{2\_os}}{G_1} + \frac{V_{3\_os}}{G_1 G_2} + \cdots\cdots + \frac{V_{P\_os}}{G_1 G_2 \cdots G_{P-1}} \tag{3.9}$$

Furthermore, the amplified residue must equal the conversion range of the next stage, and we can observe that if the deviation in the residue characteristic exceeds or is within the maximum output range, it separately results in missing decision level (i.e. wide code) and missing code, which can not be compensated by digital error correction. Besides, the transition magnitudes of residue transfer curve are constant in spite of offset errors with deviation.

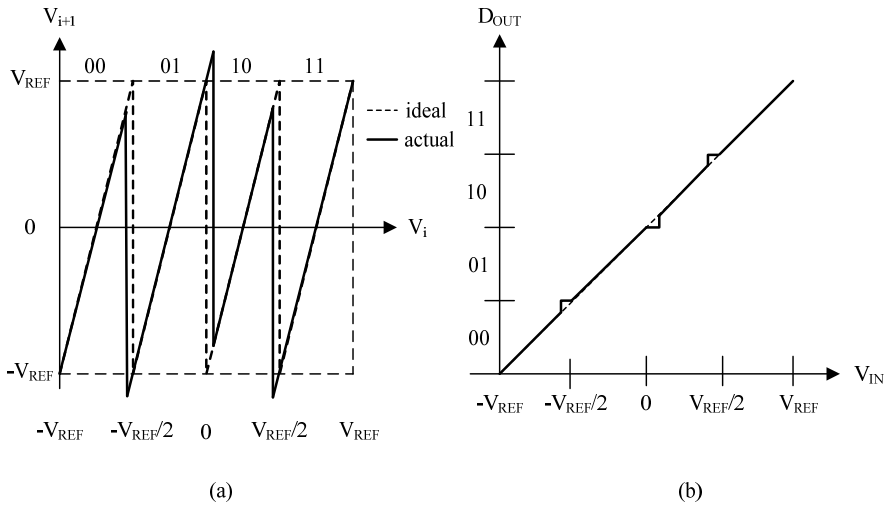


Figure 3.6 2-bit/stage with offsets (a) residue transfer curve (b) conversion characteristic

3.3.2 Non-idealities in the Sub-DAC

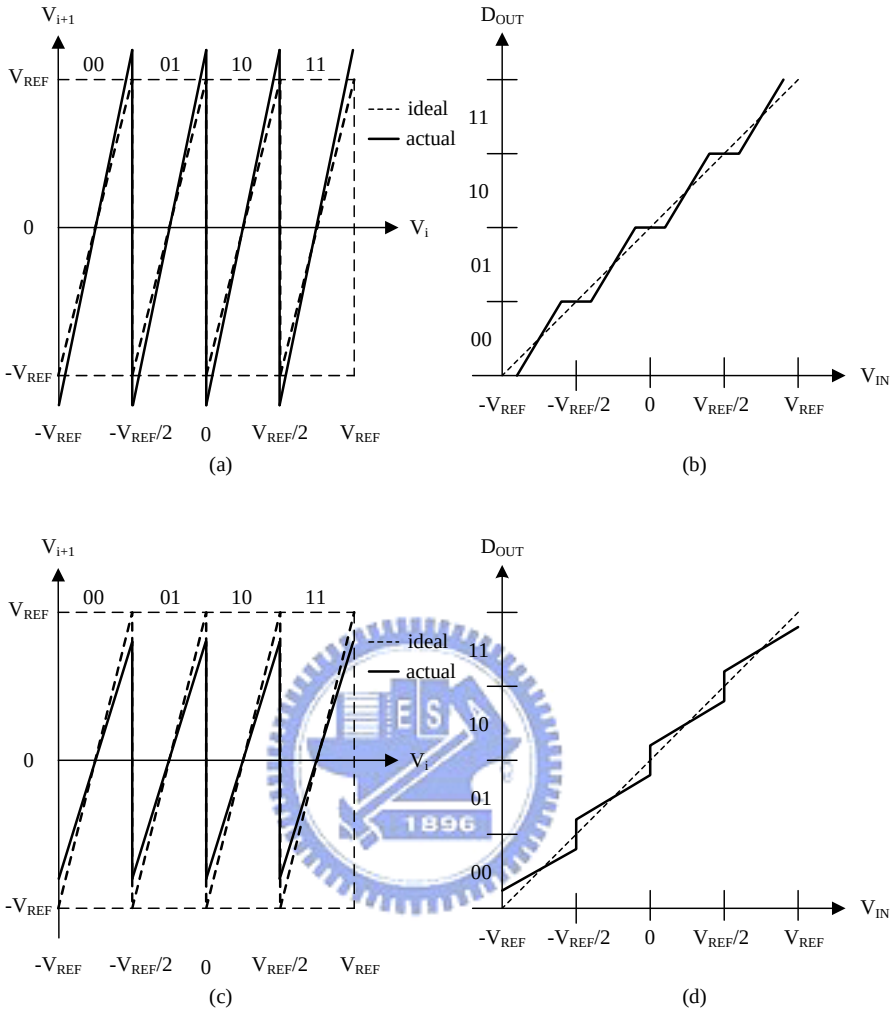


Figure 3.7 Residue transfer curve and conversion characteristic of 2-bit/stage with gain error (a) (b) larger and (c) (d) smaller than 4

The non-idealities in the Sub-DAC, which combines the functions of S/H, subtraction, and amplification, include offsets, gain error, and non-linearity. In the Pipelined ADC popularly using the switch-capacitor technique, these error sources are mainly from charge-injection, capacitor-mismatches, the finite op-amp gain and bandwidth. The offset errors of the Sub-DAC only contribute a constant offset value to the ADC. On the contrary, the gain error and the non-linearity of the Sub-DAC

determine the performance of linearity in the whole ADC. The gain errors in each stage result from two causes: one is the capacitor-mismatch between the sampling capacitors and the feedback capacitors in the MDAC, and the other is the limited DC gain of the operational amplifier. For a given plot of the Pipelined stage with gain error is shown in Figure 3.7, and we can observe that the gain errors in the residue transfer curve will cause the output range to be larger or smaller than the conversion range of the following stage. As a result, wide codes and missing codes occur separately.

The non-linearity of the Sub-DAC produce differences in the transition magnitudes of residue transfer curve and is the most stringent issue for the Pipelined ADC. It involves various parts of non-linearity factors in MDACs and can be seen in Figure 3.8. This effect results in both wide code and missing code, which make the conversion characteristic as a zigzag line. To overcome these non-linearity errors, various analog or digital calibration techniques [22][23][24][25][26] are employed to improve the linearity of the conversion characteristic.

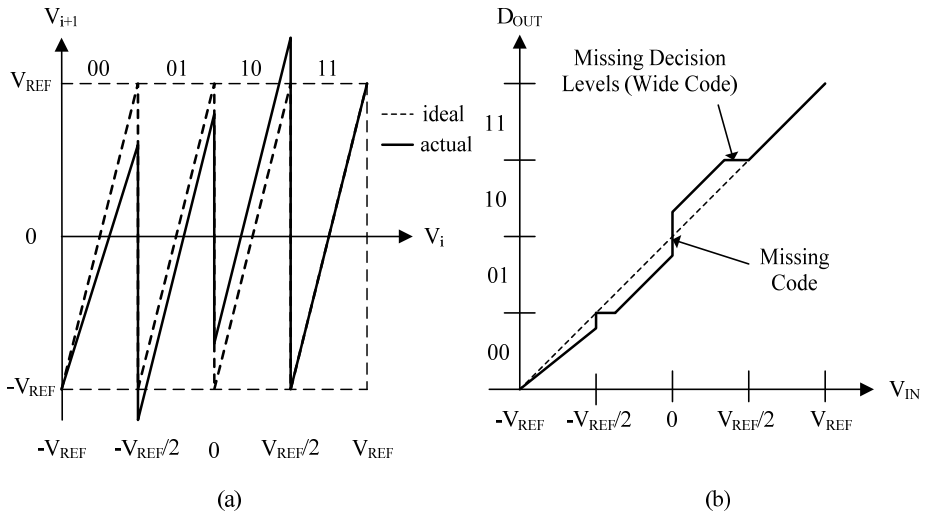


Figure 3.8 2-bit/stage with non-linearity in MDAC (a) residue transfer curve (b) conversion characteristic

3.4 Digital Error Correction with Stages Redundancy

We can realize that the Pipelined ADC is highly sensitive to non-idealities of threshold offsets, gain errors, and the non-linearity discussed in last section. To build the Pipelined ADC with a large tolerance to components non-idealities, the redundancy of stages is introduced in this section by making the sum of the individual stage resolution greater than the total resolution. When the redundancy is removed by digital error correction algorithm, it can be adopted to eliminate the effects of the Sub-ADC non-linearity and inter-stage offsets on the overall linearity.

In many previous implementations adopting digital error correction algorithm do both addition and subtraction to correct errors. Since subtraction is equivalent to addition with negative offsets, the required correction logic can be simplified through the introduction of offsets that reduce the requirement for the correction logic doing subtraction. As mentioned in section 3.2, the comparator offset and stage-gain error may cause the residue to exceed the conversion range of the next stage, even more out of range in subsequent stages, and thus determine wrong output codes [27]. In order to solve this over-range problem, we can increase the input range of each stage beyond the normal output range of the previous stage or reduce the inter-stage gain respect to the original design [28]. Two approaches of digital error correction algorithms mentioned above are shown in Figure 3.9.

The residue transfer curve of approach A implies that there are two extra comparators comparing in two input ranges of top and bottom; that is, the input range can be increased by designing the number of comparators $Y>G_i-1$, where $Y=G_i-1$ in normal design. This approach can be verified to have an over-range capability of $\pm 2V_{REF}/G_i$, which means the tolerable range of comparator offset.

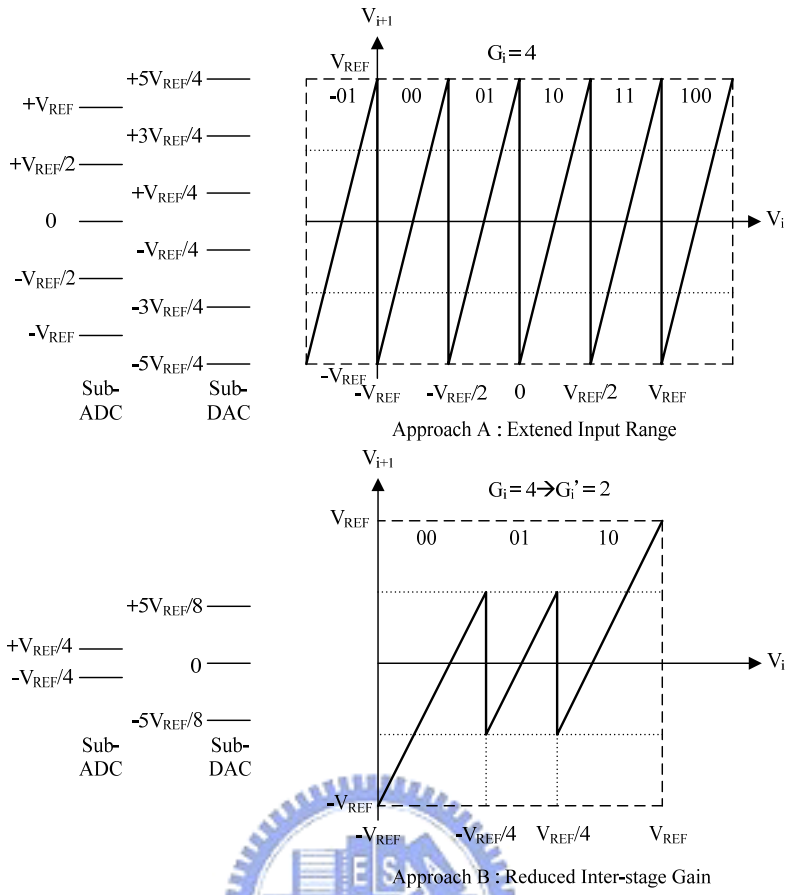


Figure 3.9 Two types of digital error correction for 2-bit/stage

Approach B reduces the inter-stage gain and adopts one redundant comparator instead of the normal design. In this case, $Y=G_i-2$, and this approach is like a redundant signed digit (RSD) algorithm [16][17][18] as well as the architecture of K.5-bit/stage, where K=1, 2, 3….etc. Furthermore, approach B can be verified to have an over-range capability of $\pm 2V_{REF}/2G_i$.

As a summary, the reduced inter-stage gain algorithm is adopted in this thesis for the reason of fewer comparators, which consume less power and area, as well as the reason for high speed requirement.

To illustrate the digital error correction of approach B in more detail, we take a 2-bit/stage for example and Figure 3.10 shows the block diagram.

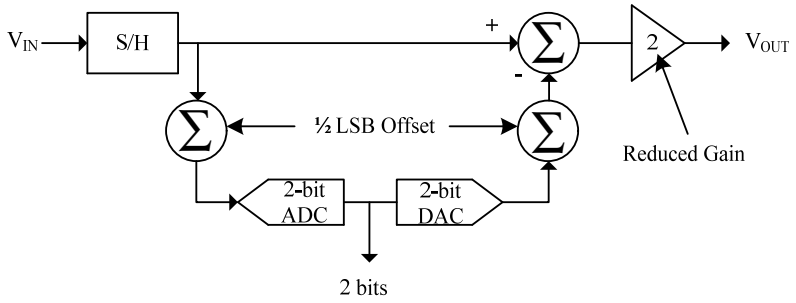


Figure 3.10 Block diagram of one stage with offset in ADC and DAC

First, when the inter-stage gain is reduced to 2, the residue transfer plot is compressed between the output range of $1/2V_{REF}$ and $-1/2V_{REF}$, as shown in Figure 3.11(a). Even if the comparator offset shown in Figure 3.11(b) occurs, the residue output range is still within V_{REF} and $-V_{REF}$, and then the following stage will correct the output codes by addition or subtraction operation.

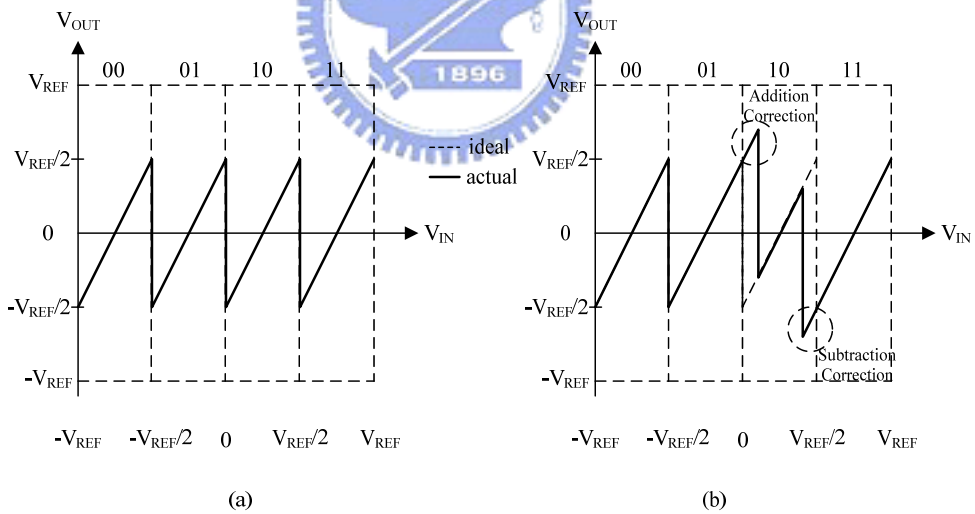


Figure 3.11 Residue plot with inter-stage gain of 2 (a) without offsets (b) with offsets

Second, since subtraction is equivalent to addition with offset, we can intentionally model a maximum offset of 1/2 LSB ($V_{REF}/4$) to both Sub-ADC and Sub-DAC. This adding offset uniformly shifts the location of the decision levels to the

right by 1/2 LSB, which is shown in Figure 3.12.

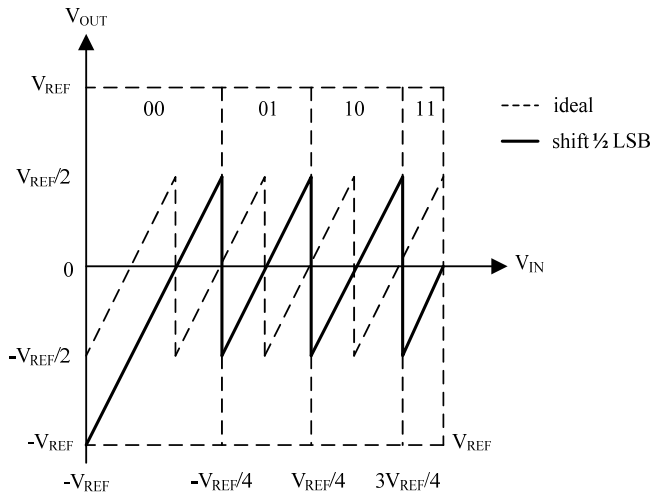


Figure 3.12 Ideal residue with 1/2 LSB offset

Let the correction range to be defined as the amount of decision-level movement that can be tolerated without error. If the DAC and S/H are ideal and the inter-stage gain is 2, the amplified residue of Figure 3.12 remains within the conversion range of the next stage when the Sub-ADC offsets shift the decision levels by no more than ± 1/2 LSB. Under these conditions, errors caused by the Sub-ADC can be corrected; therefore, the correction range here is ±1/2 LSB (or $V_{REF}/4$) at a 2-bit level. Furthermore, because the offset introduced in Figure 3.10 shifts the decision levels to the right by the amount of the offset, the digital output is always less than or equal to its ideal value if the Sub-ADC offsets shift the decision levels back to the left by no more than this amount. Thus, the correction only requires the function of addition or no change.

Because errors caused by the Sub-ADC offsets between ±1/2 LSB can be corrected as described above and the top-most decision level is 1/2 LSB below the maximum stage input. We can observe from Figure 3.12 that the top-most comparator

in each stage except the last stage is not required and can be removed. Figure 3.13 shows the new residue plot.

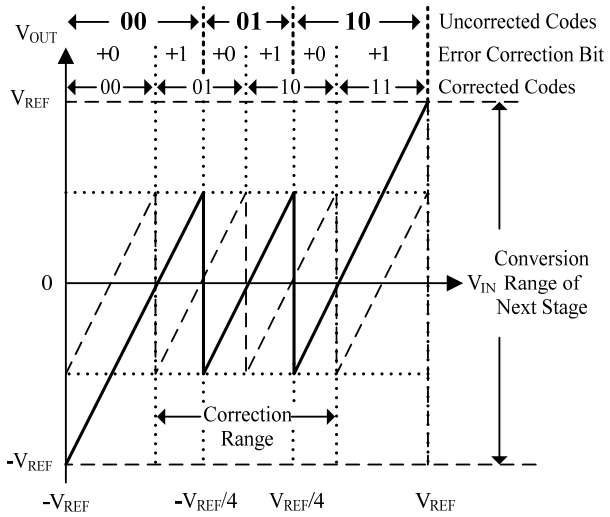


Figure 3.13 New residue without the top-most comparator

However, removal of the top-most comparator does not change the correction range because the decision levels in Figure 3.13 still can be shifted by ±1/2 LSB before producing residues which meet the next stage. Therefore, only two comparators are required in each stage except the last stage and the digital output code $(11)_2$ is eliminated, which can be recovered by the digital error correction of the next stage. The above description means that this resolution/stage is actually about 1.5 bits. Furthermore, the minimum residue in Figure 3.13 occurs on the left end of the plot and rests on the lower conversion-range boundary of the next stage. In Figure 3.13, the corrected output codes is obtained by overlapping one bit between neighboring stages to correct the overhanging section from the previous stage; that is, one of the three possible uncorrected codes $(00)_2$, $(01)_2$, $(10)_2$ is corrected by one redundant bit of adjacent stages if comparators offsets do not exceed $\pm V_{REF}/4$. Figure 3.14 shows an example that even if the offset occurs at the stage_3, the digital error correction

still makes the final result as the ideal case.

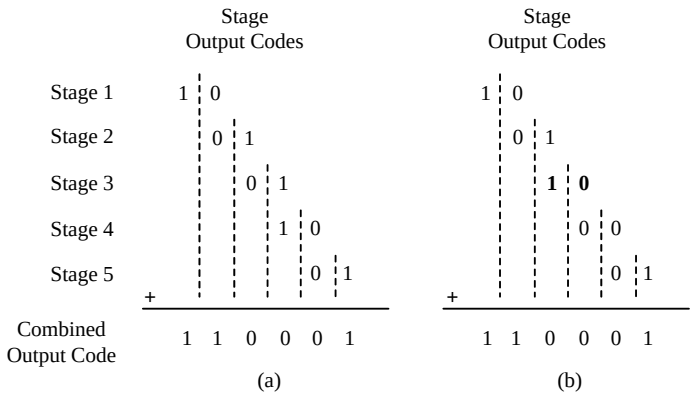


Figure 3.14 RSD correction in digital domain (a) ideal case (b) offset within $\pm V_{REF}/4$

As a summary, with the digital error correction in the 1.5-bit/stage architecture, the most benefit is that the Pipelined ADC has a large tolerance of the comparator offset. Furthermore, because there is no decision level at half-scale in Figure 3.13, a multi-stage ADC adopting stages with this transfer characteristic will inherently have excellent linearity at the half scale [29].

3.5 1.5-Bit/Stage Architecture

As we have known, the 1.5-bit/stage Pipelined architecture is characteristic for generating only three possible digital output codes, $(00)_2$, $(01)_2$, $(10)_2$, which correspond to the following transfer function.

$$V_{OUT} = \begin{cases} 2V_{IN} + V_{REF}, if\ -V_{REF} < V_{IN} < \dfrac{-V_{REF}}{4} \Leftrightarrow D = (00)_2 \\ 2V_{IN}\quad\quad , if\ \dfrac{-V_{REF}}{4} < V_{IN} < \dfrac{+V_{REF}}{4} \Leftrightarrow D = (01)_2 \\ 2V_{IN} - V_{REF}, if\ \dfrac{+V_{REF}}{4} < V_{IN} < +V_{REF} \Leftrightarrow D = (10)_2 \end{cases} \quad (3.10)$$

, where the Sub-ADC has the decision levels at $+V_{REF}/4$ and $-V_{REF}/4$ shown in Figure

3.13. The prototype of 10-bit Pipelined ADC with 1.5-bit/stage architecture is shown in Figure 3.15, which totally consists of 9 stages.

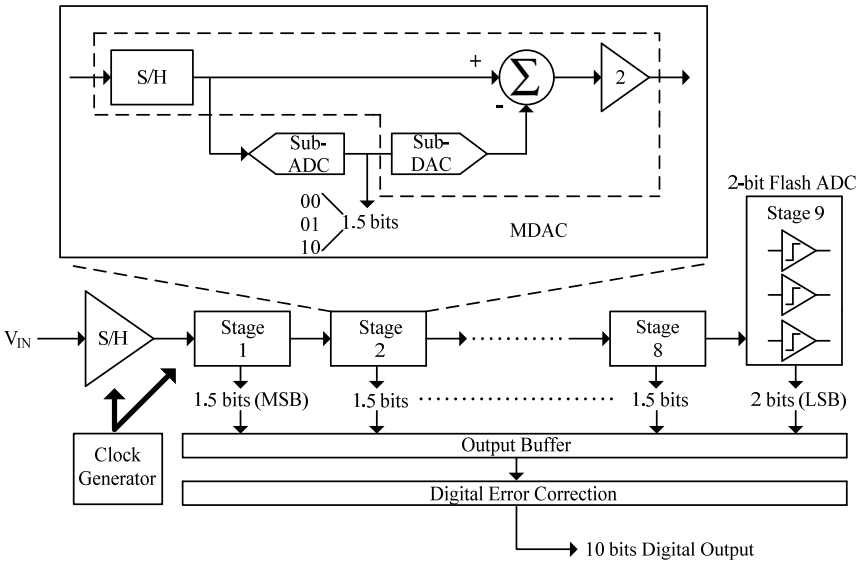


Figure 3.15 10-bit Pipelined ADC with 1.5-bit/stage architecture

The 1.5-bit/stage architecture is employed in the first 8 stages, and the last stage is only composed of a Flash quantizer. Each stage resolves 2 bits with a Sub-ADC and combines redundant bits by the RSD algorithm to yield a resolution of 10 bits.

For the implementation of a Pipelined stage, Figure 3.16 is illustrated to understand how the 1.5 bit/stage architecture works [30].

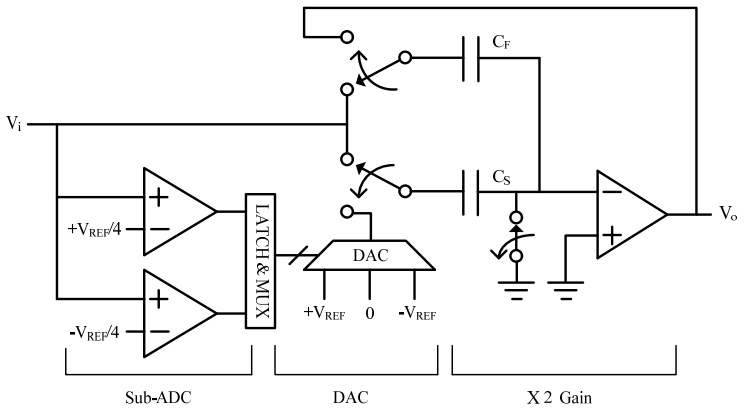


Figure 3.16 Switched-capacitor implementation of 1.5-bit stage

Although a single-ended is shown in Figure 3.16 for simplicity, the actual implementation is fully differential. A common, the switched-capacitor (SC) technique is chosen for implementation, which is operated by two-phase clock. During the first phase, the input signal V_i whose range is within $-V_{REF}$ to $+V_{REF}$ is applied to the input of the Sub-ADC which has thresholds at $+V_{REF}/4$ and $-V_{REF}/4$. Simultaneously, V_i is applied to sampling capacitors C_S and C_F. At the end of the first clock phase, V_i is sampled across C_S and C_F, and the output of the sub-ADC is latched. During the second clock phase, C_F closes a negative feedback loop around the op-amp, while the bottom plate of C_S is switched to the DAC output. This configuration generates the stage residue at V_o. The three possible outputs of the Sub-ADC are used to select the DAC output voltage V_{DAC} through an analog multiplexer, and V_{DAC} is capacitively subtracted from the residue such that

$$V_o = \begin{cases} (1+\frac{C_S}{C_F})V_i - \frac{C_S}{C_F}V_{REF} & \text{if } V_i > \frac{V_{REF}}{4} \\ (1+\frac{C_S}{C_F})V_i & \text{if } -\frac{V_{REF}}{4} < V_i < \frac{V_{REF}}{4} \\ (1+\frac{C_S}{C_F})V_i + \frac{C_S}{C_F}V_{REF} & \text{if } V_i < -\frac{V_{REF}}{4} \end{cases} \quad (3.11)$$

, where $C_S = C_F = C$ is chosen to give a gain of two in the transfer function.

The resolution per stage largely dominates the speed, power, and accuracy requirements of each stage in Pipelined ADC. In an SC circuit with the single-pole operational amplifier, the closed-loop bandwidth ***(BW)*** is given by

$$BW = Gm / C_L \times f \quad (3.12)$$

, where *Gm* is the transconductance of the op-amp, C_L is the output load capacitance, and *f* is the feedback factor. The feedback factor *f* of the *i*-th K-bit stage is defined as

$$f = C_i / (2^K \times C_i + C_{i\_op-amp}) \quad (3.13)$$

, where $C_{i\_op\text{-}amp}$ is the input capacitance of the op-amp. Therefore, the total output

load capacitance of the *i*-th stage is given by

$$C_L = (1-f)\times C_i + 2^K \times C_{i+1} + C_{i+1\_comp} \tag{3.14}$$

, where C_{i+1_comp} is the total input capacitance of the comparators in the next stage.

Based on equations described above, decreasing the resolution K of each stage is significant if the speed is a key design constraint; that is, lower resolution gives a larger feedback factor to maximize the bandwidth of the SC circuit, which limits overall conversion rate. Furthermore, for fewer numbers of bits per stage, which also imply smaller inter-stage gain, relax more accuracy requirements for comparators and op-amp in one stage. As a result, the low resolution of 1.5-bit per stage with digital error correction relaxes the constraints on comparators offsets and op-amp DC gain, which can be designed with fast settling time easily. Therefore, this architecture shows to be effective in achieving high throughput rate at low power consumption [18][31].

3.6 Behavior Model of Pipelined ADC

In order to get a further understanding of the Pipelined ADC, the behavior model of a 10-bit Pipelined ADC with the 1.5-bit/stage architecture is constructed by the Simulink in Matlab. The sample rate of the 10-bit Pipelined ADC is set at 100MHz.

For simplicity, the single-ended configuration is adopted. We first describe the mathematical characteristic of each circuit block, including S/H circuit, 1.5-bit Sub-ADC and MDAC for similar 8 stages, 2-bit Flash ADC of the last stage, and digital error correction, to understand how they operate. Besides the ideal mathematical analysis, each block is also added with some non-ideal properties [32].

3.6.1 S/H Circuit

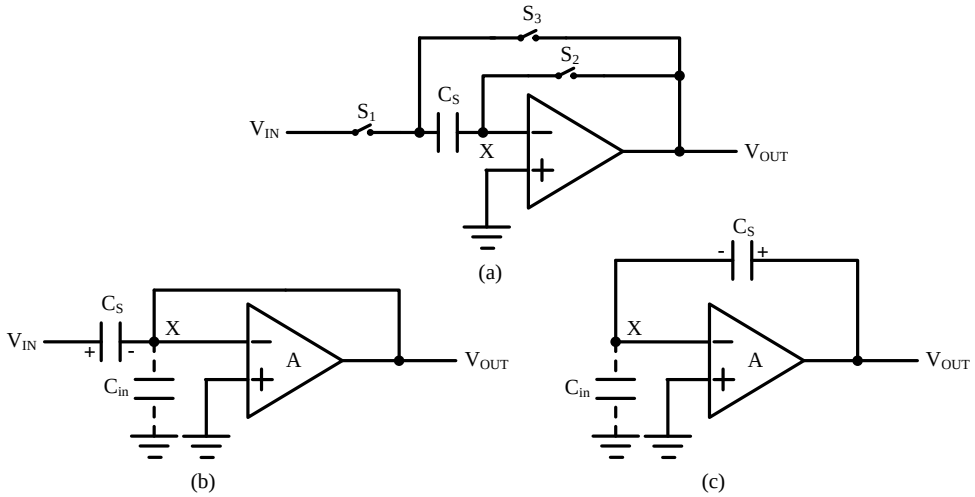


Figure 3.17 (a) Basic implementation of S/H (b) Sample mode of (a) (c) Hold mode of (a)

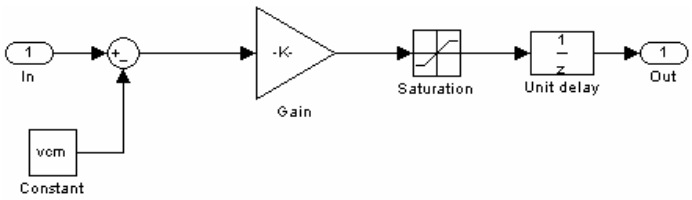
Figure 3.17(a) shows a basic implementation of unity-gain sampler which performs the functions of sample and hold, where C_S plays the roles of sampling and holding capacitor. In the sample mode showing in Figure 3.17(b), the switches of S_1 and S_2 are on, and S_3 is off, creating a virtual ground at node X and allowing the voltage across C_S to track the input voltage. In the hold mode showing in Figure 3.17(c), the switches of S_1 and S_2 are off, and S_3 is on, this makes the capacitor C_S feedback around the op-amp, and produces a unity-gain of V_{IN}. For precision considerations of how the output voltage is approximate the input voltage, we assume that the op-amp has a input capacitance C_{in} and $V_X \neq 0$ due to the finite op-amp gain of A. Therefore, the conservation of charge at node X after the hold mode can be calculated by

$$V_{OUT} - (C_S V_{IN} + C_{in} V_X) / C_S = V_X \qquad and \qquad V_X = -V_{OUT} / A \tag{3.15}$$

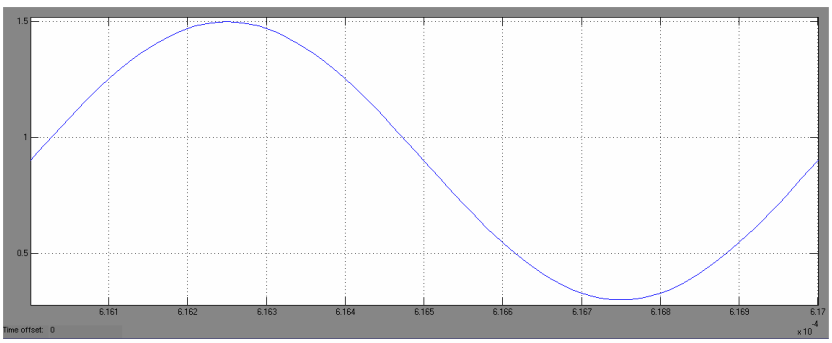
Thus, the mathematical description of the S/H circuit is expressed as

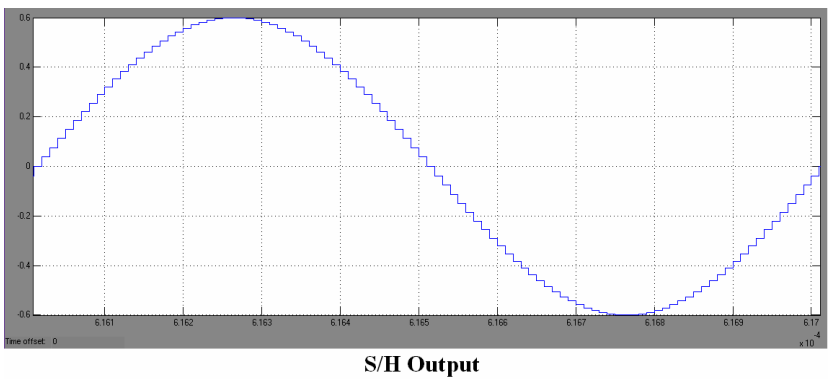
$$V_{OUT} = \frac{C_S}{C_S + \left(\frac{C_S + C_{in}}{A}\right)} V_{IN} Z^{-1} \tag{3.16}$$

The behavior model charactering S/H is constructed according to (3.16), and it is shown in Figure 3.18 including simulation result, where *vcm* represents the common mode voltage subtracted from the input. The actual *Gain* is $C_S/(C_S+(C_S+C_{in})/A)$ and Z^{-1} is used to delay the held output value.



(a)



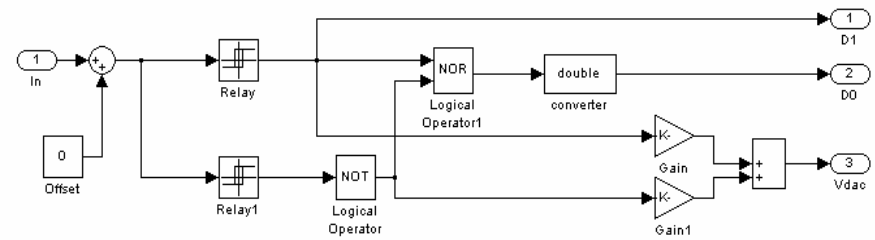


(b)

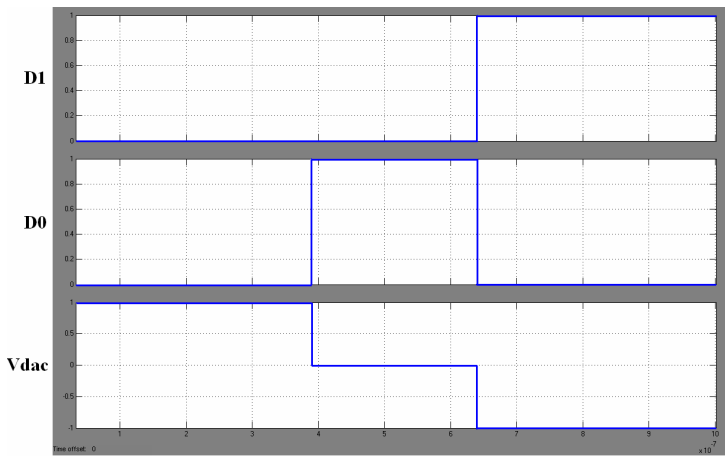
Figure 3.18 S/H with (a) behavior model (b) MATLAB simulation

3.6.2 1.5-bit Sub-ADC

Figure 3.19(a) shows the behavior model of the 1.5-bit Sub-ADC. It mainly consists of two comparators with ±1/4Vref threshold voltage. D_1 and D_0 are MSB and LSB generated from the Sub-ADC respectively. According to one of three possibilities of Sub-ADC output codes, the analog voltage V_{DAC} is generated to control the MDAC operation. The simulation result of Figure 3.19(b) shows the digital output codes of D_1 and D_0 which correspond to the V_{DAC} of V_{REF}, 0, and $-V_{REF}$ in different input ranges.



(a)



(b)

Figure 3.19 1.5-bit Sub-ADC with (a) behavior model (b) MATLAB simulation

3.6.3 Multiplying-DAC (MDAC)

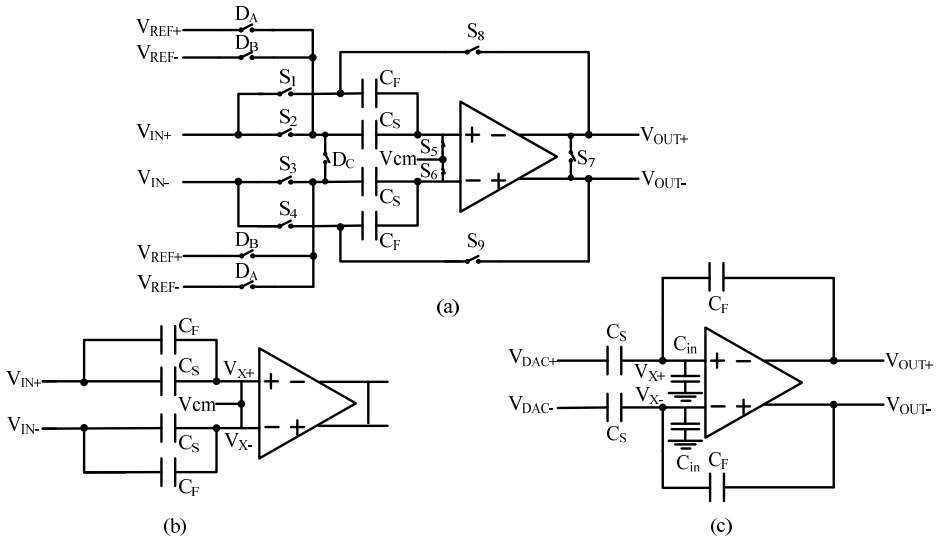


Figure 3.20 (a) Differential implementation of MDAC (b) Sample mode of (a) (c) Amplification mode of (a)

Figure 3.20(a) shows the conventional type of 1.5-bit/stage MDAC, and it is SC-implemented with differential mode. The MDAC in one stage is operated by two non-overlapping clock phase which are inversely with neighboring stages. When the front-end S/H holds the sampled input, MDAC samples its value simultaneously, as shown in Figure 3.20(b). In this phase, switches S_1~S_7 are on and the sampled charges Q on nodes X_+ and X_- are separately as

$$Q_{X+} = (V_{cm} - V_{IN+}) \cdot (C_S + C_F) \tag{3.17}$$

$$Q_{X-} = (V_{cm} - V_{IN-}) \cdot (C_S + C_F) \tag{3.18}$$

At the end of the sample mode, switches S_1~S_7 are off, S_8 and S_9 are on, which makes C_F feedback to the output. Furthermore, C_S is connected to a value of V_{DAC} determined by the output codes of Sub-ADC which also generates three sets of control codes (D_A, D_B, D_C) to control which switch on or off. Figure 3.20(c) shows

the amplification mode. During this phase, the op-amp is operated and we consider non-idealities of C_{in} as well as A like the S/H for precision design. The charges stored on nodes X_+ and X_- now can be expressed separately as

$$Q_{X+} = (V_{X+} - V_{DAC+}) \cdot C_S + (V_{X+} - V_{OUT+}) \cdot C_F + (V_{X+} \cdot C_{in}) \tag{3.19}$$

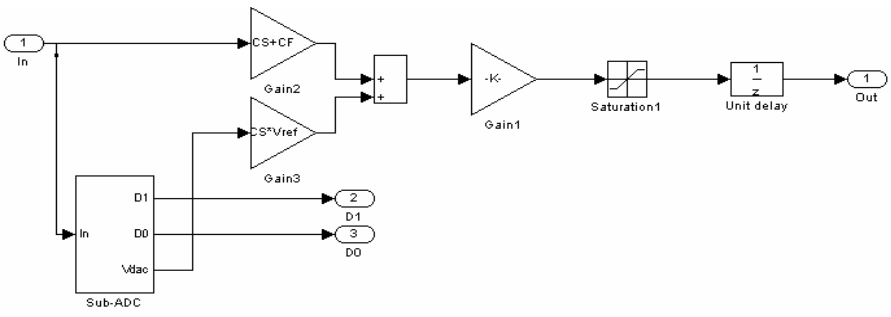
$$Q_{X-} = (V_{X-} - V_{DAC-}) \cdot C_S + (V_{X-} - V_{OUT-}) \cdot C_F + (V_{X-} \cdot C_{in}) \tag{3.20}$$

After the two phase of sample and amplification, charges at nodes X_+ and X_- are conserved, and we can combine (3.17) ~ (3.20) to get the mathematical description of the MDAC as

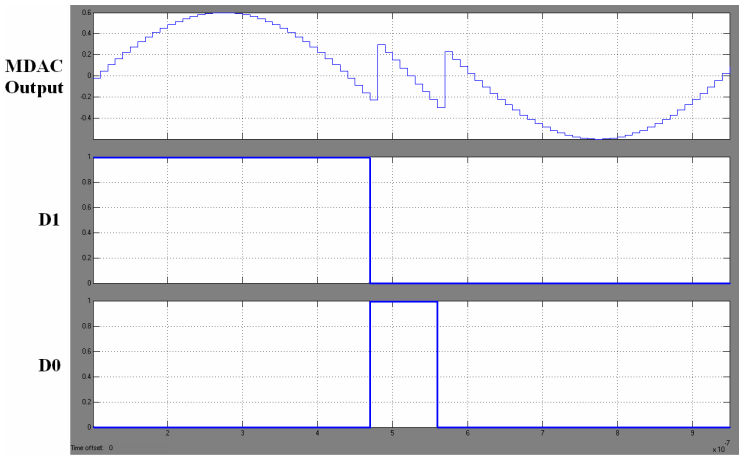
$$V_{OUT} = \frac{[(C_F + C_S) \cdot V_{IN} - C_S \cdot V_{DAC}]}{C_F + \left(\frac{C_S + C_F + C_{in}}{A} \right)} Z^{-1} \tag{3.21}$$

, where $V_{IN}=V_{IN+}-V_{IN-}$, $V_{OUT}=V_{OUT+}-V_{OUT-}$, $-V_{OUT}/A=V_{X+}-V_{X-}$, and $V_{DAC}=V_{DAC+}-V_{DAC-}$ are assumed, and V_{DAC} is mentioned in section 3.6.2.

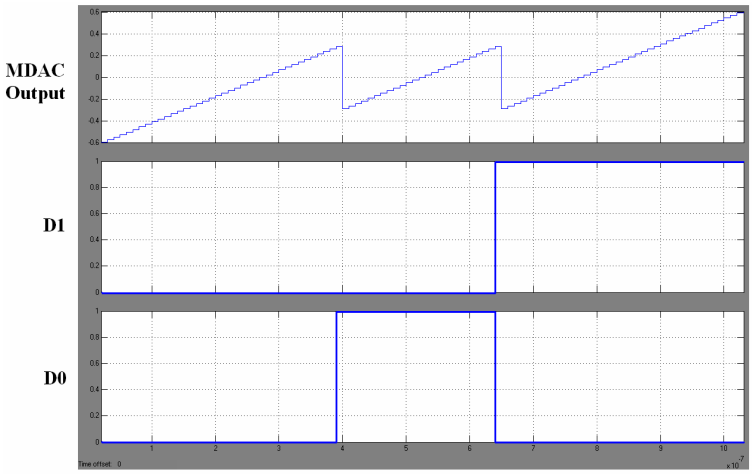
The MDAC according to Equation (3.21) is modeled and is combined with the Sub-ADC in Figure 3.21(a). Figure 3.21(b) and (c) shows the MATLAB simulation results of the output residue versus digital codes, which are respectively generated by the sinusoidal and ramp input.



(a)



(b)

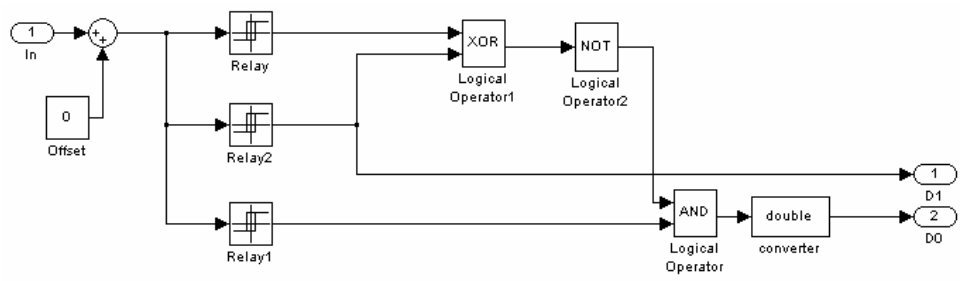


(c)

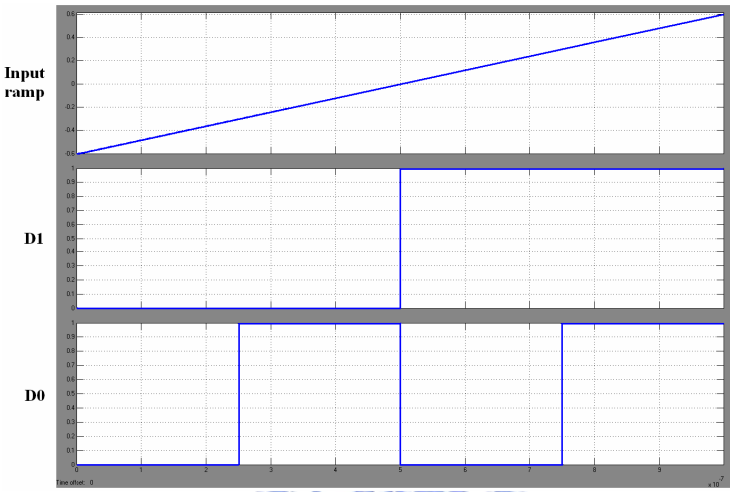
Figure 3.21 MDAC with (a) behavior model (b) MATLAB simulation with sine input (c) MATLAB simulation with ramp input

3.6.4 2-bit Flash

The final stage of the 10-bit Pipelined ADC is a classical 2-bit Flash, which does not require the digital error correction and only consists of three comparators with threshold values of $-V_{REF}/2$, 0, and $V_{REF}/2$ respectively. Figure 3.22(a) shows the behavior model of 2-bit Flash ADC, and Figure 3.22(b) illustrates the digital output codes of the MSB and LSB corresponding to the different input ranges.



(a)



(b)

Figure 3.22 2-bit Flash ADC with (a) behavior model (b) MATLAB simulation

3.6.5 Digital Error Correction Logic

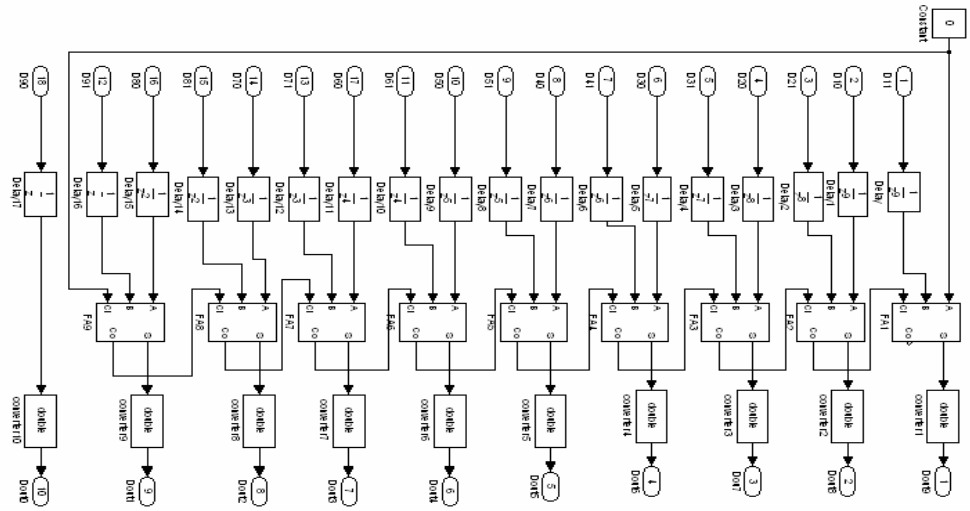


Figure 3.23 Behavior model of digital error correction

The digital circuits in Pipelined ADC include D-type latches for synchronization of digital codes and full-adders for digital error correction. Figure 3.23 is the model of digital circuits.

The correction is executed by 9 adders, which begin to add the MSB of the last stage with the LSB of the 8-th stage, and then propagate the carry-out of each stage in the direction of the MSB in the first stage. With 9 stages in this model, total 18 bits are generated and then combined to yield a resolution of 10-bit (Dout9~Dout0) at the ADC output.

3.6.6 Ideal 10-bit Pipelined ADC

Figure 3.24 shows the behavior model of the complete 10-bit Pipelined ADC, which is ideally made up of a front-end S/H, 8 identical stages, a last stage of 2-bit Flash ADC, and digital error correction logics.

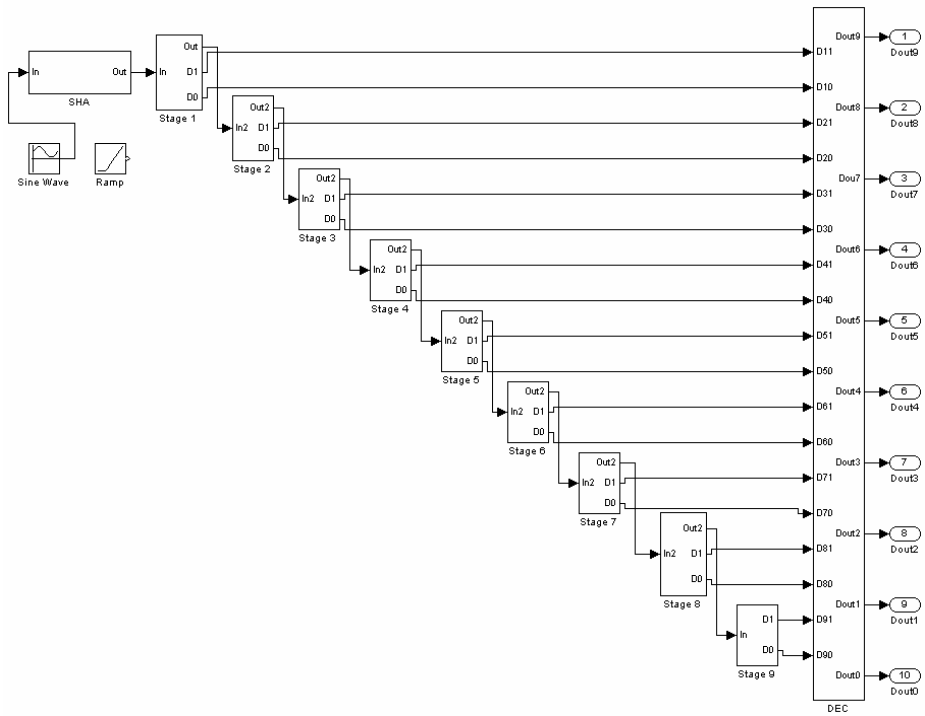
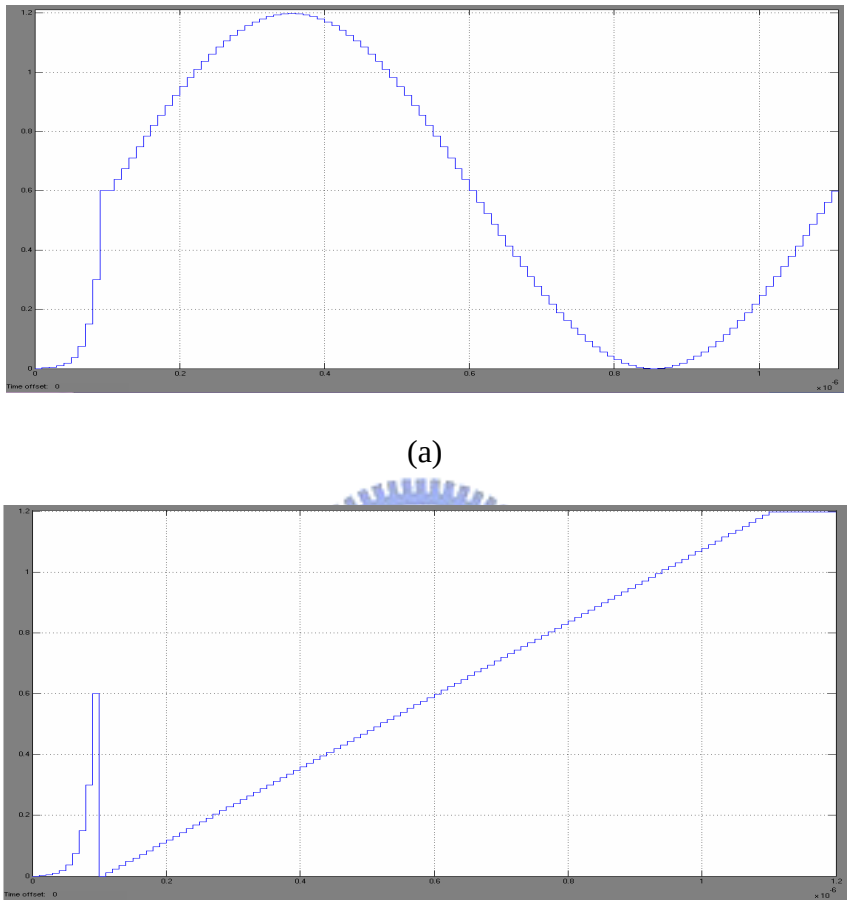


Figure 3.24 Behavior model of ideal 10-bit Pipelined ADC

The 10-bit digital output can be transformed into the analog result of binary weighting by an ideal DAC model. Figure 3.25 shows the time-domain reconstructed signals, which are separately generated by the sinusoidal and ramp input.

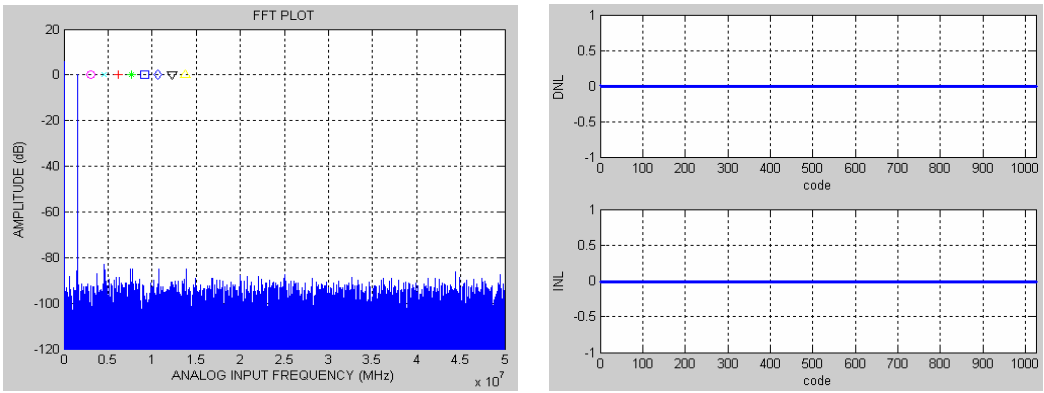


(a)

(b)

Figure 3.25 The reconstructed waveform of (a) sine wave (b) ramp

The linearity of the ADC is mainly determined by FFT spectrum, DNL, and INL. Because there are no non-ideal effects in this behavior model, the frequency-domain plot shown in Figure 3.26(a) has the SFDR of 82.36dB and SNDR of 62.13 with 1.5MHz sinusoidal input. Both DNL and INL are almost 0LSB, which show good linearity in Figure 3.26(b).



(a) (b)

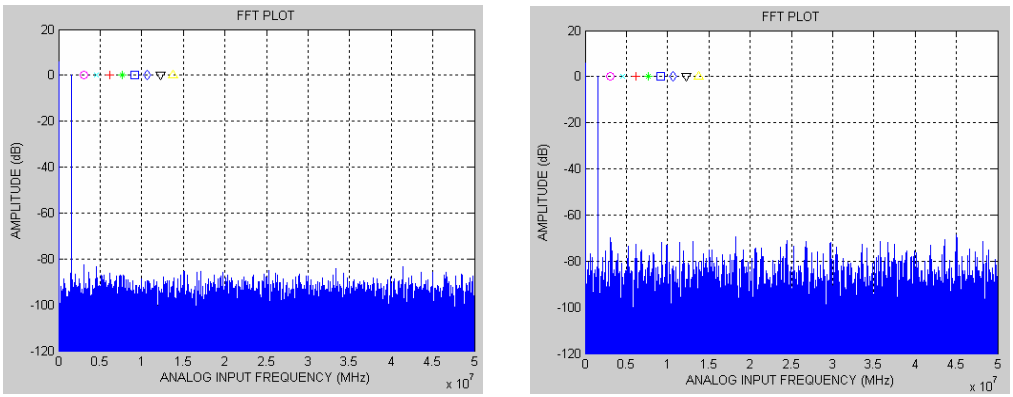
Figure 3.26 Ideal Pipelined ADC model with (a) FFT spectrum (b) DNL and INL versus code

3.6.7 Non-ideal Effects in Behavior Models

In the ideal case, the complete behavior model of Pipelined ADC is without any non-ideal factors. Nevertheless, there are non-ideal errors of offset and non-linearity in the actual circuit design, which are mainly caused by comparator offsets, finite op-amp gain, and mismatch of capacitors.

3.6.7.1 Comparator Offset Effect

The offsets of comparators result from devices mismatch and the charge injection of switches. The simulated FFT spectrum of Figure 3.27(a) illustrates that an offset is modeled in the Sub-ADC, which equals $0.2V_{REF}$ and is less than $V_{REF}/4$.; while the offset modeled in Figure 3.27(b) is $0.4V_{REF}$, which is beyond $V_{REF}/4$ and can not be corrected by digital error correction.

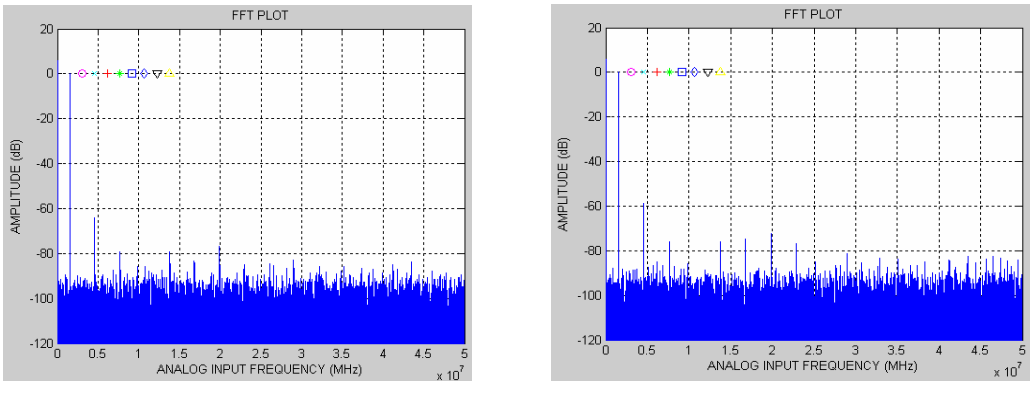


(a) (b)

Figure 3.27 FFT spectrum with an offset effect of (a) $0.2V_{REF}$ (b) $0.4\ V_{REF}$

3.6.7.2 Finite Op-amp Gain Effect

The gain of op-amp in the Pipelined stage must be large enough to prevent the non-linear effect. In the ideal ADC behavior model discussed before, we assume DC gain of 80dB for the op-amps, which is enough for a total 10-bit resolution. Figure 3.28 shows the influence of the finite op-amp gain effect, where the odd harmonic is larger when the gain is smaller.

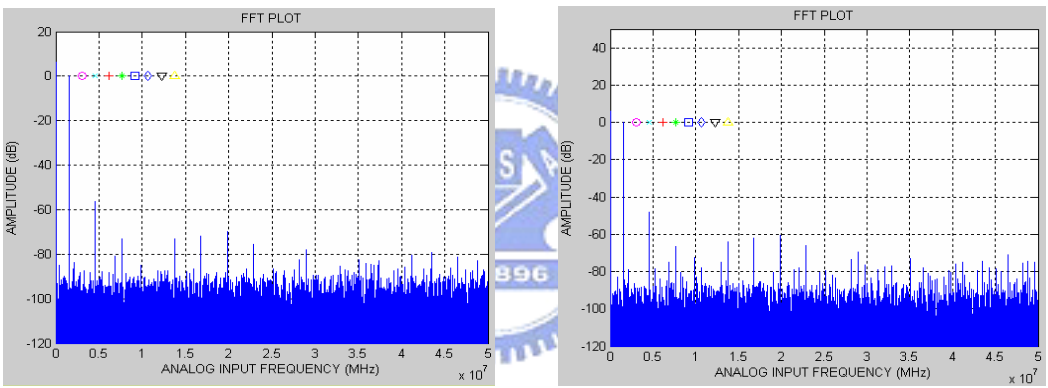


(a) (b)

Figure 3.28 Finite op-amp gain effects of (a) 60dB (b) 54dB

3.6.7.3 Capacitor-Mismatch Effect

The accuracy in one stage is mostly determined by the match of capacitors. For the output residue of MDAC circuits, the amplified gain is related to the capacitor ratio ($1+C_S/C_F$), where C_S ideally equals C_F. If $C_S>C_F$ (or $C_S<C_F$) due to the process variation, the transfer curve of one stage will be deviated and be larger (or smaller) than the full signal range, thus, the signal has severe distortions and wrong codes are resolved due to this non-linear effect. Figure 3.29 shows the effect of capacitor-mismatch.



(a) (b)

Figure 3.29 Capacitor-mismatch effects with (a) 1% mismatch (b) 3% mismatch

3.7 Proposed Capacitor-Mismatch Calibration Technique

Nowadays, the requirements for the Pipelined ADC have been increasing rapidly. Many applications demand several tens of megahertz high-speed conversion rates and 10-bit or even better resolution .To achieve both higher speed and higher resolution, the conventional structure of Pipelined ADC must be innovated. Since the linearity of a Pipelined ADC is primarily determined by the linearity in each of Pipelined stage,

so it is necessary to carefully consider the non-linearity effects in every stage.

The effect of the comparator offset error can be eliminated by incorporating digital error correction, which is a successful algorithm of the redundant signed digit (RSD) technique. However, linearity is still limited by components mismatch, especially the mismatch among capacitors. Numerous background calibration techniques had been developed to improve the accuracy of ADCs [33][34][35]. However, these techniques usually require a large amount of complex (analog or digital) circuits or require extra clock period for calibration, which may not be suitable for the high conversion rate application and not be cost effective as well.

The proposed capacitor-mismatch calibration technique randomly swaps the feedback capacitor with the sampling capacitor in the MDAC circuit, and it corrects the errors caused by capacitor mismatch to improve the linearity. This technique is not complex in circuit implementation, and it does not require extra clock cycle. Hence, It can be easily adopted either for single- or multi-bit Pipelined stages. The 1.5-bit Pipelined stage is adopted in this thesis to demonstrate the proposed technique.

Capacitor-Mismatch Calibration Technique: We first consider Figure 3.30, which is the conventional "capacitor-flip-around" multiplying digital-to-analog converter (MDAC), where for simplicity a single-ended implementation is shown.

This configuration is widely utilized to realize 1-bit or 1.5-bit Pipelined stages. In Figure 3.30, *IN* represents the input signal of the stage, that is, the analog residue from previous stage; the digit *D* is the reference voltage depending on the input signal (IN) level, which is $\pm V_{REF}$ or 0, and *OUT* is the output residue.

This MDAC of conventional type uses fixed C_F as the feedback capacitor during the amplifying cycle of phase Φ_h. Here, we define the capacitor-mismatch error factor as

$$\Delta C \equiv \left(C_S - C_F\right) / C_F \tag{3.22}$$

, and also assume that there are no gain errors due to op-amp non-idealities. After the normal ADC conversion of two non-overlapping phase Φ_s and Φ_h, the MDAC output residue can then be expressed as

$$OUT = 2IN(1+\frac{\Delta C}{2}) - D(1+\Delta C) \tag{3.23}$$

, where this analog residue including capacitor-mismatch factors, causes non-linearity effects.

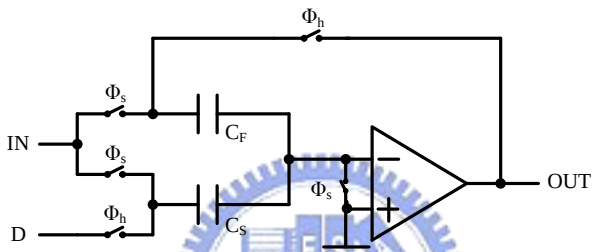


Figure 3.30 Conventional MDAC for 1-bit or 1.5-bit Pipelined stages

In the proposed capacitor-mismatch calibration technique, we do not need complex circuitry so that there is less hardware implementation (less area), and do not require extra clock cycle for calibration so that this can be adopted for high speed application (high speed). In this architecture depicted in Figure 3.31(a), unlike the conventional one, the roles of capacitors C_S and C_F are randomly interchanged (i.e., C_S and C_F are randomly swapped) during the phase Φ_h. Such a capacitor-swapping operation is achieved by using a pseudo-random clock generator that randomly generates the random control signal $S_{OUT.}$, which is shown in Figure 3.31(b)

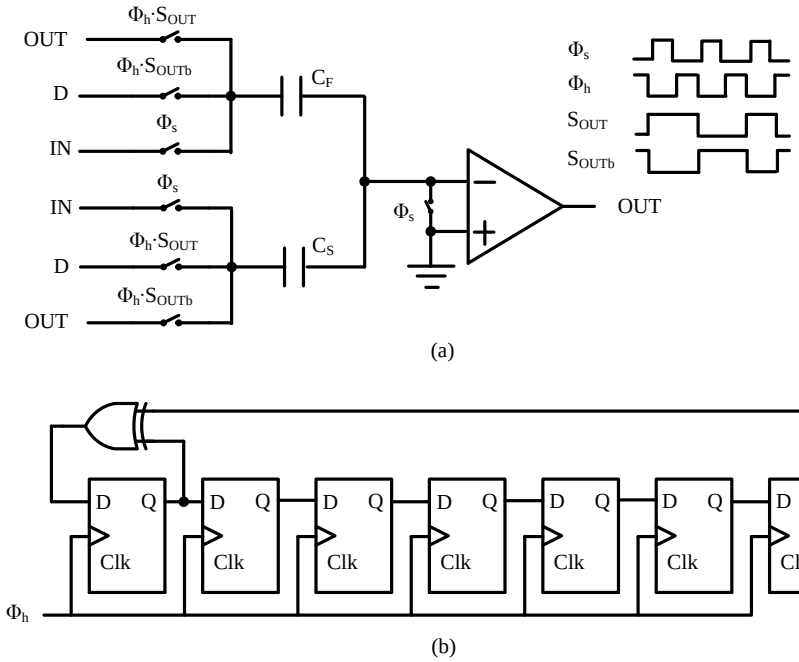


Figure 3.31 (a) 1.5-bit MDAC with capacitor-swapping technique (b) Pseudo-random clock generator

When the operation is in the amplifying phase (Φ_h), if S_{OUT} is 1, C_F is connected in the feedback loop such that the capacitor-mismatch error factor is ΔC, as expressed in Equation (3.22); otherwise, if S_{OUT} is 0, the roles of C_F and C_S are interchanged and the C_S is connected in the feedback loop. Thus, the value of ΔC becomes

$$\Delta C\big|_{S_{OUT}=0} \equiv (C_F - C_S)/C_S = -(\Delta C + \Delta C^2) \approx -\Delta C \qquad (3.24).$$

According to the proposed capacitor-swapping technique, the MDAC residue signal *OUT* can be expressed in terms of *N* as:

$$OUT = 2IN(1 + N\frac{\Delta C}{2}) - D(1 + N\Delta C) \qquad (3.25)$$

When S_{OUT} is 1, making *N* to be +1; otherwise, if S_{OUT} is 0, *N* becomes -1. Thus, we can find that the operation of MDAC with the pseudo-random number generator, ΔC and $-\Delta C$ mismatch error randomly appear, so the capacitor-mismatch effect could be averaged out and overall ADC linearity is improved [36].

3.8 Summary

At the beginning of this chapter, we focused on the analysis of one Pipelined stage, including the mathematical description and circuit implementation. The common non-idealities in one stage were also discussed. In order to eliminate the offset errors caused by the Sub-ADC, the digital error correction adopting redundant signed digit (RSD) algorithm was incorporated into the ADC circuit and introduced in detail. With digital correction algorithm for large tolerance of comparator offset, a low-resolution of 1.5-bit/stage structure was implemented in this thesis to get the advantages of higher speed, less hardware, and lower power than other stage resolution. Besides, the ADC behavior model was built by Simulink in Matlab to help our design, which simplifies large number of transistors into function blocks and takes the advantage of short simulation time. Finally, we focused on the technique for linearity-improving against the capacitor-mismatch effect. The design and implementation of related circuits in this thesis will be given in the next chapter.

Chapter 4

Design and Simulation of The Pipelined ADC With Capacitor-Mismatch Calibration Technique

4.1 Introduction

In the section 3.7, we briefly introduced a linearity-improving technique for the Pipelined ADC. As compared with the conventional architecture, the linearity errors due to capacitor-mismatch could be efficiently corrected through this method in each Pipelined stage. The feedback capacitor is randomly swapped with the sampling capacitor during the amplifying cycle of the ADC operation, which effectively improves the ADC overall linearity.

In this chapter, the design of the 10-bit, 100MHz Pipelined ADC with random capacitor error-averaging technique are introduced in detail. First of all, we find the accuracy requirements for this ADC specification and take care of the implemented switched-capacitor (SC) technique. Second, the analog Sub-circuits including the operational amplifier (Op-amp), the sample-and-hold (S/H) circuit, multiplying-DAC (MDAC), and comparators operated by supply voltage 1.8V are all presented with their simulation results; the part of digital circuits contains the clock generator and the digital error correction logics, which are also operated with 1.8V supply voltage. Finally, the layout of the overall Pipelined ADC is also presented with its floor plan. This prototype of ADC was implemented with the TSMC 0.18μm CMOS 1P6M process technology.

4.2 Accuracy Requirements of One Pipelined Stage

To achieve the desired conversion rate, resolution, and linearity, each Pipelined stage must be designed carefully such that non-ideal effects do not excessively degrade the overall performance. Therefore, the accuracy requirements of one stage are all critical to the ADC performance.

4.2.1 Op-amp Requirements

In the Pipelined ADC, the accuracy requirement of each stage is different because the resolved resolution decreases down stage by stage. For example, an N-bit ADC with the effective resolution of n-bit/stage, the first stage has to achieve N-bit accuracy and is the most significant for whole ADC linearity. However, the next stage meets only N-n bits accuracy requirement, which is further reduced n-bit/stage for the following stages. Although more errors are accumulated in latter stages, the reduced stage resolution for accuracy means that design constraints in latter stages are more relaxed; that is, in terms of this viewpoint, the constraints of op-amp gain accuracy, op-amp bandwidth, op-amp settling time, capacitor matching (DAC accuracy), and thermal noise are more relaxed in latter stages.

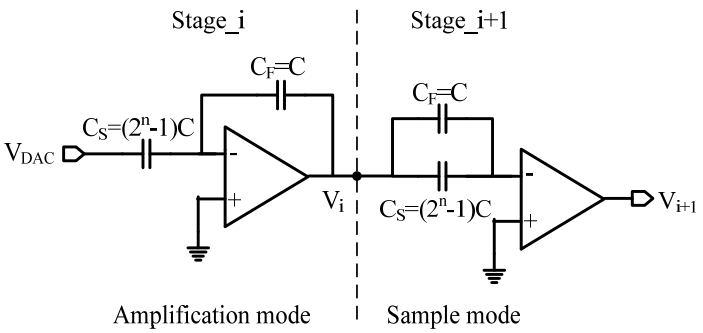


Figure 4.1 Operation of adjacent Pipelined stages

In Figure 4.1, the adjacent Pipelined stages are depicted that the stage_i is in the amplification mode, while stage_i+1 is in the sample mode. For a given total resolution of N bits, the per-stage resolution of n, and op-amp non-idealities, the relationship between the input and output of stage_i can be known as

$$V_i = G_i \cdot (V_{IN} - V_{DAC}) \tag{4.1}$$

and

$$G_i = \left(1 + \frac{C_S}{C_F}\right) \cdot \left(1 - e^{-\frac{t}{t}}\right) \cdot \left(\frac{1}{1 + \frac{1}{A} \cdot \frac{1}{b}}\right) \tag{4.2}$$

, where β is the feedback factor and is shown in Equation (4.3). The exponential term is the considered finite settling time t of the single pole op-amp (τ is the time constant for the SC configuration), and A represents the finite op-amp gain.

$$b = \frac{C_F}{C_F + C_S + C_{Op-amp}} \tag{4.3}$$

Because the i-th stage resolves n-bit, the ideal inter-stage gain G_i can be known as

$$G_i = 1 + \frac{C_S}{C_F} = 1 + \frac{(2^n - 1)C}{C} = 2^n \tag{4.4}$$

, where Equation (4.4) depends on the matching of capacitors.

In order to achieve total N-bit linearity for the first stage where the accuracy is significantly demanded, the finite gain error in the inter-stage amplification should be theoretically less than 1/2 LSB for safe design, and the finite gain error is defined as

$$e_r = \left|\frac{G_{actual} - G_{ideal}}{G_{ideal}}\right| = \left|\frac{1}{Ab}\right| \tag{4.5}$$

Therefore, we can get

$$e_r < \frac{1}{2} \cdot \frac{1}{2^N} \tag{4.6}$$

, then combine (4.5) and (4.6), the limit of finite op-amp gain is yielded as following

$$A > \frac{1}{b} \times 2^{N+1} = \frac{C_F + C_S + C_{Op-amp}}{C_F} \times 2^{N+1} = 2^{N+1} \times \left(2^n + \frac{C_{Op-amp}}{C}\right) \tag{4.7}$$

If $C_{op\text{-}amp}$ is ignored, Equation (4.7) equals 2^{N+1+n} and is the minimum requirement of A for the first stage. In practice, the op-amp gain should be much larger than this value since errors caused by other sources such as incomplete amplifier settling and capacitor-mismatch are not taken into account.

After realizing that how the accuracy is limited by the finite op-amp gain, the error caused by the finite settling time is further defined. We first consider Figure 4.2 [37], the speed constraints influencing the accuracy include the slew time of large signal and the settling time of small signal. The slew time is related to the bias current and load capacitance of the op-amp, as well as the signal level; while the settling time depends on the unity-gain frequency (f_μ) and phase-margin of the op-amp, the feedback factor(β), and total resolution (N).

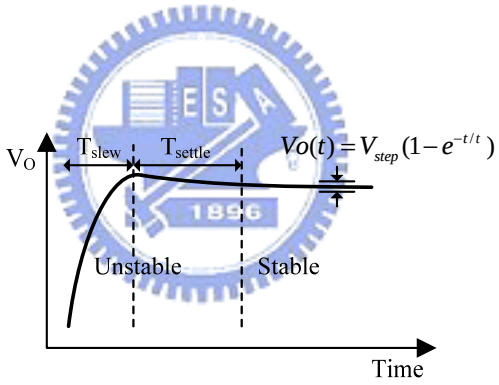


Figure 4.2 Settling analysis of step response

In Figure 4.2, the settling error of output response can be defined as

$$e_{rr} = e^{-t/t} \tag{4.8}$$

, where $t = \frac{1}{w_{3dB}} = \frac{1}{2p \cdot f_u \cdot b}$ for the single pole op-amp. For the same reason, the settling error must be less than 1/2 LSB to achieve N-bit resolution

$$e^{-T_{settle}/t} < \frac{1}{2} \cdot \frac{1}{2^N} \tag{4.9}$$

According to (4.9), we can obtain the required minimum unity-gain frequency f_μ

$$f_u > \frac{(N+1)\cdot ln2}{2p\cdot T_{settle}\cdot b} = \frac{(N+1)\cdot ln2}{2p\cdot T_{settle}}\cdot\left(2^n + \frac{C_{Op-amp}}{C}\right) \quad (4.10)$$

, where T_{settle} is the allowed settling time and is usually 75%~90% of half conversion period [28] ($T_{settle} \cong (0.75 \sim 0.9)\cdot\frac{T_S}{2}$ *where* $F_S = \frac{1}{T_S}$), depending on the design style. In general, the margin of 10%~25% is conserved for the non-overlapping of Φ_s and Φ_h, as well as for the slew time of a slew-rate limited op-amp. Therefore, total unstable time in Figure 4.2 can be estimated by

$$T_{unstable} = T_{slew} + T_{settle} = \frac{V_{step}}{SR} + (N+1)\cdot ln2\cdot t \quad (4.11)$$

We can observe from Equation (4.10) and (4.11) that more resolution for N and n, the larger bandwidth f_u and T_{settle} are required to sustain the speed and accuracy of the Pipelined ADC.

4.2.2 Capacitor Requirements

In the Pipelined ADC, the required matching of sampling and feedback capacitors in MDACs are determined by the required DAC accuracy. Generally, the capacitors C_S and C_F are not equal exactly due to the process variation.

We assume that the value of capacitors deviates by ΔC, which makes C_S=C+ΔC/2 C_F=C-ΔC/2, the MDAC residue output is then given by

$$V_{OUT} = (2+\frac{\Delta C}{C})V_{IN} \pm (1+\frac{\Delta C}{C})V_{DAC} \quad (4.12)$$

Equation (4.12) sets the requirement of the MDAC in the first stage, where ΔC/C for each capacitor must be less than $1/2^N$ to ensure that ΔV_{DAC} is less than 1LSB.

$$\frac{\Delta C}{C} < \frac{1}{2^N} \quad (4.13)$$

In addition to above deterministic errors, there are also random errors which

mainly result from the thermal noise KT/C in SC circuits. Assuming this random error is Gaussian variable G(μ, σ^2) and its power is represented by the variance σ^2. Therefore, the total power of thermal noise referred to the input of stage_1 can be expressed by

$$s^2_{total,1} = \left(\frac{1}{2^n}\right)^2 s^2_1 + \left(\frac{1}{2^n}\right)^4 s^2_2 + \left(\frac{1}{2^n}\right)^6 s^2_3 + \cdots\cdots \tag{4.14}$$

, where σ^2_1 is the output referred noise power from stage_1, and $\sigma^2_{total,1}$ should be much less than 1LSB to maintain sufficiently SNR for N-bit accuracy requirement.

$$s^2_{total,1} << \frac{1}{2^N}(=1LSB) \tag{4.15}$$

Notice that the noise contribution is reduced stage by stage due to the accumulated inter-stage gain. Therefore, the constraint of thermal noise mainly from ON-resistances of the switches and op-amp is most stringent for the first stage, and is relaxed down the subsequent stages.

As we know, larger capacitors tend to have better matching property and less KT/C contribution than smaller capacitors. However, smaller capacitors provide less loading and faster settling for enabling high speed. That is, we can reduce the sampled thermal noise by increasing the size of sampling capacitors, nevertheless, the power consumption also increases and output settling is more limited at the same time.

As a result, there exists a tradeoff when determining the capacitor size. In the design of ADCs, thermal noise power is necessarily designed smaller than the power of the quantization noise which had been shown to be $V_{LSB}^2/12$. Thus, this sets a lowest limit for the capacitor value of C as follows [38].

$$C >> \frac{4KT \cdot 12}{V_{FS}^2} \cdot 2^{2N} \tag{4.16}$$

, where N is the total resolution of the ADC which has a full-scale input signal V_{FS} and four sampling capacitors C in the MDAC. Furthermore, the SNR under the

combined effects of quantization noise and thermal noise can be set an upper bound as

$$SNR \le 10log\left(\frac{V_{FS}^2/2}{\frac{(V_{FS}/2^N)^2}{12}+\frac{kT}{C_{total}}}\right) \quad (4.17)$$

4.3 Design of Analog Sub-Circuits

This section emphasizes on the analog part of building circuits adopted in the prototyped ADC. These circuits which include the operational amplifiers in the front-end S/H and MDACs, comparators in 1.5-bit and 2-bit Flash ADCs, even the switches, are overviewed with the general analysis and design techniques.

All analog circuits are fully differential, which have advantages of reducing the even-order harmonic distortions, the substrate noise, common-mode disturbances, charge-injection and clock-feedthrough effects, and have larger dynamic range.

4.3.1 Input-Stage Sample-and-Hold Circuit

The S/H of input-stage dominates the speed and linearity of whole Pipelined ADC. The speed means sampling rate, while linearity means characteristics such as signal-to-noise ratio. Most CMOS S/H circuits are based on the switched-capacitor technique. Therefore, before introducing the S/H with precharging technique, we first concern the switched-capacitor technique which is critical for the design of the ADC.

4.3.1.1 Switched-Capacitor Technique

The switched-capacitor (SC) technique is recently pervasive in highly integrated,

mixed signal circuits. The simplest switched-capacitor circuit is shown in Figure 4.3, which has the functions of sample and hold. If the signal must be processed by a discrete time system, such as the ADC, this circuit topology is ubiquitous for its good linearity of data sampled and stored.

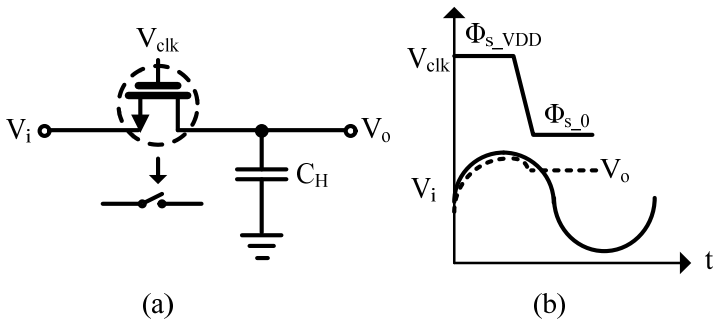


Figure 4.3 (a) The simple sampling circuit (b) Functionality

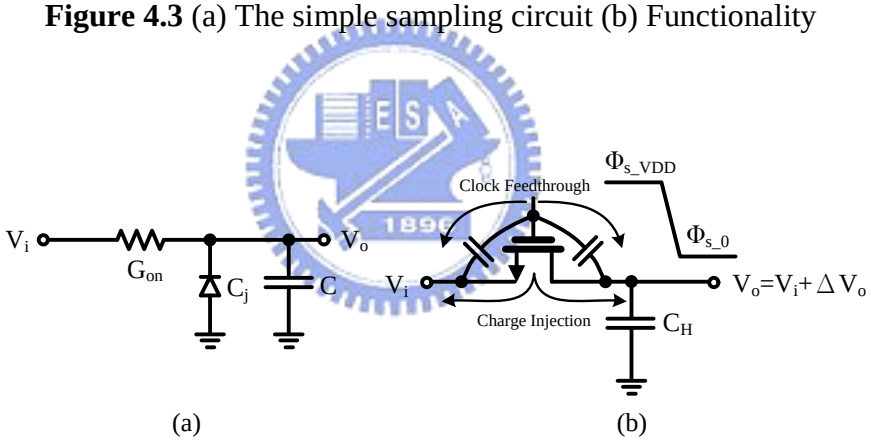


Figure 4.4 (a) Equivalent circuit of sample mode (b) Transition from sample mode to hold mode

However, there are several practical limitations in this switch-implemented circuit. In the operation of sample mode shown in Figure 4.4(a), the switch has an effective on-conductance of G_{ON}, which is given by

$$G_{on} = \frac{1}{R_{on}} = m_n C_{ox} \frac{W}{L}(\Phi_{s\_VDD} - V_i - V_t) \tag{4.18}$$

, and introduces thermal noise KT/C at the output. Because the RC network has finite

bandwidth, the time required for V_o to track V_i to within a specified tolerance is called *acquisition time*. The junction capacitor C_j is induced between drain and substrate of the MOSFET, while the capacitor C includes the capacitors of C_H and C_{gd}. Therefore, we can obtain the frequency response during the sample mode as follows

$$V_o = \frac{1}{1 + j\frac{v\,(C + C_j)}{G_{on}}} V_i \tag{4.19}$$

, where G_{ON} and C_j are signal-dependent to introduce non-linearity effects, and V_o nearly equals V_i by designing $G_{on} >> jv\,(C + C_j)$.

When the switch turns off from the sample mode to hold mode, there is an error voltage ΔV_o stored on the capacitor C_H along with the instantaneous sampled voltage V_i. The error voltage ΔV_o is called *pedestal error* and is due to effects of ΔV_{o1} for channel charge injection and ΔV_{o2} for clock feedthrough. As illustrated in Figure 4.4(b), the total charge Q_{CH} in the inversion layer is

$$Q_{CH} = WLC_{ox}(\Phi_{s\_VDD} - V_i - V_t) \tag{4.20}$$

, where L denotes the effect channel length. Channel charge injection means that Q_{CH} injects into two terminals of drain and source in a blink of switching-off. The charge injected to the direction of V_i can be absorbed and creates no error on this node; while the charge injected into C_H causes a change of voltage across it. If there is α % of Q_{CH} (theoretically 50% of Q_{CH}) injected into C_H, the resulting error equals

$$\Delta V_{o1} = \frac{a\,WLC_{ox}(\Phi_{s\_VDD} - V_i - V_t)}{C_H} \tag{4.21}$$

Equation (4.21) shows that the change of voltage across C_H is non-linear with respect to V_i due to the threshold voltage V_t with body-effect. Therefore, the charge injection is signal-dependent and causes three types of errors in sampled-data systems: gain errors ε, dc offsets V_{os}, and non-linearity. In many cases, the first two effects can be easily managed whereas the last cannot due to the causality of harmonic distortion.

It is instructive to consider the speed-precision trade-off resulting from charge injection. We represent the speed by a time constant τ and the precision by the error voltage ΔV_{o1}, and then define a figure of merit as $F = t \cdot \Delta V_{o1}$ [39]. Combining Equation (4.21) and (4.22)

$$t = R_{on} \cdot C_H = \frac{C_H}{m_n C_{ox} \frac{W}{L} (\Phi_{s\_VDD} - V_i - V_t)} \tag{4.22}$$

, we can get

$$F = \frac{a L^2}{m_n} \tag{4.23}$$

Thus, the effect of F can be minimized by designing minimal channel length and the use of NMOS instead of PMOS. The factor α can be also degraded by the use of dummy switch or differential sampling. Note that the effect of charge injection also exists when the switch turns on.

Also, the gate-controlled clock will couple to the capacitor C_H through overlap capacitances of C_{gs} and C_{gd}. When the switch turns on, this capacitive feedthrough has no effect on the final value V_o; while the switch turns off, where the clock makes the transition to low, a capacitive voltage divider exists between C_{gd} and C_H. That is, a portion of clock signal Φ_s appears across C_H as

$$\Delta V_{o2} = \frac{\Phi_{s\_VDD} \cdot C_{gd}}{C_{gd} + C_H} \tag{4.24}$$

, which is the error voltage added on the sampled output voltage. Note that the error of ΔV_{o2} is independent of the input level and can be treated as a constant offset. As with charge injection, clock feedthrough leads to a trade-off between speed and precision as well. In addition to charge injection and clock feedthrough, the third error called *droop* occurs during the hold mode. This error is related to the leakage current from parasitic capacitors and MOSFET substrate. We can design with larger sampling

capacitor to minimize the error of droop. However, the trade-off is to increase the acquisition time with slower output settling.

In reality, the clock transition between the sample and hold modes has a finite falling time instead of an infinite slope. In this time period, the switch will not turn off until the gate voltage Φ declines to a value less than V_i+V_t, as illustrated in Figure 4.5. The time of Δt is called *aperture jitter* (or *aperture uncertainty*) with random variation, and creates sampling error if a periodic signal is repeatedly sampled at the same points. Note that the worst aperture error occurs at the zero crossing of the sinusoidal input, where the rate of change is the greatest [4][39][40].

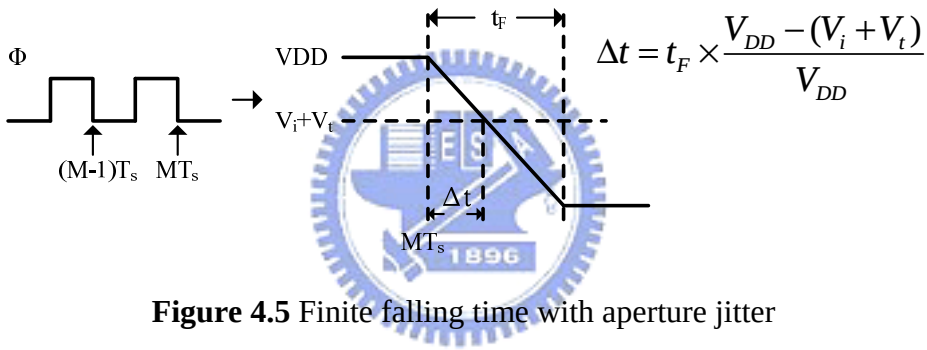


Figure 4.5 Finite falling time with aperture jitter

Furthermore, the signal-to-noise ratio is also limited by the aperture noise such as

$$SNR = 20log(2p \cdot f_i \cdot \Delta t_{R.M.S})^{-1}\ dB \tag{4.25}$$

We can observe that SNR is independent of signal amplitude, and it is degraded as the signal frequency f_i and the R.M.S value of jitter Δt increases. Finally, with errors described above, output V_o sampled at *M*-th sampling period can be summarized as

$$V_o(k) = (1+e) \times V_i(MT_s + \Delta t) + V_{os} \tag{4.26}$$

4.3.1.2 Bootstrapped Switch

With the decreasing supply voltage in advanced CMOS process, analogue NMOS or PMOS switches are not suitable for switching rail-to-rail analogue signal, even the transmission-gate (CMOS) switch also faces the challenge of reduced dynamic range.

Furthermore, from section 4.3.1.1, we know that there exists finite resistance which varies with different values of input signal V_i when the switch is on. This signal-dependent resistance makes the sampled input to be distortion at output and degrades the linearity, especially more severe with lower supply voltage. As a result, a gate-voltage boosting switch is implemented in the front-end sample-and-hold circuit to avoid problems described above.

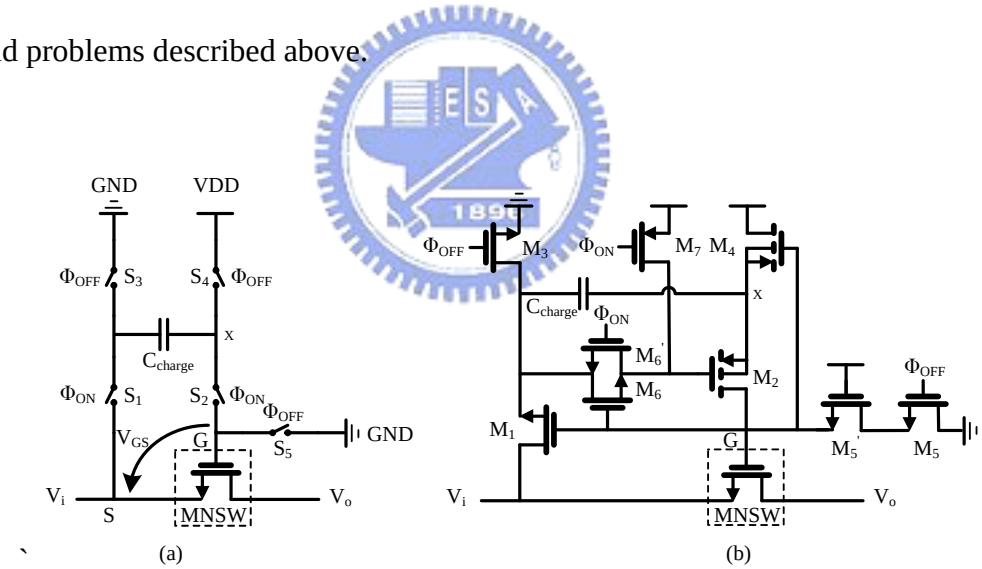


Figure 4.6 Bootstrapped switch with (a) basic idea (b) transistor-level implementation

Figure 4.6(a) shows the basic idea of the gate-voltage boosting switch, which contains the signal switch MNSW together with five additional switches (S_1~S_5), and a charging capacitor C_{charge}. During the OFF-phase Φ_{OFF} for switch MNSW, C_{charge} is precharged to VDD through S_3 and S_4, and switch S_5 connects the gate voltage V_G of MNSW to GND to make sure that the transistor is in the OFF state; while during the

ON-phase Φ_{ON}, a loop is formed between gate and source of MNSW, that is, VDD stored in C_{charge} is treated as a constant V_{GS}. This guarantees the switch conductance independent of V_i and decreases distortions. The fixed V_{GS} also eliminates the high gate oxide voltage when the input signal is low, and a bootstrapped clock boosted to V_i+VDD is generated at node G to handle all levels (rail-to-rail) of input signal. Besides, this switch technique makes charge-injection error in Equation (4.21) only a constant offset instead of a signal-dependent error deteriorating the accuracy.

Figure 4.6(b) shows this circuit implementation to achieve goals stated in above paragraph. Transistors M_1~M_5 correspond to five switches shown in Figure 4.6(a), and additional transistors are added as well as modified connectivity to allow all transistors with exact operation. Points deserved to be mentioned is that the voltage at node X may exceed VDD during Φ_{ON} operation, that is, the source voltage of M_2 and M_4 would be higher than their substrate voltage which is usually connected with VDD. This problem would cause leakage currents due to a biased-forward junction diode between the source and substrate, therefore, sources and substrates of M_2 and M_4 should be tied together at node X respectively. Furthermore, additional transistor M_5' reduces V_{ds} stress on M_5. The simulation result is shown in Figure 4.7 with a sinusoidal input, and maximum V_G is not equal to 2VDD due to circuit imperfections.

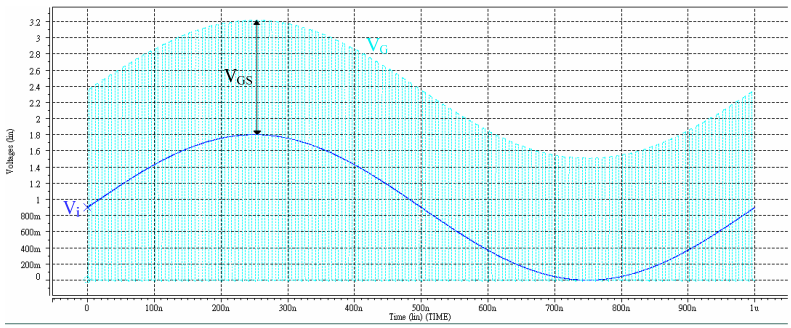


Figure 4.7 Simulation result of bootstrapped switch

Generally, the switch with gate-boosting technique resolves problems in conventional switches, nevertheless, this boosted clock strategy may have an issue of reliability which is that the circuit lifetime is not assured [41][42].

4.3.1.3 Precharged S/H

The resolution accuracy and conversion speed of whole ADC critically depends on the performance of front-end sample-and-hold amplifier, which should be capable of acquiring wideband input signal, and driving large load capacitance of the next stage with low distortion for high speed target.

Figure 4.8 shows the implemented S/H and its timing operation in this prototype ADC. Instead of the conventional "flip-around" architecture [43], the S/H with precharged technique [44] is adopted.

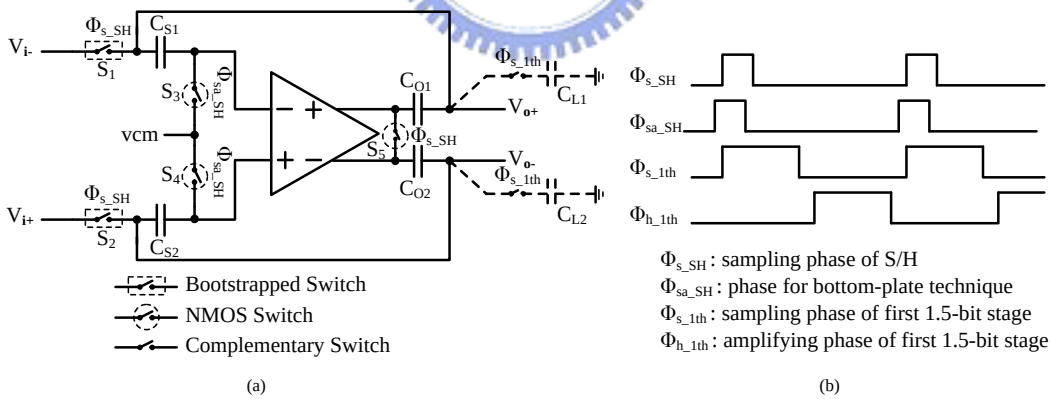


Figure 4.8 Precharged S/H with (a) fully differential scheme (b) timing operation

As seen in the figure, three types of analog switches are employed. Two bootstrapped switches are adopted as the input sampling switches for reducing distortion which depends on input frequencies; NMOS are selected as three switches connected to the fixed bias voltage of vcm which does not swing largely as input

signal, and CMOS transmission gates are used in the signal path of subsequent 1.5-bit stages [45]. Basic operation and requirements of the S/H had been illustrated in section 3.6.1 and section 4.2, and here, some evolutions are presented in this architecture. First of all, during the sample mode (Φ_{s_SH} =1 and Φ_{s_1th} =1) shown in Figure 4.9(a), which is single-ended for simplicity, charges from V_i are not only stored in C_{S1}, but also stored in C_{O1} and C_{L1}, where C_{L1} is the output load induced by the next stage. Because the input is sampled on C_{S1}, C_{O1} and C_{L1} respectively, the sampled noise power is

$$\overline{V^2_{n,s}} = \frac{KT}{C_{S1} + C_{O1} + C_{L1}} \tag{4.27}$$

, which is smaller than the value of KT/C_S in conventional "flip-around" architectures, and smaller capacitors C_{S1} and C_{O1} can be selected for power-saving and fast-settling.

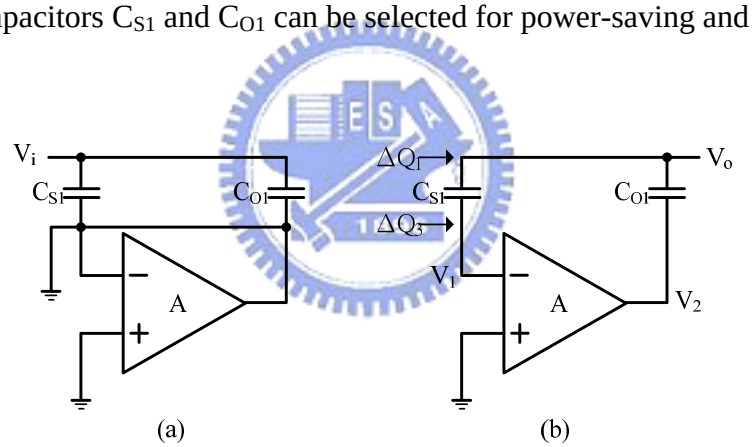


Figure 4.9 Precharged S/H with (a) sample mode (b) hold mode

When switching to the hold mode (Φ_{s_SH} = 0), switches S_3 and S_4 turn off a moment earlier than switches S_1 and S_2 to reduce effects of charge injection, which is called bottom-plate technique and will be introduced later. In Figure 4.9(b), let ΔQ_3 be the signal-independent charge injection to node V_1 when the switch S_3 turns off, and thus

$$\Delta Q_3 = C_{S1}(\Delta V_1 - \Delta V_o), \quad \Delta V_o \approx \Delta V_2 = -A\Delta V_1 \tag{4.28}$$

, where ΔV_1, ΔV_2 and ΔV_o are variations caused by ΔQ_3. Therefore, we can get

$$\Delta V_1 = \frac{1}{1+A} \cdot \frac{\Delta Q_3}{C_{S1}}, \quad \Delta V_o = -\frac{A}{1+A} \cdot \frac{\Delta Q_3}{C_{S1}} \tag{4.29}$$

A moment later, let ΔQ_1 be the charge injection to node V_o when the switch S_1 turns off. In the same way, we can get

$$\Delta Q_1 = C_{S1}(\Delta V_o - \Delta V_1) + C_{o1}(\Delta V_o - \Delta V_2) \tag{4.30}$$

, where

$$\Delta V_1 \approx \Delta V_o, \quad \Delta V_2 = -A\Delta V_1 \approx -A\Delta V_o \tag{4.31}$$

, and get

$$\Delta V_o = \frac{1}{1+A} \cdot \frac{\Delta Q_1}{C_{O1}} \tag{4.32}$$

Finally, combining Equations (4.29) and (4.32), we can observe that variations at S/H output after hold mode is

$$\Delta V_o = \frac{1}{1+A} \cdot \frac{\Delta Q_1}{C_{O1}} - \frac{A}{1+A} \cdot \frac{\Delta Q_3}{C_{S1}} \tag{4.33}$$

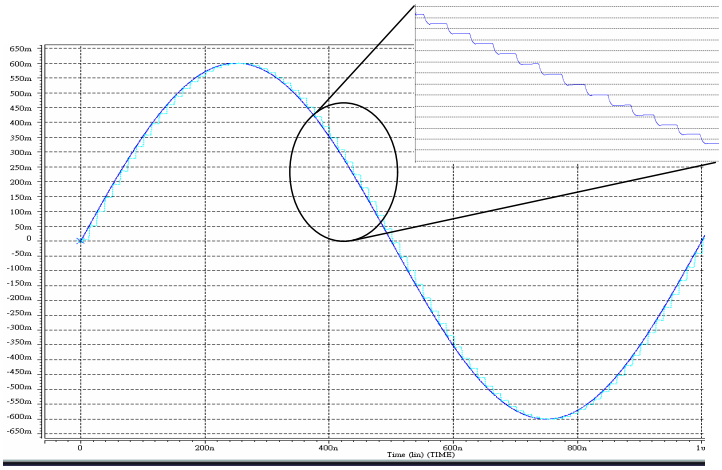
, which varies slightly and is less affected by the signal-dependent error ΔQ_1. That is, instead of the reset of V_o in sample mode by conventional "flip-around" architectures, there are two output capacitors C_{O1} and C_{O2} precharged with small variations during the sampling phase, and the op-amp output can settle to desired values in a much shorter time period. As a result, the slew-rate and settling time of the op-amp in S/H can be relaxed for higher-speed demand. Finally, the output at the end of hold mode can be expressed as

$$V_o \approx V_i \left[1 + \frac{1}{A}\left(\frac{V_{CO}}{V_i} - 1 \right) + \frac{1}{A}\frac{C_L}{C_O}\left(\frac{V_{CL}}{V_i} - 1 \right) \right] \tag{4.34}$$

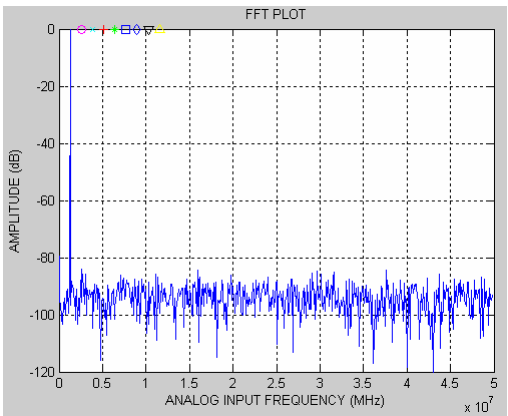
, where errors also relate to ratios of stored voltage in capacitors, and are almost equal to 1 with slow-varying input. Thus, the DC gain requirement for the op-amp is more relieved [44][46].

In summary, the best achievable performance of this Pipelined ADC is dominated by the transient behavior of the closed-loop S/H in the hold mode, where

the distortion is caused by the finite DC op-amp gain and sampling switches, while noise is mainly contributed from sampling switches and the aperture jitter. Figure 4.10(a) shows the S/H simulation result with transient response, while Figure 4.10(b) is the FFT spectrum analysis. All simulations are under conditions of 1MHz sinusoidal input with the amplitude of ±600mV, 100MHz sampling rate, as well as output load capacitances of 2pF. With low distortion and noise floor shown in FFT, SNDR is about 75dB and ENOB equals about 12-bit to confirm enough 10-bit linearity in latter stages.



(a)



(b)

Figure 4.10 S/H simulation results with (a) input/output transient response (b) FFT spectrum

4.3.1.4 Bottom-Plate Sampling Technique

In Figure 4.8, the connection of C_{S1}, S_1 and S_3 is sometimes called *bottom-plate sampling*, which is that the bottom plate of sampling capacitor is connected with input signal instead of the op-amp input for better substrate-noise isolation and feedback factor. Furthermore, the Φ_{sa_SH} controlled switch should be turn off slightly before the Φ_{s_SH} controlled switch, and Figure 4.11 illustrates why.

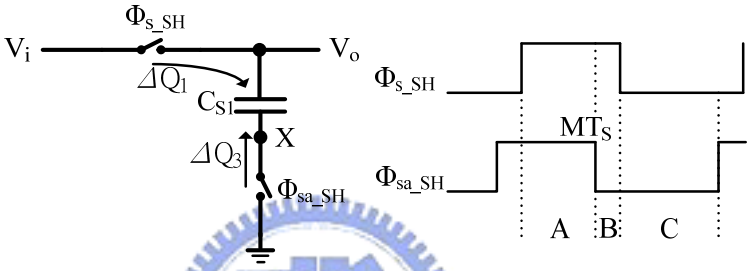


Figure 4.11 Bottom-plate sampling

First, we can observe charges stored in C_{S1} during three different time period. In time period of A, switches S_1 and S_3 are on, and the charge sampled on C_{S1} is $C_{S1}\times V_i(t)$; in period of B, S_3 turns off first, and the charge stored in C_{S1} has a little variation as $C_{S1}\times V_i(MT_S)-\Delta Q_3$; a moment later, S_1 turns off during period of C, and the signal-dependent charge injection of S_1 is injected into C_{S1}. Since C_{S1} had been floated during this period, ΔQ_1 does not alter charges stored in C_{S1} due to charge conservation. Therefore, the voltage held in capacitor C_{S1} only has a constant offset with ΔQ_3 instead of containing signal-dependent error. Note that ΔQ_1 may be enhanced by parasitic capacitance from node X to ground [40].

4.3.2 Operational Amplifier

The core component in front-end S/H stage and 8 subsequent stages of the Pipelined ADC is the operational amplifier, which actually has some limitations such as finite DC gain, finite bandwidth, stability, and linearity to be considered and analyzed in ADC design. For analog circuits, speed and accuracy are two of the most significant properties, and are dominated by the settling behavior of the op-amp. Fast settling requires high unity-gain bandwidth to achieve, whereas accurate settling requires high DC gain to support. Nevertheless, realization of an op-amp with high DC gain has been a difficult problem without sacrificing high unity-gain bandwidth in low-voltage CMOS process.

Architectures of the op-amp can be roughly classified into two of single-stage and multi-stage, and different architectures having their own ascendancy among above limitations are adopted for suitable purposes. A multi-stage architecture may have large DC gain and high swing for different stages functionality, however, it is not suitable for high-speed application since there is at least one pole in each stage, which decreases the bandwidth and stability of the feedback system. Popular architectures of single-stage such as telescopic and folded-cascode are usually designed for high-speed requirements, which are also capable of high gain due to cascode stage with large output impedance. Although the operation speed of telescopic op-amp is fastest, the output swing is severely restricted by a large amount of cascoded transistors, especially in low-voltage process. Therefore, a folded-cascode architecture which slightly improves small output swing and input common mode range in telescopic architectures and is more stable with lager bandwidth than multi-stage architectures due to only one dominant pole, is commonly adopted in high speed circuits. The performance such as speed and gain of the folded-cascode op-amp may be not the best

in all kinds of architectures, nevertheless, it can almost meet circuits requirements in all aspects for its good balance among gain, speed, and output swing.

As shown in Figure 4.12, a folded-cascode op-amp with PMOS input differential pair is adopted in the S/H stage as well as 8 Pipelined stages, and the fully-differential architecture has advantages of higher immunity to "environmental" noise, reducing even-order harmonic distortion, and doubling of the output swing.

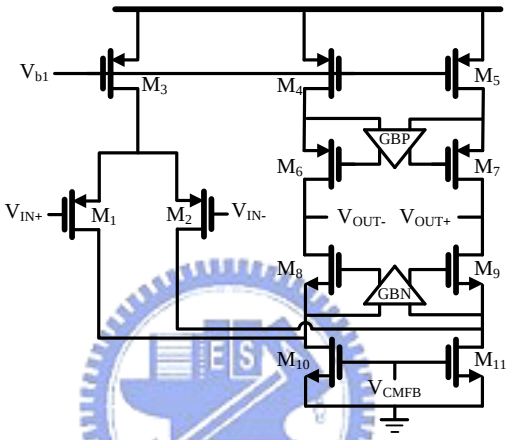


Figure 4.12 Fully-differential folded-cascode op-amp with gain boosting

In Figure 4.12, a gain enhancement method is employed without adding additional stages or stacking more cascode devices to increase the DC gain for higher resolution accuracy. This method is called gain-boosting [47][48][49] and is illustrated by Figure 4.13(a), where the original output impedance $g_{m2}r_{o2}r_{o1}$ is enhanced by A_1. The idea is to drive the gate of M_2 by the amplifier A_1 that forces V_S to be equal to V_b, which makes M_2 in a negative feedback loop of current-voltage. Thus, voltage variations at the drain of M_2 affect V_S to a lesser extent because A_1 "regulates" this voltage, keeping more constant current to yield higher output impedance. The small signal model in Figure 4.13(b) proves the enhanced impedance R_{OUT} as follows

$$R_{OUT} = \frac{V_a}{I_a} = \frac{I_a r_{o1} + (I_a - g_{m2} V_{GS2}) r_{o2}}{I_a} \approx A_1 g_{m2} r_{o2} r_{o1} \tag{4.35}$$

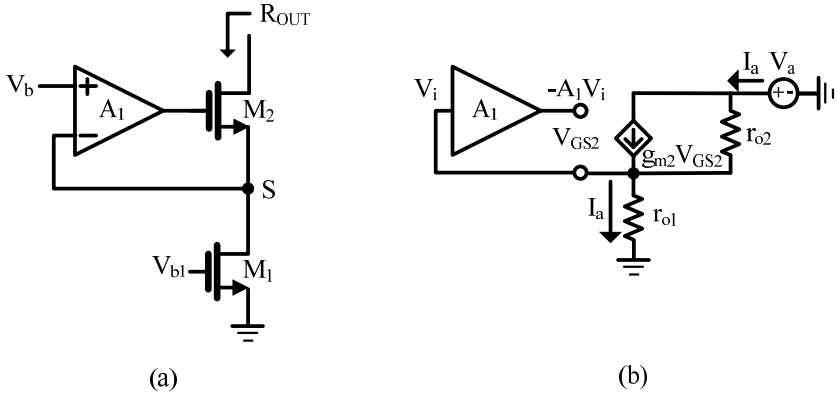


Figure 4.13 (a) Impedance boosting with feedback (b) Small signal model

Therefore, the open-loop gain of the fully-differential folded-cascode op-amp with gain boosting can be represented as

$$A = G_m \times R_{OUT} \tag{4.36}$$

, where the transconductance G_m is approximately equal to g_{m1} and output impedance R_{OUT} enhanced by boosting amplifiers of A_{GBN} and A_{GBP} can be calculated as

$$R_{OUT} \approx \left[A_{GBP} \left(g_{m6} + g_{mb6} \right) r_{o6} r_{o4} \right] \| \left[A_{GBN} \left(g_{m8} + g_{mb8} \right) r_{o8} \left(r_{o10} \| r_{o1} \right) \right] \tag{4.37}$$

Assuming total output capacitance and resistance are C_L and R_{OUT} respectively, the frequency response of this folded-cascode op-amp is given by

$$A(s) = \frac{g_{m1} R_{OUT}}{1 + s R_{OUT} C_L} \tag{4.38}$$

For high frequency response, where $sR_{OUT}C_L >> 1$, getting the approximation of unity-gain frequency ω_u as

$$w_u = \frac{g_{m1}}{C_L} \tag{4.39}$$

From the unity-gain frequency, we can find the dominant pole as follows

$$w_m = \frac{g_{m1}}{C_L} = A \cdot w_{P1} = g_{m1} \cdot R_{OUT} \cdot w_{P1}$$
$$\Rightarrow w_{P1} = \frac{1}{R_{OUT} \cdot C_L} \tag{4.40}$$

, which locates at the output of the op-amp. Because of the single-stage topology, the second pole is far away from the unity-gain frequency, which should be designed with five to ten times of the sampling frequency. It is also worth noting that there are non-dominant poles at the "folding point", i.e., the sources of M_8 and M_9, which are more far away from the origin than the architecture of NMOS input differential pair due to the effective small-signal g_m of NMOS instead of PMOS. Total effect capacitance on the source of M_8 contains C_{GS8}, C_{SB8}, C_{GD1}, C_{DB1}, C_{GD10} and C_{DB10}, where C_{GD10} and C_{DB10} are significant to be considered because M_{10} must be wide enough to carry a large current with small overdrive voltage [39].

However, the output common-mode (CM) of the fully-differential architecture must be well defined, which is quite sensitive to devices mismatch and power-supply variations. Hence, a common-mode feedback (CMFB) circuit which can sense and compensate the error of output CM level is required for proper control. Figure 4.14 shows the implemented CMFB, which is designed with SC architecture to allow larger output swing and have no additional parasitic poles in the CM loop.

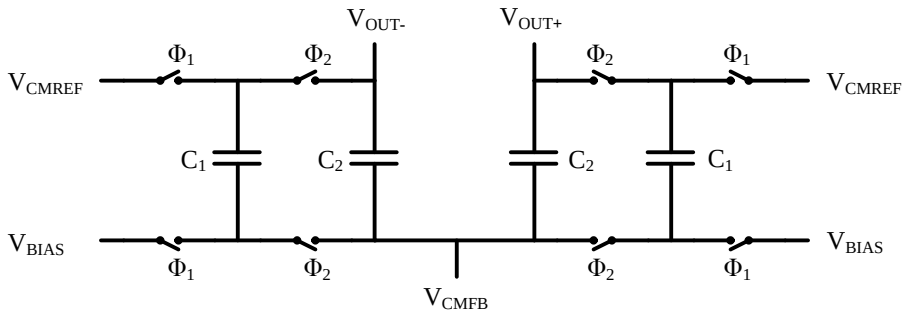


Figure 4.14 Switched-capacitor CMFB circuit

In Figure 4.14, V_{CMREF} is the desired output common-mode voltage, usually being half of the supply voltage. This circuit is operated by two non-overlapping phase of Φ_1 and Φ_2, where Φ_2 is the feedback period of the op-amp. Capacitors C_2 generate the average of the output voltages, which is used to create control voltage V_{CMFB} for the op-amp current source of M_{10} and M_{11}, and the desired DC voltage of V_{CMREF}-V_{BIAS} across C_2 is determined by capacitors C_1. If there are variations in CM voltages of V_{OUT+} and V_{OUT-}, V_{CMFB} coupling this variation senses error and returns V_{OUT+} and V_{OUT-} to the desired CM level through the functionality of negative feedback. Furthermore, all switches are realized by CMOS transmission gates with minimum length to reduce charge injection effects, and capacitors C_1 might be between one-quarter and one-tenth the sizes of capacitors C_2 [10].

Figure 4.15 shows the simulation of the fully-differential folded-cascode op-amp, including open-loop gain and phase margin of AC response. Table 4.1 shows simulation results of five process corners.

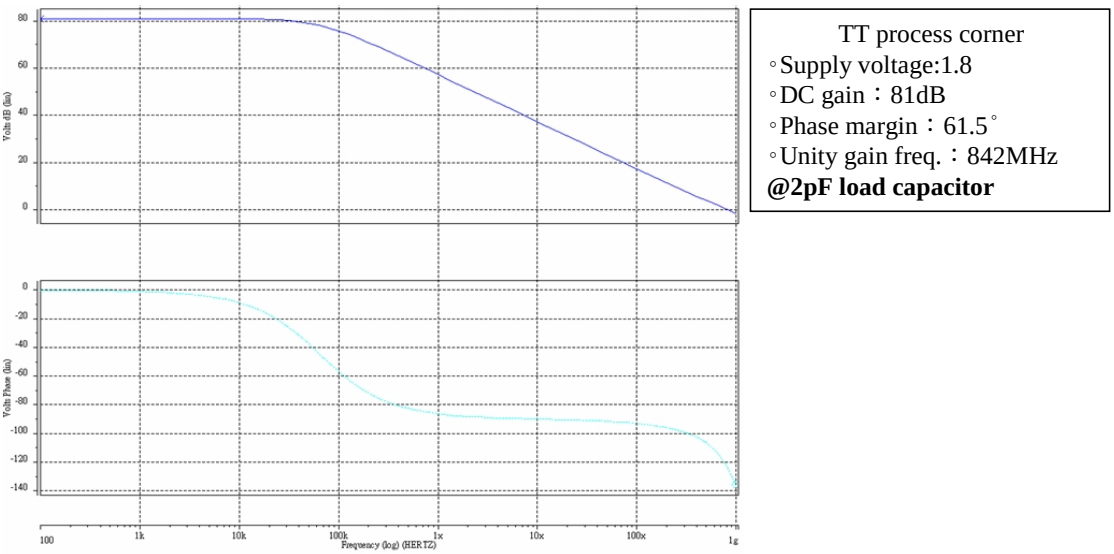


Figure 4.15 AC response simulation of the op-amp

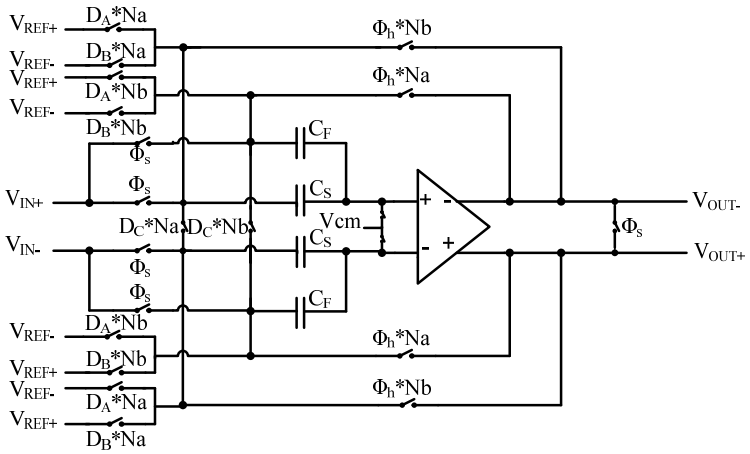
	TT	SS	FF	FS	SF
DC Gain(dB)	81	79.7	80.4	83.3	82.5
PhaseMargin(deg)	61.5	65.2	63.4	63.3	64.3
Unity GB(MHz)	842	796	822	813	810

Table 4.1 Simulation of the op-amp in five process corners

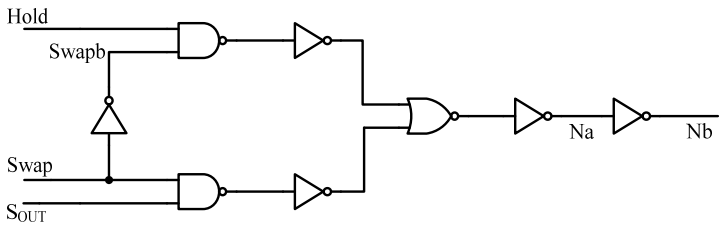
4.3.3 Random Capacitor-Swapping Multiplying-DAC

The principle and operation of conventional 1.5-bit/stage Multiplying-DAC (MDAC) had been illustrated in section 3.6.3. The capacitor-matching in MDACs is significant for stage accuracy, having powerful influence on whole ADC resolution. In this section, a new design and scheme of MDAC against capacitor-mismatch is shown in Figure 4.16(a). According to the idea introduced in section 3.7, we realize the random capacitor-swapping MDAC with a swapping-enable circuit which enables the ADC to perform capacitor-swapping randomly. The swapping-enable circuit is depicted in Figure 4.16(b), which has a function of

$$Na = Swap \cdot S_{OUT} + Swapb \cdot Hold \tag{4.41}$$



(a)



(b)

Figure 4.16 Random capacitor-swapping MDAC with (a) circuit implementation (b) swapping-enable circuit

In Figure 4.16(b), S_{OUT} represents the random output of the pseudo-random clock generator; *Hold* represents the phase of amplification in MDACs; *Swap* is the control signal which decides to perform random capacitor-swapping or not. When the applied Swap is high and thus Swapb (inverse of Swap) is low, the function of Equation (4.41) becomes $Na=S_{OUT}$. Therefore, capacitors C_F and C_S are swapped randomly depending on the S_{OUT} to be high or low. If Na=1 (Nb=0), C_F is in the feedback path; otherwise, if Na=0 (Nb=1), C_S is in the feedback path. Under this condition, the feedback capacitors are randomly swapped with the sampling capacitors in the MDAC of each Pipelined stage during the amplifying cycle of the ADC operation, which is the new method against the capacitor- mismatch effect to sustain overall ADC linearity. On the other hand, if Swap is low, the function becomes Na=Hold. Under this condition, C_F is fixed to be the feedback capacitor, so the operation is the same as the conventional architecture, whose linearity is vulnerable to the mismatch among capacitors. Note that Hold represents the phase of feedback in odd or even stages, so there are two swapping-enable circuits to meet two amplification phase. That is, we have two sets of swapping-enable circuits to control in odd and even stages respectively. The transient response simulation of MDAC is shown in Figure 4.17.

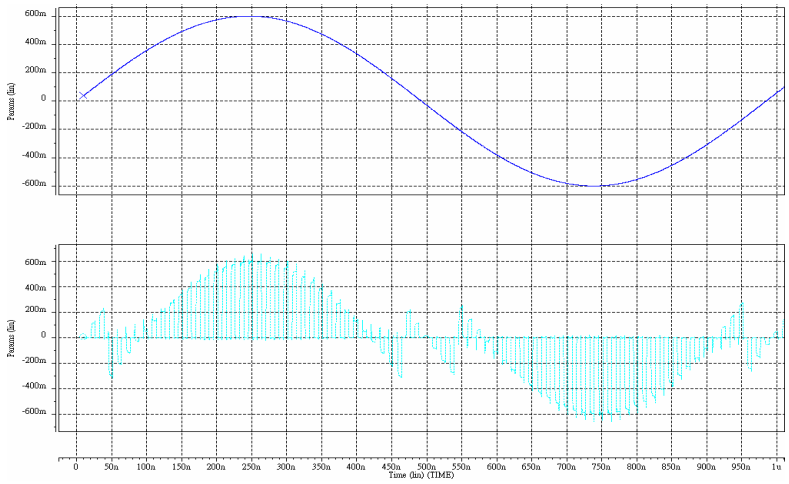


Figure 4.17 MDAC simulation result of input/output transient response

4.3.4 Low-Power Dynamic Comparator

The 1.5-bit/stage architecture allows a large error correction range for the comparator offsets of up to $\pm V_{REF}/4$. With a $1.2V_{P-P}$ dynamic range in differential mode, this redundant range is hundreds of milli-volts, which allows the use of dynamic latch-type comparators without preamplifiers to reduce the offset voltage [18][50]. In this ADC, a dynamic comparator having capabilities of low power, low offset, and high speed is adopted in 8 low resolution stages, as shown in Figure 4.18.

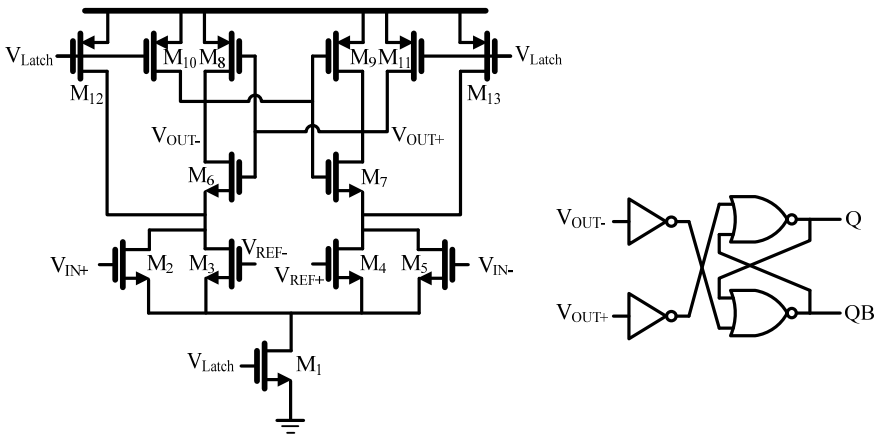
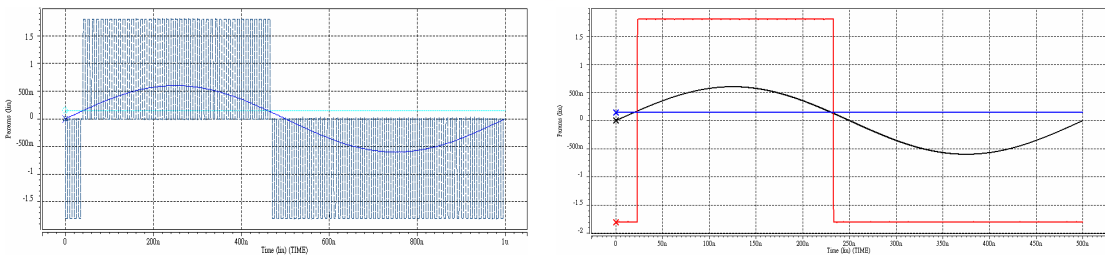


Figure 4.18 Low-power dynamic comparator

When V_{Latch} goes high, M_1 turns on and the cross-coupled input differential pairs M_2-M_3 and M_4-M_5 are biased. The input differential voltage is compared with the built-in threshold reference generated by $W_3/W_2*(V_{REF+}-V_{REF-})$, where $W_2=4W_3$ is designed for $+V_{REF}/4$. Then, the upper regenerative latches M_6~M_9 determine which of the outputs V_{OUT+} and V_{OUT-} goes to high (1) or low (0) in the two current paths M_6 and M_7. Furthermore, a SR latch is required at outputs to store data. When V_{Latch} goes low, M_{10}~M_{13} conduct and force both differential outputs to reset to VDD, where Q and QB are sustained. Note that conducting of M_{12} and M_{13} also makes the source of M_6 and M_7 to be VDD, and thus M_6 and M_7 are cut off. Therefore, there is no power dissipation when V_{Latch} is low [51]. Furthermore, all transistors M_1~M_5 are saturation in latching mode, which can be more insensitive to offsets resulting from devices mismatch, even though M_6 and M_7 are in triode region. The power and area are also reduced due to free of preamplifiers. Figure 4.19 shows simulation results with the threshold of $+V_{REF}/4$.



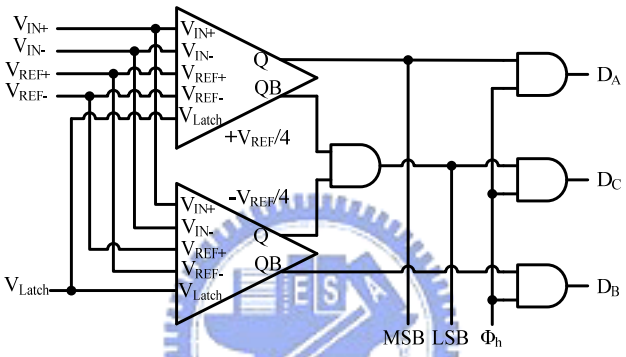
(a) (b)

Figure 4.19 Comparator simulation result (a) without SR latch (b) with SR latch

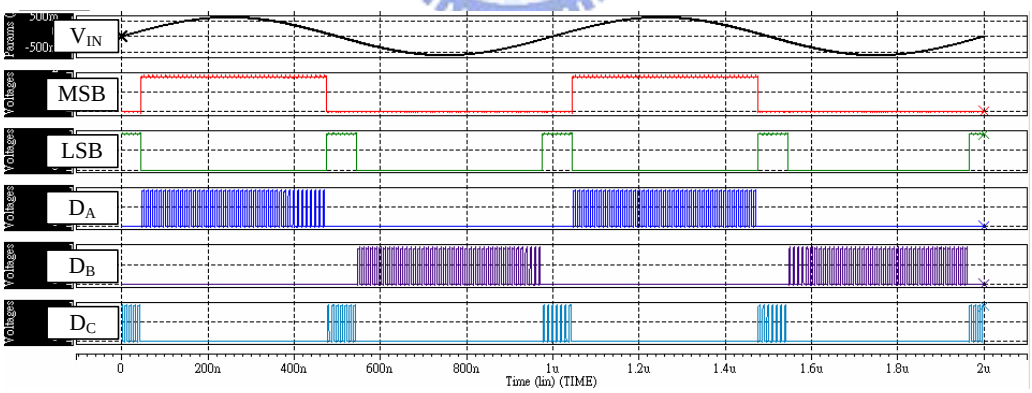
4.3.5 Flash Quantizers

Flash quantizers in first 8 Pipelined stages are 1.5-bit Flash ADCs of 1.5-bit/stage architecture, as shown in Figure 4.20(a). It consists of two

fully-differential comparators and some simple logic gates, and the threshold voltages of two comparators are $+V_{REF}/4$ and $-V_{REF}/4$ respectively, where $\pm V_{REF}$ are set to ±600mV. This 1.5-bit sub-ADC compares the differential input signal with above two decision levels and generates three possible codes of (00), (01), (10) according to the signal range. Figure 4.20(b) is the simulation result, where (D_A, D_B, D_C) are codes generated from (MSB, LSB) at amplifying phase Φ_h to control what level of reference to be connected in MDACs.



(a)



(b)

Figure 4.20 (a) 1.5-bit Flash Sub-ADC (b) Simulation result

The Flash quantizer in the last Pipelined stage is a typical 2-bit Flash ADC and is shown in Figure 4.21(a). It has three threshold value of $-V_{REF}/2$, 0, $+V_{REF}/2$ and four

possible output codes of (00), (01), (10), (11) depending on the signal range. The simulation result is shown in Figure 4.21(b).

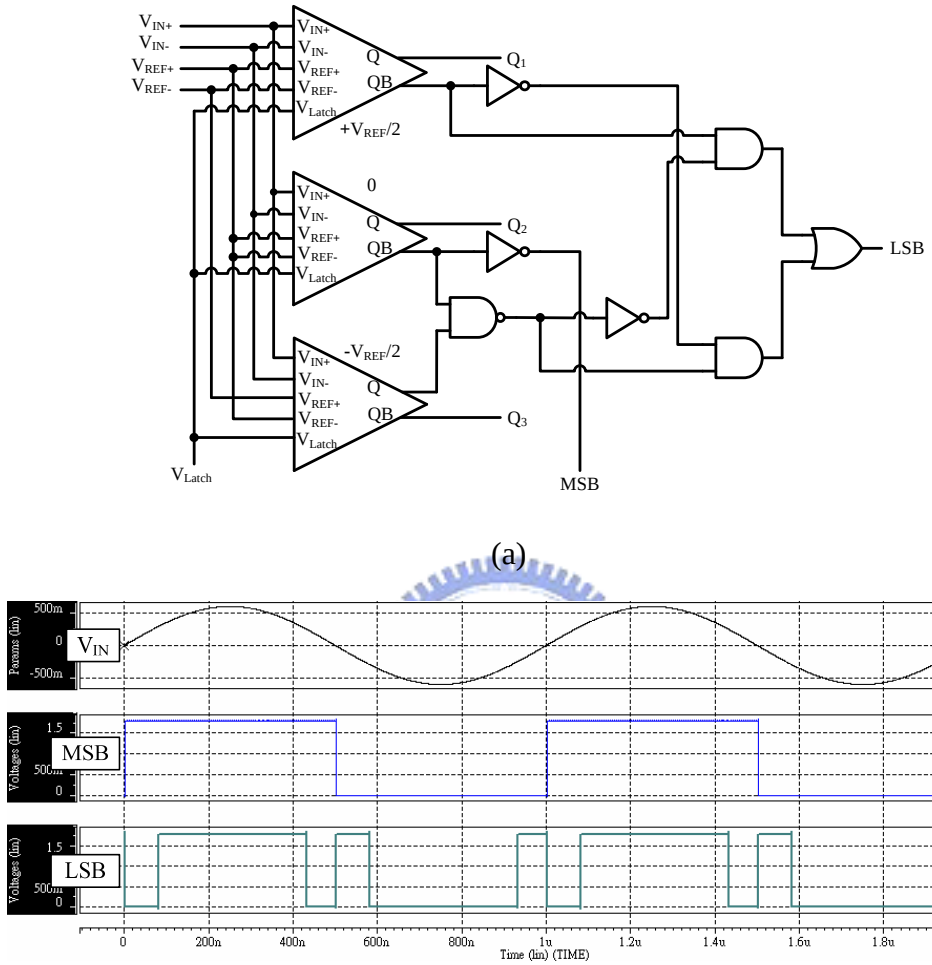


Figure 4.21 (a) 2-bit Flash Sub-ADC (b) Simulation result

4.4 Digital Circuitry

Digital circuitry includes delay elements for synchronization of stages output data and full adders for digital error correction, as shown in Figure 4.22.

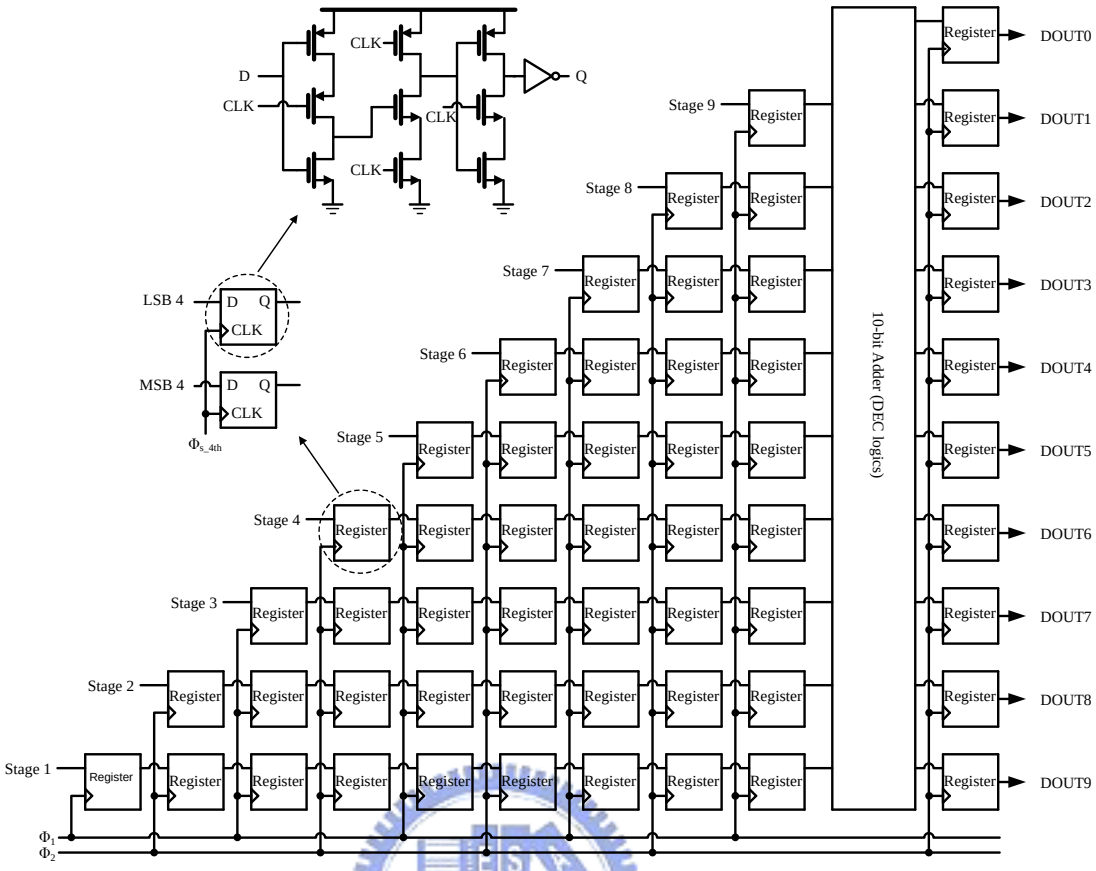


Figure 4.22 Shift register arrays and digital error corrections logics

From Figure 4.22, we can observe that the MSB and LSB of each stage are generated and fed into 9 sets of shift registers, which are different in delay time for 9 Pipelined stages. Then, asynchronous data bits from each of 9 stages are aligned to execute digital error correction, which simply adds and overlaps the aligned data bits by full adders to yield 10-bit effective codes (D_{OUT9},…..D_{OUT0}). A positive edge-triggered of single-phase clocked D-latch is adopted in the design of the shift register. Only one clock phase is required in the register, thus, the complexity of the register arrays can be reduced.

4.5 Two Non-Overlapping Clock Generator

The switched-capacitor realization of Pipelined ADC is mainly operated by two non-overlapping clock phase, which are generated by the scheme in Figure 4.23 [43]. The input clock, CLKIN, is inserted off-chip with the maximum frequency of 100MHz. Then, Φ_1 and Φ_2 respectively representing the sampling clock in odd stages and in even stages are generated. The purpose of non-overlapping period in Φ_1 and Φ_2 is to prevent the charge loss when both Φ_1 and Φ_2 are off. The other required phase Φ_{1a}(or Φ_{2a}) which has slightly earlier falling time, is also generated for reducing charge injection and leakage current of switches. To maximize the settling time, the rising edge of Φ_1 and Φ_{1a} is aligned, whereas the duration of non-overlapping is minimized. Note that buffers are added at each phase output to drive the load of capacitance in layout wires and MOSFET gates, and the number of logic gates can be optimized for better clock skew control. Finally, inverted phase of Φ_{1b} and Φ_{2b}, are also generated to control PMOS gates in CMOS switches.

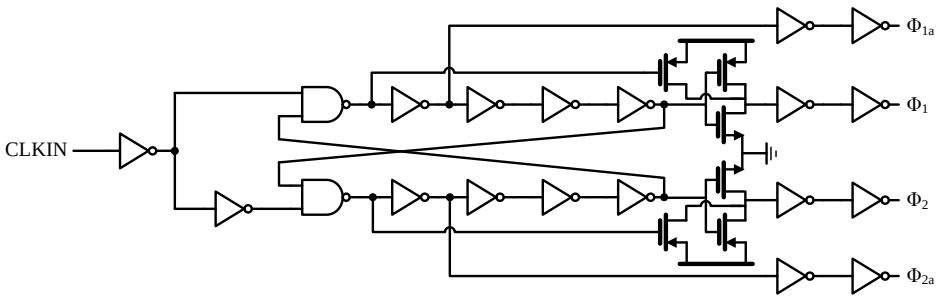


Figure 4.23 Multi-phase clock generator

Figure 4.24 shows the simulation result, where the rise and fall time are designed to be 0.1ns for 100MHz clock input, and the non-overlapping period is about 0.4ns.

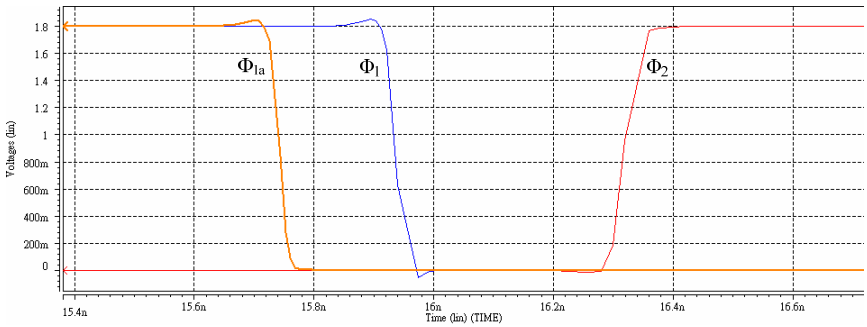
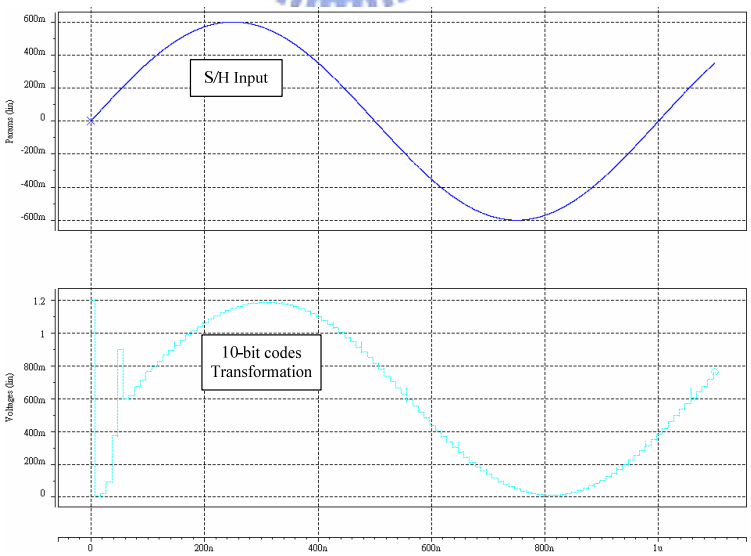


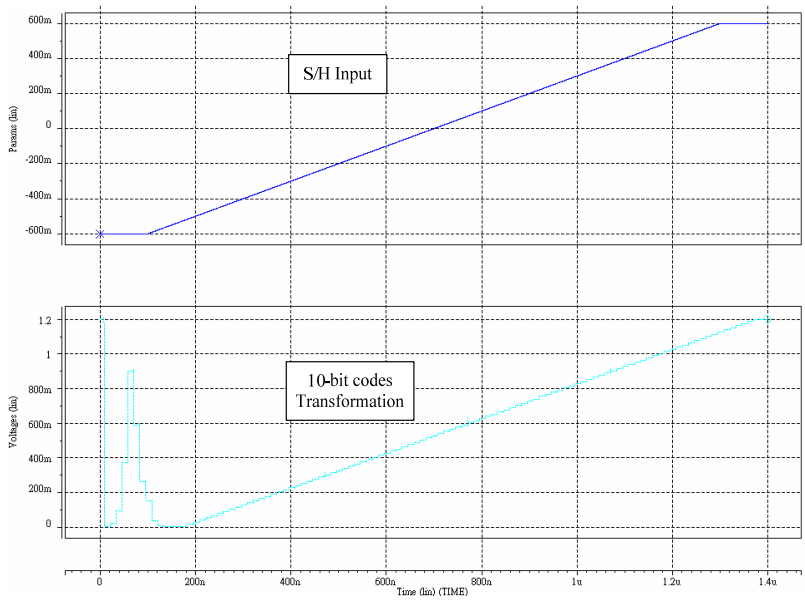
Figure 4.24 Simulation result of different clock phase

4.6 Simulation Results of Overall Pipelined ADC

Simulations results verifying functionality and performance of this 10-bit, 100MS/s random capacitor error-averaging Pipelined ADC are shown in this section. Through the ideal DAC simulation, 10-bit output codes are converted to analog signal, as shown in Figure 4.25, which are the recovered sinusoidal and ramp signal respectively.



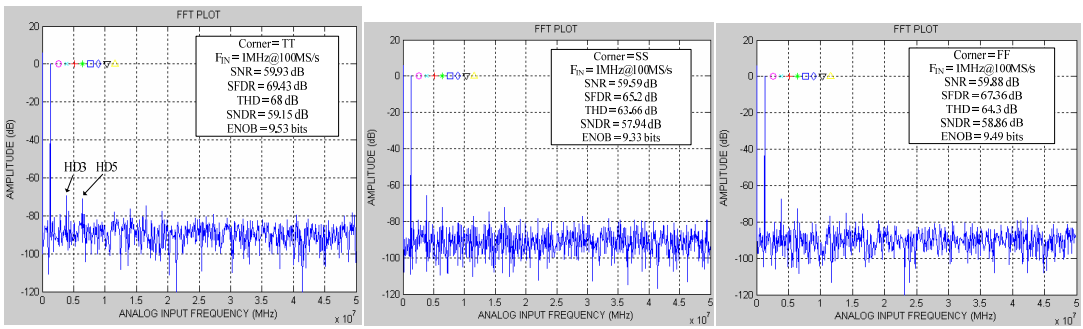
(a)



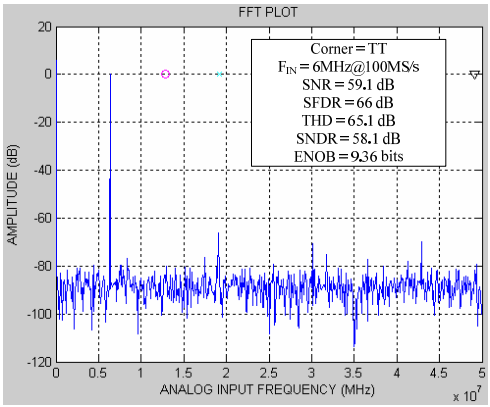
(b)

Figure 4.25 Transient response simulation with (a) sinusoidal (b) ramp input signal

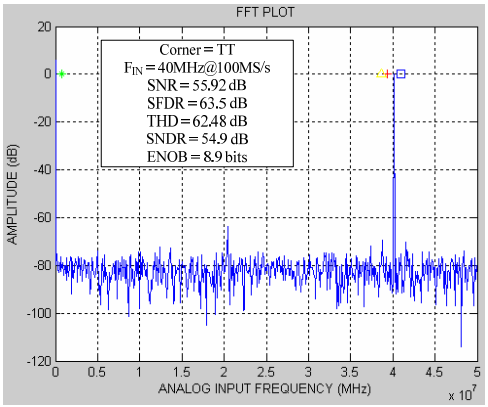
To analyze the linearity and noise effects of 10-bit output digital codes being simulated periodically with sinusoidal input, the obtained output data of 2^K points, where K usually equals 10,11,…16, are loaded into Matlab to execute fast Fourier transform (FFT). At 100MHz sampling rate, the FFT spectrums with different input frequencies are shown in Figure 4.26, which are analyzed by 1024 points output data.



(a-1) (a-2) (a-3)



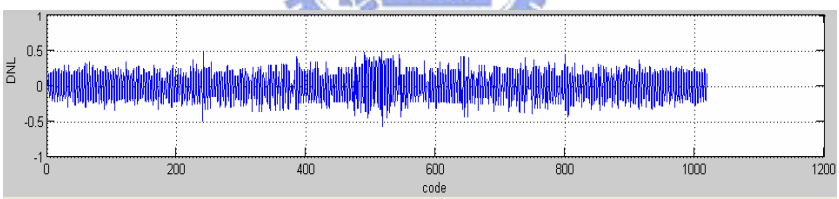
(b)



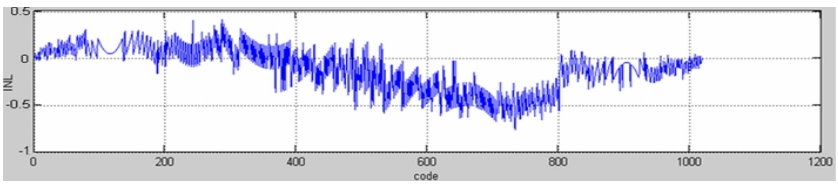
(c)

Figure 4.26 FFT spectrum of 10-bit output codes with (a) 1MHz (b) 6MHz (c) 40MHz sinusoidal input

The other performance characterizing the linearity of the ADC are DNL and INL, and simulation results are shown in Figure 4.27(a) and (b) respectively. The maximum DNL and INL are -0.55 LSB and -0.7 LSB.



(a)

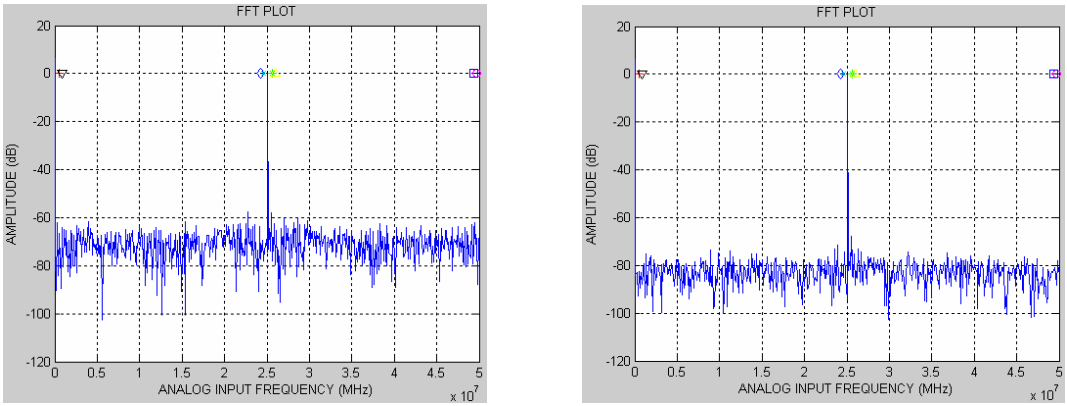


(b)

Figure 4.27 Simulation results of (a) DNL (b) INL

Furthermore, when we assume that there exists a 3% capacitor mismatch, we can observe that the linearity performance with capacitor-swapping (improved technique)

and without capacitor-swapping (conventional architecture) respectively, as shown in Figure 4.28. With intentional 3% capacitor mismatch, the ADC adopting the improved technique still sustain good linearity, but the performance of the conventional operation is deteriorated.



(a) (b)

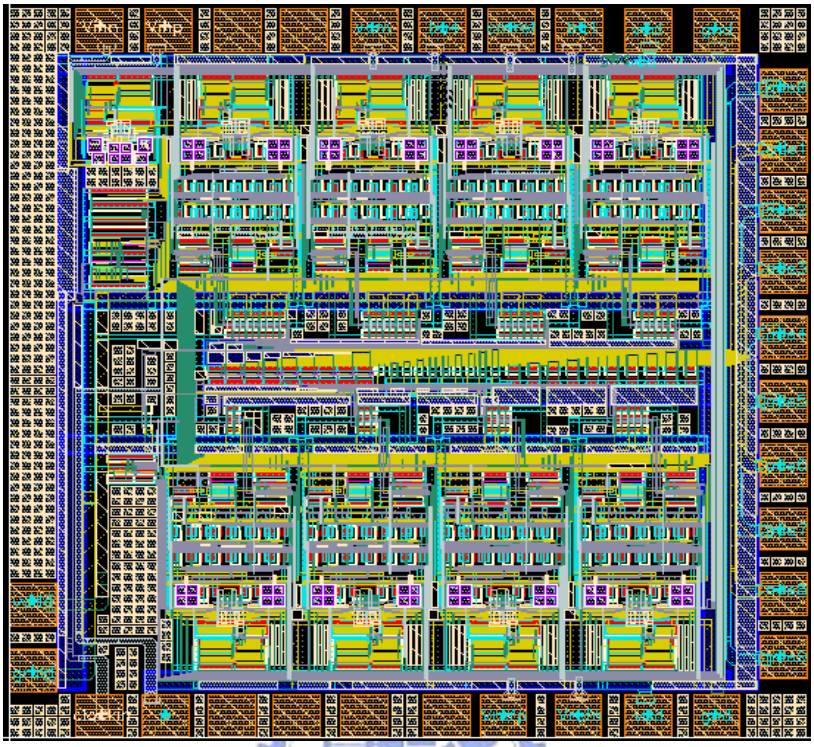
Figure 4.28 Linearity with 3% capacitor-mismatch (a) capacitor-swapping is OFF (b) capacitor-swapping is ON

Table 4.2 illustrates the improvement by the new technique, which is compared with the conventional work.

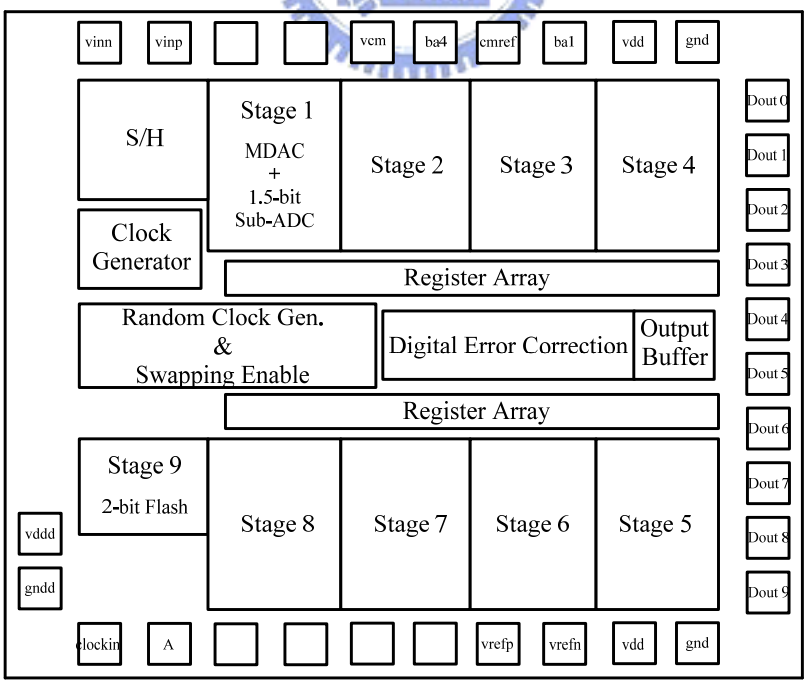
	Capacitor-swapping is ON (Swap=1)	**Capacitor-swapping is OFF (Swap=0)**
Capacitor error	3%	3%
Sampling rate	100MHz	100MHz
THD	66dB	55dB
SFDR@F_{IN}=25MHz	67.6dB	58dB
SNDR@F_{IN}=25MHz	55.8dB	42dB
ENOB	9-bit	6.7-bit

Table 4.2 Performance comparison between capacitor-swapping ON and OFF with 3% capacitor-mismatch

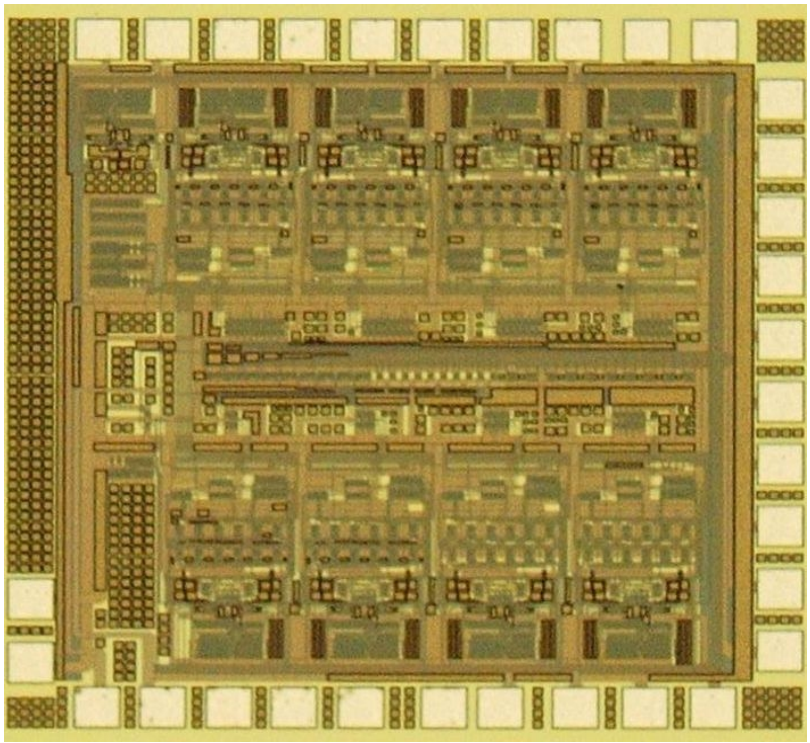
4.7 Layout and Floor Plan



(a)



(b)



(c)

Figure 4.29 (a) Layout (b) Floor plan (c) Die photograph of the whole chip

The layout of this experimental prototype chip is shown in Figure 4.29(a), which occupies die area of 1.365mm × 1.368mm and consumes total power of 88mW. In the layout, we use the mirror symmetry to enhance the rejection of common mode noises in the fully differential circuits. Analog circuits are separated from the digital circuit, which are powered from the separated power supply. Figure 4.29(b) and (c) are the die photograph and floor plan respectively. Table 4.3 summarizes the simulation results of this prototype ADC.

Parameters	Simulation Results
Process	TSMC 0.18μm CMOS Mixed-Signal
Supply Voltage	1.8 V
Input Range	±0.6V Fully differential
Resolution	10 bits
Operation Frequency(max)	100 MHz
DNL(max)/INL(max)	-0.55 LSB /-0.7 LSB
SNDR@F_{IN}=1MHz	59.15 dB
ENOB@F_{IN} =1MHz	9.53 bits
Chip Size	1.87mm^2
Power Dissipation	88mW

Table 4.3 Simulation summary of this prototype ADC

4.8 Summary

In this chapter, the design process of the whole ADC, including circuit optimization, simulation, and layout are illustrated in detail. However, some effects can not be revealed in Hspice simulation; that is, after fabrication of the chip, matching property of input differential pairs and capacitors may be lost due to process variation, and there also exists a problem of parasitic capacitance due to metal wires. Furthermore, when measuring the chip, noises from outside environment should be considered, which is treated as thermal noise and can not be known in simulation results of Hspice.

Chapter 5

Testing Setup and Measurement Results

5.1 Introduction

The Pipelined ADC with capacitor-mismatch calibration had been fabricated by TSMC 0.18um 1P6M CMOS Mixed-Signal process. In this chapter, the testing environment including the printed circuit board (PCB) and required instruments for measurement are shown. Finally, the measurement results are also presented and summarized.

5.2 PC Board Design and Testing Setup

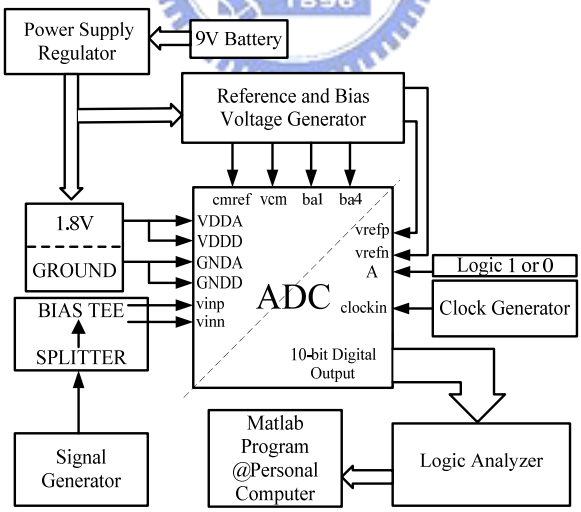


Figure 5.1 Testing setup on PCB

First of all, the design of PCB is important, which also influences the performance of the testing chip. The scheme of testing setup used to evaluate the ADC performance in this work is depicted in Figure 5.1, which mainly consists of the

power supply regulator, the reference and bias voltage generator, the signal generator, the clock generator, and the logic analyzer.

The supply voltages 1.8V for both analog and digital parts of this testing chip are generated by the regulator shown in Figure 5.2, which is named as the LM317 adjustable regulator [52][53][54]. The input voltage of this regulator is connected to a 9V battery for smaller noise disturbance, and the output voltage is specified with 1.8V, which is adjusted by the resistor R_1 as

$$V_{OUT} = 1.25 \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1 \tag{5.1}$$

, where I_{ADJ} is the DC current that flows out of the adjustment terminal ADJ of the regulator.

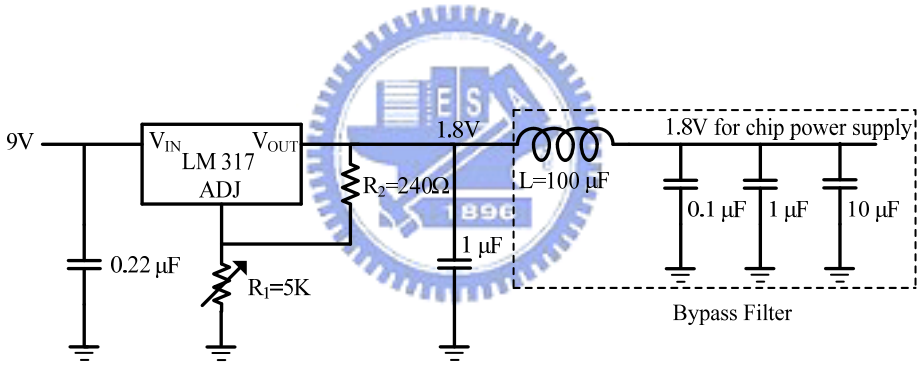


Figure 5.2 Power supply regulator with bypass filter

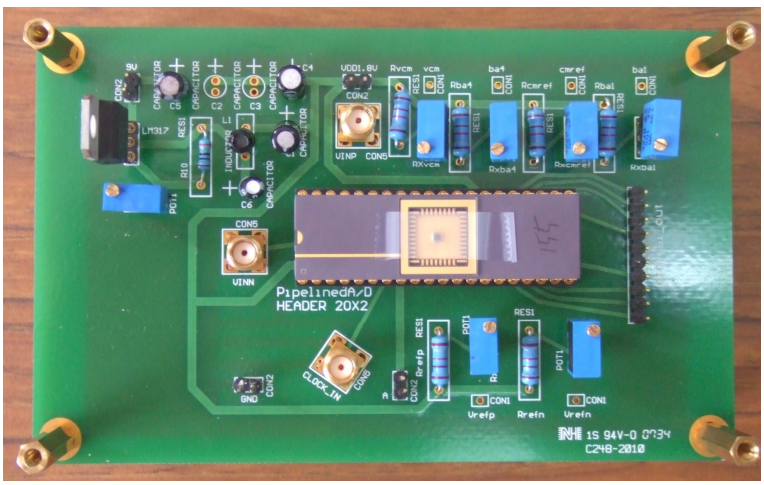


Figure 5.3 Photograph of the testing ADC on PCB

Furthermore, the output of the regulator should connect different sizes of capacitors to bypass noises. The required DC voltages including bias, common-mode voltage, and reference voltages are generated through small resistors dividing 1.8V at regulator output. Figure 5.3 shows the photo of the PC board with the testing chip.

After completing PCB design, we then apply all signal sources to this testing ADC. The single-ended input signal is provided by the function generator, Agilent 33250A, which is shown in Figure 5.4(a). A single to differential device called SPLITTER is used to generate differential signals. Two DC couple devices called BIAS TEE are connected with two outputs of SPLITTER to add DC bias on differential signals. Figure 5.4(b) and (c) show the SPLITTER and BIAS TEE respectively. The required clock signal is generated by a pulse/pattern generator, Agilent 81130A, which is shown in Figure 5.5. The 10-bit output data is primarily captured and stored with 65536 points in the logic analyzer, Agilent 16702B, which is a window based instrument and is shown in Figure 5.6. Finally, the stored data is processed and analyzed by the Matlab program in the personal computer.

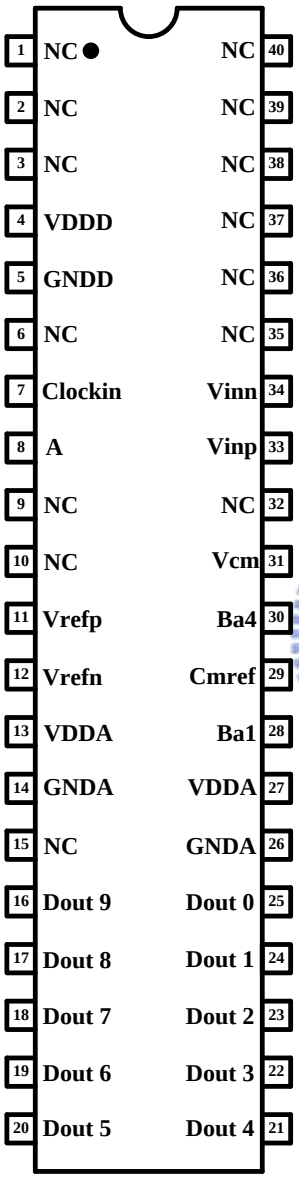
(a) (b) (c)

Figure 5.4 (a) Function/arbitrary waveform generator (b) SPILLTER (c) BIAS TEE

Figure 5.5 Pulse/pattern generator

Figure 5.6 Logic analyzer

Figure 5.7 presents the pins configuration and assignments of this experimental Pipelined ADC.

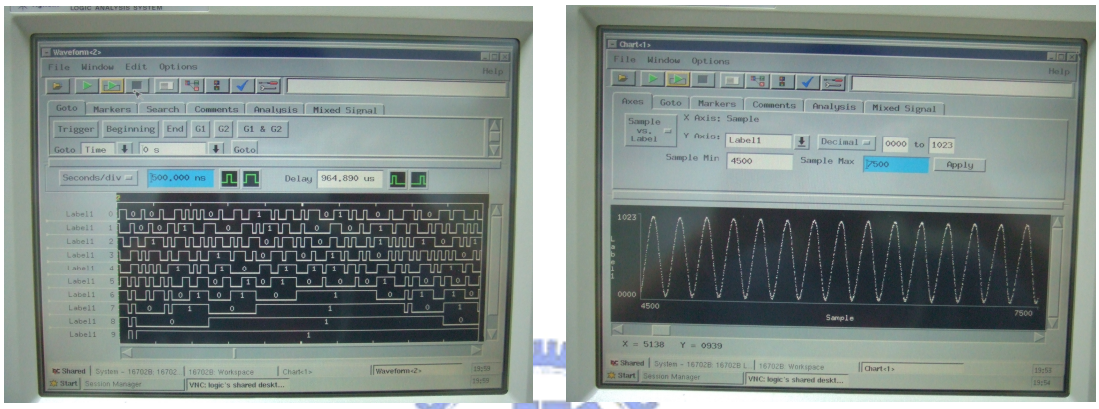


Pin	Name	I/O	Description
1	NC	-	No connection
2	NC	-	No connection
3	NC	-	No connection
4	VDDD	In	Digital power supply
5	GNDD	In	Digital ground
6	NC	-	No connection
7	Clockin	In	System clock input
8	A	In	Logic 1 or 0
9	NC	-	No connection
10	NC	-	No connection
11	Vrefp	In	Reference voltage＞Vcm
12	Vrefn	In	Reference voltage＜Vcm
13	VDDA	In	Analog power supply
14	GNDA	In	Analog ground
15	NC	-	No connection
16	Dout 9	Out	Digital data output
17	Dout 8	Out	Digital data output
18	Dout 7	Out	Digital data output
19	Dout 6	Out	Digital data output
20	Dout 5	Out	Digital data output
21	Dout 4	Out	Digital data output
22	Dout 3	Out	Digital data output
23	Dout 2	Out	Digital data output
24	Dout 1	Out	Digital data output
25	Dout 0	Out	Digital data output
26	GNDA	In	Analog ground
27	VDDA	In	Analog power supply
28	Ba1	In	Bias voltage
29	Cmref	In	Common-mode voltage
30	Ba4	In	Bias voltage
31	Vcm	In	Common-mode voltage
32	NC	-	No connection
33	Vinp	In	Input signal (+)
34	Vinn	In	Input signal (-)
35	NC	-	No connection
36	NC	-	No connection
37	NC	-	No connection
38	NC	-	No connection
39	NC	-	No connection
40	NC	-	No connection

Figure 5.7 Pins configuration and assignments

5.3 Measurement Results

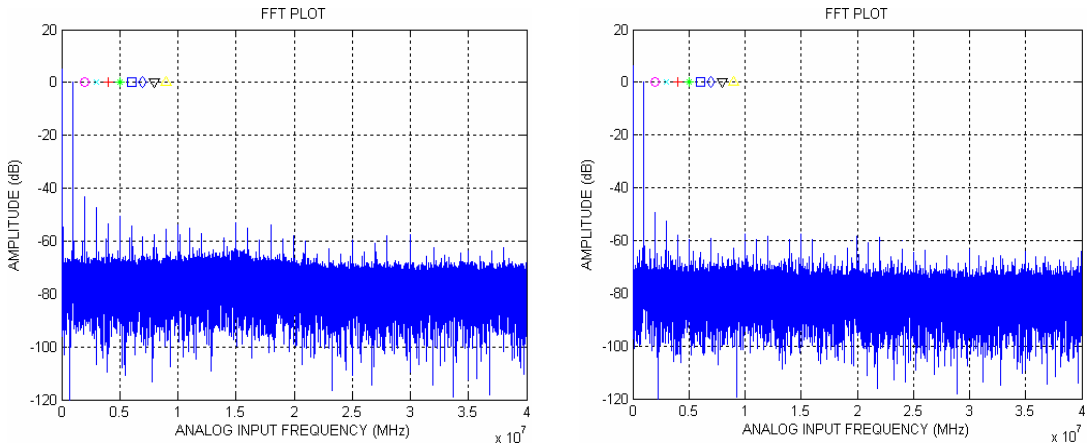
First, the measured 10-bit output data of this testing ADC is captured and stored by the logic analyzer. Figure 5.8(a) and (b) show the presented 10-bit codes and the decimal-recovered chart when applying a differential sinusoidal input signal.



(a) (b)

Figure 5.8 Measured results of (a) 10-bit codes (b) decimal-recovered sine wave

From the measured time-domain results shown in Figure 5.8, the frequency-domain showing linearity is calculated by collecting 65536 samples of the input signal and performing a 65536-point fast Fourier transform (FFT). At the sampling rate of 80MHz with 1MHz sinusoidal input, Figure 5.9(a) and (b) show the linearity comparison of capacitor-swapping off and on illustrated in the section 4.3.3. When we apply logic 0 to this testing ADC, the operated conventional work shows peak SFDR of 43.2dB and peak SNDR of 33.57dB in Figure 5.9(a); when we apply logic 1, the capacitor-swapping operation of MDACs is enabled, hence, the better peak SFDR of 50dB and peak SNDR of 42.73dB is shown in Figure 5.9(b) than the conventional work.



(a) (b)

Figure 5.9 Comparison of FFT spectrum between (a) conventional operation and (b) capacitor-swapping operation

From Figure 5.9, we can know that harmonic distortions are mainly caused by the non-linearity effects of actual circuits. The worst reason is that the DC gain of op-amps at the highest output swing is no longer large enough to meet the required specification. Besides, the charge injection of signal-dependent error and the drift of common-mode which will accumulate stage by stage are also the possible reasons. Finally, even-order harmonics should be suppressed for the differential topology while the 2^{nd} harmonic is larger than the 3^{rd} harmonic in the measured FFT spectrums. We find that this phenomenon results from the mismatch of input differential signals, which is because the applied input signal from the instrument has slight distortion and imperfect differential property, and furthermore the process variation of input differential devices also leads to the match issue, even though the layout skill of common-centroid had been used. In Figure 5.10, the measured SNDR with different sampling frequencies and input frequencies F_{in} are shown, and the maximum operation frequency is 100MHz with capacitor-swapping operation.

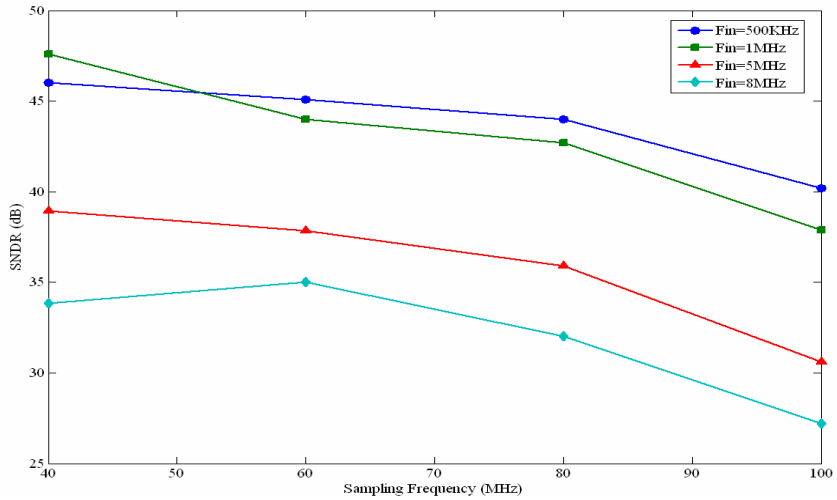


Figure 5.10 The measured SNDR against the sampling frequency

5.4 Summary

Table 5.1 summarized the measured results of this ADC with the innovative MDAC.

Parameters	Measured Results
Process	TSMC 0.18μm CMOS Mixed-Signal
Supply Voltage	1.8 V
Input Range	±0.6V Fully differential
Sampling Frequency	80 MHz
SNDR@F_{IN}=1MHz (Capacitor-Swapping)	42.73 dB
ENOB (Capacitor-Swapping)	6.81 bits
SNDR@F_{IN}=1MHz (No Capacitor-Swapping)	33.57 dB
ENOB (No Capacitor-Swapping)	5.28 bits
Chip Size	1.87mm^2
Power Dissipation	88mW

Table 5.1 Summary of measured results of this testing chip

Chapter 6

Conclusions

6.1 Conclusions

Among numerous architectures of CMOS ADC, the Pipelined ADC is the most popular solution for its capability of medium-accuracy/high-speed or high-accuracy/ high-speed. Furthermore, the CMOS and SC implemented Pipelined ADC makes the integration of digital/analog circuits on the same chip with the same supply voltage to be easy, even for the SoC. In this thesis, a 10-bit, 100MS/s Pipelined ADC with 1.8V power supply had been designed, laid-out, fabricated, and measured completely. There are many non-idealities in actual circuit implementations and we consider these effects with design. The front-end S/H with precharged technique is employed for reducing requirements of the op-amp; the 1.5-bit/stage architecture with the digital error correction is adopted for tolerating comparators offsets. With the innovative technique of capacitor-mismatch calibration, the role of the feedback capacitor in MDACs is no longer fixed, which averages out the capacitor-mismatch errors and improves overall ADC linearity. All approaches mentioned above are desired for less power consumption and die area, higher conversion speed and resolution accuracy.

This testing chip was fabricated by TSMC 0.18um 1P6M CMOS process technology. For 1MHz input signal frequency, the measured SNDR is 44dB at 60MHz sampling rate, 42.7dB at 80MHz sampling rate, and 37.88dB at 100MHz sampling rate. The measured results of the maximum conversion rate are worse than the simulation, because there are many extra parasitic capacitors that the post-layout extraction didn’t extract out, and the measuring skills are not good enough, as well as

other reasons like the instruments issue and the high frequency effects that need to discover and discuss. Furthermore, when measuring the chip, the applied input signal itself already has distortions due to instruments and devices interference, which is especially sensitive to the signal wire of clock. Therefore, when designing the PCB, we must consider and take care of the problem of clock disturbances to the input signal, which is more severe for higher frequency of clock or input signal.

6.2 Future Works

Nowadays, the trend of Pipelined ADC design is toward the direction of higher resolution, faster speed, lower power consumption, and smaller chip area. As the scaling process technology, the reduced supply voltage brings benefits to digital circuits whereas makes the design of analog circuits more difficult.

For higher resolution accuracy, although a wide variety of calibration methods had been proposed and we can develop to implement, few of them can be operated with high conversion rate exceeding 100MHz due to an extra clock cycle for calibration. For faster conversion speed, a method of time-interleaved which can compensate the speed constraint of the op-amp can be adopted by combining more parallel channels instead of single channel, while matching issues, such as timing skew in multiple channels are the indispensable problem to increase the sampling rate much greatly.

Finally, with the reduced supply voltage, we have to do more efforts to achieve high accuracy and low power at the same time. In order to reduce total power consumption, scaling down of the capacitors stage by stage will be necessary. Therefore, the design spec. combining high speed and high resolution of an ultra low power ADC will become the most significant topic and have more challenges for the future work.

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