國 立 交 通 大 學

電信工程學系

碩 士 論 文

雙向放大器之實現與改善暨
主動式混頻器與被動式分離器之整合

Implementation and Improvement of Bi-directional Amplifier
and
Active Mixer with an Integrated Passive Balun

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摘　　要

本論文分為雙向放大器與 90° hybrid及混頻器三個部份。利用標準 TSMC 0.18μm RF CMOS 製程完成本論文中所設計的電路。

第一部份描述應用在回波式天線陣列的雙向放大器之分析與設計。此雙向器據有不須使用切換器或控制電壓方向即可達到雙向放大之功用，它包含了兩個反射式放大器與一個 90° hybrid。此雙向放大器可達增益為 11dB，S11<-10dB，功率損耗為 9mW。

第二部份描述設計一個縮小化 90° Hybrid以改善第一部份利用集總原件設計的 90° hybrid。使用主動式電感取代一般電感可降低面積的損耗及增加品質因子，另一個優點可以增加可調範圍使其在 5~6GHz頻段皆可使用。量測結果 S11<-10dB、S21 為-4dB、S31 為-2dB、S41< -15dB，相位差為 94~100 度。

最後一部份是主動混頻器與被動式分離器之整合，所設計的重點在於微小化的被動式分離器，利用並聯電容方式使耦合線縮短長度並且在電容與耦合線共振時可增加兩個極點，模擬結果 CG 為 11.7 ± 0.6 dB、IIP3 為-3.7 dBm、P-1dB 為-11 dBm、功率損耗為 5mW

Implementation and Improvement of Bi-directional Amplifier and Active Mixer with an Integrated Passive Balun

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ABSTRACT

The thesis consists of three parts: bi-directional amplifier and quadrature hybrid and mixer. These proposed circuits are fabricated using a standard TSMC 0.18μm RF CMOS process technology.

The first part of the thesis describes the design and analysis of a bi-directional amplifier for retro-directive antenna. A modified bi-directional amplifier is used to amplify the signals coming from both ports without any switch or controlled voltage. It contains two identical reflection-type amplifiers and a 3-dB quadrature hybrid. The achieved gain is 11dB , return loss is under -10dB, and the power consumption is 9mW.

Since the lump element of quadrature hybrid cost more area, the second part is the design of miniaturized quadrature hybrid. By employing the active inductors, the area can be reduction in this design and the quality factor can be improved. And another advantage of this design is the tuning range from 5GHz to 6GHz. The measurement S11 is under -10dB, S21 is about -4dB, S31 is about -2dB, S41 is under -15dB and the phase difference between S21 and S31 is $94^\circ \sim 100^\circ$.

The finally part is the design of an active mixer with miniaturized balun. It focus on the design of the miniaturized balun, applied in the integration of mixer. By adding two capacitors, the coupled lines length can be reduced and two poles induce because of the coupled resonators. The simulation results of proposed mixer achieves power conversion gain of 11.7 ± 0.6 dB, IIP3 of -3.7 dBm, and P-1dB of -11 dBm in the power consumption of 5 mW.

Acknowledgements

從對於射頻電路一知半解到現在順利完成畢業，研究所兩年的學習過程，衷心的感謝指導教授鍾世忠博士指導，提供我一個很優質的研究環境學習成長，除了相當充足的資源，感謝指導教授在這兩年內給予非常大的自由度，並且在廣大的思考空間內不斷的指引正確的方向，使我在高頻晶片設計領域獲益良多。也衷心地感謝口試委員孟慶宗教授、郭建男教授以及張志揚教授，能在百忙之中抽空前來，給予論文上的指導與建議，讓我受益良多，也使論文更為完備。

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最後最感謝我的家人，從不給我壓力讓我無後顧之憂地完成學業與研究，親愛的爸爸、媽媽，還有一直很疼我的哥哥、姊姊，謝謝你們的支持、關懷、與無怨無悔的付出。謹以此論文獻給所有幫助過我與關心我的人。

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Chapter 1 *Introduction*

1.1 Motivation

Recently the wireless communication becomes more and more popular. The wireless communication systems must be portable, low cost, high performance, highly integration, low power and small size. All of these constraints combine to make the design quite challenging. One approach to reach the requirements for wireless communication is CMOS technology. The CMOS circuits have many drawbacks such as noisy and low current driving capability. But with the rapid scaling of CMOS process technologies, it has dramatically improved CMOS performance and achieving frequency of gigahertz. In addition, CMOS offers low power and highly integration. For these reasons, many papers of CMOS RF circuits have been published. Based on the CMOS RFIC advantages of integrated with baseband circuits, more transceiver circuits are realized by using CMOS process. Therefore, CMOS RFIC becomes a new trend for the wireless communication system.

The goal of this thesis is to research the radio frequency circuits in CMOS process technology. In this thesis, we focus on bi-directional amplifier, quadrature hybrid, and mixer. A modified bi-directional amplifier is used to amplify the signals coming from

both ports without any switch or controlled voltage. The main problem of quadrature hybrid is to reduce chip size. We will describe how to improve it in later chapters. Mixer has played an important role in wireless communication receivers. A modified passive balun, used to reduce balun size and power consumption, is integrated with mixer.

1.2 Thesis Organization

This thesis is organized into 6 chapters. It was devoted to the implementation and improvement of bi-directional amplifier and active mixer with an integrated passive balun. This chapter is the first one and introduces the motivation of the research and the arrangement of this thesis. In Chapter 2, we will introduce the fundamentals of bi-directional amplifier, quadrature hybrid, and mixer with passive balun. Chapter 3 is a main chapter that has the implement of the bi-directional amplifier. This chapter encompasses the detailed analysis of the proposed circuits. The simulation and measurement results will be included. Chapter 4 is improving on the design of reducing the quadrature hybrid size. Also, the simulation and measurement results will be included. Chapter 5 is focus on the design of the miniaturized balun, applied in the integration of mixer. The simulation results will be included. At last, the conclusion is made in chapter 6.

Chapter 2 *General Backgrounds*

In this chapter, we will introduce the fundamentals of retro-directive antenna, basic amplifier architecture, direct conversion receiver, and mixer.

2.1 Retro-directive Antenna

Retro-directional antenna arrays are applied in many wireless communication systems, such as RF identification apparatuses and intelligent transport systems [1]-[4]. These kinds of antenna systems can reflect the received signals along the incident direction without any portended signals as shown in Fig. 2.1.

There are two familiar categories of retro-directional antennas. One is the type of phase-conjugated-array elements; the other is the form of Van Atta arrangement [5]. The former antenna has to connect an oscillator on each unit cell in order to form the

conjugated phase. Therefore, the reflection-type waveform transports along the incident way by this approach. The advantages of this antenna are that the distance between random unit cells can be the same. And it is able to modulate readily the reflected signals by modifying the operating frequency of oscillators. Nevertheless, the frequent difference between the RF and LO signals of each oscillator must be large extremely. This shortcoming will make the antenna system much complex and expensive. The antennas of Van Atta arrangement have to let each unit cell symmetrize to the central point. And two unit cells are connected by simple microwave transmission line. The framework of the antenna of Van Atta arrangement is shown in Fig. 2.2(a). The corresponding electric field in the incident direction is $E_{Passive}(\theta) = C \cdot N \cdot F^2(\theta)$, where C is the constant value which has relations with the distance of a signal source and the strength of an incident waveform, N is the amount of antennas in the array and F(θ) is the pattern of each unit cell. For the sake of improving the strength of the radiating field, the transmission line can be replaced by an active amplifier, as shown in Fig. 2.2(b) and Fig. 2.2(c). The architecture in Fig. 2.2(b) only has a half of antennas in the array to receive the incident waveform due to utilizing a unilateral amplifier. This kind of antennas possesses the corresponding field $E_{Uni-amp}(\theta) = C \cdot N/2 \cdot G \cdot F^2(\theta)$, where G is the gain of a unilateral amplifier. If the architecture adopts a bi-directional amplifier, each unit antenna can be used to receive and transmit a signal, which field is $E_{Bi-amp}(\theta) = C \cdot N \cdot G \cdot F^2(\theta)$. Compared with two architectures, we can acquire a conclusion that the reflected power level of a system which adopts a bi-directional amplifier has 6dB much than the one with a unilateral amplifier. Similarly, when two antennas are designed to have the same reflected power level, the system which utilizes a bi-directional amplifier can reduce the half amount of unit antenna cells.

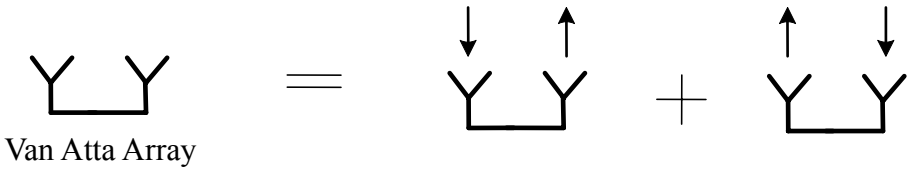

Fig. 2.1 The principle of Van Atta Array

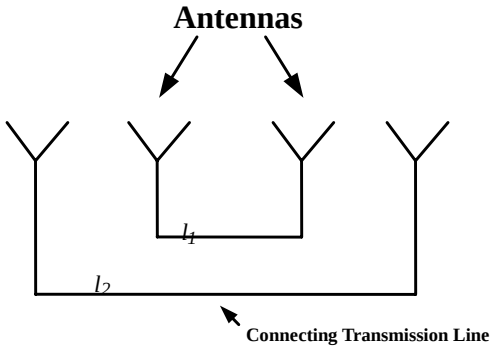

Fig. 2.2(a) Passive Van Atta retro directive array

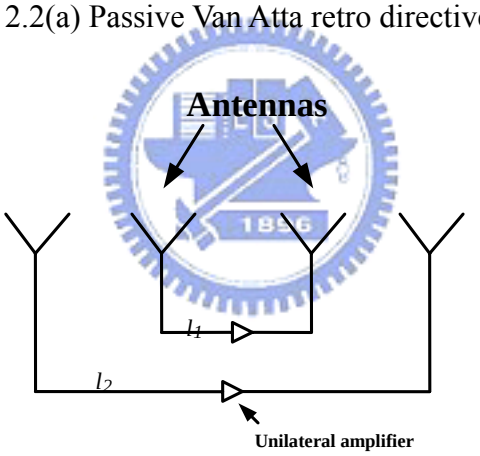

Fig. 2.2(b) Active Van Atta retro directive array with unilateral amplifier

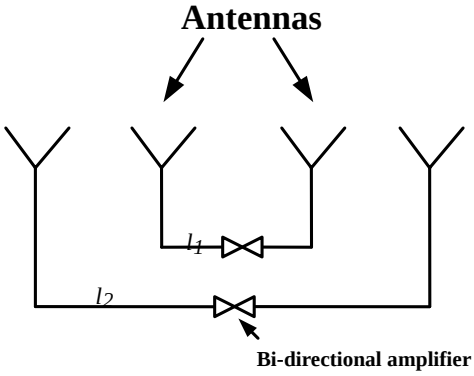

Fig. 2.2(c) Active Van Atta retro directive array with bi-directional amplifier

2.2 The Basic Microwave Transistor Amplifier

This section develops some basic principles used in the analysis and design of microwave transistor amplifier. Based on the S parameters of the transistor and certain performance requirements, a systematic procedure is developed for the design of a microwave transistor amplifier.

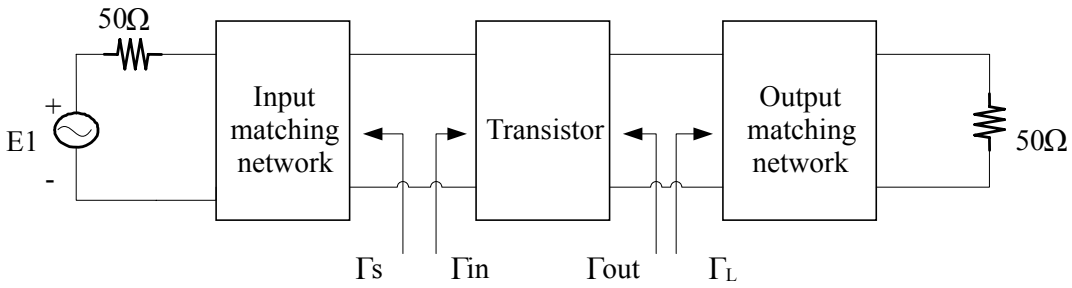

Fig. 2.3 Transistor amplifier block diagram

2.2.1 Power Gain Equations

The transducer power gain G_T, the power gain G_P, and the available power gain G_A are defined as followes:

$$G_T = \frac{P_L}{P_{AVS}} = \frac{1-|\Gamma s|^2}{|1-\Gamma in\Gamma s|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma L|^2} \tag{2.1}$$

$$G_P = \frac{P_L}{P_{in}} = \frac{1}{1-|\Gamma in|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma L|^2} \tag{2.2}$$

$$G_A = \frac{P_L}{P_{AVS}} = \frac{1-|\Gamma s|^2}{|1-S_{11}\Gamma s|^2}|S_{21}|^2 \frac{1}{1-|\Gamma out|^2} \tag{2.3}$$

2.2.2 Stability Consideration

The stability of an amplifier, or its resistance to oscillate, is a very important

consideration in a design and can be determined from the S parameters, the matching networks, and the terminations. The two-port network shown in Fig. 2.3 is said to unconditionally stable at a given frequency if the real parts for Zin and Zout are great than zero for all passive load and source impedances. If the two-port is not unconditionally stable, it is potentially unstable. That is, some passive load and source terminations can produce input and output impedances having a negative real part.

2.3 The Direct Conversion Receiver

Because of the rapid growth in demand for broadband wireless communications, wireless local area networks (WLAN) are becoming more attractive not only to exchange large amount of data locally but also as access points for the cellular infrastructure. The superheterodyne has been the architecture of choice for wireless transceivers for many years. On the other hand, due to the increase of the integration level of RF front-ends, alternative architectures, targeting reduced power consumption and minimization of the number of off-chip components, have been considered, in the recent past. Among them, the direct conversion receiver (DCR) or zero-IF receiver has increasingly gained widespread attention due to its potentially of low power consumption, lower complexity, low manufacturing costs, and easy integrating with the baseband circuits [6]-[9]. Fig. 2.4 shows the block diagram of the direct conversion RF front-end, where the LO frequency is equal (or approximate) to input carrier frequency and the LO will translate the center of the desired signal to zero IF or low IF.

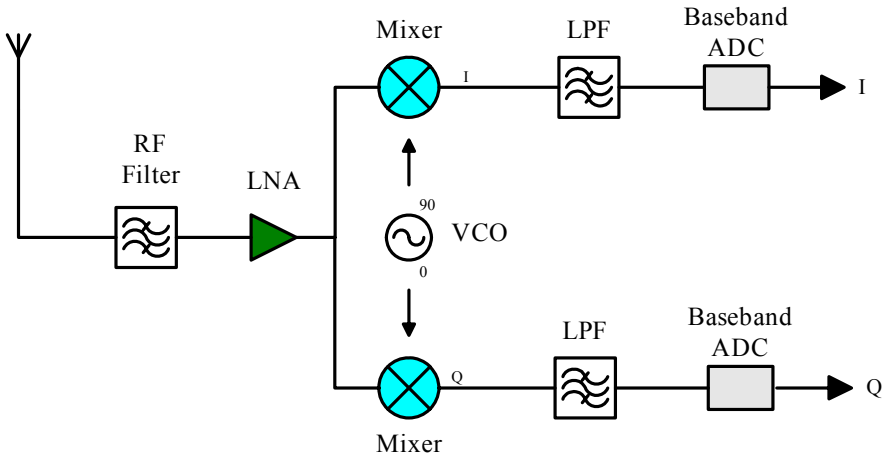

Fig. 2.4 Block diagram of direct conversion receiver architecture

The most important advantage of the direct conversion receiver is that the intermediate frequency (IF) passband filter can be neglected and replaced by a low pass filter. Low pass filter is much easier to integrate in standard semiconductor technology. However, some issues which do not exist or are not serious in the heterodyne architecture become critical in the direct conversion receiver. These drawback include DC offset, flicker noise, even order distortion, I/Q mismatch, and so on. Among these the DC offset generated by self-mixing is the most critical. The DC offset is caused by carrier leakage from the local oscillator to the mixer input and to the antenna as shown in Fig. 2.5 Interferer leakage will also cause a DC offset at the mixer output as shown in Fig. 2.6 To overcome the drawback of DC offset, the improving isolation between LO and RF ports is important. The second-order intermodulation distortion (IMD2) is a fundamental problem, because the second-order intermodulation term interferes the reception of the wanted signal as shown in Fig. 2.7. In a perfectly balanced Gilbert cell mixer, the IMD2 is a common-mode signal and therefore does not a serious problem. However, due to the mismatch of device, the balance between the negative and positive branch of the mixer is degraded and the IMD2 becomes a problem. About I/Q mismatch, if the

modulation is complex modulation, the I/Q mismatch can equal to image interferer. This mismatches between the amplitudes of the I and Q signal corrupt the constellation of the down converted signal. Therefore influences the bit error rate. Finally, flicker noise or l/f-noise may be a problem in the mixer and subsequent filter because the signal is converted directly to baseband.

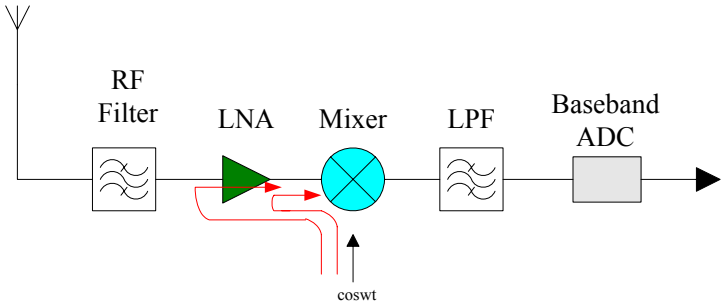

Fig. 2.5 LO signal leakage

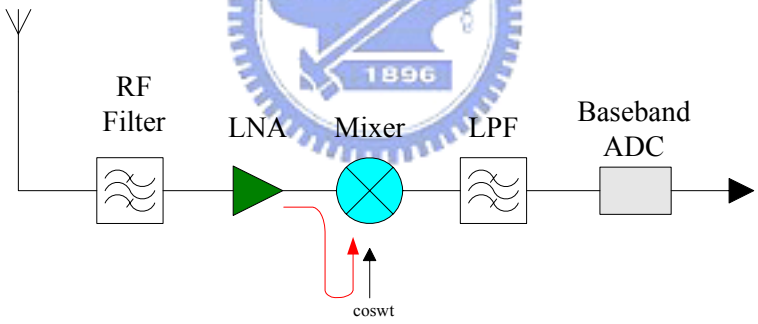

Fig. 2.6 A strong interferer signal leakage

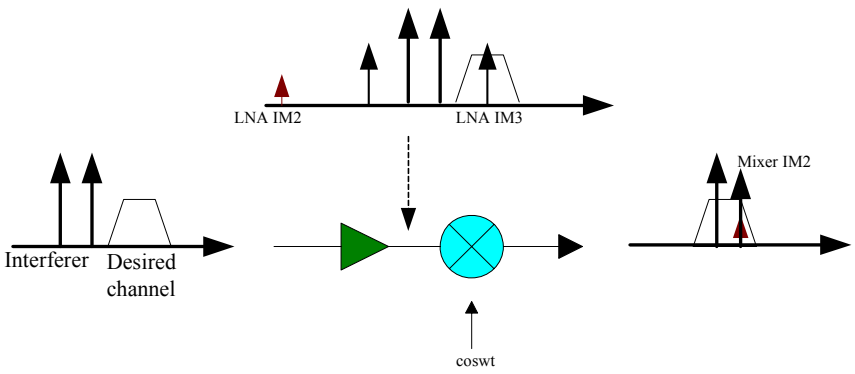

Fig. 2.7 Even order distortion

2.4 Mixer Fundamentals

2.4.1 Principles of Mixer

The mixer is an essential building block in the receivers, which is responsible for frequency up-conversion and down-conversion. It is also an important component associated with the linearity of the front-end receivers. The first stage of mixer must have high linearity to handle the large input signals from LNA without significant intermodulation. Nonlinearity causes many problems, such as cross modulation, desensitization, harmonic generation, and gain compression, but even-order nonlinearity can be easily reduced by differential architecture. However, odd-order nonlinearity is difficult to be reduced, especially the third-order intermodulation distortion (IMD3). IMD3 is the dominant part of the odd-order nonlinearity.

Mixer is a three ports circuit, which are the RF port, the LO port and the IF port. It is a multiplication of two signals which are the RF signal amplified from the low noise amplifier and the signal from the local oscillator (LO) to achieve the function of frequency transformation. This is depicted by equation (2.4). Then the RF signal is down-converted to the intermediate frequency (IF).

$$\left(A\cos\omega_1 t\right)\left(B\cos\omega_2 t\right)=\frac{AB}{2}\left[\cos\left(\omega_1+\omega_2\right)t+\cos\left(\omega_1-\omega_2\right)t\right] \tag{2.4}$$

From the equation (2.4), the multiplication of two signals at the frequencies of ω1 and ω2 together produce signals at the sum (ω1+ω2) and difference (ω1-ω2) frequencies. The amplitudes are proportional to the RF and LO amplitudes. The multiplications in the time domain would result in convolutions in the frequency domain. Thus, the mixer can responsible for frequency translation. In equation (2.4), signals at the frequency of (ω1+ω2) can be easily filtered out because they are far away from desired frequency in the frequency domain. The signals at the frequency of (ω1-ω2) are our desired outputs. In circuit implementations, the multiplication can be

achieved by passing the input signal $A\cos\omega t$ from RF through a switch driven by another signal $B\cos\omega t$ from LO. If the LO amplitude is constant, any amplitude modulation in the RF signal is transferred to the IF signal.

The most important parameters for determining the performance of a mixer are power conversion gain, and linearity. We will describe these parameters in the subsequent contents.

2.4.2 Performance Parameters

2.4.2.1 Conversion Gain

One of important parameters of mixer's characteristics is conversion gain, which is defined as the ratio of the desired IF output to the value of the RF input as shown in equation (2.5). In general, the conversion gain of the mixer has two types: one is voltage conversion gain and the other is power conversion gain.

$$Conversion\ \ Gain = \frac{The\ \ desired\ \ output\ \ IF\ \ power}{The\ \ input\ \ RF\ \ power} \tag{2.5}$$

Assuming input a sinusoidal signal and the output would include signals at integer multiples of the frequencies of the input signal as equation (2.6). In equation (2.6), the terms with the input frequency are called the fundamental signal, and the higher order terms are called the harmonics. The harmonics would cause performance degradations.

$$\begin{aligned} V_{OUT}(t) &= \alpha_1(A\cos\omega t) + \alpha_2(A\cos\omega t)^2 + \alpha_3(A\cos\omega t)^3 + ... \\ &= \alpha_1(A\cos\omega t) + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) + ... \end{aligned} \tag{2.6}$$

The output function of mixers is a compressive function of input levels. When the input level grows sufficiently high, the output eventually saturates and the conversion gain begins decreasing. If α3 holds a negative value, this phenomenon will happen. At small values of input level A, the second term is negligible and the gain remains

constant. The gain starts decreasing when the input level gets large as shown in equation (2.7).

$$Gain = \alpha_1 + \frac{\alpha_3 A^2}{4} \tag{2.7}$$

2.4.2.2 Linearity

The mixers are assumed to be linear and time-invariant. The linearity is a significant parameter in the mixer design. Here we will introduce two parameters of linearity: P1dB and IIP3.

The IF output is proportional to the RF input signal amplitude ideally. However, as the input signal becomes large, the output signal fails to exhibit this characteristic. We use the value departing the ideal linear curve 1 dB as the referenced point, 1 dB compression point, shown in Fig. 2.8. The dashed line in Fig. 2.8 shows our desired output characteristics. The solid line shows the real characteristic. The 1dB compression point characterizes the input level where the output level is 1dB less than our desired output level. A higher 1dB compression point stands for a better linearity performance.

The linearity of a mixer can also be evaluated by intermodulations. The two-tone third-order intercept is often used to characterize mixer linearity. Ideally, each of two different RF input signals will be translated without interacting with each other, and we can only gain the desired IF signal from the output port. However, practical mixers will always exhibit some intermodulation effects. This is because that two or more different frequencies of input signals will degrade the linear region of the system. The third intercept point (IP3) is measured with two tone test. Two tones are closely placed and injected as input simultaneously. If we consider the region where the input level is small, the output characteristic is approximately linear. The third-order

intercept is the intersection of these two curves as illustrated in Fig. 2.9 which is the extrapolation of the signal line and the third-order harmonic line. The higher intercept, the more linear.

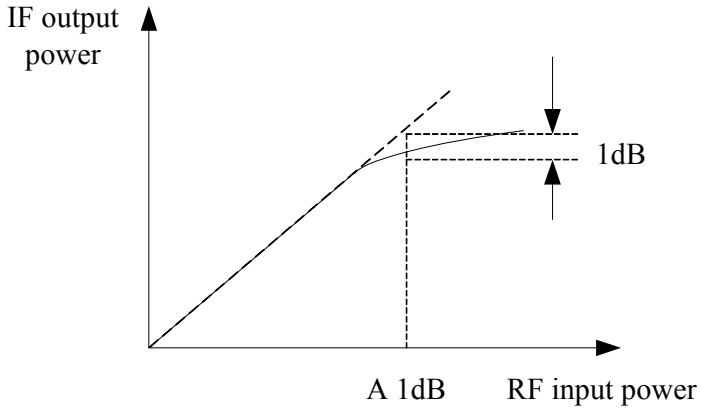

Fig. 2.8 P1dB

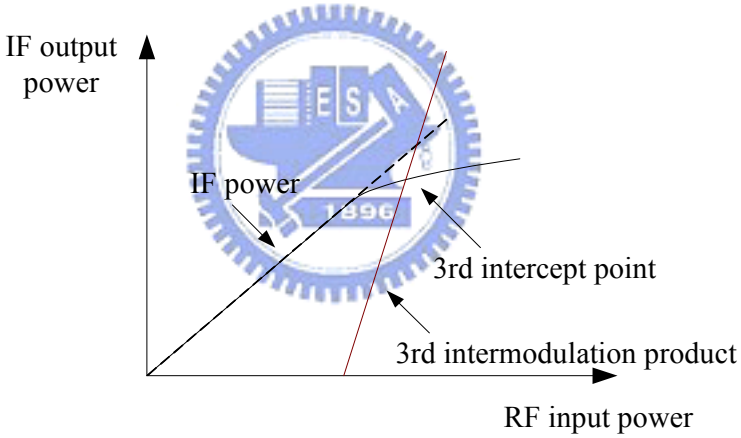

Fig. 2.9 IIP3

2.4.2.3 Isolation

Another important parameter of mixer is isolation, which shows the interaction among RF, IF and LO ports. The isolation between each two ports of the mixer is important. The LO to RF feedthrough is means the LO leakage to the LNA and (or) leakage to the antenna. The RF to LO feedthrough allows strong interferers in the RF path to interact with the LO driving the mixer. The LO to IF feedthrough is also important. If substantial LO signal exists at the IF output, the following stage may be

desensitized. The feedthrough can be reduced largely by use double balanced mixers. The RF to IF isolation means the signal in the RF path directly appears in the IF. In the homodyne receivers, this is a critical issue with respect to the IMD2 problem.

2.4.3 The Basic Mixer Architecture

The implementation of CMOS down-conversion mixer can be passive or active. The simple passive mixer is shown in Fig. 2.10 It is usually using MOS transistor as a switch to modulate the RF signal by LO signal and down convert to IF band. Because passive mixer operates in the linear region, it has high linearity and excellent IIP3. But it provides poor conversion gain and noise figure. The simple active mixer is presented in Fig. 2.11 The active mixer provides better conversion gain than passive mixer. Its conversion gain is decided by the product of the input conductance g_m and load impedance to suppress the noise contributed by the subsequent stages. But the linearity of an active mixer is worse than that of a passive mixer.

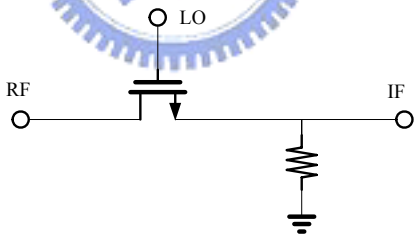

Fig. 2.10 Passive mixer

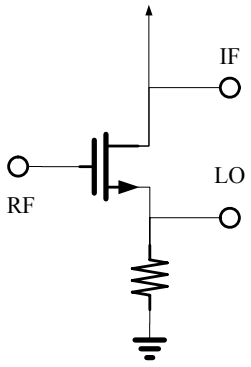

Fig. 2.11 Active mixer

Chapter 3 *The Design of 5.8GHz Bi-directional Amplifier*

Based on the background, a bi-directional amplifier plays a significant role in the Retro-directional antenna system of active Van Atta arrangement. When a bi-directional is designed to possess the high gain, the circuit must be watched out for the isolation of signal in the input port so as to prevent the reflected signal from affecting the circuit performance of the input port. The contents of this chapter below will introduce the complete framework of this bi-directional amplifier using a 0.18 um CMOS process in detail and discuss the principles and considerations of each section.

3.1 Architecture of the Bi-Directional Amplifier

A two-port bi-directional amplifier, which may simultaneously amplify the waves

coming from both ports, is proposed and demonstrated in this chapter. Fig. 3.1 shows the proposed configuration of the bi-directional amplifier, which contains two identical reflection-type amplifiers and a 3-dB quadrature hybrid [10]. The quadrature hybrid circuit can separate the input signal into two output signals with the phase difference of 90 degree and the same power level, and eliminate the signal at isolation port. The reflection-type amplifier, the device of only one end as the input and output ports, can amplify and reflect the incident signal. Port I and port II are the input and output of the bi-directional amplifier. In accordance with the principles of this circuit above, two signals produced by the quadrature hybrid circuit will be amplified by the reflection-type amplifiers and flash back to the hybrid circuit. Let a wave be incident on the bi-directional amplifier from port I as shown in Fig. 3.2, the signals with the same power and out of phase resulted at port I will cancel and the signals with the same power and the same phase resulted at port II will add. The Port I and Port II is the input and output ports of this amplifier. The role of two ports can be exchanged due to its bi-directional amplified capability. This designed process must pay attention to the oscillation condition of this circuit because its principles are similar to them of an oscillator.

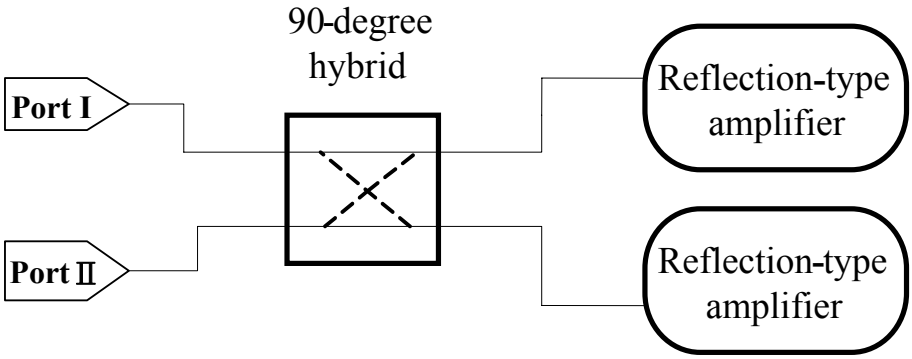

Fig. 3.1 Configuration of the proposed bi-directional amplifier

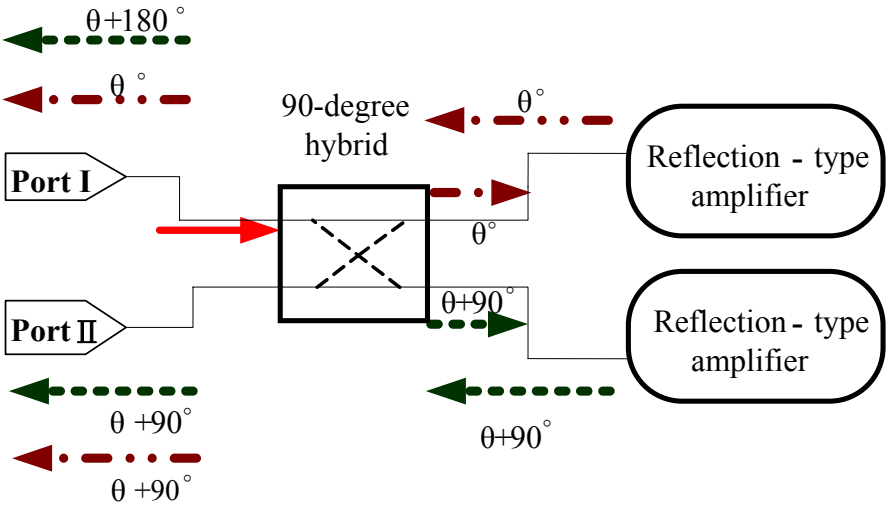

Fig. 3.2 The principle of the bi-directional amplifier

3.2 Circuit Design of the Bi-Directional Amplifier

3.2.1 Quadrature Hybrid

As shown in Fig. 3.3, the quadrature hybrid must be realized by means of transmission lines with the quarter wavelength. The length is about 8mm at the operating frequency of 5.8GHz. The transmission line is not suitable for integrated circuit implementation.

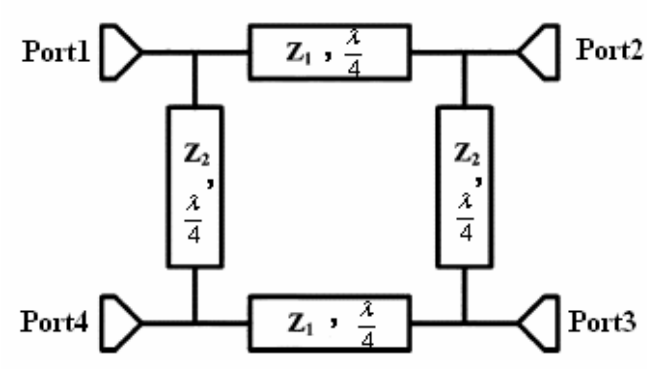

Fig. 3.3 Circuit diagram of the conventional quadrature hybrid

It is completed by adopting lump devices as shown in Fig 3.4 [11]. The symmetry of this circuit is important so that the inductors L1~L4 are using symmetric inductors provided by the standard CMOS process. Due to the lower Quality factor of the inductor implemented in integrated circuit implementation, the quadrature hybrid exhibits a through loss (S31) of 2 dB and a coupling loss (S41) of 2dB. The return loss and isolation, characterized by |S11| and |S21|, is better than 15dB as shown in Fig. 3.5(a). The phase difference between S31 and S41 is about 88° as shown in Fig. 3.5 (b).

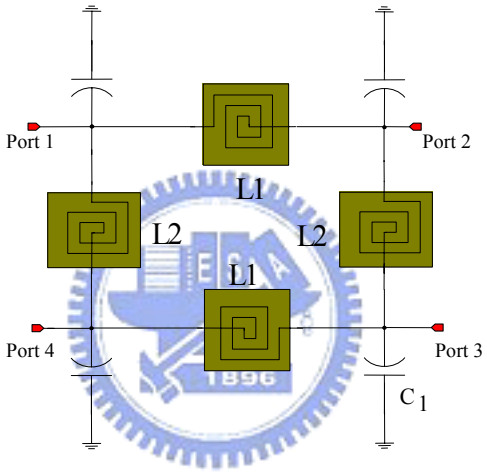

Fig. 3.4 The lumped quadrature hybrid

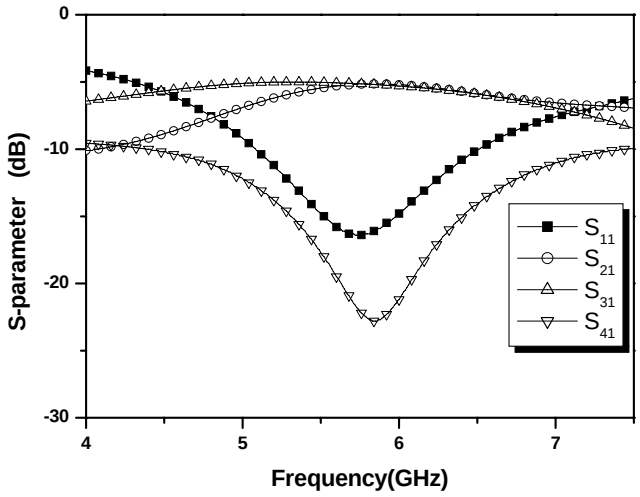

Fig. 3.5(a) The S parameters of the quadrature hybrid

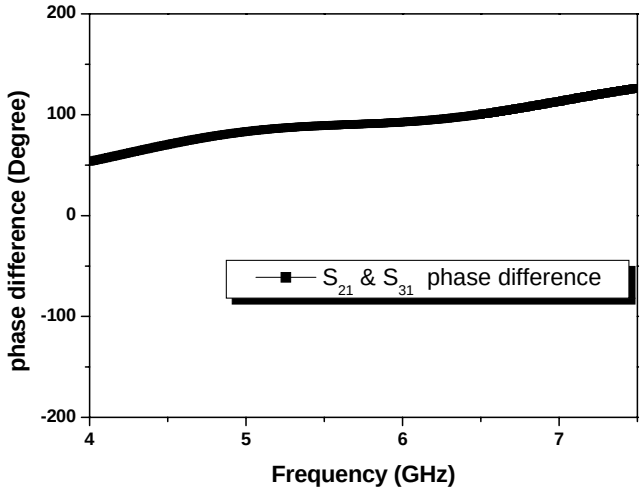

Fig. 3.5(b) The phase difference between S31 and S41

3.2.2 Reflection-type Amplifier

The incident signal can be reflected and amplified by the reflection-type amplifier. It means that the reflection coefficient Γ must be greater than one. The reflection coefficient Γ at the input port of the reflection-type amplifier is expressed as

$$\Gamma = \left| \frac{Z_L - Z_O}{Z_L + Z_O} \right| \tag{3.1}$$

where Z_L is the input impedance of the reflection-type amplifier and Z_0 is the output impedance of the quadrature hybrid. From equation (3.1), the reflection coefficient Γ will be greater than one when the input impedance Z_L is negative [12]-[13]. The reflection-type amplifier is designed as shown in Fig. 3.6. And Fig. 3.7 illustrates small-signal circuit of the reflection-type amplifier. The input resistance Zin can be derived as

$$Zin = \frac{1}{jw}\left(\frac{1}{C_{gs}} + \frac{1}{C_f}\right) - \frac{g_{m1}}{w^2 C_{gs} C_f} + r_{g1} \tag{3.2}$$

From (3.2), the negative resistance $-\frac{g_{m1}}{w^2 C_{gs} C_f}$ can decrease by increasing g_{m1} or decreasing C_f. The r_{g1}, resulted from MOS poly-gate, can be ignored due to multi-finger. Fig. 3.8 illustrates the simulation of input resistance.

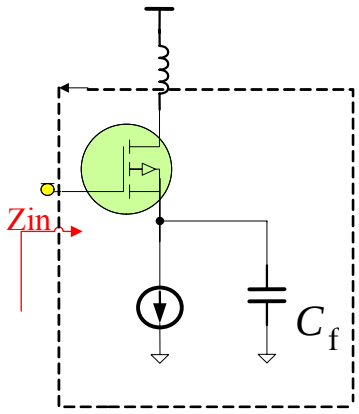

Fig. 3.6 Schematic of the reflection-type amplifier

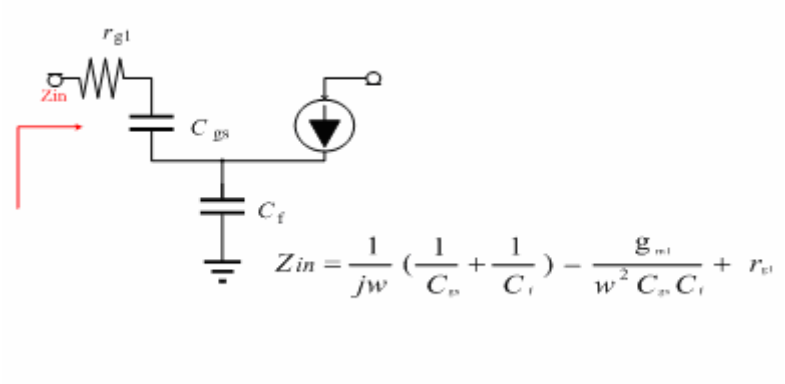

Fig. 3.7 Small-signal equivalent circuit model of reflection-type amplifier

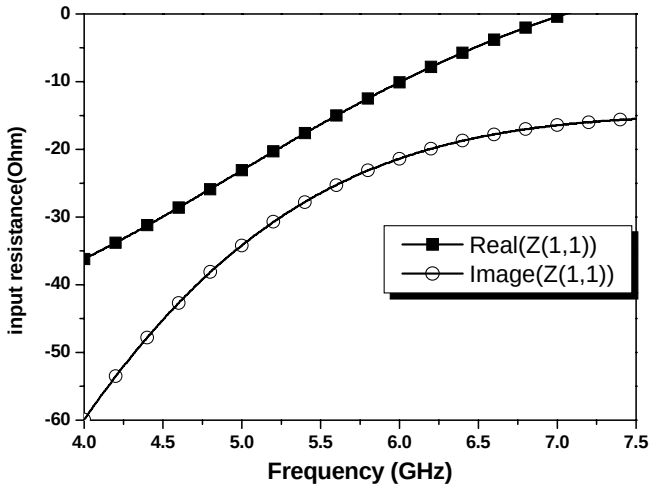

Fig. 3.8 The input resistance of reflection amplipier

3.2.3 Noise Discussion

Fig. 3.10 shows the noise figure at operating frequency if the negative resistance shown in Fig 3.9 is ideal. The noise figure in Fig. 3.10 is caused by the loss of quadrature hybrid. However, there is no ideal negative resistance in practice. The negative resistance is designed as shown in Fig. 3.11. The noise figure and gain is depended on channel width. Fig. 3.12 illustrates the bi-directional amplifier noise figure increased when the channel width increase gradually. Fig. 3.13 illustrates the bi-directional amplifier gain increased when the channel width increase gradually. It means that the noise figure and gain in this design must be trade off. In order to improve the radiating filed, the focus of this design is the gain of the bi-directional amplifier.

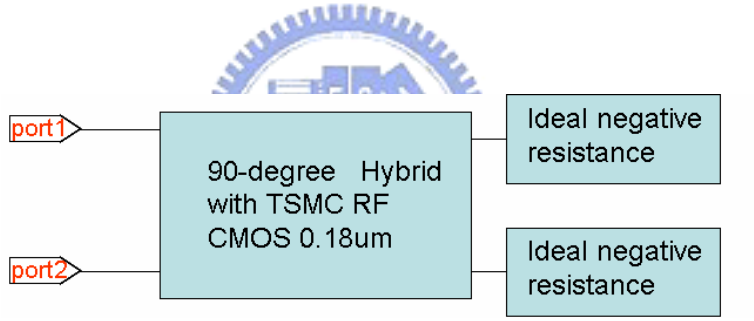

Fig. 3.9 Bi-directional Amplifier with ideal negative resistance

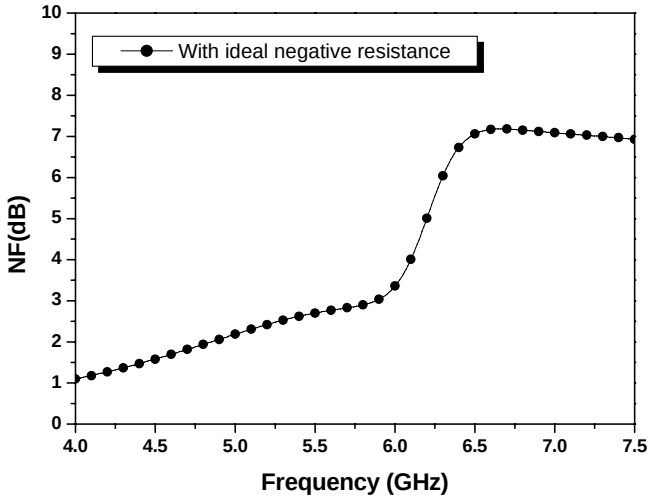

Fig. 3.10 The noise figure of bi-directional amplifier with ideal negative resistance

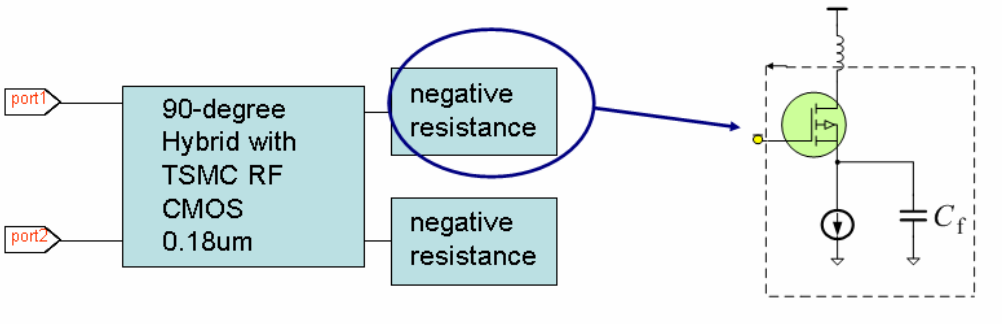

Fig. 3.11 Bi-directional Amplifier with negative resistance

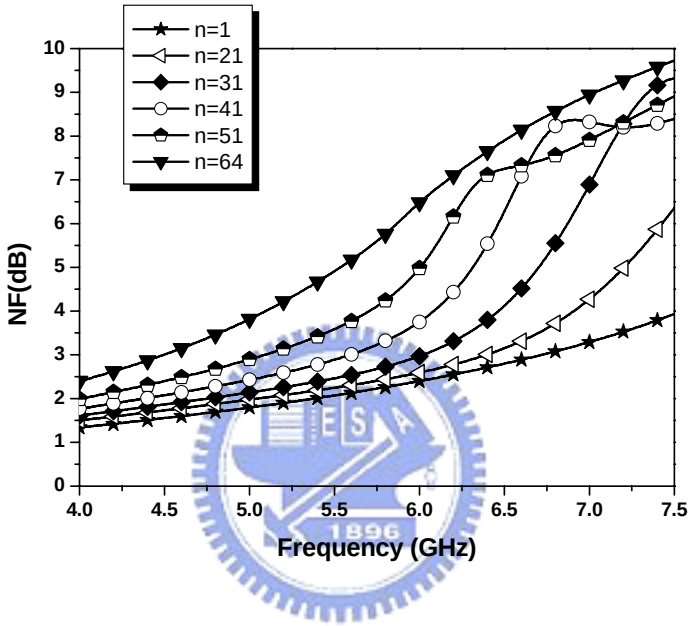

Fig. 3.12 The noise figure increase as the width increase

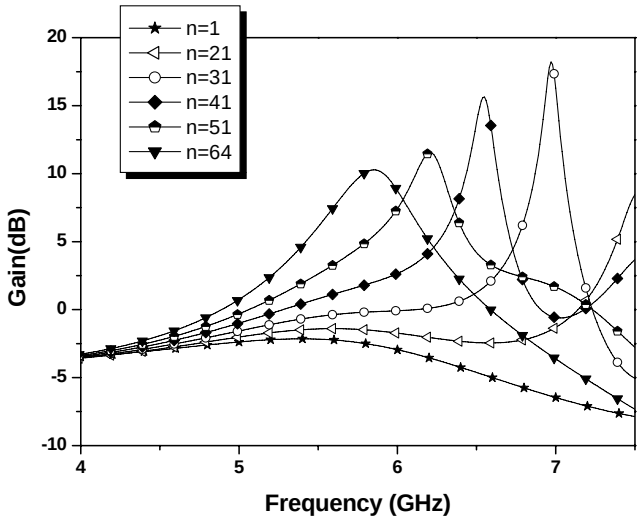

Fig. 3.13 The gain increase as the width increase

3.2.4 Bi-directional Amplifier

According to above analysis, Fig. 3.14 shows the proposed bi-directional amplifier, which is composed of a quadrature hybrid, two identical reflection-type amplifiers and current source for reflection-type amplifiers.

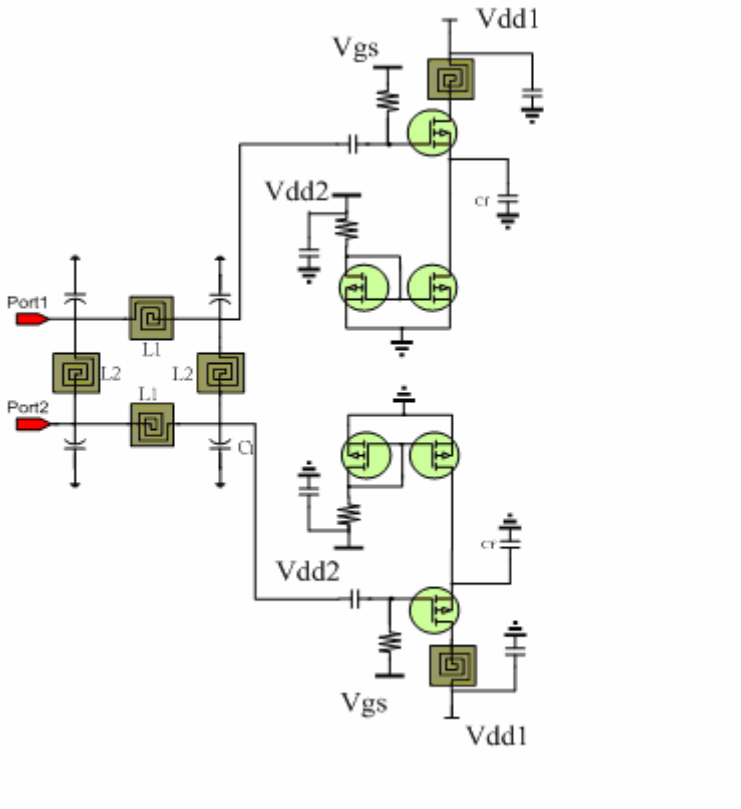

Fig. 3.14 Schematic of the proposed Bi-directional Amplifier

3.3 Simulated and Measured Results

In this section, we show the simulation performance and measurement results of the bi-directional amplifier. For the poor experience in the beginning, the result is bad. Then we find the reason that the result is bad and improve on the layout.

3.3.1 Simulation Performance

Fig. 3.15 shows the magnitude of S11 and S21. Fig. 3.16 shows the magnitude of S12 and S22. The characteristic of the bi-directional amplifier was verified from Fig.

3.15 and Fig. 3.16. Fig. 3.17 shows the noise figure of the bi-directional amplifier. Table 3.1 summarizes the bi-directional amplifier performance of simulated results.

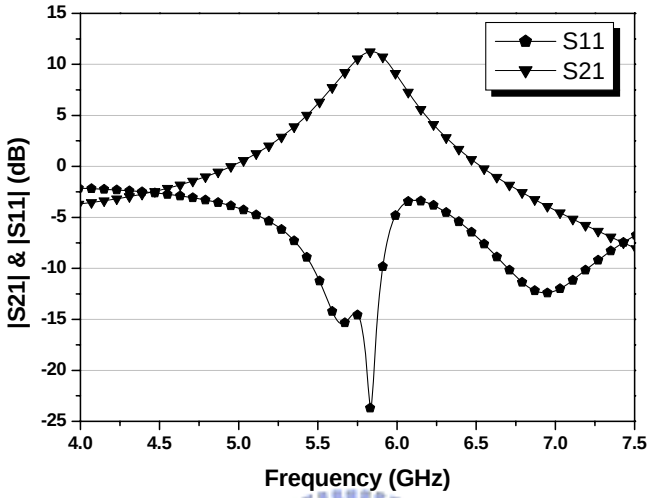

Fig. 3.15 |S21| & |S11| simulation

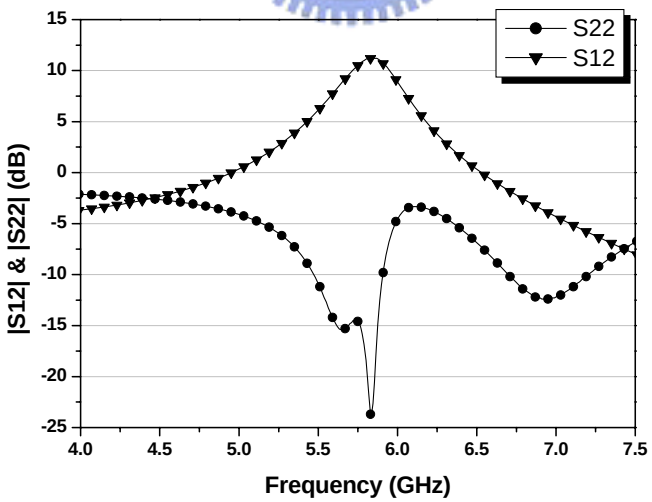

Fig. 3.16 |S12| & |S22| simulation

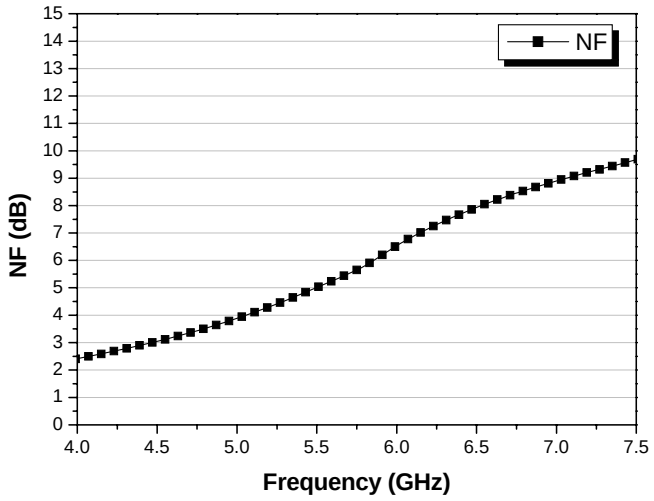

Fig. 3.17 NF simulation

Table 3.1 Summary of the bi-directional amplifier simulation results

Parameters	Simulation result
Technology	TSMC 0.18um CMOS
Center frequency(GHz)	5.8
Id(mA)	9.1
P-1dB(dBm)	-21
Gain S21(dB)	11
Return Loss S11(dB)	<-10
Noise figure(dB)	5.8
Bandwidth(MHz)	250
Power dissipation(mW)	9.1
Chip size(mm^2)	0.96*1.15

3.3.2 Measured results

Fig. 3.18 shows the layout of the proposed bi-directional amplifier. The size of the layout is 1.13mm by 1.05mm including pads. The measurements were performed with the chip AC probe and DC bond-wire. Fig. 3.19 and Fig. 3.20 show the measured results of the bi-directional amplifier.

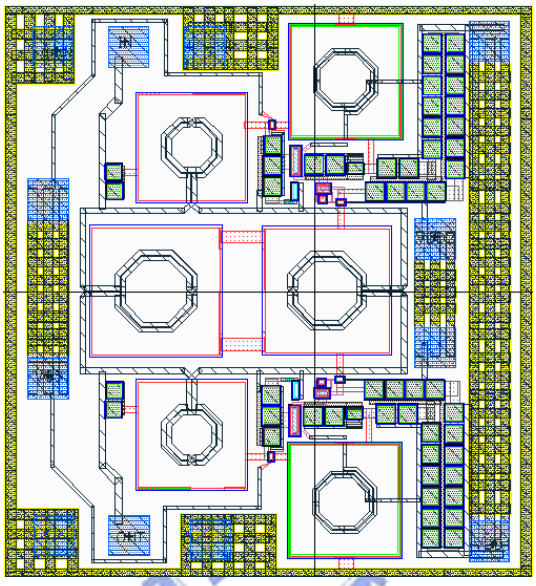

Fig. 3.18 Layout of the proposed bi-directional amplifier

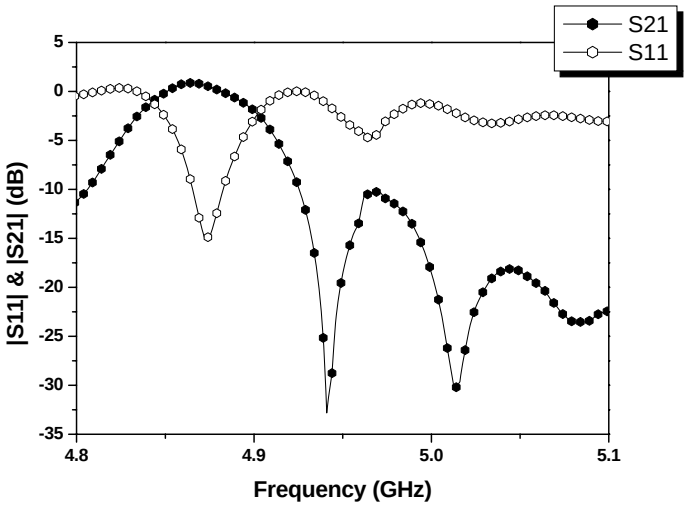

Fig. 3.19 |S21| and |S11| measurements

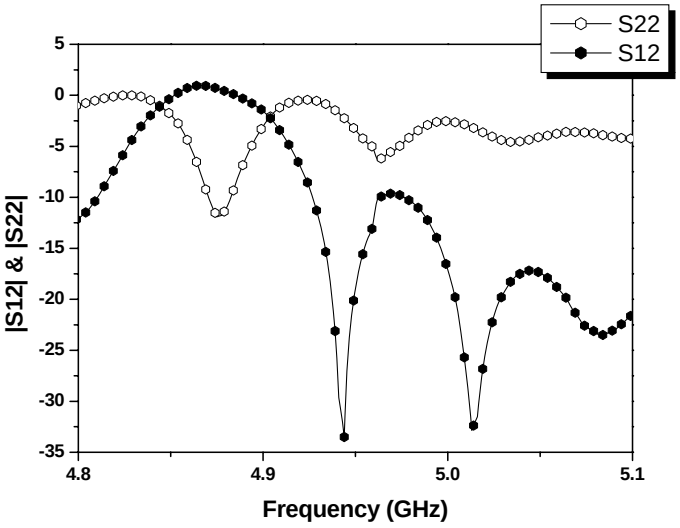

Fig. 3.20 |S12| and |S22| measurements

3.3.3 The reason for bad measured performance

Experience teaches it. The grounding effect is important in the IC environment in spite of the short line. The quadrature hybrid consists of four grounding capacitances. In the layout the four capacitances didn't connect to ground but to connect to shielding ground of the inductors as shown in Fig. 3.21. The shielding ground of the inductor is excessively narrow. Considering the shielding ground effect, we flatten the model of the inductors provided by the standard CMOS process and take the thin lines as shown in Fig. 3.22. Then we run EM simulation by ADS Momentum and obtain the layout effect model. Because of the effect caused by the shielding ground, the measurement with no DC bias was shown in Fig. 3.23. Fig. 3.24 shows the simulation with no DC bias. Fig. 3.25 shows the simulation with the shielding ground effect and no DC bias. Fig. 3.26 and Fig. 3.27 show the bi-directional amplifier simulation results with the shielding ground effect. We can verify that the bad results due to the shielding ground from above pictures.

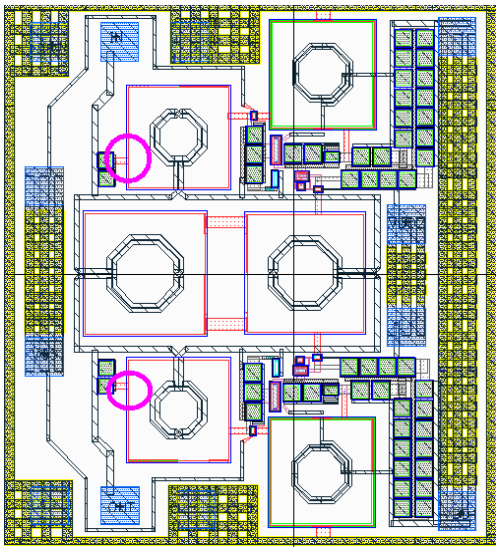

Fig. 3.21 Bug of the proposed layout

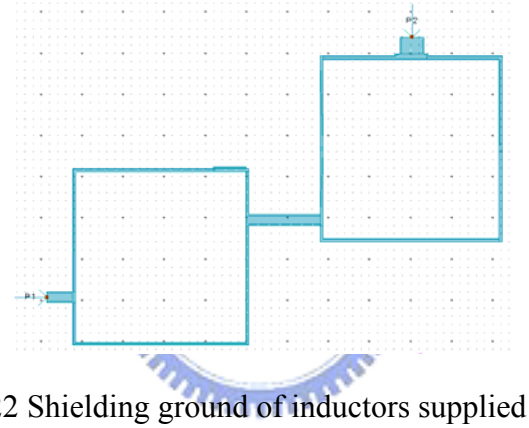

Fig. 3.22 Shielding ground of inductors supplied by TSMC

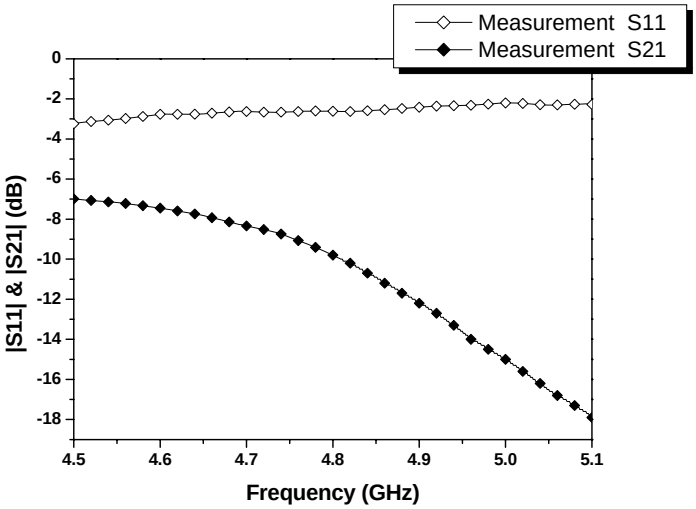

Fig. 3.23 Measurement with no DC bias

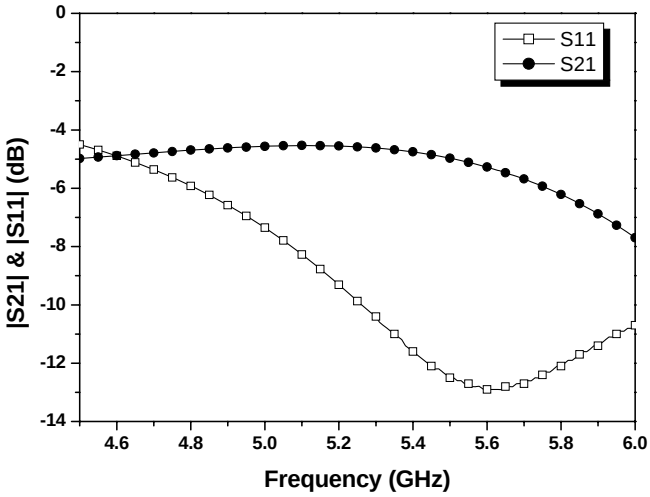

Fig. 3.24 Simulation with no DC bias

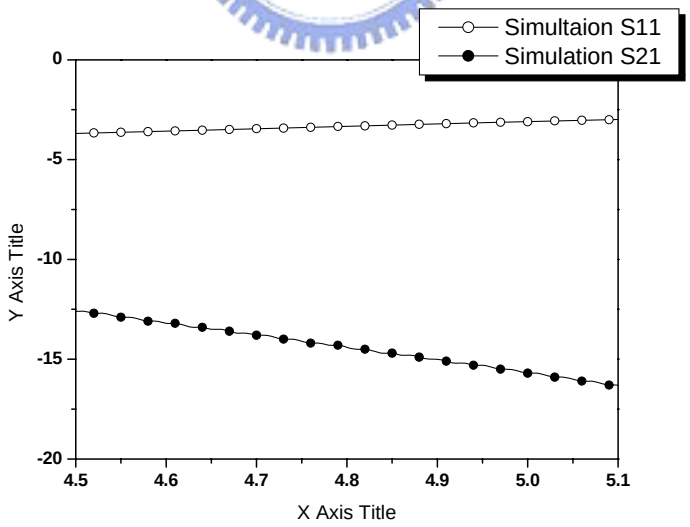

Fig. 3.25 Simulation with shielding ground effect and no DC bias

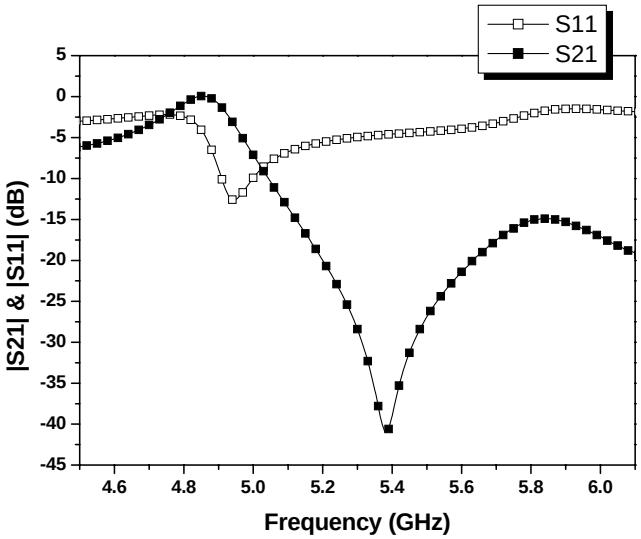

Fig. 3.26 Simulation with shielding ground effect

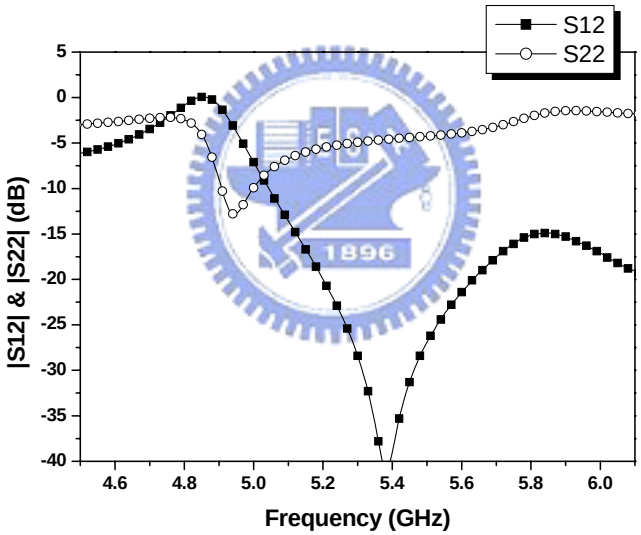

Fig. 3.27 Simulation with shielding ground effect

3.3.4 Improvement

Fig. 3.28 shows the layout of the proposed bi-directional amplifier. The size of the layout is 1.15mm by 0.96mm including pads. Considering the layout effect, we take the long layout line as shown in Fig. 3.29 and run EM simulation by ADS Momentum so as to obtain the layout effect model. The improved chip will be back in August.

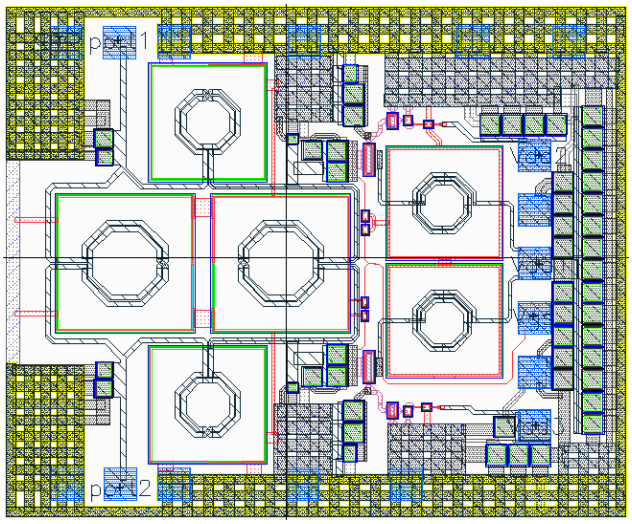

Fig. 3.28 Layout of the improved bi-directional amplifier

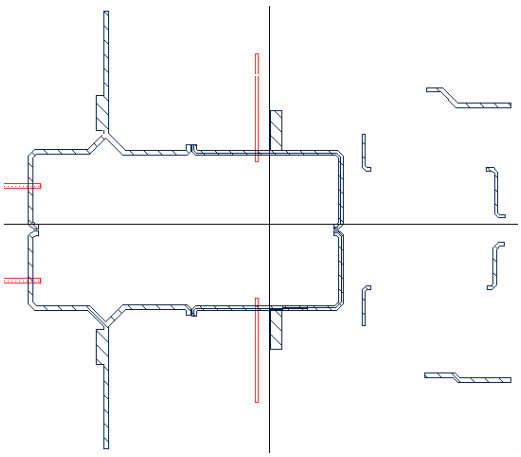

Fig. 3.29 EM consideration

3.4 Comparison and Summary

The comparison of the proposed bi-directional amplifier against recently reported on amplifiers with bi-direction characteristic is shown in Table 3.2. It needn't any switch to change the amplifier direction and needn't control voltage to change the amplifier direction.

Table 3.2 Summary of the comparison

Ref.	Freq-Range (GHz)	Gain S21 (dB)	Return Loss (dB)	switch	Voltage Control Direction	Size (mm^2)
[14]	42	6	10	Yes	NO	N/A
	40	10	8			
[15]	2 ~ 18	0 ~ 4.5	12 ~ 30	Yes	NO	7.6*8.3
	6 ~ 18	0 ~ 12	12 ~ 30			
[16]	8~12	10	10	NO	Yes	5
[10]	6	9	6	NO	NO	Off-chip
This work	5.8	11	15	NO	NO	1.15*0.96

This section presents the amplifier provided with two directions by consisting of a quadrature hybrid and two reflection amplifier. The simulation result shows the achieved gain of 11 dB at 5.8GHz while the bi-directional amplifier draws 9.1mA. The size of the layout is 0.96mm by 1.15mm including pads.

Chapter 4 *The Design of A Miniaturized Quadrature Hybrid Using CMOS Active Inductors*

Quadrature hybrid has been widely used in microwave systems for decades. Typically, quadrature hybrids are useful as power dividers or power combiners in various microwave circuits such as balanced amplifiers, balanced mixers, and phase shifters. Up to now, quadrature hybrids were implemented using the microstrip [17], stripline [18], finite-ground coplanar waveguide (CPW) [19], multilayer structures [20], and low-temperature co-fired ceramic (LTCC) [21]. Their sizes are relatively large due to the use of quarter-wavelength transmission lines, however the quarter-wavelength transmission line length has long impeded its applications in monolithic microwave integrated circuits (MMICs), especially for frequencies below 10 GHz. The ways to reduce the size of transmission lines such as using the folded lines configuration, capacitive loading, lumped element components, or the T or π equivalent-circuit model were employed to miniaturize quadrature hybrid [14].

Though a smaller circuit size can be achieved, it suffers from higher insertion loss due to the lower quality factor (Q) in monolithic microwave integrated circuits.

In this chapter, a lumped quadrature hybrid with active inductors is proposed to overcome the limitations of the on-chip passive components. The contents of this chapter below will introduce the complete framework of this quadrature hybrid using a 0.18 um CMOS process in detail and discuss the principles and considerations of each section.

4.1 Architecture of the Quadrature Hybrid

As shown in Fig. 4.1, the quadrature hybrid must be realized by means of transmission lines with the quarter wavelength. In order to reduce the circuit size effectively, the concept of replacing the transmission line sections with lumped passive components has also been adopted. Equation (4.1) is the ABCD matrix of the transmission line as shown in Fig. 4.2. Equation (4.2) is the Z matrix of the T-network as shown in Fig. 4.3. From equation (4.1), (4.2) and (4.3), a transmission line section with a characteristic impedance Z0 and electrical length βd can be replaced by its lumped equivalent T-network if βd=90°.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\beta d & jZ0\sin\beta d \\ jY0\sin\beta d & \cos\beta d \end{bmatrix} \tag{4.1}$$

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} ZA+ZC & ZC \\ ZC & ZB+ZC \end{bmatrix} \tag{4.2}$$

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} \frac{A}{C} & \frac{AD-BC}{C} \\ \frac{1}{C} & \frac{D}{C} \end{bmatrix} \tag{4.3}$$

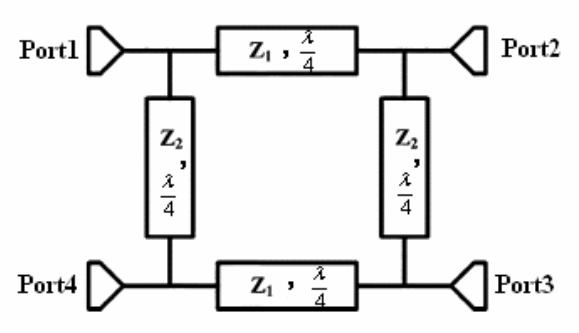

Fig. 4.1 Circuit diagram of the conventional quadrature hybrid

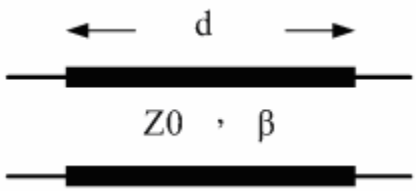

Fig. 4.2 Transmission line section

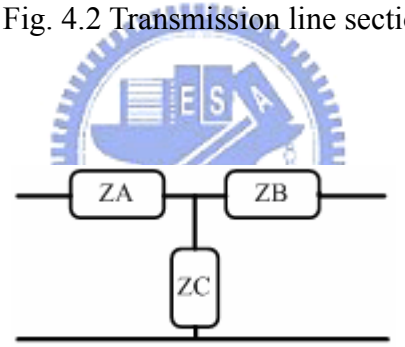

Fig. 4.3 Lumped T-network

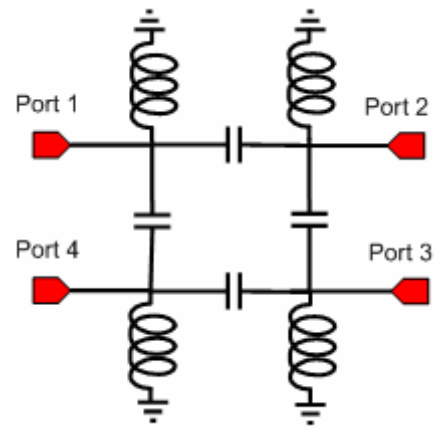

Fig. 4.4 Lumped quadrature hybrid

Since shunt inductance is preferable for the implementation of active inductors, an electrical length of $3\lambda/4$ is employed in the proposed circuit topology. By replacing the transmission line sections with the π-networks, the equivalent circuit of the lumped quadrature hybrid is illustrated in Fig. 4.4.

4.2 Circuit Design of the Quadrature Hybrid

4.2.1 Passive Inductor

Using the spiral inductor provided by the standard CMOS process is convenient for designer. However, it is bad to use due to the lower Quality factor (Q) of the inductor implemented in integrated circuit implementation. Fig. 4.5 shows the inductance value and lower Q-factor of spiral inductor using a 0.18 um CMOS process. It means that the higher insertion loss suffers from the higher parasitical resistance of the spiral inductor implemented in integrated circuit implementation than SMD component. Also, the die size of one inductor as shown in Fig. 4.6 is about 0.26*0.26 mm^2, and it will be larger if the inductance value is increasing. In order to reduce the circuit size and improve the Q-factor, the active inductor will be used and discussed later.

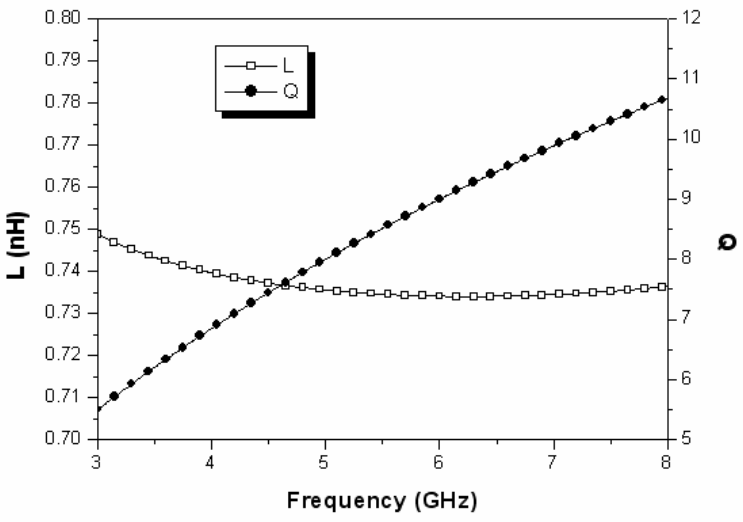

Fig. 4.5 Simulation of the spiral inductor using a 0.18 um CMOS process

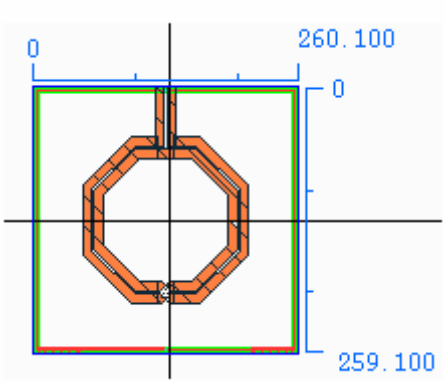

Fig. 4.6 The die size of an inductor is about 0.26*0.26 mm^2

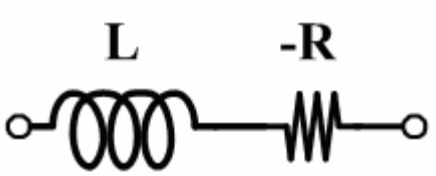

Fig. 4.7 Spiral inductor connect with negative resistance

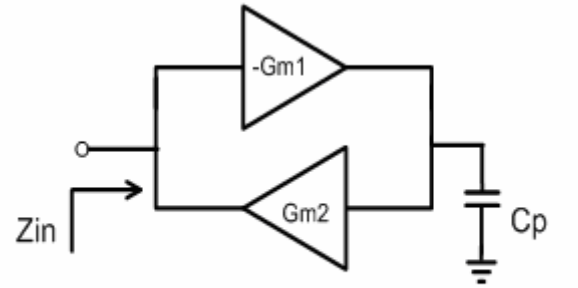

Fig. 4.8 The diagram of active inductor

4.2.2 Active Inductor

There are two ways to increase the quality factor, which plays an important role in the insertion loss. One is using spiral inductor connecting with a negative resistance [22]; the other is using the active inductor [23]. The former used negative resistance to cancel the parasitic resistance of spiral inductor as shown in Fig. 4.7. Though the quality factor is improved, the die size is large. Active inductors have advantages of

superior quality factor and small die size. The basic principle of the active inductor is based on a well-known gyrator theory [24]. The input impedance in Fig. 4.8 can be expressed by using Kirchoff's law.

$$-Ix = -G_{m2}\left(G_{m1}V_x \times \frac{1}{sC}\right) \tag{4.4}$$

$$\frac{V_x}{I_x} = \frac{sC_p}{G_{m1}G_{m2}} = sL \tag{4.5}$$

$$Leq = \frac{C_p}{G_{m1}G_{m2}} \tag{4.6}$$

From equations (4.4)、(4.5)、(4.6),Gm1 and Gm2 are the transconductor of the amplifier and Cp is the parasitic capacitance of the amplifier. The basic active inductor based on a gyrator topology can be realized by using a single MOS transistor as the transconductance (G_m) element, as shown in Fig. 4.9.

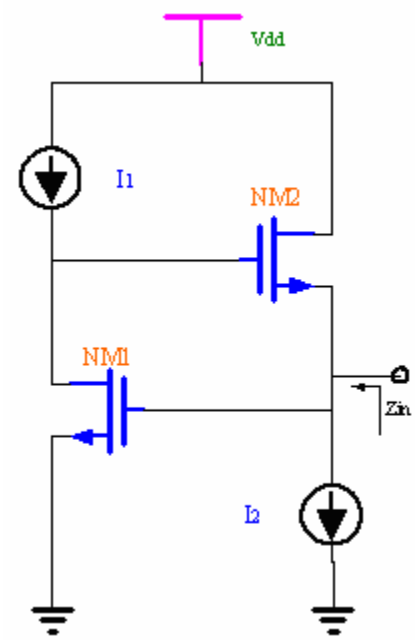

Fig. 4.9 Schematic of the basic active inductor

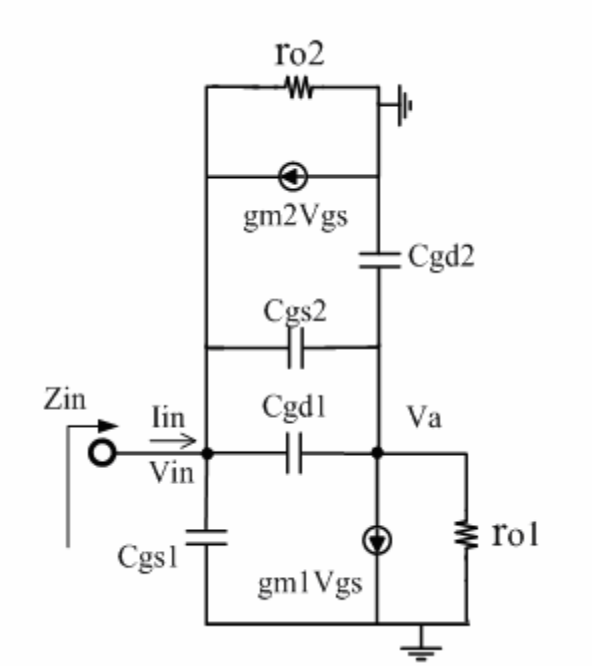

Fig. 4.10 Small-signal model of the basic active inductor

The input impedance of this basic active inductor, the small signal model as shown in Fig. 4.10, can be expressed by using Kirchoff's law.

$$\frac{Vin}{r_{o2}} + (Vin - Va) \times (sCgs2 + sCgd1 + gm2) + Vin \times sCgs1 = Iin \tag{4.7}$$

$$Va \times (sCgd2 + \frac{1}{r_{o1}}) + (Va - Vin) \times (sCgs2 + sCgd1) + Va \times gm1 = 0 \tag{4.8}$$

$$\begin{aligned} Yin &= sCgs1 + \frac{1}{r_{o2}} + \frac{(sCgs2 + sCgd1 + gm2)(sCgd2 + \frac{1}{r_{o1}} + sCgs1 \times gm1)}{sCgs2 + sCgd1 + sCgd2 + \frac{1}{r_{o1}}} \\ &\approx sCgs1 + \frac{1}{r_{o2}} + gm2 + \frac{gm1gm2}{sCgs2 + \frac{1}{r_{o1}}} \qquad (\because sCgdi << sCgsi) \end{aligned} \tag{4.9}$$

From equation (4.9), Zin is equivalent to the conductance Yin. For the real part and the imaginary part, Zin can be equivalent RLC network as shown in Fig. 4.11. Equation (4.10)、(4.11)、(4.12) 、(4.13), derived by equation (4.9), show the values of all components in Fig. 4.11.

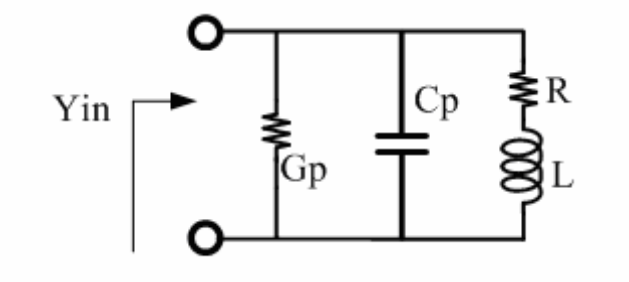

Fig. 4.11 Equivalent RLC model of active inductor

$$L = \frac{Cgs2}{gm1gm2} \tag{4.10}$$

$$R = \frac{1}{gm1gm2r_{o1}} \tag{4.11}$$

$$Cp = Cgs1 \tag{4.12}$$

$$Gp = \frac{1}{r_{o2}} + gm2 \tag{4.13}$$

4.2.3 Quadrature Hybrid

There are many methods to improve quality-factor of active inductors. Gain boosting, here we choose as shown in Fig. 4.12 [25], have the advantages of lower resistance. Fig. 4.13 shows the inductance and quality-factor simulation of this active inductor. The quality-factor of active inductor as shown in Fig. 4.13 is higher than spiral inductor. Also, the die size of one inductor as shown in Fig. 4.14 is about

0.0851*0.070 mm^2. The shunt inductances in the lumped equivalent circuit, as shown in Fig. 4.4, are replaced by the cascode active inductors. By employing the active inductors, the area can be reduction in this design. Fig. 4.15 shows the total circuit element. Also, another advantage of this design is the tunable frequency. The inductance is depended on the bias currents of transistors. The center frequency of the quadrature hybrid can be tunable by adjusting the bias current.

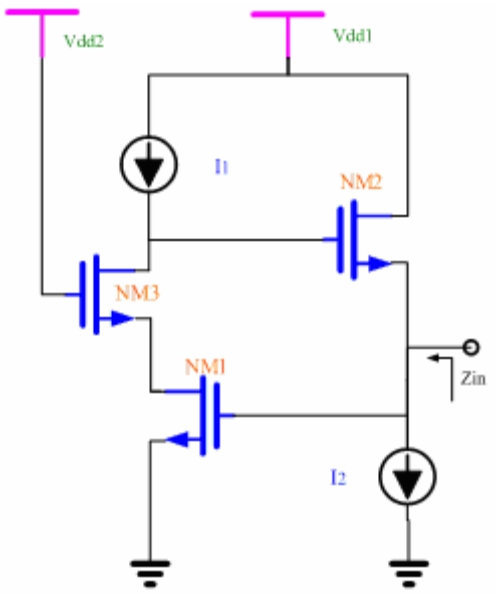

Fig. 4.12 Q-enhanced of cascode active inductor

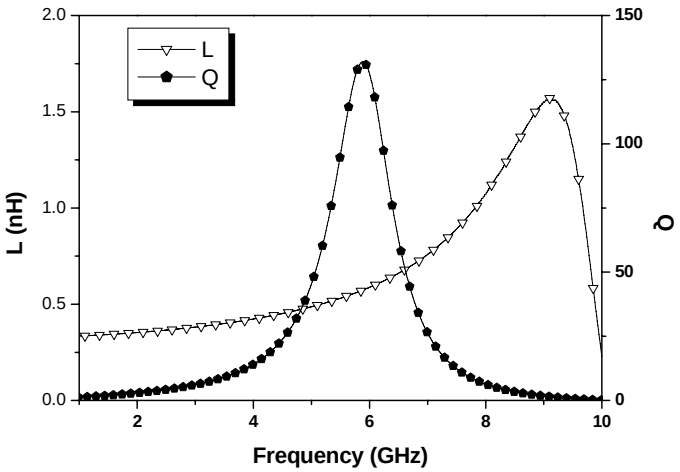

Fig. 4.13 Simulation inductance of cascade active inductor

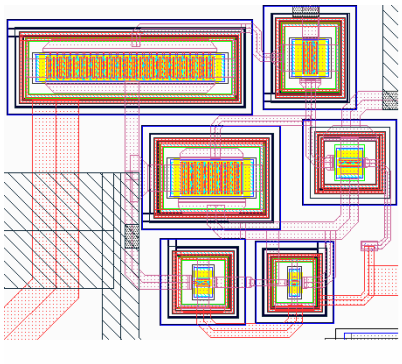

Fig. 4.14 The die size of an inductor is about 0.0851*0.070 mm^2

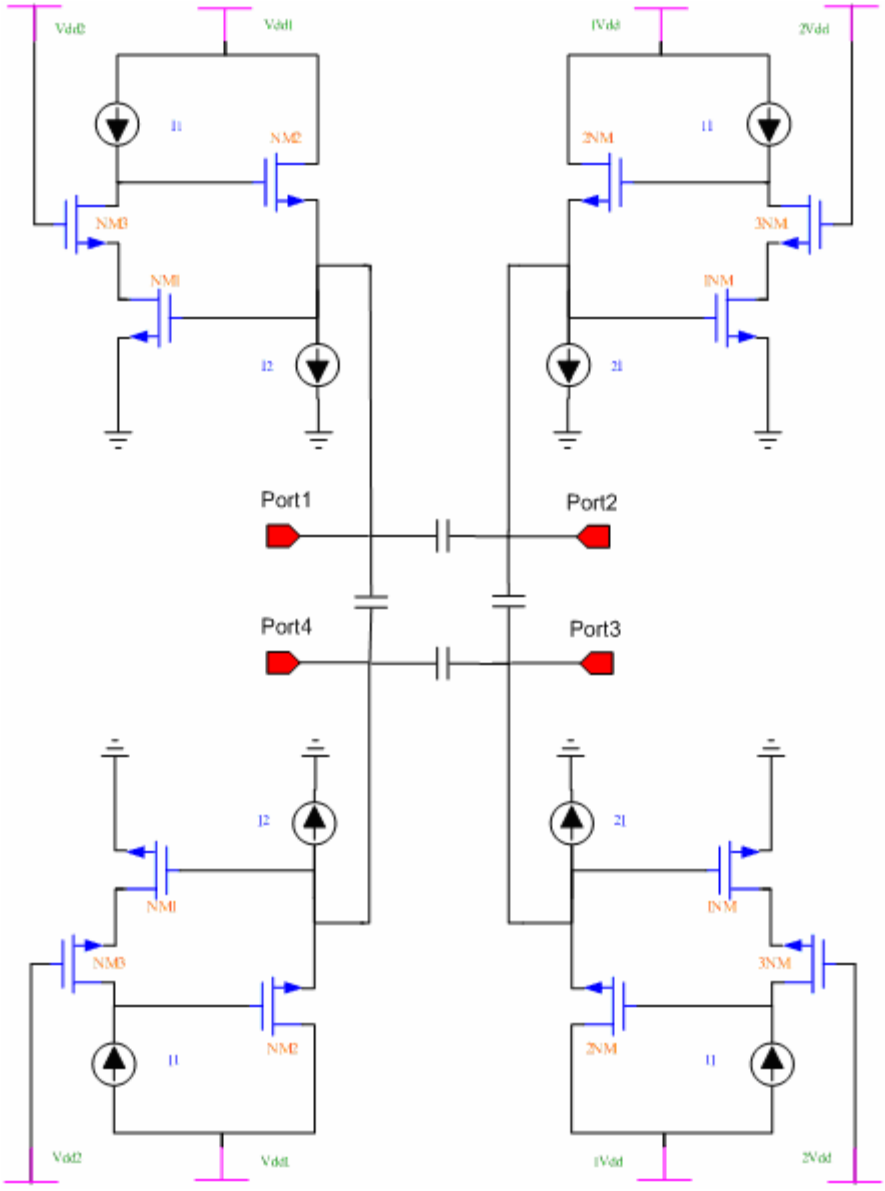

Fig. 4.15 Complete schematic of quadrature hybrid with active inductors

4.3 Simulation and Measurement Results

In this section, we show the simulation performance and measurement results of this minimized quadrature hybrid. The chip layout and microphotograph of the proposed quadrature hybrid are shown in Fig. 4.16 and Fig. 4.17. The size of the layout is 0.74mm by 0.81mm including pads. The measurements were performed with the chip AC and DC probes.

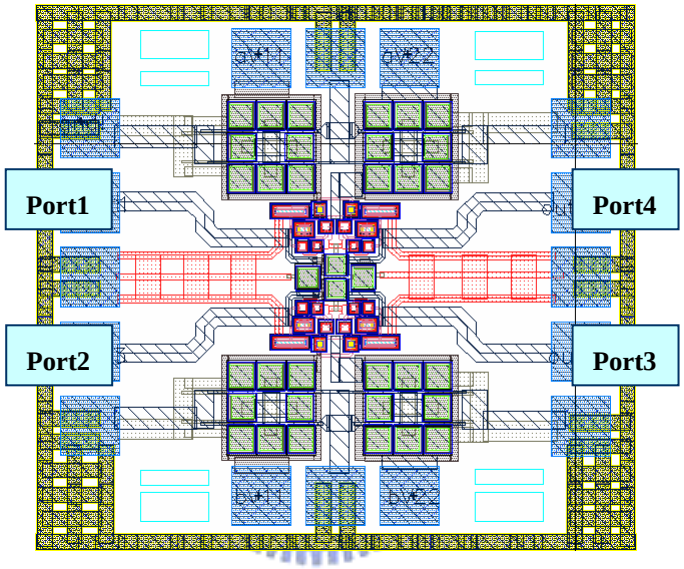

Fig. 4.16 The chip layout of the proposed quadrature hybrid

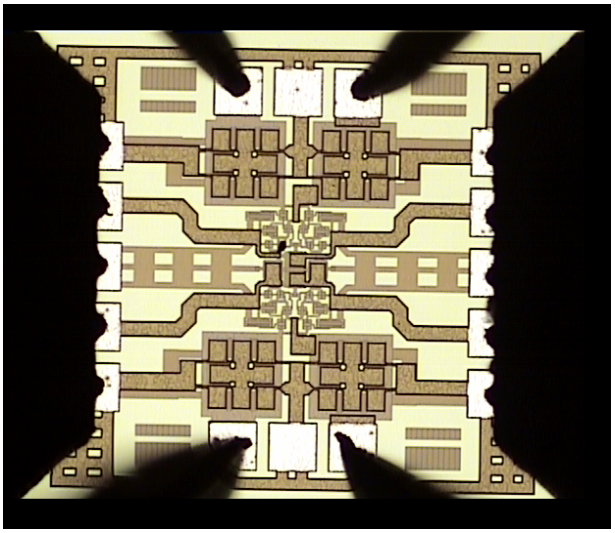

Fig. 4.17 Microphotograph of the proposed quadrature hybrid

Based on the corner-case SS, the compare of simulation performances and measurement results at 1.8V and 1.5V supply voltage was shown from Fig. 4.18 to Fig. 4.21. Fig. 4.18 shows the simulated and measured S11 and S21. The measurement S11 is under -10dB and S21 is about -4dB. Fig. 4.19 shows the simulated and measured S31 and S41. The measurement S41 is under -15dB and S31 is about -2dB.

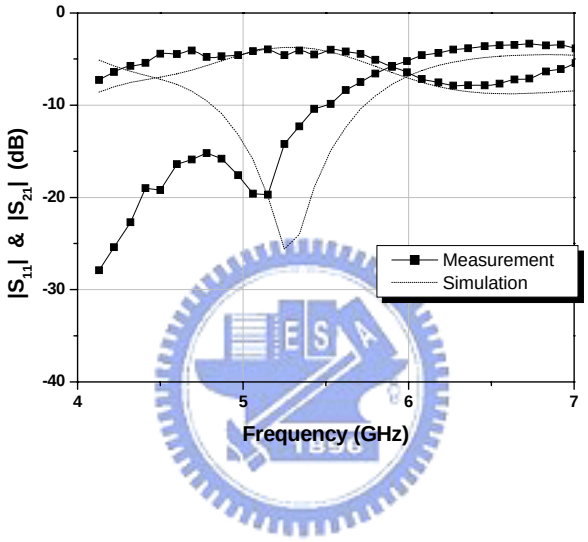

Fig. 4.18 Simulated and measured S11 and S21

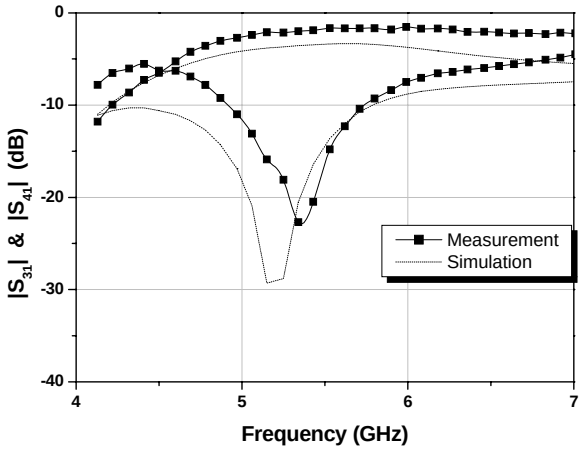

Fig. 4.19 Simulated and measured S31 and S41

The phase difference between S21 and S31 is 94°~100° as shown in Fig. 4.20. Another advantage of this design is the tuning range. Fig. 4.21 shows the tuning range of S11.

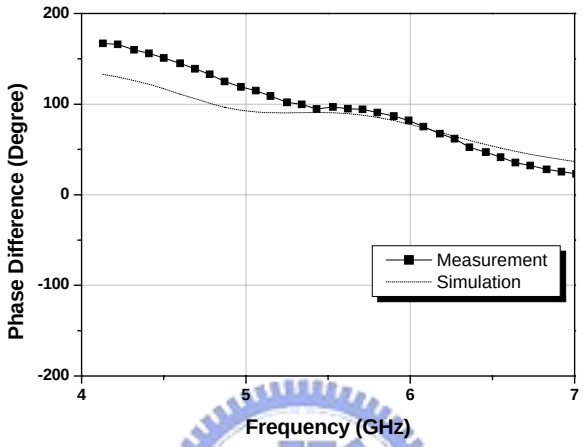

Fig. 4.20 Simulated and measured phase difference between S21 and S31

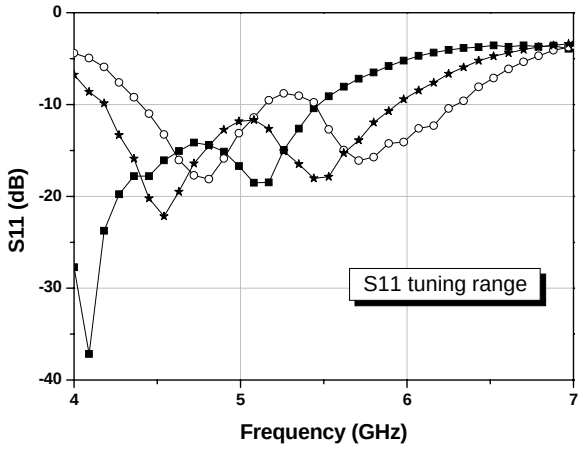

Fig. 4.21 S11 tuning range

Fig. 4.22 shows the tuning range of S21. The tuning range of S31 is shown in Fig. 4.23.

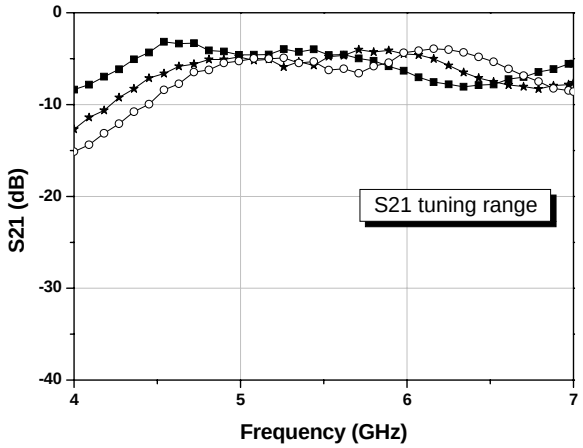

Fig. 4.22 S21 tuning range

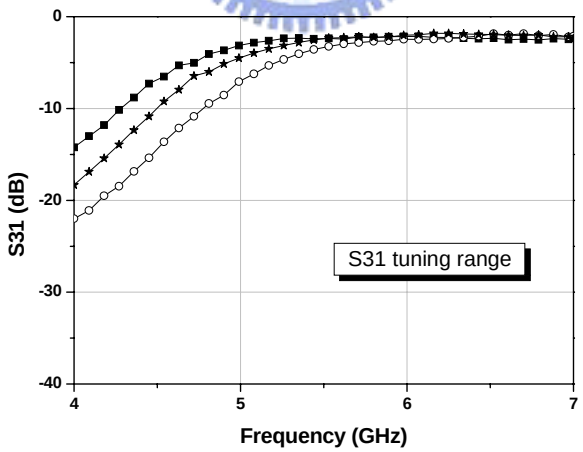

Fig. 4.23 S31 tuning range

The tuning range of S41 is shown in Fig. 4.24. Fig. 4.25 shows the phase difference between S21 and S31. The tuning range of this design is from 5GHz to 6GHz. Table 5.1 is the summary of the quadrature hybrid simulation and measurement results.

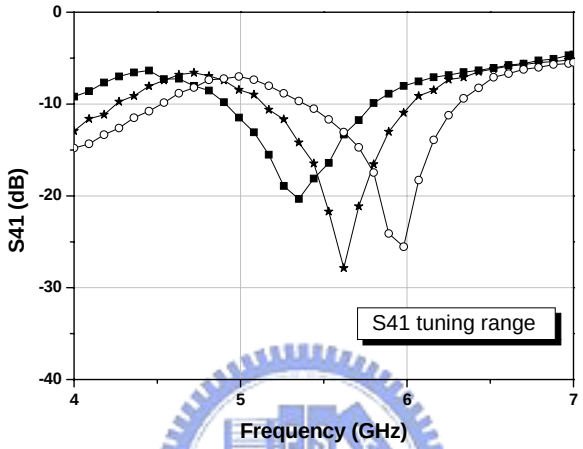

Fig. 4.24 S41 tuning range

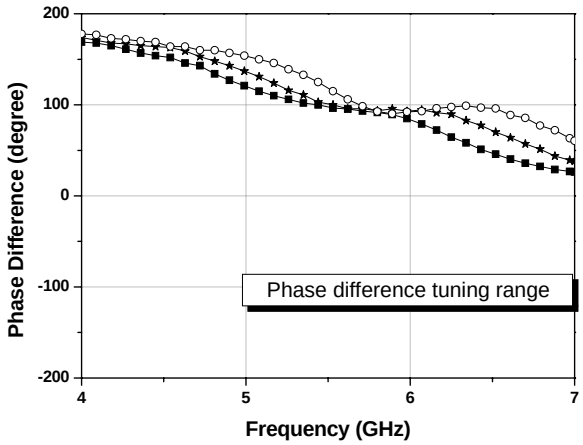

Fig. 4.25 Phase difference tuning range

Table 4.1 Summary of simulation and measurement results

Specification	Simulation results	Measurement results
Id(mA)	20.6	21mA
Central frequency(GHz)	5.3	5.4
Through loss (dB)	0.7	1
Coupling loss (dB)	0.7	-1
Return Loss S11(dB)	<-20	<-10
Isolation (dB)	<-20	<-15
Phase difference	90° ±2°	95° ~100°
Bandwidth (MHz)	500	280
Tuning Range (GHz)	5~6	5~6
Power dissipation(mW)	37	37.8
Active Area/ Die Area (mm^2)	0.33*0.5 / 0.732*0.8	NA / 0.8*0.9

4.4 Comparison and Summary

The comparison of the proposed quadrature hybrid with active inductors against recently reported quadrature hybrid is shown in Table 4.2. It indicates that the proposed quadrature hybrid provides more compact chip size, good dissipated loss and tuning range.

Table 4.2 Summary of the comparison

Ref.	Process	Freq-Range (GHz)	S11 (dB)	S21 (dB)	S31 (dB)	S41 (dB)	Phase difference	Tuning range (GHz)	Active Area/ Die Area (mm^2)
[11]	Si substrate	8.5	<-18	-4.6	-5.2	<-20	90°	No	0.6 * 0.6
[20]	GaAs	18-27	<-15	-5.5±0.5	-5.5±0.5	<-15	N/A	No	0.49 * 0.53
[21]	LTCC	2.147-2.47	<-15	-4 ~ -5.1	-2.6~ -2.89	<-15	93° ~105°	No	4.126 * 3.835
This work	0.18um CMOS	5.4	<-10	-4	-2	<-15	95° -100°	5-6	0.33*0.5 / 0.8*0.9

Chapter 5 *The Design of WiMAX Mixer with an Integrated Miniaturized Passive Balun*

Balun is useful for conversion between differential and single-ended signal. The balance LNA usually involves double power consumption than single topology. Balun, transition the single-ended input signal to differential output signal, is necessary while the LNA is single topology. On-chip balun can reduce the size of off-chip balun. Passive baluns is preferred for the reduction of power consumption in wireless system than general active baluns. In this chapter, the miniaturized balun is applied in the integration of Gilbert Mixer and implemented on 0.18 um CMOS process.

5.1 Architecture of the proposed Mixer

Fig. 5.1 shows the block diagram of the proposed Mixer. Connecting single-ended LNA and double-balance mixer, the on-chip balun is necessary. The passive loss of On-chip balun is higher than off-chip or active balun due to the worst quality-factor. The loss incurs noise penalty, however the signal incurs only a slight noise penalty because the passive loss occur after the LNA.

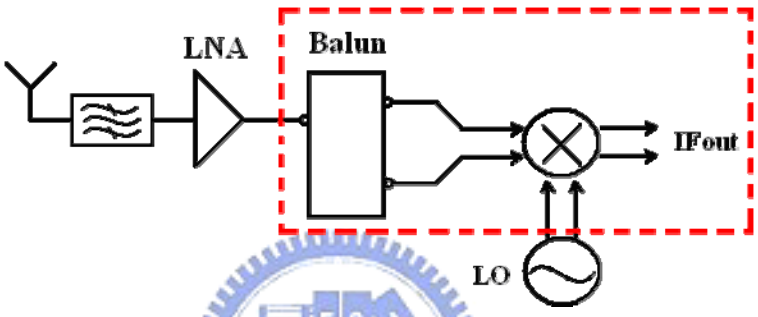

Fig. 5.1 The block diagram of the proposed Mixer

5.2 Circuit design of the proposed Mixer

5.2.1 Balun

Most balun structures utilize either distributed or lumped elements. Distributed baluns are composed of sections of λ/2 transmission line orλ/4 coupled line. These structures occupy large size especially in the integrated circuit implementation. As lumped element balun is formed with low pass filter, 90° ahead, and high pass filter, 90° behind, it always exhibit poor balun balance across frequency [26].

Recently, balun structures consisted of both distributed and lumped elements have been proposed [27]. The balun as shown in Fig. 5.2 has been investigated in [28]. By adding two capacitors C2 and C3, the coupled lines length can be reduced and two poles induce because of the coupled resonators. C1 is the input matching. Fig. 5.3 shows the S-parameter. The phase difference is as shown in Fig. 5.4. Fig. 5.5 shows the die size of the proposed balun is about 0.26*0.26 mm^2.

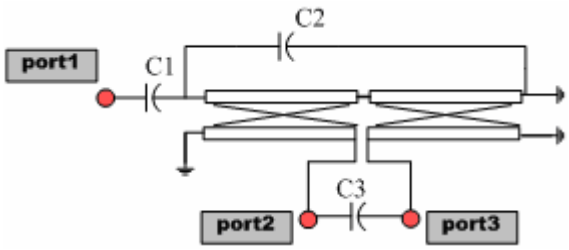

Fig. 5.2 The schematic of the proposed balun

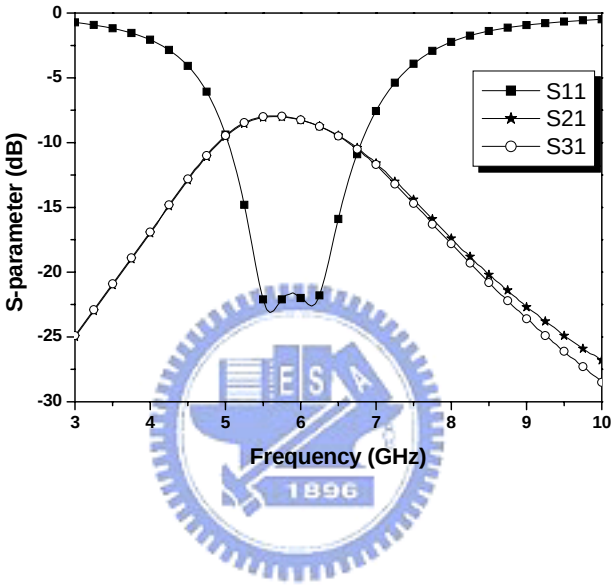

Fig. 5.3 The simulation s-parameters of the proposed balun

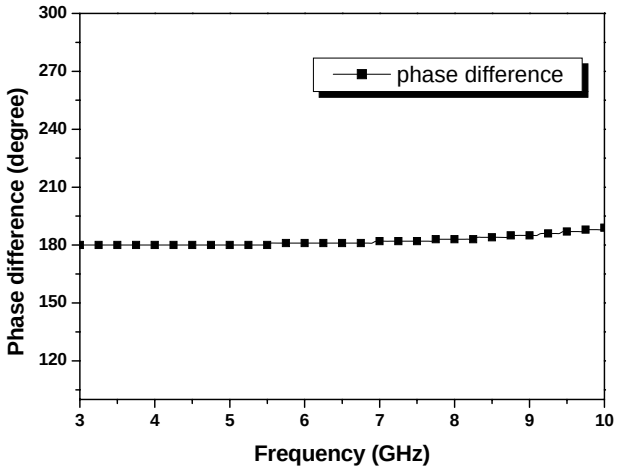

Fig. 5.4 The simulation phase difference of the proposed balun

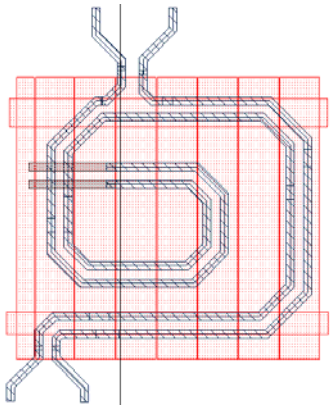

Fig. 5.5 The layout of the proposed balun

5.2.2 Input matching

Fig. 5.6 shows the input matching of single transistor commonly. From equation (5.1), the input impedance can be expressed by small signal model.

$$Z_{in} = \frac{V_{in}}{I_{in}} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{5.1}$$

Using this method in the double balance mixer need four inductors and it cost more area. Fig. 5.7 shows the input matching with balun and it needn't extra inductors to match.

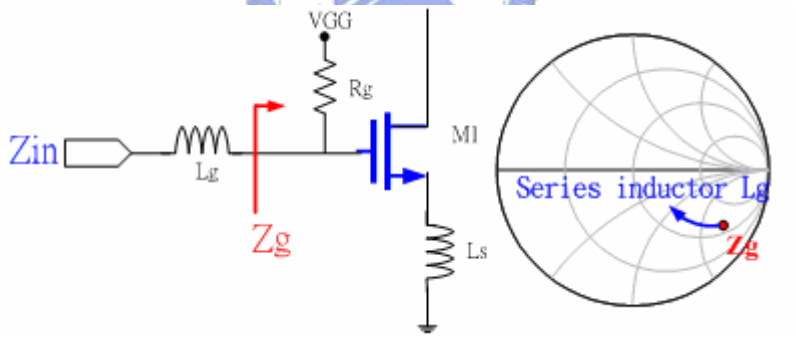

Fig. 5.6 The commonly input match with Ls and Lg

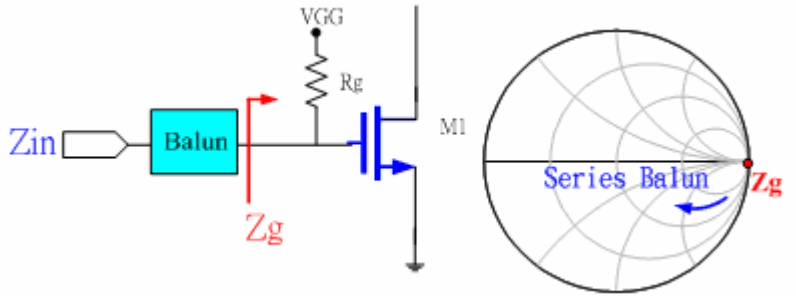

Fig. 5.7 The input match with balun

5.2.2 Double-balance mixer

The Gilbert cell topology is a typical type used in active mixers. The advantages of this topology are the high conversion gain, low LO power, and low offset voltage. The Gilbert cell mixer consists of three stages: transconductor stage, switching stage, and load stage. The linearity of Gilbert mixer is dominated by the transconductor stage as shown in Fig. 5.8. The function of three stages is described as follow. RF input stage is a differential pair that converts the RF voltage to current. The transconductance of this stage directly affects the linearity and the gain of the mixer. LO switch stage usually applies two differential pairs as modulated switch to construct double balanced structure. To achieve the goal that this two differential pairs completely switch the input power of the LO port must be larger. The value of the LO port also affects the conversion and the noise figure of the system. The output stage is load stage.

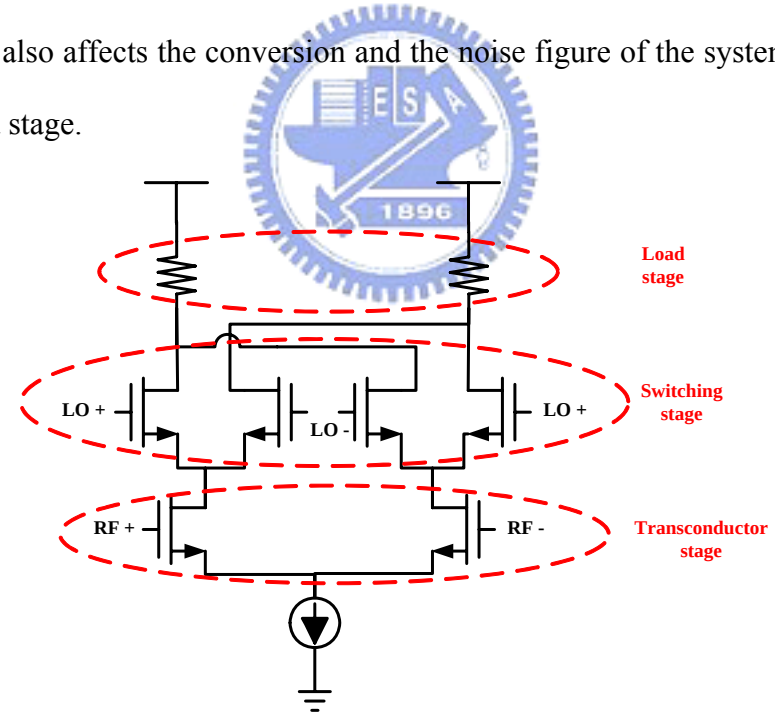

Fig. 5.8 The prototype of the CMOS Gilbert mixer

Fig. 5.9 shows the Gilbert mixer with extra current sources. M1~M2 are the transconductor stage, M3~M6 are the switching stage, Rd is load stage, and M7~M8 are the output buffer. While maintaining high gain of M1 and M2, it need extra

current sources M9 and M10 to decrease the DC current of M3~M6.

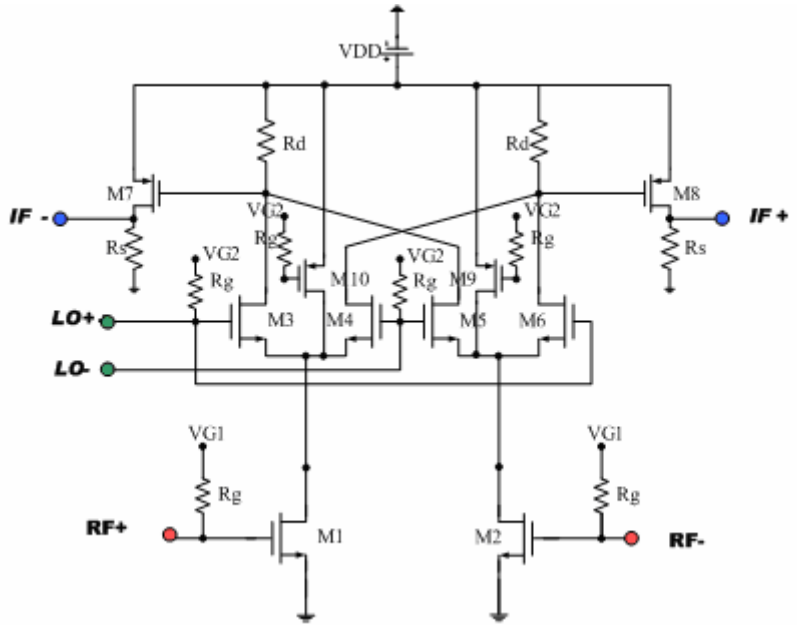

Fig. 5.9 The Gilbert mixer with extra current sources

5.2.3 The proposed Mixer

Fig. 5.10 shows the complete schematic of proposed mixer.

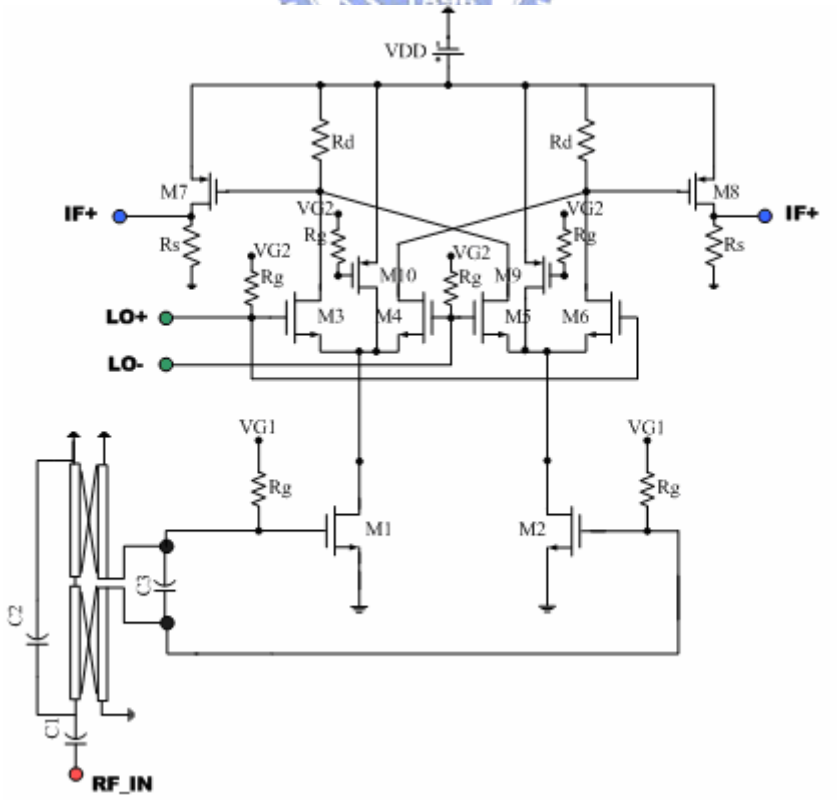

Fig. 5.10 Complete schematic of the proposed mixer

5.3 Simulation Results

Fig. 5.11 shows the layout of the proposed mixer. The size of the layout is 0.95mm by 0.6mm including pads. Considering the layout effect, we take the long layout line and run EM simulation by ADS Momentum so as to obtain the layout effect model. The mixer is designed using TSMC 0.18μm CMOS technology. The simulations were done at 1.8 V supply voltage and the power consumption is 5 mW including the output buffer.

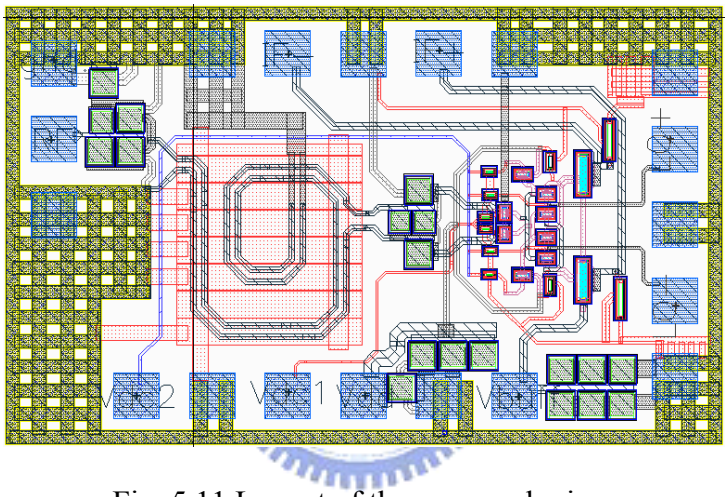

Fig. 5.11 Layout of the proposed mixer

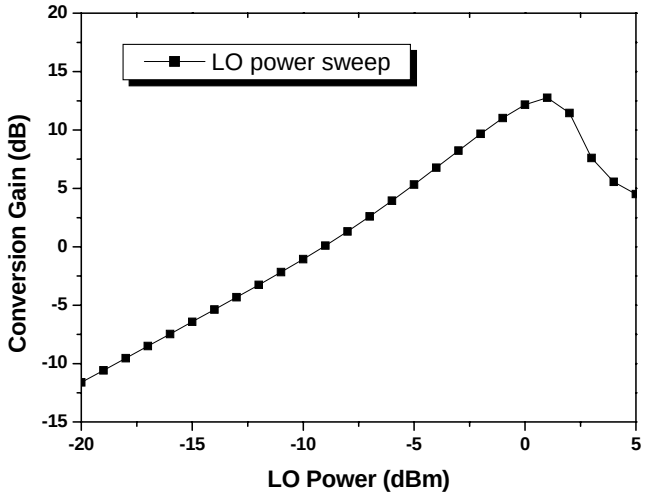

Fig. 5.12 Conversion Gain VS. LO power

Fig. 5.12 illustrates the conversion gain versus the LO power. Fig. 5.13 illustrates the conversion gain versus the RF frequency with both RF and LO ports swept in frequency from 4 to 7 GHz, a fixed IF frequency of 20 MHz, RF power of -30 dBm, and LO power of 0 dBm. Fig. 5.12 illustrates the conversion gain versus the IF frequency.

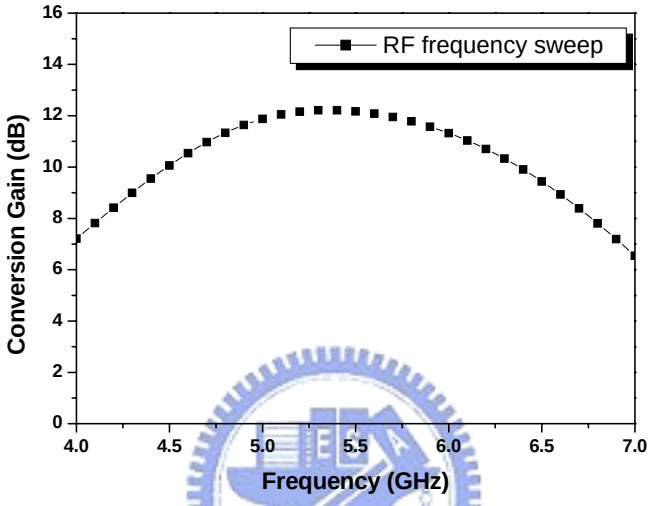

Fig. 5.13 Conversion Gain VS. RF Frequency

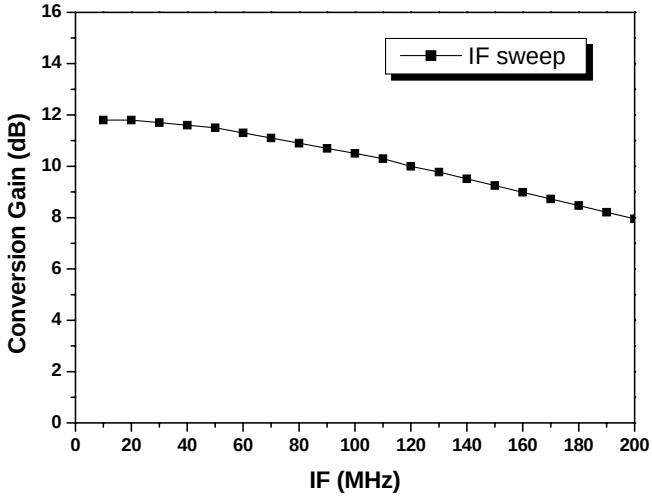

Fig. 5.14 Conversion Gain VS. IF frequency

Fig. 5.15 shows the P1dB and IIP3 when RF frequency is 5.2GHz and fixed IF frequency is 20MHz. P1dB is about -11dBm and IIP3 is about -3.8dBm. Fig. 5.16 shows the P1dB and IIP3 when RF frequency is 5.8GHz and fixed IF frequency is 20MHz. P1dB is about -11dBm and IIP3 is about -3.7dBm.

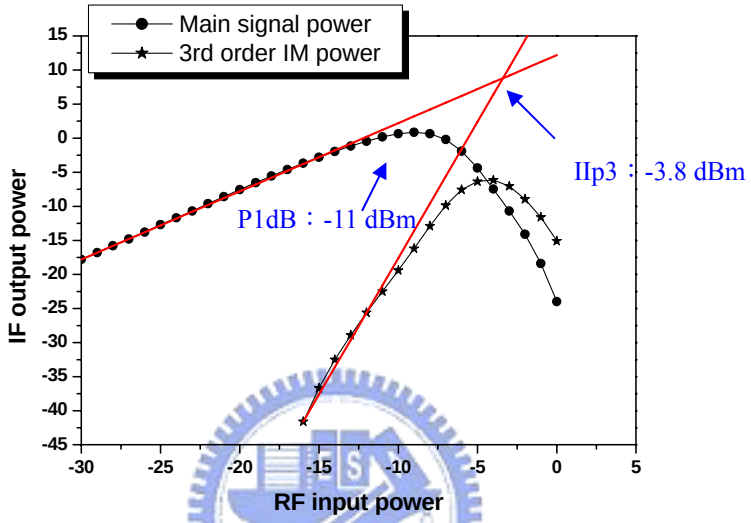

Fig. 5.15 P1dB and IIP3 at 5.2GHz

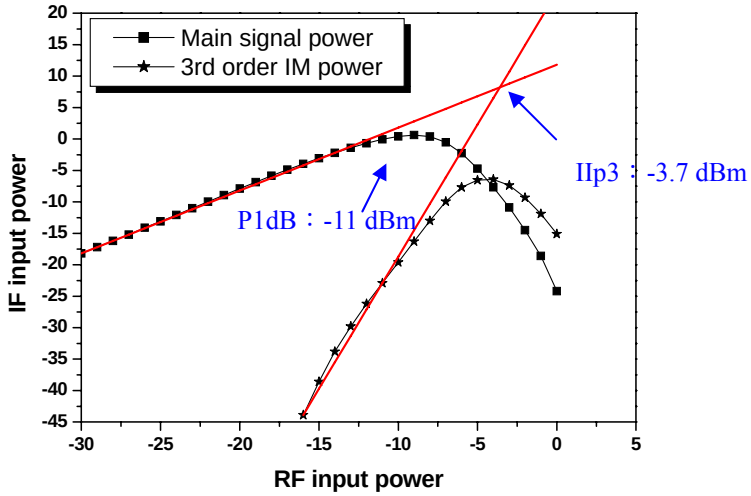

Fig. 5.16 P1dB and IIP3 at 5.8GHz

The simulated RF return loss is better than 10 dB as shown in Fig. 5.17. The simulated IF return loss are also better than 10dB as shown in Fig. 5.18. Table 5.1 is the summary of mixer simulation results.

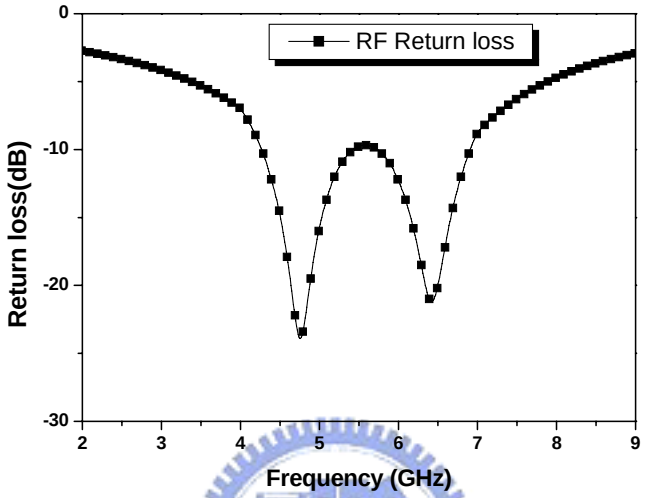

Fig. 5.17 RF Return Loss

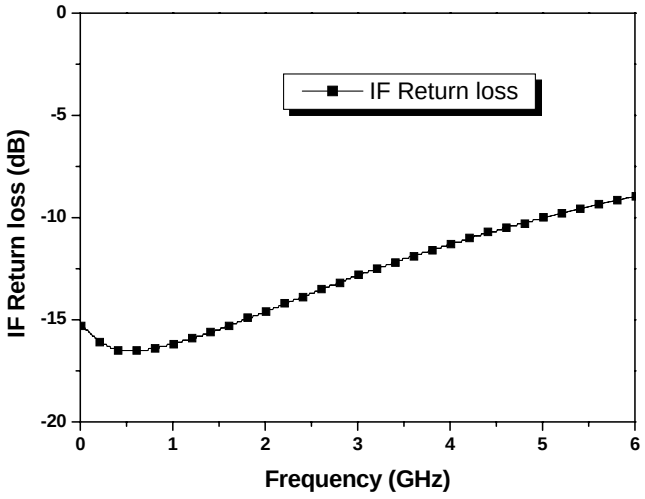

Fig. 5.18 IF Return Loss

Table 5.1 Summary of mixer simulation results

Parameters	Simulation results
Process	TSMC 0.18um CMOS
Id(mA)	2.74
Frequency(GHz)	5~6
IF Frequency(MHz)	20
Supply voltage	1.8
Power conversion gain(dB)	11.7± 0.6
RF Return Loss S11(dB)	<-10
Input P1dB(dBm)	-11
IIP3(dBm)	-3.7~-3.8
LO power(dBm)	0
Die Area (mm^2)	0.95*0.68
Power Consumption(mW)	5

5.4 Comparison and Summary

The comparison of the proposed mixer against recently reported mixer with passive balun is shown in Table 5.2. It indicates that the proposed mixer provides smaller balun size, better linearity, more compact chip size.

Table 5.2 Summary of the comparison

Ref.	Process	Freq-Range (GHz)	CG(dB)	IP1(dBm)	IIP3(dBm)	Balun size (mm*mm)	Chip size (mm*mm)
[29]	GaAs HBT	20–40	16	N/A	-7.5	0.7*1.4 (at fc=30GHz)	3.5*1.5
[30]	0.35um SiGe	3.5 to 14.5	15	-19	-7	0.66*0.25 (at fc=9GHz)	1*1
This work	0.18um CMOS	5~6	11.7	-11	-3.7~-3.8	0.26*0.26 (at fc=5.5GHz)	0.95*0.68

Chapter 6 *Conclusion*

In this thesis, we present bi-directional amplifier, quadrature hybrid, and mixer with the miniaturized balun. These proposed circuits are fabricated using a standard TSMC 0.18μm CMOS process.

In chapter 3, a bi-directional amplifier without any switch or controlled voltage for 5.8GHz applications is presented. The bandwidth of this design is about 250MHz. The bi-directional amplifier contains two identical reflection-type amplifiers and a 3-dB quadrature hybrid. The chip area is 0.96 × 1.15 mm^2. The simulation result shows the achieved gain is 11dB , return loss is under -10dB. For the poor experience in the beginning, the result is bad. Experience teaches it. The technology of layout is the key factor in the circuit design. The improved chip will be back in August. Since the lump element of quadrature hybrid cost more area in chapter 3, the miniaturized quadrature hybrid is proposed in chapter 4 to reduce chip size. By employing the active inductors, the area can be reduction and the quality factor can be improved. The size of the layout is 0.74mm by 0.81mm including pads. The measurement S11 is under -10dB and S21 is about -4dB. The measurement S41 is under -15dB and S31 is about -2dB. The phase difference between S21 and S31 is 94°~100°. The tuning range of this design is from 5GHz to 6GHz.

In chapter 5, an active mixer with miniaturized balun is proposed. The balun structure is consisted of both distributed and lumped elements. By adding two capacitors, the coupled lines length can be reduced and two poles induce because of the coupled resonators. The die size of the proposed balun is about 0.26*0.26 mm^2. The size of the total circuit layout is 0.95*0.6 mm^2 including pads. The simulation results of proposed mixer achieves power conversion gain of 11.7 ± 0.6 dB, IIP3 of -3.7 dBm, and P-1dB of -11 dBm in the power consumption of 5mW from a 1.8V power supply including the output buffer.

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