國立交通大學

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碩士論文

新型三維微機電埋藏式結構與其應用

A Novel 3-D Embedded MEMS Structure And Its Application

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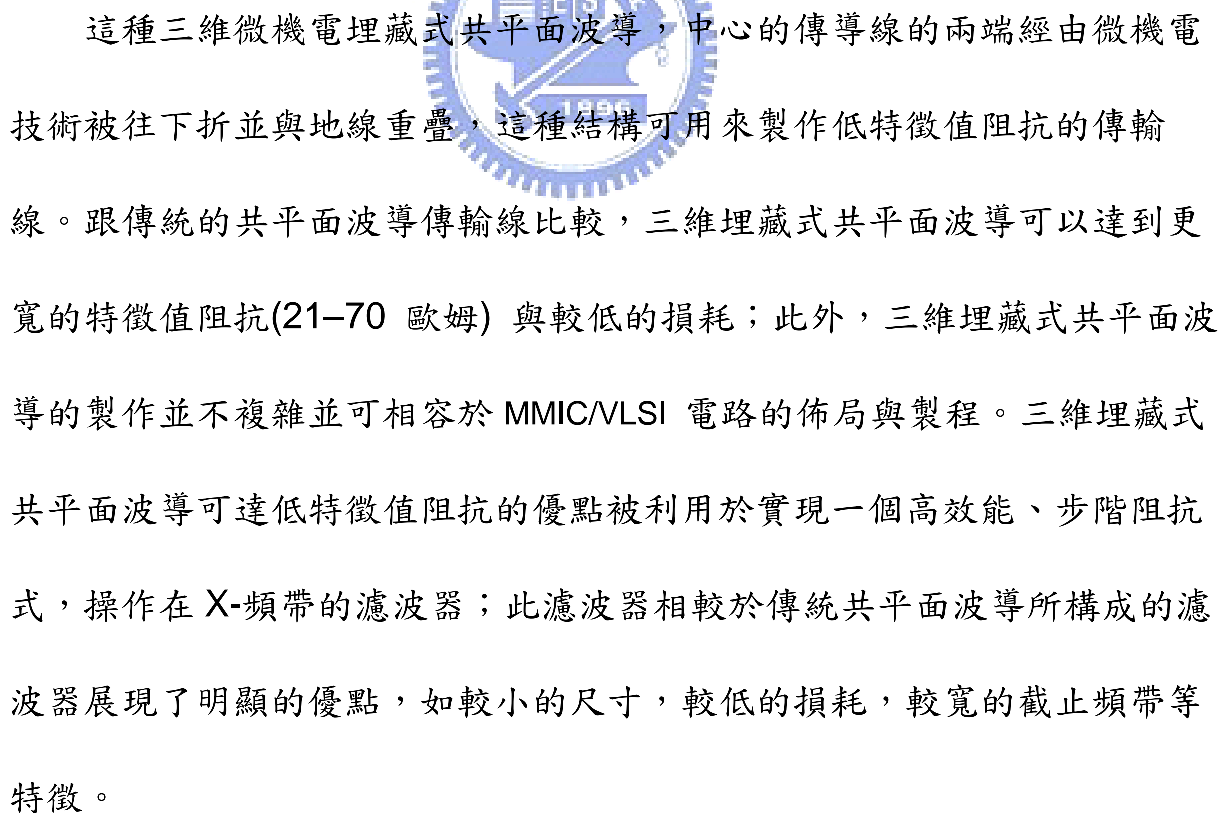
中文摘要

本論文裡提出了一種新型三維微機電埋藏式裝置與其相關的製作技術，我們利用矽的深蝕刻技術與金屬化技術來製作一種新型的共平面波導結構。

這種三維微機電埋藏式共平面波導，中心的傳導線的兩端經由微機電技術被往下折並與地線重疊，這種結構可用來製作低特徵值阻抗的傳輸線。跟傳統的共平面波導傳輸線比較，三維埋藏式共平面波導可以達到更寬的特徵值阻抗(21–70 歐姆) 與較低的損耗；此外，三維埋藏式共平面波導的製作並不複雜並可相容於 MMIC/VLSI 電路的佈局與製程。三維埋藏式共平面波導可達低特徵值阻抗的優點被利用於實現一個高效能、步階阻抗式，操作在 X-頻帶的濾波器；此濾波器相較於傳統共平面波導所構成的濾波器展現了明顯的優點，如較小的尺寸，較低的損耗，較寬的截止頻帶等特徵。



A Newly 3-D Embedded MEMS Structure And Its Application

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ABSTRACT

A novel embedded three dimensional (3-D) RF-MEMS devices and the related fabrication technology were shown in this thesis. The silicon deep etching and metallization technology were utilized to form a newly micromachined coplanar-waveguide (CPW) structure.

In these 3-D embedded CPW, the edges of the center conductors are bended down by micromachining techniques and partially overlapped with the ground plane to fabricate the low-impedance lines. Compared with the traditional coplanar-waveguide (CPW) lines, the 3-D embedded CPW lines show wider impedance range (21–70 Ω) and lower loss. Besides, the fabrication processes of the 3-D embedded CPW lines are not complex and compatible with MMIC/VLSI circuit layouts and processing. The advantages of 3-D embedded CPW for low-Zo lines are utilized to realize a high-performance stepped-impedance low-pass filter at X-band. The 3-D embedded CPW filter shows distinct advantages over the conventional CPW filter in terms of size, loss, skirt, and stop-band characteristics.

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在這兩年的碩士班生涯中，我首先要感謝指導教授周復芳老師，給予我所研究的主題相當大的支持和體諒，讓學生在碩士生涯獲益良多。並且特別感謝博士班黃俊源和陳一宇學長的耐心指點，在問題重重的兩年提供我不少研究方向，並在學業上鼓勵及給予信心。

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Chapter 1 INTRODUCTION

1.1 Background and Motivations

With the rapid growth of the microelectromechanical system (MEMS) in these years, it had been widely used in various fields, such as optical (MEMOS), Bio (BioMEMS) and RF (RFMEMS) applications. Besides, due to the increasing demands on the wireless systems, many researchers had paid a lot of attentions and efforts on the field of RFMEMS. The MEMS technology has the potential of replacing many Radio Frequency (RF) components such as switches, inductors, capacitors, phase shifters, surface acoustic wave (SAW) devices and ceramic filters used in today's mobile, communication and satellite systems. In many cases, such RF MEMS components would not only reduce substantially the size, weight, power consumption and component counts, but also promise superior performance in comparison with current technologies. In wireless and space applications complete RF systems, such as redundancy switch matrices, input multiplexers, and integrated front-end receivers, can be built with low cost, mass producibility and high reliability. Micromachining also enables new functionality and system capability that are not possible with current technologies. By using RF MEMS technology, System-on-chip (SoC) or System-in-package (SiP) wireless system can be possibly achieved. [1~3]

Due to the advantages of MEMS technology applied to RF components. This thesis uses a newly fabrication technology that is different from conventional Surface Micromachining technology. The new fabrication technology is to fabricate 3-D embedded RF-MEMS devices and it's slightly

similar to SCREAM process in Bulk Micromachining. The application of this technology is facilitate to form a newly structured CPW and a monopole patch antenna. The relative design and the characteristics are studied in detail in this dissertation.

1.2 Thesis Organization

In this thesis, MEMS technology had been employed to design and fabricate newly CPW structures and monopole antenna.

Chapter 2 is devoted to the general descriptions of the MEMS technology. The description only provides up to the level sufficient to comprehend the research work carried out in this thesis.

In chapter 3, a new 3-D embedded structure MEMS process is facilitate to form CPW and the 3-D embedded CPW line characteristics are studied in detail. To demonstrate the practical usefulness of the structure, and X-band Chebyshev seven-section step impedance low-pass filter has been designed and fabricated using low-Zo 3-D embedded CPW.

In chapter 4, the monopole patch antenna has been designed and fabricated with the 3-D embedded structure on the patch for ultra wide-band application.

In chapter 5, conclusions are made and the new ideas for further research are also suggested as the future works.

Chapter 2 Micromachining and 3-D embedded MEMS structure

2.1 MEMS Technology

From a historical point of view, I would like to refer to a paper titled "There's plenty of room at the bottom" [4], which based on a seminar given in 1959 by the famous Nobel laureate physicist Richard Feynman. This paper is usually considered as the initial idea of the Microelectromachanical systems (MEMS) technology. In that paper, Dr. Feynman considered issues such as the manipulation of matter on an atomic scale and the feasibility of fabricating denser electronic circuits for computers. He also considered the issue of building smaller and smaller tools that could make even smaller tools so that eventually the individual atoms could be manipulated.

With the rapid growth and progress of the microelectronics technology which uses the single-crystal silicon as the basic material. The ability for realization of microstructure is well-established by using suitable integrated circuit (IC) process steps, such as thin film deposition, lithography, etching and so on. In the United States, such as a micro-fabrication technology is known as MEMS, whereas in Europe, it is called Microsystems technology (MST), and in Japan it is referred as Micromachines.

MEMS technology is a multi-disciplinary technology, it includes radio frequency(RF MEMS), optical(Optical MEMS), chemistry, biology(BIO MEMS) [5] and other technologies. [6-7] Generally, it can be categorized into three

groups: surface micromachining, bulk micromachining, and LIGA (lithography, galvanoforming, moulding) [8-9]; each has their own advantages strengths weaknesses and applications [10]and will be discussed in the following subsections.

2.1.1 Surface Micromachining

Surface micromachining is a technology in which all functional features are built up on the surface of a substrate layer by layer[11,12]. This technique is based in deposition and patterning of thin film materials such as polysilicon, silicon nitride, or metallic thin film over a patterned sacrificial film such as silicon dioxide, polymer, or photoresist thin film. When the sacrificial layer is etched away, an undercut and freely suspended or movable structure can be obtained. The dimensions of these surface micromachined structures can be several orders of magnitude smaller than bulk-micromachined structures. The prime advantage of surface-micromachined structures is their easy integration with IC components, since the wafer is also used for IC elements fabrication. It should be noted that as miniaturization in immensely enabled by surface micromachining, the small mass structure involved may be insufficient for a number of mechanical sensing and actuation application.

Figure 2-1 shows the basic surface micromachining process. First a sacrificial layer is formed and patterned (Fig. 2-1a), followed by a similar process for the mechanical layer (Fig. 2-1b). Finally, the sacrificial layer is removed by sacrificial etching to leave the free standing structure (Fig. 2-1c). Note that the suitable sacrificial layer is dependent upon the mechanical layer used, with the important factor being the availability of an etchant which etches the sacrificial layer

without significantly etching the mechanical layer or the substrate. The prime advantage of surface-micromachined structures is their easy integration with IC components, because the wafer is also the working area for IC elements.

2.1.2 Bulk Micromachining

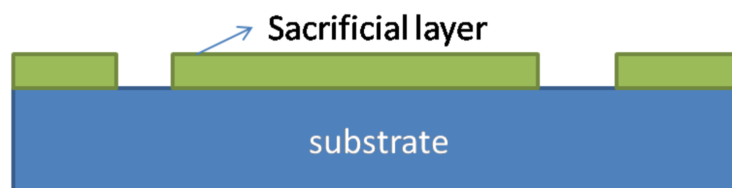
Bulk micromachining is the more mature one of the two silicon micromachining technologies. In bulk micromachining, structures are constructed by etching into a large single crystal substrate. Note that silicon is the most widely used material for substrate. The bulk micromachining technique can be divided into wet etching and dry etching of silicon according to the phase of etchants. Liquid etchants, almost exclusively relying on aqueous chemicals, are referred to as wet etching, while vapor and plasma etchants are referred to as dry etching. The term bulk micromachining comes from the fact that this type of micromachining is used to realize micromechanical structures within the bulk of a single-crystal silicon wafer by selectively removing ('etching') wafer material. The microstructures fabricated using bulk micromachining may cover the thickness range from submicron to full wafer thickness (200 to 500 μm) and the lateral size range from submicron to the lateral dimensions of a full wafer. Bulk micromachining technique allows to selectively removing significant amounts of silicon from the substrate to form membranes on one side of a wafer. Fig. 2-2 shows some typical bulk- micromachining structures. Fig. 2-2(a) and (b) show the isotropic and anisotropic etching in silicon substrate. These properties are defined by the nature of the chemical reactions, the diffusion of reactants and products, the additives, and other factors. By removing parts of the substrate, floating structures can be formed, as shown in Fig. 2-2 (c). Note that the etching

stop layer is usually used in bulk micromachining technology to control the etching depth or construct the micro-structures, such as cantilevers and membranes.

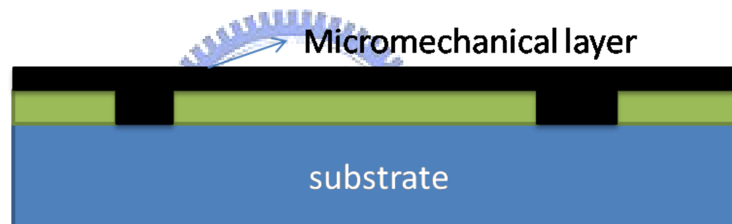
By the combination of isotropic and anisotropic etching, robust structures can be built on or “in” the silicon wafers. Besides, by removing parts of the substrate, the performance of the RF device can be enhanced due to less substrate loss. Bulk micromachining technology now has attracted interest more in integration with complementary metal oxide semiconductor (CMOS) technology.

2.1.3 LIGA

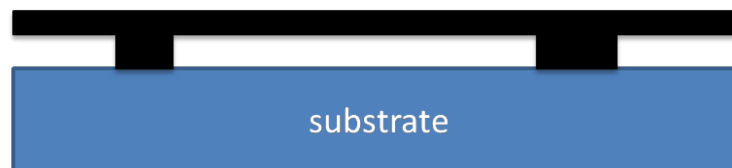
LIGA is a German acronym standing for X-ray lithographie (X-ray lithography), galvanoformung (electroplating) and abformung (molding). The principal steps of the LIGA technology are shown in Fig.2-3. First, a thick photoresist is patterned with extend exposure to X-ray radiation, and the desired structures are formed after development (Fig.2-3a). Metal is then electroplated on the exposed conductive surface of the substrate, filling the space and covering the top surface of the resist. After the photoresist is removed, the metal structure is formed (Fig.2-3b). Then, the metal structure is used as a mold insert for injection molding to form plating bases (Fig.2-3c). The plating base replica is, in turn, used to electroplate additional metal parts, and is so-called second electroforming process (Fig.2-3d). After removing the plastic part, the final product is formed. The structures with high aspect ratio can be achieved by LIGA technique without the restriction of the crystal orientation. In addition, a large variety of materials are usable, like metals, ceramics, and polymers. The replication by micromolding offers the possibility of low cost mass production.



a. Sacrificial layer deposition and patterning



b. Micomechanical layer deposition and patterning



c. Sacrificial layer removal

Figure 2-1: Schematic illustration of the basic process steps in surface micromachining

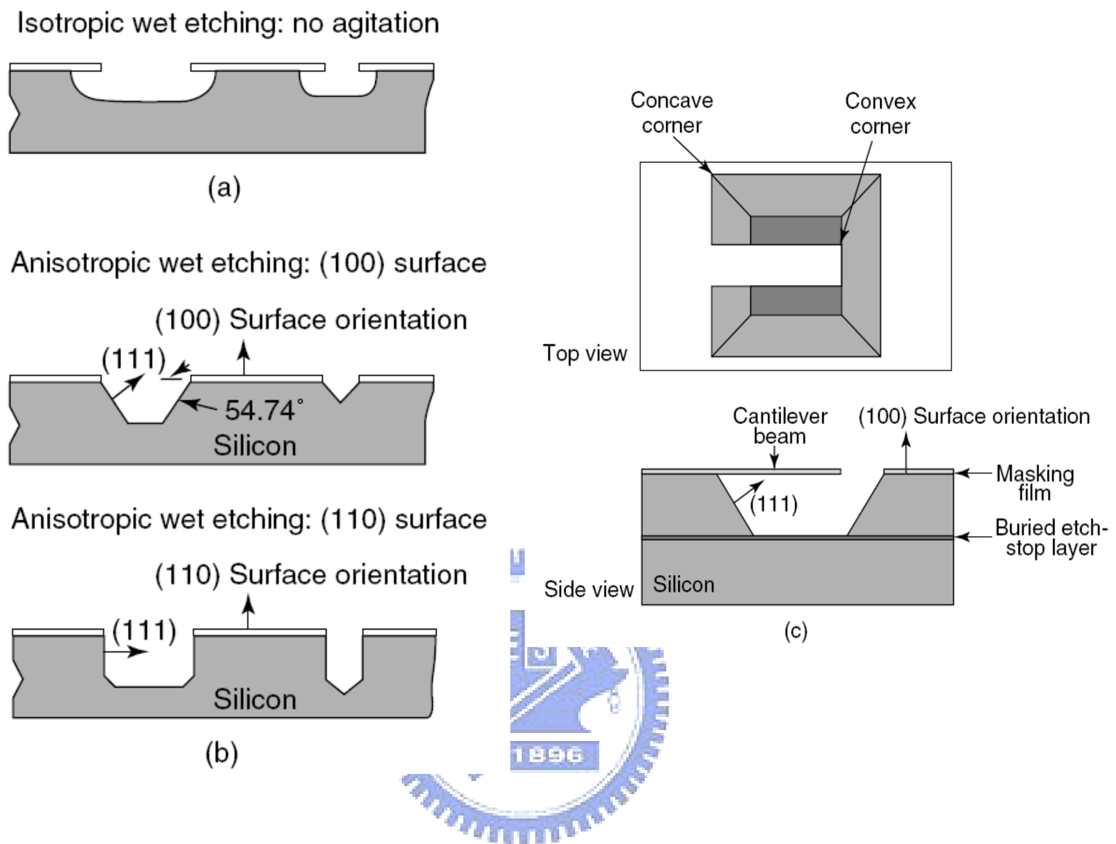


Figure 2-2: Illustration of possible bulk-micromachined structures.

(a) Rounded, isotropically etched pits in a silicon substrate.

(b) Pyramidal pits etched into (100) and (110) silicon using anisotropic wet etchants, bounded by (111) crystal planes.

(c) A Pyramidal pits etched down to a buried etch-stop layer in (100) silicon, with an undercut cantilever beam

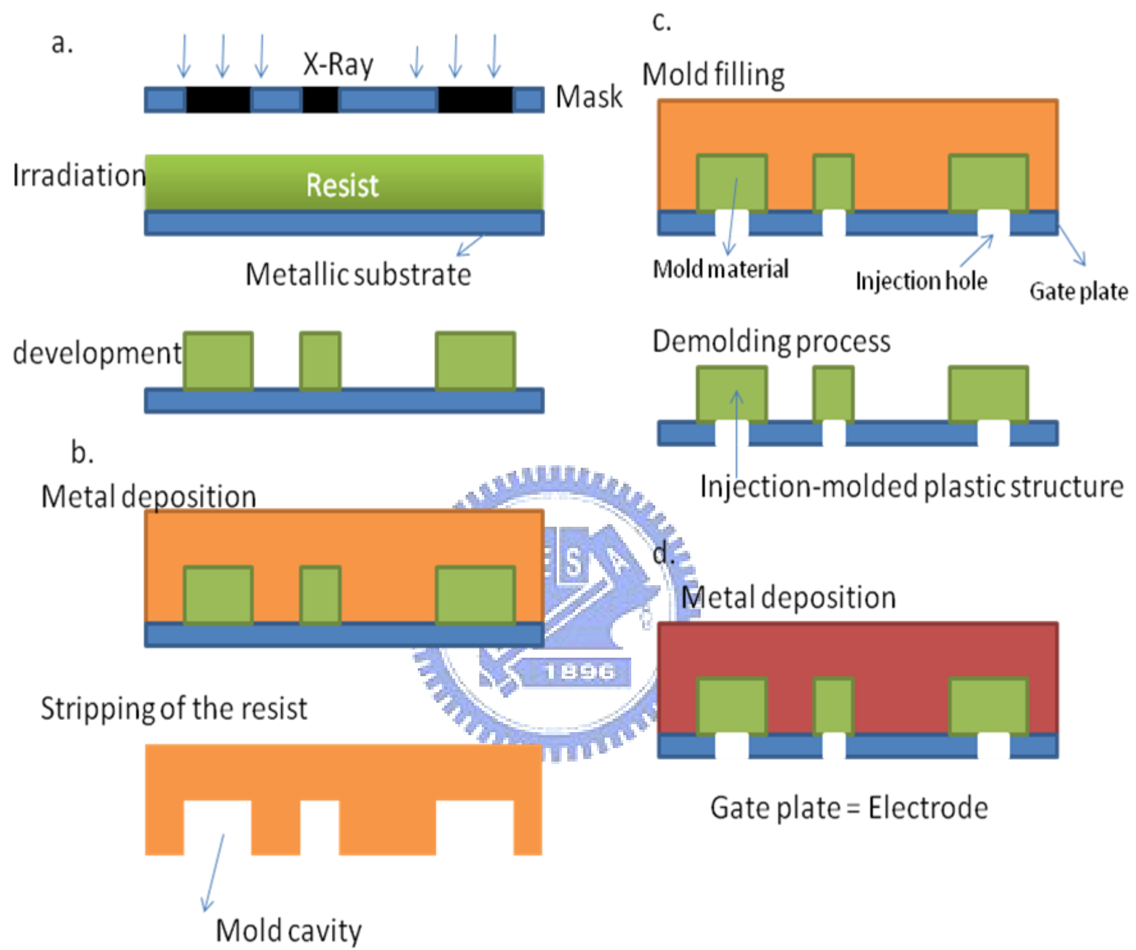


Fig. 2-3: typical sequence for the production of microstructure based on the LIGA technique

2.2 3-D Embedded MEMS technology

2.2.1 Introduction

VLSI and microwave monolithic integrated circuit (MMIC) applications require efficient use of chip real estate. Due to ever-increasing circuit densities, MMIC and VLSI designers seek to maximize the utility of the available space. This is demonstrated by the growing use of three-dimensional microstructures for CMOS trench isolation [13], V-grooved silicon solar cells [14], VMOS FET channel regions [15] and optical waveguides [16].

The trench waveguide structure was first described in1988 [17]. Trench waveguide is a three-dimensional interconnect structure, utilizing not only the surface area of the substrate but also the unused bulk of the substrate. However, the related research about the trench waveguide structure is rarely found. In this thesis, the fabrication steps of the trench waveguide are varied and simplified. The fabrication steps of the 3-D embedded CPW lines are shown in the following sections, and its characteristics are also studied in detail.

The advantages of trench waveguide as a circuit interconnect include the following features:

(i) Compatibility with MMIC/VLSI circuit layouts and processing

(ii) Ability to realize low characteristic impedances

(iii) Reducing current density near conductor strip edges, thus reducing conductor loss

(iv) Allowing the use of thick substrates during processing, thus reducing the damage during handling and enhancing the yield of production.

(v) Eliminating the need of via holes, thus reducing associated parasitics.

(vi) Exempting from crosstalk due to the presence of ground plane between any adjacent lines.

2.2.2 Metal deposition

Chemical Vapor deposition (CVD) and Physical Vapor Deposition (PVD) are two kinds of metallization technologies used in IC fabrication processes. They are different in reaction mechanism and deposition characteristics. Both of them will be described concisely as follows.

Chemical Vapor Deposition (CVD) is the process of depositing a solid film on the wafer surface through a chemical reaction of a gas mixture. The wafer surface or its vicinity is heated in order to provide additional energy to the system to drive the reactions. There are several essential aspects of CVD listed in below.

1. Chemical action is involved, either through chemical reaction or by thermal decomposition
2. All material for the thin film is supplied by an external source.
3. The reactants in a CVD process must start out in the vapor phase.

The fundamental CVD reactions have following steps and the explanations of the reaction mechanism are also shown in it.

1. Transport of the reactants by forced convection to deposition region.
2. Gas-phase reactions leading to the formation of the film precursors and by-products.
3. Mass transport of the precursors to the growth surface of the wafer.
4. Adsorption of the precursors to the wafer surface.
5. Surface diffusion of film precursors to the film growth sites.

6. Surface process, including chemical decomposition or reaction, surface migration to attachment sites, site incorporation, and other surface reaction.
7. Desorption of the by-products of the surface reactions.
8. Transport of byproducts by diffusion through the boundary layer and back to main gas stream.
9. Transport of byproducts by forced convection away from the deposition region.

CVD is widely used to deposit metal layers. Metal CVD is a conformal deposition and has well gap-filling ability. It is usually used to fill the contact via thus formed the plug between adjacent metal layers. However, due to its conformal deposition and well gap-filling capability, metal CVD is not suitable for our applications in fabricating 3-D CPW structures..

Physical Vapor Deposition (PVD) is the process of depositing thin films by means of heating or sputtering the solid target into vapor phase and then condenses on the surface of the substrate. The condensing of the vapor thus can form a thin film on the wafer surface. There are several differences between PVD and CVD. PVD techniques are generally more versatile than CVD methods, allowing for the deposition of almost any material. The constituent species, individual atoms or molecules, are produced by either evaporation of a solid or the atoms from a source “target”. These atoms or molecules then travel though a vacuum or a very low pressure gas phase, impinge on the wafers, and condense on the surface to form the film. CVD has better step coverage of deposited thin film and PVD has better film quality. There are two methods of PVD metal deposition, Evaporation and Sputtering. In IC metallization process, sputtering is the most common PVD process. Because sputtering process can deposit high quality metal layers also the uniformity and reliability are very good.

Besides, sputtering has better step coverage than evaporation. Though that the sputtering can not achieve conformal deposition as metal CVD do. It becomes a benefit to our applications surprisingly. DC sputtering thus is chosen as the best candidate to do the metallization process in this thesis due to its limited step coverage.

Step coverage is a measurement of the deposited film reproducing the slope of a step on the substrate surface. It's a very important parameter of the PVD process. Fig. 2-4 shows the definition of aspect ratio, side-wall step coverage, bottom step coverage, conformality and overhang. Step coverage depends on the arriving angle and the surface mobility of the precursor. The arriving angle mentioned above is shown in Fig. 2-5. As we can see that angle A has the largest arriving angle, 270°, and the angle C is the smallest. When the source material diffuses through the boundary layer, more source material will arrive to angle A than angle C. If source material react immediately after absorb to the wafer surface and without movement, angle A will have more deposition than angle C and overhang will be formed as shown in Fig.2-6. Overhang is not expected. Because overhang on each side of the trench top will soon merges and causes a void (keyhole). By reducing the process pressure, MFP of precursor will increase. When MFP is longer than the gap depth, there will be few collisions inside the gap. Therefore precursors have little chance to go backward to reach corner A from inside the gap. This will efficiently reduce the arriving angle and improve the step coverage.

As mentioned in above paragraph, poor step coverage is unexpected in VLSI process. Because it will cause voids in metal layer then increase the metal resistivity and cause defects and reliability problems. Thus, evidently evaporation is not suitable for our application. In this thesis we will take the

advantage of limited step coverage of metal deposition of sputtering. The desired 3-D embedded structure is mainly relying on the utilization of this limited step coverage and the details will be shown in the following subsection.

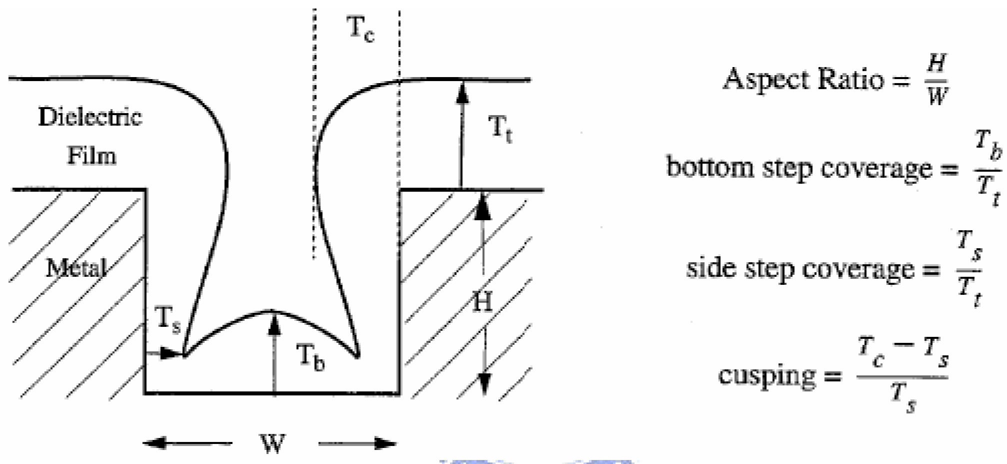


Fig 2-4. The phenomenon and the definition of step coverage

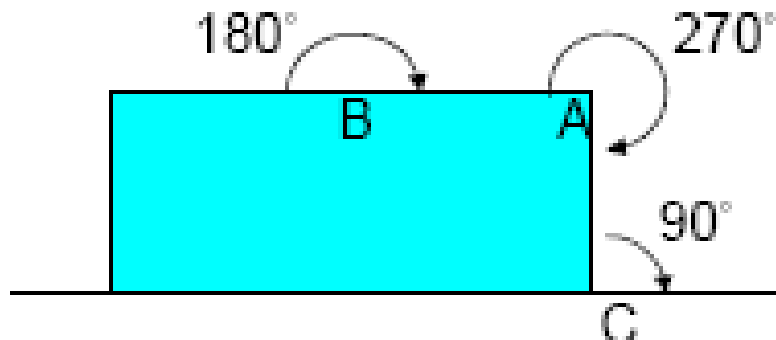


Fig 2-5. The arriving angles at the each corner.

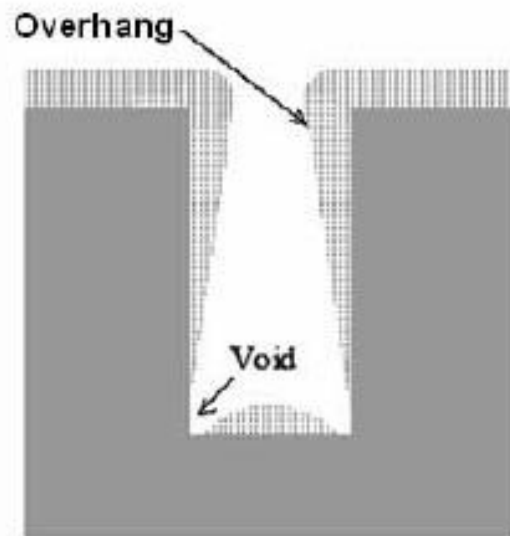


Fig 2-6. Overhang and void formed during thin film deposition.

2.2.3 Utilization of limited step coverage

As mentioned in last paragraph, we expect conformal deposition than limited step coverage deposition in semiconductor fabrication. But the characteristic of limited step coverage deposition can be utilized to form the 3-D embedded RF-MEMS devices that will be demonstrated latter in this thesis. As shown in Fig. 2-7, when the trench is deep enough, the aspect ratio of the trench will be larger than the ability of sputtering. Thus, a discontinuity will start to appear at the bottom of the side wall of the trench after thin film deposition. It means that terminal A and B in Fig. 2-7 are disconnected and there is a big

parallel plate capacitor in the trench. Hence, it can be utilized to form a strong coupling, or tight coupling structure.

Fig. 2-8 (a) ~ (d) are the SEM pictures of Cu film deposition with DC sputtering onto the trenches with different aspect ratio followed with XeF_2 isotropic etching. Note that the XeF_2 isotropic etching can make us observe the depth of the deposited Cu film in the trench more easily. Besides, we can use such isotropic etching to remove the silicon underneath the CPW lines for improving its performance in the future. In Fig. 2-8, we can find that the aspect ratio of the trench must be larger than 4 so that the discontinuity could happen. It is worthy to note that this result is just suitable for certain process condition, if we modify the conditions of thin film deposition, such as pressure, gas flow and so on, the minimum aspect ratio of the trench would be different. Thus the different size of parallel plate capacitor can be achieved.

A lot of RF passive devices can be constructed by using the high coupling structure. For example, low impedance transmission line, DC block, filter, lateral type switch/relay, phase shifter …etc. Hence, we believe that we can have smaller RF passive devices with better performance by using such 3-D structure.

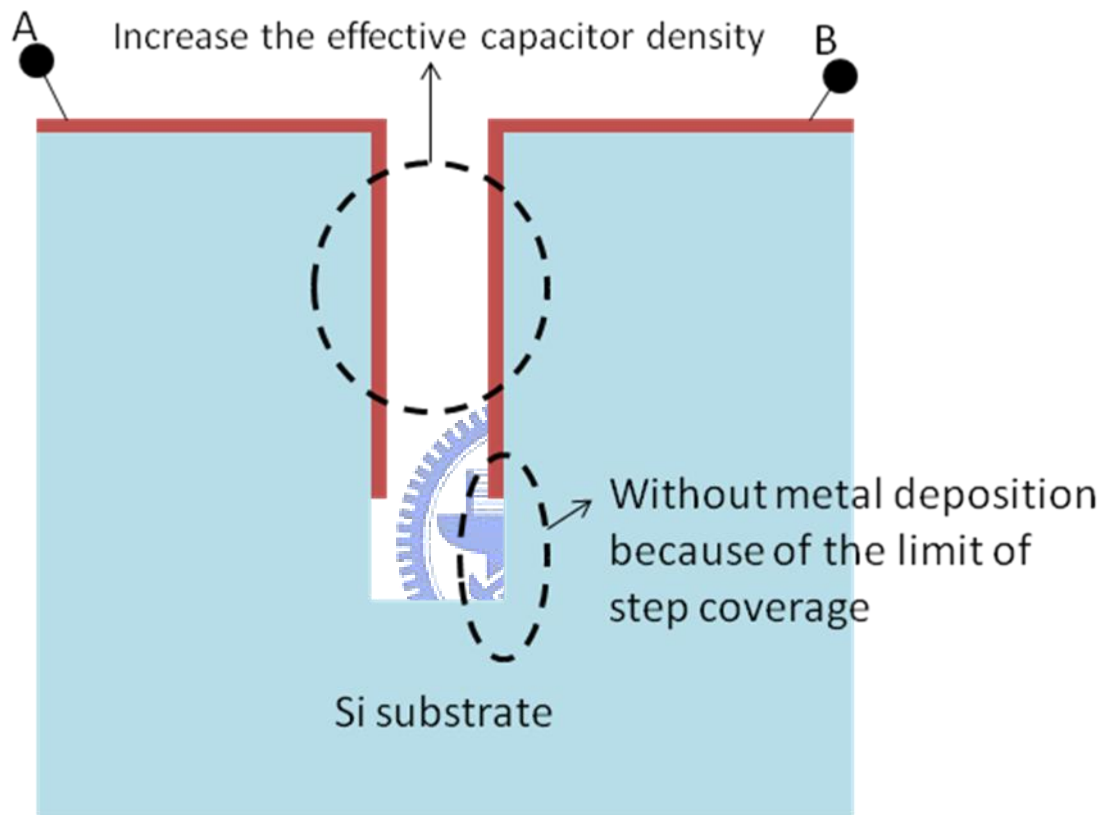


Fig. 2-7 Explanation of the utilization of limited step coverage

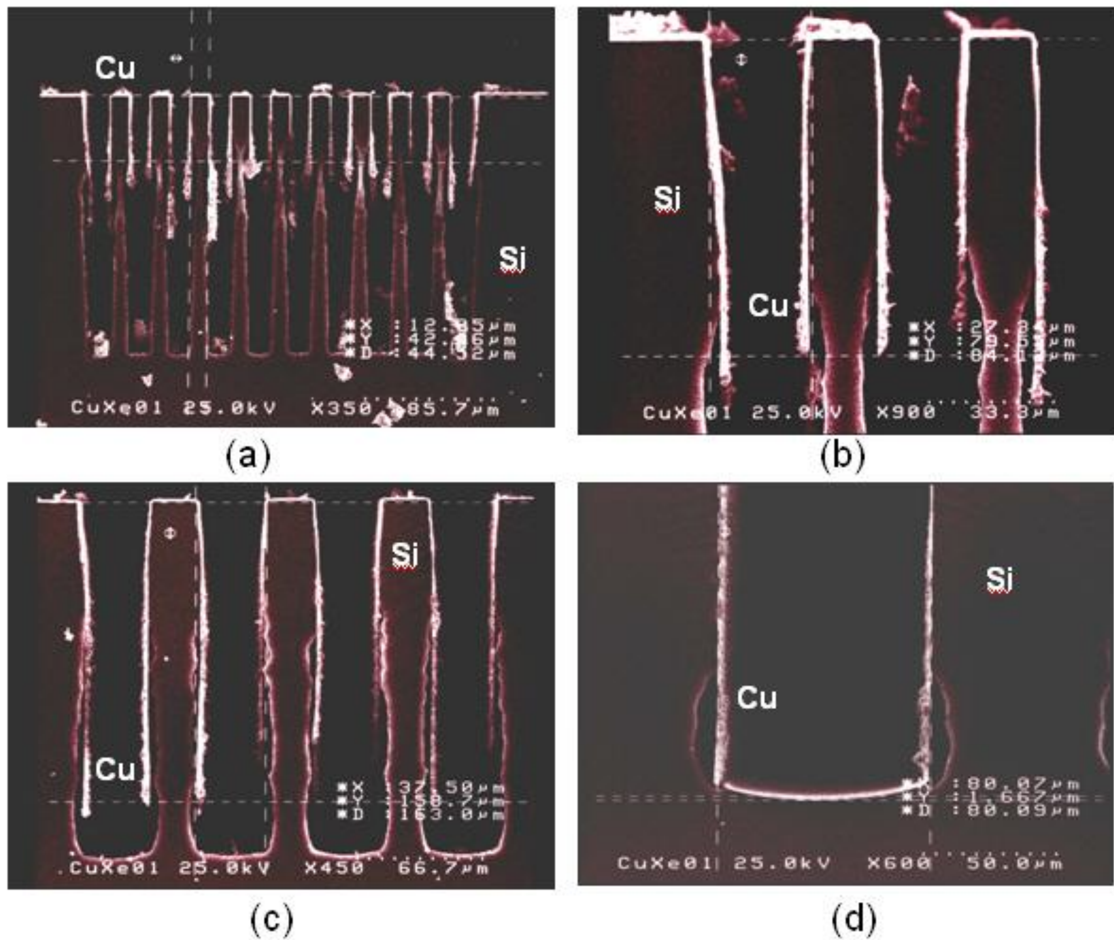


Fig. 2-8 (a) ~ (d) are the SEM pictures of Cu film deposition with DC sputtering onto the trenches with different aspect ratio followed with XeF_2 isotropic etching.

Fig. 2-8 SEM picture of step coverage phenomenon

Chapter 3 3-D Embedded CPW

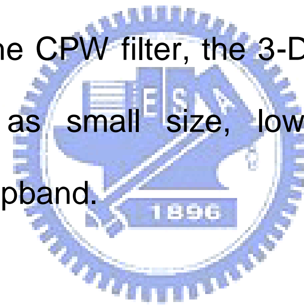
3.1 Introduction

Conventional coplanar-waveguide (CPW) has been widely used in microwave and RF system. But it suffers from high conductor losses at high and low characteristic impedance extremes due to its narrowing of the center conductor and slot width, respectively [13], [14]. Moreover, very low-Zo lines are practically impossible to realize in CPW due to the minimum slot size limit imposed by the fabrication process. Therefore, designers are often restricted in their choice of impedance values when designing monolithic-microwave integrated-circuit (MMIC) circuits with CPW.

There were several papers trying to reduce the losses of the high-Zo lines, by different ways [15]–[17]. As far as the low-Zo lines are concerned, a way to elevate the edges of the center conductors and partially overlapped with the ground plane had created and showed great line characteristics. The overlap between signal and ground lines makes very low-Zo lines possible without the slot size constraint. However, the fabrication process is complex and it can't be facilitate to SoC system.

In this thesis, a new 3-D embedded CPW structure, in which the edges of center conductor are partially bended and overlapped with ground, as shown in Fig. 3-2(f). The broad ranges of characteristic impedance and low losses can be achieved by using such 3-D structure. The structure used in this thesis is sample comparing to other relative low-Zo CPW lines structures. Only 2 masks are needed.

The loss characteristics of the 3-D embedded CPW lines are studied in detail for various dimension values. Field simulations and comparative experiments have been performed to fully characterize the 3-D embedded CPW lines. An X-band Chebyshev seven-section stepped-impedance low-pass filter (LPF) is simulated and fabricated by using the low-Zo 3-D embedded CPW lines. To demonstrate the practical usefulness of the 3-D embedded CPW, an X-band 0.5-dB equiripple Chebyshev seven-section stepped-impedance low-pass filter (LPF) has been designed and fabricated using low-Zo 3-D embedded CPW lines. It is shown that low-Zo 3-D embedded CPW lines can be used as lumped capacitors, which help to solve the inherent problems of the LPF using distributed structures, such as low cutoff rates and poor attenuation in the stopband. Compared with the CPW filter, the 3-D embedded CPW filter shows distinct advantages such as small size, low insertion loss, sharp skirt characteristics, and wide stopband.



3.2 Conventional CPW

The coplanar waveguide (CPW) was invented by Wen [18] in 1969 as a novel surface strip transmission line fabricated on a dielectric substrate. The CPW transmission line has demonstrated several advantageous features over the conventional microstrip line, for instance, easy surface mounting of external devices, easy fabrication of both shunt and series passive elements, low-frequency dispersion, and easy adjustment of desirable characteristic impedance. Since its proposal, the CPW technology has been progressively gaining a tremendous application in exploration of advanced RF and microwave integrated circuits, modules, and subsystems. For this purpose, much effort has

been carried out to construct a new variety of modified CPW transmission lines with varied cross-sectional configurations and accurately characterize their propagation performance in theory and experiment, as summarized in two relevant books [19,20]. In particular, various static and fullwave methods have been effectively developed to deal with these inhomogeneous transmission lines and derive the two per unit length transmission parameters, i.e., effective dielectric constant and characteristic impedance.

GEOMETRY AND ANALYSIS

The conventional CPW transmission line [18] consists of the central strip conductor and the two infinite-width ground planes on two sides that are formed in close proximity on the same surface of a dielectric substrate with finite height. By equalizing the electric potentials at the two ground planes, only the even symmetric dominant CPW mode can be excited. At high frequencies, this CPW mode becomes non-TEM with a longitudinal component of magnetic field. In such a case, the tangential magnetic field, on the surface of the coupled slots between the strip conductor and two ground planes, becomes elliptically polarized.

In Wen's work [18], the relative permittivity is assumed much larger than the unity ($\varepsilon_r \gg 1$) so that the finite height of a substrate can be reasonably treated as the infinity ($h \to \infty$) for simplifying the theoretical analysis. But, in practice, ε_r and h have to be finite as shown in Fig. 3a. Also, the actual ground width of this CPW is usually finitely wide so as to formulate the call finite-ground CPW or FGCPW as shown in Fig. 3b.

Up to present, relative work in theory has been done to characterize

a variety of CPW transmission lines in terms of per unit length characteristic impedance and propagation constants by developing the quasistatic and full-wave analysis approaches [19,20]. The quasistatic conformal mapping technique was initially utilized to model the CPW line with infinite dielectric thickness. However, an accuracy of larger than 1% for a wide range of physical dimensions and dielectric permittivity is achieved as compared with that of the full-wave spectral-domain method [21]. Of vital importance, this technique gives rise to analytical expressions for effective dielectric constants and characteristic impedance in terms of the ratio of complete elliptic integral of the first kind and its complement, K(k)/K' (k), where k is the variable.

The detailed mathematics of this procedure can be found in the literature [e.g., 1–7] and are not discussed here. In this section, the infinite-ground CPW is characterized by the three sets of closed-form design formulas in Figs. 3-1a with respect to various physical dimensions. The analytical expressions of the ratio K(k)/K' (k), are provided below in two different regions of the variable k for infinite- and finite-width-ground CPWs:

$$\frac{K(k)}{K'(k)} = \frac{\pi}{\ln[2(1+\sqrt[4]{1-k^2})/(1-\sqrt[4]{1-k^2})]} \quad (0 \le k \le 0.707) \qquad \text{(1-a)}$$

$$\frac{K(k)}{K'(k)} = \frac{\ln[2(1+\sqrt{k})/(1-\sqrt{k})]}{\pi} \quad (0.707 \le k \le 1) \qquad \text{(1-b)}$$

For conventional CPW with infinite-width ground as in Fig. 3-1a, the two variables k_1 and k_2 are defined in terms of the dimensions a, b, and h, respectively, where the strip width W=2a and S=b-a:

$$k_1 = \frac{a}{b} \quad (2\text{-a})$$

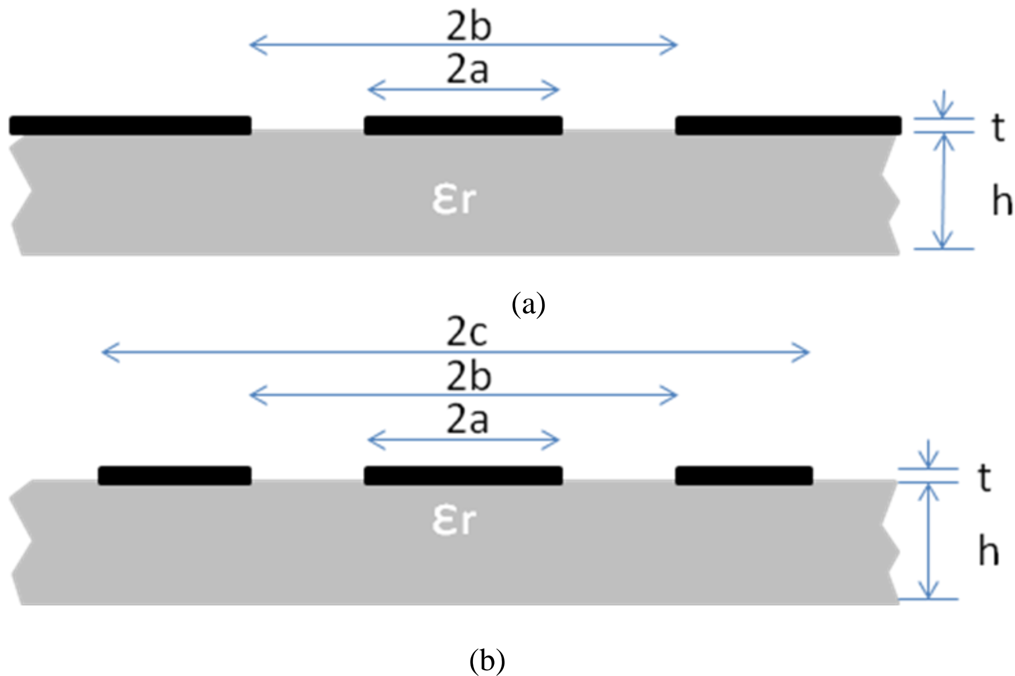
$$k_2 = \frac{\sinh(\pi a/2h)}{\sinh(\pi b/2h)} \quad (2\text{-b})$$

As such, the per unit length effective dielectric constant and characteristic impedance can be deduced:

$$\varepsilon_{re} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K(k_2)}{K'(k_2)} \frac{K'(k_1)}{K(k_1)} \quad (3)$$

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{re}}} \frac{K'(k_1)}{K(k_1)} \quad (4)$$

By verifying the results of Eqs. (3) and (4). The impedance (Zo) definitely increases as the slot is widened for all the four listed h/W because of reduced capacitive coupling between the strip conductor and two ground planes. As h/W increases, the Zo curve converges to that with very thick thickness (h/W=20). Meanwhile, the effective dielectric constant (ε_{re}) falls down as the slot width is enlarged under the fixed finite thickness (h/W) and it eventually becomes almost independent of h if h/W is larger than 20. It can be further deduced from these results that the effect of finite dielectric substrate is almost ignorable if h exceeds 2b=W+2S.



(b)

Fig. 3-1 Cross section view of (a) infinite-ground CPW; (b) finite- ground CPW

3.3 Modified CPW comparison

In the section, six different modified CPW which have many promising features for applications in high-performance at millimeter-wave are mentioned and described briefly. The theoretical characteristics of multilayered CPW transmission lines have been reported in the literature [5–7]. In this paragraph, two of these CPW structures that exhibit enhanced electrical performance such as elevated and insulated CPW, are discussed here (check cross-sectional views in Fig. 3-1(a) (b)). The elevated CPW in Fig. 3-2a is proposed [22] for construction of a nonlinear transmission line fabricated with Schottky diodes on GaAs substrate. This CPW has several attractive features such as low loss, high wave velocity, and broad frequency bandwidth. By using the full-wave approach, its propagation performance is characterized with respect to varied elevated

heights [23]. The CPW is fabricated on silicon substrate for low-cost application in radio frequency integrated circuits (RFICs). Due to high attenuation, the CPW is usually constructed by forming an insulated layer, such as low-loss polyimide [24] or SiO_2 [25], above the silicon substrate, as shown in Fig. 3-2b. The measured results show that attenuation can be reduced if the insulated layer is thick relative to the strip and slot widths [24].

The silicon micromachining technique has been developed to effectively remove the lossy substrate or dielectric material below, above, or around the coupled apertures in CPW in an effort to minimize propagation loss and reduce frequency dispersion. Fig. 3-2c shows the micromachined CPW [26], where the material underneath the coupled apertures is partially removed for construction of the free-space V-shaped grooves. This resulting line minimizes the total propagation loss since the EM fields are distributed mainly in the lossless V-shaped region and current density flow on the conductor is reduced. Fig. 3-2d shows a practical microshielded membrane CPW that is fabricated by attaching two silicon wafers together [3, 26]. The upper wafer, with a metallized cavity, supports a membrane with the CPW. Because of an extremely thin electric membrane, the overlapping capacitances between the top ground planes and cavity sidewalls are very large in the microwave region, thus virtually short-circuiting the overlapped region. The lower wafer is metallized on the top surface and provides the bottom wall of the cavity. Fig. 3-2e shows a micromachined overlay CPW [27]. By partially elevating the edges of the central conductor and further overlaying them with the two outer ground planes, this CPW has a lower propagation loss because the current density is redistributed on the conductors and the impedance range widens. At last, Fig. 3-2f shows the three-dimensional CPW [28]. By etching the trench and angle evaporation, the

structure can be fabricated. The overlay zone between central conductor and ground planes are within the trench. The loss reduction concept is similar to the structure in Fig. 3-1e. But, by doing so, the specified orientation of wafer is needed and two angle evaporation processes enlarge the complexity of the transmission line fabrication. Such a process can not be applied and integrated with other devices for further applications.

In this thesis, the focus is on the design and fabrication of 3-D embedded structure. The complete analysis of the structure is shown in the following section.

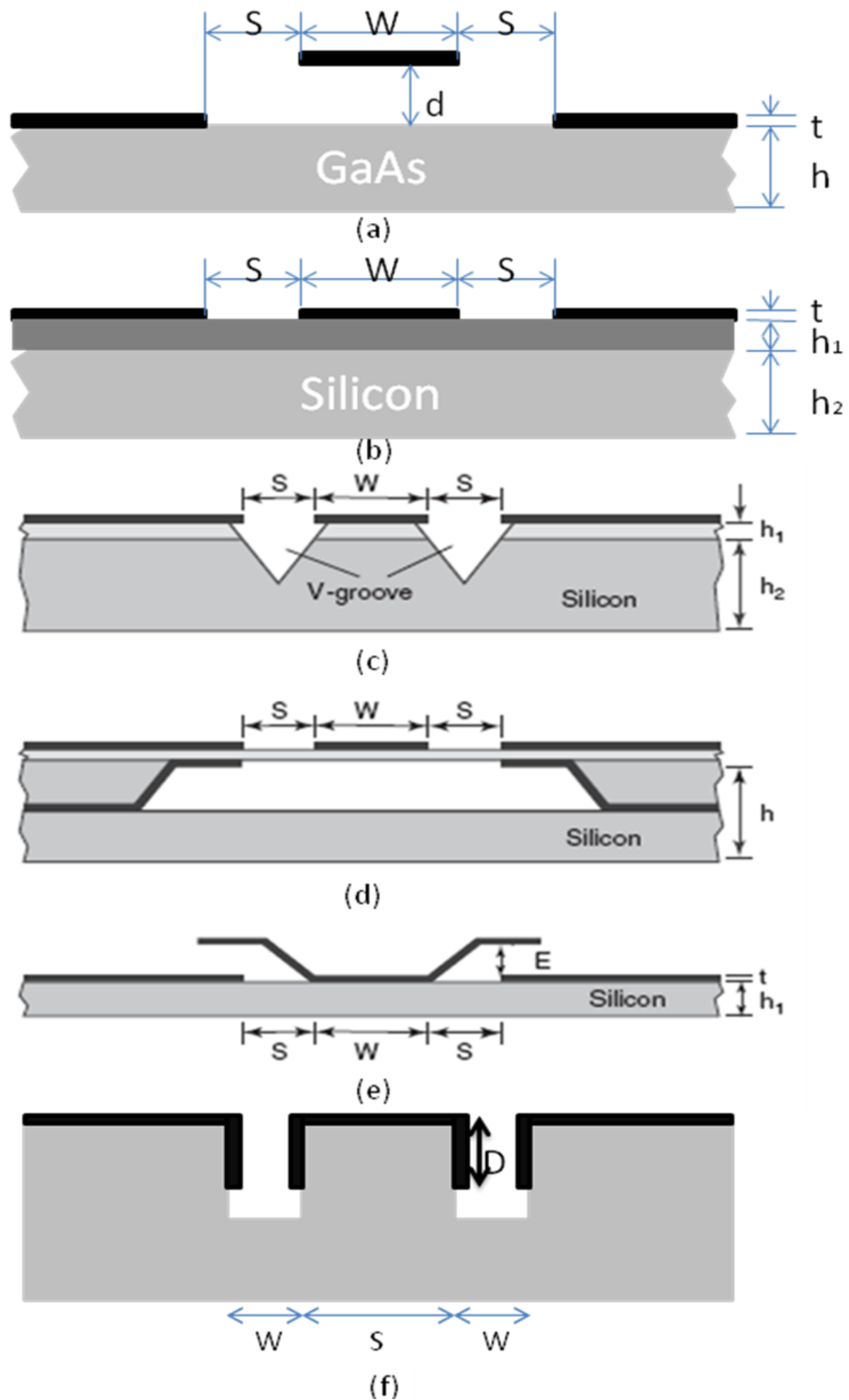


Fig. 3-2 Cross-sectional view of different CPW transmission lines (a) elevated CPW; (b) insulated CPW; (c) micromachined CPW with V-shaped groove; (d) microshielded membrane CPW; (e) micromachined overlay CPW; (f) 3-D embedded CPW

3.4 Newly Structured CPW

3.4.1 Simulation Results

The schematic of a 3-D embedded CPW is shown in Fig. 3-3 together with the associated parameters. The edges of the center conductor and ground plane are partially bended using micromachining techniques and two of them are overlapped with each other. It can be easily varied the characteristic impedance from high-Zo to low-Zo by increasing the overlap ("D" in Fig. 3-3) between the center conductor and the ground. The 3-D embedded CPW helps to reduce the conductor loss by reducing the field concentration and current crowding at the edges of the signal lines. Moreover, the 3-D embedded CPW is expected to reduce not only the conductor loss, but also the substrate loss by confining the electric field in the air between the overlapped conductor plates.

The loss analysis of both the 3-D embedded CPW (W=10, 20 and 30μm ; D= 5, 10, 20, 40, and 80μm) and CPW (and W=40, 30, 20, 5 and 2μm) lines is performed using a 525-μm-thick silicon substrate (ε_r=11.9) and the metal plane thickness is set to be 1μm. In the 3-D embedded CPW, the width of the center conductor touching the substrate is fixed at 27μm (S=27μm). All simulations have been carried out at 20 GHz with a commercial electromagnetic (EM) simulator (Ansoft HFSS). The simulation results are shown in Fig. 3-4 and Fig. 3-5. From Fig. 3-4, as CPW and 3-D ECPW consume the same surface area, 3-D ECPW can reach lower characteristic impedance. In case of the CPW lines, it is practically impossible to achieve the values of characteristic impedance lower than 30 Ω. Due to the limit of photolithography, the minimum spacing between the signal and ground lines is about 2 μm. On the contrary, a

wide impedance range down to 20 Ω can easily be obtained by controlling the overlap (D) in the 3-D embedded CPW.

The loss of 3-D embedded CPW lines with a trench width 20μm is maintained to less than 2 dB over a wide impedance range from 20 to 70 Ω, while that of the CPW line increases rapidly as the impedance decreases below 30–40 Ω.

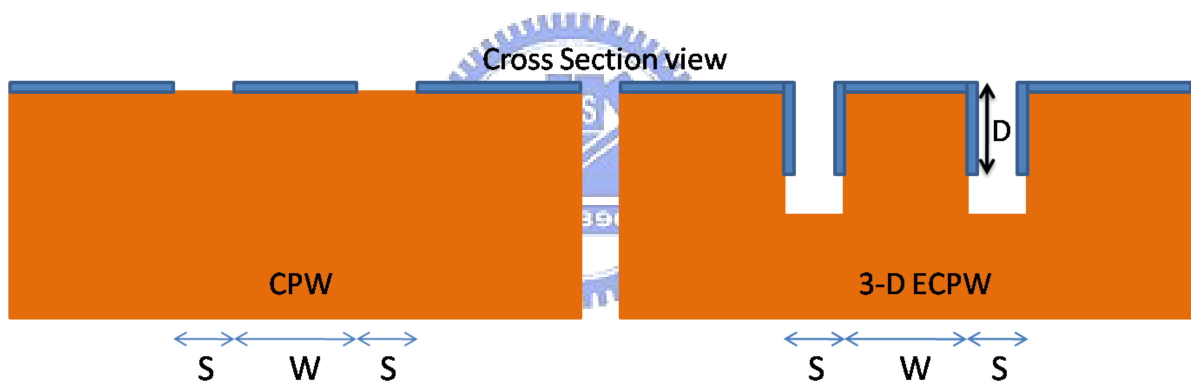


Fig. 3-3 cross section view of CPW and 3-D ECPW

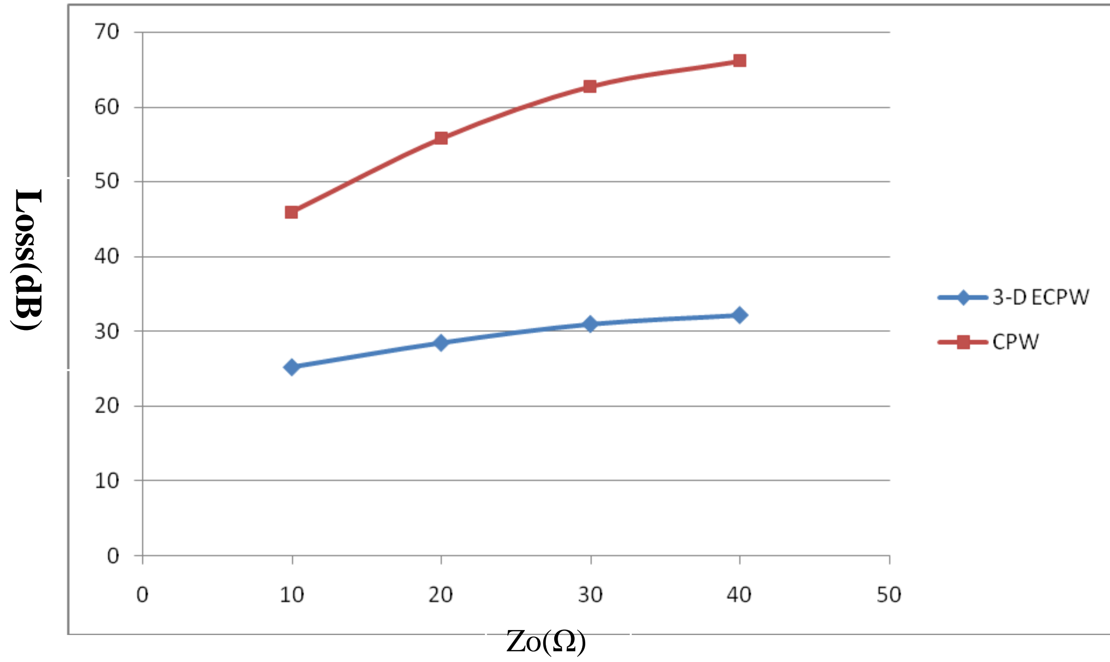


Fig. 3-4 Comparison of characteristic impedance for 3-D embedded CPW and CPW with the same surface area

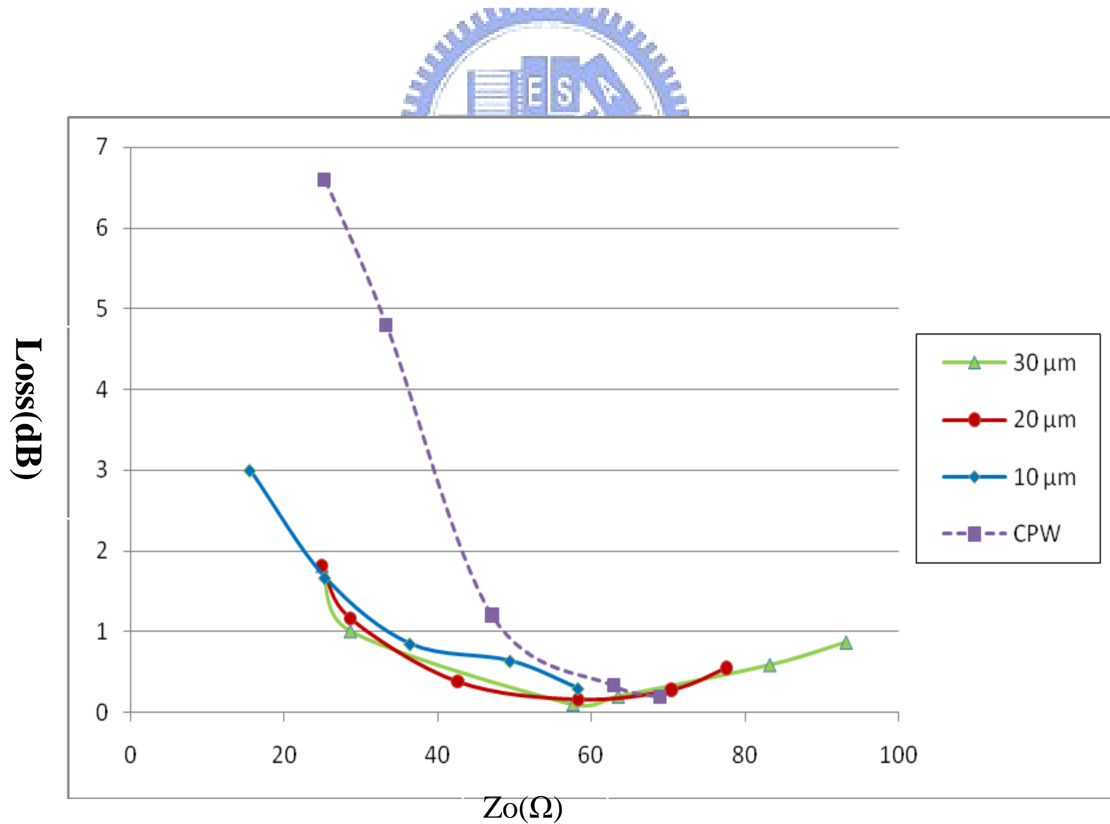


Fig. 3-5 Comparison of calculated loss for 3-D embedded CPW and CPW

3.4.2 Fabrication Process

The 3-D embedded CPW lines in this thesis are fabricated on both the silicon substrates and the high resistivity silicon substrates. The fabrication steps are identical on two different substrates. The steps of fabrication process are shown in Fig. 3-6. First of all, a 5000 Å silicon dioxide is grown on the silicon substrate surface for better isolation and it can slightly reduce the conduction loss and substrate loss. In the first step, the desired trench position and size are defined by standard photolithography process. In the next step, trenches are fabricated by deep etching technology with Inductively Coupled Plasma (ICP) system. The ICP etching system has widely been used in silicon-based IC process for deep trench formation. In the forth step, the dry film photoresist is used in the photolithography process to define the desired position and area for the metallization step as followed. It is worthy to note that dry film photoresist used here is necessary for preventing the photoresist flowing into the trench. Then the metal sputtering process is used for the deposition of copper (Cu) film. Note that the thickness of the Cu is about 1 μm and a titanium (Ti) with 100 nm thick is used as the adhesion layer. The reasons for the use of sputtering process are mentioned in the section 2.2.3. In the last step, we want to get rid of the metal in the unwanted place. The "lift-off" technology is utilized to remove the photoresist together with the metal above it. Finally, the 3-D structure is completed, as shown in Fig. 3-6.

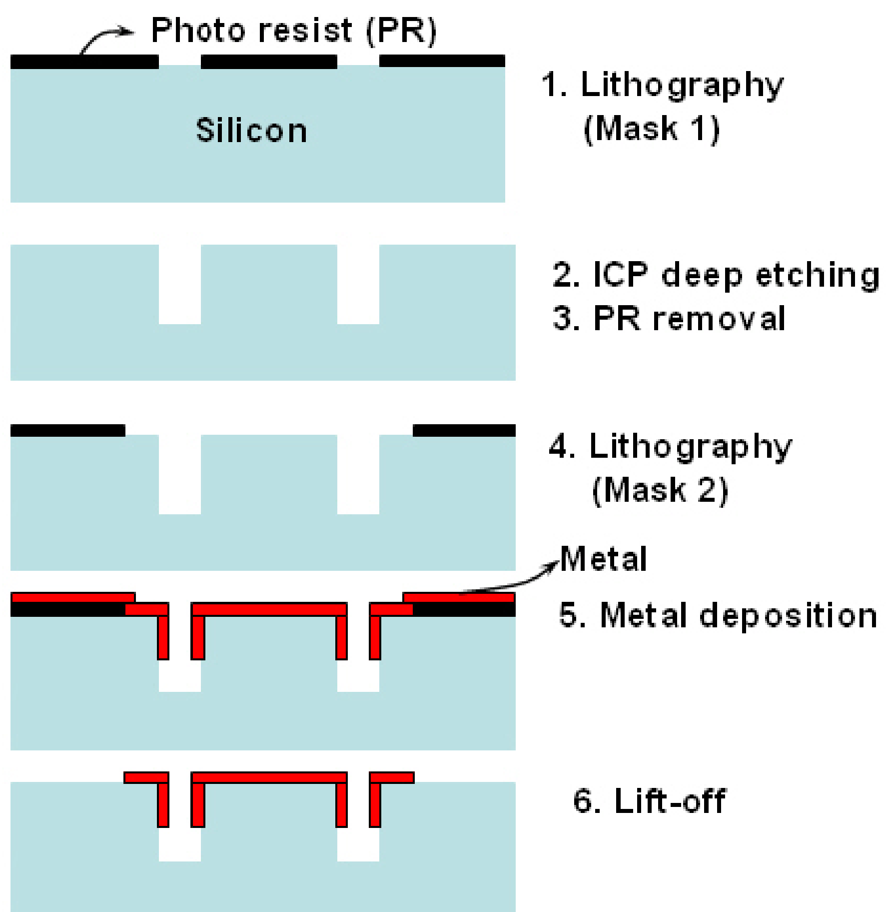


Fig. 3-6 Process flow the 3-D embedded CPW

3.4.3 Measurement

3.4.3-1 Characteristic Impedance Measurement

It's the important issue to determine the characteristic impedance of transmission lines on the lossy substrates such as silicon. This issue has been studied by several researchers. In this thesis, we adopt the method that was published in Dylan F. Williams' paper [29].

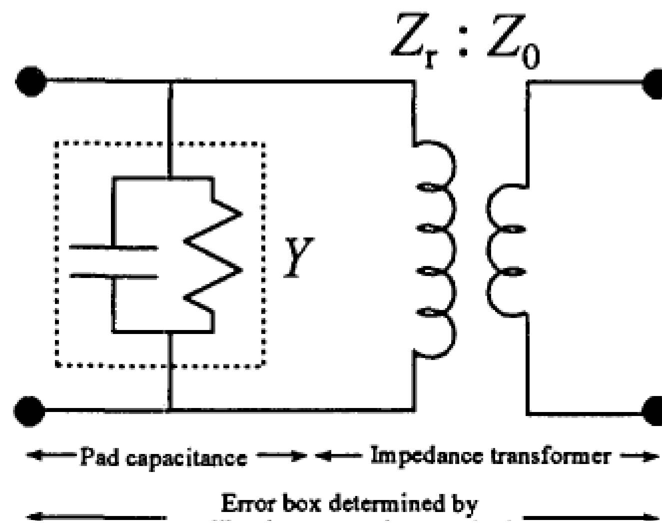


Fig. 3-7 The equivalent circuit model for the contact pads and impedance transformer

Fig. 3-7 shows a simple model for a transition between a probe tip and a transmission-line. The model consists of a lossy shunt contact-pad with admittance *Y* followed by an impedance transformer mapping the reference impedance Zr, of the probe-tip calibration into the reference impedance Zo of the second-tier TRL calibration. The transmission matrix *X* of the circuit in Fig. 3-7 is

$$X = \frac{1}{\sqrt{1-\Gamma^2}}\begin{bmatrix} 1 & \Gamma \\ \Gamma & 1 \end{bmatrix} + \frac{YZ_r}{2}\begin{bmatrix} -1 & -1 \\ 1 & 1 \end{bmatrix} \qquad (1)$$

Where

$$\Gamma \equiv \frac{Z_0 - Z_r}{Z_0 + Z_r}. \qquad (2)$$

When transition parasitics are dominated by contact pad capacitance and conductance, the error box *X'* measured by the calibration comparison method will be approximately equal to *X.*

From reference [30] estimates Γ **as:**

$$\Gamma_0 \equiv \sqrt{\frac{X_{12}'X_{21}'}{1 + X_{12}'X_{21}'}} \qquad (3)$$

It shows that Γo is insensitive to arbitrarily large reference plane transformations of the probe-tip calibration. However, while Γo, may not be sensitive to these reference plane transformations, **(1)** shows that it will be sensitive to *Y.*

On the other hand, the term **YZr/2** in (1) adds to X_{21} but subtracts from X_{12}, so its effect cancels completely from the mean $\frac{1}{2}(X_{12} + X_{21})$**.** Thus, even for very large **Y,**.

$\Gamma / \sqrt{1 - \Gamma^2} \approx \frac{1}{2}(X_{12}' + X_{21}')$. In the new method we propose here, we will use **(2)** and the estimate

$$\Gamma_1 \equiv \sqrt{\frac{\frac{1}{2}(X_{12}' + X_{21}')}{1 + \frac{1}{2}(X_{12}' + X_{21}')}}, \qquad (4)$$

which is insensitive to contact-pad capacitance and conductance ***Y,*** to determine ***Zo.***

3.4.3-2 Measurement Results

The S-parameters of the lines were measured by HP 8510C network

analyzer, and the method for characteristic impedance calculation is as described in section 3.4.3-1. The 3-D embedded CPW structure of trench width=10 um. The conventional CPW of W= 20μm and 30μm are also measured. The measurement result comparing to the simulation result shows in Fig. 3-8. In the figure, we can find that the measurement results are quiet reasonable comparing to the simulation data.

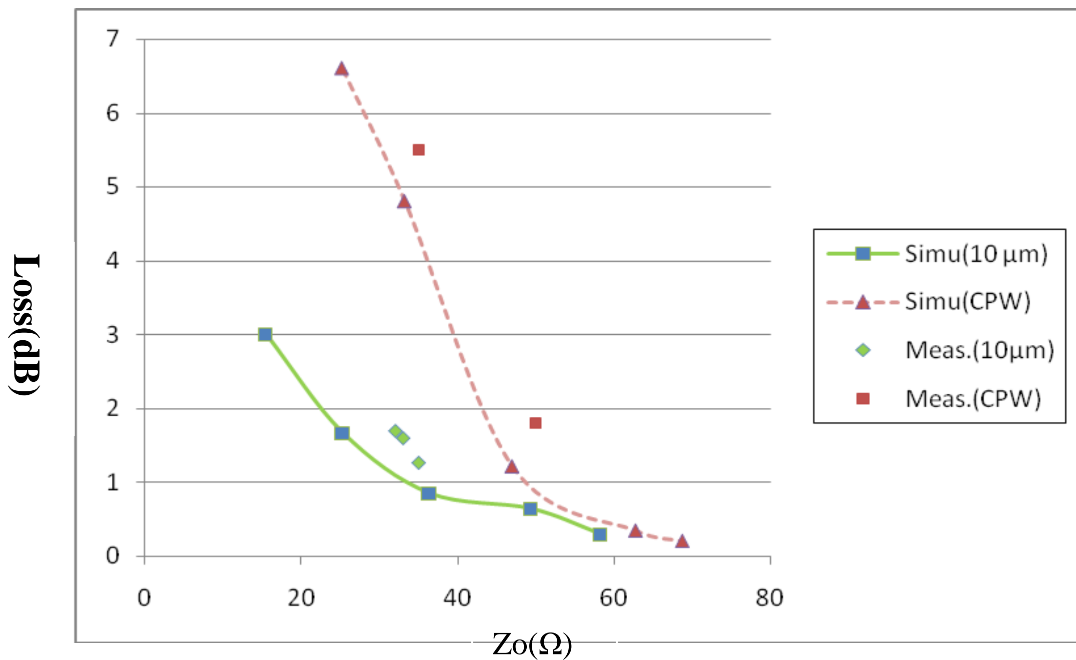
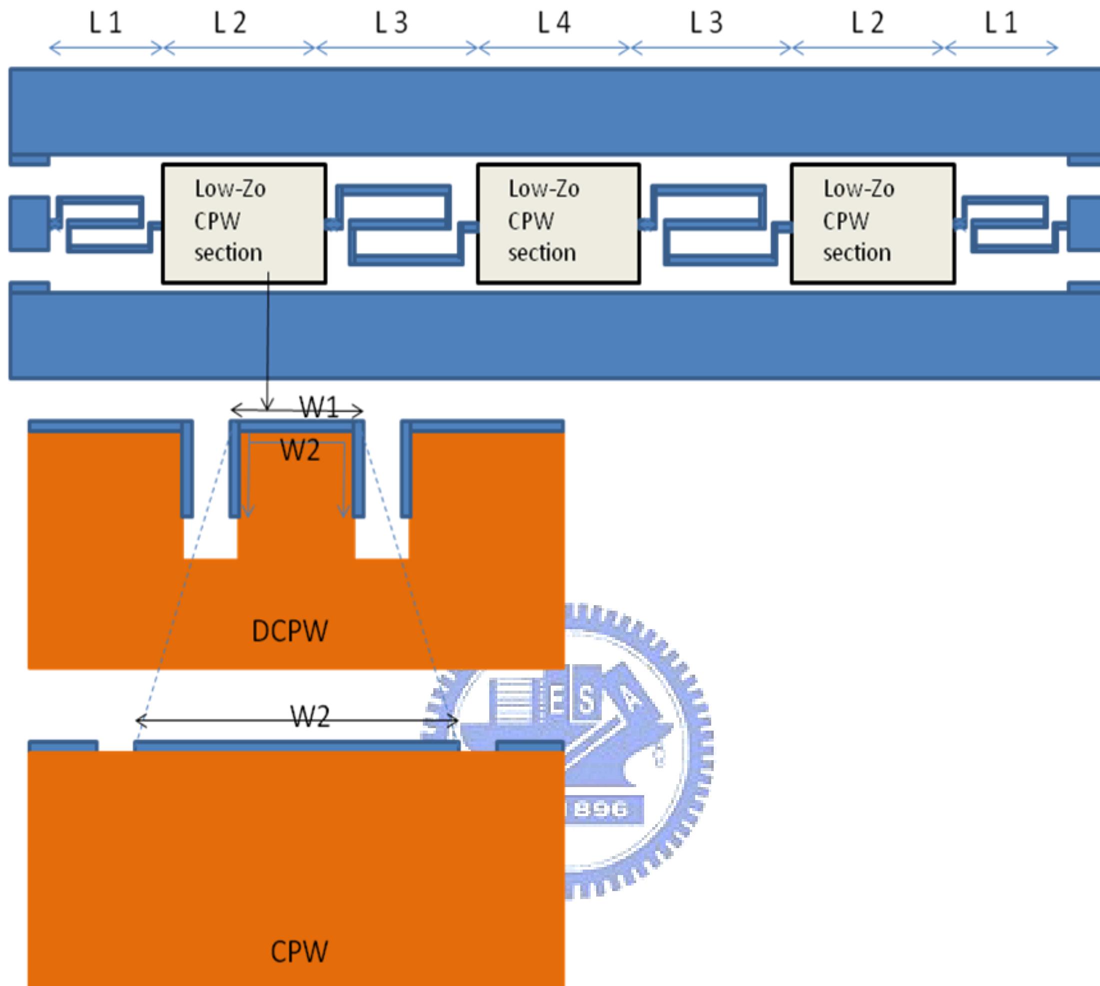


Fig. 3-8 The comparison of the simulation and measurement result.

3.5 Low-pass Filter Application

In this thesis, we have employed low-Zo 3-D embedded CPW lines as capacitive elements in the stepped-impedance LPF. Thus, this LPF is expected to benefit from the low-loss and low-Zo capabilities of 3-D embedded CPW structures. For experimental verification, X-band Chebyshev seven-section stepped-impedance LPFs have been implemented using both CPW and 3-D embedded CPW lines on 525- μm-thick silicon substrate. The element values of the filters were calculated using a standard design procedure [11]. The simulation is carried out by Ansoft HFSS. Based on these informations, the lengths of each section were determined so that they might meet the element values of the filters. In the actual layout, the inductive sections were realized using meandered high-Zo CPW lines for size reduction and were common to both filters. The capacitive sections were implemented with low-Zo 3-D embedded CPW lines for the 3-D embedded CPW filter, while low-Zo CPW lines were employed for the conventional CPW filter. The detailed dimensions and the schematics are shown in Fig. 3-9 and Fig. 3-10 shows the mask layout of the filters. The length of the center conductor of low-Zo lines was fixed at 97 μm for both filter cases. Due to the enhanced capacitance, the 3-D embedded CPW line showed lower characteristic impedance and smaller effective dielectric than the CPW line. Therefore, the length of low-Zo lines of the 3-D embedded CPW filter was effectively reduced. In this way, the capacitive sections using the low- 3-D embedded CPW line show the properties more similar to the lumped elements. The comparison between the simulated performance of both filters is shown in Fig. 3-11. Besides the benefit of size reduction as I stated earlier, the 3-D embedded CPW filter offers additional advantages of low insertion loss, and

sharp skirt characteristic.



(low Zo line)	W1 (um)	W2 (um)	L1 (um)	L2 (um)	L3 (um)	L4 (um)
CPW	27	97	720	2180	890	2183
3-D E-CPW	27	97	720	1628	890	1682

Fig. 3-9 The layouts and detailed dimensions of CPW and OCPW X-band LPFs.

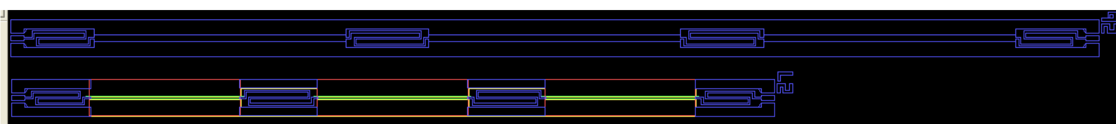
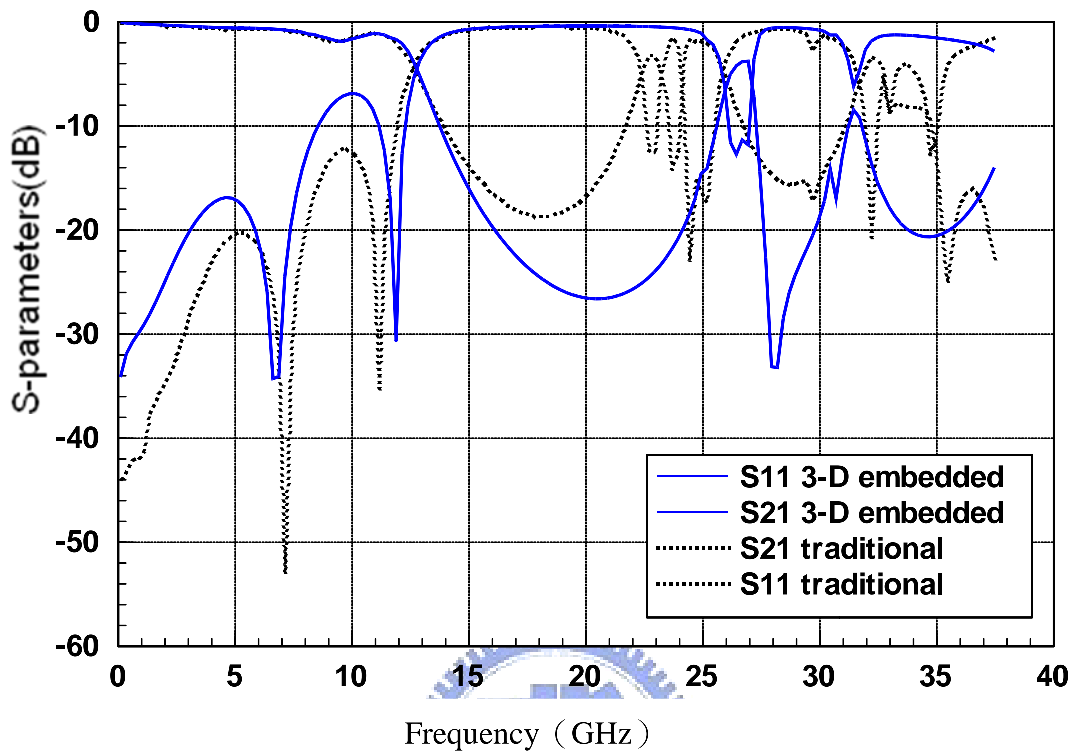


Fig. 3-10 Mask layouts of CPW and 3-D embedded CPW.



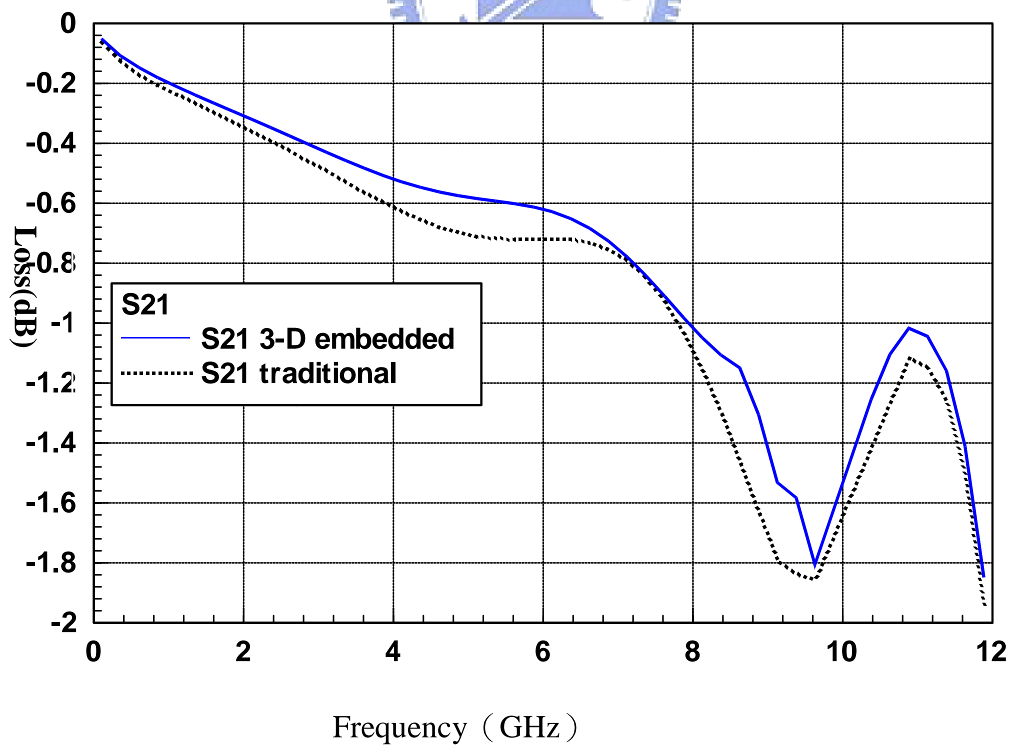


Fig. 3-11 Simulation results of both CPW and 3-D embedded CPW filters.

3.6 Conclusions

In this section, a 3-D embedded CPW structure was developed to solve the loss problems of the low-impedance CPW lines and to extend the usable impedance ranges. Micromachined technology was employed to bended both the center conductor and ground plane partially overlap with each other. A systematic and comparative study has been performed to characterize the 3-D embedded CPW lines. Compared with the conventional CPW, the fabricated 3-D embedded CPW lines with 20- μm trench width showed lower losses (less than 3 dB on silicon substrate at 20 GHz) over a wider range (20–90Ω). To demonstrate practical usefulness of the 3-D embedded CPW lines, an X-band stepped-impedance LPF was fabricated using 3-D embedded CPW lines. The 3-D embedded CPW LPF showed distinct advantages over the conventional CPW filter such as lower loss and reduced size, together with improved spurious responses, including sharp skirt and wide stop-band characteristics. Thanks to their wide impedance and low-loss characteristics, the proposed 3-D embedded CPW is expected to be very useful for integration with various uniplanar microwave/millimeter-wave integrated circuits.

Chapter 4 Applications in Monopole Antenna

4.1 Introduction

Nowadays, wireless communication systems are becoming increasingly popular. However, the technologies for wireless communication still need to be improved further to satisfy the higher resolution and data rate requirements. That is why ultra wideband (UWB) communication systems covering from 3.1 GHz to 10.6 GHz released by the FCC in 2002 [31] are currently under development. Various antennas for wideband operation have been studied for communications and radar systems for many years [32], [33]. The design of wideband antenna is a very difficult task especially for hand-held terminal since the compromise between size, cost, and simplicity needs to be achieved. In UWB communication systems, one of key issues is the design of a compact antenna while providing wideband characteristic over the whole operating band. Due to their appealing features of wide bandwidth, simple structure, omidirectional radiation pattern, and ease of construction several wideband monopole configurations, such as circular, square, elliptical, pentagonal, and hexagonal have been proposed for UWB applications [34]–[36].

In this thesis, a new microstrip-fed patch antenna with a tuning 3-D trench is presented. In order to improve the impedance bandwidth, a 3-D trench on the patch and stepped ground are used in the design of the antenna.

4.2 Antenna Design

Fig. 4-1 (a) shows the evolution of the proposed antenna fabricated on the quartz substrate, which consists of a rectangular patch with two notches at the two lower corners of the rectangular patch and a truncated ground plane with the notch structure. These notches alter the electromagnetic coupling between the rectangular patch and the ground plane. Matching improvement can also be obtained by inserting a slot in the truncated ground plane. It is found that much enhanced impedance bandwidth can be achieved for the proposed antenna. Moreover, the 3-D embedded technology mentioned in chapter 2 will be applied to this monopole antenna in order to improve the band-width and matching. The proposed antenna has compact dimension of 36 mm X 16 mm with thickness of 0.52 mm and relative dielectric constant of 3.7. From the simulation, the optimized dimensions are: W=8.4 mm, L=10.6 mm, Wg=16mm, Lg=23.5 mm, Ws=6 mm, Ls= 1mm, Wn=1.6 mm, Ln=1.4 mm, We=2.4mm, Lf1=1mm, Lf2=23mm and the width of fed-in line is 1mm. The detail trench dimensions is shown in Fig. 4-1(b)

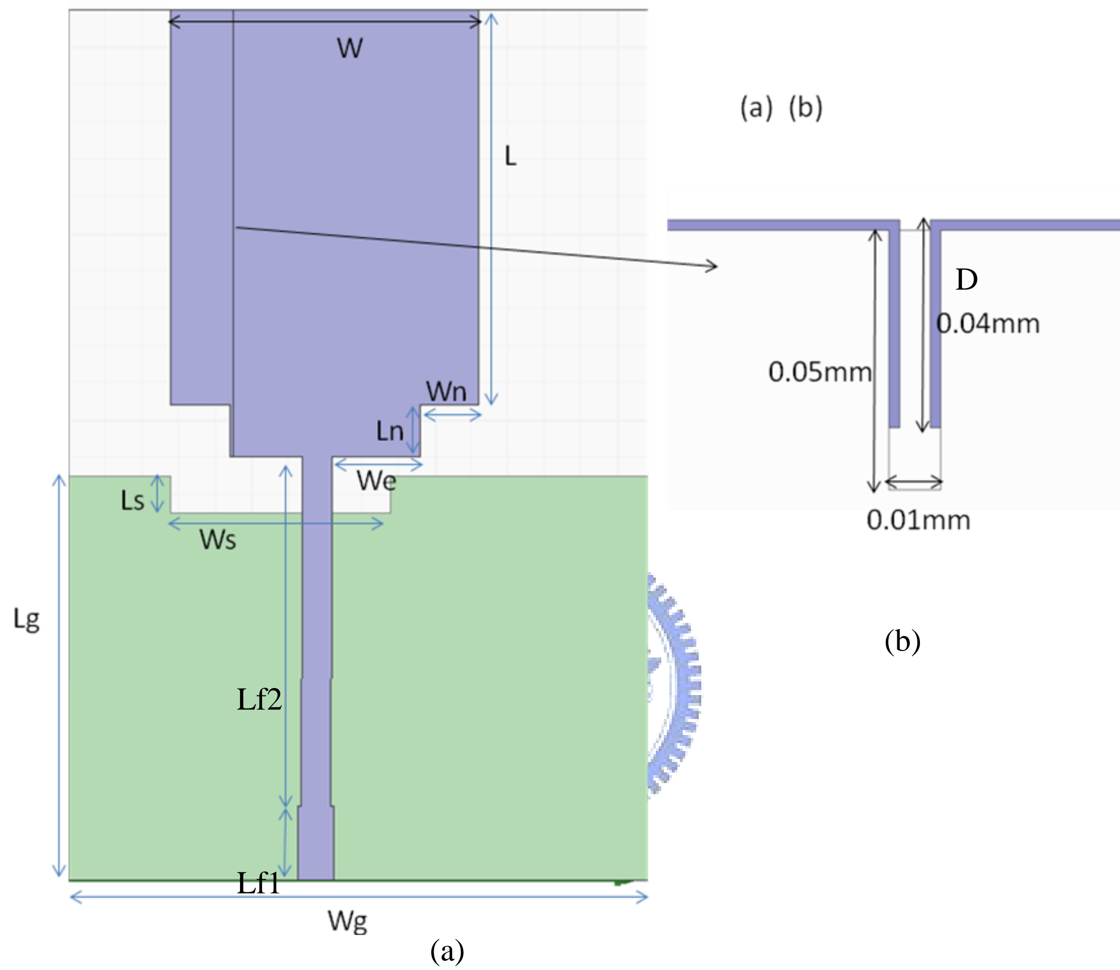
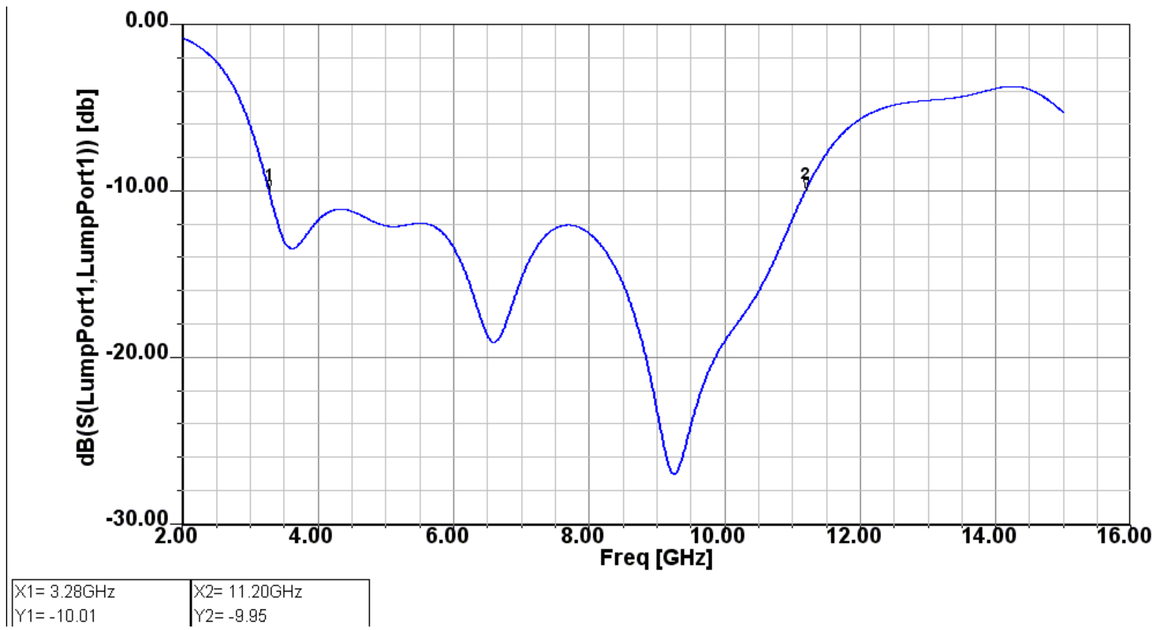


Fig. 4-1: The dimension of the monopole patch antenna
(a)Geometry of the proposed antenna
(b)cross section view of the trench on the patch

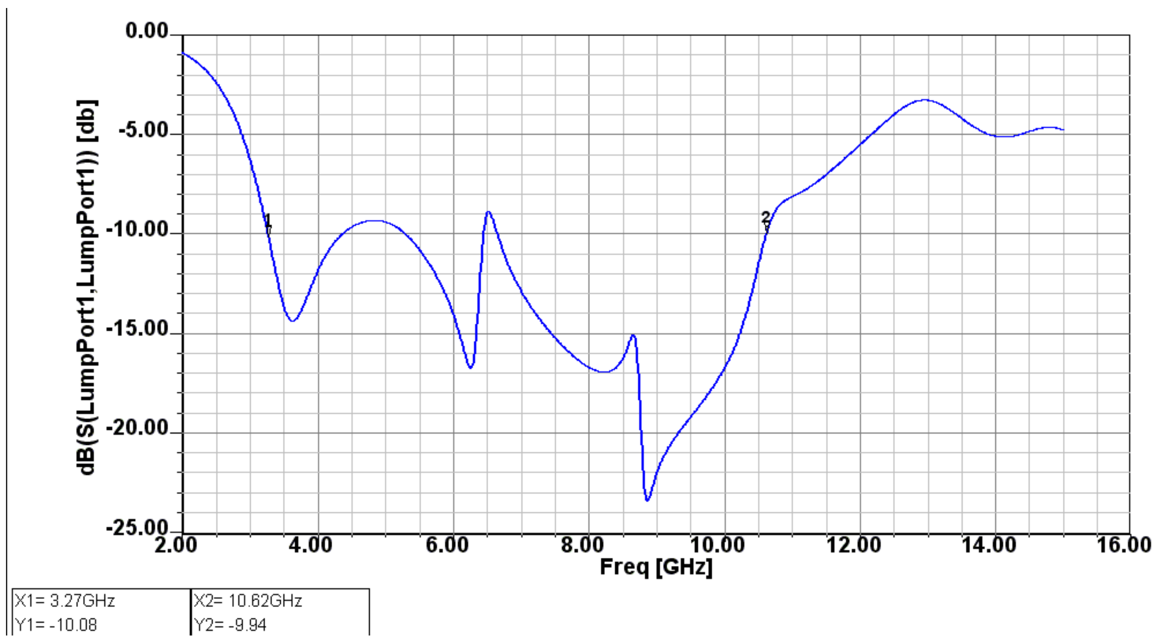
4.3 Simulation Results

Fig. 4-2 (a) and (b) show the comparison of the simulation results of the antennas with and without 3-D embedded structure. The bandwith for -10 dB return loss covers the range of 3.28~11.2 GHz. Comparing with the antenna without 3-D embedded structure, the proposed antenna shows better impedance matching.

The geometrical parameters related to the trench include the dimensions of the trench (0.05mm X 0.01mm) and the metal depth (D). Fig. 4-3 exhibits the effects of varying the parameters on the impedance matching. From Fig. 4-3, we can see that the length of the metal (D) would affect the impedance matching especially at the lower operating frequencies around 5 GHz and increasing the length extend the higher edge frequency of the bandwidth. The depth of the metal (D) and location of the trench slightly affect the higher edge frequency. In general, all the trench-related parameters influence the impedance matching to a certain extent.



(a)



(b)

Fig. 4-2 (a) proposed antenna with 3-D embedded structure;
(b) the antenna without 3-D embedded structure

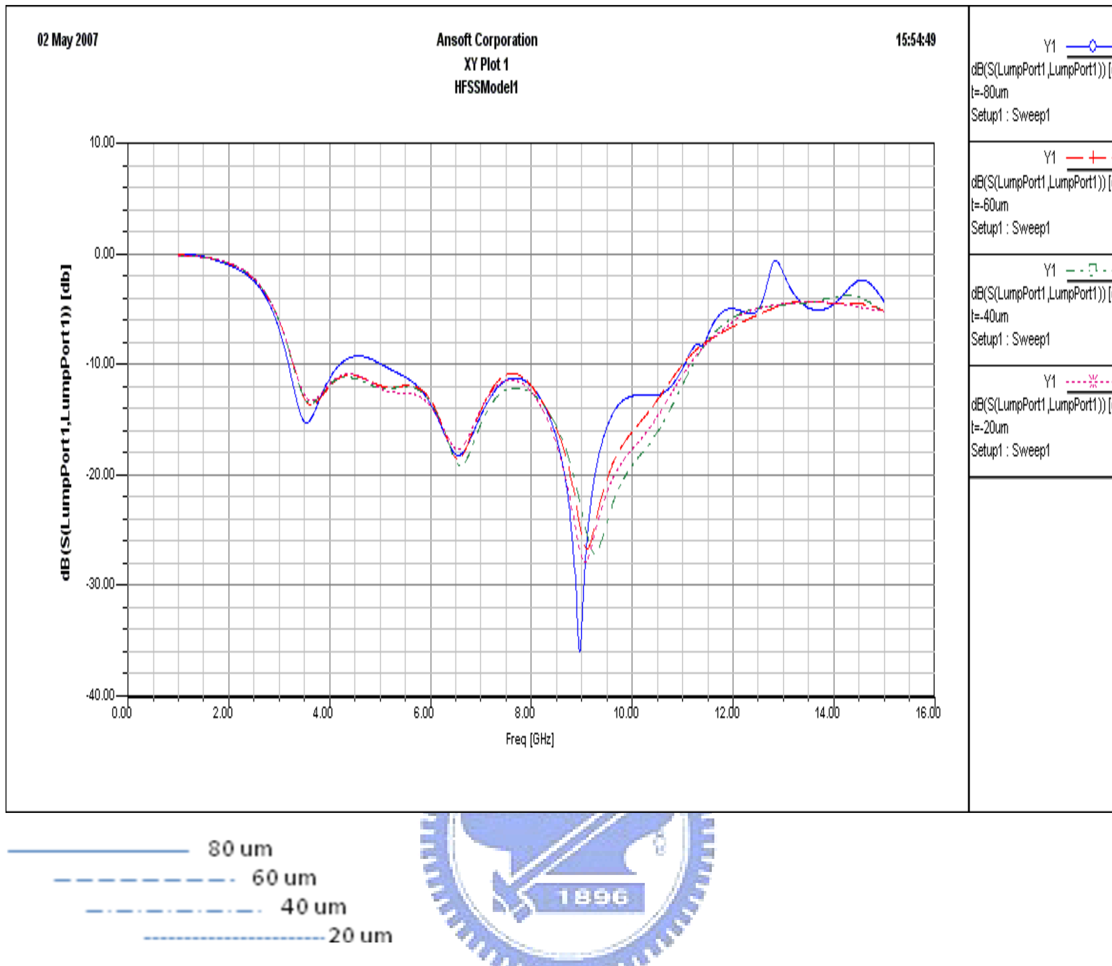


Fig. 4-3 The effect of varying the parameters (D) on the impedance matching.

4.4 Conclusions

In this section, a monopole patch antenna has been proposed for promising ultrawideband applications. The antenna has been designed to supply a new matching structure by placing the trench on the radiator. The study has shown that the trench is able to vary the matching of bandwidth of the antenna and offer a better matching characteristic.

Chapter 5 Conclusions and Future Works

5.1 Conclusions

The 3-D embedded structure mentioned in this thesis shows several advantages as below:

(i) compatibility with MMIC/VLSI circuit layouts and processing,

(ii) ability to realize low characteristic impedances,

(iii) reducing current density near conductor strip edges, thus reducing conductor loss,

(iv) allowing the use of thick substrates during processing, reducing damage during handling and enhancing yield,

(v) eliminating the need for via holes, thus reducing associated parasitics,

(vi) exempting from crosstalk due to presence of ground plane between any adjacent lines.

The 3-D embedded structure is used to design the newly structured CPW and monopole antenna. Compared with the conventional CPW, the fabricated 3-D embedded CPW lines with 20- μm trench width showed lower losses (less than 3 dB on silicon substrate at 20 GHz) over a wider range (20–90Ω). Moreover, the 3-D embedded CPW LPF showed distinct advantages over the conventional CPW filter.

The monopole antenna has been designed to supply a new matching method by etching the trench on the radiator. The designed antenna satisfies the 10 dB return loss requirement from 3.2 to 11 GHz and provides good monopole-like radiation patterns.

5.2 Future Works

The results presented in this thesis represent a work in progress, and hence there are still other efforts can be done. The 3-D embedded CPW mentioned in chapter 3 is considerable to integrate to MMIC/VLSI process. Besides, other applications of 3-D embedded structures are described as follows:

(1) DC Block

DC Block is widely used in microwave circuit in order to isolate the DC voltage level from different blocks. In general, DC block must have very low insertion loss and tolerable to high voltage. In normal high frequency circuit, DC block is composed of electromagnetic coupling structure. Fig. 5-1 and Fig. 5-2 show the layouts of traditional DC blocks.

However the structures in Fig. 5-1 and 5-2 are a 2-D circuit, they consume big area of the substrate to get the desired capacitance value. Moreover, it can only operate in high frequency because the capacitance value is not big enough. By using the 3-D embedded structure, high coupling effect can be achieved due to the increase of the effective capacitance and the area consumption will be less. Both top and cross section view is shown in Fig. 5-3.

(2) Coupler

As mentioned in last paragraph, the 3-D embedded structure can also facilitate to fabricate coupler. The size of the coupler would be reduced due to the high coupling effect in the 3-D embedded structures. Fig. 5-4 shows the construction of the coupler with 3-D embedded structures in it.

Comparing with the traditional planer (vertical type) RF-MEMS device, the 3-D embedded structure shows more advantages. For instance: size

reduction, compatible with CMOS process, low cost, easy to fabricate (1~2 masks can be done) and etc. Besides, with proper design, movable parts would be added in the 3-D embedded structure and thus the ability of tuning could be achieved.

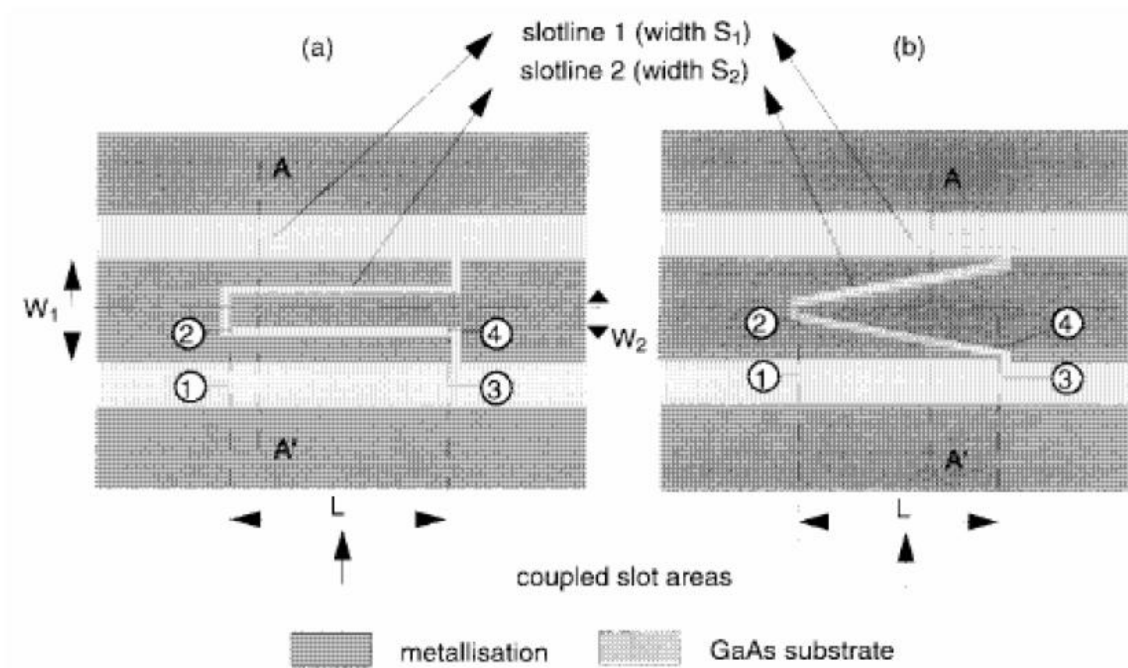


Fig. 5-1 DC block made by series CPW

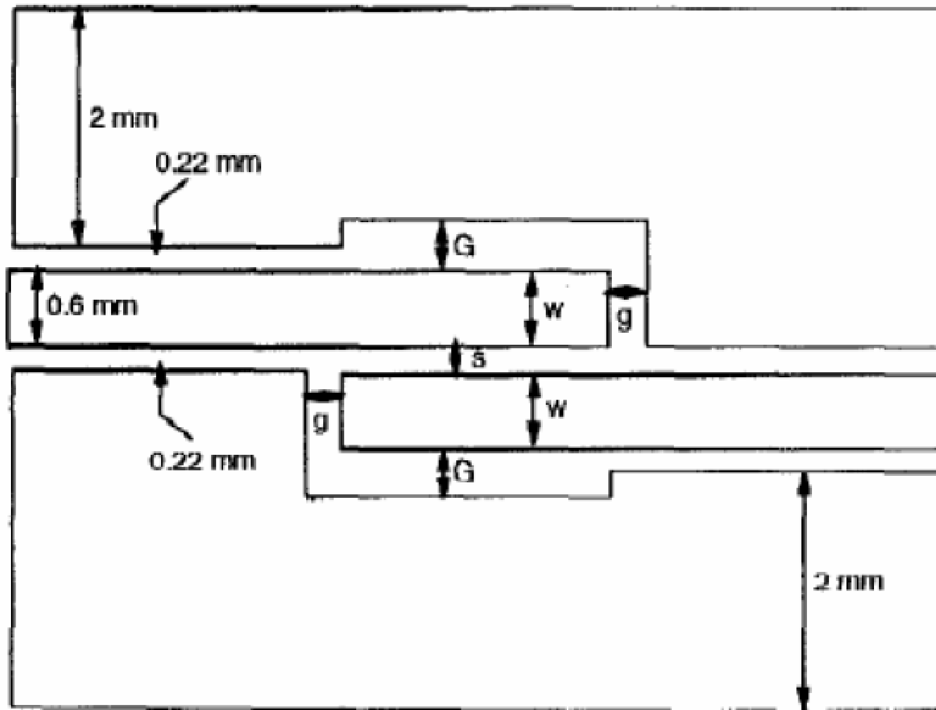


Fig. 5-2 coupling CPW DC block

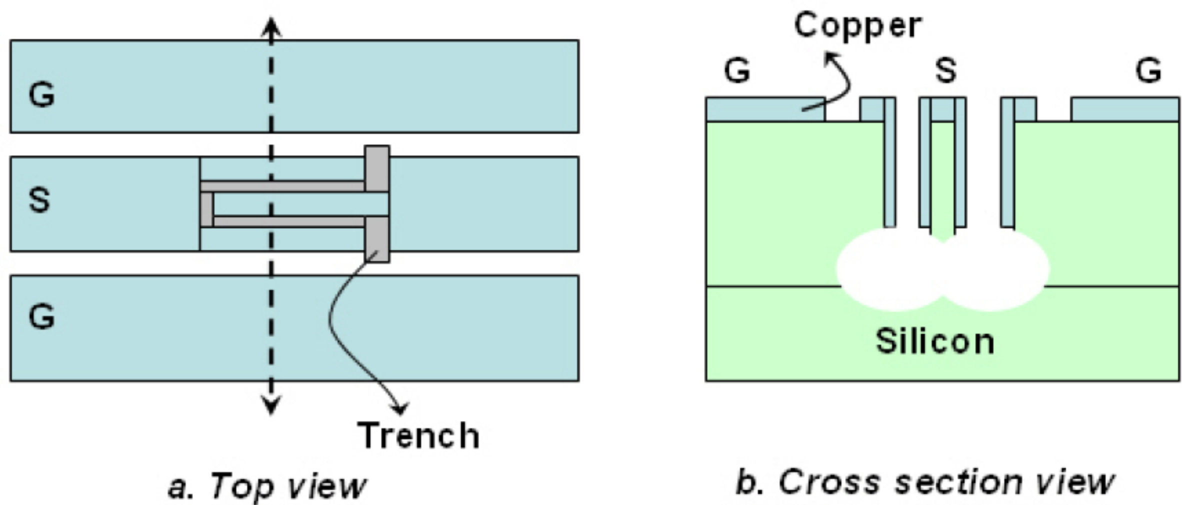


Fig. 5-3 Newly embedded DC block

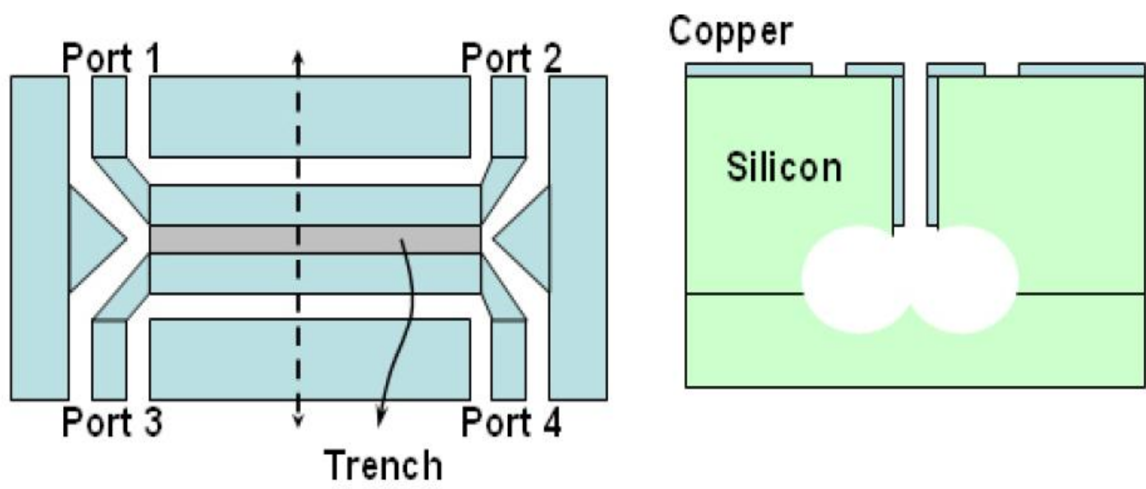


Fig. 5-4 newly embedded coupler

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