國立交通大學

電信工程學系

碩士論文

應用於超寬頻無線射頻接收機之 CMOS 低雜訊放大器與混頻器設計與研究

Design of CMOS Low-noise Amplifier and Mixer for UWB Wireless RF Receiver

研究生：熊子豪

指導教授：周復芳　博士

中 華 民 國 九 十 六 年 六 月

應用於超寬頻無線射頻接收機之 CMOS 低雜訊放大器與混頻器設計與研究

Design of CMOS Low-noise Amplifier and Mixer for UWB Wireless RF Receiver

研究生：熊子豪　　Student: Zi.Hao.Hsiung

指導教授：周復芳　博士　　Advisor: Dr. Christina F. Jou

國 立 交 通 大 學

電 信 工 程 學 系 碩 士 班

碩 士 論 文

A thesis

Submitted to Department of Communication Engineering

College of Electrical and Computer Engineering

National Chiao Tung University

In Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in Communication Engineering

June 2007

Hsinchu, Taiwan, Republic of China

中華民國九十六年六月

應用於超寬頻無線射頻接收機之 CMOS 低雜訊放大器與混頻器設計與研究

研究生：熊子豪　　指導教授：周復芳　博士

國立交通大學電信工程學系碩士班

摘　　要

本論文討論應用於超寬頻射頻接收機的高頻電路設計且主要分為兩個主題探討。其中第一主題是超寬頻低雜訊放大器的分析和設計。第一主題中：探討兩種不同類型的低雜訊放大器：低電壓 (0.75 伏特)、低雜訊放大器和電晶體寄生電容回授式低雜訊放大器。為了達到偏壓於 0.75 伏特，電路主體架構選擇褶疊式疊接組態，量測結果顯示：在供應電壓 0.75 V 功率消耗 11 毫瓦的條件下，頻寬 3.1-7.5 GHz 達到 7.5 dB 增益，雜訊指數為 4.8-7.5dB。電容回授式低雜訊放大器，主要利用低頻的電容回授和高頻的電阻回授形成兩個頻率點匹配，達成超寬頻匹配。量測結果顯示出：頻寬 2.7- 12 GHz，輸入端反射係數皆小於-10dB。3dB 增益頻寬為 1.8-8.3 GHz，功率增益約為 10dB。

第二主題為：摺疊式電流再利用式超寬頻混頻器。此超寬頻混頻器量測結果顯示使用-10dBm 的本地震盪器，頻寬 3.1-8.1 GHz 的範圍內，在中頻 100MHz，可得到 13.5-15.5dB 的降頻轉換功率增益，-11.5dBm 三階諧波交會點，和 11-14.5dB DSB 雜訊指數，主電路功率消耗為 11.3 毫瓦。

最後，一個使用 0.18um CMOS 整合型超寬頻前端電路已被模擬，此超寬頻前端電路也當作此論文的將來專題研究

Design of CMOS Low-noise Amplifier and Mixer for UWB Wireless RF Receiver

Student: Zi.Hao.Hsiung Advisor: Dr. Christina F. Jou

Department of Communication Engineering

National Chiao Tung University

ABSTRACT

This thesis discusses high frequency circuit design for ultra wide-band RF receivers and it mainly includes two parts. One is the analysis and design of ultra wide-band LNA. In part one, we discuss two kinds of UWB LNA：Low voltage (0.75 V), low noise amplifier, and wide-band matched LNA design using transistor's intrinsic gate-drain capacitor. Because the supply voltage is low, we choose folded cascode stage for amplifying stage. The measured results reveal that power gain is 7.5 dB, noise figure is 4.8-7.5 dB and power consumption is 11 mW. The capacitor feedback low noise amplifier makes use of capacitor feedback in low frequency mode and resistor feedback in high frequency mode to achieve two matching mechanism to form wide-band matching. The measured results reveal that the S11 is better than -10 dB from 2.75-12 GHz, S21 is about 10 dB and the 3 dB band-with is 1.9-8.3 GHz.

In part two, we demonstrate a folded, current reused UWB mixer in a standard 0.18um CMOS technology. This UWB mixer achieves measured high conversion power gain of 13.5-15.5 dB at IF=100 MHz with -10 dbm LO power, -11.5 dBm IIP3, and 11-14.5 dB of DSB noise figure. The power consumption of core circuit is 11 mW.

Finally, integrated Ultra wide-band RF front end circuit in 0.18um CMOS has

been simulated. This wide-band RF front end circuit is treated as feature work in our thesis.

致謝

研究所兩年的生活，首先我要感謝我的指導教授周復芳博士，讓我在射頻的領域能有效率的成長，並對於人生的意義有不一樣的見解。同時要感謝口試委員郭建男博士及胡政吉博士的不吝指導，使這篇論文更為完善。此外，要特別感謝國家晶片中心量測課人員在量測上所給予的協助與指導，使我可以精確的量測到晶片的各項參數。

另外要感謝匯儀學長的教導，指引了我研究方向，讓研究更有目標。還有要感謝實驗室的同學瑞嫻、智鵬、宇清和怡星，因為有你們陪伴我的碩士生活，使我在學習成長的路上不曾感到孤單；在此特別感謝智鵬所擁有的個人特色，讓我們實驗室總是在出奇不意的狀況下沉醉在歡樂的氣份中；也很感謝瑞嫻不時的莫名臉紅，常惹得實驗室的成員開懷大笑。另外要感謝已畢業的學長文明、仕豪、博揚、政展、秋榜和宏斌，你們認真的研究態度一直是我的榜樣。也要感謝俊緯學長、昱舜、志豪等學弟，因為有你們的搞笑，讓我度過愉快的碩二。也感謝老劉這兩年的陪伴與支持，讓我更有勇氣完成碩士論文。

最後我要感謝我最愛的父母親和姐姐，在求學的路上給予我最大的支持和包容，讓我能順利地完成碩士學業。在此僅以小小的研究成果貢獻給我家人，並與你們分享我的喜悅。

子豪 於 2007 年 風城 夏

CONTENTS

LIST OF TABLE

LIST OF FIGURE

Chapter 1 Introduction

1.1 Background and motivation

By the rapid development and large demand of wireless communication, fully integrated monolithic radio transceivers are the most significant considerations for communication applications. CMOS technology is attractive due to its advantages of high-level integration, low cost, and enhancing performance by scaling.

IN 2002, the Federal Communications Commission (FCC) has allocated 7500-MHz bandwidth for ultra-wideband (UWB) applications in the 3.1–10.6 GHz frequency range [1]. The related technologies have attracted much attention from both industry and academia. UWB is defined as any signal whose fractional bandwidth is equal to or greater than 20% of the center frequency or that occupies a bandwidth equal to or greater than 500MHz. The large occupied bandwidth (7500MHz) provide high data rates up to several hundred Mbps. Direct sequence code division multiple access (DS-CDMA) and multi-band orthogonal frequency division multiple access (MB-OFDM) are two mainly modulation technologies for UWB communications.

1) Direct-sequence UWB (DS-UWB) proposal [2]:

The DS-UWB supports data communication using both BPSK and 4-BOK. The 4-BOK modulation is optional and BPSK is mandatory. BPSK modulation is low complexity and easy to implement. Every compliant device will be able to both transmit and receive BPSK modulated signals. DS-UWB supports two independent bands of operation. Fig.1.1 shows the reference spectral mask for DS-UWB scheme. The lower band occupies the spectrum from 3.1-4.85GHz and the upper band occupies the spectrum from6.2-9.7GHz. The 5-6GHz band is dedicated to WLAN 802.11a systems.

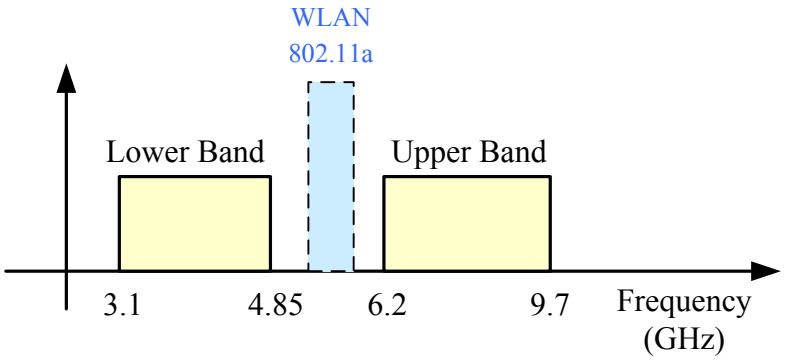


Figure 1.1 DS-UWB spectrum allocation

2) Multi-band orthogonal frequency division multiplexing UWB (MB-OFDM UWB) proposal [3]: In Multi-Band-OFDM (MB-OFDM) UWB, frequency span is grouped into 5 major Band Groups which are in turn sub-divided into 14 bands in total, as shown in Fig. 1.2 Each band is 528MHz bandwidth, and the center frequency of each band is m×264 MHz, where m is from 13 to 39 as shown in Table 1.1. Each band includes 128 sub-channels, sub-channel is 4.125 MHz as shown in Figure 1.3.

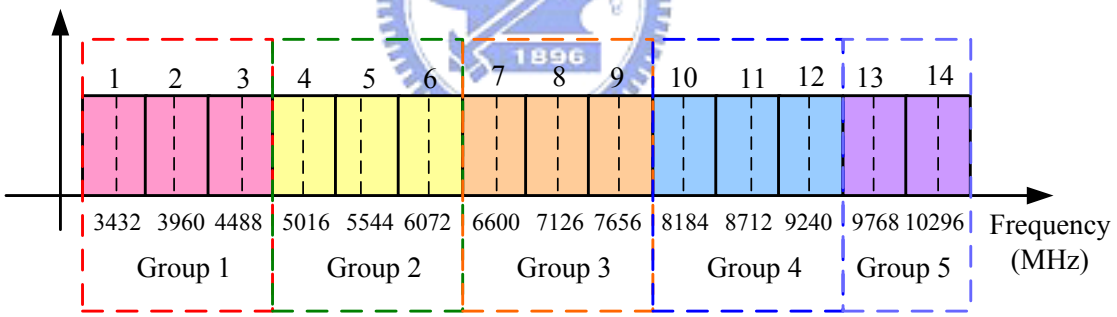


Figure 1.2 Multi-band spectrum allocation

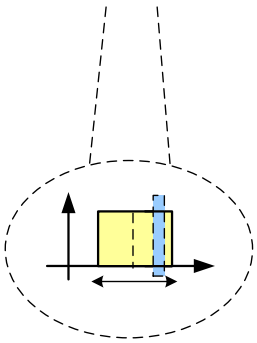


Figure 1.3 MBOA channelization

Band Group	Band ID	Lower frequency	Center frequency	Up frequency
1	1	3168 MHz	3432 MHz	3696 MHz
	2	3696 MHz	3960 MHz	4224 MHz
	3	4224 MHz	4488 MHz	4752 MHz
2	4	4752 MHz	5016 MHz	5280 MHz
	5	5280 MHz	5544 MHz	5808 MHz
	6	5808 MHz	6072 MHz	6336 MHz
3	7	6336 MHz	6600 MHz	6864 MHz
	8	6864 MHz	7128 MHz	7392 MHz
	9	7392 MHz	7656 MHz	7920 MHz
4	10	7920 MHz	8184 MHz	8448 MHz
	11	8448 MHz	8712 MHz	8976 MHz
	12	8976 MHz	9240 MHz	9504 MHz
	13	9504 MHz	9768 MHz	10032 MHz
	14	10032 MHz	10296 MHz	10560 MHz

Table 1.1 MBOA band plan

1.2 Thesis organization

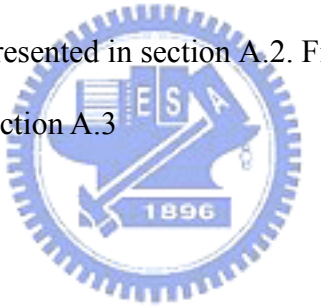
This thesis discusses about the circuit design and implementation of Ultra-wideband Low-Noise amplifier and wide-band mixer, in chapter 2 and 3, respectively. In chapter 4, we will make a conclusion and discuss the future work. We will present the design flow and experimental results in TSMC 0.18-μm CMOS process. Moreover, we will discuss the reasons of differences between simulation and measurement results.

In chapter 2, this chapter includes two circuits. The first section is low-voltage ultra wide-band LNA, The second section is 3–8 GHz wideband LNA using transistor's

intrinsic capacitor feedback. We will discuss these configurations, wideband input/output matching, noise and linearity of LNA. Besides, electromagnetic simulated software Sonnet and Momentum is used to approach simulated results to practical circuited property.

In Chapter 3, we will present the design and implementation of wide-band mixer for UWB applications. Firstly we review the topology and operation theory of basic mixer in section 3.1. The proposed wide-band mixer is presented in section 3.2. Section3.3 discusses layout and measurement consideration of the proposed mixer. Finally, the experiment results and comparison are presented in section 3.4.

Finally, an integrated RF receiver front-end for Ultra-wideband application is proposed in appendix. Firstly we review the architecture of receiver in section A.1. The proposed front-end circuit is presented in section A.2. Finally, the simulation results and comparison are presented in section A.3



Chapter 2

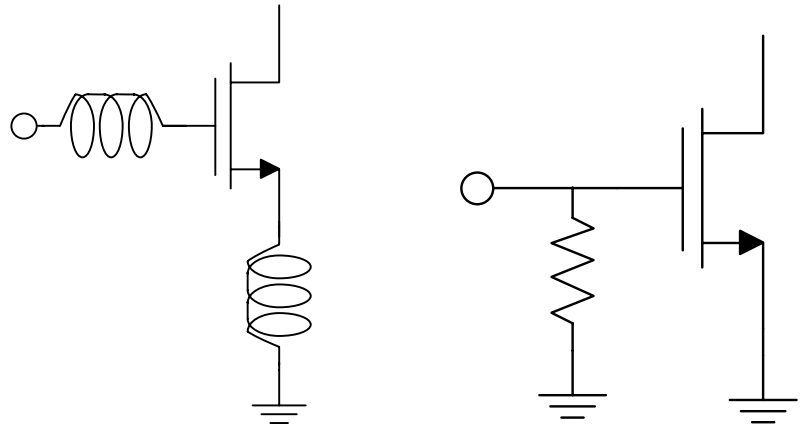
CMOS Low-Noise Amplifier for UWB System

2.1 Introduction

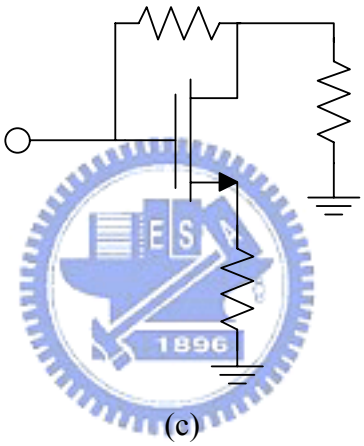
A low-noise amplifier is the first stage, after antenna in the receiver block of a communication system. For UWB applications, the criteria to judge its performances are slightly different from narrow system. Because transmitted power spreads over a wide range and is restricted to be less than -41.3 dBm per MHz, the requirement on linearity in UWB system is not such important as in narrow system. The important requirements for UWB applications are wide-band input impedance matching, low power consumption, low noise performance, and enough gain to suppress noise of the next stages.

In order to connect to an antenna port, the first problem facing is 50 Ohm wide-band input matching. Fig. 2.1.1 shows the four basic 50 Ohm input matching techniques. However, these topologies have some drawbacks. Fig. 2.1.1 (a) is traditional source degeneration topology, because it only resonances at one frequency, it can't achieve wide-band 50 Ohm matching. It realizes only narrow band matching. Fig. 2.1.1 (b) is the resistive termination matching, because of the loading effect, it will loss a lot of voltage if resistive termination matching is used. Fig. 2.1.1 (c) is feedback method. It can achieve wideband input matching. But because of feedback mechanism, it can't achieve high gain to suppress noise of the next stages. Fig. 2.1.1 (d) is LC 3'rd

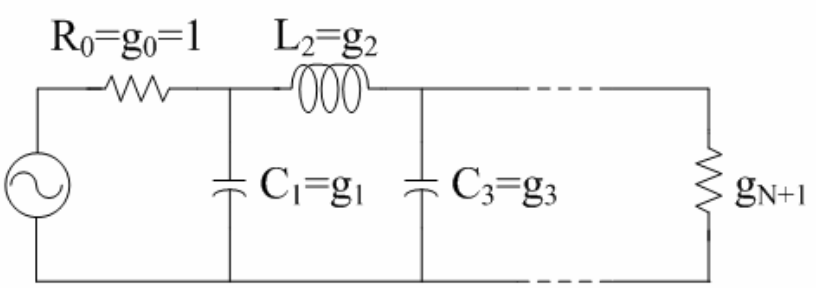
Chebyshev band-pass filter. It can perform good input matching, but it consumes large chip area because of using four inductors for input matching.



(a) (b)



(c)



(d)

Fig. 2.1.1 Conventional input matching technology

Several CMOS LNA design techniques had been reported for broadband communication applications. Recent research shows that relatively flat gain can be achieved over the 3.1- to 10.6-GHz UWB band using CMOS distributed amplifiers. However, due to the additive nature of each transistor's gain, the distributed amplifiers

cannot achieve high gain. The average gain of the reported DAs is around 8 dB, which is insufficient to amplify the received UWB signal. On the other hand, as shown in Fig. 2.1.2, it requires several area consuming inductors to perform signal delay and many stages to provide a given gain that consumes much power [4-5]

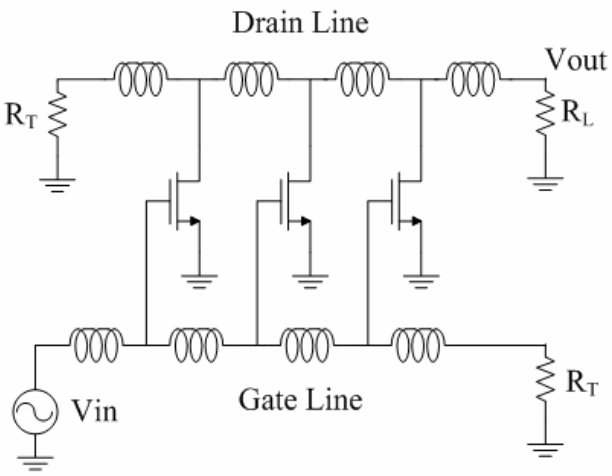


Fig. 2.1.2 Conventional distributed amplifier

2.2 Ultra Wide-band Low-Noise Amplifier

2.2.1 Low-voltage, Low noise Ultra-Wideband Amplifier

2.2.1.1 Architectures

For the UWB technology to be widely employed in the hand-held wireless applications, it cannot be avoided that power consumption is one of the main issues. So we present low-voltage UWB LNA topology.

The fundamental architecture of the low-voltage UWB LNA as shown in Fig. 2.2.1 is composed of cascode configuration and shunt peaking method. The shunt peaking method is used for the requirement of low power consumption and flat gain

performance over wide bandwidth [6]. The cascode structure also has good properties of better reverse isolation, frequency response, lower noise figure and less Miller effect. In order to achieve wideband input matching from 3.1 to 10.6 GHz, the three-section Chebyshev filter is used in the input matching network by combining the gate-drain parasitic capacitance of M1 and the inductance Ls.

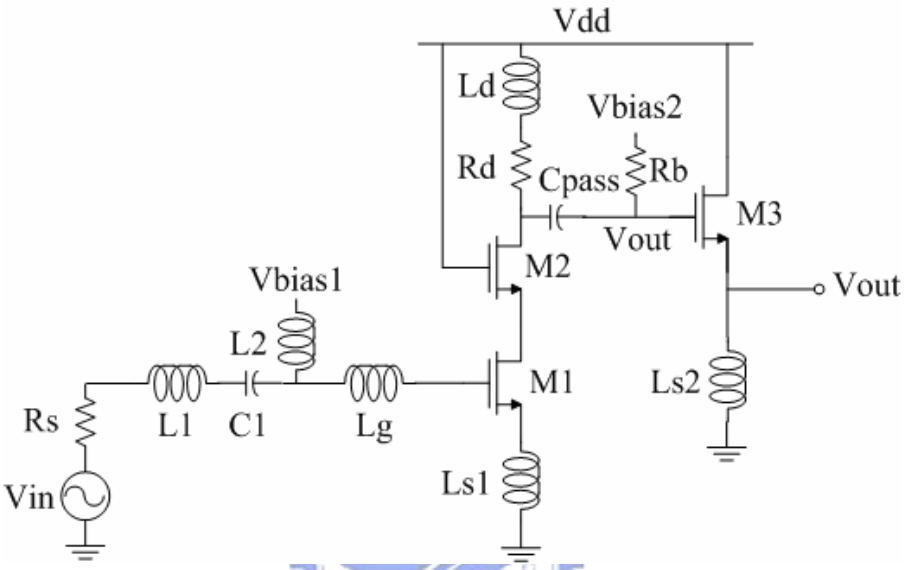


Fig. 2.2.1 Fundamental architecture of the UWB LNA [6]

The proposed low-voltage, low-noise amplifier is shown in Fig. 2.2.2. The LNA circuit can be divided into three blocks –input matching stage, amplifying stage and output buffer stage. Here, we employ a common-gate stage and folded-cascode architecture with shunt peaking method to achieve good performance from 3.1 to 10.6G-Hz with only 0.75V supply.

For input matching stage: common-gate stage (M1) not only is suit for wideband input matching, but also can amplify RF signal. For amplifying stage: L1 is RF chock inductor which is open in small signal mode. The folded-cascode structure has good properties of better reverse isolation, frequency response, less Miller effect and low-voltage operation. Shunt peaking method (Lpd, Rpd) can enhance flat degree of power gain. TL is parasitic inductor of layout path and it can increase stability of the low-noise amplifier. An output buffer composed of common collector amplifier (Mb) is

added for measurement purposes.

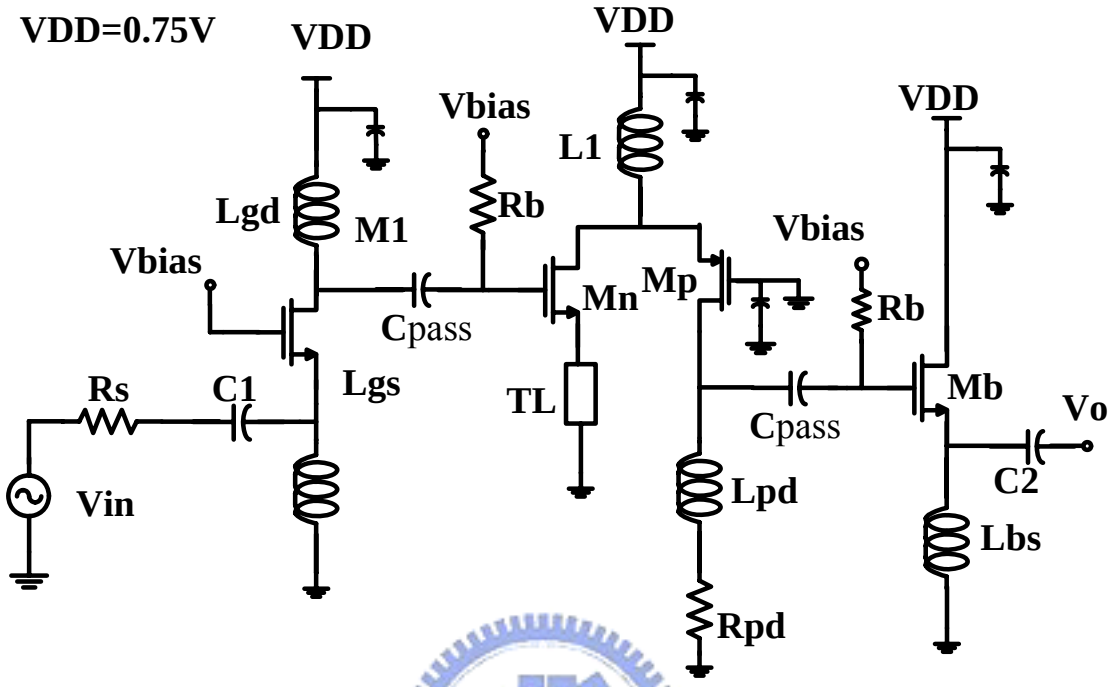


Fig. 2.2.2 Proposed architecture of the low voltage UWB LNA

2.2.1.2 Design considerations

A. Input matching analysis

A common-gate (M1) is used to match to 50Ω, its small signal equivalent circuit is shown in Fig. 2.2.3. Cgs and Cgd respectively are the gate-to-source and the gate-to-drain parasitic capacitance; r_o is the channel length modulation resistor of MOS transistor. The input impedance of the common-gate can be derived as [8]

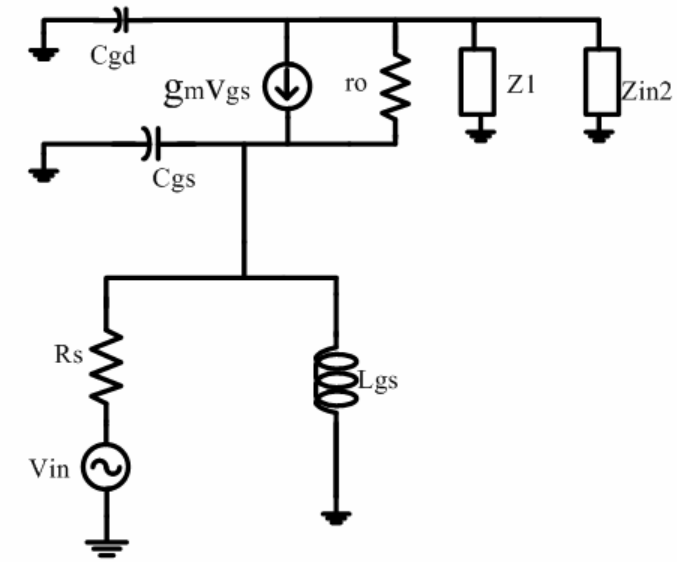


Fig. 2.2.3 Input small signal equivalent circuit

$$Z_{in} = \frac{1}{g_m + \frac{1}{Zs(w)} + \frac{1 - g_{m1} Zo(w)}{r_o + Zo(w)}} \tag{2-1}$$

Where

$$Zs(w) = jwLs // \frac{1}{jwCgs} \tag{2-2}$$

$$Zo(w) = Z_L // \frac{1}{jwCgd} // Z_{in2} \tag{2-3}$$

In equation (2-1), the third term in denominator is induced by finite channel length modulation of a MOS. To obtain more insight on the impact of r_o on the input impedance, we may assume that:

$$Zs(w) = jX_S(w) \tag{2-4}$$

$$Zo(w) = jX_o(w) \tag{2-5}$$

Equation (2-1) can be re-written by substituting (2-4) and (2-5) into (2-1) and we get

$$\begin{aligned} Z_{in} &= \frac{1}{g_m - j\frac{1}{Xs(w)} + \frac{1 - jg_{m1} X_o(w)}{r_o + jX_o(w)}} \\ &= \frac{1}{(g_m - \frac{g_m \cdot X_o^2(w) - r_o}{r_o^2 + X_o^2(w)}) - j(\frac{1}{X_s(w)} + \frac{1 + g_m \cdot r_o}{r_o^2 + X_o^2(w)} \cdot X_o(w))} \end{aligned} \tag{2-6}$$

Because that $r_o^2 + X_o^2(w) >> g_m \cdot r_o \cdot X_o(w)$ throughout the frequency of interest, the term $X_s(w)$ dominates the imaginary part of equation (2-6).

Some observations can be made based on the equation (2-6): One is that the trans-conductance of the MOS transistor in common-gate configuration should be set slightly greater than 20 mS for better matching due to the effect of the MOS transistor's finite output resistance r_o, and at the resonated frequency of Ls and Cgs has the best input reflection coefficient.

B. Noise analysis

a. Noise in MOSFETS

To develop good CMOS RF circuit design skills, a fundamental understanding of noise source in a MOSFET is necessary. In part a. section, we will focus on the inherent noise of a MOSFET, which can be categorized into two parts: drain noise source and gate noise source.

(i) Drain noise source

The dominant noise source in a MOSFET is the channel thermal noise, which basically is a thermal noise originated from the voltage-controlled resistor mechanism of a MOSFET. Detailed theoretically considerations lead to the following expression for the channel noise of a MOSFET, which is modeled as a shunt current noise "$\overline{i_{nd1}^2}$"in the output current of the device, as shown in Fig. 2.2.5. Another source of drain noise is flicker noise. Flicker noise appears as 1/f character and is found in all active devices, as well as in some discrete passive element such as carbon resistors. In diodes, flicker noise is caused by traps associated with contamination and crystal defects in the depletion regions. In MOSFET, charge trapping phenomena are invoked in surface, and his type of noise is much greater than that of the bipolar transistor. The flicker noise in MOSFET can be given by

$$\overline{i_{nd2}^2} = \frac{k}{f}.\frac{g_m^2}{WLC_{ox}2}\ .\Delta f \approx \frac{k}{f}.\omega_T^2.A.\Delta f$$

where K is the process-dependent constant, and A is the area of the gate.

Hence, the total drain noise source is given by

$$\overline{i_{nd}^{\,2}} = \overline{i_{nd1}^{\,2}} + \overline{i_{nd2}^{\,2}} = 4kT\gamma.g_{d0}.\Delta f + \frac{k}{f}\cdot\frac{g_m^{\,2}}{WLC_{ox}^{\,2}}\ .\Delta f$$

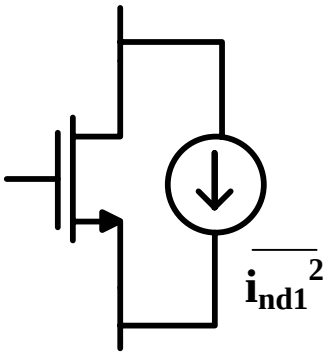


Fig. 2.2.5 channel thermal noise model

(ii) Gate noise

In addition to drain current noise, the thermal agitation of channel charge has another important consequence: gate noise. The fluctuating channel potential couples capacitively into the gate terminal, leading to a noisy gate current. Noisy gate current may also be produced by thermally noisy resistive gate material. Although this noise is negligible at low frequencies, it can dominate at radio frequencies. The gate current noise may be expressed as

$$\overline{i_g^{\,2}} = 4kT\delta.g_g.\Delta f$$

$$\text{Where}\quad g_g = \frac{\omega^2 C_{gs}^{\,2}}{5.g_{d0}}$$

And δ is the coefficient of gate noise, classically equal to 4/3 for long-channel devices. The gate noise is correlated with the drain noise, with a correlation coefficient expressed as

$$C \equiv \frac{\overline{i_g i_{nd1}^{\,*}}}{\sqrt{\overline{i_g^{\,2}}\,\overline{i_{nd1}^{\,2}}}} \approx -0.395\,j$$

The value of -0.395j is exact for long-channel devices. The correlation can be treated by expressing the gate noise as the sum of two components, the first of which is fully correlated with the drain noise, and the second of which is uncorrelated with the drain noise. Hence, the gate noise is re-expressed as

$$\frac{\overline{i_g^{\,2}}}{\Delta f} = 4kT\delta.g_g(1-|c|^2) + 4kT\delta.g_g|c|^2$$

A standard MOSFET noise model can be presented in Fig. 2-2.2.6, where $\overline{i_{nd}^{\,2}}$ is the drain noise source, $\overline{i_g^{\,2}}$ is the gate noise source, and $\overline{v_{rg}^{\,2}}$ is thermal noise source of gate parasitic resistor r_g.

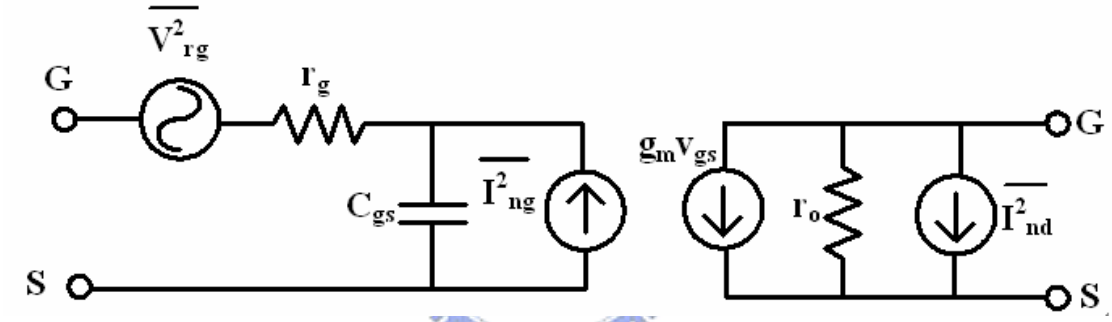
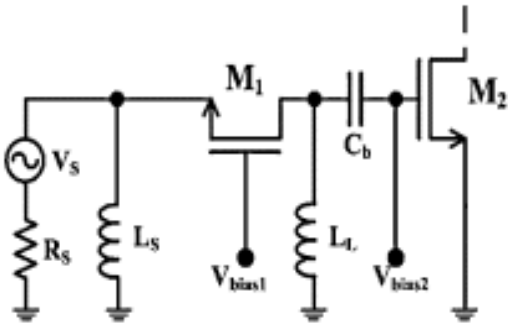


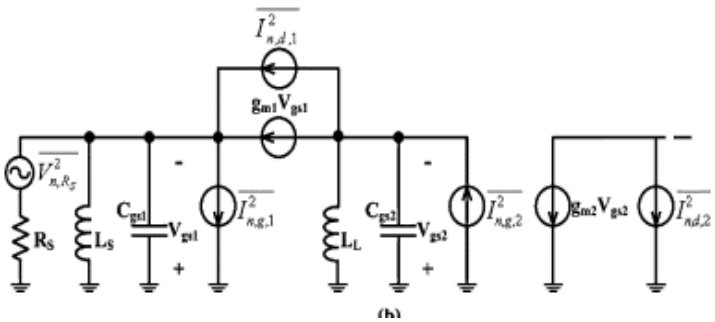
Fig. 2.2.6 MOSFET noise model

b. Common-Gate Stage Noise Analyze

Based on MOSFET noise model, the equivalent noise circuit of the proposed low-noise amplifier is shown in Fig. 2.2.7. TL is omitted because of its value is small.



(a)



(b)

Fig. 2.2.7 Common-gate cascade common-source stage noise circuit

The output noise PSD contributed by the source resistor is given as:

$$S_{n,Rs} = \frac{4kTR_s g_{m1}^{\ 2} g_{m2}^{\ 2} \mid Z_o(w) \mid^2}{(1+g_{m1}R_s)^2 + \dfrac{R_s^{\ 2}}{\mid Z_o(w) \mid^2}}$$

The noise contributed by the part of the induced gate noise in M_1 that is fully uncorrelated with the drain noise is given by:

$$S_{n,g,u,1} = \frac{4kT\alpha\delta \cdot (1-\mid c \mid^2) \cdot w^2 C_{gs1}^{\ 2} R_s^{\ 2} g_{m1} g_{m2}^{\ 2} \mid Z_o(w) \mid^2}{5 \cdot [(1+g_{m1}R_s)^2 + \dfrac{R_s^{\ 2}}{\mid Z_s(w) \mid^2}]}$$

$$= \frac{\alpha\delta \cdot (1-\mid c \mid^2) \cdot w^2 C_{gs1}^{\ 2} R_s}{5 \cdot g_{m1}} S_{n,Rs}$$

The output noise PSD due to the two noise sources in M1 is then given by:

$$S_{n,g,d,c,1} = [\frac{\gamma}{\alpha \cdot g_{m1}R_s}(1 + \frac{R_s^{\ 2}}{\mid Z_s(w) \mid^2}) + \frac{R_s C_{gs1}^{\ 2} w^2 \mid c \mid^2 \alpha\delta}{5g_{m1}} + \frac{2 \mid c \mid^2 \sqrt{\dfrac{\gamma\delta}{5}} wC_{gs1}R_s}{jg_{m1}Z_s(w)}] \cdot S_{n,Rs}$$

Where the first term is contributed by the channel thermal noise of M_1, the second term by the correlated part of the induced gate noise, and the last term arises from the correlation of these two noise sources. The noise contributions by M2 are given by:

$$S_{n,g,u,2} = \{\frac{C_{gs1}^{\ 2} w^2 (1-\mid c \mid^2) \alpha\delta}{5g_{m2} \cdot R_s} \cdot [(\frac{1}{g_{m1}} + R_s)^2 + \frac{R_s^{\ 2}}{g_{m1}^{\ 2} \cdot \mid Z_s(w) \mid^2}]\} \cdot S_{n,Rs}$$

$$S_{n,g,d,c,2} = 4kT\frac{\gamma}{\alpha}g_{m2} + \frac{4}{5}kT\alpha\delta\cdot|c|^2\cdot w^2\cdot {C_{gs2}}^2\cdot|Z_s(w)|^2 - j8kT\cdot g_{m2}\cdot Z_0\cdot|c|\cdot w\cdot C_{gs2}\cdot\sqrt{\frac{\gamma\delta}{5}}$$

$$= \left(\frac{\gamma}{\alpha R_S g_{m2}\cdot|Z_0(w)|^2} + \frac{\alpha\cdot\delta\cdot|c|^2\cdot w^2}{5{R_S}^2{\omega_{T2}}^2} + \frac{2\cdot Z_0\cdot|c|\cdot w\sqrt{\frac{\gamma\delta}{5}}}{jR_S\omega_{T2}\cdot|Z_0(w)|^2}\right)\cdot\left[\left(\frac{1}{g_{m1}}+R_S\right)^2 + \frac{{R_S}^2}{{g^2}_{m1}\cdot|Z_s(w)|^2}\right]\cdot S_{n,Rs}$$

The total noise factor is derived as:

$$F = 1 + \frac{S_{n,g,u,1} + S_{n,g,d,c,1} + S_{n,g,u,2} + S_{n,g,d,c,2}}{S_{n,Rs}} = F_1 + \frac{S_{n,g,u,2}}{S_{n,Rs}} + \frac{S_{n,g,d,c,2}}{S_{n,Rs}}$$

F_1 is the noise factor of the single common-gate stage, excluding the effect of the noise contributed by the common source stage which is given by the later two terms.

Where F_1 is given by:

$$F_1 = 1 + \frac{\alpha\delta(1-|C|^2)w^2 Cgs_1 Rs}{5g_{m1}} + \frac{\gamma}{\alpha R_s g_{m1}}\left(1 + \frac{R_s^2}{|Zs(w)|^2}\right) + \frac{\alpha\delta|c|^2 w^2 {C_{gs1}}^2 R_s}{5g_{m1}} + \frac{2|c|\sqrt{\frac{\delta\gamma}{5}}wC_{gs1}R_s}{jg_{m1}Zs(w)} \quad (2\text{-}7)$$

$$\text{Where} \quad Zs(w) = jwLs // \frac{1}{jwCgs}$$

In equation (2-7), because g_{m1} is in the denominator, the trans-conductance (g_{m1}) of M1 should be increased to decrease noise factor and at the resonated frequency of Ls and Cgs has the minimal noise figure. But the input matching will be worse than -10dB when g_{m1} increases to 35 mS. There is a trade-off between input matching and noise factor for common-gate circuit. For the proposed circuit , g_{m1} is set about 33ms to decrease noise factor, but input return loss still better than -10db.

C. Gain analysis (Shunt peaking method)

Shunt peaking is a bandwidth extension technique in which an inductor connected in series with the load resistor shunts the output capacitor C. A common-source amplifier with shunt peaking is shown in Fig. 2.2.8. For the shunt-peaked network:

$$Z(s) = \frac{R[s(L/R)]+1}{s^2LC + sRC + 1} = \frac{R(\tau s + 1)}{s^2\tau^2 m + s\tau m + 1}$$

The inductor introduces a zero in Z(s) that increases the impedance with frequency, compensates the decreasing impedance of C, and thus extends the -3 dB bandwidth. The magnitude of the impedance, normalized to the DC value as a function of frequency, is then

$$\frac{|Z(j\omega)|}{R} = \sqrt{\frac{(\omega\tau)^2 + 1}{(1-\omega^2\tau^2 m)^2 + (\omega\tau m)^2}}$$

so that

$$\frac{\omega}{\omega_1} = \sqrt{\sqrt{(-\frac{m^2}{2} + m + 1)^2 + m^2} + (-\frac{m^2}{2} + m + 1)}$$

where ω_1 is the uncompensated -3dB frequency. We can choose congruous m to achieve flat wide-band gain.

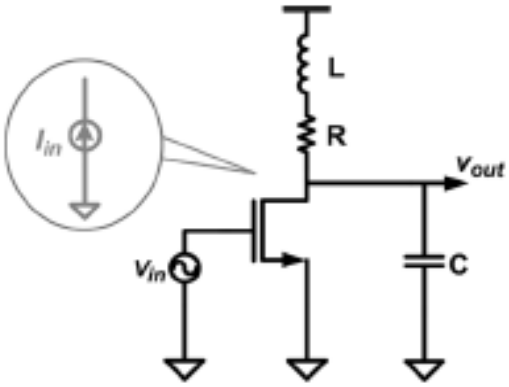


Fig. 2.2.8 A common-source amplifier with bridged-shunt peaking.

2.2.2 3–8 GHz wideband LNA Using Capacitor Feedback

2.2.2.1 Architectures

A simple wide-band input matching network is present in a standard 0.18um CMOS technology in this section. The proposed circuit using transistor's intrinsic capacitor

feedback achieve -10 dB input reflection coefficient from 2.75 GHz to 12 GHz. Compared with traditional matching network of narrow band LNA, such matching mechanism is not an additional inductor, input broadband matching still can be reached. The fabricated wideband LNA achieves average power gain (S21) of about 10 dB from 2.75-GHz to 7.7-GHz .From the bandwidth, the broadband LNA exhibits a noise figure of 3.64–5.5 dB. The DC supply is 1.5 V.

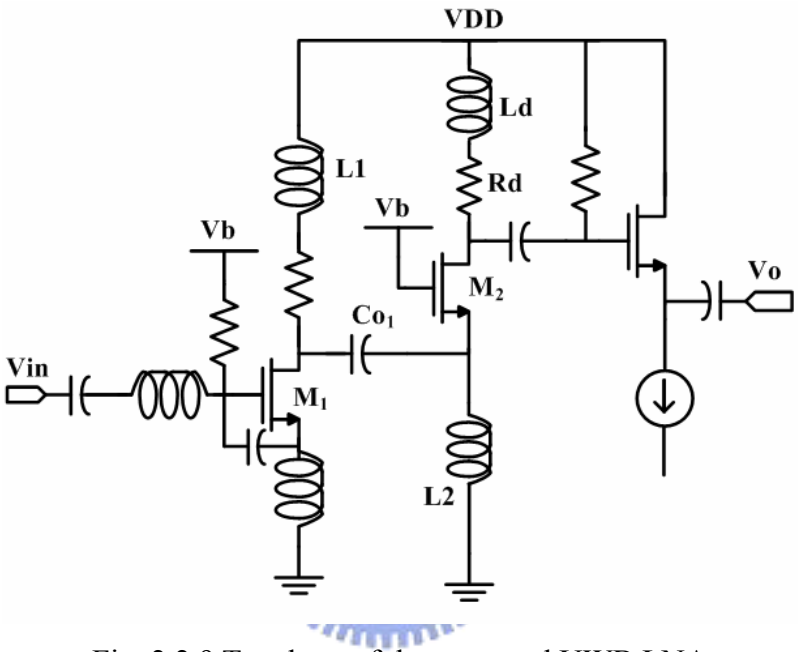


Fig. 2.2.9 Topology of the proposed UWB LNA

Fig. 2.2.9 shows the schematic of the proposed wideband LNA circuit composed of common source stage and common gate stage. L1 and L2 are RF choke inductors which are open in small signal mode. M1、M2、Rd、Ld form cascode amplifier with shunt-peaking load to achieve flat power gain, better reverse isolation, better frequency response, lower noise figure and less Miller effect. An output buffer composed of common collector amplifier is added for measurement purposes.

2.2.2.2 Design considerations

A. Input matching analysis [30]

In this section, we focus on the design of input matching network. Fig. 2.2.10 shows

the small signal circuit of the proposed wide-band LNA. In order to analyze the input-matching network, the small signal circuit of the wideband LNA is decomposed into two parts. One is resistor feedback in high frequency mode, the other one is capacitor feedback in low frequency mode, as shown in Fig. 2.2.11 (a) (b), respectively.

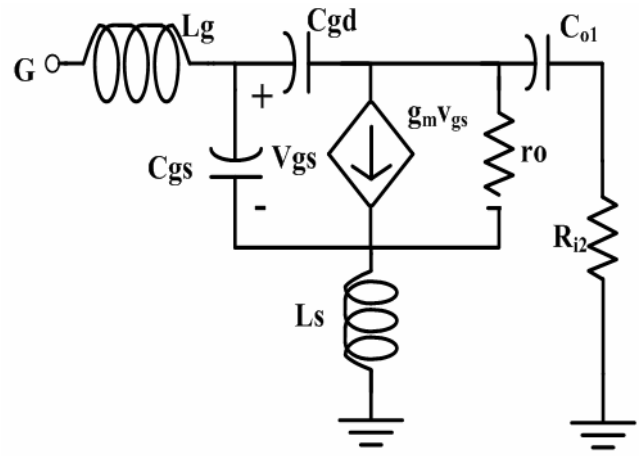


Fig.2.2.10 LNA small signal diagram

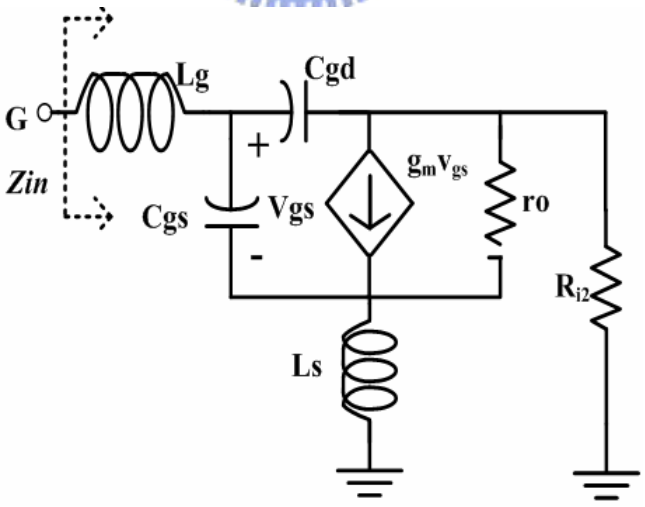


Fig. 2.2.11 (a) LNA small signal diagram at high frequency mode

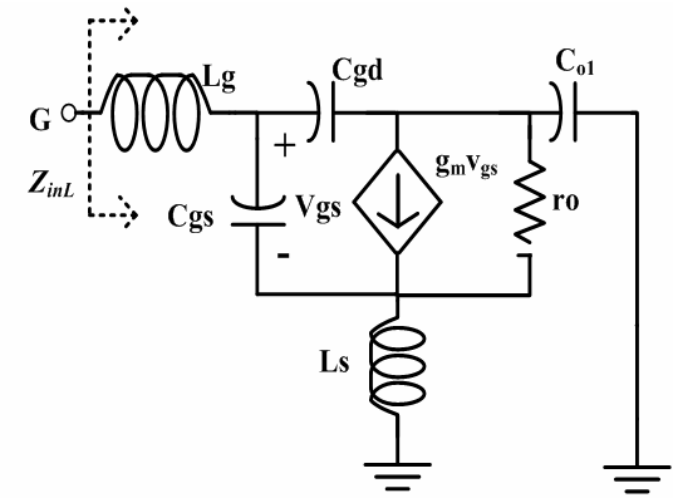


Fig. 2.2.11 (b) LNA small signal diagram in low frequency mode

At high frequency mode small signal circuit as shown in Fig. 2.2.11 (a): Using KCL KVL theory, approximate input impedance can be got that:

$$Z_{inH} = j\omega L_g + \left(\frac{1}{j\omega \cdot C_g} + \frac{L_s \cdot \phi \cdot g_m}{C_g}\right)\left[1 + \frac{C_{gd}}{C_g}(1 + \phi \cdot g_m \cdot R_{i2})\right]^{-1} \quad (1)$$

Where $\phi = \dfrac{r_o}{r_o + R_{i2} + j\omega L_s}$

it is assumed that $j\omega L_S << j\omega C_{gs}$

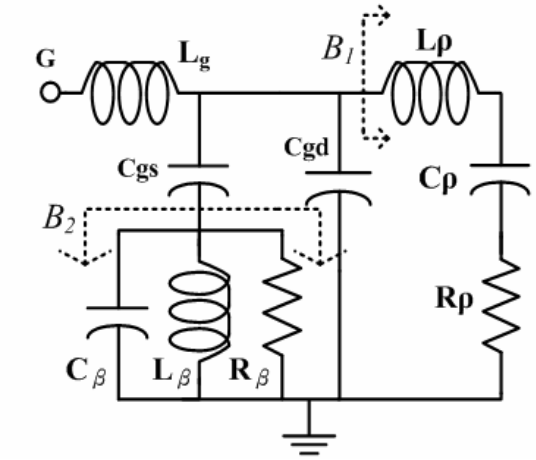


Fig. 2.2.11 (C) Low frequency mode input port equivalent circuit

At low frequency mode as shown in Fig. 2.2.11 (b): Using KCL KVL theory, approximate input impedance equivalent circuit can be shown in Fig. 2.2.11. (c). Because C_β L_β are much small and R_β is much large, B_2 branch is omitted. B_1 branch

dominates the low frequency mode impedance function. Where:

$$R_\rho = \frac{C_{O1}}{g_m C_{gd}},\ C_\rho = g_m r_o C_{gd},\ L_\rho = \frac{L_s C_{o1}}{g_m r_o C_{gd}}(1+g_m r_o)$$

The matching frequency at low frequency mode is that:

$$f_{Low} = \frac{1}{2\pi\sqrt{C_\rho(L_\rho + L_g)}} = \frac{1}{2\pi\sqrt{(g_m r_o C_{gd} L_g) + L_s C_{o1}(1+g_m r_o)}} \quad (2)$$

To make use of equation of (1) and (2), two-frequency matching mechanism is realized and wideband input matching can be achieved.

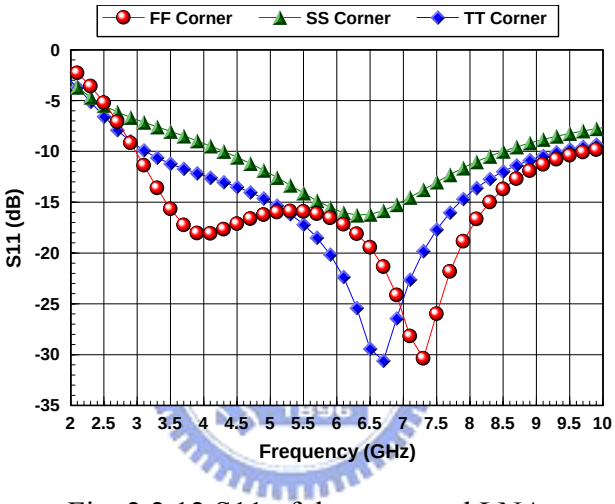


Fig. 2.2.12 S11 of the proposed LNA

2.3 Chip implementation and measured result

A. Measurement consideration

The two UWB Low-Noise amplifiers are designed for on-wafer testing. Therefore the arrangement of each pad must satisfy rules of CIC's (Chip Implementation Center's) probe station testing rules.

For folded LNA: Two six-pin dc probes are required to feed with dc voltages. In addition, two RF probes are also needed for RF signals.

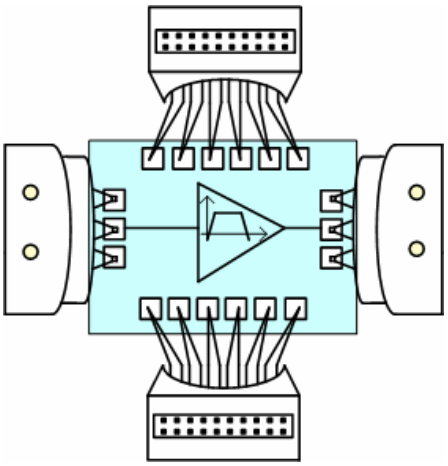


Fig. 2.3.1 (a) On-wafer measurement of low-voltage UWB LNA test diagram

For 3-8 GHz capacitor feedback LNA: One six-pin dc probe, one three-pin dc probe and two RF probes are required. Fig 2.2.13 (a~c) shows the arrangement for dc and RF probes.

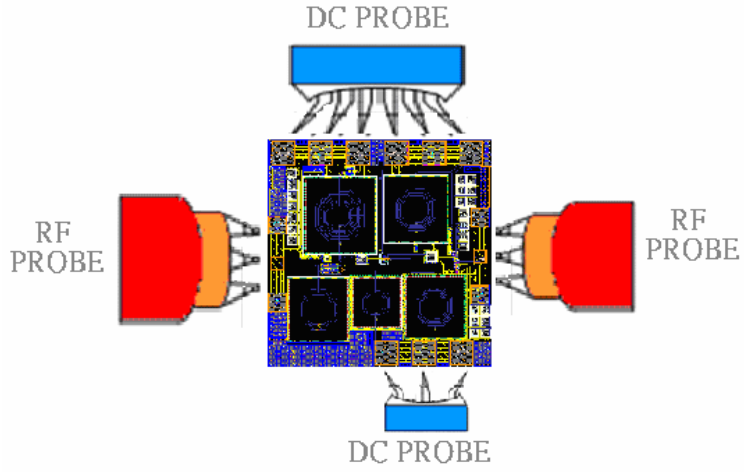


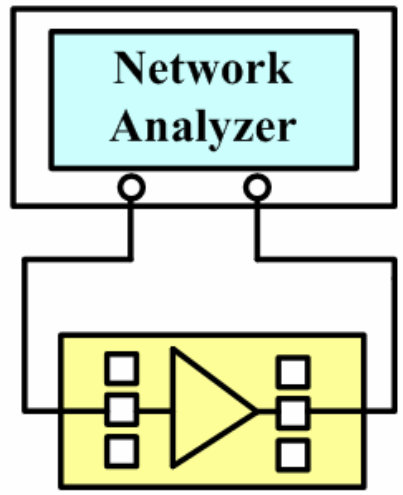
Fig. 2.3.1 (b) On-wafer measurement of 3-8 GHz LNA test diagram

Fig. 2.3.1 (c) The photo for measurement environment

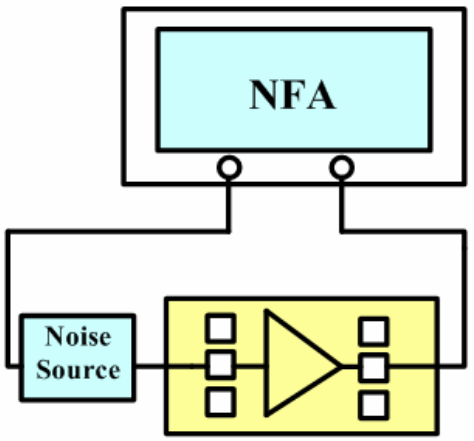
The measurement equipments include a network analyzer (HP8510C), a noise analyzer (Agilent N8975A), a spectrum analyzer (Agilent E4407B), two signal generators, and several dc power supplies. The measurement setups for S-parameter, noise figure are shown in Fig. 2.2.14 (a~b). We use the RF IC measurement system powered by LabView to measure the linearity of the UWB LNA. The measurement setups for 1-dB compression point (P1dB), IIP3 are shown in Fig. 2.2.14 (c~d). We will discuss the experimental and testing results of this circuit in following sections.

HP-8510C network analyzer

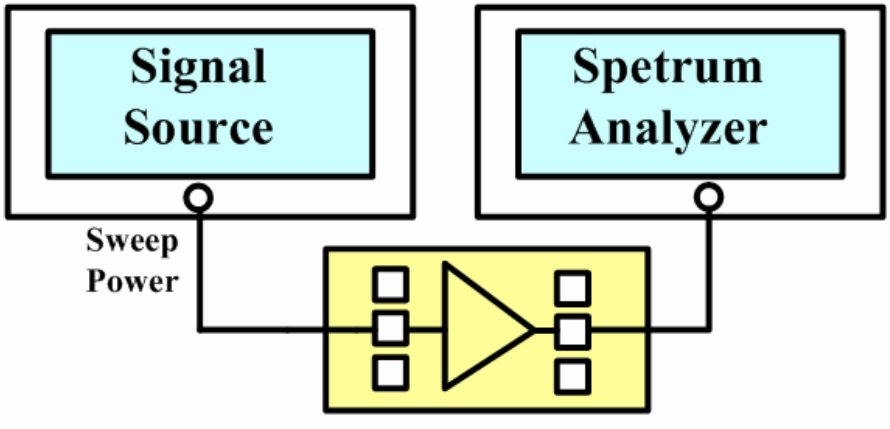
N 8975A 之雜訊分析儀



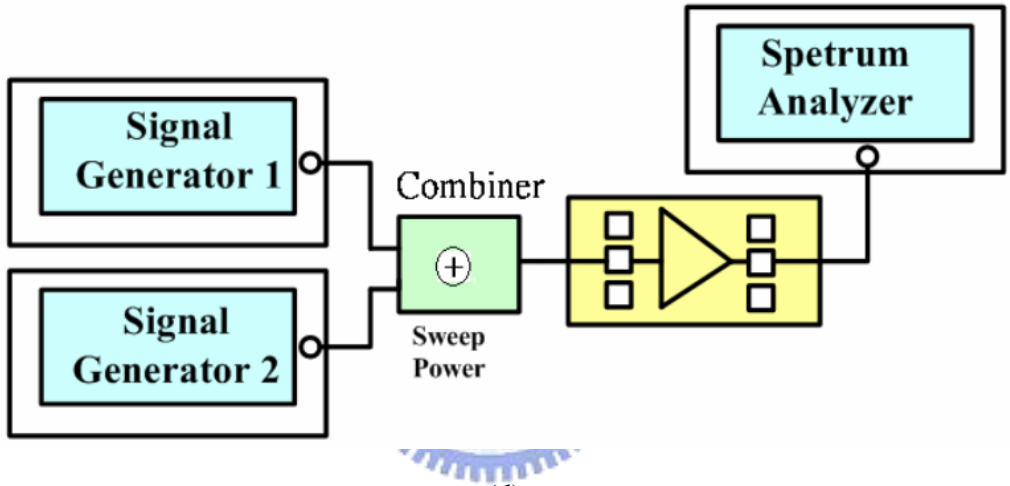
(a)



(b)



(c)



(d)

Fig. 2.3.2 Measurement setups for (a) S-parameter (b) noise figure (c) P1dB (d) IIP3

B. Folded UWB LNA Measurement result

The layout and chip photo of the proposed folded UWB LNA is shown in Fig 2.2.15 and Fig 2.2.16, respectively. A DC block capacitor is needed in the input of the UWB LNA to isolate the dc between circuit and equipment.

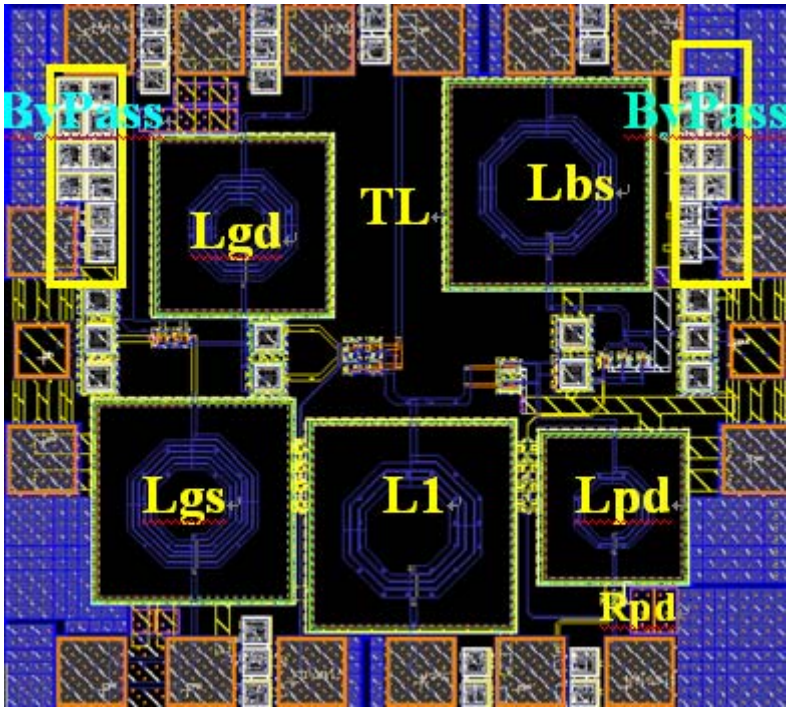


Fig 2.3.3 Layout of the proposed low-voltage LNA

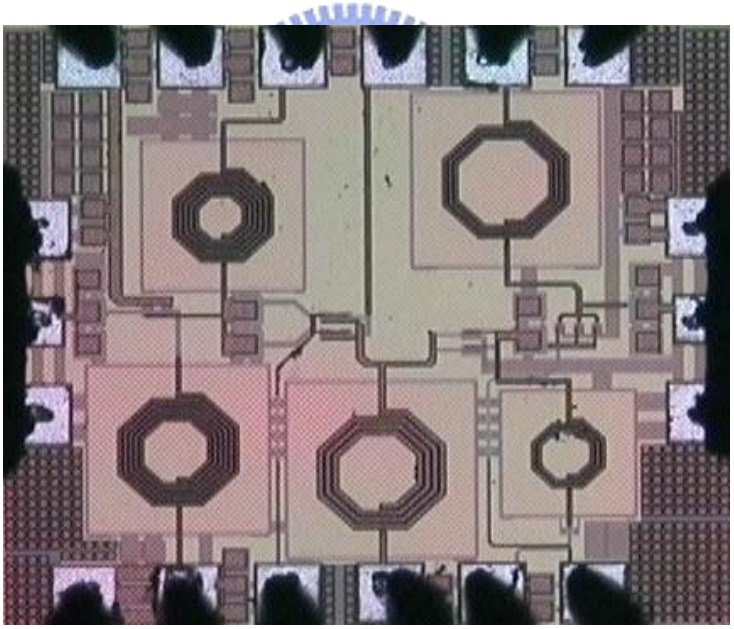


Fig2.3.4 Micrograph of the proposed low-voltage LNA

This work is designed and processed using TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology. The S-parameter are shown in Fig. 2.2.17(a) (b), Fig. 2.2.18 and Fig. 2.2.19, where the measured S11 < -10dB and S22 < -9 dB from 3.1 GHz to 10.6 GHz, except the point which produces peak value. The power gain (S21) is around 7.5dB from 3.1 to 7.5 GHz, the 3dB bandwidth is 2.9-8.7 GHz. The measured noise figure of

4.8-7.5 dB from 2.75 to 7.7 GHz has been presented in the proposed as shown in Fig. 2.2.20. The measured P_{1dB} are -14dBm at 5.1 GHz, and -10dBm at 7.5 GHz in Fig. 2.2.21. The measured IIP3 are -4dBm at 5.1 GHz, and -1.2dBm at 7.5 GHz in Fig. 2.2.22.Table2.2.1 summarizes the measured data of proposed wideband LNA.

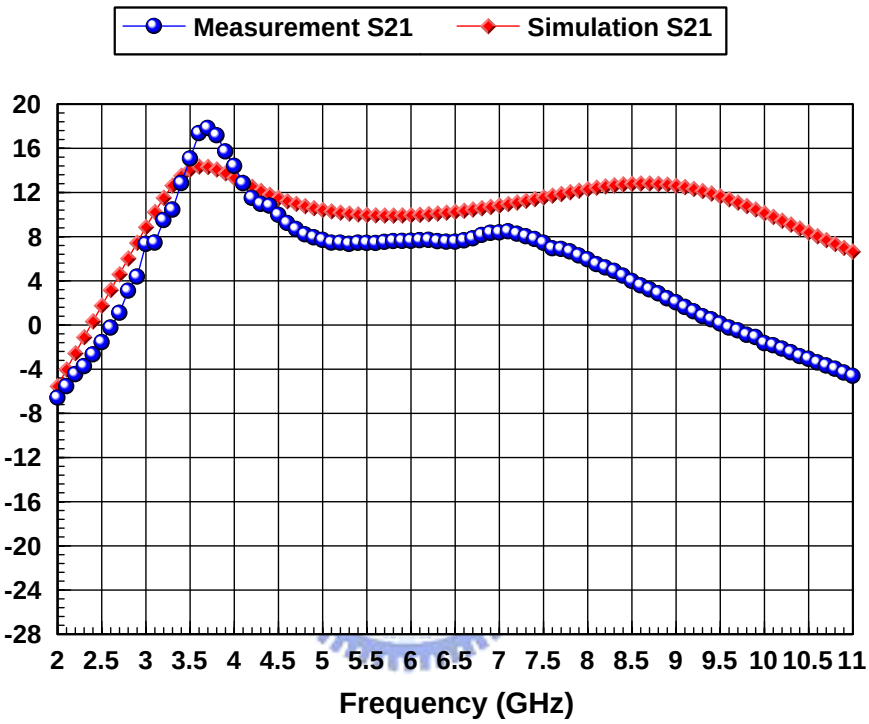


Fig. 2.3.5 (a) Power gain vs. Frequency

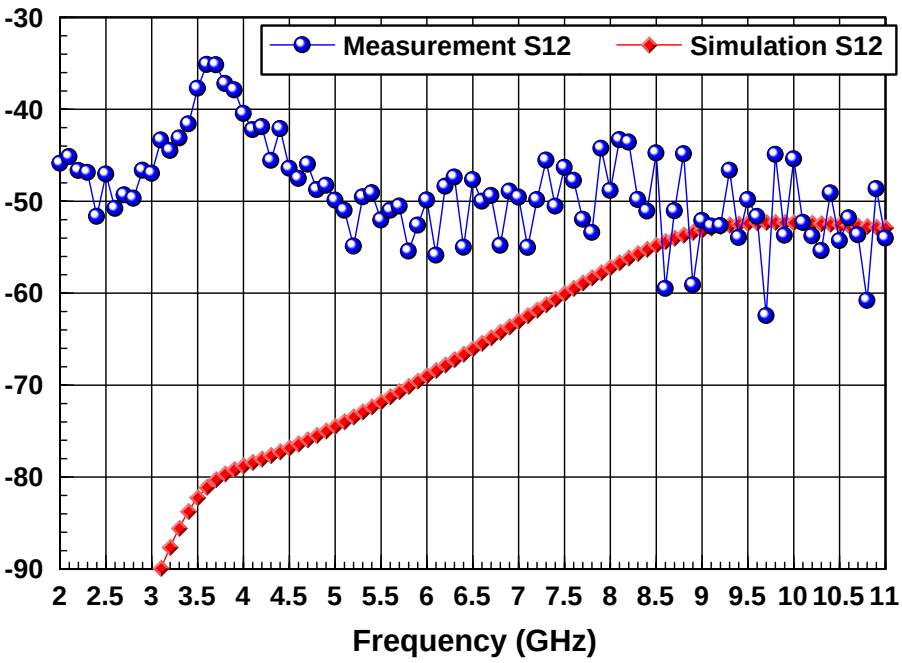


Fig. 2.3.5 (b) Isolation vs. Frequency

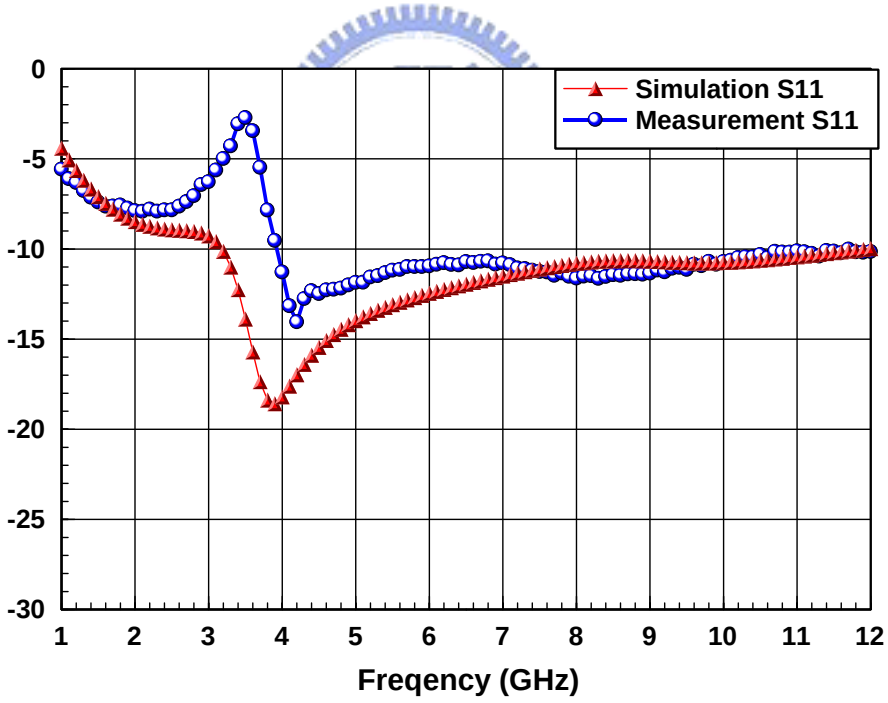


Fig. 2.3.6 Input return loss coefficient vs. Frequency

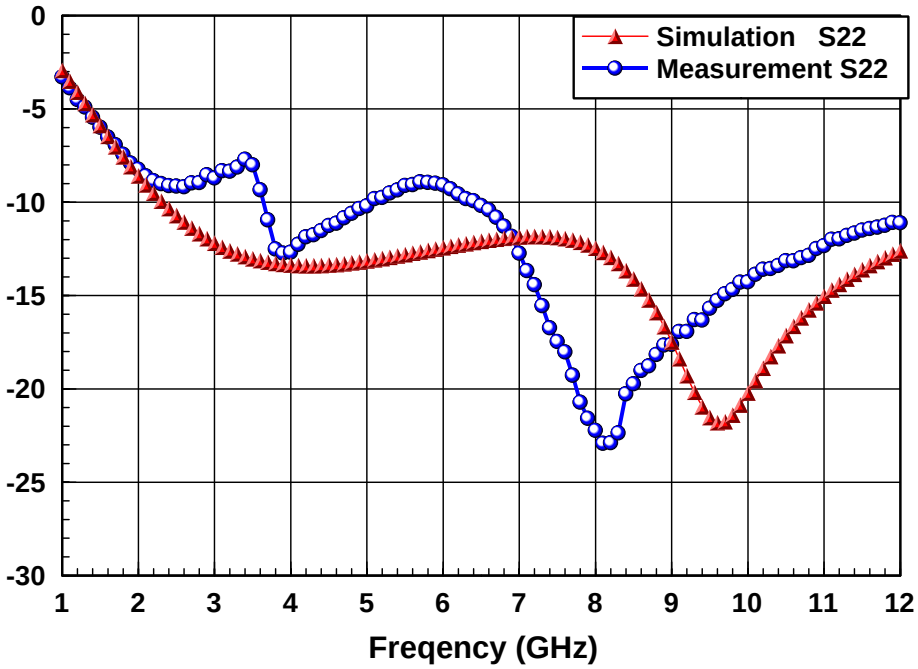


Fig. 2.3.7 Output return loss coefficient vs. Frequency

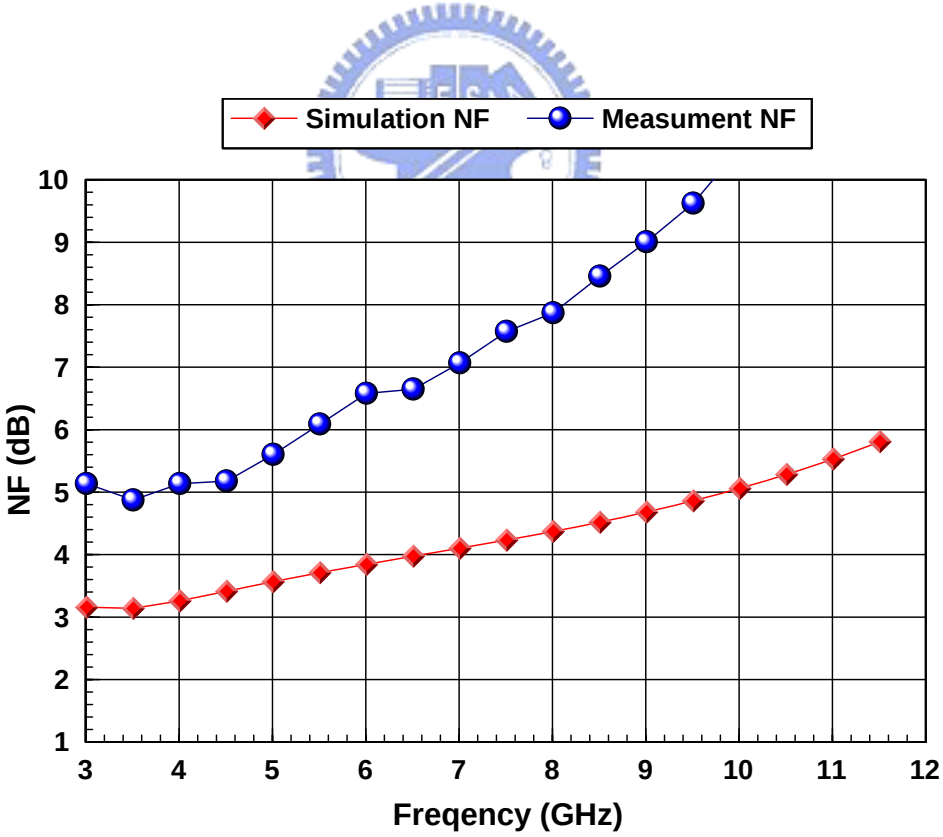


Fig. 2.3.8 Noise Figure vs. Frequency

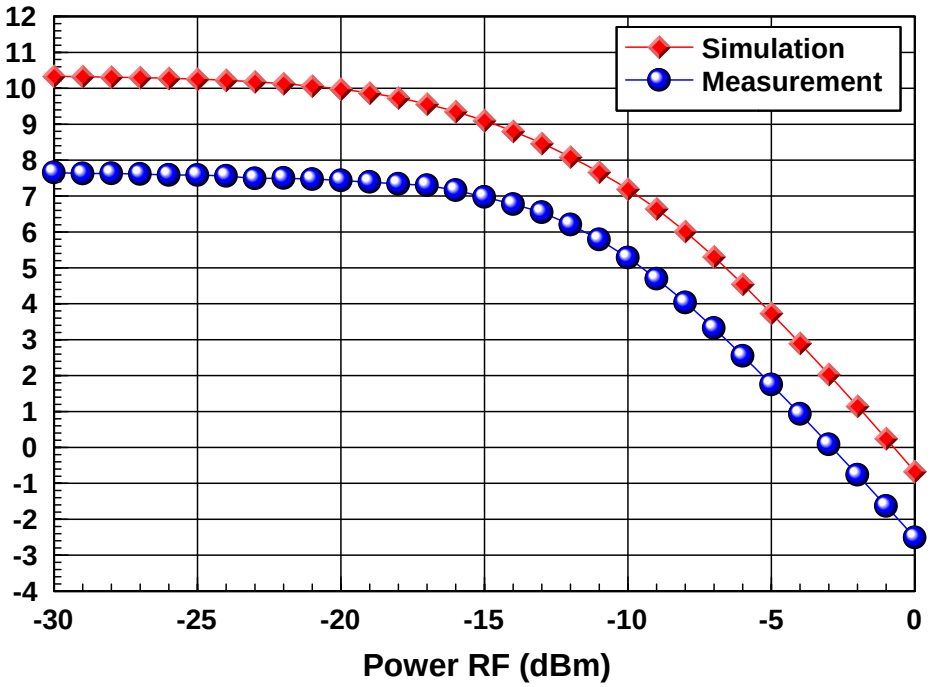


Fig. 2.3.9 (a) P1db at 5.1 GHz

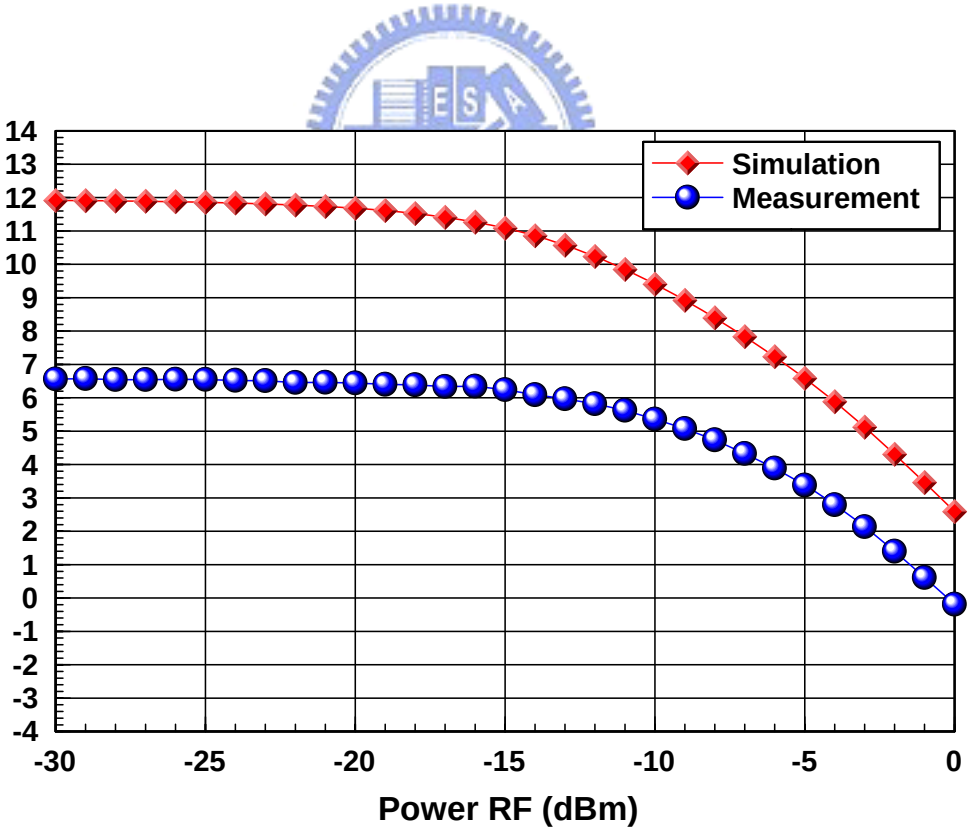


Fig. 2.3.9 (b) P1db at 7.5 GHz

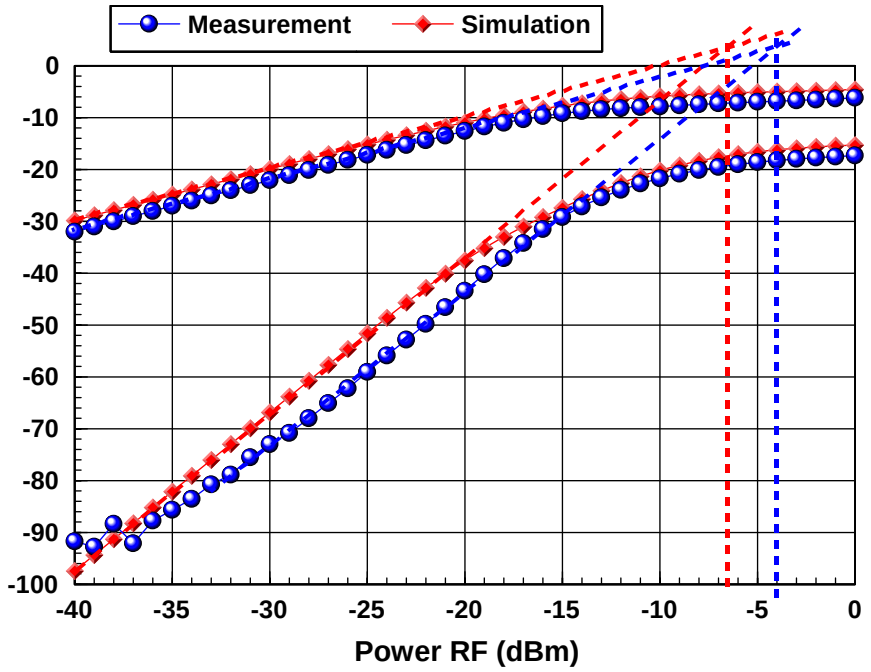


Fig. 2.3.10 (a) IIP3 at 5.1 GHz

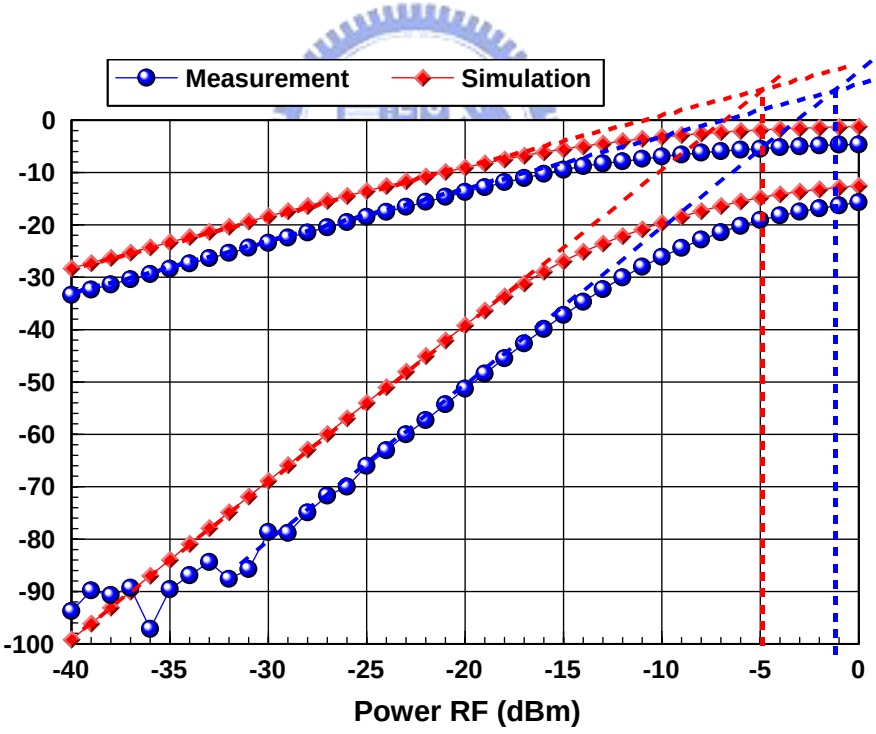


Fig. 2.3.10 (b) IIP3 at 7.5 GHz

Table.2.3.1 Performance summary of the proposed LNA

Specification	Measurement	Post Simulation
BW (GHz)	3 — 7.5	3 — 10
S11 (dB)	<—10	<—10
S22 (dB)	<—9	<—10
S21 (dB)	7.5 (flat gain)	10.5 (flat gain)
S12 (dB)	<—34	<—50
Noise Figure (dB)	4.8-7.5	3.1-5.1
P_{1dB} (dBm)	-14 *	-16 *
IIP3 (dBm)	-4 *	-6.5 *
Vdd (V)	0.75 V	0.75 V
Total Power (mW)	11	11.3

*at 5.1 GHz

C. Capacitor Feedback UWB LNA Measurement result

The layout and microphotograph of the UWB LNA circuit is shown in Fig. 2.3.11 and 12, respectively. The circuit is fabricated in the TSMC 0.18μm CMOS process technology. The die area including bonding pads is 0.825 mm by 0.94 mm.

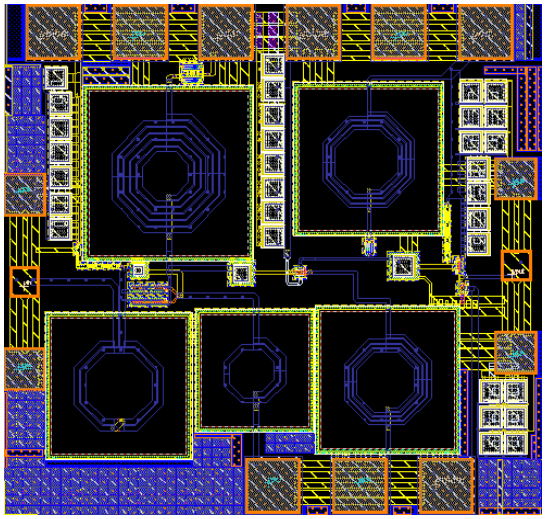


Fig. 2.3.11 (a) Layout of UWB LNA (0.88*0.93mm^2)

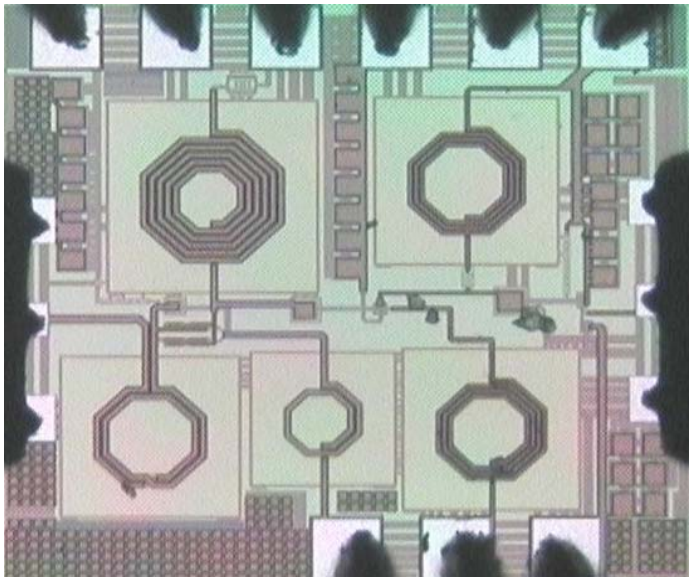


Fig. 2.3.12 (b) Photograph of UWB LNA (0.88*0.93mm^2)

The S-parameter of simulation and measured results are plotted as shown from Fig.2.2.24 to Fig.2.2.26. The measured power gain S21 achieves the maximum value of 10.8dB at 2.7 GHz and the 3-dB bandwidth of power gain is from 1.9 GHz to 8.2 GHz. The variation of inductor (Ld) lead to shunt peaking method don't achieve adaptable m to enhance bandwidth and thus the power gain in high frequency will become small. The average simulated and measured result of S22 are both smaller than -10dB, as shown in Fig.2.2.26. The S11 is shown in Fig .2.2.25. The measured result shows that the proposed circuit using transistor's intrinsic capacitor feedback achieve -10 dB input reflection coefficient from 2.75 GHz to 12 GHz. The measurement and simulation result of noise, NF, is shown in Fig.2.2.27. The simulated minimum noise figure is 2.45dB at 5GHz, and the average noise figure is about 2.6dB. The measured minimum noise figure is 3.64dB at 3 GHz, and the average noise figure is about 4.6dB. Fig.2.2.28. is the simulation and measurement result of the input 1 dB compression point (P1dB). The two-tone test measured results for third-order intermodulation distortion are shown in Fig. 2.2.29. The measured result of IIP3 is -1.8 dBm and 1 dBm at 4.1 GHz and 7.5 GHz, individually. The core current of the proposed LNA is 15mA with a power supply

1.5V. Table 2.2.2 is the summary of simulated and measured performance of the proposed amplifier.

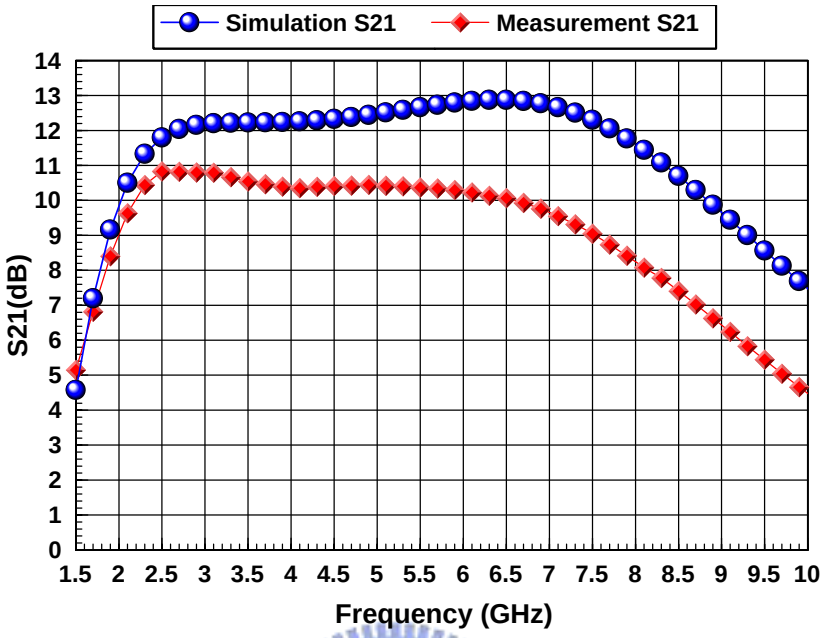


Fig. 2.3.13 S parameter vs. frequency

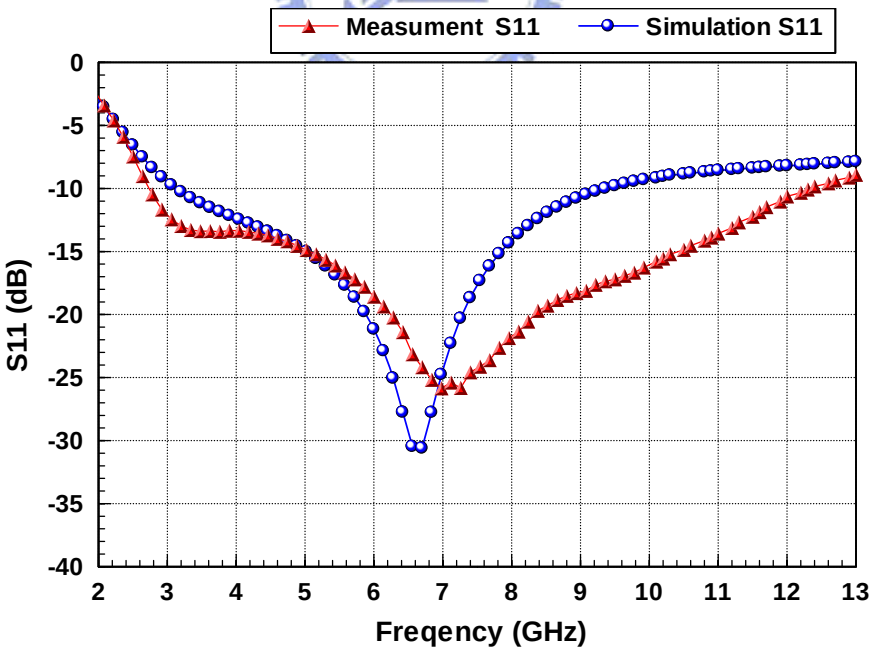


Fig. 2.3.14 S11 vs. frequency

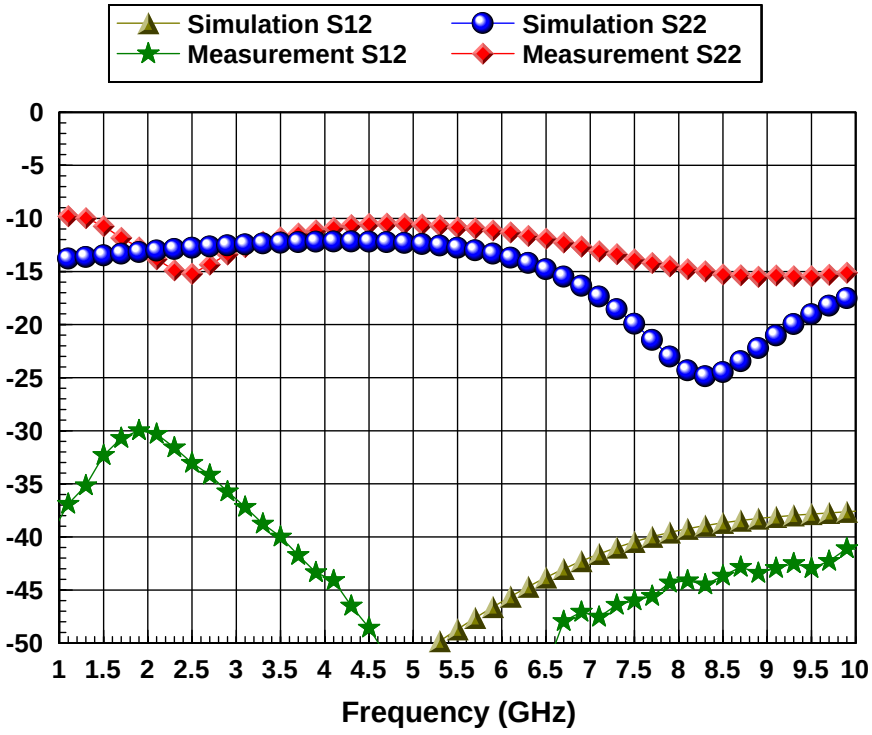


Fig. 2.3.15 S22 vs. frequency

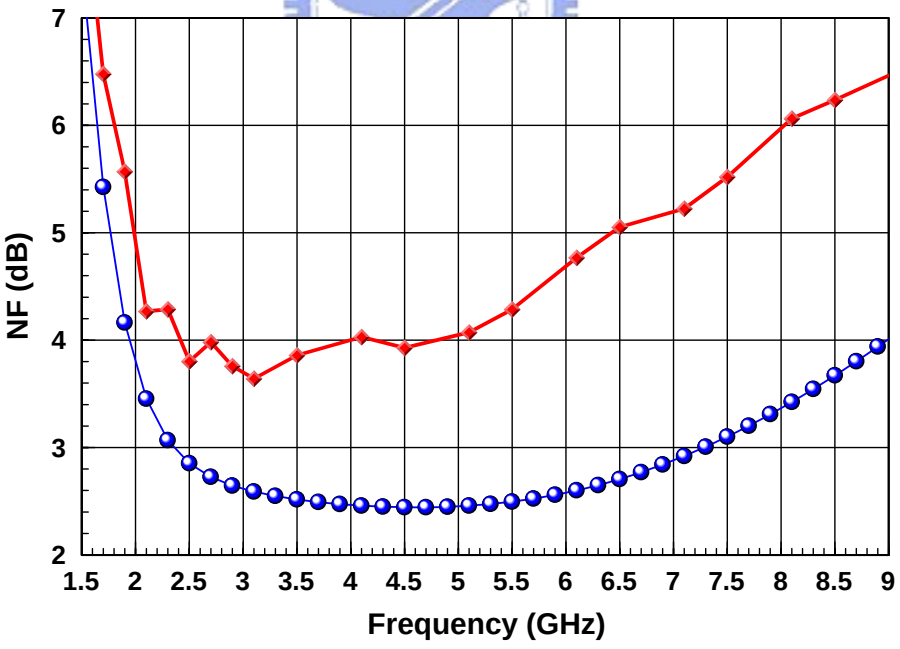


Fig.2.3.16 Noise Figure vs. frequency

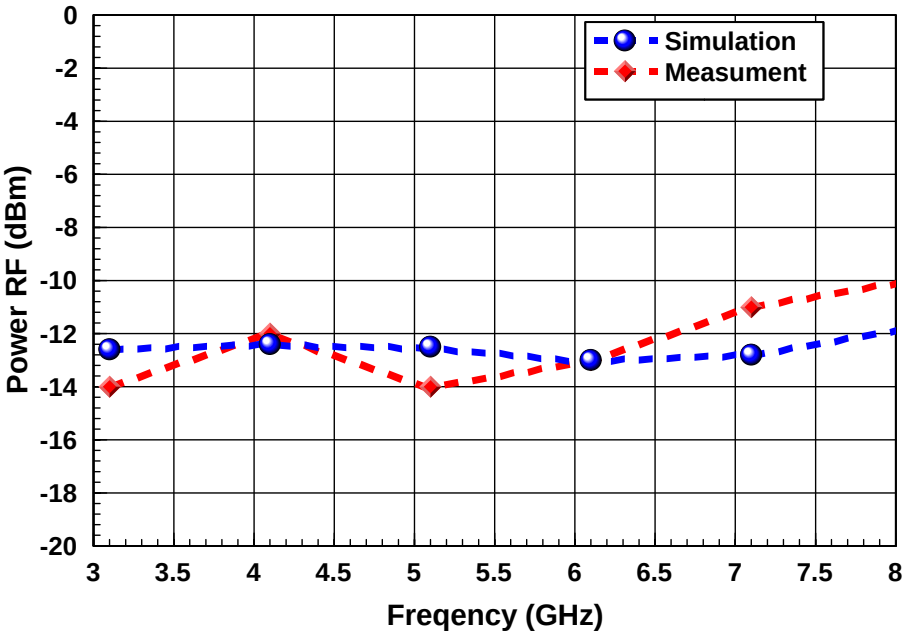


Fig. 2.3.17 Input 1 dB compression point vs. frequency

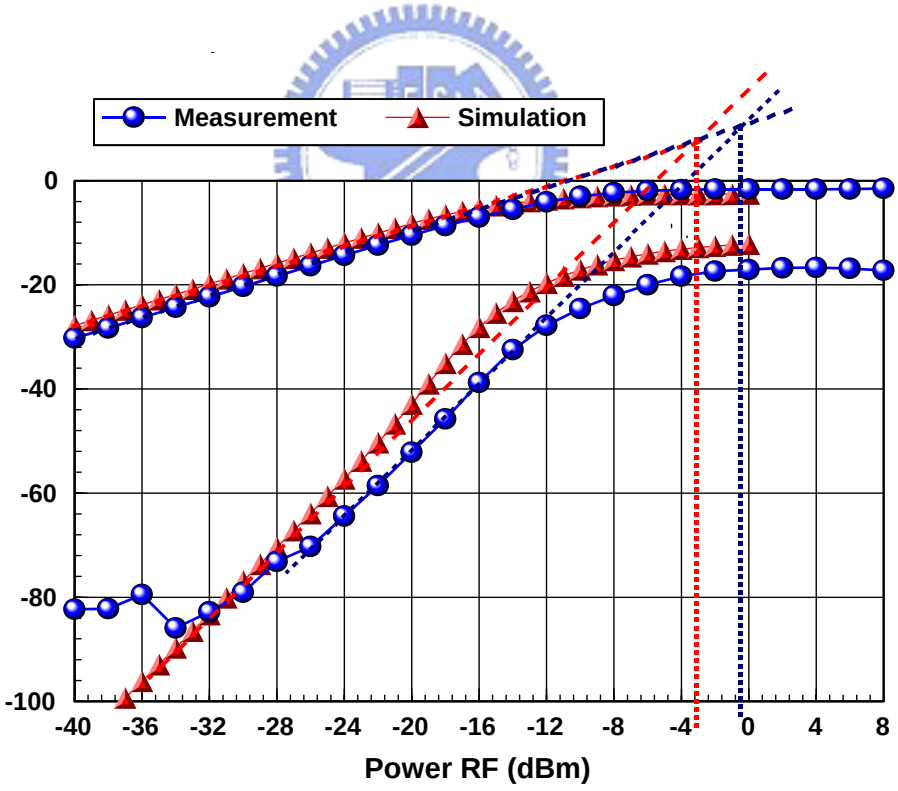


Fig. 2.3.18 (a) IIP3at 4 GHz

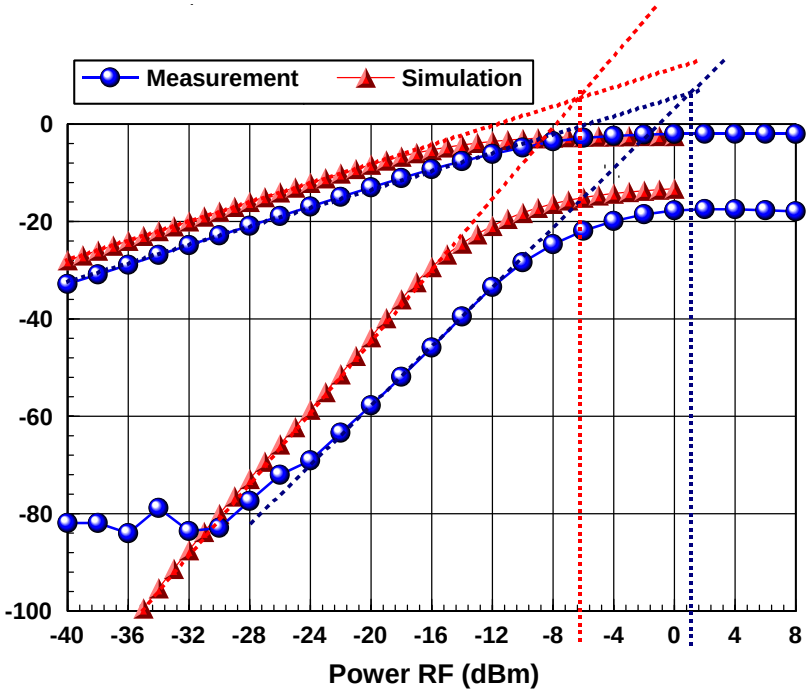


Fig. 2.3.18 (b) at 7.5 GHz

Table.2.3.2 Performance summary of the proposed LNA

	Simulation	Measurement
VDD	1.5	1.5
Band Width	3.1Ghz-8.1Ghz	2.75-7.7Ghz
3dB-bandwidth	1.9-9.5Ghz	1.8-8.3Ghz
$S21_{max}$(dB)	12.8	10.8
S11(dB)	< -10.1	< -10.0
S22(dB)	< -12	< -10
$NF_{average}$(dB)	2.6	4.6
P1db(dBm)	>-13	>-14
IIP3(dBm) at 4 GHz	-3	-1.8
UWB LNA Current	15mA	15.3mA
Buffer	5.5mA	5.8mA

2.4 Comparison and Discussion

Table 2.4.1 Comparison of Ultra Wide-band LNA

Ref.	Process	BW (GHz)	S11 (dB)	S22 (dB)	Gain $_{Ave.}$(dB)	NF (dB)	P1dB (dBm)	VDD (V)	Power (mW)
Work 1 (Meas.)	0.18um CMOS	3.1-7.5	<-10	<-9	7.5	4.8-7.7	-14#	0.75	11.3
Work 2 (Meas.)	0.18um CMOS	2.75-7.7	<-10	<-10	10	3.7-5.5	>-14	1.5	23*
[28] 2004 (Meas.)	0.18um CMOS	2.3-9.2	<-9.9	<-10	9.3	4.0 (min)	-6.7	1.8	9 *
[4] 2004 (Meas.)	0.18um CMOS	3.1-10.6	<-10	<-9	18	5-7	N/A	1.8	54
[29] 2007 (Meas.)	0.18um CMOS	3.1-10.6	<-9	<-15	12	3.8 (min)	N/A	1.8	9.8*
[8] 2006 (Sim.)	0.18um CMOS	3.1-10.6	<-9	<-13	16-17.5	3.1-5.7	-33#	1.8	33.2
[26] 2007 (Mea.)	0.18um CMOS	2.7-9.1	<-10	<-10	10	3.8-6.9	N/A	0.6	7
[27] 2005 (Mea.)	0.18um CMOS	2-4.6	<-9	<-10	9.8	2.3-4.2	N/A	1.8	12.6*

at 5 GHz *Core circuit

In the first work (Low-voltage UWB LNA) which reveal wideband performance under low voltage situation. But it is unexpected in the measured results at 3-4 GHz as simulation. Because the fabricated inductor value of TL (common source degeneration inductor) is not expected as simulated inductor value of TL, it causes the circuit is seemly unstable at 3-4 GHz. The unstable behaviors make the S11 and S22 to produce peaking value as measured results. And the variation of inductor (Ld) lead to shunt peaking method don't achieve adaptable m to enhance bandwidth and thus the power

gain in high frequency will become small. The phenomenon of decreasing power gain in high frequency is maybe caused by parasitic capacitor of layout path. The second work (3-8 GHz capacitor feedback wideband low noise amplifier) which achieves perfect ultra wide-band input impedance matching from 2.75 to 12 GHz. The measured noise figure is greater than simulated result about 2 dB, it may be caused by the inexactitude noise model and the abridgement of power gain. Table 2.4.1 shows the comparisons of these two works and other recently ultra wide-band LNA papers.

Chapter 3 A Folded Current-Reused Mixer for UWB Applications System

3.1 Introduction

Fig. 3.1.1 shows the architecture of UWB receiver. The mixer of the receiver is introduced in this chapter. In order to realize ultra wide-band circuits, many specialized technologies and devices like SiGe, GaAs, InP, HBT and HEMT have been employed. Although using specialized technologies and devices can achieve good performances, but there are some drawbacks such as high dc power consumption, high supply voltage and were not suitable for UWB system applications.

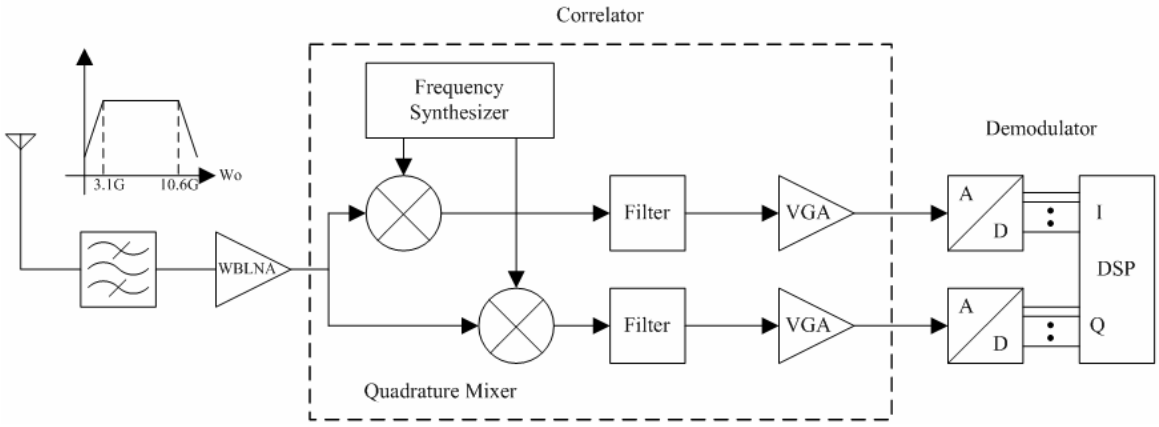


Fig. 3.1.1 Block diagram of a UWB receiver [7]

A distributed mixer has been designed in 0.18um CMOS technology [9], as shown in Fig 3.1.2. Although the design exhibits good noise performance, but the bandwidth could not cover the entire frequency band from 3.1 to 10.6 GHz and large die area is needed.

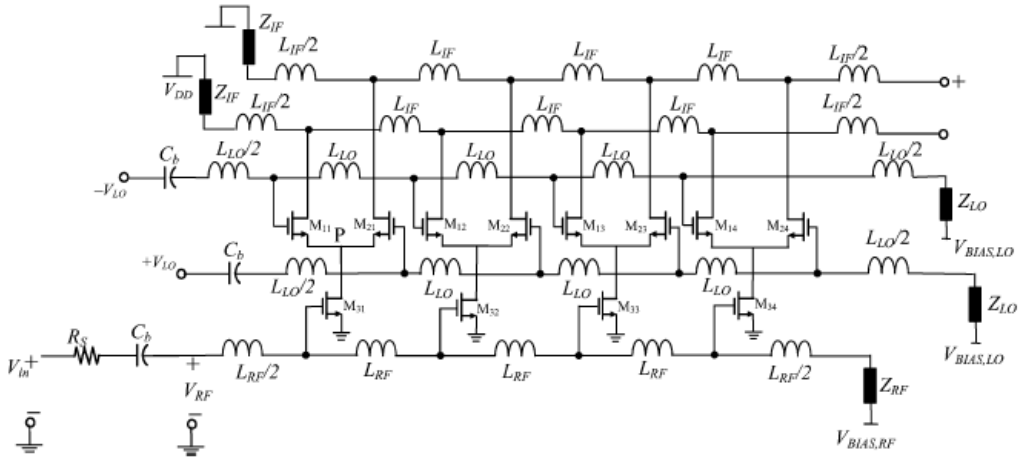


Fig 3.1.2 Ultra wide-Band Distributed CMOS Mixer [9]

A CMOS UWB mixer has been designed in 2004 year as shown in Fig 3.1.3 [10]. This design has some disadvantages. It uses multiple voltage sources, the values of which are 3.3-5V. And its power consumption is high.

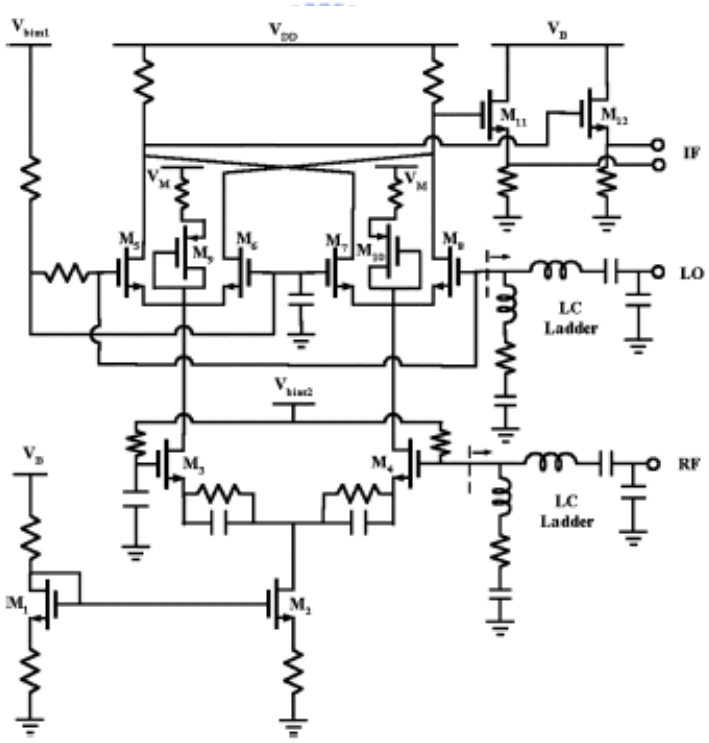


Fig 3.1.3 CMOS Ultra wide-Band Mixer [10]

In this work, a wide-band mixer based on Gilbert cell architecture combined with folded current-reused pair is proposed in 0.18μm CMOS technology. It still achieves high conversion power gain in low dc power consumption and low supply voltage

situation. The proposed mixer achieves a simulated conversion power gain of 10.3-13.7 dB and double side-band noise figure of 11.1-14.7 dB from 3.1 to 10.6 GHz with a fixed IF of 100 MHz under dc power consumption of 10.95 mW.

3.2 Review of basic mixer

3.2.1 Basic mixer topology

The mixer is a frequency translation device. The operation function of the mixer can be shown in Fig 3.2.1. It performs frequency translations by multiplication of a RF signal and a LO signal.

$$(A\cos\omega_1 t)\bullet(B\cos\omega_2 t)=\frac{AB}{2}[\cos(\omega_1-\omega_2)t+\cos(\omega_1+\omega_2)t]$$

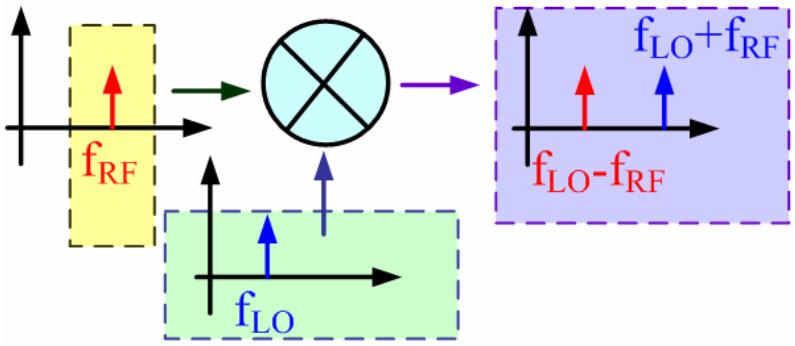


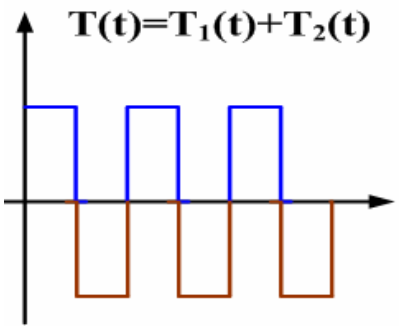
Fig 3.2.1 Operation of mixer

Based on the mixer topologies, the mixer can be divided into three parts: Single balance mixer, double balance mixer, passive mixer [11] [12] [13] [14].

A. Single balance mixer

Fig 3.2.2 shows a single balance mixer which is a switching type mixer. Feed-through is a basic problem in switching mixer. But the problem can be eliminated by using a differential IF output and polarity reversing LO switch called “Single balance mixer”. It consists of three stages. One is the trans-conductance stage which

converts the RF voltage in a current. One is the switching stage which performs multiplication to RF current into IF current. One is the load stage which converts IF current into IF voltage. The LO function is shown in equations (3-1).



Switching Function [11]

$$\mathrm{T(t)=Square\ Wave=T_1(t)+T_2(t)}=\frac{4}{\pi}[\sin(\omega_{Lo}t)+\frac{1}{3}\sin(3\omega_{Lo}t)+...] \qquad (3\text{-}1)$$

So

$$V_{IF}(t)=R_L\cdot[I_{DC}+g_m v_{RF}\cos(w_{RF})t]\cdot\frac{4}{\pi}[\sin(w_{LO})t+\frac{1}{3}\sin(3w_{LO})t+...]$$
$$=\frac{4R_L}{\pi}\{I_{DC}\sin(w_{LO})t+\frac{1}{2}g_m v_{RF}[\sin(w_{RF}+w_{LO})t+\sin(w_{RF}-w_{LO})t]+...\} \qquad (3\text{-}2)$$

Conversion Gain= $\frac{2g_mR_L}{\pi}$

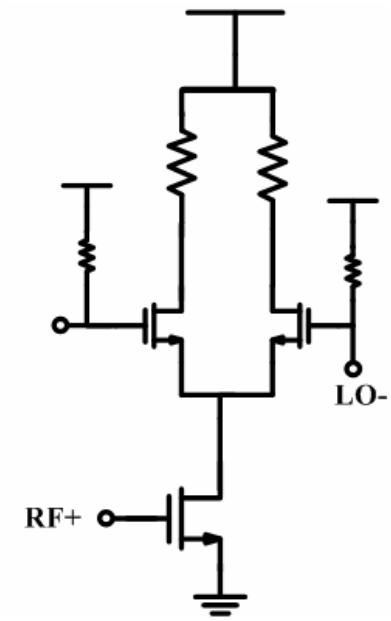


Fig 3.2.2 Single balance mixer

B. Double balance mixer

Single balance mixer still has LO feed-through problem. Fig 3.2.3 shows a double balance mixer which can eliminate the drawback of LO feed-through.

For double balance mixer:

$$\begin{aligned} V_{IF}(t) &= R_L[I_{DC} + g_m v_{RF}\cos(\omega_{RF}t)]\cdot\frac{4}{\pi}[\sin(\omega_{LO}t)+\frac{1}{3}\sin(3\omega_{LO}t)+...] \\ &- R_L[I_{DC} - g_m v_{RF}\cos(\omega_{RF}t)]\cdot\frac{4}{\pi}[\sin(\omega_{LO}t]+\frac{1}{3}\sin(3\omega_{LO}t)+...] \\ &= \frac{8}{\pi}R_L g_m v_{RF}\cos(\omega_{RF}t)[\sin(\omega_{LO}t]+\frac{1}{3}\sin(3\omega_{LO}t)+...] \end{aligned} \tag{3-3}$$

Double balance mixer removes the LO feed-through because the DC term cancels.

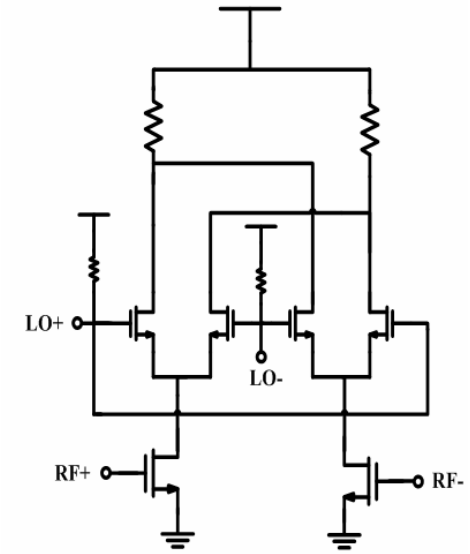


Fig 3.2.3 Double balance mixer

Comparisons of Mixers			
Mixer Type	LO-Balanced	RF-Balanced	Double-Balanced
RF/IF isolation	Good	Poor	Good
LO/IF isolation LO/RF isolation	Poor Good	Good Poor	Good Good
LO harmonics rejection	Even	All	All
RF harmonics rejection	No	Yes	Yes
Two-tone 2^{nd} order products rejection	No	Yes	Yes

3.2.2 Some special mixer topology

A. Conversion Gain Enhancement

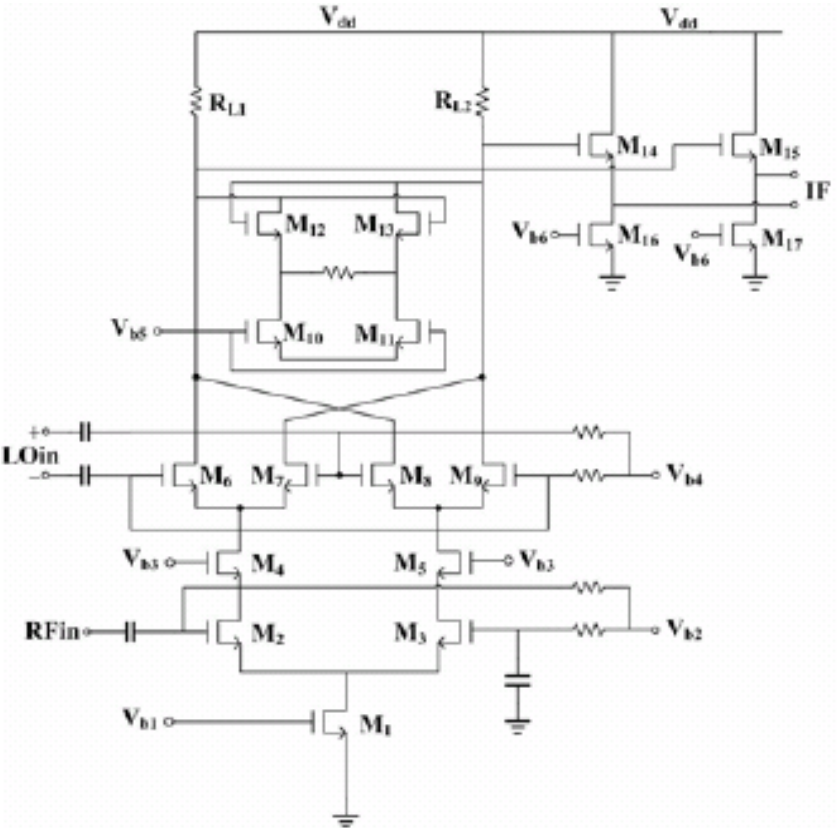


Fig 3.2.4 Negative resistor Load Gilbert Cell Mixer [15]

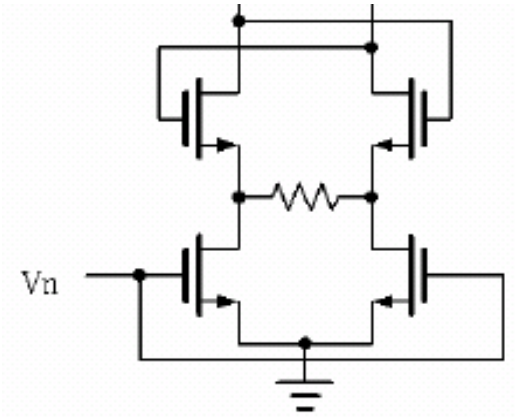


Fig 3.2.5 Negative resistor topology [16]

Figure 3.2.4 shows a Gilbert Cell Mixer with negative resistor load. A negative resistor

topology is shown in Fig 3.2.5. Conversion gain equation can be driven as shown:

$$CG = \frac{2}{\pi}.g_m.R_{load} \tag{3-4}$$

, where $Z_{load} = R_{load} // \frac{-2}{g_m}$

We can tune the bias voltage befittingly to get the optimum conversion gain and linearly. The transistors of M4 and M5 can increase isolation between LO port and RF port.

B. Current Bleeding Method [17]

From equation (3-3), the mixer gain for a CMOS double balance type mixer is given by

$$A_v = g_m R_L \frac{2}{\pi} = \sqrt{K_n I_{SS}} R_L \frac{2}{\pi} \tag{3-5}$$

And the IP3 of the CMOS Gilbert mixer is approximately given as

$$IP3 = \sqrt{\frac{32}{3} \cdot \frac{Iss}{K_n}}$$

The mixer gain and IIP3 is therefore proportional to $\sqrt{I_{ss}}$. Consequently, it seems that an arbitrary increase in the bias current can improve the conversion gain and IP3. But consider the consequence of increasing the bias current, Ohm's Law dictates that the voltage dropped across *RL* increases and the head-room voltage decreases. The output signal will therefore eventually compress at a lower level of signal input. IP3 is then lower, and the overall performance of the mixer is degraded. A method called charge injection as shown Fig 3.2.6 in can achieve conversion gain and linearity at the same time.

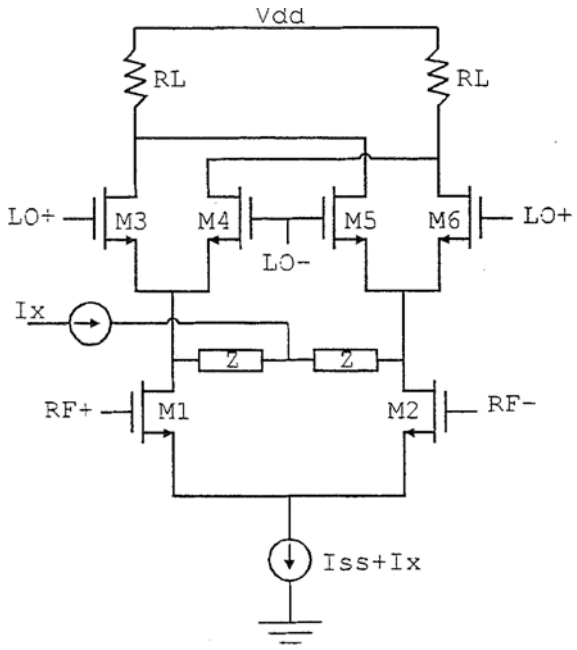


Fig 3.2.6 A Gilbert Cell mixer with charge injection

An additional current source can draw out the current which flows through load stage, so it can enhance the head-room voltage. And a single current source can decrease noise of the mixer.

C. LINEARIZATION TECHNIQUE FOR GILBERT CELL MIXER

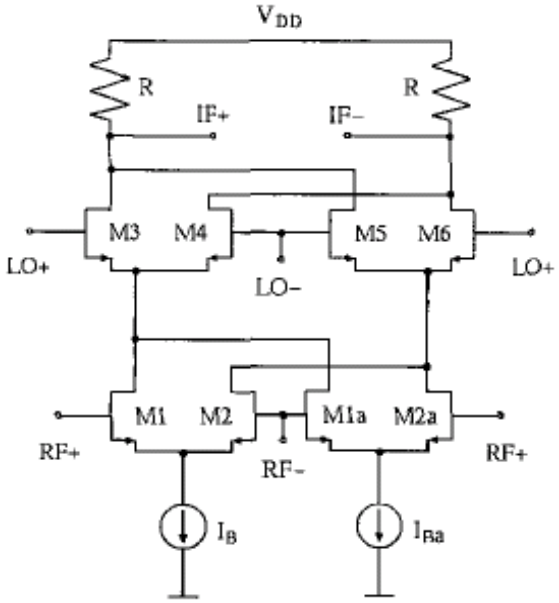


Fig 3.2.7 A Gilbert Cell mixer with multiple differential pair [18]

Figure 3.2.7 is a compensative circuit for linearization. The IIP3 of the mixer is approximately given as:

$$IIP_3 = \sqrt{\frac{32}{3}} \cdot \sqrt{\frac{\sqrt{K_{RF} I_B} - \sqrt{K_{RFa} I_{Ba}}}{K_{RF}\sqrt{\frac{K_{RF}}{I_B}} - K_{RFa}\sqrt{\frac{K_{RFa}}{I_{Ba}}}}} \tag{3-6}$$

In equation (3-6), we let denominator to be zero. We can cancel the third-order distortion term effectively. In other word, we should let

$$\frac{I_{Ba}}{I_B} = (\frac{K_{RFa}}{K_{RF}})$$

In this case, ideally we can obtain a very high intercept point ***(IIP₃*** $\rightarrow\infty$). But there are many limiting factors in achieving a very high IIP3 for multiple differential pair mixer in reality: mismatches, the simplified models and the parasitic effects.

3.3 Folded current-reused Ultra-band mixer

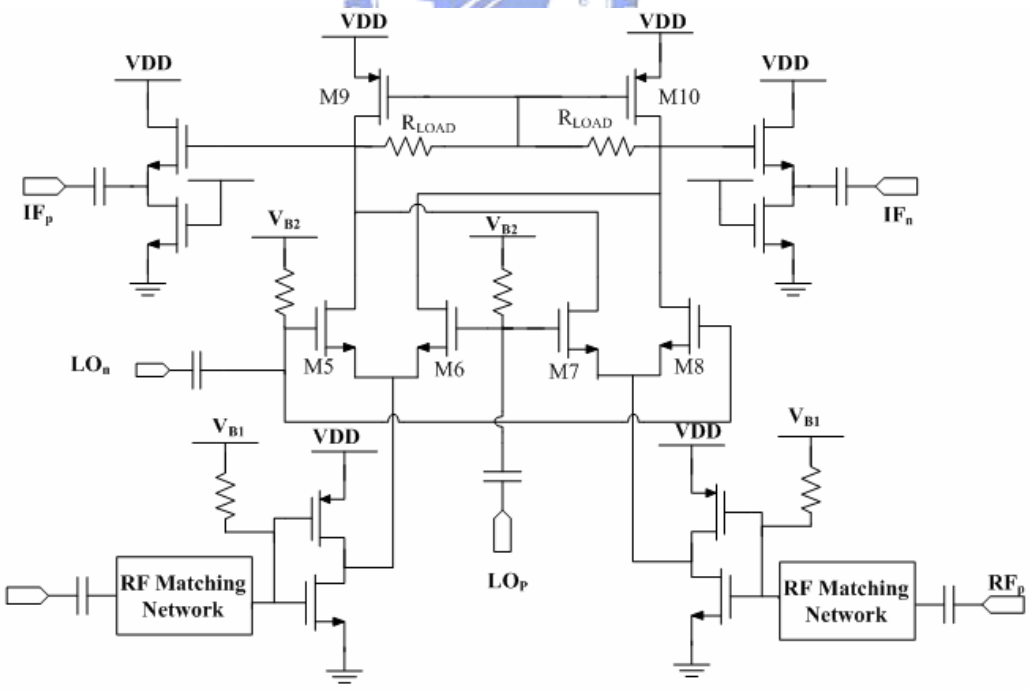


Fig. 3.3.1 Topology of the proposed UWB mixer

Fig. 3.3.1 shows the schematic of the proposed wide-band folded current-reused mixer circuit. The mixer circuit can be divided into five blocks- RF matching network,

RF trans-conductance stage, LO switching stage, active load and IF common collector amplifier.

For RF matching network is shown in Fig. 3.3.2, the second order LC ladder filter which can be equivalent to chebyshev filter is used to achieve wide-band frequency response from 3.1 GHz to 10.6 GHz. The behavior of this circuit is sensitive to the pad capacitance. If the pad capacitance increases, the return loss curve is degraded. The pad size is reduced to 50*50um^2 .The parasitic capacitor of pad is only 30~35 fF.

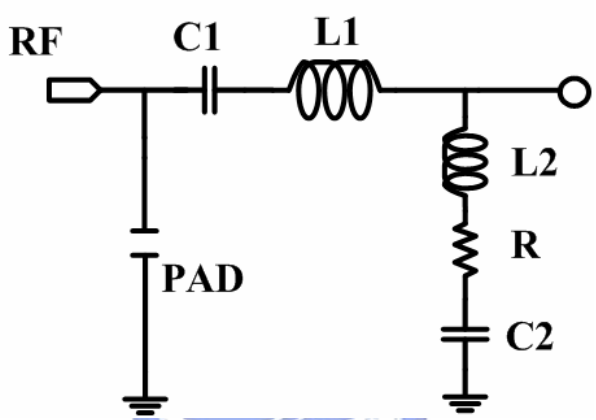


Fig. 3.3.2 RF matching network

For LO port, there is no matching circuit, because of the switch stage biasing in the edge of subthreshold region and saturation region. The transistors M9 and M10 form the simple active load with common mode feedback circuit. It can stabilize the drain voltage of the switched transistors (M5, M6, M7, and M8). In contrast to the conventional Gilbert cell mixer, the proposed mixer replaces the traditional common source trans-conductance stage with a folded current-reused pair. It not only reduces the supply voltage, but also increases trans-conductance (g_m) effectively. Such folded current-reused structure can uses DC current effectively because that the main current flows through trans-conductance stage, switching stage only consumes 100uA. The maximum conversion gain of the folded current-reuse mixer can also be verified as following:

$$V_{IF}(t) = R_L[I_{DC} + (g_{mn} + g_{mp})v_{RF}\cos(\omega_{RF}t)] \cdot \frac{4}{\pi}[\sin(\omega_{LO}t] + \frac{1}{3}\sin(3\omega_{LO}t) + ...]$$

$$- R_L[I_{DC} - (g_{mn} + g_{mp})v_{RF}\cos(\omega_{RF}t)] \cdot \frac{4}{\pi}[\sin(\omega_{LO}t] + \frac{1}{3}\sin(3\omega_{LO}t) + ...]$$

$$= \frac{8}{\pi}R_L(g_{mn} + g_{mp})v_{RF}\cos(\omega_{RF}t)[\sin(\omega_{LO}t] + \frac{1}{3}\sin(3\omega_{LO}t) + ...]$$

$$Conversion \quad Gain = \frac{2}{\pi}R_L(g_{mn} + g_{mp})$$

Where $R_L = R_{LOAD} // r_o$

When R_{LOAD} is increased to provide conversion gain, the CMFB circuit can prevent the dropping of the drain voltage of the switched transistors. This will provide a good linearity when the conversion gain is increased. An output buffer composed of common collector amplifier is added for measurement purposes.

3.4 Chip implementation and measured considerations

Fig. 3.4.1 is the layout of the proposed Ultra wideband mixer. In order to decrease the degree of mismatches, we focus on the symmetry of layout very much. The layout seems to be perfect symmetric except for the different layer of metal. Fig. 3.4.2 is the die photograph of the proposed Ultra wideband mixer.

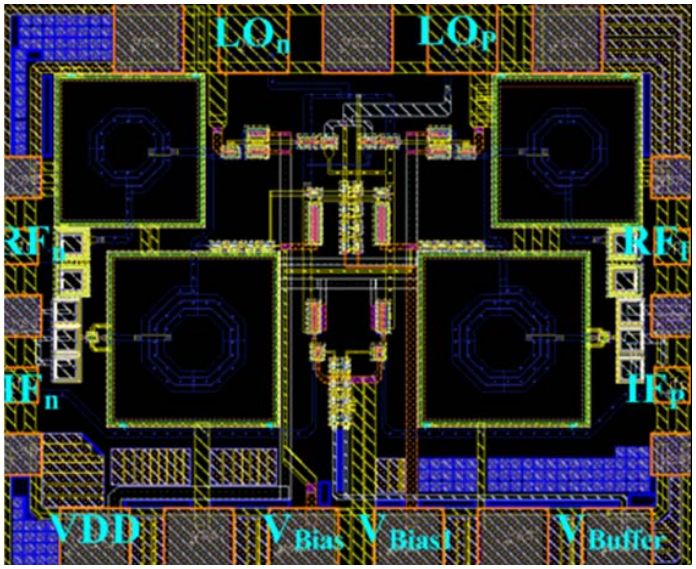


Fig. 3.4.1 Layout of the proposed UWB Mixer

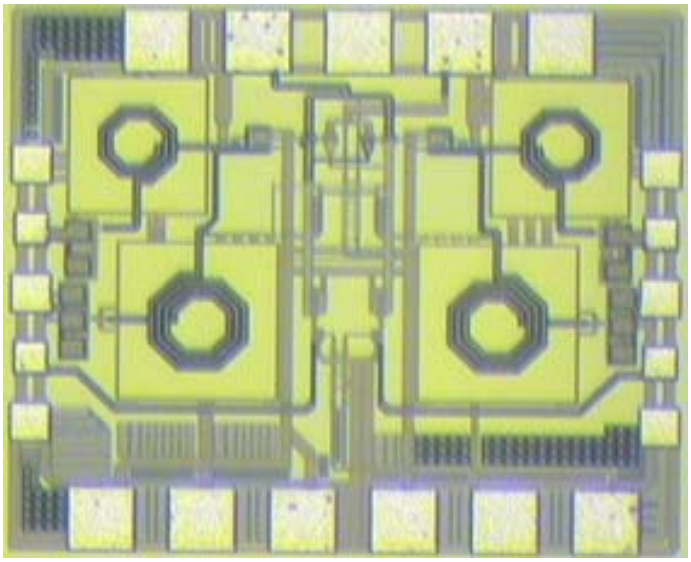


Fig. 3.4.2 Die photograph of the proposed ultra wide-band mixer

The Ultra wideband mixer is designed for on-wafer measurement so the layout must follow the rules of CIC's (Chip Implementation Center's) probe station testing rules. Fig. 3.4.3 shows the on-wafer measurement setup with four probes.

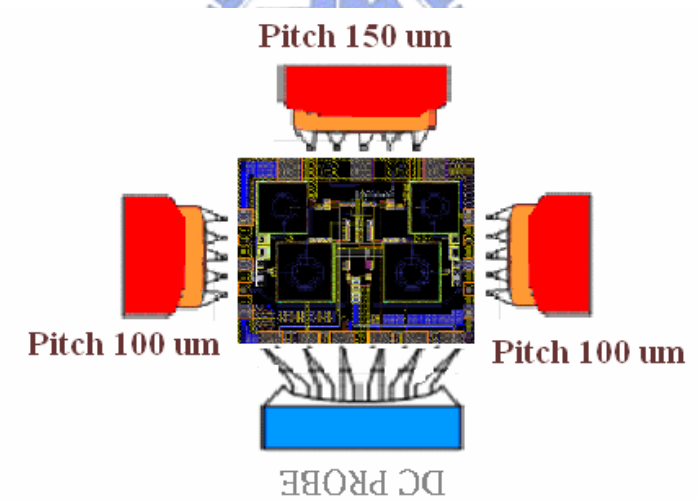
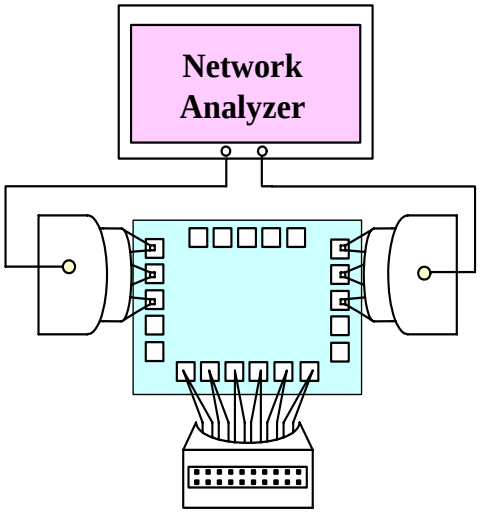
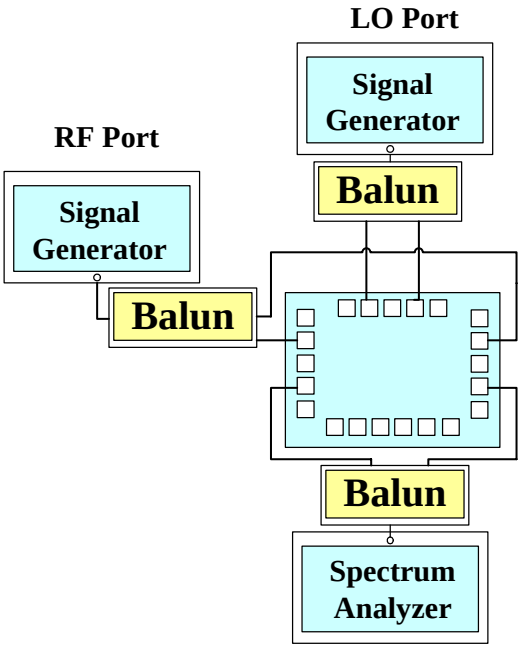


Fig.3.4.3 On wafer measurement for UWB Mixer

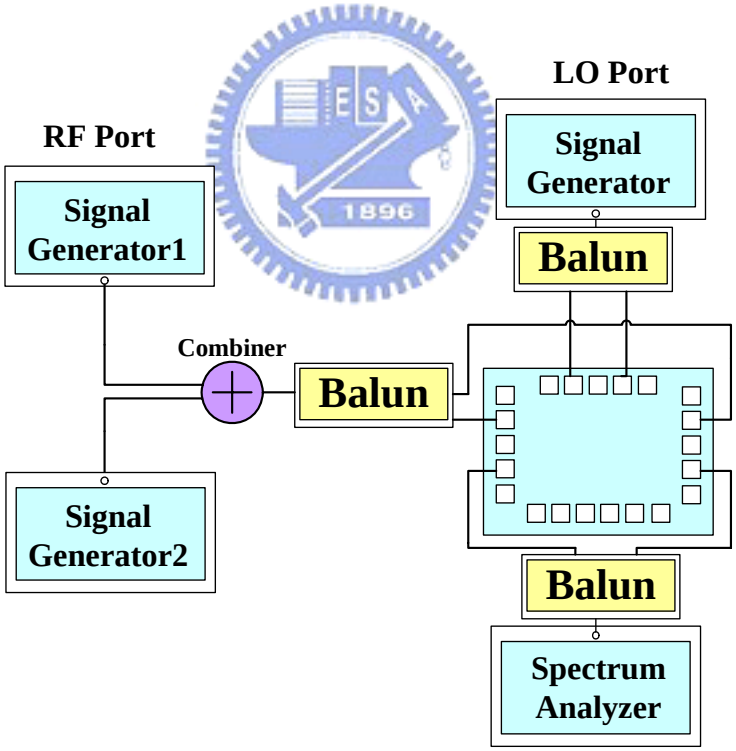
The simplified measurement setups are shown in Fig. 3.4.4 (a~d). We use the RF IC measurement system powered by LabView to measure the linearity and conversion power gain of the UWB mixer. The whole measurement environment in CIC is shown in Fig. 3.4.5.


Network
Analyzer

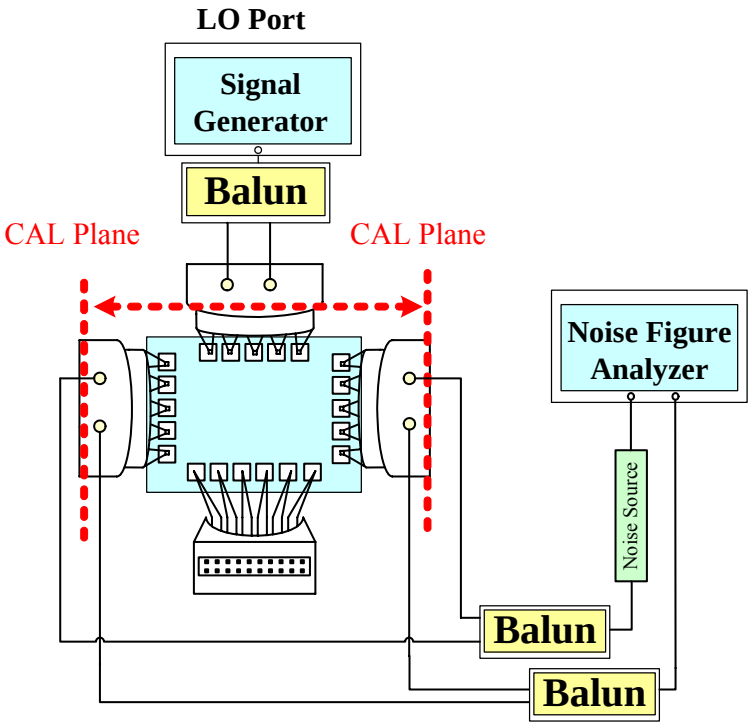
(a)


LO Port
Signal
Generator
RF Port
Signal
Generator
Balun
Balun
Balun
Spectrum
Analyzer

(b)


LO Port
RF Port
Signal
Generator1
Signal
Generator
Balun
Combiner
Balun
Signal
Generator2
Balun
Spectrum
Analyzer

(c)



(d)

Fig. 3.4.4 Measurement setup of the proposed switched Gm sub-harmonic mixer for (a) input return loss (b) conversion gain and P1dB (c) IIP3 (d) noise figure

3.5 Measurement results and discussion

3.5.1 Measurement results

In this section, the measured results are shown below. This folded current-reused mixer consumes 7.5mA and the buffer consumes 7.1mA dc current with 1.5 V power supply. As shown in Fig. 3.5.1, the measured RF port input return loss are better than -10dB through 3.1-8 GHz. As shown in Fig. 3.5.2, the measured IF port input return loss are better than -10dB through 100-528 MHz. Fig. 3.5.3 (A) ~ (M) shows the conversion power gain with lo power sweeping. It reveals that a high conversion power gain is achieved in this work. In simulation, the conversion power gain has maximum, when Lo power is during -4 and -1 dBm, but in measurement, the conversion power gain has maximum, when Lo power is during -12 and -8 dBm. Fig 3.5.4 shows that the measured results reveal that conversion power gain are 13.5-15.5 dB from 3.1 to 8 GHz. Fig. 3.5.5 shows the DSB noise figure with the IF=150 MHz. It reveals that the DSB noise figure is 11-14.5 during 3.1-8 GHz. Fig. 3.5.6 shows that the P1dB of the proposed mixer is about -24dBm to -26 dBm. Fig. 3.5.7 shows the input 3rd order intercept point (IIP3) of -11.5 dBm at 6072 MHz. Finally, Fig. 3.5.8 shows the isolation with frequency between RF and LO port.

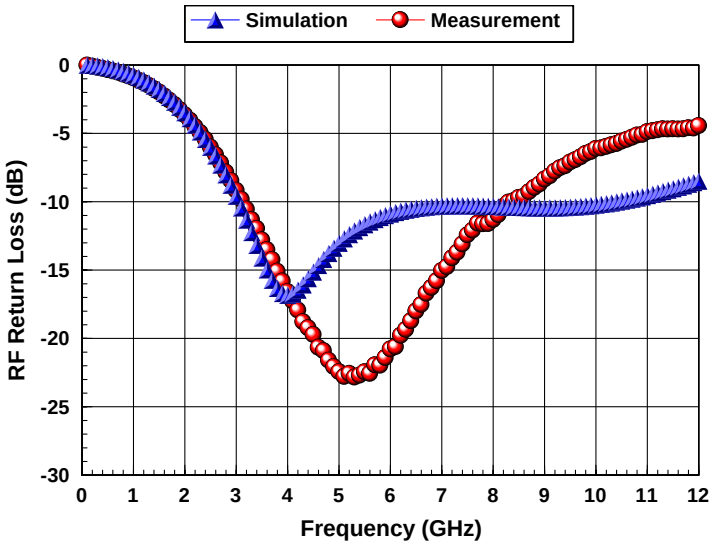


Fig. 3.5.1 RF port input return loss

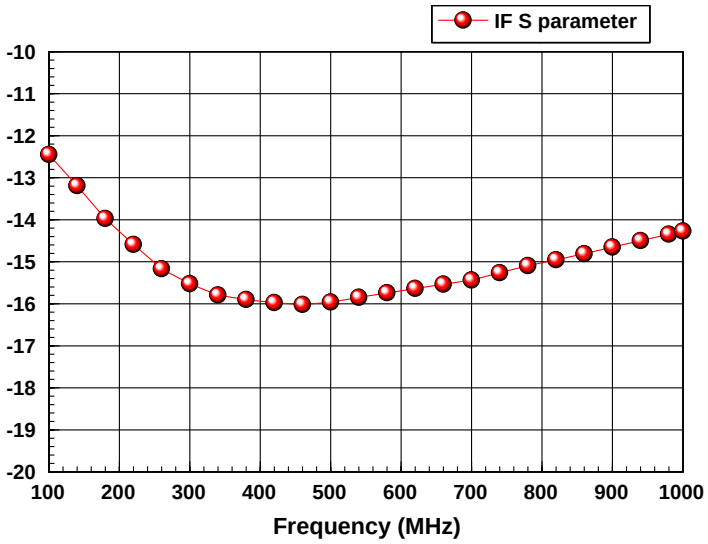


Fig. 3.5.2 IF port input return loss

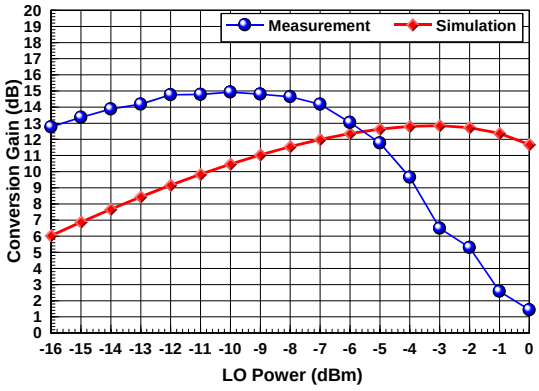


Fig 3.5.3 (A) 3432 MHz

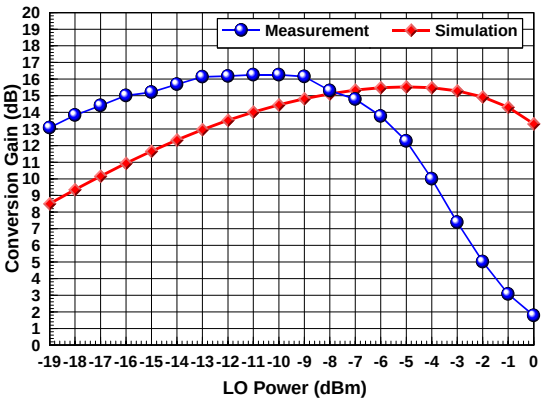


Fig 3.5.3 (B) 3960 MHz

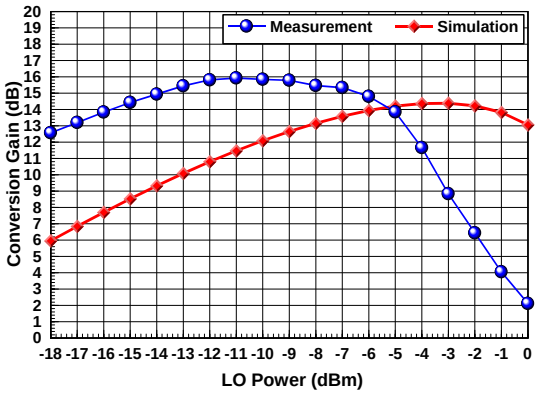


Fig 3.5.3 (C) 4488 MHz

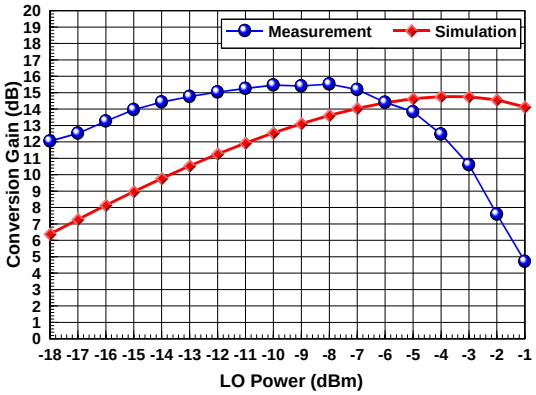


Fig 3.5.3 (D) 5544 MHz

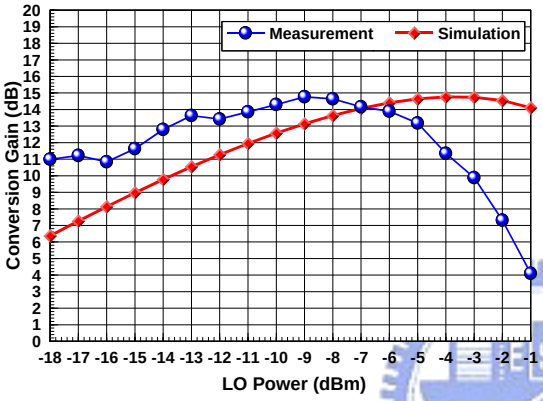


Fig 3.5.3 (E) 6072 MHz

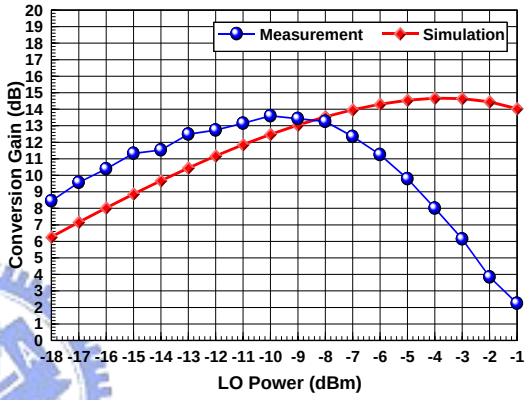


Fig 3.5.3 (F) 6600 MHz

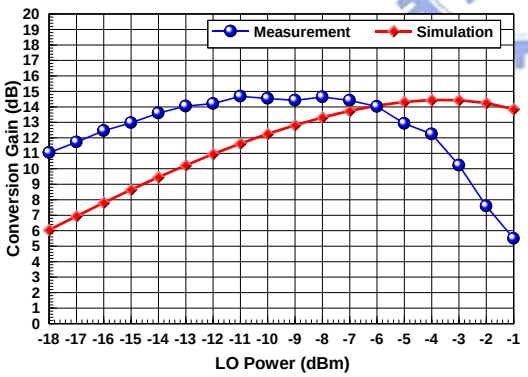


Fig 3.5.3 (G) 7128 MHz

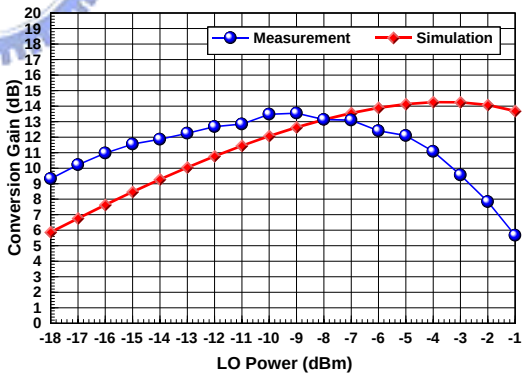


Fig 3.5.3 (H) 7656 MHz

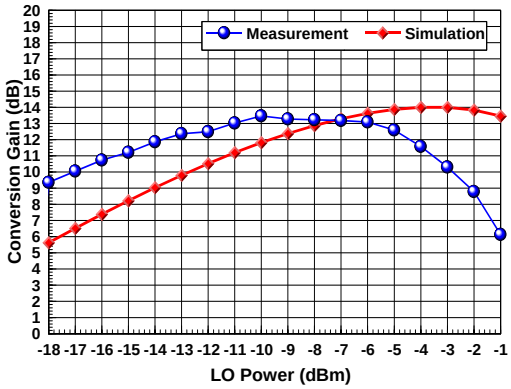


Fig 3.5.3 (I) 8184 MHz

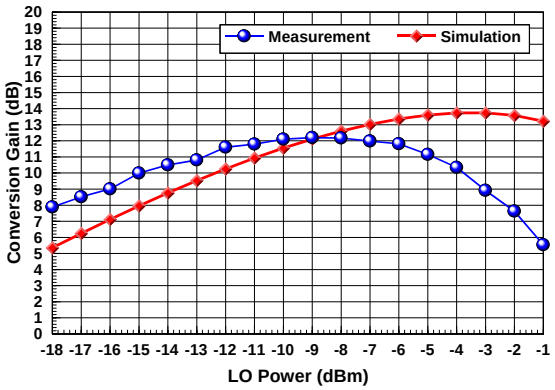


Fig 3.5.3 (J) 8712 MHz

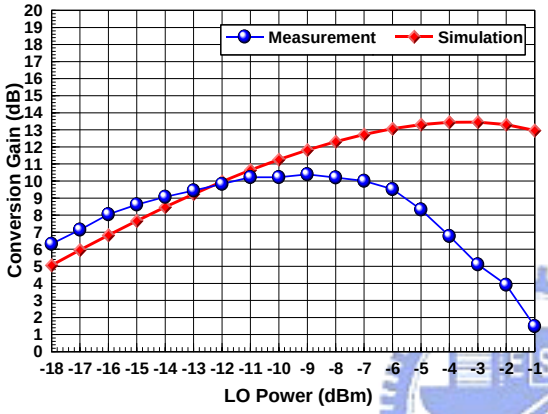


Fig 3.5.3 (K) 9240 MHz

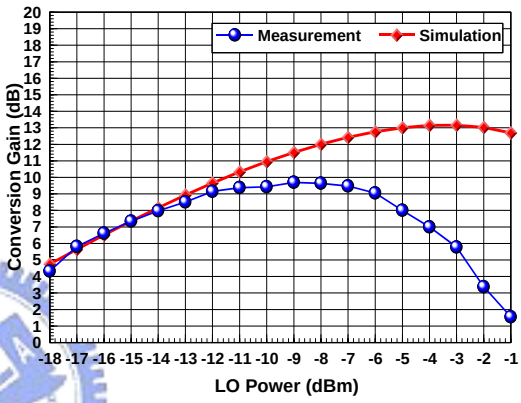


Fig 3.5.3 (L) 9768 MHz

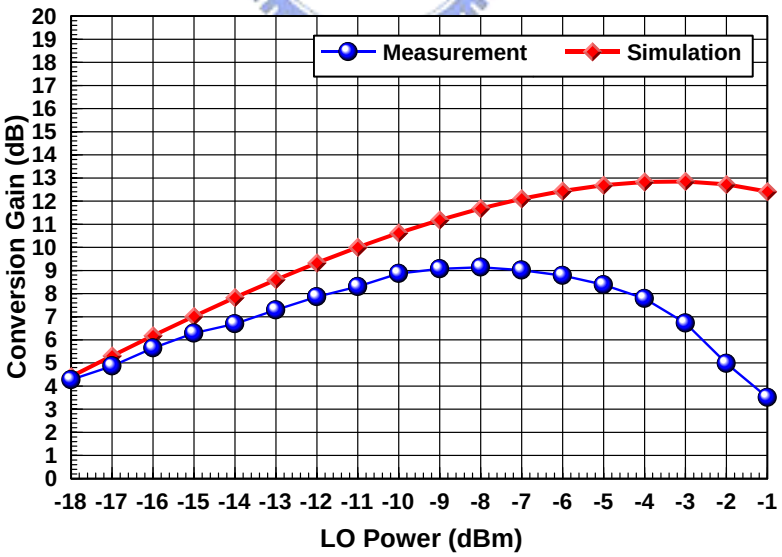


Fig 3.5.3 (M) 10296 MHz

Fig. 3.5.3 (A)~(M) Conversion Power Gain with Lo Power Sweeping

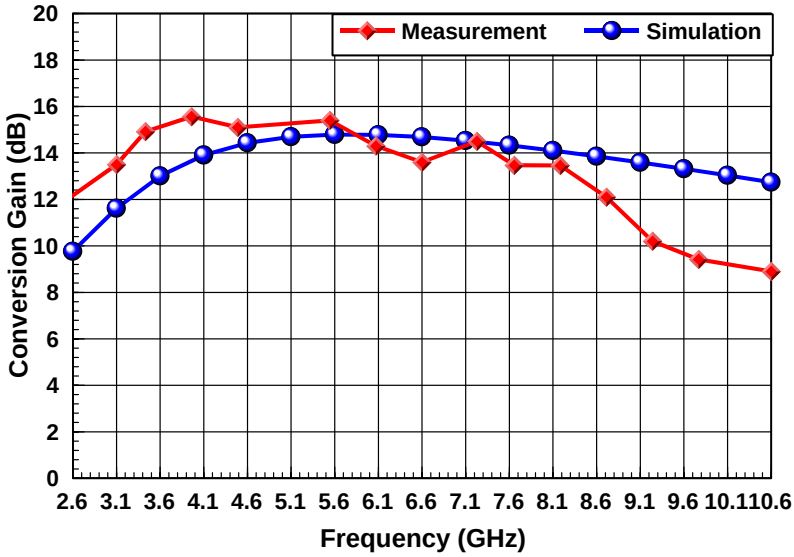


Fig. 3.5.4 Conversion Power Gain with Frequency

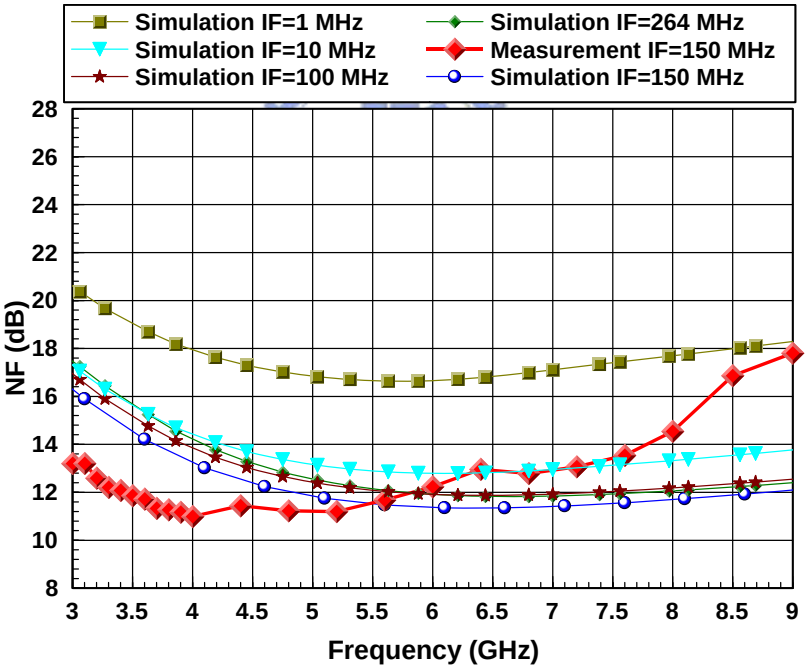


Fig. 3.5.5 DSB Noise Figure with Frequency

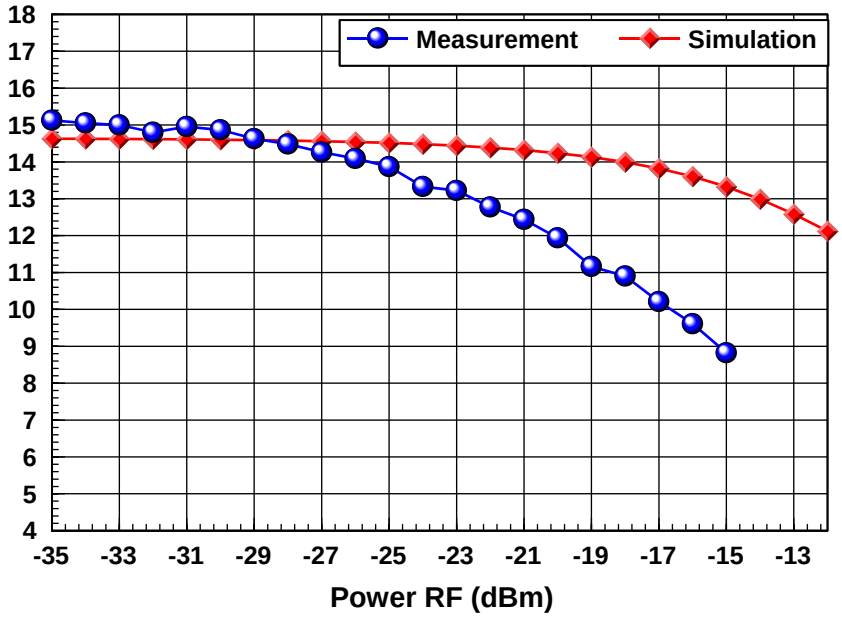


Fig. 3.5.6 (A) P1dB at 5016 MHz (-26)

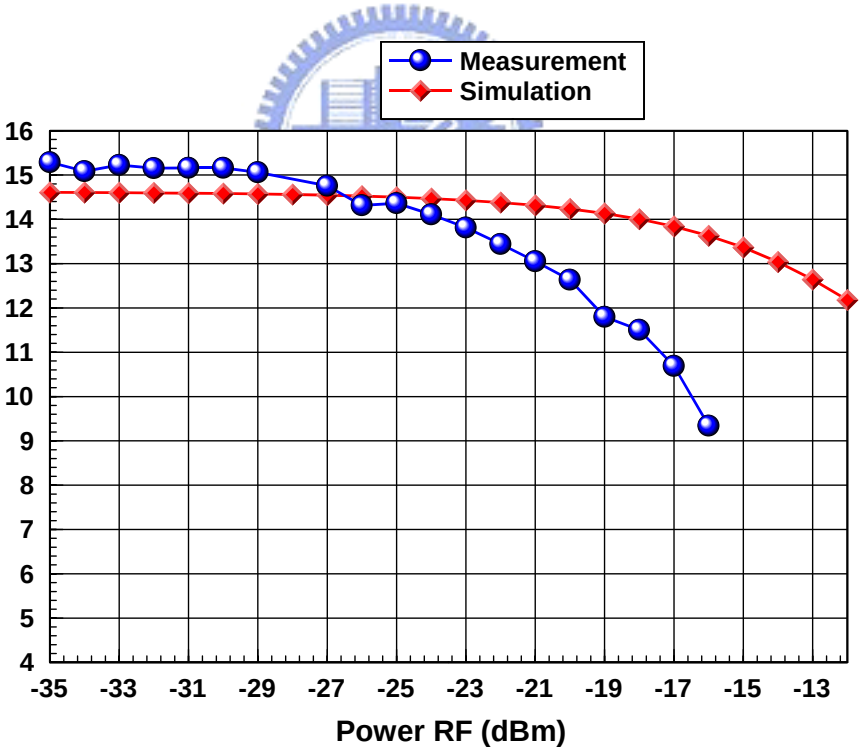


Fig. 3.5.6 (B) P1dB at 6600 MHz (-24)

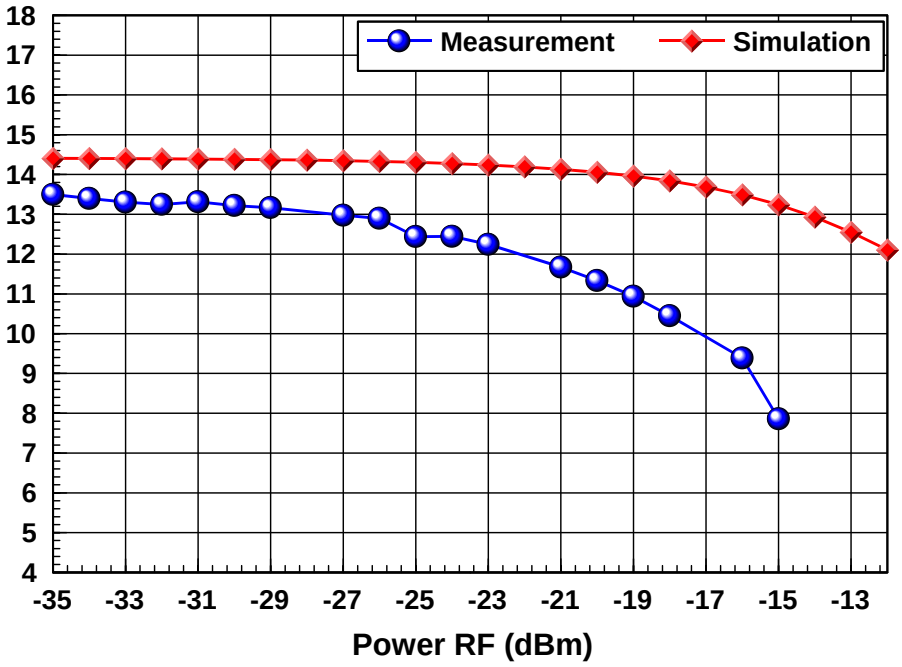


Fig. 3.5.6 (C) P1dB at 7128 MHz (-24)

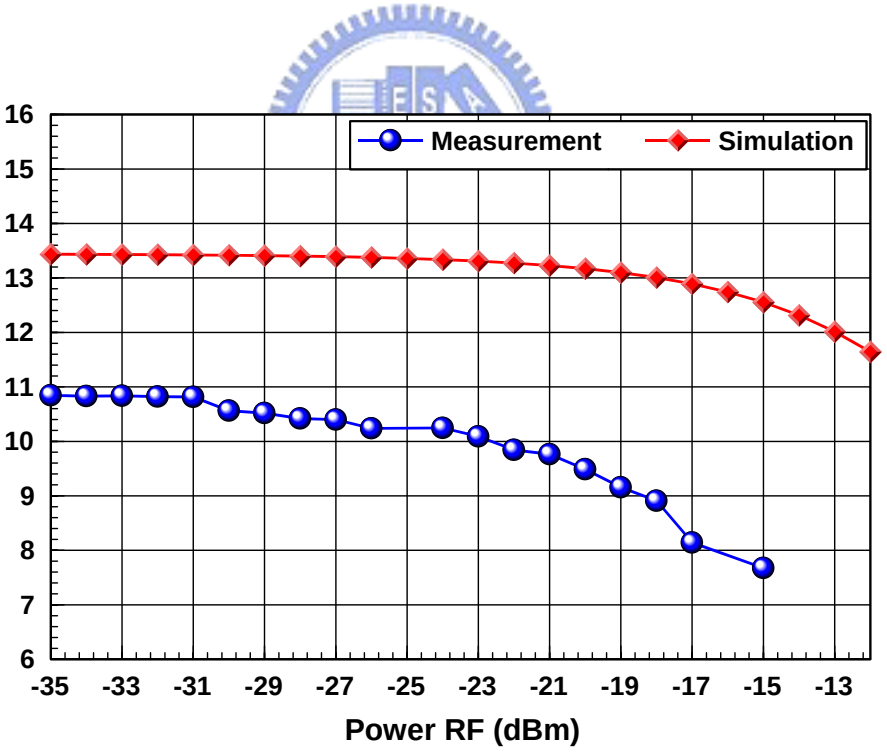


Fig. 3.5.6 (D) P1dB at 9240 MHz (-21)

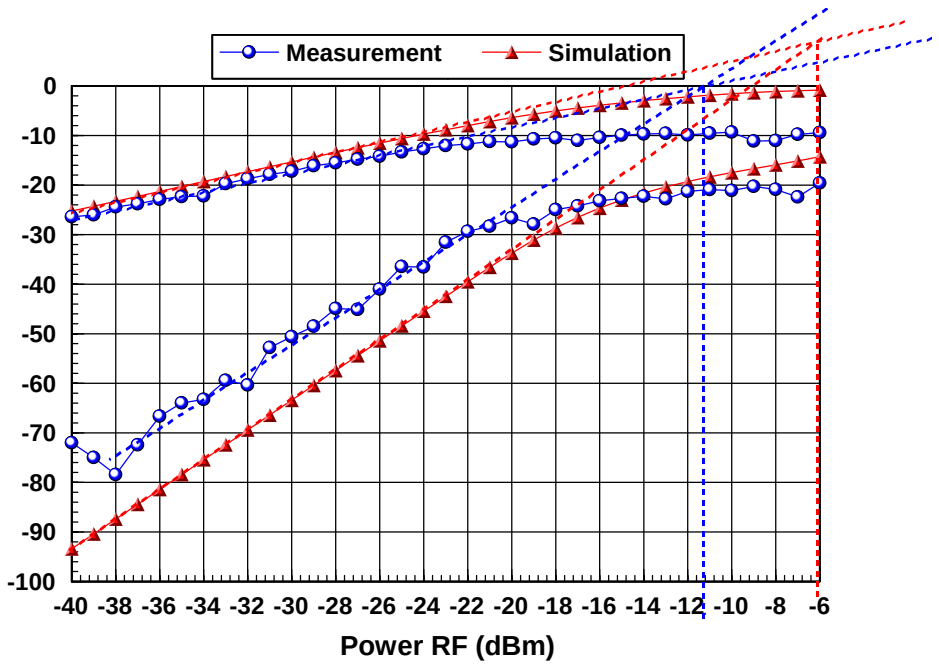


Fig. 3.5.7 (A) IIP3 at 6072 MHz

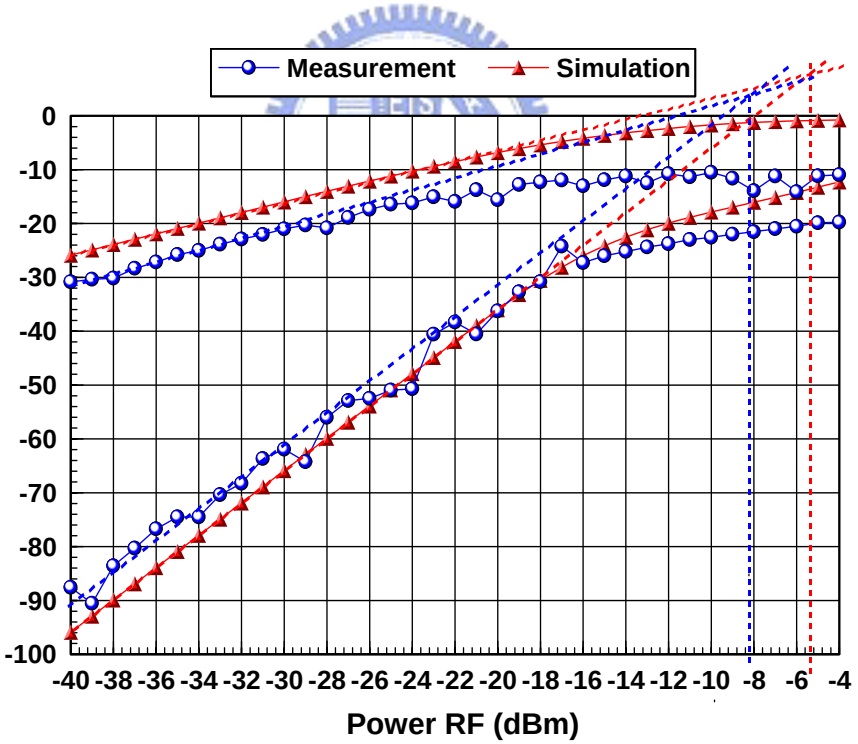


Fig. 3.5.7 (B) IIP3 at 8014 MHz

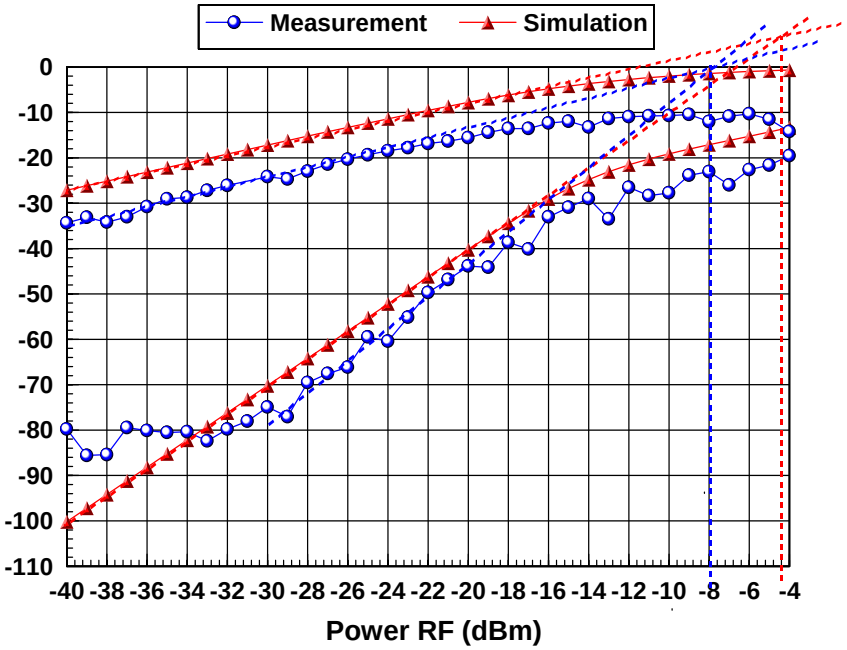


Fig. 3.5.7 (C) IIP3 at 10296 MHz

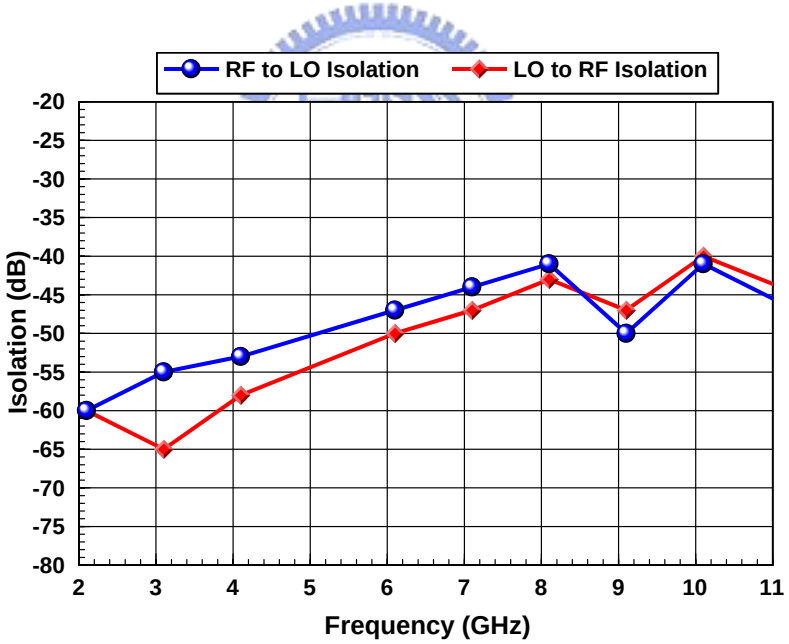


Fig. 3.5.8 Isolation with Frequency

3.5.2 Comparisons

The comparisons of the simulated and measured results are in Table 3.5.1. Because

the RF port input return loss is not having good matching to 50 ohm in high frequency, the conversion power gain degenerates about 3 dB at 10.6 GHz. The measured linearity performances are worse than simulation, because that the voltage of trans-conductance MOS's drain port is variation. The measured noise figure is worse to the simulation in high frequency owing to the degeneration of the conversion power gain in high frequency. Table 3.5.1 and Table 3.5.2 show the comparisons of this work and other recently ultra wide-band mixer paper. This work reveals highly conversion power gain comparing with other work.

Table 3.5.1 Comparison of Simulated and Measured Results

Reference / Specification	This Work Sim.	This Work . Meas.
Process	CMOS 0.18um	CMOS 0.18um
Band Width	3.1-10.6	3.1-8
Supply Voltage(V)	1.5	1.5
RF Return Loss	<-10	<-10
IF Return Loss	<-10	<-10
LO Power (dBm)	-3	-10
Conversion Power Gain	11.6~14.7	13.5-15.5
LO to RF Isolation	N/A	-40
DSB NF	11.35~15.9	11~14.5
P1db at 6.6 GHz	-16	-24
IIP3 at 6GHz	-4.25	-11.5
Core Circuit (mW)	10.95	11.25
Buffer (mW)	10.5	10.65

Table 3.5.2 Comparison of Ultra Wide-band Mixer

Ref.	Process	BW (GHz)	VDD (V)	CG (dB)	NF (dB)	IIP3 (dBm)	Core Mixer Power (mW)
This Work (Meas.)	0.18um CMOS	3.1-8.1	1.5	13.5-15.5	11-14.5	-11.5#	11.25
[20] 2007 MO (Meas.)	0.35um SiGe	3-5	3	5	N/A	N/A	7.5
[9] 2005 VLSI (Meas.)	0.18um CMOS	3.1-8.7	1.8	2.5-5	6.8-7.3	5	10.4
[21] 2005 MO (Meas.)	0.25um CMOS	3.1-5.1	1.5	-9.8~-10.4	10.2-11.7	6	6
[10] 2004 MWCL (Meas.)	0.18um CMOS	0.3-25	5	9.5-12.5	N/A	N/A	71
[22] 2007 MO (Meas.)	0.18um CMOS	3.1~10.6	1.8	-1.4~10.1*	8.8~17.6	-6.2	13.24

at 6 GHz *IF=264 MHz

Chapter 4

Conclusion and Future Work

4.1 Conclusion

This thesis contains three works: low voltage, low-noise ultra wide-band amplifier, the capacitor feedback ultra wide-band amplifier and folded current reused UWB mixer. All of the simulated results are finished through ADS and Momentum simulator. These three circuits are fabricated in TSMC 0.18 um CMOS process. In this thesis, we have presented the design concepts and simulation versus measurement results.

4.1.1 Low voltage Ultra Wide-band LNA

The low-voltage, UWB LNA topology is fabricated and analyzed in chapter 2, including input matching, noise figure, and power gain. By way of folded cascode structure and shunt peaking method, it achieves high isolation, low voltage, and wideband performances. The measured power gain is 7.5dB from 3.1 to 7.5 GHz. The input return loss is less than -10 dB from 3.1GHz to 10.6GHz, except the point which produces peak value. The fabricated inductor value of TL (common source degeneration inductor) is not expected as simulated inductor value of TL, it causes the circuit is seemly unstable at 3-4 GHz. The measured noise figure is 4.8-7.5 from 3.1 to 7.5 GHz. The measured P_{1dB} are -14dBm at 5.1 GHz, and -10dBm at 7.5 GHz. The measured results show the LNA achieves wideband performance at 0.75V supply voltage, and the total power consumption of the proposed LNA is only 11.3 mW.

4.1.2 3-8 GHz capacitor feedback Wide-band LNA

The proposed 3-8 GHz wideband LNA uses cascode stage with shunt peaking method to achieve wideband power gain. By way of transistor's intrinsic capacitor Cgd and only one inductor as input matching network, wideband input matching can be achieved. The measured results reveal that S11 is better than -10 dB from 2.7 GHz to 12.1 GHz. The fabricated wideband LNA achieves flat power gain (S21) of about 10dB and the 3 dB bandwidth is from 1.8 GHz to 8.3 GHz. The measured noise figure is 3.7-5.5dB from 3 GHz to 7.5 GHz. The matching mechanism of the proposed wide-band LNA can simply the matching network and reduce noise figure of the amplifier efficaciously.

4.1.3 Folded Current Reuse Ultra Wide-band Mixer

The Folded Current Reused Ultra wide-band Mixer has been designed and presented in this thesis. The proposed UWB mixer replaces the traditional common source trans-conductance stage with a folded current-reused pair. It not only reduces the supply voltage, but also increases trans-conductance effectively. Such folded current-reused structure can use DC current effectively because that the main current flows through trans-conductance stage. All measurements were finished through on-wafer testing. With the 1.5 V supply voltage, the UWB mixer excites 13.5-15.5 dB of power gain from 3-8 GHz with -10 dBm of LO power and 11.25 mW of power consumption in core circuit. The measured noise figure is 11-14.5 dB with IF=150 MHz and IIP3 is -11.5 dBm at 6 GHz. The measured linearity performances are not as expected, because that the voltage of trans-conductance MOS's drain port is variation. The measured results show that the folded current reused mixer exhibits a low power and high conversion power gain than the conventional Gilbert type mixer architecture.

4.2 Future Work

In this thesis, we have finished the design and measurement of UWB LNA and UWB mixer. In ultra wide-band receiver architecture, there are many important blocks needed to be implemented: Synthesizer, AGC, and A/D converter. There are some other future works needed to be implemented. First, the on-chip bias circuit should be designed to reduce the large number of DC pads. Second, the ESD protection must be designed within the thinner gate oxide process. Finally, the EM EDA tool must be used accurately and all parasitic effects including parasitic capacitance, resistance and inductance must be considered carefully.

The proposed 3-8 GHz capacitor feedback low noise amplifier may be improved as low power ultra wide-band LNA to fit UWB communication system well. And the folded current reuse mixer may be improved for its linearity to increase the total linearity of the receiver.

Appendix

A RF Receiver Front-End for UWB Wireless System

In this addendum, we demonstrate a 3-8 GHz RF receiver front-end for Ultra wide-band system. We also review the traditional receiver architecture and Multi-band orthogonal frequency division multiplexing (MBOA) receiver.

A.1 Traditional Receiver and MBOA Receiver Front End

The goal of radio receiver is to detect a signal from the electromagnetic spectrum. In this section, we will introduce heterodyne, low-IF, zero-IF, and MB-OFDM Ultra wide-band receiver architecture.

Super Heterodyne Receiver

Figure A.1.1 shows super heterodyne receiver architecture. Super heterodyne receiver down-converters the RF input signal to an intermediate frequency (IF) by two steps through image rejection filter, if filter and mixer. It can solve the trade-off between selectivity and sensitivity. The drawback of super heterodyne receiver architecture is that it requires many components. It is difficult to be integrated into a single chip because the on chip filter would occupy large areas.

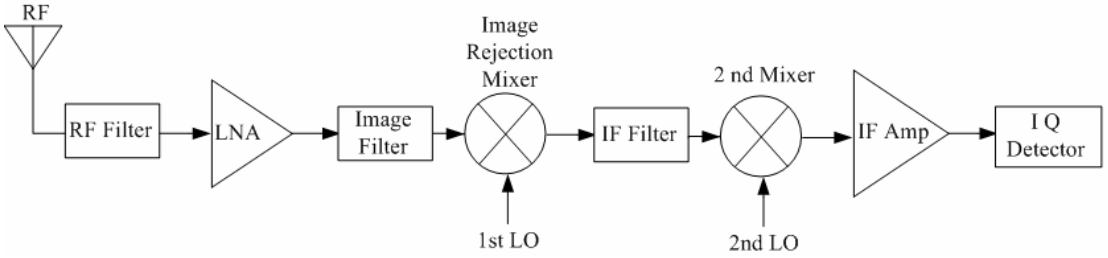


Fig.A.1.1 Super heterodyne receiver architecture

Zero-IF Receiver

Figure A.1.2 shows zero-IF receiver architecture. Zero-IF architecture is also called "homodyne", "direct-conversion". In zero-IF receiver, where the LO signal frequency is equal to the RF input frequency and the LO signal will translate the center of the desired signal to 0 Hz. It has two chief advantages of homodyne receiver. First, the problem of image is solved because of zero-IF. Second, because of simple architecture, it is easy integrated. But the chief drawbacks of zero-IF receiver are I/Q mismatch and "DC offset" as shown in Figure A.1.3. The problem of DC offset can be solved by using even-harmonic mixer [19].

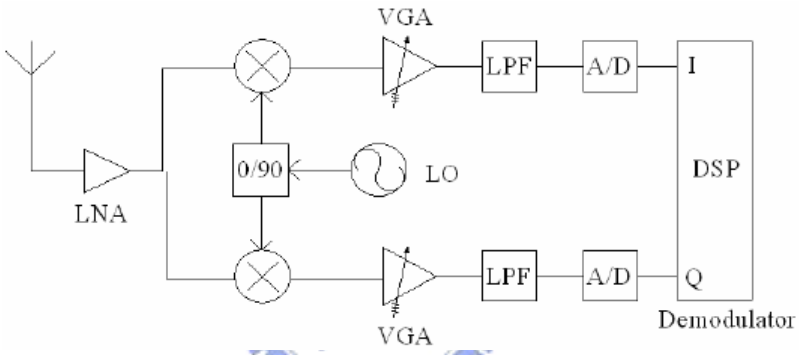
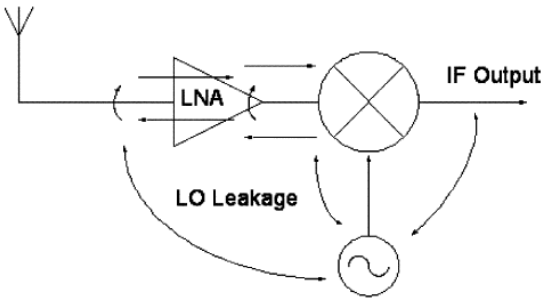
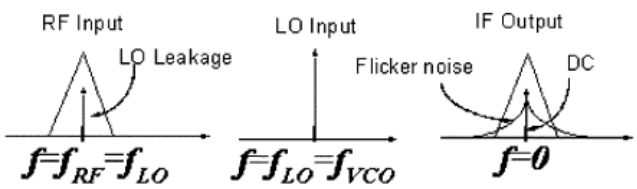


Fig A.1.2 Zero-IF receiver architecture



(a)



(b)

Fig A.1.3 (a)(b) Mechanism of direct conversion receiver with self-mixing

Low-IF Receiver

Low-IF receiver converts the RF signal to low IF signal. Low-IF receiver has great interest because of its higher level of integration. Comparing with the Zero-IF receiver, the drawbacks such as dc offset and LO self-mixing is not occurred in Low-IF receiver. The problem of image can be solved by using image reject architecture (Hartley, Weaver) as shown in Figure A.1.4.

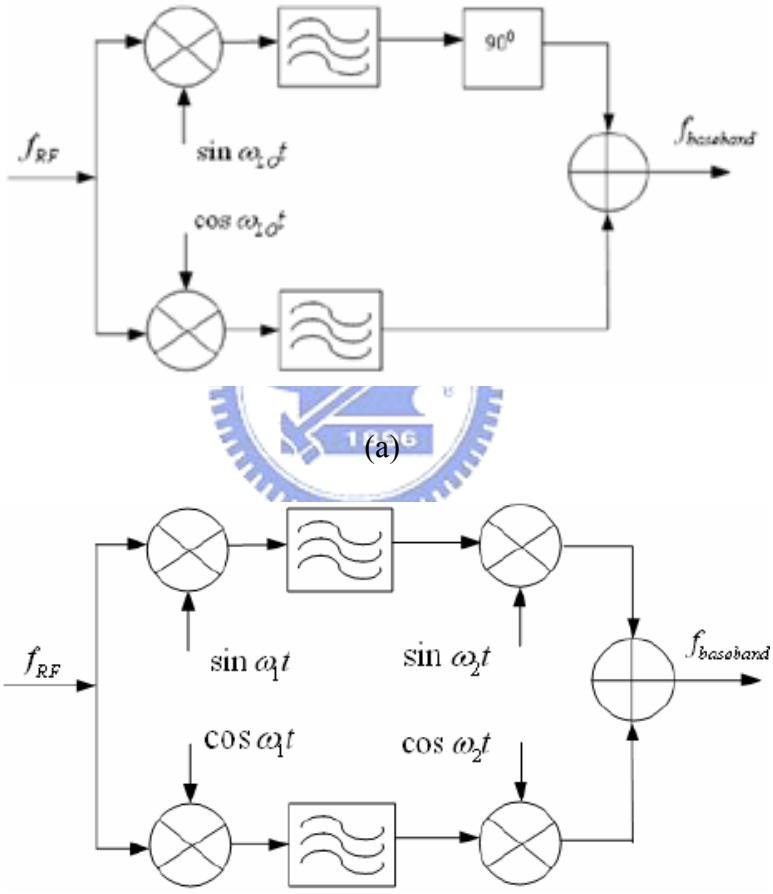


Fig A.1.4 Low-IF receiver architecture (a) Hartley (b) Weaver

MB-OFDM Ultra wide-band receiver

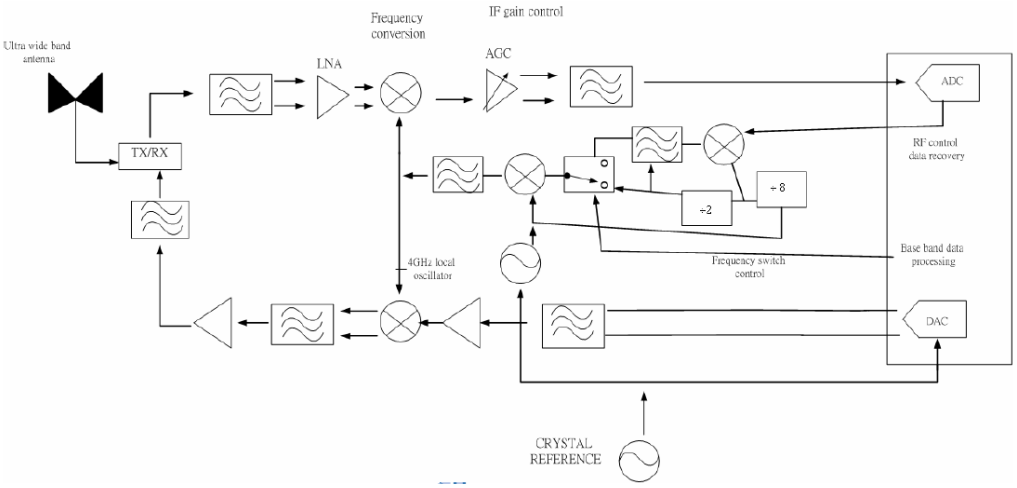


Fig A.1.5 MB-OFDM Ultra wide-band receiver architecture

Figure A.1.5 shows receiver architecture for MB-OFDM UWB system. For architectural point, the MB-OFDM receiver is similar to WLAN receiver. The chief difference is in local oscillator and the bandwidth of base-band signal.

Because MB-OFDM UWB system cover 14 bands through entire spectrum, tradition signal generator can't produce so wide bandwidth. The frequency synthesizers used in UWB system are usually designed with high frequency voltage-controlled oscillator (VCO), multi-stage dividers, and SSB mixer in order to produce multi-band LO signals. For mode 1 is shown in Figure A.1.6.

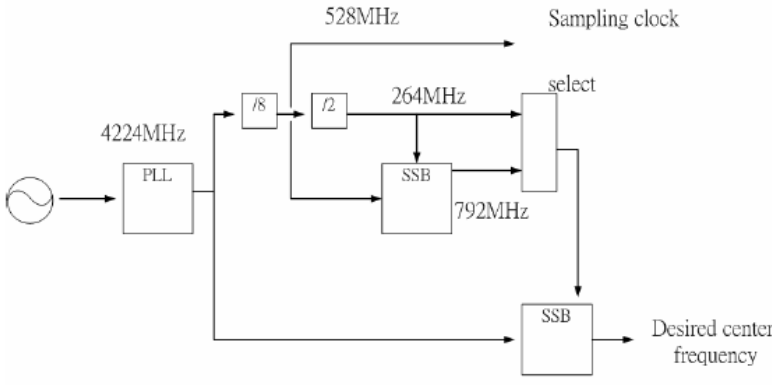


Fig A.1.6 MB-OFDM Mode1 signal generator architecture

By 4224 MHz phase lock loop combined with divided by eight and two circuit, 264 MHz and 792MHz can be produced. Make use of 4224 MHz, 264 MHz, 792MHz, and

SSB mixer. We can get three center frequencies of mode 1 (3432 MHz, 3960 MHz, and 4488 MHz).

A.2 Main Block Description

Figure A.2.1 shows a 3-8 GHz ultra wide-band front-end. The low noise amplifier is the first stage of the front-end circuit. The first stage must provide sufficient power gain through entire bandwidth to suppress the noise of next stage.

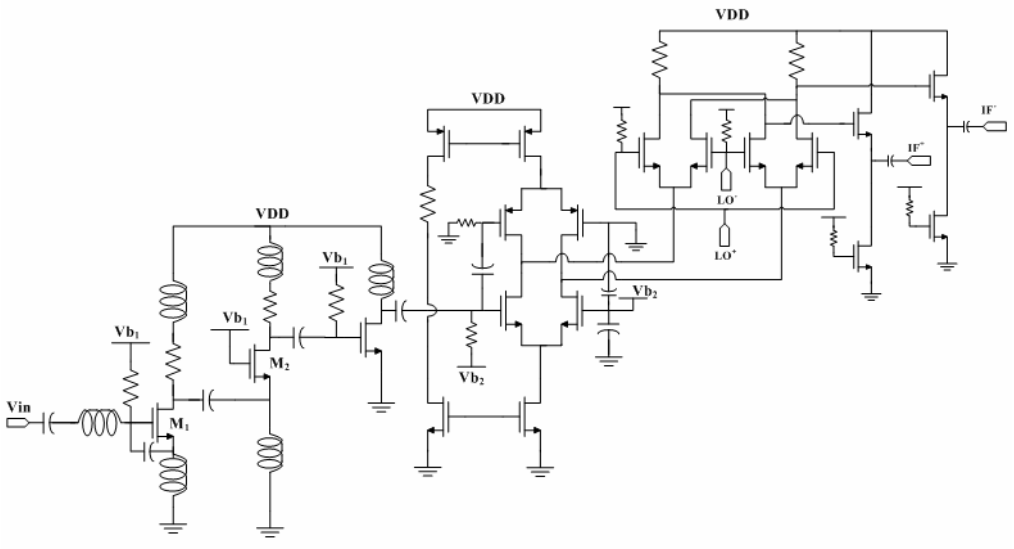


Fig A.2.1 The proposed 3-8 GHz front-end circuit

A.2.1 LNA

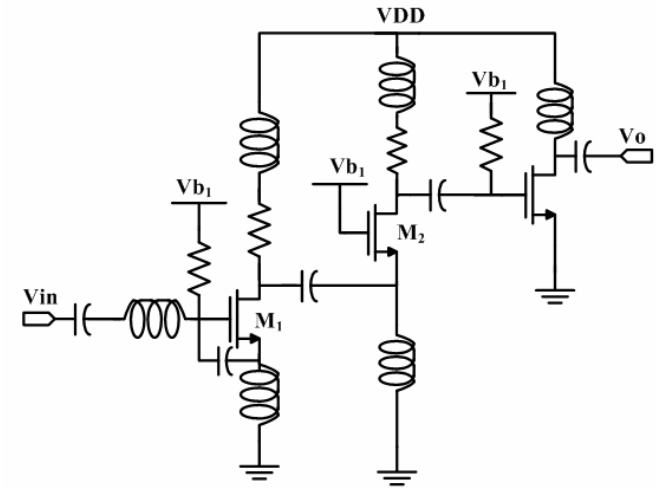


Fig A.2.2 The schematic of low noise amplifier

Figure A.2.2 shows the schematic of the proposed wide-band LNA circuit composed of common source stage and common gate stage with shunt-peaking method. L1 and L2 are RF chock inductor. In small signal mode, the LNA is cascaded by cascode stage and common source stage. By way of transistor's intrinsic capacitor Cgd and only one inductor (Lg) as input matching network, wideband input matching can be achieved. This matching mechanism can simplify the matching network effectively. The main principle of the LNA is introduced in chapter2.

A.2.2 Mixer

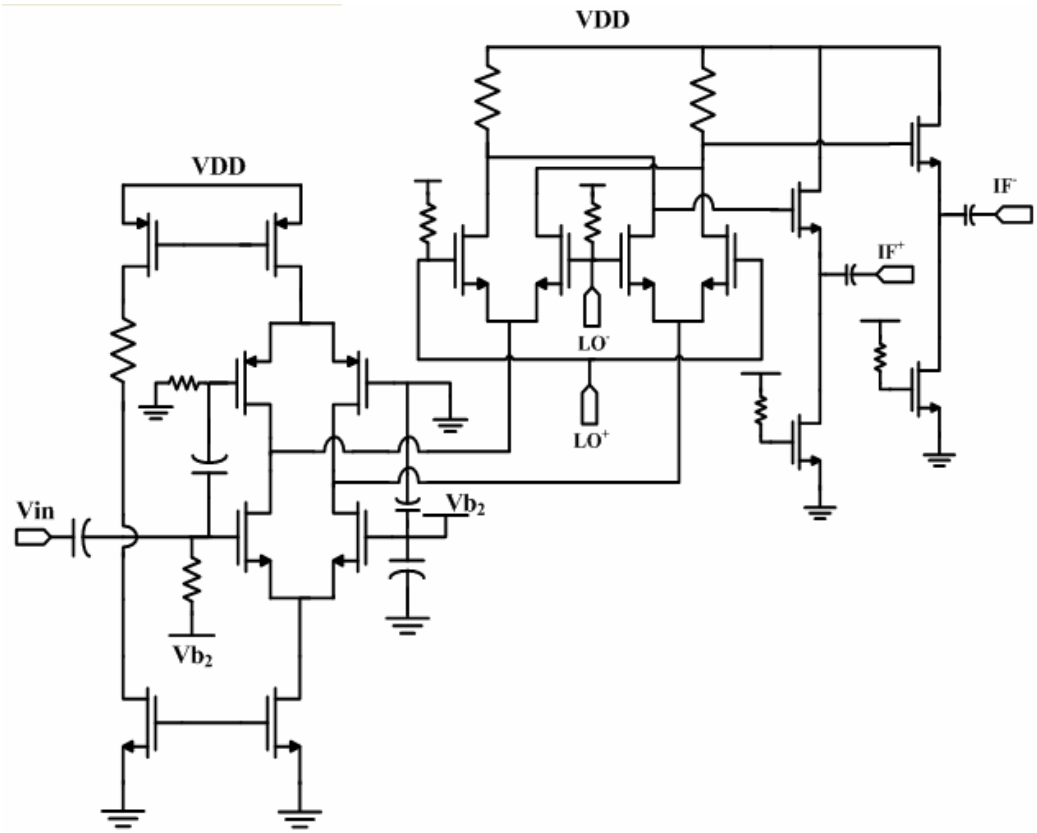


Fig A.2.3 The schematic of down converter mixer

A Gilbert cell like mixer, shown in Fig A.2.3, follows the LNA directly on-chip. It translates the input signal from RF to a 0-256 MHz intermediate frequency. The mixer is AC coupled by the LNA output. A single-ended-to-differential converter is merged at

mixer. In a classical Gilbert cell, only the NMOS input trans-conductor is used. This stage is designed trading between trans-conductance gain, noise, linearity, and current consumption. In this design, a PMOS trans-conductor shunts the NMOS, as shown in the figure. This allows us to save current consumption, for given gain. In the case of the double balance mixer, the AC-coupled CMOS inverter is used as the trans-conductor. The lowest supply voltage of the mixer can be derived as below:

$$V_{dd,\min} = V_{ov1} + V_{ov2} + 2V_t + V_{rfdcp} - V_{rfdcp} + V_{ov3} + V_{ov4}$$

We can choose adaptable V_{rfdcp} and V_{rfdcp} to increase headroom voltage efficaciously. And $G_m=(g_{mn}+g_{mp})$ value is increased efficaciously. The biasing currents of PMOS and NMOS devices are slightly different in order to bias the switching stage and the output load. In order to achieve wide-bandwidth (264 MHz) at IF port, resistive load is used at load stage.

A.3 Layout and Simulation Results

A.3.1 Layout Consideration

Figure A.3.1 is the layout of the proposed Ultra wideband front-end circuit. The proposed circuit is designed for on-wafer measurement with three DC bound wires. It follows the rules of CIC's (Chip Implementation Center's) probe station testing rules. Figure A.3.2 shows the on-wafer measurement setup with four probes and three bound wires. In layout consideration, we add many by-pass capacitors to prevent oscillation in low frequency and to increase the degree of perfect ac ground. Total die area including pads is 1.16 mm^2.

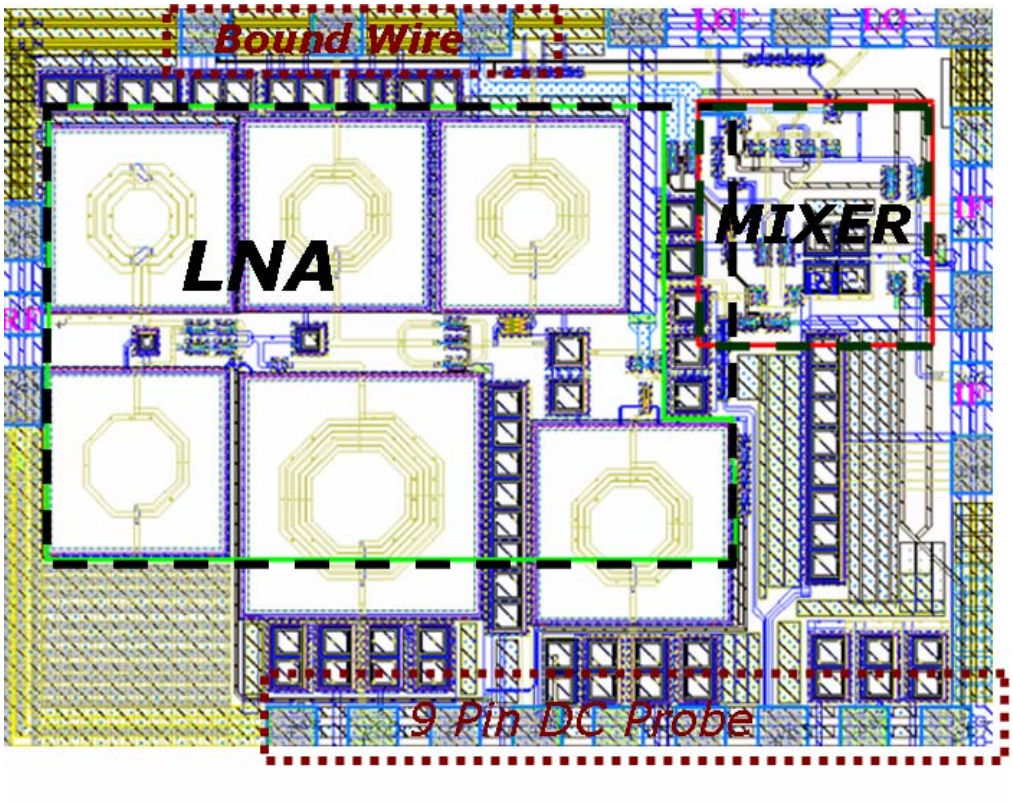


Fig A.3.1 The layout of the front-end circuit

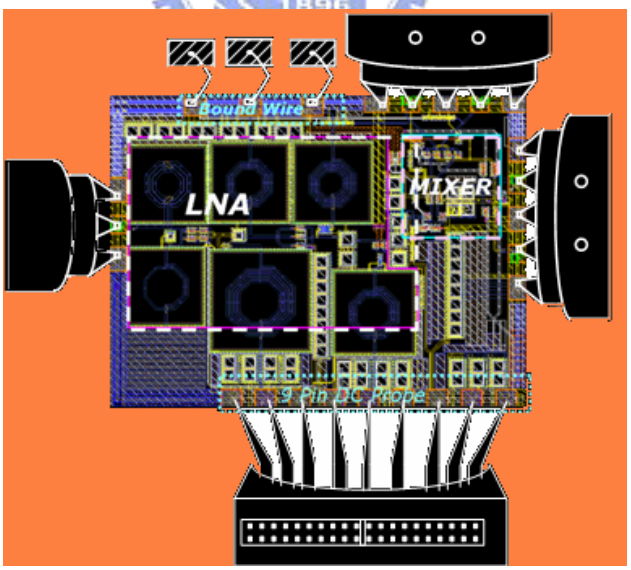


Fig A.3.2 The measurement setup of the front-end circuit

A.3.2 Simulation Results

Input impedance matching is characterized in Fig. A.3.3, which reveals the simulated

input return loss of better than -10 dB is attained over the 3-8 GHz. Fig A.3.4 shows the simulated power gain over the group1~3 of ultra wide-band receiver front-end achieves a power gain of 19-21.5 dB. The simulated method of conversion power gain adopts to fix LO frequency at center frequency and to sweep RF frequency from low band frequency to high band frequency. Fig A.3.5 shows the simulated noise figure of the circuit, which achieves noise figure of 4.3-6.2 dB from 3.1 to 8 GHz with IF=100 MHz. Fig A.3.6 shows the input 1-dB compression point of the circuit, which is from -25.5 to -27.5 dBm. A two-tone test for the in-band third-order intercept point (IIP3) by sweeping the input power level was simulated at 3.1 GHz, 5.1 GHz and 8.1 GHz with tone spacing of 1 MHz. The output levels of the fundamental tone and the third-order intermodulation distortion are shown in Fig A.3.7 (a)-(c). An input IP3 (IIP3) of -15~-17.5 dBm is extrapolated. The supply voltage is 1.5 V and measured core current consumption is 13.1 mA. The performance of the RF front-end is finally summarized in Table A.1. Table A.2 lists the comparison of the recently ultra wide-band front-end circuit with this work.

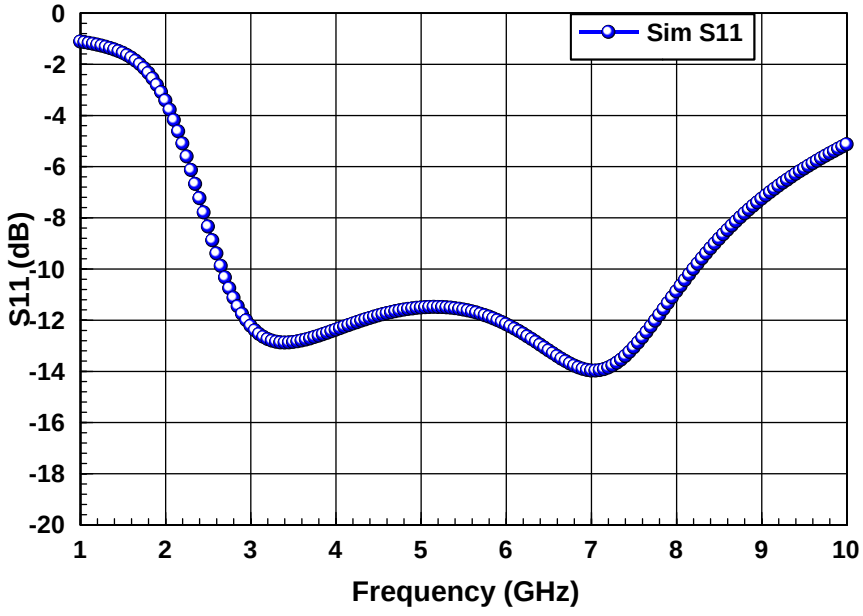


Fig A.3.3 Simulated S11 of the front-end circuit

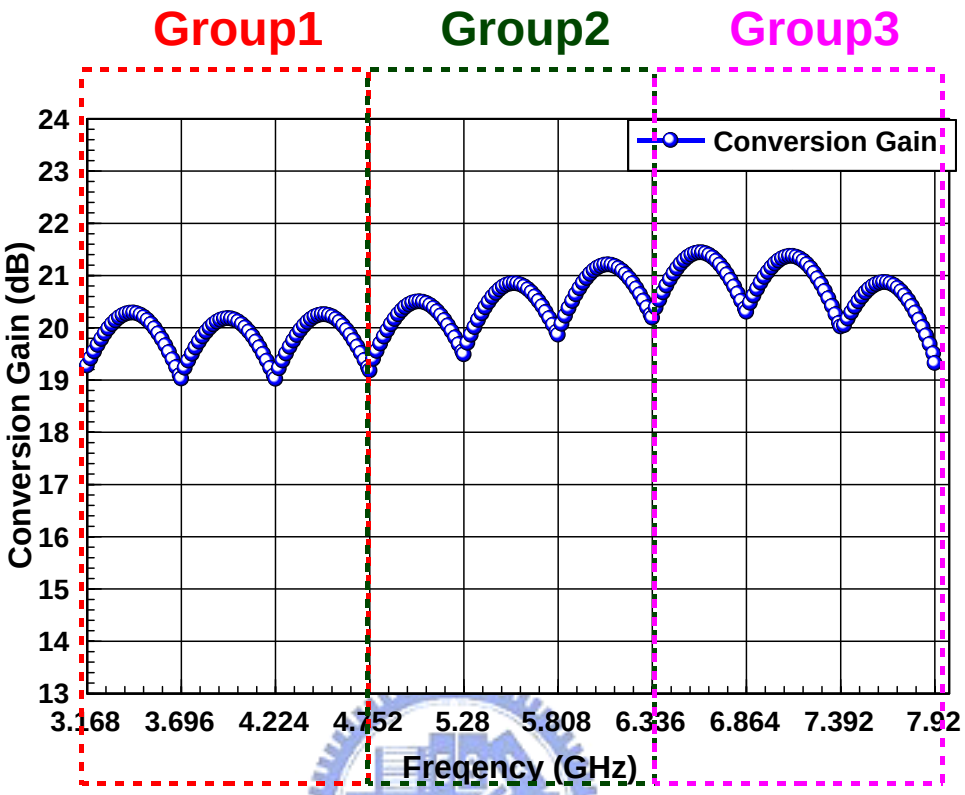


Fig A.3.4 The simulated conversion power gain of the front-end circuit

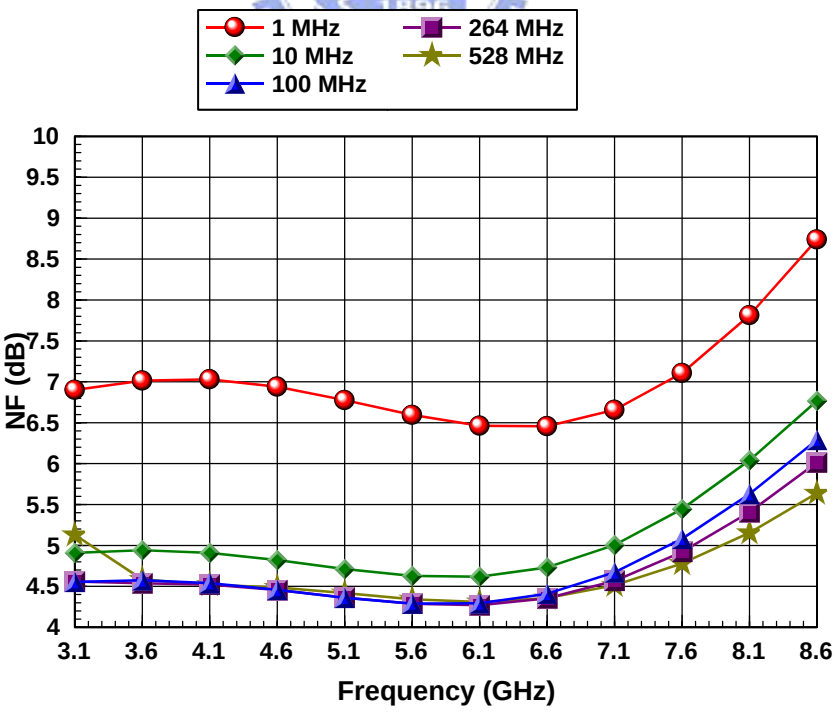


Fig A.3.5 The simulated noise figure of the front-end circuit

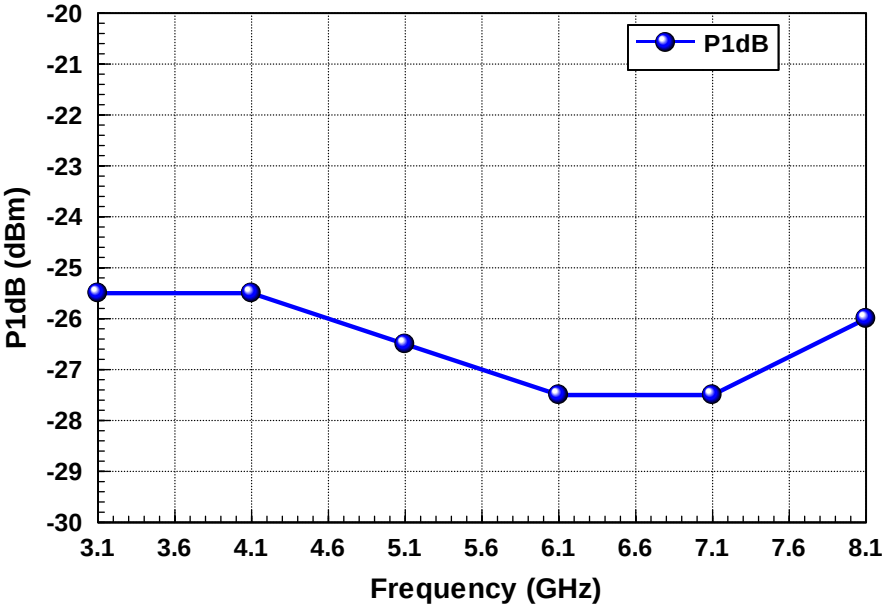
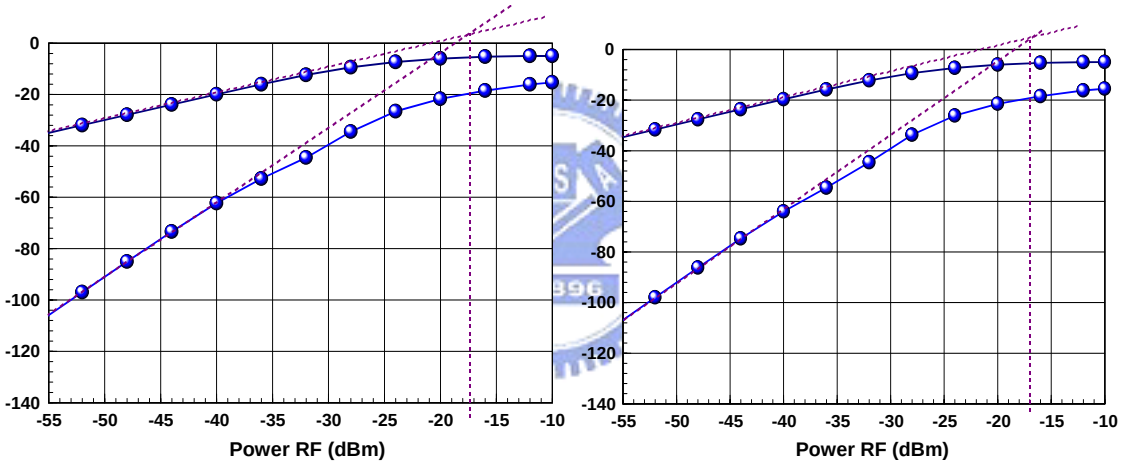
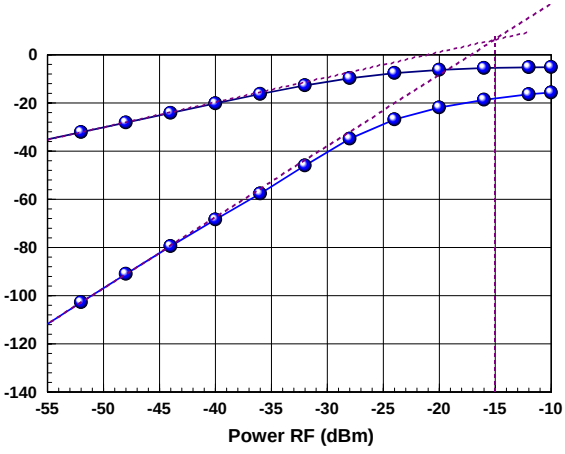


Fig A.3.6 The P1dB of the front-end circuit



(a) IIP3 at 3.1 GHz (b) IIP3 at 5.1 GHz



(c) IIP3 at 8.1 GHz

Fig A.3.7 Third-order intercept point of the circuit

Table A.1 Simulated performance of the UWB receiver front-end

Reference / Specification	This Work . Sim.
Process	CMOS 0.18um
Band Width	3.1-8.1
Supply Voltage(V)	1.5
RF Return Loss	<-10
LO Power (dBm)	-5
Conversion Power Gain	19-21.5
DSB NF	4.3-6.2
P1db at 6.6 GHz	-25.5~-27.5
IIP3 at 6GHz	-15~-17.5
Core Circuit (mW)	19.25
Buffer (mW)	12.24

Table A.2 Comparison of recently UWB front-end circuit

Ref.	Process	BW (GHz)	VDD (V)	CG (dB)	NF (dB)	IIP3 (dBm)	Total Power (mW)
This Work (Sim.)	0.18um CMOS	3.1-8	1.5	19-21.5	4.3-6.2	-17#	Core: 19.25 Buffer: 12.24
[23] 2006 (Meas.)	0.18um CMOS	3-5	1.8	10	N/A	-13	46.8
[24] 2006 (Sim.)	0.13um CMOS	3.1-10.6	1.5	22.9~26.4	4.8-7.7	-11.3	57.6
[25] 2005 (Meas.)	0.25um SiGe	3.1-10.6	2.7	20.6~21.8	4.1-6.2	-12.8	83

at 5 GHz

Reference

[1]IEEE 802.15 WPAN High Rate Alternative PHY Task Group 3a (TG3a). http//www.ieee802.org/15/pub/TG3a.html.

[2] *DS-UWB Physical Layer Submission to 802.15 Task Group 3a*,[Online]. Available: ftp://ftp.802wirelessworld.com/15/04/15-04-0137-03-003a-merger2-proposal-ds-uwb-update.doc, available at

[3]*Multi-Band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a*, [Online]. Available: ftp://ftp.802wirelessworld.com/15/ Archive/2003/Jul03/03268r3P802-15 TG3a-Multi-Band-CFP-Document. doc, available at

[4]Kuan-Hung Chen and Chorng-Kuang Wang, "A 3.1~10.6 GHz CMOS Cascaded Two-stage Distributed Amplifier for Ultra-Wideband Application," *IEEE Asia-Pacific Conference* on 4-5 Aug. 2004 Page(s):296 – 299.

[5]R.-C. Liu, K.-L. Deng, and H. Wang, "A 0.6-22 GHz broadband CMOS distributed amplifier," in *IEEE Radio Frequency Integrated Circuits Symp*. Dig. Papers, 2002, pp. 103-106

[6]Po-Yang Chang, "Low-voltage, Low-power, LNA and Multiband Frequency Synthesizer For UWB Receiver," *Thesis of Master's Degree, Institute of communication engineering, NCTU*, Taiwan, ROC, June 2005.

[7]Po-Yang Chang, "Low-voltage, Low-power, LNA and Multiband Frequency Synthesizer For UWB Receiver," *Thesis of Master's Degree, Institute of communication engineering, NCTU*, Taiwan, ROC, June 2005.

[8]Yang Lu, Kiat Seng Yeo, Alper Cabuk, Jianguo Ma, Manh Anh Do and ZhenghaoLu, "A Novel CMOS Low-Noise Amplifier Design for 3.1-to 10.6-GHz Ultra-Wide-Band Wireless Receivers", *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I:*

REGULAR PAPERS, VOL. 53, NO. 8, AUGUST 2006

[9] A. Safarian, A. Yazdi, and P. Heydari, "Design and Analysis of an Ultra wide-Band Distributed CMOS Mixer", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 13, No. 5, pp. 618-629, May, 2005.

[10] M. Tsai, H. Wang, "A 0.3-25 GHz Ultra-Wideband Mixer using Commercial 0.18um CMOS Technology", IEEE Microwave and Wireless Components Letters, Vol. 14, No. 11, pp. 522-524, November 2004.

[11] Pao-Lin Wu "Low-Power CMOS RF Receiver Front-End With Stacked LNA- Mixer", *Thesis of Master's Degree, Institute of Electro-physics, NCTU*, Taiwan, ROC, June 2003.

[12] Stephen I. Long, Course Notes of Communication Electronics, University of California, Santa Barbara, 2003.

[13] Stephen I. Long , "RFIC MOS Gilbert cell mixer design", Agilent EEsof design seminar.

[14] Chien-Nan Kuo, Course Notes of RF Integrated Circuits, National Chiao Tung University, 2003.

[15] Wei-zen cheng "Design of CMOS front-end circuits for MB-OFDM Ultra-Wideband System ", *Thesis of Master's Degree,* Department of Electrical Engineering *ccu*, Taiwan, ROC, June 2006.

[16]Shuzuo lou and howard c.long, "A WIDEBAND CMOS Variable gain low noise amplifier for acble tv tuners," IEEE ASSCC 2005

[17]Leonard A. MacEachern, Tajinder Manku, "A Charge-Injection Method for Gilbert Cell Biasing," Electrical and Computer Engineering, 1998. IEEE Canadian Conference on

[18] O. *Mitrea,* C. *Popa, A. M. Manolescu, M. Glesner* "A LINEARIZATION TECHNIQUE FOR RADIO FREQUENCY CMOS GILBERT -TYPE MIXERS"

ICECS-2003

[19]Shuenn-Yuh Lee, Ming-Feng Huang, Chung J. Kuo," Even Harmonic Mixer With Current Reuse for Heterodyne/Direct Conversion Receivers" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 52, NO. 9, SEPTEMBER 2005

[20]Song Ruifeng, Liao Huailin, Huang Ru, Wang Yangyuan " Design of a 3-5-GHz ultra wideband BiFET mixer using 0.35-m SiGE BiCMOS technology" Microwave and Optical Technology Letters Volume 49, Issue 4, Date: April

[21] W. L. Chen, G. W. Huang, S. F. Chang " BROADBAND CMOS MIXER CELL FOR UWB APPLICATIONS" Microwave and Optical Technology Letters Volume 49, Issue 1, Date: January 2007, Pages: 127-128

[22] Goo-Young Jung, Jae-Hoon Shin, Tae-Yeoul Yun " low-noise UWB CMOS mixer using current bleeding and resonant inductor techniques" Microwave and Optical Technology Letters Volume 49, Issue 7, Date: July 2007, Pages: 1595-1597

[23] Jiseon Paek1, Bonghyuk Park2 and Songcheol Hong1 ," A 3-5 GHz RF Receiver Front-End for UWB Wireless System "Proceedings of the 36th European Microwave Conference

[24] Bo Shi and Michael Yan Wah Chia , "A CMOS Receiver Front-End for 3.1-10.6 GHz Ultra-Wideband Radio " Proceedings of the 3rd European Radar Conference

[25] Bo Shi and Michael Yan Wah Chia , "A 3.1 - 10.6 GHz W Front-End for Multi-Band UWB Wireless Receivers " Radio Frequency Integrated Circuits Symposium.

[26] Yueh-Hua Yu; Chen, Y.-J.E.; Heo, D., "A 0.6-V Low Power UWB CMOS LNA" Microwave and Wireless Components Letters, IEEE Volume 17, Issue 3, March 2007.

[27] Chang-Wan Kim; Min-Suk Kang; Phan Tuan Anh; Hoon-Tae Kim; Sang-Gug Lee;, "An ultra-wideband CMOS low noise amplifier for 3-5-GHz UWB system"

Solid-State Circuits, IEEE Journal of Volume 40, Issue 2, Feb. 2005 Page(s):544 - 547

[28] Bevilacqua, A.; Niknejad, A.M.;, "An ultra-wideband CMOS LNA for 3.1 to 10.6 GHz wireless receivers" Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International 15-19 Feb. 2004 Page(s):382 - 533 Vol.1

[29] Xie, Haolu; Wang, Xin; Wang, Albert; Wang, Zhihua; Zhang, Chun; Zhao, Bin;, "A Fully-Integrated Low-Power 3.1-10.6GHz UWB LNA in 0.18um CMOS" Radio and Wireless Symposium, 2007 IEEE

[30] Robert Hu, " Wide-Band Matched LNA Design Using Transistor's Intrinsic Gate–Drain Capacitor" IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 54, NO. 3, MARCH 2006

Vita and Publication

姓 名: 熊子豪

學 歷:

國立新竹高級中學 (87 年 9 月 ~ 90 年 6 月)

私立逢甲大學電子工程學系 (90 年 9 月 ~ 94 年 6 月)

國立交通大學電信工程所碩士班 (94 年 9 月 ~ 96 年 6 月)

Publication Remarks:

1. Zi-Hao Hsiung and Christina F. Jou, "Novel Wideband CMOS LNA with Only an inductor as input matching network", *IEEE TENCON Conference, October 30 – November 2, 2007, Taipei, Taiwan*.
2. Hui-I Wu, Zi-Hao Hsiung and Christina F. Jou, "A 0.75V CMOS Low-Noise Amplifier for Ultra Wide-band Wireless Receiver", *PIERS 26-30 March, 2007 in Beijing, China*.
3. Win-Ming Chang, Zi-Hao Hsiung, Christina F. Jou **"**Ka-band 0.18 um CMOS low noise amplifier with 5.2 dB noise figure**"** Microwave and optical technology letters, Published Online: 27 Mar 2007 (p 1187-1189)