國 立 交 通 大 學

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碩 士 論 文

低功率、低相位雜訊之雙頻帶
電壓控制振盪器設計

A Dual-Band LC-VCO with Low Power
Low Phase Noise

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摘要

本篇論文的研究焦點著重於降低電壓控制振盪器其功率消耗及相位雜訊的設計。利用電流再利用的架構，可以使電壓控制振盪器在運作時的工作電流只需傳統型電壓控制振盪器運作時的一半而達到低功率消耗的目的。同時，我們也提出在NMOS的基極端外加電阻，此方法可有效降低NMOS熱雜訊進而降低電壓控制振盪器的相位雜訊。根據上述架構及方法，我們完成低功率、低相位雜訊2.5/3.5GHz之雙頻帶電壓控制振盪器。由量測結果(TSMC 0.18-μm 1P6M CMOS製程)，實作之IC均與模擬結果相近並達到預期之特性。在距離中心頻率10-kHz和1-MHz相位雜訊分別下降7.0dB和4.0dB。此設計的提供電壓為1.3V消耗功率為3.12mW，其工作頻率於2.5GHz和3.5GHz時，相位雜訊在距離中心頻率1 MHz分別為-121dBc/Hz和-117dBc/Hz。

A Dual-Band LC-VCO with Low Power Low Phase Noise

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Abstract

The research described in this thesis focuses on the design of a low power consumption and phase noise LC-VCO. With the current-reused topology, the proposed LC-VCO can operate using only half amount of DC current compared with the conventional topologies to achieve low power consumption. Here, we also propose to add an external resistor at the substrate node of the NMOS transistor, which reduces the substrate thermal noise of the NMOS transistor effectively and the phase noise of the LC-VCO as well. Based on proposed topology and novel method, we implement a low power and low phase noise dual-band LC-VCO, which operates at 2.5/3.5 GHz. The proposed dual-band LC-VCO is implemented by TSMC 0.18-μm 1P6M CMOS process and the measured results are similar to simulation ones. Therefore, the performances of the proposed LC-VCO achieve anticipation. The result shows that the phase noise reduction is about 7.0 dB and 4.0 dB at 10-kHz and 1-MHz offset frequency, respectively. With only 1.3 V bias voltage and 3.12 mW power

consumption, the proposed LC-VCO operates 2.5 GHz and 3.5 GHz with phase noise of -121 dBc/Hz and -117 dBc/Hz, respectively, at 1 MHz offset frequency.

誌　　謝

在碩士研究的這二年歲月，首先要感謝的是我的指導教授 唐震寰教授並致上我最誠摯的謝意。感謝老師在專業的通訊領域中，給予我不斷的指導與鼓勵，並賦予了實驗室豐富的研究資源與環境，使得這篇碩士論文能夠順利完成。

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九十六年六月

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Chapter 1 *Introduction*

1.1 Background and Problems

The 802.16 WiMAX (Worldwide Interoperability for Microwave Access) is a recently proposed metropolitan area network that may ignite the broad band wireless access as well as providing backhaul for 802.11 WLAN hotspots [1]. WiMAX communication techniques have attracted great interests in both academia and industry in the past few years for applications in wide-range and high-speed wireless systems. Many people expect that the combination of WiMAX and WLAN will give a complete promising wireless solution for delivering high speed internet access to business, homes, and WiFi hotspots [2]. The Institute of Electrical and Electronics Engineers (IEEE) has recently approved 2.3 GHz, 2.5 GHz, 3.5 GHz, and 5.2 GHz bands for WiMAX deployment. Figure 1.1 shows the global spectrum of WiMAX. Requirements of WiMAX transceivers are strict since the transmission distance is very far and the data rate is very fast. Therefore how to design a high performance transceiver is an important issue and challenge.

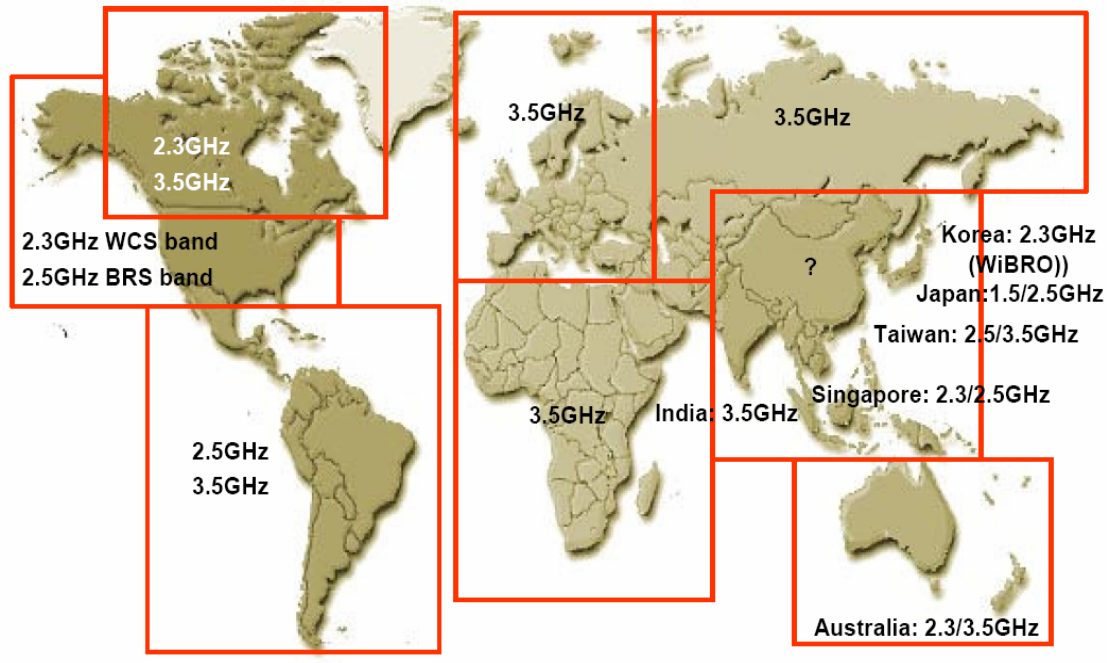


Figure 1.1 Global spectrum of WiMAX.

The VCO is used to provide clean, stable, and precise carrier signals of frequency translation in wireless transceivers. There are several common goals in design WiMAX VCO including low phase noise, low power consumption, low cost, satisfactory output power, and sufficient tuning range. How to design a low phase noise, low power consumption, satisfactory output power, and sufficient tuning range VCO is an arduous challenge. We start this thesis with the deep analysis of the phase noise, power consumption, output power, and tuning range problems, and get thorough insight into the recently-published literatures. After that, we try to find new ways of achieving these problems.

The thesis proposes a new dual-band VCO architecture to cover 2.5 GHz to 2.69 GHz and 3.4 GHz to 3.7 GHz for WiMAX systems, which uses a current-reused

architecture to achieve low power consumption and decrease the area of the circuit. In addition, a novel and effective method by adding an external and large resistor to the substrate node of the MOS is also proposed. The proposed method reduces the thermal noise of the substrate and then yields low phase noise. The novel proposed dual-band VCO topology not only achieves low power consumption but also attains low phase noise.

1.2 Related Works

In the design a VCO, low phase noise and low power consumption are two important requirements. The low power consumption may be achieved by reducing the supply voltage and/or the current in the VCO core circuit. The low voltage operation mainly relies on scaling down metal-oxide-semiconductor (MOS) threshold voltage V_T.

However, the low voltage limits the signal amplitude, which in turn limits the signal-to-noise ratio (SNR) and increases the phase noise of VCO. Therefore, how to control a low phase noise effectively at the low power level becomes an important and challenge issue. [3] suggests to add an external circuit called a harmonic tuned (HD) LC tank to suppress the harmonic frequency of the circuit. This method can reduce the phase noise effectively, but it also increases both the die area and power consumption. Another method is to use high Q (quality factor) passive components such as inductors and varactors in the circuit to reduce resonator's thermal noise [4-5]. However, this method may be not so effective since the maximum achievable Q of the passive component is mainly limited by the semiconductor process and may only be slightly improved by design or layout techniques [6].

1.4 Thesis Organization

The thesis is organized into five chapters including the introduction. Chapter 2 deals with the basic concepts of VCO design, its metrics and some popular voltage-controlled oscillator (VCO) topologies. Chapter 3 proposes new method to reduce the thermal noise at the substrate of the NMOS effectively. In chapter 4, we design the low phase noise low power consumption dual-band VCO with the simulated and measured results. Chapter 5 conclusion is drawn.

Chapter 2 *Basics of Voltage Controlled Oscillator (VCO)*

2.1 Conventional LC-VCO Architectures

The frequency of most radio frequency (RF) oscillators must be adjustable, hence the voltage-controlled oscillator (VCO) is an extremely important block of the wireless communication system. The VCO is used as a local oscillator to up-conversion or down-conversion signals. Although ring oscillator has wider tuning range, phase noise is worse. On the other hand, the LC-tank VCO has lower phase noise, but the tuning range is narrow. In the modern wireless communication system, the VCO must be have extremely low phase noise, hence the LC-tank VCO is be adopted. In this section, the some kinds of LC-tank oscillators are presented.

The basic ingredients in these oscillators are simple：one transistor plus a resonator. Many of the oscillators are named after the fellows who first came up with the topologies but, as we'll see, a more or less unified description of these designs is possible. As mentioned in the earlier example, a capacitive voltage divider off of the tank provides feedback to an amplifier in a Colpitts oscillator as shown in Figure 2.1.

In alternative versions of the Colpitts, the feedback is from source back to the gate rather than from drain to source. Illustrated in Figure 2.1, the equivalent parallel resistance in the tank is approximately equal to $(1+C_1/C_2)^2/gm$.

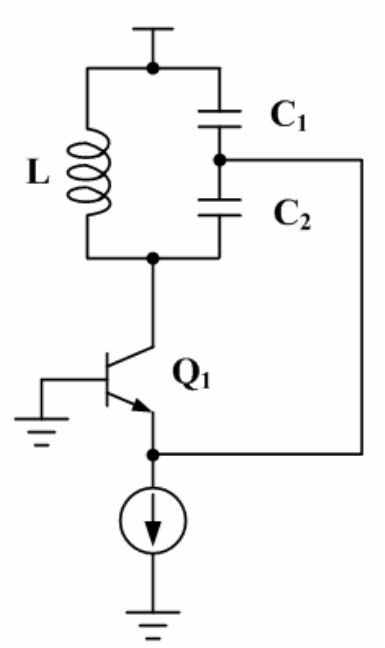


Figure 2.1 Colpitts oscillator (biasing not shown).

Illustrated in Figure 2.2, the equivalent parallel resistance in the tank is approximately equal to $(1+L_2/L_1)^2/gm$, enhancing the equivalent *Q* by roughly the same factor. As shown in Figure 2.2, this oscillator called Hartley oscillator is essentially identical to the Colpitts, but use a tapped inductor for feedback instead of a tapped capacitor. The Hartley oscillator has its origins in the very early days to radio, when tapped inductors were readily available. It is much less common today. One could also use a tapped resistor, in principle, but that particular configuration doesn't seem to have a name attached to it.

A modified Colpitts oscillator is called the Clapp oscillator as shown in Figure 2.3, with a series LC replacing the long inductor. The Clapp oscillator is actually just a Colpitts oscillator with an additional tap on the capacitive divider chain.

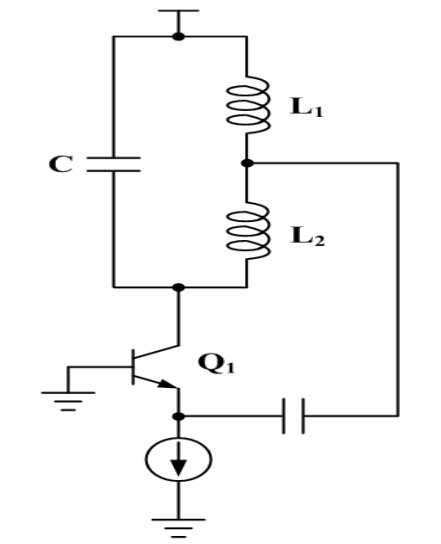


Figure 2.2 Hartley oscillator (biasing still not shown).

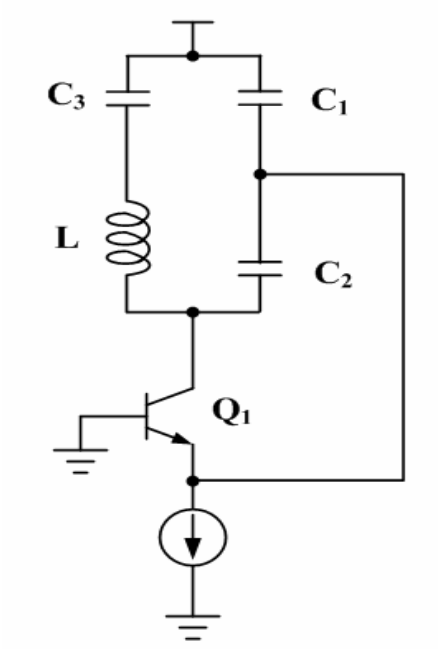


Figure 2.3 Clapp oscillator (biasing still not shown).

As shown in Figure 2.4, a circuit that has become a frequently recurring idiom in recent years uses a cross-coupled differential pair to synthesize the negative resistance. The signal fed back from the drain of a transistor to its source must pass through an impedance transformer so as to avoid loading the tank excessively. In

many oscillators, such as the circuit of Figure 2.7, the allowable signal amplitudes are constrained by the available supply voltage or breakdown voltage considerations. Useful output may be obtained either through a buffer interposed between the oscillator core and load, or through a capacitive voltage divider to avoid spoiling resonator *Q*.

Tuning of all LC-tank oscillators may be accomplished by realizing all or part of C1 or C2 as a variable capacitor (varactor), and tuning its effective capacitance with an appropriate bias control voltage. Since CMOS junction capacitors have relatively poor Q, it is advisable to use only as much junction capacitance as necessary to achieve the desired tuning range.

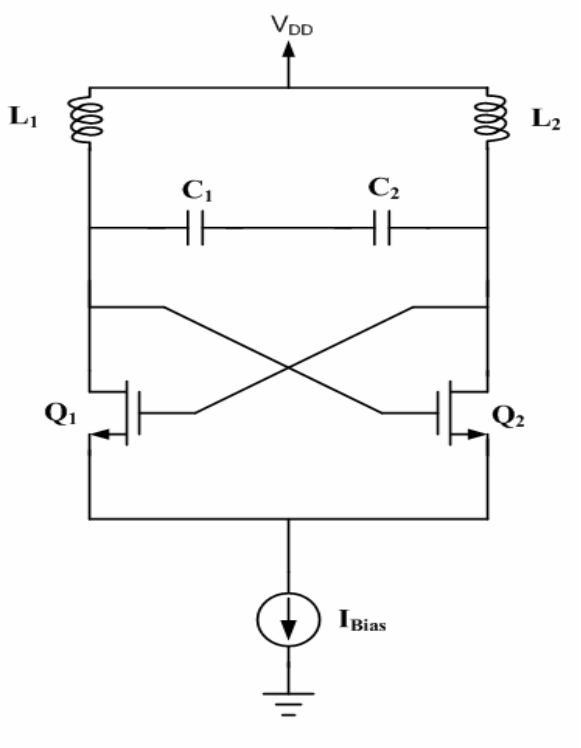


Figure 2.4 The simple differential negative resistance oscillator.

2.2 Performance Parameters

2.2.1 Phase Noise

An ideal output spectrum of oscillator has only one impulse at the fundamental frequency as shown in Figure 2.5(a). A realistic oscillator has a spectrum with spurious signals due to its harmonics or intermodulation products. In addition, the frequency spectrum of the realistic oscillator exhibits skirts around the carrier frequency. The realistic oscillator output spectrum and the definition of phase noise is shown in Figure 2.5(b). The phase noise due to random fluctuations caused by thermal and other noise sources, and appears as a broad continuous distribution localized about the output signal. The phase noise is defined as the ration of power in one phase modulation sideband to the total signal power per unit bandwidth at a particular offset, f_m, from the signal frequency, and is denoted as $L(f_m)$. It is usually expressed in describes relative to the carrier power per Hertz of bandwidth (dBc/Hz). Phase noise is typical expressed as [10]

$$L(f_m) = 10\log\left[\frac{P_{SSB,1Hz}(f_m)}{P_C}\right] \quad (dBc/Hz), \tag{2-1}$$

Where $P_{SSB,1Hz}(f_m)$ represents the single sideband power at a frequency offset of f_m from the carrier with a measurement bandwidth of 1Hz, P_C is the carrier power. From (2-1), the output power must be maximized in order to reduce to phase noise, but it will suffer from high DC power consumption.

Lesson has proposed an equation of phase noise by analyzing a feed back oscillator and is written as [11]

$$L(\Delta\omega) = 10\log\left\{\frac{2FKT}{P_S}\cdot\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\cdot\left[1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right]\right\}, \tag{2-2}$$

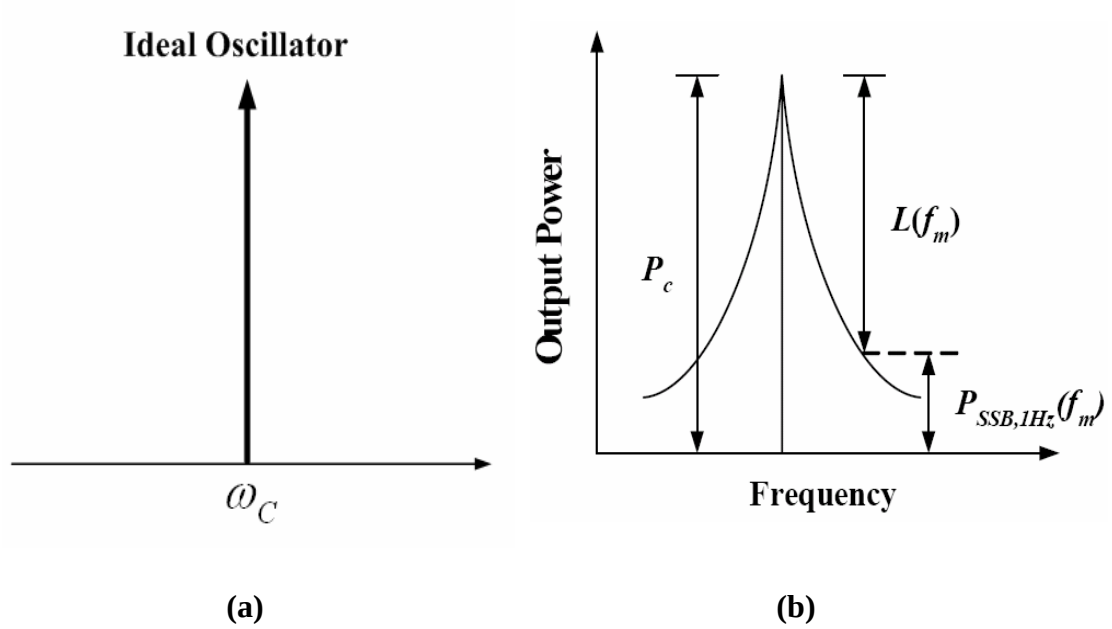


Figure 2.5 Output spectrum of ideal and realistic oscillators.

where F is the excess noise factor, K is the Boltamann's constant, T is the standard noise temperature, ω_0 is the oscillator frequency, Q is the loaded Q, and $\Delta\omega_{1/f^3}$ is the corner frequency, where the slope of the phase noise spectral density changes from -30 dB/dec to -20 dB/dec. Figure 2.6 shows the Lesson's phase noise model. The equation is from the cure fitting after measured results of VCO. Therefore, $\Delta\omega_{1/f^3}$ is from measured results. If the output wave form is odd-symmetry, it can suppress $1/f$ noise effectively. This will be lower $\Delta\omega_{1/f^3}$. From equation (2-2), increase Q factor of LC-tank and output power can improve phase noise.

Low phase noise can be achieved by using low noise figure or low flicker noise active device and high-Q resonator. Moreover, using a low noise power supply or filtering out the noise of power supply are good approaches to reduce phase noise.

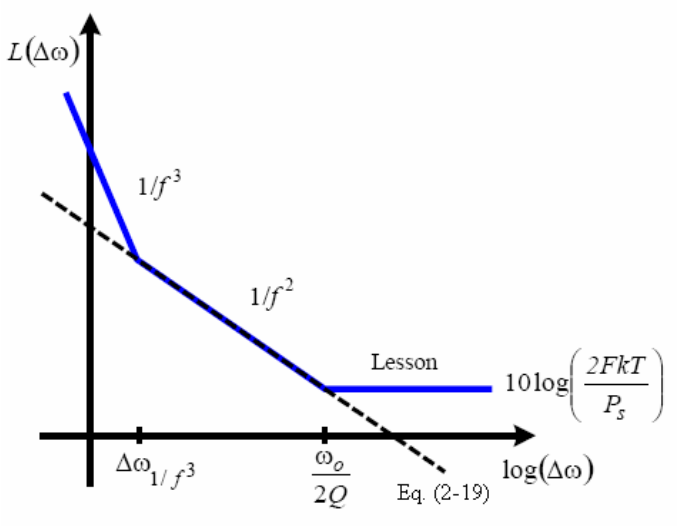


Figure 2.6 Lesson's phase noise model.

2.2.2 Tuning Range

For the LC-VCO design, Choosing suitable inductors and varactors to cover all the frequency band of the specified application is important. A CMOS oscillator must be designed with a large tuning range to overcome process variations. The output frequency of LC-VCO is tuned by varactors, which is like as diode varactors or MOS varactors, so the capacitance versus tuning voltage characteristic is important. In general, the NMOS cross-coupled pair LC-VCO has higher tuning range than double cross-coupled LC-VCO topology for equal effective tank transconductance.

When control voltage change, the bias voltage of transistor will also change. S parameter and Γ_{in} will change according to DC current variation. This phenomenon will cause output frequency shift. This is called pushing effect. To avoid pushing effect, using high quality resonator can reduce the pushing effect. In addition, using regulator also can overcome pushing effect such as band gap circuits. Loading effect is another important issue. When loading change, its impedance is also change. This will cause output frequency shift, too. This called load pulling effect. To avoid this

issue, we can use buffer circuit to overcome load pulling effect.

2.2.3 Tuning Sensitivity (K_{VCO})

The varactor is basically a reverse biased *pn* junction diode whose depletion capacitance is a function of voltage [12]. Even though popular, this type of tuning does not have a wide tuning range and is also sensitive to temperature variation. We now quantify the K_{VCO} of such an arrangement. We definition of K_{VCO} with units in Hz/s：

$$K_{VCO} = \frac{1}{2\pi} \cdot \frac{d\omega_0}{dV_{If}} = \frac{1}{2\pi} \cdot \frac{d\omega_0}{dV_{tune}} = \frac{df_0}{dV_{tune}} \tag{2-3}$$

K_{VCO} in general should be designed to be as small as possible. However, it must be large enough that f_0 can span the whole frequency range with a tuning voltage, V_{tune}, that is within the power supply. K_{VCO} should be made small because the varactor is connected to the LC-tank via a small fixed capacitor. If K_{VCO} is large, then this coupling capacitor is large and the varactor has a large influence on the resonant frequency of the LC-tank. In addition, the varactor itself has a low Q factor, in particular when compared with the inductor or capacitor in the oscillator. This is due to the resistance in the varactor itself and also due to packing. A large varactor influence and a low Q varactor mean that the varactor resistance is translated across to the tank circuit, and this would reduce the Q of the tank significantly.

The gain, K_{VCO}, of idea LC-VCO must keep constant in the whole tuning range. In fact, the K_{VCO} is not a constant, the tuning characteristic (oscillation frequency versus control voltage) is nonlinearity. Thus, the minimum variation of K_{VCO} across the tuning range is needed for phase-locked loops (PLLs) performance like setting time.

2.2.4 Output Power

In general, it is not easy to predict the output power of the realistic VCO, but we can know that the maximum output power of VCO is not larger than the output power of the transistor in the VCO through large-signal analysis. The output power must be maximized in order to make the waveform less sensitive to noise or to lower phase noise. It trades with power consumption, supply voltage, and tuning range. The designer can choose the active devices whose parameter is known. Therefore, when the VCO is designed, we also can predict the output power of the VCO.

2.2.5 Harmonic Rejection

The VCO has a good harmonic rejection performance that means it is closed to a sinusoidal output waveform. In wireless communication systems, harmonic rejection is specified how much smaller the harmonics of the output signal are compared with the fundamental output power.

2.2.6 Power Consumption

With fast growth in the radio-frequency (RF) wireless communications market, the demand for low-power and high-performance but low-cost RF solutions is rising. Low–power operation can extend the lifetime of the battery and save money for consumers.

2.3 Noise Model of VCO

Phase noise is the most important parameter in the VCO design since the most critical performance specification for an oscillator is phase noise. In a receiver, the phase noise of the LO limits the ability to detect a weak signal in the presence of a strong signal in an adjacent channel. In a transmitter, phase noise results in energy being transmitted outside of the desired band. There are two models that are Lesson's model and Hajimiri model to be presented. Lesson has developed a time invariant model to describe the noise of oscillators. Hajimiri proposed a linear time variant phase noise model. This model can more accurately predict the phase noise of VCO.

2.3.1 Time Invariant Model

In this section, phase noise analysis is described by using time invariant model. Time invariant means whenever noise sources injection, the phase noise in VCO is the same. In the other words, phase shift of VCO caused by noise is the same in any time. Therefore, it's no need to consider when the noise is coming. Suppose oscillator is consists of amplifier and resonator. The transfer function of a band-pass resonator is written as

$$H(j\omega) = \frac{j\omega\frac{1}{RC}}{\frac{1}{LC} + j\omega\frac{1}{RC} - \omega^2} \tag{2-4}$$

The transfer function of a common band-pass is written as

$$H(j\omega) = \frac{j\omega\frac{\omega_0}{Q}}{\omega_0^2 + j\omega\frac{\omega_0}{Q} - \omega^2} \tag{2-5}$$

Compare equation (2-4) with (2-5). Thus,

$$\omega_0 = \frac{1}{LC} \quad \text{and} \quad Q = \omega_0 RC \tag{2-6}$$

The frequency $\omega = \omega_0 + \Delta\omega$ which is near oscillator output frequency. If $\omega_0 \gg \Delta\omega$, we can use Taylor expansion for only first and second terms. Hence

$$H(j\omega) \approx 1 + \frac{2}{j\frac{\omega_0}{Q}} \cdot \Delta\omega \tag{2-7}$$

The close-loop response of oscillator is expressed by

$$G(j\omega) = \frac{1}{1 - H(j\omega)} \approx \frac{-j\frac{\omega_0}{Q}}{2 \cdot \Delta\omega} \tag{2-8}$$

When input noise density is $S_i(\omega)$, the output noise density is

$$S_0(\omega) = S_i(\omega)\left|G(\omega)\right|^2 = FkT\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \tag{2-9}$$

The above equation is double sideband noise. The phase noise faraway center frequency $\Delta\omega$ can be expressed by

$$L(\Delta\omega) = 10\log\left[\frac{2FkT}{P_S} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{2-10}$$

Where F is empirical parameter (“often called the device excess noise number”), k is Boltzman’ s constant, T is the absolute temperature, P_S is the average power dissipated in the resistive part of the tank, ω_0 is the oscillation frequency, and Q is the effective quality factor of the tank with all the loading in place(also known as loaded Q). From equation (2-10), increasing power consumption and higher Q factor can get better phase noise. Increasing power consumption means increasing the power of amplifier. This method will decrease noise figure (NF) and improve phase noise.

From, equation (2-10), we can briefly understand phase noise. But the equation and actual measured results are different. The VCO spectrum is shown as Figure 2.9. The phase noise equation can be modified as the same as equation (2-19) that is called

Lesson's model.

$$L(\Delta\omega) = 10\log\left\{\frac{2FKT}{P_S}\cdot\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\cdot\left[1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right]\right\}$$

2.3.2 Time Variant Model

In this section, we use the Hajimiri model to explain the phase noise. An oscillator can be modeled as a system with n inputs (each associated with one noise source) and two outputs that are the instantaneous amplitude and excess phase of the oscillator, $A(t)$ and $\Phi(t)$. $A(t)$ and $\Phi(t)$ are functions of time. Noise inputs to this system are in the form of current sources injecting into circuit nodes and voltage sources in series with circuit branches. For each input source, both systems can be viewed as single-input, single-output systems. The time and frequency-domain fluctuations of $A(t)$ and $\Phi(t)$ can be studied by characterizing the behavior of two equivalent systems shown in Figure 2.7.

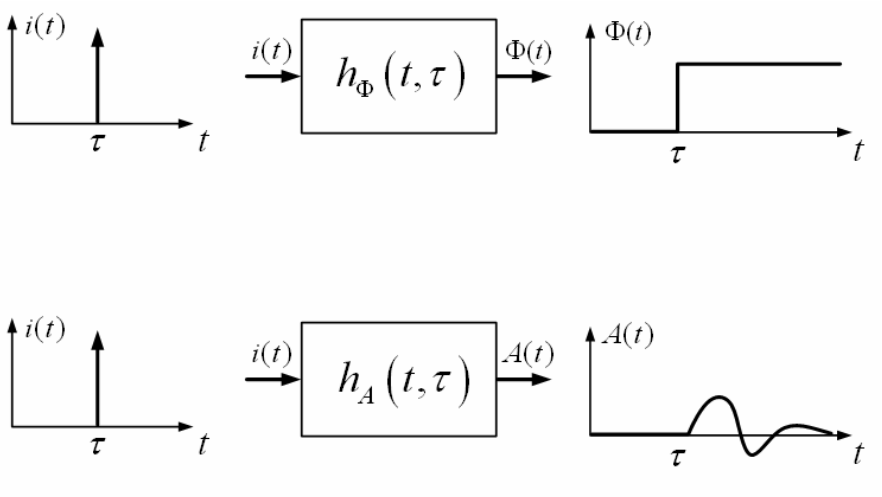


Figure 2.7 Phase and amplitude impulse response model.

At first, we assume that an impulse current injects into a lossless LC-tank as illustrated in Figure 2.8. If the impulse happens to coincide with a voltage maximum as shown in top of Figure. 2.9. The amplitude increase $\Delta V = \Delta Q/C$, but the timing of the zero crossings does not change. An impulse injected at any other time displaces the zero crossing as shown in bottom of Figure 2.9. Hence, an impulsive input produces a step in phase, so the integration is an inherent property of the impulse to phase transfer function. Because the phase displacement depends on that the impulse is applied, the system in time variant.

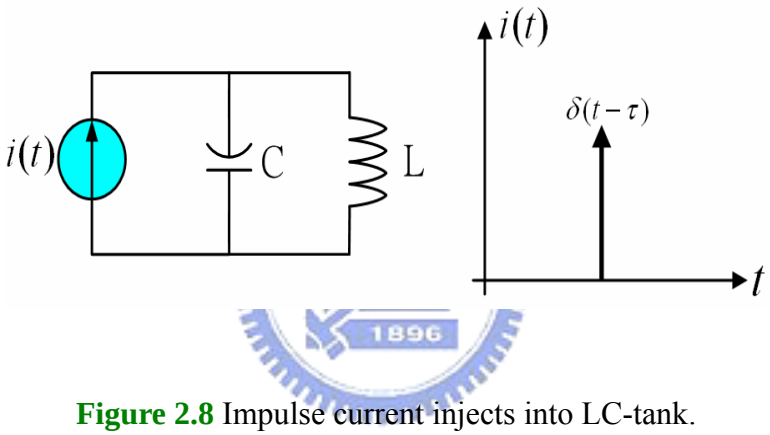


Figure 2.8 Impulse current injects into LC-tank.

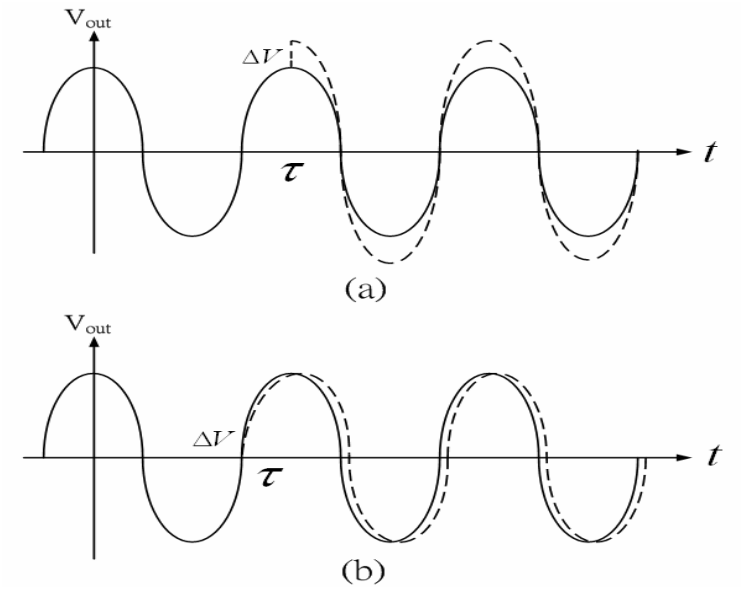


Figure 2.9 Waveforms for impulse excitation.

Hajimiri proposed a linear time variant phase noise model which is different from the Lesson's model. This impulse response can be written as

$$h_{\Phi}(t,\tau)=\frac{\Gamma(\omega_0\tau)}{q_{\max}}u(t-\tau), \tag{2-11}$$

where q_{max} is the maximum charge displacement across the capacitor and $u(t)$ is the unit step. The function $\Gamma(x)$ is called the impulse sensitivity function (ISF), and is a frequency and amplitude independent function that is periodic in 2π. Once the ISF has been determined, we may compute the excess phase through use of the superposition integral. Hence

$$\Phi(t)=\int_{-\infty}^{\infty}h_{\Phi}(t,\tau)\cdot i(t)\,d\tau=\frac{1}{q_{\max}}\int_{-\infty}^{1}\Gamma(\omega_0\tau)\cdot i(t)\,d\tau \tag{2-12}$$

This equation can be expanded as a Fourier series：

$$\Gamma(\omega_0\tau)=\frac{C_0}{2}+\sum_{n=1}^{\infty}C_n\cos(n\omega_0\tau+\theta_n) \tag{2-13}$$

Where the coefficients C_n are real and θ_n is the phase of nth harmonic of the ISF. We assume that noise components are uncorrelated, so that their relative phase is irrelevant, we will still ignore θ_n. Equation (2-13) can be rewritten as

$$\Phi(t)=\frac{1}{q_{\max}}\left[\frac{C_0}{2}\int_{-\infty}^{t}i(\tau)d\tau+\sum_{n=1}^{\infty}C_n\int_{-\infty}^{t}i(\tau)\cos(n\omega_0\tau)d\tau\right] \tag{2-14}$$

Equation (2-14) allows us to compute the excess phase caused by an arbitrary noise current injected into the system, once the Fourier coefficients of the ISF have been determined. Now we consider the injection of a sinusoidal current whose frequency is near an integer multiple m of the oscillation frequency, so that

$$i(t)=I_m\cos\left[(m\omega_0+\Delta\omega)t\right] \tag{2-15}$$

Substituting (2-15) into (2-14) where $\Delta\omega \ll \omega_0$ and n=m. We can simplify Equation (2-14) as

$$\Phi(t) \approx \frac{I_m C_m \sin(\Delta\omega t)}{2q_{\max}\Delta\omega} \tag{2-16}$$

$$V_{out}(t) = \cos[\omega_0 t + \Phi(t)] \tag{2-17}$$

Then, substituting equation (2-16) into (2-17). Suppose $\frac{I_m C_m}{2q_{\max}\Delta\omega} < 1$. Therefore, the sideband power relative to the carrier is given by

$$P_{SBC}(\Delta\omega) \approx 10\log\left(\frac{I_m C_m}{4q_{\max}\Delta\omega}\right)^2 \tag{2-18}$$

In general, a noise signal can be separated into two type noise source：white noise and flicker noise. First, input an noise current only with the white noise and its noise power spectral density is $\overline{i_n^2}/\Delta f$. The total single sideband phase noise spectral density in dB below the carrier per unit bandwidth is given by

$$C_{SBC}(\Delta\omega) \approx 10\log\left(\frac{\overline{i_n^2}/\Delta f \sum_{m=0}^{\infty} C_m^2}{4q_{\max}^2\Delta\omega^2}\right) \tag{2-19}$$

According to Parseval's theorem. Thus,

$$\sum_{m=0}^{\infty} C_m^2 = \frac{1}{\pi}\int_0^{2\pi} |\Gamma(x)|^2 dx = 2\Gamma_{rms}^2 \tag{2-20}$$

Therefore we can use quantitative analysis to analyze the phase noise sideband power due to the white noise source as following equation

$$C_{SBC}(\Delta\omega) \approx 10\log\left(\frac{\overline{i_n^2}/\Delta f \,\Gamma_{rms}^2}{2q_{\max}^2\Delta\omega^2}\right) \tag{2-21}$$

Where $q_{max} = CV_{max}$, V_{max} is the largest amplitude of VCO, and $\overline{i_n^2}/\Delta f = 4kT/R$.

Substituting these relations into (2-21). We have

$$L(\Delta\omega) \approx 10\log\left[\frac{4kT}{P_S}\Gamma_{rms}^2\left(\frac{\omega_0}{Q\Delta\omega}\right)^2\right] \tag{2-22}$$

If input noise of VCO is *1/f* noise, the power spectral density is written as

$$\overline{i_{n,1/f}^2} = \overline{i_n^2}\frac{\omega_{1/f}}{\Delta\omega}, \tag{2-23}$$

Where $\omega_{1/f}$ is the *1/f* corner frequency of *1/f* noise. This equation represents the phase noise spectrum of an arbitrary oscillator in $1/f^2$ region of the phase noise spectrum. Quantitative analysis for the relationship between the device corner *1/f* and the $1/f^3$ corner of the phase noise can be illustrated by following equation.

$$L(\Delta\omega) \approx 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}C_0^2}{8q_{\max}^2\Delta\omega^2}\cdot\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{2-24}$$

Here we consider the case of a random noise current $i_n(\omega)$ whose power spectral density has both a flat region and a *1/f* region as shown in Figure 2.10. Noise components located near integer multiples of the oscillation frequency are transformed to low frequency noise sidebands for $S_\Phi(\omega)$ and it is become phase noise in the spectrum of $S_v(\omega)$ as illustrated in Figure 2.10.

It can be see that the total $S_\Phi(\omega)$ is given by the sum of phase noise contributions from device noise of the integer multiples of ω_o and weighted by the coefficients C_n. The theory predicts the existence of $1/f^2$, $1/f^3$, and flat regions for the phase noise spectrum. The low frequency noise sources are weighted by the coefficient C_0 and show a dependence on the offset frequency. The white noise terms are weighted by other C_n coefficients and give rise to the $1/f^2$ region of phase noise spectrum. From Figure 2.10, it is obviously that if the original noise current *i(t)* contains $1/f^n$ low frequency noise terms, they can appear in the phase noise spectrum as $1/f^{n+2}$ regions.

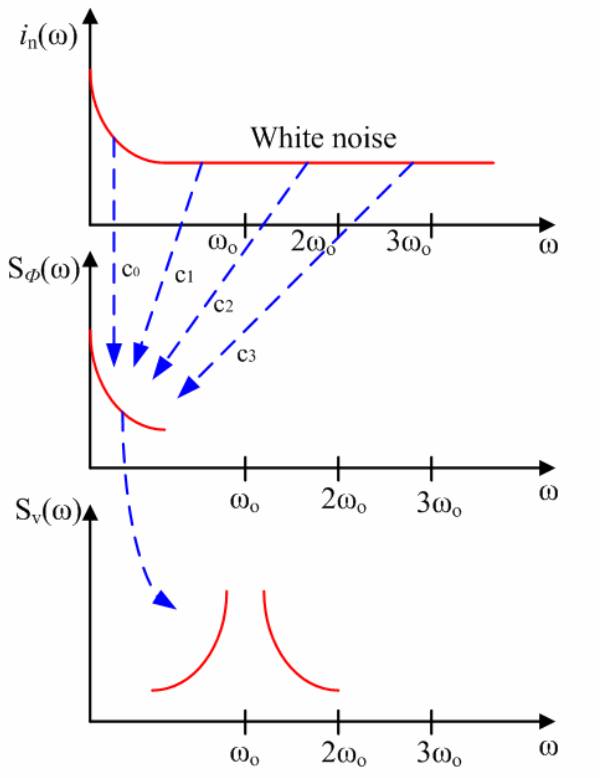


Figure 2.10 Conversion of noise to phase noise sidebands.

Chapter 3 *An Effective Way to Reduce Thermal Noise of NMOS Transistors*

3.1 Introduction

Even though the performances of RF CMOS transistors have been improved by advanced semiconductor process technology, the inherent noise is still an arduous problem to the design of RF circuits. In addition, it is the trade-off between low power consumption and low noise in the RF circuit design, therefore, how to reduce the noise without increasing the power consumption is extremely important issue and greatly valued.

In the RF circuit, the main noise sources come from the MOS transistors, the power supplies, the current sources, the resistances, and the thermal noise associated with the loss in the LC resonator. However, resonator's thermal noise can be reduced by using inductors, capacitors, and varactors which have a high quality factor, Q.

At past research, two popular ways to reduce phase noise of the LC-VCO are adding external circuits and enhancing the quality factor (Q) [3], [6]. [3] suggests that

an external circuit called a harmonic tuned (HD) LC tank is added to suppress the harmonic frequency of the circuit, but this method has some drawbacks. This method leads to the area of circuit become larger and the cost goes up. In addition, it also makes the power consumption increase.

Another method is to enhance the Q. This method can reduce phase noise of LC-VCO without increasing area and power consumption, however, this method is not so effective since the maximum achievable Q for passive components is mainly limited by semiconductor process technology.

A new and efficient method to reduce noise without increasing power consumption is proposed. The proposed method is that adding an external and large resistance at the substrate node of NMOS transistor can reduce the thermal noise at substrate injecting the drain. Furthermore, the low noise amplifier (LNA) and the LC-tank voltage controlled oscillator (VCO) are instanced to illustrate the proposed method. This reduction can decrease not only noise figure of the low noise amplifier (LNA) and phase noise of the LC-tank voltage controlled oscillator (VCO) but also improve input matching performance of the LNA. The proposed method is analyzed through mathematical derivations and simulations for ultra-wideband (UWB) LNA and worldwide interoperability for Microwave Access (WiMAX) LC-VCO circuit designs. It is found that the method could have broad applications in RF circuit design.

In this chapter, section 3.2 briefly describes the RF MOS architecture. Some noise sources which affect the noise level in the RF circuit are presented in Section 3.3. In section 3.4, the simulation results are provided, including some comparisons.

3.2 The Small-Signal Model of MOS Transistors

Recently, many researches focus on modeling a complete device models in order to predict the circuit performance correctly. It has been known that for analog and RF applications, the accuracy of circuit simulation is strongly determined by device models. To have an efficient design environment, design tools with accurate models for devices and interconnect parasitics are essential. So the accurate device models become crucial to predict the circuit performance. Figure 3.1 shows RF NMOS schematic cross section with the parasitic components [15]. Resistances and capacitances which are produced by parasitic effect have relations with semiconductor process.

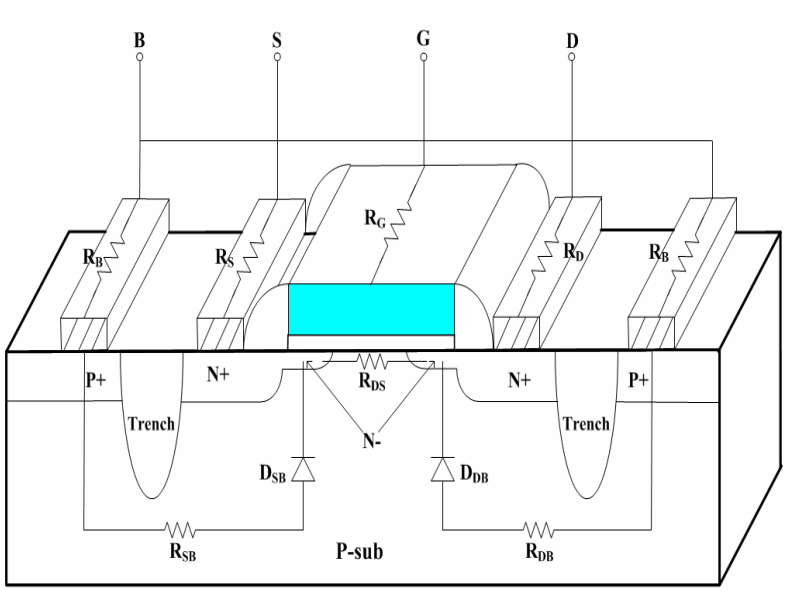


Figure 3.1 RF NMOS schematic cross section with the parasitic components.

MOS transistor models have been originally developed for digital and low-frequency analog circuit designs which focus on the dc current, the conductance, and intrinsic charge/capacitance behavior up to the megahertz. In the modern wireless communication systems, the operating frequency increases to gigahertz range.

Therefore, an RF model with the consideration of the high-frequency (HF) behavior of both intrinsic and extrinsic components in MOS is extremely important to achieve accurate and predicts results in the simulation of RF circuit design. Figure 3.2 shows the equivalent circuit model for RF MOS transistor including parasitic resistances and capacitances. We design and analyze RF circuits using 0.18-μm semiconductor process in this study. The 0.18-μm process and the device models are provided by Taiwan Semiconductor Manufacturing Company (TSMC), hence the semiconductor parameters of MOS and the characteristic parameters of devices are based on TSMC providing.

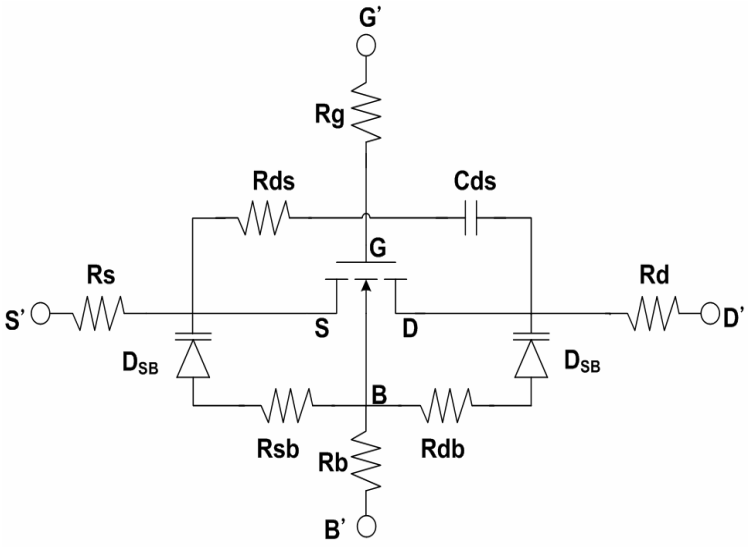


Figure 3.2 The equivalent circuit model for RF MOS transistor.

Figure 3.3 shows the gate-body capacitance C_{gb}, parasitic gate-drain capacitance C_{gdo}, parasitic gate-source capacitance C_{gso}, gate-drain resistance R_{gd}, intrinsic drain-body resistance R_{bd}, intrinsic source-body resistance R_{sb}, parasitic drain-body capacitance C_{db}, and parasitic source-body capacitance C_{sb} [16]. It is the complete small-signal circuit model for RF MOS transistor. In order to simplify the circuit and some components be negligibly small, we neglect the L_g, L_s, L_d, C_{gso}, C_{gdo}, C_{gb}, and R_{gd}.

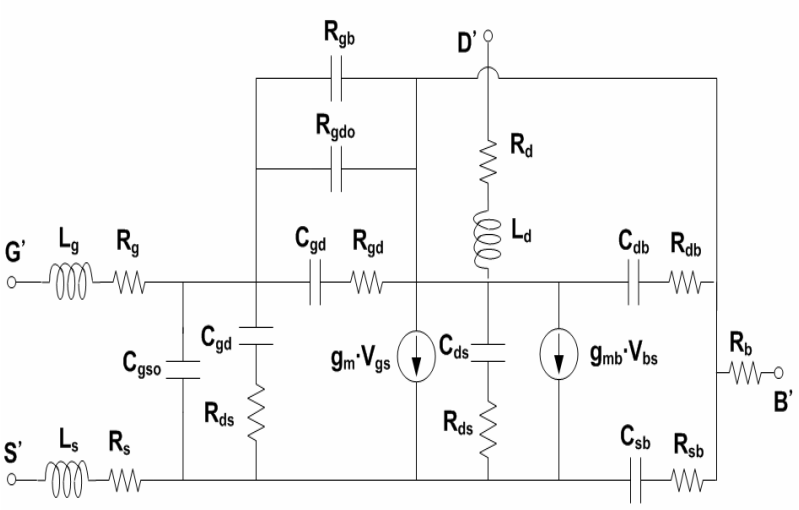


Figure 3.3 The complete small-signal circuit model for RF MOS transistor.

Figure 3.4 that shows the adopted small-signal circuit model for RF MOS transistor is similar to the model of TSMC providing. We use the model showed in Figure3.5 to design and analyze the RF circuit in the after discussion.

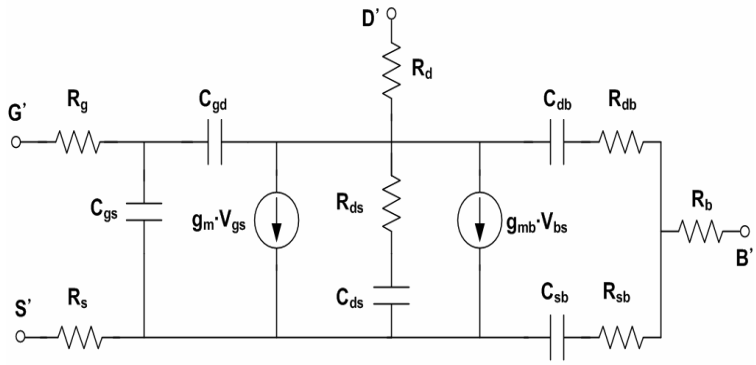


Figure 3.4 The adopted small-signal circuit model for RF MOS transistor.

3.3 Reducing Thermal Noise of NMOS

In CMOS technology, the substrate parasitic impedance can induce the substrate thermal noise of RFIC circuits due to the leaky current through the drain/source to the substrate. We propose the new and effective method that is adding

an external and large resistance at the substrate node of NMOS to reduce the thermal noise of the substrate node injecting the drain node in the NMOS. In this thesis, we do no add this resistance at the PMOS. The reason is the source node of PMOS that connects to V_{DD}. Since the source node connect to V_{DD}, the thermal noise of substrate at PMOS increase. The source of NMOS connects to ground, so this phenomenon does not exist. To explore the method, a small signal equivalent circuit model of the substrate with an external added resistor is developed and is shown in Figure 3.5. In order to simplify the circuit and the component be negligibly small, we neglect the R_s and R_{ds}.

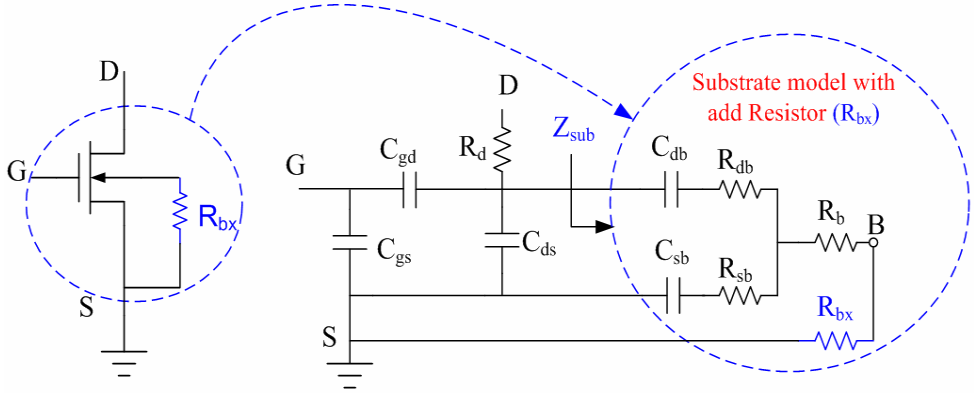


Figure 3.5 Equivalent circuit model of the substrate with an added resistor R_{bx}, which is located between the substrate node and the source node of the RF NMOS transistor.

The impedance of the substrate, Z_{sub}, is derived and given as：

$$Z_{sub} = R_{bd} + \frac{1}{j\omega_0 C_{bd}} + \left[(R_b + R_{bx}) // (R_{sb} + \frac{1}{j\omega_0 C_{sb}}) \right] \tag{3-1}$$

in (3-1), we find that

$$(R_b + R_{bx}) // (R_{sb} + \frac{1}{j\omega_0 C_{sb}}) = \frac{(R_b + R_{bx}) \times \frac{1 + j\omega_0 R_{sb} C_{sb}}{j\omega_0 C_{sb}}}{(R_b + R_{bx}) + \frac{1 + j\omega_0 R_{sb} C_{sb}}{j\omega_0 C_{sb}}}$$

$$(R_b + R_{bx}) // (R_{sb} + \frac{1}{j\omega_0 C_{sb}}) = \frac{(R_b + R_{bx}) \times (1 + j\omega_0 R_{sb} C_{sb})}{1 + j\omega_0 \left[R_{sb} + (R_b + R_{bx}) \right] C_{sb}} \quad (3\text{-}2)$$

If R_{bx} is large enough, let $\omega_0^2 \left[R_{sb} + (R_b + R_{bx}) \right]^2 C_{sb}^2 \gg 1$, and since $R_{bx} \gg R_b$, $R_{bx} \gg R_{sb}$, (3-1) can be written as

$$Z_{sub} = R_{bd} + \frac{1}{\omega_0^2 (R_b + R_{bx}) C_{sb}^2} + \frac{C_{sb} + C_{bd}}{j\omega_0 C_{sb} C_{bd}} \quad (3\text{-}3)$$

Let $Z_{sub} = R_{sub} + \frac{1}{j\omega_0 C_{sub}}$

$$R_{sub} \approx R_{bd} + \frac{1}{\omega_0^2 (R_b + R_{bx}) C_{sb}^2} \quad (3\text{-}4)$$

$$C_{sub} \approx \frac{C_{sb} \times C_{bd}}{C_{sb} + C_{bd}} = C_{sb} // C_{bd} \quad (3\text{-}5)$$

From equation (3-4), increase of the added external resistance, R_{bx} lead to reduction of the equivalent substrate resistance R_{sub} and the C_{sub} is not affected by R_{bx}. So we know that R_{sub} is proportion to R_{bx}. Figure 3.6 shows the simplified equivalent circuit model of the substrate with an added resistor R_{bx}.

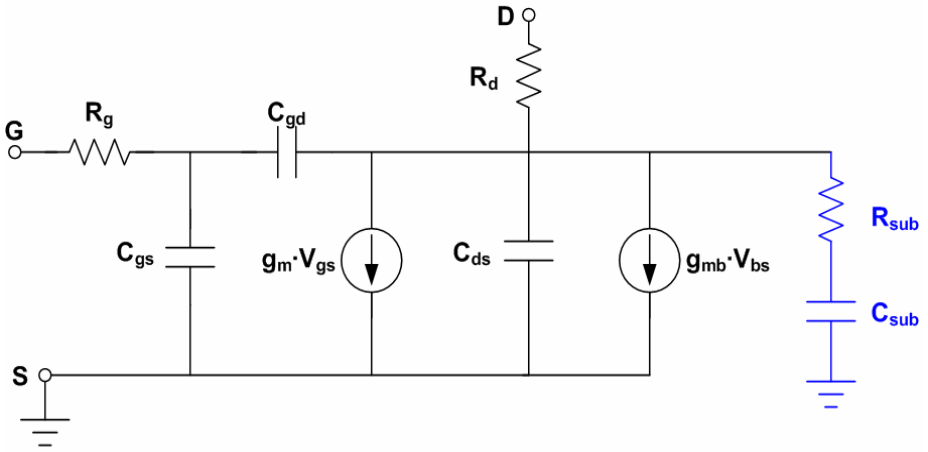


Figure 3.6 Simplified equivalent circuit model of the substrate with an added resistor R_{bx}.

Figure 3.7 (a) shows the simplified equivalent voltage noise circuit model with the added external resistor and Figure 3.7 (b) shows the simplified equivalent current noise circuit model with the added external resistor.

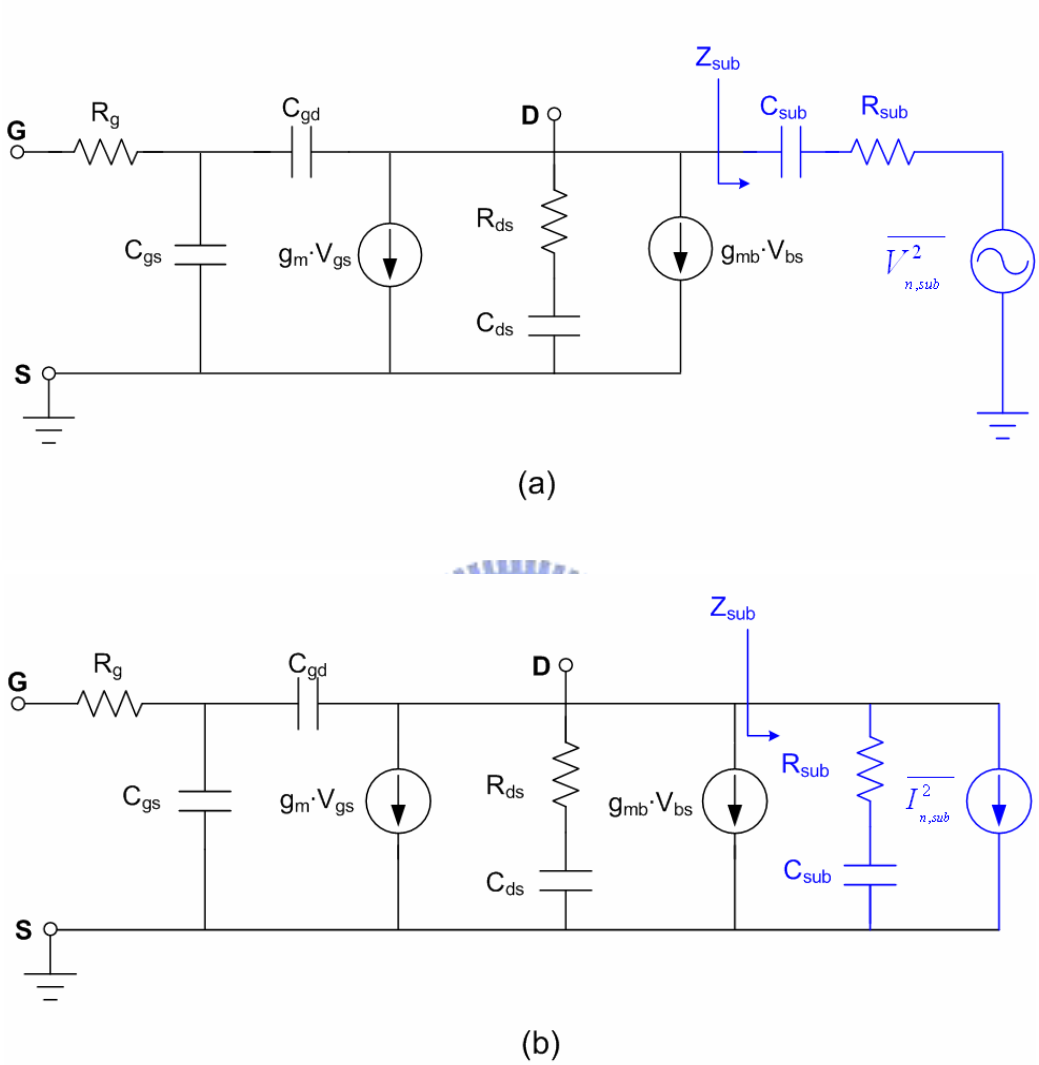


Figure 3.7 the simplified equivalent noise circuit model with the added external resistor R_{bx}：(a) the voltage noise model and (b) the current noise model.

We choose the current noise model since the noise factor of the LNA and the phase noise of LC-VCO are based on current noise model to calculate. Here, the proposed method is applied to ultra-wideband (UWB) LNA and worldwide interoperability for Microwave Access (WiMAX) LC-VCO to validate its effectiveness. Figure 3.8 (a) illustrates the proposed UWB LNA architecture with an

external resistance R_{bx} added to the transistor M_1. To explore the noise figure of the LNA, the noise factor is derived first and is equal to the ratio between the input noise power and the output noise power of the circuit.

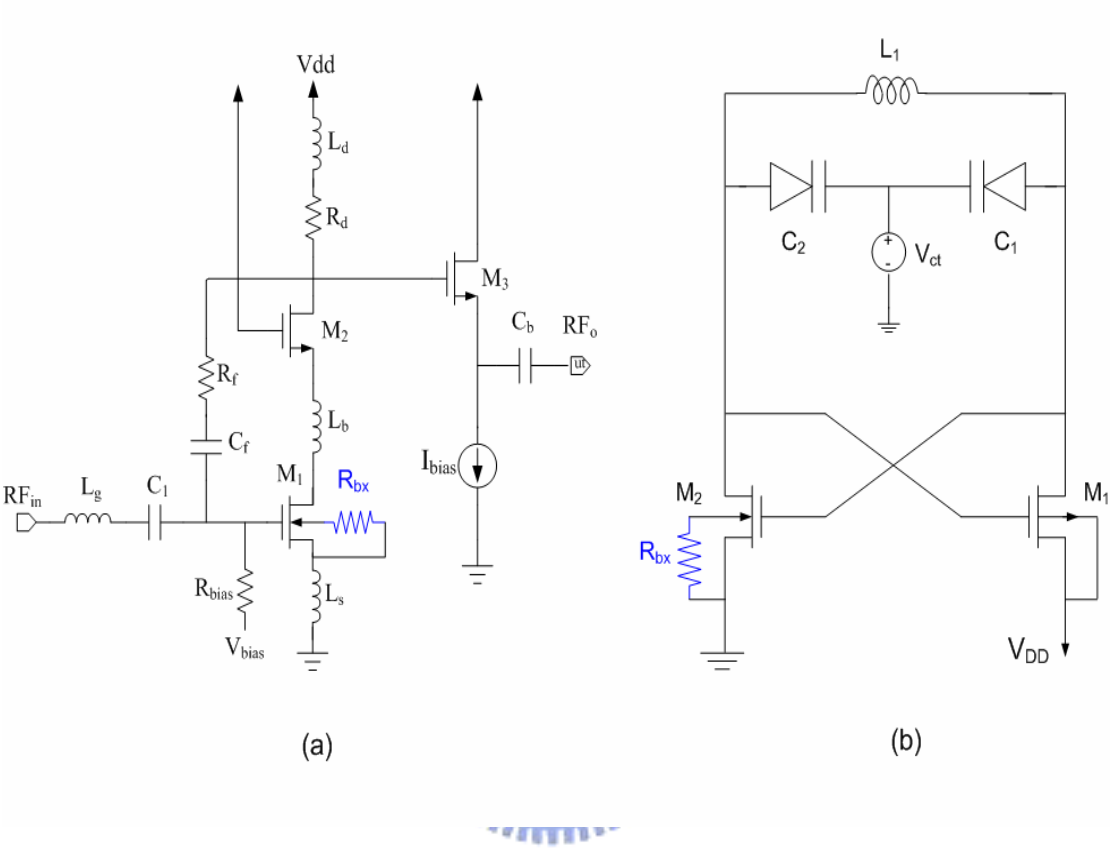


Figure 3.8 Circuit schematics (a) Proposed UWB LNA (b) Proposed WiMAX LC-VCO In both circuits, the external resistor is added between the body and the source.

According to the proposed UWB LNA and using the substrate model shown in Figure 3.7 (b), after some derivations the noise factor of the LNA is given by

$$F = 1 + \frac{\gamma}{Q_s \alpha}\left(\frac{\omega_0}{\omega_T}\right) + \left(\frac{1+Q_s^2}{Q_s^2}\right)\frac{\delta\alpha}{5}\left(\frac{\omega_0}{\omega_T}\right) + \frac{Z_{sub}}{Q_s^2 R_s} + 2|C|\frac{1}{Q_s}\sqrt{\frac{\delta\gamma}{5}}\left(\frac{\omega_0}{\omega_T}\right) + 2|C_2|\frac{1}{Q_s}\sqrt{\frac{\delta\alpha G_m}{5} Z_{sub}}\left(\frac{\omega_0}{\omega_T}\right), \quad (3\text{-}19)$$

where $Q_s = \frac{1}{R_s \omega_0 C_{gs}}$, α and γ are bias-dependent parameters, δ is the coefficient of gate noise, and C is the correction coefficient for the gate noise and drain noise, and ω_0 is the center frequency, ω_T is the cutoff frequency. C_2 is the correction coefficient

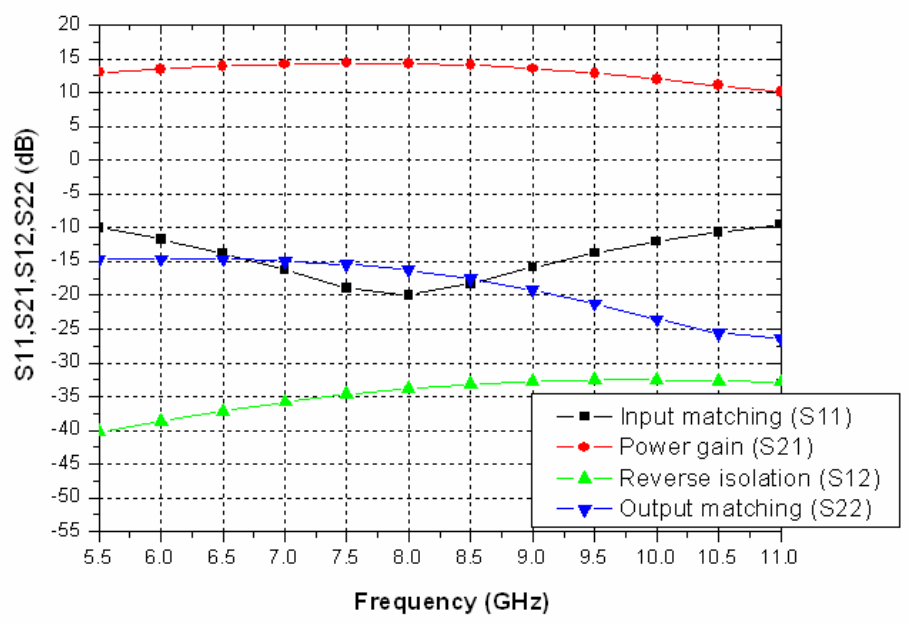
for the gate noise and substrate noise. From equation (3-19), we find that the noise factor is direct proportion to Z_{sub} and Z_{sub} is inverse proportion to R_{bx}. Therefore, the noise factor, F, is inverse proportion to R_{bx}. Figure 3.8 (b) shows the proposed WiMAX LC-VCO using an external resistance R_{bx} of transistor M_1. According to the Hajimiri-Lee phase noise model and after some derivations, phase noise of the LC-VCO is given by

$$L\{\Delta f\} = 10\log\{(\frac{\Gamma_{rms}^2 \dfrac{\overline{inp^2}}{\Delta f}}{q_{\max}^2 8(2\pi\Delta f)^2})(1+\frac{\omega_{p1/f^3}}{2\pi\Delta f})+(\frac{\Gamma_{rms}^2 \dfrac{\overline{inn^2}}{\Delta f}}{q_{\max}^2 8(2\pi\Delta f)^2}) \\ (1+\frac{\omega_{p1/f^3}}{2\pi\Delta f})+(\frac{\Gamma_{rms}^2 \dfrac{\overline{inl^2}}{\Delta f}}{q_{\max}^2 2(2\pi\Delta f)^2})\}, \tag{3-20}$$

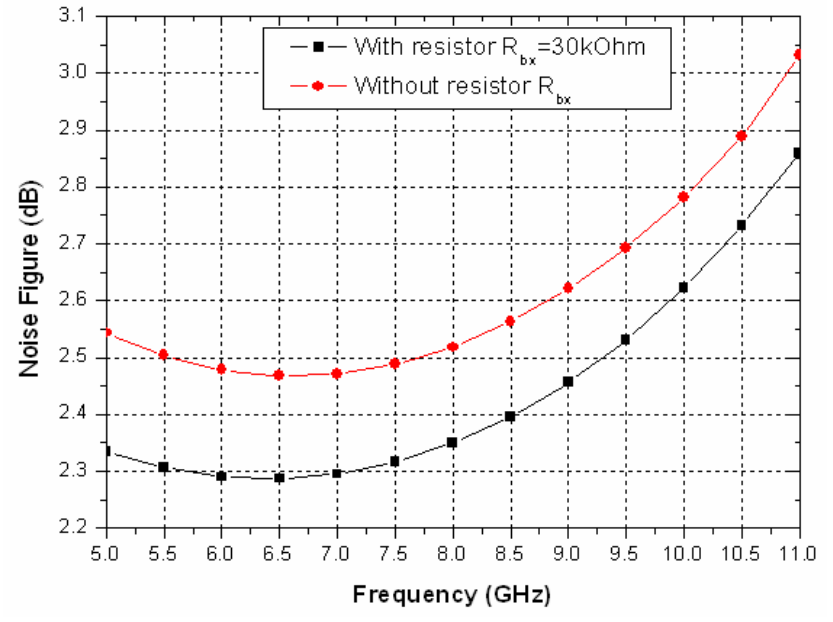
where Δf is the offset frequency from the carrier, $q_{\max}$ is the total charge swing of the tank, Γ_{rms} is root mean square value of impulse sensitivity function, $\overline{inp^2}/\Delta f$, and $\overline{inn^2}/\Delta f$ is PMOS and NMOS noise power spectral density, $\overline{inl^2}/\Delta f$ is resonator's thermal noise. It is noted that with the external resistance $\overline{in_{sub}^2}/\Delta f$ is a part of $\overline{inn^2}/\Delta f$ equal to $4kTR_{sub}g_{mb}^2$ that is decreased with the external resistance according to equation (3-17). We propose the new method is effective since the most noise contribution is provided by NMOS in this LC-VCO topology.

In simulation, the TSMC 0.18-μm 1P6M CMOS process, the low power UWB LNA design is proposed. A low supply voltage of 1.5V is chosen, and the total power consumption is 9.0mW. This proposed method not only reduces the noise figure but also improve the input matching performance in the LNA. The simulation results are shown as Figure 3.9 (a).In the Figure 3.9 (b), it shows that the noise figure (NF) is smaller when R_{bx}=30kΩ to compare with the case without R_{bx}. It is found that the

noise figure is at least less than 2.7dB in 6.0~10.6GHz and its minimum value is 2.28dB at 6.5GHz. Furthermore, the simulation result shows that there is about 0.1 dB to 0.3 dB of noise figure (NF) reduction with common source UWB LNA.



(a)



(b)

Figure 3.9 Simulation results (a) S-parameters versus signal frequency of LNA; (b) Noise figure versus signal frequency with and without R_{bx}.

A low power and low phase noise WiMAX LC-VCO is proposed. A low supply voltage of 1.2V is chosen, and the core circuit power consumption is 0.996mW. In the Figure 3.10, it shows that the phase noise of LC-VCO is smaller when R_{bx}=30 kΩ to compare with the case without R_{bx}. It is found that when LC-VCO operates at 3.5 GHz, there is about 7.0 dB and 4.0 dB of phase noise reduction at 100 kHz and 1 MHz offset frequency, respectively. In addition, the proposed LC-VCO operates at 3.5 GHz with phase noise of -121 dBc/Hz at 1 MHz offset frequency.

The phase noise versus R_{bx} as shown in Figure 3.11, we can find that when the value of R_{bx} is about larger than 30 kΩ, the phase noise almost limited. Therefore, it is a reason that why we choose the value of Rbx to be 30 kΩ. In addition, this proposed method is effective through mathematical derivations and numerical simulations for UWB LNA and WiMAX LC-VCO. The performance of the propose LNA and LC-VCO are summarized in Table 3.1 and Table 3.2, respectively, with comparison to other recently published papers.

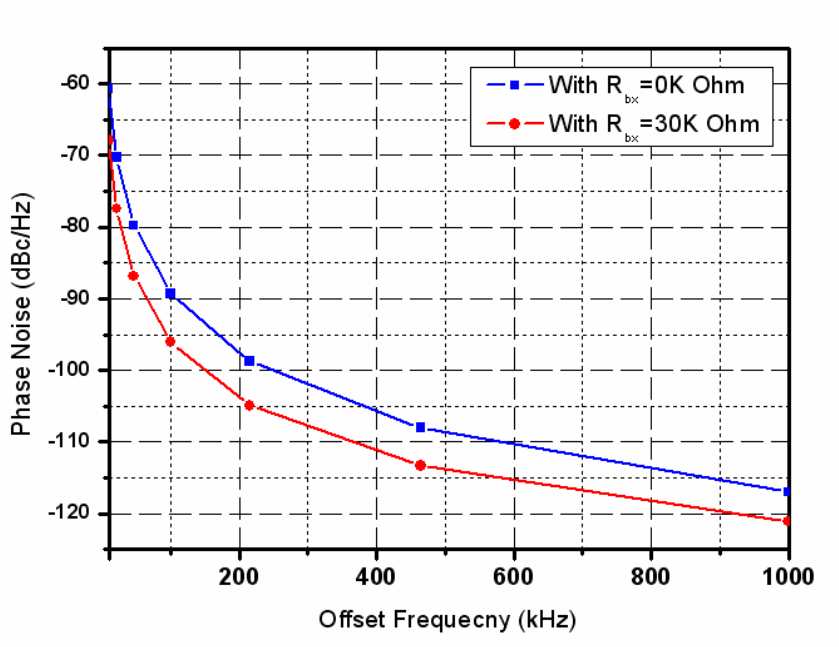


Figure 3.10 Simulated results of phase noise versus offset frequency with and without R_{bx}.

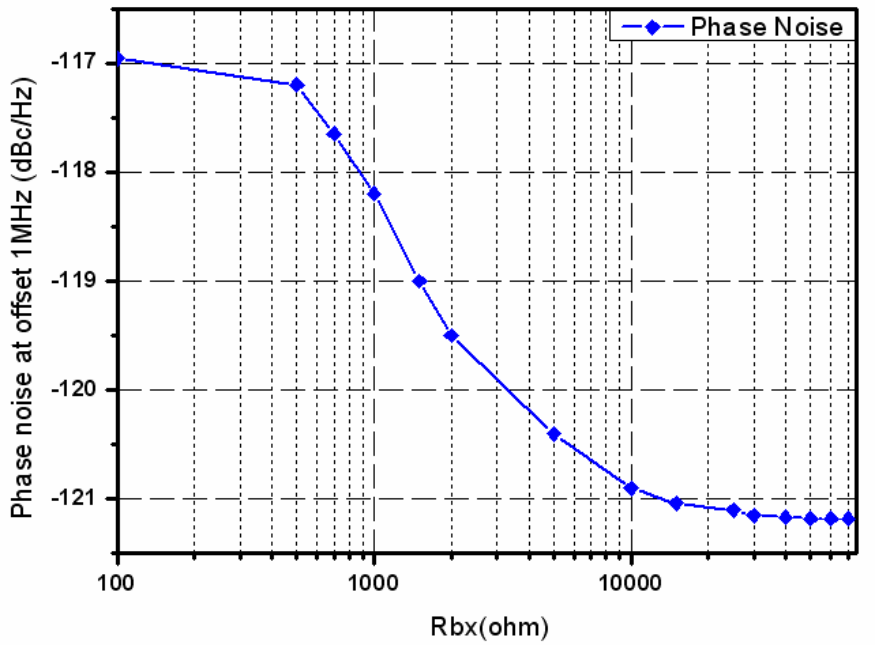


Figure 3.11 Simulated results of phase noise versus R_{bx}.

Table 3.1

Summary of LNA performance and comparison with published LNAs.

Ref.	Tech.	BW (GHZ)	S11 (dB)	Gain (dB)	NF (dB)	VDD (V)	Power (mW)
[21]	0.18-μm CMOS	2.3-9.2	<-9.9	9.3	4.0	1.8	9.0
[22]	0.18-μm CMOS	2.6-9.2	<-11.5	10.9	3.5	1.8	7.1
[23]	0.18-μm SiGe	0.1-11	<-12	8	2.9	1.8	21.6
[24]	0.13-μm CMOS	7.2-8.6	<-9	28	3.9	1.5	3.9
[25]	0.18-μm CMOS	2-10.1	<-9.76	10.2	3.68	1	7.2
Our work	0.18-μm CMOS	5-10.6	<-13.7	14	2.8	-0.75	2.8

Table 3.2

Summary of LC-VCO performance and comparison with published LC-VCOs.

Ref.	**Tech.**	**Freq. (GHz)**	**PN (dBc/Hz)#**	**Out Power (dBm)**	**Power (mW)**	**F.O.M (dBc/Hz)**
[4]	0.35-μm CMOS	2.06	-116*	2.33	22.62	-173.2*
[14]	0.18-μm CMOS	2.2	-122.5	N/A	5.92	-189.5
[26]	0.18-μm GaAs	4	-120	2	25.5	-178
[27]	0.13-μm CMOS	2.17	-132	N/A	5.92	-189.5
Our work	0.18-μm CMOS	3.5	-121	-2.16	22.62	-191

PN (dBc/Hz)# ：at 1 MHz offset frequency. *： at 600 kHz offset frequency.

Chapter 4 *Design of a Dual-Band LC-VCO for 2.5/3.5 GHz WiMAX*

4.1 Introduction

A critical building block of almost any wireless or wireline transceiver is the local oscillator (LO). When use with a mixer, the LO allows frequency translation and channel selection of radio frequency (RF) signals. The LO is typically implemented as a phase-locked loop (PLL) as shown as Figure 4.1, wherein a voltage-controlled oscillator (VCO) is phase-locked to a high-stability crystal oscillator [30].

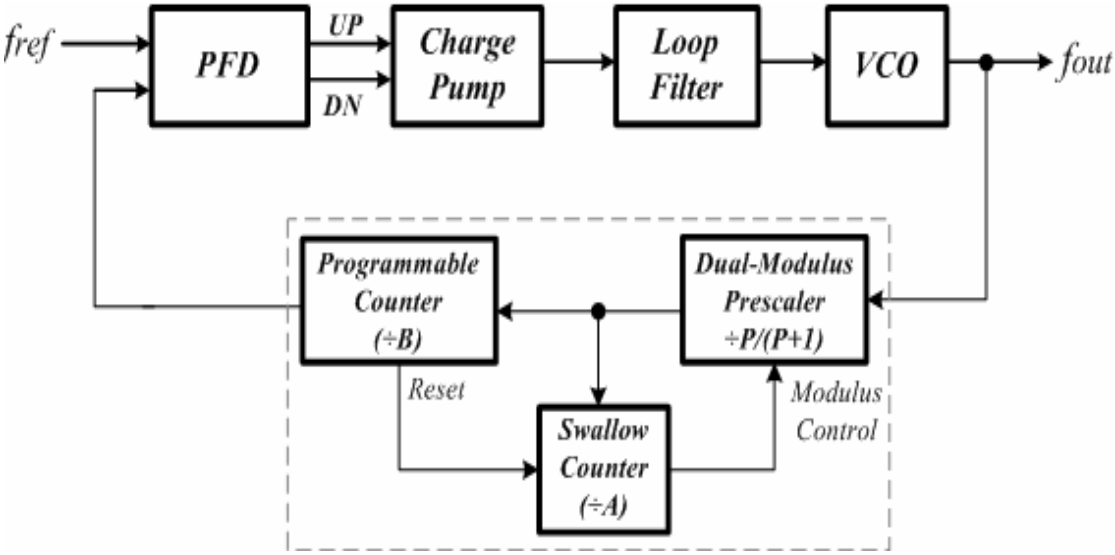


Figure 4.1 Block diagram of a PLL-based frequency synthesizer.

In the design of the frequency synthesizer, the most critical building block is the VCO, which dominates the PLL performance, such as phase noise and tuning range. The VCO is usually embedded in a PLL as a tunable frequency synthesizer to provide clean, stable, and more precise carrier signals for frequency up/down-conversion [31]. A high-frequency (HF) CMOS VCO has strict requirements in the transceivers of wireless communication systems. Low power consumption and low phase noise are the challenges in VCO designs. Typically, a VCO is usually comprised of a gain element and a resonator. The resonator determines the oscillation frequency, and when it is composed of energy-storing inductors and capacitors, it is often referred to as an LC tank. A voltage-controlled varactor diode allows the oscillation frequency of the VCO to be varied.

Recently, the demand for high-quality performances but low-cost solutions is raising in the transceivers of modern wireless communication systems [32]. Low–power operation can extend the lifetime of the battery and save money for consumers. The low power consumption can be achieved by reducing the supply voltage and/or the current in the VCO core circuit. Although the low voltage operation can relies on scaling down metal-oxide-semiconductor (MOS) threshold voltage V_T, the low voltage limits the signal amplitude, which in turn limits the signal-to-noise ratio (SNR) and degrades the VCO performance. Kwok and Luong [33] proposed a transformer-feedback oscillator, which swing the output signals dynamically above the supply voltage and below the ground potential to increase the carrier power and to lower the phase noise. This approach does not reduce the V_T but in fact it increases the effective dynamic drain-to-source voltage at a fixed DC voltage. In addition, the another challenge in designing VCOs is minimizing phase noise while maintaining smallest power consumption [34].

The low power is an important concern, but the phase noise performance must

be low enough since the most critical performance specification for an oscillator is phase noise. In a receiver, the phase noise of the LO limits the ability to detect a weak signal in the presence of a strong signal in an adjacent channel. In a transmitter, phase noise results in energy being transmitted outside of the desired band. To achieve low phase noise, we have discussed and proposed the new and efficient method to reduce the phase noise of a VCO without increasing power consumption in Chapter 3.

In this chapter, we will focus on how to design a low-power-consumption low-cost and low-phase-noise dual-band LC-VCO for WiMAX. In order to conform with Taiwan giving fresh impetus to WiMAX, we design a dual-band LC-VCO covering 2.5 GHz and 3.5 GH. The section 4.2 briefly describes the current-reused LC-VCO topology that can only operate with only half the amount of DC current compared to those of the conventional LC-VCO topology. The current-reused dual-band LC-VCO combined with an external and large resistor at the substrate node of NMOS is proposed in the section 4.3. In section 4.4, the simulated and measured results are compared.

4.2 Proposed Voltage Controlled Oscillator Architecture

Figure 4.2 shows two typical LC tank oscillators. Figure 4.2(a) uses all-NMOS cross-coupled pair to provide negative-G_M and Figure 4.2(b) employs all-PMOS cross-coupled pair. In both structures, MOS coupled pair is an active element to compensate for the losses of the inductor and the capacitor.

The phase noise of PMOS cross-coupled pair oscillator is lower than NMOS structure since the intrinsic noise of PMOS is lower than NMOS. Nevertheless, the output power of NMOS cross-coupled pair oscillator is larger than PMOS structure.

To sum up, we can use the NMOS and PMOS cross-coupled pairs that is called complementary cross-coupled pair) to provide negative G_M. There are several reasons why the complementary structure is superior to the all-NMOS structure [35].

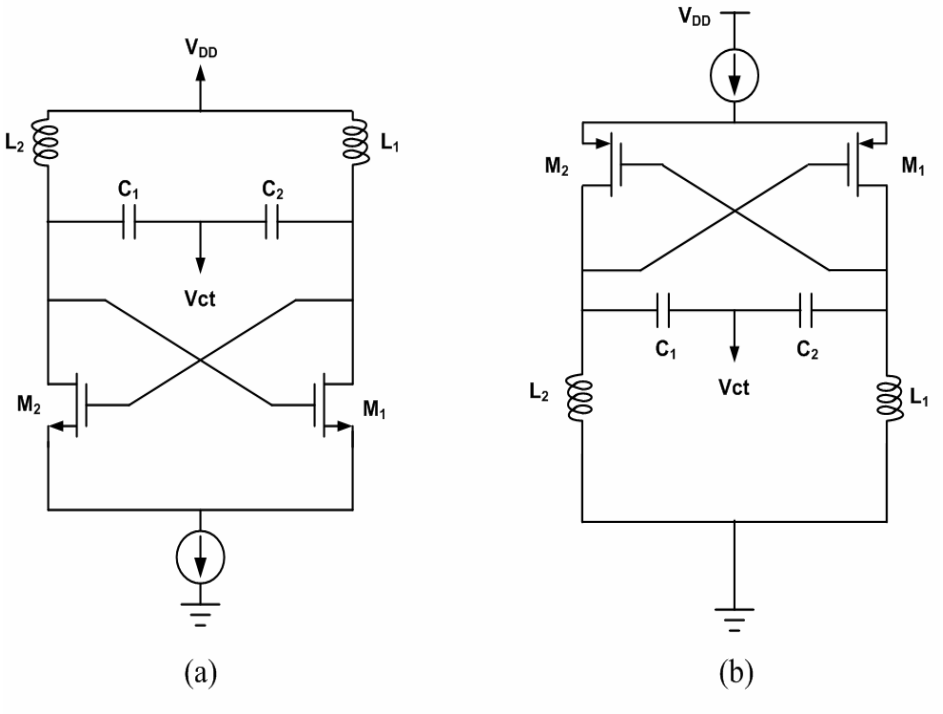


Figure 4.2 Two typical LC tank oscillator structures.

1. The complementary structure offers better rise- and fall-time symmetry. It makes less up-conversion of $1/f$ noise and other lower frequency noise sources.
2. The complementary structure offers higher transconductance for a given current, which results in a better start-up behavior.
3. The complementary structure also exhibits better noise performance for all bias points illustrated in Figure 4.3

As long as the oscillator operates in the current-limited regime, the tank voltage swing is the same for both oscillators. However if we desire to operate in the voltage-limited region, the all-NMOS structure can offer a larger voltage swing.

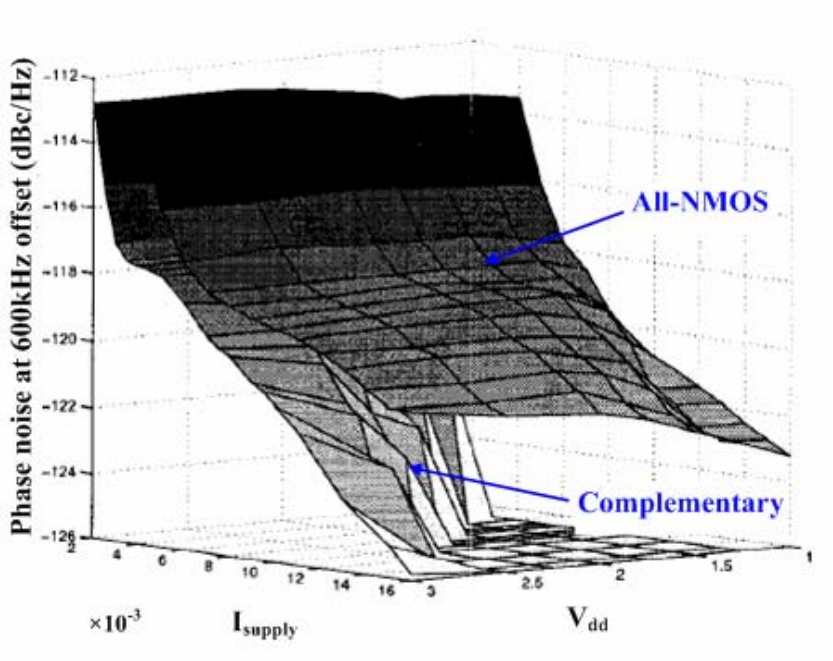


Figure 4.3 Phase noise for the complementary and All-NMOS.

Figure 4.4 illustrates the schematic of the complementary cross-coupled LC-VCO without the tail current source, which is adopted in this work. From the phase noise point of view, this topology reveals better noise performance than the one in Figure 4.3. This is due to the fact that the $1/f^3$ noise of the topology without the tail current can only originate from the flicker noise of the MOS transistor switches.

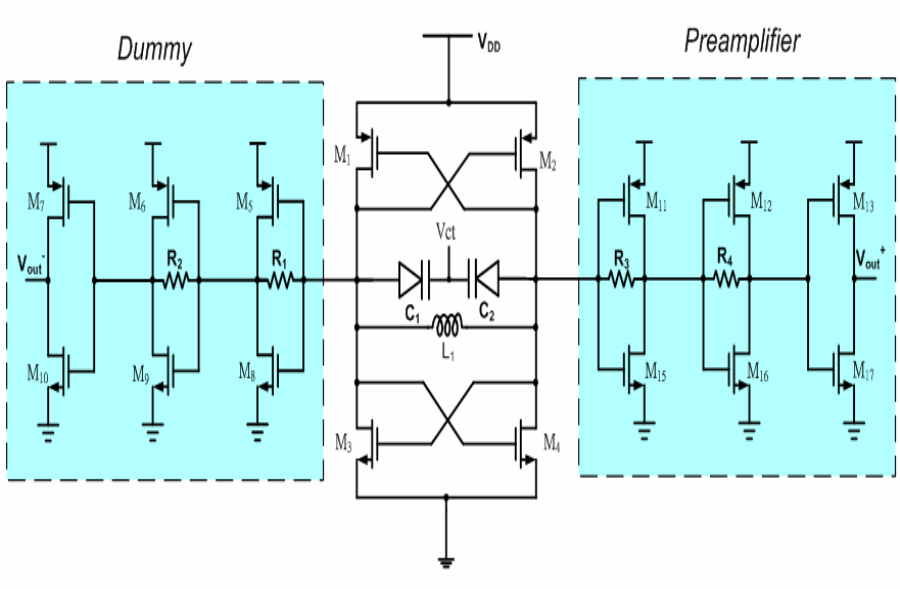


Figure 4.4 Complementary cross-coupled LC-VCO without the tail current source.

These switches are expected to feature lower flicker noise than the tail current source that dominates the $1/f^3$ noise, for two main reasons. First, the switches operate in triode region for large portions of the oscillation period; hence, they exhibit lower current flicker noise than the tail transistor that continuously operates in saturation. Second, switched MOS transistors are known to have lower flicker noise than transistors biased in the stationary condition [36]. Nevertheless, the main drawback of this topology is a higher sensitivity of the frequency to the voltage supply (frequency pushing). This effect can be alleviated by using a supply voltage regulator.

Here, we propose the current-reused LC-VCO that uses both NMOS and PMOS transistor in cross-coupled pair as a negative conductance generator to achieve low power consumption easily. As shown in Figure 4.5, the series stacking of NMOS and PMOS allows the supply current to be reduced by half compared to that of the conventional LC-VCO while providing the same negative conductance. This topology is not only low-power-consumption but also low-cost since it only used one inductor and two MOS transistors, but the conventional LC-VCO used two inductors and four MOS transistors.

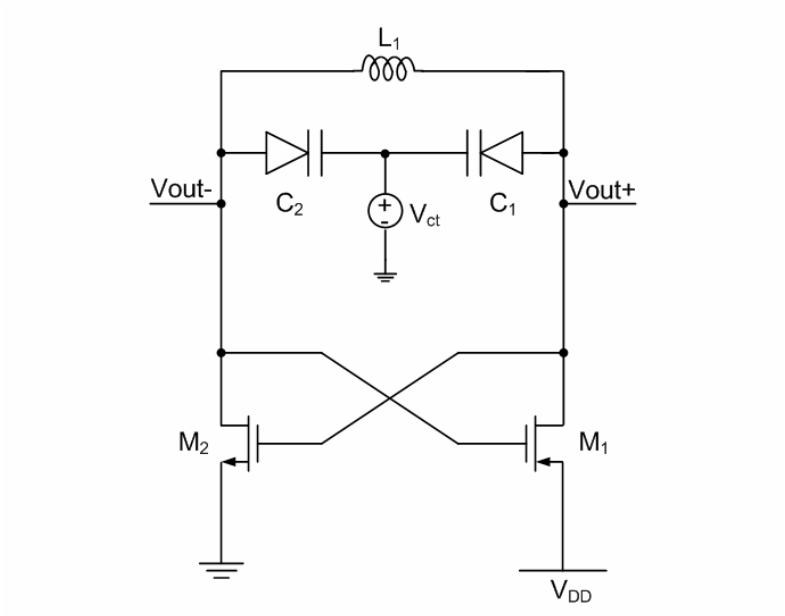


Figure 4.5 The current-reused LC-VCO.

The conventional and current-reused LC-VCOs operate at 3.4GHz to 3.7GHz as shown in Figure 4.6 and the tuning sensitivity (K_{VCO}) of both topologies are shown in Figure 4.7.

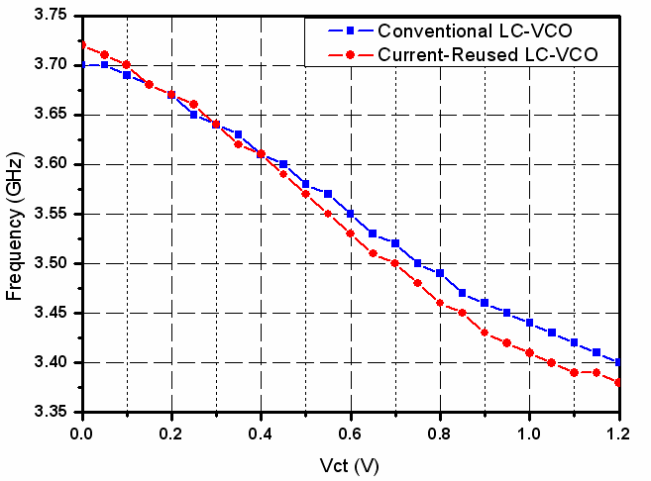


Figure 4.6 Simulated tuning range of the conventional and proposed LC-VCO at 3.5 GHz.

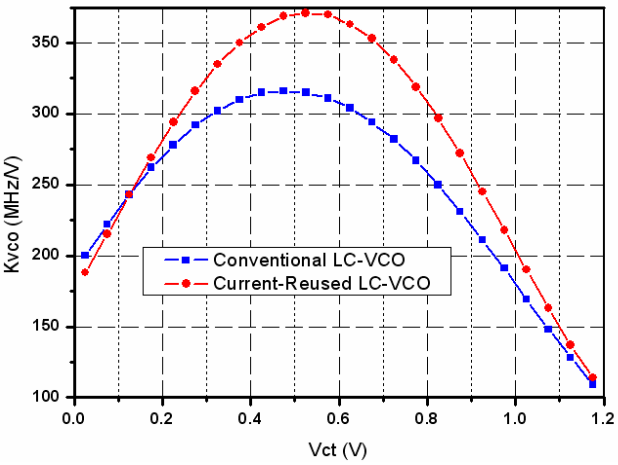


Figure 4.7 Simulated K_{VCO} of the conventional and proposed LC-VCO at 3.5 GHz.

Figure 4.8 shows simulated phase noise for both the conventional and current-reused LC-VCOs which operate at 3.4GHz to 3.7GHz. The simulated values for the conventional LC-VCO and current-reused LC-VCO -119 dBc/Hz and -117 dBc/HZ, respectively, at 1MHz offset frequency. In addition, the power consumption of the

conventional topology and the current-reused topology are 1.973mW and 0.996mW, respectively. Figure 4.9 shows the output power of conventional and current-reused LC-VCO. It is found that the minimum values of output power are -1.13 dBm and -2.11 dBm, respectively, in the conventional topology and the current-reused topology. Therefore, we know that the phase noise and the output power performances of conventional LC-VCO are better than current-reused LC-VCO, but the power consumption of current-reused topology is lower than the conventional topology.

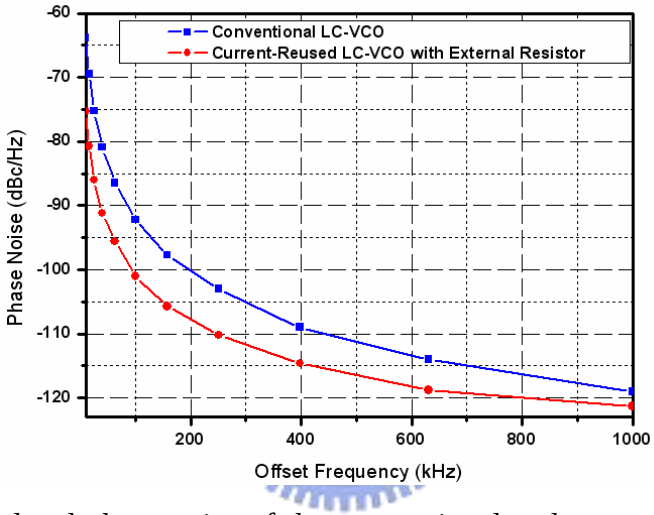


Figure 4.8 Simulated phase noise of the conventional and proposed LC-VCO at 3.5 GHz.

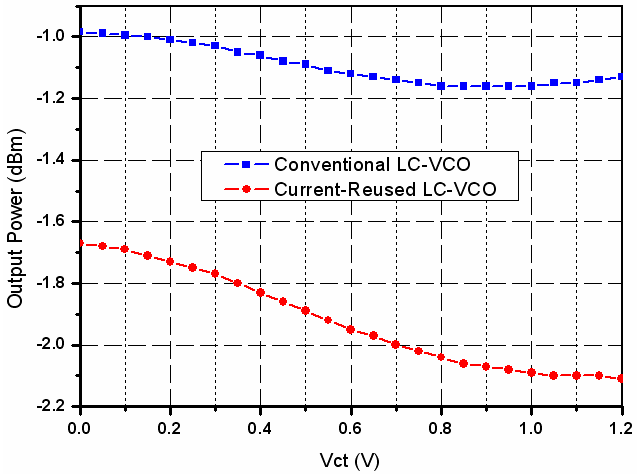


Figure 4.9 Simulated output power of the conventional and proposed LC-VCO at 3.5 GHz.

Although the proposed topology can operate with only half amount of DC current compared to that of the conventional topology, the phase noise of current-reused topology is higher than conventional topology. In the modern wireless communication systems, the low power is an important concern, but the phase noise performance must be low enough since the most critical performance specification for an oscillator is phase noise. Hence, the current-reused LC-VCO combines with the Chapter 3 proposed that is adding an external and large resistor, which is located between the substrate node and the source nod of NMOS transistor. As shown in Figure 4.10, the current-reused LC-VCO combined with the external and large resistor Rbx is proposed.

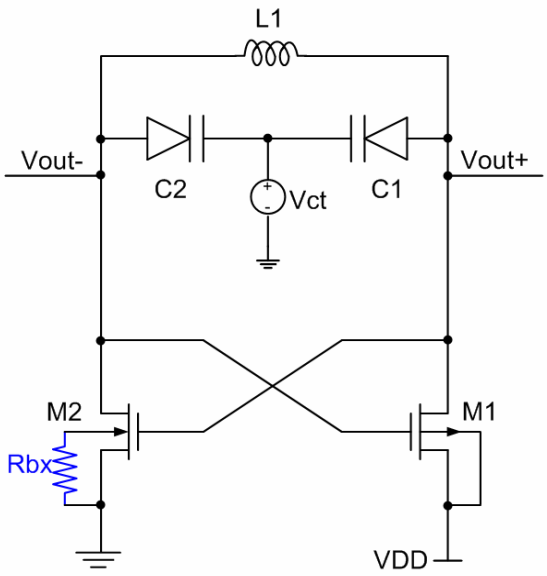


Figure 4.10 Current-reused LC-VCO combined with the external resistor Rbx.

The conventional, current-reused, and proposed LC-VCOs operate at 3.4GHz to 3.7GHz as shown in Figure 4.11. Figure 4.12 shows the simulated tuning sensitivity (K_{VCO}) for conventional, current-reused, and proposed LC-VCOs which operate at 3.5GHz.

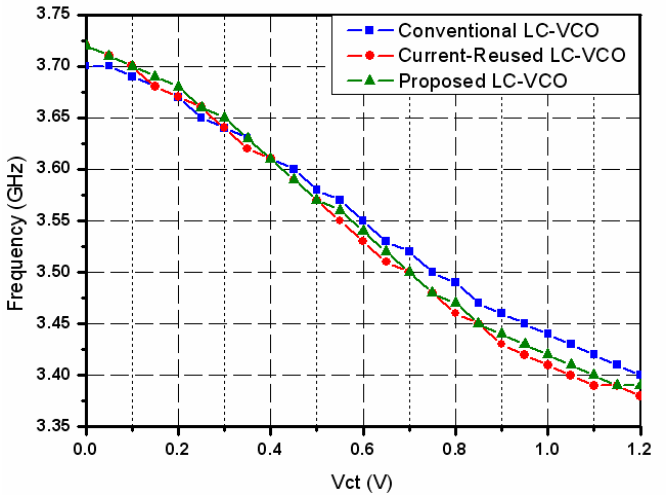


Figure 4.11 Simulated tuning range of the conventional, current-reused, and proposed LC-VCO at 3.5 GHz.

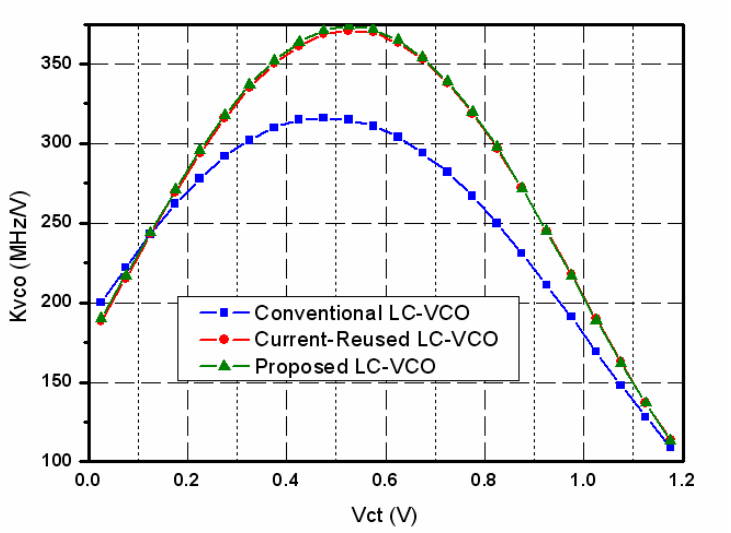


Figure 4.12 Simulated K_{VCO} of the conventional, current-reused, and proposed LC-VCO at 3.5 GHz.

Figure 4.13 shows simulated phase noise for the conventional current-reused and the proposed LC-VCOs which operate at 3.4GHz to 3.7GHz. The simulated values for the conventional, current-reused, and proposed LC-VCOs are -119 dBc/Hz, -117 dBc/HZ, and -121 dBc/Hz at 1MHz offset frequency. In addition, the power consumption of the conventional topology is 1.973mW, but the current-reused and the proposed topologies are both only 0.996mW.

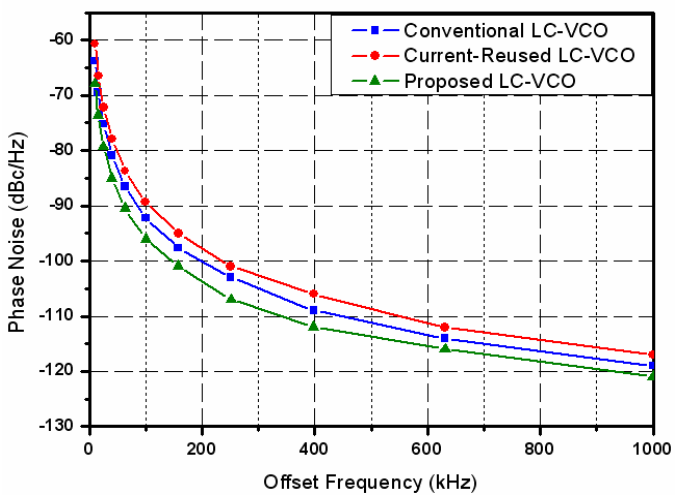


Figure 4.13 Simulated phase noise of the conventional, current-reused, and proposed LC-VCO at 3.5 GHz.

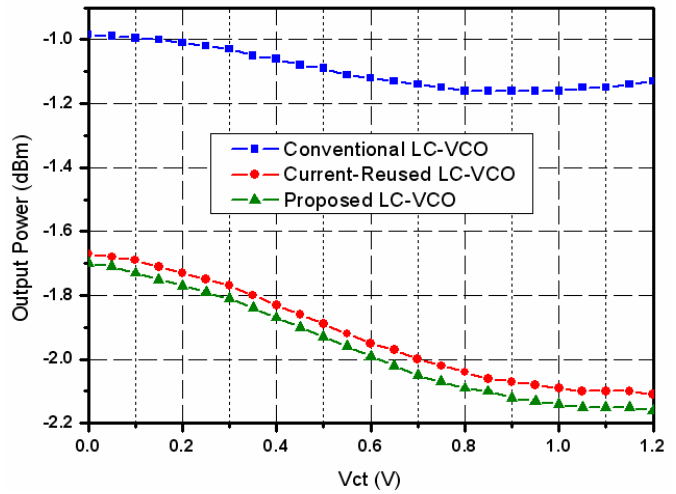


Figure 4.14 Simulated output power of the conventional, current-reused, and proposed LC-VCO at 3.5 GHz.

Figure 4.14 shows the output power of current-reused and proposed LC-VCO. It is found that the minimum values of output power are -1.13 dBm, -2.11 dBm and -2.16 dBm in the conventional, current-reused, and proposed topologies. Therefore, we know that the phase noise and the output power performances of conventional LC-VCO are better than current-reused and proposed LC-VCOs, but the power

consumption of current-reused and proposed topologies is lower than the conventional topology.

From the simulated, the current-reused LC-VCO which combines with the Chapter 3 proposed that is adding an external and large resistor, which is located between the substrate node and the source nod of NMOS transistor can achieve low phase noise performance without increasing power consumption. Although the output power of proposed LC-VCO is the least less than the others, its still can be allow applying wireless communication systems. In order to achieve the low-power and low-phase-noise performance, we choose the current-reused LC-VCO combined with the external resistor to implement the dual-band LC-VCO. This proposed topology is not only to achieve low-power and low-phase-noise easily but also realizing to low-cost.

4.3 A Dual-Band LC-VCO for 2.5 GHz/3.5 GHz WiMAX

As wireless applications proliferate, demands for low-cost wireless communication which can support multiple bands and multiple standards with minimal hardware implementations are rapidly increasing [37]. In response to this, multiband terminals using multiple RF transceivers have been reported. This, however, increase die area or chip count in a radio, which, in turn, increases cost and complexity of radios. Another of the major issues in a dual-band transceiver is the implementation of a dual-band LC-VCO. The most popular implementation method of a dual-band LC-VCO is to use switching devices in the tank to change either capacitance [38] or inductance [39]. The resistance of the switching devices, however, is likely to cause the degradation of the tank quality factor (Q) and, consequently, the

oscillator's phase-noise. A wide tuning range LC-VCO can be another choice to cover the dual bands [40], but the required varactors with wide tuning range are not usually available in a standard process and the relatively large LC-VCO gain (K_{VCO}) can easily lead to severe phase-noise degradation [41]. A set of multiple LC-VCOs can support multiple bands [42], however, this could be unaffordable in portable devices due to the overwhelming circuit overheads. In spite of these endeavors, the design of integrated dual band LC-VCOs still poses many challenges.

In general, the design of dual band LC-tank voltage controlled oscillator (VCO) still uses the complementary cross-coupled pair topology. Figure 4.15 shows the Simplified equivalent circuit of dual band complementary cross-coupled pair LC-VCO. This topology usually uses the switched resonator concept to realize the dual-band LC-VCO. In addition, the switched resonator concept also can reduce the degradation of phase noise.

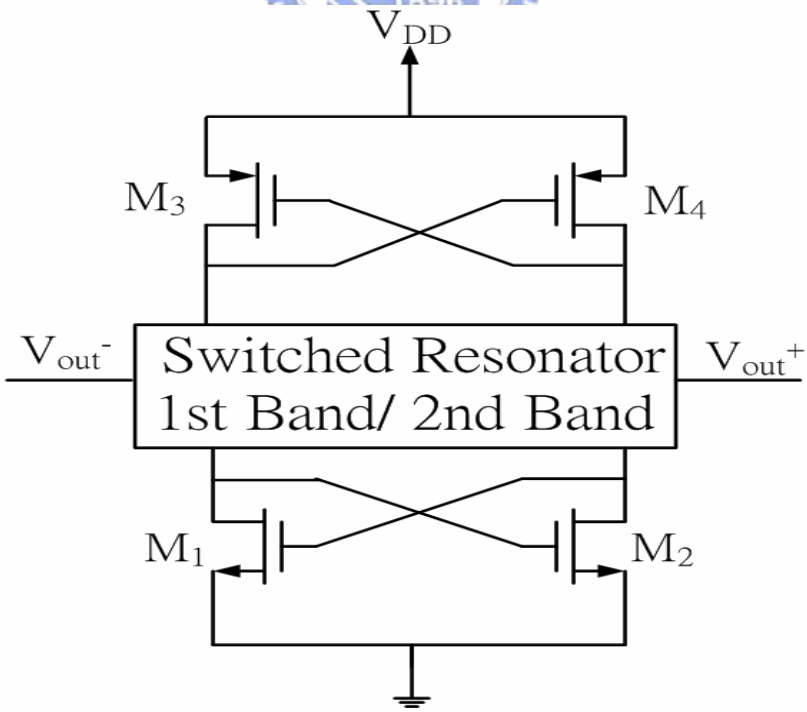


Figure 4.15 Simplified equivalent circuit of dual band LC-VCO.

Figure 4.16 shows the conventional complementary cross-coupled pair dual band LC-VCO [43-44]. The topology consists of two identical half circuits composed of switching transistors (M_1、M_2、M_3、M_4), band switching transistors (M_5、M_6), inductors (L_1、L_2、L_3、L_4), and varactors (C_1、C_2). A signal feeds back from the drain of M_1、M_3 (M_2、M_4) to the gate of M_2、M_4 (M_1、M_3) which acts as an active buffer, and vice versa.

In the design of radio frequency (RF) circuits, the demands for low-cost and low-power-consumption are important issues. Although this dual band LC-VCO has excellent phase noise performance, its power consumption is higher than NMOS or PMOS cross-coupled LC-VCO and it also uses over three inductors to achieve dual operation-frequency. This topology leads to the cost go up since the area of RF circuit is increased since the area of an inductor is large in the IC layout.

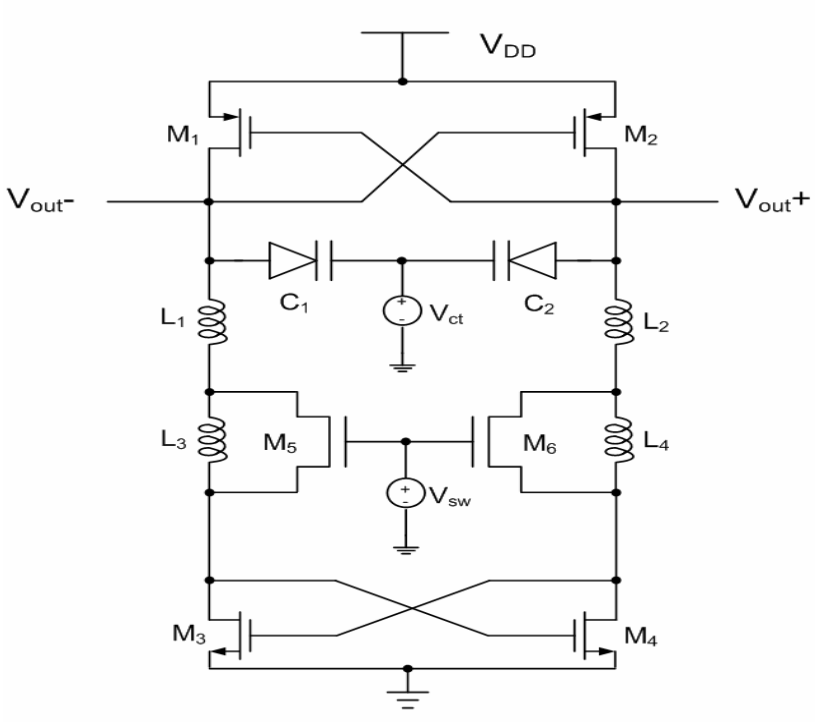


Figure 4.16 The conventional complementary cross-coupled pair dual band LC-VCO.

At the last section, we choose the current-reused LC-VCO to implement the LC-VCO since this topology can achieve low-power and low-cost. If the dual-band LC-VCO can use current-reused topology, it also can achieve low-cost and low-power-consumption easily. Therefore, the Figure 4.16 can be simplified by Figure 4.17 which is called current-reused dual-band LC-VCO. The current-reused dual-band LC-VCO that uses both NMOS and PMOS transistor in cross-coupled pair as a negative conductance generator can achieve low-power-consumption and low-cost easily. Its theorem of circuit is as similar as last section, but the current-reused dual-band LC-VCO has the same issue that is the phase-noise performance must be worse than conventional topology.

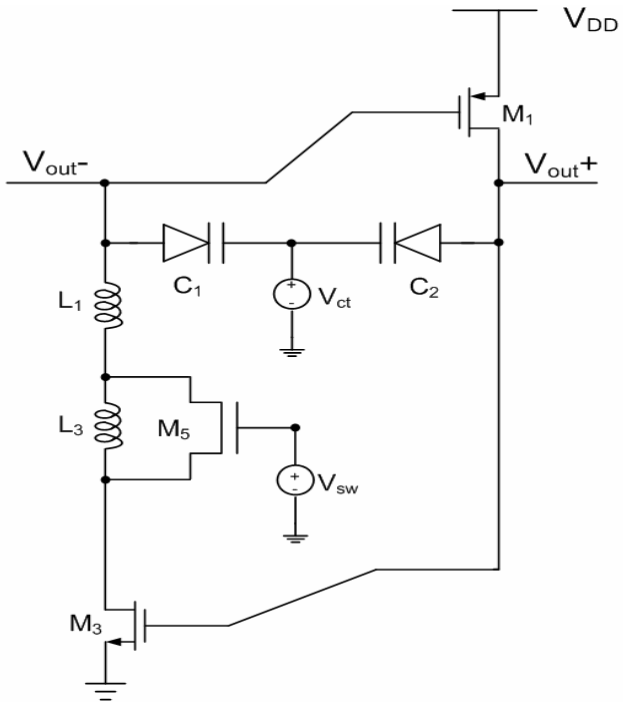


Figure 4.17 The current-reused dual-band LC-VCO.

Therefore, we use the same method that is adding an external and large resistor, which is located between the substrate node and the source nod of NMOS transistor to reducing the phase noise of the current-reused dual-band LC-VCO. The proposed dual-band LC-VCO is shown in Figure 4.18. We choose the 2.5 GHz and 3.5 GHz

operating frequency to design the dual-band LC-VCO in order to conform to Taiwan giving fresh impetus to WiMAX (Worldwide Interoperability for Microwave Access). In addition, we add the C_3 and C_4 which shunt between the drain node and the source node of NMOS and PMOS transistors to provide negative conductance [45]. The value of negative conductance is

$$G_N = \frac{\omega^2 Cgs(C_N + Cgd)}{gm} \tag{4-1}$$

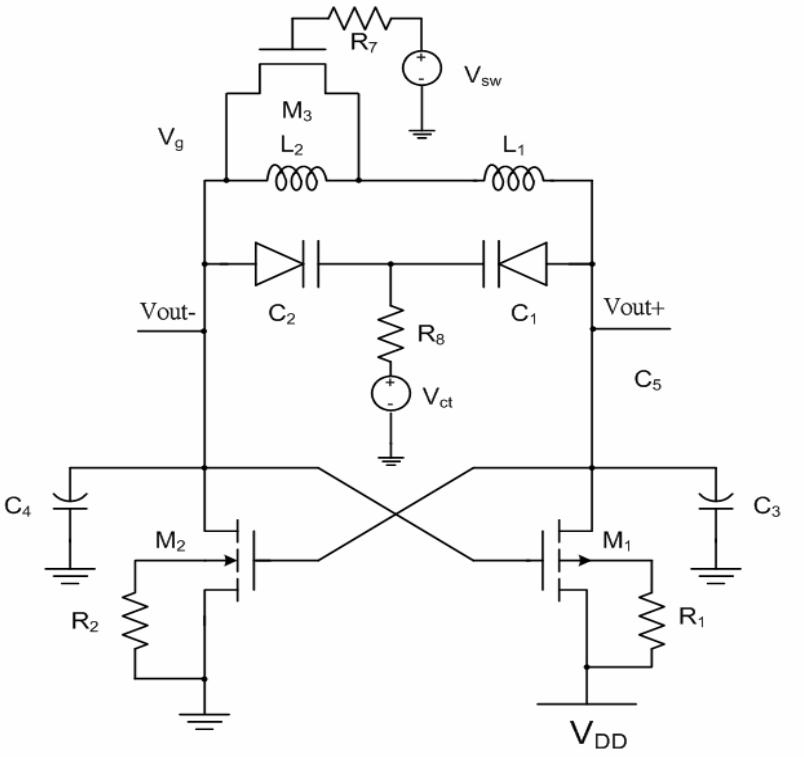


Figure 4.18 The proposed dual-band LC-VCO.

The negative conductance can reduce the phase noise of LC-VCO since it not only reduces the loss but also increases the quality factor, Q, in the inductance. The phase noise is proportional to Q. The equivalent circuit of LC-Tank is shown in Figure 4.19 after shunting the C_3 and C_4.

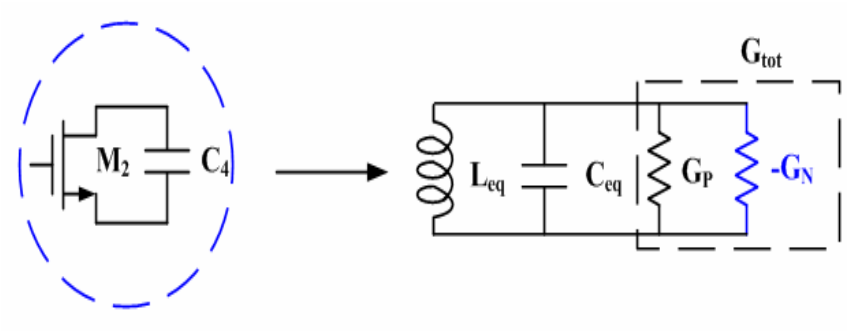


Figure 4.19 The equivalent circuit of LC-Tank after shunting the C_3 and C_4.

When the switch-transistors of conventional, current-reused, and proposed LC-VCOs are off, the LC-VCOs both operate at lower band frequency. The lower band frequency is 2.5GHz and tuning range is 2.5 GHz to 2.69 GHz as shown in Figure 4.20. We also can know that the tuning range of proposed dual-band LC-VCO is the maximum and it operates at 2.49 GHz to 2.72 GHz from Figure 4.20. In addition, Figure 4.21 shows the simulated tuning sensitivity (K_{VCO}) for the conventional, current-reused, and current-reused LC-VCOs. From Figure 4.21, we can see that the K_{VCO} of current-reused and proposed dual-band LC-VCOs are almost the same.

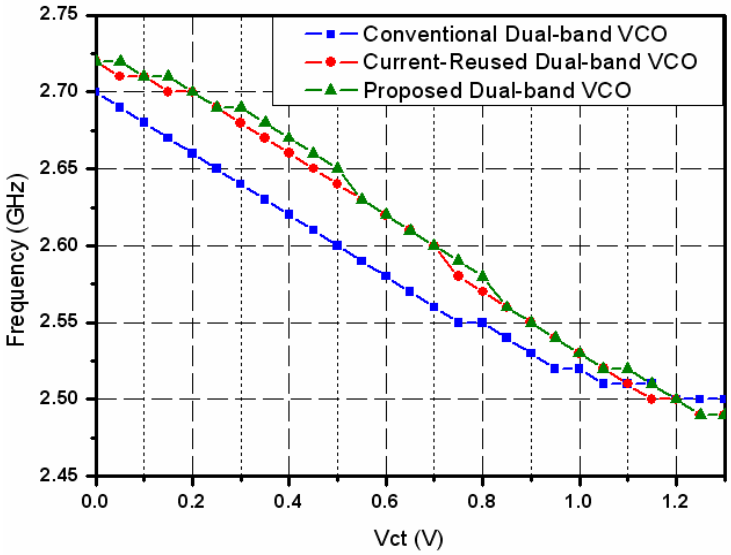


Figure 4.20 Simulated tuning range of the conventional and current-reused LC-VCO at 2.5 GHz.

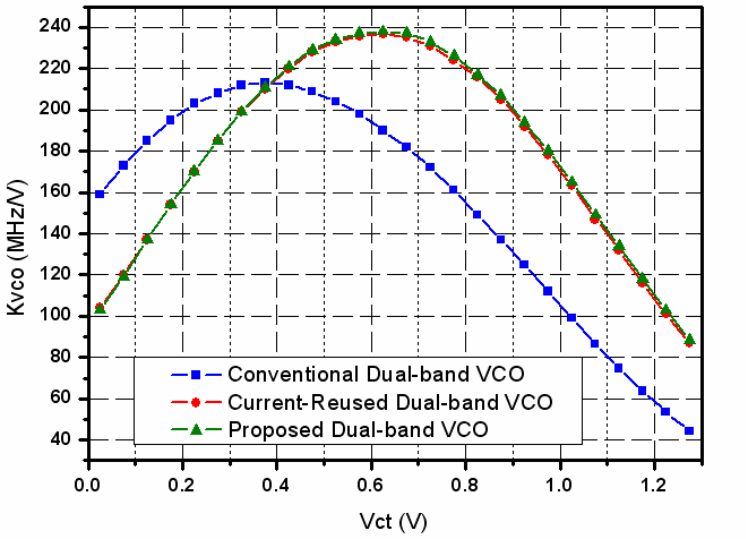


Figure 4.21 Simulated K_{VCO} of the conventional and current-reused LC-VCO at 2.5 GHz.

In the Figure 4.22, the simulated result shows phase noise for the conventional, current-reused, and the proposed LC-VCOs which operate at 2.5 GHz to 2.69 GHz. The simulated values for the conventional, current-reused, and proposed LC-VCOs are -118 dBc/Hz, -117 dBc/HZ, and -120 dBc/Hz at 1MHz offset frequency. We also can know that the phase noise of proposed dual-band LC-VCO reduction is about -3 dB compared to the current-reused dual-band LC-VCO. In addition, the power consumption of the conventional topology is 4.342mW, but current-reused and proposed topologies are only 1.456mW, respectively. Figure 4.23 shows the output power of conventional and current-reused LC-VCOs. It is found that the minimum values of output power are -0.52 dBm, -1.39 dBm, and -1.44 dBm in the conventional, current-reused, and the proposed topologies.

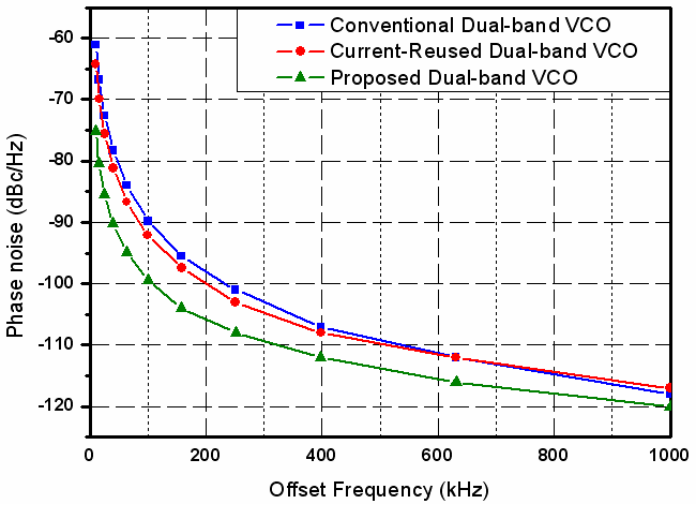


Figure 4.22 Simulated phase noise of the conventional and current-reused LC-VCO at 2.5 GHz.

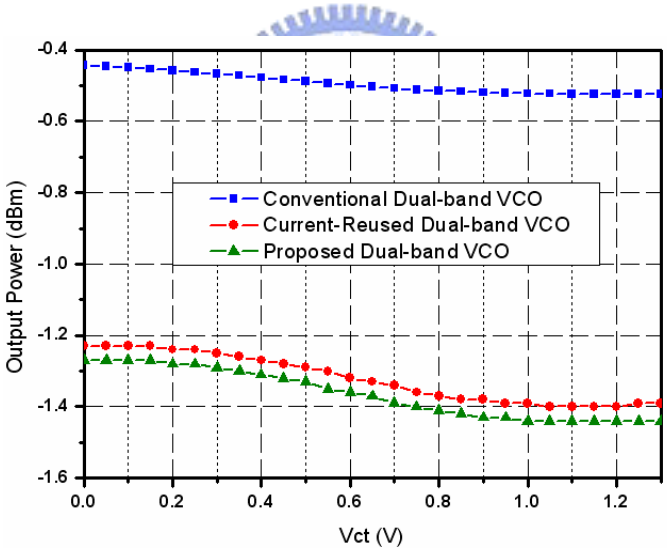


Figure 4.23 Simulated output power of the conventional and current-reused LC-VCO at 2.5 GHz.

In the other hand, when the switch-transistors of conventional, current-reused, and proposed LC-VCOs are on, the LC-VCOs both operate at higher frequency band. The higher frequency band is 3.7 GHz and tuning range is 3.4 GHz to 3.7 GHz as shown in Figure 4.24. We also can know that the tuning range of the conventional

LC-VCO is 3.4 GHz to 3.7 GHz and the proposed and current-reused topologies are wider. The two topologies operate at 3.38 GHz to 3.71 GHz. In addition, Figure 4.25 shows the simulated tuning sensitivity (K_{VCO}) for the conventional, current-reused, and proposed LC-VCOs. From Figure 4.25, we can see that the K_{VCO} of current-reused and proposed dual-band LC-VCOs are almost the same. The maximum value of K_{VCO} is about 375 MHz/V in the current-reused and the proposed LC-VCOs.

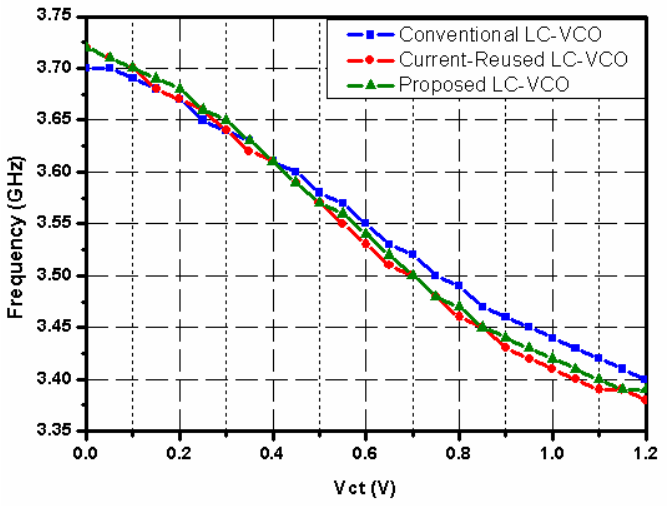


Figure 4.24 Simulated tuning range of the conventional and current-reused LC-VCO at 3.5 GHz.

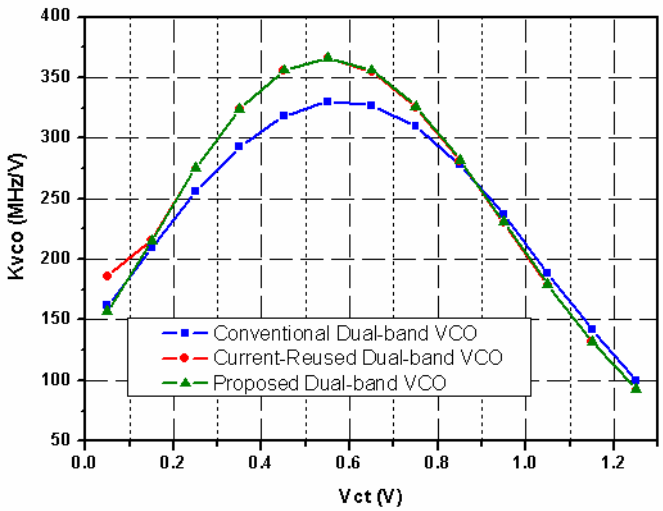


Figure 4.25 Simulated K_{VCO} of the conventional and current-reused LC-VCO at 3.5 GHz.

In the Figure 4.26, the simulated result shows phase noise for the conventional, current-reused, and the proposed LC-VCOs which operate at 3.4 GHz to 3.7 GHz. The simulated values for the conventional, current-reused, and proposed LC-VCOs about are -115 dBc/Hz, -114 dBc/HZ, and -117 dBc/Hz at 1MHz offset frequency. We also can know that the phase noise of proposed dual-band LC-VCO reduction is about -3 dB compared to the current-reused dual-band LC-VCO. In addition, the power consumption of the conventional topology is 4.342mW, but current-reused and proposed topologies are only 1.456mW. We can know the result the same as the single-band which reduce the phase noise of current-reused VCO effectively without increase the power consumption. Figure 4.27 shows the output power of conventional and current-reused LC-VCOs. It is found that the minimum values of output power are -1.03 dBm, -2.06 dBm, and -2.07 dBm in the conventional, current-reused, and the proposed topologies.

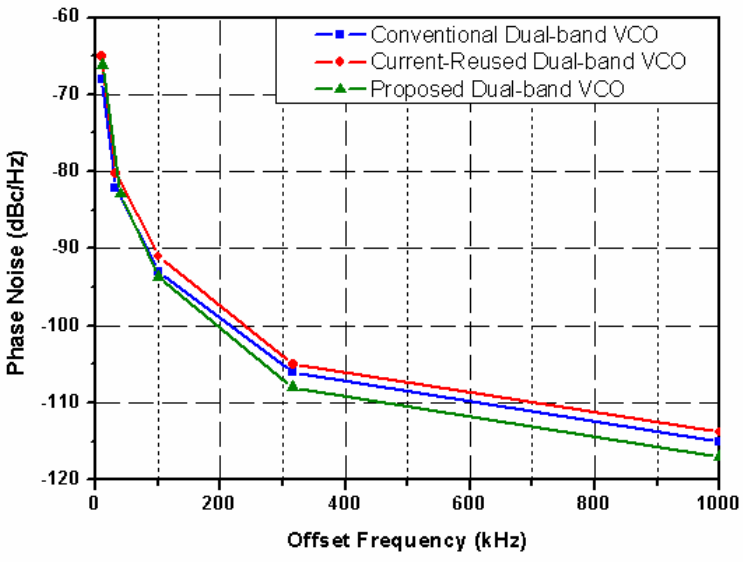


Figure 4.26 Simulated phase noise of the conventional and current-reused LC-VCO at 3.5 GHz.

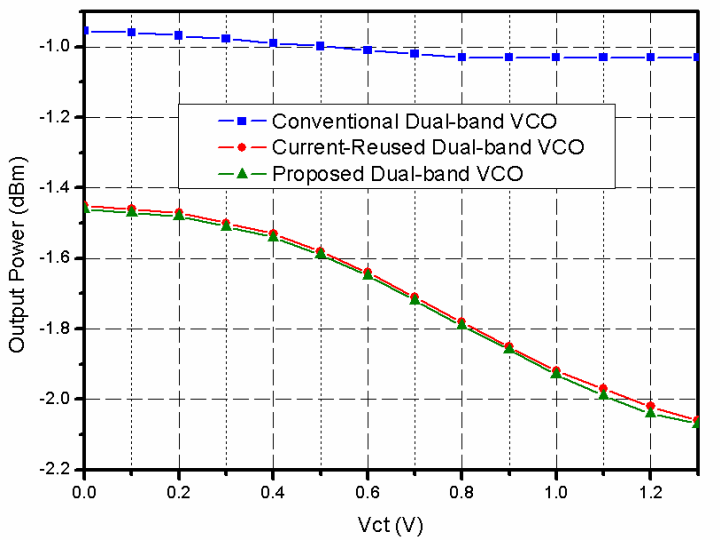


Figure 4.27 Simulated output power noise of the conventional and current-reused LC-VCO at 3.5 GHz.

Therefore, we know that the output power performances of the conventional LC-VCO are better than current-reused and proposed topology, but the power consumption of proposed and current-reused topology is lower than the conventional topology. In addition, the phase noise of proposed LC-VCO is lower than the conventional LC-VCO. The current reused topology combines with an external and large resistor has lower phase noise power consumption, although its output power is lower than the conventional topology. Finally, we choose the proposed topology to implement a low-power low-phase-noise dual-band LC-VCO.

The power supply is added externally in the design the LC-VCO, so we have to bond wire to the print circuit board (PCB). Therefore, we must consider the pad-effect and bond-wire-effect which are provided by national chip implementation center (CIC) as shown in Figure 4.28and Figure 4.29, respectively, to avoid the frequency shifting and the higher phase noise issues. In addition, we also consider the layout effect to take the long layout line as shown in Figure 4.30. Running EM

simulation by advanced design system (ADS) Momentum and obtain the layout effect model.

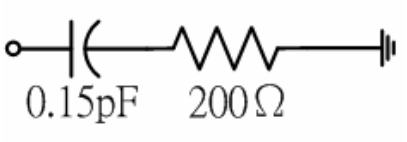


Figure 4.28 The equivalent model of pad-effect.

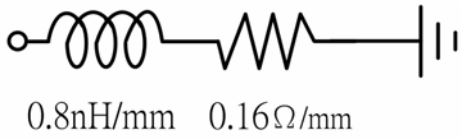


Figure 4.29 The equivalent model of bond-wire-effect.

Figure 4.30 The equivalent circuit of parasitic effect of a wire.

When the LC-VCO is measured, the output of the circuit is terminated with 50 Ω, we also must design a buffer to connect with the output node of LC-VCO. The complete proposed dual-band LC-VCO circuit is shown as Figure 4.31.

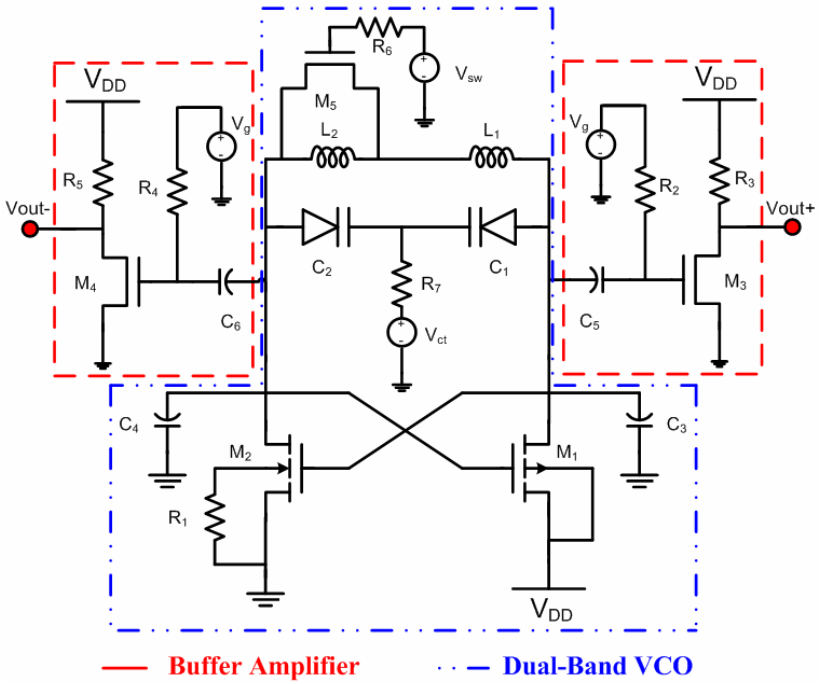


Figure 4.31 The complete circuits of proposed LC-VCO.

4.4 Simulated and Measured Results

In this section, the measurement results of the proposed dual-band LC-VCO are presented. The chip layout and microphotograph of the proposed LC-VCO are shown, respectively, in Fig. 4.32 and Figure. 4.33. The LC-VCO is fabricated in TSMC 0.18-μm 1P6M CMOS process. Its die area including pads is 0.64×0.96 mm^2.

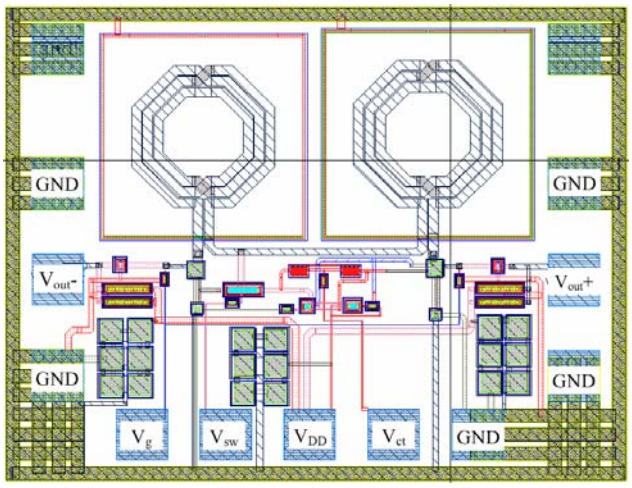


Figure 4.32 The chip layout of proposed LC-VCO.

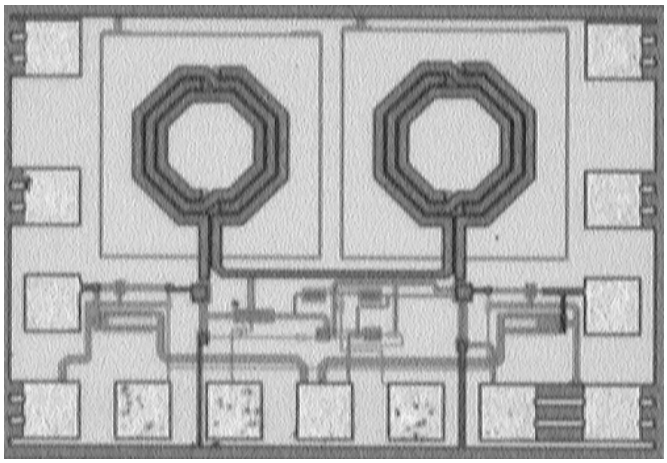


Figure 4.33 The Microphotograph of proposed LC-VCO.

The LC-VCO chip was measured by using on-wafer probing, but the power supply is added externally. Hence, the chip was directly mounted on FR4 PCB and the Fig. 4.34 shows the PCB layout. Finally, Fig. 4.35 shows the test board with chip mounted on FR4 PCB. The DC power supplier provides 1.3 V DC source to LC-VCO in measurement. The chip drew a total 2.4 mA and 2.8 mA DC current from the 1.3 V supply voltage at operating frequency 2.5 GHz and 3.5 GHz, respectively. The power consumption of core circuit is 3.12 mW and 3.64 mW, respectively, at 2.5 GHz and 3.5GHz in the proposed LC-VCO.

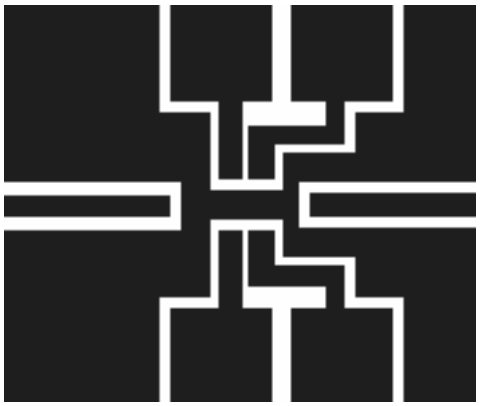


Figure 4.34 The PCB layout.

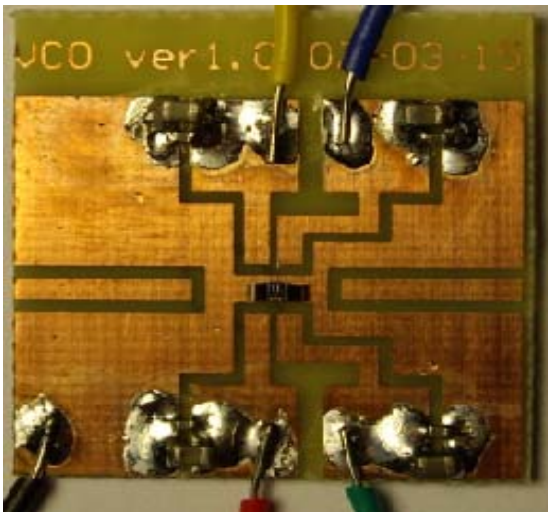


Figure 4.35 Chip bonded to the PCB.

The simulated and measured results of tuning range at 2.5 GHz are depicted as shown in Figure 4.36. From Figure 4.36, although the frequency dropped about 30 MHz, the operating frequency still covered 2.5 GHz. In addition, the tuning range performance of proposed LC-VCO is excellent well. The tuning range is 2.26 GHz to 2.67 GHz at 2.5 GHz band.

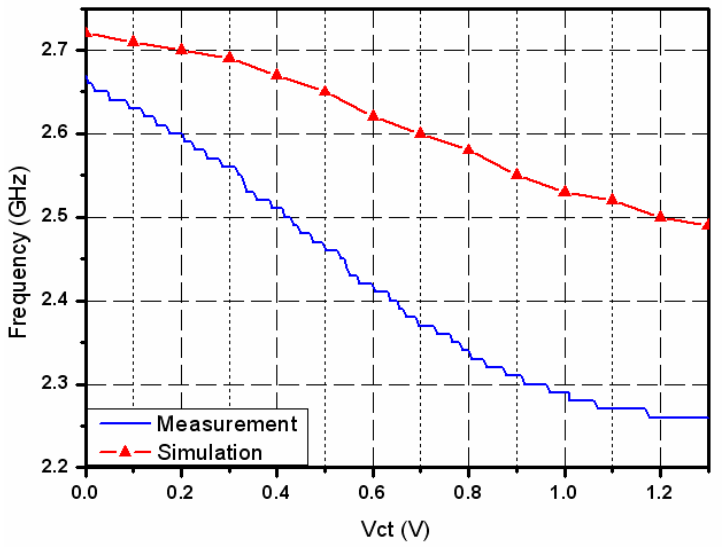


Figure 4.36 Measured and simulated tuning range of proposed VC0 at 2.5 GHz.

As shown in Figure 4.37, the simulated and measured results of output power at 2.5 GHz are depicted. The measured result shows the proposed LC-VCO output power with minimum values of -5.69 dBm at 2.5 GHz band. In addition, the measured output spectrum of the proposed LC-VCO at 2.5 GHz is shown in Figure 4.38. The value of output spectrum of the LC-VCO is -5.4 dBm at 2.5GHz. The simulated and measured results of phase noise at 2.5 GHz are depicted as shown in Figure 4.39. From Figure 4.39, the measured phase noise of the proposed LC-VCO for low band is -121 dBc/Hz at 1 MHz offset frequency from 2.5 GHz carrier. In addition, the measured phase noise almost matched with simulated result.

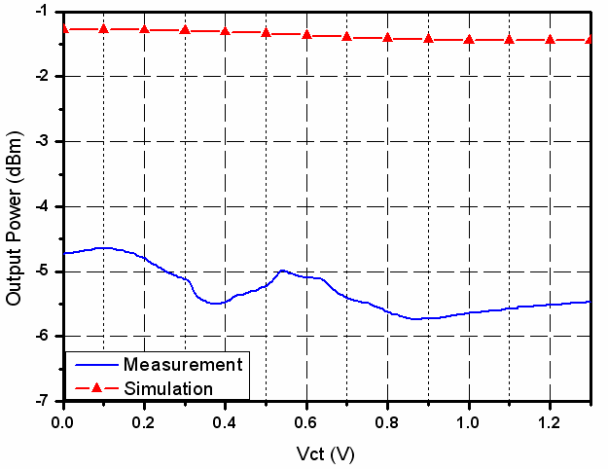


Figure 4.37 Measured and simulated output power of proposed VC0 at 2.5 GHz band.

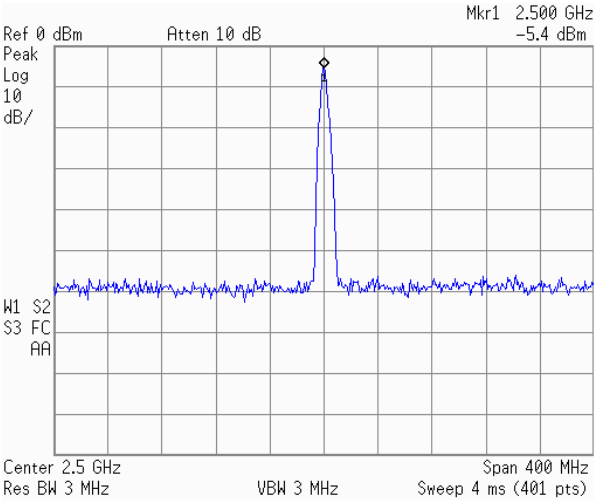


Figure 4.38 Measured output spectrum of proposed LC-VCO at 2.5 GHz.

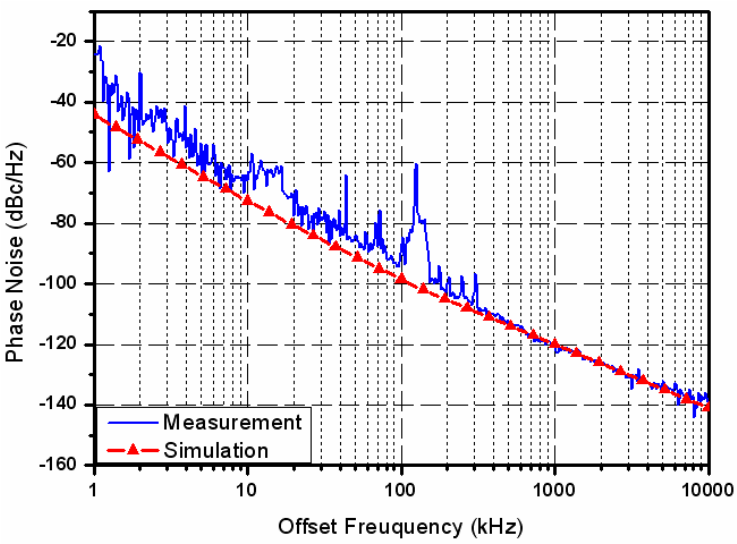


Figure 4.39 Measured and simulated phase noise of proposed VC0 at 2.5 GHz.

The simulated and measured results of tuning range at 3.5 GHz are depicted as shown in Figure 4.40. From Figure 4.40, the measured tuning range of the proposed LC-VCO is 3.09 GHz to 3.79 GHz at 3.5 GHz band. In addition, the tuning range performance of proposed LC-VCO is excellent well.

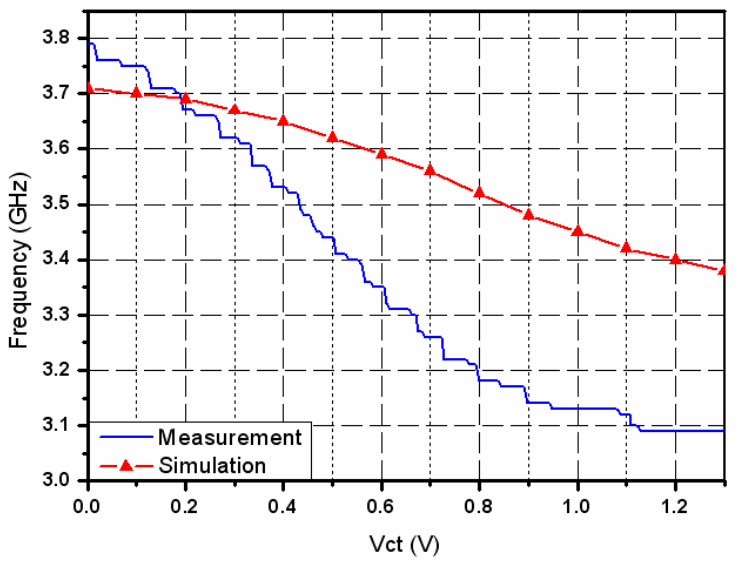


Figure 4.40 Measured and simulated tuning range of proposed VC0 at 3.5 GHz.

As shown in Figure 4.41, the simulated and measured results of output power at 3.5 GHz are depicted. The measured result shows the proposed LC-VCO output power with minimum values of -13.68 dBm at 3.5 GHz band. In addition, the measured output spectrum of the proposed LC-VCO at 3.5 GHz is shown in Figure 4.42. The value of output spectrum of the LC-VCO is -8.78 dBm at 3.5GHz. The simulated and measured results of phase noise at 3.5 GHz are depicted as shown in Figure 4.43. From Figure 4.43, the measured phase noise of the proposed LC-VCO for low band is -117 dBc/Hz at 1 MHz offset frequency from 3.5 GHz carrier. In addition, the measured phase noise almost matched with simulated result.

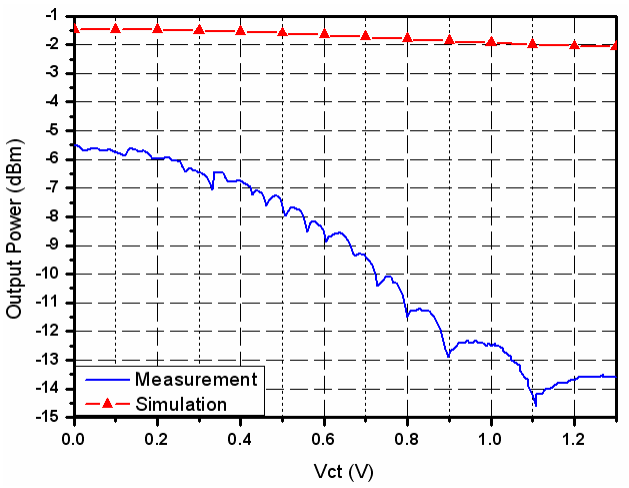


Figure 4.41 Measured and simulated output power of proposed VC0 at 3.5 GHz.

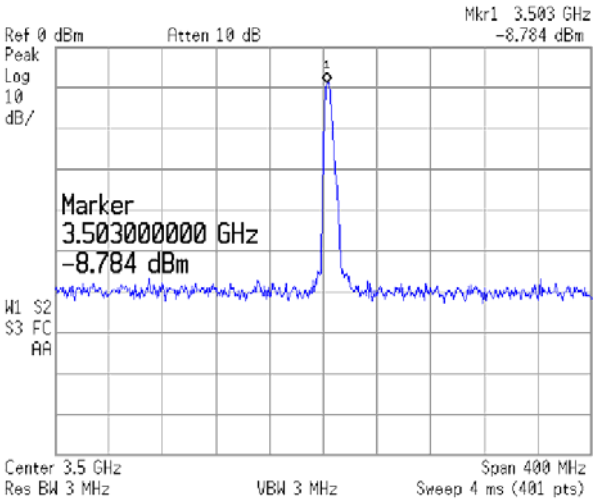


Figure 4.42 Measured output spectrum of proposed LC-VCO at 3.5 GHz.

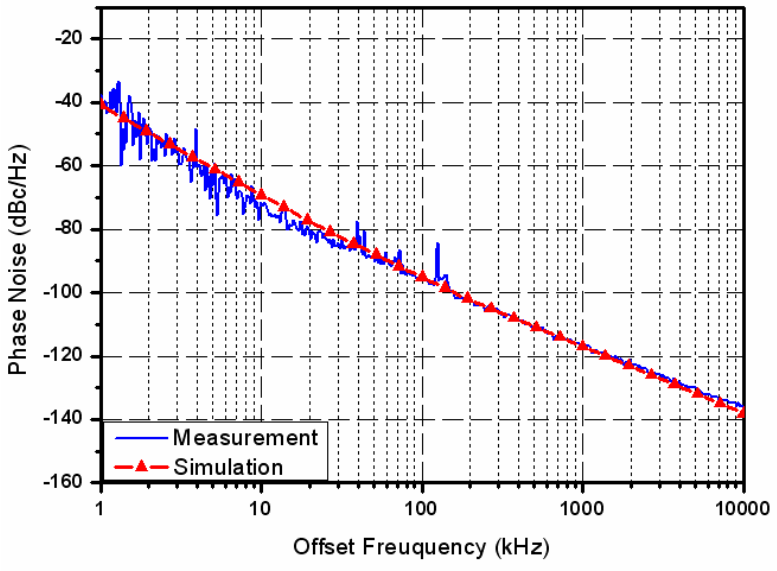


Figure 4.43 Measured and simulated phase noise of proposed VC0 at 3.5 GHz.

The figure of merit (FoM) of a VCO is defined (4) by

$$FOM = L\{\Delta f\} + 10 \times \log\left(\frac{P_{DC}}{1mW}\right) - 20 \times \log\left(\frac{f_0}{\Delta f}\right) \qquad (4\text{-}2)$$

where f_0 is the oscillating frequency, Δf is the offset frequency, $L\{\Delta f\}$ is the measured phase noise at Δf, P_{DC} is the DC power consumption of VCOs in mW. With (4-1), FoMs of the proposed LC-VCO are evaluated and are equal to -184 dBc/Hz and -183 dBc/Hz at 2.5 GHz and 3.5 GHz, respectively at 1 MHz offset frequency. To make a comparison, Table I summarizes the measured PN, f_0, power and FoM of the proposed LC-VCO and other published results. Table 4.1 shows that our LC-VCO has the lowest power consumption with nearly equal performance of FoM compared with the others. [43] has lower PN because of lower frequency.

TABLE 4.1

COMPARED THE PROPOSED LC-VCO WITH RECENTLY PUBLISHED LC-VCOS

Ref.	Tech. (um)	f_o (GHz)	PN (dBc/Hz)	V_{DD} (V)	P_{DC} (mW)	FoM (dBc/Hz)
Our work	0.18 CMOS	2.5 3.5	-121 -117	1.3 1.3	3.12 3.64	-184 -183
[14]	0.18 CMOS	2.2	-122	1.8	18.5	-176.2
[37]	0.18 CMOS	2.4 5.15	-112 -98	1.8 1.8	5.4 8	-173.4 -163.7
[43]	0.18 CMOS	0.9 1.8	-125 -122	1.8 1.8	16 16	-176 -181
[47]	0.18 SiGe	6 9	-106 -104	1.8 1.8	19 19	-176.7 -178.2

Chapter 5 *Conclusions*

A low power and low phase noise dual-band LC-VCO operating at 2.5 GHz and 3.5 GHz is proposed and implemented by TSMC 0.18-μm 1P6M CMOS process. The design uses the current-reused topology combined with an external-added resistor at the substrate node of the NMOS to achieve low power and low phase noise. With the current-reused topology, the proposed LC-VCO can operate using only half amount of DC current compared with the conventional topologies. The external resistor reduces the thermal noise of the NMOS and the reduction of the thermal noise decreases the phase noise of the LC-VCO effectively. The proposed LC-VCO consumes 3.12 mW and 3.64 mW at 2.5 GHz and 3.5 GHz, respectively. The measured phase noise at 1 MHz offset frequency is -121 dBc/Hz and -117 dBc/Hz in the 2.5 GHz and 3.5 GHz. Generally, the FoM of dual-band LC-VCO is -178 dBc/Hz at 1MHz offset frequency. The FoM of proposed LC-VCO is -184 dBc/Hz and -183 dBc/Hz at operating frequency 2.5 GHz and 3.5 GHz, respectively. Although the power consumption is obviously improved, there is still a lot of space for noise reduction. Several extensive studies have been underway to further reduce phase noise of LC-VCOs. In this field, it maybe worth our effort in the future works, such as low phase noise LC-VCOs.

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Appendix A *Basic Oscillator Theory*

The oscillator is an energy transfer device which is able to transfer DC power to AC power. The two methods to analysis the oscillator are Barkhausen's criteria [7] and negative resistance. The core of oscillator circuit is a loop that causes a positive feedback at a selected frequency as shown in Figure A.1. In this closed-loop feedback system, the oscillated condition can be established by combining the transfer functions of the active circuit $H_A(S)$ with the feedback stage $H_F(S)$ to the closed-loop transfer function as follow

$$\frac{V_{out}}{V_{in}} = \frac{H_A(s)}{1 - H_F(s)H_A(s)} \tag{A-1}$$

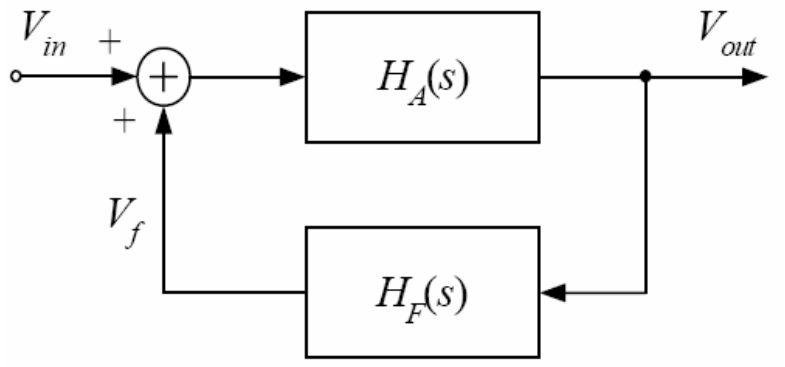

Figure A.1 The block diagram of closed-loop feedback system.

The denominator of the transfer function must become zero at the frequency of interest for a self-sustaining oscillation. Thus, $S = j\omega_0$, $H_F(j\omega_0)\cdot H_A(j\omega_0) = +1$, then the closed-loop gain approaches infinity at ω_0. The small signal whose frequency makes the above situation happen will be unlimitedly amplified by the circuit every cycle. Therefore, the oscillation happens.

For steady oscillation, two conditions must be simultaneously met at the oscillation frequency ω_0. Both of the equations are called as Barkhausen's criteria. The above conditions imply that any feedback system can oscillate if its loop gain and phase shift are chosen properly.

$$\left|H_F(j\omega_0)\cdot H_A(j\omega_0)\right| = 1 \tag{A-2}$$

$$\angle H_F(j\omega_0)\cdot H_A(j\omega_0) = 0 \tag{A-3}$$

For example, Figure A.2 shows the ring oscillator which is cascade of N stages with an odd number of inverters is placed in a feedback loop. We suppose that the gain of every inverter is A_0 and the inverter has only one pole ω_0. The transfer function of the ring oscillator is given by

$$H(j\omega) = -\frac{A_0^n}{\left(1+\frac{j\omega}{\omega_0}\right)^n} \tag{A-4}$$

From equation (2-4), we can know that $180°$ of phase shift is proved by the chain of N stages, each stage must provide $\frac{180°}{N}$ of phase shift sufficient gain at ω_0. Therefore, the oscillation frequency is

$$\tan^{-1}\frac{\omega_{osc}}{\omega_0} = \frac{180°}{N} \Rightarrow \omega_{osc} = \omega_0 \tan\left(\frac{180°}{N}\right), \tag{A-5}$$

and the gain of the ring oscillator must be one,

$$\frac{A_0^n}{\left[\sqrt{1+\left(\frac{\omega_{osc}}{\omega_0}\right)^2}\right]^n}=1, \tag{A-6}$$

From (2-5) and (2-6), the gain of every inverter is calculated by

$$A_0=\sqrt{1+\left[\tan\left(\frac{180°}{N}\right)\right]^2} \tag{A-7}$$

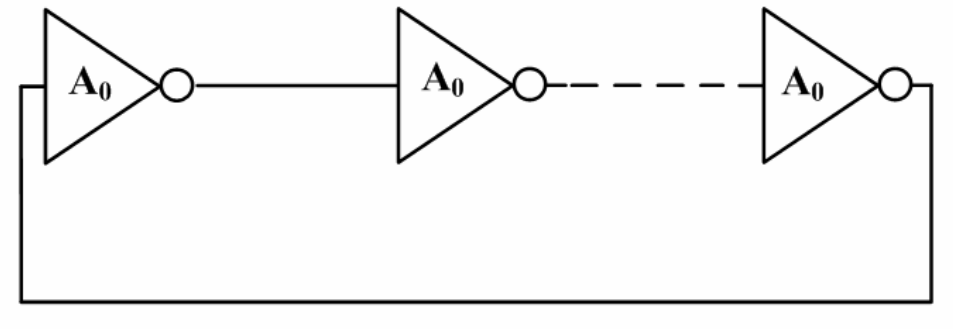

Figure A.2 Schematic of the ring oscillator.

In fact, the gain of every inverter is 2-3 times the proportions of A_0, because it ensures that the ring oscillator operates normally. The ring oscillator is analyzed effectively by Barkhausen's criteria. However, the LC-tank oscillator can be analyzed easily by negative resistance analysis.

The negative resistance analysis is developed to design the oscillator [8]. The canonical RF circuit for a one-port negative-resistance oscillator is shown in Figure A.3. The input impedance of the active device is $Z_{in}=R_{in}+jX_{in}$, and the device is terminated with a passive load impedance, $Z_L=R_L+jX_L$.

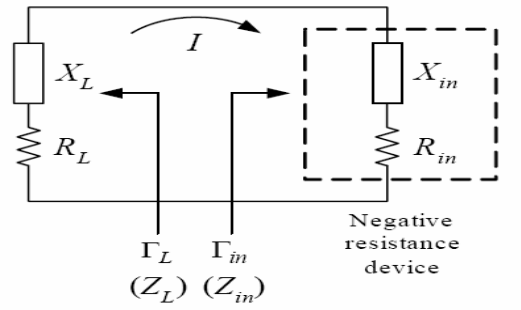

Figure A.3 Schematic diagram of the one-port negative-resistance oscillator.

Applying Kirchhoff's voltage law gives

$$(Z_{in} + Z_L)I = 0 \tag{A-8}$$

When oscillation is occurring, the RF current I is nonzero. The following conditions must be satisfied：

$$R_{in} + R_L = 0, \tag{A-9}$$

$$X_{in} + X_L = 0. \tag{A-10}$$

From the equation (A-5), while a positive resistance ($R_L > 0$) implies energy dissipation, a negative resistance ($R_{in} < 0$) implies and energy source. The condition of (A-6) controls the frequency of oscillation. For the steady-state oscillation condition, $Z_{in} + Z_L = 0$, implies that the reflection coefficients Γ_L and Γ_{in} are related as

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{-Z_{in} - Z_0}{-Z_{in} + Z_0} = \frac{1}{\Gamma_{in}}. \tag{A-11}$$

Thus, for steady-state oscillation, the condition of $\Gamma_L \cdot \Gamma_{in} = 1$ must be satisfied.

At the higher operating frequency, the S-parameters are usually used to design oscillators. Hence, the two-port analysis is needed in the transistor oscillator design, and the circuit model is shown in Figure A.4. A negative-resistance one-port network is created by terminating a potentially unstable transistor with and impedance designed to drive the device in an unstable region.

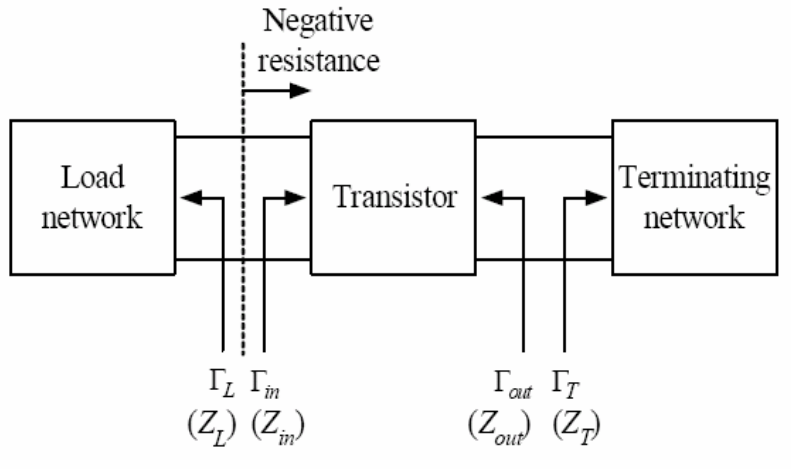

Figure A.4 Schematic diagram of the two-port negative-resistance oscillator.

For the oscillator design, the positive feedback is used on active device to enhance the instability of the device. The output stability circuit can be drawn in the Γ_T plane, and Γ_T is selected to produce a large value of negative resistance at the input to the transistor. The Z_L can be chosen to match Z_{in}. To start the oscillation, the value of

$$R_L = \frac{-R_{in}}{3} \tag{A-12}$$

is typically used, and the reactive part of Z_L is chosen to resonate the circuit,

$$X_L = -X_{in} \tag{A-13}$$

From the equation (A-7), the input reflection coefficient is

$$\Gamma_{in} = \frac{1}{\Gamma_L} = S_{11} + \frac{S_{12}S_{21}\Gamma_T}{1-S_{22}\Gamma_T} = \frac{S_{11}-\Delta\Gamma_T}{1-S_{22}\Gamma_T}, \tag{A-14}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. Γ_T can be obtained as

$$\Gamma_T = \frac{1-S_{11}\Gamma_L}{S_{22}-\Delta\Gamma_L} \tag{A-15}$$

Also, the output reflection coefficient is

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{11}\Gamma_L} = \frac{S_{22}-\Delta\Gamma_L}{1-S_{11}\Gamma_L} \tag{A-16}$$

From equations (A-11) and (A-12) it follows that

$$\Gamma_T \Gamma_{out} = 1 \qquad \text{(A-17)}$$

and $Z_T = -Z_{out}$. Therefore, the condition for oscillation of the terminating network is satisfied.

LC-tank VCO is using negative resistance of active circuit to cancel the resistance of LC-tank as shown in Figure A.5 [9]. The series transfers to parallel as shown in Figure A.6. Figure A.7 shows the equivalent resonant model. The LC-tank oscillator is also called the negative-Gm oscillator.

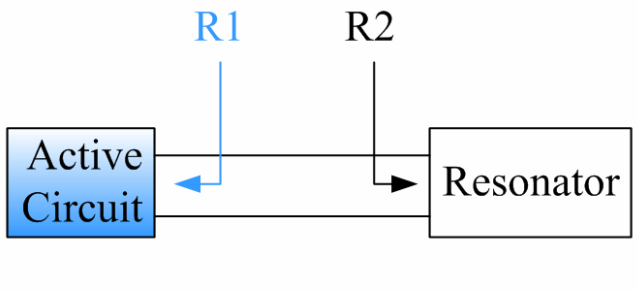

Figure A.5 Negative resistance and LC-tank resistance.

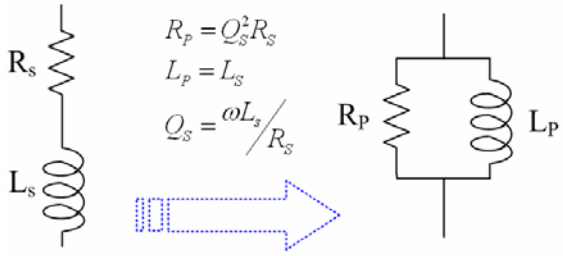

Figure A.6 Series to parallel.

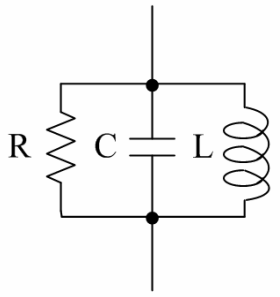

Figure A.7 Equivalent resonant model.

The negative resistance is produced from cross-coupled pair which is positive feedback. The impedance seen at the drain of M1 and M2 can be calculated which is $R_{in} = -2/g_m$ as shown in Figure A.8. In general, the phase noise of PMOS-corss coupled pair is lower than NMOS-cross coupled pair.

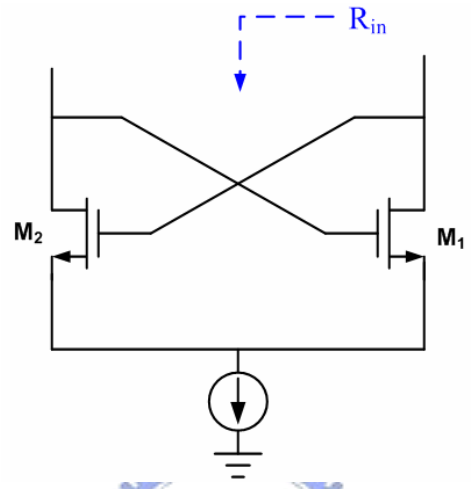

Figure A.8 Input impedance of NMOS cross-coupled pair.

Appendix B *Classifications of Noises*

The noise sources remained mysterious until H. Nyquist, J. B. Johnson and W. Schottky published a series of papers that explained where the noise comes from and how to expect it [17]. The sensitivity of communications systems is limited by noise, because it does no separate, suppose, artificial noise sources from more fundamental sources of noise. We have to understand the theorem of noise, and we can improve the noise performance of RF circuits.

B.1 Thermal Noise of Resistor

As shown in Figure B.1, the thermal noise of a resistor R can be modeled by a series voltage source. The mean-square open-circuit noise voltage is therefore

$$\overline{V_n^2} = 4kTR\Delta f \tag{B-1}$$

Where k is the Boltzmann's constant that is 1.38×10^{-23} J/K, T is the absolute temperature in kelvins, and Δf is the noise bandwidth in hertz over which the measurement is made.

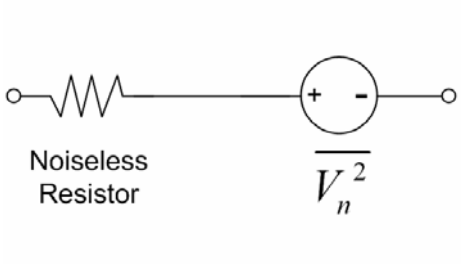

Figure B.1 The thermal noise model of resistor.

B.2 Thermal Noise in MOS

Since metal-oxide-silicon (MOS) is essentially voltage-controlled resistors, it exhibit thermal noise. In the triode region of operation particularly, one would expect noise proportional to the resistance value. The thermal noise mainly includes the drain current noise, the gate noise, the substrate noise, etc.

A. Drain Current Noise

The drain current noise model of MOS is shown in Figure B.2. It can be modeled by a current source connected between the drain and source terminals with a spectral density：

$$\overline{I^2_{nd}} = 4kT\gamma g_{d0}\Delta f \tag{B-2}$$

Where g_{d0} is the drain-source conductance at zero V_{DS}. The parameter γ that has a value of unity at zero V_{DS} in long devices decreases toward a value of 2/3 in saturation region. Unfortunately, measurements show that short channel NMOS devices in saturation exhibit noise far in excess of values predicted by long-channel theory, sometimes by large factors.

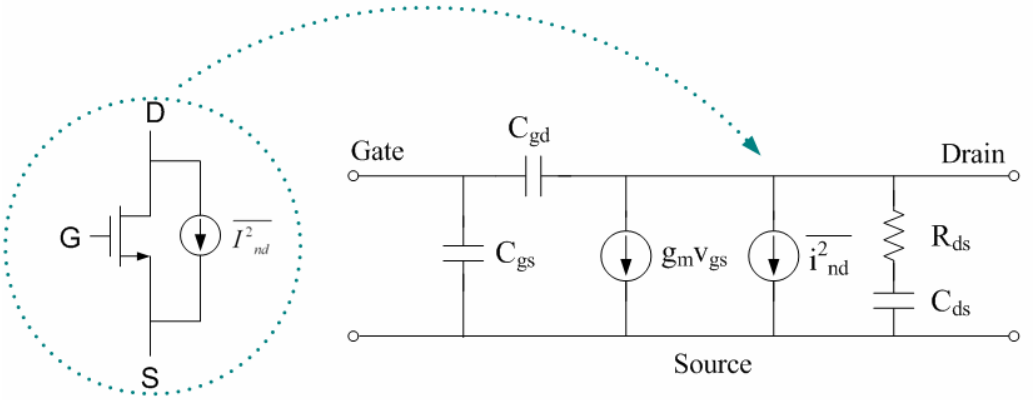

Figure B.2 The drain current noise model of MOS transistor.

B. Gate and Substrate Noise

In addition to drain current noise, the ohmic sections of a MOS also contribute thermal noise. The gate, source, and drain materials exhibit finite resistivity, thereby introducing noise. For a relatively wide transistor, the source and drain resistance is typically negligible, but the gate distributed resistance may become noticeable. The contribution to the effective gate resistance is not only from the physical gate electrode resistance but also from the distributed channel resistance as shown in figure B.3 [18]. In the noise model of figure B.4, a lumped resistor R_g represents the distributed gate resistance and the noise source is modeled by a series voltage source. The gate noise can be expressed as

$$\overline{V_{ng}^2} = 4kT\delta R_g \Delta f \tag{B-3}$$

The δ is the coefficient of gate noise, classically equal to1.33 for long-channel device. Although the noise behavior of long channel devices if fairly well understood, the precise behavior of δ in the short channel regime is unknown at present, it is probably reasonable as a crude approximation to assume that δ continues to be about

twice as large as γ. Hence, γ is typically 2-3 for short channel NMOS devices, δ may be taken as 4-6. The gate distributed resistance is given by：

$$R_g = \frac{R_H W}{3n^2 L} \tag{B-4}$$

Where R_H is the sheet resistance of the poly-silicon, W is the total gate width of the device, L is the gate length of the device, and n is the number of gate fingers used to layout the device.

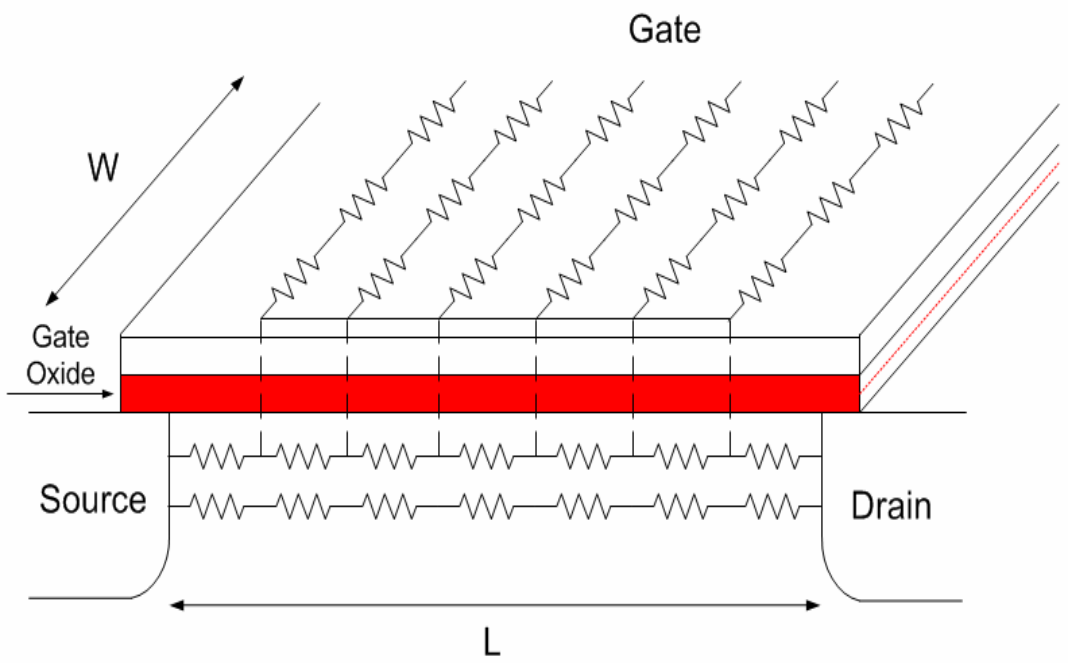

Figure B.3 Equivalent gate resistance consists of gate poly and channel.

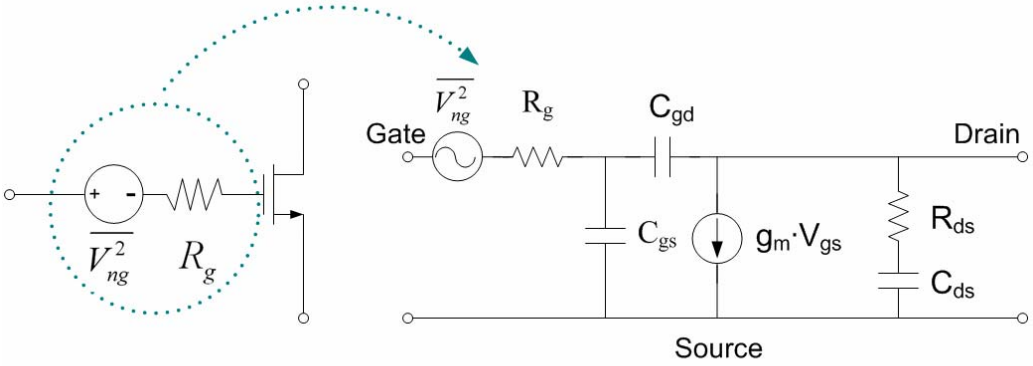

Figure B.4 The gate noise model of MOS transistor.

The material of substrate also exhibit finite resistivity, so the thermal noise of substrate in the MOS can be expressed as：

$$\overline{V_{n,sub}^2} = 4kTR_{sub}\Delta f \tag{B-5}$$

Where R_{sub} is the resistor in the substrate of the MOS transistor. The equivalent noise voltage of this resistor modulated the back gate, producing a mean-square drain noise current component whose value is given by

$$\overline{I_{n,sub}^2} = 4kTR_{sub}g_{mb}^2\Delta f \tag{B-6}$$

g_{mb} is the parameter that is caused by body effect.

C. Induced Gate Current Noise

At high-frequency, the local channel voltage fluctuations due to thermal noise couple to the gate through the oxide capacitance and cause an induced gate noise current to flow. Figure B.5 shows the induced gate current noise and its small signal model in the MOS transistor. A simple gate circuit model that includes both of a shunt noise current $\overline{i_g^2}$ and a shunt conductance g_g have been added. Mathematical expressions for these sources are are given by:

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g \quad , \quad g_g = \frac{\omega_0^2 C_{gs}^2}{5g_{d0}} \tag{B-7}$$

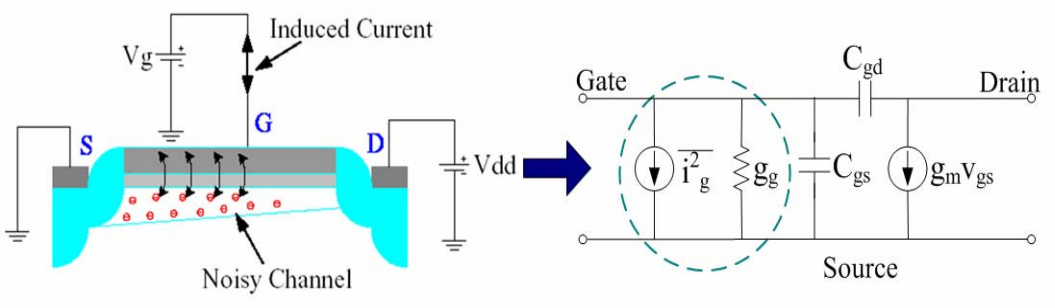

Figure B.5 Induced gate current noise and small signal model in MOS transistor.

D. The Correlation between Drain Noise and Induced Gate Noise

From Figure B.5, the drain noise and induced gate noise share a common physical origin and it is expressed by cross-correlation between the two noise.

$$\overline{i_d i_d^*} = \frac{2}{3} 4kTg_{d0}\Delta f \tag{B-8}$$

$$\overline{i_g i_g^*} = \frac{4}{3} 4kTg_{d0}\Delta f \tag{B-9}$$

$$\overline{i_g i_d^*} = \frac{1}{6} j\omega C_{gs} 4kT\Delta f \tag{B-10}$$

The cross-correlation coefficient is defined as equation (9) and is about 0.395j in MOS device:

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g i_g^*} * \overline{i_d i_d^*}}} = 0.395j \tag{B-11}$$

For the noise analysis, the induced gate noise can be split into two components. The first one is fully uncorrelated with the drain noise, and the other is fully correlated with the drain noise. It can be written as:

$$\overline{i_g^2} = 4kT\varsigma g_g (1-|c|^2)\Delta f + 4kT\varsigma g_g |c|^2 \Delta f \tag{B-12}$$

The correlation noise circuit for RF MOS transistor is shown in Figure B.6.

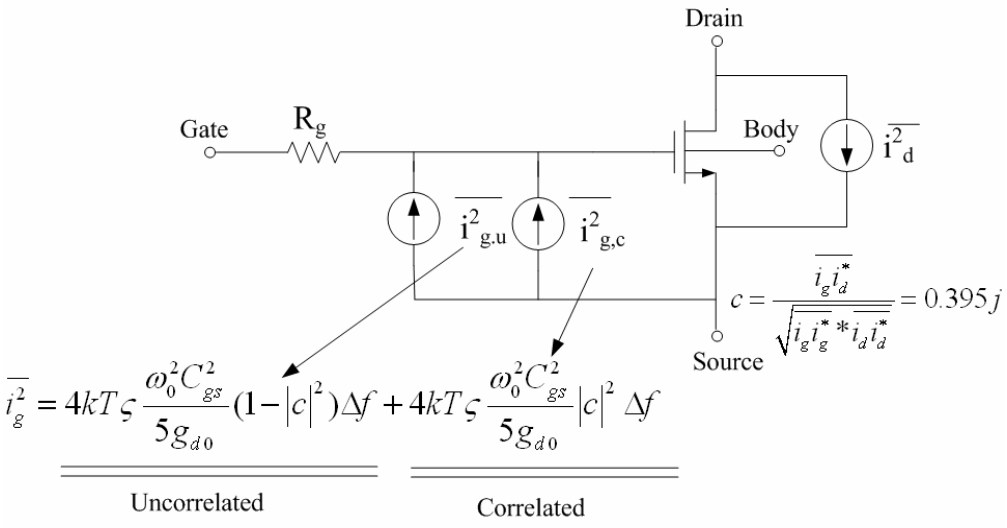

Figure B.6 The correlation noise circuit for RF MOS transistor.

B.3 Flicker Noise

It is the most mysterious type of noise. No universal mechanism for flicker noise has been identified, yet it is ubiquitous. Flicker noise shows up in ordinary resistors, where it is often called “excess noise,” since this noise is in addition to what is expected from thermal noise considerations. It is found that a resistor exhibits $1/f$ noise only when there is DC current flowing through it, with the noise increasing with the current. In the electronic devices, the interface between the gate oxide and the silicon substrate in a MOS entail an interesting phenomenon. Since the silicon crystal reaches an end at this interface, many ”dangling“ bonds appear, giving rise to extra energy state. As charge carriers move at the interface as shown in Figure B.7 (a), some are randomly trapped and later released by such energy states, introducing flicker noise in the drain current. But we can find that the noise spectrum density is inversely proportional to the frequency as shown in Figure B.7 (b). For this reason, flicker noise is also called $1/f$ noise [19]. Furthermore, Larger MOS transistors exhibit less $1/f$ noise because their larger gate capacitance smooths the fluctuations in channel charge. Hence, if good $1/f$ noise performance is to be obtained from MOS transistors, the largest practical device sizes must be used.

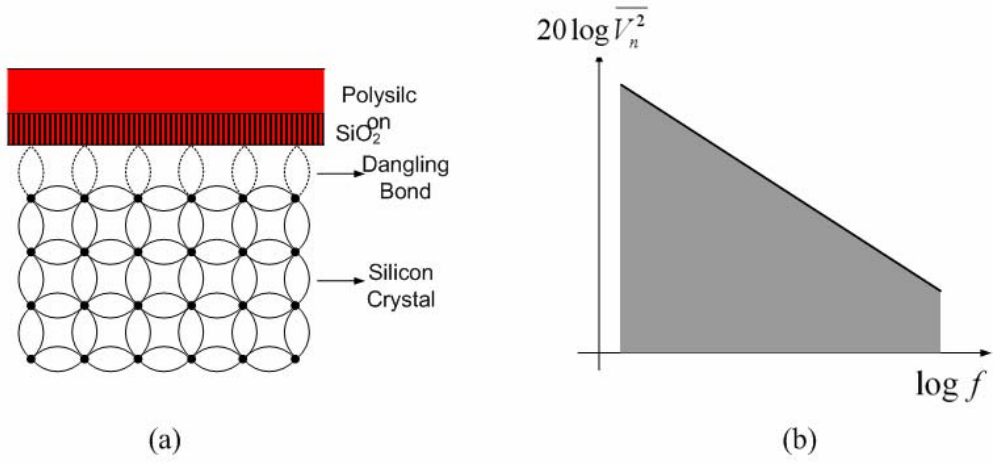

Figure B.7 (a) Dangling bonds at oxide-silicon interface and (b) flicker spectrum.

B.4 Shot Noise

The shot noise was first described and explained by Schottky in 1918. It is therefore occasionally known as Schottky noise in recognition of his achievement. The fundamental basis for shot noise is the granular nature of the electronic charge, but how the granularity translates into noise is perhaps not as straightforward as one might think. Two conditions must be satisfied for shot noise to occur. There must be a direct current flow and there must also be potential barrier over which the charge carriers hop. So the ordinary, linear resistors do not generate shot noise, despite the quantized nature of electronic charge. Figure B.8 shows a cross sectional view of the NMOS with two possible sources of shot noise [20] and the shot noise is expressed as：

$$\overline{I_{nsh}^2} = 2qI_{DC}\Delta f \tag{B-13}$$

Where $\overline{I_{nsh}^2}$ is the rms noise current, q is the electronic charge that is about 1.69×10^{-19} C, IDC is the DC current in amperes, and Δf is the noise bandwidth in HZ.

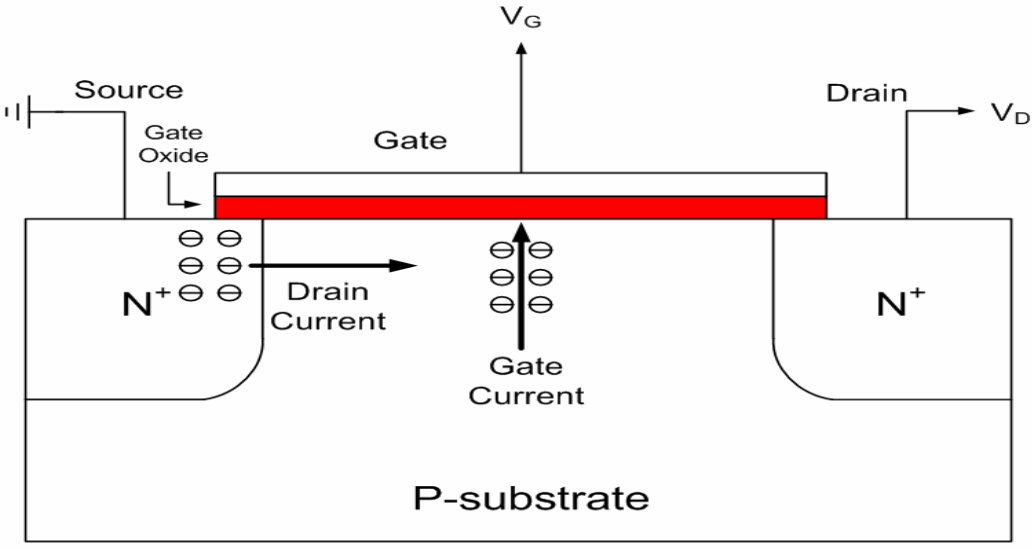

Figure B.8 Tow major shot noise in the NMOS.

B.5 Popcorn Noise

The popcorn noise, also called burst noise or random-telegraph-signal (RTS), appears to be related to imperfections in semiconductor material and heavy ion implants. The popcorn nose is not periodic and it occurs in pulses. It is understood even more poorly than1/ f noise.

In the RF circuit, the shot noise and popcorn noise are ignored. The flicker noise does not have great effect on RF circuit, generally we also neglect it. So the complete noise model of RF MOS transistor is shown in Figure B.9.

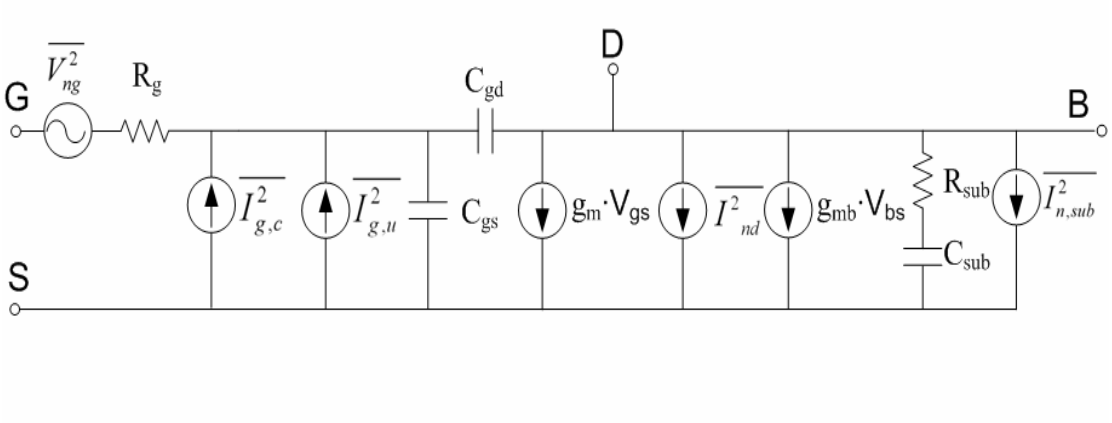

Figure B.9 The complete noise model of RF NMOS transistor.