國 立 交 通 大 學

電信工程學系

碩 士 論 文

可設定式雙模低失真類比數位轉換器

Configurable Dual-mode Low-distortion A/D Converter

研究生：林明澤

指導教授：洪崇智 博士

中 華 民 國 九十六 年 十 月

可設定式雙模低失真類比數位轉換器

Configurable Dual-mode Low-distortion A/D Converter

研 究 生：林明澤　　Student：Ming-Tze Lin

指導教授：洪崇智 博士　　Advisor：Dr. Chung-Chih Hung

國 立 交 通 大 學

電 信 工 程 學 系 碩 士 班

碩 士 論 文

A Thesis

Submitted to Department of Communication Engineering

College of Electrical Engineering and Computer Science

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of Master

In

Communication Engineering

October 2007

Hsinchu, Taiwan.

中華民國九十六年十月

可設定式雙模低失真類比數位轉換器

研究生：林明澤　　指導教授：洪崇智 教授

國立交通大學

電信工程學系碩士班

摘要

隨著多功能裝置需求的快速成長，如手機、mp3 播放器等，多功能在今日已經變得越來越重要。在今日的裝置應用，數位電路主導整個晶片的面積。無論如何，類比轉數位介面是不可少的。使用超取樣與雜訊型化的三角積分器調變器是非常有效的技術應用在高解析度類比數位轉換器上。它本身對原件不匹配與漂移非常不敏感，而這項特點非常適合今日的 VLSI 設計。考慮兩種三角積分調變器，應用在音頻的三角積分調變器與應用在量測的累加調變器， 他們擁有相似的架構，並且可以用共用或者整合的方式設計在一起。因此，這個可調式超取樣類比數位轉換器不僅可以擁有兩種功能，並且可以減少晶片面積。除此之外，多級或疊接調變器，也叫做 MASH，在實現方面不會有穩定性的問題還可以更適合做設計上的控制。此外，向前饋入的架構更適合此種電路，讓它有低失真的效果。

因此，為了將兩種電路合併用低失真 MASH 的架構實現，這個研究重點放在如何設計可設定式雙模低失真類比數位轉換器。晶片是以台積電 0.18 微米標準互補式金氧半導體製程所製造。在音頻應用上使用過取樣率 128，也就是操作頻率為 5.12 MHz，量測結果是 58 dB 動態輸入範圍和 55 dB 訊號失真雜訊比。在量測應用上使用操作頻率 5.12 MHz 的量測結果與預測使用同樣的轉換時間相比低 3 bit。這個論文證明此架構引導出一種簡單且模組化的架構。

Configurable Dual-mode Low-distortion A/D Converter

Student：Ming-Tze Lin　　Advisor：Prof. Chung-Chih Hung

Department of Communication Engineering

National Chiao Tung University

Hsinchu, Taiwan

Abstract

With the rapid growth in demand for multi-function device such as cellular phone and MP3 player, multi-function has become more and more important today. In today's device application, digital circuits dominate the whole chip function. However, the analog-to-digital converter (ADC) is indispensable. The Sigma-delta modulation, associated with oversampling and noise shaping, is a well-known technique used in high-accuracy A/D converters. It is almost insensitive to component matching and variation and is suitable for today's VLSI design. Concerning the two sigma-delta modulators, the Sigma-delta modulator for audio application and incremental modulator for measurement, they have similar architectures and can be combined together by sharing or merging their similar parts. Therefore, this configurable oversampling A/D converter can not only have two functions but also reduce the chip area. Besides, multistage or cascade modulators, also called MASH, can be realized without stability problems and more programmable. In addition, feedforward configuration is suitable for this circuit to have low-distortion.

In order to combine the two circuits using feedforward MASH configuration, this research will focus on how to design a configurable dual-mode low-distortion A/D converter. The chip has been fabricated by TSMC 0.18-um CMOS process. With an oversampling ratio of 128 and a clock frequency of 5.12 MHz, the modulator achieves a 58 dB dynamic range and a peak SNDR of 55 dB for audio application. The measured resolution of the measurement application is 3 bit lower than the prediction in the same conversion time with a clock frequency of 5.12 MHz. This thesis

demonstrates that this concept leads to a very simple modular architecture.

誌謝

隨著這份碩士論文的完成，兩年來在交大的求學生活也即將告一個段落，往後迎接著我的，又是另一段嶄新的人生旅程。本論文得以順利完成，首先，要感謝我的指導教授洪崇智老師在我兩年的研究生活中，對我的指導與照顧，並且在研究主題上給予我寬廣的發展空間。而類比積體電路實驗室所提供完備的軟硬體資源，讓我在短短兩年碩士班研究中，學習到如何開始設計類比積體電路，乃至於量測電路，甚至單獨面對及思考問題的所在。此外要感謝李育民教授、黃淑娟教授、陳科宏教授撥冗擔任我的口試委員並提供寶貴意見，使得本論文更為完整。也感謝國家晶片系統設計中心提供先進的半導體製程，讓我有機會將所設計的電路加以實現並完成驗證。

另一方面，要感謝所有類比積體電路實驗室的成員兩年來的互相照顧與扶持。首先，感謝博士班的學長羅天佑、薛文弘、廖介偉、黃哲揚以及已畢業的碩士班學長何俊達、黃琳家、蔡宗諺、林政翰、楊家泰和陳家敏在研究上所給予我的幫助與鼓勵，尤其是俊達學長，由於他平時不吝惜的賜教與量測晶片時給予的幫助，使得我的論文研究得以順利完成。另外我要感謝白逸維、廖德文、高正昇、邱建豪、吳國璽、黃旭佑和傅崇賢等諸位同窗，透過平日與你們的切磋討論，使我不論在課業上，或研究上都得到了不少收穫。尤其是電資718實驗室的同學們，兩年來陪我一塊兒努力奮鬥，一起渡過同甘苦的日子，也因為你們，讓我的碩士班生活更加多采多姿，增添許多快樂與充實的回憶。此外也感謝學弟們林永洲、郭智龍、夏竹緯、楊文霖，秋楓翔，黃介仁的熱情支持,因為你們的加入，讓實驗室注入一股新的活力與朝氣。

到這邊，特別要致上最深的感謝給我的父母及家人們，謝謝你們從小到大所給予我的栽培、照顧與鼓勵，讓我得以無後顧之憂地完成學業，朝自己的理想邁進，衷心感謝你們對我的付出。

最後，所有關心我、愛護我和曾經幫助過我的人，願我在未來的人生能有一絲的榮耀歸予你們，謝謝你們。

林明澤 于 交通大學工程四館 718 實驗室

2007.10.1

List of Figures

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

List of Tables

Chapter 1 Introduction

1.1 Motivation

Recently, as the continued scaling of VLSI technology, the digital circuit has more attractive advantages than analog circuit, such as high level resolution, power consumption reduction, noise robustness and less chip area. Therefore, analog circuit dominates the whole chip area relative to digital circuit. However, in real world, human only can sense analog signals. Whether how advanced the digital circuit technique become, the interface to convert analog signal and digital signal is necessary, which called Analog to Digital Converter(ADC) or Digital to Analog Converter(DAC).

Understanding why reduce chip size is important. The yield (number of good die/total number of die on the wafer) is increased with smaller die size. Another benefit of reducing die size comes from the realization that processing costs per wafer are relatively constant. Increasing the number of die on a wafer decreases the cost per die. Therefore, reducing chip area is important, and it can be the result of having better layout of fabricating the chip in a process with smaller device dimensions.

Along with rapid growth of multi-function device in many applications, such as cellular phone, PDA, and mp3 players, system on a chip (SOC) is an important issue to help devices become smaller and lighter. How integrate these functions and reduce the chip area is what we want to do.

Oversampling techniques based on sigma-delta modulation offer numerous advantages for realization of high-resolution analog-to-digital (A/D) converters. First, oversampling converters relax the requirements placed on the analog circuitry at the expense of more complicated digital circuitry. The other advantage is that they simplify the anti-aliasing filter for A/D converters and smoothing filter for D/A converters. Besides, it has less chip area than Nyquist rate converters. Then, concerning two different applications of the sigma-delta modulator, sigma-delta modulator for audio and incremental for measurement, can be designed together in a smart manner. In addition, feedforward configuration does not only relax the linearity of the opamp but also simplify the mash architecture and improve the input dynamic range.

In this thesis, a 3.066mW, 14-bits for audio, 16-bits for measurement, and 5.12MS/s configurable dual-mode low-distortion analog to digital converter with the 1.8V supply voltage has been designed and implemented with the standard TSMC 0.18μm CMOS 1P6M process.

1.2 Thesis Organization

This thesis is organized into seven chapters.

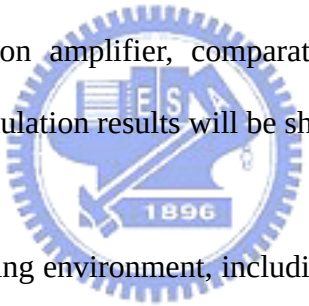
Chapter 1 briefly introduces the motivation of the thesis.

Chapter 2 describes the concepts of oversampling sigma-delta data converters. First, extra bits of resolution can be extracted from oversampling will be introduced. Second, the use of shaped quantization noise applied to oversampling signals will be

described mathematically. Finally, the various architectures of sigma-delta modulators will be compared.

Chapter 3 describes the concepts of incremental converters. First, the basic operation of the incremental modulator will be introduced. Then, higher order modulator to reduce conversion time will be discussed. Finally, because of high resolution and offset cancellation for instrumentation application, the offset cancellation technique will be described.

Chapter 4 presents the system level design consideration. The merging method will be discussed first. After building the behavior model, we continue the circuit level design, including the operation amplifier, comparator, and nonoverlapping clock generator. The circuits and simulation results will be shown in this chapter.



Chapter 5 presents the testing environment, including the instruments and external circuits on the printed circuit board (PCB). Measured results for the configurable dual-mode low-distortion A/D converter, which is fabricated in a standard TSMC 0.18μm CMOS mixed-signal process, will be plotted and summarized

Finally, the conclusions of this thesis are summarized in Chapter 6.

Chapter 2 An Overview of Sigma-Delta Data Converters

2.1 Introduction

In this chapter, the overview of various analog-to-digital converters having difference advantages and drawbacks will be discussed first. Then, the sampling theorem will be introduced and we shall see that how extra bits of resolution can be extracted from oversampling theorem and how it relax anti-aliasing filter. Next, getting higher resolution through using noise shaping strategy and digital decimation filter will be discussed mathematically.

2.2 Overview of Analog-to-Digital Data Converters

Although today is an ever-increasing digital world, analog-to-digital converter also play an important role to translate the digital data from our inherently analog world. However, with the ADC, the input is an analog signal with an infinite number of values, which then has to be quantized into an N-bit digital word. Then, these digital words can be coded and be transmitted into DSP unit or digital systems.

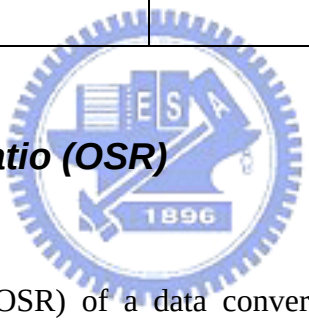
2.2.1 Categories of Analog-to-Digital Data Converters

There are many different structures to realize analog-to-digital converters. According to speed and resolution, we can categorize these structures into three parts

shown in Table 2.1. There is a trade off between speed and resolution and it is difficult to design ADCs satisfying both demands at the same time. We shall understand this trade off and choose the adaptable structure for difference application.

TABLE 2.1 Various Kinds of Analog-to-Digital Data Converters

Speed	Slow	Medium	Fast
Resolution	High	Medium	Low
Structure	Integrating Oversampling	Successive approximation Algorithmic Single-bit pipeline	Flash Multiple-bit pipeline Folding Interpolating Time-Interleaved



2.2.2 Oversampling Ratio (OSR)

The oversampling ratio (OSR) of a data converter is a ratio of the sampling frequency to Nyquist-rate.

$$OSR = \frac{f_s}{2 f_b} \tag{2.1}$$

where f_s is the sampling frequency and f_b is the signal bandwidth. When the OSR is equal to 1 ($f_s = 2 f_b$), it means the data converter is the Nyquist-rate data converter, however, when the OSR is great than 1, it means the data converter is the oversampling data converter. The OSR is the important parameter for oversampling data converters. We shall see that the increase in dynamic rage is only 3 dB for every double of the sample rate. To obtain much higher dynamic-range improvement as the

sampling rate is increased, noise shaping through the use of feedback can be used [1].

2.2.3 Signal to Noise Ratio (SNR)

The signal-to-noise ratio (SNR) of a data converter is the ratio of the signal power to the noise power, which measured at the output of the data converter. A more common SNR formula is to assume input is a sinusoidal waveform. Then, the theoretical value of SNR for Nyquist-rate ADC is given by

$$SNR = 6.02 \cdot N + 1.76 \quad dB \tag{2.2}$$

But for oversampling ADC with no noise shaping, the theoretical value of SNR is

$$SNR = 6.02 \cdot N + 1.76 + 10\log(OSR)\ dB \tag{2.3}$$

We can see that every doubling the sampling rate will acquire additional 3 dB SNR than Nyquist-rate ADC.

2.2.4 Signal to Noise and Distortion Ratio (SNDR)

The signal to noise and distortion ratio (SNDR) of a data converter is the ratio of the signal power to the power of the noise plus the harmonic distortion components, which measured at the output of the data converter. The maximum SNDR that a converter can achieve is called the peak signal to noise and distortion ratio. Generally, SNDR is lower than SNR.

2.2.5 Spurious Free Dynamic Range (SFDR)

The spurious free dynamic range (SFDR) is defined as the ratio of rms value of amplitude of the fundamental signal to the rms value of the largest harmonic distortion component in a specified frequency range. SFDR may be much larger than SNDR of a data converter.

2.2.6 Dynamic Range (DR)

The useful signal range, or dynamic range (DR), of the A/D converter for sinusoidal inputs is defined as the ratio of the output power at the frequency of the input sinusoid for a full-scale input to the output signal power for a small input for which the SNDR is unity [2].

2.2.7 Effective Number of Bits (ENOB)

For data converter, a specification often used in place of the SNR or SNDR is ENOB, which is a global indication of how many bits would be required to get the same performance as the converter. ENOB can be defined as follows:

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad bits. \tag{2.4}$$

2.2.8 Overload Level (OL)

OL is defined as the relative input amplitude where the SNR is decreased by 6dB compared to peak SNR value.

2.3 Sampling Theorem

Sampling is the first step for A/D conversion process that transform an analog input signal into a sequence of digital code. The Nyquist Criterion defines how fast the sampling rate needs to be to represent an analog signal accurately. This criterion requires that the sampling rate is at least two times the highest frequency contained in the analog signal.

$$f_s \geq 2 f_b \tag{2.5}$$

We shall know if there is some signal that we don't want above the highest frequency, the aliasing will occur. Thus, we shall add a low-pass filter before sampling to filter out the signal above the highest frequency. This low-pass filter, sometimes called the anti-aliasing filter, must have flat response over the frequency band of interest (base-band) and attenuate the frequencies above the Nyquist frequency enough to put them under the noise floor, but a low-pass filter having narrow transition band is expensive. We have another way to deal with this problem. Increasing sampling rate higher than Nyquist frequency will relax the transition band of the anti-aliasing filter. Oversampling converters require considerably simpler anti-aliasing filters than Nyquist rate converters with similar performance.

2.4 White Noise

We can model a quantizer as adding quantization error e(n), as shown in Figure 2.1. The output signal, y(n), is equal to the closest quantization level value of x(n). The quantization error is the difference between the input signal and output signal.

This quantization error is on the order of one least-significant-bit (LSB) in amplitude, which equals the difference between two adjacent quantization levels.

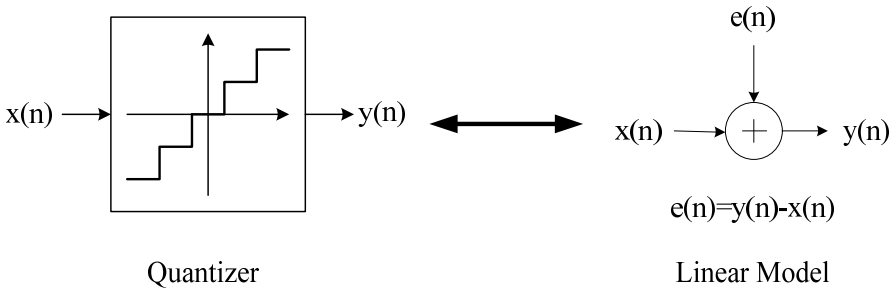


Figure 2.1 A general quantizer and its linear model

Many of the original results and insights into the behavior of quantization error are due to Bennett [3]. Bennett first developed conditions under which quantization noise could be reasonably modeled as additive white noise. A common statement of the approximation is that the quantization error has the following properties, which we call it the "input-independent additive white-noise approximation" [4]:

Property 1. q[n] is statistically independent of the input signal

Property 2. q[n] is uniformly distributed in [-Δ/2, Δ/2], where Δ equals one LSB

Property 3. q[n] is an independent identically distributed sequence or q[n] has a flat power spectral density (white).

Therefore, quantization noise, e(n) can be approximated as an independent random number uniformly distributed between $\pm\Delta/2$. Thus, the quantization noise power equals $\Delta^2/12$ and is independent of the sampling frequency, f_s. Also, the spectral density of e(n), Se(f), is white (i.e., a constant over frequency) and all its

power is within $\pm f_s / 2$ (a two-side definition of power).

2.5 Oversampling Technique

Oversampling means that the converters operate much faster than the input signal's Nyquist-rate. Oversampling can not only relax the requirement of the anti-aliasing filter, but also improve the resolution of the A/D converters. We have shown how oversampling can relax the requirement of the anti-aliasing filter in section 2.3. Next, we will show how it can increase the output's signal-to-noise ratio (SNR) by filtering out quantization noise that is not in the signal's bandwidth.

First, we define the oversampling ratio (OSR) as

$$OSR = \frac{f_s}{2 f_b} \tag{2.6}$$

Figure 2.2 shows a possible oversampling system without noise shaping, where $y_1(n)$ is equal to the closest quantized value of input signal, u(n), $y_1(n)$ is filtered by H(f) to create the $y_2(n)$, and q(n) is the quantization noise.

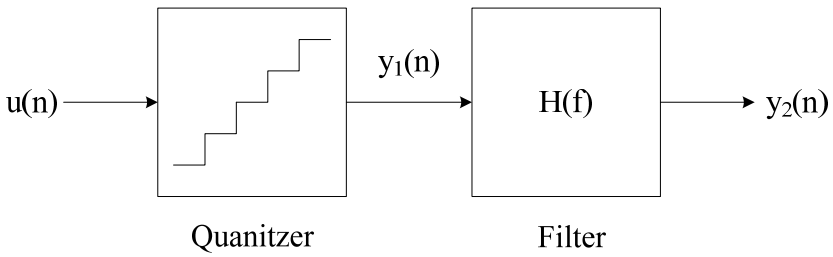


Figure 2.2 A possible oversampling system without noise shaping

Assuming the input signal is a sinusoidal wave and quantization noise is white noise. After quantization, the spectral density of $y_1(n)$ is shown in Figure 2.3. We can see that the signal of interest are below $\pm f_b$. Since the quantization noise is white noise, it means that noise power is uniformly distributed between $-f_s/2$ and $+f_s/2$.

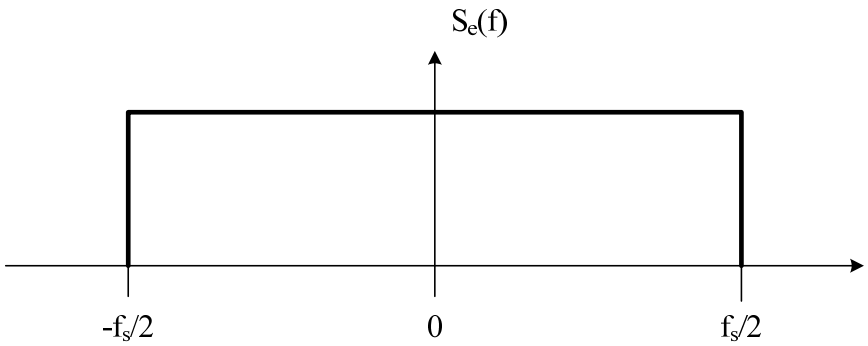


Figure 2.3 The spectral density of y1(n) after quatization

Figure 2.4 shows the brick-wall response of H(f). After filtering, the spectral density of $y_2(n)$ is shown in Figure 2.5. The brick-wall response filter out the quantization noise which are out of our interest bandwidth, and only a small fraction of quantization noise fall into the range of $-f_b$ and f_b. However, we know the total power amount of quantization noise is $\Delta^2/12$, and the in-band noise power can reduce to

$$P_{e,inband} = \frac{fs}{2f_b} \times \frac{\Delta^2}{12} = \frac{\Delta^2}{12}\left(\frac{1}{OSR}\right) \tag{2.7}$$

Therefore, doubling OSR decrease the quantization noise power by one-half or, equivalently, 3dB (or, equivalently, 0.5 bits).

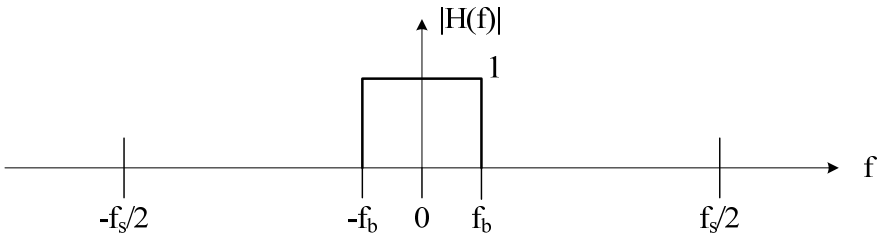


Figure 2.4 The brick-wall response of the filter to remove out of band quantization noise power

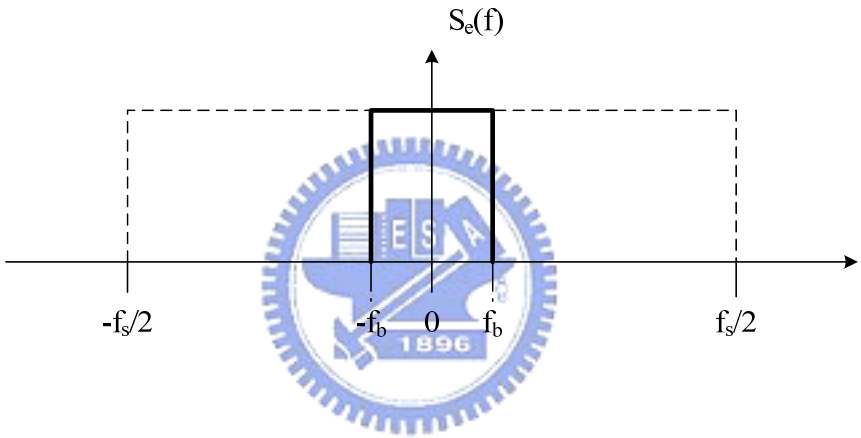


Figure 2.5 The spectral density of y2(n) after filtering

Assuming the peak amplitude of the sinusoidal wave is $2^N(\Delta/2)$. For this maximum peak value, the signal power, P_S, has a power equal to

$$P_S = \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8} \tag{2.8}$$

Now we can calculate the maximum SNR (in dB) to be the ratio of the maximum sinusoidal power to the quantization noise in the signal $y_2(n)$. Using (2.7) and (2.8),

the $SNR_{\max}$ is equal to

$$SNR_{\max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log(OSR) \tag{2.9}$$

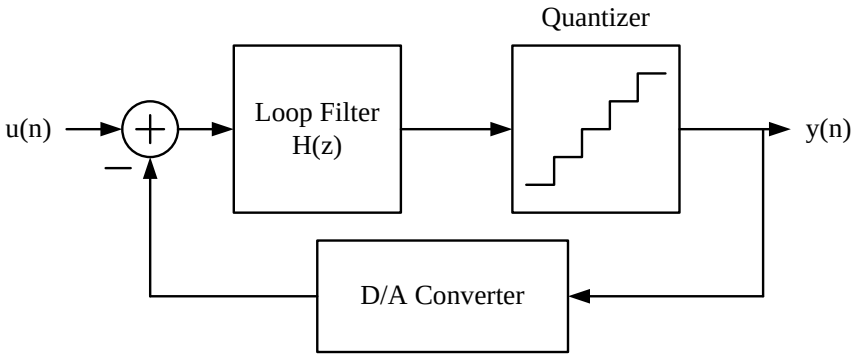
which is also equal to

$$SNR_{\max} = 6.02N + 1.76 + 10\log(OSR) \tag{2.10}$$

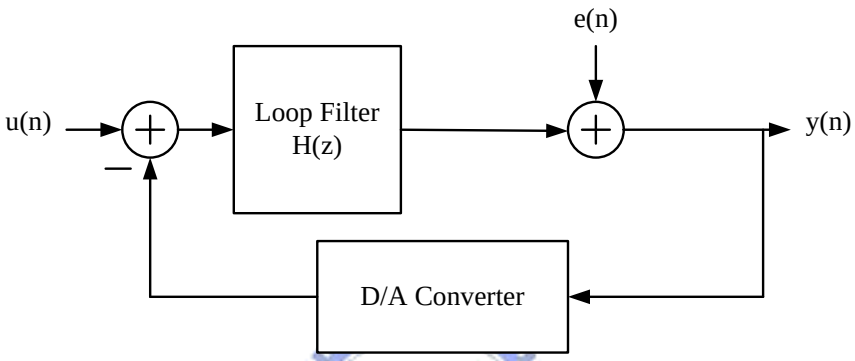
N means that N-bit quantizer using in converter, and increasing 1 more bit can improve 6.02 dB SNR. Here, we see that doubling OSR will give SNR 3 dB or, equivalently, 0.5 bits improvement. The reason for this improvement is the constant quantization noise power uniformly distribute between $-f_s/2$ and $+f_s/2$. Therefore, after filtering out of band signal power, it remains a little amount of the quantization noise power, and SNR improve.

2.6 Noise Shaping Strategy

In this section, using feedback to get the advantage of noise shaping the quantization noise will be discussed. First, a general noise-shaped sigma-delta modulator and its linear model have been shown in Figure 2.6.



(a)



(b)

Figure 2.6 (a) A general noise-shaped sigma-delta modulator (b) Linear model of the modulator showing injected quantization noise

Treating the linear model shown in Figure 2.6 as having two independent inputs, u(n) and e(n), we can derive a signal transfer function, $S_{TF}(z)$, and a noise transfer function, $N_{TF}(z)$.

$$S_{TF}(z) \equiv \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)} \tag{2.11}$$

$$NTF(z) \equiv \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \tag{2.12}$$

According to (2.11) and (2.12), the zeros of the noise transfer function, $N_{TF}(z)$,

will be equal to the poles of $H(z)$. In other words, we can control the zeros of the noise transfer function by choosing the function of the loop filter. We can also using super position to combine two signals, and find out the output as

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \tag{2.13}$$

The STF generally have all-pass or low-pass frequency response and the NTF have high-pass frequency response. In other words, the STF will be approximately unity over the signal band and the NTF will be approximately zero over the same frequency band. The quantization noise will be removed to high frequency band when using noise-shaping strategy [01]. The quantization noise over the frequency band of interest will be reduced and do not affect the input signal. This would improve the SNR significantly for overall system.

2.6.1 First-Order Sigma-Delta Modulator

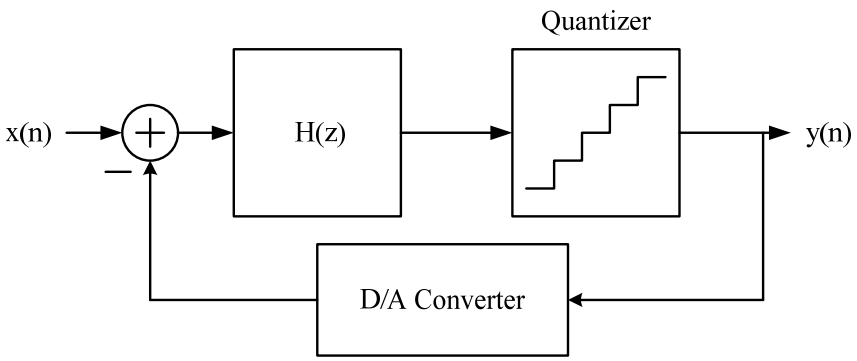


Figure 2.7 A simple block diagram of the first-order low-pass sigma-delta modulator

In Figure 2.7, it is a simple block diagram of the first-order low-pass sigma-delta modulator. It includes an integrator and a quantizer. The input of the integrator is the

input signal minus the output signal of the modulator through the DAC. In this example, since the loop filter is a high-pass filter, the noise function should have a zero at dc (i.e., z = 1). The transfer function of the discrete-time integrator (i.e., have a pole at z = 1) is

$$H(z) = \frac{1}{z-1} \tag{2.14}$$

Its block diagram for such a choice is shown in Figure 2.8.

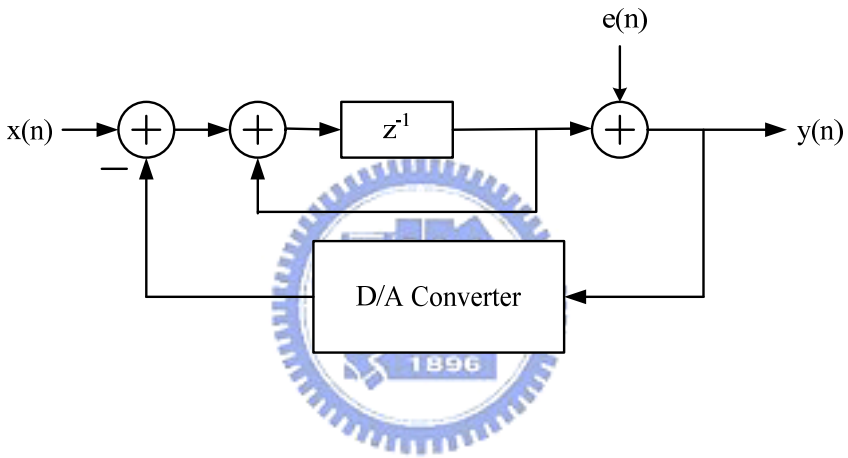


Figure 2.8 The block diagram for the first-order low-pass sigma-delta modulator

According to (2.11) and (2.12), we can obtain the signal transfer function, $S_{TF}(z)$, is given by

$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{1/(z-1)}{1+1/(z-1)} = z^{-1} \tag{2.15}$$

and the noise transfer function, $N_{TF}(z)$, is given by

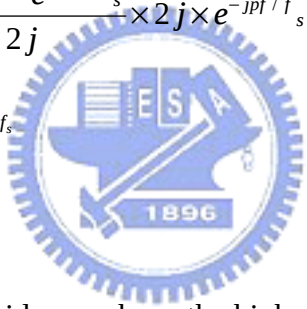
$$N_{TF} = \frac{Y(z)}{E(z)} = \frac{1}{1+1/(z-1)} = (1-z^{-1}) \tag{2.16}$$

Combine two signal transfer function, we obtain the output as

$$Y(z) = z^{-1} \cdot U(z) + (1 - z^{-1}) \cdot E(z) \tag{2.17}$$

We see that the input signal is just through a delay to output, and the quantization noise is through a discrete-time differentiator (i.e., a high-pass filter) to output. We are interesting in the magnitude of the noise transfer function, $|N_{TF}(f)|$, we let $z = e^{jwT} = e^{j2pf/f_s}$ and write the following:

$$\begin{aligned} N_{TF}(f) &= 1 - e^{-j2pf/f_s} = \frac{e^{jpf/f_s} - e^{-jpf/f_s}}{2j} \times 2j \times e^{-jpf/f_s} \\ &= \sin\left(\frac{pf}{f_s}\right) \times 2j \times e^{-jpf/f_s} \end{aligned} \tag{2.18}$$



Taking the magnitude of both sides, we have the high-pass function

$$|N_{TF}(f)| = 2\sin(\frac{pf}{f_s}) \tag{2.19}$$

Now we can integrate the quantization noise power over the frequency bandwidth we interest as below

$$P_e = \int_{-f_b}^{f_b} S_e{}^2(f) |N_{TF}(f)|^2 df = \int_{-f_b}^{f_b} \left(\frac{\Delta^2}{12}\right) \frac{1}{f_s} \left[2\sin\left(\frac{pf}{f_s}\right)\right]^2 df \tag{2.20}$$

When $f_b << f_s$ (i.e., OSR>>1), we can approximate $\sin((pf)/f_s)$ to be $(pf)/f_s$, so we have

$$P_e \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{p^2}{3}\right)\left(\frac{2f_b}{f_s}\right)^3 = \frac{\Delta^2 p^2}{36}\left(\frac{1}{OSR}\right)^3 \tag{2.21}$$

Now we can estimate the maximum SNR by assuming the input signal having maximum amplitude. We can obtain as

$$SNR_{\max} = 10\log(\frac{P_S}{P_E}) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{3}{p^2}(OSR)^3\right] \tag{2.22}$$

or, equivalently,

$$SNR_{\max} = 6.02N + 1.76 - 5.17 + 30\log(OSR) \tag{2.23}$$

We can see that the first-order noise shaping can give an SNR improvement for 9 dB or, 1.5 bits by doubling the OSR. This result should be compared to the 0.5 bits/octave when oversampling with no noise shaping.

2.6.2 Second-Order Sigma-Delta Modulator

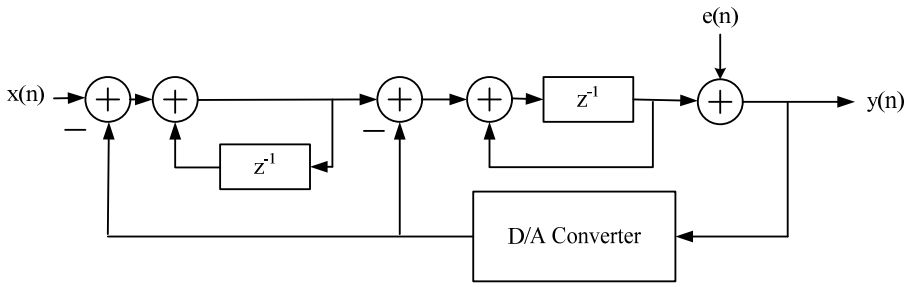


Figure 2.9 A simple block diagram of the second-order noise shaping SDM

The second-order noise shaping SDM is shown in Figure 2.9. Through the arrangement of the block diagram, we can obtain the noise transfer function, $N_{TF}(f)$, as a second-order high-pass function

$$N_{TF}(f) = (1 - z^{-1})^2 \tag{2.24}$$

and the signal is just a delay to output. The signal transfer function is given by

$$S_{TF}(f) = z^{-1} \tag{2.25}$$

Combine two signal transfer function, we obtain the output as

$$Y(z) = z^{-1} \cdot U(z) + (1 - z^{-1})^2 \cdot E(z) \tag{2.26}$$

The same as before, we interest in the magnitude of the noise transfer function can be show to given by

$$\left|N_{TF}(f)\right| = \left[2\sin\left(\frac{pf}{f_s}\right)\right]^2 \tag{2.27}$$

Integrate the quantization noise power over the frequency band of interest and use the approximation, and result is given by

$$P_e = \int_{-f_b}^{f_b} S_e{}^2(f)\left|N_{TF}(f)\right|^2 df = \int_{-f_b}^{f_b} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2\sin\left(\frac{pf}{f_s}\right)\right]^4 df$$

$$\cong\left(\frac{\Delta^2}{12}\right)\left(\frac{p^4}{5}\right)\left(\frac{2f_b}{f_s}\right)^5=\frac{\Delta^2 p^4}{60}\left(\frac{1}{OSR}\right)^5 \tag{2.28}$$

Again, assuming the maximum signal power is used, the maximum SNR for this case is given by

$$SNR_{\max}=10\log(\frac{P_S}{P_E})=10\log\left(\frac{3}{2}2^{2N}\right)+10\log\left[\frac{5}{p^4}(OSR)^5\right] \tag{2.29}$$

or, equivalently,

$$SNR_{\max}=6.02N+1.76-12.9+50\log(OSR) \tag{2.30}$$

We can see that the second-order noise shaping can give an SNR improvement for 15 dB or, 2.5 bits by doubling the OSR.

Compare with shape of zero-, first-, and second-order noise-shaping curves in Figure 2.10. The noise power decreases as the noise-shaping order increases over the band of interest. But the out-of-band noise power increases for the higher-order modulators.

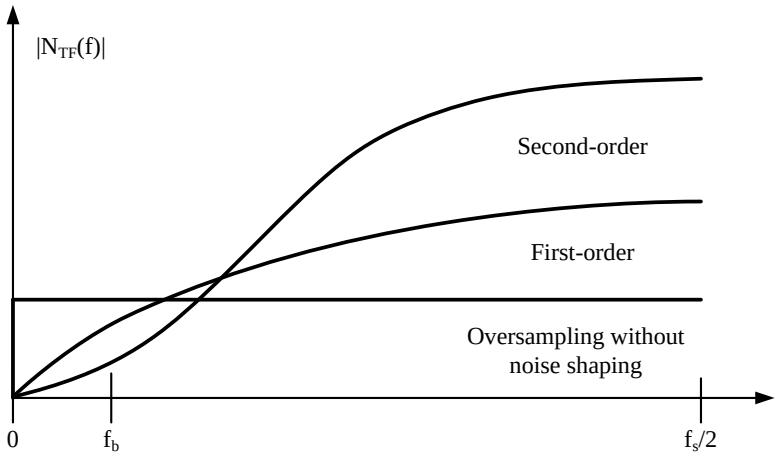


Figure 2.10 Different order noise shaping curves

2.6.3 Higher-Order Sigma-Delta Modulator

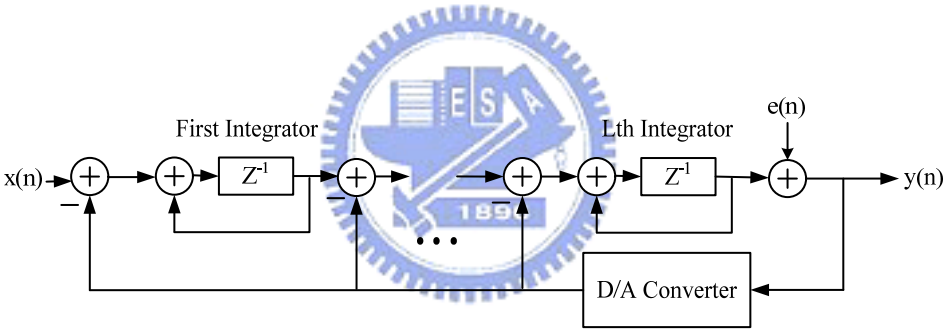


Figure 2.11 A simple block diagram of the second-order noise shaping SDM

In Figure 2.11, it shows the block diagram of the Lth-order SDM. We will discuss the behavior of the high-order SDM in mathematically. Now the noise transfer function is given by

$$N_{TF}(z) = (1 - z^{-1})^{L} \tag{2.31}$$

We let $z = e^{jwT} = e^{j2pf/f_s}$, and the magnitude is given by

$$\left|N_{TF}(f)\right| = \left[2\sin\left(\frac{pf}{f_s}\right)\right]^L \tag{2.32}$$

Integrate the quantization noise power over the frequency band of interest and use the approximation, and result is given by

$$P_e = \int_{-f_b}^{f_b} S_e{}^2(f)\left|N_{TF}(f)\right|^2 df = \int_{-f_b}^{f_b}\left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2\sin\left(\frac{pf}{f_s}\right)\right]^{2L} df$$

$$\cong\left(\frac{\Delta^2}{12}\right)\left(\frac{p^{2L}}{2L+1}\right)\left(\frac{2f_b}{f_s}\right)^{2L+1} = \frac{\Delta^2 p^{2L}}{12\cdot(2L+1)}\left(\frac{1}{OSR}\right)^{2L+1} \tag{2.33}$$

Again, assuming the maximum signal power is used, the maximum SNR for this case is given by

$$SNR_{\max} = 10\log(\frac{P_S}{P_E}) = 10\log\left(\frac{3}{2}2^{2N}\right)+10\log\left[\frac{2L+1}{p^{2L}}(OSR)^{2L+1}\right] \tag{2.34}$$

or, equivalently,

$$SNR_{\max} = 6.02N+1.76-10\log\left(\frac{p^{2L}}{2L+1}\right)+(20L+10)\log(OSR) \tag{2.35}$$

From equation (2.35) shows the information that we can improve SNR (6L+3) dB (ie., resolution will increase L+0.5 bits) by doubling OSR, or improve SNR 6.02 dB (ie., resolution will increase 1 bit) by increasing the level of the quantizer.

2.6.4 Multi-Stage Sigma-Delta Modulator (MASH) (Cascaded)

There is a problem to improve SNR by increasing the order of the SDM. Modulators with more than two integrators suffer from potential instability owing to the accumulation of large signals in the integrators. Another approach for realizing high-order modulators is to use a cascade-type structure where the overall higher-order modulators is constructed using lower-order ones. The advantage of this approach is that since the lower-order modulators are more stable, the overall system should remain stable. Such an arrangement has been called MASH (Multi-stAge noise SHaping) [5].

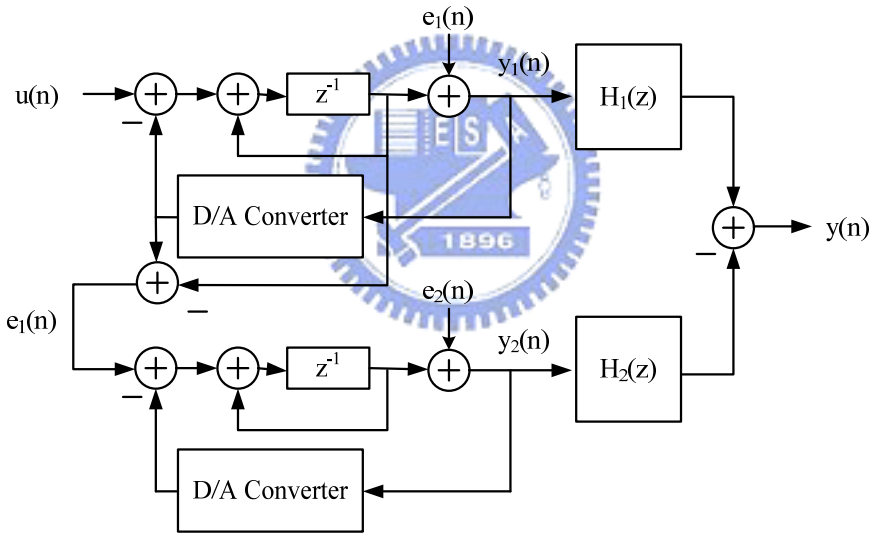


Figure 2.12 A second-order MASH modulator using two first-order modulators

The basic ideal is to pass along the quantization error of the first stage to another modulator and combine the outputs using digital filter. Then, the arrangement will remove the quantization error of the first stage, and left only the second section's quantization noise of the second stage which has been filtered twice.

A second-order MASH modulator using two first-order modulators is shown in Figure 2.12. We can see that the output of the first stage is given by

$$\begin{aligned} Y_1(z) &= S_{TF1}(z)U(z) + N_{TF1}(z)E(z) \\ &= z^{-1}U(z) + (1-z^{-1})E_1(z) \end{aligned} \tag{2.36}$$

and the output of the second stage is given by

$$\begin{aligned} Y_2(z) &= S_{TF2}(z)E_1(z) + N_{TF2}(z)E_2(z) \\ &= z^{-1}E_1(z) + (1-z^{-1})E_2(z) \end{aligned} \tag{2.37}$$

Now we design the digital filter stage H_1 and H_2 at the outputs of the two modulators. The goal is to remove the quantization noise of the first stage, and this can achieve if the condition

$$H_1 \cdot N_{TF1} - H_2 \cdot N_{TF2} = 0 \tag{2.38}$$

holds. The simplest choice for H_1 and H_2 are $H_1 = S_{TF2} = z^{-1}$ and $H_2 = N_{TF1} = (1-z^{-1})$. The overall output is given by

$$Y(z) = z^{-2}U(z) - (1-z^{-1})^2 E_2(z) \tag{2.39}$$

Thus, a MASH approach has the advantage that higher-order noise filtering can be achieved using lower-order modulators. Since the lower-order modulator is robust, the overall MASH modulator is stable too. In similar way, we can apply this approach to complete higher-order modulator without stability problem.

2.6.5 System Analysis of Sigma-Delta Analog-to-Digital Converters

The system architecture for typical oversampling ADC is shown in Figure 2.13. The analog domain includes anti-aliasing filter, sample-and-hold, and SDM. The digital domain includes decimation filter which contains as digital low-pass filter and a down-sampling. The anti-aliasing filter is used to filter the out-of-band noise of original input signal to avoid noise folding into signal band after sampled and held. Then, the sample-and-held transform the signal filtered from the anti-aliasing filter to the signal which has the same value during sampling time, and its value is equal to the original signal at the moment when the sampling occurring. Next, SDM push the quantization noise power to high frequency domain, and transform the output to digital domain. The digital low-pass filter will remove any higher-frequency signal content that was originally on the input signal, and downsample the sampling frequency to Nyquist-rate. Note that the digital low-pass filter here is like an anti-aliasing filter to limit signals to one-half the output sampling rate. The decimation filters generally are implemented using digital circuit technique in order to reduce the power dissipation and are easy to implement. Figure 2.14 shows the signal and spectra of each stage of oversampling ADC [01]. There are example signal spectra of an oversampling A/D converter with one bit quantizer in figure, and we can obtain more acquaintance with the overall system.

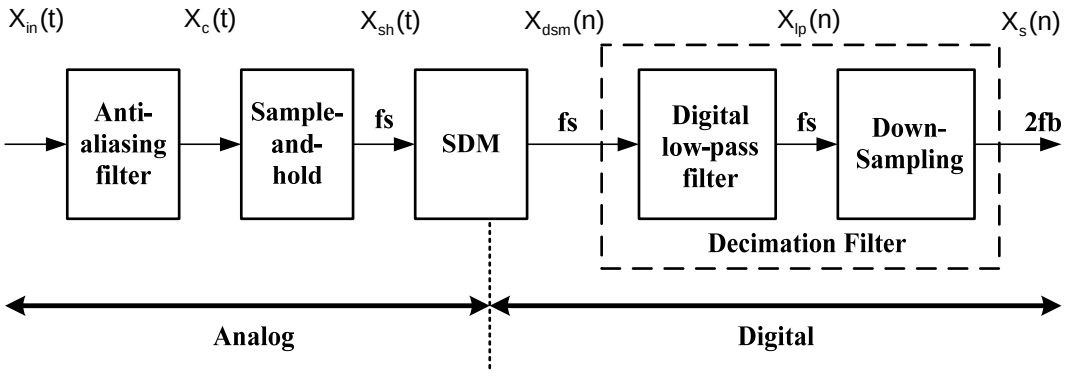


Figure 2.13 Block diagram of an oversampling A/D converter

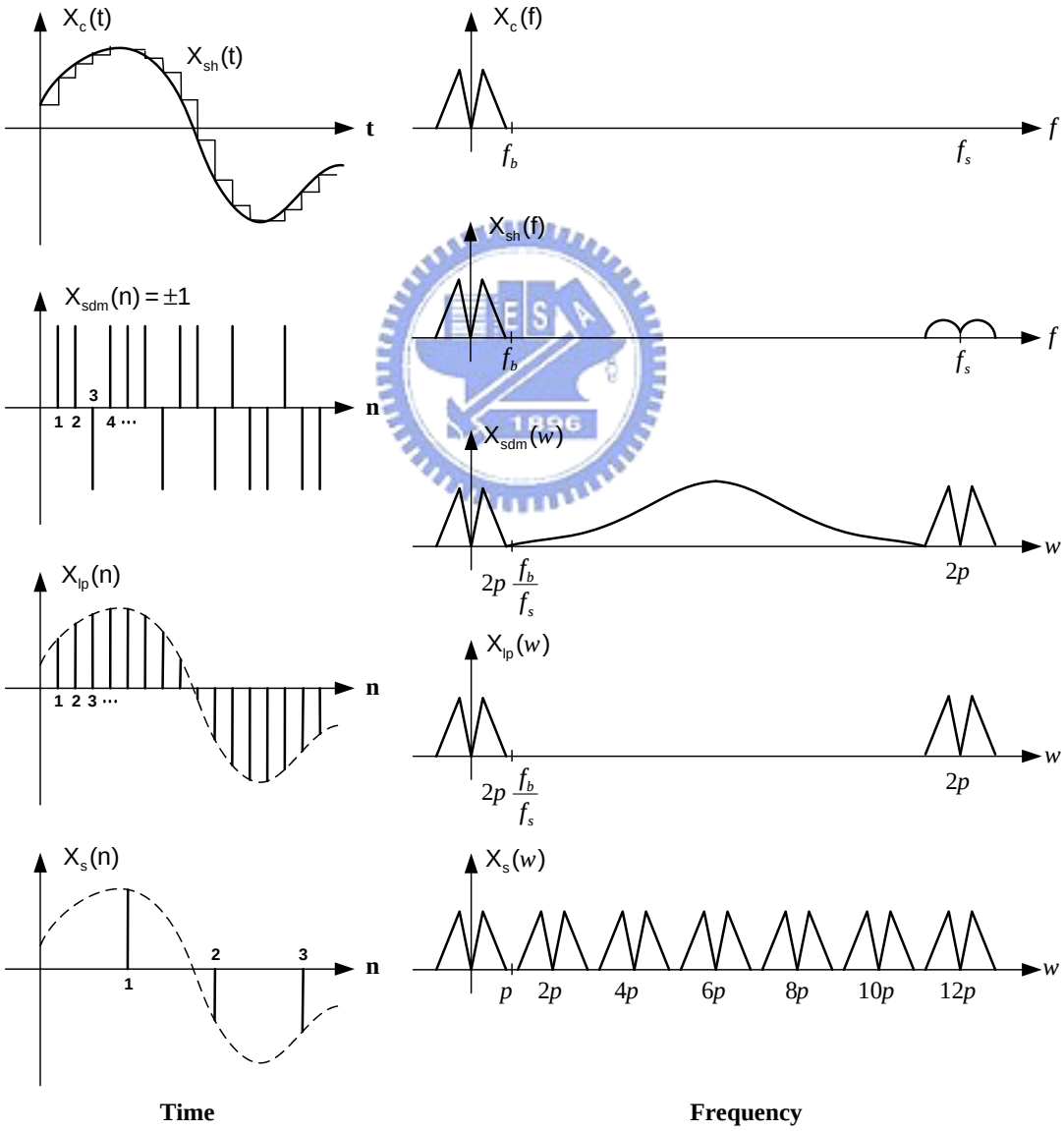


Figure 2.14 Signal and spectra in an oversampling ADC

2.7 Digital Decimation Filter

Although there are many techniques for realizing digital decimation filters for oversampling A/D converter, we discuss the multi-stage decimation filters in this section [01].

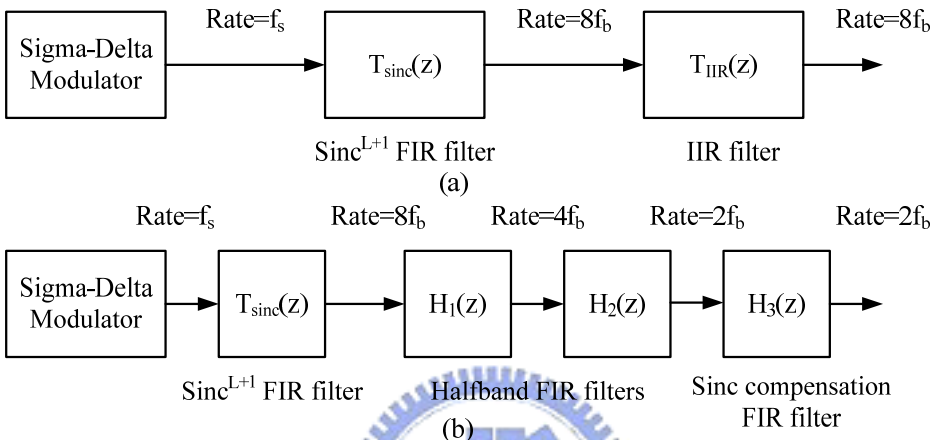


Figure 2.15 Multi-stage decimation filters: (a) sinc followed by an IIR filter; (b) sinc followed by halfband filters

One method for realizing decimation filters is to use a multi-stage approach, as shown in Figure 2.15. The first-stage Sinc^{L+1} FIR filter removes out of band quantization noise and down sample the signal to four times the Nyquist rate. The second-stage can be an IIR filter or a cascade of FIR filters to down sample the output of the first-stage to Nyquist rate. The first-stage Sinc^{L+1} FIR filter is a cascade of L+1 averaging filters where the transfer function of a single averaging filter, $T_{avg}(z)$, is given by

$$T_{avg}(z) = \frac{Y(z)}{U(z)} = \frac{1}{M}\sum_{i=0}^{M-1} z^{-i} \tag{2.40}$$

where M is the integer ratio of f_s to 8 f_b. Then, rewrite (2.40) we can see the frequency response of an averaging filter, $T_{avg}(z)$, is given by

$$MY(z) = \left(\sum_{i=0}^{M-1} z^{-i} \right) U(z) = (1 + z^{-1} + z^{-2} + \mathbf{L} + z^{-(M-1)}) U(z) \tag{2.41}$$

which can also be rewritten as

$$\begin{aligned} MY(z) &= (z^{-1} + z^{-2} + \mathbf{L} + z^{-M}) U(z) + (1 - z^{-M}) U(z) \\ &= Mz^{-1} Y(z) + (1 - z^{-M}) U(z) \end{aligned} \tag{2.42}$$

Finally, we group together Y(z) terms an find the transfer function of this averaging filter can also be written in the recursive form as

$$T_{avg}(z) = \frac{Y(z)}{U(z)} = \frac{1}{M} \left(\frac{1 - z^{-M}}{1 - z^{-1}} \right) \tag{2.43}$$

The frequency response for this filter is found by substituting $z = e^{j\omega}$, which results in

$$T_{avg}(e^{jw}) = \frac{\sin c\left(\frac{wM}{2} \right)}{\sin c\left(\frac{w}{2} \right)} \tag{2.44}$$

Where sinc(x) $\equiv$ sin(x)/x.

A cascade of L+1 averaging filter has the response $T_{avg}(z)$ given by

$$T_{\sin c}(z) = \frac{1}{M^{L+1}}\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^{L+1} \tag{2.45}$$

The reason for choosing to use L+1 of these averaging filters in cascade is similar to argument that the order of the analog low-pass filter in an oversampling D/A converter should be higher than the order of the sigma-delta modulator. An efficient way to realize this cascade-of-averaging filter is to write (2.45) as

$$T_{\sin c}(z) = \left(\frac{1}{1-z^{-1}}\right)^{L+1}(1-z^{M})^{L+1}\frac{1}{M^{L+1}} \tag{2.46}$$

and thus realize it as shown in Figure 2.16 [10].

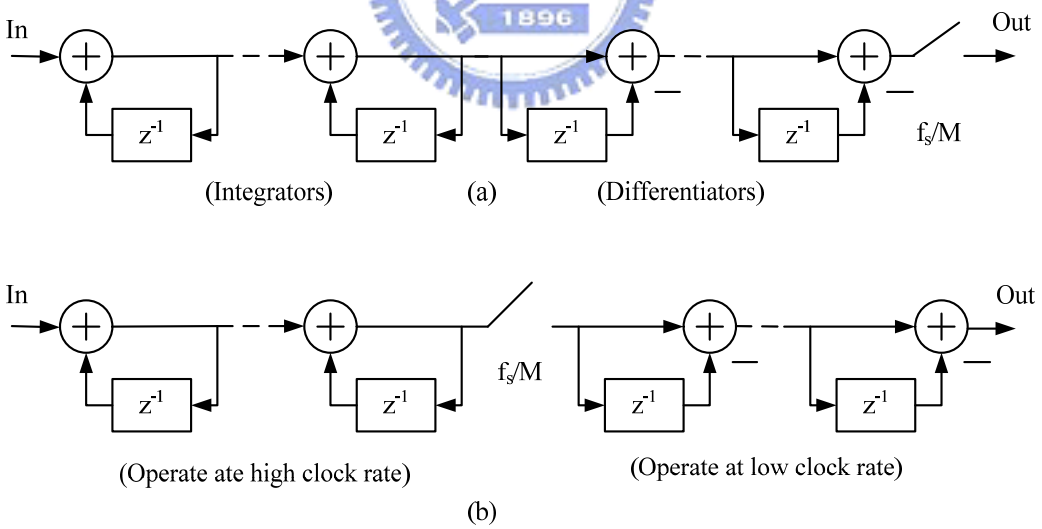


Figure 2.16 Realizing Tsinc(z) as a cascade of integrators and differentiators: (a) downsampling performed after all the filtering; (b) a more efficient method where downsampling is done before the differentiators

2.8 Summary

In this chapter, we have introduced the basic principles of sigma-delta modulator. The advantages of the sigma-delta modulator are obtained form oversampling and noise shaping. By oversampling, the quantization noise is uniformly distributed over $\pm f_s/2$, and there is a little part of original quantization noise in our interesting bandwidth. Then, by feedback arrangement, noise shaping suppress the noise power in signal bandwidth, and improve SNR. Here, various architectures of SDM such as single-loop and cascaded was introduced and compared. Besides, we discuss the overall architecture of the oversampling A/D converter, and describe how the signals change in different sections. Subsequently, we give an example to show the signal and spectra of each stage of oversampling ADC. Finally, we simply introduce the principle of the decimation filter. Now we get the common sense of the sigma-delta A/D converter.

Chapter 3 Basic Concept of Incremental $\Delta\Sigma$ Converters

3.1 Introduction

For instrumentation application requiring high resolution and offset cancellation, the converters are mostly based on the dual-slope principle. The drawbacks of this approach are the large external capacitors that are required for the integration of the input voltage and the relatively large conversion time [6]. Indeed, both are exponentially increasing with resolution. In [7], a better implementation , called incremental A/D converter, has been proposed. The integration of the input signal and of the voltage reference are mixed in time. This suppresses the need for large storage devices. An important feature of this converter is that it can achieve a very good offset and 1/f noise cancellation. In this chapter, the theory and application of incremental $\Delta\Sigma$ converter will be introduced first. Second, high-order single loop incremental and high-order MASH incremental will be discusses mathematically. Finally, the main problem of incremental $\Delta\Sigma$ converter are offset and charge injection problem, and offset cancellation will be described.

3.2 Theory and application of incremental $\Delta\Sigma$ converter

The first-order incremental A/D converter represents a hybrid between a Nyquist-rate dual slope converter and a $\Delta\Sigma$ one [8]. Here, we will describe the operation of the uni-polar first-order incremental A/D converter. In Figure 3.1, it is the

block diagram of the first-order incremental A/D converter including an integrator in the loop, one-bit quantizer after integrator, and a digital counter at output. The main difference is that there the integration of the input and the reference is performed separately, while here, they are alternating.

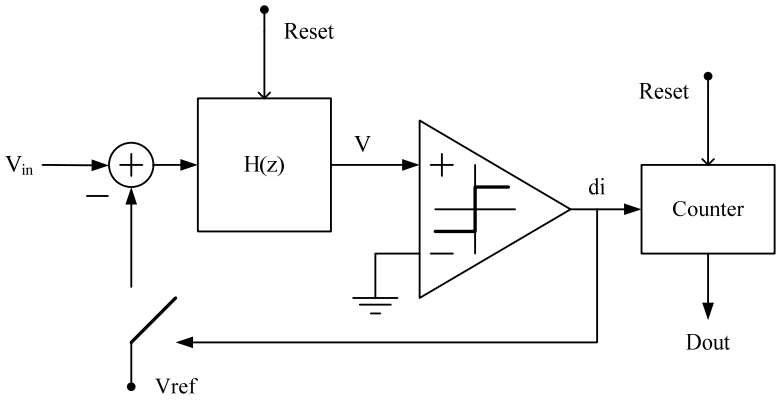


Figure 3.1 The block diagram of the first-order incremental A/D converter

We introduce the operation of this circuit step by step. Now we assume the input signal close to DC, and nearly a constant DC level. At the beginning of the conversion, the integrator in the loop and the digital counter at output are both reset. We can set the conversion time ($n = 2^{n_{bit}}$) according to the required resolution (n_{bit}). For example, if the required resolution is 6bit, the conversion time will be 2^6 steps. Whenever the input to the quantizer exceeds zero, its output becomes 1, and $-V_{ref}$ is added to the input of the analog integrator. After n steps, the output of the integrator becomes

$$V = nV_{in} - NV_{ref} \tag{3.1}$$

, where N is the number of clock periods when feed back was applied. Since this

circuit is a feedback topology, the output of the integrator V must satisfy $-V_{ref} < V < V_{in}$, it follows that

$$N = n\left(\frac{V_{in}}{V_{ref}}\right) + e \tag{3.2}$$

where e between -1 and 1. We can easily get the digital representation of the input signal N by a simple counter at the output of the modulator. Note that the residual error at the output of the integrator is

$$V = -2e_q V_{ref} \tag{3.3}$$

where e_q between -0.5 and 0.5 is the quantization error of the conversion. For example, the input signal $V_{in} = 0.075V_{ref}$, resolution $n_{bit} = 6bit$, and the conversion time $n = 64$ will be calculated. When the output of the integrator accumulates up to switch point, the output of the quantizer will becomes 1, and the input signal will be minus V_{ref} next step. After conversion, the digital representation of the input signal N is 5.

The incremental converter is structurally similar to the conventional $\Delta\Sigma$ converter, but there are significant differences: (1) the conversion is operated and realized in the form of discrete-time circuit; (2) both analog and digital integrators are reset before and after each conversion; (3) the decimating filter following the $\Delta\Sigma$ modulator can be realized with a much simpler structure (in this case, with a simple

counter).

3.3 High-order incremental converters

The biggest drawback of the first-order incremental A/D converter is that its conversion time is too long: for n-bit resolution, it needs 2^n clock periods for each conversion cycle. To reduce the number of cycles during one conversion, we can increase the order of the incremental. The main purpose is to speed up the accumulation of the integrator. In [08], high-order single loop incremental converter was described and in [9], the use of the two-stage (MASH) incremental converter was described.

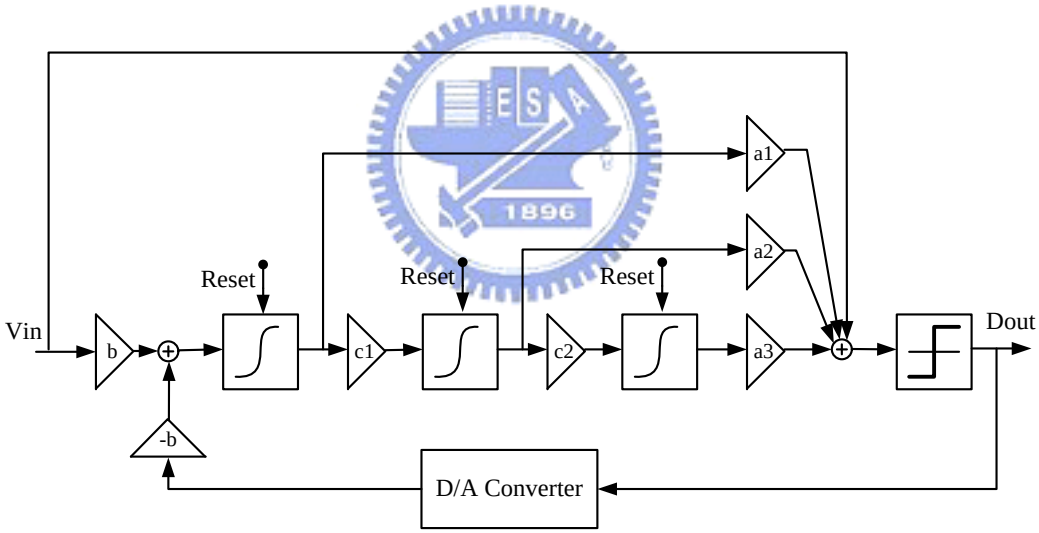


Figure 3.2 A third-order cascaded-integrator/feed-forward modulator structure

First, we describe the high-order single loop incremental converter. The operation will be discussed in terms of a third-order cascaded-integrator/feed-forward modulator structure shown in Figure 3.2. As in the first-order modulator, all memory elements, both analog and digital, must be reset at the beginning of each conversion

cycle. We use the notations of Figure, the output of all integrators can be found in the time domain after n clock cycles. The first integrator's output samples are given by

$$
\begin{aligned}
&V_{i1}[0] = 0 \\
&V_{i1}[1] = b(V_{in}[0] - d_0 V_{ref}) \\
&V_{i1}[2] = V_{i1}[1] + b(V_{in}[0] - d_1 V_{ref}) \\
&\quad \text{M} \\
&\quad = b(V_{in}[0] + V_{in}[1] - d_0 V_{ref} - d_1 V_{ref}) \\
&V_{i1}[n] = b\sum_{k=0}^{n-1}(V_{in}[k] - d_k V_{ref})
\end{aligned}
\tag{3.4}
$$

where $d_k = \pm 1$ is the quantizer output in the k th cycle.

similarly, the second integrator's output samples are given by

$$
\begin{aligned}
&V_{i2}[0] = 0 \\
&V_{i2}[1] = c_1 V_{i1}[0] + V_{i2}[0] = 0 \\
&V_{i2}[2] = c_1 V_{i1}[1] + V_{i2}[1] = c_1(V_{i1}[1] + V_{i2}[0]) \\
&\quad \text{M} \\
&V_{i2}[n] = c_1 \sum_{l=0}^{n-1} V_{i1}[l] = c_1 b \sum_{l=0}^{n-1}\sum_{k=0}^{l-1}(V_{in}[k] - d_k V_{ref})
\end{aligned}
\tag{3.5}
$$

and the third integrator's output samples are given by

$$
\begin{aligned}
&V_{i3}[0] = 0 \\
&V_{i3}[1] = c_2 V_{i2}[0] + V_{i3}[0] = c_2 V_i 2[0] = 0 \\
&V_{i3}[2] = c_2 V_{i2}[1] + V_{i3}[1] = c_2(V_{i2}[1] + V_{i2}[0]) = 0 \\
&\quad \text{M} \\
&V_{i3}[n] = c_2 \sum_{m=0}^{n-1} V_{i2}[m]
\end{aligned}
$$

$$= c_2 c_1 b \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} \left(V_{in}[k] - d_k V_{ref} \right) \tag{3.6}$$

In the following, a constant V_{in} is assumed. In circuit design, it can be achieved by using sample-and-hold (S/H) circuit at the input of the converter. If the loop is stable for all possible dc inputs, $V_{i3}[n]$ will be bounded by $\pm V_{ref}$. Rearranging (3.6) and assuming a constant V_{in}, we can get

$$V_{i3}[n] = \frac{c_2 c_1 b (n-2)(n-1)n}{3!} V_{in} - c_2 c_1 b \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k V_{ref} \tag{3.7}$$

It is bounded by $\pm V_{ref}$, and we can get

$$-V_{ref} < \frac{c_2 c_1 b (n-2)(n-1)n}{3!} V_{in} - c_2 c_1 b \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k V_{ref} < V_{ref} \tag{3.8}$$

Rearrange (3.8) and compare with the equation $-\frac{V_{LSB}}{2} < Vin - D_{Vin} V_{LSB} < \frac{V_{LSB}}{2}$ we common used in A/D converter, we can get

$$-\frac{3!}{c_2 c_1 b (n-2)(n-1)n} V_{ref} < V_{in} - \frac{3!}{(n-2)(n-1)n} V_{ref} \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k < \frac{3!}{c_2 c_1 b (n-2)(n-1)n} V_{ref} \tag{3.9}$$

Thus, after n clock periods, an estimate of V_{in} can be found as

$$\hat{V}_{in} = D_{Vin} V_{LSB} = \frac{3!}{(n-2)(n-1)n} V_{ref} \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k \tag{3.10}$$

and D_{Vin} can be easily got from cascading three digital counter at the output of the

converter. Besides, we can find the equivalent value of the LSB voltage as

$$V_{LSB} = \frac{3!}{c_2 c_1 b(n-2)(n-1)n} V_{ref} \tag{3.11}$$

The relative quantization error (in LSBs) can also be found. It is given by

$$e_q = \frac{\hat{V}_{in} - V_{in}}{V_{LSB}} = \frac{1}{2} c_1 c_2 b \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k - \frac{1}{2} c_1 c_2 b \frac{(n-2)(n-1)n}{3!} \frac{V_{in}}{V_{ref}} \tag{3.12}$$

Hence, from (3.7)

$$V_{i3}[n] = -2V_{ref} e_q \tag{3.13}$$

Thus, the quantization error can be found in analog form at the output of the last integrator. From (3.11), the equivalent number of bits (ENOB) can be derived as

$$n_{bit} = \log_2\left(\frac{2V_{ref}}{V_{LSB}}\right) = \log_2\left(c_2 c_1 b \frac{(n-2)(n-1)n}{3!}\right)$$

$$\approx 3\log_2(n) + \log_2(c_1 c_2 b) - 2.6 \tag{3.14}$$

Where $n >> 1$ was assumed.

In design, one needs to find the lowest value of n consistent with the required resolution. However, the scale factors cannot be chosen independently since they affect the stability of the loop. We can choose these coefficients by computer to reduce the required conversion time and avoid overloading the integrators [08].

The derivations can easily be generalized to an arbitrary-order CIFF $\Delta\Sigma$ modulator. The general expression is

$$D_{Vin} = \frac{1}{C_L^n} \sum_{k_L=0}^{n-1} \sum_{k_{(L-1)}=0}^{k_L-1} \mathbf{L} \sum_{k_1=0}^{k_2-1} d_k \tag{3.15}$$

Where L is the order of the analog loop.

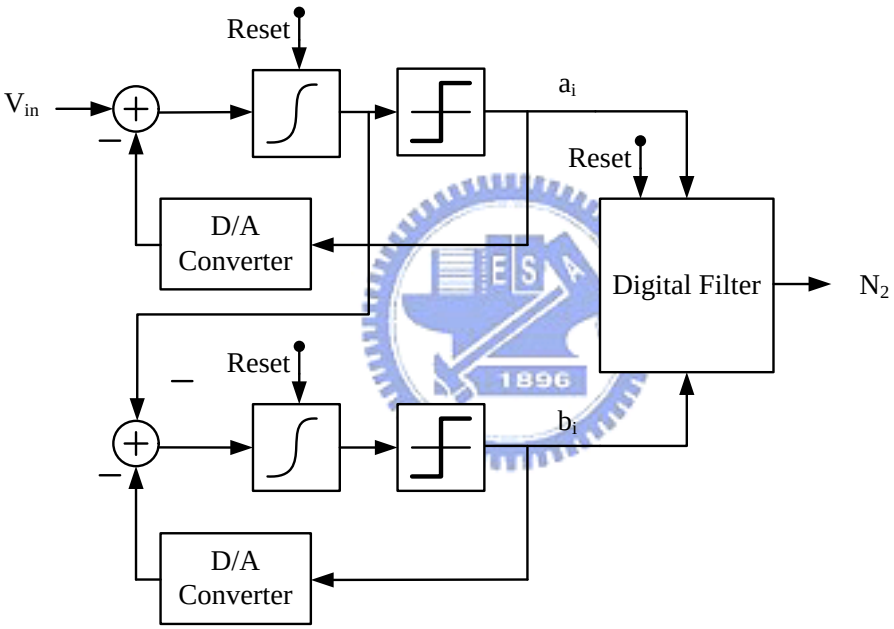


Figure 3.3 The second-order 1-1 MASH incremental A/D converter

Since the high-order single loop incremental modulator have more than two integrators in the loop, their outputs can be very large and mush be limited, which is not acceptable in the design of high-order incremental A/D converter. The high-order incremental modulator using MASH structure was proposed [08]. The second-order 1-1 MASH incremental A/D converter is shown in Figure 3.3. The stability of this

modulator is ensured because there is only one integrator in each loop. The basic operation is the same as the first-order incremental converter, and the main difference is that the first modulator delivers its output of the integrator to the input of the second modulator. The signals continue to accumulate at the output of the integrator of the second modulator, and reduce the conversion time. Next, we will describe this structure mathematically.

At the beginning of the conversion, the integrator in the loop and the digital counter at output are both reset. Assuming the input V_{in} is constant. In the first period, the output of the each integrator is given by

$$V_{i1}[1] = V_{in} - a_1 V_{ref} \tag{3.16}$$

$$V_{i2}[1] = 0 \tag{3.17}$$

In the next period, the output of the each integrator is given by

$$V_{i1}[2] = 2V_{in} - (a_1 + a_2)V_{ref} \tag{3.18}$$

$$V_{i2}[2] = V_{in} - a_1 V_{ref} - b_2 V_{ref} \tag{3.19}$$

$$V_{i1}[3] = 3V_{in} - (a_1 + a_2 + a_3)V_{ref} \tag{3.20}$$

$$V_{i2}[3] = 3V_{in} - (2a_1 + a_2)V_{ref} - (b_2 + b_3)V_{ref} \tag{3.21}$$

In the n period, we can rearrange the output of the each integrator

$$V_{i1}[n] = nV_{in} - \sum_{i=1}^{n} a_i V_{ref} \tag{3.22}$$

$$V_{i2}[n] = (n-1)nV_{in}/2 - \sum_{i=1}^{n-1} a_i (n-i)V_{ref} - \sum_{i=2}^{n} b_i V_{ref} \tag{3.23}$$

and in the $n+1$ period, we can obtain

$$V_{i2}[n+1] = n(n+1)V_{in}/2 - \sum_{i=1}^{n} a_i (n+1-i)V_{ref} - \sum_{i=2}^{n+1} b_i V_{ref} \tag{3.24}$$

Again, it can be shown that the dynamic range of $V_{i2}[n+1]$ is given by

$$-V_{ref} \le V_{i2}[n+1] \le V_{ref} \tag{3.25}$$

with (3.24), (3.25) can be rewritten in the form of

$$-V_{ref} \le n(n+1)V_{in}/2 - \sum_{i=1}^{n} a_i (n+1-i)V_{ref} - \sum_{i=2}^{n+1} b_i V_{ref} \le V_{ref} \tag{3.26}$$

Rearranging (3.26) is given by

$$-\frac{2}{n(n+1)}V_{ref} \le V_{in} - \left\{\sum_{i=1}^{n} a_i (n+1-i) + \sum_{i=2}^{n+1} b_i\right\}\frac{2}{n(n+1)}V_{ref} \le \frac{2}{n(n+1)}V_{ref} \tag{3.27}$$

Compare with the ideal A/D converter quantization error is normally given by

$$-\frac{V_{LSB}}{2} < Vin - D_{Vin}V_{LSB} < \frac{V_{LSB}}{2} \tag{3.28}$$

We can obtain the digital code of V_{in} N_2, V_{LSB}, and resolution n_{bit} as follow

$$V_{LSB} = \frac{4}{n(n+1)} V_{ref} \tag{3.29}$$

$$N_2 = \left\{ \sum_{i=1}^{n} a_i (n+1-i) + \sum_{i=2}^{n+1} b_i \right\} \tag{3.30}$$

$$n_{bit} = \log_2 \left(\frac{2V_{ref}}{V_{LSB}} \right) = \log_2 [n(n+1)] - 1$$

$$= 2\log_2 (n) - 1 \quad \text{if} \quad n >> 1 \tag{3.31}$$

As an example, a 16-bit resolution, which requires from (3.31) that n=362.

An extra-bit accuracy can be obtained by detecting the sign of $V_{i2}[n+1]$ at the end of the conversion cycle. This can be achieved without increasing significantly the conversion time. Equations (3.29)-(3.31) are replaced by

$$V_{LSB} = \frac{2}{n(n+1)} V_{ref} \tag{3.32}$$

$$N_2 = \left\{ \sum_{i=1}^{n} a_i (n+1-i) + \sum_{i=2}^{n+1} b_i \right\} + sign(V_{i2}[p+1]) \tag{3.33}$$

$$n_{bit} = \log_2 [n(n+1)] \tag{3.34}$$

Hence, for a 16-bit resolution, a total number of $n+1$=257 integration periods is required for each conversion cycle.

We can extended to a Lth (L>2) order incremental A/D converter. Due to the use of a multistage structure, there are no overload effects even if L>2. The resolution of Lth-order incremental is given by

$$n_{bit} = \log_2\left\{\left[\prod_{i=1}^{L}(n+i-i)\right]\Big/ L!\right\}+1$$

$$= L\log_2(n) - \log_2(L!) + 1 \qquad (3.35)$$

and the total number of integration periods becomes $N_{IP} = n + L - 1$ required for each conversion cycle as a function of the resolution and the order.

After optimization the coefficients of the single-loop high-order incremental A/D converter, we compare the conversion cycle of multistage high-order incremental A/D with the conversion cycle of the single-loop high-order incremental A/D converter, and we will find that the conversion cycle of the multistage high-order structure is better than the conversion cycle of the single-loop high-order structure at the same resolution. Besides, the stability of the multistage high-order modulator is ensured because it only has one integrator in each loop.

3.4 Offset and charge injection compensation

The above discussion ignored the errors introduced by the offset voltage of the op amp and by charge injection due to the clock-feedthrough effect. These errors must be compensated to avoid reducing resolution. Through circuit technique, these errors can be constant (i.e., it is signal independent). There are two way to compensate constant errors, the digital error compensation method and the analog error compensation method.

3.4.1 Conversion using analog error compensation

The analog error compensation method use discrete-time circuit technique in Figure 3.4 [09]. In this circuit, $G_{m1}R$ is the gain of the opamp used in the integrator, while G_{m2} is an attenuator stage. The G_{m2} compensation circuit is not in the signal path. The original frequency/speed performance can be maintained.

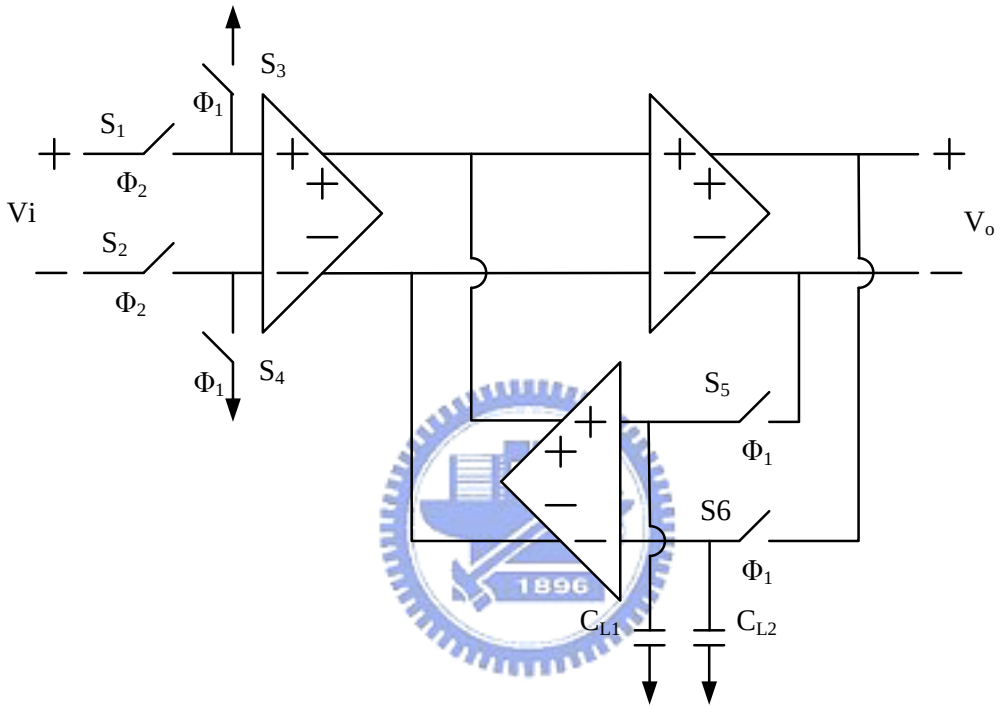


Figure 3.4 The analog error compensation method use discrete-time circuit technique

During reset mode ($f_1 = 1$), we can obtain

$$V_o = V_{OS1} \cdot G_{m1}R + (V_{OS2} - V_o) \cdot G_{m2}R \tag{3.36}$$

where V_{OS1} and V_{OS2} are the input-referred offset of the $G_{m1} - R$ and $G_{m2} - R$ pairs. Then, we rearrange (3.36), and obtain the output of the opamp used in the integrator

$$V_o = \frac{V_{OS1} \cdot G_{m1}R + V_{OS2} \cdot G_{m2}R}{1 + G_{m2}R} \tag{3.37}$$

and, we approximate (3.37), if $G_{m2}R >> 1$

$$V_o \approx V_{OS1} \cdot \frac{G_{m1}}{G_{m2}} + V_{OS2} \tag{3.38}$$

During reset mode ($f_1 = 2$), we can obtain ,

$$V_o = V_i \cdot G_{m1}R + V_{OS1} \cdot \frac{G_{m1}}{G_{m2}} + V_{OS2} + \Delta V \cdot G_{m2}R$$

$$= G_{m1}R\left(V_i + \frac{V_{OS1}}{G_{m2}R} + \frac{V_{OS2}}{G_{m1}R} + \Delta V \frac{G_{m2}}{G_{m1}} \right) \tag{3.39}$$

Then, (3.39) divide by $G_{m1}R$, and the input-referred offset is given by

$$V_{OS,in} = \frac{V_{OS1}}{G_{m2}R} + \frac{V_{OS2}}{G_{m1}R} + \Delta V \frac{G_{m2}}{G_{m1}} \tag{3.40}$$

where ΔV is due to the mismatch between the switching errors of $S5$ and $S6$. Its effect on V_o can be reduced by making G_{m2}/G_{m1} small.

3.4.2 Conversion using analog error compensation

The digital error compensation method has been proposed in [08]. In order to compensate the effect of the input-independent offset caused by switches and amplifier, the conversion cycle is divided into three periods preceded by a reset of

each integrator output and a sample and hold of input.

(1) During the first period, which requires N_{IP} integration periods, the operation of the modulator has been described. The output of the last integrator V_L is given by

$$V_L[N_{IP}] = \left\{\prod_{i+1}^{L}(p+i-1)\right\}V_{in}/L! + F_1(a,b,\mathbf{L},V_{ref},p,L) + \sum_{i=1}^{L}\left\{2V_{os}\prod_{j=1}^{L}(p+L-j)\right\}\Big/(L-i+1) \quad (3.41)$$

where $F_1(a,b,\mathbf{L},V_{ref},p,L)$ represents the voltage component of V_L related to the reference voltage.

(2) During the second period, the output voltages of the first $L-1$ integrators are reset ($V_i[p+L]=0$, $1 \le i \le L-1$), while $V_L[N_{IP}]$ is inverted:

$$V_L[N_{IP}+1] = -V_L[N_{IP}] \quad (3.42)$$

(3) During the third period, which requires N_{IP} integration periods, the circuit operation is analogous to that of the first period, except that the voltage V_1 integrates $-V_{in}$ instead of V_{in}. The output of the last integrator V_L is given by

$$V_L[2N_{IP}+1] = -\left\{2\left(\prod_{i=1}^{L}(p+i-1)\right)V_{in}/L! + F2(a,b,\mathbf{L},V_{ref},p,L)\right\} \quad (3.43)$$

Then, all error terms have disappeared. It can be shown that resolution is now given

by

$$n_L = \log 2\left\{\prod_{i=1}^{L}(p+L+1)\right\}\Big/ L!+2$$
$$= L\log(p) - \log 2(L!) + 2 \quad \text{[bits]}, \quad \text{if} \quad p >> 1. \tag{3.44}$$

After compensation, the total number of integration periods $N_{IPC} = 2p + L$ required for each conversion cycle as a function of the resolution and the order.

3.5 Summary

In this chapter, we introduce the theory of the incremental converter for instrumentation application requiring high resolution and offset cancellation. Then, we discuss the trade off between resolution and conversion time mathematically. In order to reduce conversion time, high-order converters in the form of single loop or multistage have been introduced. Besides, the offset and charge injection compensation using analog compensation and digital compensation have discussed. Now we get the common sense of the incremental A/D converter.

Chapter 4 Design of Configurable Dual-mode Low-distortion A/D Converter

4.1 Introduction

This chapter introduces the design of configurable dual-mode low-distortion A/D converter. It will focus on how to merge the MASH sigma-delta and incremental A/D modes using low-distortion architecture. In system level, we will discuss how to merge two function circuits and introduce the basic building block of the configurable dual-mode low-distortion A/D converter. Next, the behavior mode will be constructed and checked by MATLAB. Then, we implement this circuit in circuit level and considerate its non-ideal effects. Finally, we will show the whole chip performance and layout of this circuit.

4.2 System consideration

Before determining the basic block diagram of this circuit, we should know the concept of the incremental and sigma-delta. Now the basic concept block diagram is shown in Figure 4.1. Although there are different types to implement incremental function, they have the same basic concept that is through the feedback to control the output of the integrator distributing between $-V_{ref}$ and V_{ref}. Then, compare this relation to $-\frac{V_{LSB}}{2} < V_{in} - D_{vin} < \frac{V_{LSB}}{2}$ which we usually use to check the resolution of ADCs.

There is an example to show the function of the incremental modulator. As shown in Figure 4.1, no matter what order or architecture it has the same concept. When the loop is running, the output of the last integrator is given

$$-V_{ref} < (N_{vin}) \times V_{in} - (Na_i) \times V_{ref} < V_{ref} \tag{4.1}$$

where N_{vin} and N_{ai} are the coefficients which the input and V_{ref} accumulate at the output of the last integrator respectively. We can rearrange (4.1) to

$$-\frac{V_{ref}}{(N_{vin})} < V_{in} - \frac{(Na_i)}{(N_{vin})} \times V_{ref} < \frac{V_{ref}}{(N_{vin})} \tag{4.2}$$

Ideal ADC quantization error is normally given by

$$-\frac{V_{LSB}}{2} < V_{in} - D_{vin} < \frac{V_{LSB}}{2} \tag{4.3}$$

Now we can define the V_{LSB} and D_{vin} as

$$V_{LSB} = \frac{2V_{ref}}{(N_{vin})} \tag{4.4}$$

$$D_{vin} = \frac{(Na_i)}{2} \times V_{LSB} \tag{4.5}$$

We can even know the relation of the conversion time and resolution if we can get N_{vin} and N_{ai}. Definitely, we can trace the output of the modulator to the last integrator and let it through the same type digital accumulator. Then the output of the digital accumulator will be N_{ai}, and so does N_{vin}.

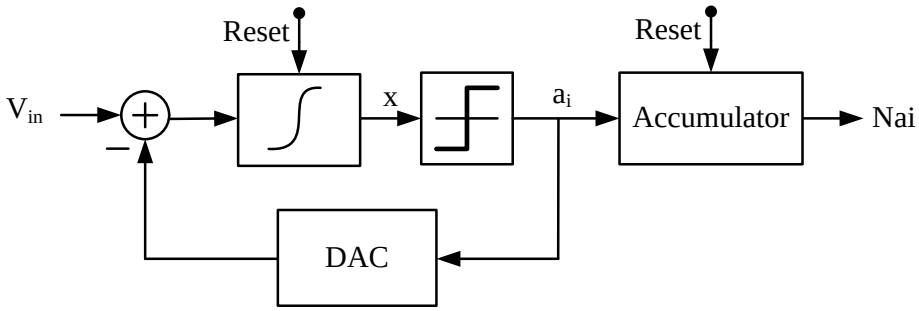


Figure 4.1 The basic concept of the the incremental modulator

The second-order incremental A/D converter was proposed [09], but we know the incremental modulator must sequentially accumulate the signal in the loop and it is not suitable to sigma-delta modulator because the action of creating quantization of the first stage. On configurable oversampled A/D converter was proposed [06]. This circuit controls its feedback delay in order to let the output of the integrator to be the quantization noise. This arrangement can make this merge function work, but the trade off is its addition capacitor. Using separate capacitor of the input and reedback will affect the coefficient of the modulator. Besides, more capacitor at the input terminal will cause lager capacitor area in design because of the thermal noise consideration.

The feedforward low-distortion topology was proposed [11]. This topology can reduce sensitivity to opamp nonlinearities and improve input signal range. By using this topology, high-order design need only one feedback path. This advantage is very remarkable when design multi-bit quantizer in the loop. Besides, it simplify MASH architectures. We explain these advantages as below.

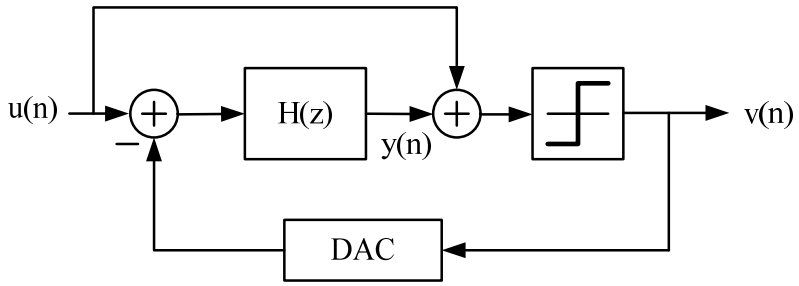


Figure 4.2 The first-order low-distortion topology

Figure 4.2 show the first-order low-distortion feedforward topology. Through arrangement, feedforward topology can maintain the original transfer function. First, the signal and noise transfer function is given by

$$STF(z) = \frac{1+H}{1+H} = 1 \tag{4.6}$$

$$NTF(z) = \frac{1}{1+H}(1-z^{-1}) \tag{4.7}$$

Where $H(z) = \frac{z^{-1}}{1-z^{-1}}$

Second, we calculate the output of the integrator as follow.

$$\begin{aligned} Y(z) &= H(z)\cdot[U(z)-V(z)] \\ &= H(z)\cdot\{U(z)-[U(z)+NTF(z)\cdot Q(z)]\} \\ &= -H(z)\cdot NTF(z)\cdot Q(z) \\ &= -z^{-1}Q(z) \end{aligned} \tag{4.8}$$

It is quite obvious that the output of the integrator is only a delay of the

quantization noise without input signal. In other word, the filter does not deal with the input signal and the input signal directly feed forward to the input of the quantizer. This can improve input signal range because the signal will not be limited by the opamp nonlinearities. Therefore, the need of the sensitivity to opamp nonlinearities is decrease. Moreover, because the quantization noise is just at the output of the integrator, we can directly let it to the next stage without any additional circuit when design MASH architectures.

Now we design the second-order incremental modulator using mash 1-1 low-distortion topology as Figure 4.3. Since the incremental modulator need to sequentially accumulate the signal in the loop, this topology is suitable to the incremental modulator, and it can achieve more advantages. As above discussion, we trace the output of each quantizer, and let it through the same path using digital accumulators. Therefore, the V_{LSB} and D_{vin} are given by

$$V_{LSB} = \frac{2V_{ref}}{(N_{vin})} \tag{4.9}$$

$$D_{vin} = \frac{(Na_i b_i)}{2} \times V_{LSB} \tag{4.10}$$

where N_{vin} and N_{aibi} are the coefficients which the input and V_{ref} accumulate at the output of the last integrator respectively. Of course, every conversion need reset integrator first.

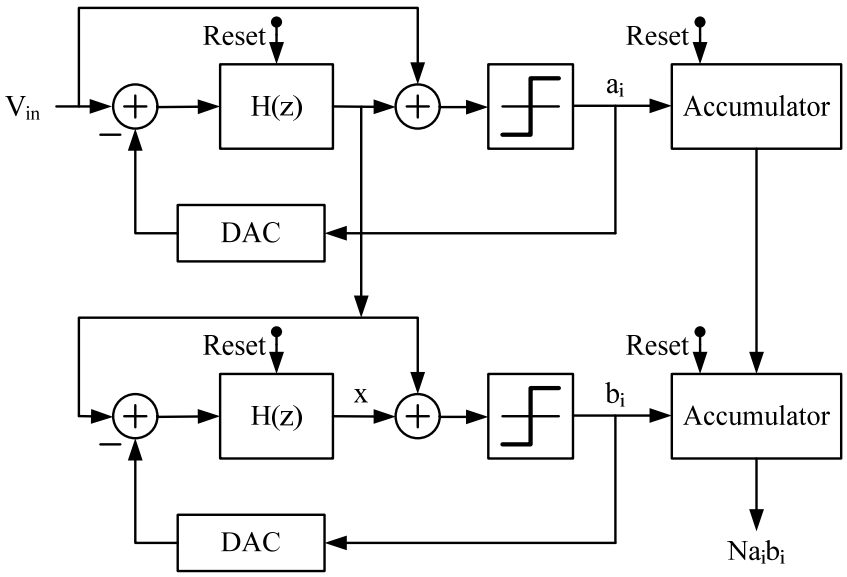


Figure 4.3 The second-order incremental modulator using mash 1-1 low-distortion topology

Figure 4.4 shows the second-order sigma-delta modulator using mash 1-1 low-distortion topology. The output of the first modulator and the second modulator are given by

$$V_{out1} = Vin + (1 - z^{-1})Q_1 \tag{4.11}$$

$$V_{out2} = -z^{-1}Q_2 + (1 - z^{-1})Q_2 \tag{4.12}$$

where Q_1 and Q_2 are the quantization noise of the first modulator and the second modulator respectively. The spirit of the MASH architectures is that the output digital filter function is to cancel the quantization noises expect the last quantization noise. Therefore, it can achieve high-order using lower-order without stability problem. Through this arrangement as Figure 4.4, the overall output of the modulator is given

by

$$V_{out} = z^{-1} \times V_{out1} + (1 - z^{-1}) \times V_{out2}$$

$$= Vin + (1 - z^{-1})^2 Q_2 \qquad (4.13)$$

where V_{out1} and V_{out2} are the output of the first stage and the second stage respectively. Therefore, we obtain the second-order sigma-delta function.

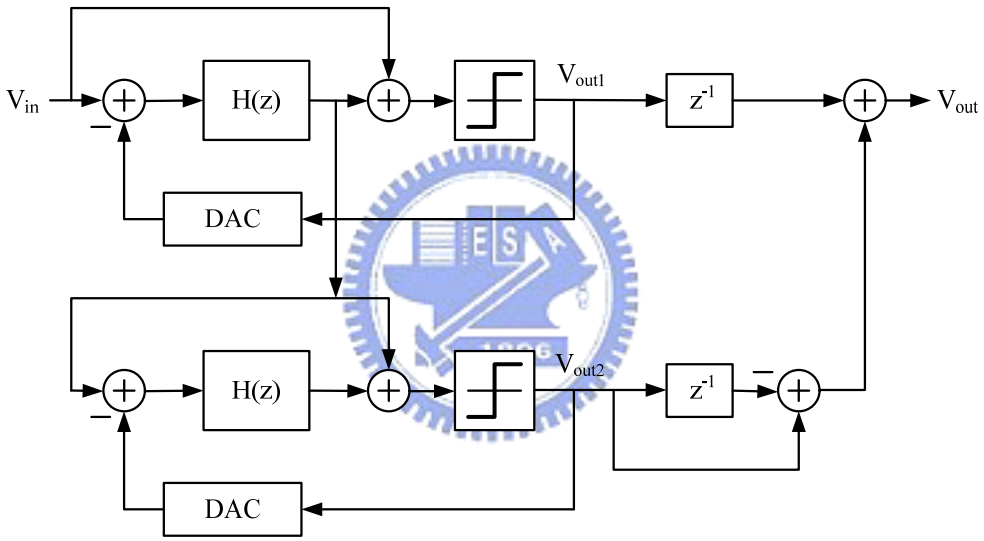


Figure 4.4 The second-order sigma-delta modulator using mash 1-1 low-distortion topology

In addition to, we also merge the digital filter follow the two type modulator [06]. The left side of Figure 4.5 shows the classical digital part of a second-order converter. The output V_{out1} and V_{out2} are from the different stages of the modulator are first separately differentiated and delayed. After that, they are added together. The result of this summation is then fed into the cascade of accumulators of the comb filter. The

simplified circuit, shown in the right side of Figure 4.5, is obtained by suppressing for each signal path the differentiations and a corresponding number of accumulations. This is achieved by feeding the different output of the stage directly into the corresponding stages of the cascade of accumulators.

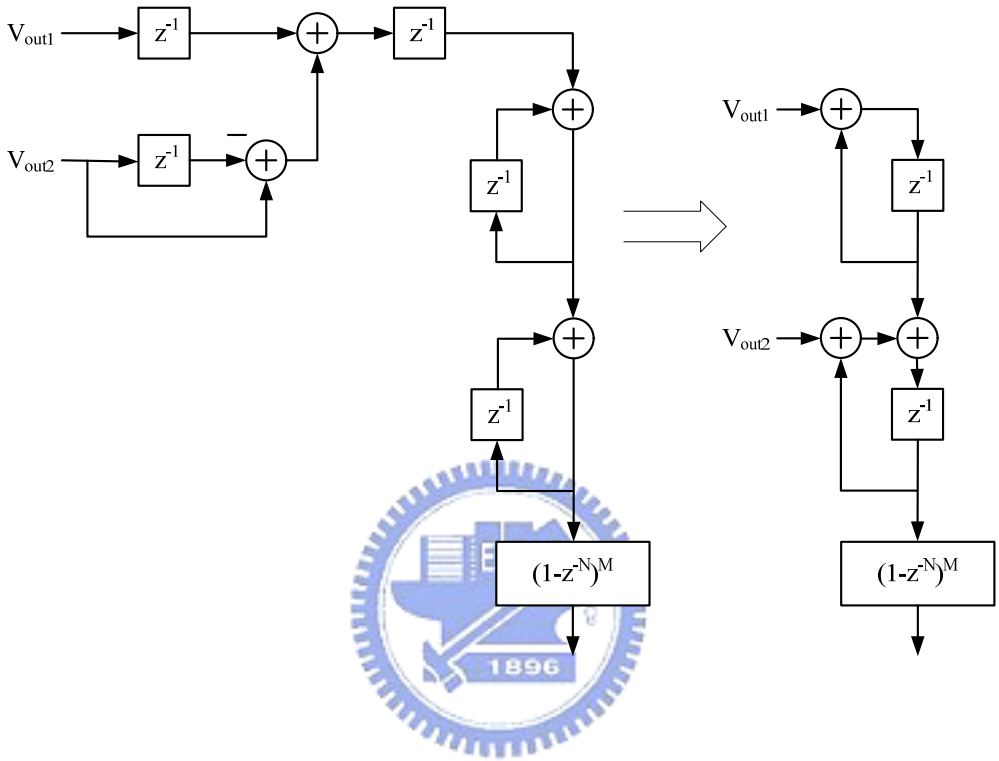


Figure 4.5 Merging digital filters of two type circuits

Finally, the proposed configurable dual-mode low-distortion A/D convert is shown in Figure 4.6. Two function circuits share most circuit except an additional digital integrator and digital differentiators. The differentiator is used only in sigma-delta conversion mode. It is shunted in the incremental conversion mode. Figure 4.6 shows the output location of two mode converter. Besides, this topology can extend to higher-order dual-mode converter. The concept circuit is shown in Figure 4.7. Understanding the trade off between the conversion time and resolution can help designer to configure the circuit to fit their requests.

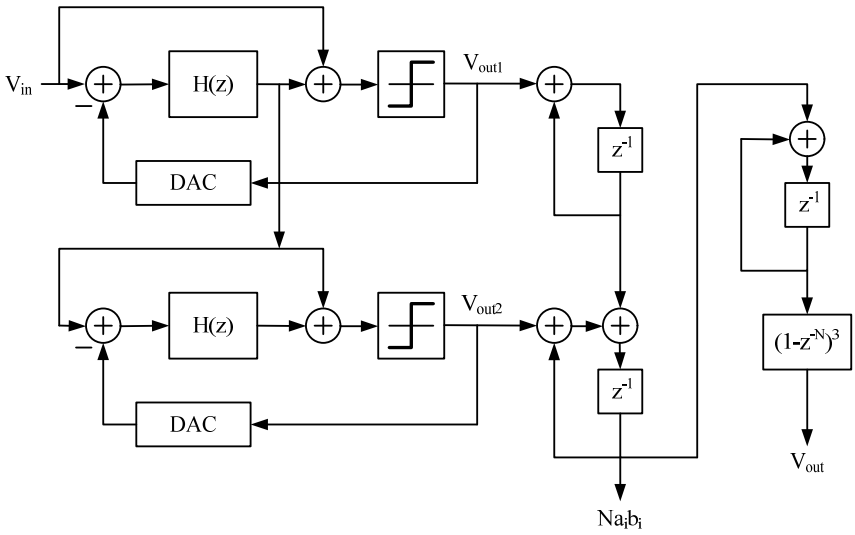


Figure 4.6 The second-order configurable dual-mode low-distortion A/D converter

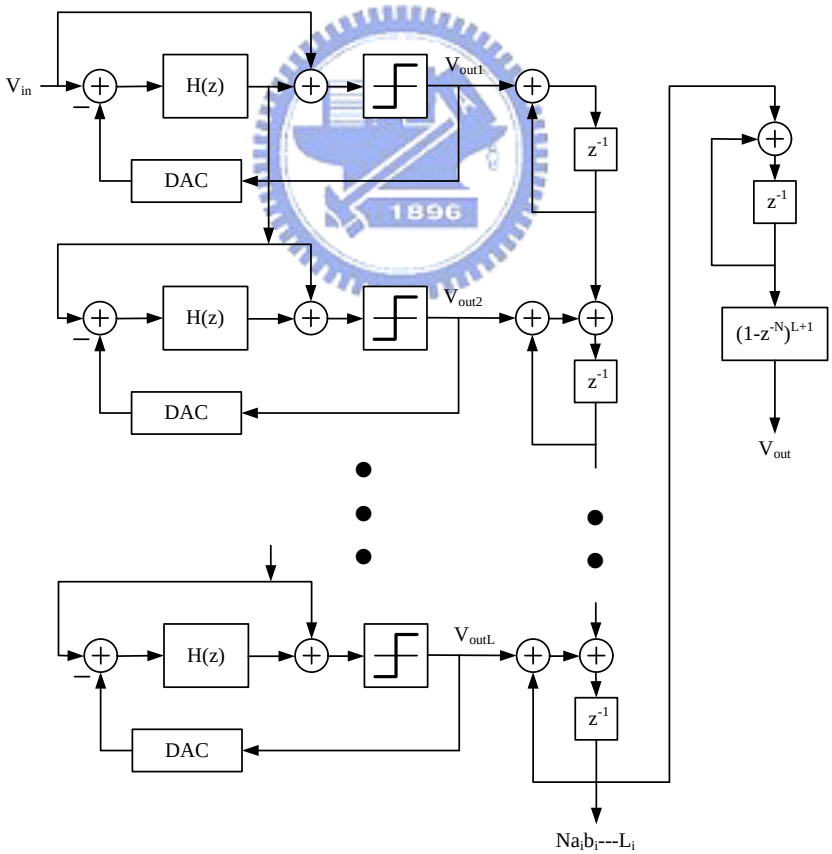


Figure 4.7 The concept of the higher-order configurable dual-mode low-distortion A/D converter

4.3 Behavior simulation

Figure 4.8 is the system architecture of the second-order configurable dual-mode low-distortion A/D converter. Before the circuit level implementation, we need to simulate the behavior of the system. Here, we used MATLAB to simulate and analysis the system performance. We need to simulate the configurable dual-mode low-distortion A/D converter in discrete-time domain as discuss above.

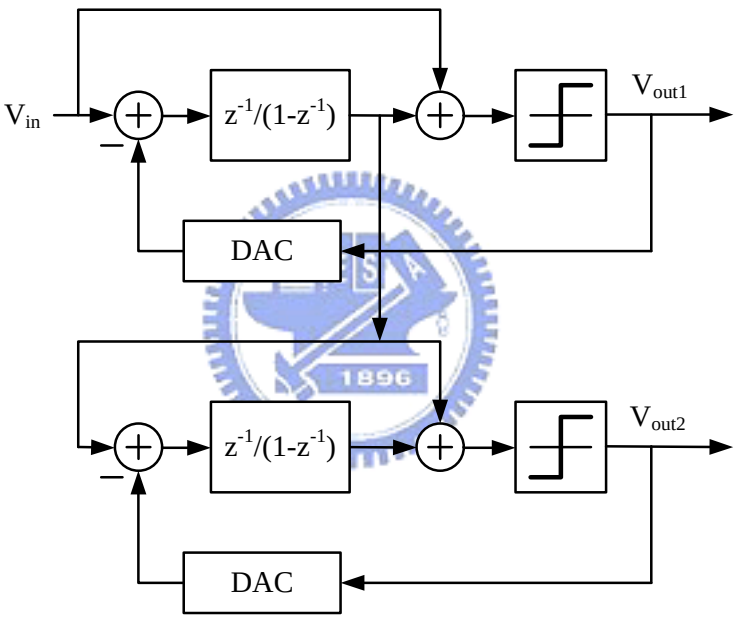


Figure 4.8 The system architecture of the second-order configurable dual-mode low-distortion A/D converter

First, we use MATLAB code to simulate the incremental mode. When this program execute, we can input the vin, nbit and clock period. Then, this program will help us to calculate the conversion time, V_{LSB}, D_{vin} and check the resolution is right or wrong. For example, the program will show

“Please input vin, nbit and T to calculate Dvin, period and Tconcersion”

Then, after inputting our configuration the program will show

vin=0.4123

nbit=16

T=1/(5.12*10^6)

Conversion period =363

VLSB =1.530432653311091e-005

Dvin =0.04122985568020

check (-VLSB/2)<(vin-Dvin)<(VLSB/2) ok

Tconversion =7.089843750000000e-005

This program can help us configure our circuit and estimate the trade off between the conversion and resolution. When simulate in circuit level, this program is very convenient for us to configure and compare with.

For sigma-delta mode, we also can use the same program to estimate the system behavior. For this design, the OSR is equal to 128 and reference voltage is equal to 0.5V. First, we should check the signal swing in each joint of the system. The signal swing of the output of each integrator is shown in the top of Figure 4.9 and the signal swing of the input of each quantizer is shown in the bottom of Figure 4.9. We get the information that the swing of the input of the quantizer will be twice of the output of the integrator. Therefore, for TSMC CMOS 0.18 μm standard process design we choose the full scale as 1V and the reference voltage as 0.5V. Second, we should observe the spectrum of each joint of the system. The spectrum of the output of each

integrator is shown in the top of Figure 4.10 and the spectrum of the input of each quantizer is shown in the bottom of Figure 4.10. As we discuss above, the output of the integrator will be the quantization noise and its spectrum should be a white noise. The reason why the spectrum of the first output of the integrator is not a white noise is that the white noise assumption for 1-bit quantizer is too rough. The quantization noise of 1-bit quantizer is greatly input dependence.

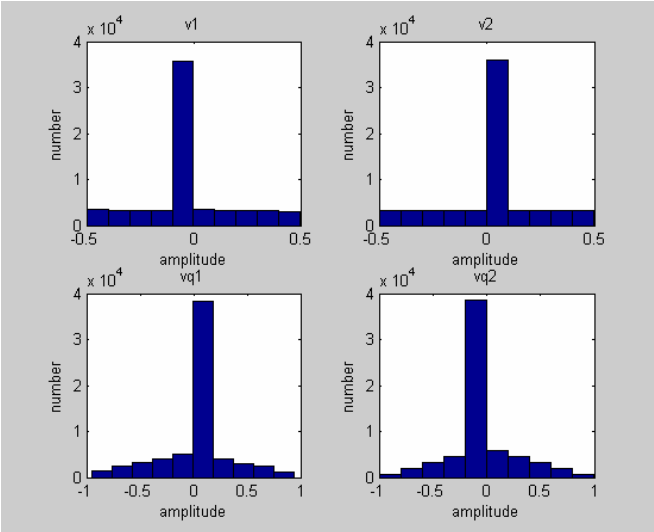


Figure 4.9 The signal swing in each joint of the system

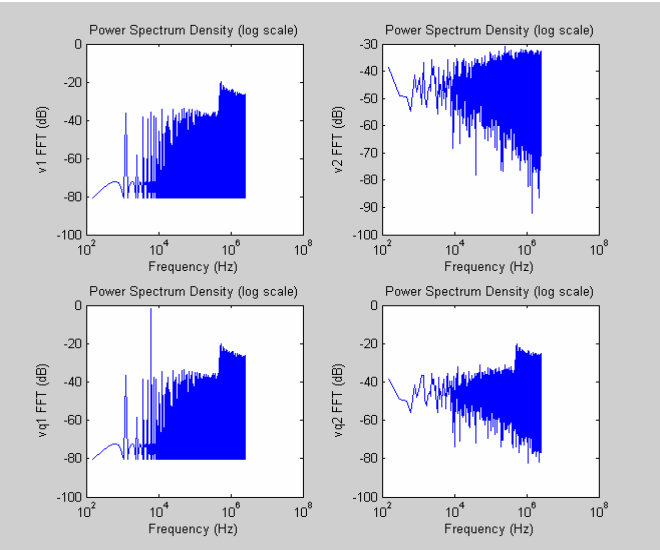


Figure 4.10 The spectrum of each joint of the system

Besides, we also can sweep the input dynamic range of the system in Figure 4.11. The dynamic range is linear without distortion and its can achieve nearly 98db.

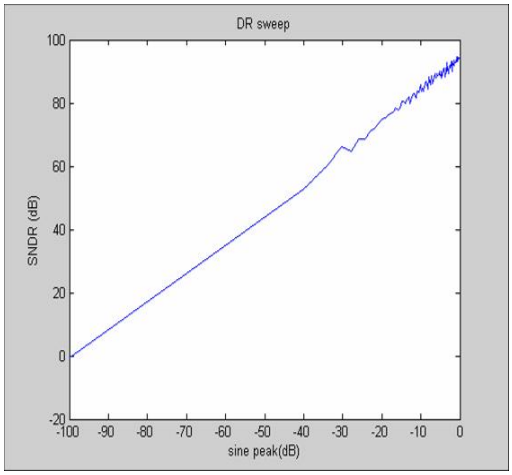


Figure 4.11 the input dynamic range of the system

Finally, the overall spectrum of the system is shown in Figure 4.12. The SNDR can achieve 91.58db where the input is a sine wave with 0.4V amplitude. Because the circuit level simulation time is too large, choosing appropriate input amplitude is importance. We simulate this performance in system level for checking the subsequent performance in circuit level.

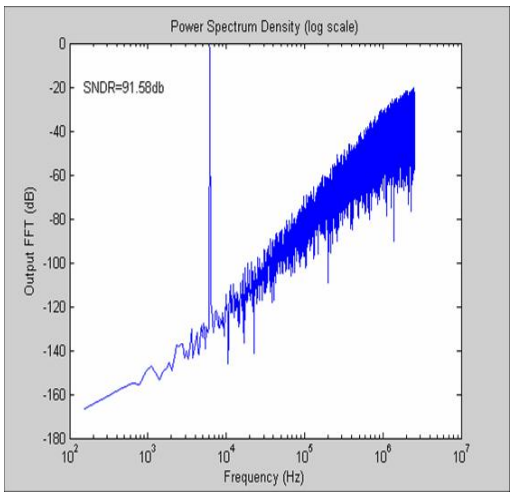


Figure 4.12 The overall spectrum of the system

4.4 Circuit level implementation

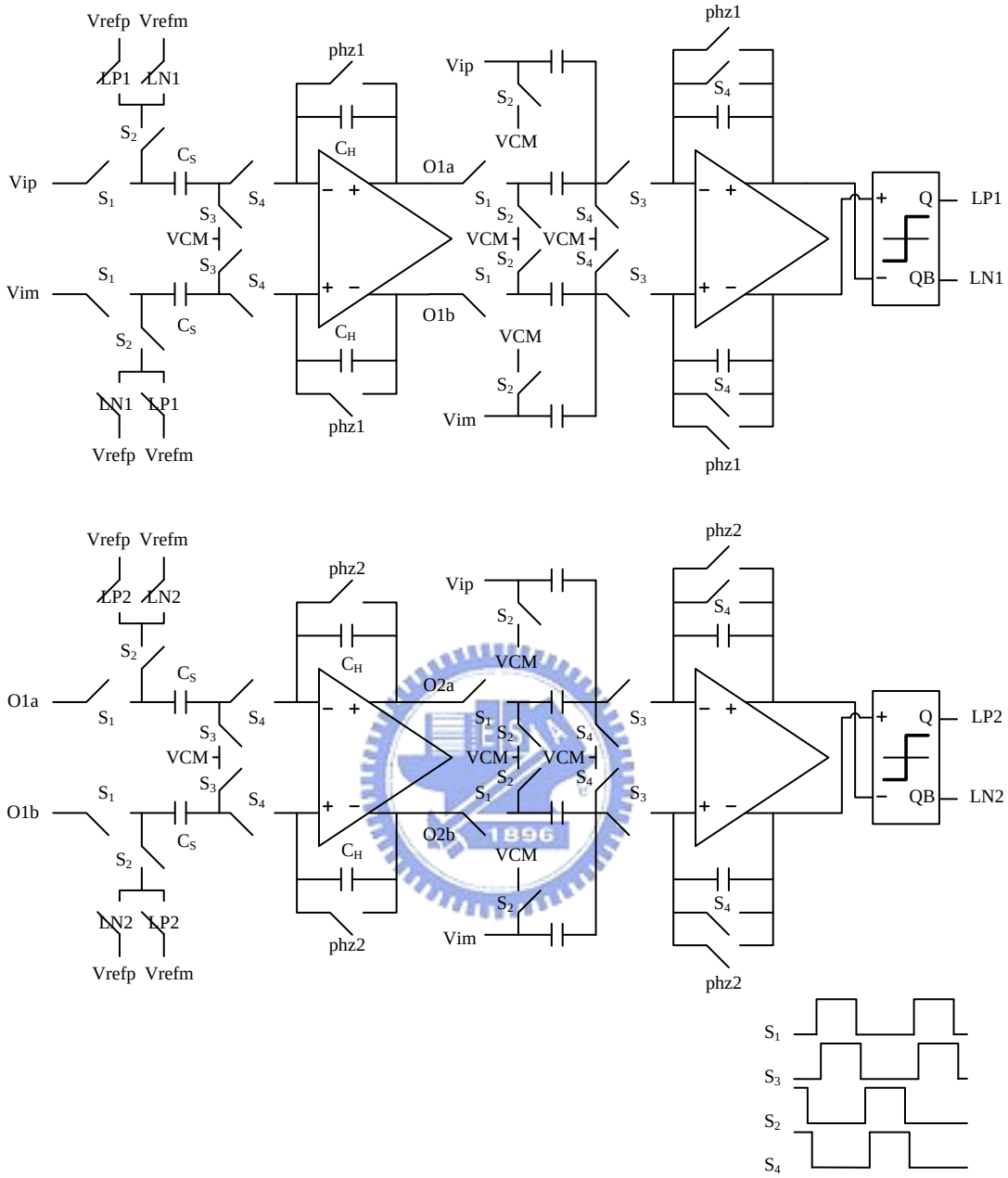


Figure 4.13 The analog circuit of the second-order configurable dual-mode low-distortion A/D converter and its clock phase

From the system level simulation, we can predict and obtain the system performance roughly. There are many ideal components in the system level simulation. But for circuit level implementation, there are more detail considerations in the design.

The whole analog part of the circuit is shown in Figure 4.13. A fully differential configuration has been adopted in order to ensure high power supply rejection, reduced clock feedthrough and switch charge injection errors, improved linearity, and increased dynamic range. Operation of the modulator is controlled by a nonoverlapping two-phase clock. During phase 1 all of the switches labeled S_1 and S_3 are open, while those labeled S_2 and S_4 are closed, and the input to the integrator is sampled onto the capacitor C_S, and the adder adds the input and the output to the integrator. In phase 2, switches S_1 and S_3 open, while S_2 and S_4 close, and charge stored on C_S is transferred to C_H, and the adder reset. During this phase, the closing of switches S_2 has the effect of subtracting the output of the two-level D/A network from the input to the integrator. The charge injected by the MOS switches in the circuit of Figure 4.13 is a common-mode signal that is canceled by the differential implementation of the modulator. Signal-dependent charge injection is further suppressed by opening switches S_3 and S_4 slightly before S_1 and S_2, respectively [12].

In discrete-time circuit design, we should promise that the thermal noise will not dominate whole performance. Model opamp as a one-pole system. The research of the relation between the switch noise and the opamp noise is shown in Figure 4.14. For x<<1(i.e., for gm1<<1/Ron), the op-amp dominates both the bandwidth and the noise, while for x>>1(gm1>>1/Ron), the switch effects dominate. Since the general case is gm1>>1/Ron, we should estimate the switch noise to lower than our design noise level. The total noise power is minimized, and becomes $2kT/C_s$, if x>>1, i.e., if the condition gm1>>1/Ron holds. Although there are other noises in the circuit, they can be ignored [16]. The noise power within the base-band of an oversampling modulator introduced by a first-stage integrator is then

$$P_N = \frac{4kT}{OSR \cdot C_s} \tag{4.14}$$

where C_s is the sampling capacitor. If the maximum amplitude of the differential input to the modulator is V_{sw}, then the power of a full-scale sinusoidal input is

$$P_S = \frac{V_{sw}^{\ 2}}{2} \tag{4.15}$$

We can also calculate the SNR to be the ratio of the maximum sinusoidal power to the switch noise. Mathematically, we have through the use of (4.14) and (4.15)

$$SNR = \frac{P_S}{P_N} = \frac{V_{sw}^{\ 2} \cdot OSR \cdot C_s}{8kT} \tag{4.16}$$

If we want to design a high resolution circuit, the large capacitor is critical. To design the resolution and OSR will depend on the equation

$$SNR_{\max} = 6.02N + 1.76 - 12.9 + 50\log(OSR) \tag{4.17}$$

We design 14bit equal to 86.04dB for audio, and use one-bit quantizer. After calculating, OSR larger than 67 is critical for this design. For switch noise and other nonlinearities consideration, we choose OSR equal to 128 and the sampling frequency is also equal to

$$f_s = OSR \times 2 f_b = 128 \times 2 \times 20kHz = 5.12MHz \tag{4.18}$$

Now we can estimate the sampling capacitor for switch noise consideration. We design the sampling capacitor 1pF to let the noise floor lower than 89dB.

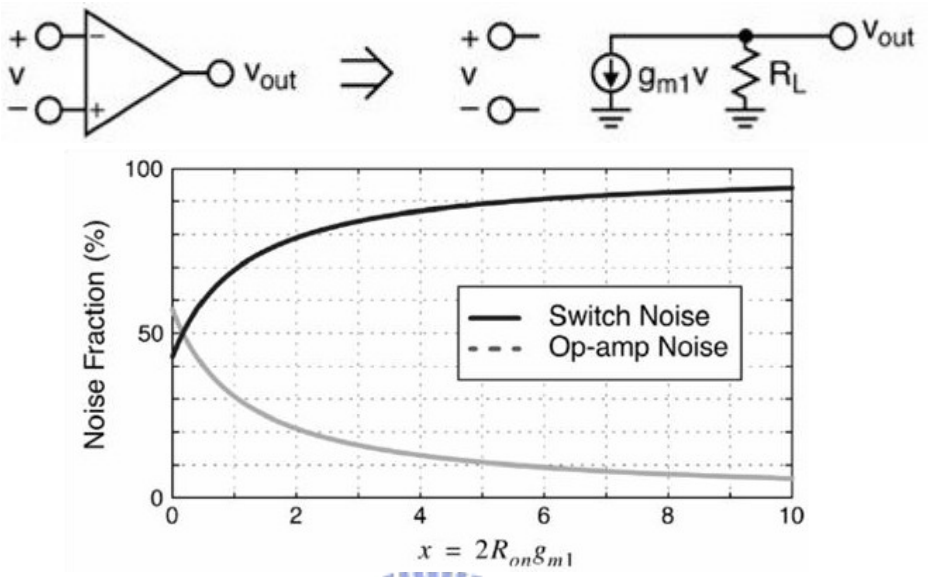


Figure 4.14 Noise analysis for a single-stage amplifier

The design of the differential operational amplifier is key to successful realization of the integrators. A consideration of integrator leak mandates that the amplifier open-loop gain be at least equal to the oversampling ratio, OSR=128 [02]. However, the gain must generally be somewhat larger than this in order to adequately suppress harmonic distortion. An operational amplifier that is not slew-rate limited is essential in order to avoid slewing distortion. The integration is accomplished only during phase 2 and thus must be completed within one-half the clock cycle. For an amplifier with a single dominant pole and unity-gain frequency f_u, the impulse response of the integrator output during phase 2 will be exponential with a time constant [13].

$$t = \frac{1}{bw_u} \tag{4.20}$$

It is equal to

$$t = \frac{1 + C_1/C_2}{2pf_u} \tag{4.21}$$

The fact that only one-half of the clock period T is available for the integration has been accounted for in this equation.

$$f_u \geq \frac{1 + C_1/C_2}{pT} \tag{4.22}$$

The fact that only one-half of the clock period T is available for the integration has been accounted for in this equation. The bandwidth fu must be greater than approximately one-half the sampling rate, provided that the step response is purely exponential. In practice, this latter requirement is not met precisely because of secondary effects such as nondominat poles and the dependence of the pole location on the amplifier operating point, which in this design changes during transients.

4.4.1 Operational Amplifier

The opamp is the most important element in the discrete-time circuit. There are many non-ideal considerations in real circuit implement, such as finite gain, bandwidth, stability, and linearity. We design the opamp base on the period of the clock. A two-stage opamp may achieve higher DC gain than a single-stage amplifier. However, the optimal design can be achieved by using single-stage amplifier topology, because it has higher bandwidth and smaller power consumption. Therefore, the opamp is implemented as a fully differential folded cascade amplifier shown in Figure

4.16.

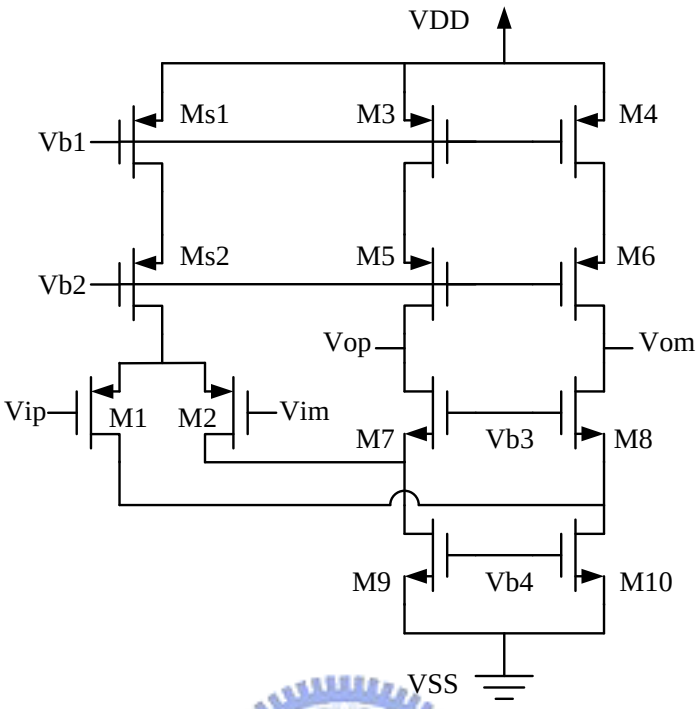


Figure 4.16 Folded cascode opamp

The dc gain of the fully-differential folded cascade opamp can be written as

$$|A_v| = G_m \times R_{out} . \tag{4.23}$$

$$R_{out} = [(g_{m5} + g_{mb5}) r_{o5} r_{o3}] \,||\, [(g_{m7} + g_{mb7}) r_{o7} (r_{o9} \,||\, r_{o2})] \tag{4.24}$$

The transconductance G_m is approximately equal to g_{m2}. Substituting equation (4.24) in equation (4.23), we obtain

$$|A_v| = g_{m2} \times \{[(g_{m5} + g_{mb5}) r_{o5} r_{o3}] \,||\, [(g_{m7} + g_{mb7}) r_{o7} (r_{o9} \,||\, r_{o2})]\} \tag{4.25}$$

Because of the single-stage topology, the second pole is far away from the unity-gain frequency. Assuming the output capacitance and resistance are C_L and R_{out}, the frequency response of the folded-cascode opamp is derived by

$$A(s) = \frac{g_{m2} R_{out}}{1 + sR_{out} C_L} \tag{4.26}$$

For the high frequency response, because of $sR_{out}C_L >> 1$ we can get the transfer function as follows

$$A(s) = \frac{g_{m2}}{sC_L} \tag{4.27}$$

The unity-gain frequency is given by

$$|A(s)| = \left| \frac{g_{m2}}{sC_L} \right| = 1 \tag{4.28}$$

$$w_u = \frac{g_{m2}}{C_L} \tag{4.29}$$

Besides, we design the phase margin higher than 65° for no peaking in frequency response. Figure 4.17 shows the AC simulation results including the gain and phase margin. The simulated performance of the fully-differential folded cascade op-amp is summarized in Table 4.1.

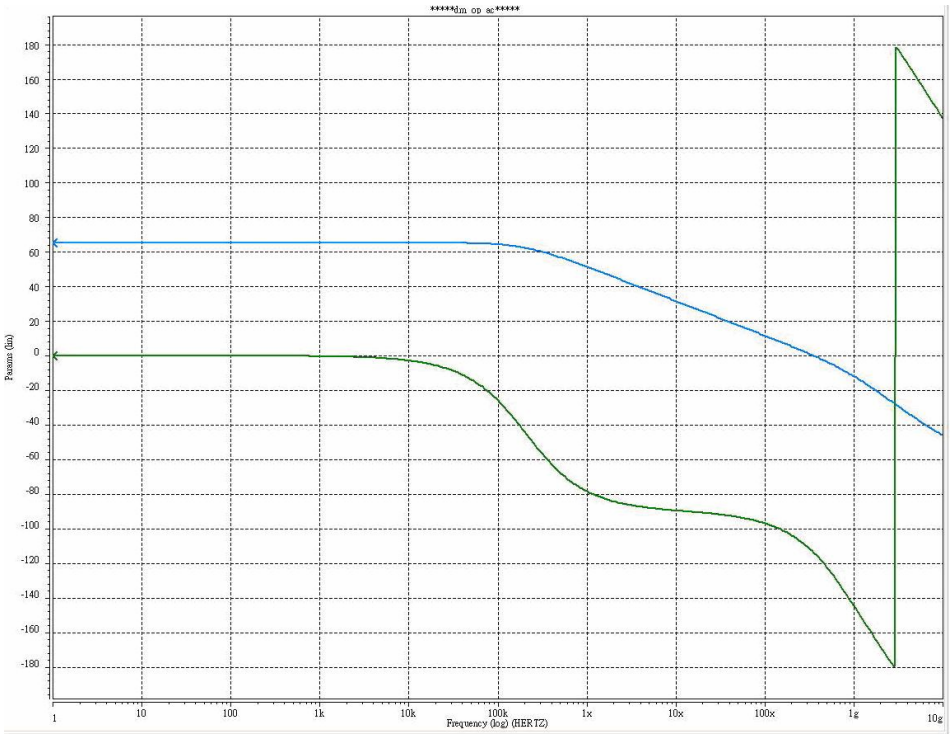


Figure 4.17 The frequency response of the opamp

TABLE 4.1 Specification of the first amplifier

Parameters	***Simulation Result***
DC gain	69 dB
Phase Margin	65 degree
Unity Gain Frequency	334 MHz
Slew Rate	133 V/μs
Output Swing	0.3V~1.5V
Power Dissipation	760μW
Technology	Standard TSMC 0.18μm 1P6M

4.4.2 Comparator

The one-bit quantizer is realized with a dynamic comparator and an SR latch, shown in Figure 4.18 [18]. While clock is low, the output nodes are precharged to VDD. While clock goes high, transistors M1 and M2 will work in saturation region, and the respectively precharged parasitic capacitances of the output nodes. When the

voltage of the output nodes drops to the threshold voltage of the latch formed by two cross-coupled inverters, the regeneration process starts. Finally, the voltage of the output nodes reaches the rail voltage according to the decision made. The result is then latched by the SR latch following. This comparator is very power efficient. When clock is low, it would not consume any power because transistors M7, M8, M9 and M10 would cut off transistors M3 and M4. Another advantage of this comparator is its low offset because of transistor M1 and M2 working in saturation region.

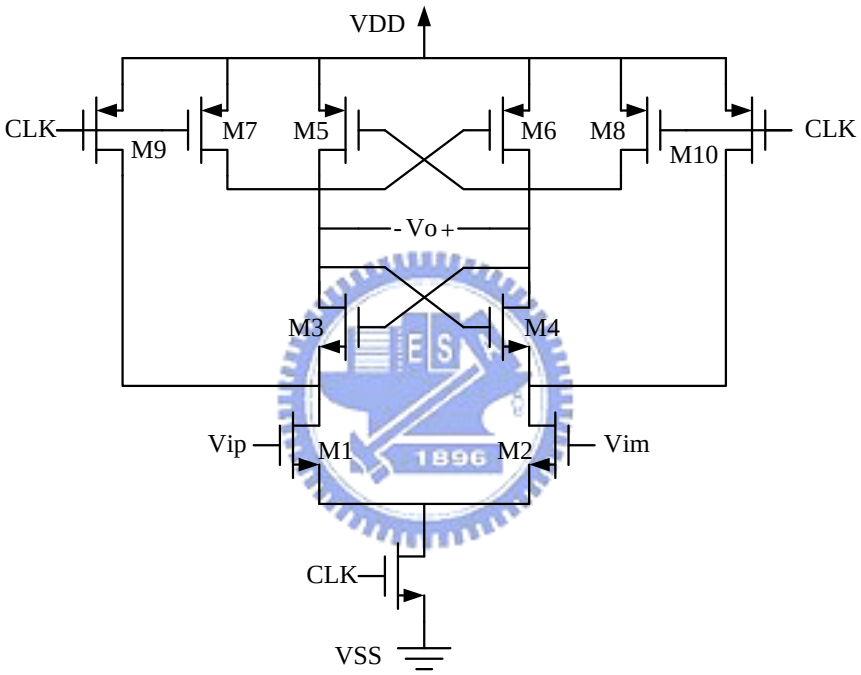


Figure 4.18 Low-offset regenerator

We give this 1-bit quantizer some input to check its logic. The simulation result shown in Figure 4.19 form top to bottom is input signal, output signal, and clock. While the clock goes high, the output changes to the input logic. Besides, its power dissipation is equal to 13.112 μ w

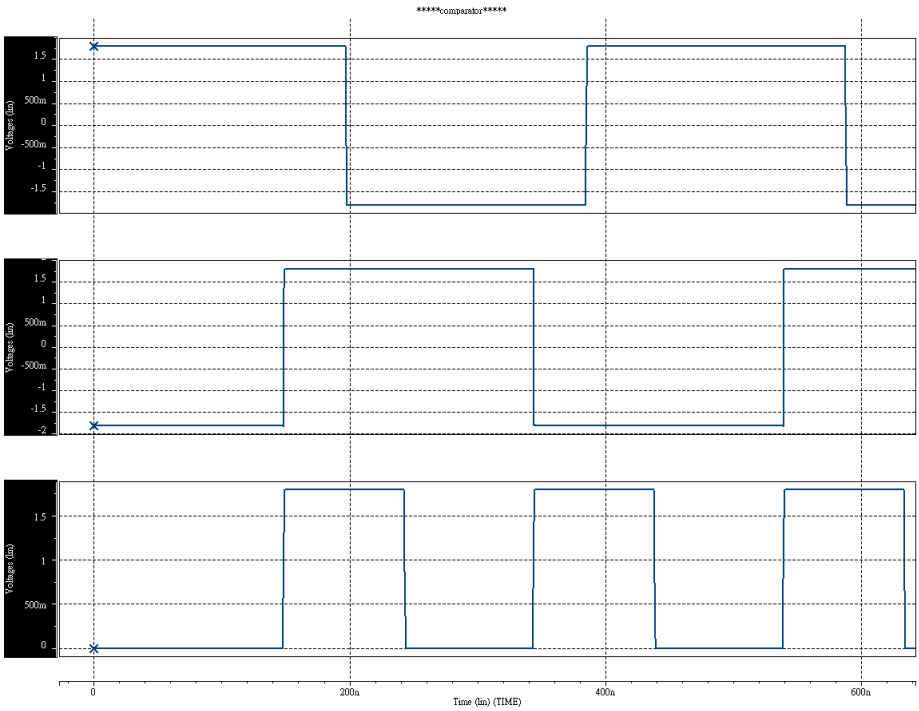


Figure 4.19 The logic test of the comparator

4.4.3 Clock generator

The clock generator is shown in Figure[16]. The external input is buffered and then two then two nonoverlapping clock signals are generated. To avoid the signal dependent charge injection, two delayed clocks are also generated. Figure 4.21 shows the two nonverlapping clock signals and its two delayed clock.

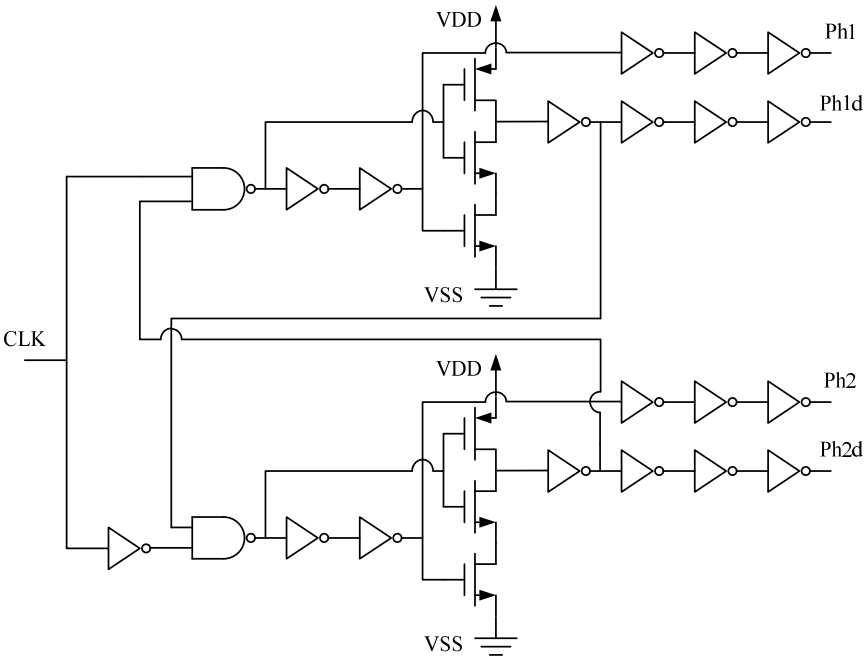


Figure 4.20 The nonoverlapping clock generator

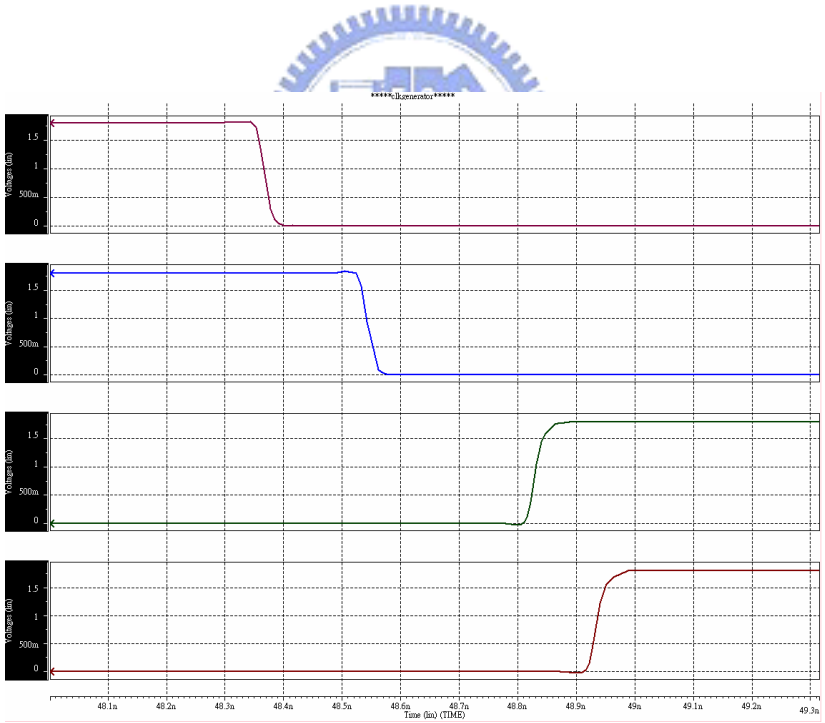


Figure 4.21 The two nonverlapping clock signals and its two delayed clock

4.4.4 Bootstrapped switches

While the over-drive voltage of the input switches varies from input signal, the

on-resistance is signal dependence. A widely used method to improve the linearity is to bootstrap the switch transistor gate voltage to reduce the on-resistance signal dependency. Figure 4.22 shows the well known gate-source bootstrapping technique [17]. During clock high, the capacitor C_b is precharged to VDD and the transistor Ms is off. During clock low, the transistor Ms is on and its V_{GS} is constant equal to VDD. The advantage is that the constant R_{ON} due to the fixed V_{GS} makes the time constant $t = R_{ON} \times C$ independent of the input signal. It not only reduces harmonic distortion but also reduces on-resistance by increasing V_{GS} to VDD.

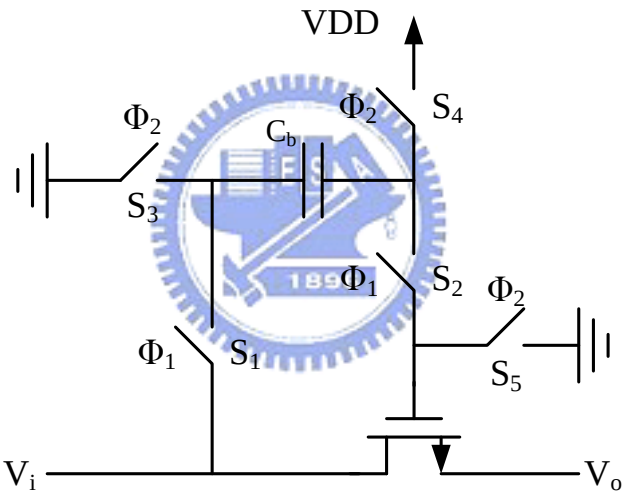


Figure 4.22 Bootstrapped switches

The gate voltage of the switch and input signal are shown in Figure 4.23. We can see that the V_{GS} of the switch is nearly constant equal to VDD=1.8V. The reason why the V_{GS} of the switch not equal to VDD is due to parasitic capacitor and reverse-bias current of the transistors.

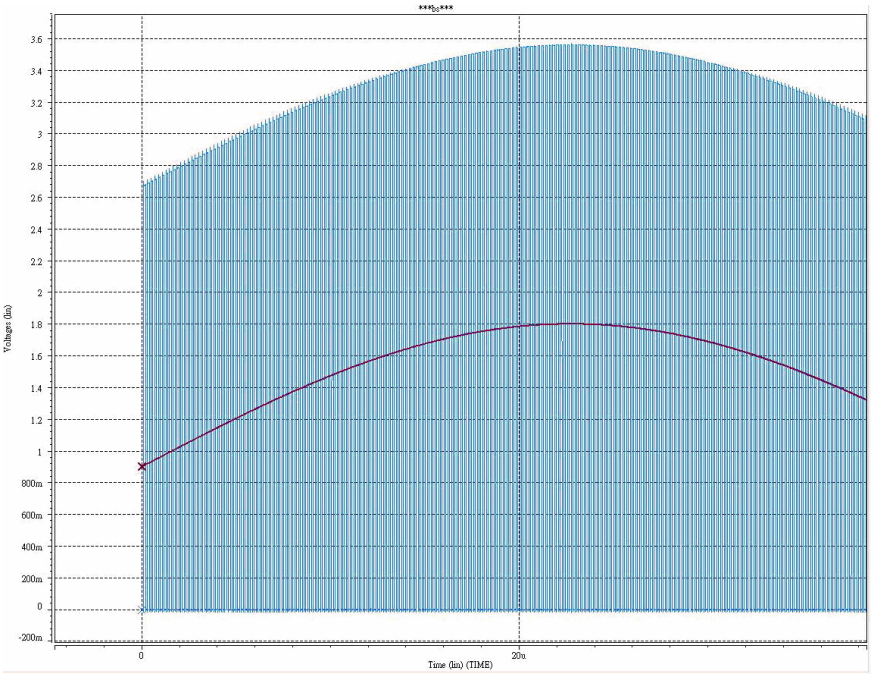


Figure 4.23 The gate voltage of the bootstrapped switch and input signal

4.5 Simulation result

For audio band application, the sampling rate is 5.12 MS/s and input signal frequency is 6.25 kHz. Figure 4.24 is the plot of the time domain of the joints of the proposed configurable dual-mode low-distortion A/D converter. The voltage in Figure from top to down are the output of the first integrator, the output of the second integrator, the output of the first adder, and the output of the second adder, the output of the first modulator, and the output of the second modulator respectively. Use MATLAB to simulate the digital filter, and get the output of the whole modulator. Figure 4.25 is the plot of power spectrum of the proposed configurable dual-mode low-distortion A/D converter. The ENOB is 13.82 and SNDR is 84.97 dB.

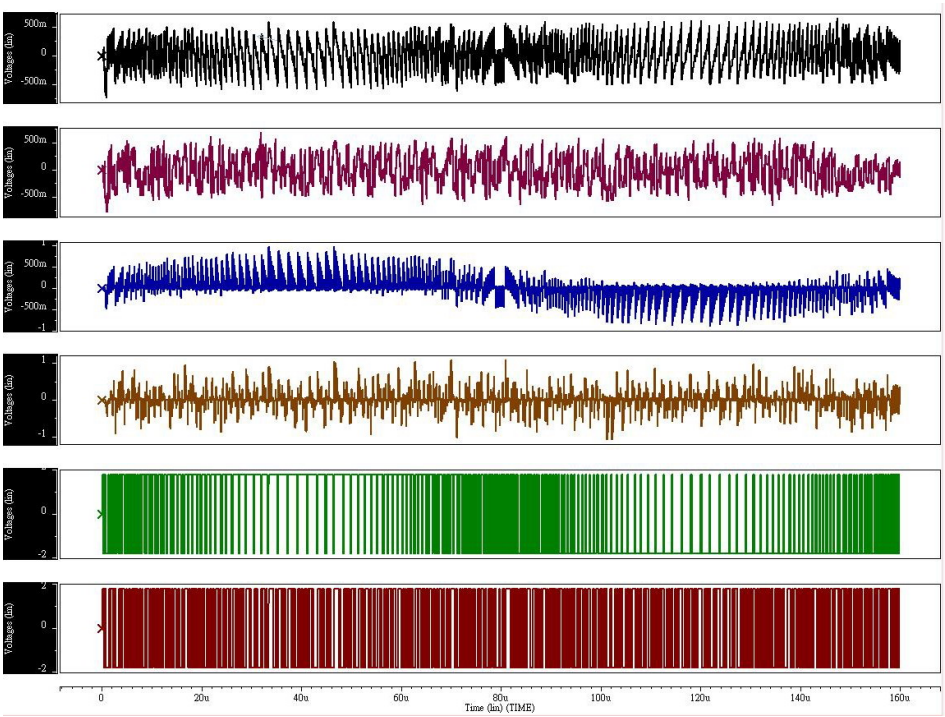


Figure 4.24 The time domain of the joints of the proposed configurable dual-mode low-distortion A/D converter

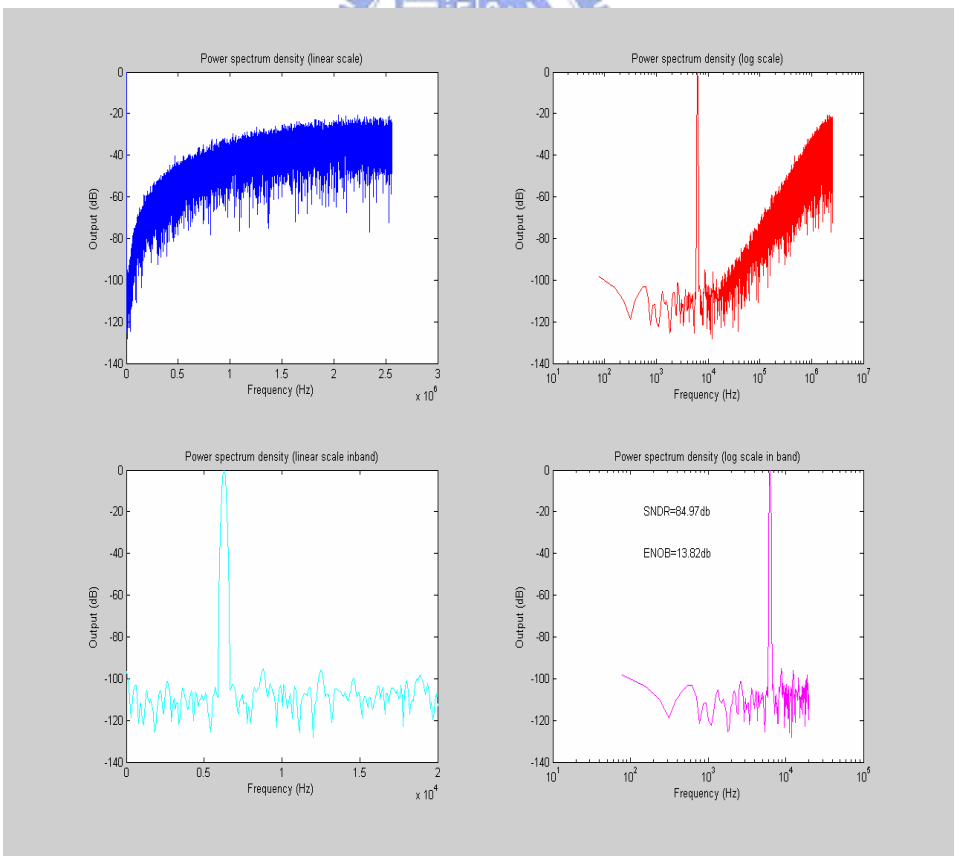


Figure 4.25 The power spectrum of the proposed configurable dual-mode low-distortion A/D converter

For measurement application, the resolution can be adjusted by user according to the relation of the resolution and conversion time. Figure 4.26 is the plot of the time domain of the joints of the proposed configurable dual-mode low-distortion A/D converter. The voltage in Figure from top to down are the output of the first integrator and the output of the second integrator respectively. The input constant voltage is 0.0134 V, and the reference voltage is 0.5 V. According to the relation of the resolution and conversion time, simulate 16bit will cost 366 cycles. We check the output of the integrators, and they are belong to $+V_R$ and $-V_R$. After using MATLAB to simulate the digital filter, VLSB is equal to $1.52200051748018\times10^{-5}$, N2 is equal to 880, and check $(-VLSB/2)<(vin-N2\times VLSB)<(VLSB/2)$.

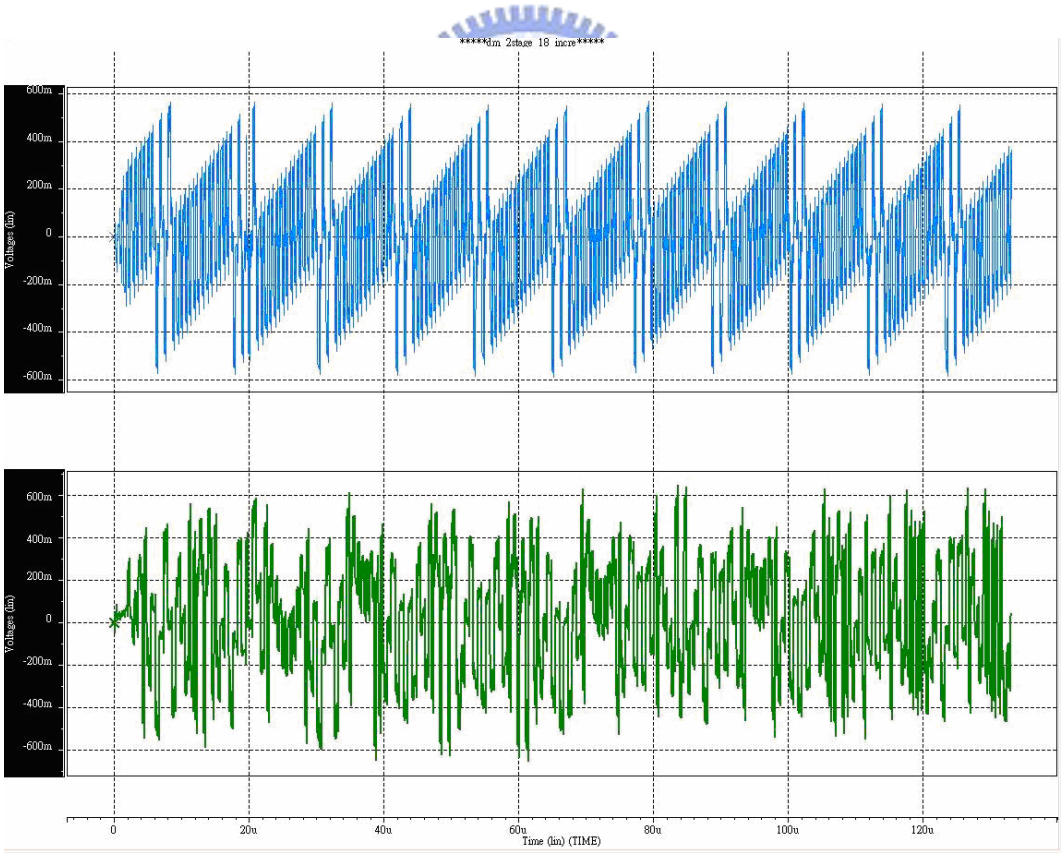


Figure 4.26 The time domain of the joints of the proposed configurable dual-mode low-distortion A/D converter

For audio application, the specification of the configurable dual-mode low-distortion A/D converter is summarized in Table 4.2.

Table 4.2 Specification of the configurable dual-mode low-distortion A/D converter

Parameters	Simulation Result
Technology	TSMC 0.18μm Mixed-Signal
Power Supply	1.8 V
Signal Bandwidth	20 kHz
Chip area	0.42 mm2
Sampling Frequency	5.12 MHz
Peak SNDR	84.97 dB
Resolution	14 bit
Power Dissipation	3.066 mw

For measurement application, the resolution can be adjusted by user according to the relation of the resolution and conversion time. For this design, we design to 16bit, and need 366 cycles conversion time.

4.6 Layout level design

In mixed-signal layout issues, analog ICs are more sensitive to noise than digital ICs. We must take more consideration in mixed-signal layout issues. Many mixed-signal layout issues have been proposed [19]. First, Grounding and power supply routing must also be considered when using digital and analog circuitry on the same substrate. We separate power supply and ground pins are then connected externally. It is not wise to use two separate power supplies because if both types of circuits are not powered up simultaneously, latch-up could easily result. Second, Guard rings should be used wisely throughout a mixed-signal environment. Circuits

that process sensitive signals should be placed in a separate well with guard rings attached to the analog VDD supply. Third, performance depends on the matching of devices is important aspect of differential pairs. Oxide gradients and other process variations are inevitable. Therefore, common-centroid layout constructs two devices symmetrically about a common center in the layout. The layout diagram is present in Figure 4.27 and the layout size is 0.83×0.86 mm^2.

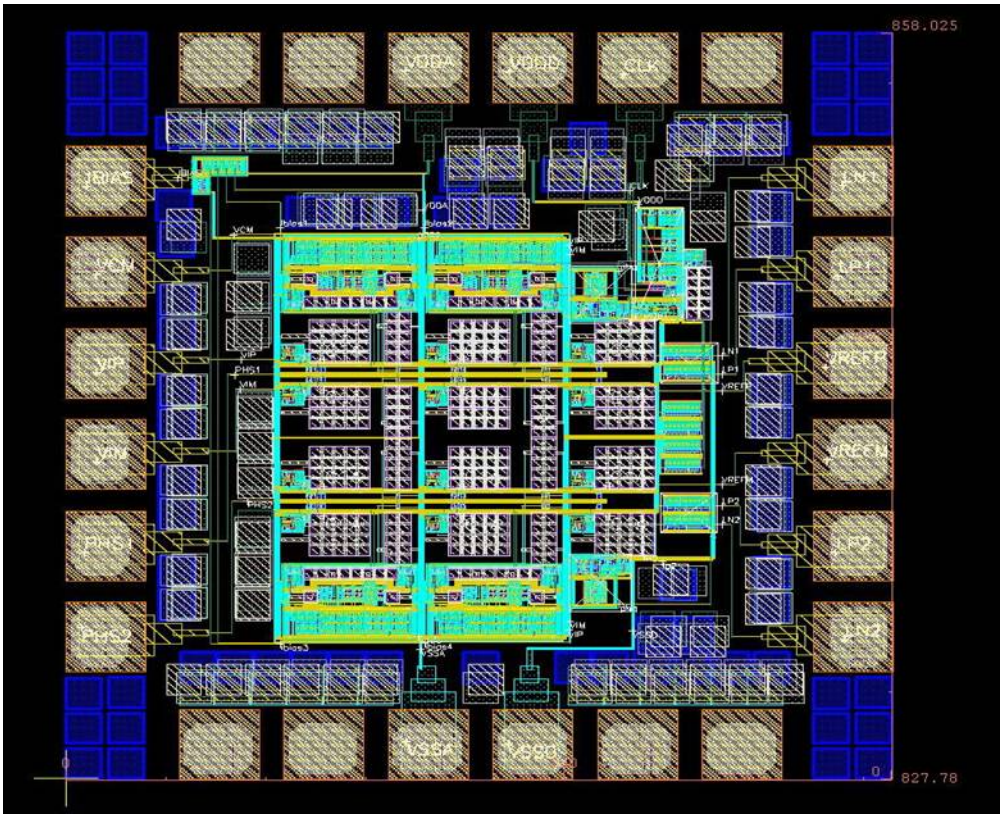


Figure 4.27 The layout diagram of the chip

Chapter 5 Test Setup and Experimental Results

5.1 Introduction

This configurable dual-mode low-distortion A/D converter has been fabricated by TSMC 0.18-μm CMOS Mixed-Signal process with one poly and six mental. In this chapter, we present the testing environment, including the component circuits on the DUT (device under test) board and the instruments. The measured results are presented in this chapter, too

5.2 Measuring Environment

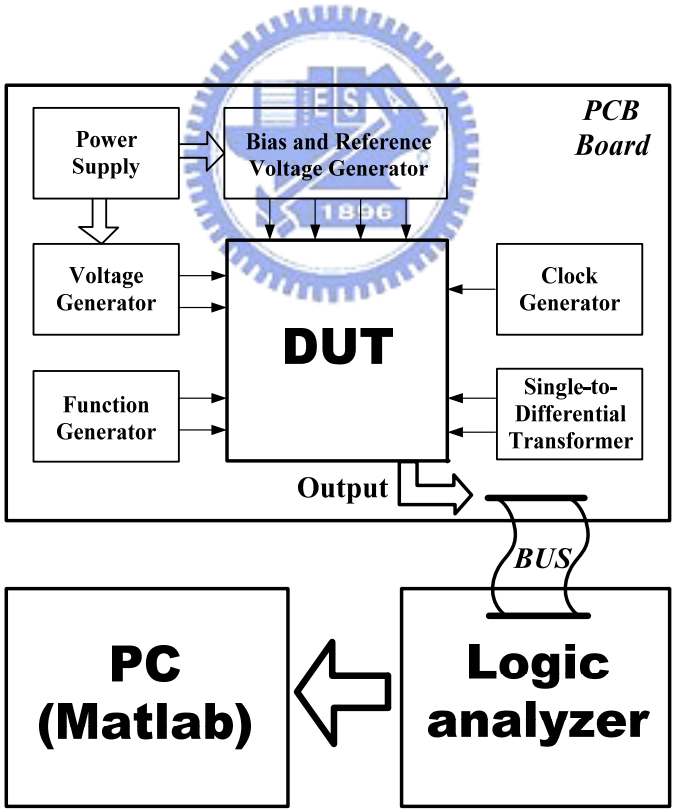


Figure 5.1 Experimental testing setup

Figure 5.1 shows the whole measurement process and the testing setup used to

measure the performance of the proposed configurable dual-mode low-distortion A/D converter. We adopt a PC (for MATLAB processing), an oscilloscope, three power supplies, a function generator and a pulse generator. The testing printed circuit board (PCB) contains voltage regulator, clock generator, single to differential transformer circuit, and the DUT. The supply voltages for regulators are supplied by the 9V batteries and the input signal and clock are provided by the function generators Agilent 33220A as shown in Figure 5.2. The digital output signals will be fed into the logic analyzer Agilent 16702B as shown in Figure 5.3. And we can show the output waveform by the oscilloscope Agilent S4832D as shown in Figure 5.4. Finally, the data will be loaded into the PC and be analyzed with MATLAB to obtain the specification of the proposed configurable dual-mode low-distortion A/D converter

.

Figure 5.2 Function generator Agilent 33220A

Figure 5.3 Logic analyzer Agilent 16702B

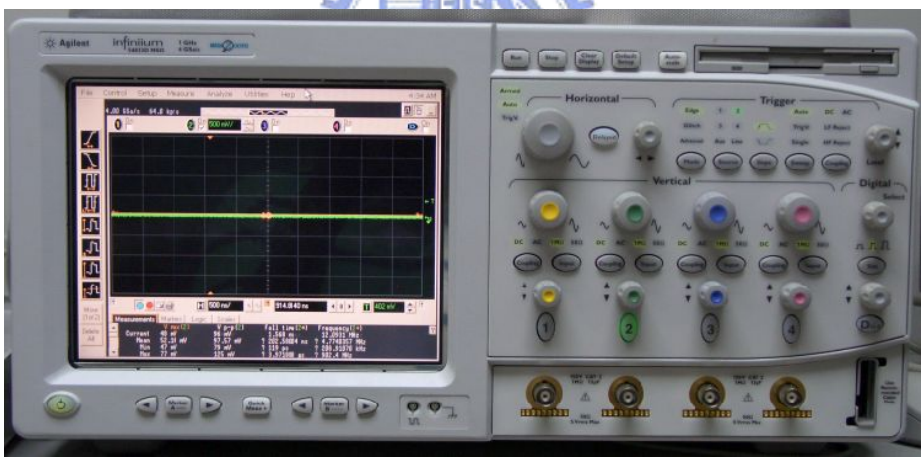


Figure 5.4 Oscilloscope Agilent S4832D

5.2.1 Power Supply Regulators

The supply voltages are generated by LM317 adjustable regulators as shown in Figure 5.5. The capacitor C1 is added to improve the transient response and capacitor C2 is the bypass capacitor. The output voltage of the Figure 5.5 can be expressed as

$$V_{out} = 1.25 \cdot \left(1 + \frac{R2}{R1}\right) \cdot I_{ADJ} \cdot R2\,, \tag{5.1}$$

where I_{ADJ} is the DC current that flows out of the adjustment terminal ADJ of the regulator [14].

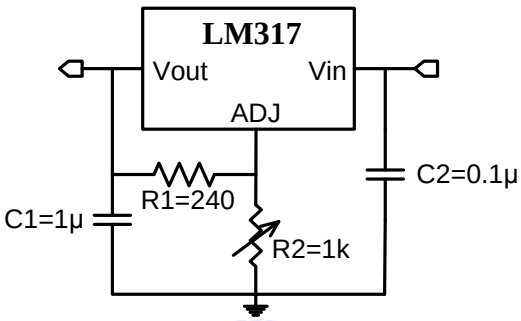


Figure 5.5 Power supply regulator

5.2.2 Input Terminal Circuit

A function generator can only provide AC component of input signal and the input signal is single-end. So we need the input terminal circuit which combined single-to-differential transformer circuit and AC couple circuit as shown in Figure 5.6. Because we can't ensure the common mode voltage is that we need, we need the adjustable resistances to tune the voltages. The operation amplifiers are OP-27 and supplied by 12V for best operation condition.

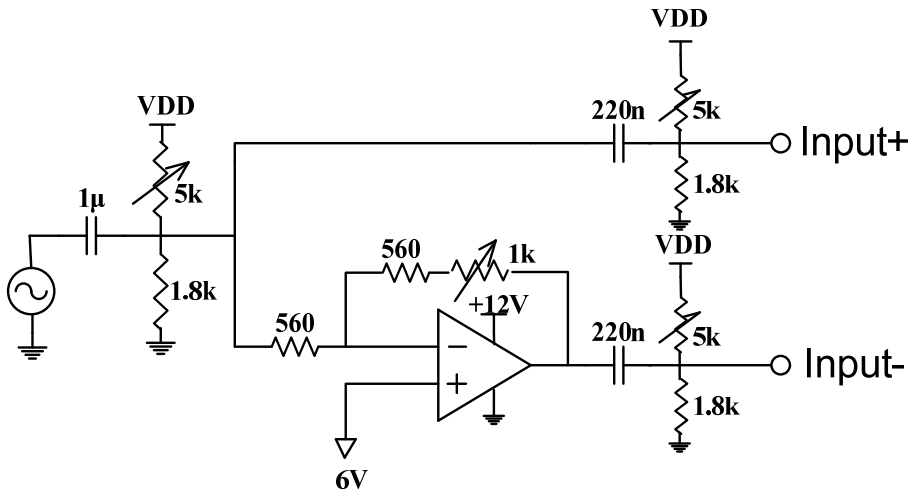


Figure 5.6 Input terminal circuit

5.3 Testing Board, and Pin Configuration

Figure 5.7 shows the photograph of the testing DUT board. Figure 5.8 presents the pin configuration and lists the pin assignments of the experimental dual-mode converter..

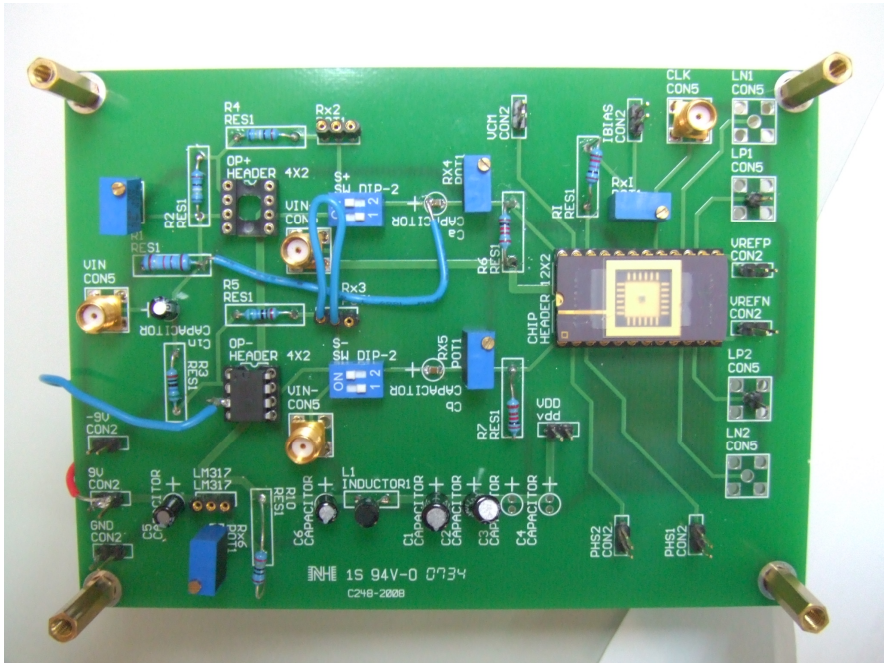
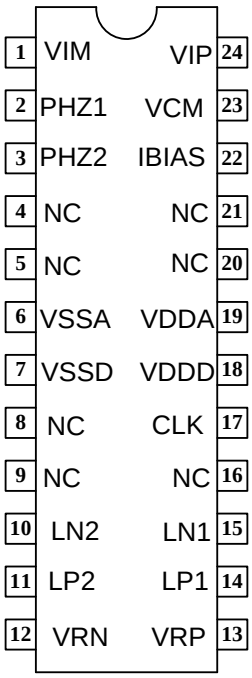


Figure 5.7 Photograph of the dual-mode converter DUT board

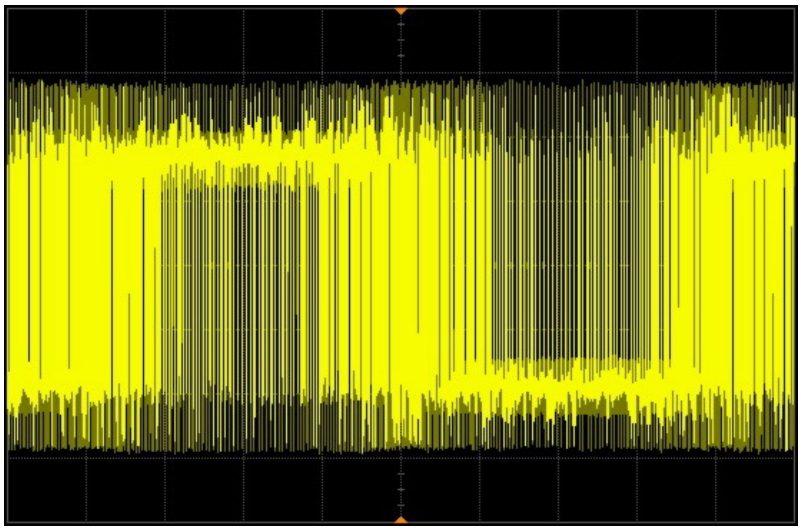


Pin	Name	I/O	Describe
1	VIM	In	Output Signal (180°)
2	PHZ1	In	Logic Voltage
3	PHZ2	In	Logic Voltage
4	NC	-	No connection
5	NC	-	No connection
6	VSSA	-	DUT Ground
7	VSSD	-	DUT Ground
8	NC	-	No connection
9	NC	-	No connection
10	LN2	Out	Output2 Signal (180°)
11	LP2	Out	Output2 Signal (0°)
12	VRN	In	DAC Feedback Voltage
13	VRP	In	DAC Feedback Voltage
14	LP1	Out	Output1 Signal (0°)
15	LN1	Out	Output1 Signal (180°)
16	NC	-	No connection
17	CLK	In	System clock input
18	VDDD	-	DUT Supply Voltage
19	VDDS	-	DUT Supply Voltage
20	NC	-	No connection
21	NC	-	No connection
22	IBIAS	In	Bias current control
23	VCM	In	Common Voltage
24	VIP	In	Output Signal (0°)

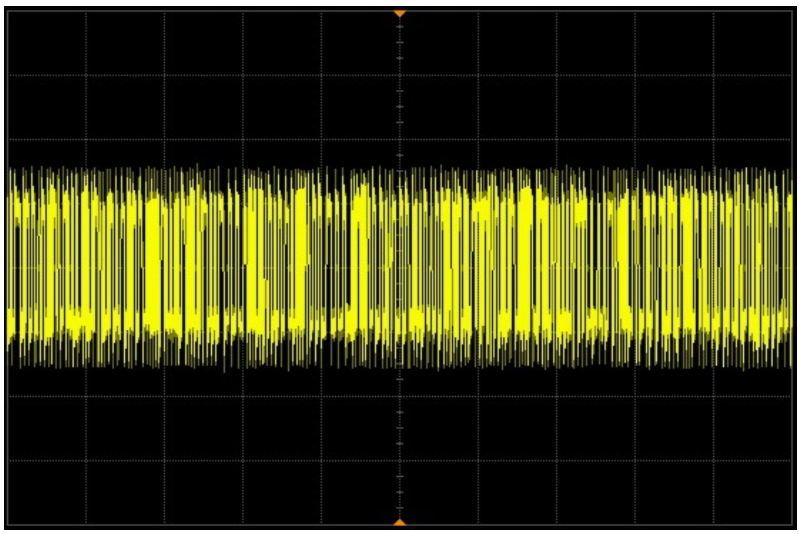
Figure 5.8 (a) Pin configuration diagram and (b) Pin assignment

5.4 Performance Evaluations of Configurable Dual-mode Low-distortion A/D Converter

This proposed SDM chip has fabricated by TSMC 0.18 μm technology. It was powered by 1.8 V supply. A 6.25 kHz sine wave is applied and the clock rate is 5.12 MHz while the corresponding bandwidth is 20 kHz. The time-domain analysis is measured by an oscilloscope and is shown in Figure 5.9(a) and Figure 5.9(b). It can be compared with the simulation result.



(a)



(b)

Figure 5.9 Measurement result (a) the output of the first stage (b) the output of the second stage

Next, we should know the spectrum of the second-order sigma-delta modulator. The input signal frequency is 6.25 kHz and the signal bandwidth is 20 kHz. Then, the output bit streams can be recorded with a logic analyzer, so that the data can be processed with MATLAB. Simulate the digital filter with MATLAB. Then, do the fast Fourier transformation with 65536 points. Figure 5.10 is the plot of power spectrum of the proposed configurable dual-mode low-distortion A/D converter. The ENOB is 8.74 and SNDR is 54.37 dB. Figure 5.11 shows the SNDR versus normalized input

signal. The peak SNDR and DR are 54.37dB and 58dB, respectively. The power consumption is 3.066mW. The complete measured performance summary of the second-order sigma-delta modulator is given in Table 5.1.

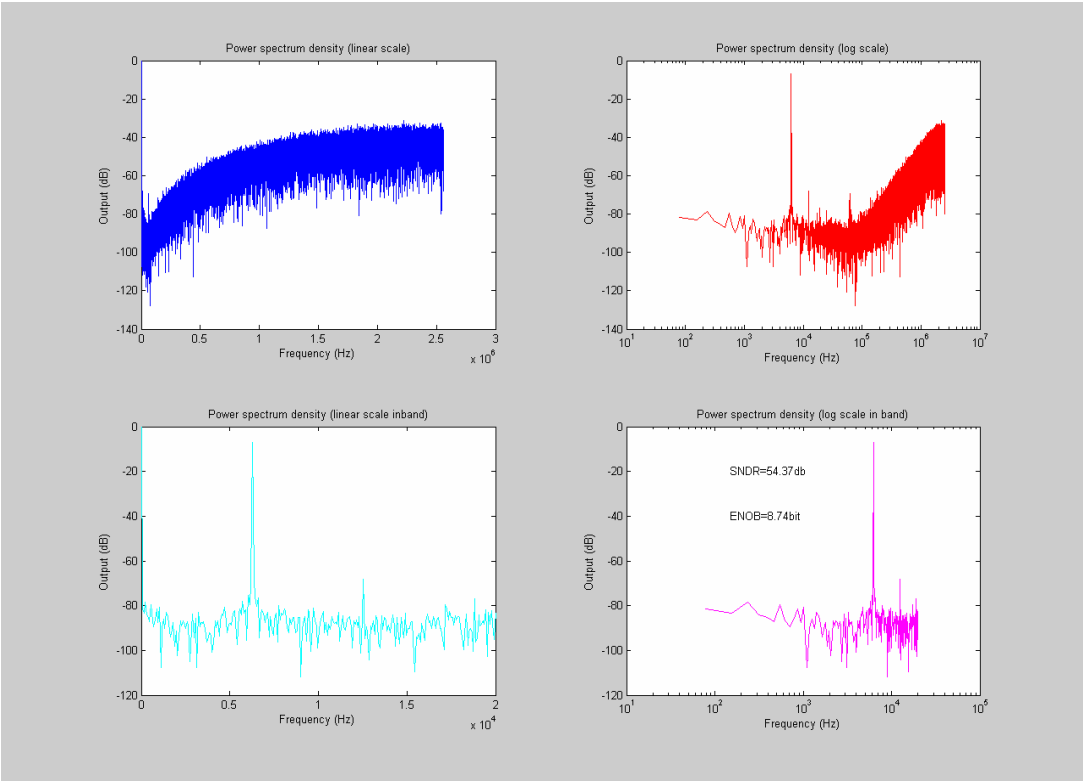


Figure 5.10 Measured output spectrum

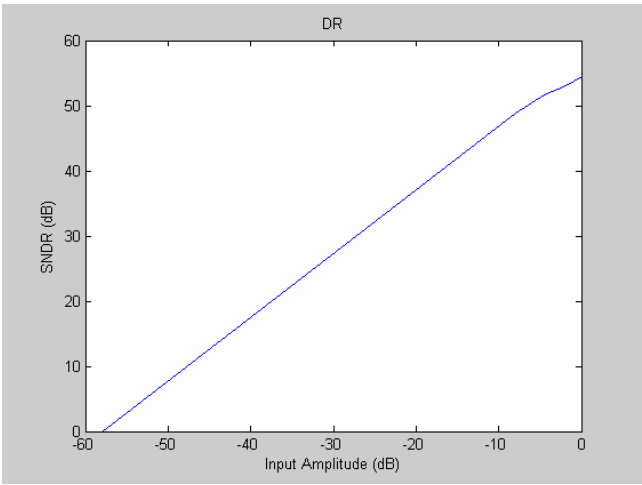


Figure 5.11 Plot of SNDR versus normalized input signal

Table 5.1 Summary of measured results of the SDM

Parameters	Measured Result
Technology	TSMC 0.18μm Mixed-Signal
Power Supply	1.8V
Signal Bandwidth	20kHz
Chip area	0.42 mm^2
Sampling Frequency	5.12 MHz
Dynamic Range	58 dB
Peak SNDR	54.37 dB
Resolution	9 bit
Power Dissipation	3.6 mw (including bias circuits and output buffer)

For incremental mode measurement, we use pattern generator to generate the reset pulse and clock. This can promise that the reset pulse and clock are synchronal. We adjust the variable resistor to change our input voltage and reference voltage. Then, the output bit streams can be recorded with a logic analyzer, so that the data can be processed with MATLAB. Resolution versus conversion time is shown in Figure 5.12.

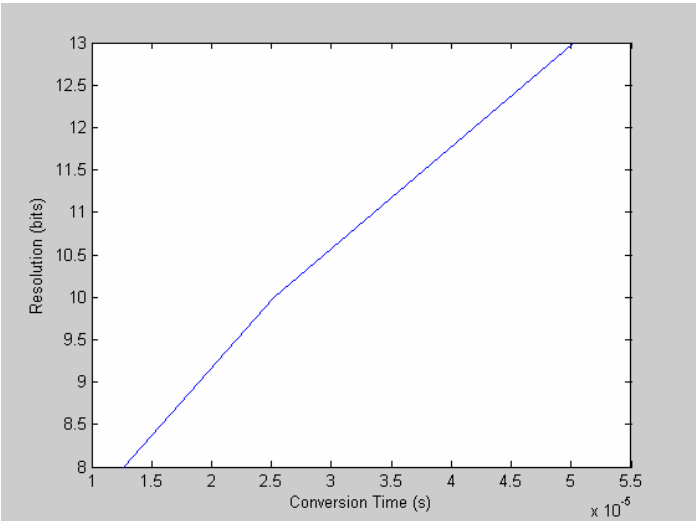
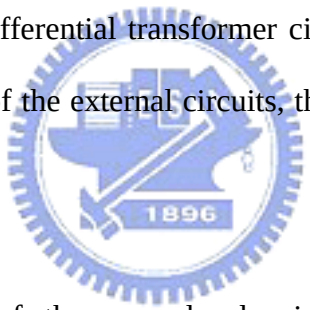


Figure 5.12 Plot of resolution versus conversion time

5.5 Summary

The design of configurable dual-mode low-distortion A/D converter was completed. It took the design considerations described in Chapter 3 and Chapter 4 into account.

The original resolution of the second-order sigma-delta modulator was predicted to achieve 14bits. The measured result shows that the actual performance is 9bits. The possible reasons of performance decay are that the resistances variation, thermal noise, the interference from clock signal, and the noise of external circuits on the testing printed circuit board. The even-order distortion is a little large due to the external circuits which are single-to-differential transformer circuit and AC couple circuit. If we could reduce the number of the external circuits, the performance would be much better.



The original resolution of the second-order incremental modulator can be predicted by user through the control of the conversion time. The measured result shows that the actual performance ENOB is lower than prediction. The possible reasons of performance decay are that the interference from clock signal, offset of the opamp, the input voltage variation, and reference voltage variation. We adjust the input voltage and reference voltage by variable resistor and check these voltages by voltameter. This process is very rough especially in high-resolution measurement, since the voltameter can't achieve high-resolution and other loading effect will also decay the precision. This is a challenge for designer to check the precision voltage.

The noise floor of the input signal is a little large due to the external circuits which

are single-to-differential transformer circuit and AC couple circuit. And the mismatch of input differential signal is also the possible reason which causes the performance decay. If we could reduce the number of the external circuits, the performance would be much better.

Chapter 6 Conclusions

Generally, a very versatile and modular A/D converter with low-distortion topology has been implemented. It can be configured in two main operation modes. The first one, which is the sigma-delta conversion mode, is suited for communications and speech applications. The second one, which is the incremental conversion mode, is well suited for instrumentation applications. This thesis presents the basic concepts for sigma-delta modulator including quantization noise, noise shaping strategy, and system overview of sigma-delta are introduced. This thesis also presents the basic concepts for incremental including the consideration of the trade off between resolution and conversion time and offset cancellation. Then, the design of the configurable dual-mode low-distortion A/D converter is presented. After system level simulation for building the behavior model to understand the characteristics of configurable dual-mode low-distortion A/D converter and determine the specification, the circuit level and layout level design are presented.

The chip was fabricated by TSMC 0.18μm standard process. With an oversampling ratio of 128 and a clock frequency of 5.12 MHz, the modulator achieves a 58 dB dynamic range and a peak SNDR of 55 dB for audio application. The measured resolution of the measurement application is 3 bit lower than the prediction in the same conversion time with a clock frequency of 5.12 MHz. The measurement problems have been discussed. However, the dual-mode converter architecture based on low-distortion topology which can achieve more advantages has been implemented. This thesis demonstrates that this concept leads to a very simple modular architecture.

Bibliography

[1] D.A. Johns and K. Martin, "Analog Integrated Circuit Design", John Wiley & Sons, Inc., 1997.

[2] Bernhard E. Boser, and Bruce A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters," *IEEE J. Solid-State Circuits*, vol. 23, NO. 6, December 1988.

[3] W. R. Bennet, "Spectra of quantized signals", Bell Syst. Tech. J., vol.27, pp.446-472, July 1948.

[4] S. R. Northworthy, R. Schreier, and G. C. Temes, Delta-Sigma Data Converters-Theorem, Design, and Simulation, John Wiley & Sons, Inc., 1997

[5] Y. Matsuya, et al. "A 16-bit Oversampling A-to-D Conversion Technology Using Triple-Integration Noise Shaping," *IEEE J. of Solid-State Circuits*, Vol. 22, pp. 921-929, December 1987.

[6] Olivier J. A. P. Nys and Evert Dijkstra, "On configurable Oversampled A/D Converters," *IEEE J. Solid-State Circuits*, vol. 28 NO. 7, July 1993.

[7] J. Robert, G. C. Temes, V. Valencic, R. Dessoulavy, and P. Deval, "A 16-bit low-voltage A/D converter," *IEEE J. Solid-State Circuits*, vol. 22, pp 157-163, Apr. 1987.

[8] J. Markus, J. Silva, G. C. Temes, " Theory and Applications of incremental ΔΣ Converters," *IEEE J. Circuits and Systems*, vol.51 NO.4, April 2004.

[9] J. Robert and P. Deval, " A second-order high-resolution incremental A/D converter with offset and charge injection compensation, " *IEEE J. Solid-State Circuits*, vol.28, pp. 736-742, July 1993.

[10] J. C. Candy and G. C. Temes, "Oversampling Methods for A/D and D/A Conversion," *Oversampling Delta-Sigma Data Converters*, ed. J. C. Candy and G. C. Temes, IEEE Press, New York, 1992.

[11] J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, "Wideband low-distortion delta-sigma ADC topology," *IEE Electronics Letters*, vol. 37, no. 12, pp. 737-738, June 2001.

[12] T. Choi, R. Kaneshiro, P. Gray, W. Jett, and M. Wilcox, "High frequency CMOS switched-capacitor filters for communications application," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 652-664, Dec. 1983.

[13] G. C. Temes, "Finite amplifier gain and bandwidth effects in switched-capacitor filters," *IEEE J. Solid-State Circuits*, vol. SC-15, pp 358-361, June 1980.

[14] National Semiconductor, LM117/LM317A/LM317 3-Terminal Adjustable

Regular Data Sheet, Nation Semiconductor, Inc., 1997.

[15] Libin Yao, Michiel S. J. Steyaert, and Willy sansen, " A 1-V 140- μW 88-dB Audio Sigma-Delta Modulator in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, NO. 11, November 2004.

[16] Richard Schreier, Jose Silva, Jesper Steensgaasrd, and Gabor C. Temes, "Design-Oriented Estimation of Thermal Noise in Switched-Capacitor Circuits," *IEEE Transactions on Circuits and Systems*, vol. 52, NO. 11, November 2005.

[17] Waltari, M.; Halonen, K., "Booststrapped switch without bulk effect in standard CMOS technology," *Electronics Letters*, vol. 38, Issue 12, , pp. 55-557, 6 June 2002.

[18] B. Razavi, 1999 ISSCC Short Course.

[19] R. J. BAKER, "CMOS Circuit Design, Layout, and Simulation," IEEE, Inc., 2005.