# 國 立 交 通 大 學

# 電信工程學系

# 碩 士 論 文

## 應用於 UWB 頻率合成器之
## 突波雜訊抑制設計

## Spurious Suppressing Design
## for UWB Synthesizers


研 究 生:黃昱瑞　　Yu-Ruei Huang

指導教授:趙學永 博士　Dr. Hsueh-Yung Chao

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國立交通大學

電信工程學系 電信研究所碩士班


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電信工程學系　電信研究所碩士班

## 摘要

本論文提出一個利用除二電路放置在混頻器的下一級的方式，有效的抑制頻率合成器中頻帶內的突波雜訊。並完成利用 UWB 頻率 3.1-GHz 到 6.3-GHz 作為測試平台的頻率合成器，突波雜訊將產生在頻帶外於欲得到載波頻率兩倍的地方。因此，可與其他操作在 2.5-GHz 及 5.2-GHz 頻段的無線區域網路共同存在。其他突波雜訊抑制的技術，例如：在選頻器上加上 dummy-pair，或是 LC 共振腔內加上可調式的負電阻，都被運用在此工作內來降低雜訊。此外，並完成利用單一頻率源合成出 UWB 所有的頻帶且突波雜訊在所有的頻帶可被壓制在-25dBc 以下。本電路利用聯電 0.13 製程技術完成。

# Spurious Suppressing Design for UWB Synthesizers

Student：Yu-Ruei Huang　　Advisor : Dr. Kuei-Ann Wen

Co-advisor : Dr. Wen-Shen Wuen

*Department of Communication Engineering*

*National Chiao-Tung University*

## Abstract

This thesis presents a CMOS frequency synthesizer with an efficient algorithm for in-band spurious suppression by using the divide-by-two circuit after the mixer. An implementation example had been developed with UWB Synthesizer from 3.1-GHz to 6.3-GHz as the test bench. The spurious are introduced at the twice of the desired carrier frequencies and out of the band. Therefore, it allows to co-existence with WLAN applications operating in 2.5-GHz ISM and 5.2-GHz ISM. Other spurious suppressing techniques, such as selector with dummy pairs and LC resonant loads with tunable negative resistance, are also used in this work to help degrade the undesired tons. Furthermore, a single frequency source is adopted to generate all the bands specified by UWB and the spurious suppression is better than -25dBc in all band groups. The circuits are designed by UMC 0.13-μm CMOS.

# 誌　　謝

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誌予　2007

黃昱瑞

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# Chapter 1
# Introduction

## 1.1 Background

Recently, the Federal Communications Commission (FCC) in US approved the use of ultra-wideband (UWB) technology for commercial applications in the 3.1-10.6 GHz. UWB performs excellently for short-range high-speed uses, such as automotive collision-detection systems, through-wall imaging systems, and high-speed indoor networking. It plays an increasingly important role in wireless personal area network (WPAN) applications. This technology will be potentially a necessity in our daily life, from wireless USB to wireless connection between DVD player and TV, and the expectable huge market attracts various industries. European Computer Manufacturers Association (ECMA) has released a UWB standard (ECMA-368) based on the proposal of Multi-Band OFDM Alliance for a distributed medium access control (MAC) sublayer and a physical layer (PHY) for wireless networks and a standard (ECMA-369) for the interface between implementations of the PHY and MAC [1].

The newly unlicensed UWB technology opens doors to high-speed wireless communications and has been exciting tremendous academic research interest.

## 1.2 Motivation

UWB is a multi-band system, wherein the UWB frequency band from 3.1-10.6 GHz is divided into several bands. According to ECMA-368 standard, the spectrum is divided into 14 sub-bands, each with a bandwidth of 528 MHz. The bands are grouped into five band groups. The first 12 bands are grouped into 4 band groups consisting of 3 bands, and the last two bands are grouped into a fifth band group as shown in Figure 1.1. The supporting data rate can be up to 480Mbps.

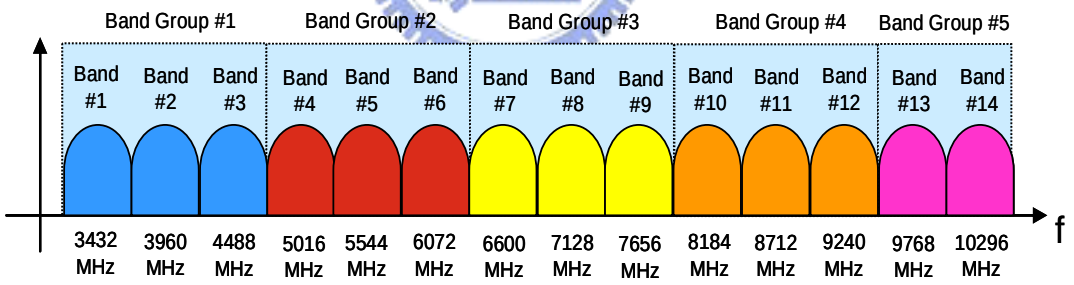



Figure 1.1 The Multi-Band OFDM frequency band plan

Figure1.2. illustrates a UWB transceiver architecture consisting a homodyne transmitter and receiver.

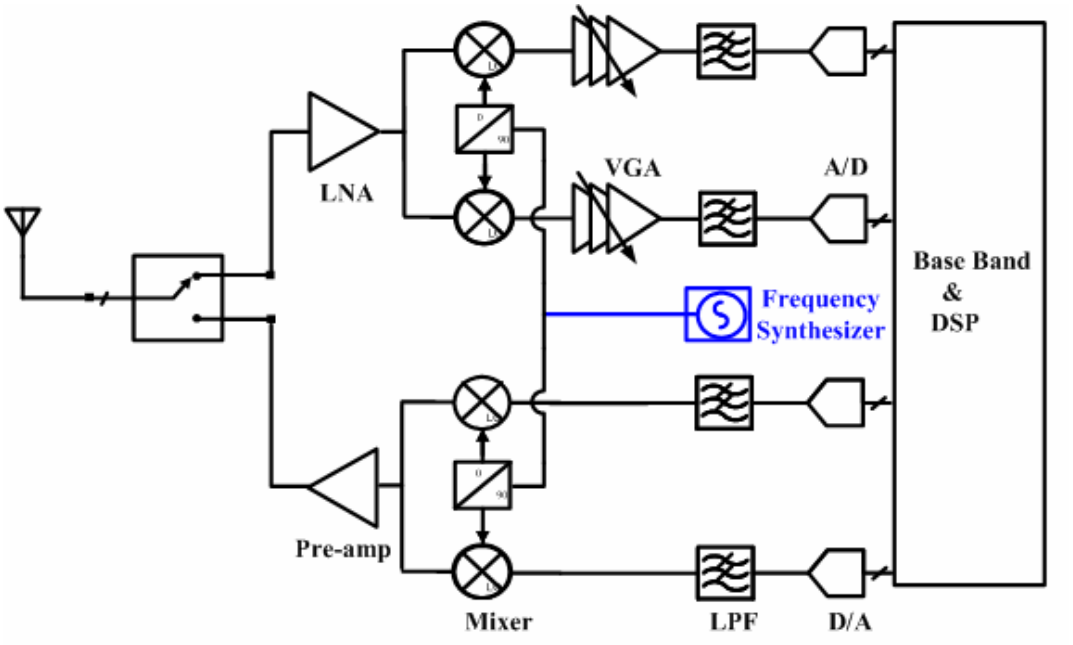



Figure 1.2 The homodyne architecture for UWB transceiver

To perform frequency translation for receiving and transmitting signals, the transceiver consists of a receiver, a transmitter and a frequency synthesizer. In Figure 1.2, the homodyne architecture is also called "direct-conversion" or "zero-IF". The advantage of the homodyne architecture for receiver is that the problem of image in the heterodyne is avoided because $\omega_{IF} = 0$. As the result, no image filter is required to suppress large interferers. But it still exits some problems, such as DC offset, I/Q mismatch, even-order distortion, flicker noise, and etc. However, due to the property of high-integration, we choose the homodyne architecture for RF-SoC.

The synthesizer must provide a clean and stable local oscillator (LO) frequency for receiver and transmitter paths. The frequency band of UWB is from 3.1-10.6 GHz. The frequency range is such wide and the spurious emission will be an important issue. The

spurious will be the series interferer for other nearby wireless systems. In order to co-existence with other wireless systems, such as WLAN applications operating in 2.4-GHz ISM (e.g., IEEE 802.11b/g and Bluetooth) and 5.2-GHz ISM (e.g., IEEE 802.11a), spurious tones must be suppressed near these frequency ranges. The goal of the thesis is to design a frequency with low spurious emission for UWB transceivers.

## 1.3 Specifications of UWB

ECMA368 partitions the spectrum from 3.1-GHz to 10.6-GHz into 528-MHz bands and employs OFDM in each band to transmit data rates as high as 480Mb/s. The relationship between center frequency and band number is given by the following equation :

$$\text{Band center frequency} = 2904 + 528 * Nb,\ Nb = 1 \ldots 14\ (\text{MHz}) \qquad (1.1)$$

The band allocation is summarized in Table 2.1. Each band consists of 128 sub-carriers of 4.125MHz bandwidth. In contrast to IEEE 802.11a/g, MB-OFDM UWB employs only QPSK modulation in each sub-carrier. The system hops at the end of each OFDM symbol (every 312.5ns). The band switching must be in less than 9.47ns. The in–band spurious tones must be less than -12.6dBc. In order to allow co-existence with WLAN applications, the spurious must be less than -36.9dBc at 2.5-GHz and -30.7dBc at 5.2-GHz.

| Band Group | BAND_ID | Lower frequency | Center frequency | Upper frequency |
|---|---|---|---|---|
| 1 | 1 | 3168 MHz | 3432 MHz | 3696 MHz |
| | 2 | 3696 MHz | 3960 MHz | 4224 MHz |
| | 3 | 4224 MHz | 4488 MHz | 4752 MHz |
| 2 | 4 | 4752 MHz | 5016 MHz | 5280 MHz |
| | 5 | 5280 MHz | 5544 MHz | 5808 MHz |
| | 6 | 5808 MHz | 6072 MHz | 6336 MHz |
| 3 | 7 | 6336 MHz | 6600 MHz | 6864 MHz |
| | 8 | 6864 MHz | 7128 MHz | 7392 MHz |
| | 9 | 7392 MHz | 7656 MHz | 7920 MHz |
| 4 | 10 | 7920 MHz | 8184 MHz | 8448 MHz |
| | 11 | 8448 MHz | 8712 MHz | 8976 MHz |
| | 12 | 8976 MHz | 9240 MHz | 9504 MHz |
| 5 | 13 | 9504 MHz | 9768 MHz | 10032 MHz |
| | 14 | 10032 MHz | 10296 MHz | 10560 MHz |

Table 1.1 OFDM PHY band allocation

### 1.3.1 Spurious Tones

To derive the spurious tones specification of the frequency synthesizer, consider the Table 1.2 from [1], we can use maximum tolerable interferer at the antenna to calculate.

| | Microwave Oven | Bluetooth & 802.15.1 Interferer | 802.11b & 802.15.3 Interferer | 802.11a Interferer | 802.15.4 Interferer |
|---|---|---|---|---|---|
| Front-end pre-select filter attenuation (dB) | 35 | 35 | 35 | 30 | 35 |
| Max. tolerable interfere power at the antenna(dBm) | -7.3 | -5.8 | -5.8 | -17 | -7.1 |

Table 1.2 Interference and Susceptible Analysis

In the receive path, the SNR of the wanted signal is calculated as the following :

$$SNR = P_{wnated} - P_{noise} \tag{1.5}$$

$$SNR = P_{wnated} - (P_{\text{int}erfer} - P_{spurs}) \tag{1.6}$$

$$P_{spurs}(\Delta\omega) = P_{wanted} - P_{\text{int}erfer} - SNR \tag{1.7}$$

If we have front-end pre-select filter attenuation, the changes are as the following equations:

$$P_{spurs}(\Delta\omega) = P_{wanted} - P_{\text{int}erfer} - SNR + P_{filter} \tag{1.8}$$

For example, if the transceiver operates at band 1, and the data rate is 110Mb/s, the spurious specification at 1.032GHz can be calculated. The minimum sensitivity of the receiver is -74.1dBm.The required SNR is 3.6dB.

$$P_{spurs}(1.032GHz) = -74.1 + 7.3 - 3.6 + 35 = -35.4(dBc) \tag{1.9}$$

The interferers may be mixed with the spurs of the LO signal and down-converted to baseband, corrupting the desired signal. In the UWB system, it is difficult to meet the LO spurs specification.

### 1.3.2 Switching Time

In the UWB system, the time between two hopping carrier frequency is 9.47ns. It is difficult to use only phase-locked loops to meet the requirement. Dividers, selectors and mixers can be used to change the synthesized frequency to different bands, and

therefore the switching time can be less than 9.47ns.

The overall design specification of the frequency synthesizer for UWB standard is shown in Table 1.3. The power consumption is designed as small as possible.

| Parameters | Specification |
|---|---|
| Frequency range | 3432Mhz~10296Mhz |
| Switching Time | <9.47ns |
| In-band spurs | <-12.6dBc |
| Out-band spurs(at2.5G) | <-36.9dBc |
| Out-band spurs(at5.2G) | <-30.7dBc |
| Supply Voltage | 1.2 V |
| Process | UMC 0.13-μm CMOS |

Table 1.3 Overall design Specification of the frequency synthesizer.

# 1.4 Organization

This thesis describes the design of spurious suppressing for frequency synthesizers with application to ultra wideband transmitter and receiver. Chapter 1 introduces the motivation and the specifications of frequency synthesizer for the UWB WPAN applications. Chapter 2 discusses the spurious suppressing techniques for frequency synthesizer. Chapter 3 presents the state of the art, frequency planning and design of the frequency synthesizer in this work. The implementation of the frequency synthesizer,

the layout, and the testing setup are described in Chapter 4. Chapter 5 gives the conclusions and the future works.

# Chapter 2
# Spurious Suppressing Techniques

## 2.1 Divide-by-Two After the Mixer

The spurious after divide-by-two circuit are lower than spurious before it was presented in lecture [3]. The divide-by-two circuit consists of two flip-flops. In Figure 2.1, considering two tones at ω1 and ω2 are applied to the input of a D-flip-flop, which is part of a divide-by-two circuit. ω1 is the interest signal and ω2 is the undesired spurious with the amplitude A. The spurious tone frequency ω2= ω1+Δω and by using linear superposition, it can be decomposed into equal amplitude modulation (AM) and phase modulated (PM) sidebands. Each of them is the same amplitude A/2, and they disposed symmetrically at $\omega_1 \pm \Delta\omega$.

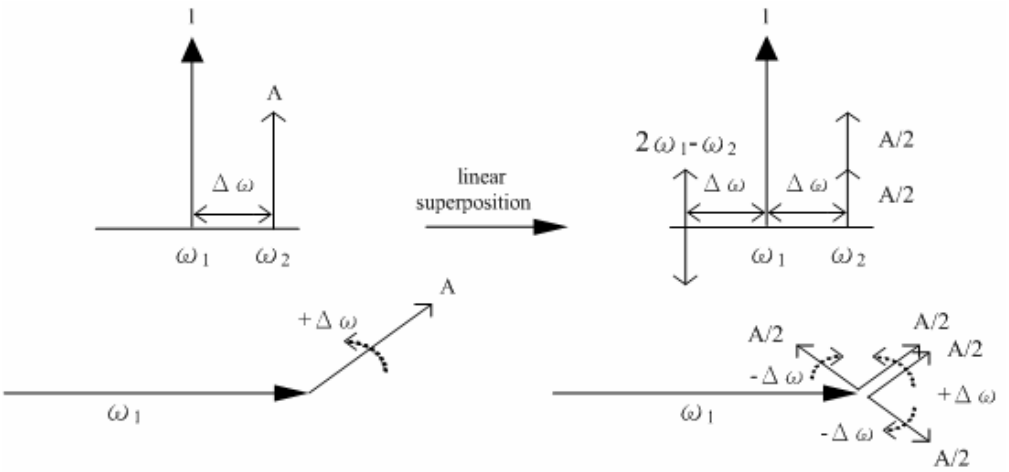



Figure 2.1 Decomposing a unwanted tone into equivalent AM and PM sidebands

Assuming the differential threshold is zero, the flip-flop is only sensitive to the threshold crossing of the input signals. It does not react to variations in the input amplitude. Therefore, while input AM and PM signals are applied to the flip-flop, it only responds to the input PM signal.

Now, assuming the input PM signal is applied to the flip-flop. When the differential clock input across zero with positive slope, the flip-flop output toggles. It is clear in the time-domain input and output waveforms, which is shown in Figure 2.2. The output waveform tracks every other input waveform with positive slope. The deviation in time is also tracked by the flip flop. However, the output frequency is half of the input frequency, and it also corresponds to the deviation in phase which at output signal is half to the input signal. Thus, the output PM sidebands are half of the input PM sidebands. The amplitude of the PM sidebands at output are $\frac{A}{4}$. However, the rate or

relative frequency of PM is still unchanged. Thus, the sidebands are located at $\frac{\omega_1}{2} \pm \Delta\omega$.

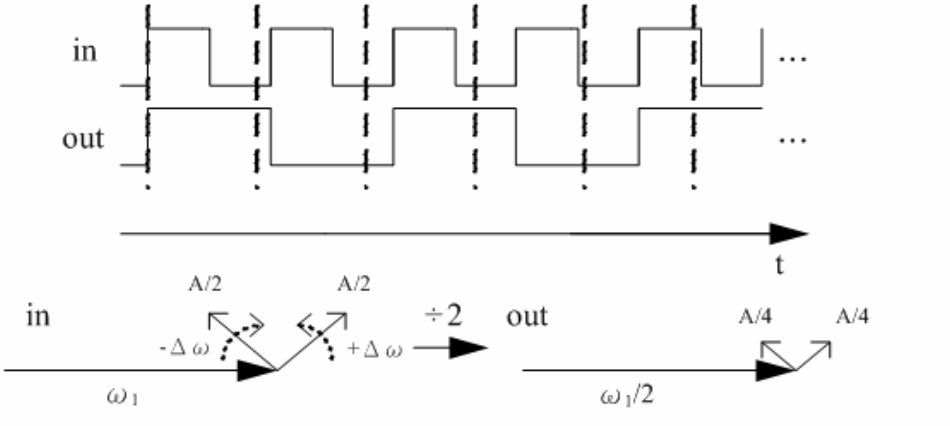



Figure 2.2 Output waveforms of a divide-by-2 circuit when PM signal is input

To sum up, when large input tone and small undesired spurious are applied to the to the divide-by-two, the large input tone is divided by two, and each of the small undesired spurious is surrounded symmetrically located around the large tone at the same frequency offset as the single input spurious. But the spurious' relative amplitude with input amplitude is at 1/4 (-12 dB). In Figure 2.3, further frequency divide-by-two conserves the spur separation but lowers the relative levels by 6 dB.

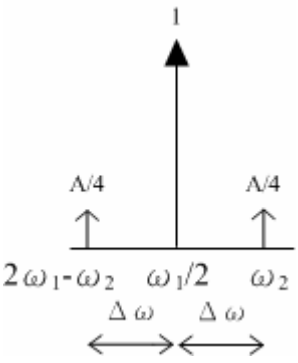



Figure 2.3 Output spectrum of divide-by-2 circuit

About the single-sideband mixer, it needs quadrature input signals. When there are gain and phase mismatches in quadrature input signals or the single-sideband mixer, the spurious tones will be introduced at the output of the mixer. From above discussing, if the divide-by-two circuit is after the mixer, it can help to suppress the spurious which are generated by the mixer.

Figure 2.4(a) shows the carrier frequency at the output of the mixer and before the divide-by-two circuit. And Figure 2.4(b) shows the spectrums after the divide-by-two after the divide-by-two circuit. Each of the small spurious is surrounded symmetrically around the large carrier frequency at the same frequency offset as the input spurious. The spurious' amplitude is lower -12dB than the input amplitude.

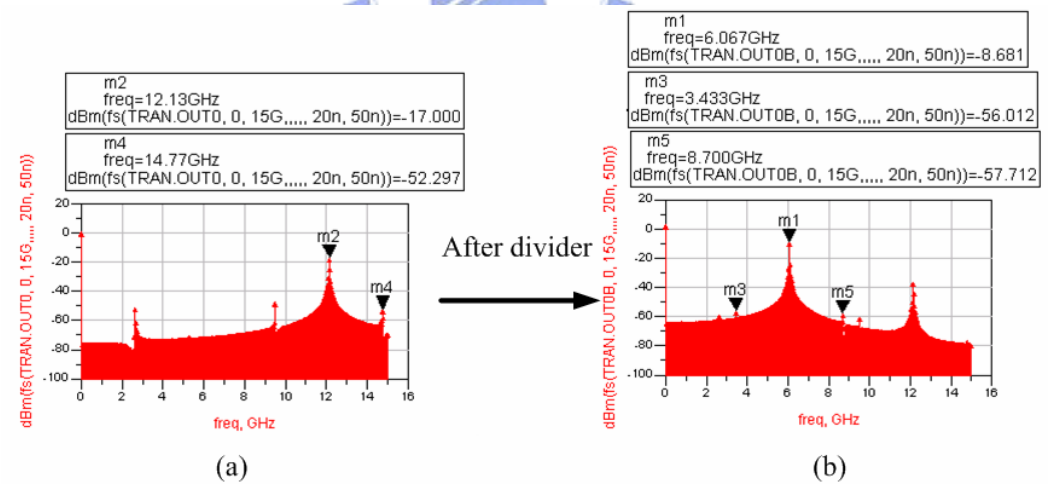



Figure 2.4 Frequency spectrums before and after the divide-by-two circuit

## 2.2 Selector with Dummy Pairs

For a selector, it must provide fast switching and symmetry with respect to its two

inputs. In Figure 2.5, there are two input signal $V_{in1}$ and $V_{in2}$. A conventional current-steering selector may suffer from unwanted modulation, since the unselected signal in the disabled pair would still couple to the output through the parasitic capacitance $C_{gd}$. It will produce the spurious at the selector output. In Figure 2.6, two dummy pairs, $M_5$-$M_6$ and $M_7$-$M_8$, are introduced to selector to reduce the undesired coupling to the first order while consuming no extra power. The simulation results are shown in Figure 2.7, the selector with dummy pairs can suppress the undesired spurious almost 20dB.

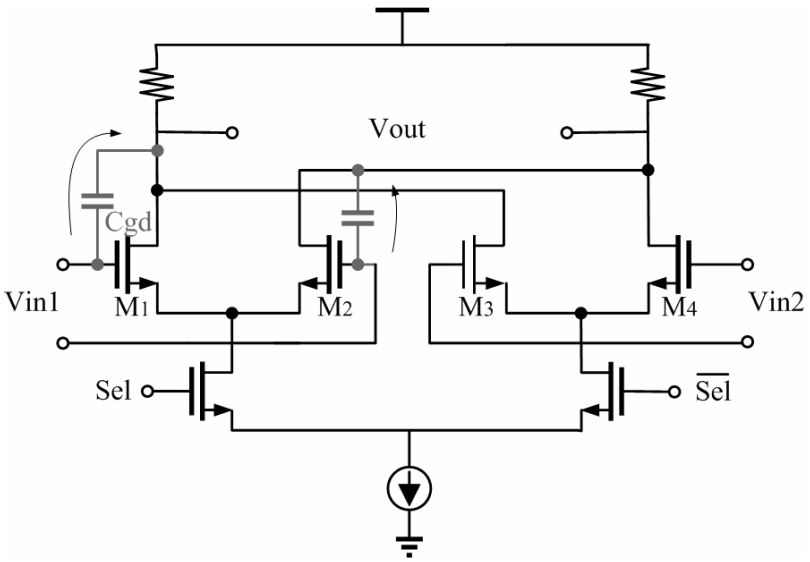



Figure 2.5 Conventional selector

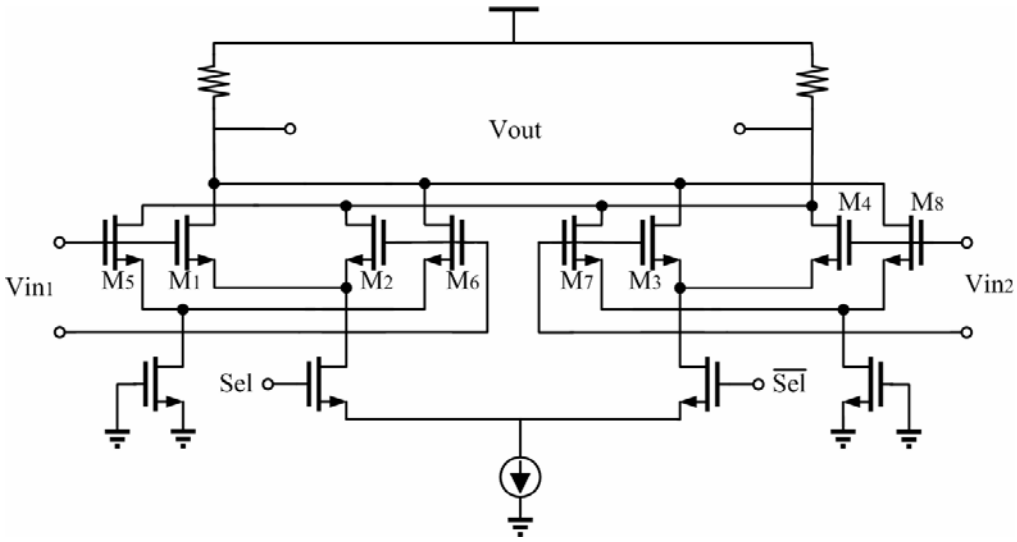
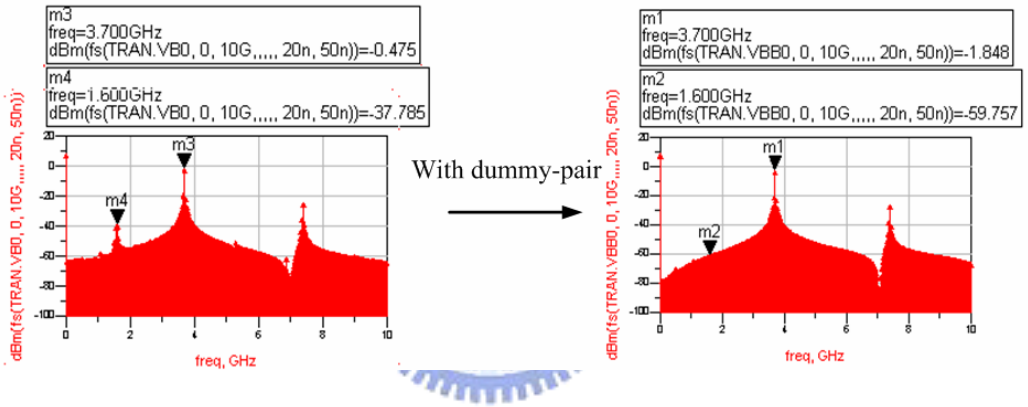



Figure 2.6 Selector with coupling cancellation technique




(a) Conventional selector (b) Selector with dummy-pair

Figure 2.7 Selector with and without cancellation technique

## 2.3 Single-Sideband Mixer

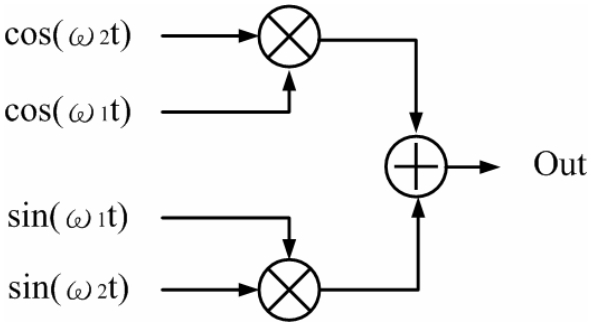



Figure 2.8 Ideal SSB mixer

Single-sideband mixers are used in the proposed synthesizer. As shown in Figure 2.8, the equation between the output and the input of the mixer can be expressed as following.

$$Out = \cos(\omega_1 t)\cos(\omega_2 t) \pm \sin(\omega_1 t)\sin(\omega_2 t) = \cos(\omega_2 \mp \omega_1)t \quad (2.1)$$

Therefore, the single-sideband mixer can make the undesired sideband lower. Because it requires quadrature inputs, the two issues which are the mismatches between the quadrature inputs and the nonlinearities will be concerned.

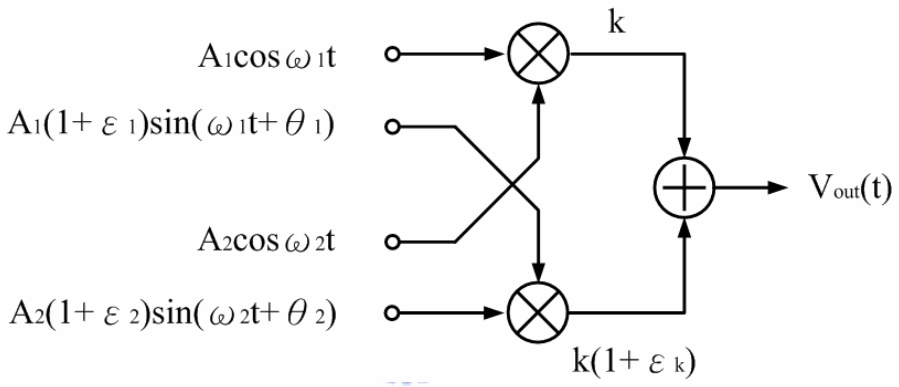



Figure 2.9 Non-ideal SSB mixer

To evaluate the sideband caused by mismatches, considering a non-ideal single-sideband mixer shown in Figure 2.9. The gain mismatches between two inputs present $\varepsilon_1$ and $\varepsilon_2$, and phase imbalance of $\theta_1$ and $\theta_2$. And the gain mismatch between the two mixers represent as $\varepsilon_k$. The output is expressed to

$$v_{out}(t) = kA_1A_2\cos(\omega_1 t)\cos(\omega_2 t)$$

$$+ k(1+\varepsilon_k)A_1(1+\varepsilon_1)A_2(1+\varepsilon_2)\sin(\omega_1 t+\theta_1)\sin(\omega_2 t+\theta_2) \quad (2.2)$$

where $A_1, A_2$ is denoted the input amplitudes and $k$ is the gain of mixer. Denoting

$C_1 = kA_1A_2$ and $C_2 = k(1+\varepsilon_k)A_1(1+\varepsilon_1)A_2(1+\varepsilon_2)$, we obtain that

$$v_{out}(t) = C_1 \frac{\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t}{2} + C_2 \frac{\cos[(\omega_1+\omega_2)t+\theta_1-\theta_2] - [\cos(\omega_1-\omega_2)t+\theta_1+\theta_2]}{2} \quad (2.3)$$

The desired signal at $\omega_1 - \omega_2$ is given by

$$v_{sig}(t) = \frac{C_1}{2}\cos(\omega_1-\omega_2)t + \frac{C_2}{2}\cos[(\omega_1-\omega_2)t+\theta_1-\theta_2] \quad (2.4)$$

$$= \sqrt{k_1^2+k_2^2}\cos[(\omega_1-\omega_2)t+\alpha] \quad (2.5)$$

where $k_1 = [C_1 + C_2\cos(\theta_1-\theta_2)]/2$, $k_2 = C_2\sin(\theta_1-\theta_2)]/2$, and $\alpha = \tan^{-1}(k_2/k_1)$.

And the image sideband at $\omega_1+\omega_2$ can be expressed

$$v_{im}(t) = \frac{C_1}{2}\cos(\omega_1+\omega_2)t - \frac{C_2}{2}\cos[(\omega_1+\omega_2)t+\theta_1+\theta_2] \quad (2.6)$$

$$= \sqrt{k_3^2+k_4^2}\cos[(\omega_1+\omega_2)t-\beta] \quad (2.7)$$

where $k_3 = [C_1 - C_2\cos(\theta_1+\theta_2)]/2$, $k_4 = C_2\sin(\theta_1+\theta_2)]/2$, and $\beta = \tan^{-1}(k_4/k_3)$.

Thus, the sideband rejection caused by mismatches is given by

Sideband Rejection (dB)

$$= 10\log_{10}\frac{k_1^2+k_2^2}{k_3^2+k_4^2} \quad (2.8)$$

$$= 10\log_{10}\frac{1+2\frac{C_2}{C_1}\cos(\theta_1-\theta_2)+(C_2^2/C_1^2)}{1-2\frac{C_2}{C_1}\cos(\theta_1+\theta_2)+(C_2^2/C_1^2)} \quad (2.9)$$

Therefore, the phase and gain errors of a single-sideband mixer cause the image sideband. For example, if $\theta_1 = 1^o$, $\theta_2 = 0^o$, and C2/C1 = 0.1dB, The sideband of -39.6dBc would be presented at the single-sideband mixer output.

## 2.4 LC Tank

The single-sideband mixer shown in Figure 2.10 incorporates band pass loads to suppress spurious [2]. In order to achieve broadband operation, the single-sideband mixer with inductor loads are used. Band selection is accomplished by using capacitor arrays to change the resonances frequency of the tanks. However, the tank impedance would be degraded with increasing capacitances. Thus, the tank impedance at lower frequencies is lower than higher frequencies.

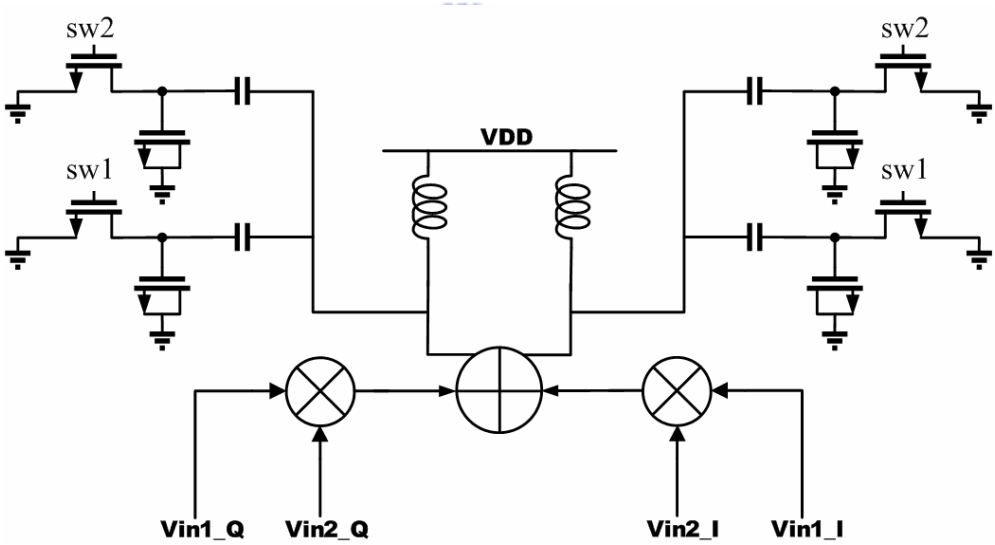



Figure 2.10 A SSB mixer with band pass loads

In Figure 2.11, the capacitor array is accomplished by using the capacitor, the varactor and the NMOS switch. The capacitor is designed larger than the varactor. When the voltage $V_C$ is GND, the NMOS switch is open, the capacitor is series to the varactor and the capacitance is dominant by the varactor. On the other hand, when the

voltage $V_C$ is VDD, the NMOS switch is turned on, the capacitance is equal to the capacitor. Therefore, using capacitor arrays can achieve the wide range operation.

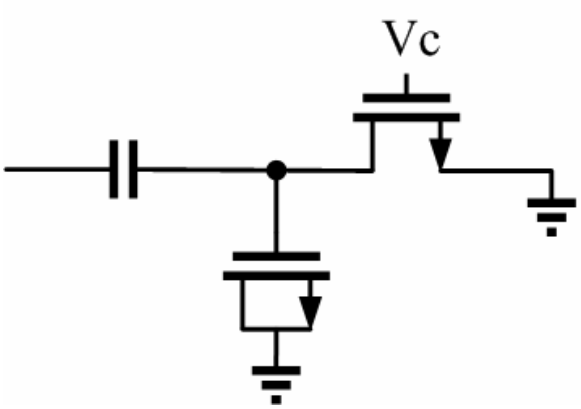



Figure 2.11 Consist of capacitor array

In Figure 2.12, the impedance of the LC tank with 3-bit capacitor arrays is shown. The impedance is lower at the lower frequency. Therefore, it must be compensated.

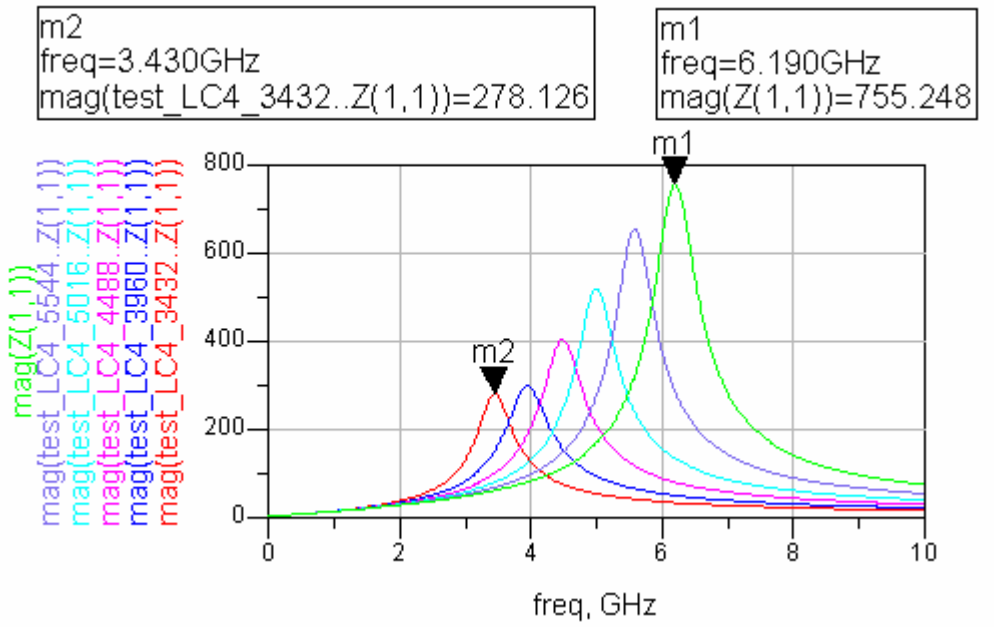



Figure 2.12 The impedance of the LC tanks with 3-bit capacitor arrays

## 2.5 LC Tank with Tunable Negative Resistance

In order to have band-pass load which can operate many band groups in system, a lot of capacitance arrays are used to change the resonant frequency. More capacitance also means more parasitic resistances which will degrade the quality factor of the LC tank. In order to have a high quality factor, a negative resistance is put in parallel in the LC tank.

Figure 2.13(a) shows the implement of the negative resistance. Consider the potential difference between two gates is equal to V, which is shown is Figure 2.13(b).

Then it can be expressed as following :

$$V_{gs1} - V_{gs2} = -V \tag{2.10}$$

$$I = g_m V_{gs1} = -g_m V_{gs2} \tag{2.11}$$

$$\therefore \frac{-I}{g_m} - \frac{I}{g_m} = V \tag{2.12}$$

Therefore, the negative resistance can be obtained :

$$Z_{in} = \frac{V}{I} = \frac{-2}{gm} \tag{2.13}$$

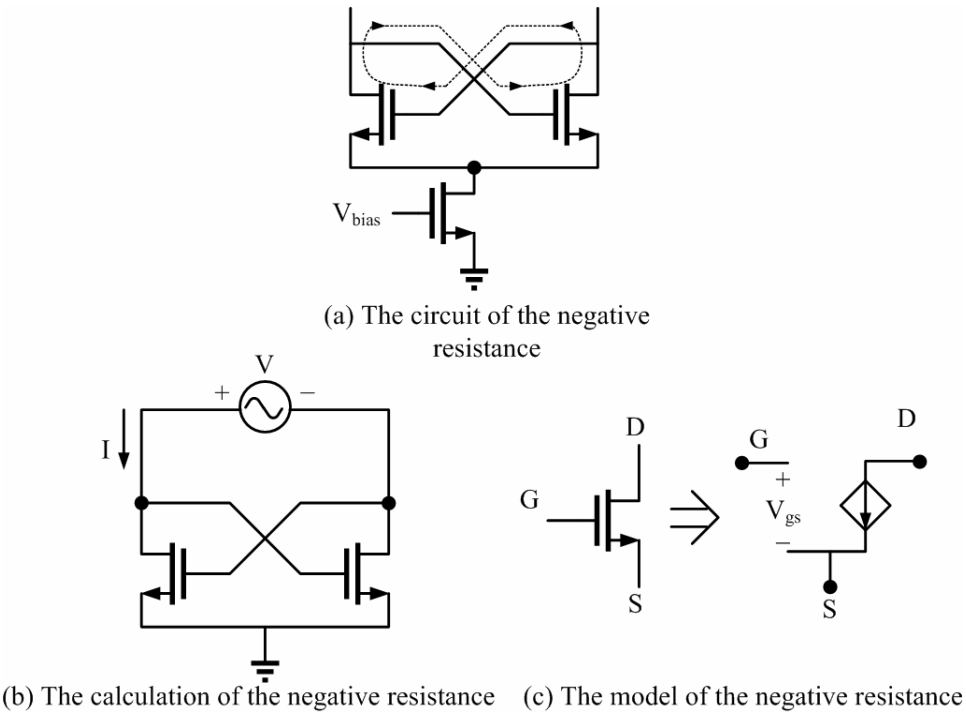



Figure 2.13 The negative resistance

Even though the negative resistance can compensate for the quality factor, the impedance at the lower frequency is still lower. Thus, another tunable negative resistance is also put in the tank to improve the impedance at lower frequency. The architecture is shown in Figure 2.14. The tunable negative resistance can compensate the parasitic resistance and increase the quality factor.

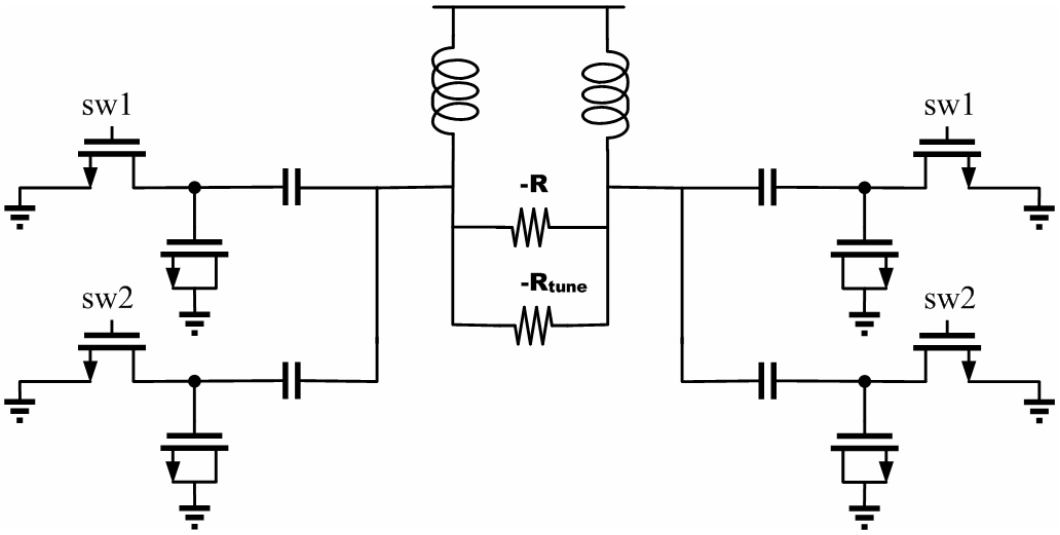



Figure 2.14 LC tanks with tunable negative resistance

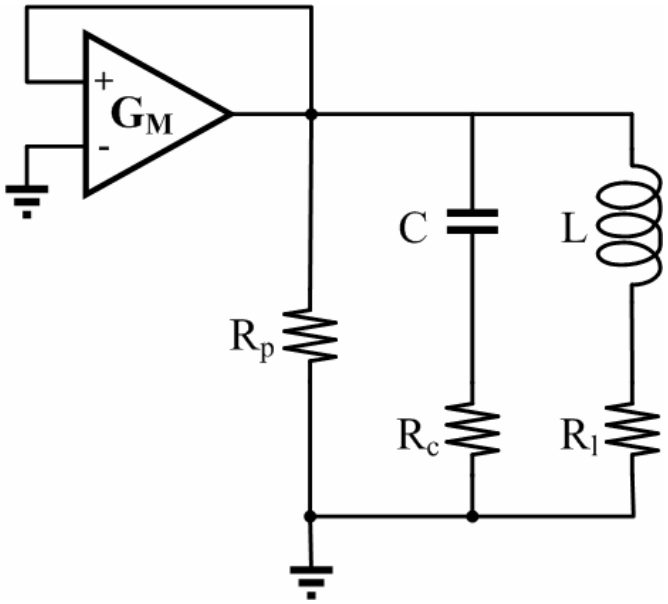



Figure 2.15 The model of the LC tank with negative resistance

The model of the LC tank with negative resistance is shown in Figure 2.15. The feedback over the transconductor $G_M$ is positive. The parasitic resistances are also shown. A series resistance $R_C$ with the capacitor C, a series $R_l$ with the inductor L, and the output resistance of the transconductor, and the parallel resistances across C and L, are represented by $R_p$. Then, the method of superposition is used. First, considering $R_p$

is the only parasitic effect. The loop transfer function is derived by cutting the loop and the result in this case is

$$T_{Rp}(s) = G_m \cdot \frac{sL}{1 + s\frac{L}{R_p} + s^2 LC} \tag{2.14}$$

The imaginary part of the loop transfer function is equal to

$$\mathrm{Im}\{T_{Rp}(\omega)\} = G_m \cdot \frac{\omega L \cdot (1 - \omega^2 LC)}{(1 - \omega^2 LC) + \omega^2 \cdot (\frac{L}{R_p})^2} \tag{2.15}$$

and is zero for

$$\omega_0 = \frac{1}{\sqrt{L \cdot C}} \tag{2.16}$$

The frequency $\omega_0$ is the resonant frequency. The transconductance $G_M$ necessary to have a loop transfer function exactly equal to one. The transconductance value is the one needed to compensate for the losses in the resistor $R_p$ and represented by $G_{M,Rp}$. It is given by

$$G_{M,Rp} = \frac{G_M}{T_{Rp}(\omega_0)} = \frac{1}{Rp} \tag{2.17}$$

In the same way, considering the only parasitic resistance is $R_l$ which is the series resistance of the inductor. The transconductance $G_{M,Rl}$ is given by

$$G_{M,R_l} = R_l \cdot \frac{C}{L} \tag{2.18}$$

And when the capacitor series resistance $R_C$ is only for consideration, the transconductance $G_{M,Rc}$ is equal to

$$G_{M,R_C} = R_C \cdot \frac{C}{L} \tag{2.19}$$

Now, the previous equations can be summarized by the following :

$$R_{eff} = R_C + R_l + \frac{1}{R_p \frac{C}{L}} \tag{2.20}$$

$$G_M = R_{eff} \cdot \frac{C}{L} \tag{2.21}$$

Therefore, the transconductance $G_M$ is proportional to the capacitor C. When the capacitor increases, it also means that the current of the positive feedback must be raised to increase the transconductance but can not make the LC tank oscillate. Thus, the quality factor of the LC tank can be improved.

Figure 2.16 and 2.17 show the impedance of the LC tank without and with negative resistance respectively. And Figure 2.18 shows the impedance of the LC tank with another tunable negative resistance. With the tunable negative resistance, the resonant impedance at lower frequency is much higher and the impedance is much flatter.

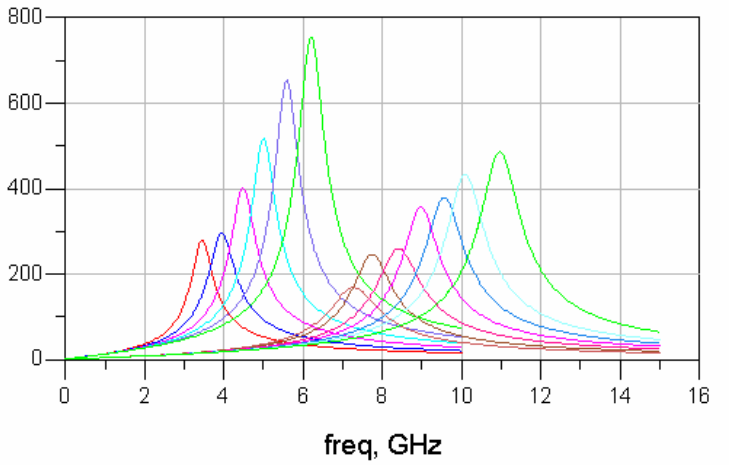



Figure 2.16 LC tanks without negative resistance

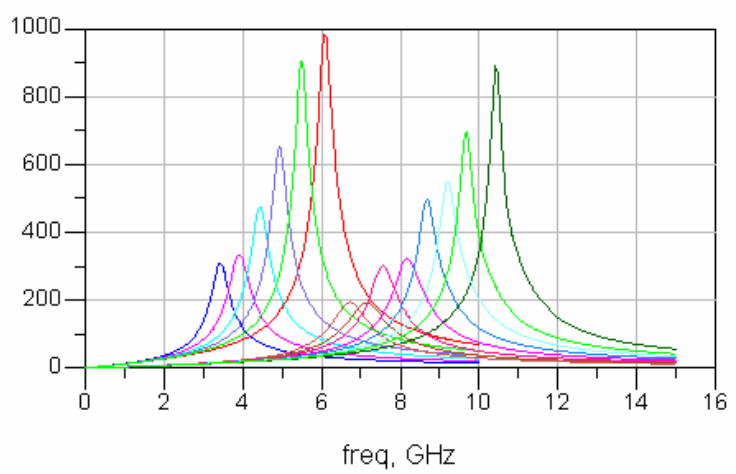



Figure 2.17 LC tanks with negative resistance

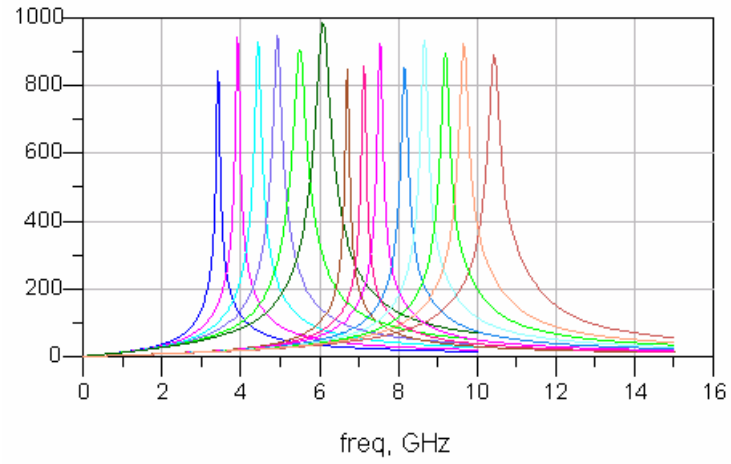



Figure 2.18 LC tanks with tunable negative resistance

The current through the tunable negative resistance from the frequency 3432-MHz to 6072-MHz is shown in Figure 2.19. The maximal current at 3432-MHz is 2.1mA. And the current through the tunable negative resistance from the frequency 6600-MHz to 10296-MHz is shown in Figure 2.20. The maximal current at 6600MHz is 1.164mA.

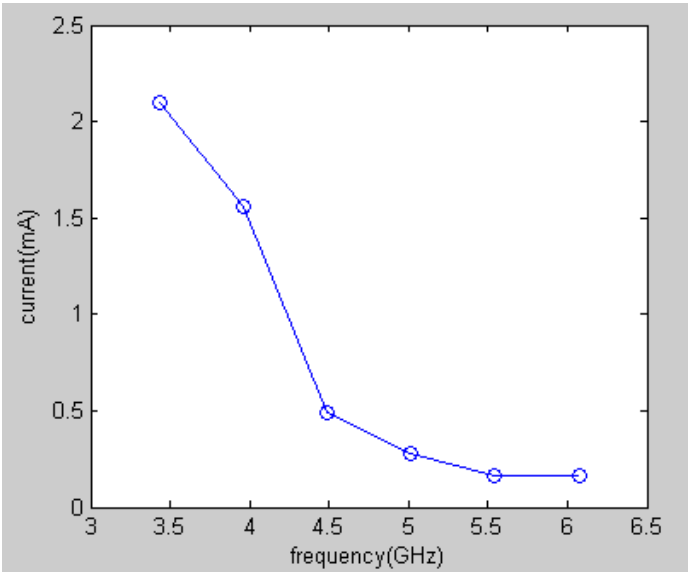



Figure 2.19 The current through the tunable negative resistance from 3432MHz to 6072MHz

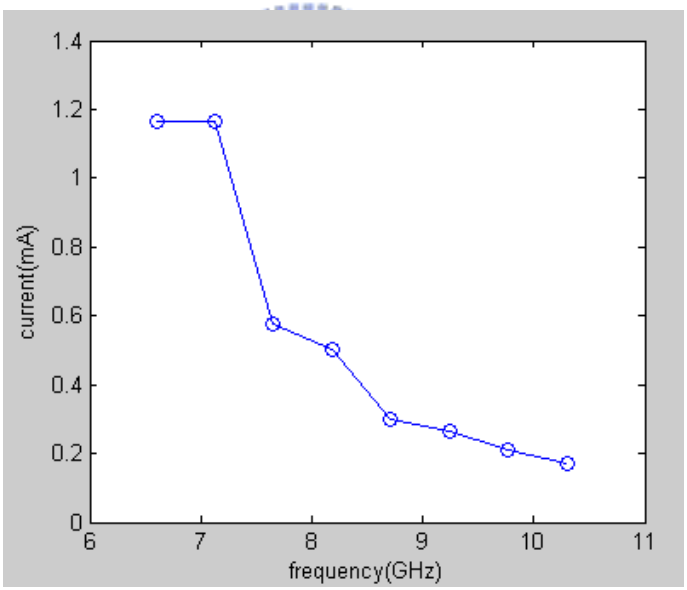



Figure 2.20 The current through the tunable negative resistance from 6600MHz to 10296MHz

Figure 2.21 and 2.22 show the comparison with the single-sideband mixer with R loads and with LC loads. The mixer with the LC loads which is compensated with the

tunable negative resistance can efficiently suppress the spurious at the output of the mixer.

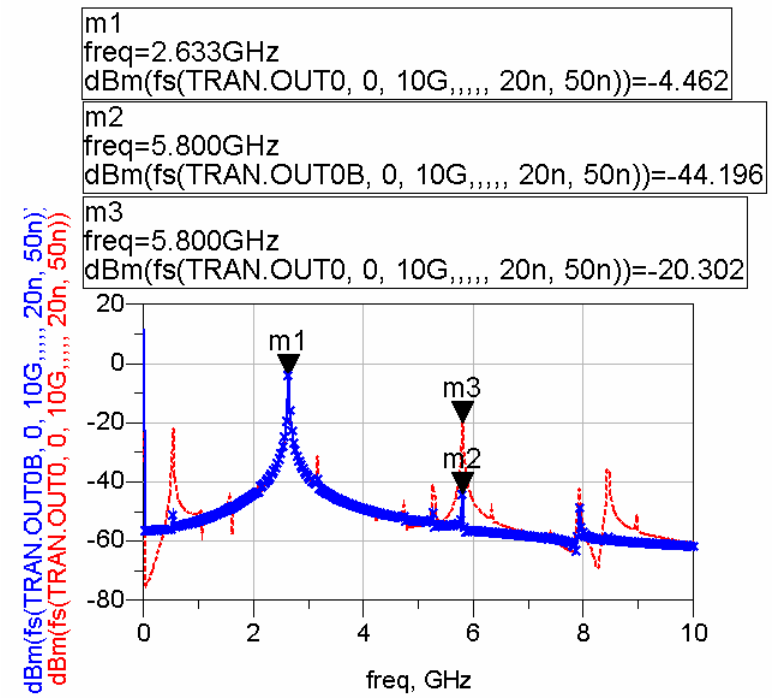



Figure 2.21 Output spectrums at 2640-MHz

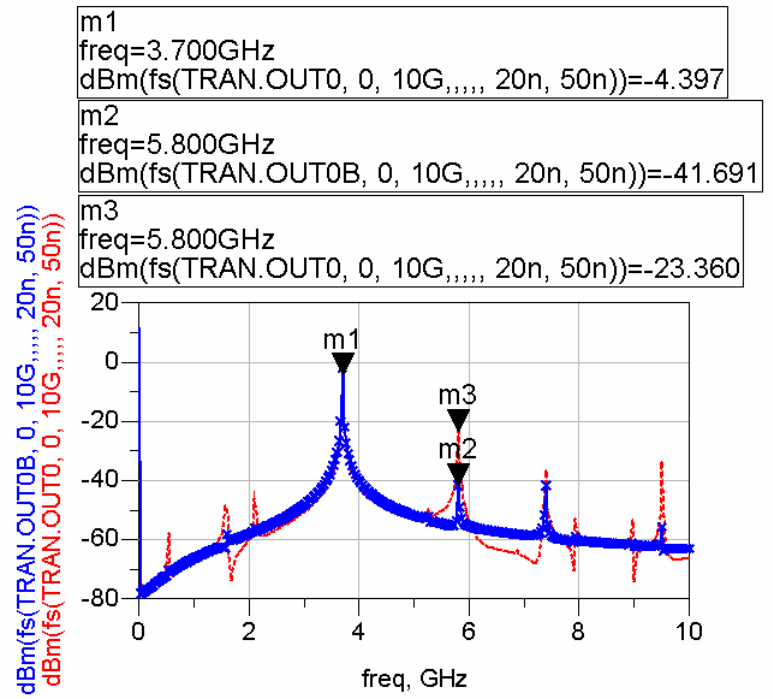



Figure 2.22 Output spectrums at 3696-MHz

# Chapter 3
# UWB Synthesizer Design

## 3.1 Architecture of UWB Synthesizer

In the UWB system, the range of the frequency is from 3.1 GHz to 10.6 GHz, and the switching time is 9.47ns. For using the conventional PLL-base frequency synthesizer, it is difficult to meet the switching time because the locking time of the phase-locked loop is almost several hundreds of nano seconds or several micro seconds. In order to achieve the fast-hopping, there are some ways can be used, such as using multiple PLLs or some PLLs with the single-sideband mixers to synthesize the frequency bands. They are discussed in the following sections. And to allow co-existence with wireless LAN applications operating, such as 802.11a/b/g, the spurious suppressing is also an important issue for consideration.

### 3.1.1 Topology 1

In [7], the UWB synthesizer is shown in Figure 3.1. It is designed to operate in the

band group 1. The frequencies of the band group 1 are 3432-MHz, 3960-MHz, and 4488-MHz. These three frequencies are generated by using three fixed-modulus phase-locked loops. Therefore, the spurious at the phase-locked loop output is lower because the single-sideband mixer can be avoided using. The gain or phase mismatch of the single-sideband mixer will introduce the undesired sideband at the output of the single-sideband mixer. The output frequency is decided by the selector between the three output frequencies of the phase-locked loops. But it may sensitive to inductor coupling and carrier leakage in this architecture. Thus a good layout to provide good isolation is important. If the number of the bands increases, more phase-locked loops must be used, and it will consume more power and production cost.

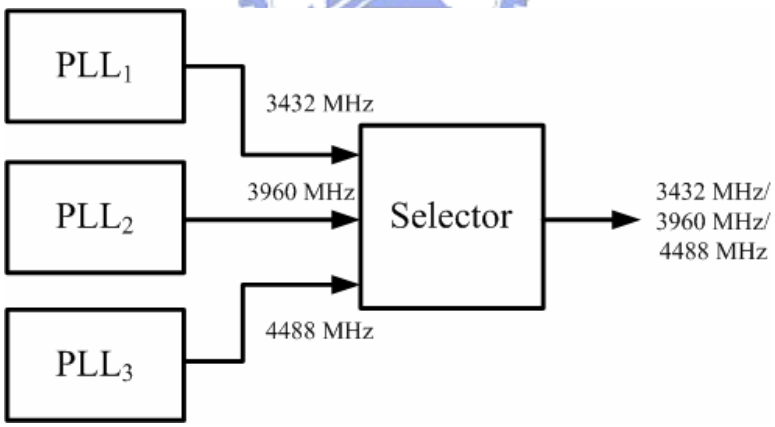



Figure 3.1 The three PLLs frequency synthesizer

### 3.1.2 Topology 2

In [10], the synthesizer generates all fourteen bands and the frequency plan is shown in Figure 3.2. There are two phase-locked loops and three single-sideband

mixers in the architecture as shown in Figure 3.3. The 3 sub-bands in the first group, 3432-MHz, 3960-MHz, and 4488-MHz, are realized by the first phase-locked loop and the first mixer. The first phase-locked loop generates the center frequency of 3960-MHz in the first group and the second phase-locked loop provides the band spacing frequency of 528-Hz and the group spacing frequencies of 1584-MHz, 3168-MHz, and 6336-MHz. Therefore, the third and fifth groups can be obtained from the second mixer by up-converting the first group with the group spacing frequencies. Then, the fourth group is generated from the third mixer by down-converting the fifth group with group spacing frequency of 1584-MHz. But it arises a problem of the spurious which are due to the cascading mixers. The spurious at the first mixer output will be the input of the second mixer and generate the higher-order spurious at the output of the second mixer. Therefore, the higher-order spurious tones must be taken into consideration when the groups are up-converted by the second mixer and third mixer. And the switched-capacitor LC tanks are placed at the mixer output as the output buffers to suppress the spurious.

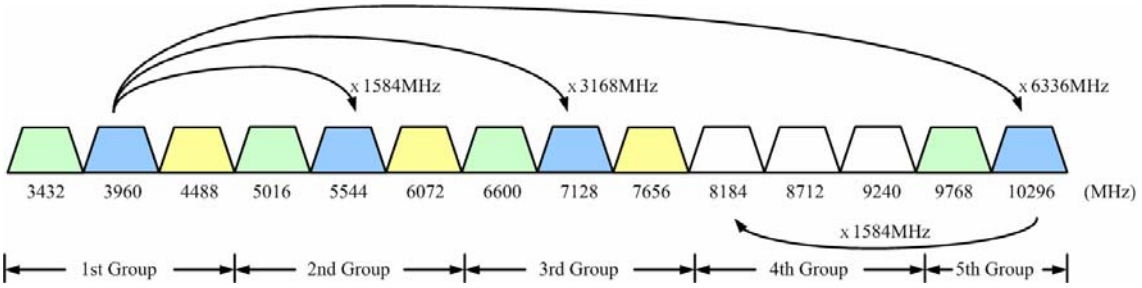



Figure 3.2 The frequency plan of the synthesizer

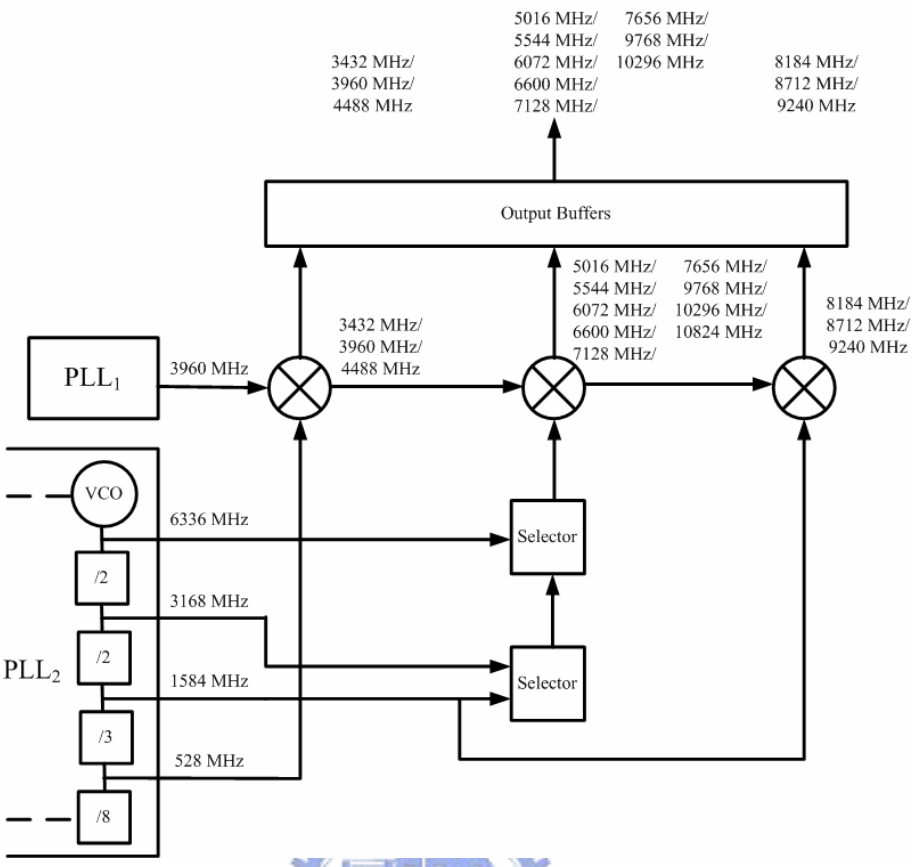



Figure 3.3 The 14-bnad UWB frequency synthesizer

## 3.1.3 Topology 3

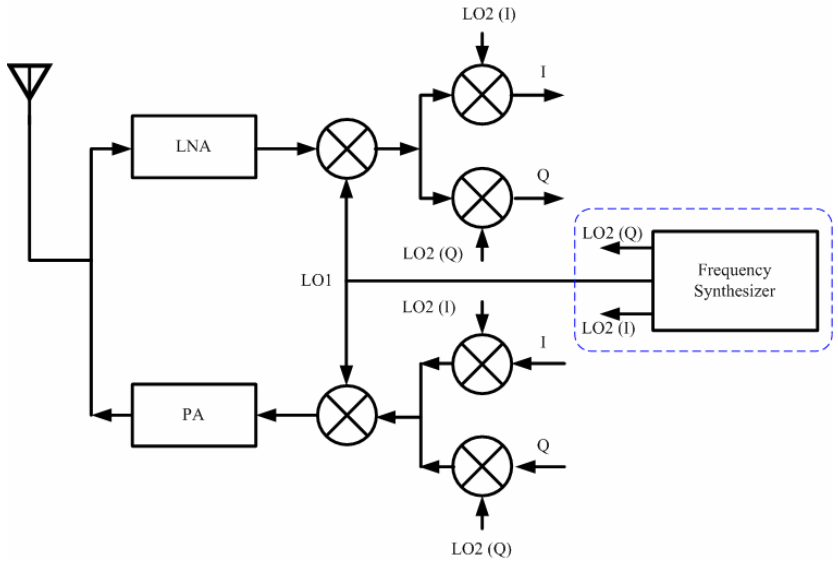



Fig 3.4 Dual-conversion UWB synthesizer

In [13], the dual-conversion frequency synthesizer is presented in Figure 3.4. The first three band groups with total nine bands are included, which is from 3.1 to 8 GHz. The frequency synthesizer makes down-conversion twice. As Figure 3.5 and the architecture in Figure 3.6, it uses a phase-locked loop, three single-sideband mixers, and a selector to synthesize two LO signals. LO1 frequencies from 6336-MHz to 10560-MHz is generated from the local frequency 8448-MHz mixing with the offset frequencies such as 2112-MHz, 1584-MHz, 1056-MHz, 528-MHz, and DC. And LO2 frequency of 2904-MHz is obtained with using the spurious suppressing technique of the divide-by-two after the mixer. The band pass LC tank is also used in this architecture.

The first LO1 signal down-converts RF signals to a fixed IF frequency at 2904-MHz. Then the second LO2 signal further down-converts the IF signal to zero IF. The dual-conversion frequency synthesizer can provide the advantages of avoiding the LO leakage. The LO leakage will not appear in the frequency bands.

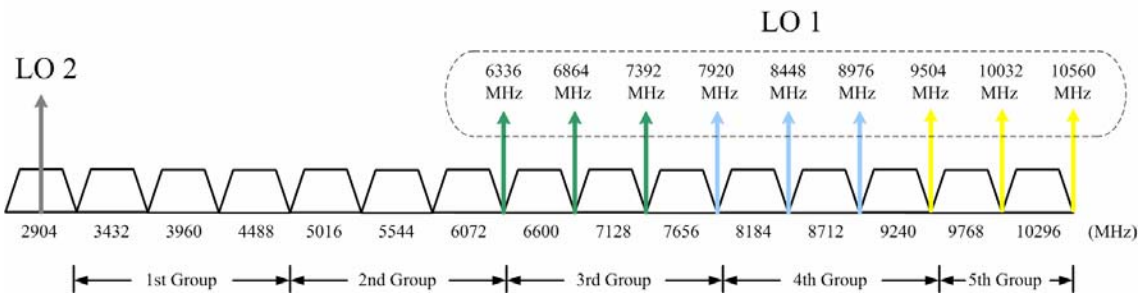



Fig 3.5 Dual-conversion frequency scheme

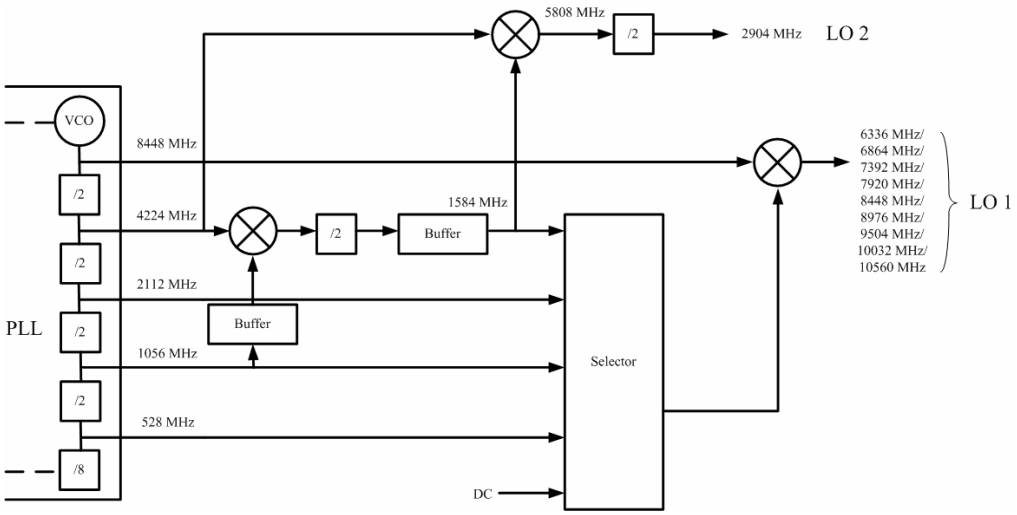



Fig 3.6 The architecture of dual-conversion synthesizer

### 3.1.4 Topology 4

In [14], the frequency plan is shown in the Figure 3.7 and the architecture is in Figure 3.8. Only one PLL is used in this architecture and generated the frequency of 8448-MHz. Using the divide-by-two produces the frequency of 4224-MHz from 8448-MHz. Now these two frequencies take the UWB center frequencies into two parts. One part is close to 4224-MHz and the other part is close to 8448-MHz. And the offset frequencies such as 264-MHz, 792-MHz, 1320-MHz, and 1848-MHz are produced from other frequency dividers and the single-sideband mixer. The spurious suppressing technique of the divide-by-two after the mixer is used in this architecture. The frequency divider is placed after the first single-sideband mixer. The LC tanks as band pass filters are also used at the output of the frequency synthesizer.

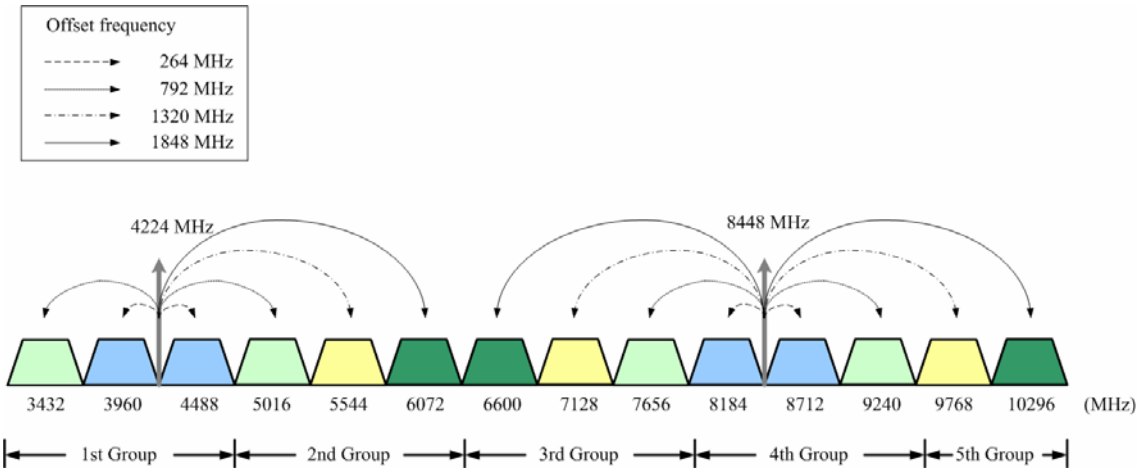



Fig 3.7 The frequency plan of the 3.1-GHz to 10.6-GHz UWB frequency synthesizer

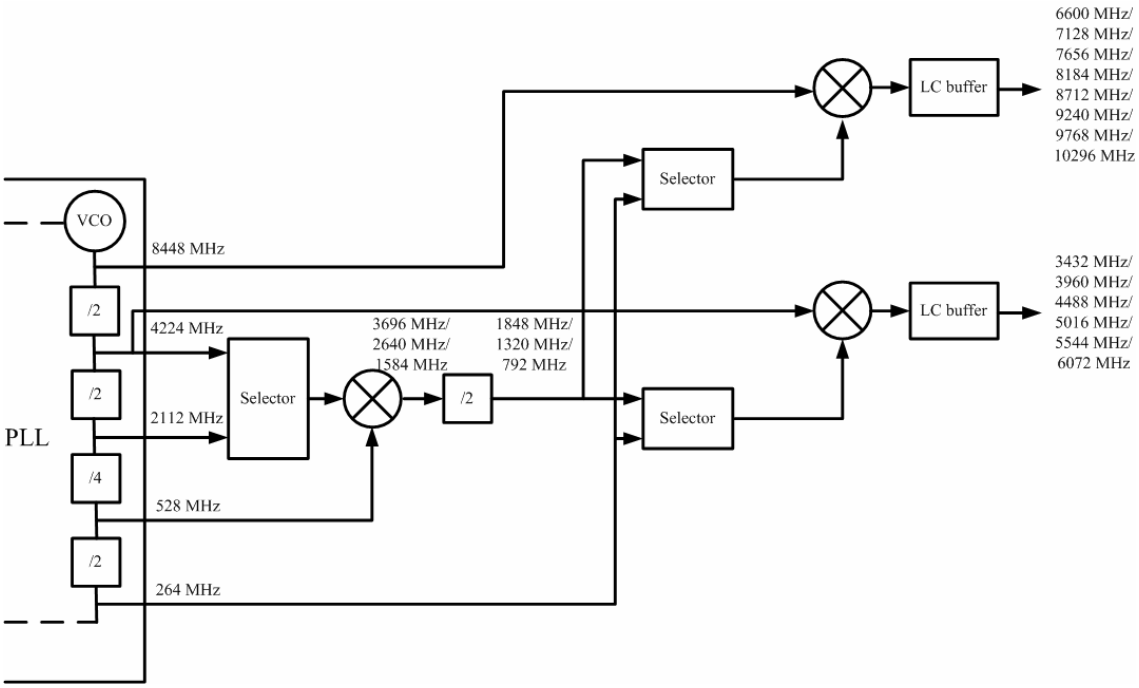



Fig 3.8 The architecture of the 3.1-GHz to 10.6-GHz UWB frequency synthesizer

There are a lot of ways to implement the UWB frequency synthesizer. If the architecture only uses the phase-locked loops to accomplish the synthesizer, the spurious problem is not series because the mixers are not employed in it. But in order to obtain more frequency bands, more phase-locked loops will be used. More phase-locked

loops means more power will be consumed and the problem of carrier leakage will be increased. If the mixers are included in the frequency synthesizer, fewer phase-locked loops are used and the power consumption will be saved. But the mismatch of mixer will introduce the spurious problem. The trade off must be make carefully in the design to achieve fast switching time and lower spurious while do not increase the area and power.

## 3.2 Frequency Planning

Because the switching time of UWB is 9.47ns, and in order to synthesize all band group frequencies, more single-sideband mixers are used in the architecture. One of the advantages is that multiple phase-locked loops will not be used. It only needs less phase-locked loops and can synthesize all frequencies. Much die area and power will be saved. But using more single-sideband mixers means that the unwanted sidebands are accumulated through multi-stage mixing. And the issue of the spurious suppressing will be important.

Based on the architecture of [14], only one phase-locked loop is used, and the frequencies 8448-MHz and 4224-MHz are generated in it. The UWB frequencies are separated into two parts. One part is the frequencies from 3432-MHz to 6067-MHz, and they are synthesized by using the center frequency 4224-MHz and offset frequencies

such as 264-MHz, 792-MHz, 1320-MHz, and 1848-MHz which 264-MHz is generated from the phase-locked loop and others are generated from the divider after the first single-sideband mixer. Another part is the frequencies from 6600-MHz to 10296-MHz, and they are synthesized by using center frequency 8448-MHz with the same offset frequencies.

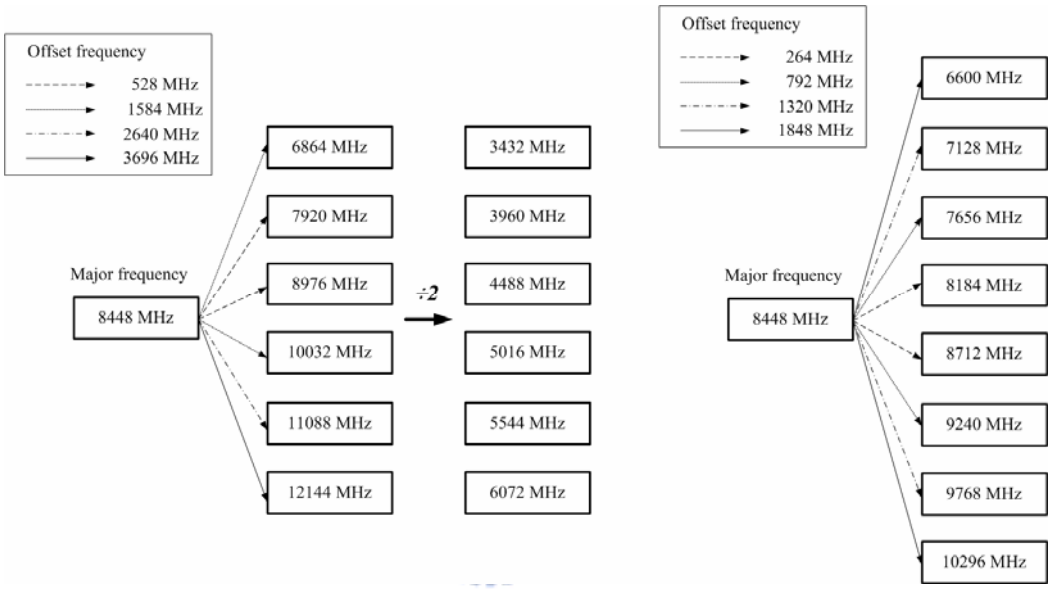



Figure 3.9 Two parts of the UWB frequency bands

For the consideration of spurious suppressing, the technique of the divide-by-two circuit after the mixer is used at the second stage before the output of frequency synthesizer in the new architecture in this work. The frequency planning is shown in Fig 3.9 and Fig 3.10 is the architecture of this work. The first part with center frequency 4224-MHz in the original architecture is changed to use the center frequency 8448-MHz, as same as the second part. It also means the offset frequencies are twice as before, such as 528-MHz, 1584-MHz, 2640-MHz, and 3696MHz. The frequency 528-MHz is

generated from the phase-locked loop and others are generated from the first single-sideband mixer. After the second stage of the mixer with up-converting or down-converting, the frequencies are introduced from 6867-MHz to 12144-MHz, such as twice UWB frequencies from 3432-MHz to 6072-MHz. Using the spurious suppressing technique of the divider after the second stage of the mixer to obtain the UWB frequencies. The LC tank with switched-capacitor arrays and the tunable negative resistance are also used at the output of synthesizer and the first single-sideband mixer as band pass loads. But the second part of UWB frequencies from 6600-MHz to 10296-MHz is the same frequency planning as before. The frequencies are synthesized by using the center frequency 8448-MHz and the offset frequency such as, 264-MHz, 792-MHz, 1320-MHz, and 1848-MHz. The divide-by-two circuit after the mixer before the output of frequency synthesizer is not used at the second part. This is because that if the divider is added at the output of the second stage of the single-sideband mixer, it also means the frequencies at the output of single-sideband mixer will be twice as the UWB frequencies, and the maximum frequency will be up to 20592-MHz. The performance will degrade because more undesired high frequency effects are induced and it will also consume more power. Because the center frequencies of these two parts are also 8448-MHz, only one mixer is used at the second stage to generate all UWB frequency.

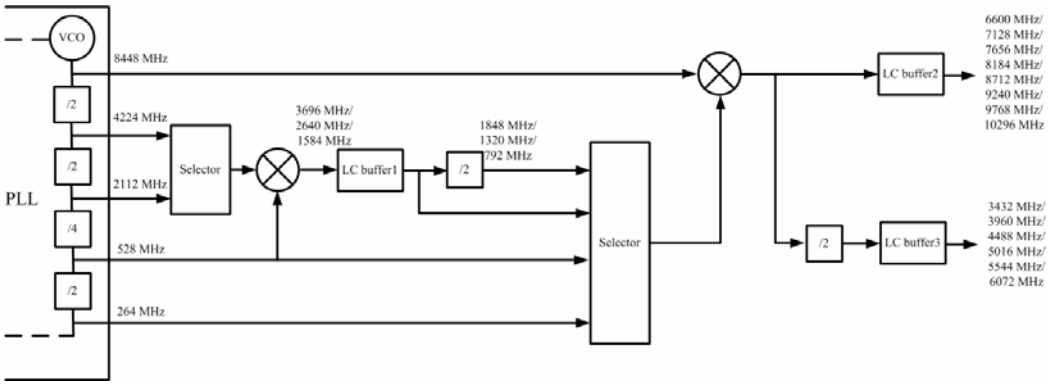



Figure 3.10 Architecture of this work

# 3.3 Circuit Design

## 3.3.1 Frequency Divider

High-speed frequency dividers are critical in a variety of applications from frequency syntheses in wireless communications to broadband optical fiber communication systems. For the considerations of high speed, low power, and high sensitivity, the divide-by-two circuit is realized by using source-coupled logic (SCL) in this work.

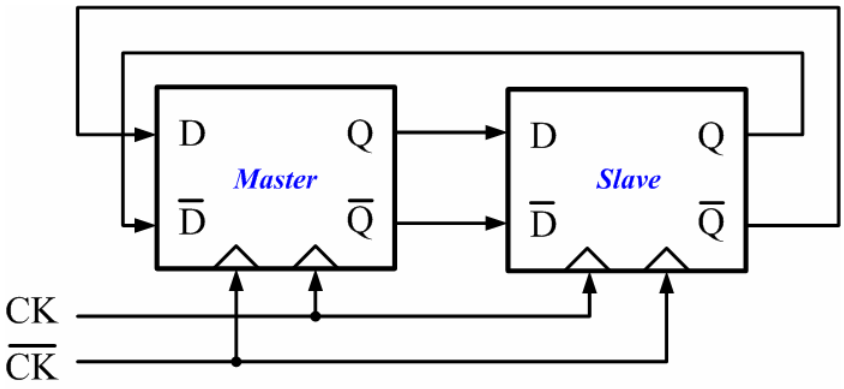



Figure 3.11 Block diagram of the frequency divider

Fig. 3.11 shows the block diagram of the divide-by-two circuit. The divider is

based on the classical mister-slave D-type flip-flop in which the inverted slave outputs are connected to the master inputs.

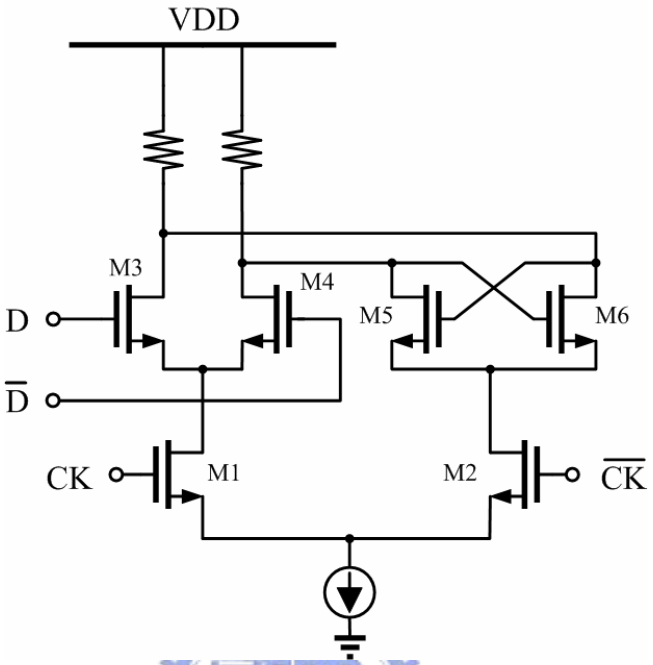



Figure 3.12 The circuit diagram of each latch

Fig. 3.12 shows a typical source-couple latch. The master or slave consists of an evaluate stage (M1, M3, M4) and a latch stage (M2, M5, M6). When the clock signal is high, the evaluate stage turns on, and the input sampling pair M3-M4 senses the input signal. On the other hand, when latch stage turns on, the cross-coupled pair M5-M6 forms a positive feedback loop. The operating speed is dominated by the RC time constant at the output node and the transconductance of the regenerative pair.

In order to increase the maximum operating speed of the frequency divider, the internal voltage swing should be kept as small as possible. Thus, the time required for toggling the logic state is shorter. Increasing the current source or supply voltage, but

the power consumption will also be increased.

Figure 3.13 shows the required minimal input voltage swing versus input frequency of the frequency divider. In Figure 3.14, the transient simulation result of the frequency divider is shown. And the output frequency spectrum is shown in Figure 3.15. The input signal is 8.448-GHz, and the output frequency is obtained 4.224-GHz.

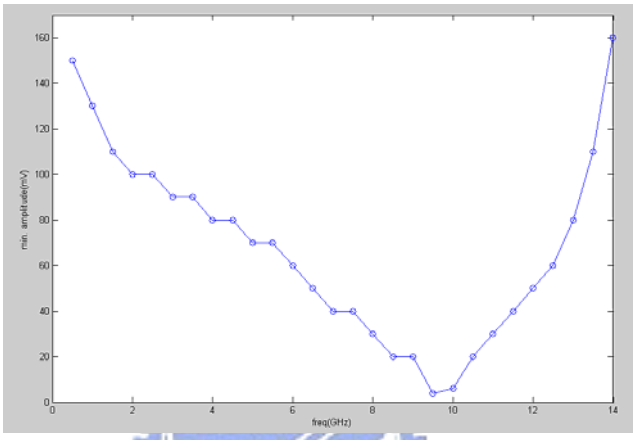



Figure 3.13 The minimal input voltage swing versus input frequency

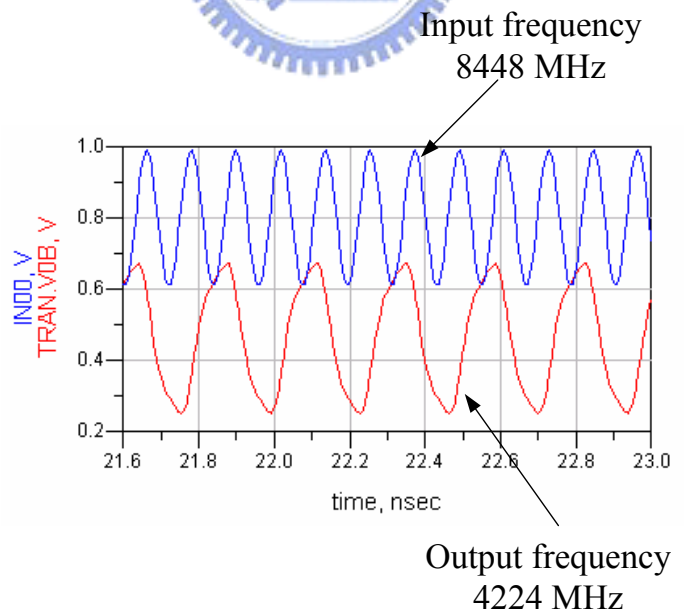



Figure 3.14 Transient simulation result of the frequency divider

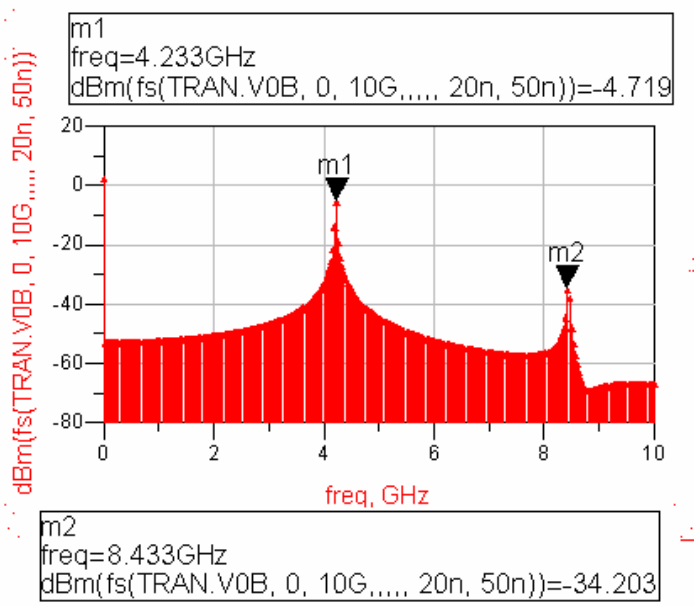



Figure 3.15 The output spectrum of the frequency divider

## 3.3.2 Single-Sideband Mixer with LC Buffer

In Figure 3.16, the double-balanced mixer with the resistive load is presented. The double-balanced mixer generates less even-order distortion and it needs quadrature inputs to perform frequency additions and subtractions. In order to cover wide input frequency range, The multiple current sources and Gm stages are used. When the current source transistor pair M1-M2 turns on, the Gm stage transistors M5-M8 translate the input voltages to currents and mix the other input signals of the mixer. Similarly, when the current source transistor pair M3-M4 turns on, the Gm stage transistors M9-M12 translate the input voltages to currents and mix the input signals of the mixer. Thus, the output frequencies are changed between the current source transistor pair which is selected.

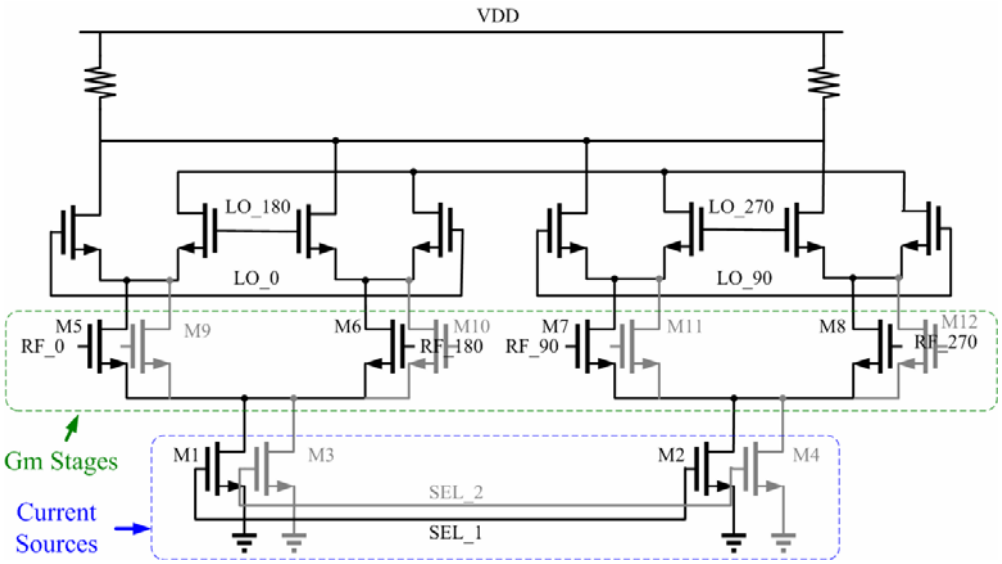



Figure 3.16 The SSB mixer with multiple Gm stages and current sources

In order to obtain the pure carrier frequency at the mixer output, the resistive load is replaced with the programmable band pass load to suppress the spurious. The programmable band pass can operate at the hopping frequency. The resonant frequency of the band pass load is decided by the capacitor arrays. And the tunable resistance is inserted to increase the quality factor of the tank. As Figure 3.17, the programmable band pass load is combined with the single-sideband mixer.

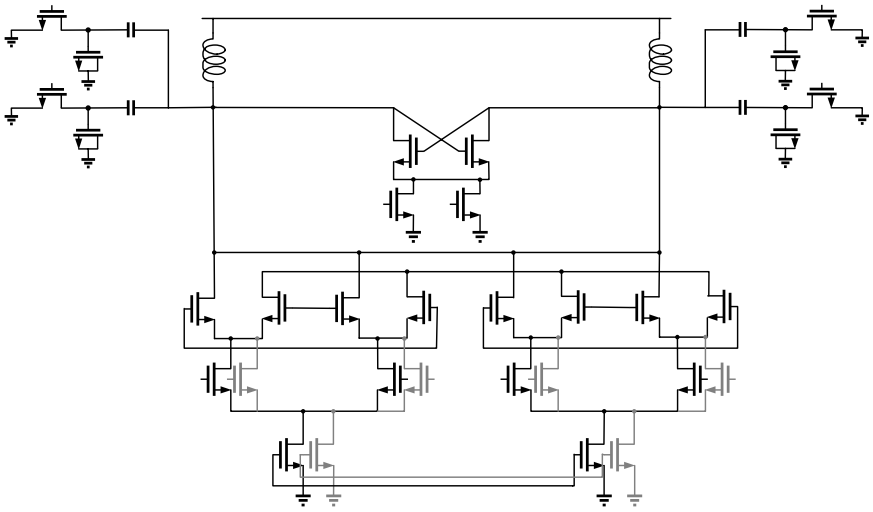


Figure 3.17 The SSB mixer with band pass load

The last building block of the frequency synthesizer is the selector, passive mixer, and LC buffer shown in Figure 3.18. The selector is with dummy pairs to reduce the undesired coupling. The architecture is folded with LC loads. Thus, the carrier swing will not limit by the small overdrive voltage and can be amplified by the LC buffer. The tunable negative resistances are also used in the LC buffer to compensate the parasitic resistance of the LC tank.

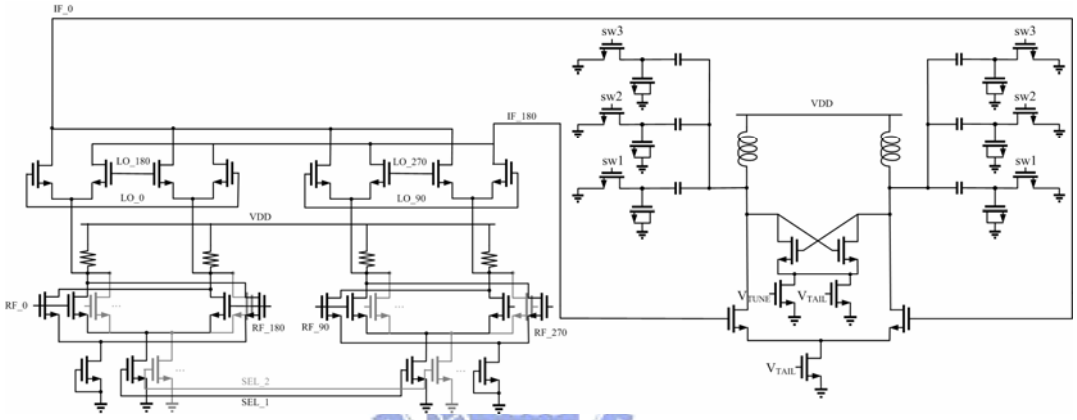
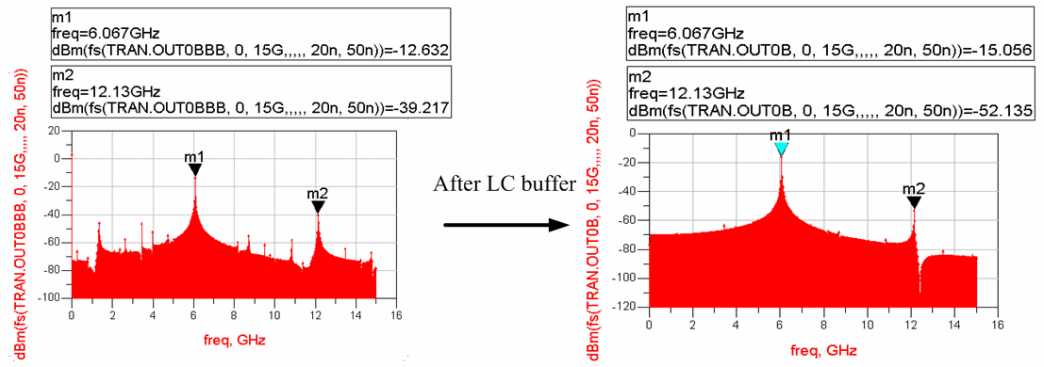


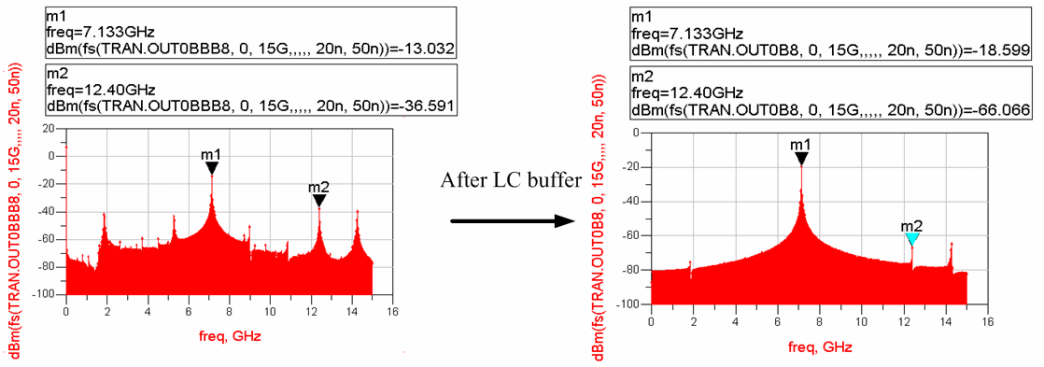

Figure 3.18 The selector, the passive mixer, and the LC buffer

The output spectrum is shown in Figure 3.19 and Figure 3.20. The carrier frequencies are 6072-MHz and 7128-MHz. After the LC buffer, the frequency spectrum is purer. In Figure 3.21, the switching time between two different carrier frequencies is shown. The switching time is less than 9.47ns.



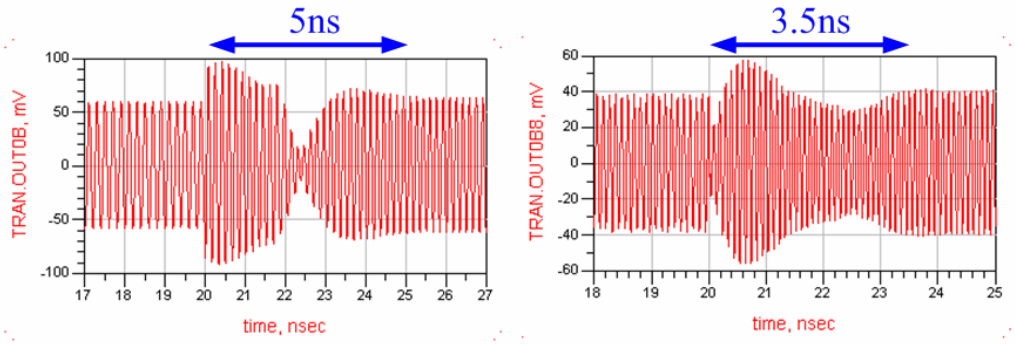

(a) Spectrum before the LC buffer (b) Spectrum after the LC buffer

Figure 3.19 Output frequency spectrums (f = 6072-MHz)




(a) Spectrum before the LC buffer (b) Spectrum after the LC buffer

Figure 3.20 Output frequency spectrums (f = 7128-MHz)




(a) The frequency changes from 5016-MHz to 6072-MHz (b) The frequency changes from 9240-MHz to 10296-MHz

Figure 3.21 Switching time between two different carrier frequencies

## 3.4 Summary

The simulation results of the signal generator circuit are shown in Table 3.1. The spurious tones at frequency bands from 3432-MHz to 6072-MHz appear at the twice of the carrier frequencies and the comparison with lecture [14] is presented in Table 3.2. The spurious are better than -25dBc in all frequency bands. The switching time is less than 9.47 ns.

| Frequency band (MHz) | Output power (dbm) | Spurs (dbc) | Distance to spur (MHz) |
|---|---|---|---|
| 3432 | - 10.803 | - 34.715 | 3434 |
| 3960 | - 13.009 | - 37.513 | 3966 |
| 4488 | - 15.401 | - 35.895 | 4467 |
| 5016 | - 18.337 | - 35.071 | 5030 |
| 5544 | - 16.085 | - 38.502 | 5567 |
| 6072 | - 15.056 | - 37.079 | 6063 |
| 6600 | - 15.413 | - 41.164 | 6600 |
| 7128 | - 18.599 | - 47.467 | 5267 |
| 7656 | - 22.325 | - 35.442 | 3163 |
| 8184 | - 20.962 | - 25.027 | 1040 |
| 8712 | - 20.118 | - 26.514 | 1060 |
| 9240 | - 21.132 | - 31.132 | 553 |
| 9768 | - 22.565 | - 42.407 | 5267 |
| 10296 | - 21.566 | - 51.302 | 2900 |

Table 3.1 Simulated performance of the signal generator circuit

| | This work | | | [14] | | |
|---|---|---|---|---|---|---|
| Frequency band (MHz) | Output power (dbm) | Spurs (dbc) | Distance to spur (MHz) | Output power (dbm) | Spurs (dbc) | Distance to spur (MHz) |
| 3432 | - 10.803 | - 34.715 | 3434 | - 18.928 | - 37.2 | 3474 |
| 3960 | - 13.009 | - 37.513 | 3966 | - 16.644 | - 30.744 | 1080 |
| 4488 | - 15.401 | - 35.895 | 4467 | - 21.717 | - 32.618 | 1067 |
| 5016 | - 18.337 | - 35.071 | 5030 | - 20.631 | - 32.584 | 1858 |
| 5544 | - 16.085 | - 38.502 | 5567 | - 17.153 | - 32.057 | 1050 |
| 6072 | - 15.056 | - 37.079 | 6063 | - 15. 99 | - 39.904 | 2133 |

Table 3.2 Performance comparison with lecture [14]

The performance comparison of the frequency synthesizer is summarized in Table 3.2.

| | Process ( $\mu$ m) | Power ( mW) | Spurious ( dBc) | Supply voltage(V) | Frequency range( GHz) | No. of bands | Architecture | Year |
|---|---|---|---|---|---|---|---|---|
| [7] | 0.13 CMOS | 45 | -60 (only one on ) | 1.5 | 3.1~4.5 | 3 | PLL*3 | 2005 |
| [8] | 0.18 CMOS | 18 | -20 | 1.8 | 3.1~4.5 | 3 | PLL+SSB*3 | 2005 |
| [5] | 0.25 SiGe | 27 | -35 | 2.7 | 3.1~4.5 | 3 | PLL*2+SSB | 2005 |
| [3] | 0.18 SiGe | 46 | N/A | 2.7 | 3.1~7.9 | 7 | PLL+SSB*2 | 2005 |
| [4] | 0.18 CMOS | 116.28 | -52 | 1.8 | 3.1~7.9 | 7 | PLL*2 | 2005 |
| [2] | 0.18 CMOS | 48 | -37 | 2.2 | 3.1~7.9 | 7 | PLL*2+SSB | 2006 |
| [6] | 0.09 CMOS | 47 | -20 | 1.1 | 3.4~9.2 | 12 | PLL+SSB*2 | 2006 |
| [14] | 0.18 CMOS | 76.5 | -24 | 1.8 | 3.1~10.3 | 14 | PLL+SSB*3 | 2006 |
| [10] | 0.18 CMOS | 90 | -35 | 1.8 | 3.1~10.3 | 14 | PLL*2+SSB*3 | 2006 |
| [11] | N/A | N/A | -24 | N/A | 3.1~10.3 | 14 | PLL*1+SSB*5 | 2007 |
| [13] | 0.18 CMOS | 59 | -22 | 1.5 | 3.1~7.9 | 9 | PLL*1+SSB*3 | 2007 |
| This work | 0.13 CMOS | 54.6 (without PLL) | -34 (with cancellation technique) -25 (without cancellation technique) | 1.2 | 3.1~10.3 | 14 | PLL*1+SSB*2 | 2007 |

Table 3.3 Performance comparison

# Chapter 4
# Layout and Implementations

## 4.1 Layout Considerations

The layout of the partial signal generator is shown in Figure 4.1 and Figure 4.2. In high frequency circuit design, the layout must be as symmetry as possible. Because the difference of the quadrature signal paths will cause the phase error. The coupling effect should also be concerned for layout because it will degrade the performance. The inductors in the layout are put a long distance away to avoid the coupling effect. And the large by-pass capacitors are inserted between the bias line and ground line to steady the bias voltage. The total chip area is 1000*1000 $um^2$.

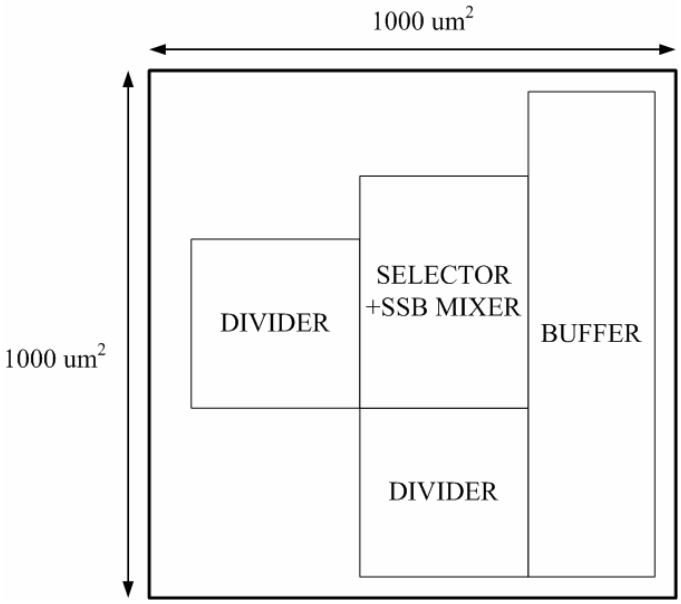



Figure 4.1 Floor-plan of the partial signal generator

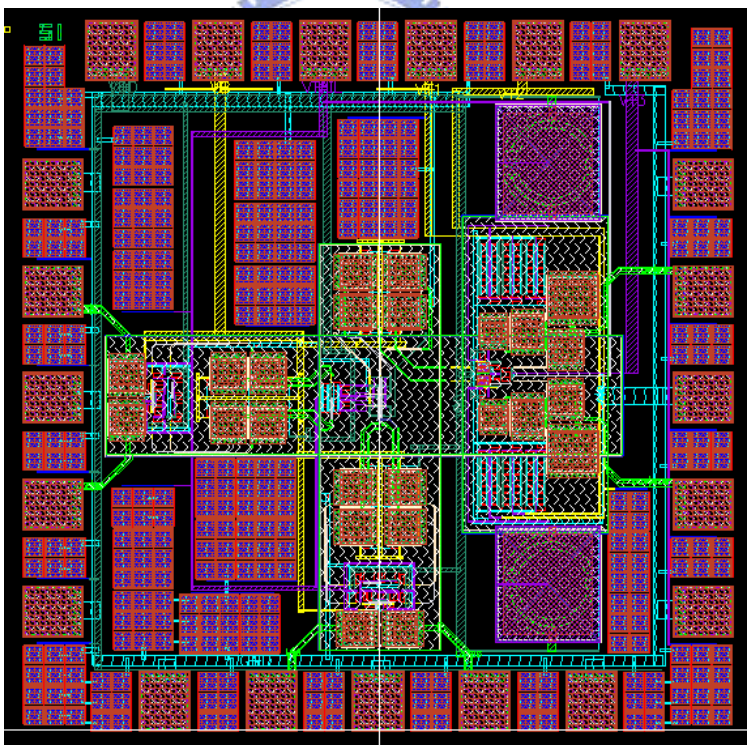


Figure 4.2 Layout of the partial signal generator

## 4.2 Simulation Results

The schematic of the signal generator is illustrated in Figure 4.3. The circuit includes two dividers, three bias buffers, a selector with dummy-pair, a passive mixer, and a LC buffer with tunable negative resistance. The input LO frequency is 8448-MHz, and the input RF frequencies are 1584-MHz, 2640-MHz, and 3696-MHz. The output frequencies are 5016-MHz, 5544-MHz, and 6072MHz. Because the single-sideband mixer needs the quadrature inputs, the dividers are used to generate quadrature signal for it. The post-layout simulation is in the Figure 4.4 to Figure 4.6 and the comparison with pre-simulation is in Table 4.1. The total power consumption is 18.816 mW.

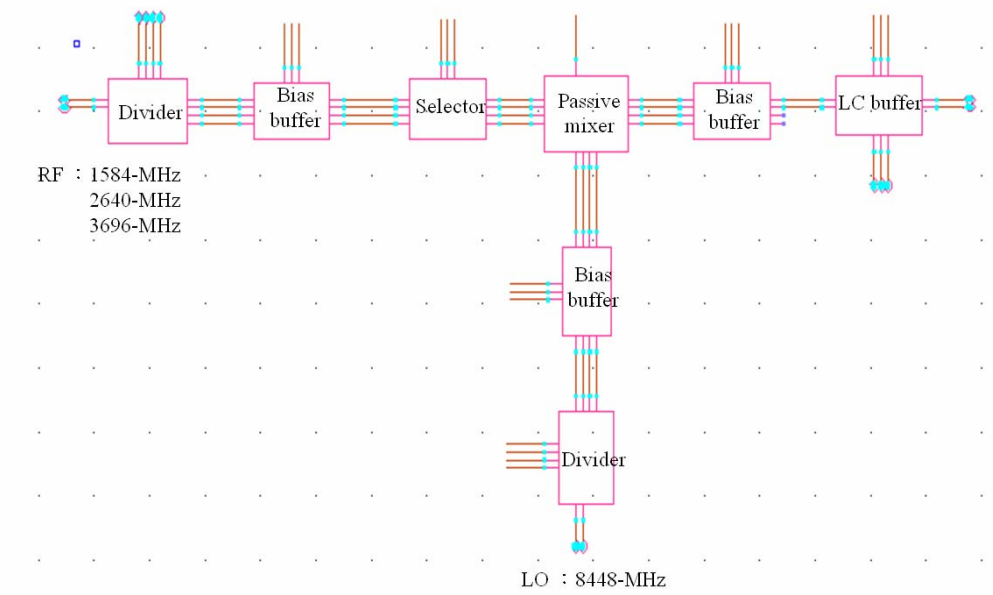



Figure 4.3 The schematic on RFDE

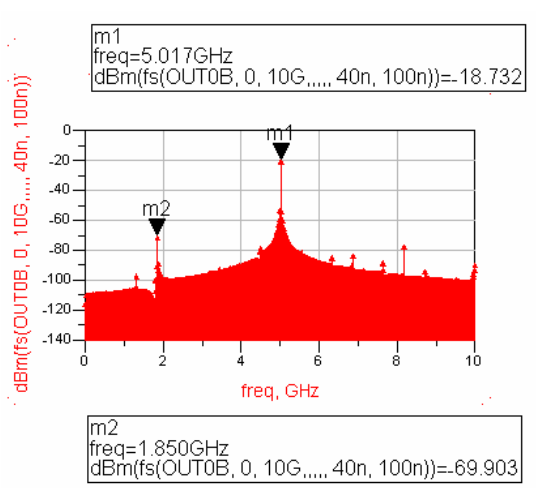



Figure 4.4 The output at 5016-MHz

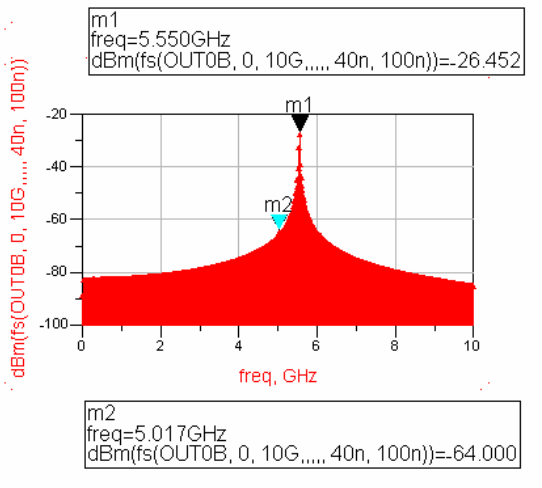



Figure 4.5 The output at 5544-MHz

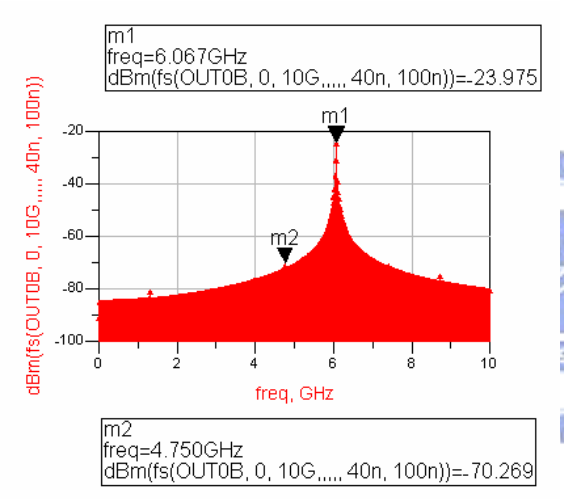



Figure 4.6 The output at 6072-MHz

| | Pre-simulation | | Po-simulation | |
|---|---|---|---|---|
| Band frequency (MHz) | Output power (dBm) | Spurs (dBc) | Output power (dBm) | Spurs (dBc) |
| 5016 | -17.62 | **-52.38** | -18.73 | **-51.2** |
| 5544 | -25 | **-35** | -26.45 | **-37.5** |
| 6072 | -22.66 | **-46** | -23.97 | **-46.3** |

Table 4.1 Comparison table

## 4.3 Measurement Plan

During the measurement of the implemented partial signal generator, three probes of GSGSG and a six-pin DC probe are needed. Before the measurement starts, the line loss should be considered at first. As Figure 4.7, The LO frequency and RF frequencies are generated from the ESGs. The broadband baluns are inserted between the probes and ESGs to obtain the differential signals. And there are six power supplies in use. The output probe is connect with the spectrum analyzer.

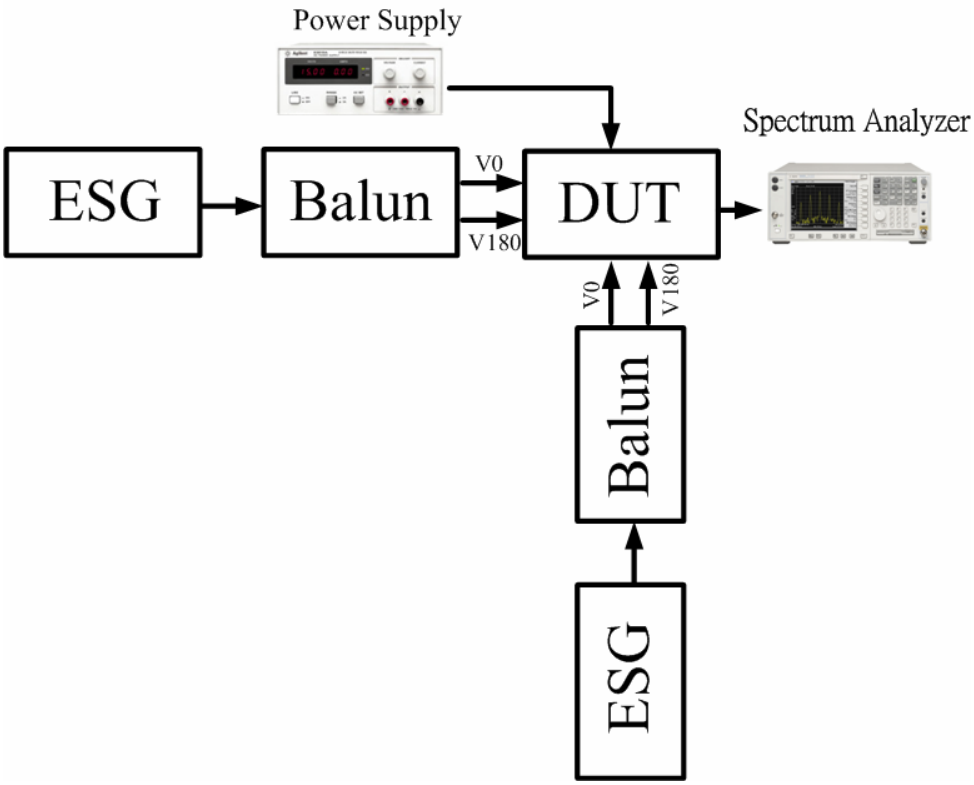



Figure 4.7 Measurement setup

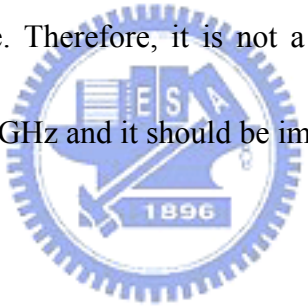
# Chapter 5
# Conclusions and Future Works

## 5.1 Conclusions

The wireless frequency synthesizer has been designed and implemented for ECMA UWB WPAN with single a frequency source being adopted by UMC 0.13-μm CMOS. And the specification of switching time is met by using the divide-by-two circuits and single-sideband mixers. The spurious are suppressed by using the divide-by-two circuit after the mixer, the selector with dummy pairs, and the LC tanks with the tunable negative resistance. The divide-by-two circuit is inserted between the mixer and the output LC buffer from 3.1-GHz to 6.3-GHz. Thus, the in-band spurious are suppressed. The out-band spurious are located at the twice frequencies of the desired frequencies. And it allows co-existence with WLAN applications operating in 2.5-GHz ISM and 5.2-GHz ISM.

## 5.2 Future Work

The spurious tones from the carrier frequency 6.3-GHz to 10.6-GHz must be improved. Even though the LC buffer is used before the output of the frequency synthesizer to suppress the spurious, the spurious tones are lower but still disappear around the carrier frequency. It is difficult to use the spurious suppressing technique of the divide-by-two circuit after the mixer in this frequency range. When the method is used in these carrier frequencies, the maximum frequency will be up to 20.6-GHz, and more unwanted high frequency effect issues must be concerned. The power consumption will also increase. Therefore, it is not a good approach to suppress the spurious from 6.3-GHz to 10.6-GHz and it should be improved by other techniques.



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# 簡　　歷

姓　名：黃昱瑞

性　別：男

籍　貫：台北市

生　日：西元 1982 年 03 月 18 日

地　址：新竹市光明新村 89 號

學　歷：國立交通大學電信研究所碩士班　　2005/09 ~ 2007/06

國立東華大學電機工程學系　　2000/09 ~ 2005/06

台北市私立延平高中　　1997/09 ~ 2000/06

論文題目：　Spurious Suppressing Design for UWB Synthesizers

應用於 UWB 頻率合成器之突波雜訊抑制設計