國 立 交 通 大 學

電信工程學系碩士班

碩 士 論 文

低功率、低電壓之超寬頻低雜訊放大器設計

Low-Power/Low-Voltage Low Noise Amplifiers for
Ultra-Wideband Radio Systems

研 究 生：李奕慶

指導教授：唐震寰　教授

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摘要

　　低雜訊放大器在無線通訊接收前端電路扮演一個重要的角色，負責放大接收天線後的微弱訊號並維持最小的雜訊為原則。功率消耗、寬頻輸入阻抗的匹配、雜訊指數和增益都是設計低雜訊放大器時的考量因子，然而這些考量因子之間彼此相互衝突所以必須適當的取捨。本篇論文設計超寬頻低雜訊放大器時提出結合共閘極放大器的架構和帶通濾波器的架構，不但達到降低功率消耗(電壓為1.5V，功率消耗僅為3mW)，也完成超寬頻的輸入阻抗匹配(3.1GHz-10.6 GHz)。同時也讓雜訊指數均低於4.5dB、最大增益為12.4dB。本篇論文也提出另一種設計超低電壓的低雜訊放大器電路，是利用在電晶體的基極端上外加上一個額外的偏壓電路來達到低功率消耗(低電壓為0.75V並且消耗功率為2.8mW)，也完成寬頻的輸入阻抗匹配(6GHz-10.6GHz)。同時也讓雜訊指數均低於3.8dB、最大增益為14.0dB。

Low-Power/Low-Voltage LNAs for Ultra-Wideband Radio Systems

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Abstract

Low noise amplifier (LNA) plays an important role in wireless communication receiver front-ends and is usually used for amplifying the weak signal after the receiving antenna with minimized noise contribution. Power consuming, broadband input impedance matching, noise figure, and power gain, are the major issues to be considered in LNA design. It is well-known that these issues are trade-offs one another. Here, two research topics are included in the thesis and the both focuses on low power consumption of UWB LNAs without sacrificing other important performances such as power gain and noise figure. The first topic propose the common gate combined with band pass filters for the input matching network can easily to low power consumption (1.5V power supply, and dissipates 3mW) and ultra-wideband (3GHz to 10.6GHz). It achieved 12.4dB maximum gain and noise figure less than 4.5dB. The second topic proposes very low voltage LNA, which uses an external bias circuit to the body node of transistor leads to low power consumption (0.75V power supply, and dissipates 2.8mW). It achieved 14.0dB maximum gain from 6 GHz to 10.0 GHz and noise figure less than 3.8dB.

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Chapter 1   *Introduction*

1.1   Background and Problems

Ultra-wideband (UWB) communication techniques have attracted great interests in both academia and industry in the past few years for applications in short-range and high-speed wireless mobile system. The Federal Communication Commission (FCC) has recently approved the 3.1GHz to 10.6GHz band for UWB deployment as shown in Figure 1.1. Due to the U-NII bands (5.15GHz-5.85GHz in the United States and 4.9GHz-5.1GHz in Japan (GROUP B)) to lie in the middle of the allocated spectrum, the UWB spectrum is broken into two distinct and orthogonal bands that are free from interference: 3.1GHz-4.8GHz and 6.0GHz-10.6GHz. We subsequently refer to these two bands as the lower and upper UWB bands, respectively.
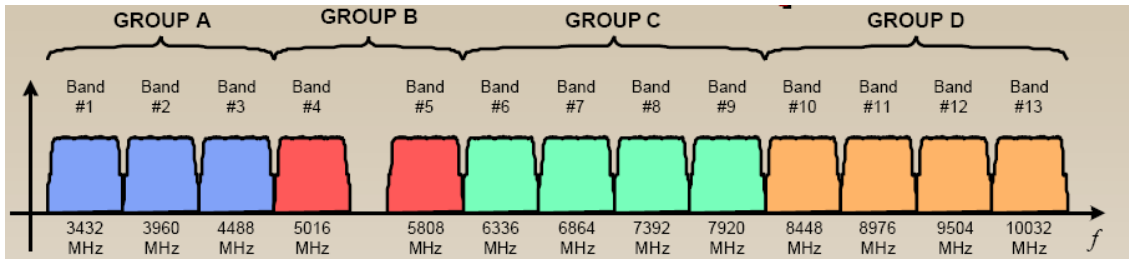
Figure 1.1 Multi-Band OFDM Proposal

A LNA is the first stage, after antenna in the receiver block of a communication system. It is widely used in the front end of narrow band communication system. For UWB applications, which ranges from 3.1GHz to 10.6GHz, because transmitted power spreads over a wide range and is restricted to be less than -41.3 dBm per MHz. There are several common goals in the design of UWB LNA including input impedance matching, low power consumption, low noise performance, small sizes, sufficient linearity, and enough power gain to overcome the noise of subsequent stages. The thesis starts with a deep analysis of the noise figure, wideband, and flatness gain problems, and reviews recently-published literatures thoroughly. After that, we try to find new ways of achieving these goals.

The thesis firstly proposes a new UWB LNA architecture, which incorporates a filter architecture and feedback resistor to enhance the bandwidth. The proposed LNA architecture covers from 3GHz to 11GHz, and shows low power consumption, and much better power gain flatness. Secondly, a novel low voltage design method is proposed for a common-source UWB LNA to attain very low power consumption.

1.2 Related Works

Three major CMOS UWB LNA design techniques had been reported for wideband

communication applications. The well-developed distributed amplifier is known as its wide bandwidth, but it requires large power consumption and layout area [8]. The filter design technique and source inductor degeneration technique are employed to incorporate the transistor gate-source capacitance as a part of the LC-ladder matching network and extend the bandwidth to a wide range [1], [7], [10], [13]-[17]. A common gate (or the 1/gm termination) amplifier has the highest potential to achieve the wideband input matching, good linearity, and input-output isolation, but it leads to lower gain and higher noise figure than using a common source amplifier [3]. Only a few literatures have reported on the design of a common gate LNA [3], [4], [5].

1.3   Thesis Organization

The thesis is organized into five chapters including the introduction. Chapter 2 deals with the receiver basics and basic concepts of low noise amplifier design, its metrics and some popular LNA topologies with their comparison. Chapter 3 proposes ultra-wideband LNA of proposed low power design with simulation results. In chapter 4, the noise analysis of the UWB LNA, and low voltage LNA design. In Chapter 5, conclusion is drawn.

Chapter 2 *Basic Concepts of Low Noise Amplifier Design*

2.1 System Specifications of the LNA

2.1.1 S-Parameters

Scatter Parameters, also called S-parameters, belong to the group to two-port parameters used in two port theory [47]-[50]. S-parameters are important in microwave design because they are easier to measure and to work with at high frequencies than other kinds of two-port parameters. The S-parameters are defined as:

$$\begin{pmatrix} |b_1|^2 \\ |b_2|^2 \end{pmatrix} = \begin{pmatrix} |S_{11}|^2 & |S_{12}|^2 \\ |S_{21}|^2 & |S_{22}|^2 \end{pmatrix} * \begin{pmatrix} |a_1|^2 \\ |a_2|^2 \end{pmatrix} \tag{2.1}$$

$|a_i|^2$: Power wave traveling towards the two-port gate

$|b_i|^2$: Power wave reflected back from the two-port gate

$|S_{11}|^2$: Power reflected from port 1

$\left|S_{12}\right|^2$: Power transmitted from port 1 to port 2

$\left|S_{21}\right|^2$: Power transmitted from port 2 to port 1

$\left|S_{22}\right|^2$: Power reflected from port 2

Since the two-port is imbedded in a characteristic impedance of Z_0, these 'waves' can be interpreted in terms of normalized voltage or current amplitudes. This is explained in Figure 2.1. In other words, we can convert the power towards the two-port into a normalized voltage amplitude of

$$a_i = \frac{V_{towards\_two-port}}{\sqrt{Z_0}} \qquad (2.2)$$

and the power away from the two-port can be interpreted in terms of voltages like

$$b_i = \frac{V_{away\_from\_two-port}}{\sqrt{Z_0}} \qquad (2.3)$$
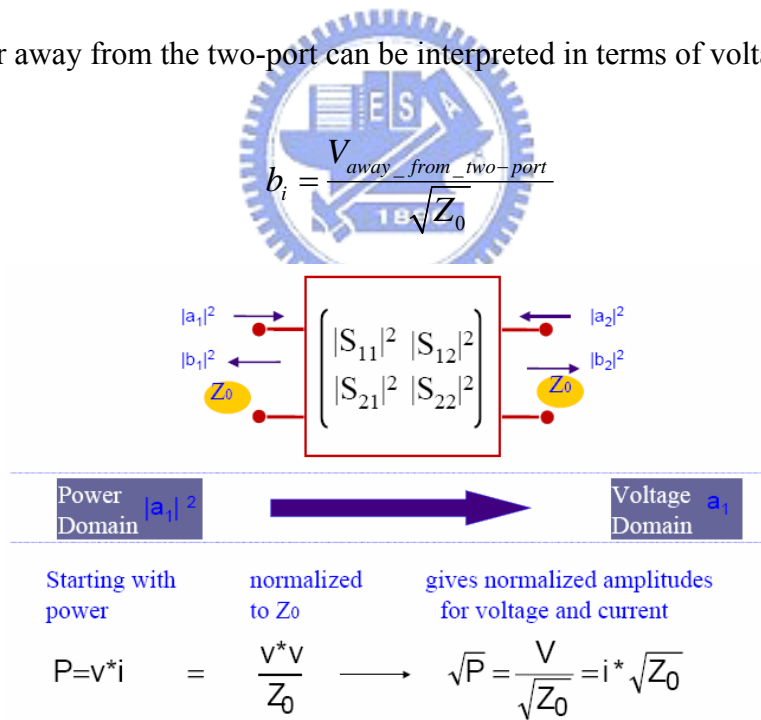
Figure 2.1 S-Parameters and Characteristic Impedance Z_0

The following signal flow graph gives the situation for the S-parameter interpretation in voltage as shown in Figure 2.2.
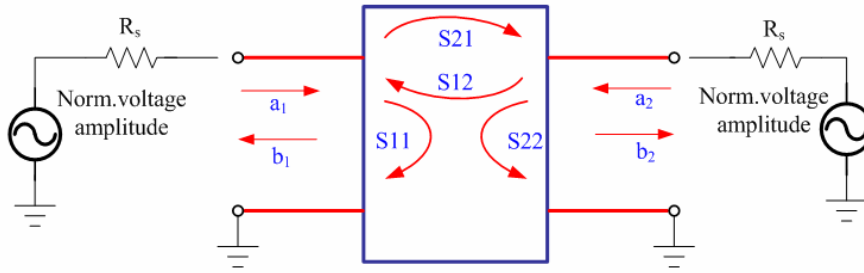
Figure 2.2 The following signal flow graph

Looking at the S-parameter coefficients individually, we have:

$$S_{11} = \frac{b_1}{a_1} = \frac{V_{reflected\_at\_port1}}{V_{towards\_port1}}\Big|a_2 = 0 \tag{2.4}$$

$$S_{12} = \frac{b_1}{a_2} = \frac{V_{out\_of\_port1}}{V_{towards\_port2}}\Big|a_1 = 0 \tag{2.5}$$

$$S_{21} = \frac{b_2}{a_1} = \frac{V_{out\_of\_port2}}{V_{towards\_port1}}\Big|a_2 = 0 \tag{2.6}$$

$$S_{22} = \frac{b_2}{a_2} = \frac{V_{reflected\_at\_port2}}{V_{towards\_port2}}\Big|a_1 = 0 \tag{2.7}$$

2.1.2 Power Gain

In this section we develop several expressions for the power gain of a general two-port amplifier circuit in terms of the S-parameters of the amplifier.

Definitions of Two-Port Gains:

Consider an arbitrary two-port network [S] connected to source and load impedances Z_s and Z_L, respectively, as shown in Figure 2.3. We will derive expressions for three types of power gain in terms of the S parameters of the two-port network and the reflection coefficients, Γ_S and Γ_L of the source and load [47]-[50].
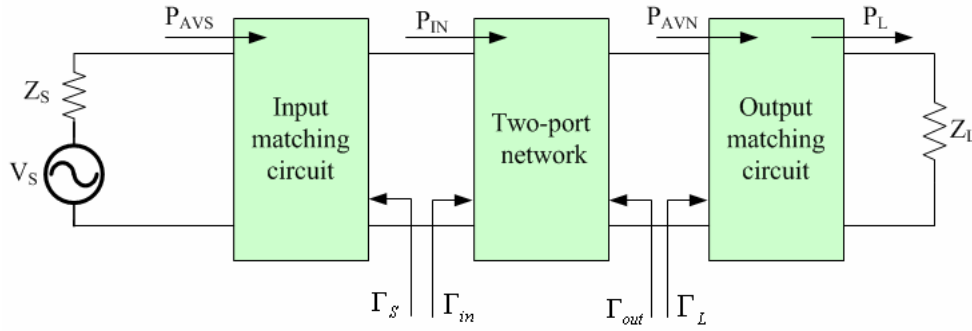
Figure 2.3 A two-port network with general source and load impedance

- Power Gain = G = P_L/P_{in} is the ratio of power dissipated in the load Z_L to the power delivered to input of the two-port network. This power gain is independent of Z_S, although some active circuits are strongly dependent on Z_S.

$$G = \frac{P_L}{P_{in}} = \frac{|S_{21}|^2 \left(1 - |\Gamma_L|^2\right)}{\left(1 - |\Gamma_{in}|^2\right)|1 - S_{22}\Gamma_L|^2} \tag{2.8}$$

- Available Gain = G_A = P_{AVN}/P_{AVS} is the ratio of the power available from the two port network to the power available from the source. This assumes conjugate matching of the both the source and the load, and depends on Z_S but not Z_L.

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{|S_{21}|^2 \left(1 - |\Gamma_S|^2\right)}{\left(1 - |\Gamma_{out}|^2\right)|1 - S_{11}\Gamma_L|^2} \tag{2.9}$$

- Transducer Power Gain = G_T = P_L/P_{AVS} is the ratio of the power delivered to the load to the power available from the source. This depends on both Z_S and Z_L .

$$G_T = \frac{P_L}{P_{AVS}} = \frac{|S_{21}|^2 \left(1 - |\Gamma_L|^2\right)\left(1 - |\Gamma_S|^2\right)}{|1 - \Gamma_S\Gamma_{in}|^2 |1 - S_{22}\Gamma_L|^2} \tag{2.10}$$

A special case of the transducer power gain occurs when both the input and output are matched foe zero reflection. Then $\Gamma_S = \Gamma_L = 0$, and equation (2.10) can given

by:
$$G_T = \left| S_{21} \right|^2 \qquad (2.11)$$

Where

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \qquad (2.12)$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \qquad (2.13)$$

Γ_S, Γ_L are the designed input and output matching points, respectively.

2.1.3 Noise Figure (NF) of LNA

In Figure 2.4, we can indicate the input signal by drawing a simple diagram as follows: If low noise amplifier has smaller noise figure, the output signal has a little distortion. Oppositely, low noise amplifier has larger noise figure, the output signal has a great deal distortion. Two methods for analyzing the effect of noise in electronic devices and LNA circuits [49] are illustrate in Appendix A.
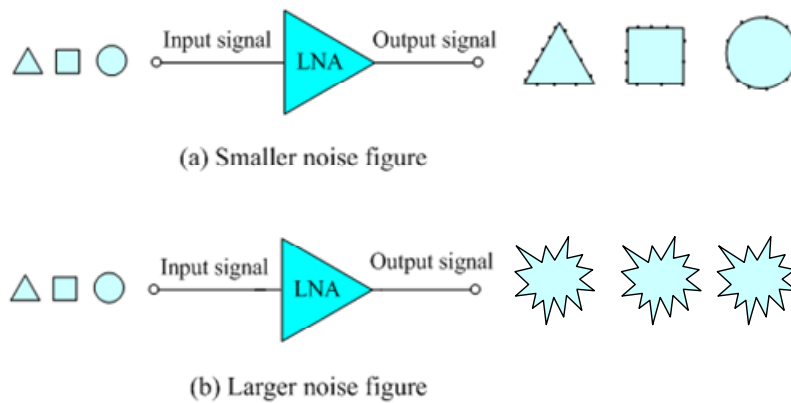
Figure 2.4 (a) Signal versus smaller noise figure, and (b) signal versus larger noise figure

2.1.4   Sensitivity

In wireless communication systems, the definition of sensitivity is limited by noise figure. The sensitivity of RF front end receiver is defined as the minimum signal level that the system can detect with acceptable signal-to-noise ratio [48]. Sensitivity determines the maximum distance that a receiver can be away from the transmitter or the base station for a mobile phone case. Its can be specified in the unit of dBm (decibels relative to one milli-watt) along with the reference impedance (50Ohm for most systems) and is typically measured in the interference-free environment. Usually, the minimal detect signal power can be written as

$$P_{in,\ min}\big/_{dBm} = P_{rs}\big/_{dBm/Hz} + NF\big/_{dB} + SNR_{min}\big/_{dBm} + 10\log B , \quad (2.14)$$

where NF is the noise figure of the receiver system, B is the signal channel bandwidth, SNR_{min} is the minimal acceptable signal-to-noise ratio. Assuming conjugate matching at the output, we can obtain P_{rs} as the noise power that source resistance delivers to the receiver.

$$P_{rs} = \frac{4kTR_s}{4}\frac{1}{R_{in}} = kT = -174\,dBm/Hz\,(R_s = R_{in}) \quad (2.15)$$

Assuming equation (2.47) at room temperature, its can be written as

$$P_{in,\ min}\big/_{dBm} = -174\,dBm/Hz + NF + 10\log B + SNR_{min} \quad (2.16)$$

2.1.5   Harmonics

The input-output relationship of a nonlinear system:

$$y(t) = \alpha_1 s(t) + \alpha_2 s(t)^2 + \alpha_3 s(t)^3 \quad (2.17)$$

Here s(t) is the input signal, y(t) is the output signal, and the nonlinearity, distortion is

generated. Using the input-output relationship (2.17) with a signal tone at the input $s(t)=A\cos\omega_0 t$, the output of the nonlinear systems can be viewed mathematically as

$$y(t) = \alpha_1 A \cos \omega_0 t + \alpha_2 A^2 \cos^2 \omega_0 t + \alpha_3 A^3 \cos^3 \omega_0 t$$

$$= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4} \right) \cos \omega_0 t + \frac{\alpha_2 A^2}{2} \cos 2\omega_0 t + \frac{\alpha_3 A^3}{4} \cos 3\omega_0 t \quad (2.18)$$

Harmonic distortion is defined as the ratio of the amplitude of a particular harmonic to the amplitude of the fundamental. For example, third-order harmonic distortion (HD3)is defined as the ratio of amplitude of the tone at $3\omega_0$ to the amplitude of the fundamental at ω_0 applying this definition to (2.18), we have

$$HD_3 = \frac{1}{4} \frac{\alpha_3}{\alpha_1} A^2 \quad (2.19)$$

Next, we take the Fourier transform of (2.18):

$$Y(\omega) = \alpha_2 A^2 \pi \delta(\omega) + \pi \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4} \right) [\delta(\omega - \omega_0) + \delta(\omega + \omega_0)]$$

$$+ \pi \frac{\alpha_2 A^2}{2} [\delta(\omega - 2\omega_0) + \delta(\omega + 2\omega_0)] \quad (2.20)$$

$$+ \pi \frac{\alpha_3 A^3}{4} [\delta(\omega - 3\omega_0) + \delta(\omega + 3\omega_0)]$$

Equation (2.20) is plotted in Figure 2.5.
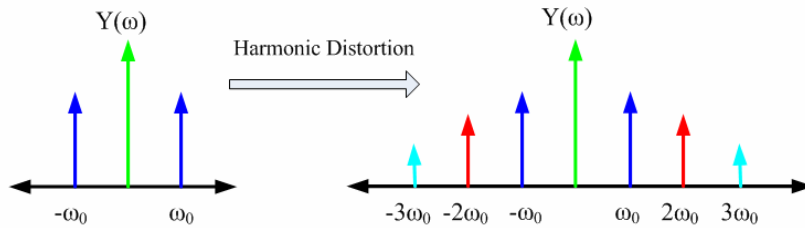
Figure 2.5 Frequency spectrum of input, output of the nonlinear system

2.1.6 Inter-Modulation

Inter-modulation arises when more than one tone is present at the input. Assume that

two strong interferers occur at the input of the receiver, specified by s(t)= $A_1\cos\omega_1 t$ + $A_2\cos\omega_2 t$. The inter-modulation distortion can be expressed mathematically by applying s(t) to (2.17):

$$y(t) = \alpha_1 \left(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \right) + \alpha_2 \left(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \right)^2 \\ + \alpha_3 \left(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \right)^3 \tag{2.21}$$

Using trigonometric manipulations, we can find expressions for the second and the third-order inter-modulation products as follows:

$$\omega_1 \pm \omega_2 : \alpha_2 A_1 A_2 \cos \left(\omega_1 + \omega_2 \right) t + \alpha_2 A_1 A_2 \cos \left(\omega_1 - \omega_2 \right) t;$$

$$2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4} \cos \left(2\omega_1 + \omega_2 \right) t + \frac{3\alpha_3 A_1^2 A_2}{4} \cos \left(2\omega_1 - \omega_2 \right) t;$$

$$2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_2^2 A_1}{4} \cos \left(2\omega_2 + \omega_1 \right) t + \frac{3\alpha_3 A_2^2 A_1}{4} \cos \left(2\omega_2 - \omega_1 \right) t. \tag{2.22}$$

The third-order inter-modulation products at $2\omega_2-\omega_1$, $2\omega_1-\omega_2$ and a nonlinear system (ex: LNA, PA..), the output signal will be corrupted are illustrated in Figure.2.6.
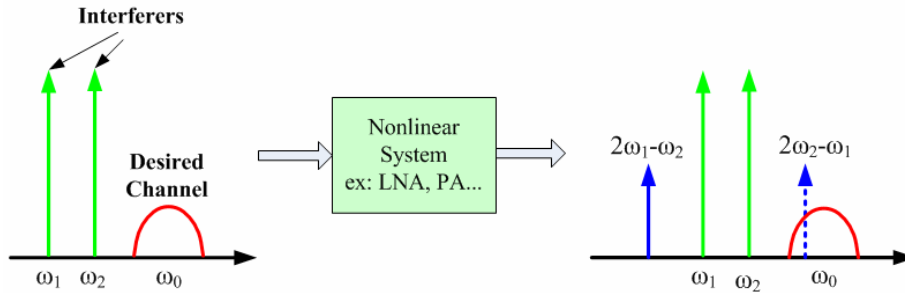
Figure 2.6 Inter-modulation in a nonlinear system

The output spectrum in the frequency domain can be determined from (2.22) by evaluating its Fourier transform $Y(\omega)$. This is shown in Figure 2.9, where the following signals: ω_0: desired signal, ω_1, ω_2: strong interferers, $2\omega_1$, $2\omega_2$: harmonics of the interferers, $\omega_1 \pm \omega_2$: second order inter-modulations products, $2\omega_{1,2} \pm \omega_{2,1}$: Third order inter-modulation products. It can be seen from Figure 2.7 that the inter-modulation product with frequency $2\omega_2-\omega_1$ lies at ω_0 and corrupts the desire signal at ω_0.

Furthermore, ω_1, ω_2 are close to ω_0 ; therefore, trying to filter them out requires a filter bandwidth that is very narrow and is impractical. Keeping down $2\omega_2$-ω_1 by keeping the nonlinearity small is the only solution.
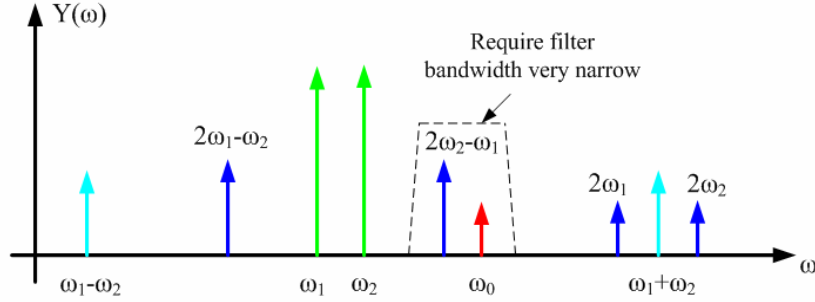
Figure 2.7 The effect of the inter-modulation distortion in the frequency domain

2.1.7 Third Order Harmonics Intercept Point (IP3)

From (2.21), we note that as the input level A increase, the desired signal at the output is proportional to A (by the small signal gain α_1). On the other hand, from (2.22) we can see that the third-order product increases in proportion to A^3. This is plotted on a linear scale in Figure 2.8 (a). Figure 2.8 (a) is re-plotted on a logarithmic scale in Figure 2.8 (b), where power level is used instead of amplitude level. As shown in Figure 2.10 (b), the third-order intercept point IP3 is defined to be the intersection of the two lines.

From Figure 2.8 (b), we can see that the amplitude of the input interferer at the third-order intercept point, A_{IP3}, is defined by the relation

$$20\log\left(\alpha_1 A_{IP3}\right) = 20\log\left(\frac{3\alpha_3}{4}A_{IP3}^3\right) \tag{2.23}$$

From (2.23), we can solve for A_{IP3}:

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.24}$$

For a 50Ω load, we define the input third-order intercept point (IIP3) as IIP3=

$A^2_{\text{IP3}}/50\Omega$.(IIP3 is hence interpreted as the power level of the input interferer for a 50Ω load at the third-order intercept point).
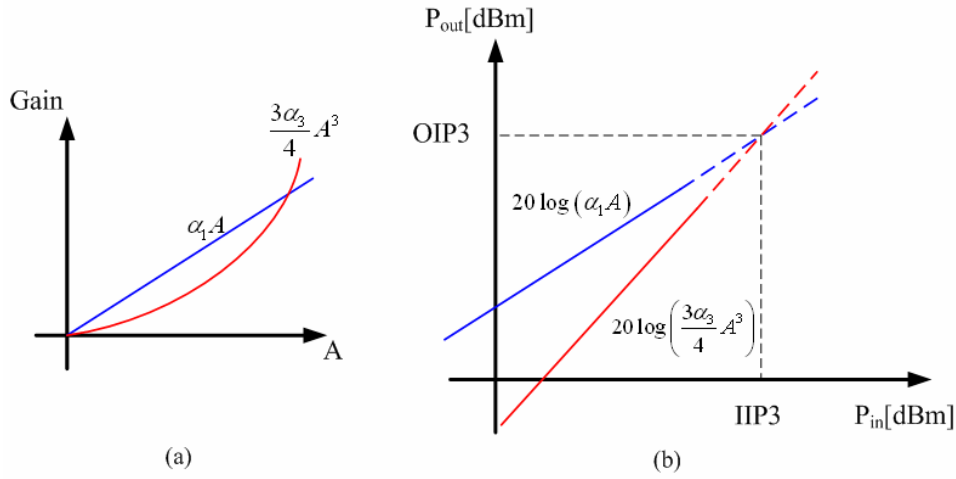
Figure 2.8 (a) The linear gain ($\alpha_1 A$) and the nonlinear component ($3\alpha_3 A^3 /4$); (b) The input and output third order intercept point (IIP3, OIP3)

2.1.8 1-dB Gain Compression Point (P1dB)

When the input signal to an amplifier is large, the amplifier will be saturates, hence clipping the signal. When the strength of the input signal is further increased, the output signal is no longer amplified. At this point, the output is said to be compressed. From (2.17), we observe that in y(t) there are two terms with frequency ω_0 due to the nonlinear behavior. Assume that the other terms in y(t) have frequency outside the band of interest and hence are removed by the BPFs. Thus, y(t) becomes

$$y(t) = \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4} \right)\cos\omega_0 t = \left(\alpha_1 + \frac{3\alpha_3 A^2}{4} \right)A\cos\omega_0 t \qquad (2.25)$$

In the case where α_3 is negative, the second term is decreasing the gain. As the input starts to increase, the impact of the second term becomes important in the sense that it saturates the active device. The $A_{1\text{-dB}}$ specifies the amplitude (in voltage) of the input

signal when the linear voltage gain drops by 1dB. Form (2.25), we see that the 1-dB compression point can be expressed mathematically by

$$\left(\alpha_1 + \frac{3\alpha_3 A_{1-dB}^2}{4}\right)\Big|_{dB} = \alpha_1\big|_{dB} - 1dB \tag{2.26}$$

We can rewrite (2.26) in terms of decibels:

$$20\log\left|\alpha_1 + \frac{3\alpha_3 A_{1-dB}^2}{4}\right| = 20\log|\alpha_1| - 20\log 1.122 = 20\log\left|\frac{\alpha_1}{1.122}\right| \tag{2.27}$$

From (2.27), the $A_{1\text{-dB}}$ input level is given by

$$A_{1-dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.28}$$

The ideal of the 1dB compression point is shown graphically in Figure 2.9. In
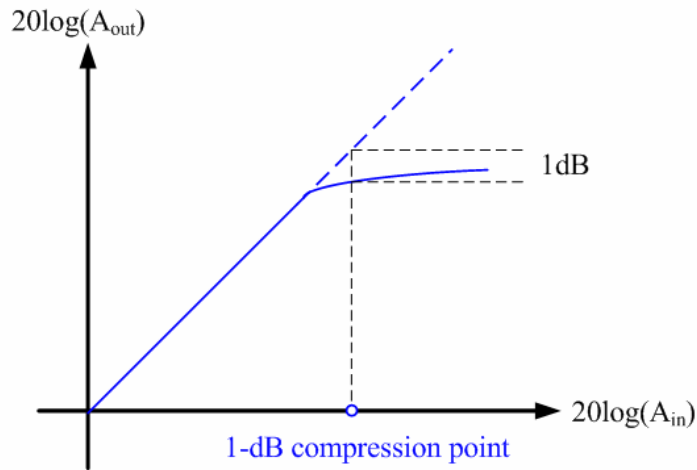
Figure 2.9 Illustration of the 1-dB compression point

Figure 2.10 illustrates that when input signal is -20dBm, gain is 10dB, and P_{1dB} is 0dBm, the output signal will be -20dBm+10=-10dBm. Due to output signal < P_{1dB}= 0dBm, so the output signal will not distortion. Oppositely, if input signal is -5dBm, the output signal will be -5dBm+10=+5dBm. But the output signal over the P_{1dB}= 0dBm, so

the output signal will distortion. In Figure 2.11 illustrates that P1dB large when input

signal is -20dBm or -5dBm, the output signal will not distortion.
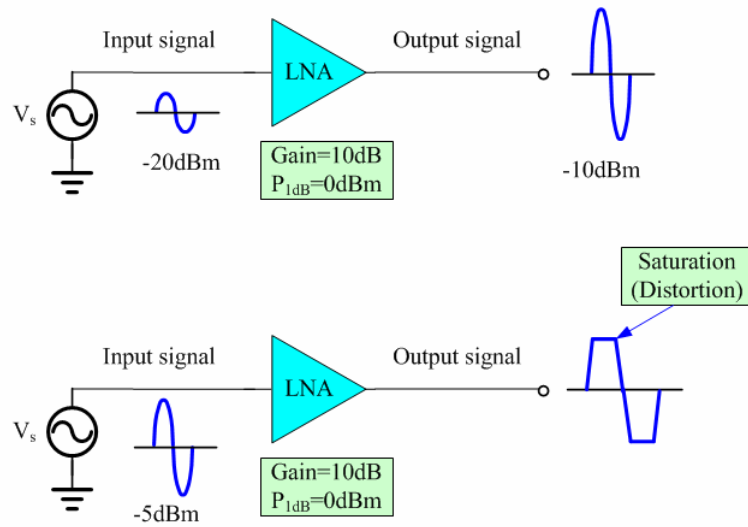
Figure 2.10 Illustration of the P1dB small
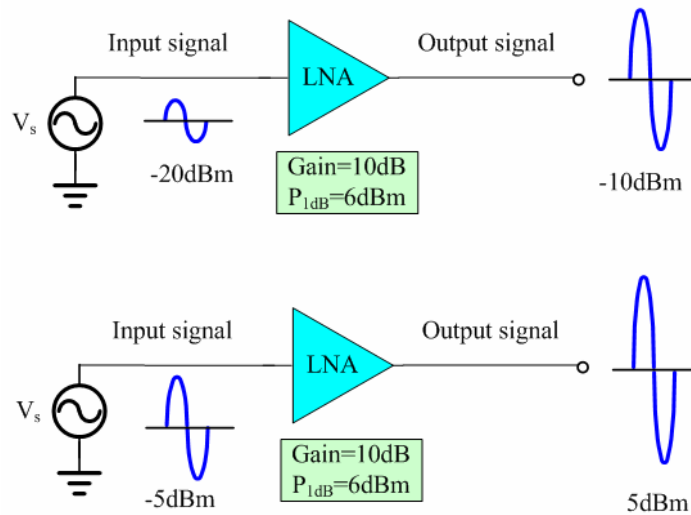
Figure 2.11 Illustration of the P1dB large

2.2 Conventional LNA input matching Architecture

Low noise amplifier is the first stage in the receiver front-end circuits and is used to

amplify the received weak RF signal with the minimum noise figure. Between the wideband input matching and the noise figure of the UWB LNA should be carefully studied and decide. Impedance matching is very important in LNA designs. There are four basic 50Ohm input matching architectures that have been explored in the traditional transistor-amplifier shown in Figure 2.12. In this section, we will investigate a number of circuit architecture that can be used of the task and discussed.

(a) Resistive termination   (b) 1/gm termination   (c) Shunt-series feedback   (d) Inductive degeneration
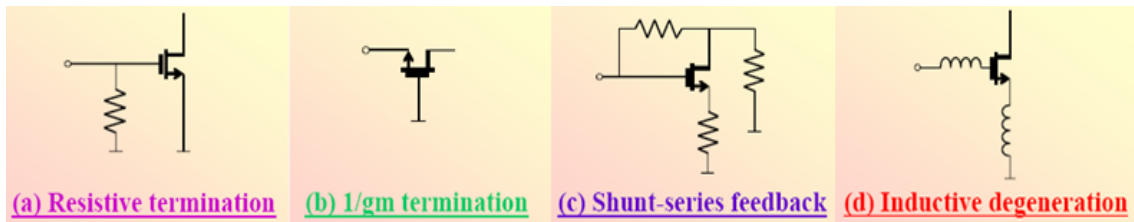
Figure 2.12 Traditional transistor-amplifier of input matching

a. Resistive Termination architecture

Resistive termination architecture is the most straightforward approach to achieve the wideband 50Ohm matching at the input as shown in Figure 2.13. The 50Ohm resistor (R) is placed across the input terminal of the LNA and hence providing a wideband matching.
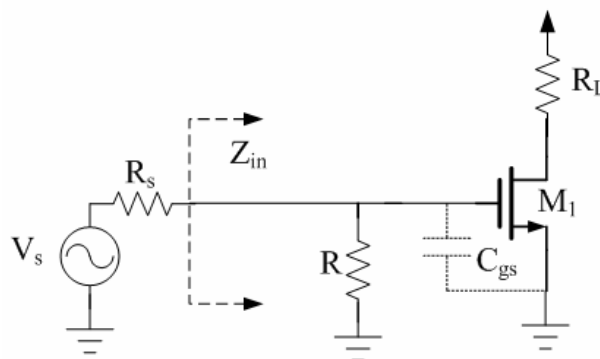
Figure 2.13 Resistive termination matching technique

The bandwidth of this matching technique is determined by the input capacitance of the transistor M_1 and can be very high. However, the resistor R adds into circuit will

good input matching, but leads to high thermal noise in circuit. If ignoring all the noises from the transistors, the lower bound of the noise factor is equal to 2. Hence, the resistor termination technique is not practical in most application.

b. Common Gate input architecture (1/gm termination)

The last input matching method is to use a common-gate architecture as shown in Figure 2.16. [3], [4], [12]. A common gate (or the 1/gm termination) architecture has the highest potential to achieve the wideband input matching, good linearity, and input-output isolation, but it leads to lower gain and higher noise figure than using the other mentioned techniques. Using the common gate architecture has the lower bound noise factor is $F \approx 1 + \dfrac{\gamma}{\alpha} \geq 2.2$. (i.e Long channel F=2.2, Short channel F=4.7～6).
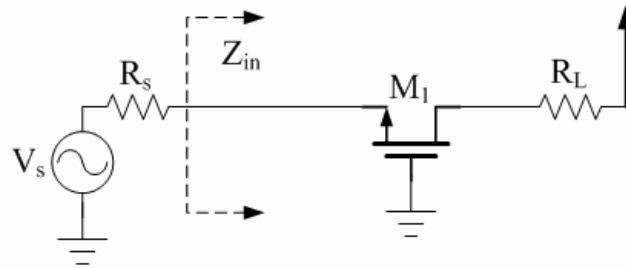
Figure 2.14 Common gate input matching technique

c. Shunt-Series resistor feedback architecture

The resistor feedback technique is used for getting a good input matching architecture as shown in Figure 2.15 [9], [14], [21], [22], [23], [25]. This technique unlike resistive termination case, it does not attenuate the signal by a noisy attenuator before reaching the gate of amplifying device and hence the noise figure is expected to be much higher. However, the feedback resistor (R_F) continues to generate thermal noise if its own.
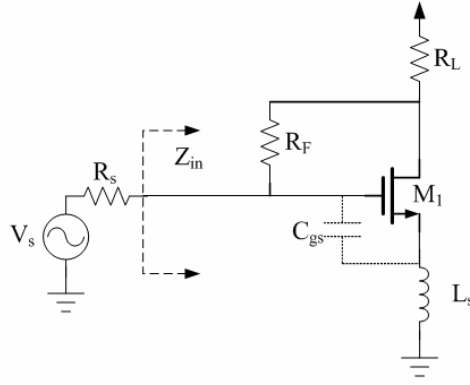
Figure 2.15 Shunt series resistor feedback matching technique

d. Inductive Source Degeneration architecture

The inductive source degeneration architecture is popular with input matching technique of LNA. [1], [5]-[7], [10], [13]-[18], [24], [26]-[30]. This matching technique provides a perfect matching without adding any noise to the system or giving any restrictions on the device g_m. It uses an inductor as a source degeneration device and has another inductor connecting to the gate as shown in Figure 2.16.
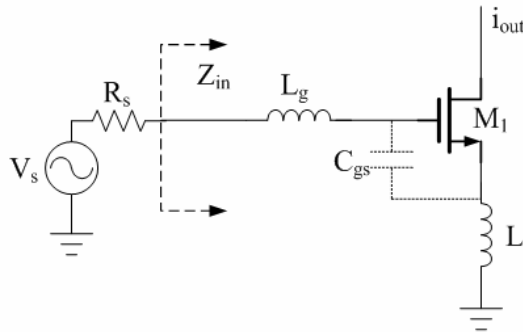
Figure 2.16 Inductive source degeneration matching technique

Using the small signal analysis and neglecting C_{gd} of transistor M_1, the impedance looking through the gate inductor can be written as:

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \omega_T L_s \qquad (2.29)$$
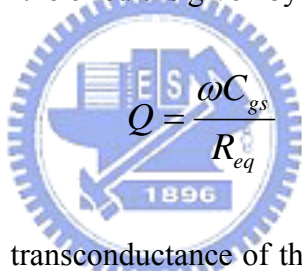
Where
$$\omega_T = \frac{g_m}{C_{gs}} \tag{2.30}$$

At the resonance frequency where the inductor impedance and capacitor impedance are canceled out, the input impedance is then just the last term in the equation (2.29). The tuned impedance is given by:

$$Z_{in}(\omega_0) = R_{eq} = \omega_T L_s \tag{2.31}$$

Where
$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{2.32}$$

In Figure 2.17 shows the equivalent model of the inductive source degeneration architecture, the quality factor of the circuit is given by:

$$Q = \frac{\omega C_{gs}}{R_{eq}} \tag{2.33}$$

The effectively increase the transconductance of the input transistor by a factor can written as $G_m = Qg_m$. In typical narrow band matching, the quality factor is usually around 3-5. Assuming that the matching network is lossless, helps to reduce the input-referred added noise by a factor of Q as well as increasing the voltage gain of the circuit by the same factor.
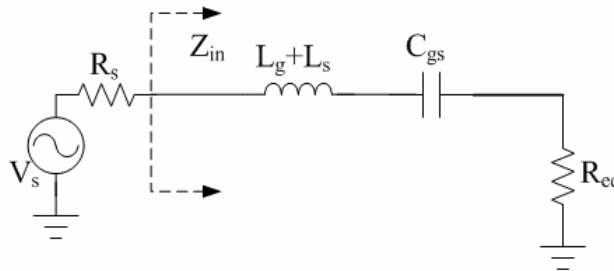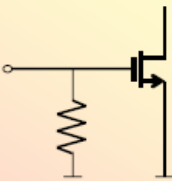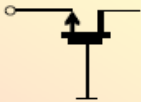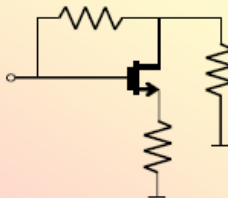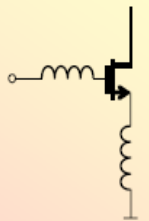
Figure 2.17 Equivalent circuit of inductive source degeneration matching

e. LNA design and comparison of input matching architecture

In general, the following should be considered in LNA design:

a. Input and Output matching (return loss): In wireless receiver, the component placed before LNA is usually the filter and antenna with characteristic impedance 50Ω, so input impedance matching of LNA must be matching to close to 50Ω. But, the input impedance matching is always different from the optimum noise matching.

b. Low Noise Figure (NF): The low noise figure of the LNA is dominates all noise figure of the entire receiver system. Thus, noise figure of LNA is the most important parameters to evaluate the performance. The low noise figure and low power dissipation are well-known that two issues are trade-offs one another.

c. Sufficient power gain: The sufficient power gain of the LNA is important, because it amplify the receiver RF signal and reduce the noise contribution from the following stages. But, the larger power gain will degrade the linearity of LNA.

d. Low power dissipation: Design a wide band low noise amplifier, the low power issue is important, but it trade off with noise figure and power gain.

Table 2.1 Comparison of LNA input matching architecture

Input matching architecture of LNA	Advantage	Drawback
(a) Resistive termination	Good wideband input matching. Good power gain. Good linearity.	Higher thermal noise.
(b) 1/gm termination	Good wideband input matching. Good linearity. Good reverse isolation. Low power dissipation.	Lower power gain. Higher noise figure.
(c) Shunt-series feedback	Good wideband input matching. Good power gain	High power dissipation. Poor reverse isolation. Feedback resistor generate thermal noise.
(d) Inductive degeneration	Good narrow band input-matching. Best noise performance. Good power gain. Good linearity.	Large area.

2.3 Methods to Reduce Noise Figure of LNA

Due to the various requirements of low noise amplifiers, the low noise characteristic. There are several methods to reduce the noise figure were proposed [6], [14], [31], [34].

2.3.1 External gate-source capacitor method

Since the induced gate current noise grows with the gate-source capacitance (C_{gs}), the addition gate-source capacitor (C_E) can reduce the noise figure from the induced gate current noise by reducing C_{gs}. The input stage of LNA with an external capacitor (C_E) is shown in Figure 2.18.
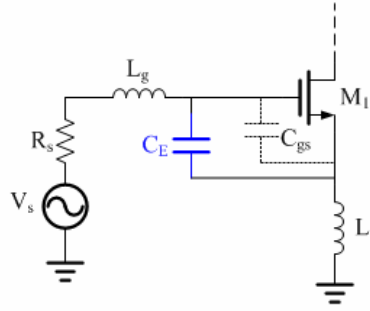
Figure 2.18 LNA with an external capacitor (C_E)

The input impedance of circuit in Figure 2.20 can be given by:

$$Z_{in} = s(L_g + L_s) + \frac{1}{s(C_E + C_{gs})} + \frac{g_m L_s}{C_E + C_{gs}} \tag{2.34}$$

The quality factor Q of the input circuit is:

$$Q = \frac{1}{(R_s + \frac{g_m L_s}{C_E + C_{gs}})\omega_0(C_E + C_{gs})} = \frac{1}{2R_s\omega_0(C_E + C_{gs})} \tag{2.35}$$

The noise figure can be derived as [1]

$$F = 1 + \frac{\beta(Q^2 + \frac{1}{4})(\frac{C_{gs}}{C_E + C_{gs}})^2 \frac{g_m^2}{g_{dn}} + \frac{\gamma}{4}g_{dn} + \sqrt{\frac{\beta\gamma}{4}}c\frac{C_{gs}g_m}{C_E + C_{gs}} + \frac{1}{R_{out}}}{R_s Q^2 g_m^2} \tag{2.36}$$

From equation (2.36), the value of Q from C_{gs} allows for an adjustable Q for any given C_{gs} to reduce the noise figure [1].

2.3.2 Thermal noise canceling method

Figure 2.19 illustrates that a thermal noise canceling method with straightforward implementation using an ideal feed-forward voltage amplifier A with a gain $-A_v$ (with $A_v > 0$) [6].
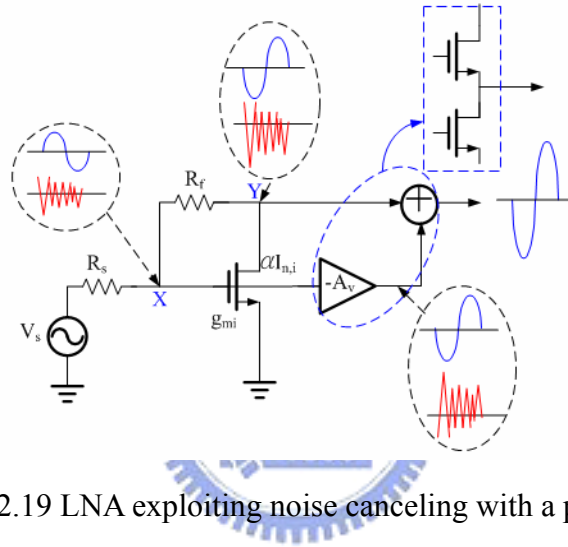
Figure 2.19 LNA exploiting noise canceling with a plus adder

By circuit inspection, the matching device noise voltages at node X and Y are

$$
\begin{aligned}
V_{X,n,i} &= \alpha(R_s, g_{mi})I_{n,i}R_s \\
V_{Y,n,i} &= \alpha(R_s, g_{mi})I_{n,i}(R_s + R)
\end{aligned}
\tag{2.37}
$$

The output noise voltage due to the noise of the matching device, $V_{out,n,i}$ is then equal to

$$
\begin{aligned}
V_{out,n,i} &= V_{Y,n,i} - V_{X,n,i} \cdot A_V \\
&= \alpha(R_s, g_{mi})I_{n,i}(R_s + R - A_V R_s)
\end{aligned}
\tag{2.38}
$$

Output noise cancellation, $V_{out,n,i} = 0$, is achieved for a gain A_V equal to

$$
A_V = \frac{V_{Y,n,i}}{V_{X,n,i}} = 1 + \frac{R}{R_s}
\tag{2.39}
$$

2.3.3 Gate-drain overlap capacitance neutralization method

The feedback from the gate-drain overlap capacitance (C_{gd}) can not be ignored in the high frequency, which leads to input matching and gain degradation. To reduce the feedback effect is by using cascade architecture, which leads to low voltage technique. The inductor-tuned technique can be implemented as shown in Figure 2.20.
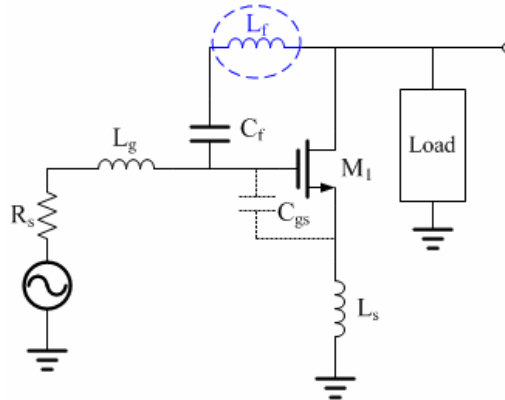
Figure 2.20 LNA with gate-drain overlap capacitance

It may not be suitable for on-chip implementations because the required inductance to resonant the C_{gd} is quite large for on-chip integration.

2.3.4 Quality factor (Q) of inductor enhancement method

Integrated high-Q inductors can improve the performance and integration-level of RFIC's while reducing their power dissipation and cost. Poor quality factors of on-chip matching inductors are affects the noise at high frequency. A new implementation of high quality factor (Q) copper inductor on CMOS silicon substrate using a fully process is presented. The Q factor of such inductors depends upon the conductivity of metal layer and other parasitic components. Planner spirals can be of different shapes i.e. square, hexagonal, octagonal and circular as shown in Figure 2.21.
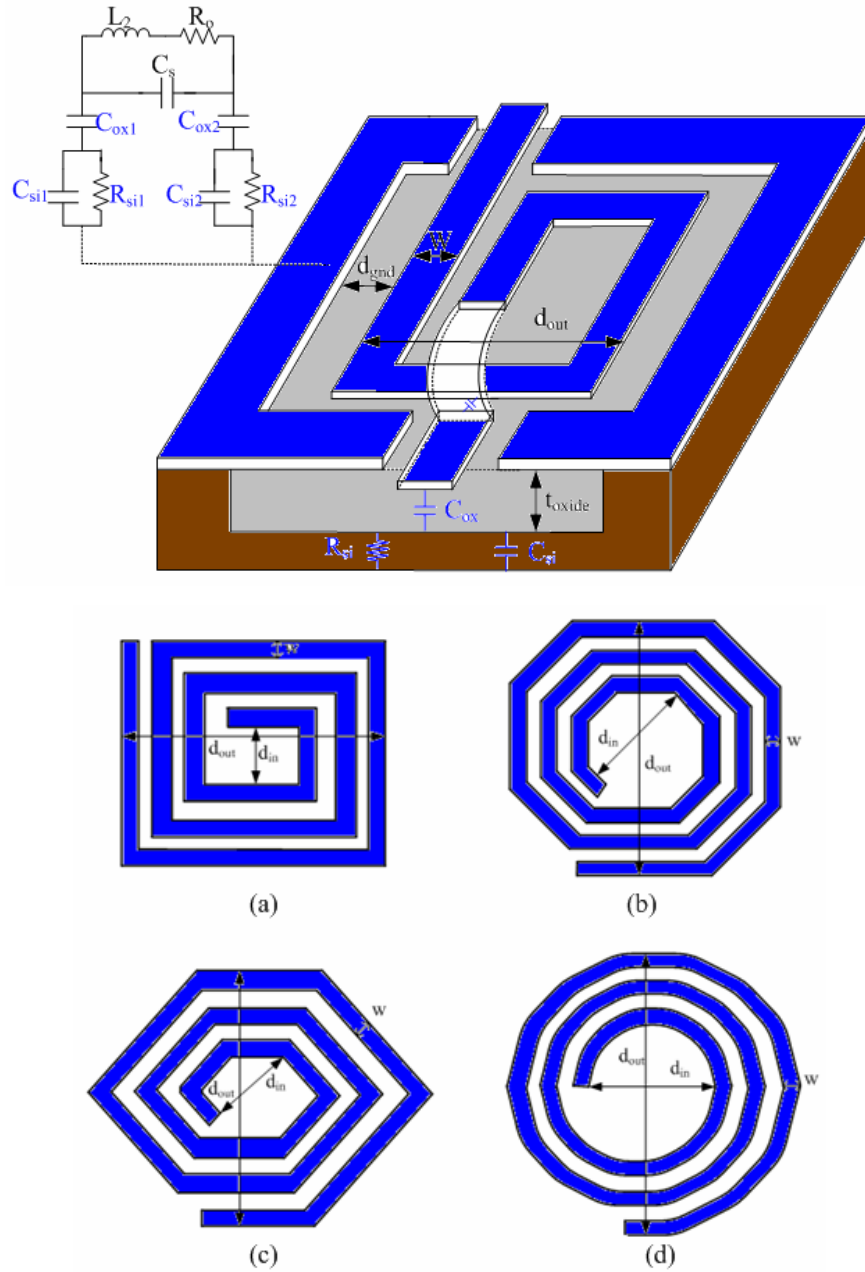
Figure 2.21 On-chip Planner Spiral Inductors of different shapes

Chapter 3   *Design of the Low Power Ultra-Wideband Low Noise Amplifier*

3.1   Introduction

In this chapter, instead of using a common source amplifier, a common-gate amplifier is proposed for wideband input matching of UWB LNAs. It is well known that compared with using the common source amplifier, using the common gate amplifier can easily achieve wideband input matching, good linearity, and input-output isolation, but provides lower gain and higher noise figure. The π-section LC network technique is employed in the LNA to achieve sufficient gain with a reasonable noise figure level. The gain flatness throughout the band is within $\pm$ 1.0dB. Here, we also propose a structure to combine the common gate with band pass filters, which can reduce parasitic capacitance of the transistor and leads low power consumption.

3.2   Proposed Low Power UWB LNA architecture

Bandwidth, power consuming, input impedance matching, noise figure, and

reasonable power gain, are the major issues to be considered in the circuit design. It is well-known that these four issues are trade-offs one another [44]. Here, achieving optimum low power performance is our first priority. Our proposed UWB LNA circuit is shown in Figure 3.1, which employs the CMOS process. The LNA is composed by an input matching network and a π-section LC network.
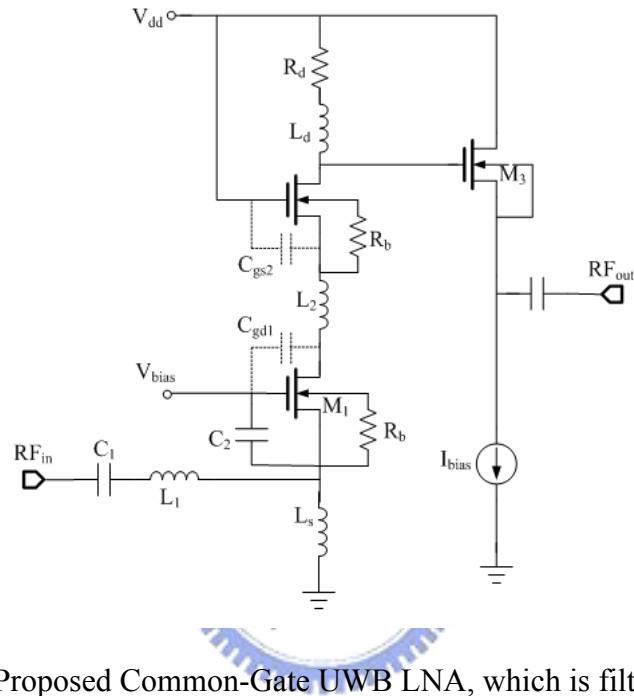
Figure 3.1   Proposed Common-Gate UWB LNA, which is filter configuration

3.2.1 Wideband Input Matching Design

Here, a common-gate amplifier is used as an important component for the input matching network of the proposed LNA. Although the common gate amplifier can easily achieve wideband input matching, good linearity, and input-output isolation, its parasitic capacitances of the transistor, will degrade the LNA performance in the high frequency region. Therefore, a two-order band pass filter is also introduced to reduce the parasitic capacitance. Demonstrates the proposed input matching network, which is composed of a common gate amplified and a two-order band pass filter, and its small signal equivalent circuit model are shown in Figure 3.2.
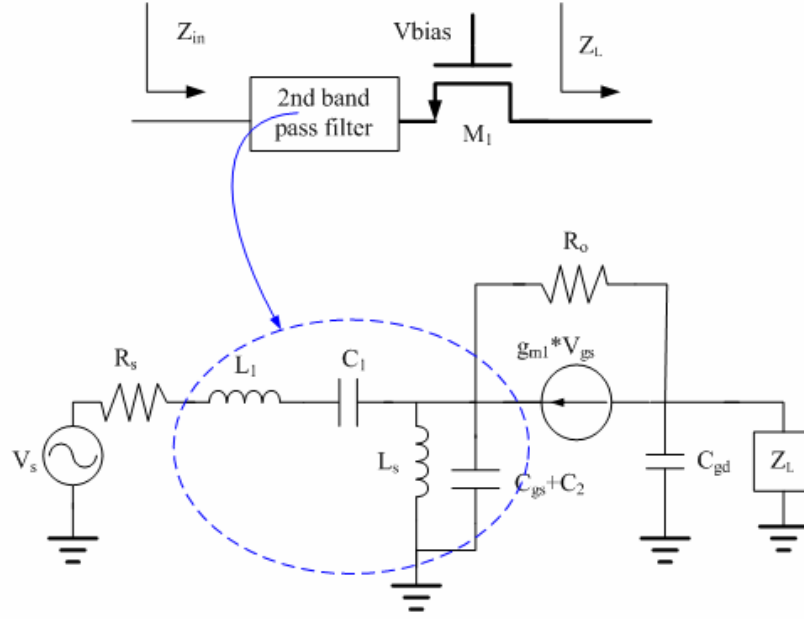
Figure 3.2   Common gate LNA input stage, which 2nd band-pass filter, and small

signal equivalent circuit model

In the equivalent circuit (Figure 3.2), Z_L is the input impedance of the cascode

stage and g_{m1} is the transconductance of the MOS transistor in common gate

configuration, R_o is the parasitic resistance of the transistor. L_1, C_1, L_s, and C_2+C_{gs} are

lumped-element circuits for the two order band-pass filter. Series and shunt L-C tanks

are used to adjust the pass band and the ripple. Based on band pass filter design

fundamental [43], L_1, C_1, L_s, and C_2+C_{gs} are given by, respectively,

$$L_1 = \frac{\Delta Z_0}{\omega_0 g_1} \qquad C_1 = \frac{g_1}{\Delta \omega_0 Z_0} \tag{3.1}$$

$$L_S = \frac{g_2 Z_0}{\Delta \omega_0} \qquad C_2 + C_{gs} = \frac{\Delta}{\omega_0 g_2 Z_0} \tag{3.2}$$

Here, $\Delta=(\omega_2-\omega_1)/\omega_0$ is the fractional bandwidth of the filter. ω_2 and ω_1 are the upper

(10.6GHz) and lower (3.1GHz) frequencies of the pass band. g_1 and g_2 are two

empirical constants and are equal to 1.5963 and 1.0967, respectively [43]. The matching

network is adopted for noise and impedance match to the 50 Ohm source with

L1=0.9nH, C1=850fF, Ls=3.50nH, C2+Cgs=240fF, which reflection coefficient and gain response simulation shown in Figure 3.3.
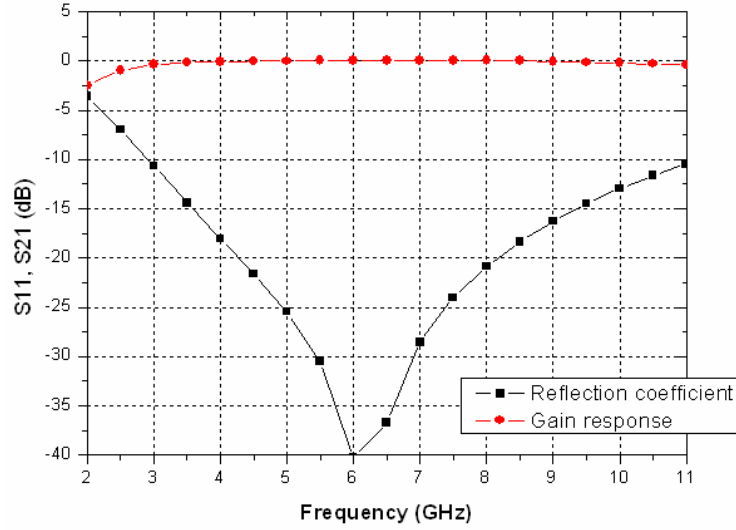
Figure 3.3 Reflection coefficient and gain response of 2nd band-pass filter

With the small signal equivalent circuit model (Figure 3.2), the input impedance of the MOS transistor can be treated as a series RLC circuit and is written as below:

$$Z_{in} = j\omega L_1 + \frac{1}{j\omega C_1} + \frac{1}{g_{m1} + \frac{1}{Z_S(\omega)} + \frac{1 - g_{m1}Z_1(\omega)}{R_o + Z_1(\omega)}} \qquad (3.3)$$

, where $Z_s(\omega)$ and $Z_1(\omega)$ are given by (1) and (2) below, respectively.

$$Z_S(\omega) = \frac{1}{j\omega C_{gs} + \frac{1}{j\omega L_S}} \qquad (3.4)$$

$$Z_1(\omega) = \frac{1}{j\omega C_{gd} + \frac{1}{Z_L}} \qquad (3.5)$$

From the smith chart in Figure 3.4, shows the reflection coefficient S11 of the proposed low power UWB low noise amplifier with a structure to combine the common gate with band pass filters and compares that of the amplifier without band pass filters. The addition of band pass filters gathers the values of input reflection coefficient S11 closer to the center of the smith chart. The orbit of input impedance reflection

coefficient with feedback circuit for frequency range is close to 50Ω matching.
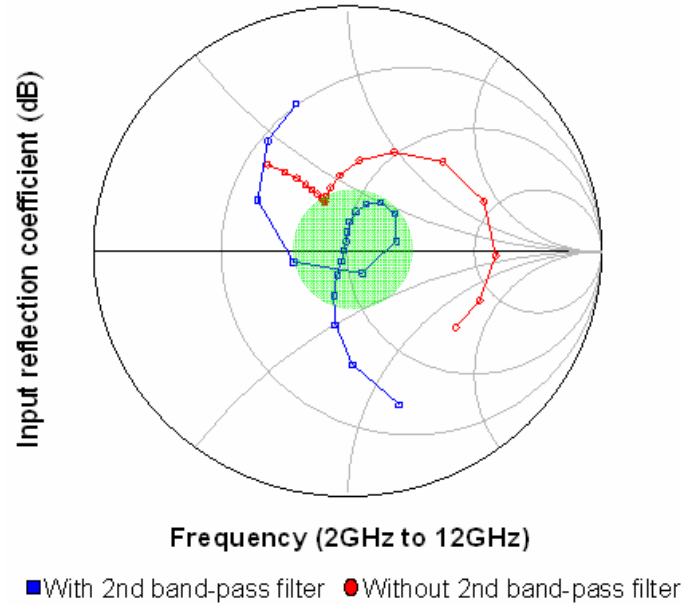
Figure 3.4   The smith chart of input reflection coefficient with 2nd band-pass filter

3.2.2 π-section LC network Design

Flat gain over the entire bandwidth, is another important requirement of the UWB LNA design. However, the shunt of M_1's gate-drain parasitic capacitance, C_{gd1}, and M_2's gate-source parasitic capacitance, C_{gs2}, provides an additional path for the RF signal current to the ground, which leads to power gain reduction especially for the high frequency band. In order to solve this problem, a π-section LC network technique is first adopted and proposed for our design. Figure 3.5 (b) shows the circuit of the π-section LC network, which is formed by an inductor and the gate-source parasitic capacitances.

The small signal equivalent circuit of the π-section LC network circuit is illustrated in Figure 3.6. I_{d1} is the small signal drain current of M_1. L_2 is the introduced passive inductor. R_o and C_o represent the parasitic resistance and capacitance of the inductor, respectively. R_o is the series resistance and is around 3 to 20 Ohms, and C_o is the fringing field capacitance of the spiral, which is also called "feed-through capacitance".
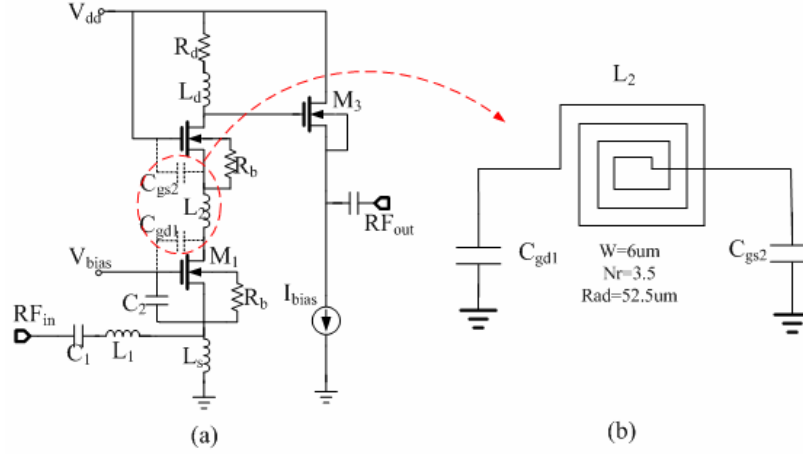
Figure 3.5   (a) Proposed low power LNA, and (b) π-section LC network of proposed LNA.
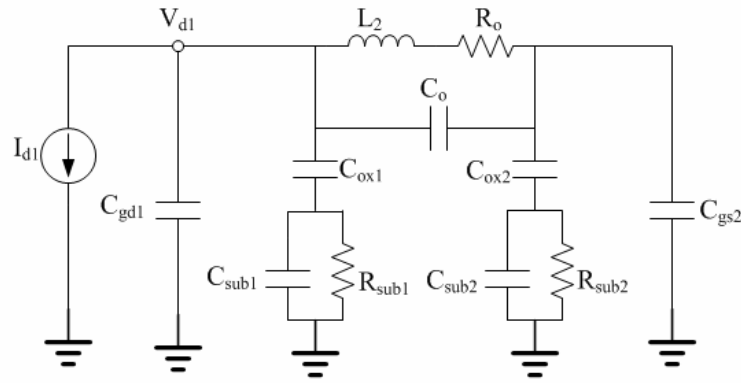
Figure 3.6   π-section small signal equivalent circuit model

After some derivations, the π-section LC network circuit gain, V_{d1}/I_{d1}, is found and given by

$$\frac{V_{d1}}{I_{d1}}(\omega) = \cfrac{1}{j\omega C_{gd1} + \cfrac{1}{Z_{sub1}(\omega)} + \cfrac{1}{\cfrac{1}{j\omega C_{gs2}} + \cfrac{j\omega L_2 + R_o}{1 + j\omega C_o(j\omega L_2 + R_o)} + Z_{sub2}(\omega)}} \tag{3.6}$$

, where $Z_{sub1}(\omega)$ and $Z_{sub2}(\omega)$ are given by (3.7) and (3.8), respectively.

$$Z_{sub1}(\omega) = \frac{1}{j\omega C_{ox1}} + \cfrac{1}{j\omega C_{sub1} + \cfrac{1}{R_{sub1}}} \tag{3.7}$$

$$Z_{sub2}(\omega) = \frac{1}{j\omega C_{ox2}} + \frac{1}{j\omega C_{sub2} + \dfrac{1}{R_{sub2}}} \tag{3.8}$$

Here C_{ox}, R_{sub}, and C_{sub} are ignored in equation (3.6), where C_{ox} is the oxide capacitance between the spiral and the substrate. R_{sub}, and C_{sub} are silicon substrate resistance and silicon substrate capacitance, respectively, which are relatively small and are neglected. Then, equation (3.6) becomes

$$\frac{V_{d1}}{I_{d1}}(\omega) = \frac{1}{j\omega C_{gd1} + \dfrac{1}{\dfrac{1}{j\omega C_{gs2}} + \dfrac{j\omega L_2 + R_o}{1 + j\omega C_o(j\omega L_2 + R_o)}}} \tag{3.9}$$

$Z(\omega) = V_{d1}/I_{d1}$ is the input impedance of π-section LC network. To achieve a flat gain, finding a proper L_2 is needed to make $Z(\omega)$ close to 50 Ohm through out the whole band. From the smith chart in Figure 3.7, shows the reflection coefficient of π-section input reflection coefficient with different inductor L_2..
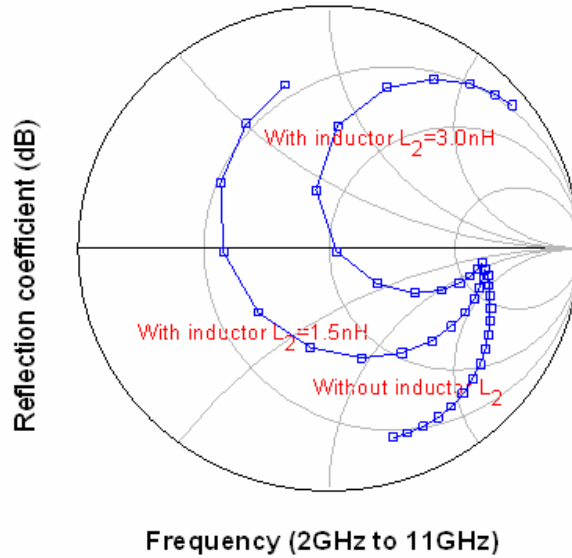
Figure 3.7   Reflection coefficient of π-section with different inductor L_2.

It is found from Figure 3.8 that $L_2=3$ nH yields a satisfied flat gain within a variation of ±1.5 dB relative to the average. Therefore, inductor $L_2=3$ nH is chosen for later simulation
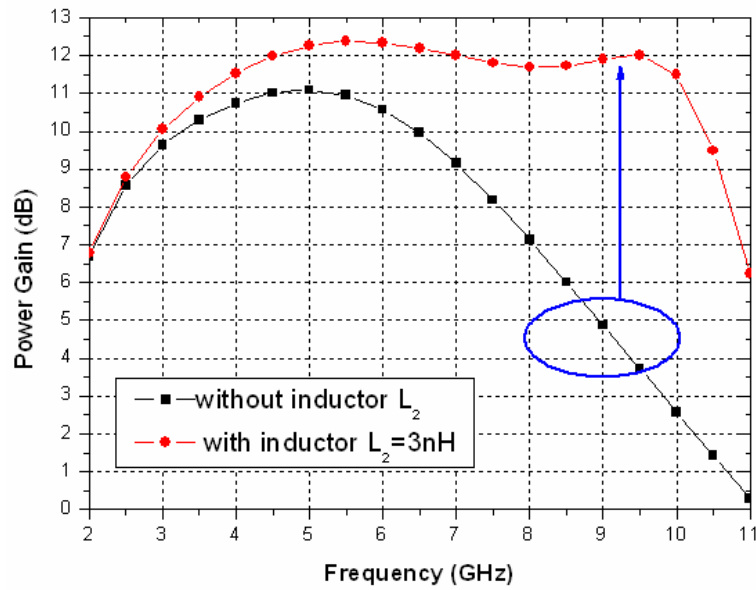
Figure 3.8   Power gain versus signal frequency with L_2

3.2.3 Low power Design

The low dc current technique and low voltage technique are employed to attain the low power for the ultra-wideband low noise amplifier design, which used in proposed common gate LNA (chapter 3), and common source LNA (chapter 4).

A. Low direct current design

The low direct current design is used in proposed common gate UWB LNA design. The typical common gate LNA is shown in Figure 3.9.
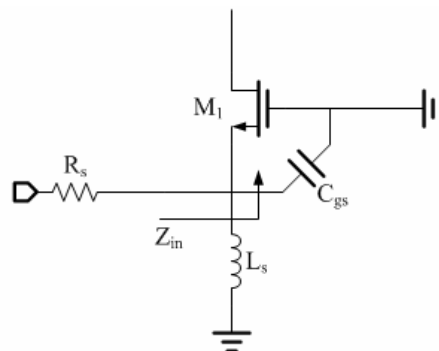
Figure 3.9 Input impedance of typical common gate LNA

The input impedance of the common gate amplifier in Figure 3.9 can be written

$$Z_{in} = \frac{1}{g_{m1} + j\omega C_{gs}}$$
(3.11)

The input impedance is approximately as $Z_{in} \approx \dfrac{1}{g_{m1}}$ in the low frequency. It has to be matched to the 50Ohm. The common gate architecture (or the $1/g_m$ termination) that is illustrate in Figure 3.10 (a) has the highest potential to achieve the wideband input impedance $Z_{in} \approx 50\Omega$. However, the drain current $I_D = \dfrac{1}{2}\mu_n C_{ox} \dfrac{W}{L}(V_{gs} - V_{thn})^2$,

transconductance (g_m) $g_m = \mu_n C_{ox} \dfrac{W}{L}(V_{gs} - V_{thn}) = \sqrt{2\mu_n C_{ox}\dfrac{W}{L}I_{D1}}$ of transistor M_1 and

input impedance $Z_{in} \approx \dfrac{1}{g_m} = \dfrac{1}{\sqrt{2\mu_n C_{ox}\dfrac{W}{L}I_{D1}}} \propto \dfrac{1}{\sqrt{I_{D1}}} = 50\Omega$. If $I_{D1} \to \dfrac{1}{2}I_{D1}$, the input

impedance of transistor M_2 $Z_{in} \approx 50\sqrt{2} = 70\Omega$ is shown in Figure 3.10 (b). In Figure 3.10 (c), we proposed a structure to combine the common gate with band pass filters technique, which can achieve the impedance transformations and leads low power consumption. The impedance transformations technique is shown in Figure 3.11 and its using two order band pass filter to achieve this design.
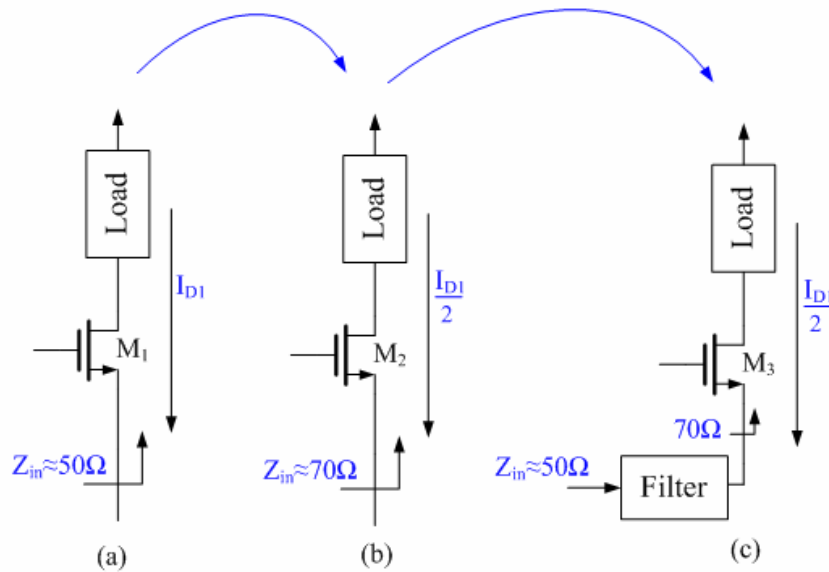
Figure 3.10   A flow chart of proposed low direct current design
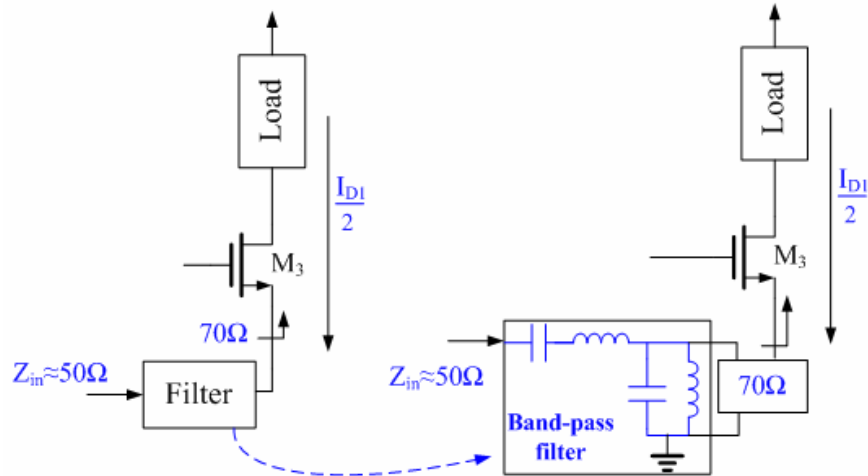
Figure 3.11   The impedance transformations technique with using band pass filter

B. Low voltage design

The bottle-neck for the low voltage design is the limitation of threshold voltage because it is not anticipated to decrease much below. The conventional cascode architecture amplifier shown in Figure 3.12 (a), it require a high supply voltage and not suitable for low voltage application. In order to overcome this problem, the cascade architecture with two LC tanks, as shown in Figure 3.12 (b). The RF signal is amplified by common-source and blocking capacitor couples the signal to common gate.
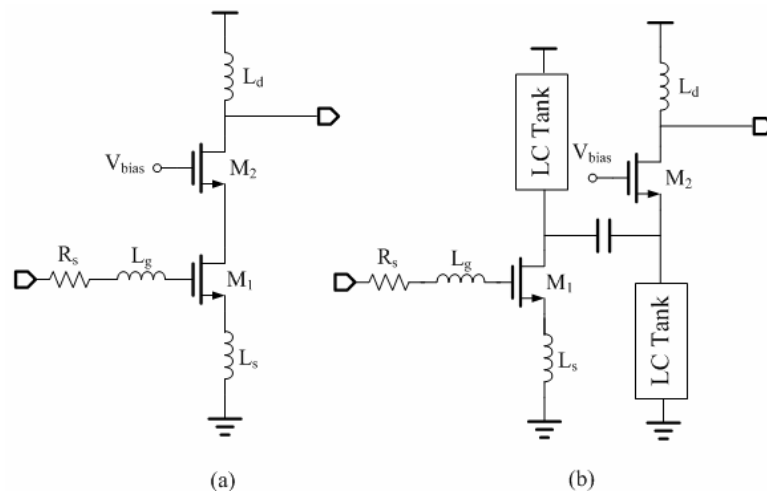
Figure 3.12 (a) Conventional cascode architecture LNA, (b) Low voltage LC tank cascade LNA.

The low voltage LNA needs two LC tanks and a large blocking capacitor which

results in a large chip area. In order to solve this problem, a solution to the reduce threshold voltage is employed to low voltage technique. The threshold voltage problem comes from the well-known relationship as given

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}) \tag{3.10}$$

, where V_{th0} is the value of V_{th} with V_{BS}=0, γ is the bulk threshold parameter and ϕ_F is the strong inversion surface potential of the MOSFET. To reduce the threshold voltage as much as possible, we want to the bias V_{BS} as high as possible. In Figure 3.13 (a) the allowable voltages cascode architecture with inductive source degeneration is a popular configuration for LNA design. If $M_1$and M_2 are both in saturation, then V_X is determined primarily by V_{b2}: $V_X=V_{b2}(=V_{DD})-V_{gs2}$. For M_2 to be saturated, $V_{DD} \geqq V_{b2}(=V_{DD})-V_{thn}$, that is, $V_{DD} \geqq V_{gs1}-V_{thn}+V_{gs2}-V_{thn}$ if V_{b2} is chosen to place M_1 at the edge of saturation. But it has not very low voltage supply applications because the power supply must satisfy the following a requirement $V_{DD} + |V_{SS}| \geq 2V_{thn}$. The V_{DD} and V_{SS} are the positive and negative power supply, V_{thn} is the threshold voltage of the each of the NMOS transistor.
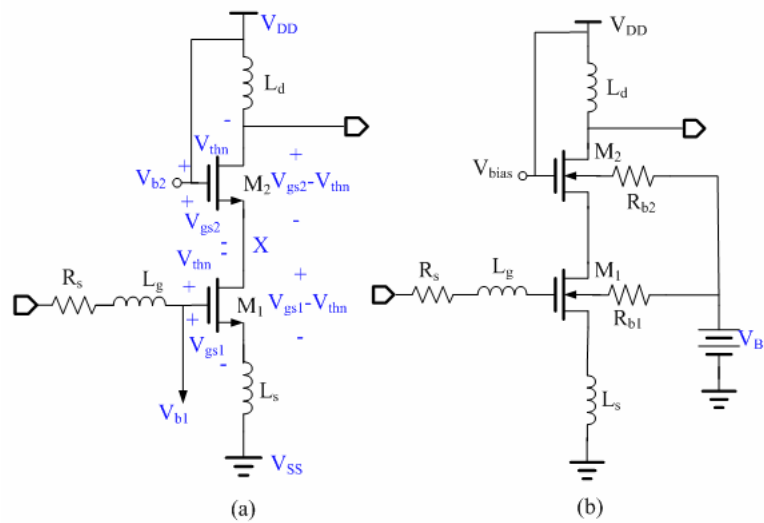
Figure 3.13   (a)The allowable voltages, and (b) low voltage design of the cascode architecture LNA.

The low voltage design of the cascode LNA is shown in Figure 3.13 (b). A V_{BS}=0.6 voltage is employed to forward-bias the body-source junction of transistor M_1 and M_2. The V_{DD} can be attained to 0.7V with dc current is 4.5mA. The proposed Low-voltage technique can be explained by UWB feedback LNA architecture is taken up in the next chapter.

3.3 Simulation Results

Figure 3.14 shows the layout of the proposed UWB LNA. The size of the layout area is 0.89mm by 0.77mm including pads. And the measure PCB is shown in Figure 3.15. In Figure 3.16, S11 and S22 versus signal frequency are illustrated. It is found that the input reflection S11＜-10.44dB and output matching S22<-12.05dB in the range of 3.1~10.6 GHz. The power gain (S21) is around 10.0~12.4dB. 3dB bandwidth of the LNA is 7.8 GHz and is satisfied the need of UWB. The noise figure of the LNA is shown in Figure 3.17. It is found that the noise figure is at least less than 4.4dB in 3.1~10.6GHz and its minimum value is 3.25dB at 8.5GHz. The linearity of an amplifier is traditionally described in terms of 1-dB compression point (P1dB) and third-order intercept point (IP3). However, the IP3 of the proposed LNA is not of great concern of this work due to the two reasons: Firstly, the UWB signals are intrinsically wideband signals rather than single tones in narrowband systems, which bring about the difficulty in defining the IP3 for the LNA. The simulation results also show that the output third-order-intercept points (OIP3s) are 7.669dBm at 3GHz, 5.33dBm at 5GHz, 5.09dBm at 6GHz, 4.24dBm at 8GHz, 2.23dBm at 10GHz. A low supply voltage of 1.5V is chosen, and the total power consumption is 3.0mW.
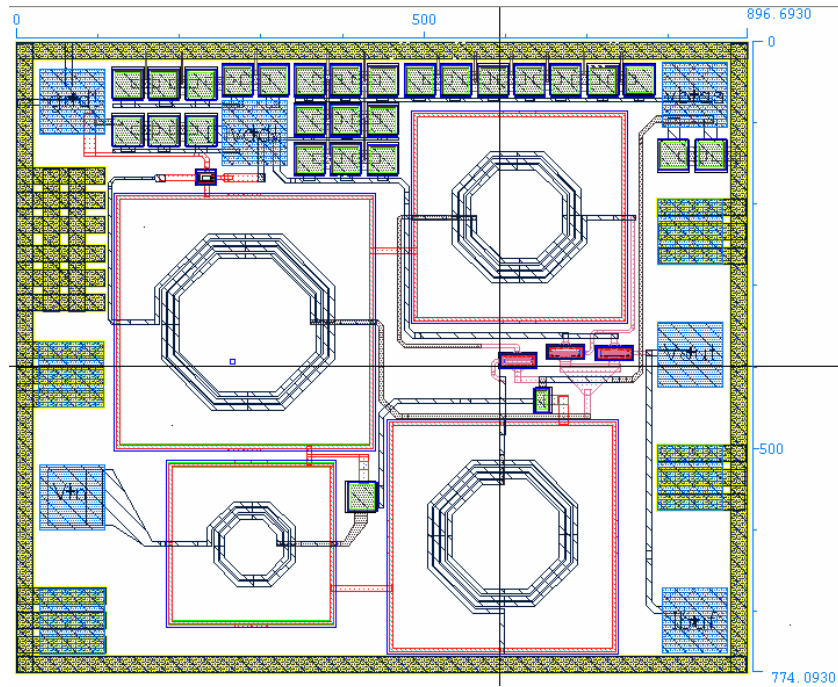
Figure 3.14 Layout of the proposed UWB LNA
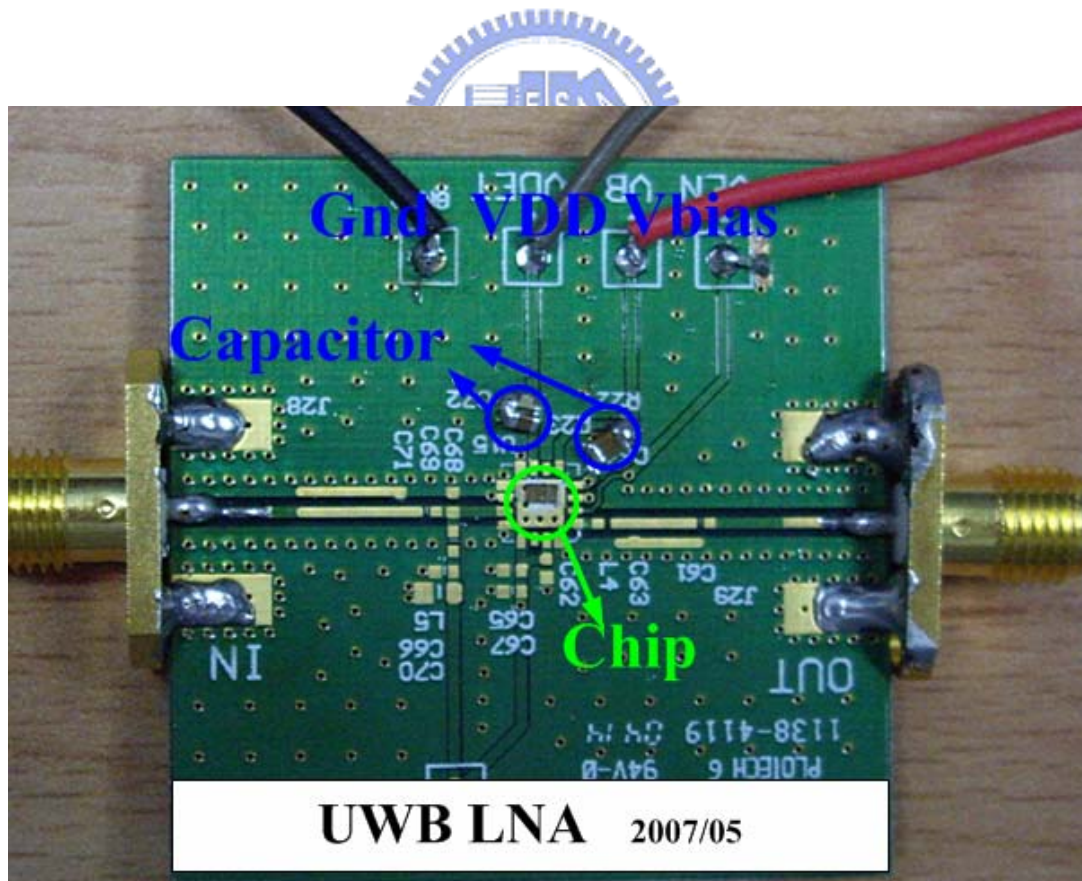
Figure 3.15 Measure PCB of the proposed UWB LNA
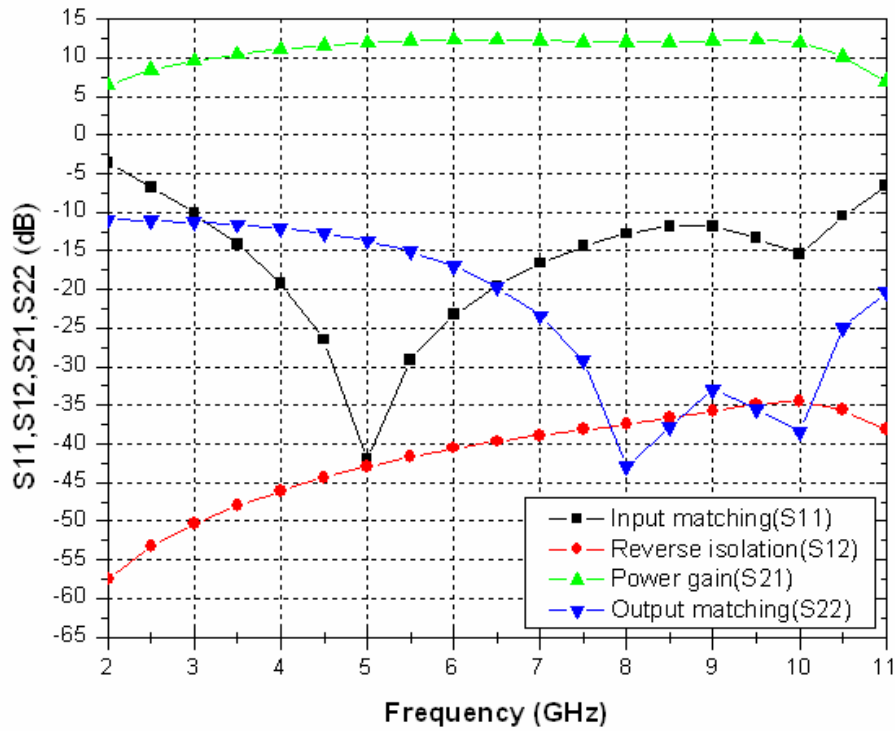
Figure 3.16 S-parameters versus signal frequency
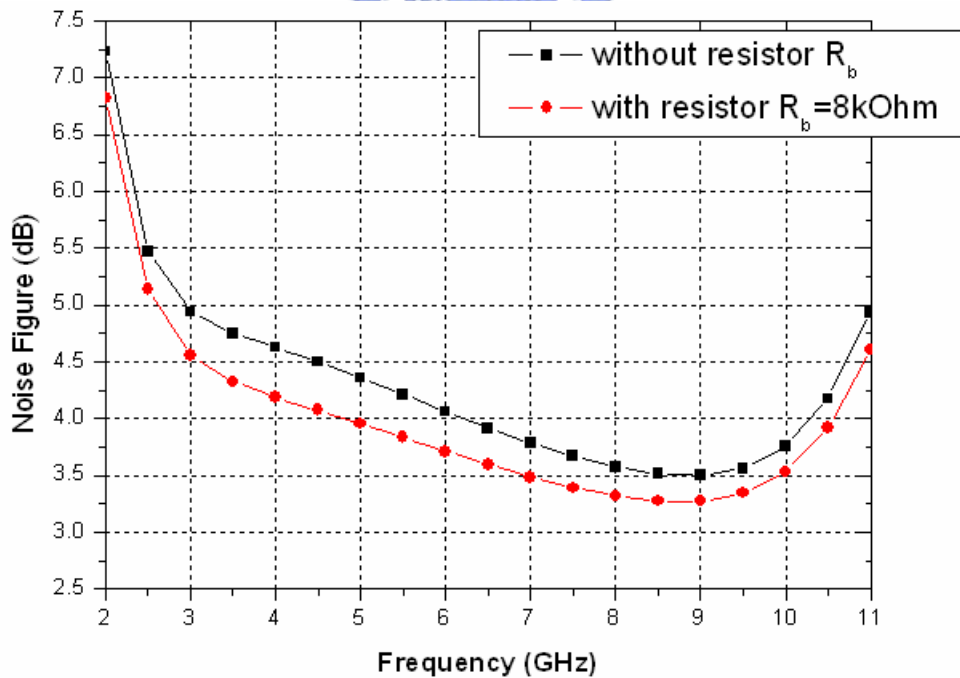
Figure 3.17 Noise figure versus signal frequency with or without R_b.

The performance of the proposed LNA is summarized in Table 3.1, with comparison to other recently published ultra-wideband LNAs' simulation results.

Table 3.1
Summary of LNA performance and comparison with published LNAs

Ref.	Tech.	BW (GHz)	S11 (dB)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)
[1-a]	0.18um CMOS	2.3-9.2	<-9.9	9.3	4.0	-6.7*	9.0
[1-b]	0.18um CMOS	2.4-9.5	<-9.4	10.4	4.2	-8.8*	9.0
[8]	0.18um SiGe	0.1-11	<-12	8	2.9	-3.4#	21.6
[4]	0.18um CMOS	3.1-10.6	<-9	17.5	3.1	N/A	33.2
[10]	0.18um CMOS	2-10.1	<9.76	10.2	3.68	-1.0*	7.2
Our work	0.18um CMOS	3-10.6	<-10.4	12.4	3.25	-3.97*	3.0

Figure 3.18 Linearity parameters P_{1dB} at 3GHz

Linearity parameters P_{1dB} can be explained by Figure 3.21.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm)=10+(-12)=-2dBm$

Simulation results of $P_{1dB}=-3.3dBm$.

Figure 3.19 Linearity parameters OIP3 at 3GHz

Linearity parameters OIP3 can be explained by Figure 3.22.

$OIP3=P_{out}+\dfrac{1}{2}IMD=-10.443+\dfrac{1}{2}(46.667-10.443)=7.669dBm$
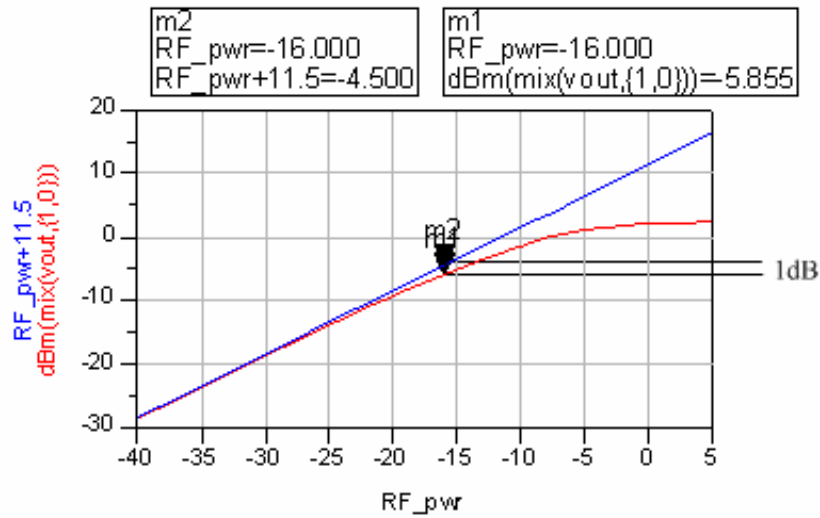
Figure 3.20 Linearity parameters P_{1dB} at 4GHz

Linearity parameters P_{1dB} can be explained by Figure 3.23.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm) = 11.5+(-16) = -5.5dBm$

Simulation results of $P_{1dB} = -5.8dBm$.

Figure 3.21 Linearity parameters OIP3 at 4GHz

Linearity parameters OIP3 can be explained by Figure 3.24.

$OIP3=P_{out}+\dfrac{1}{2}IMD=-9.29+\dfrac{1}{2}(40.868-9.29)=6.49dBm$
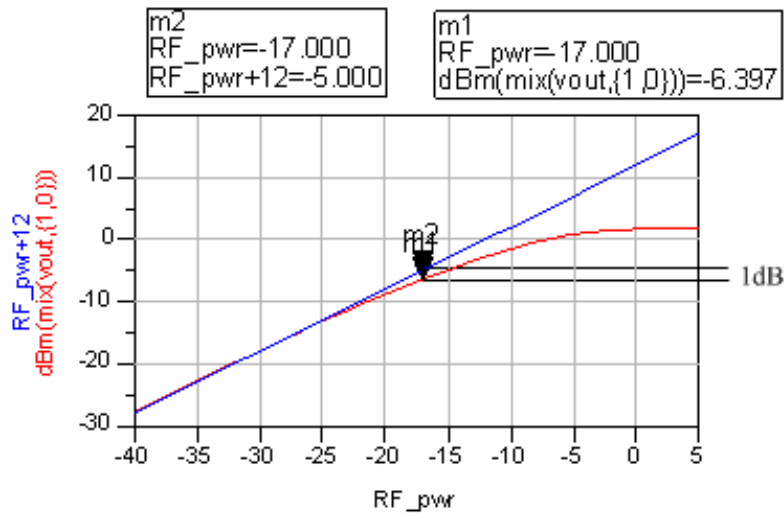
Figure 3.22 Linearity parameters P_{1dB} at 5GHz

Linearity parameters P_{1dB} can be explained by Figure 3.25.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm)=12+(-17)=-5dBm$

Simulation results of $P_{1dB}=-6.3dBm$.
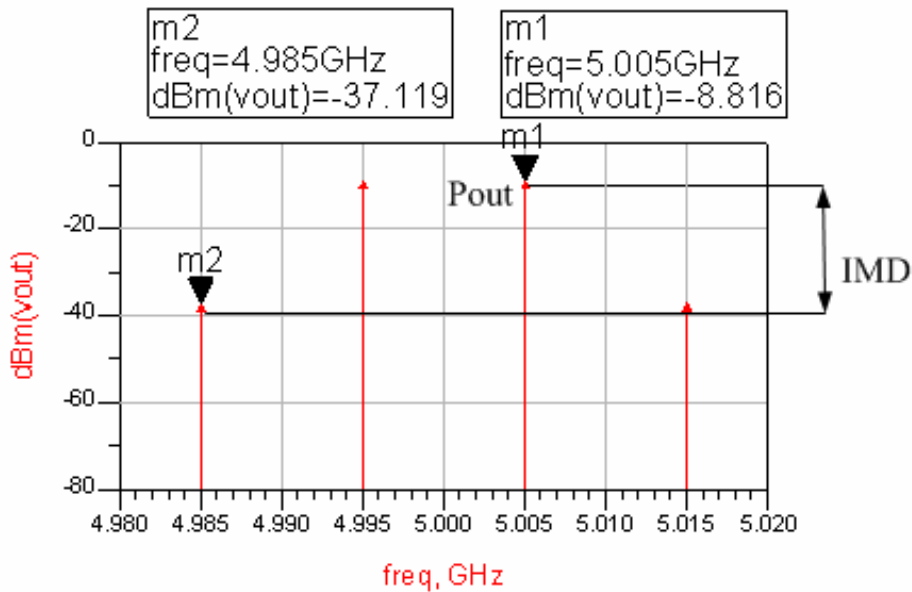
Figure 3.23 Linearity parameters OIP3 at 5GHz

Linearity parameters OIP3 can be explained by Figure 3.26.

$OIP3=P_{out}+\frac{1}{2}IMD=-8.816+\frac{1}{2}(37.119-8.816)=5.33dBm$
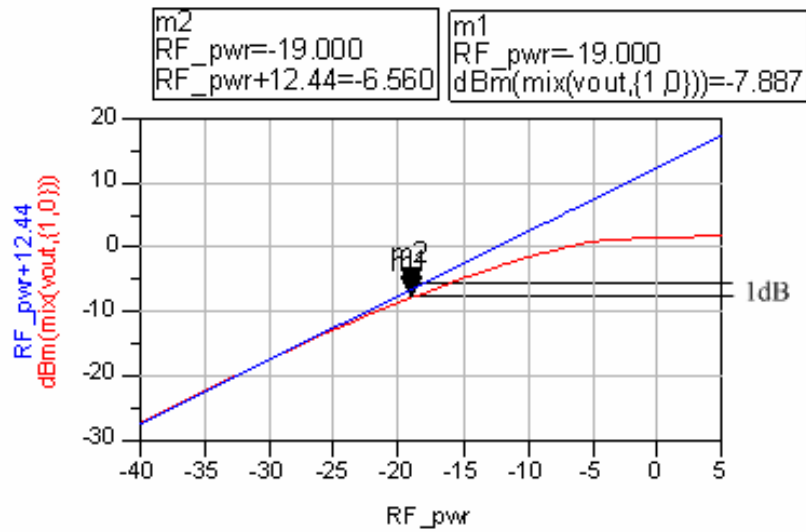
Figure 3.24 Linearity parameters P_{1dB} at 6GHz

Linearity parameters P_{1dB} can be explained by Figure 3.27.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm)=12.44+(-19)=$-6.56dBm

Simulation results of $P_{1dB}=$-7.8dBm.
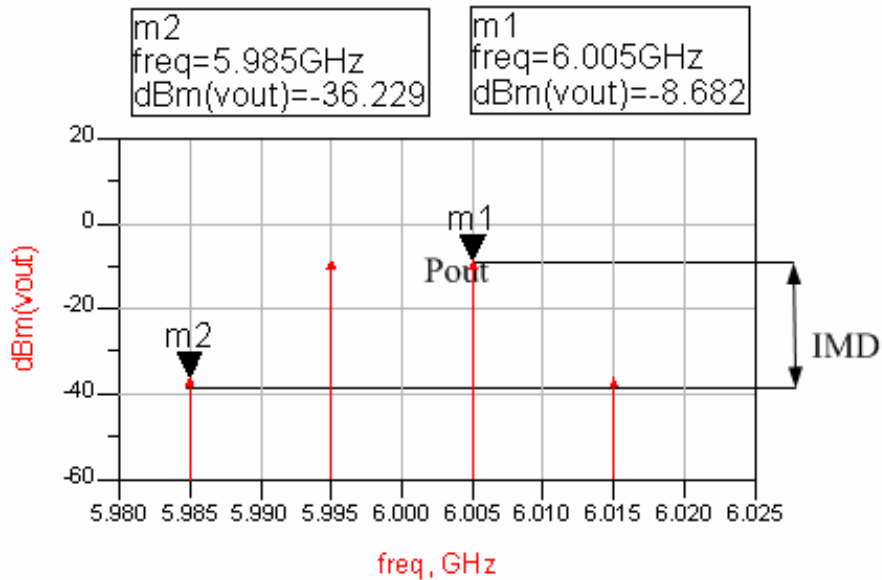
Figure 3.25 Linearity parameters OIP3 at 6GHz

Linearity parameters OIP3 can be explained by Figure 3.28.

$OIP3=P_{out}+\dfrac{1}{2}IMD=-8.682+\dfrac{1}{2}(36.229-8.682)=$5.09dBm
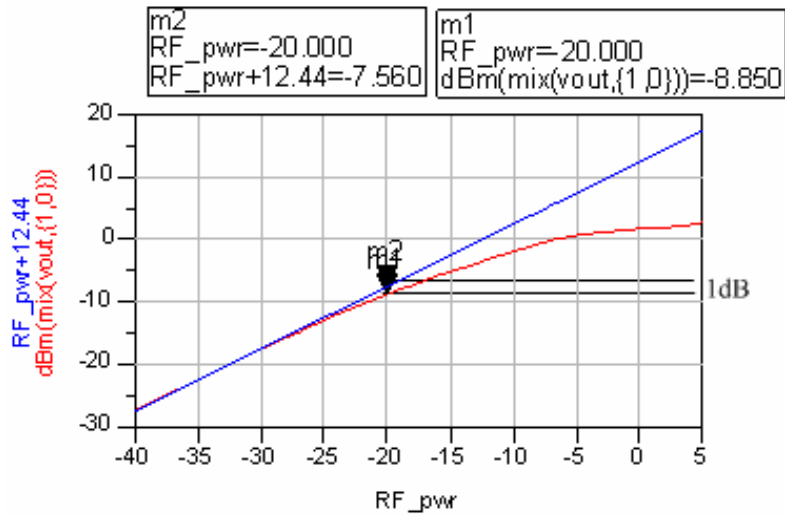
Figure 3.26 Linearity parameters P_{1dB} at 7GHz

Linearity parameters P_{1dB} can be explained by Figure 3.29.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm)=12.44+(-20)=-7.56dBm$

Simulation results of $P_{1dB}=-8.8dBm$.
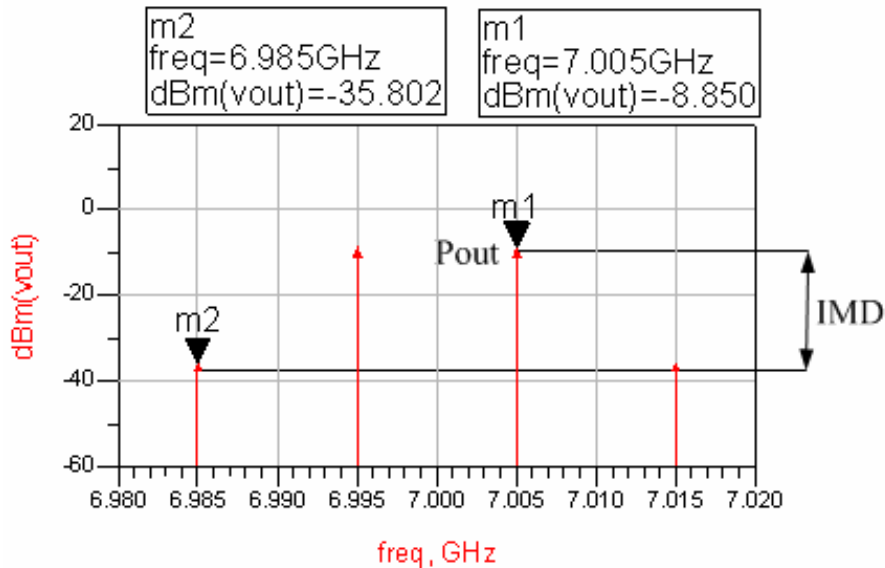
Figure 3.27 Linearity parameters OIP3 at 7GHz

Linearity parameters OIP3 can be explained by Figure 3.30.

$OIP3=P_{out}+\dfrac{1}{2}IMD=-8.85+\dfrac{1}{2}(35.802-8.85)=4.62dBm$
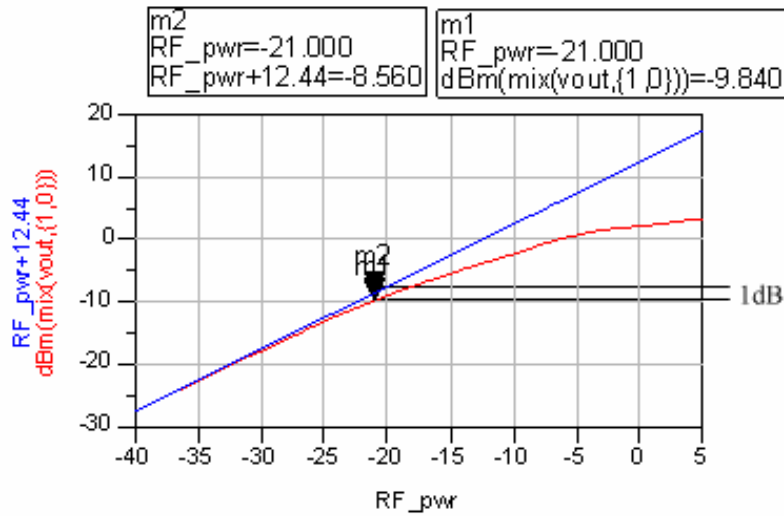
Figure 3.28 Linearity parameters P_{1dB} at 8GHz

Linearity parameters P_{1dB} can be explained by Figure 3.31.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm)=12.44+(-21)=$-8.56dBm

Simulation results of $P_{1dB}=$-9.84dBm.
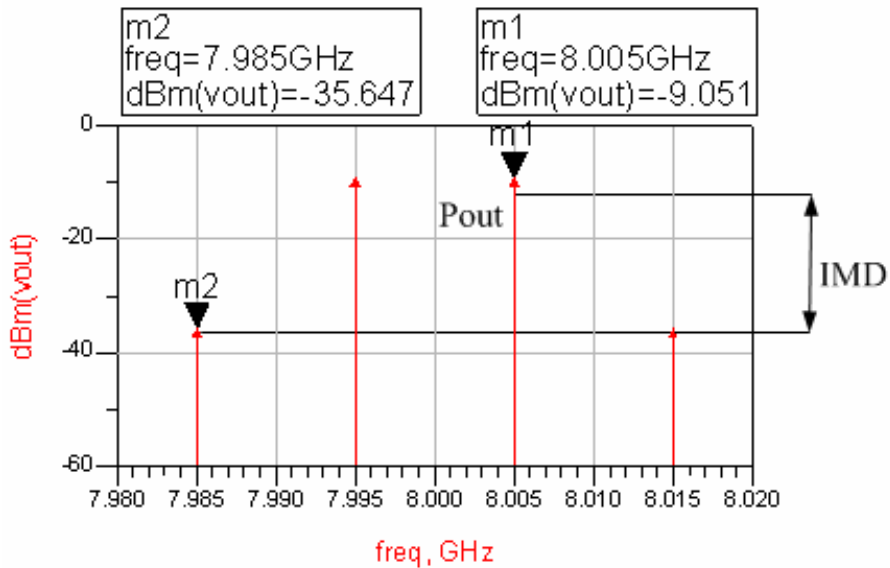
Figure 3.29 Linearity parameters OIP3 at 8GHz

Linearity parameters OIP3 can be explained by Figure 3.32.

$OIP3=P_{out}+\dfrac{1}{2}IMD=-9.051+\dfrac{1}{2}(35.647-9.051)=$4.24dBm
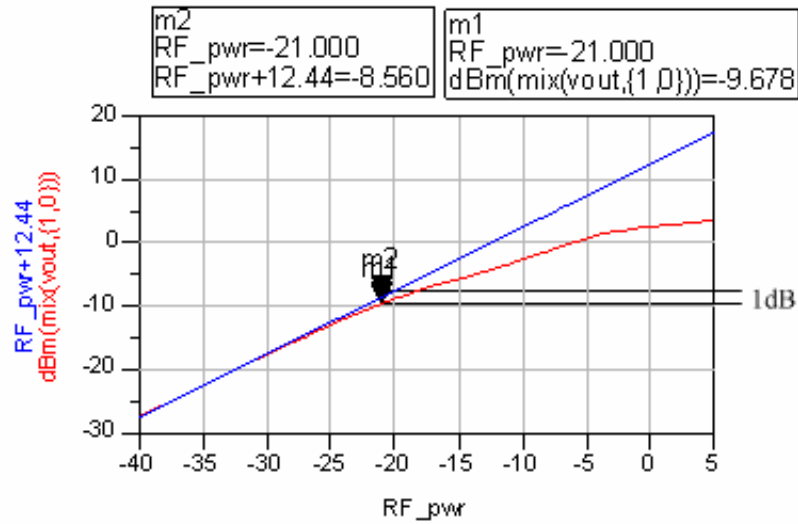
Figure 3.30 Linearity parameters P_{1dB} at 9GHz

Linearity parameters P_{1dB} can be explained by Figure 3.33.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm)=12.44+(-21)=-8.56dBm$

Simulation results of $P_{1dB}=-9.67dBm$.
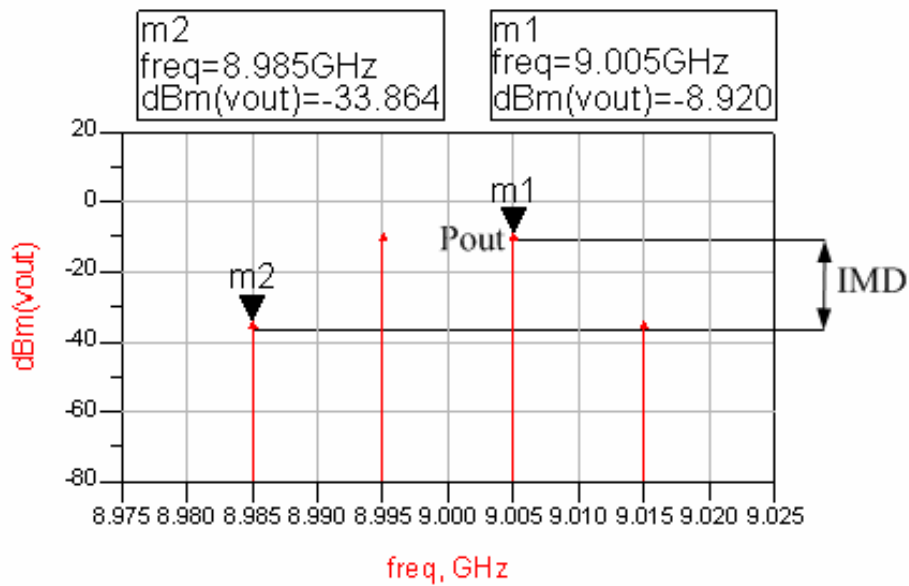
Figure 3.31 Linearity parameters OIP3 at 9GHz

Linearity parameters OIP3 can be explained by Figure 3.34.

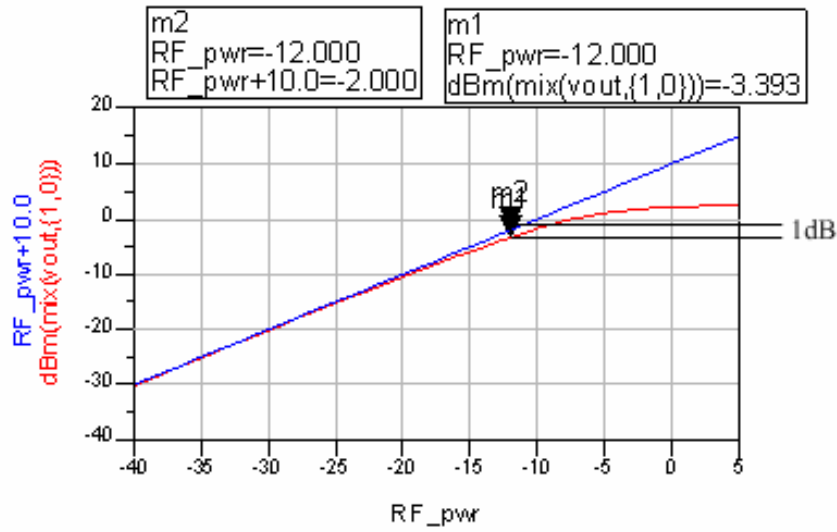$OIP3=P_{out}+\dfrac{1}{2}IMD=-8.92+\dfrac{1}{2}(33.864-8.92)=3.55dBm$
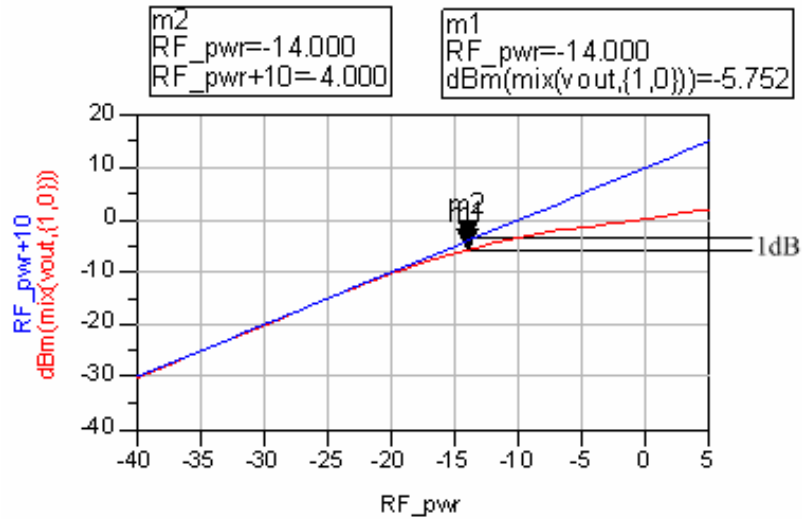
Figure 3.32 Linearity parameters P_{1dB} at 10.6GHz

Linearity parameters P_{1dB} can be explained by Figure 3.35.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm) =10+(-14)=-4dBm$
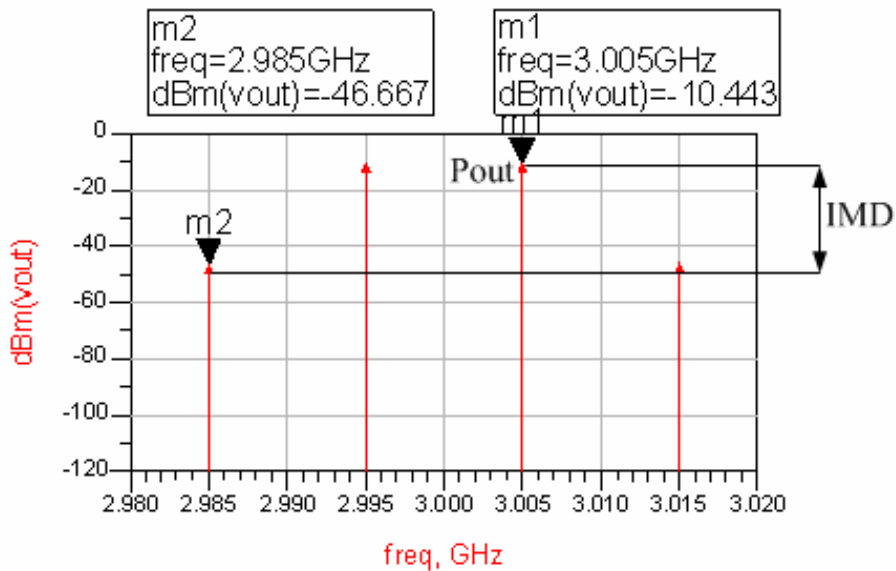
Simulation results of $P_{1dB}=-5.7dBm$.
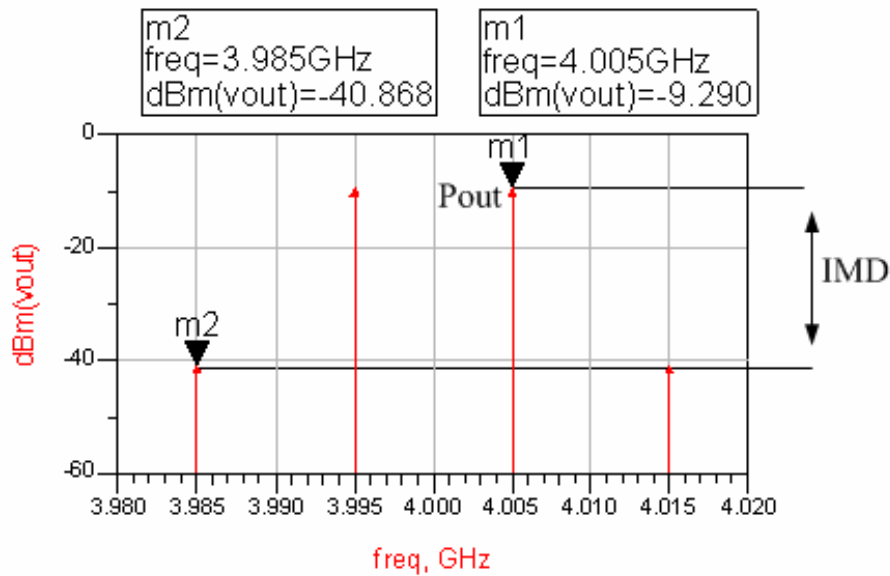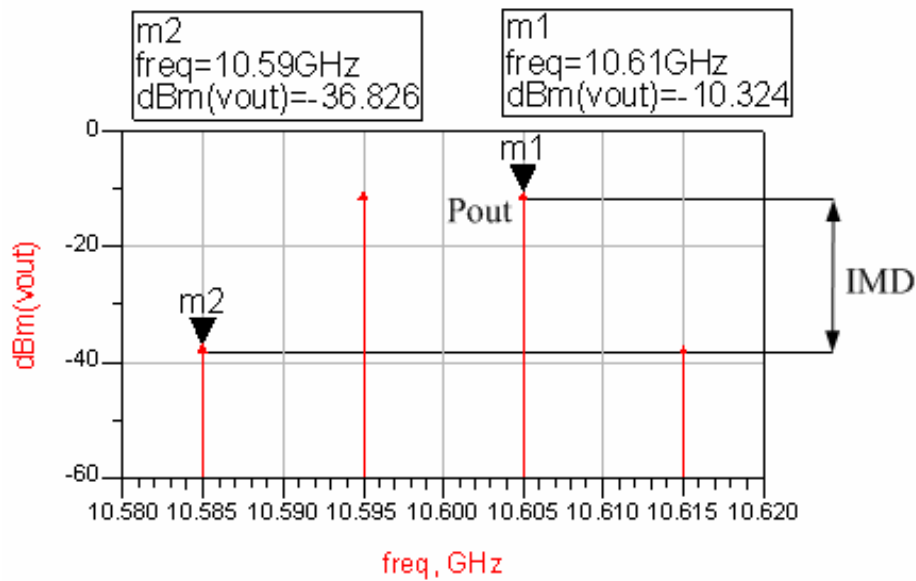

Figure 3.33 Linearity parameters OIP3 at 10.6GHz

Linearity parameters OIP3 can be explained by Figure 3.36.

$OIP3=P_{out}+\dfrac{1}{2}IMD=-10.324+\dfrac{1}{2}(36.826-10.324)=2.93dBm$

Chapter 4 *Design of the Low Voltage Ultra-Wideband Low Noise Amplifier*

4.1 Introduction

A very low-voltage ultra-wideband (UWB) low-noise amplifier (LNA) is achieved by reducing transistor's threshold voltage using an external bias to the transistor body node. To achieve ultra-wideband input impedance matching, a novel design is proposed for the LNA by adding a feedback resistor R_f to a conventional LNA cascode architecture. Based on TSMC 0.18μm 1P6M process, the numerical result shows that the LNA has 11.8~14.0dB gain from 6 GHz to 10.0 GHz with input matching S11<-13.7dB and 2.81dB noise figure in 7.0GHz. It only dissipates 2.8 mW with a small power supply of 0.75V.

4.2 Proposed LNA with feedback resistor architecture

The proposed ultra-wideband Low Noise Amplifier architecture is shown in Figure 4.1, which is different from the conventional narrowband cascode Low Noise Amplifier

architecture [8], [17] by adding a feedback circuit. In Figure 4.2, R_f is added as a feedback element to the conventional cascode narrowband and Low Noise Amplifier and L_d, and R_d are used as peaking loads at the output [1], [10]. The capacitor C_f and C_1 are used for ac coupling capacitors. The Sources-follower buffer M_3 is designed for output matching, with the bias current at 5mA.
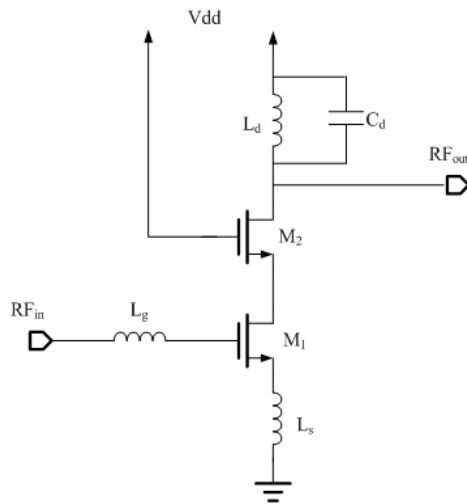
Figure 4.1   Conventional narrowband cascode LNA
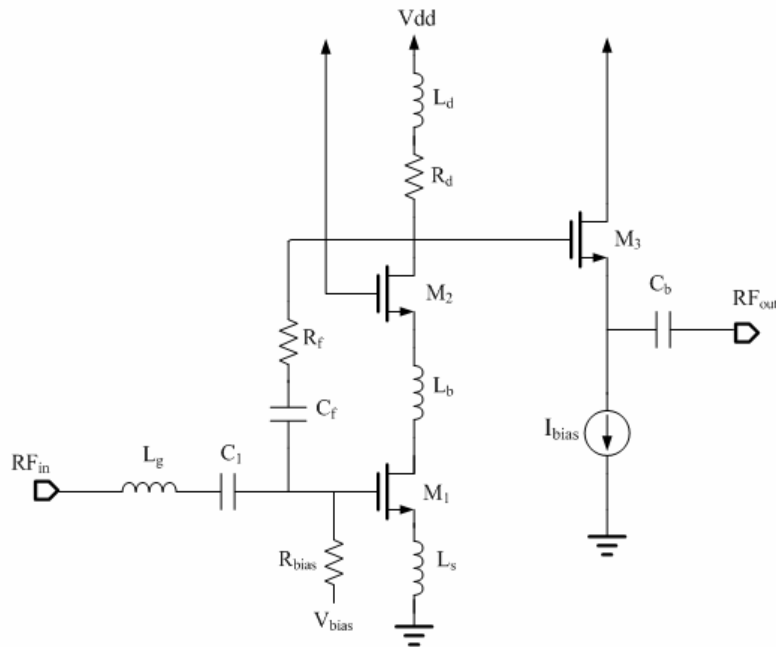
Figure 4.2   The proposed ultra-wideband LNA, which is resistor

feedback configuration

4.2.1 Resistive shunt feedback technique

The resistor feedback configuration is the most common method of negative feedback technique. First, determination of feedback resistance value R_f is important. In the proposed Low Noise Amplifier, the values of feedback resistors R_f (300-2000Ω) are employed to produce the wideband input impedance matching, without affecting the Noise Figure (NF) significantly. Due to the Noise Figure of the feedback amplifier cannot be optimized without sacrificing other important performance such as gain, gain flatness, input/output return loss.

Table 4.1 represents the minimum Noise Figure (NF$_{min}$), gain flatness, and input return loss (S11) of the feedback amplifier by different resistance values. In order to achieve a gain flatness of between 6.0-10.6 GHz, return loss S11<-10dB of 6.0GHz-10.6 GHz, and the noise figure of less than 2.5dB, the feedback resistance was chosen to between 800Ω and 1000Ω. Therefore, the Low Noise Amplifier can be tuned to achieve proper resistance value R_f for a wideband frequency range.

Table 4.1   Effect on feedback resistance

Feedback R_f	NF$_{min}$	Gain Flatness (-3dB range)	Return Loss S11< -10dB
300 Ω	2.9 dB	6.9-11.3 GHz	2.0-8.7 GHz
500 Ω	2.55 dB	5.5-10.6 GHz	3.8-10.2 GHz
800 Ω	2.36 dB	4.4-10.4 GHz	5.0-10.6 GHz
1000 Ω	2.3 dB	4.0-10.4 GHz	5.4-10.8 GHz
2000 Ω	2.26 dB	3.1-10.4 GHz	6.0-10.7 GHz

From the smith chart in Figure 4.3, shows the simulated S11 of the proposed Ultra wideband Low Noise Amplifier with feedback resistor R_f=1000Ω and compares that of the amplifier without feedback resistor R_f. The addition of feedback resistor R_f gathers

the values of input reflection coefficient S11 closer to the center of the smith chart. The orbit of input impedance reflection coefficient with feedback circuit for frequency range is close to 50Ω matching. 3dB bandwidth of the LNA is 6.4 GHz and input matching <-10dB bandwidth is 5.25GHz (Figure 4.4), which satisfied the need of UWB in the range of 6~10.6 GHz. The resistive and capacitive shunt feedbacks (R_f, C_f) also improve the better stability, gain flatness, and bandwidth.
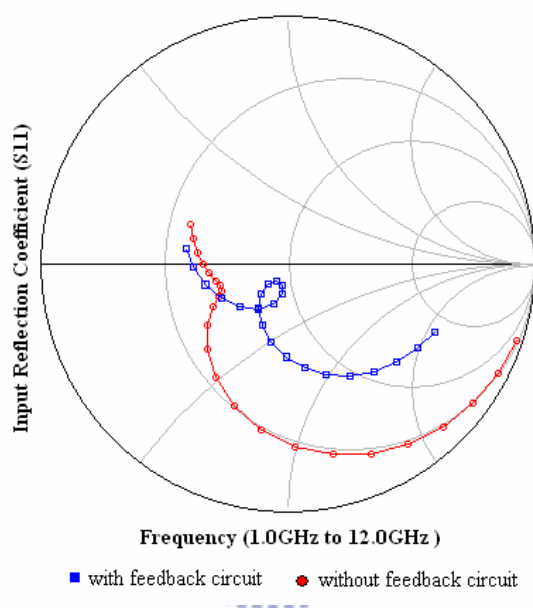
Figure 4.3   The smith chart of input impedance matching (R_f=1000Ω)
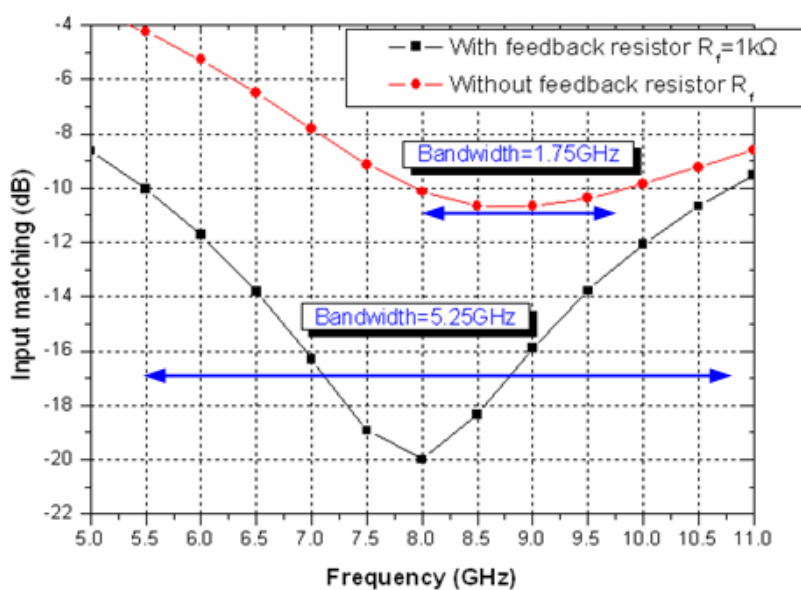
Figure 4.4   Bandwidth with R_f=1000Ω to compare with the case without R_f

4.2.2 Noise analysis

For proposed Ultra-wideband Low Noise Amplifier (Figure 4.2), its noise equivalent circuit of the input is shown in Figure 4.5
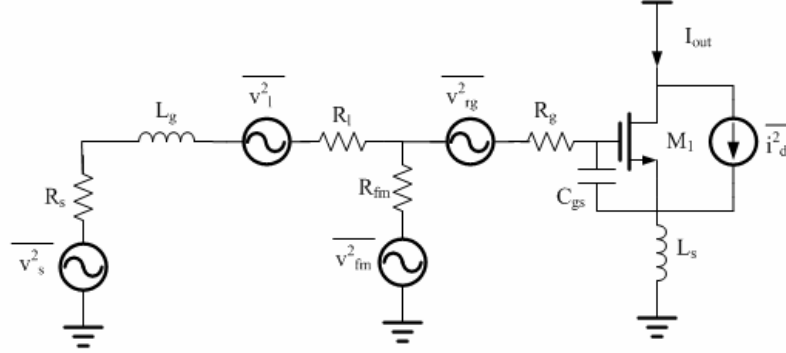
Figure 4.5   Noise equivalent circuit of the input stage of proposed

ultra-wideband LNA.

The noise factor for an amplifier is defined as:

$$F \equiv \frac{Total \quad output \quad noise}{Total \quad output \quad noise \quad due \quad to \quad the \quad source} \tag{4.1}$$

As equation (4.1) shows, the noise factor equals to total output noise divided by source induced output noise. In order to calculate it, we evaluate the noise contribution from the input source. First the input equivalent G_m is

$$G_m = g_{m1} Q_{in} \approx g_{m1} \frac{1}{\omega_0 C_{gs} \left(R_s + \dfrac{g_{m1} L_s}{C_{gs}} + \dfrac{\omega_0^2 L_g^2}{R_{fm}} \right)} \tag{4.2}$$

, where Q_{in} is the effective Q value for the input network of Low Noise Amplifier (LNA). The power spectral density (PSD, $S_x(f)$) of voltage for the source resistance R_s is equal to

$$\frac{\overline{V_s^2}}{\Delta f} = 4kTR_s \tag{4.3}$$

Multiplying this PSD by the square modulus of the trans-conductance (G_m), we

obtain the first component of the output noise power density due to the 50Ω source is

$$S_{out,R_s}(\omega_0) = S_{R_s}(\omega_0)G_{m,eff}^2$$

$$= 4kTR_s \left[g_{m1} \frac{1}{\omega_0 C_{gs}\left(R_s + \dfrac{g_{m1}L_s}{C_{gs}} + \dfrac{\omega_0^2 L_g^2}{R_{fm}} \right)} \right]^2 \tag{4.4}$$

$$= \frac{4kTg_{m1}^2}{\omega_0^2 C_{gs}^2 R_s \left(1 + \dfrac{g_{m1}L_s}{R_s C_{gs}} + \dfrac{\omega_0^2 L_g^2}{R_s R_{fm}} \right)^2}$$

From Figure 4.5, the output noise power spectral density (PSD) for the resistances R_l, R_g, and R_{fm} can be written as

$$S_{out,R_l,R_g,R_{fm}}(\omega_0) = S_{R_l,R_g,R_{fm}}(\omega_0)G_{m,eff}^2 = 4kT((R_l + R_g) // R_{fm} + R_g)G_{m,eff}^2$$

$$= 4kT((R_l + R_g) // R_{fm} + R_g) \left[g_{m1} \frac{1}{\omega_0 C_{gs}\left(R_s + \dfrac{g_{m1}L_s}{C_{gs}} + \dfrac{\omega_0^2 L_g^2}{R_{fm}} \right)} \right]^2 \tag{4.5}$$

$$= \frac{4kT((R_l + R_g) // R_{fm} + R_g)g_{m1}^2}{\omega_0^2 C_{gs}^2 R_s^2 \left(1 + \dfrac{g_{m1}L_s}{R_s C_{gs}} + \dfrac{\omega_0^2 L_g^2}{R_s R_{fm}} \right)^2}$$

The dominant noise contributor internal to the LNA is the channel current noise of the first MOS device. The output noise power density from this source is

$$S_{out,i_d}(\omega_0) = \frac{\dfrac{\overline{i_d^2}}{\Delta f}}{\left(1 + \dfrac{g_{m1}L_s}{R_s C_{gs}} \right)^2} = \frac{4kT\gamma g_{d0}}{\left(1 + \dfrac{g_{m1}L_s}{R_s C_{gs}} \right)^2} \tag{4.6}$$

The combined effect of the drain noise and the correlated portion of the gate noise is

$$S_{out,i_d,i_g,c}(\omega_0) = \kappa S_{out,i_d}(\omega_0) = \frac{\kappa 4kT\gamma g_{d0}}{\left(1 + \dfrac{g_{m1}L_s}{R_s C_{gs}}\right)^2} \tag{4.7}$$

, where

$$\kappa = \frac{\varsigma\alpha^2}{5\gamma}|c|^2 + \left(1 + |c|Q_L\sqrt{\frac{\varsigma\alpha^2}{5\gamma}}\right)^2 \tag{4.8}$$

$$Q_L = \frac{\omega_0 L_g \left(R_{fm}^2 + \omega_0^2 L_s^2\right) + R_{fm}^2 \omega_0 L_s}{R_s \left(R_{fm}^2 + \omega_0^2 L_s^2\right) + \omega_0^2 L_s^2 R_{fm}} \tag{4.9}$$

The last noise term is the drain noise and the uncorrelated portion of the gate noise. Its can be written as:

$$S_{out,i_d,i_g,u}(\omega_0) = \xi S_{out,i_d}(\omega_0) = \frac{\xi 4kT\gamma g_{d0}}{\left(1 + \dfrac{g_{m1}L_s}{R_s C_{gs}}\right)^2} \tag{4.10}$$

, where

$$\xi = \frac{\varsigma\alpha^2}{5\gamma}(1 - |c|^2)(1 + Q_L^2) \tag{4.11}$$

The total noise contribution of M_1 is

$$S_{out,M_1}(\omega_0) = (\kappa + \xi)S_{out,i_d}(\omega_0) = \frac{(\kappa + \xi)4kT\gamma g_{d0}}{\left(1 + \dfrac{g_{m1}L_s}{R_s C_{gs}}\right)^2} \tag{4.12}$$

The total output noise power density of the LNA is the sum of (4.4),(4.5),(4.12). We can express noise factor (F) as:

$$F \triangleq \frac{Total\ output\ noise}{Total\ output\ noise\ due\ to\ the\ source} = \frac{(4.4)+(4.5)+(4.12)}{(4.4)} \tag{4.13}$$

$$F = 1 + \frac{R_g}{R_s} + \frac{R_{fm}(R_l + R_g)}{R_s(R_l + R_g + R_{fm})}$$
$$+ \frac{\omega_0 g_{m1}}{C_{gs}} \left[\frac{\gamma}{\alpha Q_L} + 2|c| \sqrt{\frac{\varsigma\gamma}{5}} + \frac{\varsigma\gamma}{5} \left(\frac{1}{Q_L} + Q_L \right) \right] (1 + \frac{C_{gs}\omega_0^2 L_g^2}{g_{m1}R_{fm}R_s L_s}) \tag{4.14}$$

, where $\dfrac{C_{gs}\omega_0^2 L_g^2}{g_{m1}R_{fm}R_s L_s} \ll 1$, Noise Factor (F) can be determined as

$$F \approx 1 + \frac{R_g}{R_s} + \frac{R_{fm}(R_l + R_g)}{R_s(R_l + R_g + R_{fm})}$$
$$+ \frac{\omega_0 g_{m1}}{C_{gs}} \left[\frac{\gamma}{\alpha Q_L} + 2|c| \sqrt{\frac{\varsigma\gamma}{5}} + \frac{\varsigma\gamma}{5} \left(\frac{1}{Q_L} + Q_L \right) \right] \tag{4.15}$$

$$Noise\ Figure\ (dB) = 10 * log(F) \tag{4.16}$$

To validate our derivation, comparison between the formulated and simulated Noise Figures of the input stage is shown in Figure 4.6. The comparison shows that Noise Figure (formulate and simulated) of the proposed Ultra wideband Low Noise Amplifier with feedback resistor R_f=1000Ω and compares that of the amplifier without feedback resistor R_f can be predicted well by using equation (4.15).

The addition of feedback resistor R_f increase the values of the Noise Figure (Figure 4.6), but also increase bandwidth for proposed Low Noise Amplifier (Figure 4.2). The Noise Figure is plotted in Figure 4.7 for the five cases of power dissipation. It is clear that the optimum QL for a fixed power dissipation.
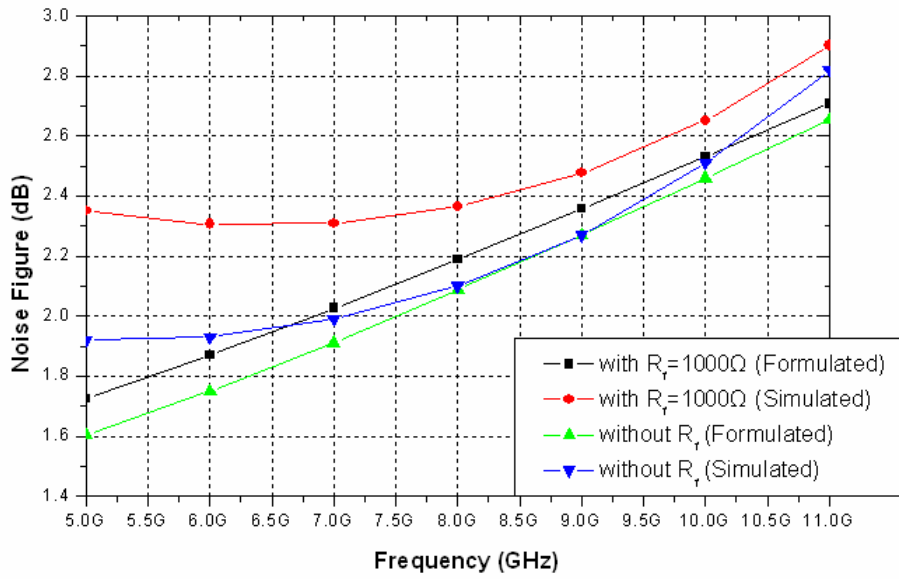
Figure 4.6 Noise Figure versus Frequency (Formulated and Simulated)
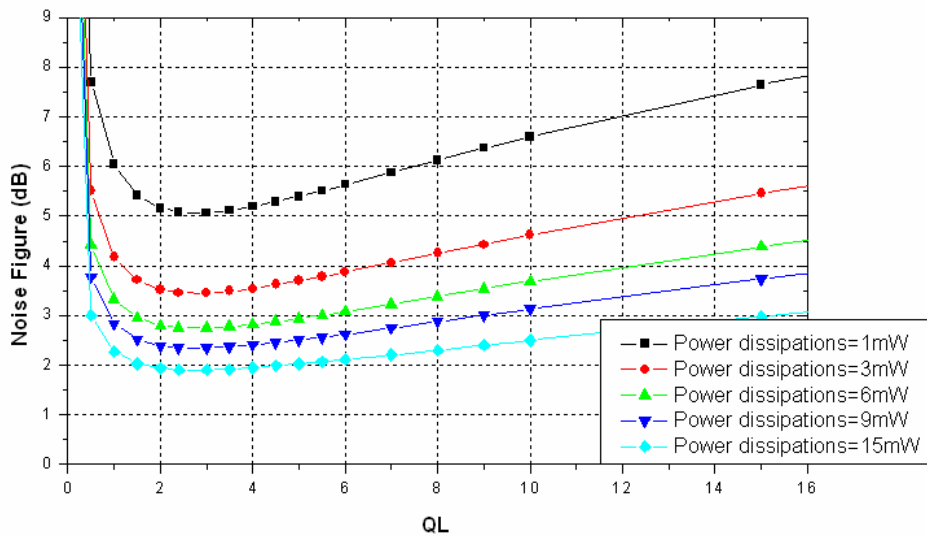
Figure 4.7 Theoretical predictions of Noise Figure for several power dissipations.

4.2.3 A novel method to reduce LNA Noise Figure

In this section, a noise-reduction method using Source-Body Resistance (R_{sb}) technique is proposed. It is found that the method can effectively reduce the noise figure of the proposed Ultra-wideband LNA.

a. Substrate thermal noise reduced by adding an external resistance

In CMOS technology, the substrate parasitic impedance can induce the substrate thermal noise of RFIC circuits due to the leaky current through the drain/source to the substrate. Here, a simple method by adding an external resistance between the source and the body is proposed to reduce the thermal noise. To explore the method, a small signal equivalent circuit model of the substrate with an added resistor is developed and is shown in Figure 4.8.
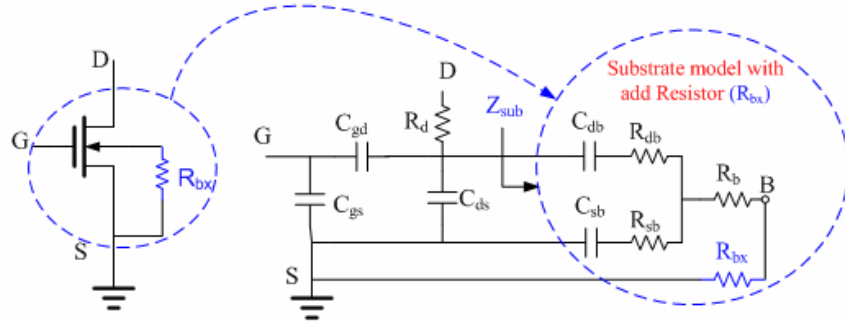
Figure 4.8 Equivalent circuit model of the substrate with an added resistor R_{bx}, which is located between the body node and the source node of transistor, and R_b, R_{sb}, R_{db} represent the effective substrate model.

The input impedance of the substrate, Z_{sub} is derived and given as:

$$Z_{sub} = R_{bd} + \frac{1}{j\omega_0 C_{bd}} + \left[(R_b + R_{bx}) // (R_{sb} + \frac{1}{j\omega_0 C_{sb}}) \right] \tag{4.17}$$

Let $Z_{sub} \triangleq R_{sub} + \dfrac{1}{j\omega_0 C_{sub}}$ and $R_{bx} \gg R_b, R_{bx} \gg R_{sb},$

$$R_{sub} \approx R_{bd} + \frac{1}{\omega_0^2 (R_b + R_{bx}) C_{sb}^2}, \quad C_{sub} \approx \frac{C_{sb} C_{bd}}{C_{sb} + C_{bd}} \tag{4.18}$$

From equation (4.18), increase of the added resistance, R_{bx} leads to a reduction of the equivalent substrate resistance R_{sub}, which validates our proposed method.

In this section, the proposed method is applied to UWB LNA to validate its effectiveness. Figure 4.9 illustrates the proposed UWB LNA architecture with an external resistance R_{bx} added to the transistor M_1. To explore the noise figure of the LNA, the noise factor is derived first and is equal to the ratio between the input noise power and the output noise power of the circuit.

According to the proposed UWB LNA and using the substrate model shown in Figure 4.9. Its shows that the small-signal equivalent circuit for substrate model with add resistor (R_{bx}). The resistor R_{bx} is an additional resistor which is connected between the body node and source node of transistor M_1. Resistor R_{bx} helps to improve the high frequency performance of the LNA noise figure.
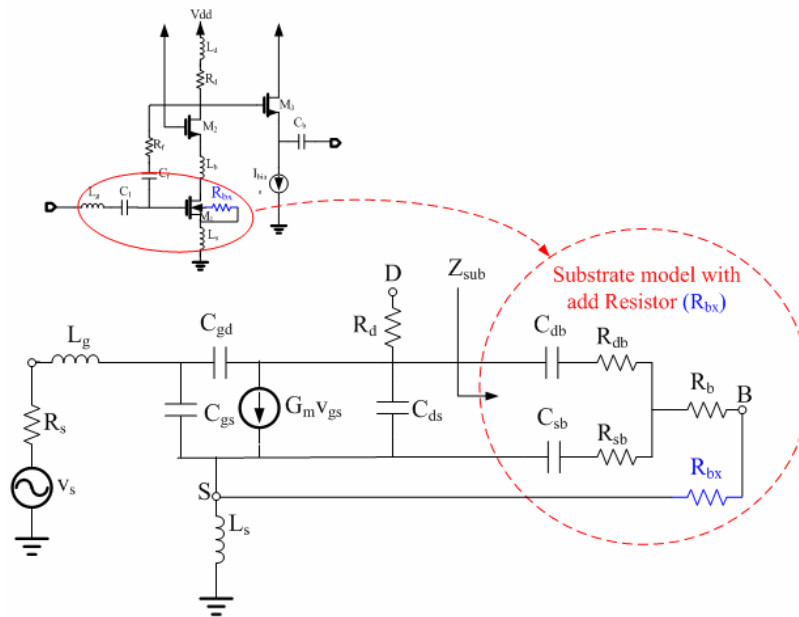
Figure 4.9   The small-signal equivalent circuit for substrate model with add resistor (R_{bx})

b. Substrate noise analysis and simulation

From Figure 4.10 noise model to derive the noise factor of the Low Noise

Amplifier. Here we will derive the noise figure according to small signal model. To obtain the expression for noise figure, it is instructive to calculate the transfer functions of the input/output noise sources in the LNA. The small signal equivalent circuit used in the computation is shown in Figure 4.10, and Z_{sub} represents simplified the substrate parasitic impedance noise from the substrate model (Figure 4.9).
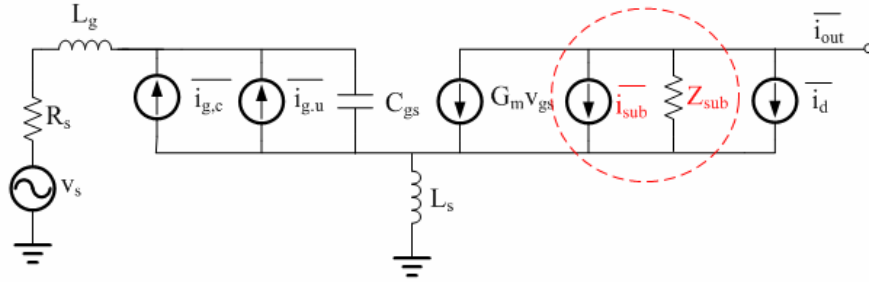
Figure 4.10 Noise equivalent circuit for LNA with substrate noise

$$V_{gs} = \frac{\overline{i_{out}} - \overline{i_d} - \overline{i_{sub}}}{G_m} \tag{4.17}$$

$$V_s = \frac{\overline{i_{out}} - \overline{i_d} - \overline{i_{sub}}}{G_m} + \left[\left(\frac{\overline{i_{out}} - \overline{i_d} - \overline{i_{sub}}}{G_m} \right) j\omega C_{gs} - \overline{i_g} \right] \left(R_s + j\omega L_g + j\omega L_s \right) + \overline{i_{out}} j\omega L_s \tag{4.18}$$

$$\text{Let} \quad A = \left(R_s + j\omega L_g + j\omega L_s \right) \qquad R_s = R_g + \frac{G_m L_s}{C_{gs}} \tag{4.19}$$

Using (4.19) to replace (4.18) can be written as

$$\overline{i_{out}} = \frac{\overline{V_s} + \overline{i_d}\left[\dfrac{1}{G_m} + \dfrac{1}{G_m} j\omega C_{gs} A \right] + \overline{i_g} A + \overline{i_{sub}}\left[\dfrac{1}{G_m} + \dfrac{1}{G_m} j\omega C_{gs} A \right]}{\dfrac{1}{G_m} + \dfrac{1}{G_m} j\omega C_{gs} A + j\omega L_s} \tag{4.20}$$

Because $\omega(L_g + L_s) = \dfrac{1}{\omega C_{gs}}$, so the total output noise (4.20) can be written

$$\overline{i_{out}} = \frac{\overline{V_s} + (\frac{jR_s\omega C_{gs}}{G_m})\overline{i_d} + (R_s + j\frac{1}{\omega C_{gs}})\overline{i_g} + (\frac{jR_s\omega C_{gs}}{G_m})\overline{i_{sub}}}{\frac{jR_s\omega C_{gs}}{G_m} + j\omega L_s} \tag{4.21}$$

According to the definition, noise factor is

$$F = \frac{\overline{i_{out}^2}\{all-sources\}}{\overline{i_{out}^2}\{R_s-only-sources\}} = \frac{\overline{i_{out}*i_{out}^*}}{\overline{V_s*V_s^*}} \tag{4.22}$$

$$F = 1 + (\frac{R_s\omega C_{gs}}{G_m})^2\frac{\overline{i_d^2}}{V_s^2} + R_s^2(1+\frac{1}{R_s^2\omega^2 C_{gs}^2})\frac{\overline{i_g^2}}{V_s^2} + (\frac{R_s\omega C_{gs}}{G_m})^2\frac{\overline{i_{sub}^2}}{V_s^2}$$

$$+(\frac{jR_s\omega C_{gs}}{G_m})(R_s - j\frac{R_s}{R_s\omega C_{gs}})\frac{\overline{i_d*i_g^*}}{V_s^2} + (R_s + j\frac{R_s}{R_s\omega C_{gs}})(\frac{-jR_s\omega C_{gs}}{G_m})\frac{\overline{i_g*i_d^*}}{V_s^2}$$

$$+(\frac{jR_s\omega C_{gs}}{G_m})(\frac{-jR_s\omega C_{gs}}{G_m})\frac{\overline{i_d*i_{sub}^*}}{V_s^2} + (\frac{jR_s\omega C_{gs}}{G_m})(\frac{-jR_s\omega C_{gs}}{G_m})\frac{\overline{i_{sub}*i_d^*}}{V_s^2} \tag{4.23}$$

$$+(R_s + j\frac{R_s}{R_s\omega C_{gs}})(\frac{-jR_s\omega C_{gs}}{G_m})\frac{\overline{i_g*i_{sub}^*}}{V_s^2} + (\frac{jR_s\omega C_{gs}}{G_m})(R_s - j\frac{R_s}{R_s\omega C_{gs}})\frac{\overline{i_{sub}*i_g^*}}{V_s^2}$$

, where

$$Q_s = \frac{1}{R_s\omega_0 C_{gs}} \qquad C_{gs} = \frac{2}{3}C_{ox}WL \tag{4.24}$$

Using (4.24) to replace (4.23) can be written

$$F = 1 + \frac{1}{Q_s^2 G_m^2}\frac{\overline{i_d^2}}{V_s^2} + R_s^2(1+Q_s^2)\frac{\overline{i_g^2}}{V_s^2} + \frac{1}{Q_s^2 G_m^2}\frac{\overline{i_{sub}^2}}{V_s^2}$$

$$+(\frac{j}{Q_s G_m})(R_s - jR_sQ_s)\frac{\overline{i_d*i_g^*}}{V_s^2} + (\frac{j}{Q_s G_m})(\frac{-j}{Q_s G_m})\frac{\overline{i_d*i_{sub}^*}}{V_s^2}$$

$$+(\frac{-j}{Q_s G_m})(R_s + jR_sQ_s)\frac{\overline{i_g*i_d^*}}{V_s^2} + (R_s + jR_sQ_s)(\frac{-j}{Q_s G_m})\frac{\overline{i_g*i_{sub}^*}}{V_s^2} \tag{4.25}$$

$$+(\frac{j}{Q_s G_m})(\frac{-j}{Q_s G_m})\frac{\overline{i_{sub}*i_d^*}}{V_s^2} + (\frac{j}{Q_s G_m})(R_s - jR_sQ_s)\frac{\overline{i_{sub}*i_g^*}}{V_s^2}$$

, where

$$\frac{\overline{i_d^2}}{V_s^2} = \frac{4kT\gamma g_{d0}}{4kTR_s} \tag{4.26}$$

$$\frac{\overline{i_g^2}}{V_s^2} = \frac{4kT\delta\omega^2 C_{gs}^2}{5g_{d0}} \frac{1}{4kTR_s} \tag{4.27}$$

$$\frac{\overline{i_{sub}^2}}{V_s^2} = \frac{4kT(G_m Z_{sub})^2}{Z_{sub} 4kTR_s} \tag{4.28}$$

$$\frac{\overline{i_d * i_g^*}}{V_s^2} = C \frac{1}{4kTR_s} \sqrt{4kT\gamma g_{d0} \frac{4kT\delta\omega^2 C_{gs}^2}{5g_{d0}}} \tag{4.29}$$

$$\frac{\overline{i_d * i_{sub}^*}}{V_s^2} = C_1 \frac{1}{4kTR_s} \sqrt{4kT\gamma g_{d0} 4kTG_m^2 Z_{sub}} \tag{4.30}$$

$$\frac{\overline{i_g * i_{sub}^*}}{V_s^2} = C_2 \frac{1}{4kTR_s} \sqrt{\frac{4kT\delta\omega^2 C_{gs}^2}{5g_{d0}} 4kTG_m^2 Z_{sub}} \tag{4.31}$$

Using (4.26) (4.27) (4.28) (4.29) (4.30) (4.31) to replace (4.25) can be written

$$
\begin{aligned}
F = 1 &+ \frac{1}{Q_s^2 G_m^2} \frac{\gamma g_{d0}}{R_s} + \left(\frac{1+Q_s^2}{Q_s^2}\right) \frac{\delta}{5g_{d0}R_s} + \frac{Z_{sub}}{Q_s^2 R_s} \\
&+ 2|C|\sqrt{\frac{\delta\gamma}{5}} \frac{1}{Q_s^2 G_m R_s} + 2|C_2|\sqrt{\frac{\delta Z_{sub}}{5g_{d0}}} \frac{1}{Q_s^2 R_s}
\end{aligned}
\tag{4.32}
$$

, where $\quad g_{d0}Q_s = \dfrac{\omega_T}{\alpha\omega_0 R_s} \qquad \alpha \triangleq \dfrac{G_m}{g_{d0}}$ $\qquad$ (4.33)

Using (4.33) to replace (4.32) can be written

$$F = 1 + \frac{\gamma}{Q_s \alpha}\left(\frac{\omega_0}{\omega_T}\right) + \left(\frac{1+Q_s^2}{Q_s^2}\right)\frac{\delta\alpha}{5}\left(\frac{\omega_0}{\omega_T}\right) + \frac{Z_{sub}}{Q_s^2 R_s}$$
$$+ 2|C|\frac{1}{Q_s}\sqrt{\frac{\delta\gamma}{5}}\left(\frac{\omega_0}{\omega_T}\right) + 2|C_2|\frac{1}{Q_s}\sqrt{\frac{\delta\alpha G_m}{5}Z_{sub}}\left(\frac{\omega_0}{\omega_T}\right)$$

(4.34)

, where $Q_s = \dfrac{1}{R_s\omega_0 C_{gs}}$, α, γ, δ, and C are process parameters [1], and ω_0 is center frequency, ω_T is cutoff frequency. C_2 is gate noise and substrate noise correction coefficients. Equation (4.34) is derived to explain why increasing resistance Z_{sub} leads to a increasing of low noise amplifier noise factor. Determination of substrate resistance value R_{bx} is important. In Figure 4.11 shows that the curve becomes gentle after $R_{bx=}10k\Omega$, the values of substrate resistance $R_{bx} = 10k\Omega$ are employed to proposed low noise amplifier.
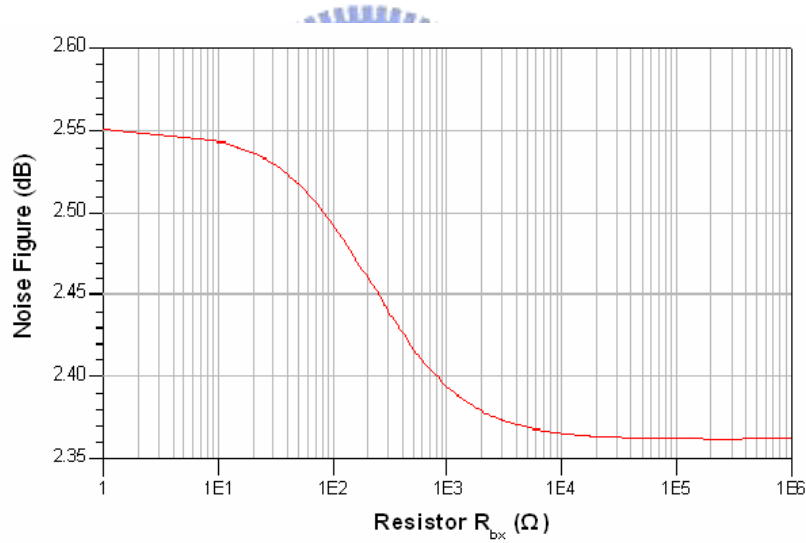
Figure 4.11 Noise Figure versus Resistor R_{bx}

4.2.4 Simulation results

A low supply voltage of 1.5V is chosen, and the total power consumption is 9.0mW. In Figure 4.12, S11, S12, S21, and S22 versus signal frequency are illustrated. It is found that the input reflection S11 < -11.72dB and output matching S22<-14.61dB in the range of 6~10.6 GHz. The power gain (S21) is around 12.0~14.4dB. The noise

figure of the proposed LNA is shown in Figure 4.13. It shows that the noise figure (NF) is smaller when R_{bx}=10kΩ to compare with the case without R_{bx}. The simulation results also show that the input third-order-intercept points (IIP3s) are -7.0dBm at 6GHz, -7.5dBm at 8GHz, -4.5dBm at 10GHz.
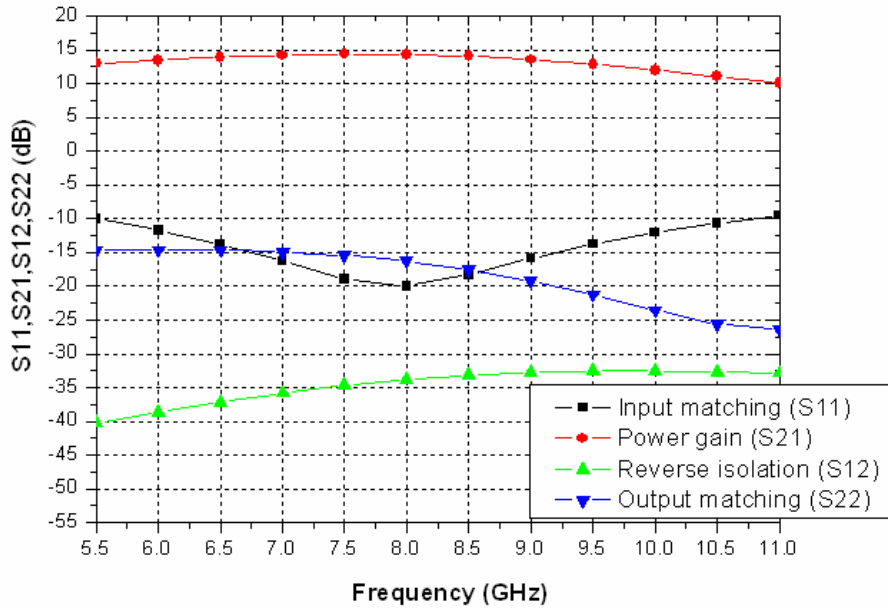
Figure 4.12　　S-parameters versus signal frequency
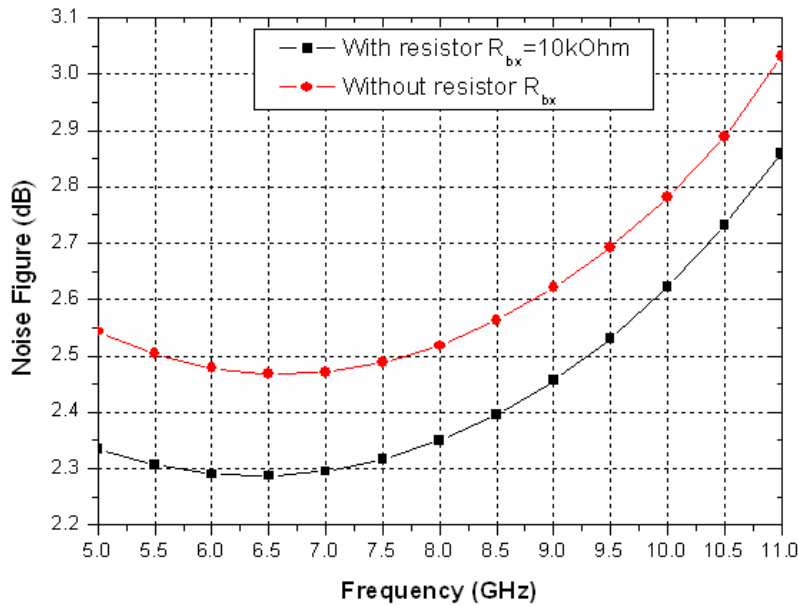
Figure 4.13　　Noise Figure versus signal frequency with R_{bx}=10kΩ to compare with

the case without R_{bx}
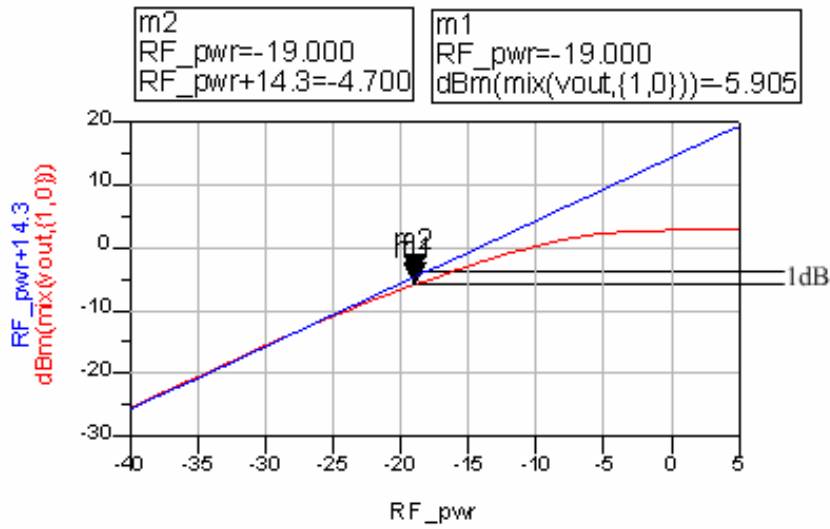
Figure 4.14 Linearity parameters P_{1dB} at 6GHz

Linearity parameters P_{1dB} can be explained by Figure 4.21.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm)=14.3+(-19)=-4.7dBm$

Simulation results of $P_{1dB}=-3.3dBm$.
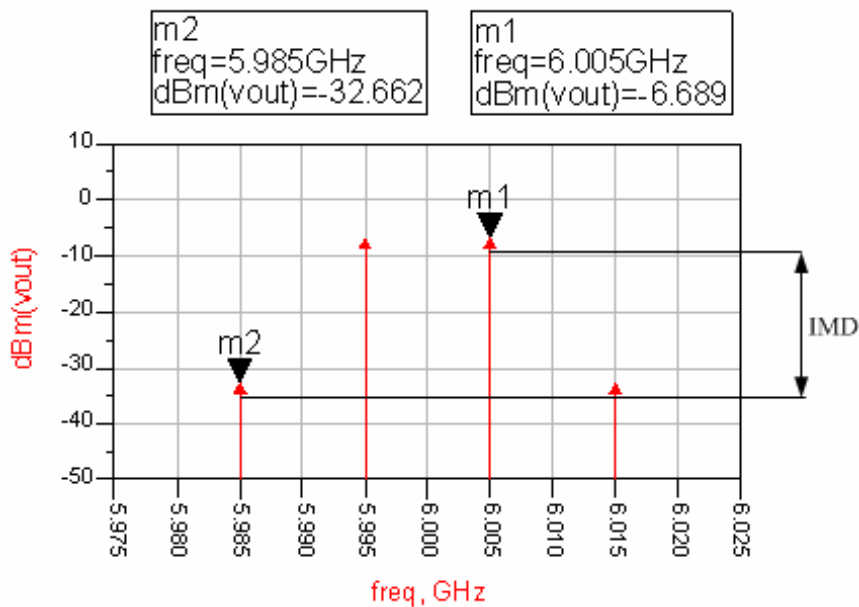
Figure 4.15 Linearity parameters OIP3 at 6GHz

Linearity parameters OIP3 can be explained by Figure 4.22.

$OIP3=P_{out}+\dfrac{1}{2}IMD=-6.689+\dfrac{1}{2}(32.662-6.689)=6.3dBm$
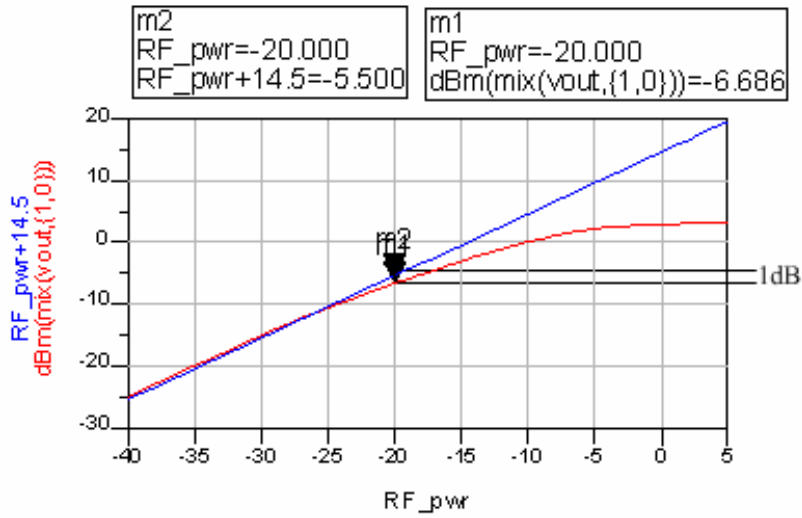
Figure 4.16 Linearity parameters P$_{1dB}$ at 7GHz

Linearity parameters P$_{1dB}$ can be explained by Figure 4.21.

P$_{1dB}$=P$_{1dB}$(dBm)=G$_{1dB}$(dB)+IP$_{1dB}$(RF_pwr)(dBm) =14.5+(-20)=-5.5dBm

Simulation results of P$_{1dB}$=-6.6dBm.
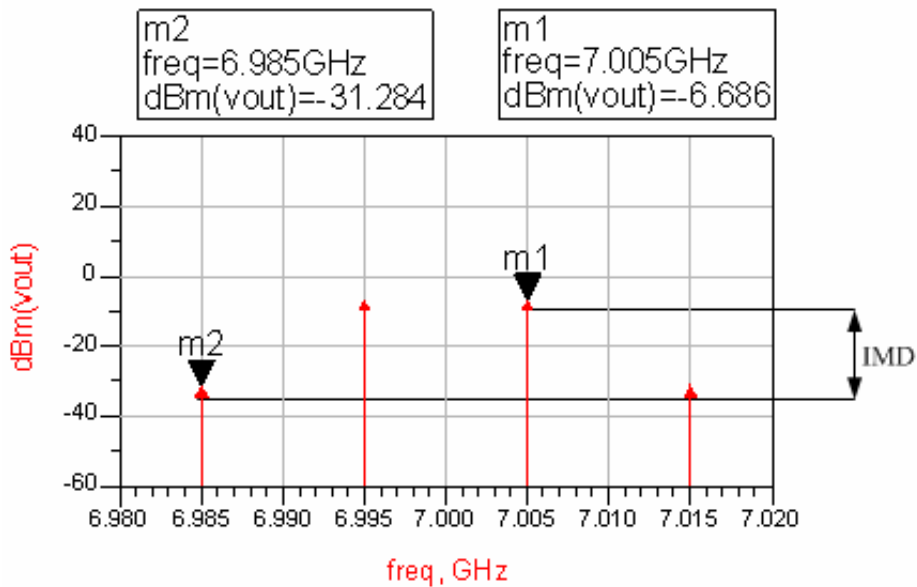
Figure 4.17 Linearity parameters OIP3 at 6GHz

Linearity parameters OIP3 can be explained by Figure 4.22.

OIP3=P$_{out}$+$\frac{1}{2}$IMD=-6.686+$\frac{1}{2}$(31.284-6.686)=5.7dBm
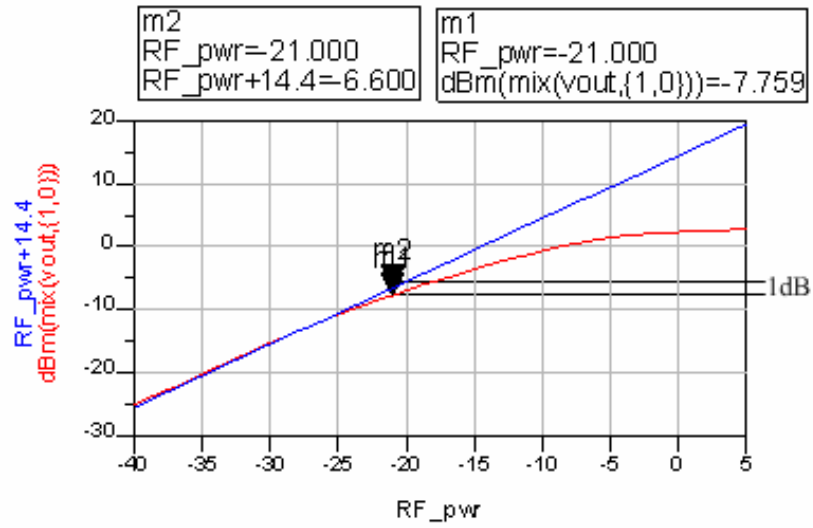
Figure 4.18 Linearity parameters P_{1dB} at 8GHz

Linearity parameters P_{1dB} can be explained by Figure 4.21.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm)=14.4+(-21)=-6.6dBm$

Simulation results of $P_{1dB}=-7.7dBm$.
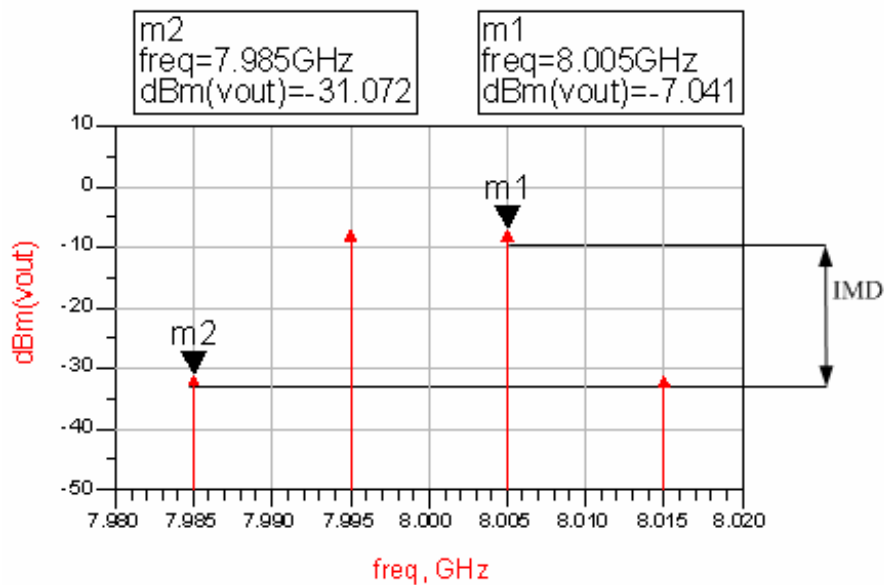
Figure 4.19 Linearity parameters OIP3 at 8GHz

Linearity parameters OIP3 can be explained by Figure 4.22.

$OIP3=P_{out}+\dfrac{1}{2}IMD=-7.041+\dfrac{1}{2}(31.072-7.04)=5dBm$
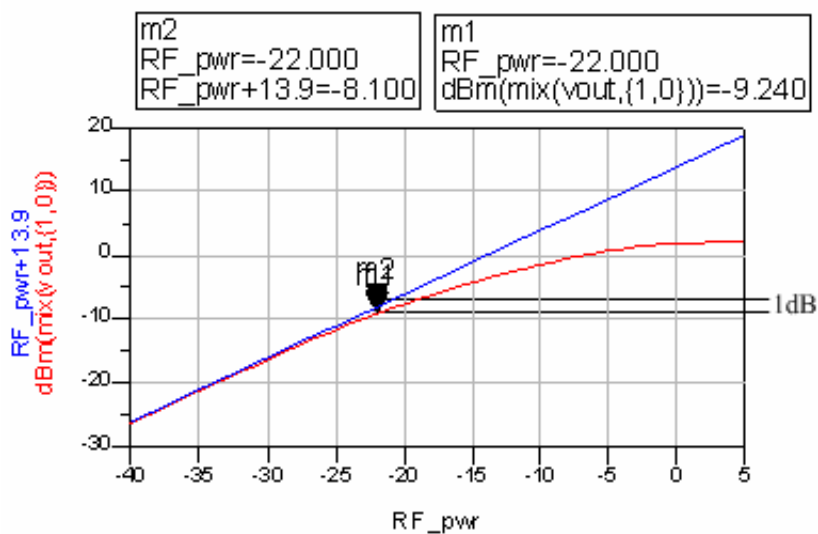
Figure 4.20 Linearity parameters P_{1dB} at 9GHz

Linearity parameters P_{1dB} can be explained by Figure 4.21.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm) =13.9+(-22)=-8.1dBm$

Simulation results of $P_{1dB}=$-9.2dBm.
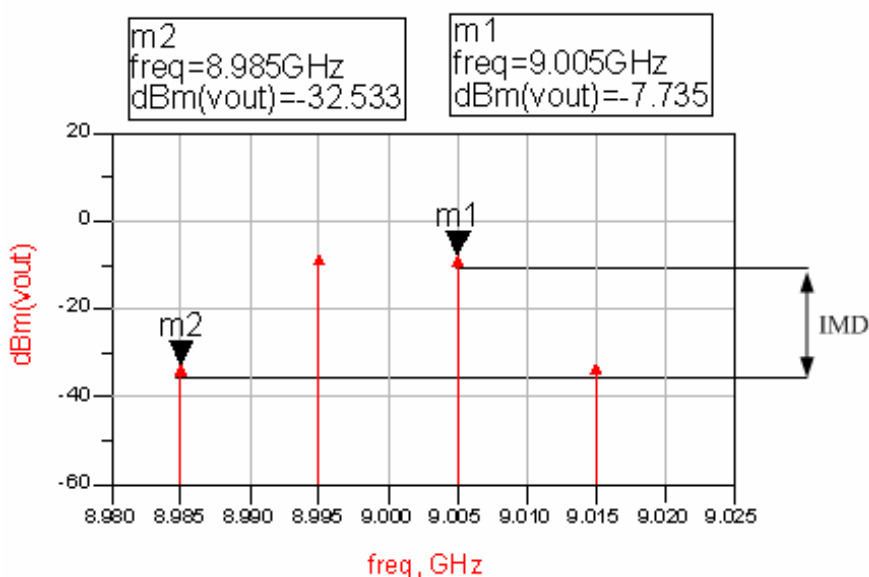
Figure 4.21 Linearity parameters OIP3 at 9GHz

Linearity parameters OIP3 can be explained by Figure 4.22.

$OIP3=P_{out}+\dfrac{1}{2}IMD=-7.7353+\dfrac{1}{2}(32.533-7.735)=4.7dBm$
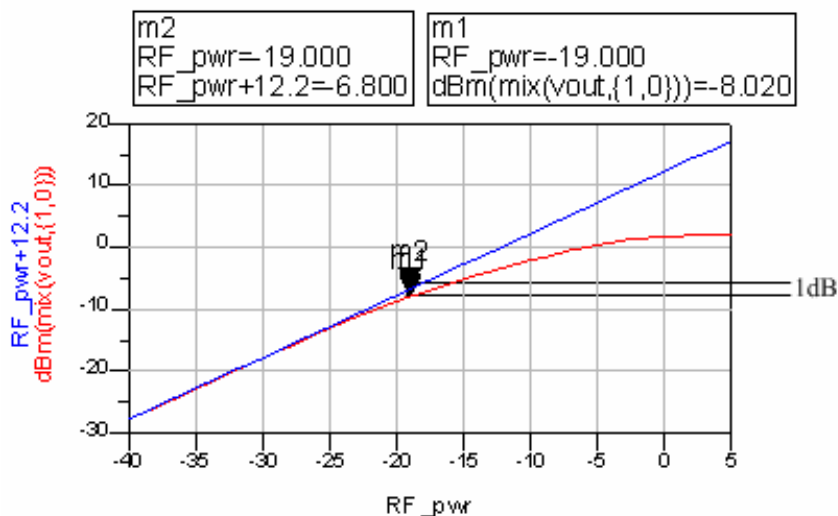
Figure 4.22 Linearity parameters P_{1dB} at 10GHz

Linearity parameters P_{1dB} can be explained by Figure 4.21.

$P_{1dB}=P_{1dB}(dBm)=G_{1dB}(dB)+IP_{1dB}(RF\_pwr)(dBm)=12.2+(-19)=-6.8dBm$

Simulation results of $P_{1dB}=-8dBm$.
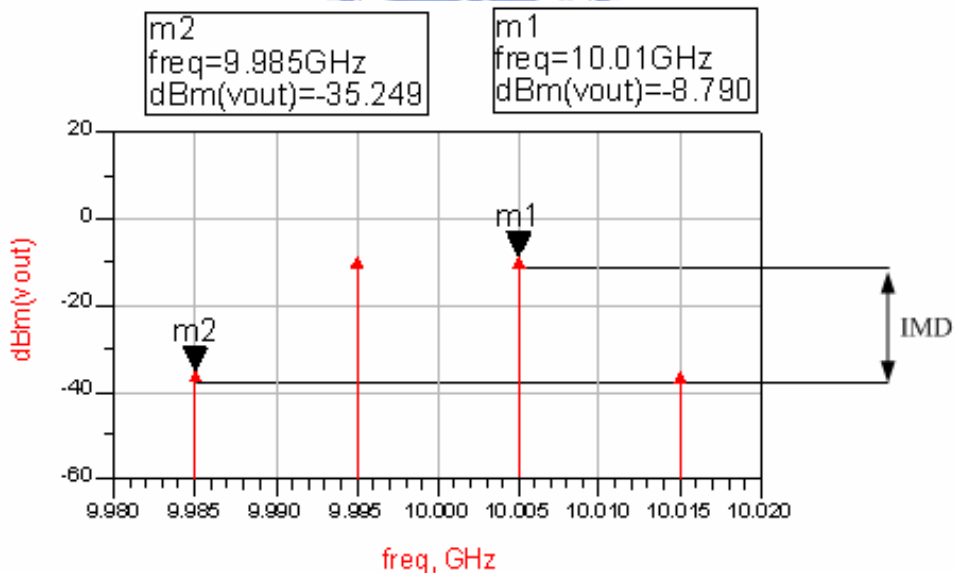
Figure 4.23 Linearity parameters OIP3 at 10GHz

Linearity parameters OIP3 can be explained by Figure 4.22.

$OIP3=P_{out}+\dfrac{1}{2}IMD=-8.79+\dfrac{1}{2}(35.249-8.79)=3dBm$

4.3 Proposed UWB LNA with low voltage design

In this section, a very low-voltage UWB LNA is achieved by reducing transistor's threshold voltage using an external bias to the transistor body node. Here, our proposed UWB LNA not only achieves low voltage requirement but also takes care of other issues.

4.3.1 Threshold Voltage

The threshold voltage of a MOS transistor is calculated for circuit analysis:

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}),$$ (4.35)

where V_{th0} is the value of V_{th} with V_{BS}=0, γ is the body effect coefficient, and Φ_F is the strong inversion surface potential of the transistors. In Figure 4.24 shows that a V_{GS}> V_{th} will be turn on NMOS transistor.
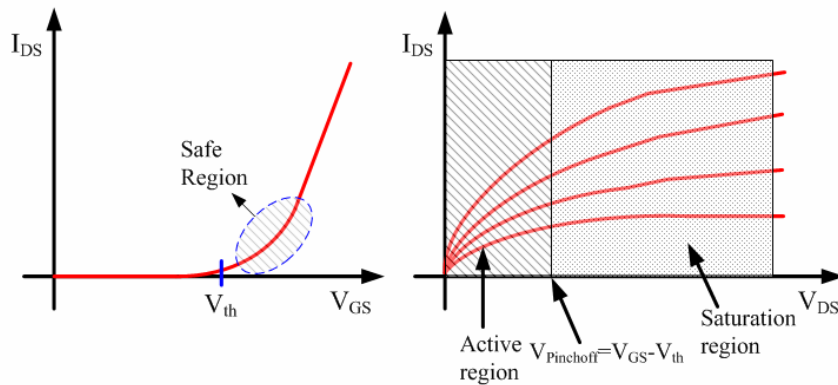
Figure 4.24 NMOS I/V characteristic

In Figure 4.25 (a), if a MOSFET is off (in depletion region), we actually have to apply a $V_{GS}<V_{th}$ to turn off the NMOS. If a MOSFET is on (in strong inversion region or saturation region), we actually have to apply a $V_{GS} \geq V_{th}$ to turn on the NMOS and will generation of conduction channels as shown in Figure 4.25 (b).
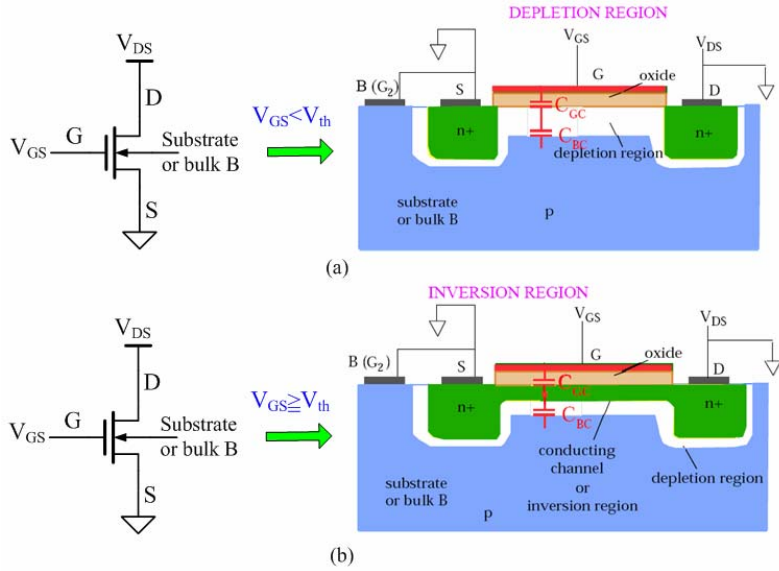
Figure 4.25 Depletion region and Inversion region (saturation region) with (a) $V_{GS}<V_{th}$,

(b) $V_{GS} \geq V_{th}$ of NMOS transistors
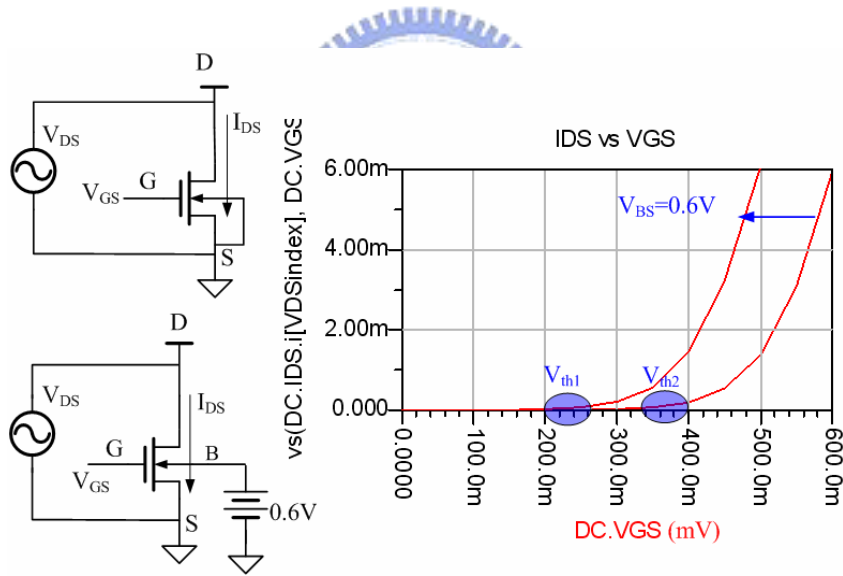
Figure 4.26 VGS (min V_{th}) with or without V_{BS}

Figure 4.26 illustrates the threshold voltage is decreased as the external bias V_{BS} is increased (V_{th1} is with external bias V_{BS}=0.6V and V_{th2} is without external bias V_{BS}). From equation (4.35), it is found that the threshold voltage is decreased as the bias V_{BS} is increased as shown in Figure 4.27. To reduce the threshold voltage as much as possible, we want to the bias V_{BS} as high as possible.
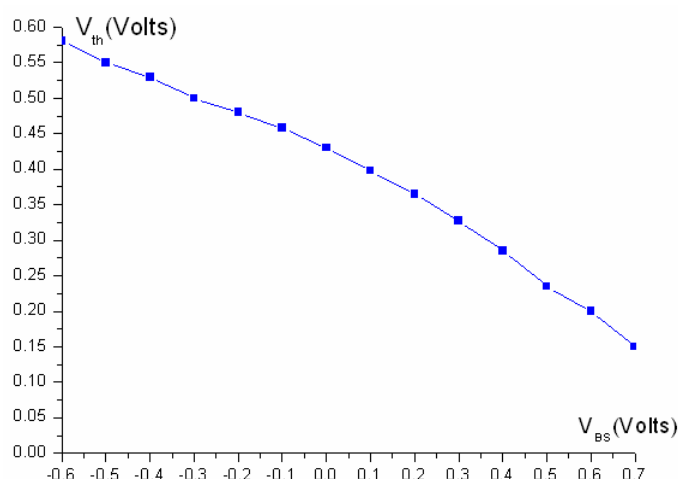
Figure 4.27 Threshold voltage V_{th} as a function of external bias V_{BS}

The cascode LNA architecture is widely used design, but requires a high supply voltage (>0.9V), which employs two transistors stacked. In Figure 4.28, the transistor M_1 and M_2 shows a device I-V curves without external bias V_{BS}. If fixed dc current 3mA, the supply voltage V_{DS} (V_{DD}) is varied between 0.9V and 1.8V with transistor working in the saturation region. Also in Figure 4.29, an external bias V_{BS}=0.6 voltage is employed to forward-bias the body-source junction of transistor M_1 and M_2. The supply voltage V_{DS} (V_{DD}) is varied between 0.65V and 1.8V with transistor working in the saturation region.
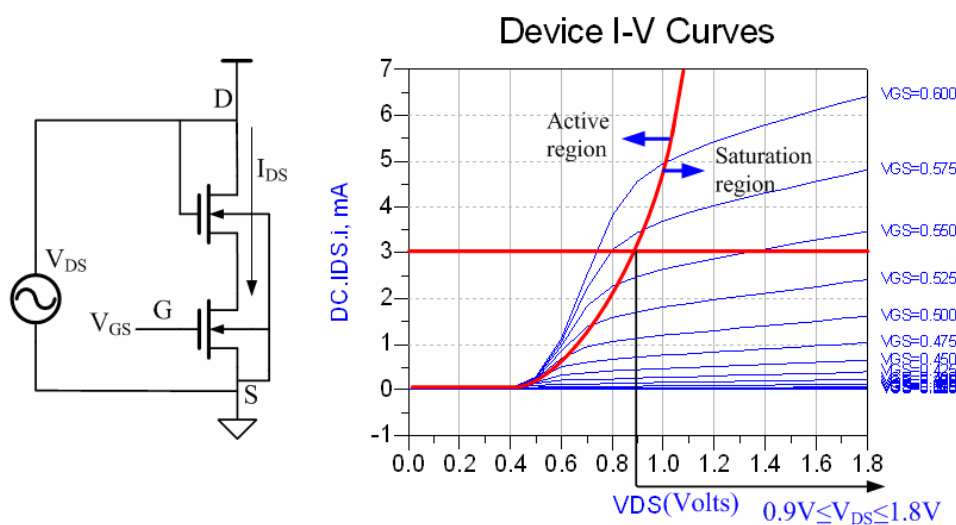
Figure 4.28 Device I-V Curves without external bias V_{BS}
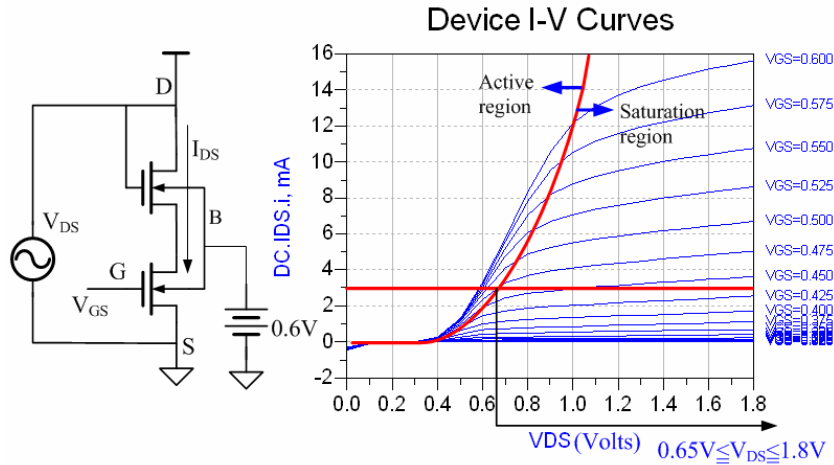
Figure 4.29 Device I-V Curves with external bias $V_{BS}=0.6$

Here the supply voltage is very low of 0.75V compare with others [1], [7], [8], [15] , [10] with dc current 3.8mA. In our design, an external bias is employed to the transistor body node as shown Fig.4.30, which leads to transistor's threshold voltage (V_{th}) reduction and supply voltage from 0.65V to 1.8V. The very low voltage design of the proposed UWB LNA is shown in Figure 4.30. A $V_{BS}=0.6$ voltage is employed to forward-bias the body-source junction of transistor M_1 and M_2. The supply voltage V_{DD} can be variation to between 0.65V and 1.8V with transistor working in saturation region. We chose the supply voltage 0.75V with dc current is 3.8mA and power consumption is 2.8mW.
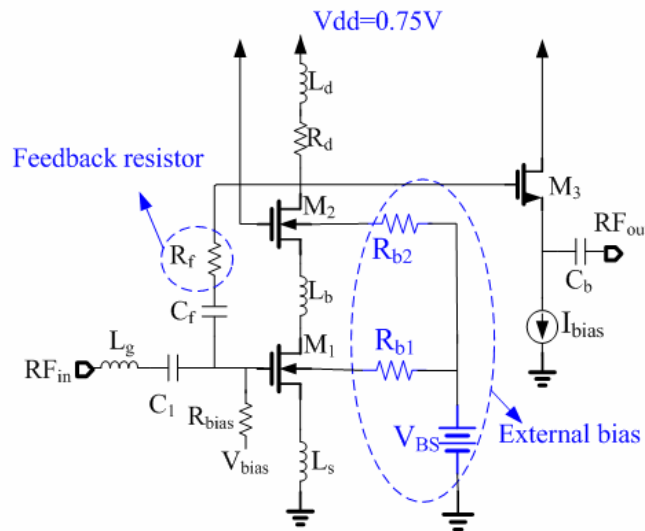
Figure 4.30 Proposed UWB LNA with Low voltage design.

4.3.2 Simulation results

In Figure 4.31, input matching S11, power gain S21, reverse isolation and output matching versus signal frequency are illustrated. The power gain S21 with proposed UWB LNA (V_{DD}=1.8V, Power=11.6mW) and proposed low voltage UWB LNA (V_{DD}=0.75V, Power=2.8mW) are small than -13.7dB in the range of 6.0~10.6 GHz as shown in Figure 4.32. The noise figure (NF) of proposed low voltage UWB LNA compare with proposed UWB LNA is shown in Figure 4.33. It is found that the noise figure is at least less than 3.6dB in 6.0~10.6GHz and its minimum value is 2.8dB at 7 GHz. The output third-order-intercept points (OIP3s) are 7.669dBm at 6GHz, 5.0dBm at 8GHz, 4.53dBm at 10GHz. The performance of the proposed UWB LNA with low voltage technique is summarized in Table 4.2, with comparison with other recently published UWB LNAs' simulation results.

Table 4.2
Summary of LNA performance and comparison with published LNAs

Ref.	Tech.	BW (GHz)	S11 (dB)	Gain (dB)	NF (dB)	VDD (V)	Power (mW)
[1]	0.18um CMOS	2.3-9.2	<-9.9	9.3	4.0	1.8	9.0
[7]	0.18um CMOS	2.6-9.2	<-11.5	10.9	3.5	1.8	7.1
[8]	0.18um SiGe	0.1-11	<-12	8	2.9	1.8	21.6
[15]	0.13um CMOS	7.2-8.6	<-9	28	3.9	1.5	3.9
[10]	0.18um CMOS	2-10.1	<9.76	10.2	3.68	1	7.2
Our work	0.18um CMOS	5-10.6	<-13.7	14	2.8	0.75	2.8
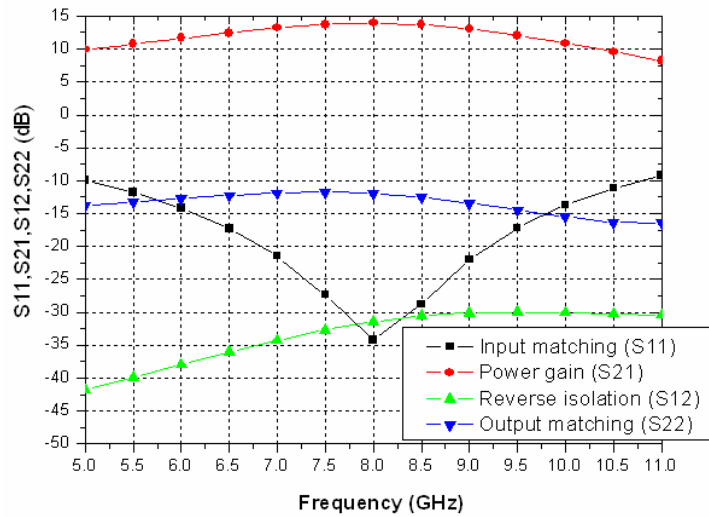
Figure 4.31 S-parameters versus signal frequency
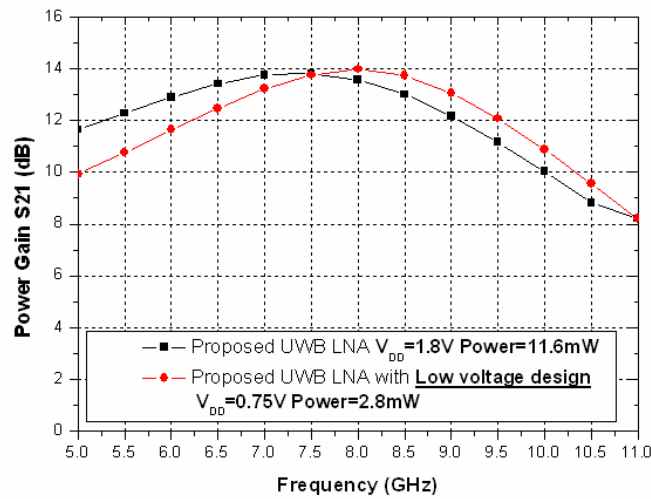
Figure 4.32 Power gain versus signal frequency with Low voltage design
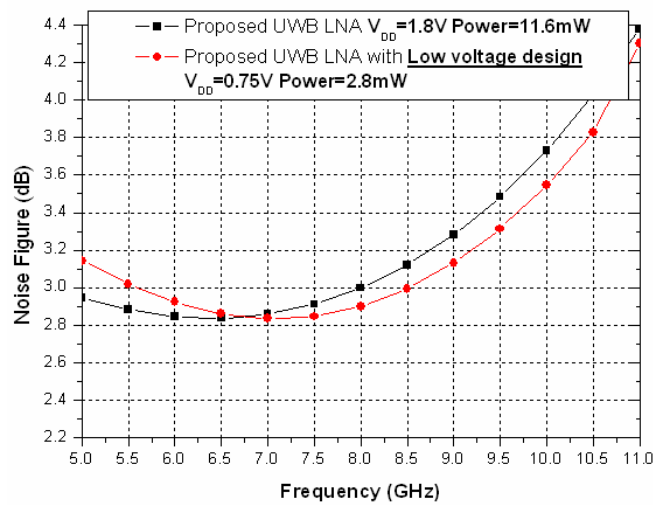
Figure 4.33 Noise figure versus signal frequency with or without Low voltage design

Chapter 5   *Conclusion*

In this thesis, low power UWB LNAs are designed by using two different approaches. The first topic propose the common gate combined with band pass filters for the input matching network can easily to reduce parasitic capacitance effects of the transistors and low power consumption. The πi-section LC network technique is also employed in the LNA to achieve a sufficient and flat gain. Numerical simulation based on TSMC 0.18μm 1P6M process. It achieved 10.0～12.4dB gain from 3 GHz to 10.6 GHz and 3.25dB noise figure in 8.5GHz, operates from 1.5V power supply, and dissipates 3mW

The second topic proposes an external bias to the body node of transistor, which leads to transistor's threshold voltage reduction and low power consumption. The proposes LNA combines a conventional LNA cascode architecture with a feedback resistor R_f, to achieve wideband input impedance matching. Based on TSMC 0.18μm 1P6M process, the numerical result shows that the LNA has 11.8～14.0dB gain from 6 GHz to 10.0 GHz with input matching S11<-13.7dB and 2.81dB noise figure in 7.0GHz. It only dissipates 2.8 mW with a very small power supply of 0.75V. Here, the second design

method can applied to low power UWB LNA to attain to under low power consumption

requirement.

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Appendix   *Basic Noise Theory*

There are two methods for analyzing the effect of noise in electronic devices and circuits [49]. The first method consists of using equivalent noise sources at the appropriate physical location in the small signal model of the device. For example, consider the noise produced by two resistors in series, as shown in Figure A.1 (a). Using the noise model of a resistor, the noise model shown in Figure A.1 (b) is obtained. The mean-square value of the open circuit voltage is

$$\overline{V_{noise,out}^2} = \overline{\left(V_{noise.1} + V_{noise,2} \right)^2} = \overline{V_{noise.1}^2} + 2\overline{V_{noise.1} * V_{noise,2}} + \overline{V_{noise,2}^2} \qquad (A.1)$$
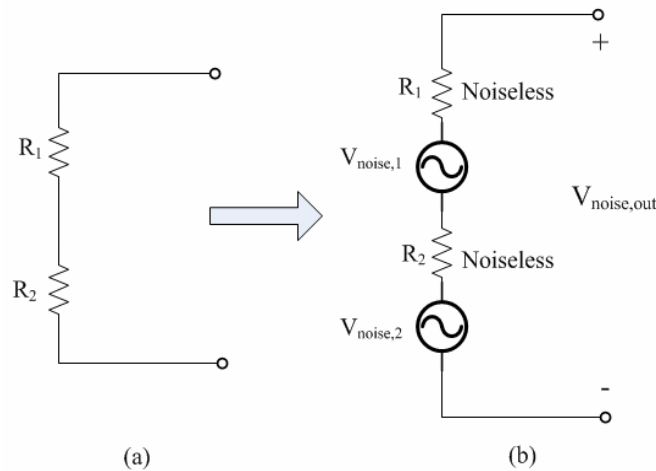
Figure A.1 The total noise voltage produced by two resistors in series

However, since $V_{noise,1}$ and $V_{noise,2}$ are statistically independent, the mean value of the product term (A.1) is zero. Therefore,

$$\overline{V^2_{noise,out}} = \overline{V^2_{noise,1}} + \overline{V^2_{noise,2}} = 4kT\left(R_1 + R_2\right)B \qquad \text{(A.2)}$$

The second method for analyzing the effect of noise in a circuit is based on the fact that a noisy circuit can be modeled by a noiseless circuit with external noise source. For example, a noisy two port network that contains internal noise sources is shown in Figure A.2 (a) The effect of the internal noise sources can be represented by the external noise voltage sources $V_{noise,1}$ and $V_{noise,2}$ placed in series with the input and output terminals, respectively, as shown in FigureA.2 (b).
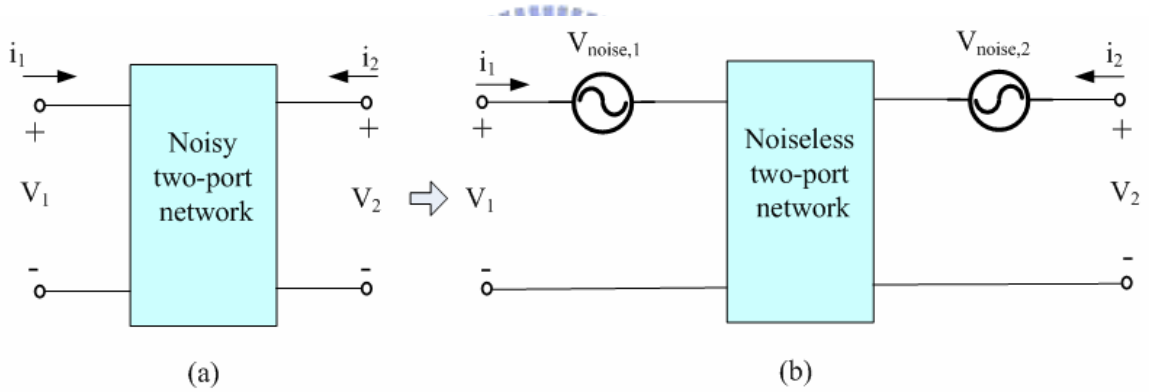
Figure A.2 (a) A noisy two-port network; (b) representation of the noisy two-port network in terms of a noise-free two-port network with external noise voltage sources $V_{noise,1}$ and $V_{noise,2}$

The values of $V_{noise,1}$ and $V_{noise,2}$ are calculated as follows. Representing the noise-free two-port network in Figure A.2 (b) by its z parameters, we can write

$$V_1 = Z_{11}i_1 + Z_{12}i_2 + V_{noise,1} \qquad \text{(A.3)}$$

and

$$V_2 = Z_{21}i_1 + Z_{22}i_2 + V_{noise,2} \tag{A.4}$$

Equations (A.3) and (A.4) show that the values of $V_{noise,1}$ and $V_{noise,2}$ can be determined from open-circuit measurements in the noisy two-port network. From (A.3) and (A.4), it follows that when the input and output terminals are open, then

$$V_{noise,1} = V_1 \big|_{i_1=i_2=0} \quad \text{and} \quad V_{noise,2} = V_2 \big|_{i_1=i_2=0} \tag{A.5}$$

The noise figure of the circuit in Figure A.3 is now derived. The total output noise power is proportional to the mean square of the short-circuit current ($\overline{i_{sc}^2}$) at the input port of the noise-free amplifier,

Figure A.3 Noise model for calculation of the amplifier noise figure

while the noise power due to the source alone is proportional to the mean square of the source current ($\overline{i_s^2}$). Hence, the noise figure NF is given by

$$NF = \frac{\overline{i_{sc}^2}}{\overline{i_s^2}} \tag{A.6}$$

Since

$$i_{sc} = -i_s + i_{noise} + V_{noise}Y_s \tag{A.7}$$

It follows that the mean square of i_{sc} is given by

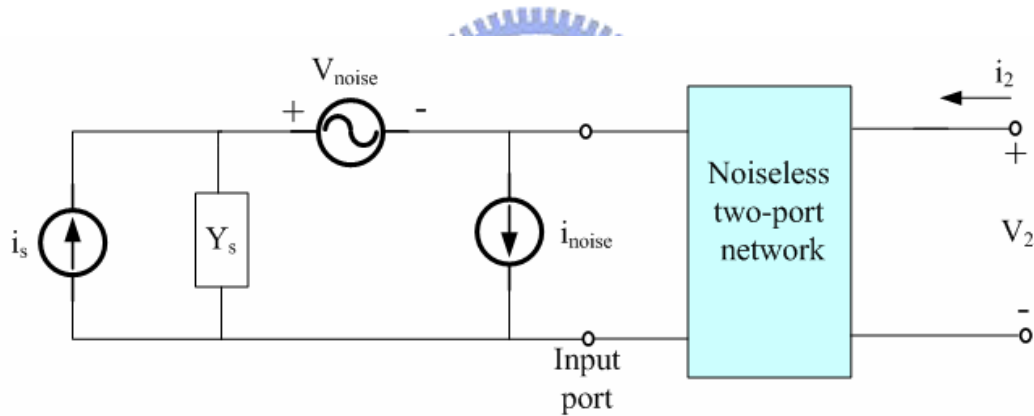$$\overline{i_{sc}^2} = \overline{\left(-i_s + i_{noise} + V_{noise}Y_s\right)^2} = \overline{i_s^2} + \overline{\left(i_{noise} + V_{noise}Y_s\right)^2} - 2\overline{i_s\left(i_{noise} + V_{noise}Y_s\right)} \tag{A.8}$$

Since the noise from the source and the noise from the two-port network are uncorrelated, we have

$$\overline{i_s\left(i_{noise} + V_{noise}Y_s\right)} = 0 \tag{A.9}$$

And (A.8) reduces to

$$\overline{i_{sc}^2} = \overline{i_s^2} + \overline{\left(i_{noise} + V_{noise}Y_s\right)^2} \tag{A.10}$$

Substituting (A.10) into (A.6) gives

$$NF = 1 + \frac{\overline{\left(i_{noise} + V_{noise}Y_s\right)^2}}{\overline{i_s^2}} \tag{A.11}$$

There is some correlation between the external sources V_{noise} and i_{noise}. Hence, we can write i_{noise} in terms of two parts; one part is uncorrelated to V_{noise} (called i_{nu}), and the other part is correlated to V_{noise} (called i_{nc}). Thus,

$$i_n = i_{nu} + i_{nc} \tag{A.12}$$

Furthermore, we can define the relation between i_{nc} and V_{noise} in terms of a correlation admittance Y_c-namely,

$$i_{nc} = Y_c V_{noise} \tag{A.13}$$

Y_c is not an actual admittance in the circuit. In fact, Y_c is defined by (A.13) and can be calculated as follows. From (A.12),

$$i_n = i_{nu} + Y_c V_{noise} \tag{A.14}$$

Multiplying (A.14) by V_n^*, taking the mean, and observing that $\overline{i_{nu} V_n^*} = 0$, we obtain

$$\overline{V_n^* i_n} = Y_c \overline{V_{noise}^2} \tag{A.15}$$

Substituting (A.14) into (A.11) results in the following expression for NF:

$$NF = 1 + \frac{\overline{\left(i_{nu} + V_{noise}\left(Y_s + Y_c\right)\right)^2}}{\overline{i_s^2}} \tag{A.16}$$

The noise produced by the source is related to the source conductance by

$$\overline{i_s^2} = 4kTG_s B \tag{A.17}$$

Where $G_s = \mathrm{Re}[Y_s]$. The noise voltage can be expressed in terms of an equivalent noise resistance R_n as

$$\overline{V_{noise}^2} = 4kTR_n B \tag{A.18}$$

And the uncorrelated noise current can be expressed in terms of an equivalent noise conductance G_u-namely,

$$\overline{i_{nu}^2} = 4kTG_u B \tag{A.19}$$

Substituting (A.17), (A.18), (A.19) into (A.11), and letting $Y_c = G_c + jB_c$ and

$Y_s = G_s + jB_s$ gives

$$\begin{aligned} NF &= 1 + \frac{4kTG_u B + \left|G_s + jB_s + G_c + jB_c\right|^2 4kTR_n B}{4kTG_s B} \\ &= 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s}\left[\left(G_s + G_c\right)^2 + \left(B_s + B_c\right)^2\right] \end{aligned} \tag{A.20}$$

The noise figure can be minimized by the proper selection of Y_s. From (A.20), NF is decreased by selecting

$$B_s = -B_c \qquad (A.21)$$

Hence, from (A.20),

$$NF\Big|_{B_s=-B_c} = 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s}(G_s + G_c)^2 \qquad (A.22)$$

The dependence of the expression in (A.22) on G_s can be minimized by setting

$$\frac{dNF\Big|_{B_s=-B_c}}{dG_s} = 0 \qquad (A.23)$$

which gives

$$\frac{dNF\Big|_{B_s=-B_c}}{dG_s} = -\frac{G_u}{G_s^2} + R_n\left(\frac{2G_s(G_s+G_c)-(G_s+G_c)^2}{G_s^2}\right) = 0 \qquad (A.24)$$

Solving for G_s, we obtain

$$G_s = \sqrt{G_c^2 + \frac{G_u}{R_n}} \qquad (A.25)$$

The values of G_s and B_s in (A.25) and (A.21) give the source admittance, which results in the minimum noise figure. This optimum value of the source admittance is commonly denoted by $Y_{opt} = G_{opt} + jB_{opt}$. That is,

$$Y_{opt} = G_{opt} + jB_{opt} = \sqrt{G_c^2 + \frac{G_u}{R_n}} - jB_c \qquad (A.26)$$

From (A.22), the minimum noise figure NF_{min} is

$$NF_{\min} = NF\Big|_{Y_s = Y_{opt}} = 1 + \frac{G_u}{G_{opt}} + \frac{R_n}{G_{opt}}\left(G_{opt} + G_c\right)^2 \tag{A.27}$$

Solving (A.25) for $\dfrac{G_u}{G_{opt}}$ and substituting into (A.27) gives

$$
\begin{aligned}
NF_{\min} &= 1 + R_n\left(G_{opt} - \frac{G_c^2}{G_{opt}}\right) + \frac{R_n}{G_{opt}}\left(G_{opt}^2 + 2G_{opt}G_c + G_c^2\right) \\
&= 1 + 2R_n\left(G_{opt} + G_c\right)
\end{aligned}
\tag{A.28}
$$

Using (A.28), we can write (A.20) in the form

$$NF = NF_{\min} - 2R_n\left(G_{opt} + G_c\right) + \frac{G_u}{G_s} + \frac{R_n}{G_s}\left[\left(G_s + G_c\right)^2 + \left(B_s - B_{opt}\right)^2\right] \tag{A.29}$$

Solving (A.25) for G_u and substituting into (A.29), the expression for NF can be simplified to read

$$NF = NF_{\min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right] \tag{A.30}$$

Equation (A.30) shows that NF depends on $Y_{opt} = G_{opt} + jB_{opt}$, R_n, and $NF_{\min}$. Once these quantities are specified, the value of NF can be determined for any source admittance Y_s. Equation (A.30) can also be expressed in the form

$$NF = NF_{\min} + \frac{r_n}{g_s}\left|y_s - y_{opt}\right|^2 \tag{A.31}$$

where $r_n = R_n/Z_0$ is the normalized noise resistance, y_s is the normalized source admittance,

$$y_s = \frac{Y_s}{Y_0} = \frac{G_s + jB_s}{Y_0} = g_s + jb_s \tag{A.32}$$

and y_{opt} is the normalized value of the optimum source admittance,

$$y_{opt} = \frac{Y_{opt}}{Y_0} = \frac{G_{opt} + jB_{opt}}{Y_0} = g_{opt} + jb_{opt} \qquad (A.33)$$

Appendix   *Noise Analysis of MOS Transistors*

There are several noise sources in MOSFET. It is important to understand these noise sources and their effect on the performance of the devices. The model of the CMOS transistor is shown in Figure B.1. And the different noise sources model in the CMOS transistor are shown in Figure B.2. They include the noise at drain constituted by the channel thermal noise and the flicker noise and the terminal gate resistance thermal noise.
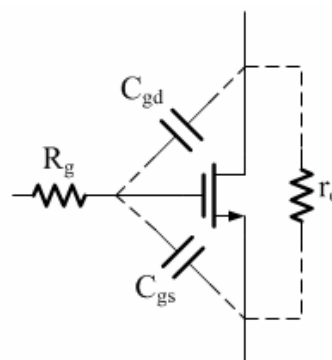
Figure B.1 Model of the CMOS transistor

The dominant noise source in CMOS devices is channel thermal noise. This source of noise is commonly modeled as a shunt current source in the output circuit of the
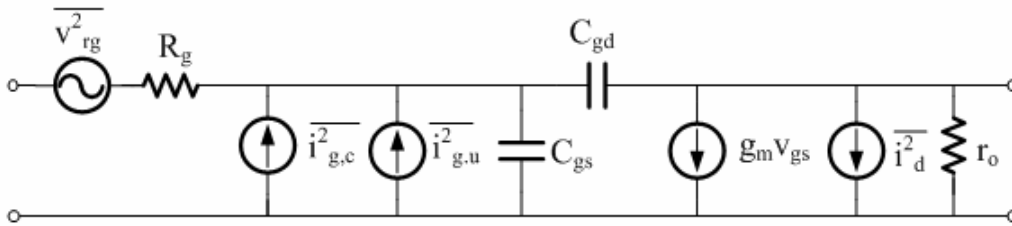
device.

Figure B.2 Different noise sources model

$\overline{i_d^2}$ **:** Drain noise current, due to the carrier thermal agitation in the channel.

$\overline{i_g^2}$ **:** Induced gate noise, due to the coupling of the fluctuating channel charge into

the gate terminal.

$\overline{v_{rg}^2}$ **:** Resistor thermal noise

C_{gs} **:** Gate-source parasitic capacitance of transistor.

C_{gd} **:** Gate-drain parasitic capacitance of transistor.

r_o **:** Output resistance of transistor.

R_g **:** Distributed gate resistance.

B.1   Channel Thermal Noise

The most significant source is the noise generated in the channel. In Figure B.3, the channel noise can be modeled by a current source connected between the drain and source terminals with a spectral density.
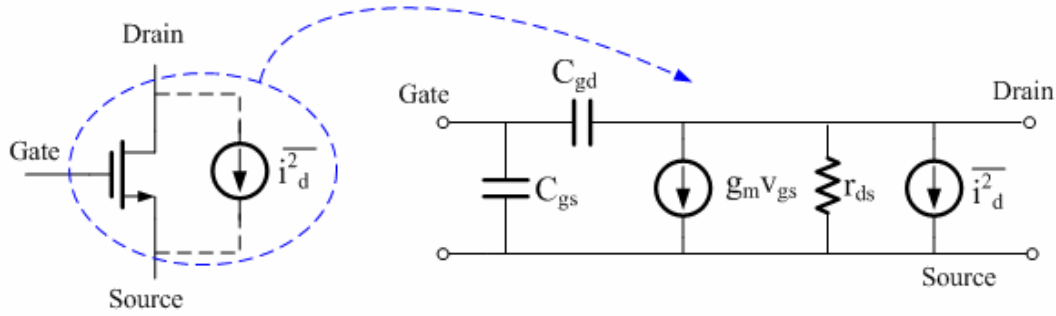
Figure B.3.   Equivalent thermal noise of a MOSFET transistor.

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma g_{d0} \tag{B.1}$$

k **:** The Boltzmann constant is $1.38*10^{-23}$J/K.

T **:** The absolute temperature.

g_{d0} **:** The zero-bias drain conductance of the device.

γ **:** A bias-dependent factor for long channel devices $\approx$ 0.67~1.33.

Δf **:** To emphasize that $4kT\gamma g_{d0}$ is the noise power per unit bandwidth.

B.2   Distributed gate resistance noise

An additional source of noise in CMOS device is the noise generated by the distributed gate resistance. This noise source can be modeled by a series resistance in the gate circuit shown in FigureB.4.
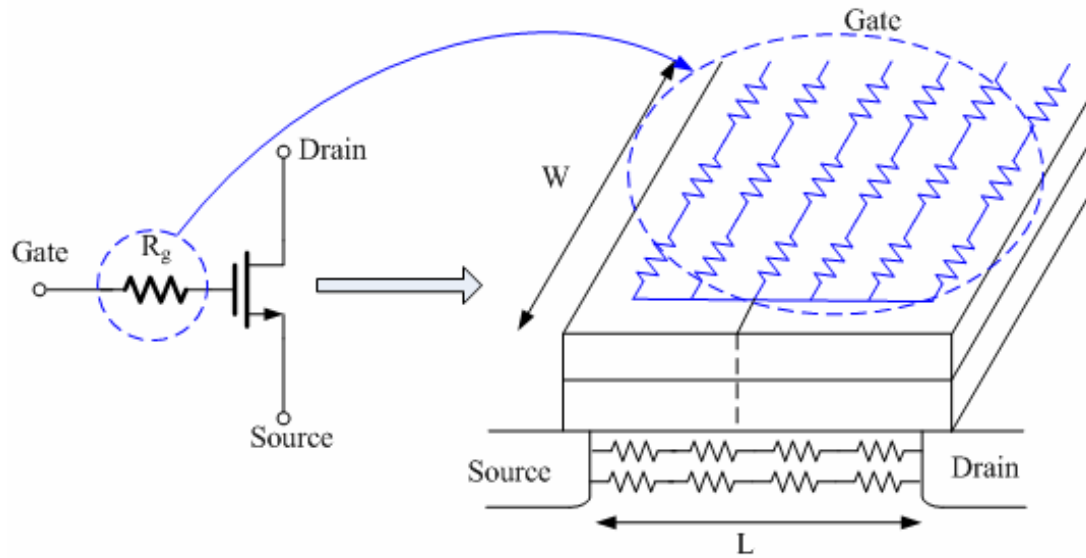
FigureB.4. Distributed gate resistance of a MOSFET

For noise purpose, the distributed gate resistance is given by:

$$R_g = \frac{R_H W}{3n^2 L}$$
(B.2)

R_H : The sheet resistance of the poly-silicon.

W : The total gate width of the device.

L : The gate length of the device.

n : The number of gate fingers used to layout the device.

B.3 Induced gate current noise

At high-frequency, the local channel voltage fluctuations due to thermal noise couple to the gate through the oxide capacitance and cause an induced gate noise current to flow is shown in Figure B.5.
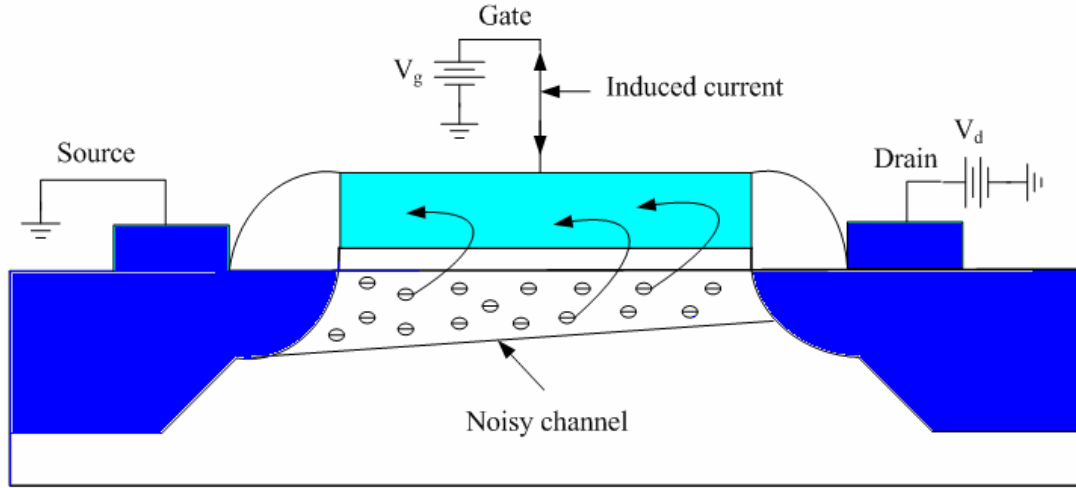
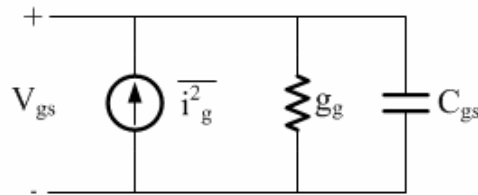Figure B.5 Induced gate current noise in MOS devices

Figure B.6. Small signal model of induced gate current noise

For an induced gate current noise, its small signal model can be represented by the circuit in Figure B.6. A simple gate circuit model that includes both of a shunt noise current $\overline{i_g^2}$ and a shunt conductance g_g have been added. Mathematical expressions for these sources are are given by:

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\varsigma g_g \quad , \quad g_g = \frac{\omega_0^2 C_{gs}^2}{5g_{d0}}$$

(B.3)

Where ς is the coefficient of gate noise, classically equal to 1.33 for long channel devices.

B.4 Correlation between Drain noise and Induced gate noise

The drain noise and induced gate noise share a common physical origin and it is expressed by cross-correlation between the two noise.

$$\overline{i_d i_d^*} = \frac{2}{3} 4kT g_{d0} \Delta f \tag{B.4}$$

$$\overline{i_g i_g^*} = \frac{4}{3} 4kT g_{d0} \Delta f \tag{B.5}$$

$$\overline{i_g i_d^*} = \frac{1}{6} j\omega C_{gs} 4kT \Delta f \tag{B.6}$$

The cross-correlation coefficient is defined as equation (B.7) and is about 0.395j in MOS device:

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g i_g^*} * \overline{i_d i_d^*}}} = 0.395 j \tag{B.7}$$

In Figure B.7, shows the induced gate noise can be split into two components. For the noise analysis, the first one is fully uncorrelated with the drain noise, and the other is fully correlated with the drain noise. It can be written as:

$$\overline{i_g^2} = 4kT \varsigma g_g (1 - |c|^2) \Delta f + 4kT \varsigma g_g |c|^2 \Delta f \tag{B.8}$$

$$\overline{i_g^2} = 4kT\varsigma \frac{\omega_0^2 C_{gs}^2}{5g_{d0}}(1-|c|^2)\Delta f + 4kT\varsigma \frac{\omega_0^2 C_{gs}^2}{5g_{d0}}|c|^2 \Delta f$$
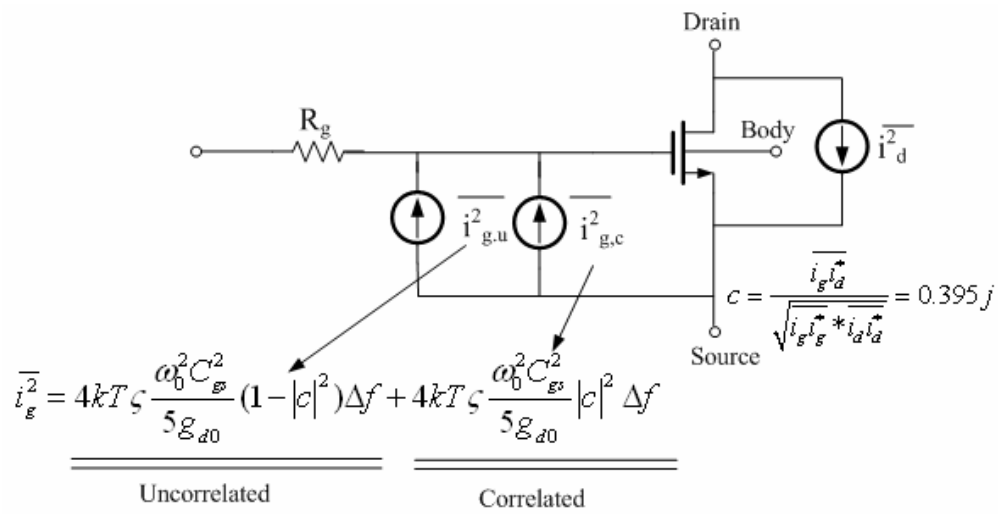
Figure B.7 The induced gate noise of split into two components

B.5   Other Noise Source

There are still many noise sources associated with the transistor, such as the Flicker noise besides the previous mentioned noise sources. In electronic devices, Flicker noise arises from a number of different mechanisms, and is most noticeable in devices that are sensitive surface traps. Hence, MOSFET exhibit significantly more flicker noise than bipolar devices do. However, the flicker noise can be ignored at the high frequency as a result of its noise power is inversely proportional to the frequency.