國立交通大學

電信工程學系碩士班

碩 士 論 文

應用於無線網路之低電壓(0.7V)變壓器迴授低雜訊放大器與應用於超寬頻系統之低雜訊放大器之設計

Design of Low-voltage (0.7V) Transformer-feedback for Wireless LAN and UWB low noise amplifier for UWB Systems

研究生：方瑞嫻

指導教授：周復芳　博士

中 華 民 國 九 十 六 年 六 月

應用於無線網路之低電壓(0.7V)變壓器迴授低雜訊放大器與應用於超寬頻系統之低雜訊放大器之設計

Design of Low-voltage (0.7V) Transformer-feedback for Wireless LAN and UWB low noise amplifier for UWB Systems

研究生：方瑞嫻　　**Student：Jui Hsien Fan**

指導教授：周復芳　博士　**Advisor：Dr. Christina F. Jou**

國立交通大學

電信工程學系碩士班

碩 士 論 文

A thesis

Submitted to Department of Communication Engineering

College of Electrical and Computer Engineering

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of

Master of Science

In Communication Engineering

June 2007

Hsin Chu, Taiwan, Republic of China

中 華 民 國 九 十 六 年 六 月

應用於無線網路之低電壓(0.7V)變壓器迴授低雜訊放大器與應用於超寬頻系統之低雜訊放大器之設計

研究生：方瑞嫻　　指導教授：周復芳 博士

國立交通大學電信工程學系碩士班

中文摘要

本論文的第一部份介紹低電壓低雜訊放大器電路設計方法，利用變壓器迴授來提升輸入輸出的隔絕度取代原有的疊接的低雜訊放大器架構。實作的低雜訊放大器顯示其並沒有達到預期的結果。第二部份探討其原因,最大的影響因素可能為晶片內部佈局不佳所造成的。將晶片銲線於 PCB 版子上並進一步探討。

在第三部份，介紹一個寬頻的低雜訊放大器，其輸入匹配利用電晶體雜散電容來達成。此方法可以使輸入匹配網路簡化，並且減少雜訊的貢獻。其模擬結果顯示 3.1GHz~10.6GHz 其輸入返回損耗和輸出返回損耗皆在-10dB 以下，增益為 12dB，最小雜訊指數為 4.5dB。但量測時與預期的模擬結果並不符合，在接下來的章節中也做了原因探討。

Design of Low-voltage (0.7V) Transformer-feedback for Wireless LAN and UWB low noise amplifier for UWB Systems

Student: Jui Hsien Fan Advisor: Dr. Christina F. Jou

Department of Communication Engineering

National Chiao Tung University

Abstract

In the first part of the thesis the design method of Low voltage LNA topology is studied which using transformer feedback to improve the isolation between input and output. This topology can replace the conventional LNA topology and is suited for low voltage application. The implemented LNA reveal that the unexpected measurement result. The second part of this thesis discussion the problem. The possible cause is the layout of this chip. Further, we also discussed the measurement result of chip bonded on the PCB board.

In the third part, an UWB LNA is designed. It uses the intrinsic capacitance of transistors to achieve the input matching and the complicated input matching network is replaced. The simulation result of UWB LNA demonstrates S11 < -10dB and S22 < -10dB from 3.1 to 10.6 GHz. The power gain (S21) is 12dB. The minimum noise figure is 4.5dB. The measurement result is different from the simulation result and in following section we discussed the possible problems.

Acknowledgement

首先，我要感謝指導教授周復芳老師，在這兩年來的指導和關心，讓我在碩士學業求學過程獲益良多。同時要感謝口試委員郭建男博士及胡政吉博士的不吝指導。另外要感謝吳匯儀學長的耐心教導，尤其當我遇到困難總能給我鼓勵和協助，並且指引了我研究方向，讓研究更有目標。

還有要感謝實驗室的同學子豪、智鵬、宜星、宇清，和你們一起熬夜晶片下線，雖然辛苦，但是卻很開心在研究所生涯中能有一起共患難的朋友，另外要感謝已畢業的學長文明、仕豪、柏揚、政展、秋榜和宏斌，你們認真的研究態度一直是我們的榜樣，也教導我們許多知識與實用的技巧，感謝和學弟昱舜、志豪等有你們陪我一起渡過這兩年的研究生生活，彼此在學業和研究各方面相互砥礪和支持，帶給了我一段美好、難忘、也最充實的時光。

最後我要感謝我最愛的父母親和家人，在我想走的路上，一路給我最大的支持和包容，讓我能順利地完成碩士學業。

瑞嫻 於 2007 年 風城 夏

Contents

List of Tables

List of Figures

Chapter 1 Introduction

1.1 Background and motivation

Wireless and mobile communications is one of the fast growing microelectronics applications. Traditionally, the RFICs are implemented in GaAs or SiGe process. With the process of scaled down CMOS technology, RFICs can be implemented in CMOS process and provide high integration and low cost. Under reduced supply voltage, many circuit topology of RF front-end can not meet the stringent dynamic range of wireless receiver. It needs more efforts toward finding out new topology suitable for sub 1-V supply voltage.

Ultra-wideband (UWB) system is an emerging high-speed and low-power wireless communication approved by Federal Communication Commission (FCC) in 2002 for commercial applications in the frequency range from 3.1 to 10.6GHz. UWB performs excellently for short-range high-speed uses, such as automotive collision-detection systems, through-wall imaging systems, and high-speed indoor networking, and plays an increasingly important role in wireless personal area network (WPAN). Designing wideband LNA for wireless applications suffer from some challenges. The LNA must have sufficient gain and low noise figure over the wideband from 3.1GHz to 10.6GHz. Because of some benefit by CMOS technology like low cost and high integration, it had been used for RF circuit popularly. But the lossy Si substrate degrades the performance of gain and noise figure. Many research studying in achieve flat gain, low noise and acceptable power consumption have been present in recently.

1.2 Thesis organization

This thesis discusses about the circuit design and implementation for low voltage and ultra-wideband applications. The contents consist of two major topics: “A 0.7V low voltage transformer feedback low noise amplifier” and “A 3.1~10.6GHz Ultra-wideband low-noise

amplifier", respectively in Chapter 2 and Chapter 3. We will present the design flow and experimental results in TSMC 0.18-μm CMOS process. Moreover, we will discuss the reasons of differences between simulation and measurement results.

In Chapter 2, we will present the design and implementation of a low-voltage for WLAN applications. We will discuss the technique of transformer feedback LNA. Besides, electromagnetic simulated software ADS momentum approach simulated results to practical circuited property. Then the difference between the simulated and measurement is discussed.

In Chapter 3, we will present the design and implementation of UWB LNA. This chapter we studied the technique of input matching. The difference between the simulated and measurement is also discussed.

Finally, we discuss our simulated and measurement results, conclusion and future work in Chapter 4.

Chapter 2 A 0.7V Low-voltage Transformer Feedback Low Noise Amplifier for 5-GHz Wireless LAN

2.1 Introduction

As CMOS technology scaling down for digital circuit, power consumption, operating speed, and number of transistors per unit area has been improved. But CMOS technology scaling is quite beneficial for digital circuits, not for RF analog circuits. The most severe consequence of technology scaling that affects the RF analog design is a reduction of the voltage supply. This is because integration of analog/RF and digital circuit on the same die is desirable from both cost and packaging considerations. Insufficient voltage headroom causes that not all circuit topologies can satisfy the required specifications.

The conventional topology of low noise amplifier is shown in Fig. 2.1.1.

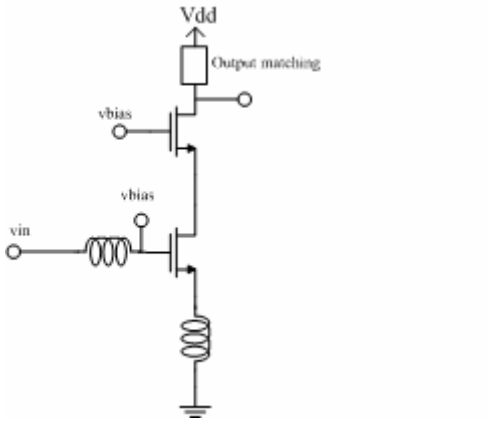


Fig. 2.1.1 Schematic of conventional low noise amplifier

The cascode structure helps increase stability, isolation between the output and input port and allows one to simultaneous match for both noise and impedance.

If each transistor has a overdrive Vov [i.e., the minimum voltage between drain and source

to operate in saturation region], the minimum supply voltage is twice Vov. It is not suit for the low voltage operation. For the classic cascode amplifier, both dc and ac currents are shared between the two transistors. If one could decouple the ac and dc portions of the circuit, one could reduce the power supply voltage.

In Fig. 2.1.2, we have illustrated the proposed decoupling scheme.[1]

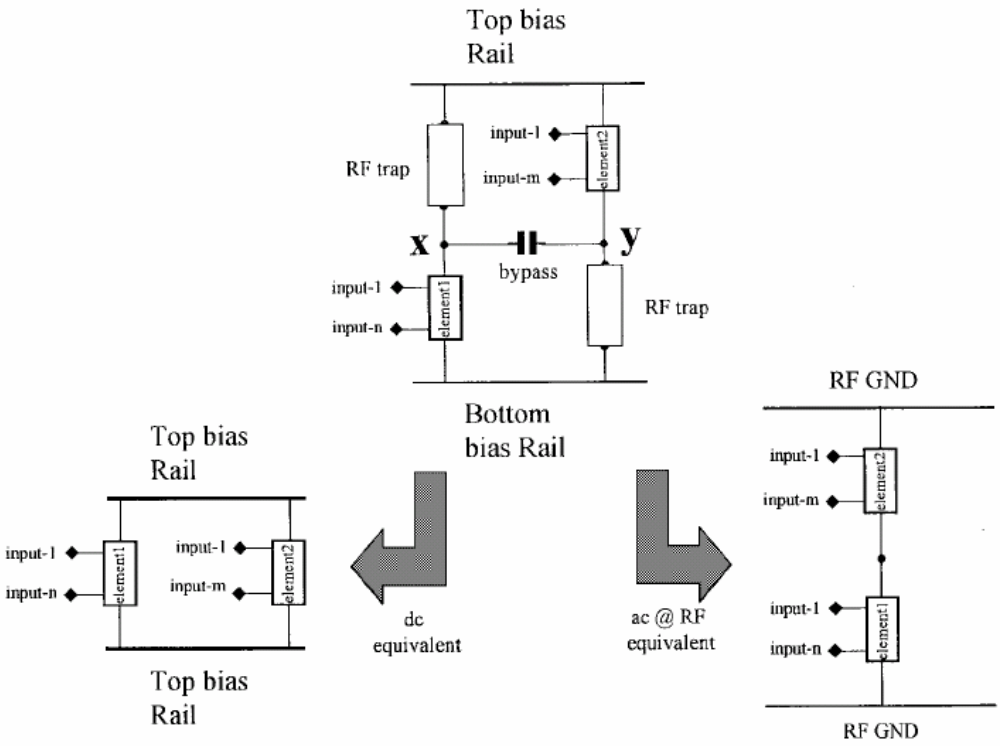


Fig. 2.1.2 Topology using capacitively coupled RF traps to isolated dc biasing from RF.[1]

The proposed scheme used two on-chip LC tanks which denoted as RF traps and one coupling capacitor. The RF trap is to provide a low impedance across its terminals at dc and relatively high impedance at RF. The coupling capacitor is to couple the RF signal between the two elements. Furthermore, since the RF traps require no dc head room, the minimum voltage supply required is only Vov, not 2Vov. This topology is suit for low voltage operation.

The folded low noise amplifier is widely used for low voltage as shown in Fig.2.1.3

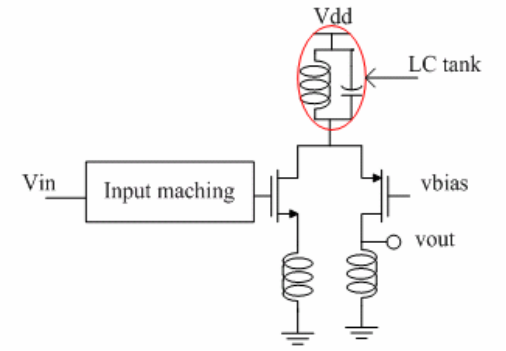


Fig.2.1.3 Folded low noise amplifier

The stacked NMOS of the conventional low noise amplifier is replaced by PMOS and the minimum supply voltage can also be reduced. The on-chip LC-tank is used to force the RF signal into the PMOS. The LC-tank resonates at the operation frequency.

The low noise amplifier using transformer-feedback is present for low voltage application. As operating frequencies increase, amplifier designers can no longer neglect the effects of the field-effect transistor gate-drain overlap capacitance C_{gd} on performance since it is comparable in magnitude to the gate-source capacitance. The conventional low noise amplifier use the cascode configuration to reduce the signal feedback via C_{gd} but a two-transistor stack is not optimal for operation at the lowest possible supply voltage. If the designer can reduce the amount of signal which feedback via C_{gd}, it allows that only one MOS configuration of low noise amplifier can be operated by a drain-source bias voltage equal to the supply voltage(i.e., $V_{DS}=V_{DD}$). Neutralization cancels signal flow through C_{gd} by adding additional signal paths around the amplifier so that the net signal floe through C_{gd} and the additional signal path is zero. The examples of C_{gd} neutralization are shown in Fig. 2.1.4.

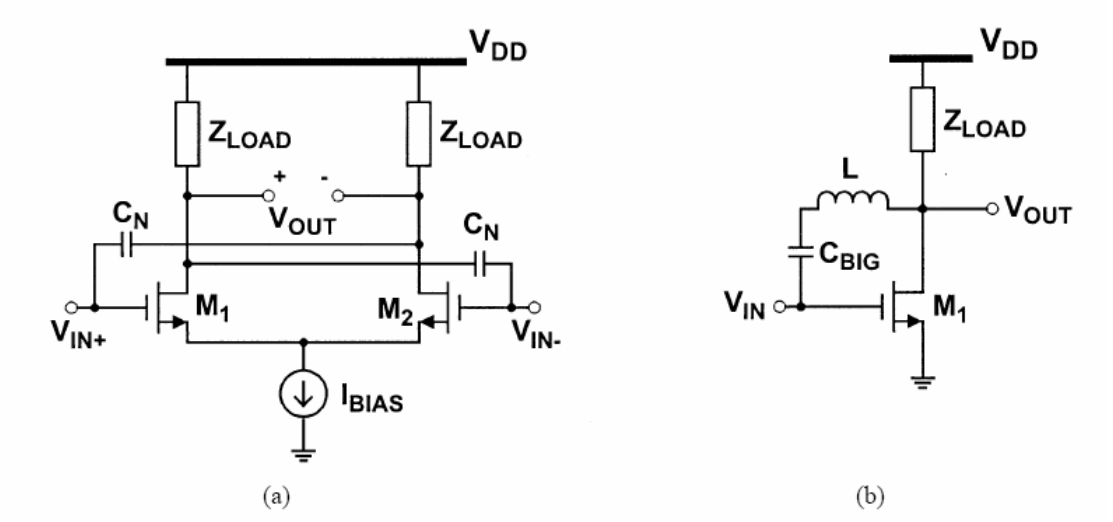


Fig. 2.1.4(a) uses neutralizing capacitors C_N to cancel the signal flow through C_{gd}.(b)Inductor-tuned technique. [2]

The signal flowing through C_N is equal in magnitude and opposite in phase to the signal flowing through C_{gd} because the drain voltages of the differential pair are 180° phase shifted. If C_N=C_{gd} it achieves neutralization. But the signal flow through C_N is actually positive feedback that can cause instability. If C_N dose not exactly equal C_{gd} a net positive feedback can result. The neutralizing capacitors C_N affects gain, bandwidth, and terminal impedances. The circuit of Fig. 2.1.4(b) uses an inductor L to resonate with C_{gd}. Because the required value of inductance is too large to be integrated it is impractical for monolithic implementations.

Another approach to neutralization use transformer feedback, which introduces magnetic coupling between drain and source inductors of a common-source transistor, as shown in Fig. 2.1.5.[3]

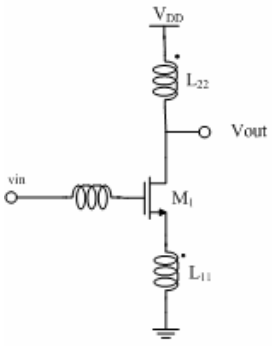


Fig. 2.1.5. Transformer-feedback low noise amplifier

2.2 Transformer

2.2.1 Introduction of transformer

The requirements for low cost and higher integration of RF ICs carry on rising due to the growing mobile wireless communication markets. On-chip transformers substantially contribute to enhance the reliability, efficiency, and performance of silicon-integrated RF circuits. Recently some research had used the transformer to get better performance. Previous papers had reported the integration of monolithic transformers in voltage-controlled oscillators, and low-noise amplifiers.

2.2.2 Numerous types of transformer [4]

The operation of a passive transformer is based upon the mutual inductance between two or more conductor, or windings. A microstrip line is the simplest on-chip element for monolithic implementation of a transmission line inductor, and the strip is normally wound into a spiral to reduce chip area of the component. A planar monolithic transformer is shown in Fig. 2.2.1

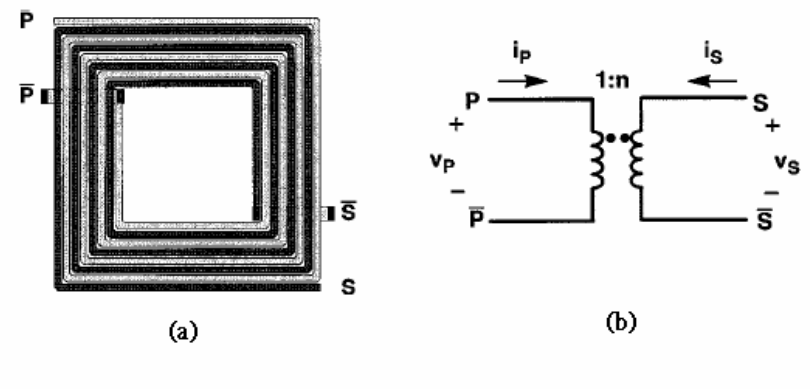
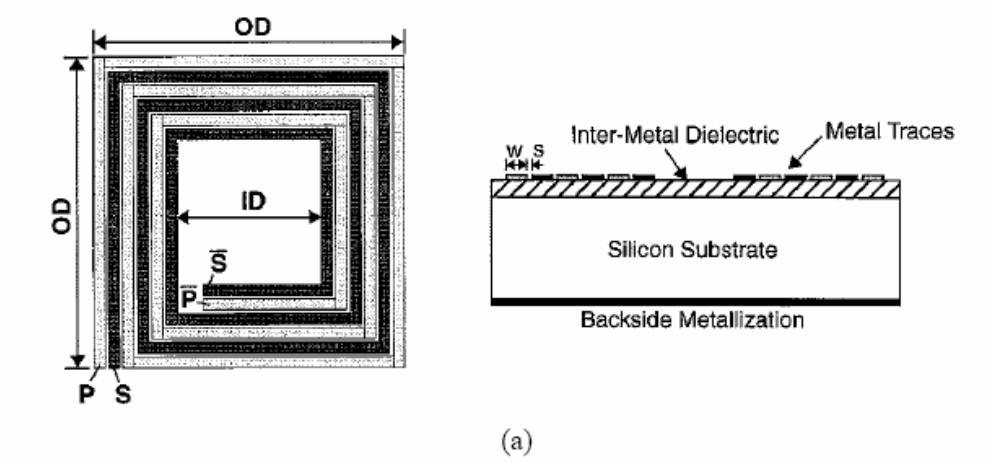


Fig. 2.2.1 Monolithic transformer. (a) Physical layout. (b) Schematic symbol.

Magnetic flux produced by current flowing into the primary winding at the terminal P induces a current in the secondary winding that flows out of terminal S. It produces a positive voltage across a load connect between terminal S and $\overline{S}$. The main electrical parameters of interest are the transformer turn ratio n and the coefficient of magnetic coupling k. The current and voltage transformation of an ideal transformer are related to turns ratio by following

equation. $n = \frac{v_s}{v_p} = \frac{i_p}{i_s} = \sqrt{\frac{Ls}{Lp}}$, L_p and L_s are the self-inductances of the primary and secondary winding. The strength of the magnetic coupling between windings is defined by the k-factor. $k = \frac{M}{\sqrt{LpLs}}$,where M is the mutual inductance between the primary and secondary winding. Since the materials used in the fabrication of an IC chip have magnetic properties similar to air, there is poor confinement of the magnetic flux in a monolithic transformer. Thus, the k-factor is always substantially less than one for a monolithic transformer. The phase of the voltage induced at the secondary of the transformer depends upon the choice of the reference terminal. If the load is connected to terminal S with $\overline{S}$ grounded there is minimal phase shift of the signal at the secondary for an ac signal source with the output and ground applied between terminals P and $\overline{P}$. A monolithic transformer is constructed using conductors interwound in the same plane or overlaid as stacked metal. Fig. 2.2.2 show numerous transformer winding configurations.



(a)

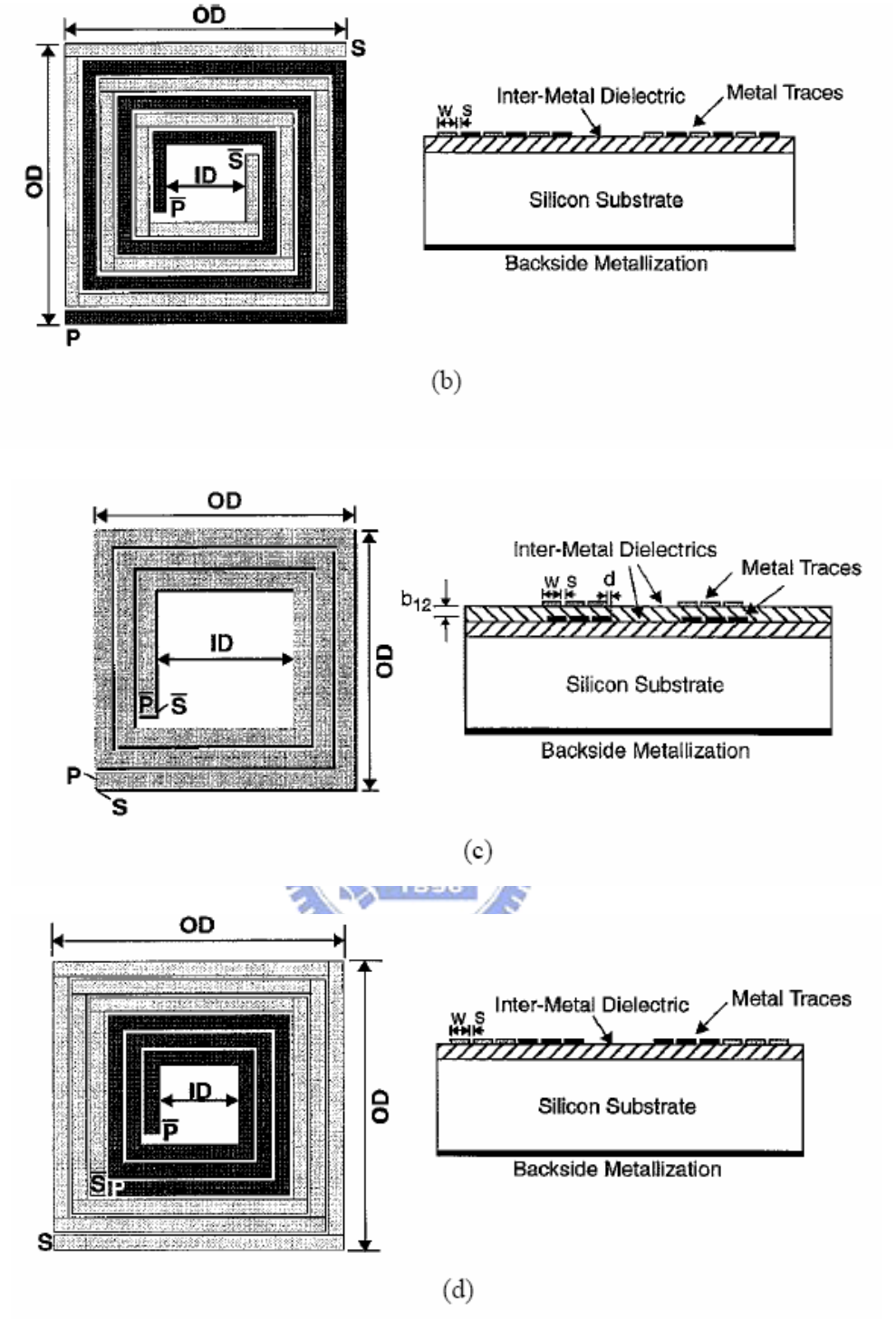


Fig.2.2.2 Monolithic transformer winding configurations (a) Parallel conductor winding. (b) Interwound winding. (c) Overlay winding (d) Concentric spiral winding

The mutual inductance of transformer is proportional to the peripheral length of each winding. In order to maximize the periphery between windings we interleave planar metal traces or overlay conductors but it increase interwinding capacitance at the same time. The

magnetic coupling coefficient k is determined by the mutual and self-inductances, which depend primarily upon the width and spacing of the metal trace. Fig. 2.2.2(a) show a transformer with two parallel conductor which are interwound to promote coupling of the magnetic field between windings. Because the length of the primary and secondary is not equal the transformer turn ratio $n \neq 1$ although there are the same number of turns of metal on each winding. The transformer shown in Fig. 2.2.2(b) eliminates the inherent asymmetry. This ensures that electrical characteristics of primary and secondary are identical when they have the same number of turns. Multiple conductor layers are used to fabricate an overlay or broadside coupled transformer as shown in Fig. 2.2.2(c). The stacked conductor utilizes both edge and broadside magnetic coupling to reduce the overall area in the physical layout. Flux linkages between the conductor layers is improved as the intermetal dielectric is thinned, which gives higher magnetic coefficient k when fabricated on an RF IC. The difference in thickness between metal layers results in unequal resistances for the upper and lower winding. The parasitic capacitance to the conductive substrate is different for each winding. There is a large parallel-plate parasitic capacitance between the upper and lower winding due to the overlapping if metal layers, which limits the frequency response. To reduce the parallel-plate parasitic capacitance we can offset the upper and lower metal layers by some distance d as shown in the cross-section of Fig. 2.2.2(c). Fig. 2.2.2(d) show another transformer which is implemented using concentrically wound planar spirals. The common periphery between the two windings is limited to just a single turn. Therefore, mutual coupling between adjacent conductors contributes mainly to the self-inductance of each winding and not to mutual inductance between the windings. The concentric spiral transformer has less mutual inductance and more self-inductance, which gives it a lower k-factor. However, a low ratio of mutual inductance to self-inductance is useful in applications such as peaking coils for high-performance broadband amplifiers.

2.2.3 Equivalent model of ideal transformer

The equivalent model of an ideal transformer is shown in Fig. 2.2.3

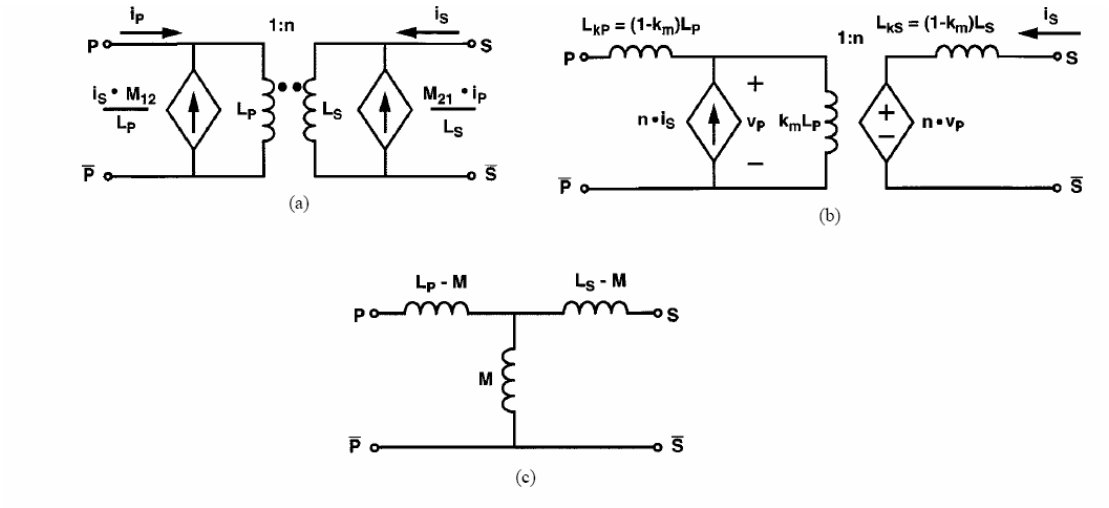


Fig. 2.2.3. Model for magnetic coupling in a 1:n transformer. (a) Direct form model. (b) Dual-source model. (c) T-section model

In Fig. 2.2.3(a) the inductance Lp and Ls model the self-inductances of the primary and secondary windings. Mutual coupling between winding is modeled by the dependent current sources, which are weighted by the parameters M_{12} and M_{21} .The parameters M_{12} and M_{21} are equal for a passive, reciprocal transformer. By using the Thevenize's theory the dependent current source on the secondary side of the direct-form model gives the dual-source model shown in Fig. 2.2.3(b). Current flowing through magnetizing inductance k_mL_p give rise to voltage v_p which controls the dependent voltage source on the secondary side. The actual terminal voltage is modified by current flow through leakage inductances L_{kp} and L_{ks} placed in series with the primary and secondary windings. $M^2 = (L_p - L_{kp})(L_s - L_{ks})$ This equation can not explicitly define two unknown leakage inductances. This arbitrary assignment of leakage inductance is not unique and other combinations are possible. The T-section model of Fig.2.2.3(c) uses three inductors to model the mutual coupling between windings. This model simplifiers hand analysis of circuits incorporating transformers, however, it is only valid for ac signals because there must be isolation of dc current flow between the primary and secondary loops in a physical transformer.

2.3 Design considerations

2.3.1 Transformer-feedback technique [3]

The schematic of low noise amplifier using transformer-feedback and its small-signal equivalent circuit are shown in Fig.2.3.1.

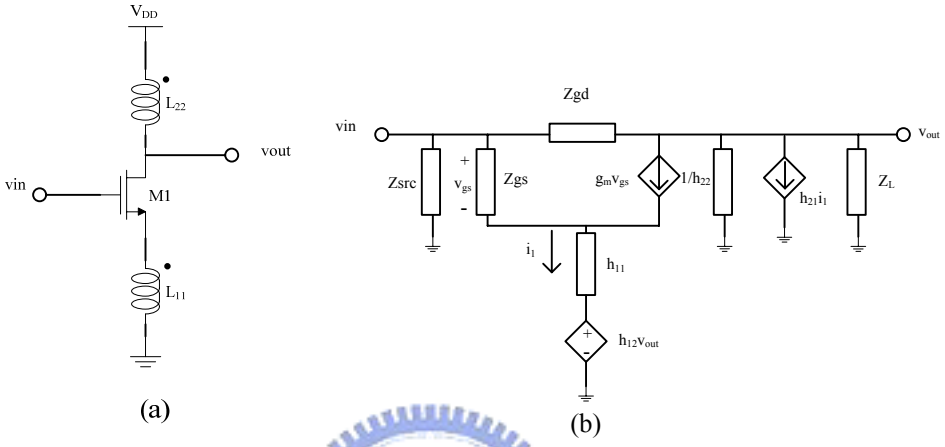


Fig. 2.3.1. (a)Schematic (b) small-signal equivalent circuit of transformer-feedback LNA

The h parameter model of transformer is shown in Fig. 2.3.2

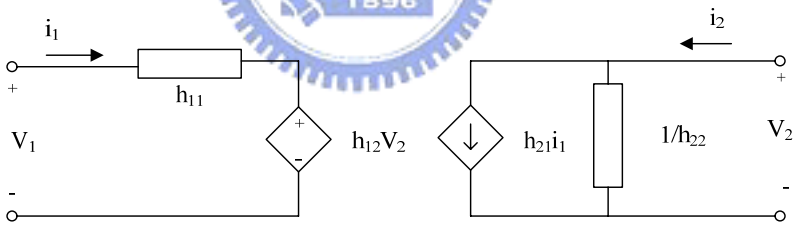


Fig. 2.3.2. h parameter model of transformer.

The transformer h parameter are given by $h_{11} = s(1-k^2)L_{11}$ $h_{12} = \frac{-k}{n}$ $h_{21} = \frac{k}{n}$ $h_{22} = \frac{1}{sL_{22}}$ $n = \sqrt{L_{22}/L_{11}}$ $k = M/\left(\sqrt{L_{11}L_{22}}\right)$. Impedances Z_{gs} and Z_{gd} represent the MOS capacitances C_{gs} and C_{gd}. In order to realize the neutralization between the input and output the forward signal-flow graph can be derived from the small signal model which is shown in Fig. 2.3.3.

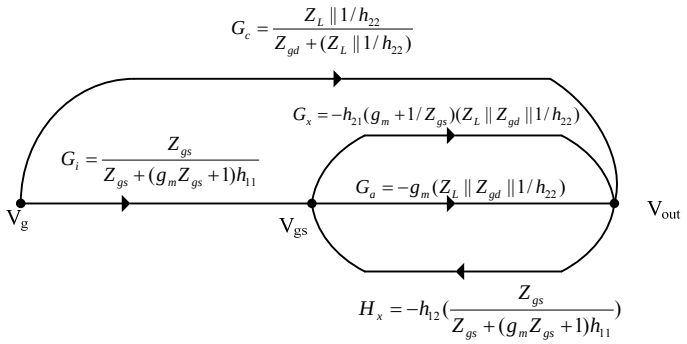


Fig. 2.3.3. The forward signal-flow graph.

In the forward signal-flow graph we can find the primary active path consists of a voltage divider between the gate-source voltage of the transistor (path G_i),which excites the MOS voltage-controlled current source and results in a voltage at the output node through active path G_a. Feedforward through the transformer is represent by path G_x and feedback through the transformer by H_x. Because of inverting transformer the h_{12} is a negative quantity and the feedback path subtracts from the signal applied at the input. The path G_c represent the signal pass through the gate-drain overlap capacitance and because the overlap capacitance connects directly to an independent voltage source V_g, feedback through C_{gd} does not affect the forward signal-flow graph. The condition required for neutralization is derived from the reverse signal-flow graph as shown in Fig.2.3.4.

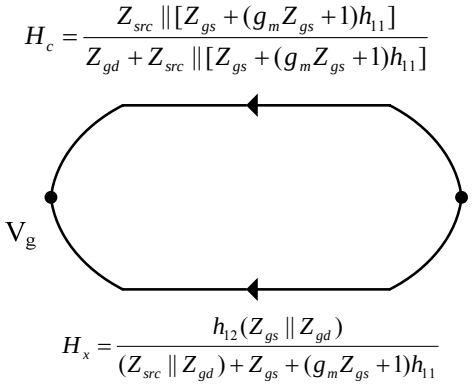


Fig. 2.3.4. Reverse signal-flow graph

When considering the reverse signal flow, output voltage v_{out} is an independent variable and the voltage at the gate V_g is a dependent variable. Because the Z_L and $1/h_{22}$ is connected

between the independent variable V_{out} and ground, they have no effect on the reverse signal flow. From the reverse signal-flow graph we can find there are two reverse signal paths. Path H_x represents reverse signal flowing through the transformer and path H_c represents reverse signal flowing through the gate-drain capacitance C_{gd}. Because h_{12} is a negative quantity, these two paths can be designed to cancel to neutralize the amplifiers. Setting H_c=-H_x results in $\frac{n}{k} \approx \frac{C_{gs}}{C_{gd}}$. For the 0.18μm CMOS technology C_{gs}/C_{gd}≈3. Therefore, neutralization is achieved when the effective transformer turns ratio n/k is set equal to capacitance ratio C_{gs}/C_{gd}.

2.3.2 0.7V low voltage low noise amplifier

We use the transformer feedback technique to implement a low voltage LNA and its schematic is shown in Fig. 2.3.5

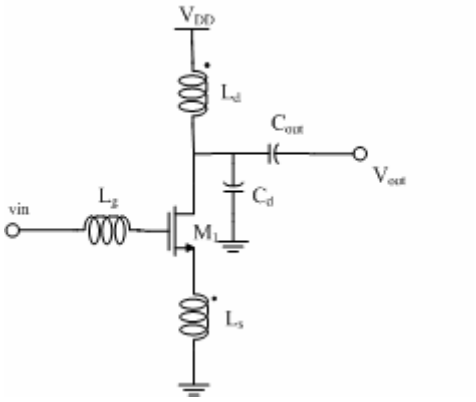


Fig. 2.3.5 Schematic of low voltage LNA

In order to achieve noise optimization the width of MOS is $W_{opt} \approx \frac{1}{3\omega C_{ox} R_s L}$ under the condition of power consumption-constrain. For 0.18μm CMOS technology the value of C_{ox} is above 8.6fF/μm^2. At the operating frequency we can find the optimum width $W \approx 114\mu m$. Next select the source degeneration inductor to make sure the amplifier is stable. To achieve the neutralization the inductor L_d have to follow the rule $n/k \approx C_{gs}/C_{gd} \approx 3$. The output matching is achieved by the C_d, C_{out} and L_d.

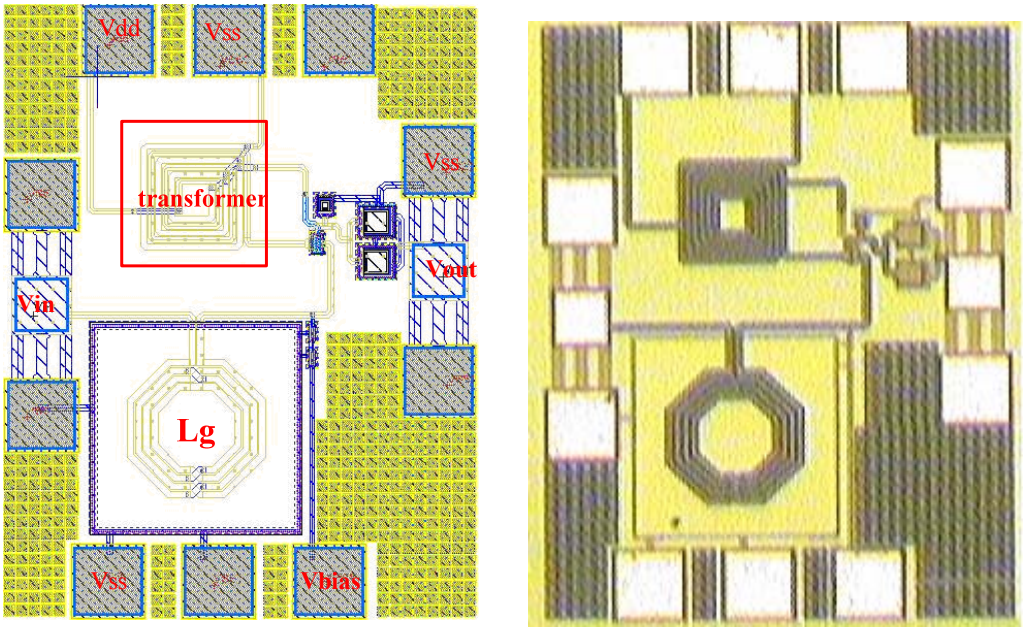
The transformer composted of the inductor L_s and L_d is simulated by ADS momentum. By EM simulation we can extract the S-parameter of transformer. Thus we can find the magnetic coefficient k is $\frac{\sqrt{\mathrm{Im}(Z_{12})\,\mathrm{Im}(Z_{21})}}{\sqrt{\mathrm{Im}(Z_{22})\,\mathrm{Im}(Z_{11})}}$ [30] according to the four ports S-parameter of transformer.

The wire connected each device is simulated by EM simulation to extract the S-parameter and used in post-simulation.

2.4 Chip implementation and measured results

2.4.1 Layout considerations

The chip layout and photo of the low voltage LNA is shown in Fig. 2.4.1. The layout skill is very important for radio frequency circuit design because it may affect circuit performance very much. In order to reduce noise , the MOSFET is used as multi-finger, which total width is 100 μm, and the power supply (Vdd) is 0.7V. The 0.18μm (minimum) gate length was chosen to get the highest speed. The MIM (Metal-Insulator-Metal) capacitors without shield and hexagonal spiral inductors (the Q-value is below 18) are used in this work. Guard-rings are added with all elements to prevent substrate noise and interference. A shielded signal GSG pad structure is used in RF input and RF output to reduce the coupling noise from the noisy substrate. All interconnections between elements are taken as a 45° corner. The RF input and the RF output are placed on opposite sides of the layout to avoid the signals coupling. The chip size is 0.84x0.63mm^2.



(a) (b)

Fig.2.4.1.(a) layout of transformer-feedback LNA. (b) Chip Photo of the transformer-feedback LNA

2.4.2 Measurement considerations

The LNA is designed for on-wafer measurement so the layout must follow the rules of CIC's (Chip Implementation Center's) probe station testing rules. This circuit needs one 3-pin two 3-pin DC PGP probe and two RF GSG probes for on-wafer measurement. A large coupling capacitor is needed in the input of the LNA to isolate the dc between circuit and equipment. Fig. 2.4.2 ~ Fig. 2.4.5 show the measurement setup for S-parameters, noise figure, 1dB compression point and third-order intercept point. We will discuss the experimental and simulation results of this circuit in following sections.

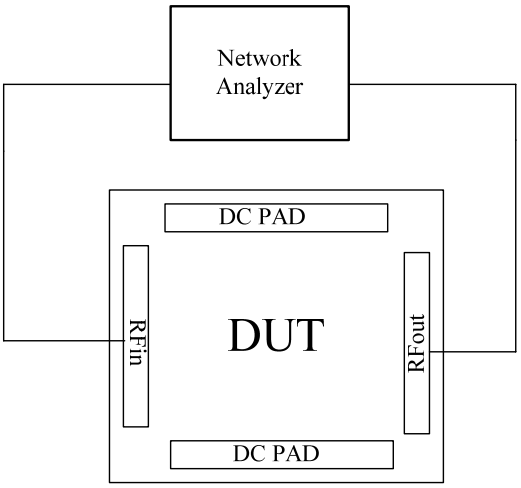


Fig. 2.4.2 Measurement setup for S-parameters

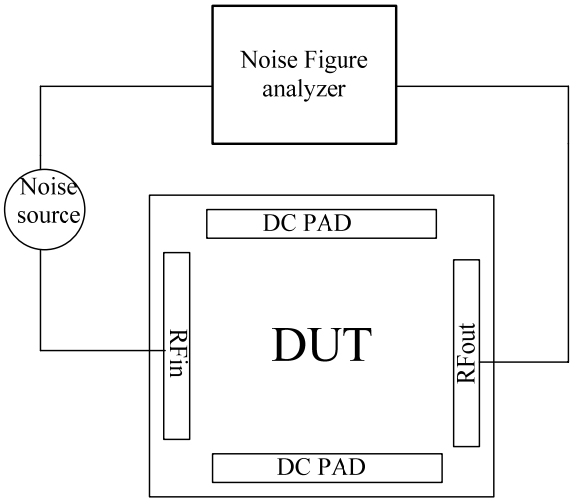


Fig. 2.4.3 Measurement setup for noise figure

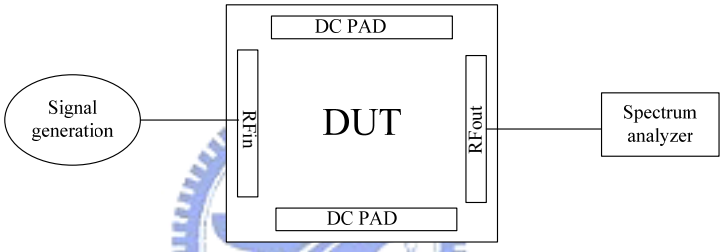


Fig. 2.4.4 Measurement setup for P1dB

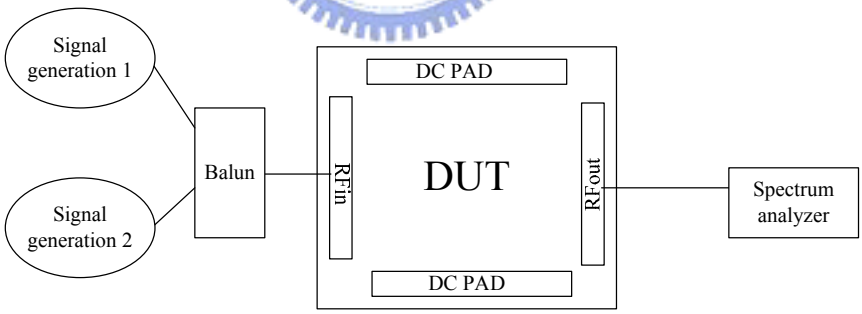


Fig. 2.4.5 Measurement setup for IIP3

2.4.3 Measurement results and discussions

This work is designed and processed using TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology. The simulation and measurement S-parameter are shown in Fig. 2.4.6(a) ~ (d), noise figure is shown in Fig. 2.4.7, P1dB is shown in Fig. 2.4.8 and IIP3 is shown in Fig. 2.4.9.

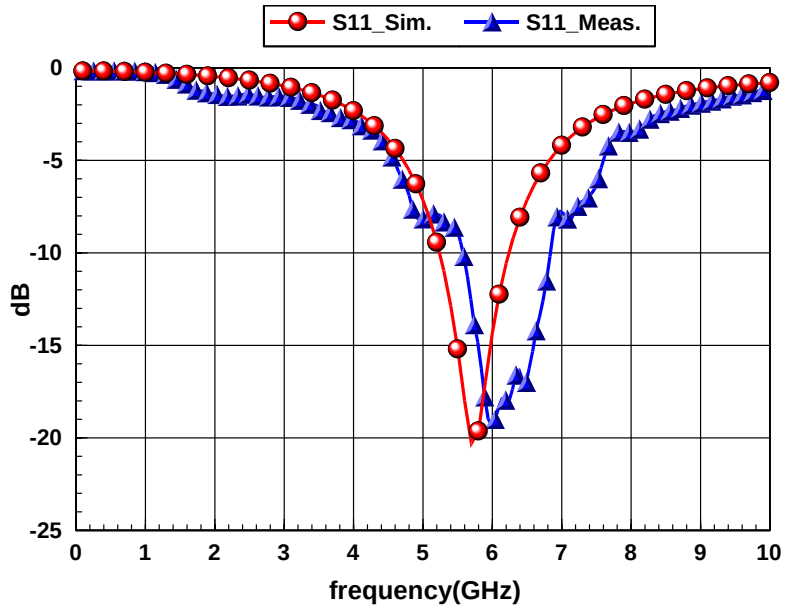


Fig. 2.4.6(a) simulation and measurement result of S_{11}.

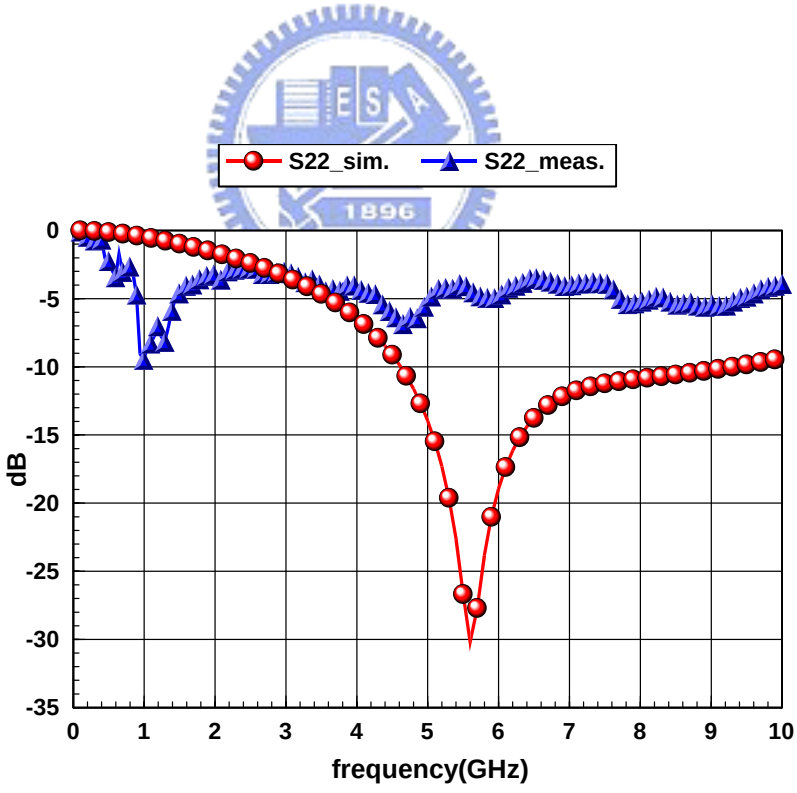


Fig. 2.4.6(b) simulation and measurement result of S_{22}.

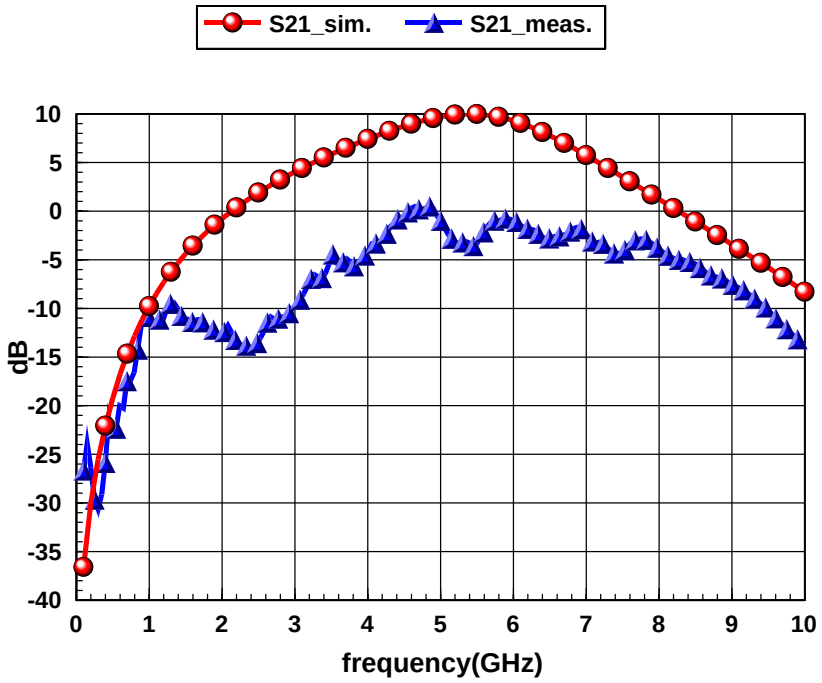


Fig. 2.4.6(c) simulation and measurement result of S_{21}.

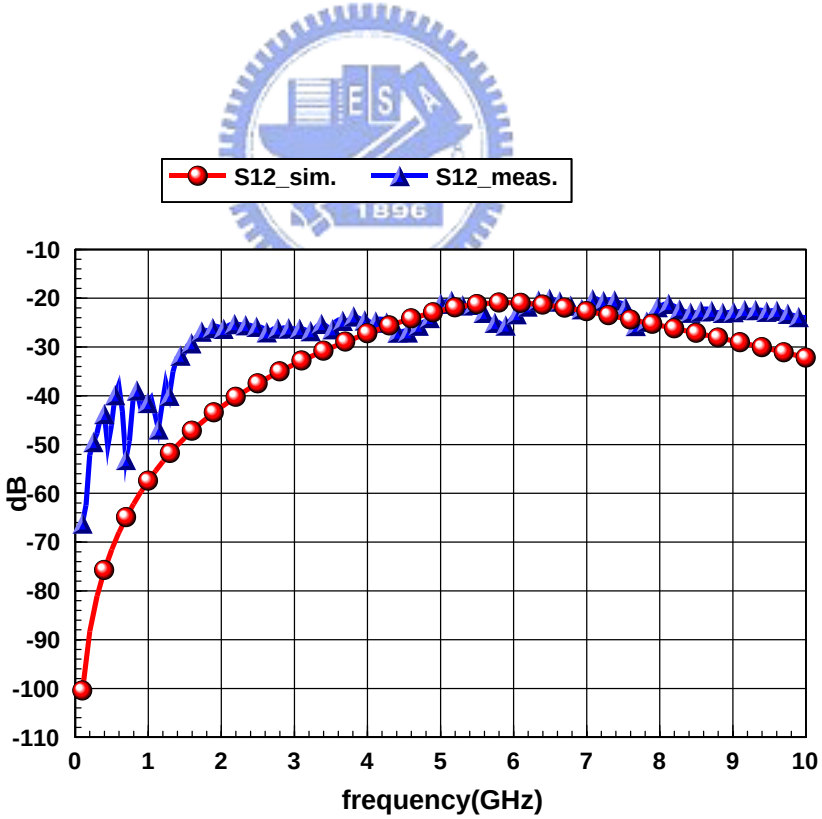


Fig. 2.4.6(d) simulation and measurement result of S_{12}.

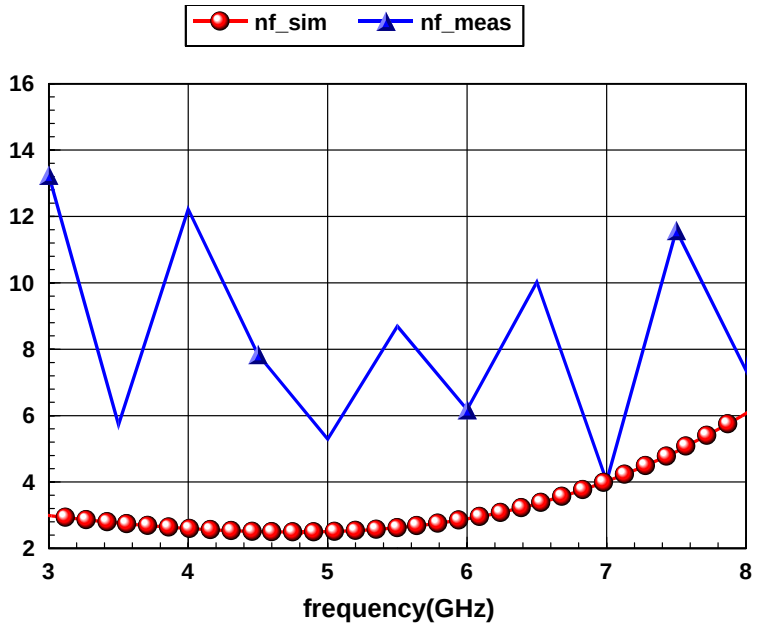


Fig. 2.4.7 simulation and measurement result of NF.

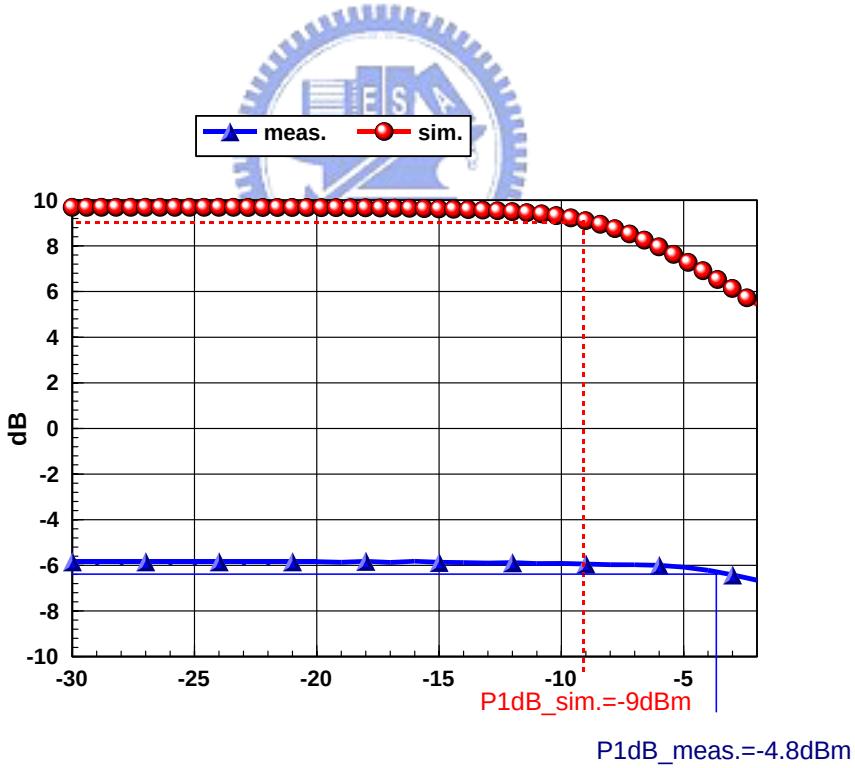


Fig. 2.4.8 simulation and measurement result of P1dB.

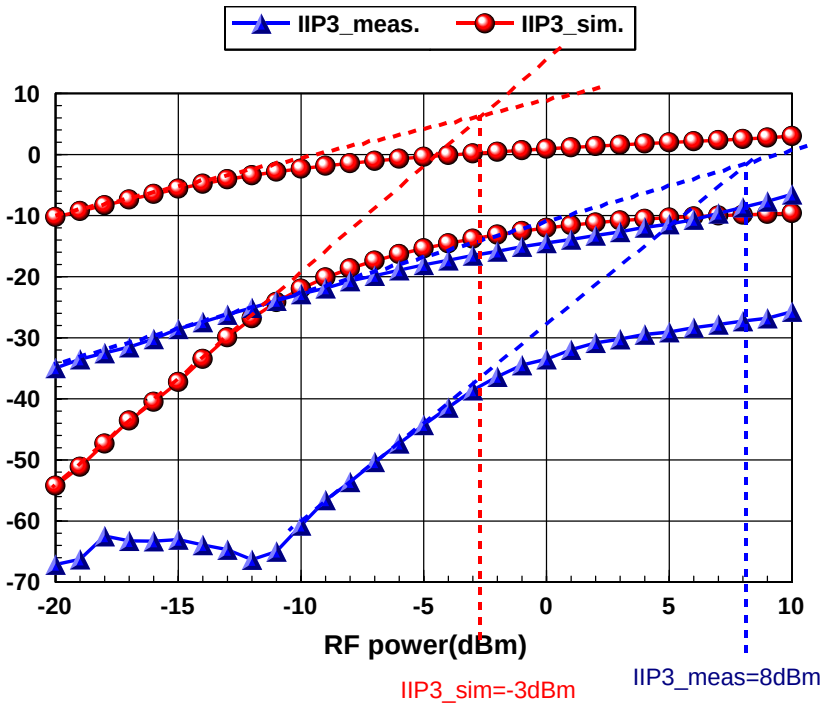


Fig. 2.4.9 simulation and measurement result of IIP3.

The simulation and measurement result is summary in Table 2.4.1.

Table 2.4.1 Performance summary of low-voltage transformer-feedback LNA@5.8GHz

Specification	Measurement	Post Simulation
S11 (dB)	-14	-20
S22 (dB)	-5	-23
S21 (dB)	-1	9.8
S12 (dB)	-24	-20
Noise Figure (dB)	7	3.4
P_{1dB} (dBm)	-4.8	-9
IIP3 (dBm)	8	-3
Vdd (V)	0.7	0.7
LNA Power (mW)	4.2mW	4.6mW

The measurement results reveals that the output is not match to 50Ω thus the power can not transmit out. We find the possible problem from the layout of circuit. In layout the four ports of the transformer composed of L_S and L_d are connected to the MOS source node, drain node,

V_{dd} pad and V_{ss} PAD. There are no connections between all V_{ss} PAD. Because of the isolation of each Vss PAD these ground nodes are no longer perfect grounded. Although we use external equipment to connect this Vss PAD between ground, it could induced parasitical effect along the ground path and influence the measurement data. The parasitic impedance arises from the external measure machine. The figure 2.4.10 shows the supposed circuit under the situation of on-wafer measurement.

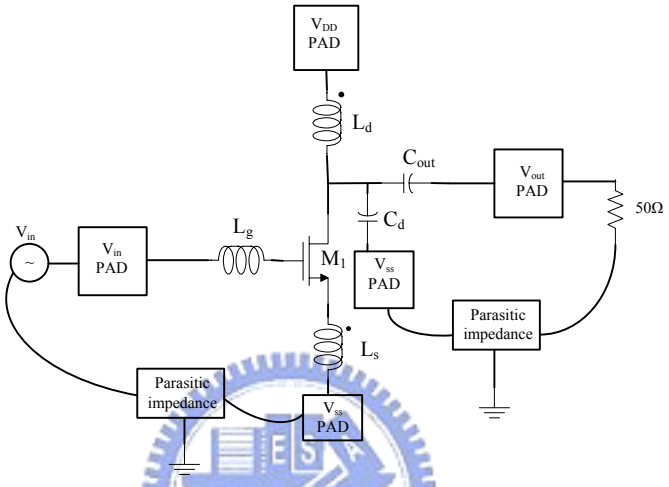


Fig. 2.4.10 Supposed circuit of on-wafer measurement

The modified simulation gives us a reasonable explanation the difference between simulation and measurement. The Fig.2.4.11(a)~(d) shows the modified simulation result and on-wafer measurement result.

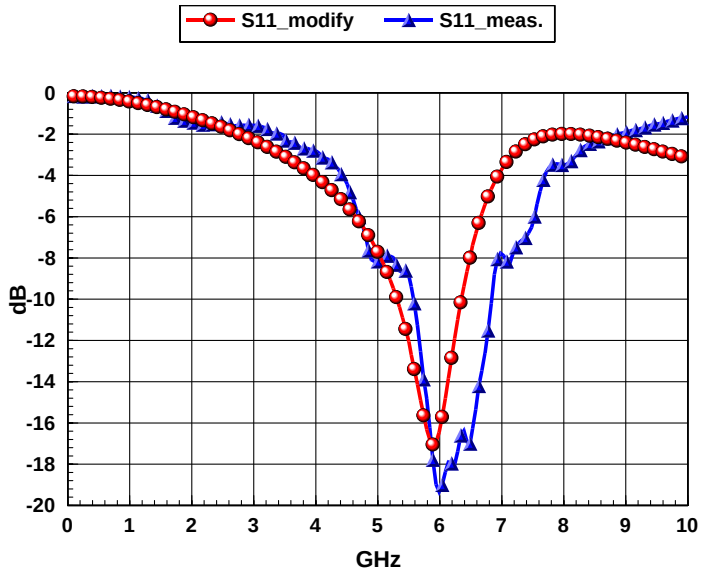


Fig.2.4.11(a) the modified simulation and on-wafer measurement result of S_{11}.

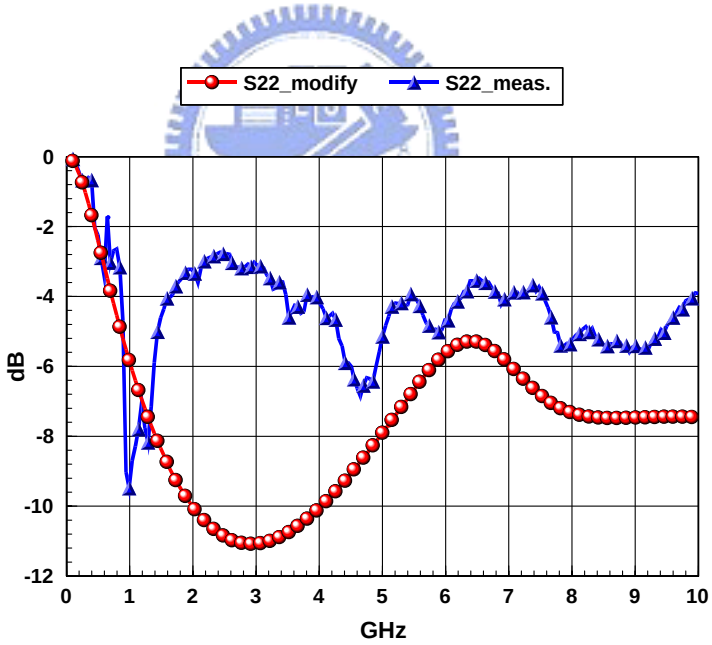


Fig.2.4.11(b) the modified simulation and on-wafer measurement result of S_{22}

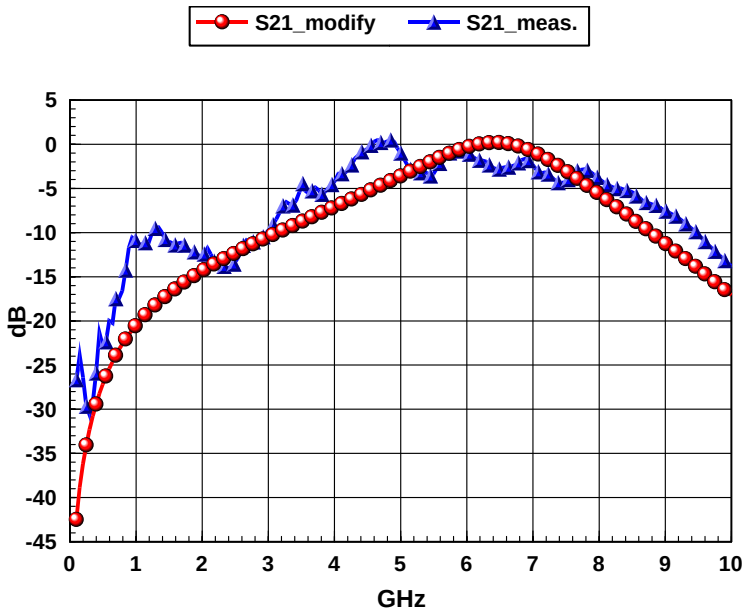


Fig.2.4.11(c) the modified simulation and on-wafer measurement result of S_{21}

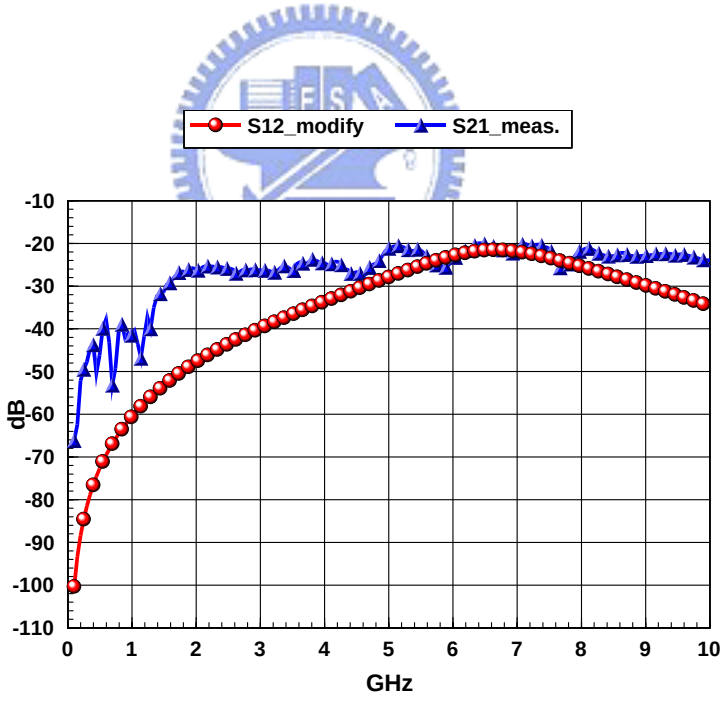


Fig.2.4.11(d) the modified simulation and on-wafer measurement result of S_{12}

According to the above figures it can be found that the issue of non-connection between Vss PAD is the possible problem of this circuit. Thus we use the external PCB board to connect the Vss PAD. The PCB trace and bond wire induce additional parasitical effect. The trace on the board can be approximate microstrip line. The height of substrate is 0.8mm,

dielectric is 4.4 and loss tangent is 0.02. The metal is copper which conductivity is $5.8x10^7$. The inductor of bond wire is above 0.8nH/mm. The Fig. 2.4.12 shows the approximately simplified circuit of the chip bonded on PCB board. The PCB layout is shown in Fig. 2.4.13. The photo of the PCB board and bonded chip is shown in Fig.2.4.14

We consider the bond-wire and PCB-trace effect and the modified simulation result are shown in Fig. 2.4.15(a)~(d). The modified simulation and PCB board measurement results of S_{11} ,S_{22} and S_{12} have the same pattern although it still exist a little difference.

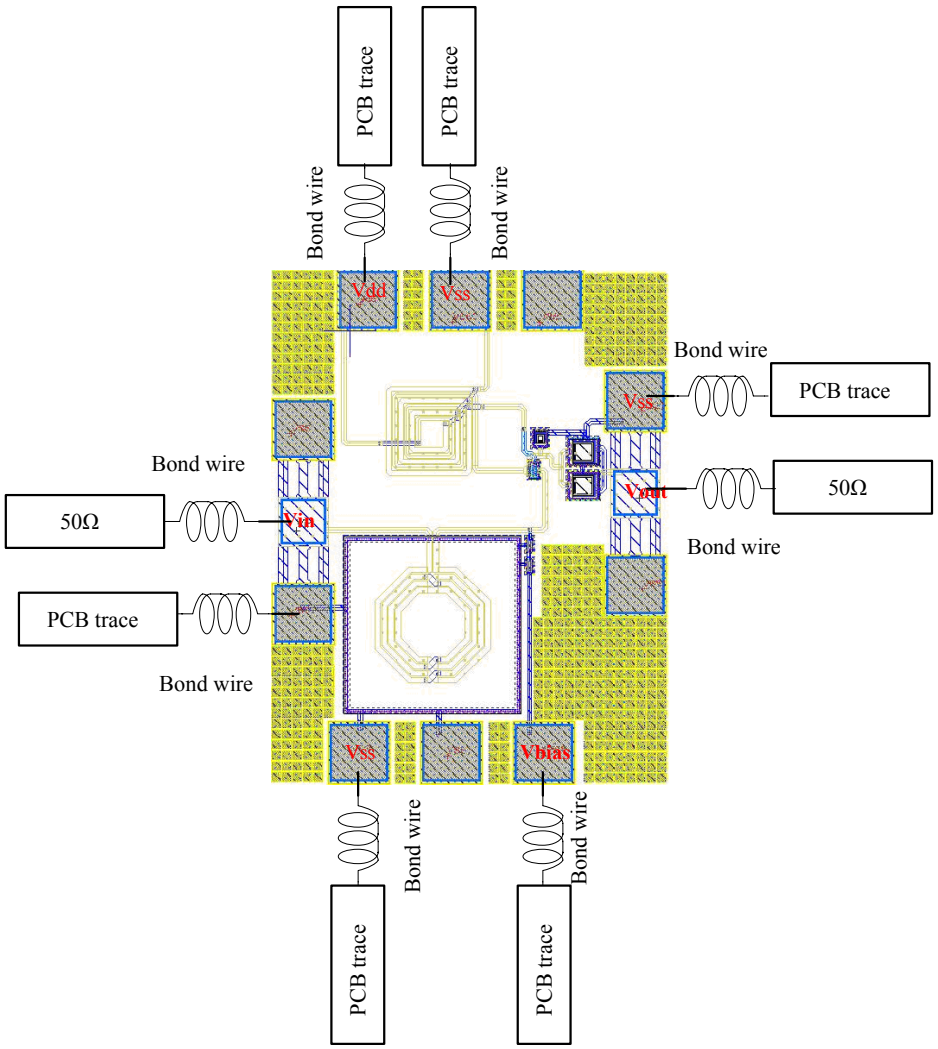


Fig. 2.4.12 the equivalent circuit of chip boned on the PCB board.

Fig. 2.4.13 PCB layout

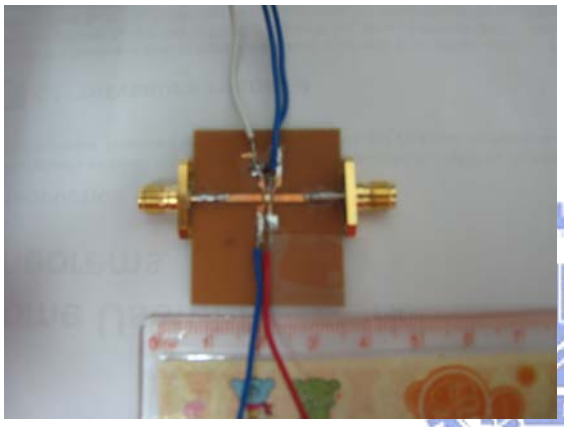


Fig. 2.4.14 (a) photo of PCB board

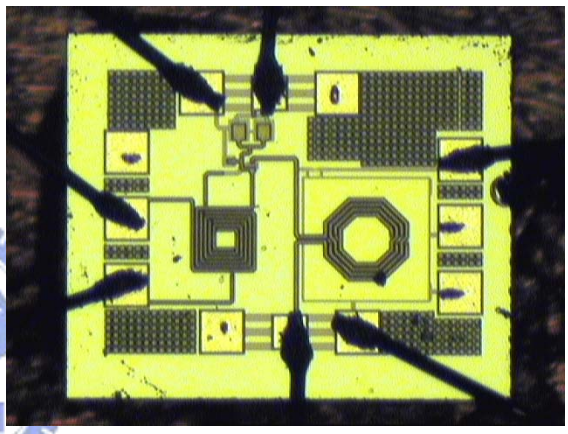


Fig. 2.4.14 (b) photo of bonded chip.

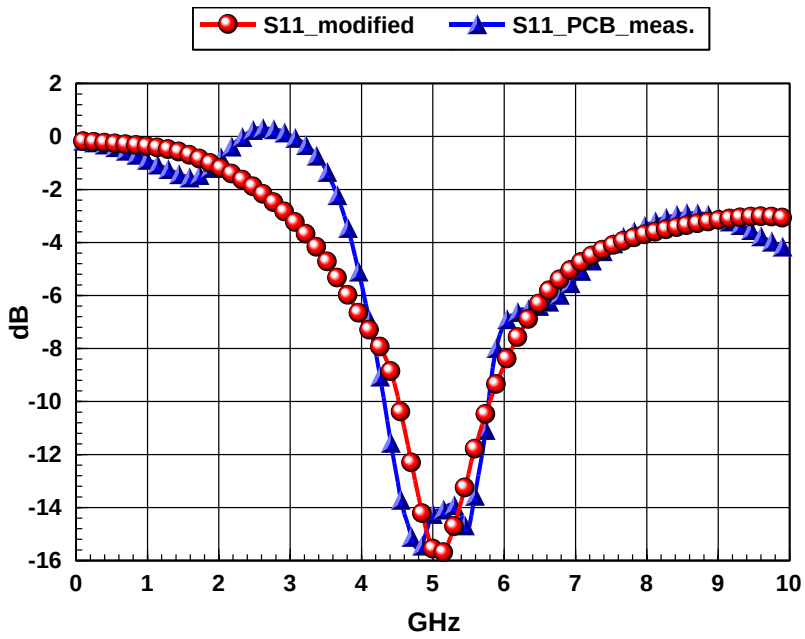


Fig. 2.4.15 (a) modified and PCB_meas. result of S_{11}.

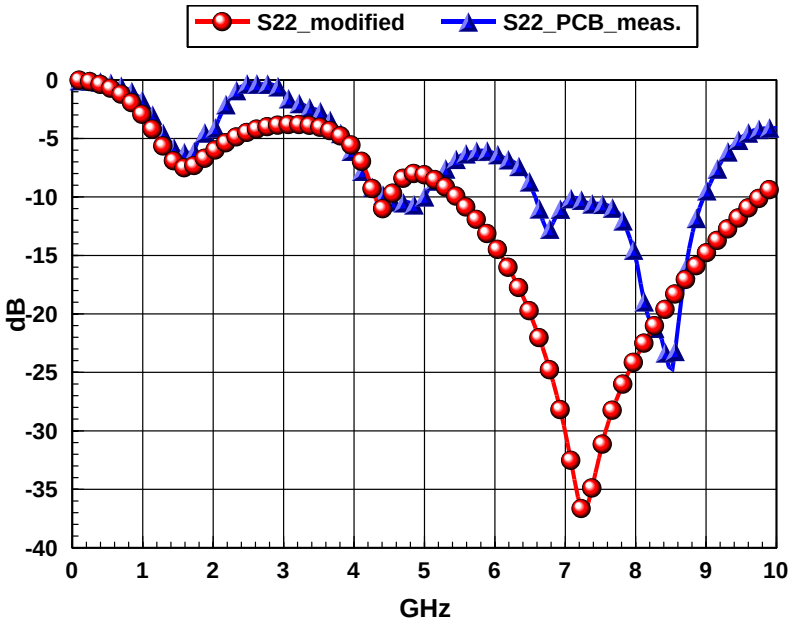


Fig. 2.4.15 (b) modified and PCB_meas. result of S_{22}.

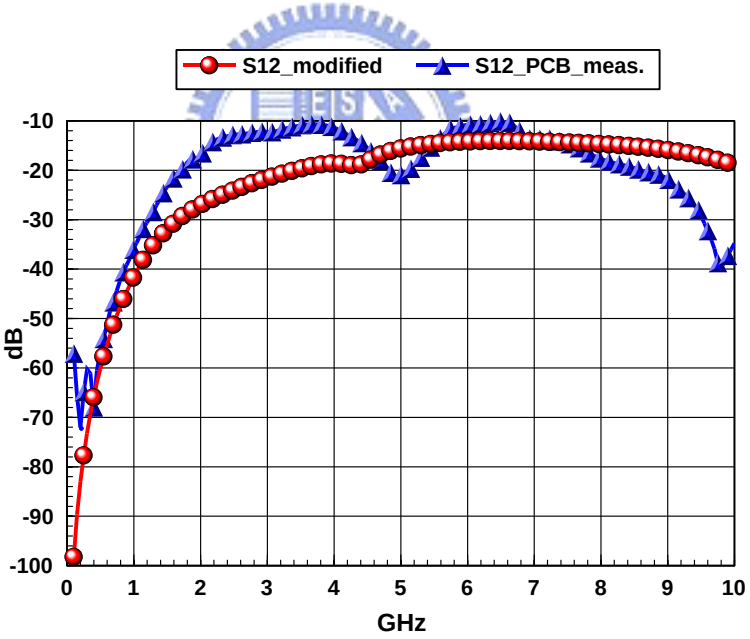


Fig. 2.4.15 (c) modified and PCB_meas. result of S_{12}.

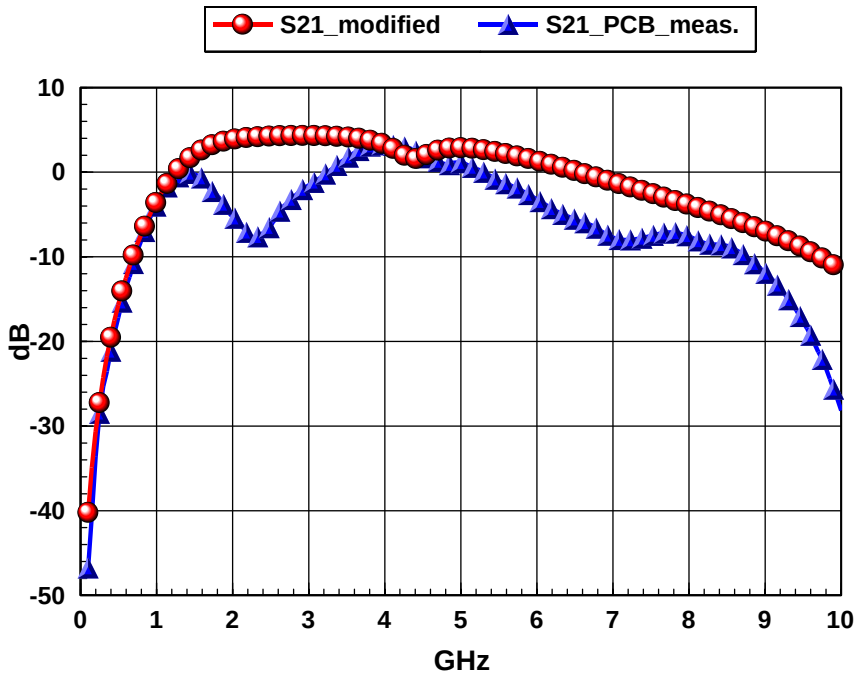


Fig. 2.4.15 (d) modified and PCB_meas. result of S_{21}.

2.4.4 Comparisons

Table 2.4.2 shows the comparisons of this work simulation result and recent LNA papers.

Table 2.4.2 The comparisons of this work simulation result and recent LNA papers.

	Tech.	Freq. (GHz)	S11(dB)	S22(dB)	S21(dB)	NF(dB)	IIP3 (dBm)	Vdd(V)	Power (mW)
this work	0.18μm CMOS	5.8	-20	-24	10.2	3.4	-3	0.7	4.6
[27]	0.18μm CMOS	5	-15	-21	20	1.4	-29	0.65	1.9
[3]	0.18μm CMOS	5.75	<-10	-8	14.2	0.9	0.9	1	16
[28]	0.18μm CMOS	5.8	-5.3	-10.3	13	2.5	-	1	22

Chapter 3 3.1-10.6GHz CMOS Ultra-wideband low noise amplifier

3.1 Introduction

The ultra-wideband (UWB) system is a new wireless technology capable of transmitting data over a wide spectrum of frequency bands approved by Federal Communication Commission (FCC) in 2002. Because the UWB system transmits information using very low power and high date rate over a wide band, it becomes more and more popular for wireless communication. The UWB standard IEEE 802.15.3a is defined by FCC, and most of the proposed applications are allowed to transmit in a band between 3.1- 10.6GHz due to its versatility in almost all of the approved UWB application. Because FCC doesn't define all spectrums completely various methods can be employed to utilize the vast spectrum. Two proposal have been refined for the final decision: Direct-sequence UWB(DS-UWB) and multi-band orthogonal frequency division multiplexing UWB(MB-OFDM UWB). The DS-UWB divides the 3.1-10.6GHz band into two discontinuous bands while the MB-OFDM UWB proposal divides the whole band into 14 528-MHz sub-bands that are grouped into five main bands. In many ways, UWB benefits from existing wireless techniques and standards, as modulation schemes, multiple-access techniques, and transmitter/receiver architectures are adapted for UWB.

3.2 Numerous topology of UWB LNA

The noise performance of an LNA is directly dependent on its input matching. The wide-band input matching is intrinsically noisier than narrow-band counterparts as the noise performance can not be optimized for a specific frequency. Thus the designer has to be trade off between

the input matching and noise. The Fig. 3.2.1 shows four basic 50Ω input matching techniques[5][6][7][8][9].

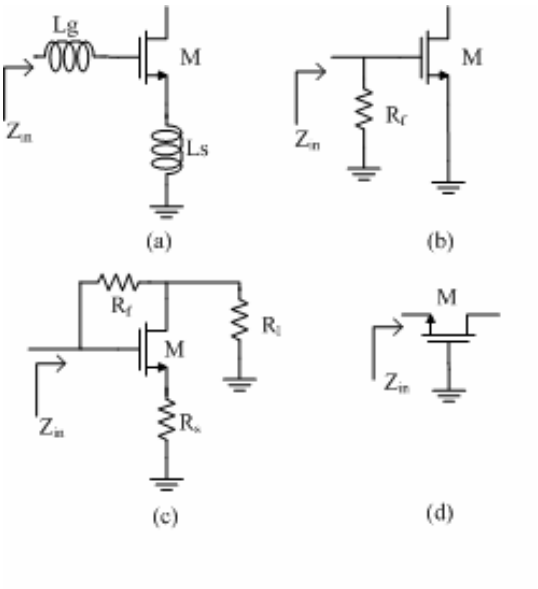


Fig. 3.2.1 Basic input matching topology. (a)Inductive source degeneration.(b)Direct resistor termination.(c)Shunt-series feedback.(d)Common-gate 1/gm termination

The four input matching is only suit for narrow band amplifier. In wireless mobile communications systems, silicon integrated circuits have been widely employed in narrow-band systems, where limited gain and increased parasitic is tolerable due to lower operation frequency and the application of tuned networks.

There are few examples of development of high-frequency wideband amplifiers employing silicon transistors, in particular in CMOS technology.

- Distributed amplifiers [10]

The Fig. 3.2.2 shows a basic four-stage single-ended distributed amplifier.

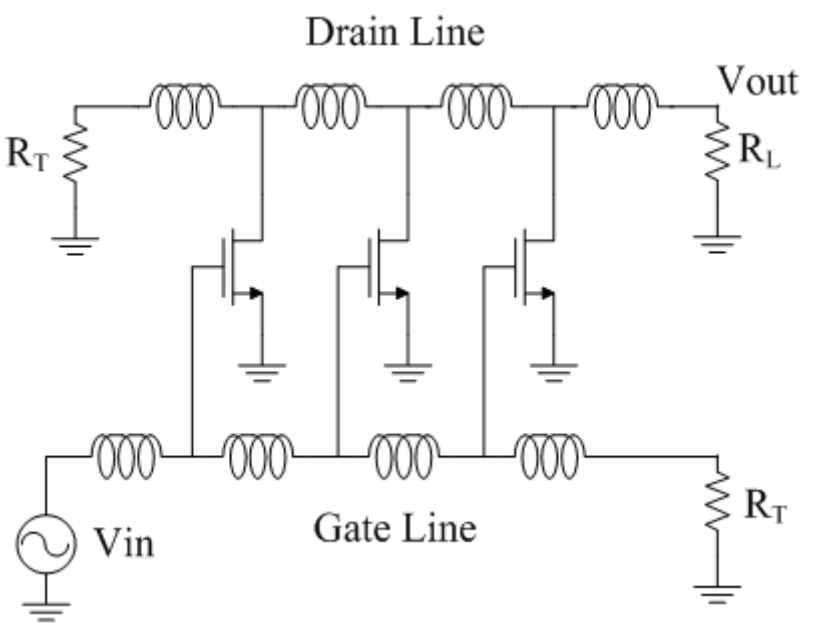


Fig. 3.2.2 Basic four single-end distributed amplifier

The distributed amplifiers normally provide wide bandwidth characteristics but they consume large dc current due to the distribution of multiple amplifying stages, which make them unsuitable for low-power application. And the distributed amplifiers are not optimized for noise. This bring the challenge of finding a low-power topology that satisfies all the other design requirements, the most stringent one being the input match.

- Resistive shunt-feedback amplifiers

In Fig. 3.2.3 a conceptual schematic of a shunt feedback amplifier is shown[11].

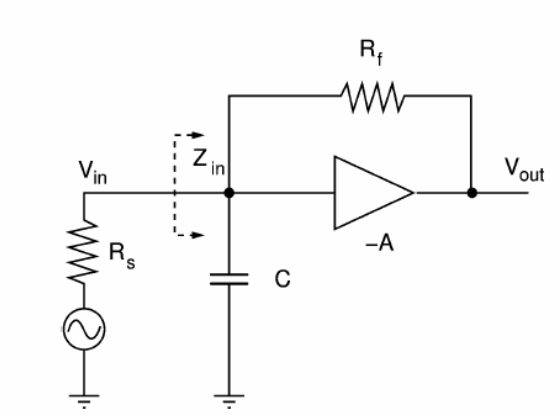


Fig. 3.2.3 Conceptual schematic of a shunt feedback amplifier.

In the resistive shunt-feedback amplifier, input resistance is determined by the feedback

resistance divided by the loop-gain of the feedback amplifier. The input impedance is $Z_{in}(s) = \dfrac{R_f \big/ (1+A)}{1+s\left[R_f \big/ (1+A)\right]}$,where the gain A is chosen such that $R_f \big/ (1+A) = R_s$ .The resistive shunt-feedback amplifier has better bandwidth than conventional low noise amplifier but it has limited input match at higher frequencies due to the parasitic input capacitance. As consequence, the maximum input capacitance that can be tolerated to achieve an input reflection coefficient equal to -10dB at f = 10 GHz is as low as $C = (1/\pi R_s f)\sqrt{|\Gamma|^2 / (1-|\Gamma|^2)}$=200fF. To satisfying this requirement with a CMOS amplifier stage while achieving sufficient gain and low noise is difficult. Some paper has been present by using this topology over the low band of UWB(3-5GHz)[12] shown in Fig.3.2.4.

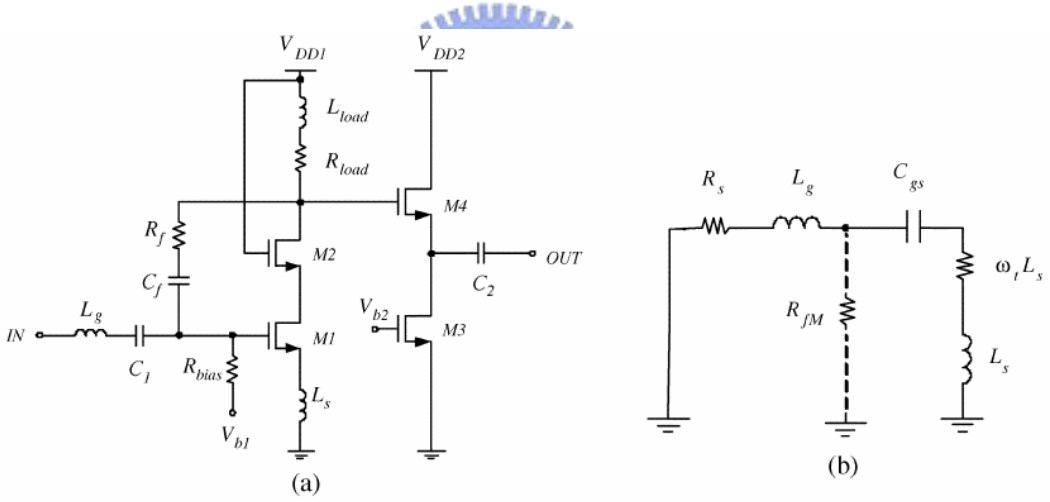


Fig. 3.2.4 UWB LNA topology. (a) Overall schematic. (b) Small-signal equivalent circuit at the input.

In this topology, one of the key role of the feedback resistor R_f is to reduce the Q-factor of the resonating narrowband LNA input circuit. The Q-factor of the circuit can be approximately given by $Q_{WB} \approx \dfrac{1}{\left[Rs + \omega_t L_s + \dfrac{(\omega_0 L_g)^2}{R_{fM}}\right] \cdot \omega_0 \cdot C_{gs}}$. According to this equation, the narrowband LNA input matching can be converted into a wideband amplifier by the proper

selection of R_f. The feedback resistor helps to extend the bandwidth of the amplifier as well as the gain flatness, while contributing a small amount in NF degradation.

- Ultra-wideband low noise amplifier using LC-ladder filter input matching network [11][13]

Recently another topology of wideband LNA has been present. It expands the conventional narrow-band LNA using source degeneration by embedding the input network of the amplifying device in a multisection reactive network so that the overall input reactance is resonated over a wider bandwidth. Fig. 3.2.5 shows a typical narrowband cascade LNA topology and its small-signal equivalent circuit.

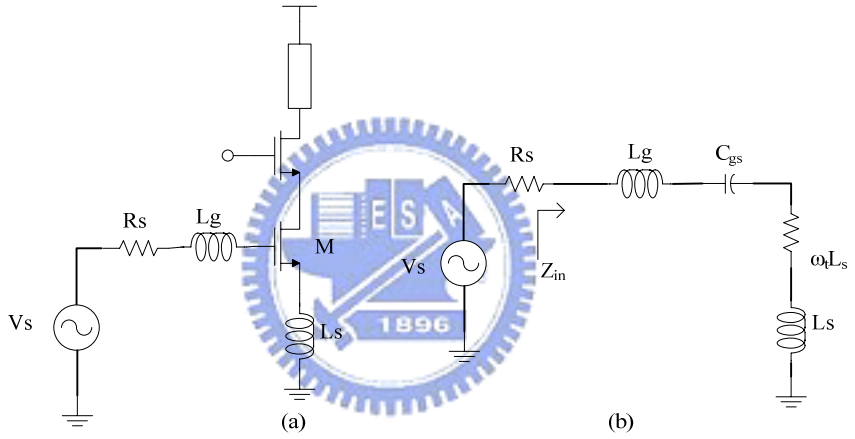


Fig. 3.2.5. Narrowband LNA topology. (a) overall schematic. (b) Small-signal equivalent circuit at the input

The inductor L_s is added for simultaneous noise and input matching and L_g for the impedance matching between the source resistance R_s and the input of the narrowband LNA[14]. Fig. 3.2.5(b) shows the equivalent small-signal circuit. Assume the gate-drain C_{gd} can be ignore the impedance of the gate terminal is a series RLC circuit. The reactive part of the input impedance is resonated at the carrier frequency in narrowband design. The basic concept of the LC-ladder input matching is expanded from the input impedance of the narrowband which is a series RLC circuit. Consider a fourth-order bandpass ladder filter, shown as in Fig. 3.2.6.

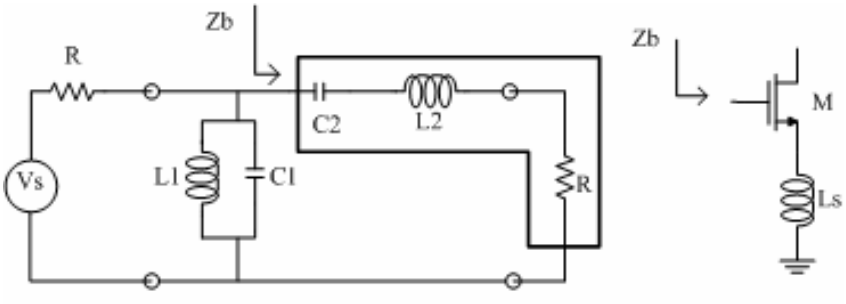


Fig. 3.2.6 Fourth-order bandpass ladder filter used for impedance matching.

The right part of the bandpass filter looks similar to the equivalent circuit of the inductively degenerated transistor in Fig. 3.2.5(b). Therefore, the bandpass filter can embed the inductively degenerated transistor and obtain the desire input impedance. The LC-ladder filter input matching of wideband LNA has two significant drawbacks. Because the LC-ladder filter at the input mandates a number of reactive elements, which could lead to a larger chip area and noise figure degradation in the case of on-chip implementation.

- Ultra-wideband low noise amplifier using the common-gate as the first stage.[15]

The common-gate architecture that is illustrated in Fig. 3.2.1(d) has highest potential to achieve the wide-band input matching. In traditional narrow-band receiver the common-gate is not used widely due to its relatively lower gain and higher noise figure than a common-source amplifier. The actual configuration of common-gate stage is shown in Fig. 3.2.7(a).

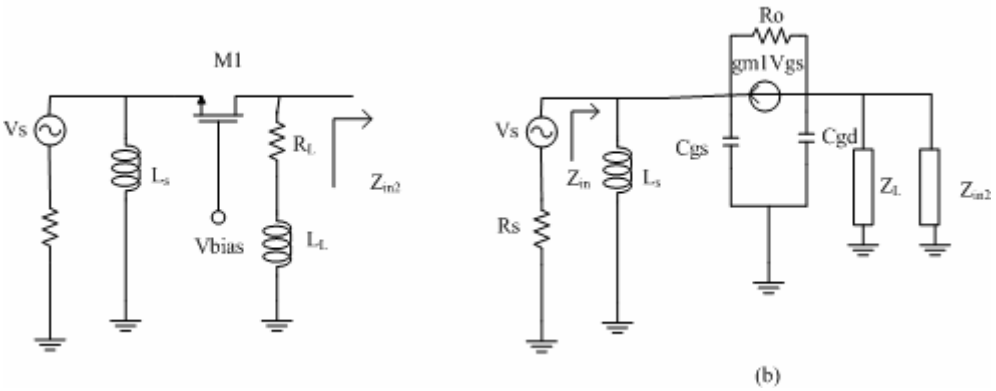


Fig. 3.2.7 (a) Configuration of a common-gate input stage. (b) The small-signal equivalent circuit.

From the Fig. 3.2.7(b),we can derive the input impedance

$$Z_{in} = \frac{1}{g_{m1} + \frac{1}{Z_s(\omega)} + \frac{1 - g_{m1} Z_o(\omega)}{R_o + Z_o(\omega)}} \cong \frac{1}{g_{m1} - j\frac{1}{X_s(\omega)} + \frac{1 - jg_{m1} X_o(\omega)}{R_o + jX_o(\omega)}}$$

In below equation we assume that the $Z_s(\omega)$ and $Z_o(\omega)$ are both composed of high-Q inductors and capacitors and can be regarded as purely reactive within the frequency band of interest. $Z_s(\omega) = j\omega Ls // \frac{1}{j\omega C_{gs}} = jX_s(\omega), Z_o(\omega) = \frac{1}{j\omega C_{gd}} // Z_L // Z_{in2} = jX_o(\omega)$

After some mathematical calculation

$$Z_{in} = \frac{1}{(g_{m1} - \frac{g_{m1}.X_o^2(\omega) - R_o}{R_o^2 + X_o^2(\omega)}) - j(\frac{1}{X_s(\omega)} + \frac{1 + g_{m1}R_o}{R_o^2 + X_o^2(\omega)} \cdot X_o(\omega))}$$

Since $gm1X_o^2(\omega) << R_o^2 + X_o^2(\omega)$,the real part in the denominator will remain relatively constant within the 3.1-10.6GHz UWB band. The imperfect matching of the common-gate stage throughout the band arise from the frequency dependent $Xs(\omega)$ that dominates the imaginary part in the denominator. To get a good matching over the wide band , the LC tank of $Xs(\omega)$ formed by Ls and C_{gs} should be selected such that they resonate at the center of the 3.1-10.6GHz, leaving only a 50Ω real input impedance. The noise figure of the common-gate input stage UWB LNA can be improved by increasing g_{m1} but it will degrade the input matching.

- Reactive-feedback wideband amplifier [16][17]

An alternate approach to the modified UWB LNA is a negative-feedback amplifier. Feedback offers numerous benefits for broadband application, including gain, stability over processing and supply variations, lower distortion and the ability to get port impedances for noise and impedance matching. However the simple feedback stage is difficulty to achieve a 50Ω input match, low noise figure and low power consumption in simultaneous. Broadband resistive feedback also meets the bandwidth target, but the reactive-feedback using transformer contributes less noise as losses are relatively small in the transformer windings. The

schematic shown in Fig. 3.2.8 is present recently [16].

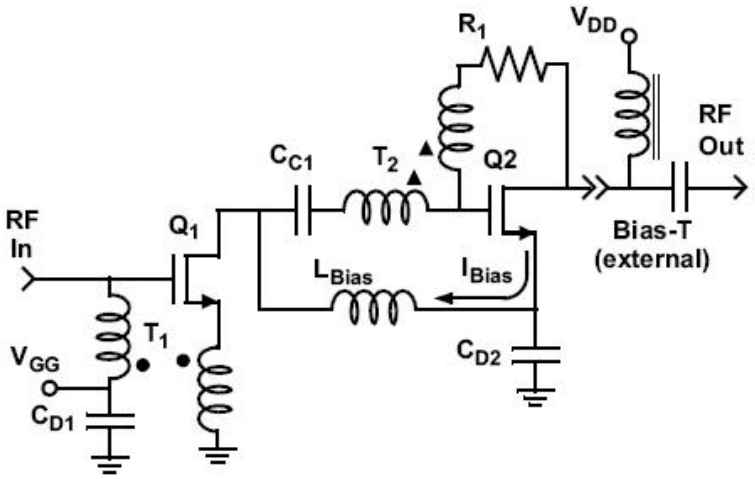


Fig. 3.2.8 Reactive feedback UWB LNA.

The transformer in the first stage give a broadband input match without multi-inductor network which will add noise and require more chip area. The current-reuse is also approved in this design for lower DC power consumption. The transformer of second stage provides a broadband output match relatively close to 50Ω so the output buffer is not need for output match.

- Wideband matching using the transistor intrinsic gate-drain capacitor [18]

Recently a novel wideband input match has been present. It considers the gate-drain capacitor has significant effect on the circuit performance. The Fig. 3.2.9 show a simple common source amplifier with source degeneration inductor and the drain loaded an equivalent capacitor and resistor from the next stage.

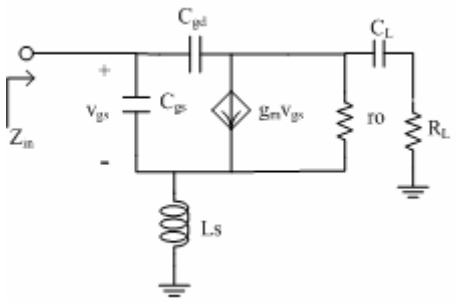


Fig. 3.2.9 The small signal equivalent circuit of common-source with inductive source degeneration

The C_{gd} and r_o are neglected in conventional analysis of low noise amplifier. It is inaccurate numerically. If both C_{gd} and r_o are considered we will find that the input match at high frequency is depend on the resistive load and at low frequency is depend on the capacitive load. We can achieve wideband match without external input match network. It also can achieve low noise match.

3.3 Design consideration

3.3.1 Wideband match technique[18]

Consider a small signal equivalent circuit of a source degeneration low noise amplifier which is shown in Fig.3.3.1 C_L and R_L present the parasitic capacitance and resistance which is contributed from the next stage.

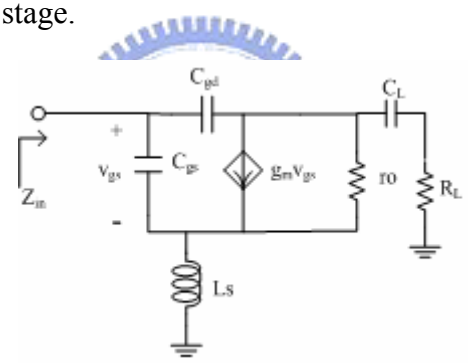


Fig. 3.3.1 The small signal equivalent circuit of source degeneration

To derive the input impedance we consider that the load of the circuit is divided into two parts, one of which is only a resistor R_L which dominates at the high frequency and another is the capacitor C_L dominates at the low frequency. The circuit of resistive loading is shown in Fig. 3.3.2.

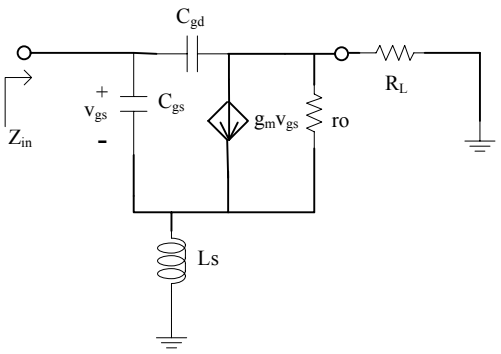


Fig. 3.3.2 The equivalent small signal circuit of resistive loading

While we assume that $\omega L_s << \frac{1}{\omega C_{gs}}$ $\omega L_s << R_L$ we can find the input impedance $Z_{in} \approx (\frac{1}{j\omega C_{gs}} + \frac{L_s \gamma g_m}{C_{gs}})[1 + \frac{C_{gd}}{C_{gs}}(1 + \gamma g_m R_L)]^{-1}$, with $\gamma = \frac{r_o}{r_o + R_L + j\omega L_s}$. As frequency as high the input impedance will approach the 50Ω when the inductor Ls is designed properly. To derive the input impedance of the capacitive loading, which is shown in Fig.3.3.3, we divided this circuit into two branches and replace the current source by voltage source.

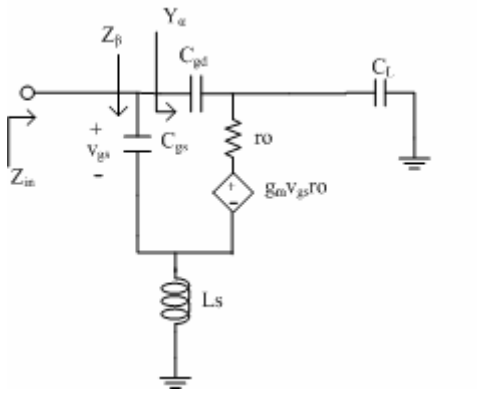


Fig. 3.3.3 The equivalent circuit with capacitive loading

One of the two branches is looking into the capacitor C_{gs} and another is looking into the capacitor C_{gd}. Y_α is the impedance looking into the C_{gd} and Z_β is the impedance looking into the C_{gs}. Assuming that the current flowing the capacitor C_{gd} and C_{gs} is smaller than the induced current $g_m V_{gs}$, the Y_α can be derived. Thus $Y_\alpha = j\omega C_{gd} + (R_\alpha + \frac{1}{j\omega C_\alpha} + j\omega L_\alpha)^{-1}$ and $Z_\beta = \frac{1}{j\omega C_{gs}} + (\frac{1}{R_\beta} + j\omega C_\beta + \frac{1}{j\omega L_\beta})^{-1}$

with $R_\alpha = \frac{C_L}{g_m C_{gd}}$ $C_\alpha = g_m r_o C_{gd}$ $L_\alpha = \frac{L_S C_L}{g_m r_o C_{gd}}(1 + g_m r_o)$

$$R_\beta = \frac{g_m L_s}{C_{gs}} \quad C_\beta = \frac{C_{gs}}{g_m r_o} \quad L_\beta = \frac{L_s g_m r_o C_L}{C_{gs}}$$

The input impedance of the capacitive loading circuit can be found out as follow $Z_{in} = (Y_\alpha + \frac{1}{Z_\beta})^{-1}$. According to above the equations the input impedance can be rearranged as a simpler RLC circuit as shown in Fig.3.3.4.

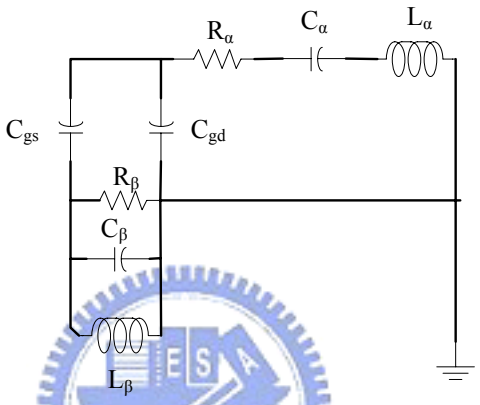


Fig. 3.3.4 the equivalent circuit of the input impedance

The C_{gd} branch is the critical branch that is a series component of RLC and its resonate frequency is $f_0 = \frac{1}{2\pi\sqrt{L_\alpha C_\alpha}} = \frac{1}{2\pi\sqrt{L_S C_L (1 + g_m r_o)}}$. At the high frequency the resistive loading is matched and the capacitive loading is matched at the comparatively low frequency. Thus the composite $R_L C_L$ load circuit is matched over a wide bandwidth.

3.3.2 3.1-10.6GHz CMOS Ultra-wideband low noise amplifier

Fig. 3.3.5 shows a UWB LNA using transistor's intrinsic gate-drain capacitor to achieve input matching. In this design we add an inductor to the original $R_L C_L$ loading circuit, as shown in figure Fig. 3.3.6.

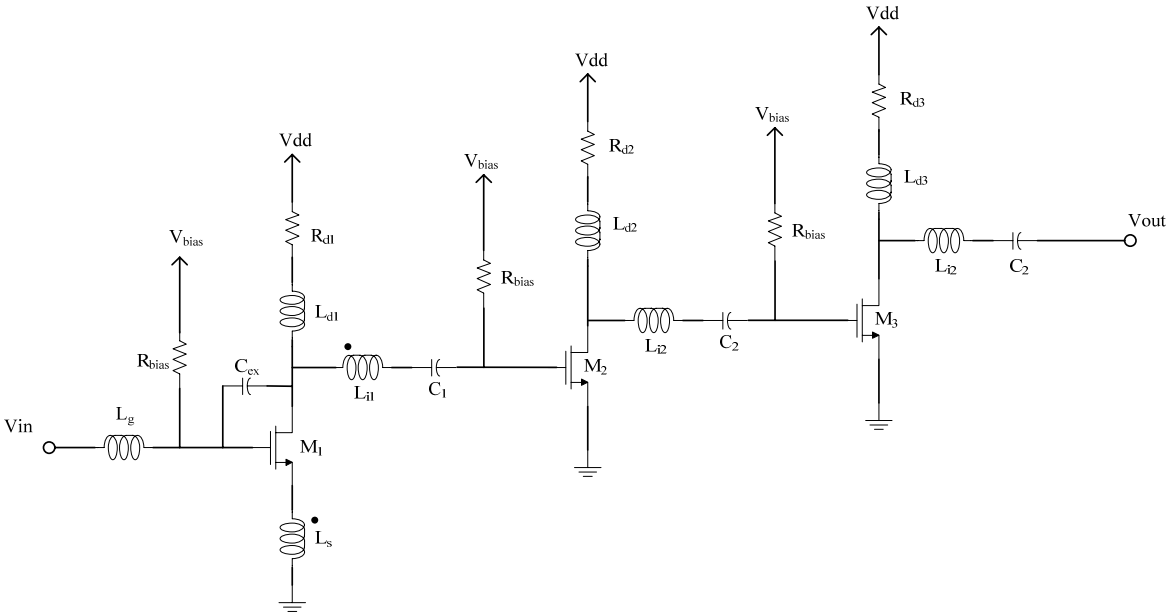


Fig. 3.3.5 The schematic of proposed UWB LNA

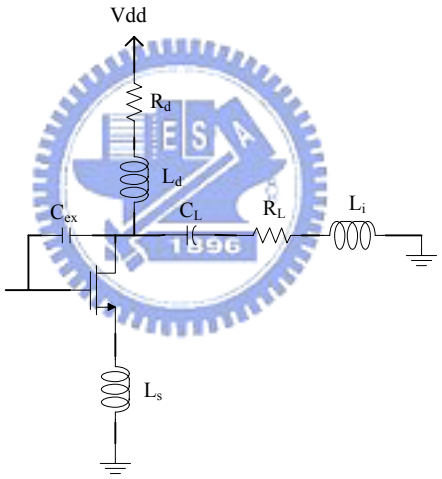


Fig. 3.3.6 The equivalent circuit of the first stage UWB LNA

In this circuit the external C_{ex} is added to increase the equivalent gat-drain capacitance, thus allowing a smaller transistor to get better input match but it effect the noise figure at lower frequency. The inductor L_i can improve the input matching. From the simulation result we can find add the inductor can help S_{11} contour around the original point (i.e. 50Ω) in the smith chart. The Fig. 3.3.7 shows this simulation result.

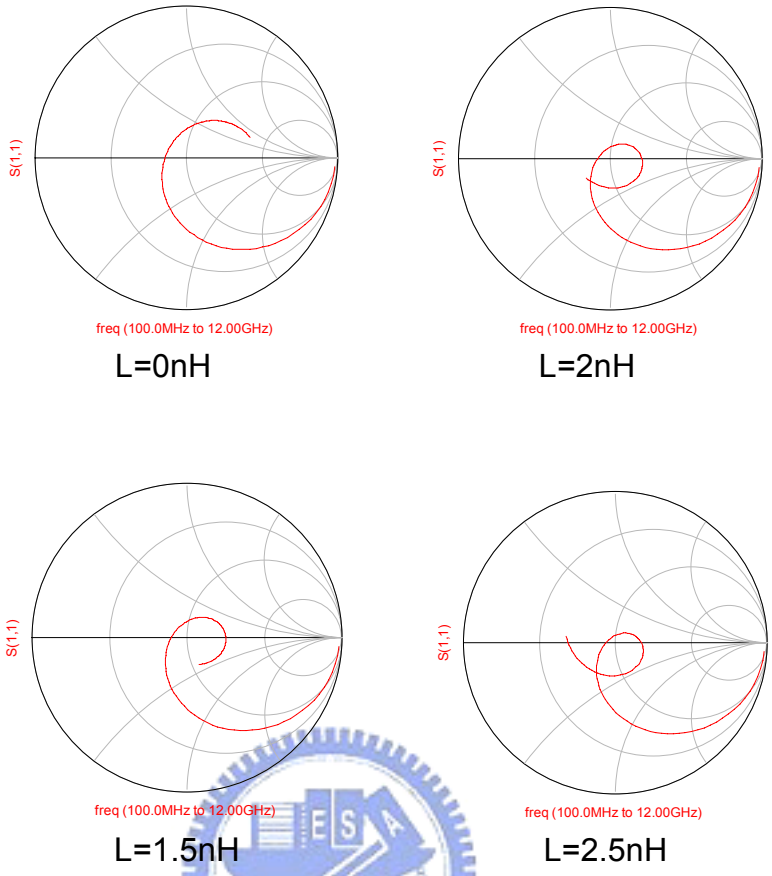


Fig. 3.3.7 The input return loss for different Li

To improve the input match at lower frequency the gate inductor is added and it will influence the noise figure. Shunt-series-peaking is a bandwidth extension technique [19] which is used in this circuit to extend bandwidth by the inductor L_d, L_i and resistor R_d. To achieve a flat gain over whole frequency range we cascade three stages.

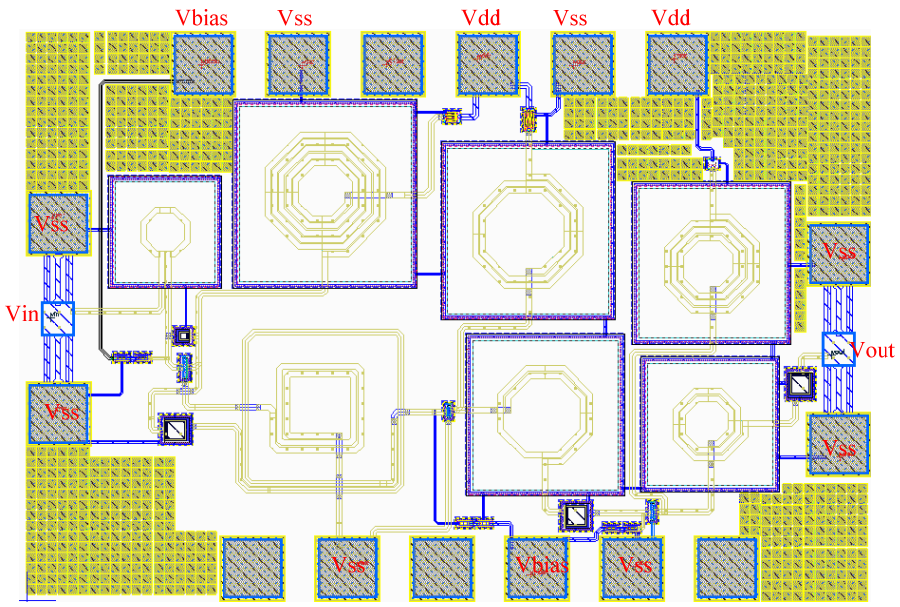
The concept of this design is that we design the first stage with a capacitive, resistive and inductive load to achieve the input return loss first. The transformer is added to improve the input retune loss and flatter gain but it may make the circuit become a little unstable and it has to be design carefully. The value of capacitive load is approximated to the next input impedance of next stage. Due to the input impedance of the common source topology is the series resistance, capacitor and inductor it is suited to be the consequence stage. We use the common source topology to be the second and third stage. Then we replace the resistance by

the common source stage with a capacitive, inductive and resistive load and fine tune all element to get input return loss and output return loss. And the third stage is designed by the same way. Finally we fine tune the drain inductor to improve the flatter gain. The three stages are response for different band of gain to maintain the flatter gain over whole wide band.

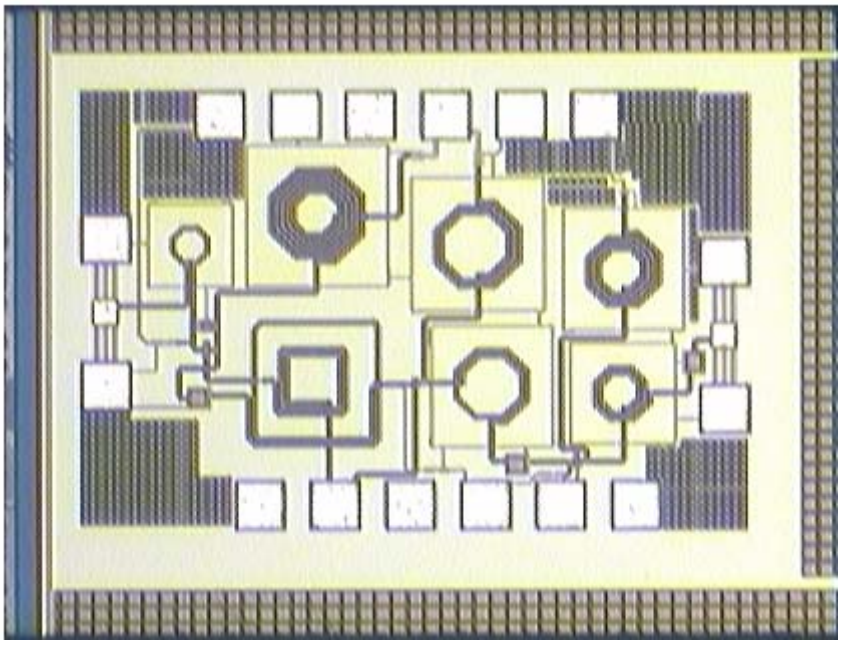
3.4 Chip implementation and measurement results

3.4.1 Layout considerations

The chip layout and photo of the UWB LNA is shown in Fig. 3.4.1. The power supply (Vdd) is 1V. The 0.18μm (minimum) gate length was chosen to get the highest speed. The MIM (Metal-Insulator-Metal) capacitors without shield and hexagonal spiral inductors (the Q-value is below 18) are used in this work. Guard-rings are added with all elements to prevent substrate noise and interference. A shielded signal GSG pad structure is used in RF input and RF output to reduce the coupling noise from the noisy substrate. All interconnections between elements are taken as a 45° corner. The RF input and the RF output are placed on opposite sides of the layout to avoid the signals coupling. The chip size is 1.314x0.89mm^2. All connection wire are simulated by ADS momentum to extract parasitical effect.



(a)



(b)

Fig. 3.4.1(a) chip layout (b) chip photo of UWB LNA.

3.4.2 Measurement considerations

The UWB LNA is designed for on-wafer measurement so the layout must follow the rules of CIC's (Chip Implementation Center's) probe station testing rules. This circuit needs four 3-pin DC PGP probe and two RF GSG probes for on-wafer measurement. A large coupling capacitor is needed in the input of the LNA to isolate the dc between circuit and equipment. Fig. 3.4.2 ~ Fig. 3.4.5 show the measurement setup for S-parameters, noise figure, 1dB compression point and third-order intercept point. We will discuss the experimental and simulation results of this circuit in following sections.

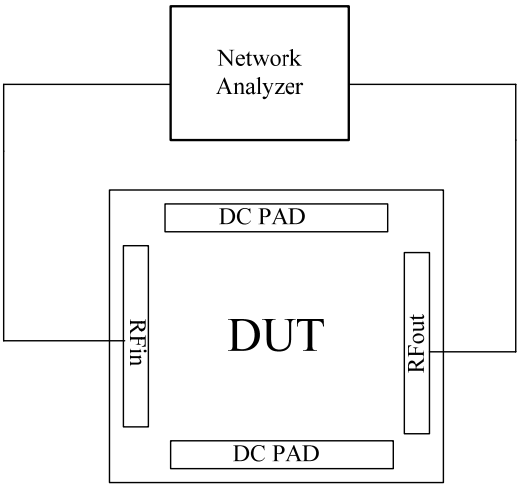


Fig. 3.4.2 Measurement setup for S-parameters

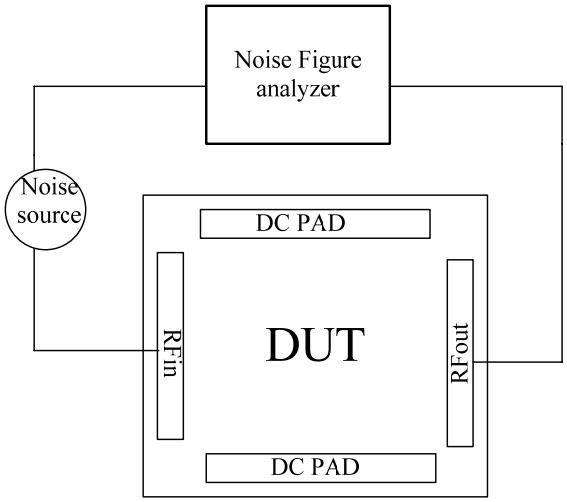


Fig. 3.4.3 Measurement setup for noise figure

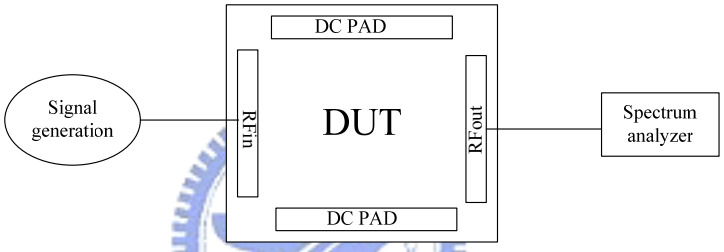


Fig. 3.4.4 Measurement setup for P1dB

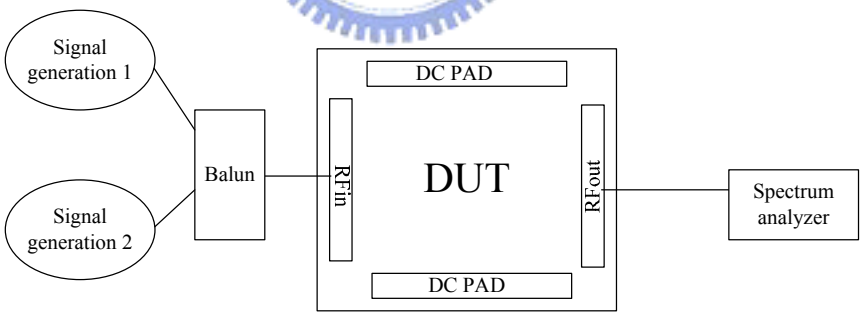


Fig. 3.4.5 Measurement setup for IIP3

3.4.3 Measurement results and discussion

The Ultra-wideband low noise amplifier is simulated by ADS. The simulation and measurement results are shown in Fig. 3.4.6(a)~(d), where the simulation S_{11} < -10dB and S_{22}<-10dB from 3.1GHz to 10.6GHz. The simulation maximum and minimum power gain (S_{21}) are 13.2dB at 4.4GHz and 12.138dB at 10.6GHz, respectively

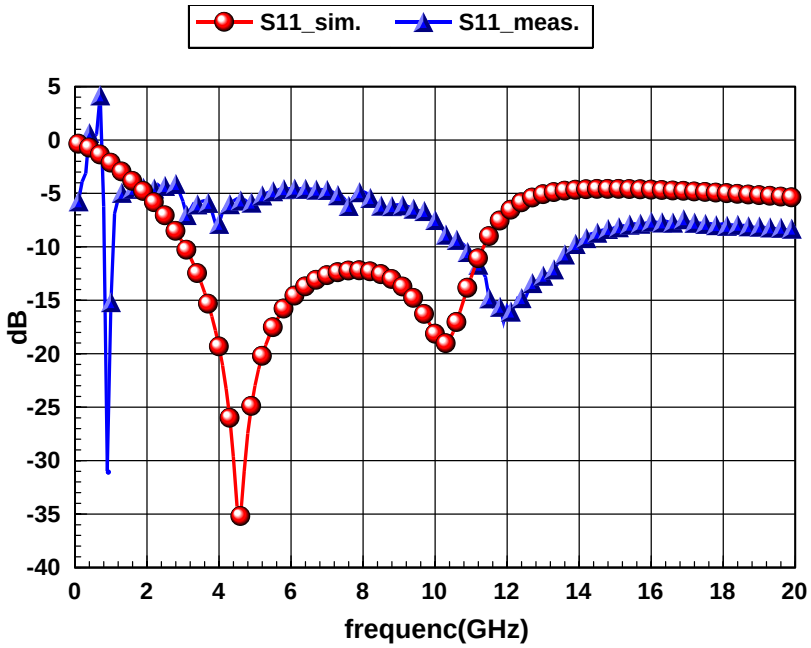


Fig. 3.4.6(a) simulation and measurement result of S_{11}

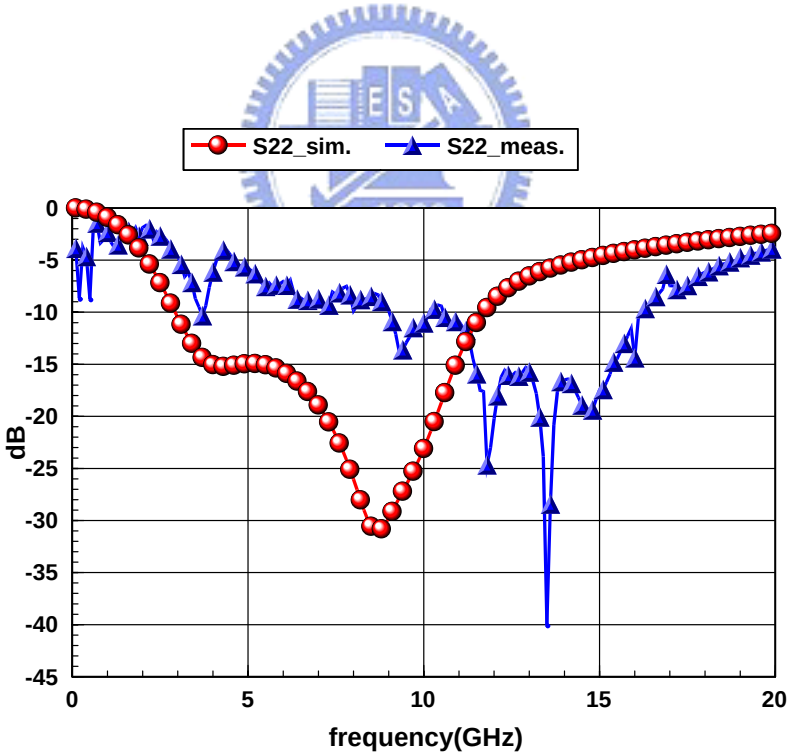


Fig. 3.4.6(b) simulation and measurement result of S_{22}

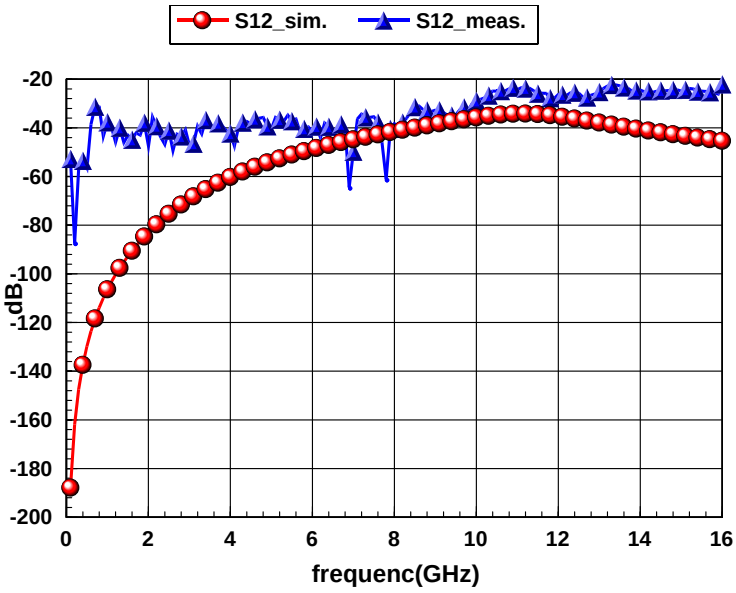


Fig. 3.4.6(c) simulation and measurement result of S_{12}

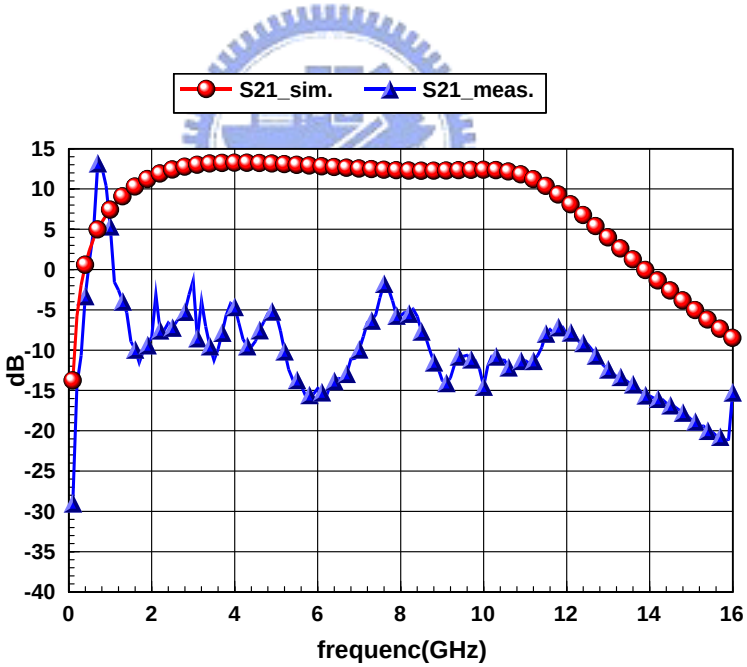


Fig. 3.4.6(d) simulation and measurement result of S_{21}

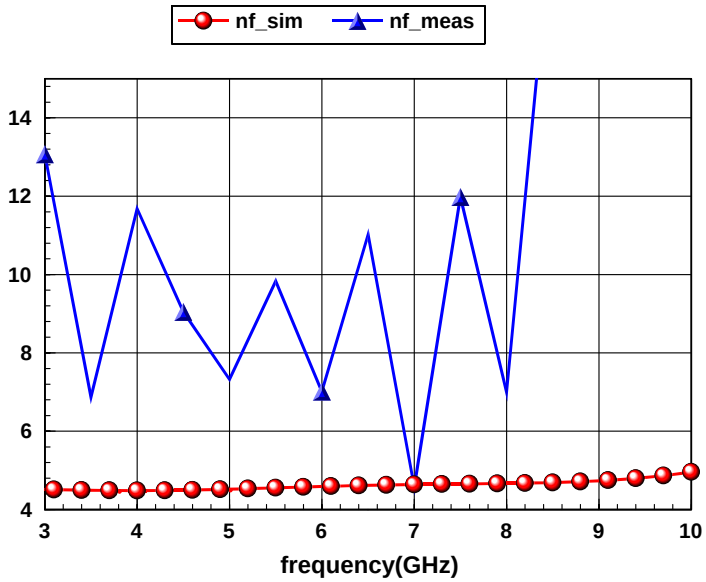


Fig. 3.4.6(e) simulation and measurement result of NF

The simulation and measurement result of P1dB are shown in Fig. 3.4.7 (a)~(c).

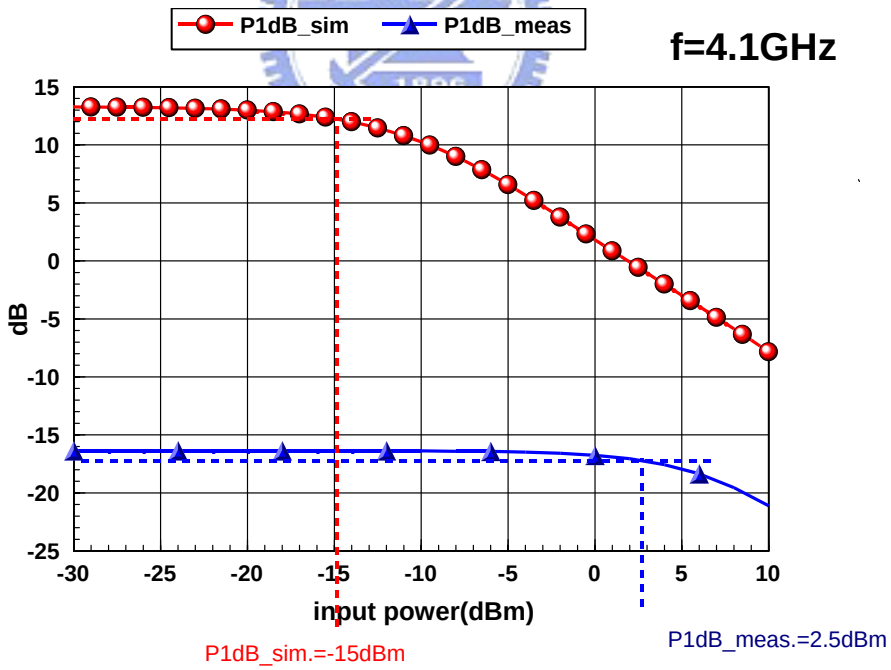


Fig. 3.4.7(a) simulation and measurement result of P1dB at 4.1GHz

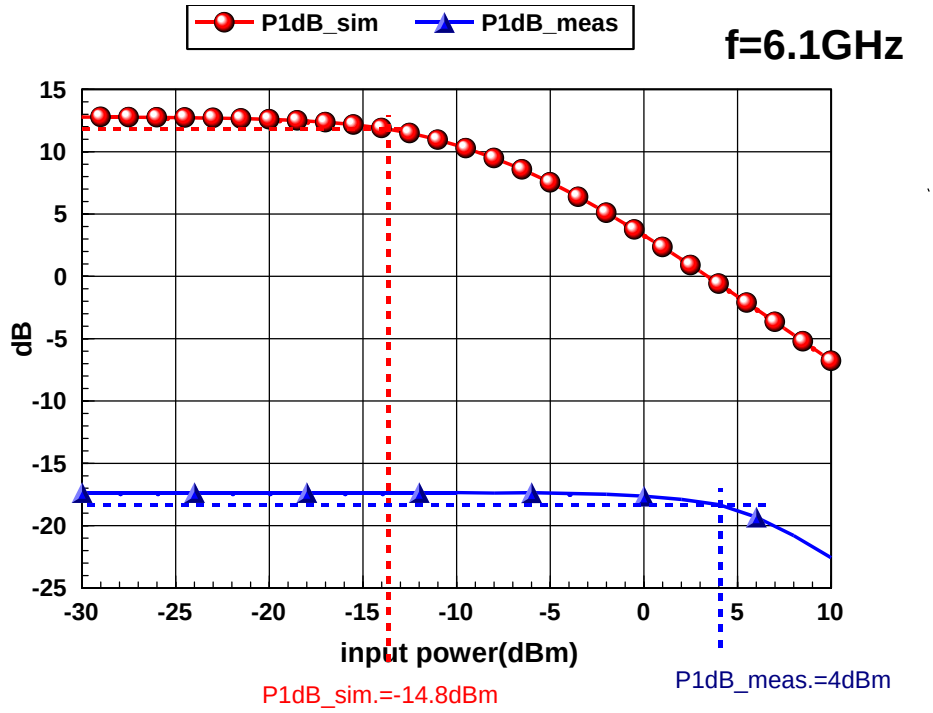


Fig. 3.4.7(b) simulation and measurement result of P1dB at 6.1GHz

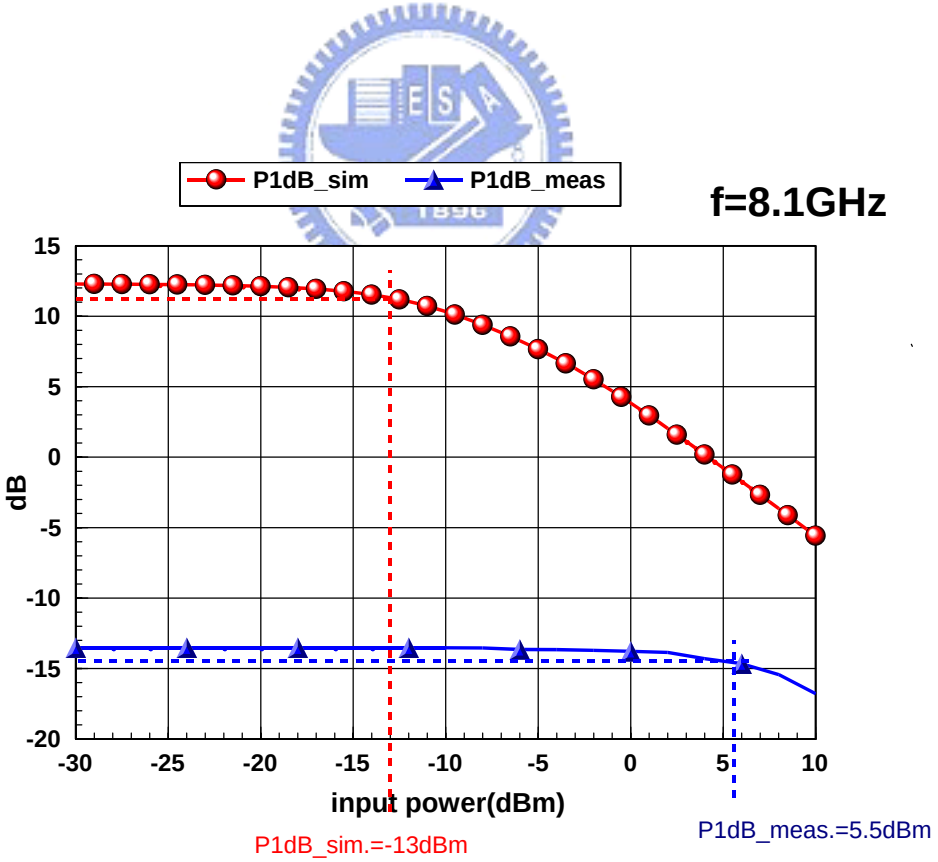


Fig. 3.4.7(c) simulation and measurement result of P1dB at 8.1GHz

The simulation and measurement results of IIP3 are shown in Fig. 3.4.8(a)~(f)

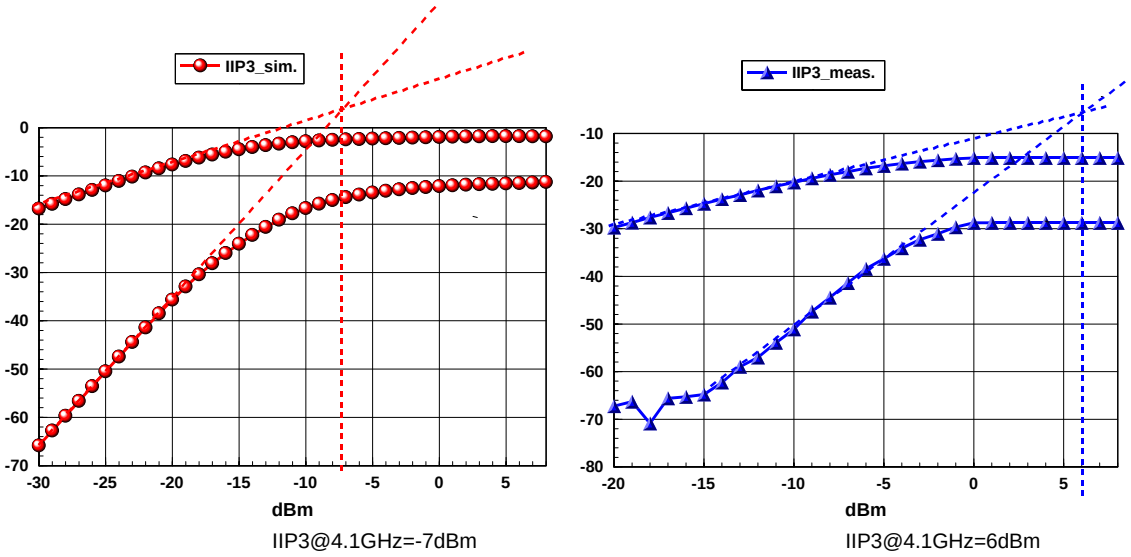


Fig. 3.4.8 (a) the simulation of IIP3 at 4.1GHz (b) the measurement result of IIP3 at 4.1GHz

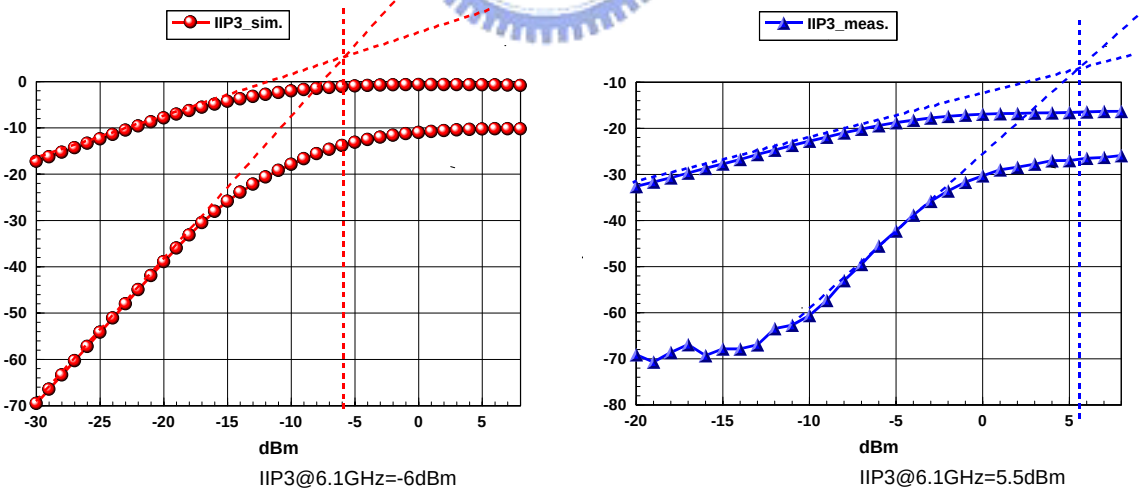
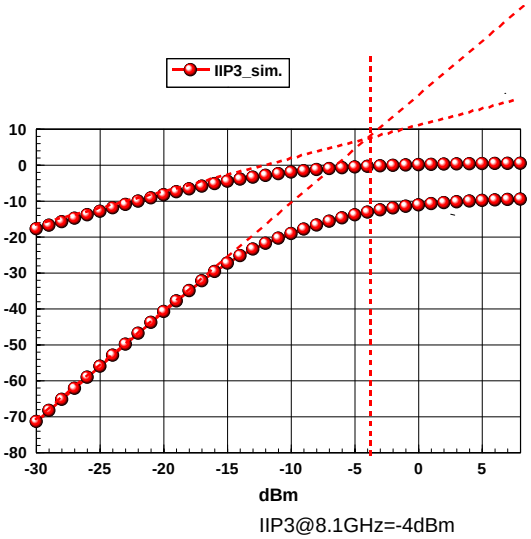


Fig. 3.4.8 (c) the simulation of IIP3 at 6.1GHz (d) the measurement result of IIP3 at 6.1GHz



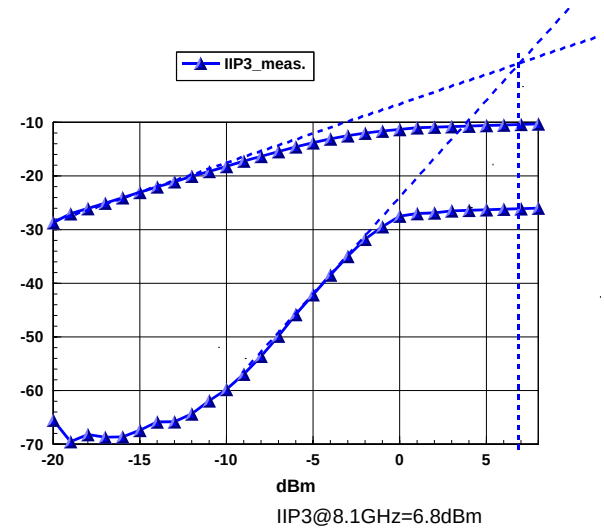


Fig. 3.4.8 (e) the simulation of IIP3 at 8.1GHz (f) the measurement result of IIP3 at 8.1GHz

The simulation and measurement result is summary in Table 3.4.1.and comparison with recent papers in Table 3.4.2.

Table 3.4.1 Performance summary of Ultra-wideband LNA

Specification	Measurement			Post Simulation		
S11 (dB)	<-5			<-10		
S22 (dB)	<-5			<-10		
S21 (dB)	-10(average)			12dB(flat gain)		
S12 (dB)	<-30			<-40		
Noise Figure (dB)	5(min)			4.5(min.)		
P_{1dB} (dBm)	4.1GHz	6.1GHz	8.1GHz	4.1GHz	6.1GHz	8.1GHz
	2.5	4	5.5	-15	-15	-13
IIP3 (dBm)	6	5.5	6.8	-7	-6	-4
Vdd (V)	1			1		
LNA Power (mW)	17			18.12		

Table 3.4.2 The comparisons of this work simulation result and recent LNA papers.

	Tech.	BW (GHz)	S11 (dB)	S22 (db)	Flat Power Gain (dB)	NFmin (dB)	VDD (V)	Power (mW)
This work simulation	**0.18μm CMOS**	**3.1-10.6**	**<-10**	**<-10**	**12.5**	**4.5**	**1**	**18**
[29]	0.18μm CMOS	2-6.5	<-7.8	N/A	11.9	4.1	1.8	27
[16]	0.13μm CMOS	3.1-10.6	<-9.9	<-6.2	15.1	2.5	1.2	9
[11]	0.18μm CMOS	2.4-9.5	< -9.4	< -10	10.4	4	1.8	9
[15]	0.18μm CMOS	3.1-10.6	<-9	<-13	15.9-17.5	3.1-5.7	1.8	33.2
[17]	0.18μm CMOS	3.1-10.6	<-10	<-10	10.87-12.0	4.7	1.5	10.57

The measurement results reveal that the input return loss is not good and no power gain. We consider the layout of the UWB LNA to find the possible problem. The simplified chart of layout is shown in Fig. 3.4.9.

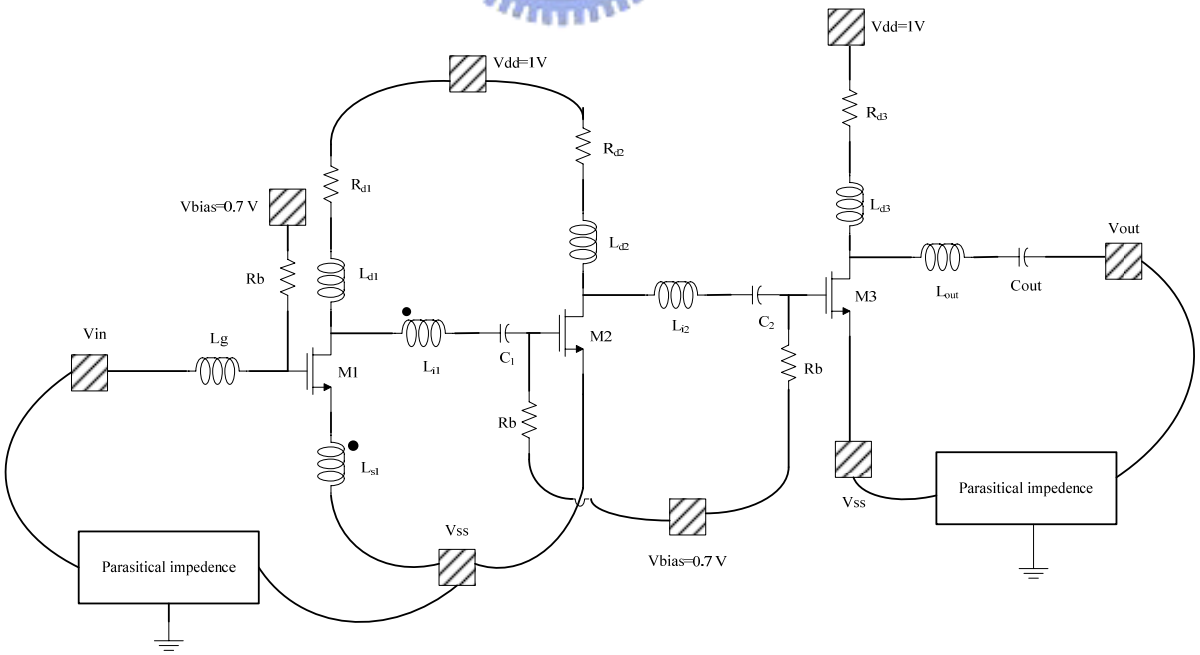


Fig. 3.4.9 simplified chart of UWB LNA layout

We find that the all Vss Pads of internal chip layout are not connected each other. They

connect each other by external measurement machine and along this path may be suffer from some unknown parasitical impedance. Thus it lets the expected ground node to become imperfect ground. We add this parasitic impedance at this Vss node and the modified simulation can reveal that the imperfect ground may effect the performance of this UWB LNA, which is shown in Fig. 3.4.10(a)~(d).

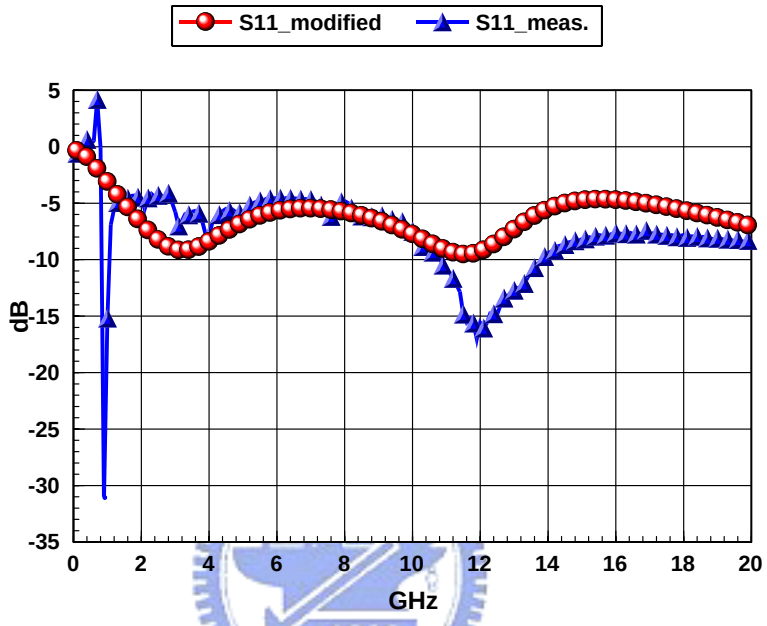


Fig. 3.4.10(a) modified and measurement result of S_{11}.

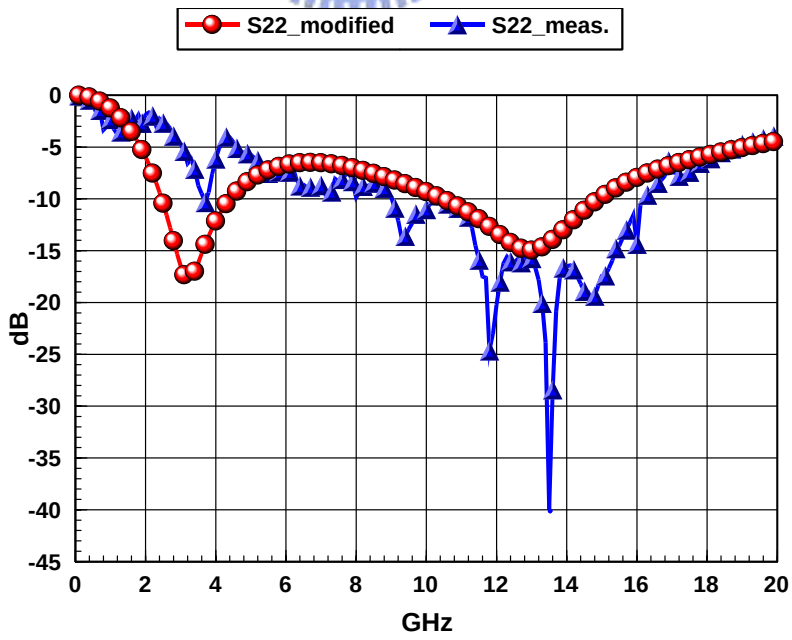


Fig. 3.4.10(b) modified and measurement result of S_{22}

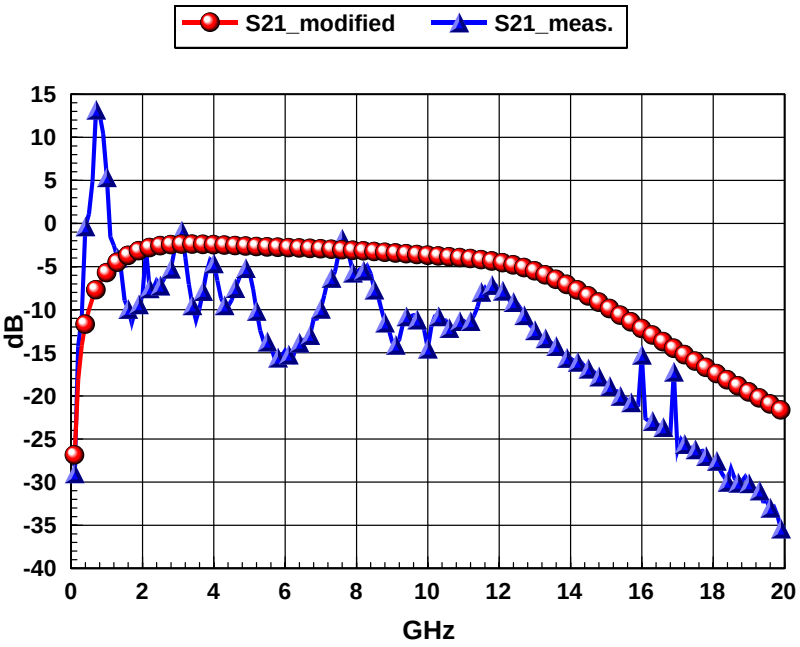


Fig. 3.4.10(c) modified and measurement result of S_{21}

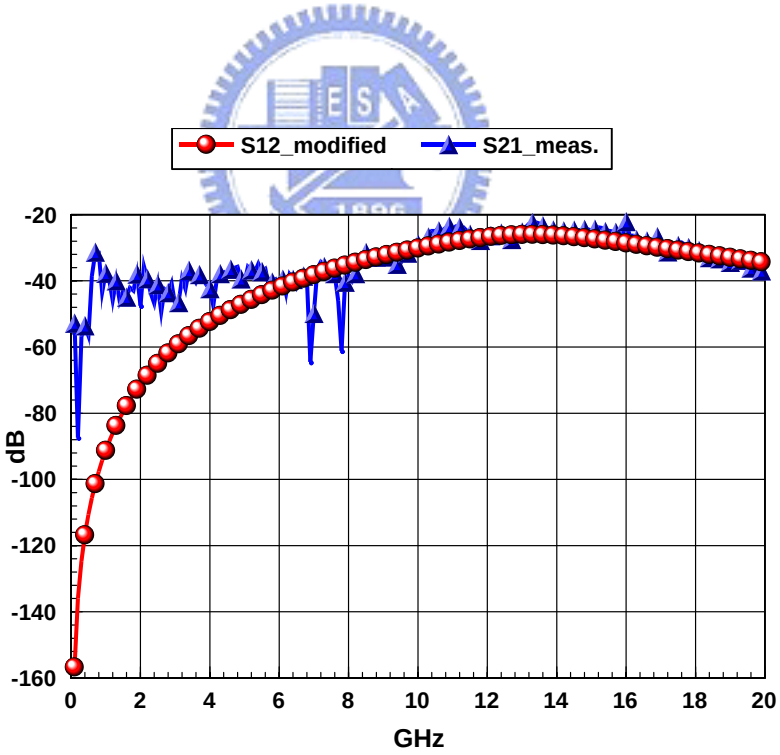


Fig. 3.4.10(d) modified and measurement result of S_{12}

According to the above figures it can be found that the issue of non-connection between Vss PAD is the possible problem of this circuit. Thus we use the external PCB board to

connect the Vss PAD. The PCB trace and bond wire induce additional parasitical effect. The trace on the board can be approximate microstrip line. The height of substrate is 0.8mm, dielectric is 4.4 and loss tangent is 0.02. The metal is copper which conductivity is $5.8x10^7$. The inductor of bond wire is above 0.8nH/mm. The Fig. 3.4.11 shows the approximately simplified circuit of the chip bonded on PCB board. The PCB layout is shown in Fig. 3.4.12. and the photo of PCB board and bonded chip is shown in Fig. 3.4.13(a),(b).

We consider the bond-wire and PCB-trace effect and the modified simulation result are shown in Fig. 3.4.14(a)~(d).

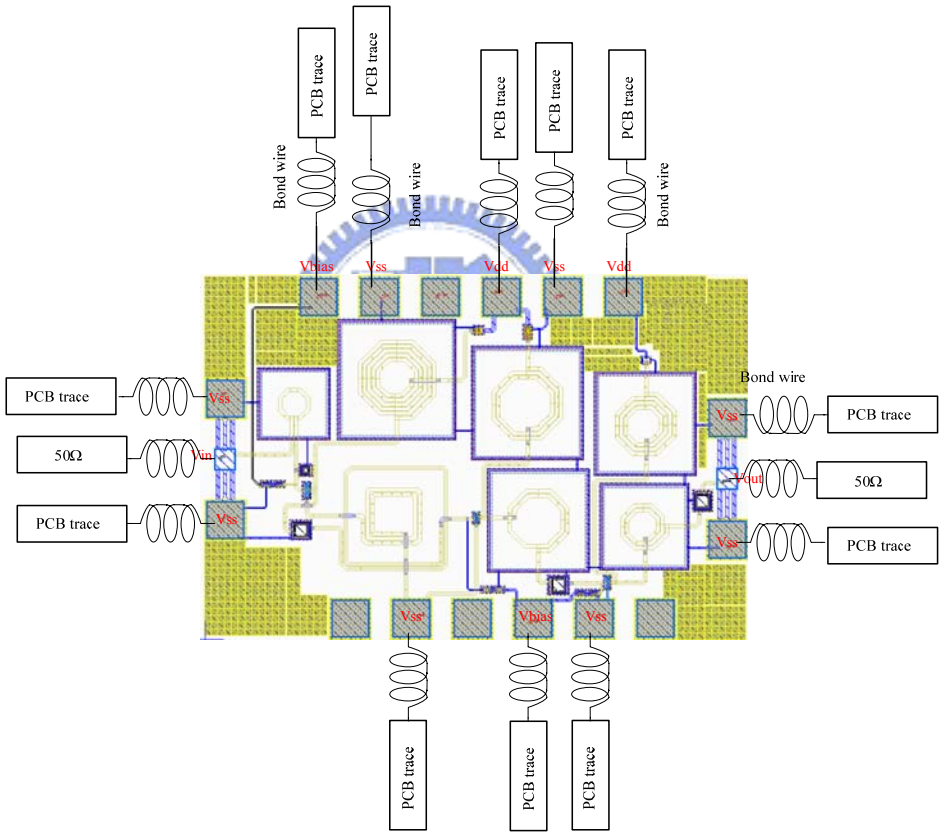


Fig. 3.4.11 approximately simplified circuit of UWB LNA

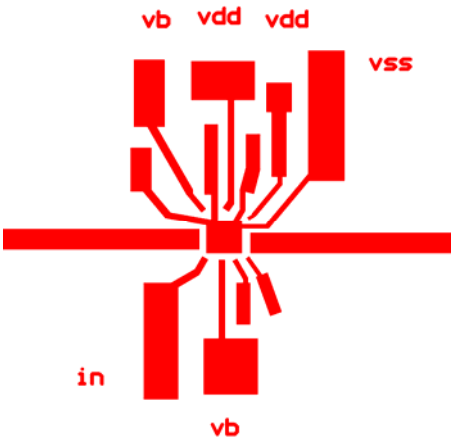


Fig 3.4.12 PCB layout

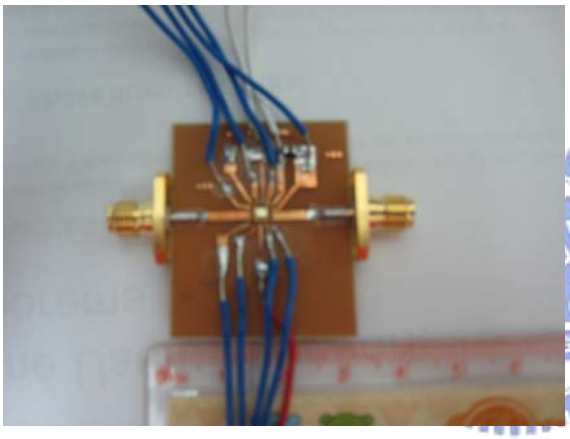


Fig. 3.4.13 (a) photo of PCB board

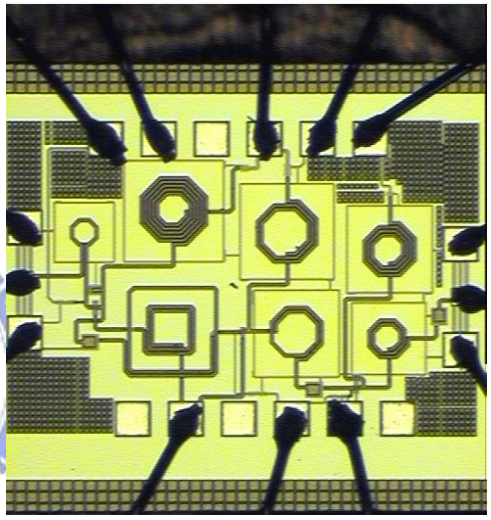


Fig. 3.4.13 (b) photo of bonded chip.

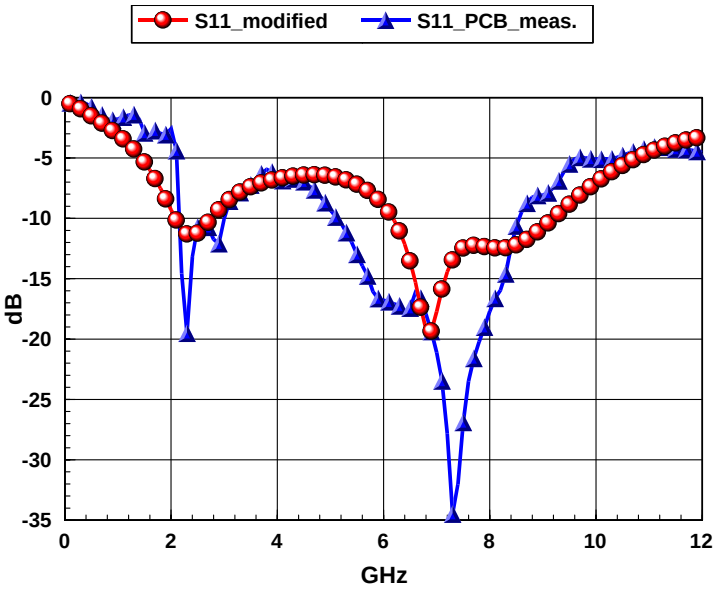


Fig. 3.4.14 (a) modified and PCB_meas. result of S_{11}.

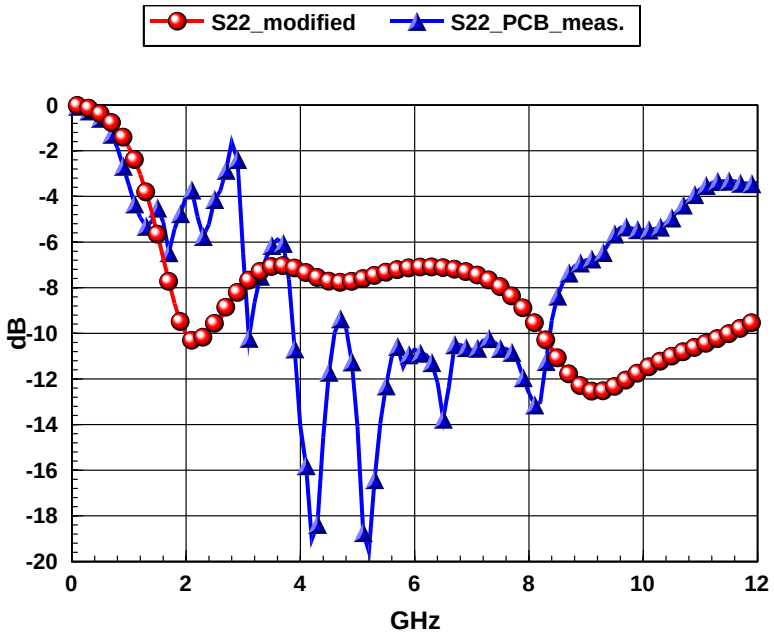


Fig. 3.4.14 (b) modified and PCB_meas. result of S_{22}.

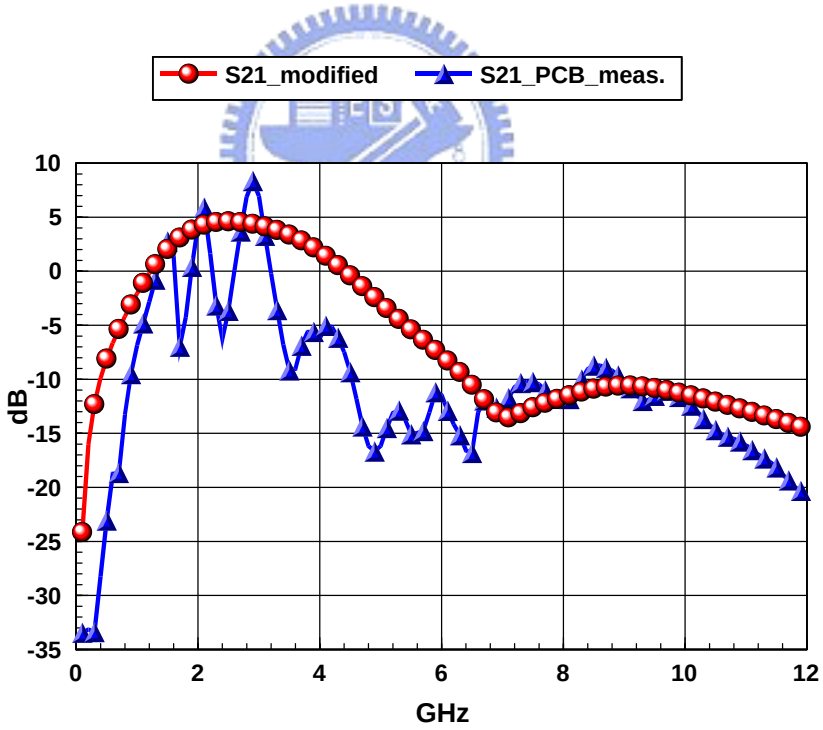


Fig. 3.4.14 (c) modified and PCB_meas. result of S_{21}.

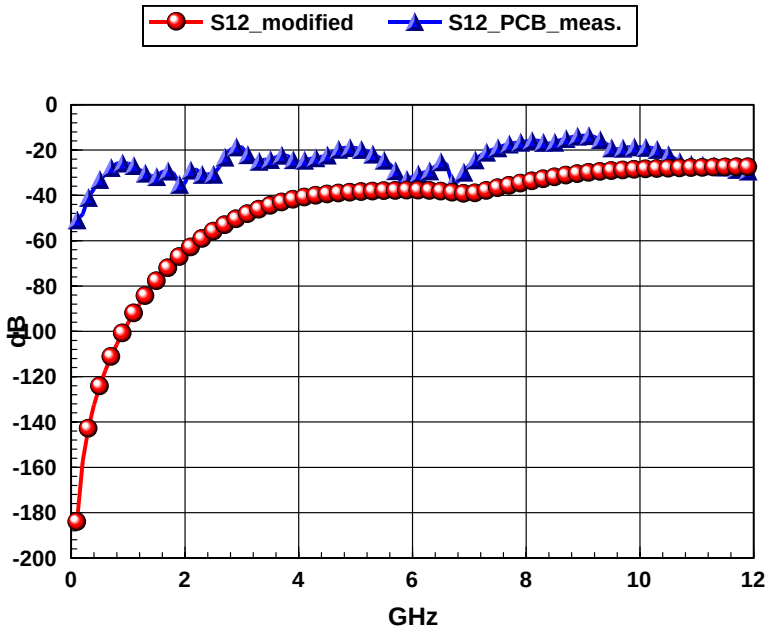


Fig. 3.4.14 (d) modified and PCB_meas. result of S_{12}.

The modified simulation and PCB board measurement results of S_{11} ,S_{22} and S_{12} have the same pattern although it still exist a little difference. This measurement result reveals that the "uncommon-ground" may be the critical problem of this circuit.

Chapter 4 Conclusions and future works

4.1 Conclusions

In Chapter 2, we design a low voltage low noise amplifier using transformer-feedback. The main advantage of this topology is the only one transistor used which is suited for low voltage application. In the Chapter 3, an UWB LNA using intrinsic capacitor matching is designed. The main advantage of this topology is that does not need a complex input matching network which induces more noise. The two designs suffer from the same problem in layout. The internal Vss ground Pad is like a “floating” Pad because they does not connect each other. It induces the unexpected influence under measurement. The problem of ground is more serious in these two circuits. In layout we often connect the guard-ring and Vss pad and then the Vss pad is connected each other by guard-rings. But in these two circuits the transformer is not added guard-ring and it is place at the input and output stage .Then in these stages the ground problem is more important than the other stage. It makes the measurement result different from the simulation result completely.

4.2 Future works

For higher frequency applications more accurate RF CMOS models should be built up for exactly matching network design for the future. All parasitic effects including parasitic capacitance, series resistance and inductance must be considered carefully. A more precise and efficient EDA tool and a accurate simulated environment setting is more important. The layout is important for RF integrated circuit. The inappropriate layout could influence the performance very much, especially for higher frequency.

Appendix:

A Current-reuse Low Noise Amplifier for Wireless LAN

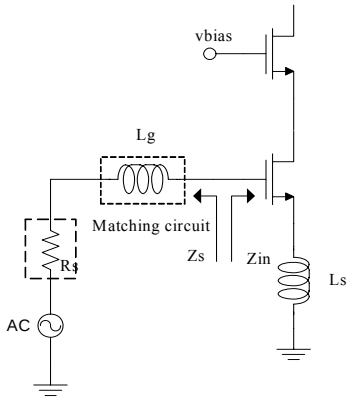
I. Introduction:

Duo to the fast growing demand for broadband wireless communications, the operating frequency is moving toward the 5GHz. Recently many RF circuits realized in the CMOS process have been reported in 0.18 μm process is a good candidate for highly integrated SOC applications. The requirements of low power and low cost push the trend toward a single radio chip. As operating frequencies increase, the field-effect transistor(FET) gate-drain overlap capacitance C_{gd} plays an more important role in performance since it's magnitude is comparable to the gate-source capacitance in deep-submicron CMOS technology. The demands for lower power consumption are gradually increased, especially for wireless personal area network. The current-reuse technique is widely used for low power operation. Two topologies of current-reuse low noise amplifier have been reported. One topology is made of inductively degenerated NMOS and PMOS pairs in shunt configuration to achieve current reuse [20],[21]. The other topology is made of two-stage common source amplifier to share the operating current and reduce current consumption [22],[23],[24]. In this design , a current-reuse topology of two-stage common source amplifier is adopted to share the operating current and using transistor's gate-drain capacitor to achieve input matching without gate inductor.

II. LNA Topology And Circuit Design

Fig. Ⅱ.1 shows a conventional cascode LNA with source degeneration inductor. If we neglect the effect of the drain-gate capacitor, its input impedance is $Z_{in} = sL_s + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}}$. This topology uses the inductor L_g to get noise and input conjugate match simultaneously [25].

In this design we have to consider the effect of the transistor's intrinsic capacitance. The small signal equivalent circuit of a source degeneration inductor is shown in Fig. Ⅱ.2[18].



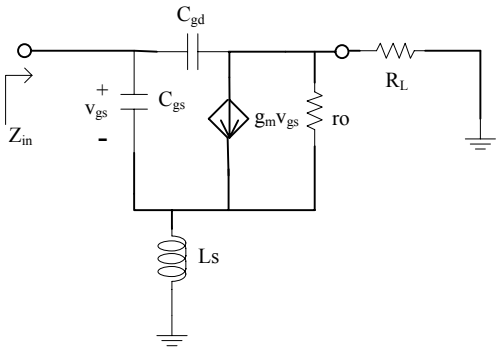


Fig. Ⅱ.1 Schematic of a cascode LNA topology. Fig. Ⅱ.2 Small-signal equivalent circuit of LNA.

The C_L presents the total capacitance of the transistor's drain node. To derive the input impedance we transform the dependent current source to voltage source as shown in Fig. Ⅱ.3.

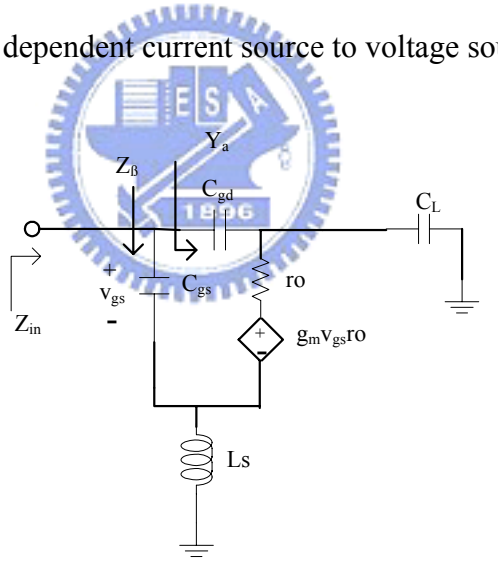


Fig. Ⅱ.3 The capacitive loading circuit used to analyze the input impedance

We derive the input impedance from two branches. Y_α is the admittance looking into the C_{gd} branch and Z_β is the impedance looking into the C_{gs} branch. We assume the induced current $g_m v_{gs}$ is much larger than the current flowing through either C_{gd} or C_{gs}. Thus the admittance looking into the C_{gd} branch is $Y_\alpha = j\omega C_{gd} + (R_\alpha + \frac{1}{j\omega C_\alpha} + j\omega L_\alpha)^{-1}$,

with $R_\alpha = \frac{C_L}{g_m C_{gd}}, C_\alpha = g_m r_o C_{gd}, L_\alpha = \frac{L_s C_L}{g_m r_o C_{gd}}(1+g_m r_o)$.

The impedance looking into the C_{gs} branch is $Z_\beta = \frac{1}{j\omega C_{gs}} + (\frac{1}{R_\beta} + j\omega C_\beta + \frac{1}{j\omega L_\beta})^{-1}$

with $R_\beta = \frac{g_m L_s}{C_{gs}}, C_\beta = \frac{C_{gs}}{g_m r_o}, L_\beta = \frac{L_s g_m r_o C_L}{C_{gs}}$. The input impedance of the capacitive loading circuit is $Z_{in} = \left(Y_\alpha + \frac{1}{Z_\beta}\right)^{-1}$. The capacitive-loading circuit can be approximated as shown in Fig. Ⅱ.4.

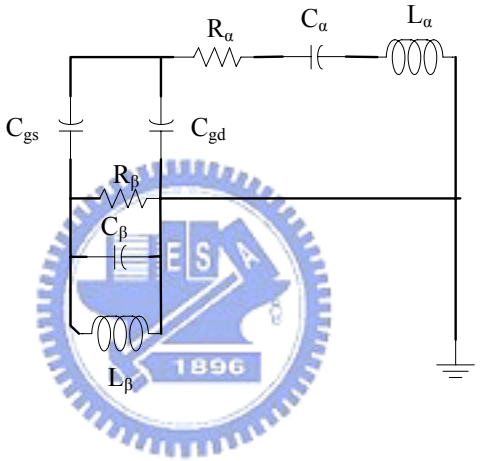


Fig. Ⅱ.4 Capacitive loading equivalent circuit

The critical components are those on $R_\alpha C_\alpha L_\alpha$. The $R_\alpha C_\alpha L_\alpha$ component form a series resonance circuit and it's resonance frequency is

$f_0 = \frac{1}{2\pi\sqrt{L_\alpha C_\alpha}} = \frac{1}{2\pi\sqrt{L_s C_L (1+g_m r_o)}}$. According to above input impedance analysis we can design a low noise amplifier without the gate inductor to achieve the input match. The LNA topology of this design is shown in Fig. Ⅱ.5. The current reuse is achieved by L_i, C_i ,C_s and C. In this topology we can find the approximately capacitive load of the first MOS M1 drain node is composed of the C and C_{gs2}. We can design the value of the size of M2 properly to get input match. In order to lower the noise of the circuit, we choose the channel length of mos $W_{opt} \approx \frac{1}{3\omega C_{ox} R_s L}$ [2], and we design the source inductor Ls to make sure that the circuit is

stable after the inductive-feedback.

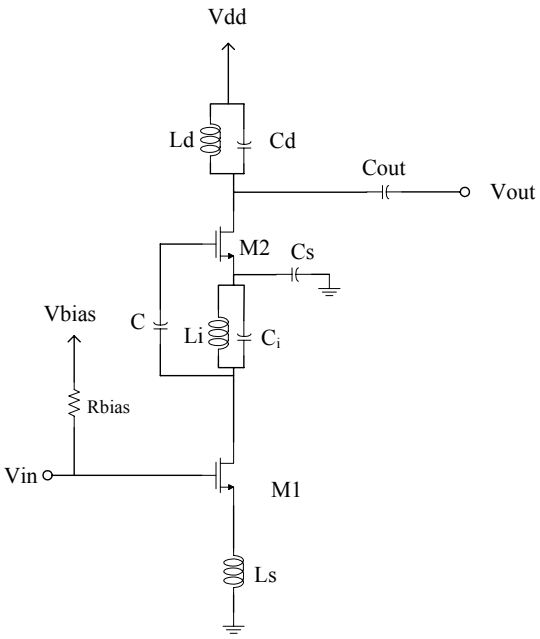


Fig. Ⅱ.5 The topology proposed by this design

The capacitor C represent the coupling capacitor and it have to large enough to couple the signal and the shunt Li and Ci have to resonate at the operating frequency like an RF choke. The bypass capacitor Cs provides AC ground and it's value has to be large enough. The output matching is achieved by the L_d, C_d and C_{out}.

III. Simulation results and conclusion

In this design we use the ADS to simulate circuit and ADS momentum to simulate the wire connected each device. The simulation result shows that the input and output return loss S11 is 18.75dB and S22 is 26dB at 5.8Ghz.The noise figure is 2.0dB. The power gain S21 is 15dB, as shown in Fig.Ⅲ.1,2. P1dB of this design is -13.5dBm, as shown in Fig.Ⅲ.3. IIP3 is , as shown in Fig.Ⅲ.4. Total consumed power is 8.24mA* 1.5V=12.36mW. The chip area is 0.684x0.614mm^2 and the layout is shown in Fig.Ⅲ.5. In this design we use the transistor's intrinsic capacitor to achieve input match and do not need the gate inductor to improve the noise figure. The TableⅢ-1 shows performance summary and comparison. This design has been submit to APMC 2007.

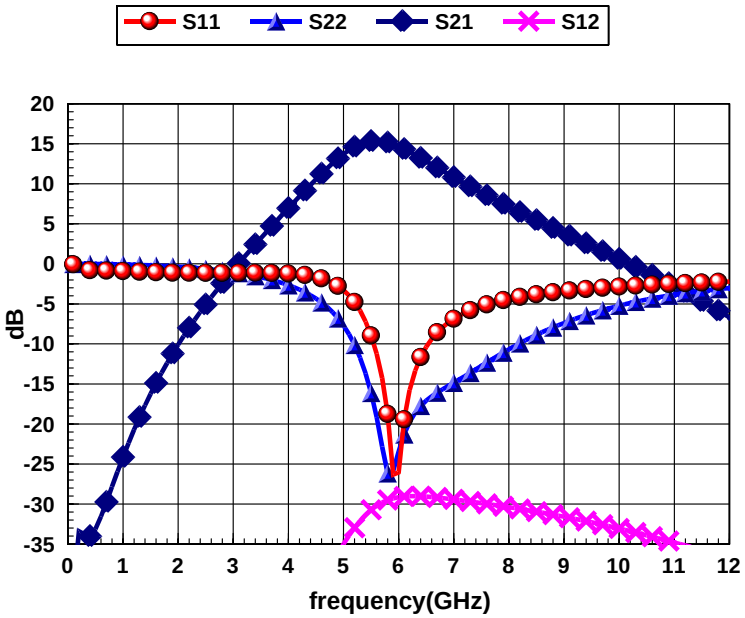


Fig. Ⅲ.1 Simulation result of S-parameter

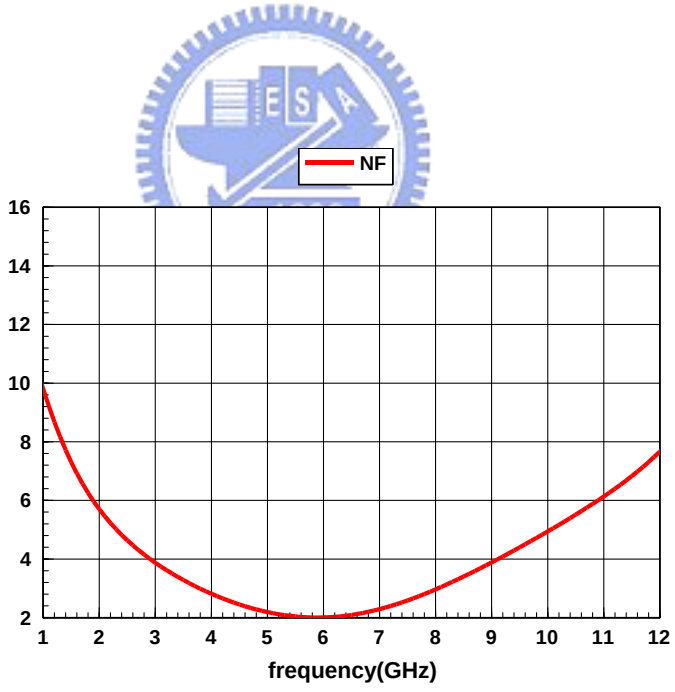


Fig. Ⅲ.2 Simulation result of NF

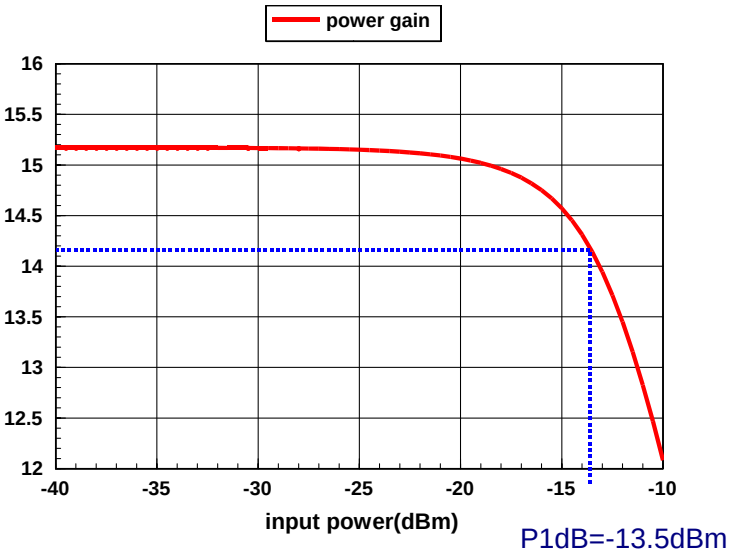


Fig. Ⅲ.3. simulation result of P1dB

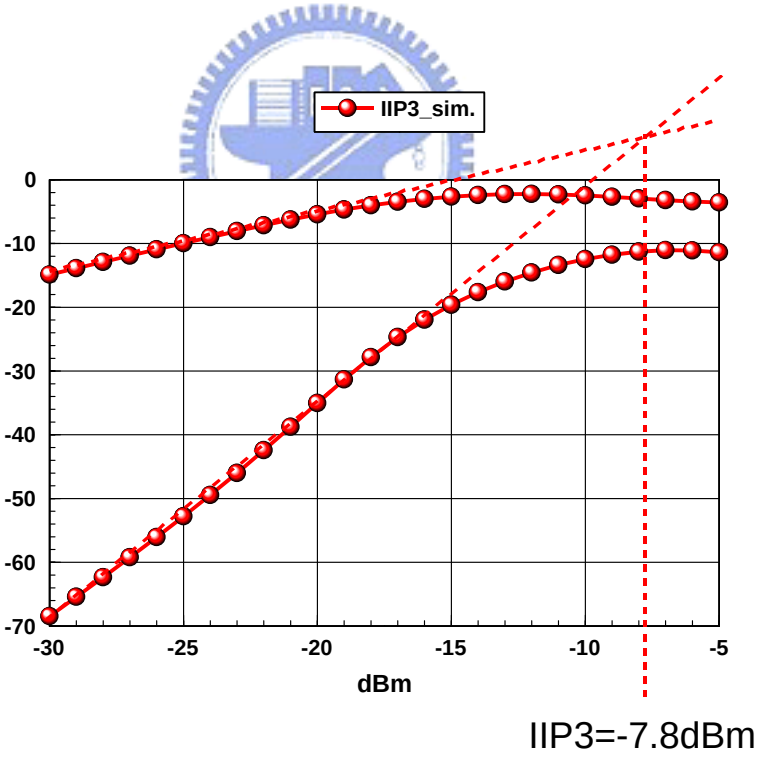


Fig. Ⅲ.4 simulation result of IIP3.

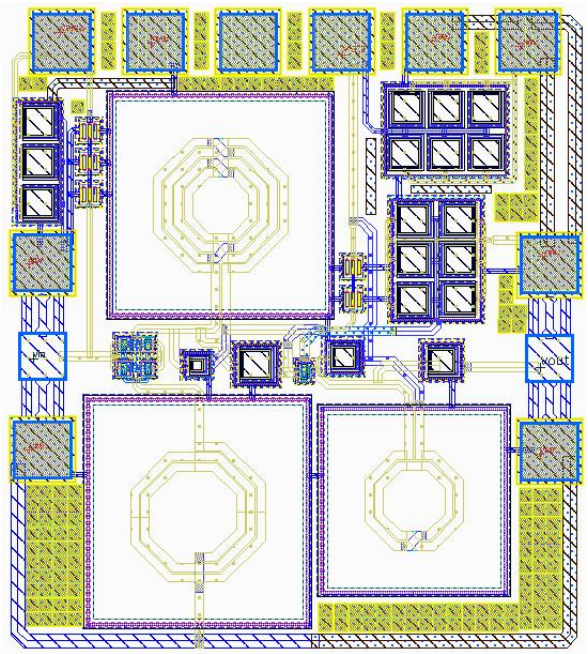


Fig.Ⅲ.5 layout of LNA.

Table Ⅲ-1 performance summary and comparison.

	comparison		
	This work	***[26]***	***[24]***
Technology	0.18umCMOS	0.18umCMOS	0.18umCMOS
Frequency (GHZ)	5.8	5.25	5.7
S11(dB)	-18.76	-14.7	-15
S22(dB)	-26.167	-	-9
Powe gain(dB)	15.136	16	12.5
NF	2.00	1.8	3.7
P1dB(dBm)	-13.5	-	-13.5
Vdd(V)	1.5	1.8	1.8
Power consumption	12.36mW	7.8mW	14.6mW

Reference

[1] Tajinder Manku, Galen Beck, and Etty J. Shin, “A Low-Voltage Design Technique for RF Integrated Circuits.” IEEE Transactions on Circuits and Systems-Ⅱ: Analog and digital Signal Processing, Vol.45, NO. 10, October 1998

[2] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambrige, U.K.:Cambrige Univ. Press, 1998.

[3] David J. Cassan, and John R. Long, “A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18um CMOS,” IEEE Journal of Solid-State Circuits, VOL. 38, No. 3, March 2003.

[4] John R. Long, “Monolithic Transformers for Silicon RF IC Design,” IEEE Journal of Solid-State Circuits, Vol. 35, No. 9, September 2000.

[5] A. Rofougaran, J. Y.-C. Chang,M. Rofougaran, and A .A. Abidi, ”A 1GHz CMOS RF front-end IC for a direct-conversion wireless receiver.” IEEE J. Solid-State Circuits, vol. 31, no.7, pp.800-889, Jul. 1996.

[6] D. K. Shaeffer and T. H. Lee, “A 1.5-V,1.5-GHz CMOS low noise amplifier,” IEEE J. Solid-State Circuits, vol. 32, no.5, pp. 745-759, May 1997.

[7] S. Andersson, C. Svensson, and O. Drugge, “Wide-band LNA for a multistandard wireless Receiver in 0.18um CMOS,” in Proc. EDDCIRC, Sep. 2003, pp. 655-658.

[8] R. S. Lee, D. D. Wentaloff, and A. P. Chandarakasan, “An ultra-wide-band baseband front-end,” in Proc. IEEE RFIC Symp. Jun. 2004, pp.493-496.

[9] C-W. Kim, M.-S. Kang, P. T. Anh, H.-T. Kim, and S.-G. Lee, “An ultra-wide-band CMOS low noise amplifier for 3-5 GHz UWB system,” IEEE J. Solid-State Circuits, vol. 40, no. 2, pp. 544-547, Feb. 2005.

[10] Brian M. Ballweber, Ravi Gupta, and David J. Allstot, ”A fully integrated 05-5.5-GHz

CMOS Distributed Amplifier ," IEEE Transactions on Solid-State Circuits, Vol. 35, No.2, February 2000.

[11] Andrea Bevilacqua, and Ali M. Niknejad, "An Ultrawideband CMOS low-noise amplifier for 3.1-10.6GHz Wireless Receivers," IEEE Journal of Solid-State Circuits, Vol. 39, No. 12, December 2004.

[12] Chang-Wan Kim, Min-Suk Kang, Phan Tuan Anh, Hoon-Tae Kim, and Sang-Gug Lee,"An Ultra-wideband CMOS low noise amplifier for 3-5-GHz UWB System," IEEE Journal of Solid-State Circuit, vol.40, No.2, February 2005.

[13] Aly Ismail and Ascad A. Aibdi, "A 3-10-GHz low noise amplifier with wideband LC-ladder matching network," Solid-State Circuits, IEEE Journal, Vol. 39, Issue 12, Dec.2004,pp2269-2277.

[14] Trung-Kien Nguyen, Chung-Hwan Kim, Gook-Ju Ihm, Moon-Su Yang, and Sang-Gug Lee, "CMOS Low-Noise Amplifier Design Optimization Techniques," IEEE Transactions on Microwave Theory and Techniques, Vol. 52, No. 5, MAY 2004.

[15] Yang Lu, Kiat Seng Yeo, Alper Cabuk, Jianguo Ma, Manh Anh Do, and Zhenghao Lu, "A Novel CMOS low-noise amplifier design for 3.1 to 10.6-GHz Ultra-wide-band Wireless Receivers," IEEE Transactions on Circuits and Systems-I: Regular papers, Vol.53, No.8 August 2006.

[16] Michael T. Reiha, and John R. Long, "A 1.2V reactive-feedback 3.1-10.6GHz Low-noise amplifier in 0.13um CMOS," IEEE Journal of Solid-State Circuits, Vol. 42, No. 5, MAY 2007.

[17] C.-T. Fu and C.-N. Kuo, "3-11-GHz CMOS UWB LNA using dual feedback for broadband matching," in Proc. IEEE RFIC Symp.,San Francisco, CA, Jun. 2007,pp. 67-70.

[18] Robert Hu, "Wide-Band Matched LNA Design using transistor's intrinsic Gate-Drain Capacitor," IEEE Transactions On Microwave Theory and Techniques, Vol. 54, No. 3.

MARCH 2006.

[19] Sudip Shekhar, Jeffrey S. Walling, and David J. Allstot,"Bandwidth Extension Techniques for CMOS Amplifiers," IEEE Journal of Solid-State Circuits, Vol. 41, No. 11, November 2006.

[20] H. Fouad, K. Sharaf, E. El-Diwany, and H. El-Hennawy,"An RF CMOS cascode LNA with current reuse and inductance source degeneration," *in Radio Science Nineteenth National Conference of the Proceedings NRSC 2002*, 2002, pp.450-457.

[21] F. Gatta, E. Sacchi, F. Svelto, P. Vilmercati, and R. Castello, "A 2-dB noise figure 900-MHz differential CMOS LNA," Solid-State Circuits, IEEE Journal, vol. 36, no. 10, Oct. 2001.

[22] C.-Y. Cha and S.-G. Lee, "A low power, high gain LNA topology," in Int. Microwave and Millimeter Wave Technology Conf., 2000, pp.420-423.

[23] K. Yamamoto, T. Heima, A. Furukawa, M. Ono, Y. Hashizume, H. Komurasaki, H. Sato, and N. Kato, "CMOS low-noise/driver MMIC amplifier for 2.4-GHz and 5.2-GHz wireless application," Silicon Monolithic Integrated Circuits in RF Systems, pp. 18-22, 2001.

[24] Che-Hong Liao, and Huey-Ru Chuang, "A 5.7-GHz 0,18-μm CMOS Gain-Controlled Differentail LNA With Current Reuse for WLAN Receiver," IEEE Microwave and Wireless Components Letters, vol. 13, no. 12, December 2003.

[25] Trung-Kien et al., "CMOS Low-Noise Amplifier Design Optimization Techniques," IEEE Transactions on Microwave Theory and Techniques, vol. 52 no.5 May 2004.

[26] Fatemeh Kalantari, Naser Masoumi, and roghaye Saeidi, "A 5.25GHz Low noise amplifier for WMAN Applications in 0.18 μm CMOS Technology," 2005 IEEE. Microelectronics, 2005. ICM 2005. The 17th International Conference on 13-15. Dec. 2005 Page(s):122-127

[27] Yanjie Wang, M.Zamin Khan and Kris Iniewski, "A 0.65V, 1.9mW CMOS Low-noise

Amplifier at 5GHz," proceeding of the 9th International Database Engineering and Application Symposium(IDEAS'05) 2005.

[28] M.N. El-Gamal, K.H Lee and T.K. Tsang, "Very low-voltage(0.8V)CMOS receiver front end for 5GHz RF application," IEEE proc. Circuits Decices Systm. vol.149. no.516, Oct./Dec. 2002.

[29] Jihak Jung, Kyungho Chung, Taeyeoul Yun, Jaehoon Choi, and Hoontae Kim, "Ultra-wideband low noise amplifier using a cascade feedback topology," Silicon Monolithic integrated Circuits in RF Systems,2006. Digest of Papers. 2006 Topical Meeting on 18-20 Jan. 2006.

[30] Quail El-Gharniti, Eric Kerherve, and Jean-Baptiste Begueret, "Modeling and Characterization of On-Chip Transformers for Silicon RFIC," IEEE Transactions on Microwave Theory and Techniques, vol. 55,no. 4, April 2007.

Vita and Publication

姓名：方瑞嫻

學歷：

國立台南女子高級中學(86 年 9 月~89 年 6 月)

國立中山大學電機工程學系(90 年 9 月~93 年 6 月)

國立交通大學電信工程所碩士班(94 年 9 月~96 年 6 月)

Publication Remarks：

International conference papers:

1. H. I. Wu, Jui Hsien Fan and Christina F. Jou, "A 0.7V Transformer-feedback CMOS Low-noise Amplifier for 5-GHz Wireless LAN", Progress In Electromagnetics Research Symposium (PIERS 2007), March 26-30, 2007, Beijing, China.